Metal-Oxide Based Transparent Conductive Oxides And Thin Film Transistors For Flexible Electronics

by

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ABSTRACT

The object of this study is to investigate and improve the performance/stability of the flexible thin film transistors (TFTs) and to study the properties of metal oxide transparent conductive oxides for wide range of flexible electronic applications.

Initially, a study has been done to improve the conductivity of ITO (indium tin oxide) films on PEN (p olyethylene naphthalate) by inserting a thin layer of silver layer between two ITO layers. The multilayer with an optimum Ag mid-layer thickness, of 8 nm, exhibited excellent photopic average transmittance (~ 88 %), resistivity (~ 2.7×10^{-5} μ-cm.) and has the best Hackee figure of merit (41.0×10^{-3} Ω^{-1}). The electrical conduction is dominated by two different scattering mechanisms depending on the thickness of the Ag mid-layer. Optical transmission is explained by scattering losses and absorption of light due to inter-band electronic transitions.

A systematic study was carried out to improve the performance/stability of the TFTs on PEN. The performance and stability of a-Si:H and a-IZO (amorphous indium zinc oxide) TFTs were improved by performing a systematic low temperature (150 °C) anneals for extended times. For 96 hours annealed a-Si:H TFTs, the sub-threshold slope and off-current were reduced by a factor ~ 3 and by 2 orders of magnitude, respectively when compared to unannealed a-Si:H TFTs. For a-IZO TFTs, 48 hours of annealing is found to be the optimum time for the

best performance and elevated temperature stability. These devices exhibit saturation mobility varying between 4.5-5.5 $cm^2/V\text{-}s$, I_{ON}/I_{OFF} ratio was 10^6 and a sub-threshold swing variation of 1-1.25 V/decade. An in-depth study on the mechanical and electromechanical stress response on the electrical properties of the a-IZO TFTs has also been investigated. Finally, the a-Si:H TFTs were exposed to gamma radiation to examine their radiation resistance. The interface trap density (N_{it}) values range from 5 to 6×10^{11} cm^{-2} for only electrical stress bias case. For "irradiation only" case, the N_{it} value increases from 5×10^{11} cm^{-2} to 2×10^{12} cm^{-2} after 3 hours of gamma radiation exposure, whereas it increases from 5×10^{11} cm^{-2} to 4×10^{12} cm^{-2} for "combined gamma and electrical stress".

DEDICATION

Dedicated to my family Venkata Indluru, Usha Indluru, Sunil Indluru, and
Sravanthi Penumarthy for their
eternal love and companionship

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Chapter 1

INTRODUCTION

1. 1. TRANSPARENT CONDUCTING OXIDES

Transparent conductive oxide films (TCO) that are both transparent in the visible region and electrically conducting have been studied widely for over 20 years as a result of their extensive applications in optoelectronic devices [1]. These include energy-efficient windows, burglar alarms, and window heaters, as well as electrodes for solar cells and especially for flat panel displays such as liquid crystal displays (LCDs), plasma display panels (PDPs), field emission displays (FEDs), organic electroluminescent (OEL) devices *etc*. Fabrication of films with as low as possible resistivity while retaining high transparency in the visible region is the aim of many works done on TCO films. Many new materials and manufacturing techniques have been developed to satisfy stringent technological requirements. The required quality of the films increases with increasing sophistication of the applications. These materials find applications in wide areas such as liquid crystal displays, transparent electrodes of solar cells, and photo-detectors. The simultaneous occurrence of high optical transparency (~90%) in the visible region together with electronic conductivity require the creation of electron degeneracy in wide-gap oxides (>3 eV) by suitably introducing nonstoichiometry and/or appropriate dopants. Many works about the

preparation, characteristic, electrical and optical properties of TCO films have been reported and a large amount of experimental data have been given; but up until now, films with a resistivity of less than 1.0×10^{-4} Ω-cm have only been reported by a few authors [2, 3].

The characteristics of the TCO films are dependent on the process conditions and deposition system. In the case of ITO deposition with magnetron sputtering, argon (Ar) and reactive oxygen (O_2) gas flow rates [4], substrate temperature [5] and deposition rate [6] are crucial process parameters. Among them, substrate temperature (> 200 °C) during the deposition or post-deposition annealing process is one of the most important parameters to optimize to produce high quality ITO films [7]. High temperature (> 200 °C) is not an effective process condition when ITO films are deposited on a polymer substrate to be applied in flexible optoelectronic devices. One way to improve the properties of ITO films destined for flexible optoelectronics applications is to use ITO/metal/ITO (IMI) sandwich structure films, which have a lower resistivity than single-layer ITO films of the same thickness. In recent years, several advantageous IMI structures with better electrical and optical properties for LCDs have been reported [8]. Hence, it is very important to explore the IMI sandwich structures. We have investigated flexible ITO-Ag-ITO multilayer system and have obtained excellent optical and electrical properties.

1. 2. AMORPHOUS SILICON THIN FILM TRANSISTORS

Thin film transistors (TFTs) are a unique type of field effect devices in which the applied voltage at one electrode (*i.e.,* the gate) controls the electric field modulating the conductivity of an underlying semiconductor layer, *i.e.* channel layer. The modulation provides an electrical path for the carriers to travel about the other two electrodes (*i.e.,* the source and drain). Figure 1.1 shows a cross-sectional schematic of the hydrogenated amorphous silicon (a-Si) TFT.

Hydrogenated amorphous silicon (a-Si:H) first came to prominence as a potentially useful electronic material through the work of Spear and coworkers in the 1970s [9]. Since then, there has been significant research and development worldwide to bring a-Si:H to the current state in which it is routinely used in TFTs with a large switching raito ($< 10^6$) and a low off current between the source and drain is suitable for controlling active-matrix liquid crystal displays (AMLCDs). [10] Although many properties of a-Si:H are similar to crystalline silicon, the amorphous nature of the material has an effect upon the electron energy band structure and the carrier transport properties. In order to understand the progress made in the field of TFTs, it is essential to first introduce the physics involved in it.

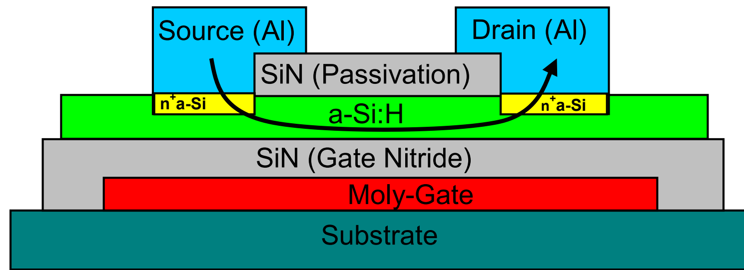


Figure 1.1 Cross-sectional schematic of hydrogenated amorphous silicon TFTs test structure.

1. 2. 1. Electron energy band diagram

The amorphous structure of a-Si:H introduces a degree of disorder into the system so that there is a range of bond lengths and bond angles, unlike crystalline silicon. Because of this there is a perturbation in the energy of the bonding and anti-bonding states in a particular bond, resulting in the formation of localized “band tail” electron states which extend into band gap, decreasing exponentially as shown in Figure 1.2. Hence, the band tails are associated with the weak bonds and its width gives a measure of disorder. The width of the tails is known as the Urbach energy. [11]

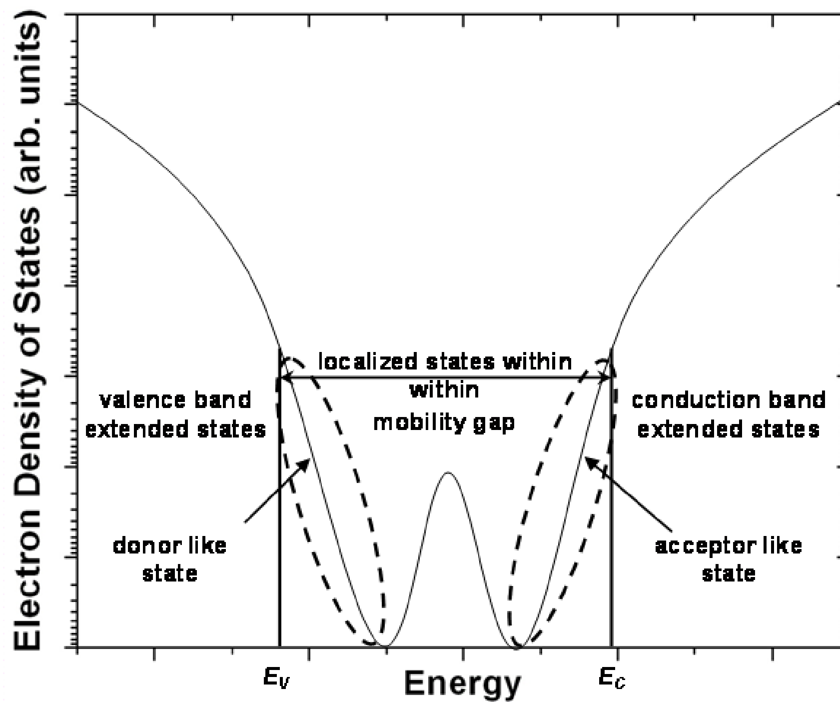


Figure 1.2 Schematic diagram of the electron density of states for an amorphous semiconductor, such as a-Si:H [adapted from reference 14].

In a-Si there are a large number of dangling bonds, typically ~ 10^{20} cm^{-3}. However, intordutcion of hydrogen reduces the defect density to as low as 10^{16} cm^{-3}. The hydrogen passivates the defects by forming a Si-H bond where the dangling bond would have been. [12] In addition it helps in lowering the local stress in the network thereby reducing the number of weaker bonds. [13] The deposition temperature provides the primary means of controlling the hydrogen content of a-Si:H. In general, the higher the substrate temperature during deposition, lowers the hydrogen content of a-Si:H.

1. 2. 2. Conduction mechanism

The amorphous structure of the a-Si:H network produces three types of electron states. Dangling bond defects produce states deep inside the band gap; weak bonds produce band tail states at the edges of the band gap, and the tetrahedral network produces the extended conduction and valence band states. The conduction mechanism is different for each of these states and is dictated by the Fermi level position and temperature. At low temperatures, an electron occupying a localized dangling bond defect state just below the Fermi level may be in close proximity with an unoccupied localized defect state just above the Fermi level. Upon the application of an electric field and with almost no expenditure of thermal energy, the electron may tunnel from the first state to the second, as shown in Figure 1.3. As the temperature increases, there is sufficient thermal energy for some electrons to be excited into the

conduction band tail. Electrons in a band tail state are localized near a weak bond. Under the application of an electric field, the electrons may tunnel from one localized state to another. This process is called band tail hopping. At temperatures above ~ 500 K, there is sufficient thermal energy in the a-Si:H system for electrons and holes to be excited beyond the band tails and into the conduction and valence bands. In these states, the carriers are not constrained by local defects or weak bonds but are in extended state and are free to move through the periodic potential of the tetrahedral silicon structure.

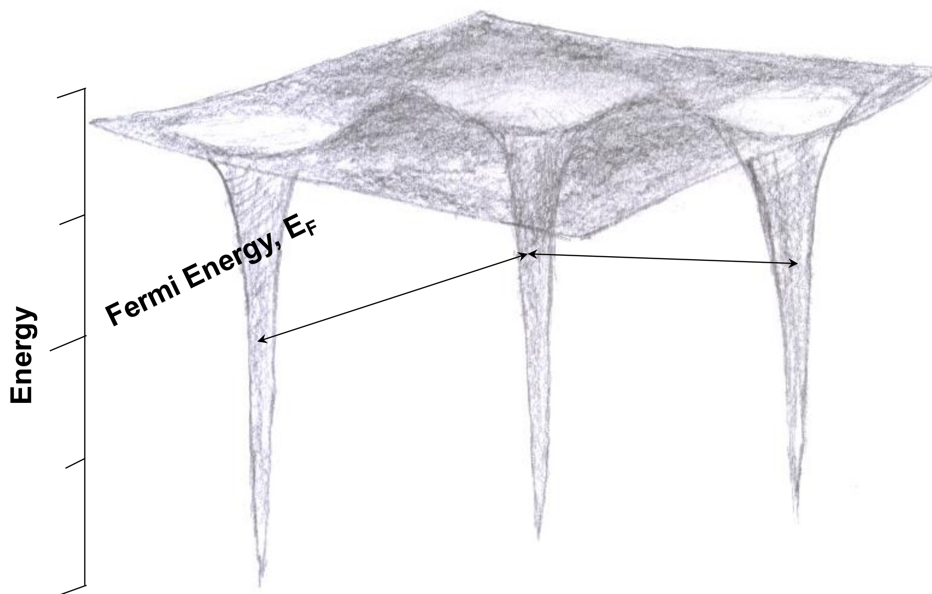


Figure 1.3 At low temperatures, and electron sees a series of potential wells associated with defect states in the mobility gaps. Under the application of an electric field, the electron may tunnel between such states while remaining at the Fermi energy. [adapted from reference 14]

1. 2. 3. Electrical instability

Unlike crystalline silicon transistors, amorphous silicon TFTs exhibit a bias induced metastability phenomena that cause degradation in both threshold voltage and the sub-threshold swing over operation time. The stability analysis is very important in predicting the long-term performance of TFT.

Two mechanisms have been proposed to explain the electrical instability in these TFTs. [15-16] The first mechanism is trapping of carriers in the gate insulator which mostly occurs in TFTs with unstable insulator. This unstable insulator usually has high density of defects that can trap charge when the TFT gate undergoes a bias stress. Electrons are first trapped within the localized interfacial states at the a-Si:H/insulator boundary, and then, thermalize to deeper energy states inside the insulator either by variable-range hopping [15] or through a multiple-trapping and emission process. [17-19] The second mechanism defect creation in the a-Si:H layer or at the a-Si:H/insulator that increases the density of deep-gap states. [20] The application of positive gate bias causes electrons to accumulate at the channel/insulator, most of these electrons reside in conduction band tail states. These tails states have been identified as weak silicon-silicon bonds which, when occupied by electrons, break to from silicon dangling bonds. [21-22] Both charge trapping and state creation mechanisms manifest themselves as a shift in the TFT threshold voltage. The charge trapping dominates at high bias

voltages and long stress times whereas; defect creation dominates at lower stress voltages and at smaller stress times. Hence, the electrical performance of the a-Si:H TFT is mostly decided by the quality of the a-Si:H film and the a-Si:H/SiN_x interface. It has been a great challenge to fabricate low leakage insulator along with good quality a-Si:H layer using low temperature-fabrication-technology for flexible electronics applications. A considerable amount of charge can be trapped inside the insulator at such low fabrication temperatures (< 150 ^oC). The trapped charge inside the insulator along with ease of state creations in the a-Si:H layer leads to threshold voltage shift (ΔV_t) after prolonged bias-stress. Along with ΔV_t hysteresis phenomenon caused due to trapped charges inside insulator is also a poor characteristic of a-Si:H TFT. This can be a major drawback to use low temperature fabricated TFTs as the pixel element of active matrix organic light emitting diode (AMOLED). Hence, techniques are needed to either inhibit or reverse this ΔV_t along with reduction of the trapped charges inside the insulator by some predictive pre- or post- fabrication treatment. Up to this date, the performance of TFTs has been improved by changing the process parameters during their fabrication [23]. Anneal studies have shown some improvements in the performances of the TFT's by elevated thermal processing (> 300 ^oC) [24]. However, high anneal temperatures become a constraint when the TFTs are grown on polymer-based flexible substrates, as they are sensitive to high temperatures. We have improved the performance and high

temperature stability of these TFTs by annealing them at 150 °C for long durations.

1. 2. 3 Limitations of a-Si:H compared to amorphous oxide TFTs

Amorphous Si:H TFTs have several undesirable electrical characteristics such as low mobility and electrical instability with operation time. This instability of the devices limits their functions in some demanding applications and is more severe for low temperature processes required for flexible backplanes. Metal oxide semiconductors such as ZnO, IZO, $(InGaZn)O_4$ *etc.* have been identified as a promising candidate for TFTs compared to a-Si:H TFTs because of their high mobility and better stability. [25] In these metal oxide semiconductors, the conduction band minima is dominated by the metal *s*-states, which are insensitive to the angular distortion and hence retain a high mobility. [26] These oxide TFTs have an added advantage over a-Si:H due to low temperature deposition and improved stability under bias stress. [27] Low temperature fabrication of these TFTs makes it easier to work with large area plastic substrates and significantly reduce the cost of producing large area electronics backplanes.

1. 3. METAL OXIDE BASED THIN FILM TRANSISTORS

In the past, amorphous or polycrystalline Si:H layer have been commonly used as channel layers for most conventional TFTs in flat panel displays. However, these TFTs have a lot of disadvantages such as low mobility (<1 cm^2/Vs), and sensitive to light [28]. As a result of which they have poor efficiency of light transmittance and brightness. To obtain a TFT with high mobility requires relatively high process temperature (> 300 °C), which makes it difficult to fabricate them on flexible polymer substrates [28].

With this in mind most of the research is moving from silicon based TFTs to transparent amorphous metal-oxide semiconductors as channel layer and source/drain electrodes [29]. These TFTs attract much attention due to their advantages such as high mobility, and high transmittance [30-33]. A number of metal-oxide based TFTs such as zinc oxide (ZnO), zinc tin oxide (ZIO), indium gallium oxide (IGO), and indium gallium zinc tin oxide (IGZSO) have demonstrated high mobility's even at room temperature fabrication [33-34]. Many TFTs were reported using crystalline ZnO [35-36], or polycrystalline SnO_2 [37], and In_2O_3 [38]. However to realize the transparent TFTs for flexible electronics, amorphous films are more suitable than crystalline type, because amorphous type oxide films have extra advantages such as low temperature deposition, good film smoothness, low compressive stress, large area deposition by sputtering, and uniformity of device

characteristics [39-41]. The fabrication of low-temperature TFTs allows flexible large area electronic devices such as electronic paper (Figure 1.4), and flexible display (Figure 1.5); which are lightweight, flexible, and shock resistant. However low temperature fabrication amorphous metal-oxide TFTs produces a number of defects in the channel layer, insulator and also at the interface. The presence of these TFTs can be a latent problem (*e.g.,* poor performance and thermal instability). Hence, it becomes very important to improve the performance/stability of these TFTs. In addition, it would be very useful to understand the role of these defects on the performance and stability of these metal-oxide TFTs. We have improved the performance of these TFTs by low temperature long anneals. This technique was further used as a tool to understand the role of these defects on their performance.

Once their performance has been improved, it is becomes important to investigate their mechanical stability for large area flexible electronics applications. Large area electronics devices need to be rollable and able to withstand mechanical strain in bent condition. The potential applications include X- ray detectors, neutron detectors, smart medical bandages, *etc*. For these applications organic polymers like poly-ethylene napthalate (PEN) is used as deformable substrates. Thus, it becomes important to study the mechanical stability of these devices. We have investigated the effects of mechanical and combined electro-mechanical

stability of these TFTs by static bend on various radii and stress times. None of the TFTs catastrophically failed for over 2 days of mechanical stress. Finally, TFT's radiation resistance was tested by irradiating the TFTs by gamma radiation because of their growing importance for space applications. NASA already uses devices in solar sails and synthetic aperture radar systems that depend on TFT-based flexible circuits to monitor their electronic health and reliability in the harsh, uncompromising space environment [42]. These lightweight, rugged, flexible displays may be beneficial in manned space applications. We have investigated the electrical reliability and lifetime of TFTs fabricated on flexible substrates in high gamma radiation environment.

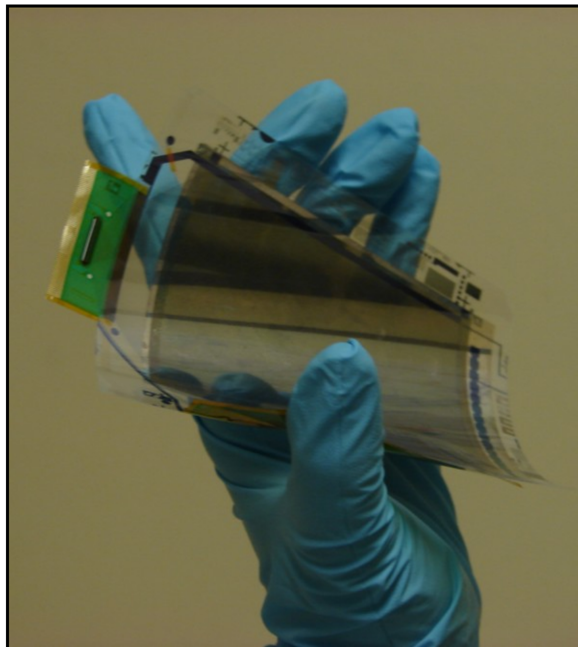


Figure 1.4 Applications of flexible electronics as an electronic paper

Figure 1.5 Example of flexible electronics in flexible display

1.4. FLEXIBLE SUBSTRATES

Flexible substrates offer advantages over their rigid counterparts in terms of weight and toughness in both commercial and military applications. Flexible electronics could have a wide range of applications including foldable electronic, sensors, displays, medical device, solar cells, deployable spacecraft structures, and even smart clothing. Fabrication of these devices is a challenge due to the limited temperature tolerance of flexible polymers. The most common approach focuses on modified, low temperature versions of conventional deposition processes, which result in amorphous and/or polycrystalline Si on polymeric substrates. Due to the limited process-temperature tolerance of the polymers, the carrier mobility of the deposited layers is very low and often unacceptable for high-speed electronics. Furthermore, polymer substrates have drawbacks such as high thermal expansion and low thermal resistance that are critical to heat processing during device fabrication. Conventionally, polyethylene terephthalate (PET) and polycarbonate (PC) have been widely researched as substrate materials for flexible displays. Including PET, several polymer layers such as polyethylene napthalate (PEN) and poly-ethersulfone (PES) are being considered for flexible substrates. These PEN films exhibit better thermal and dimensional properties than PET and thier optical properties are on par or better than PES and PC. Table I shows a summary of the processing temperatures and properties of various flexible substrates.

Table 1.1 Processing temperatures and properties of flexible substrates

Maximum process temperature	Materials	Characteristics
900 °C	Steel	Opaque, moderate CTE, moderate chemical resistance, poor surface finish
275 °C	Polyimide (Kapton)	Orange color, high CTE, good chemical resistance, expensive
250 °C	Polyetheretherketone (PEEK)	Amber color, good chemical resistance, expensive
230 °C	Polyethersulphone (PES)	Clear, good dimensional stability, poor solvent resistance, expensive
200 °C	Polyetherimide (PEI)	Strong, brittle, hazy/colored, expensive
150 °C	Polyethylene-napthalate	Clear, moderate CTE, good chemical resistance, inexpensive
120 °C	Polyester (PET)	Clear, moderate CTE, good chemical resistance, lowest cost

1. 6. THESIS ORGANIZATION

This chapter has given an introduction to and some motivation for the research on transparent conductive oxides (TCO), and thin film transistors. The first part is to obtain a TCO, on flexible substrate, with good optical and electrical properties. Silver embedded between ITO layers was chosen as the system. In the other part, a comprehensive study has been performed on the a-Si:H and a-IZO TFTs.

Chapter 2 focuses on the electrical and optical properties of the ITO-Ag-ITO multilayer system. We have obtained an excellent photopic average transmittance (~ 88 %), and resistivity (~ 2.7×10^{-5} Ω-cm.) for the case when silver just forms a continuous layer. The obtained figure of merit $41.0 \times 10^{-3}\ \Omega^{-1}$ is comparable to most of the commercial TCOs.

Chapter 3 focuses on the improvement in the electrical performance and stability of the low temperature fabricated a-Si:H on PEN. Longest annealed TFTs were found to have the best performance and elevated temperature stability. A mechanism has also been proposed to explain the obtained results.

Chapter 4 discusses the impact of low temperature long anneals on the performance and elevated temperature stability of a-IZO TFTs on PEN. The 48 hour annealed TFTs showed a stable turn-on voltage, and sub-threshold swing with operation temperatures when compared to the as-fabricated TFTs.

The mechanical and electro-mechanical stability of the a-IZO TFTs has been discussed in Chapter 5. The sub-threshold slope, mobility and I_{off} showed changes that depended on the direction and duration of the applied stress. None of the changes were catastrophic.

Chapter 6 is on the gamma radiation resistance of a-Si:H TFTs. The threshold voltage shifts in negative direction with increasing dose. A mechanism has been discussed to explain the obtained results.

Chapter 7 includes the conclusions and proposed future work.

Chapter 2

EFFECT OF AG THICKNESS ON ELECTRICAL TRANSPPORT AND OPTICAL PROPERTIES OF ITO-AG-ITO MULTILAYERS

2. 1. INTRODUCTION

Transparent conductive oxides (TCO) are materials that exhibit high transparency in the visible region along with high electrical conductivity. TCO's play an important role as transparent electrodes for flexible optoelectronic devices such as liquid crystal displays, solar cell panels, and organic light emitting devices (OLED).[1-3] A number of TCO films such as impurity-doped indium oxides, tin oxides, and zinc oxides system have been used as transparent conductors for these kinds of optoelectronic applications.[4,5] Indium tin oxide (ITO) has been a good candidate because of its low electrical resistivity (~1×10^{-4} Ω-cm) and optical transmittance as high as 90 % in the visible region.[6,7] Yet, for some advanced practical applications such resistivity values are rather high. Recently, electrical resistivity has been further improved by embedding a thin metal or metal alloy film between ITO and other oxide layers.[8-10] These structures have lower thickness than a single-layer TCO film. Amongst metals, Ag is a good candidate for such multilayer films because of its low resistivity. Several advantages of transparent conductive multilayer films, with relatively lower thicknesses, have been reported over single layered TCO films.[11,12]

The optical and electrical properties of the thin metal layer depend considerably on its thickness and deposition conditions.[13,14] The Ag mid-layer should be thin, uniform and continuous for high transmittance. The resistance of the structure will be high, if isolated islands of Ag are formed. Such isolated island growth of Ag also decreases the optical transmittance because of light scattering. Several studies have been done on the electrical and optical properties of ITO multilayers with Ag as the mid-layer.[9,14] However for these IMI multilayer films, the detailed mechanism of electrical transport and optical properties on a polymer substrate is not yet clear.

In this work, we discuss the effect of Ag mid-layer thickness on the electrical transport and optical properties of the IMI multilayer system. ITO and Ag thin films were deposited on PEN flexible substrate by rf and dc sputtering, respectively at room temperature. Annealing at 150 °C in a reducing atmosphere for 2 hours was performed after deposition to improve crystallinity along with electrical and optical properties. Comparison of sheet resistance of the IMI multilayer with the calculated sheet resistance of the Ag mid-layer indicates that most of the conduction is through the Ag film. A conduction mechanism is proposed to explain the electronic properties of the IMI multilayers with increased Ag thicknesses. We find that in this IMI system electrical transport is limited by two different scattering mechanisms depending on the thickness of the Ag mid-layer. Based on electrical and optical analysis, we deduce that the

critical thickness to form a continuous conduction path is around 8 nm. The performance of this system has been evaluated and compared to past systems using a figure of merit.

2. 2. EXPERIMENTAL DETAILS

The IMI layers were deposited by rf sputtering of ITO and dc sputtering of Ag at room temperatures onto PEN and Si. PEN polymer substrates of 125 μm thickness (Dupont Teijin Films, Teonex® Q65) were used. A sputter target of In_2O_3 containing 10 wt % SnO_2 was used for the oxide layer and pure Ag target was used for the metal layer. The base pressure of the sputter system before each deposition was approximately 1×10^{-7} Torr. The deposition was performed using pure Ar gas (99.999%) at a pressure of 6 mTorr for ITO and 10 mTorr for Ag. The ITO and Ag were deposited using an rf power of 50 W and dc power of 40 W. The time of deposition of ITO was kept constant for both top and bottom ITO layers in all of the IMI structures.

Thickness and composition of the IMI multilayer films were determined using Rutherford backscattering spectrometry (RBS) with a General Ionex Tandetron accelerator. Samples were analyzed in a vacuum of less than 10^{-6} Torr using a 2.0 MeV He ion beam. The samples were tilted to 65° to increase the depth resolution. The RUMP computer-simulation program was used to analyze the RBS data.[15] The thickness of each ITO layer was 30 nm. The Ag deposition time was varied for each IMI multilayer. The thickness of the Ag mid-layer was varied from 5.5 –

10.5 nm. Transmission electron microscopy (TEM) using a Philips CM200-FEG TEM operating at 200 kV was used to confirm the thickness of the layers.

After deposition, the samples were annealed in 5 % H_2/Ar (reducing atmosphere) at 150 °C for 2 hours. The phase of the as-deposited ITO multilayers were investigated by X-ray diffraction analysis (XRD) using a Philips X'pert MPD diffractometer with a Cu K_α radiation source. A working voltage of 45 kV was employed with a filament current of 40 mA. A glancing angle of 1° was used for the incident beam during the analysis. International center for diffraction data were used for phase identification.

Optical transmittance, reflectivity, and absorbance of the multilayers were measured using an Ocean Optics double channel spectrometer (model DS200) in a wavelength range of 300-900 nm with an aluminum mirror as the reference for reflectivity, and air reference for transmittance. Tungsten-halogen and deuterium lamps were used as sources for visible and UV light, respectively.

Hall measurements were done using a HMS3000 tool. A magnetic field of 0.51 T was applied perpendicular to the sample surface to measure carrier concentration, Hall mobility, and resistivity. A Van der Pauw test configuration was used. Surface topography was evaluated using atomic force microscopy (AFM) in acoustic mode (tapping mode), using a Molecular Imaging Pico scanning probe microscope.

2. 3. RESULTS

Figure 2.1 show 2.0 MeV RBS spectra from ITO-Ag-ITO multilayers on PEN for 5.5 and 10.5 nm thick Ag mid-layers. The indium, silver and tin peaks are difficult to differentiate due to the closeness of their atomic masses. The In + Sn peaks are located between channels 250 and 350; whereas, the oxygen peak is near the channel 130. The Ag peak overlaps with the In + Sn peak from the bottom ITO in the multilayer structure. The Ag signal exhibits increased peak height and width with increasing Ag thickness. Also, with increasing Ag thickness, the valley between the signals from top and bottom ITO becomes deeper.

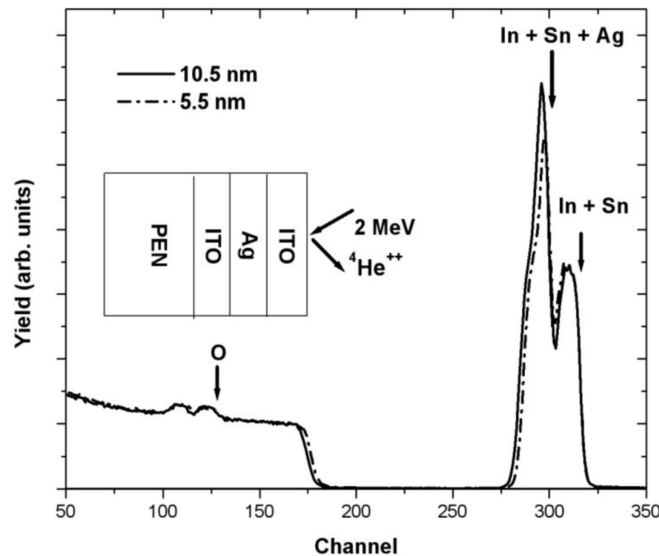


Figure 2.1 2 MeV RBS spectra obtained from ITO-Ag-ITO multilayer for 5.5 and 10.5 nm Ag mid-layer

The crystalline structures of IMI multilayers with different silver thicknesses were determined using 1° glancing angle XRD measurements. Cards 39-1058 [16] and 89-3722 [17] were used to identify the ITO and Ag peaks, respectively. Figure 2.2 shows XRD patterns obtained from both as deposited and annealed multilayers. ITO was amorphous in the as-deposited multilayers as shown in Figure 2.2 (a). However after annealing, strong crystallization of the ITO (Figure 2.2(b)) was obtained. The ITO peak at 30.66° (2 theta) corresponds to the 222 reflection of the cubic bixbyite structure of indium oxide. The intensity of the ITO (222) peaks increased with increasing Ag thickness. On the other hand, there was no change in the intensity of the silver (111) peak after annealing. Similar XRD pattern and behavior have been observed for ITO/Me/ITO (Me = Ag and Cu) [18] and ITO-Ag-ITO [12]. The intensity of the other ITO peaks decreased with increasing thickness of the Ag layer. Grain sizes (*d*) were calculated using the peak (full width at half maximum) FWHM values, with Scherrer's formula:

$$d = \frac{\mathrm{K} * \lambda}{\mathrm{FWHM} * \cos\theta} \tag{1}$$

where, K denotes the Scherrer constant (□ = 0.94 for cubic lattices), and λ is the wavelength of the incident Cu K_α radiation (0.154056 nm).

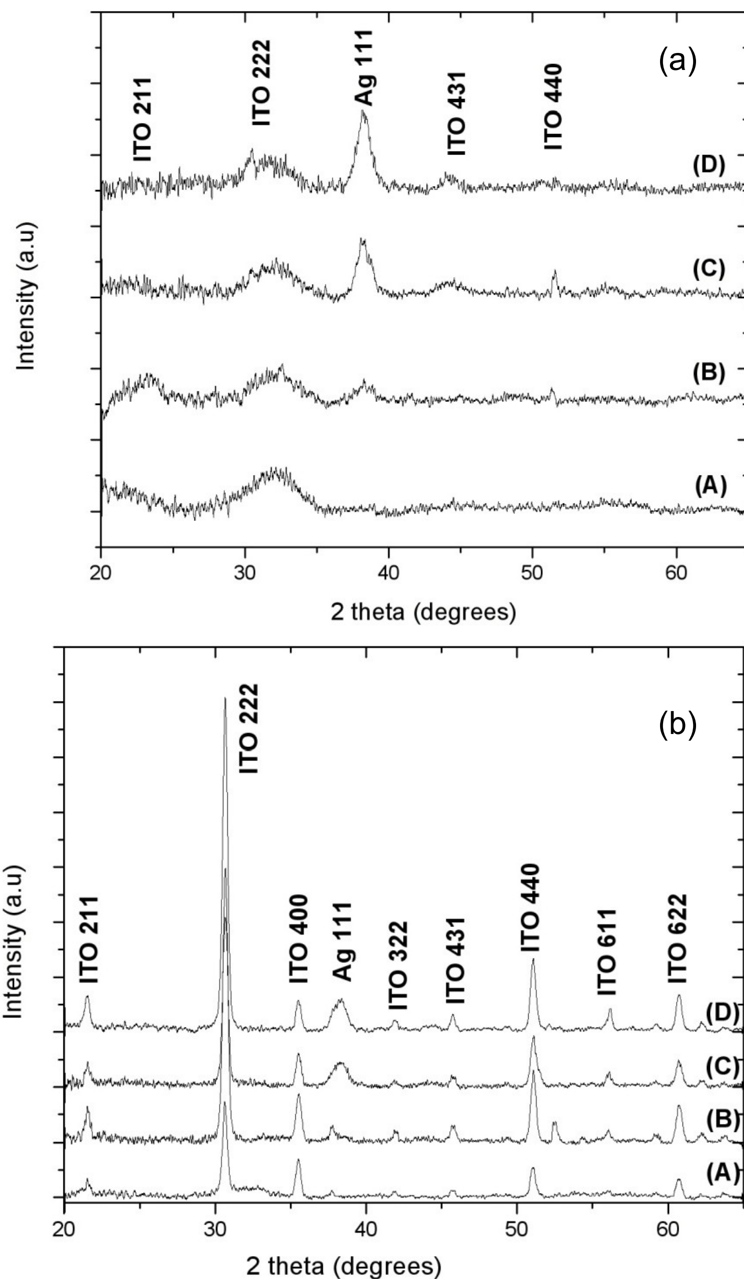


Figure 2.2 XRD patterns from ITO multilayers on Si with varying Ag mid-layer thickness: (a) as-deposited (b) annealed in 5 % H_2/Ar (reducing atmosphere) at 150 °C for 2 hours. (A) bare ITO, (B) 5.5 nm Ag, (C) 9 nm Ag, and (D) 10.5 nm Ag.

Figure 2.3 shows the surface topography of the IMI multilayer structures as measured by AFM and using 1 × 1 μm^2 scans. With increasing Ag mid-layer thickness (5.5-10.5 nm) the grain size increases from 35 to 50 nm. The rms roughness changes from 0.8 nm to 1.4 nm with increasing Ag thickness. The surface roughness of TCO film plays an important role in determining the optical properties of the multilayer films; smoother films have better transparency. Other investigations report that the surface roughness of the TCO films used for electrodes in electroluminescence plays an important role in determining the efficiency of the display device. [19]

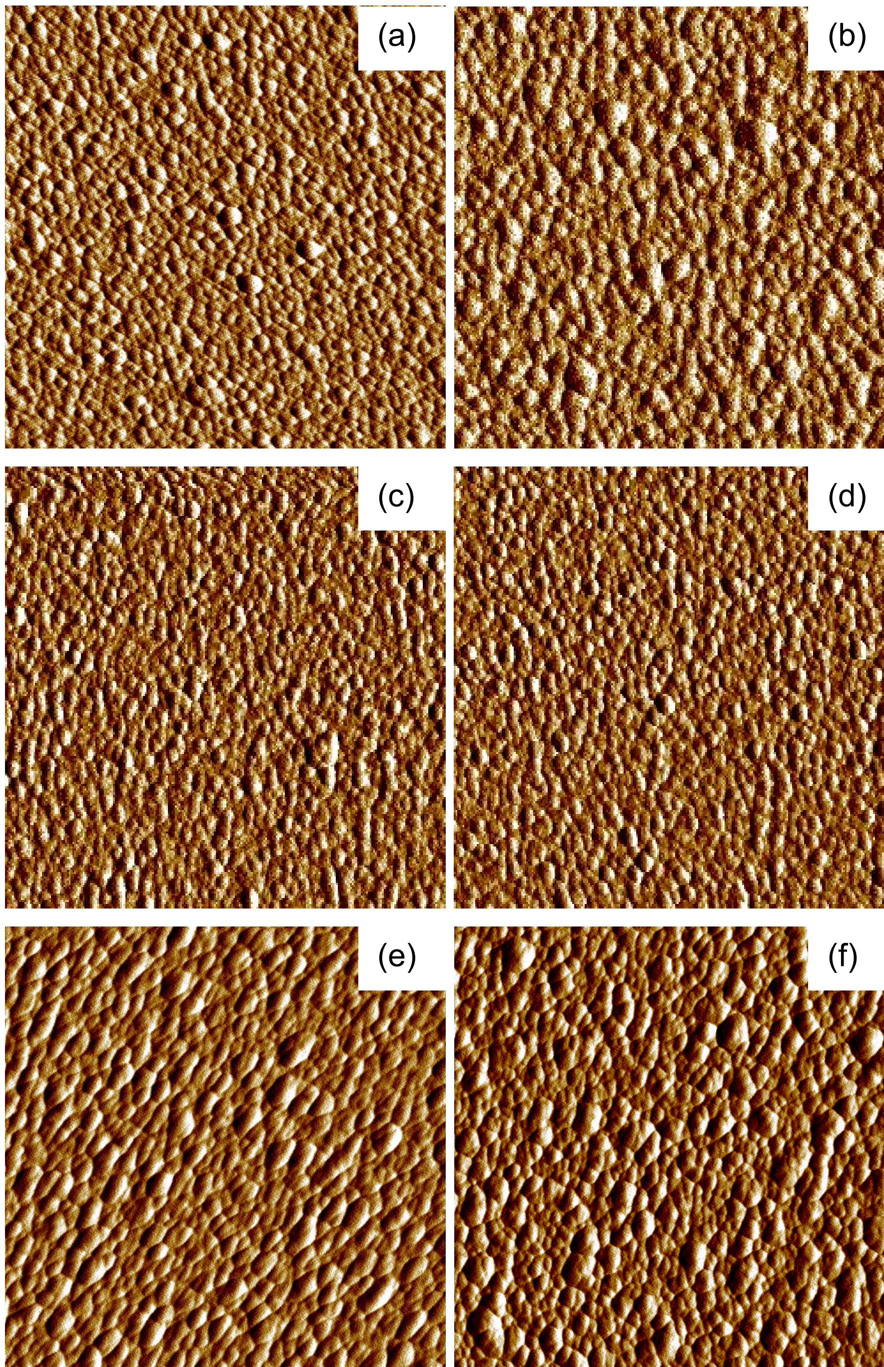


Figure 2.3 1 × 1 μm^2 AFM images from as-deposited IMI multilayers on Si for different Ag thicknesses: (a) bare ITO, (b) 5.5 nm Ag, (c) 7 nm Ag, (d) 8 nm Ag, (e) 9 nm Ag, and (f) 10.5 nm Ag

Figure 2.4 shows the effect of Ag mid-layer on the resistivity of both as-deposited and annealed IMI multilayers. Resistivity decreases with increasing thickness of the Ag mid-layer in the IMI multilayer for both as-deposited and annealed multilayers. When a 7 nm Ag film is deposited between the ITO layers, the resistivity decreases by almost an order of magnitude compared to bare ITO. As the Ag thickness is increased from 7 nm to 10.5 nm, the resistivity gradually decreases down to ~ 20 μΩ-cm. However, there is not a significant change in the resistivity of the multilayers after annealing. Assuming that the total resistance of the IMI multilayer is a result of parallel combination of the three individual layers (see Figure 2.5), it is possible to calculate the resistivity of the Ag mid-layer:

$$\rho_{Ag} = d_{Ag}\left(\frac{1}{R_{Sq}} - 2\frac{d_{ITO}}{\rho_{ITO}}\right)^{-1} \qquad (2)$$

where, ρ_{Ag} is the resistivity of Ag, d_{Ag} is the thickness of the Ag, R_{Sq} is the sheet resistance of the IMI multilayer, d_{ITO} is the thickness of the ITO layer, and ρ_{ITO} is the resistivity of the ITO. The resistance of the top and bottom ITO layer in the IMI structure has been assumed to be constant in equation 2. Table I shows the specific resistivity of the Ag mid-layer. The specific resistivity values decrease from 9.6 μΩ-cm to 4.2 μΩ-cm with increasing Ag layer thickness.

Table 2.1 Sheet resistance and specific resistivity values of Ag in ITO-Ag-ITO multilayer films.

Ag thickness (nm)	**ITO-Ag-ITO $R_{Sq.}$ (Ω/sq.)**	**Ag $R_{Sq.}$ (Ω/sq.)**	**ρ_{Ag} (μΩ-cm)**
5.5	15.2	17.5	9.6
7.0	8.2	8.8	6.2
8.0	6.8	7.2	5.8
9.0	5.5	5.8	5.2
10.5	3.9	4.0	4.2

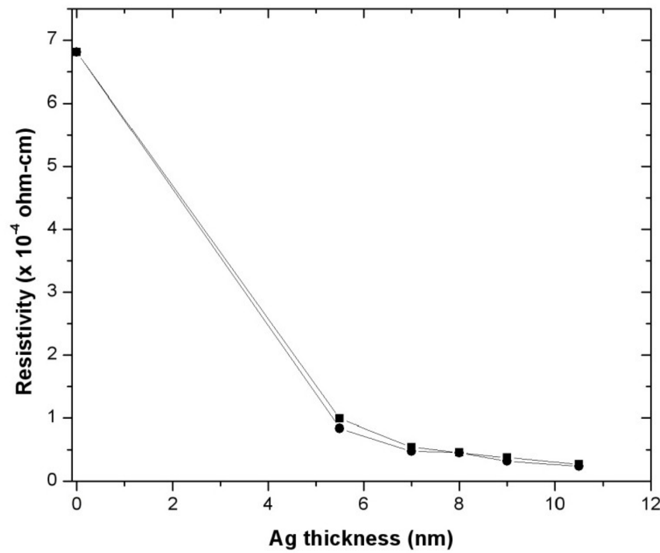


Figure 2.4 Resistivity of ITO-Ag-ITO multilayer films as a function of Ag thickness for both as-deposited and annealed samples: (a) as-deposited multilayers (— ■ —) and (b) annealed multilayers (– – ● – –)

Figure 2.6 shows the change in carrier concentration as a function of Ag thickness for both as-deposited and annealed samples. The plot indicates that carrier concentration depends strongly on the Ag thickness. The carrier concentration of the IMI multilayer has increased by about two orders of magnitude upon insertion of the 10.5 nm Ag layer compared to bare ITO. After annealing there is no significant change in the carrier concentration of the multilayers. The charge carriers in metals are also independent of temperature, as they are provided by the valence electrons.[20] Hence, metallic conduction is taking place in this IMI system

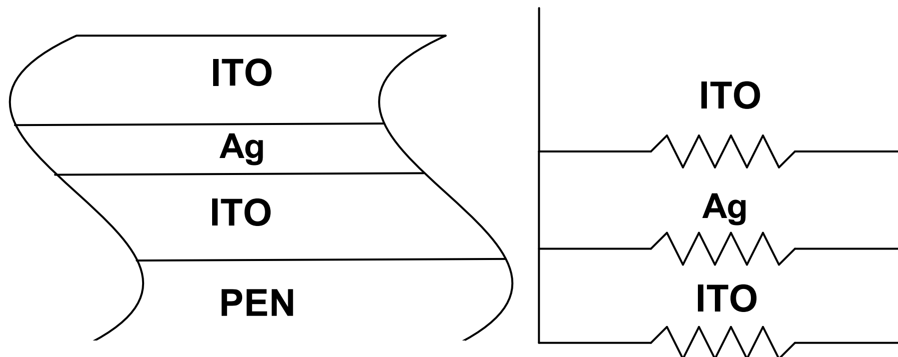


Figure 2.5 Electrical schematic of the IMI multilayer, showing the resistance due to ITO and Ag layers

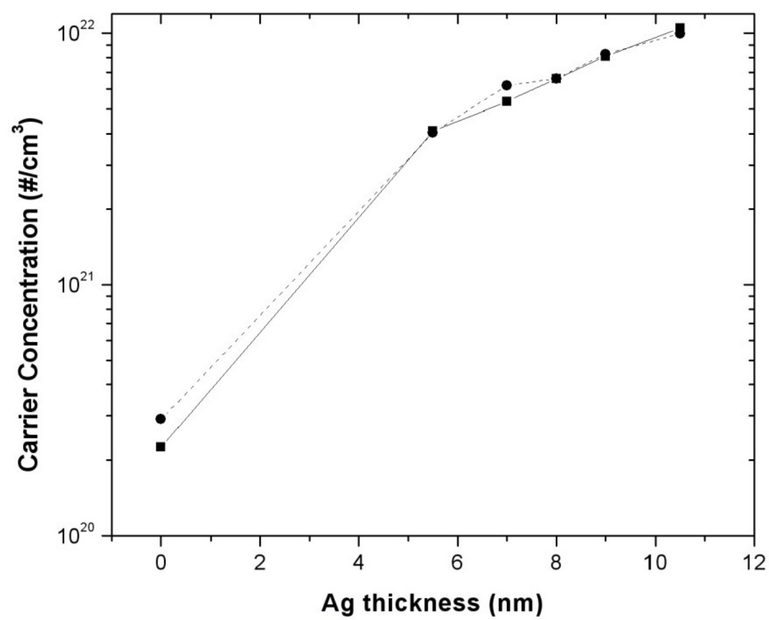


Figure 2.6 Carrier concentrations of ITO-Ag-ITO multilayer films as a function of Ag thickness for both as-deposited and annealed samples: (a) as-deposited multilayers (— ■ —) and (b) annealed multilayers (– – ● – –)

The Hall mobility of the IMI multilayer as a function of Ag thickness for both as-deposited and annealed samples is shown in Figure 2.7. The Hall mobility of the as-deposited ITO multilayers decreases from 25 cm^2/V-s for bare ITO to 10 cm^2/V-s for a 5.5 nm thickness Ag. When the Ag layer is increased to 7 nm, there is an increase in the Hall mobility. There is a slight increase in Hall mobility with further increase in the Ag thickness. Annealed multilayers showed a similar trend of Hall mobility with increasing Ag thickness.

Figure 2.8 shows cross-section TEM micrographs obtained from the multilayers. The multilayer with 5.5 nm Ag (Fig. 8 (a)) has discontinuous and island growth. At this thickness, Ag metal islands have formed and are starting to coalesce. As the Ag thickness is increased from 5.5 nm to 8 nm, a continuous Ag layer is formed as shown in Figure 2.8 (b). At this thickness a continuous path for electron conduction is formed as expected based on the Hall mobility results.

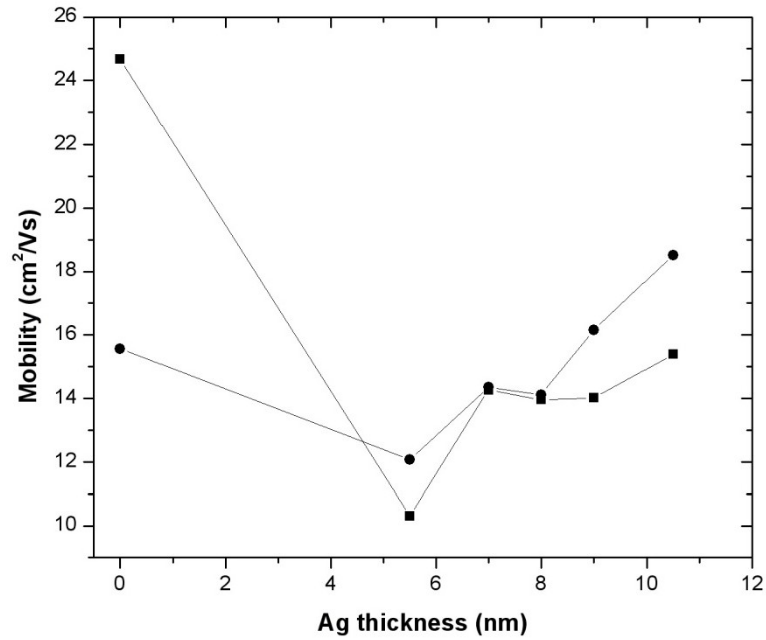


Figure 2.7 Hall mobility of ITO-Ag-ITO multilayer films as a function of Ag thickness for both as-deposited and annealed samples: (a) as-deposited multilayers (— ■ —) and (b) annealed multilayers (– – ● – –)

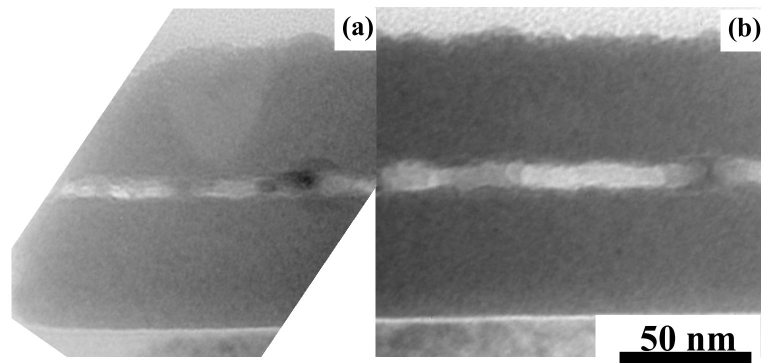
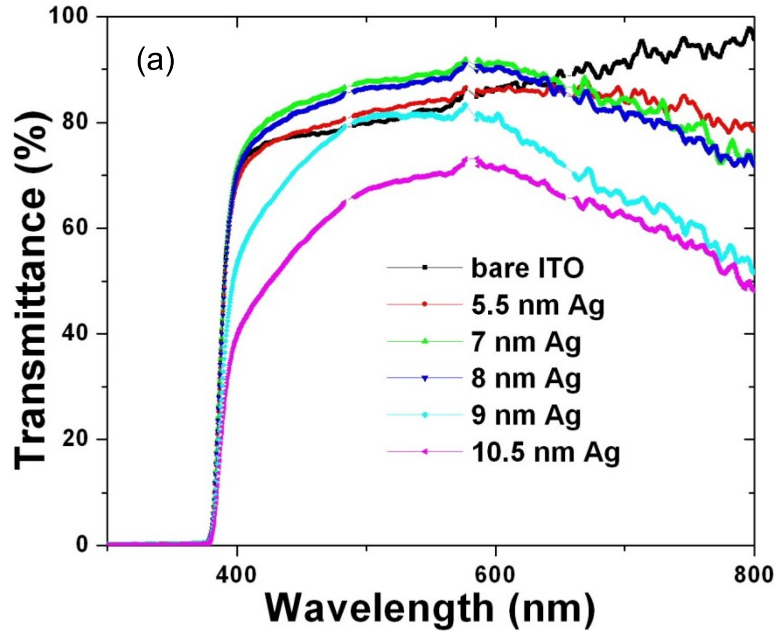


Figure 2.8 Cross section TEM micrographs of ITO/Ag/ITO multilayers with two different thicknesses: (a) 5.5 nm, and (b) 8 nm

The optical transmittance and reflectance of IMI multilayers on PEN substrates, as a function of Ag thickness, are shown in Figure 2.9 and Figure 2.10, respectively. The maximum optical transmittance of the pure single-layer ITO film is about 85% in the visible region. IMI multilayers with thicker Ag (9 nm and 10.5 nm) show maximum transmittance at around 500 nm wavelength and thinner Ag mid-layers (from 5.5 nm to 8 nm) show a maximum transmittance at around 600 nm wavelength. There is an increase in maximum transmittance as Ag mid-layer thickness is increased from 5.5 nm to 8 nm. However, the maximum transmittance drops upon further increase in the Ag thickness. IMI multilayers with Ag thicknesses of 7 - 8 nm have higher transmittance compared to multilayers with other Ag thicknesses. The rate of decline of the transmittance, for wavelengths greater than the maximum-transmittance wavelength, increases with increasing Ag thickness. Similar behavior was observed in the annealed ITO multilayers as shown in Figure 2.9(b). However, there is a slight increase in the average transmittance after the samples are annealed. The reflectance (Figure 2.10) in the multilayers at longer wavelength increases with increasing Ag thickness for both as-deposited and annealed samples.



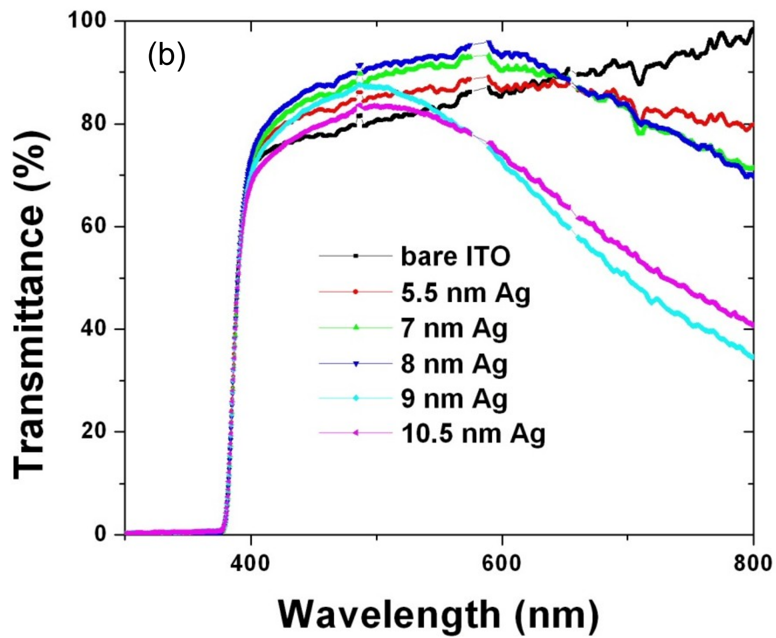


Figure 2.9 Optical transmittance spectra from as-deposited and annealed ITO-Ag-ITO multilayer films as a function of Ag thickness on the PEN substrate: (a) as-deposited multilayers (b) annealed multilayers.

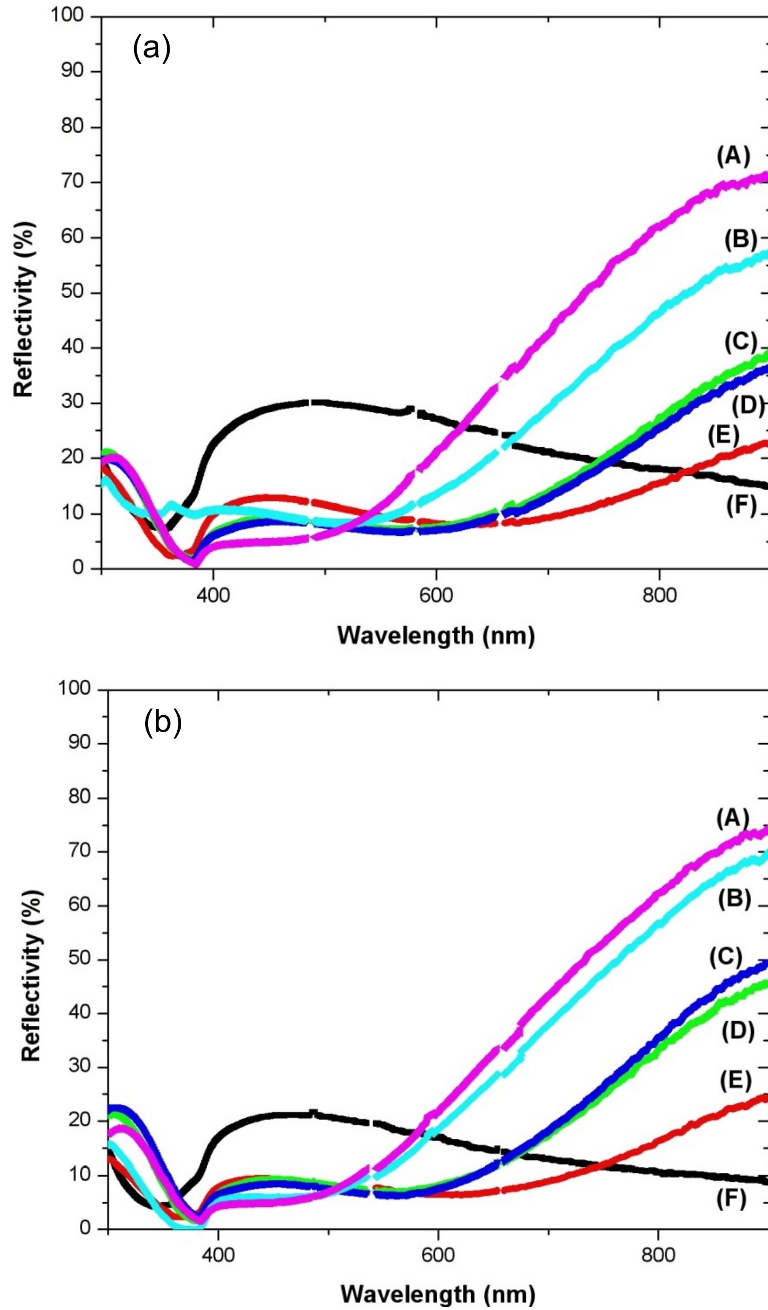


Figure 2.10 Optical reflectivity spectra from as-deposited and annealed ITO-Ag-ITO multilayer films as a function of Ag thickness on the PEN substrate: (a) as-deposited multilayers (b) annealed multialyers. (A) 10.5 nm Ag, (B) 9 nm Ag, (C) 8 nm Ag, (D) 7 nm Ag, (E) 5.5 nm Ag, and (F) bare ITO

Figures 2.11 and 2.12 show the variation in absorption coefficient (α) with phonon energy for IMI multilayers on PEN and glass substrates, respectively. The absorption coefficient data were used to determine the optical band gap (E_g), using the following equation [21]:

$$\alpha(\mathrm{h}\upsilon) \propto (\mathrm{h}\upsilon - E_g)^{1/2} \quad (3)$$

where hu is the photon energy. The optical band gap is deduced from the absorption edge by straight-line extrapolation of the absorption to zero. The optical band gap of annealed ITO on PEN obtained from Figure 2.10 is ~ 3.24 eV. The optical band gap of as-deposited ITO on glass is obtained from Figure 2.11 and has a value approximately 4.27 eV. The optical band gap of the IMI system on glass substrates decreases with increasing in Ag mid-layer thickness.

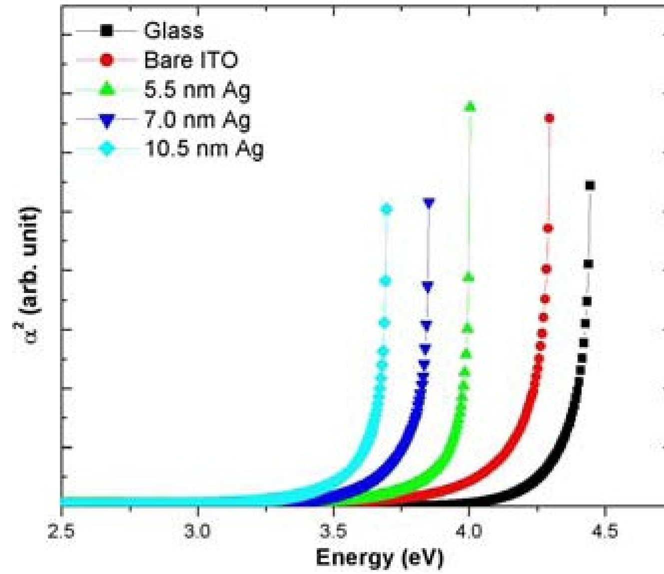


Figure 2.11 Absorption coefficient change with energy of photons showing the change in the band gap energy of the as-deposited multilayers on glass substrate

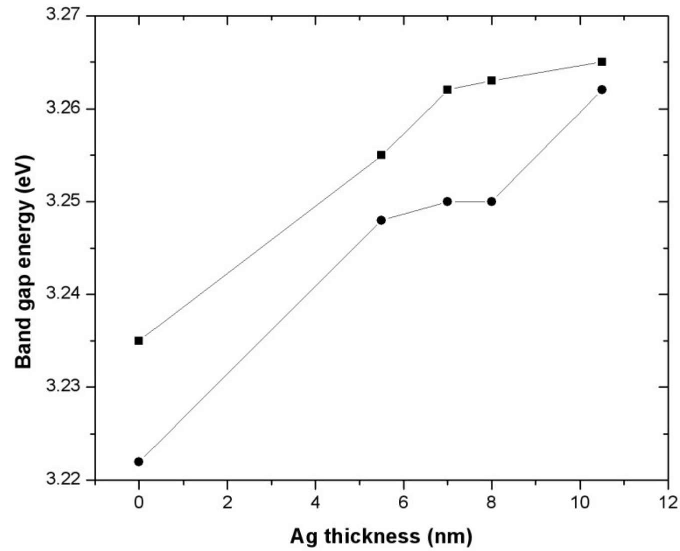


Figure 2.12 Absorption coefficient change with energy of photons showing the change in the band gap energy of the as-deposited multilayers on glass substrate

2. 4. DISCUSSION

The increase in the intensity of the ITO (222) peak with increasing Ag thickness in the annealed multilayers can be explained based on the crystal symmetry of ITO and Ag. After annealing, the amorphous ITO in the as-deposited multilayer crystallizes with cubic structure. Ag has a FCC structure and has an (111) orientation in the IMI system. As both ITO and Ag are from cubic system, the texturing of the top ITO (111) reflection is evident by the increased intensity of the (222) reflection with increasing Ag thickness.

The resistivity values of Ag calculated using Equation 2 provides information about electronic conduction taking place in the IMI multilayers. As shown in Table I, specific resistivity values of the Ag mid-layer decreases from 9.6 to 4.2 μΩ-cm with increasing Ag thickness. Based on the sheet resistance variation of the IMI multilayer and of the Ag film, with increasing Ag mid-layer thickness, it appears that the conductivity of the IMI multilayer is mainly provided by the Ag film. A similar result has been obtained for ITO-AgCu-ITO multilayers [22]. Bender *et al.* have also observed a decrease in the specific resistivities of AgCu from > 10^6 μΩ-cm to 6.2 μΩ-cm with increasing AgCu thickness.

The change in resistivity of the IMI multilayer films with increasing Ag thickness can be explained using the following basic relation:

$$\rho = \frac{1}{ne\mu} \quad (4)$$

where, ρ is the resistivity, n is the number of charge carriers, e is the charge of the carrier and μ is the mobility.[20] From this equation we see that changes in mobility, carrier concentration or both can affect the resistivity. There are many scattering mechanisms which can affect the mobility of carriers, and hence the resistivity of the film. Given that the conduction in the multilayer is primarily through the Ag mid-layer, the main scattering mechanisms that can influence charge carriers are interface scattering, surface scattering, or grain-boundary scattering.

The increase in the carrier concentration with the inclusion of Ag mid-layer can be understood based on the Schottky theory. Figure 2.13 shows the schematic of the energy band diagram of the ITO and Ag prior to (Figure 2.13(a)) and after their contact (Figure 2.13(b)). As the work function of the silver (Φ = 4.4 eV) is smaller than ITO (Φ = 4.5-5.1 eV, depending on stoichiometry, organic contamination and oxidation type), there is a transfer of electrons from Ag to ITO to align the Fermi levels at equilibrium. [23- 25]. There is a band bending at the contact and forms an accumulation-type contact. Hence, the electrons are easily injected from Ag into ITO; as there is essentially no barrier for electron flow.

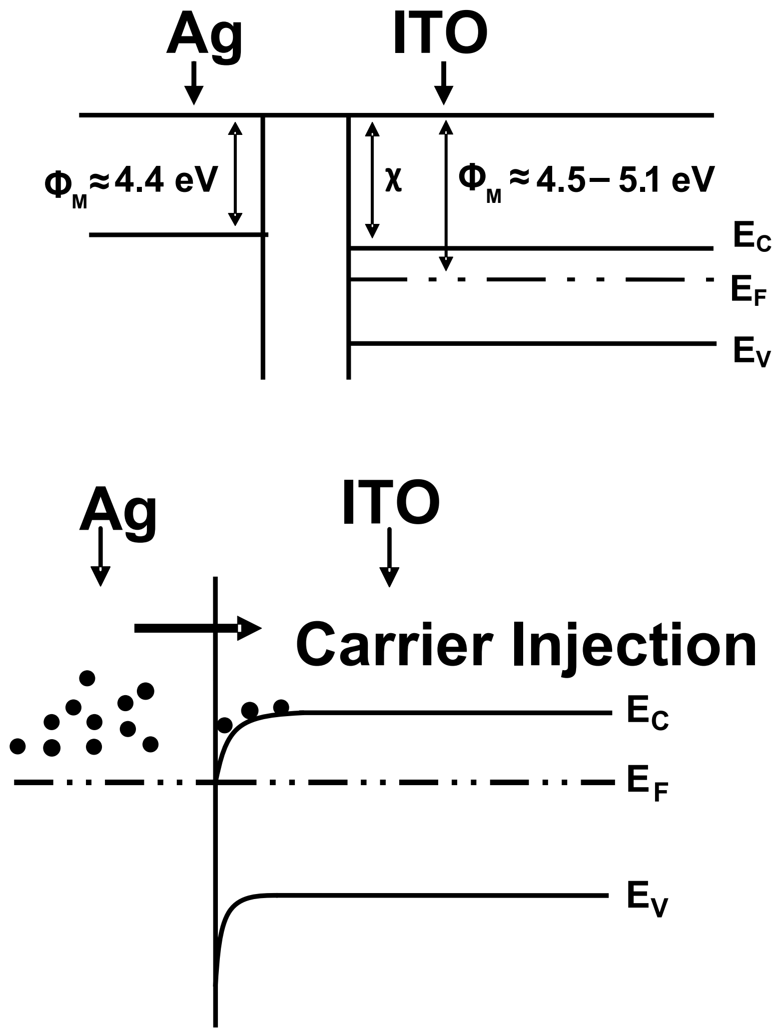


Figure 2.13 Schematic diagrams of the energy band structures of ITO and Ag: (a) before contact and (b) after contact

By the physical configuration of the IMI structure (Figure 2.5.); the large ratio of the interface area to IMI volume would imply that surface scattering is the dominant scattering mechanism. This fact will also be supported if the mean free path (MFP) is greater than the film thickness and grain size. In order to compare the MFP to features of the IMI structure, MFP is calculated by the following relation:

$$l = \left(\frac{h}{2e}\right)\left(\frac{3n}{\pi}\right)^{1/3} \mu \tag{5}$$

where, *h* is the Plank's constant, and *l* is the mean free path.[26] The calculated values are shown in Table II. Inspection of the calculated MFP values (Table II) reveals that the typical values of the MFP are comparable to the Ag thicknesses. However, the MFP values are less than the grain size (35-50 nm).To these points, the scattering due to grain boundaries cannot be excluded.

The variation in mobility with increasing Ag thickness can be explained by the combined effects of interface scattering and grain boundary scattering. Figure 2.14 shows a schematic depicting growth stages of the Ag layer a function of film thickness, prior to deposition of the top ITO layer. This schematic helps to explain the mobility variation as a function of Ag. During the initial stages of Ag growth, small Ag islands are formed on the bottom ITO (Figure 2.14 (a)). With a further increase in Ag

thickness a continuous layer is formed at the critical thickness (Figure 2.14 (b)). Figure 2.14 (c) shows a schematic for Ag thickness greater than the critical thickness. When the Ag layers are thin, the interface regions constitute a greater fraction of the total layer thickness. As the Ag layer thickness is increased, the interface regions become a smaller fraction of the total layer thickness. Therefore, the mobility is expected to be lowest for the thinnest Ag layer and to steadily increase as the Ag layer thickness is increased. As shown in Figure 2.7, the mobility drops to 10.3 cm^2/V-s for the as-deposited multilayer and 12 cm^2/V-s after annealing upon insertion of a 5.5 nm Ag mid-layer. As the Ag mid-layer thickness is increased to 7 nm, the mobility rises to 14 cm^2/V-s and 14.35 cm^2/V-s for as-deposited and annealed multilayers respectively. This trend suggests that interface scattering (*i.e.,* scattering of carriers at the Ag/ITO and ITO/Ag interfaces) is the primary mechanism. However, for higher Ag thicknesses (8 – 10.5 nm), the rise in Hall mobility values are less, in case of the as-deposited multilayer. The mobility increases from 14 cm^2/V-s (for 8 nm Ag thickness) to 15.4 cm^2/V-s (for 10.5 nm Ag thickness). This behavior for higher Ag mid-layer thicknesses can be explained by grain boundary scattering. As shown in Figure 2.3, the grain size increases from 35 to 50 nm with increasing Ag thickness. With increasing grain size, the fraction of grain boundary area decreases, resulting in an increase in the mobility. The plot shown in Figure 2.7 can be divided into two regions to

explain the scattering mechanism in the IMI multilayer. The first region is for lower Ag thickness values (less than 8 nm) and second for

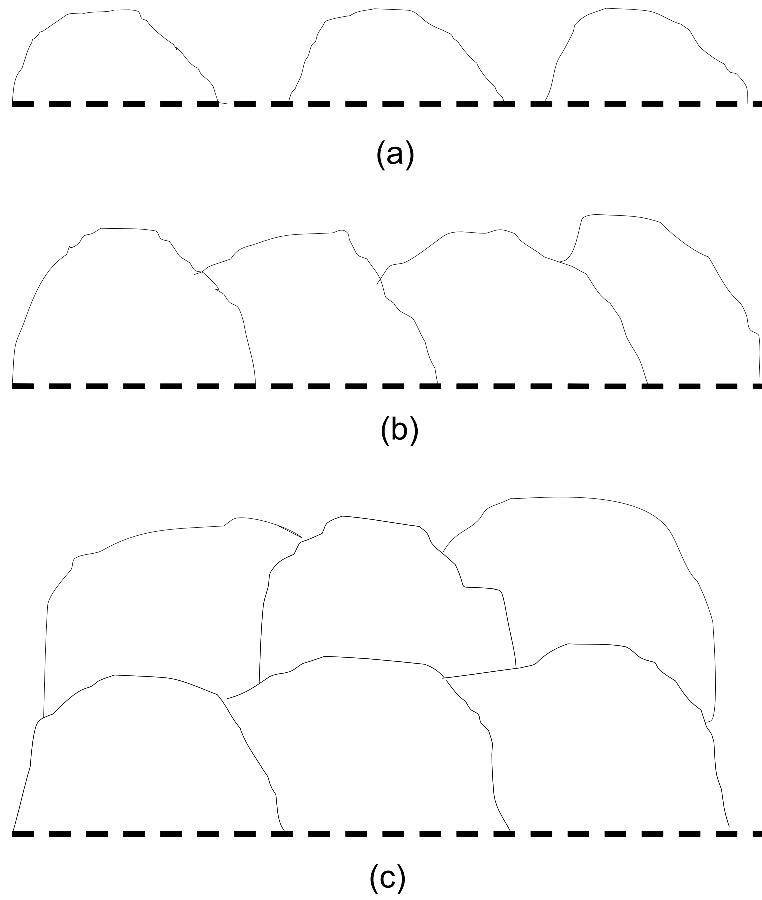


Figure 2.14 Schematic of growth stages of Ag mid-layer prior to deposition of top ITO as a function of Ag thickness. Dashed line (**-------**) is the interface between the Ag and bottom ITO layer: (a) Isolated island growth of Ag layer, (b) Continuous Ag layer at critical thickness, and (c) Continuous Ag layer for thickness greater than critical thickness

higher thickness values (8-10.5 nm). Interface scattering dominates for the first region and grain boundary scattering dominates for second region. The lesser rise in the mobility values in the second region infers that a continuous Ag layer is formed at around 7-8 nm Ag thickness. This is consistent with the result of Zhao *et al.* (Ref. 27), where a critical Ag thickness of 6.2 nm is observed to form a continuous path for conduction. As compared to as-deposited multilayers, the annealed multilayers have higher Hall mobility values. This is likely due to an increase in the crystallinity of the multilayers after annealing, as shown in Figure 2.1 (b).

The difference in optical properties of the IMI multilayer films with different Ag thicknesses is explained based on scattering and absorption by the Ag mid-layer. The difference in average optical transmittance for various Ag thicknesses at shorter wavelengths is due to light scattering at the ITO/Ag interface in Ag isolated islands and absorption of light due to interband electronic transitions.[28] Also, at shorter wavelengths, the reflectance is low. As the Ag thickness increases, the Ag becomes a continuous layer which causes decreased light scattering. The average optical transmittance is highest for the 8 nm Ag mid-layer, and transmittance decreases for Ag thicknesses greater than or less than 8 nm (as shown in Figure 2.9). The transmittance values for Ag thicknesses of 7 and 8 nm are very close. The decrease in transmittance for Ag thickness less than 8 nm is due to discontinuous island growth of Ag below 8 nm thickness leading to scattering losses. For Ag thickness greater than 8 nm,

more electrons are available for excitation and, hence there is a drop in the transmittance. These results further substantiate the inference of formation of a continuous conductive Ag layer at around 8 nm layer-thickness, based on conduction behavior. At longer wavelengths (*i.e.*, in the red part of the visible spectrum) the transmittance decreases with increasing thickness of Ag because of high reflectance (Figure 2.10) of Ag. As shown in Figure 2.9(b), annealed samples showed a slight increase in the optical transmission for all Ag thicknesses. This small change in transmission is most likely because of improved crystallinity of the ITO after annealing. This data along with electrical (mobility) data indicate that a continuous layer of Ag is formed at around 8 nm.

The optical band gap of the ITO multilayer films, on PEN substrates, was deduced from Figure 2.10. The optical band gap obtained for annealed bare ITO is ~ 3.24 eV. In contrast to the optical band gap of ITO on PEN, a study of sputter deposited ITO on glass substrates reports an optical band gap of ~ 3.8-4.2 eV[29,30] According to our results, the measured optical band gap for ITO/PEN is the optical band gap of the ITO + PEN composite because PEN is known to have a band gap of ~ 3.2 eV.[31, 32] To measure the exact optical band gap of the IMI multilayers, we deposited the multilayers on glass. The band gap decreases with increasing Ag mid-layer thickness in the IMI multilayers. The optical band gap of this IMI system decreases from 4.27 eV (Bare ITO) to 3.67 eV (10.5 nm Ag mid-layer). The decrease in the band gap with Ag thickness

is likely due to high electron concentration in the conduction band as well as some ionized Ag atoms in the Ag layer.

In degenerate semiconductors like ITO and ZnO, the optical band gap can be increased and/or decreased by carrier concentration.[21] The shift in the band gap to higher energy with increasing concentrations can be explained in terms of the Burstein-Moss (BM) effect.[21] In this case, the measured optical band-gap is a convolution of the undoped band gap of ITO and the BM shift. Kim and Park (Ref. 33) have seen band gap narrowing above the critical concentration (5×10^{19} /cm^3) in their In doped ZnO system. Band gap narrowing has also been reported in degenerate semiconductors with carrier concentrations above the Mott critical density [33, 34]. This band gap narrowing with carrier concentrations above the Mott critical density is mainly due to (*i*) merging of conduction and donor bands, (*ii*) band tailing by impurity-induced potential fluctuations, and (*iii*) electron-electron and electron-impurity scattering. In our system, the increase in carrier concentration is not due to doping effect, but rather due to carrier injection from the Ag layer (as shown in Figure 2.13). Therefore, band tailing by impurity-induced potential fluctuations cannot be the dominant mechanism in our IMI system.

The injected electrons from the Ag layer accumulate in the conduction band of the ITO. Also, some of the Ag atoms in the adjacent layer ionize and become positively charged. The electrons in the conduction band attract the positively charged Ag atoms and also repel

each other due to Coulomb repulsion. The resulting electric field is directed from positively charged Ag to the electrons in the conduction band due to this charge transfer. Hence, we believe that these many body effects cause a downward shift of the conduction band and upward shift of the valence band and results in band gap narrowing.

A figure of merit, φ_{TC}, as defined by Haacke (Ref. 35), was estimated for each of the IMI multilayers.

$$\varphi_{TC} = \frac{{T_{av}}^{10}}{R_{sh}} \tag{6}$$

where, T_{av} is the transmittance and R_{sh} is the sheet resistance. Figure 2.15 shows a plot of φ_{TC} as a function of Ag thickness for both annealed and as-deposited multilayers. From the plot, we see that the best φ_{TC} is obtained when the Ag layer is just continuous for both as-deposited and annealed ITO multilayer samples. Also, the figure of merit (FOM) improves after annealing. The jump in the FOM for the 10.5 nm Ag thickness is due to the lower sheet resistance of 10.5 nm Ag compared to the 9 nm Ag layer, with optical transmittance almost being constant. The calculated φ_{TC} ($46.1\times10^{-3}\ \Omega^{-1}$) for our annealed ITO multilayers (at Ag critical thickness) is almost 3 times better than the figure of merit for ITO films that were optimized for flat panel display applications ($\varphi_{TC} = 14.9\times10^{-3}\ \Omega^{-1}$).[22]

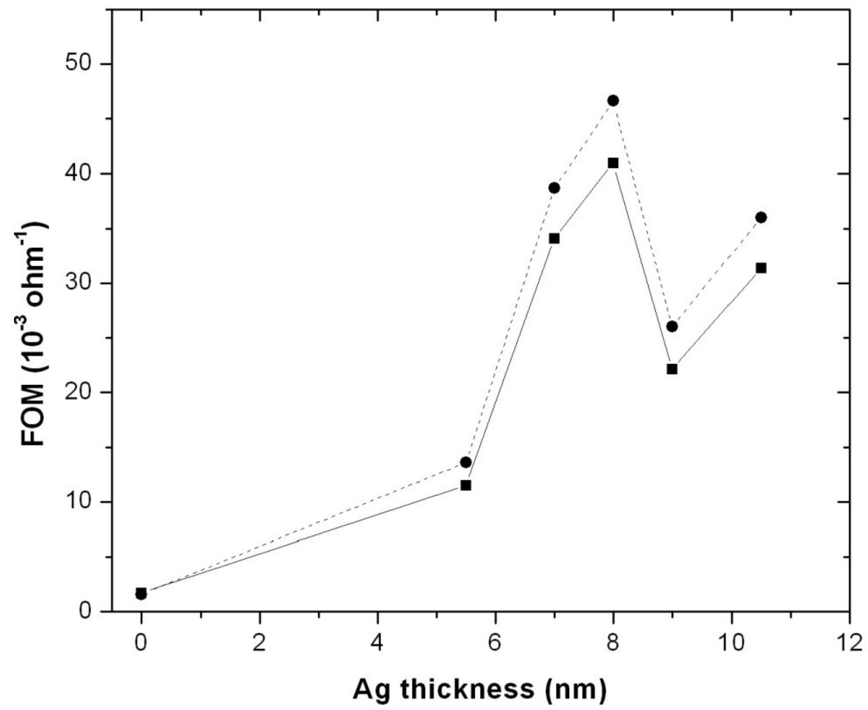


Figure 2.15 Figure of merit of ITO-Ag-ITO multilayer films as a function of Ag thickness for both as-deposited and annealed samples. (a) as-deposited multilayers (— ■ —) and (b) annealed multilayers (– – ● – –)

2. 5. CONCLUSION

IMI multilayer films were deposited on PEN at room temperature by rf and dc sputtering. Electrical and optical properties were correlated with Ag mid-layer thickness. Sheet resistance variation of the IMI multilayer combined with calculated Ag resistivity with increasing Ag mid-layer thickness, indicated that the conductivity of the ITO multilayer is mainly due to the Ag mid-layer. Hall mobility along with optical transmittance variations, as a function of Ag mid-layer thickness, suggests that the critical thickness for Ag to form a continuous path for conduction is 8 nm. There is a red shift in the band gap of the IMI multilayer films on glass substrate with increasing Ag thickness due to band tailing by impurity-induced potential fluctuations. Carrier transport is limited by either interface scattering or grain boundary scattering depending on the thickness of the Ag mid-layer. Interface scattering is dominant for thinner Ag (5.5 -7 nm) and grain boundary scattering is dominant for thicker Ag mid-layer (8 – 10.5 nm). These results can be applied to other transparent conducting IMI systems. FOM (φ_{TC} = 46.1×10^{-3} Ω^{-1}) obtained was maximum for a Ag mid-layer at the critical thickness of 8 nm, for annealed samples.

Chapter 3

HIGH TEMPERATURE STABILITY AND ENHANCED PERFORMANCE OF a-Si:H TFT ON FLEXIBLE SUBSTRATE DUE TO IMPROVED INTERFACE QUALITY

3. 1. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) thin-film-transistors (TFTs) fabricated on flexible substrates have been a desirable choice in flat panel industry for more than two decades [1-2]. They have been used as a switching element of active-matrix-liquid-crystal displays (AMLCD) and also in pixel circuits of organic light emitting displays (OLED) [3-4]. These TFTs fabricated on flexible substrate have an added advantage of flexibility, light weight, good uniformity, and ease of fabrication on large areas compared to glass substrates. However for plastic substrates, the fabrication temperature is usually lower than 180 °C. In last decade, many investigations have focused on the fabrication of high quality a-Si:H TFTs at deposition temperature below 150 °C for flexible electronics applications [5-7]. The TFTs fabricated at such low temperatures typically are less stable and posses a substantial level of defects when compared to conventional TFTs fabricated at high temperatures ~ 300 °C [8-9].

The electrical performance of the a-Si:H TFT is mostly decided by the quality of the a-Si:H film and the a-Si:H/SiN_x interface. It has been a great challenge to fabricate low leakage insulator along with good quality

a-Si:H layer using low temperature-fabrication-technology for flexible electronics applications. A considerable amount of charge can be trapped inside the insulator at such low fabrication temperatures (< 150 ^{o}C). The trapped charge inside the insulator along with ease of state creations in the a-Si:H layer leads to threshold voltage shift (ΔV_t) after prolonged bias-stress. Applications such as AMLCD, OLED etc. demands for high field-effect mobility, low threshold voltage values and high electrical stability [10]. This ΔV_t shift limits the usefulness of these TFTs in demanding applications such as in OLEDs. This adverse affect of ΔV_t is more pronounced in current driven OLEDs [3]. The non-uniform pixel-to-pixel voltage shift affects the brightness uniformity across the screen of the OLED [11]. Along with ΔV_t hysteresis phenomenon caused due to trapped charges inside insulator is also a poor characteristic of a-Si:H TFT. This can be a major drawback to use low temperature fabricated TFTs as the pixel element of active matrix organic light emitting diode (AMOLED). Hence, techniques are needed to either inhibit or reverse this ΔV_t along with reduction of the trapped charges inside the insulator by some predictive pre- or post- fabrication treatment. Up to this date, the performance of TFTs has been improved by changing the process parameters during their fabrication [12]. Anneal studies have shown some improvements in the performances of the TFT's by elevated thermal processing (> 300 ^{o}C) [13]. However, high anneal temperatures become a

constraint when the TFTs are grown on polymer-based flexible substrates, as they are sensitive to high temperatures.

To the best of our knowledge, improvement in the a-Si:H TFTs (fabricated at low temperatures) performance and high temperature stability with anneal time has not yet been investigated. This study reports the effect of different anneal times on the a-Si:H TFTs performance. The TFTs have been annealed at 150 °C for different times before any application of electrical stress. The stability and transfer characteristic of these TFTs were studied at temperatures ranging from room temperature to elevated temperatures as high as 125 °C. We have observed that the performance and stability of a-Si:H TFTs improves with longer anneals. For all TFTs under positive gate bias, the ΔV_t values follow a power law-dependence with time. It is seen that the life time of the TFT improves with longer anneals by a factor of 3 when compared to unannealed TFTs. Based on the variations of sub-threshold slope, mobility, and hysteresis with temperature; it has been inferred that the improvement in the stability is due to the reduction of interface trap density and good quality a-Si:H/insulator interface with anneal time.

3. 2. EXPERIMENTAL DETAILS

Amorphous-Si:H TFTs employed in this study have a bottom gate inverted staggered structure. Figure 3.1 shows the cross sectional schematic of the TFT. Bottom-gate inverted staggered structures were fabricated on flexible substrate like stainless steel and heat stabilized PEN

(Polyethylene Naphthalate) at 180 °C. First, the gate-metal molybdenum was deposited and patterned, followed by the deposition of silicon nitride (SiN_x), the a-Si:H active layer and n^+ amorphous silicon/ aluminum bilayer as source/drain contacts by plasma enhanced chemical vapor deposition. A nitride passivation layer is deposited before the drain/source contacts are etched. Finally after fabrication, the TFTs are annealed at 180 °C in nitrogen atmosphere for 3 hours. The width and length of all the TFTs in this study is 96 μm and 9 μm, respectively. To study the effect of anneal, the TFTs are annealed in 5 % H_2/Ar (reducing atmosphere) at 150 °C for 4, 8, 24, 48, and 96 hours. The bias-stress measurements are performed for up to 10^4 seconds and interrupted at regular intervals to measure the transfer characteristics. The source and the drain electrodes were grounded during the stress experiments. The TFTs were stressed with both positive (20 V) and negative (-20 V) gate bias voltage. Transfer characteristics were measured at source-drain voltage of 10 V and gate voltages from -20 V to 30 V. High temperature measurements were performed on a heating stage. The transfer characteristics were measured every 25 °C from room temperature to 125 °C. The threshold voltage is extracted from the intercept of the extrapolation of the linear region of the square root of I_{DS} vs V_{GS} with the horizontal axis using the following relation [14]:

$$I_{DS} = \left(\frac{W}{2L}\right) \mu_{FE} C_{ox} (V_{GS} - V_t)^2 \tag{1}$$

where W and L are width and length of the channel, μ_{FE} is the field effect mobility, C_{ox} is the capacitance per unit area, V_{GS} is the gate-source voltage and V_t is the threshold voltage. The μ_{FE} can be calculated using the following relation:

$$\mu_{FE} = \left(\frac{2L}{WC_{ox}}\right)\alpha^2 \tag{2}$$

where α is the slope of linear fit to the $I^{1/2}$ Vs V_{GS}. The sub-threshold slope is derived from the inverse of the maximum slope of the logarithmic scale I_{DS} vs V_{GS}. Subsequently, the stress induced shifts in these TFT electrical parameters as a function of stress time and gate-bias stress are determined.

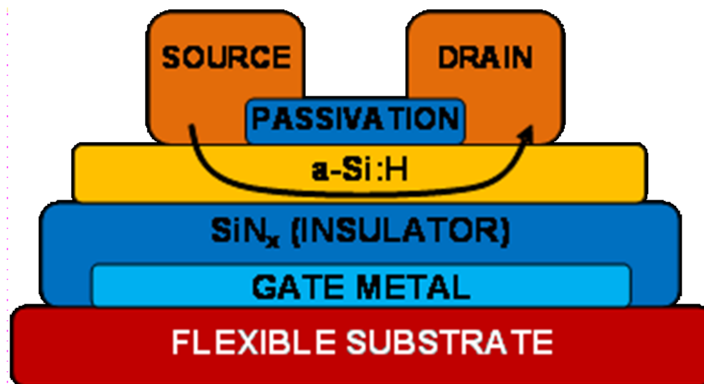


Figure 3.1 Schematic showing the cross sectional of the a-Si:H TFT. The arrow depicts the current flow through the a-Si:H layer

3. 3. RESULTS AND DISCUSSION

The performance of the TFTs are often limited by off-current and sub-threshold slope. The combination of these two parameters typically determines the on/off ratio of the devices. Figure 3.2 shows the variation of off-current and sub-threshold slope (*S*) with anneal time of TFTs. Here the sub-threshold slope becomes steeper with anneal times. The sub-threshold slope of the unannealed TFT is 1.5 V/decade and for 96 hour annealed TFT it improves to 0.54 V/decade. In addition, the off-current values reduces by two orders of magnitude with longer anneal times. The improvement in these parameters for the longer annealed TFTs when compared to values from unannealed TFTs is substantial. The *S* is mainly dictated by both deep localized states in the a-Si:H layer and interface states at the a-Si:H/SiN_x interface [15]. Figure 3.3 shows the band diagram of a-Si:H TFT under different bias conditions. At zero or very low positive gate voltage, the Fermi-level is in the middle of the band gap close to its intrinsic level; hence, most of the induced carriers go into either the deep localized states in the a-Si:H layer and/or into interface states. Only a very small fraction of electrons close to the front a-Si:H/insulator interface (interface near to the gate electrode) participate in the conduction. As the positive bias on the gate increases, the density of electrons increases and this leads to an exponential growth of current and subsequent transition to the above-threshold regime of operation.

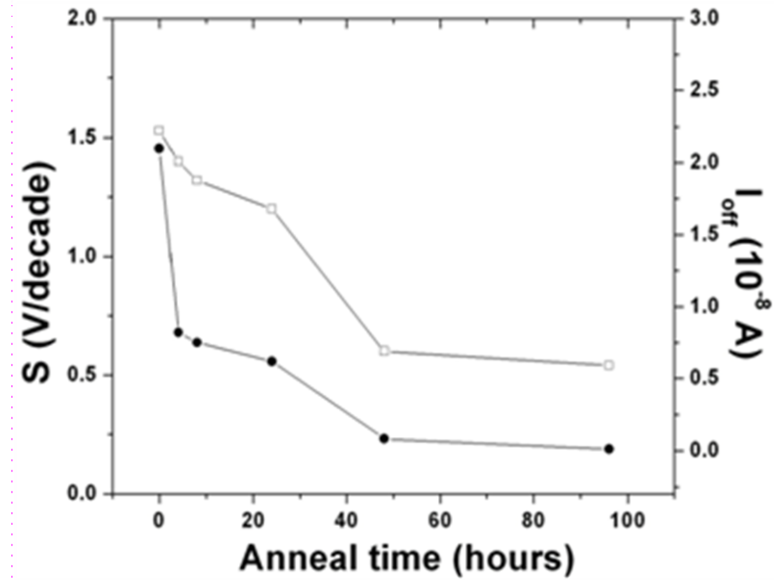


Figure 3.2 Variation of off-current and sub-threshold slope of the a-Si:H TFT with annealing times; (a) S (○), and I_{off} (●)

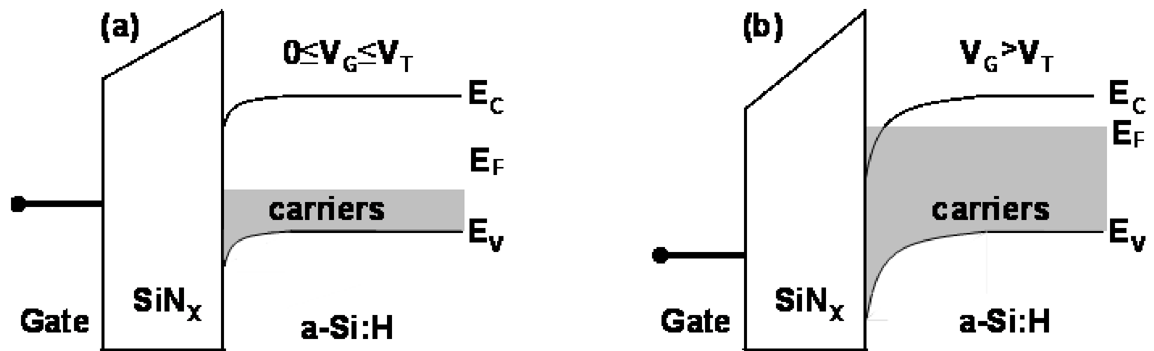


Fig. 3.3 a-Si:H TFT band-diagram under different gate-bias voltages: (a) for gate voltage less than the threshold voltage b) for gate voltage higher than the threshold voltage

Therefore increased anneal times result in a decrease in either the number of deep states in the a-Si:H layer or the interface trap states at the a-Si:H/SiN_x interface (improving the interface quality) and leads to a reduction in the off-current with a steeper sub-threshold slope.

To further investigate the effect of anneal time on the performance of the a-Si:H TFT, high temperature measurements have been performed at every 25 °C from room temperature to 125 °C. Figure 3.4 shows the variations of normalized sub-threshold slope (S/S_o) as a function of temperature for different anneal times; where, S_o is the slope at room temperature. As shown in the Figure 3.4, there is negligible increase in the S value with temperature for TFTs annealed for extended times (24, 48 and 96 hour annealed) when compared to the unannealed, 4, and 8 hour annealed TFTs. In the latter case, the S increases by a factor of 2.4 at 100 °C when compared to room temperature. However for 24, 48, 96 hour annealed TFTs, the S increases only by a factor of ~ 1.4 at 100 °C when compared to room temperature. Sub-threshold slope is largely decided by the quality of a-Si:H/SiN_x interface and localized state density near the interface. [12] The longer annealed TFTs display a stable S with temperature indicating a negligible degradation of the properties at the a-Si:H/SiN_x interface.

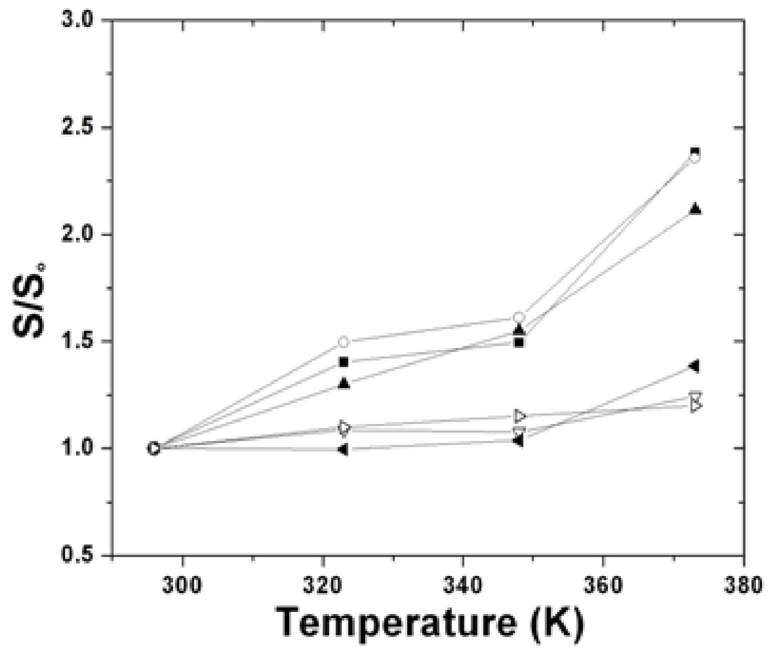


Fig. 3.4 Variations of normalized sub-threshold slope (S/S_o) with temperature for different anneal times; (a) unannealed (■), (b) 4 h annealed (○), (c) 8 h annealed (▲), 24 h annealed (▽), 48 h annealed (. ◄), and 96 hour annealed (▷)

Figure 3.5 shows the variations of field-effect mobility (μ) with temperature for different anneal times. As shown in Fig. 5 for the 24, 48, and 96 hour annealed TFTs, there is a gradual increase in μ from room temperature till 100 °C. The mobility increases (for 8, 24, 48, and 96 hour annealed TFT) from 0.5 $cm^2/V\text{-}s$ at room temperature to ~ 1 $cm^2/V\text{-}s$ at 100 °C. The increase in the mobility at higher temperatures suggests that the transport mechanism of the electrons in longer annealed TFTs is by multiple trapping model [16-17]. This model states that at high temperatures electrons move through the extended states of the conduction band tails and residing in the deep states. The transition between these two modes is due to the trap and thermal release, which causes increase in the electron mobility at high temperatures. In the multiple trapping model, the mobility varies exponential with temperature and is defined as [16-18]:

$$\mu = \mu_o exp\left(-\frac{E_A}{kT}\right) \quad (3)$$

where μ is field effect mobility, μ_o is the mobility prefactor, and E_A is the electron mobility activation energy. The 24 and 48 hour annealed TFTs have an E_A of 99 ± 7 meV and 110 ± 10 meV, respectively. This is the energy difference between conduction band edge and the Fermi energy, *i.e.* the average energy required to release the electron from the localized states to extended states [17, 19].

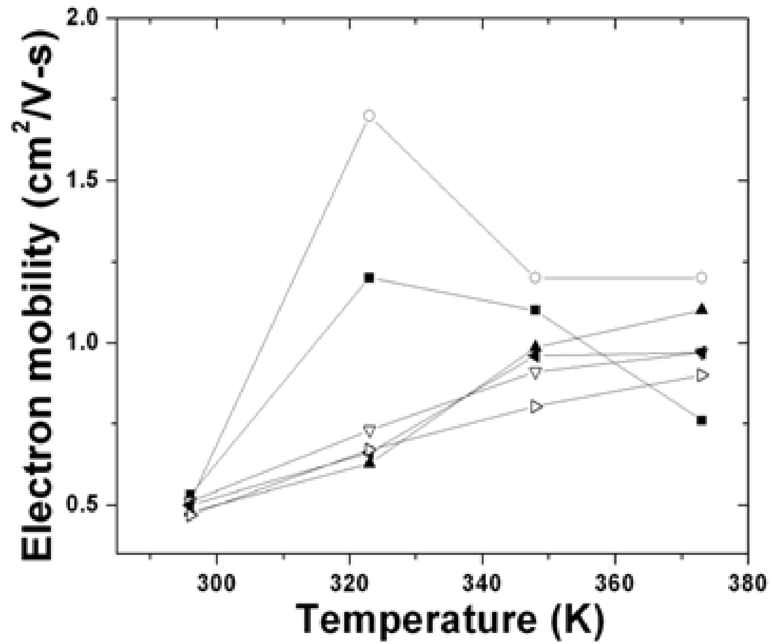


Fig. 3.5 Variations of field-effect mobility with temperature for different anneal times; (a) unannealed (■), (b) 4 h annealed (○), (c) 8 h annealed (▲), and 24 h annealed (▽), 48 h annealed (. ◀), and 96 hour annealed (▷)

However for unannealed and 4 hour annealed TFTs, the mobility has a maxima at 50 °C and then decreases at higher temperatures. As seen for unannealed TFT, the mobility increases from 0.5 $cm^2/V\text{-}s$ at room temperature to 1.7 $cm^2/V\text{-}s$ at 50 °C and it decrease at higher temperatures (> 50 °C). Based on this trend, it is apparent that there are two different mechanisms governing the mobility for unannealed and 4 hour annealed TFT. The sudden increase in the mobility value at 50 °C is due to the thermal activation of the electrons into the conduction band tail. Upon application of electric field, these electrons tunnel from one localized state to another. The drop in mobility at temperatures above 50 °C is likely due to the generation of more trap states as a result mobility starts decreasing with further increase in temperature. Lustig *et. al* [20] have also observed decrease in mobility in some of their TFTs for operation temperatures higher than 360 K. This indicates that ease of defect creation is difficult for longer annealed TFTs when compared to unannealed TFT. Hence for longer annealed TFTs, stable mobility along with stable *S* with temperature is likely due to the improvement in the interface quality [15].

Figure 3.6 shows the transfer characteristics of the unannealed a-Si:H TFT and 48 h annealed TFT at room temperature showing hysteresis. The transfer characteristics were recorded for both the forward sweep (-20 V to 30 V) and reverse sweep (30 V to -20 V) at drain-source voltage of 10 V. Curve *A* represents the forward sweep and curve *B*

represents the reverse sweep. This hysteresis obtained after sequential forward and reverse sweeps is due to electron trapping in the a-Si:H channel at the interface. This hysteresis is an important parameter which affects the OLED current resulting in poor display quality in the AMOLED application. The display quality can be improved by reducing the interface trap density in the TFT [21]. Figure 3.7 shows the variation of hysteresis with temperature for different anneal times. For all the TFTs, hysteresis increases with increase in temperature. This indicates that more charge is trapped at high temperatures [17]. However, the hysteresis is small for longer annealed TFTs when compared to unannealed TFT. Those TFTs annealed for 48, and 96 hours show a hysteresis of ~ 4.8 V when compared to 9 V of unannealed TFT at 100 °C. Hence it is seen that longer anneal times does help in the reduction the hysteresis by lowering the interface traps and improving the quality at the a-Si:H/insulator interface.

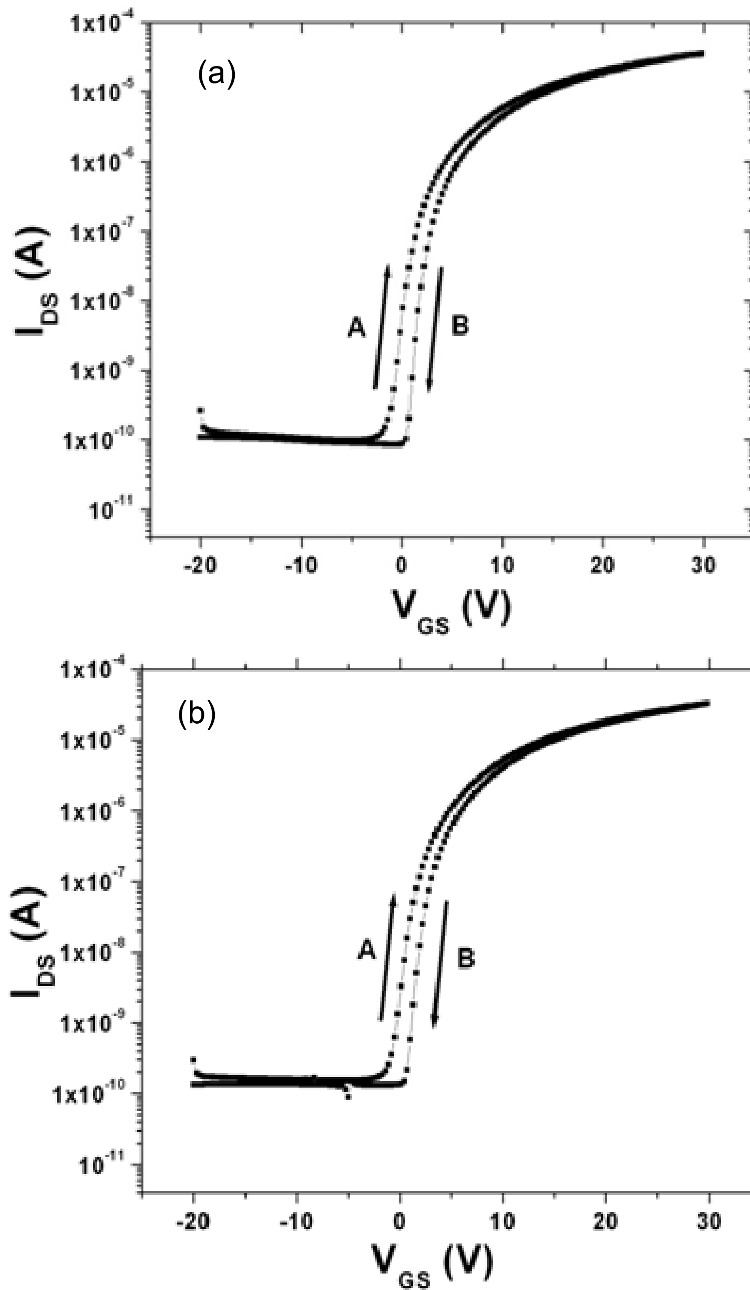


Fig. 3.6 Transfer characteristics (at V_{DS} = 10V) of (a) unannealed, and (b) 48 h annealed a-Si:H TFT at room temperature showing hysteresis

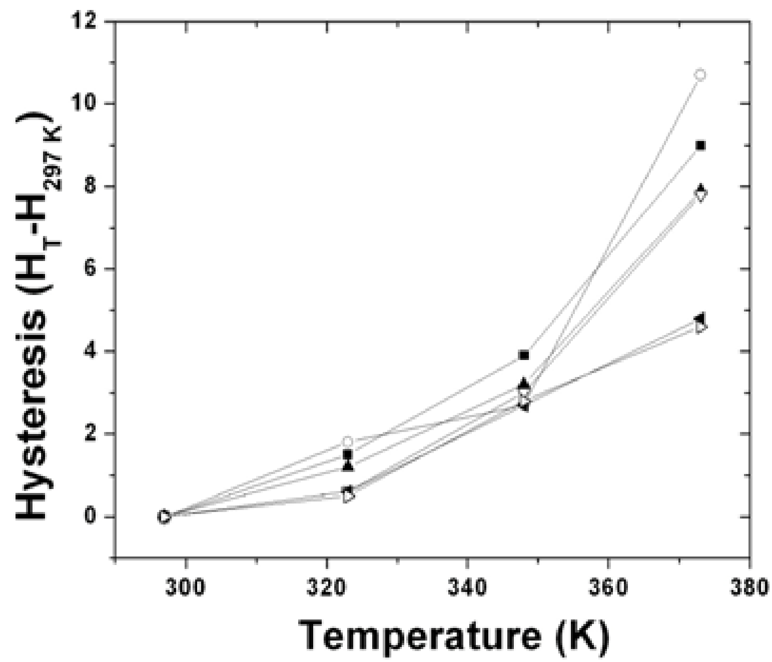


Fig. 3.7 Variations of hysteresis with temperature for different anneal times; (a) unannealed (■), (b) 4 h annealed (○), (c) 8 h annealed (▲), 24 h annealed (▽), 48 h annealed (▷), and 96 h annealed (◀)

Figure 3.8 shows the I_{DS}-V_{GS} plot for unannealed a-Si:H TFT at V_{DS} of 10 V over a temperature range from 25 to 125 °C. The variation of drain current with temperature in the saturation region is quite different. At temperatures below 100 °C, the drain current in the saturation region ($I_{DS,Sat}$) increases with increasing temperature. However above this temperature, $I_{DS,Sat}$ starts decreasing with increasing temperature. This behavior at higher temperatures is due to charge trapping in the localized states in the mobility gap of a-Si:H, into the insulator or at the a-Si:H/insulator interface resulting a reduction in the $I_{DS,Sat}$ [18]. Similar behavior is seen for all the TFTs annealed for different times. The TFTs fabricated at low temperatures have a less stable gate insulator due to a substantial amount of trapped charge inside the insulator [22]. The trapped charges are themionically excited at high temperatures which results in increase in the off-current. Figure 3.9 shows the Arrhenius plot of off-current with temperature for all the TFTs. This temperature dependence of off-current indicates that the leakage mechanism is dominated by Poole-Frenkel emission [23]. The longer anneal times show much lower leakage current when compared to unannealed TFT at even elevated measurement temperatures. This indicates that longer anneal times promote the reduction of the trapped charge inside the insulator for low-temperature fabricated TFTs. Therefore, longer anneals of these TFTs improved the high temperature stability along with reduction in the trapped charges inside the insulator.

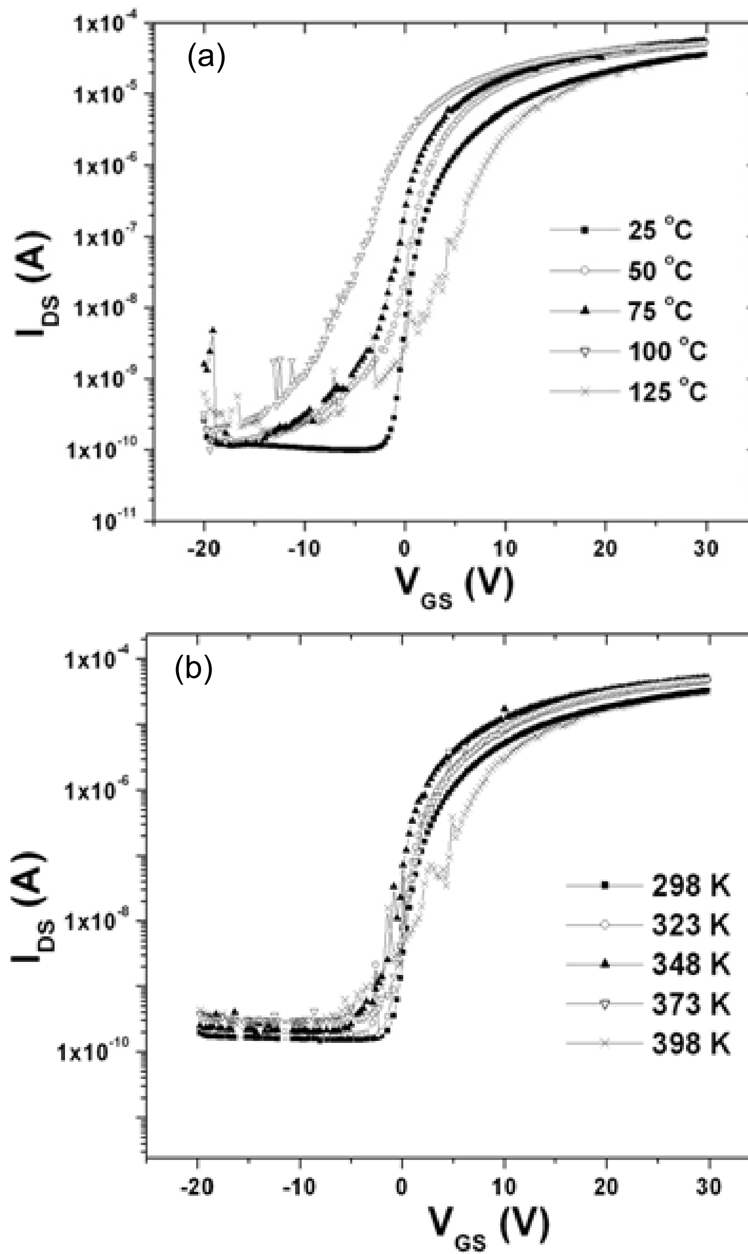


Fig. 3.8 I_{DS}-V_{GS} plot of (a) unannealed, and (b) 48 h annealed a-Si:H TFT at V_{DS} of 10 V over a temperature range from 25 °C to 125°C

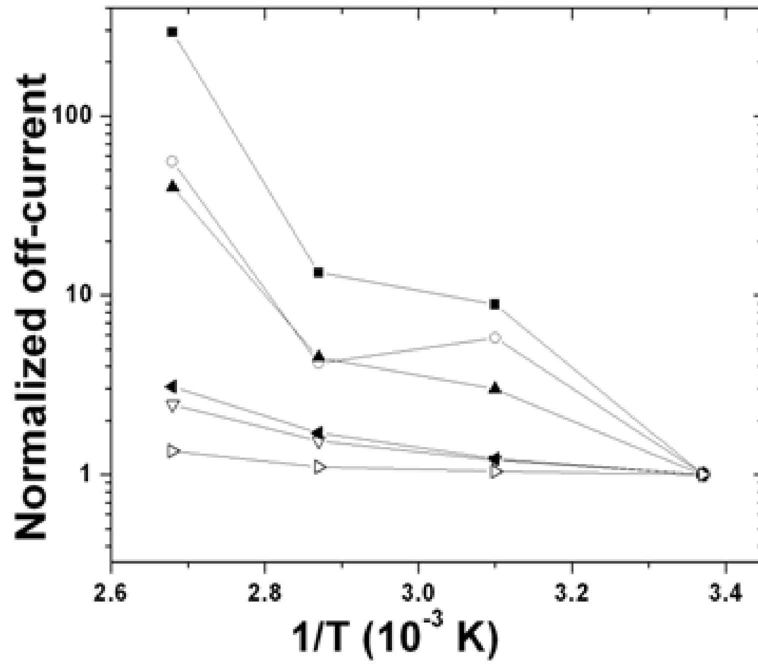


Fig. 3.9 Arrhenius plot of off-current with temperatures for all the TFTs; (a) unannealed (■), (b) 4 h annealed (○), (c) 8 h annealed (▲), and 24 h annealed (▽), 48 h annealed (◀), and 96 h annealed (▷)

Figure 3.10 illustrates the variation in ΔV_t with the bias stress time for different anneal times at a gate-bias stress of 20 V. For the positive gate-bias stress (Fig. 10), the threshold voltages are all positively shifted and increases with bias stress times. In both unannealed and annealed TFTs, the ΔV_t exhibits power-law time dependence and suggests that the dominant instability mechanism is state creation [24]. The state creation is attributed to the density and occupancy of the band tail states and hydrogen dispersion. The threshold voltage shift due to state creation is given by the following relation [23]:

$$\Delta V_t \sim t^{\beta} \tag{4}$$

where β is a constant for a given gate bias stress. Figure 3.10 shows the ΔV_t data has a straight line fit with time for different anneal times. The ΔV_t data fits well to this equation for different β values corresponding to different anneal times. The straight line fits to unannealed, 4 h annealed, 8 h annealed, 24 h annealed, 48 h, and 96 h annealed TFTs have β values of 0.6, 0.54, 0.54, 0.49, 0.4, and 0.37 respectively. These values are in good agreement with the literature [23,25-26]. The reduction in the β value from 0.6 for unannealed to 0.37 for 96 h annealed TFT indicates improvement in the properties of the a-Si:H channel and/or the a-Si:H/insulator interface. Extrapolating this straight line fit to ΔV_t = 10 V for all the TFTs show a significant increase in the life time of 96 h annealed

TFT when compared to unannealed TFT. The 96 h annealed TFTs takes ~ 3 times more time to reach ΔV_t value of 10 V when compared to unannealed TFTs. This substantiates the high temperature results that longer annealed TFTs improves the quality of a-Si:H/insulator interface as a result there is significant enhancement in their performance and stability. Anneals for longer times are beneficial for TFTs that are fabricated at low temperatures on flexible polymer substrates. This process improves the stability of these TFT by reduction of the trapped charges inside the insulator and obtainment of a better a-Si:H/SiN_x interface.

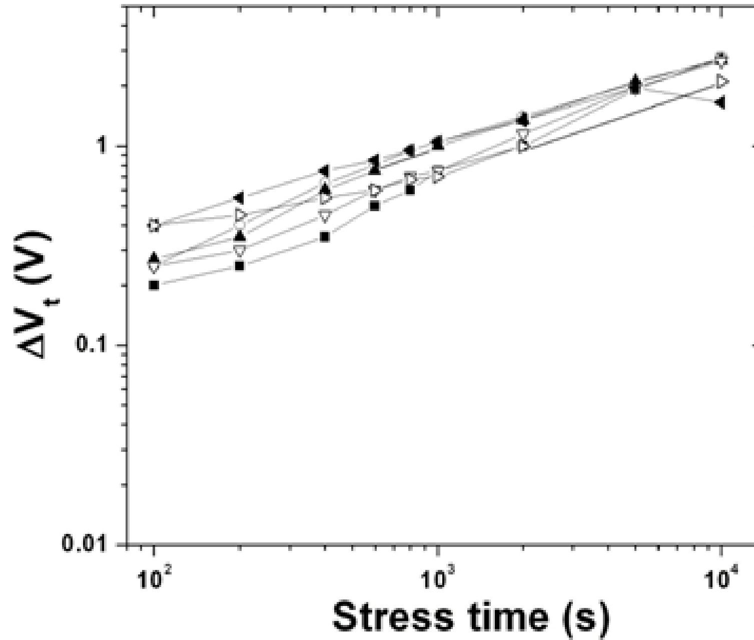


Fig. 3.10 Threshold voltage shift (ΔV_t) with the stress time for different anneal times at gate bias stress of 20 V; (a) unannealed (■), (b) 4 h annealed (○), (c) 8 h annealed (▲), and 24 h annealed (▽), 48 h annealed (◄), and 96 h annealed (▷)

3. 4. CONCLUSION

In conclusion, low temperature fabricated a-Si:H TFTs annealed for longer times showed significant temperature stability along with improvements in sub-threshold slope, hysteresis, and off-current when compared to unannealed TFTs. For 96 h annealed TFTs, values of off-current is reduced by two orders of magnitude and sub-threshold slope are steeper with longer annealing. The TFTs annealed for 96 hours showed a stable sub-threshold slope value (increases by a factor of ~ 1.4 at 100 °C) with temperature and have a low hysteresis when compared to unannealed TFTs measured at higher temperatures. Both for annealed and unannealed TFTs at positive gate bias, the ΔV_t exhibits power-law-time dependence indicating state creation with reduction in β value from 0.6 to 0.37 and thereby improving the life time of the TFTs. A stable value of *S* with temperature indicates significant improvement in the quality at the a-Si:H/SiN_x interface with less interface trap density. Hence, annealing for longer times improves the performance of the TFTs.

Chapter 4

IMPACT OF LOW TEMPERATURE, LONG-TIME ANNEALS ON THE TEMPERATURE INSTABILITY OF IZO THIN FILM TRANSISTORS

4. 1. INTRODUCTION

Metal oxide (MO) semiconductors have attracted much attention and are a strong candidate for replacing hydrogenated amorphous silicon as the dominant thin film material for emerging electronic devices. [1-3] They can be potentially used in large liquid crystal displays, and in the active matrix backplane of organic light emitting diode displays because of their high mobility, excellent uniformity, and transparency to visible light, when compared to conventional amorphous silicon. [4-5] A number of different metal-oxide-semiconductors TFTs such as zinc oxide (ZnO), indium zinc oxide (IZO), and indium gallium zinc oxide (IGZO) fabricated at low temperatures have been investigated. [6-9]

It is well known that fabrication of these TFTs at such low temperatures can generate a high defect density in the band gap due to their complex nature. [10-11] These defects can lead to potential problems: instability and poor performance of these mixed oxide TFTs. It has been previously reported that the performance and stability of the gallium indium zinc oxide (GIZO) TFTs can be improved by curing these defects by long-time anneals. [11] Jung *et al.* have improved the performance of GIZO TFTs by post thermal annealing at 250 °C. Up to

now, the performance of the MO TFTs has been improved by annealing them at elevated temperatures. [11-12] This is a constraint when the TFTs are fabricated on polymer-based flexible substrates, as they are sensitive to such high temperatures. Low-temperature long-time anneals can be a useful technique to improve the performance of these MO TFTs are fabricated on polymer substrates. To the best of our knowledge, improvement in the IZO TFTs (fabricated at low temperatures) performance and high temperature stability with low-temperature long-time anneals has not yet been reported. Moreover to date, most of the stability investigations have concentrated on electrical bias stress over extended periods of time. [13-15] However, there have been very few studies reporting on the performance and stability of these TFTs at elevated operation temperatures. [16-17] Due to the defects in these low-temperature deposited MO semiconductors, investigation of these TFTs at elevated temperatures can provide a further insight on the instability mechanisms.

In this chapter, we report the stability and performance improvement by low-temperature long-time anneals of IZO TFTs. Low-temperature long-time anneals have also been used as a tool to understand the instability mechanism at elevated operation temperatures. These long-time anneals improve the stability of TFTs by a reduction of the interface trap density, and curing the defects in the semiconductor (formed during low temperature fabrication).

4.2. EXPERIMENTAL DETAILS

Indium-zinc-oxide TFTs in this study have a bottom gate inverted staggered structure. Figure 4.1 shows the cross-sectional schematic and an optical micrograph of a TFT fabricated at 180 °C on a 300 mm diameter silicon wafer covered with a thin layer of SiO_2. First, the gate metal molybdenum is sputtered and patterned, followed by depositions of SiO_2 and IZO layers at temperatures between 180 °C and ~ 80 °C, respectively. The IZO layers are sputter deposited at a The IZO layers are sputter deposited at a pressure of 16 mTorr and power density of 0.66 W/cm^2. The gas ratio (oxygen/argon) of 1/50 was used with a total gas flow of 204 sccm. The SiO_2 layers are deposited by PECVD at a pressure of 1.5 Torr (35 sccm silane and 3 sLm nitrous oxide) using a power density of 0.43 W/cm^2. Both the IZO and SiO_2 layers are patterned with conventional photolithography and then molybdenum is sputtered to form source/drain contacts. Finally, the TFTs are annealed at 180 °C in a nitrogen atmosphere for 1 h. The entire fabrication process is also compatible with flexible polymer substrates as the maximum process temperature is 180 °C. For this study the IZO TFTs were annealed at 150 °C for various times before any electrical stress. The stability and transfer characteristics of these TFTs were characterized at temperatures ranging from room temperature to 100 °C on arrays of TFTs with width/length (*W/L*) of 96/9. The TFTs were stressed with a positive gate bias of 20 V for up to 10^4 s. The source and the drain electrodes were grounded during

the stress experiments. All measurements were made in the dark using a HP4155B semiconductor parameter analyzer.

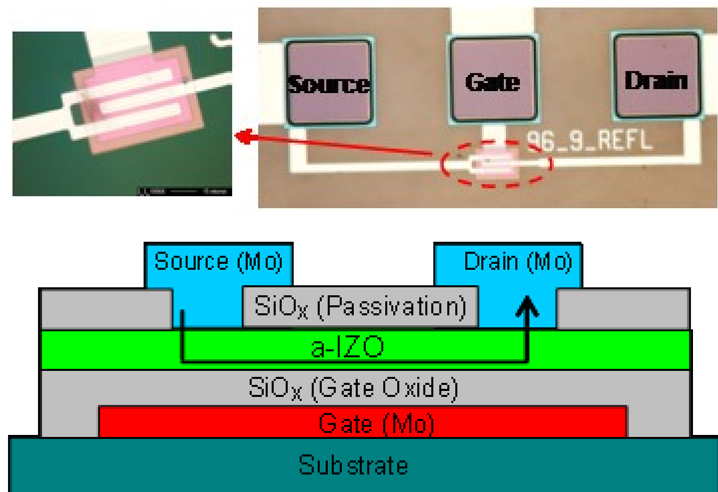


Figure 4.1 (a) Optical image of the transistor with *W/L* equal to 96/9; (b) Schematic showing the cross sectional of the IZO TFT test structure. The arrow depicts the current flow through the IZO layer.

4.3. RESULTS AND DISCUSSION

Figure 4.2 shows the output characteristics of a typical unannealed TFT. The lack of current crowding at low source-drain biases indicates a good ohmic contact. These TFTs operate as depletion-mode, *n*-channel devices, as a negative gate voltage has to be applied to turn the device off. The linear mode mobility (μ) was calculated from the following equation: [18]

$$\mu = \frac{g_m L}{W C_{ox} V_{DS}} \quad (1)$$

where g_m is the transconductance calculated in the linear region (V_{GS} = 20 V and V_{DS} = 10 V), and C_{ox} is the oxide capacitance/unit area. These devices exhibit mobilities of 5-6 cm^2/V-s and sub-threshold swings of 1-1.25 V/decade. The typical I_{on}/I_{off} ratio is 10^6. The off-state source-drain leakage currents are on the order of 10^{-11} A. As the threshold voltage is not clearly defined in these devices, the turn-on voltage, V_{ON}, is used instead of threshold voltage. [19-21] The turn-on voltage is determined from log(I_{DS}) vs. V_{GS} plots. It is defined as the value of V_{GS} corresponding to the onset of the initial sharp increase in I_{DS} as shown in Figure 4.3. [19]

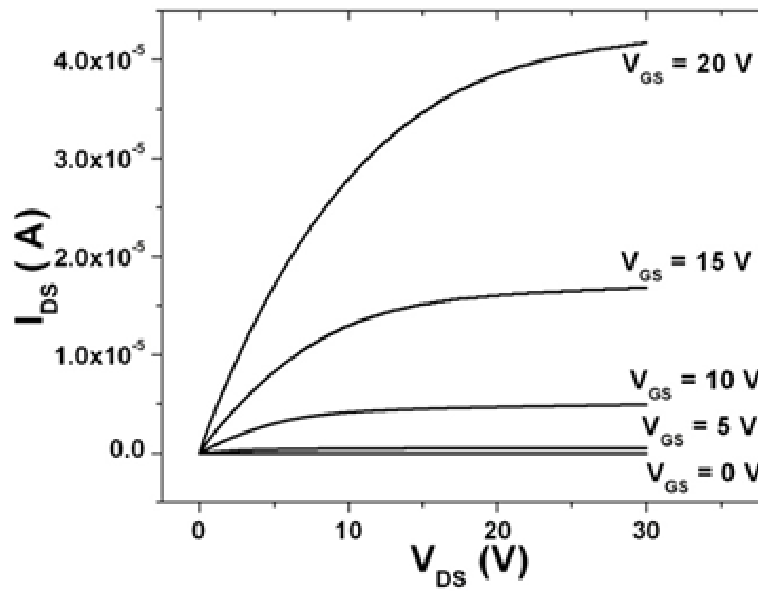


Figure 4.2 Output characteristics of a typical as-fabricated IZO TFT.

Figure 4.3 show the transfer characteristics for the unannealed and 48 h annealed TFTs after a +20 V gate-bias stress for different stress times. There is a near-parallel shift of the transfer characteristic in the positive gate voltage direction following the positive bias stress. The turn-on voltage shifts by 2.4 V (unannealed TFT), and 1.8 V (48 h annealed TFT) after 10^4 s stress. Jung *et. al* [11] have also seen improvements in their GIZO TFTs after 65 h post thermal anneals at 250 °C. The threshold voltage shift in their TFTs reduced from 8.6 V (65 h post thermal anneal) to 2.2 V (for as fabricated TFT) after 1 h positive bias stress.

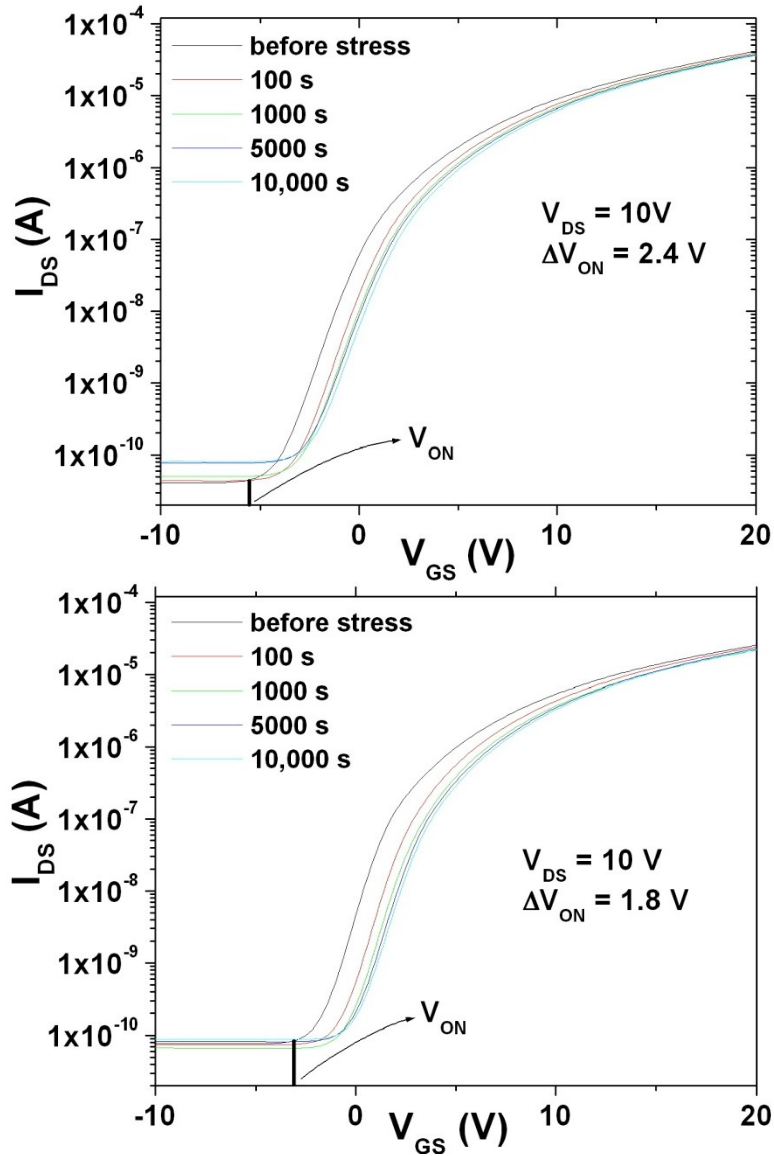


Figure 4.3 Transfer characteristics of unannealed and 48 hour annealed IZO TFTs for different bias stress times. Applied gate bias stress = 20 V; (a) unannealed TFT, and (b) 48 hour annealed TFT.

Figure 4.4 shows the variation of sub-threshold swing (*S*) with bias stress time. There is degradation in *S* at longer stress times. It has been previously reported that the positive shift in the turn-on voltage with bias stress time indicates negative charge trapping as the dominant instability. [22] However, the degradation in *S* for longer stress time indicates interface trap creation. [23] As shown in Figure 4.4, *S* is almost constant for the first 1000 s and starts increasing for later stress times. This indicates that after 1000 s stress, both interface trap creation and charge trapping can be possible reasons for the instability mechanism. The reduction in the turn-on voltage shift for longer annealed TFTs compared to the unannealed TFTs is ascribed to a reduction in the interface trap density at the semiconductor/insulator interface.

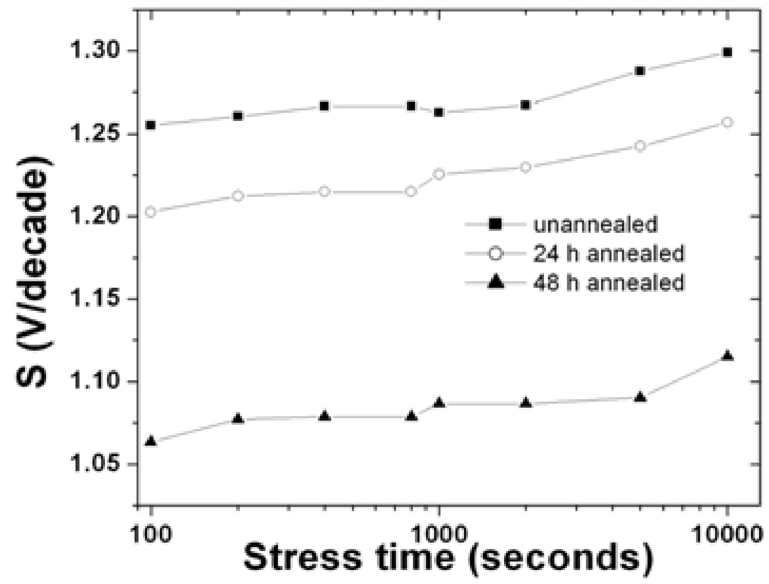


Figure 4.4 Variation of normalized sub-threshold swing with bias stress time for different anneal times.

To further explore the degradation mechanisms, our annealed TFTs are measured at elevated temperatures. Figure 4.5 shows the variation of turn-on voltage shift with operation temperature for different anneal times. The unannealed TFTs have an unstable turn-on voltage when operated at elevated temperatures. There is a sharp dip in turn-on voltage at ~370K for unannealed TFTs. Raising the operation temperature from room temperature to 370K shifts the turn-on voltage by approximately 15 V from -3 to -18 V. A similar drop in turn-on voltage (by ~3.5 V) is observed for 24 h annealed TFTs. However, 48 h annealed TFTs show a stable turn-on voltage even at high operation temperatures. Figure 4.6 shows the changes in the normalized sub-threshold swing (S/S_o) with operation temperature for different anneal times and for ideal case (S~kT/q). The ideal case considered here is for the increase in *S* due to increase in the temperature, ignoring any change in the interface trap density with temperature. There is an increase in *S* as the operation temperature increases. This increase in *S* with operation temperature is higher when compared to the ideal case, indicating that the increase in *S* with temperature is due to extra interface trap density generated at higher temperatures. However, the relative increase in *S* is lower for 48 h annealed TFTs. Both turn-on voltage and *S* are degraded at elevated operation temperature.

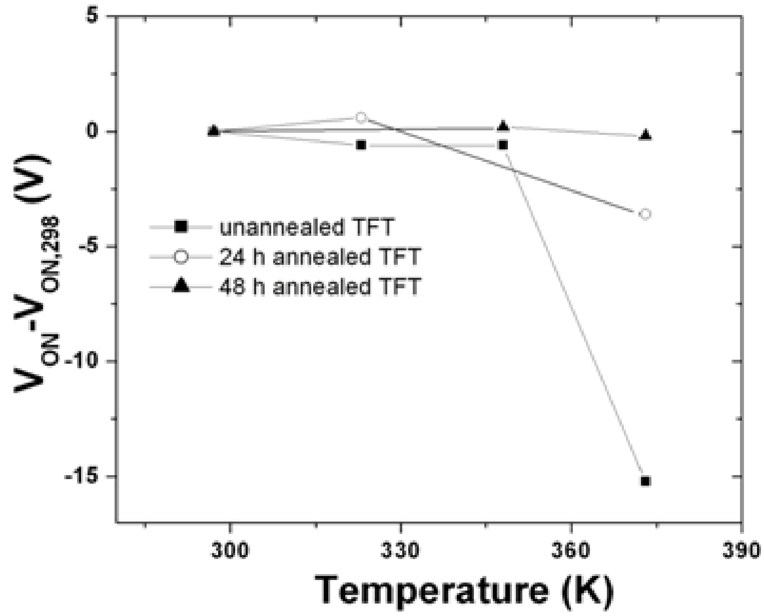


Figure 4.5 Effect of operation temperature on the turn-on voltage for different anneal times.

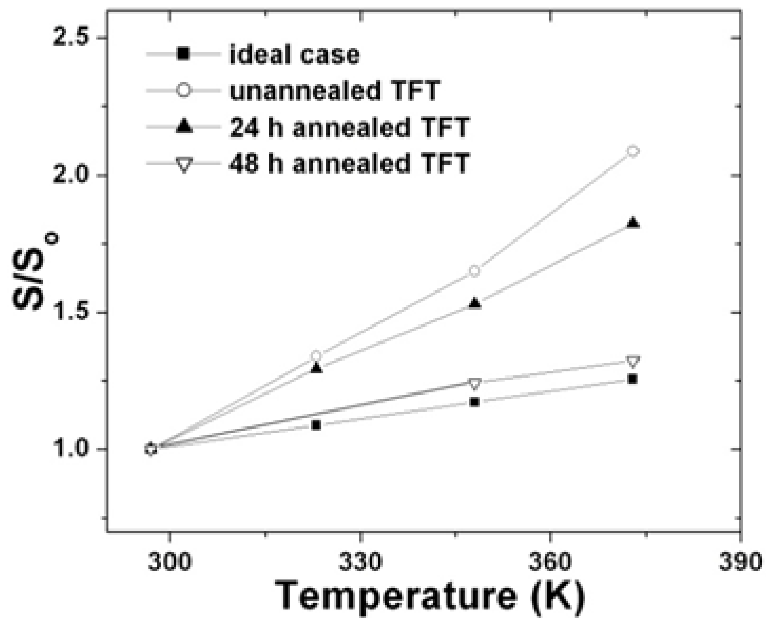


Figure 4.6 Effect of operation temperature on the sub-threshold swing for different anneal times.

It has been previously reported that the increase in the S and the instability with elevated operation temperatures is due to an increase in the interface trap density. [16-17] Jung *et. al* [11] have reported stability improvement of their GIZO TFTs after long-time post annealing and have ascribed the improvement to curing of the defect states in the GIZO channel layer. However, due to the complex nature of the metal-oxide TFTs, their instability with temperature cannot be explained only based on the temperature assisted charge trapping/de-trapping at the interface or/and in the insulator. The increase in the S with operation temperature could be due to an increase in the interface trap density with temperature. The interface trap density at the semiconductor/insulator interface was estimated by the following relation: [24]

$$S = 2.3\frac{kT}{q}\left(1 + \frac{qN_{it}}{C_{ox}}\right) \rightarrow N_{it} = \left(\frac{S\log(e)}{kT/q} - 1\right)\left(\frac{C_{ox}}{q}\right) \quad (2)$$

where k is Boltzmann's constant, T is the operation temperature, and q is the carrier charge. For unannealed TFTs, values of N_{it} are ~1.55×10^{12} cm^{-2} at room temperature. The N_{it} values range from 3-4×10^{12} cm^{-2} at high operation temperatures. Long-time annealed TFTs have N_{it} of ~ 2×10^{12} cm^{-2} at 370K. Based on these values, we propose that the interfacial quality of these devices becomes better with long-time anneals. However, the change in the turn-on voltage shift with operation temperature cannot

be explained based on the increase in the interface trap density. We suspect that defect states in the IZO play a role at elevated temperatures. As the operation temperature increases, the trapped electrons in these defect states are released and form a channel; hence, a large negative gate/source voltage has to be applied to pinch off the channel completely. The induced charge density in the channel layer (N_T) corresponding to the turn-on voltage (V_{on}) is given by the following relation: [25]

$$N_T = \frac{C_{ox} V_{on}}{qt} \tag{3}$$

where t is the thickness of the IZO channel layer. For unannealed TFTs, values of N_T are ~ 4.2×10^{16} cm^{-3} and ~ 2.6×10^{17} cm^{-3} at room temperature and 370K, respectively. This charge is ascribed to delocalized electrons from the shallow donors in the IZO channel layer. For the unannealed TFTs, electrons in the shallow donor defect states are thermally excited at 370K and form a channel. [26-27] A large negative gate/source voltage has to be applied to turn off the device. As shown in Figure 4.5, at 370K a gate/source voltage of less than -15 V has to be applied to turn off the device compared to that at room temperature. The TFTs annealed for 24 h show a smaller dip at 370K compared to unannealed TFT. Further long-time anneals for 48 h make the TFTs more stable without any appreciable change in the turn-on voltage compared to the unannealed and 24 h

annealed TFTs. For 48 h annealed TFTs, values of N_T are ~ 4.5×10^{16} cm^{-3} and ~ 3×10^{16} cm^{-3} at room temperature and 370K, respectively. We believe that a fraction of the shallow donor defect states in the IZO channel layer are cured by annealing the TFTs for long times. Hence, low-temperature, long-time anneals not only improve the electrical performance; but also improve their stability at elevated operation temperatures. Anneals for longer times are also beneficial for TFTs that are fabricated at low temperatures on flexible polymer substrates.

4. 4. CONCLUSION

In conclusion, the effect of low-temperature long-time anneals on the stability of the low-temperature fabricated IZO TFTs is investigated. The electrical performance and elevated temperature stability of these TFTs has been improved by low-temperature, long-time anneals. The poor stability at elevated operation temperatures of the as-fabricated TFTs has been significantly improved after 48 h post-annealing at 150 °C. The 48 h annealed TFTs show a stable turn-on voltage, and sub-threshold swing compared to the unannealed TFT at elevated operation temperatures. For a positive bias stress period of 10^4 s, the turn-on voltage shifts by only 1.8 V for the 48 h annealed TFTs when compared to 2.4 V for the unannealed TFTs. This improvement is attributed to the reduction in trap density at the semiconductor/insulator interface, and curing of defects states in the wide band gap of IZO.

Chapter 5

EFFECT OF MECHANICAL AND ELECTRO-MECHANICAL STRESS ON FLEXIBLE A-ZIO TFTS

5. 1. INTRODUCTION

Amorphous zinc indium oxide (a-ZIO) TFTs are a strong candidate for replacing amorphous silicon as the dominant thin film device for large area electronics (LAE) [1-2]. Large area electronic devices need to be rollable and able to withstand mechanical strain in bent condition. The potential applications include X- ray detectors, neutron detectors, smart medical bandages, *etc*. For these applications organic polymers like poly-ethylene napthalate (PEN) is used as deformable substrates. Thus, it becomes important to study the effect of mechanical stress on the electrical properties of the devices. Studies of mechanical stress on a-Si:H have been previously reported [3-5]. Although extensive studies of gate bias stress have been reported [6-8], to the best of our knowledge mechanical stress of ZIO TFTs has not been reported yet.

In this study we investigate the effects of mechanical (and combined electro-mechanical stress) on ZIO TFTs, considering both compressive and tensile strain, being applied parallel to the conducting channel length of the TFTs. We report the variation of sub-threshold slope (S), mobility (μ) and off state current (I_{off}) with mechanical stress in subsequent sections.

5. 2. FABRICATION PROCESS

The TFTs have a bottom gate staggered structure on PEN (having a thickness = 125 μm) with sputtered molybdenum gate (thickness being 150 nm). A stack of SiO_2 (100 nm), ZIO (50 nm) and SiO_2 (100 nm) is deposited next. The ZIO deposition is done between 77 and 91 °C and top layer of SiO_2 is deposited at 200 °C. The ZIO is patterned and molybdenum is sputtered to form source/drain contacts, followed by inter-layer dielectric (ILD) deposition. Indium-tin-oxide (ITO) is patterned as connecting metal to the electrophoretic material in an active matrix display. Lastly, wafers are annealed at 200°C for 1 hour. A detailed description of the process can be found in [6]. Fig. 5.1 shows the schematic of the device.

Arrays of TFTs with *W/L* equal to 96/9 were fabricated. An average threshold voltage (V_{th}) of -0.4V, saturation mobility varying between 4.5-5.5 cm^2/Vs and a sub-threshold swing variation of 0.61-0.81 V/dec was obtained with the TFTs. The typical I_{on}/I_{off} ratio was 10^6.

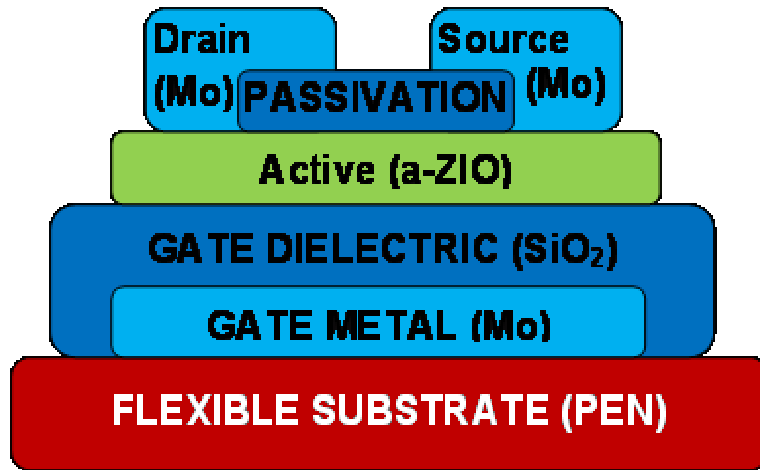


Figure 5.1 Schematic of a-ZIO TFTs test structure.

5. 3. RESULTS AND DISCUSSION

The processed TFTs on PEN were cut into cylindrical shape and were later rolled around various radii tubes. All the measurements were made with a HP 4155B semiconductor parameter analyzer. Since all bending was done on cylindrical surfaces, the stress was essentially uniaxial. Tensile stress was obtained by bending the devices outward, while compressive stress was obtained by bending them inward. For electromechanical stress the flexible substrate with TFTs were rolled around the cylindrical surface and taped at the ends while taking the measurements. The largest and smallest diameters in our experiment were 11.43 and 1.52 cm, respectively. All I-V characteristics were measured with gate to source bias (V_{GS}) varying from - 20 to 20 V at a constant drain to source bias (V_{DS}) = 10 V and 1 V. The off state current (I_{off}) was calculated as the least current value for V_{DS} = 10 V. The linear mode mobility (μ) for both the virgin devices and stressed ones (V_{GS} = 20 V and V_{DS} = 1 V) was calculated from the following equation:

$$\mu = \frac{g_m (= \partial I_d / \partial V_{GS})}{(W/L) C_{ox} V_{DS}} \tag{1}$$

where g_m is calculated in the linear region and C_{ox} is the oxide capacitance per unit area. All measurements were taken in 3 sets and

then averaged to reduce possible errors. All bending radii (R) are converted to % strain (ε) using the formula [9]:

$$\varepsilon = \left(\frac{1}{R}\right)\frac{d_f + d_s}{2}\left(\frac{\chi\eta^2 + 2\chi\eta_1 + 1}{\chi\eta^2 + (1+\chi)\eta + 1}\right) \tag{2}$$

where d_f and d_s are the corresponding thicknesses of the film (including all layers in Fig. 1) and the PEN substrate. Y_f and Y_s are the respective Young's modulii. Values of Y_f and Y_s are 145 GPa [10] and 5.5 GPa [11]. Also $\chi = Y_f/Y_s$ and $\eta = d_f/d_s$.

Fig. 5.2 shows the change in sub-threshold swing (S) and μ, when the TFTs were subjected to parallel stress, both tensile and compressive. For both cases the same TFTs were bent for 5 minutes successively on cylindrical surfaces in descending radius and then probed on a flat surface in between the bending, to measure their electrical characteristics. For a given stress the change in the electrical parameters remained constant during the time of measurement (about 1 min). S_0 and μ_0 denotes the slope and mobility of the virgin device. While S showed a reduction, μ showed an increase as the tensile stress increased by bending TFTs across smaller radii. Reverse changes were obtained for compressive stress. These effects are similar to that obtained for a-Si:H [3-5], although the magnitude of variation was found smaller in the present case.

Fig. 5.3 shows the I_{off} for both compressive and tensile stress. Here I_{off0} denotes the off current for the virgin device. The I_{off} decrease is again much more for tensile stress than compressive stress. These changes are not permanent and the I-V characteristics have been found to revert back to the virgin characteristics, when left for unstressed in flat conditions for sufficiently long period of time (*i.e.* more than a day).

The cause of these changes is not clear and is possibly due to change in band-gap and/or defect creation at the interface [4]. Density of defect states (tail states) (D_{it}) was found to reduce (increase) with uniaxial tensile (compressive) stress [12-13] for a-Si:H. Density of defect states has been demonstrated to be inversely proportional to the slope of activation energy (E_a) w.r.t V_{GS} [13]. To measure E_a we obtained I_{DS}-V_{GS} curves for different temperatures, from 25°C to 125°C, at an interval of 25°C and plotted log(I_{DS}) vs 1000/T, for different V_{GS}.

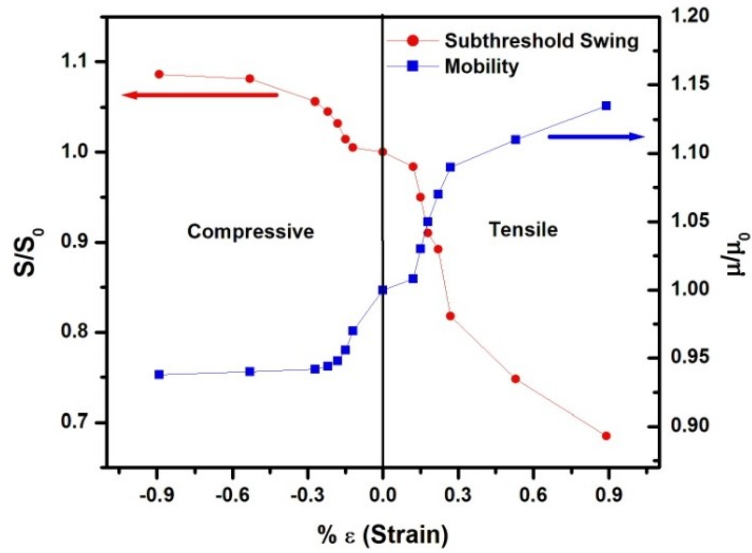


Figure 5.2 Relative S and μ as function of the applied strain (ε). V_{GS} varying from - 20 to 20 V.

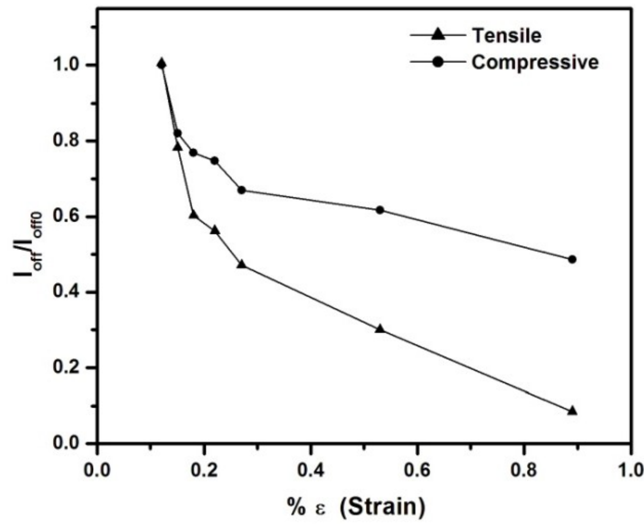


Figure 5.3 Relative I_{off} due to tensile and compressive stress vs % strain (ε). V_{GS} varying from - 20 to 20 V at V_{DS} = 10V.

Fig. 5.4 shows the E_a as a function of V_{GS}, for the virgin, tensile stressed and compressively stressed TFTs.

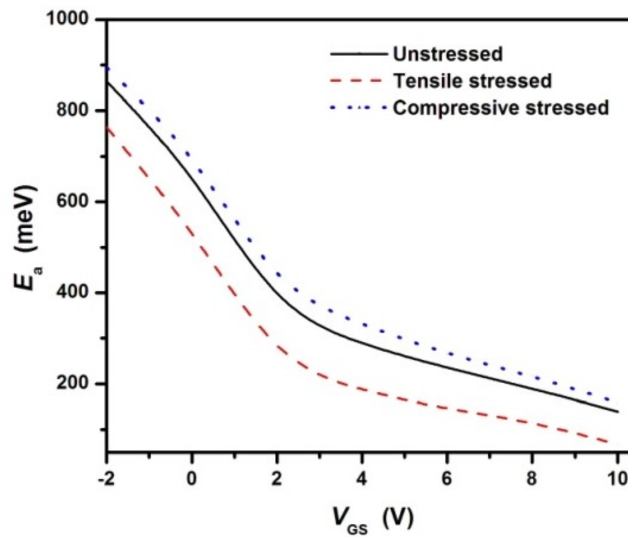


Figure 5.4 Activation energy vs gate bias (bending diameter = 5.08 cm, ε=0.27%).

The slope of E_a was found to be more (less) for tensile (compressive) stress compared to the E_a for unstressed device, indicating a decrease (increase) in D_{it} for tensile (compressive). Increase in D_{it} increases S and reduces μ via charge trapping. Mobility in presence of charge trapping is given by [14]

$$\mu = \mu_0 \left(\frac{t_{free}}{t_{trap} + t_{free}} \right) \tag{3}$$

where t_{free} and t_{trap} are the average time spent by carriers in free and trap states respectively and μ_0 is the free electron mobility. Also smaller (larger) E_a implies a smaller (larger) Urbach energy (which is the valence band tail slope) [15], in general. Because tail states are associated with network disorders, such as bond angle and length distortion, there is a possible correlation of the conduction band tail state and Urbach energy, as shown for a-Si:H [16], *i.e.* a smaller (larger) Urbach energy implies smaller (larger) tail states. So measurement of E_a or Urbach energy confirms that tensile stress reduces defect states. This reduction in conduction band tail states implies higher (lower) linear electron mobility [17] by (3). Hence is the observed result. Moreover it has been found that for a-Si:H the Urbach energy increases with decrease in band-gap [18], which in turn decreases with compressive stress [19]. Increased Urbach energy results in increased conduction band tail states, which in turn

implies lower mobility. Thus reduction in band-gap might also be cause of mobility reduction under compression. Similar mobility reduction due to residual stress has also been observed for ZnO [20]. Also the above reasoning based on changes in density of defect states does not contradict the observation that devices recover at room temperature.

To confirm that indeed stress affects D_{it} and in turn S and μ, we have conducted the following experiments. We first stressed the TFTs electrically with V_G = 20 V, grounding the source/drain on a flat surface [6]. In another experiment we conducted the same experiment; however in this case the TFTs are now held in bent position on a cylindrical diameter of 5.08 cm under tensile stress with simultaneous electrical stress. The current voltage characteristics were measured *in situ* conditions from 100 seconds onwards, without relaxing the device on a flat surface. The relative changes in S and μ are shown in Fig. 5.5. Electrical stress induces traps which reduce the mobility [14] and increases S. Tensile stress reduces D_{it} and thereby improves both S and μ, as discussed in the previous sections. The overall effect is a reduction in magnitude of change, when compared to only electrical stress being applied.

A separate set of experiments were also conducted by orienting the wafers such that the resultant stress were perpendicular to the channel length. Both tensile and compressive stress was applied, as was done for parallel stress. However, the changes in S, μ and I_{OFF} were minor and within experimental error. Hence we conclude there is almost most no

change under perpendicular stress. Similar results have also been observed for a-Si:H TFTs [5,21].

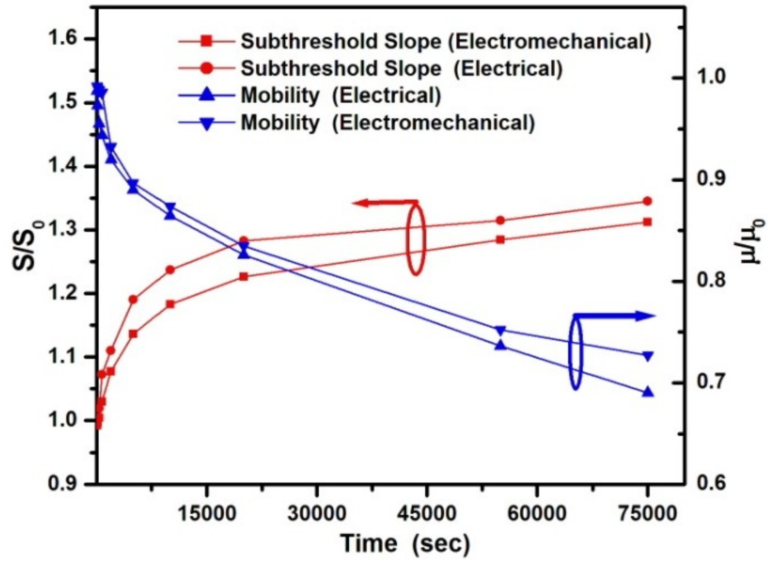


Figure 5.5 Electrical and tensile electro-mechanical stress vs time (bending diameter = 5.08 cm, ε = 0.27 %).

5. 4. CONCLUSION

ZIO TFTs were stressed mechanically by bending them inward and outward around cylindrical structure of various radii. The sub-threshold slope, mobility and I_{off} showed changes that depended on the direction and duration of the applied stress. Tensile stress showed a decrease in S and increase in μ. Compressive stress showed reverse changes. The reason we believe, is because of change in the band-gap and density of states with stress. Although these changes are similar to that observed in a-Si:H, further investigation is on way to evaluate the exact cause. However, none of the changes were catastrophic.

Chapter 6

EFFECT OF RADIATION ON THE PERFORMANCE OF A-SI:H TFTS FOR FLEXIBLE ELECTRONICS AND DISPLAYS

6. 1 INTRODUCTION

Thin-film transistors (TFTs) are of growing importance in flexible electronics for space applications. NASA already uses devices in solar sails and synthetic aperture radar systems that depend on TFT-based flexible circuits to monitor their electronic health and reliability in the harsh, uncompromising space environment [1]. TFTs are also basic components in flat panel display systems [2], including flexible displays on plastic and thin film stainless steel substrates. These lightweight, rugged, flexible displays may be beneficial in manned space applications. This study investigates the electrical reliability and lifetime of TFTs fabricated on flexible substrates in high radiation, *e.g.*, spacecraft, environments.

The effects of gamma irradiation and gate voltage electrical stress on the current-voltage characteristics of fabricated a-Si:H TFTs are discussed. Since TFTs are susceptible to degradation of their characteristics when biased with positive or negative gate voltages, it is important to compare any effects due to irradiation with the effects of such electrical stress alone. In this chapter, the changes in saturation mobility and the threshold voltage as a function of time and dose are derived from the I_{DS}–V_{GS} characteristics. By testing the TFTs with irradiation only,

electrical gate stress only, and irradiation with electrical gate stress, we examine the effects individually and in combination.

The a-Si:H TFTs suffer from degradation due to defect state creation and charge injection caused by prolonged electrical bias stress resulting in relatively rapid and large threshold voltage shift (ΔV_T). Field-effect experiments suggest the root cause of defect creation in amorphous silicon is channel charge [3,4]. Consistent with other studies, the threshold shift of our devices can be modeled using the power law as a function of time as [5]:

$$\Delta V_T(t) = A\exp\left(-\frac{E_A}{kT}\right)t^{\beta}\left(V_{GS} - \eta V_{DS} - V_{th.0}\right)^n \qquad (1)$$

where the constant A is the degradation rate, k is the Boltzmann constant, T is the absolute temperature, t is the bias stress time duration, E_A is the mean activation energy, $V_{th,0}$ is the initial transistor threshold voltage, V_{GS} and V_{DS} are the gate to source and drain to source voltages respectively, η is a fitting factor, and β and n are process-related constants.

These excess electrons create negative defect states in the lower half of the energy band-gap, producing a positive shift in the device V_T. Only a fraction of the mobile carriers are available to conduct current since charge carriers in the channel are distributed among the localized tail states. After prolonged positive gate voltage stress, enough defect states

accumulate to make the transistor's V_T approach the applied V_{GS}. Then, the density of mobile electrons becomes negligible with the result that the transistor cannot be turned on. As a practical matter, the circuit containing the degraded transistor will cease to operate effectively before this point. Display backplanes update at low rates, allowing the circuits to be operated at very low duty cycles. Additionally, row or gate drivers can be designed to remove the gate biases in unselected rows. This low duty cycle, combined with clever design, enables display backplanes to achieve commercially acceptable lifetimes.

6. 2 EXPERIMENTAL DETAILS

The TFTs used in these experiments were fabricated using a low-temperature (180°C) channel-passivated process with a 96 µm channel width and an 11 µm channel length. The transistor is a bottom-gate inverted architecture. The fabrication details of the TFTs are discussed elsewhere [2]. Three different tests on a total of 12 TFTs were performed: 1) positive V_{GS} electrical stress only, 2) Co-60 irradiation only, and 3) irradiation combined with positive V_{GS} electrical stress. Each TFT was assigned to one of the three experimental groups based on categorizing the TFTs according to their I_{DS} I_{ds}vs. V_{GS} V_{gs} and V_{DS} curves for a total of three groups of four similar TFTs.

1. In the test which applied only positive V_{GS} electrical stress, four TFTs were biased at V_{GS} = 20 V for 8 hours with V_{DS} = 0 V. At 1, 15, 30, 45 minutes, and 1, 2, 4, 8 hour intervals, their I_{DS} vs. V_{GS}

curves were extracted using a semiconductor parameter analyzer. A V_{GS} sweep from -20 to 20 V with V_{DS} = 10 V bias was performed at each interval.

2. In the irradiation only tests, another set of four TFTs were gamma irradiated at a dose rate of ~1.0 krad/minute with gate, drain, and source terminals of the transistors grounded. I_{DS} *vs.* V_{GS} measurements were made at thirteen dose levels ranging from 16 krad to 1.7 Mrad. After irradiation, the four TFTs were annealed at room temperature for 43 hours, and a final measurement was performed. Because all the TFTs were on a single die, the measurements were made in-situ.

3. The final test applied irradiation in combination with electrical gate stress. These TFTs were irradiated simultaneously with the irradiation-only group, but they were also electrically stressed at V_{GS} = 20 V with the drain grounded. The I_{DS} vs. V_{GS} curves of the four TFTs were regularly analyzed using a semiconductor parameter analyzer. The room-temperature anneal was also applied to these four TFTs without electrical stress.

6. 3 RESULTS

All four TFTs that were subjected only to the electrical stress exhibited a positive shift in V_T that follows the expected power law degradation of (1) with stress time, as shown in Fig. 6.1. In Fig. 6.2, the extracted threshold voltage and saturation mobility (β) are plotted. A fit to the extracted threshold voltage shows that β = 0.4. The mobility was extracted from the saturation current and normalized to the pre-stress value. Over the 6 hour stress time, the threshold voltage increased by 2 V and the mobility decreased by ~35%.

During the irradiation-only experiment, the four TFTs displayed a threshold voltage decreasing with radiation as shown in Fig. 6.3 and 6.4. As mentioned, the data taken during irradiation were measured in-situ, *i.e.,* while the DUT was within the gamma cell and being irradiated. The gamma irradiation results in an elevated reverse leakage current. The reverse leakage current measured outside the gamma irradiator was ~ 10^{-10} to 10^{-11} A whereas during irradiation the reverse current was ~4 × 10^{-9} A. The lack of this elevated current in the post-irradiation measurement (labeled in Fig. 6.3) indicates that this is a leakage current and is not due to degradation.

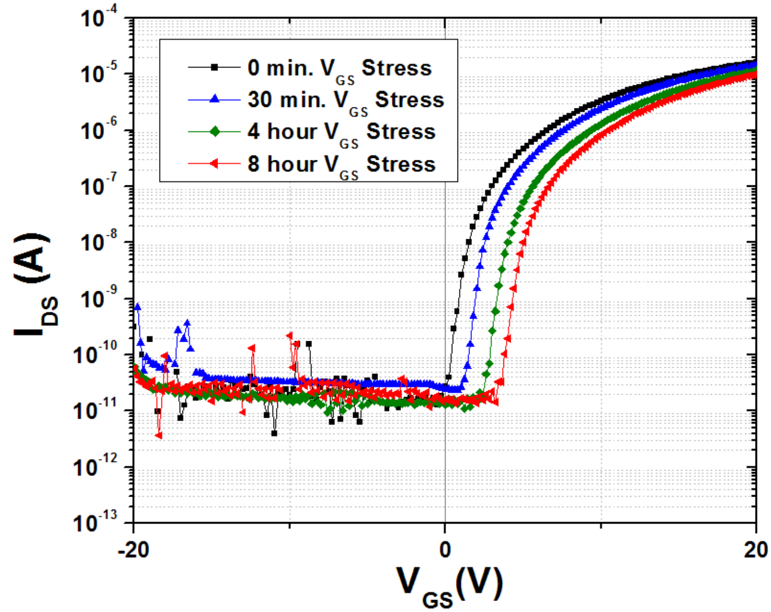


Figure 6.1 Representative I_{DS}-V_{GS} curves at V_{DS} = 10 V of the electrical gate stress only experiment where the TFTs were stressed at V_{GS} = 20 V, V_{DS} = 0V.

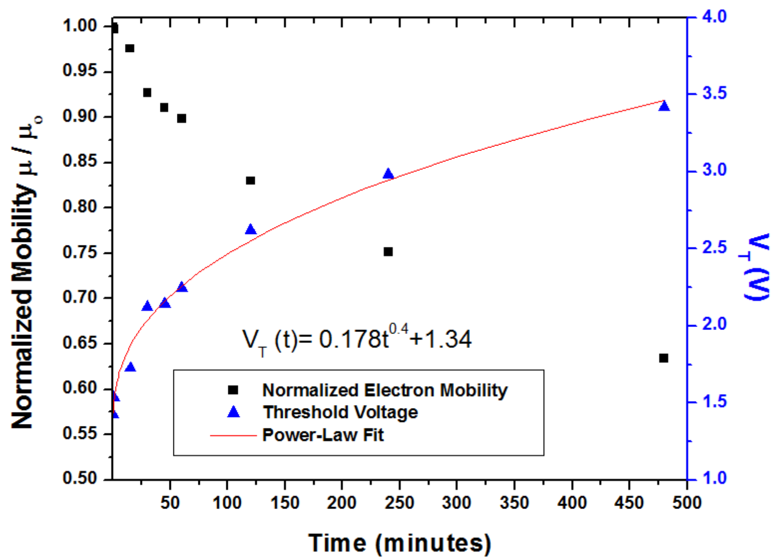


Figure 6.2 Representative mobility and threshold voltage characteristics from the electrical gate stress only experiment where the TFTs were stressed at V_{GS} = 20 V, V_{DS} = 0V.

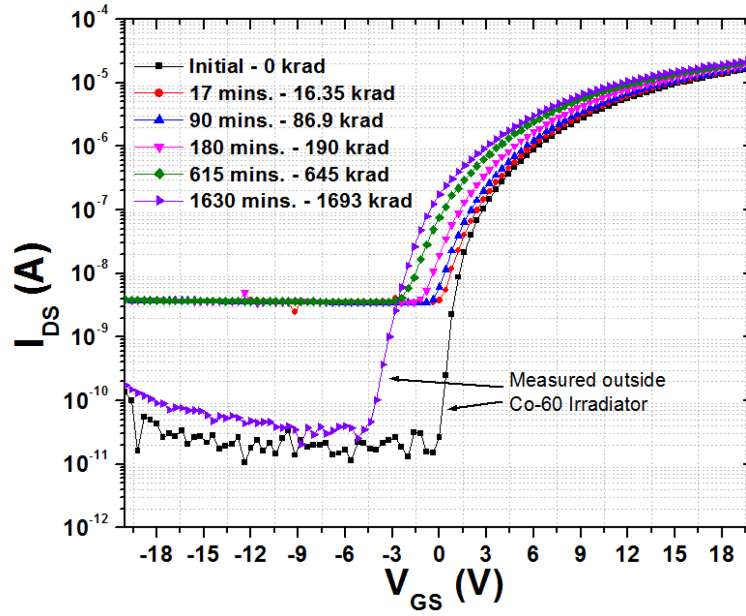


Figure 6.3 Representative I_{DS}-V_{GS} curves of the irradiation only test (no electrical stress) taken and measured inside the Co-60 irradiator with an exception to the initial and final measurements.

Unlike the previous case, the TFT drain current increases with time due to the irradiation, commensurate with the V_T shift. Note that the I_{off} increases exponentially with the V_T shift, while the I_{on} increases linearly. This is important since while the TFTs have very low I_{on}, good circuit behavior is provided by a high I_{on}/I_{off} ratio. Consequently, the device's usability, as well as the circuit leakage current is adversely affected by the irradiation.

In Fig. 6.4 the transistor's V_T and μ are plotted vs. time in the irradiator for the irradiation only test (no electrical stress – gate, drain, source are grounded). As expected from the I_{DS}-V_{GS} curves, the threshold voltage decreases, rendering the transistor a depletion device at a dose of about 200 krad. The mobility increased modestly with radiation, rising about 8% with a dose of 250 krad. From 250 krad to 700 krad, the mobility still remained at 8% higher than its pre-radiation value.

The results of "combined radiation and electrical stress" indicate that initially, the effect of electrical stress governs, shifting the I_{DS}-V_{GS} curve as shown in Figure 6.5 slightly to the right. However, with increased time (and dose), the effect of the radiation dominates, shifting the I_{DS} vs. V_{GS} curve significantly back to the left. As shown in Fig. 6.6, the threshold voltage decreases by about 1 V and the mobility increases by roughly 6% after a dose of 660 krad in a time span of roughly 650 minutes. It is also shown in Figure 6 that the V_T was initially rising and the mobility initially falling. These transient effects were evident in all of the working transistors

for the irradiation with electrical stress test. Again, there is elevated reverse leakage current when the devices were measured in the presence of radiation. The impact of the different effects on the threshold voltage for the TFTs within a similar group is compared in Figure 6.7. Since the irradiation and electrical stress shift the V_T in opposite directions, one effect mitigates the other. Specifically referring to Fig. 6.7, the combined electrical stress and irradiation results in a smaller overall ΔV_T than with the radiation alone. In the combined radiation and electrical stress test, the average threshold voltage shift was approximately –1 V as compared to –2.1 V for the irradiation only. These findings are consistent with electron-irradiation damage of gate insulators.

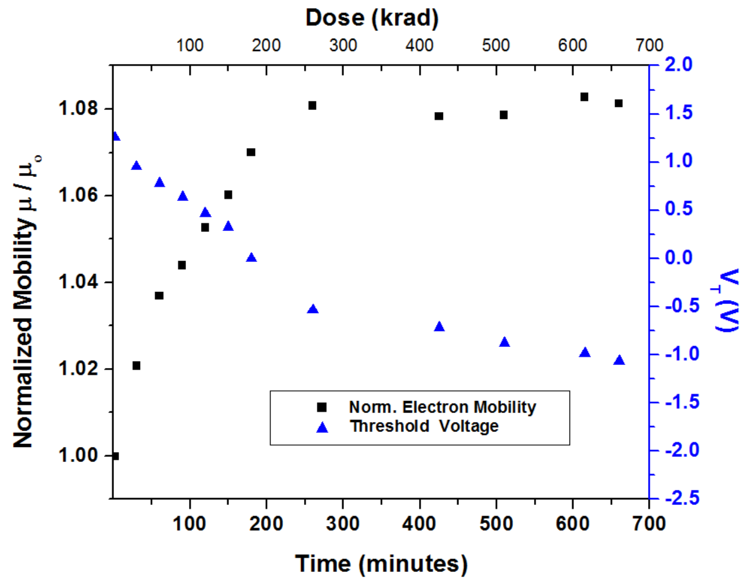


Figure 6.4 Representative mobility and threshold voltage characteristics from the irradiation only test (no electrical stress).

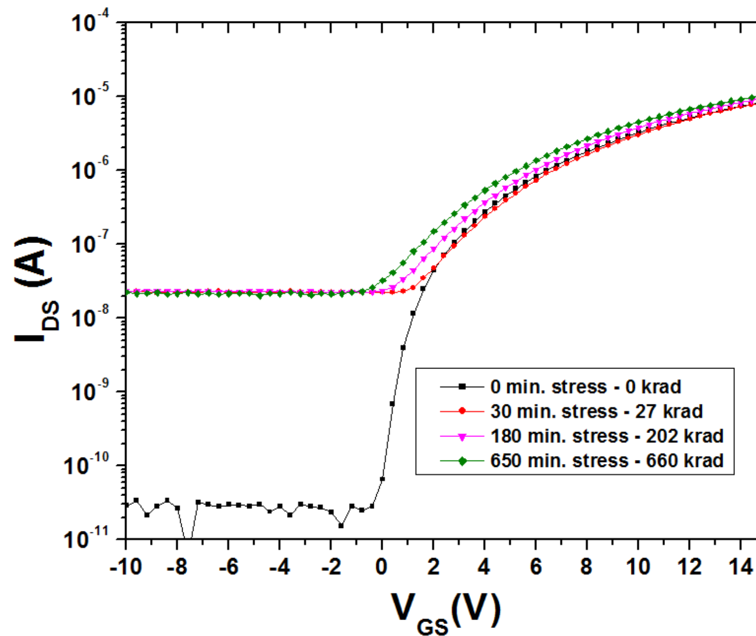


Figure 6.5 Representative I_{DS}-V_{GS} curves at V_{DS} = 10 V from the irradiation with electrical stress test where the TFTs were stressed at V_{GS} = 20 V, V_{DS} =0V.

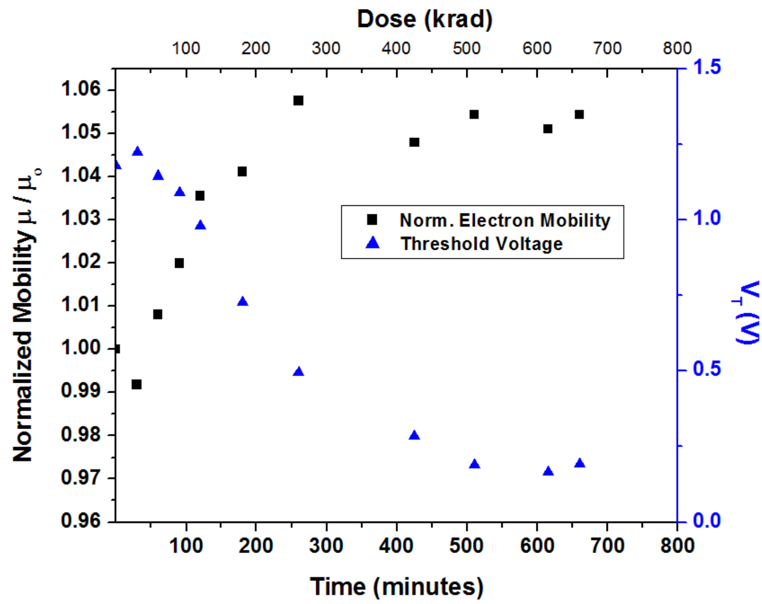


Figure 6.6 Representative mobility and threshold voltage characteristics from the irradiation with electrical stress test where the TFTs were stressed at V_{GS} = 20 V, V_{DS} = 0V.

6. 4. DISCUSSION

The results can be understood by a combination of state creation in bulk, interface state creation and electron-hole pair generation. For the "electrical bias stress only" test, the threshold voltages are all positively shifted and increase with bias stress time. The V_T exhibits power-law time dependence (Figure 6.2) and suggests that the dominant instability mechanism is state creation [6]. The decrease in the threshold voltage with irradiation dose for the "irradiation only" case is due to the presence of holes or fixed positive charge centers, as reported by other groups [7-9].

The exposure of the TFTs to gamma irradiation generates electron-hole pairs in the insulating layer [7-9]. The electrons generated by gamma radiation are trapped inside the interface states (simultaneously produced during irradiation, interface trap density has been quantified later in the discussion) resulting in substantial increase in the electron-hole recombination time. The presence of leftover holes is the primary reason for the V_T shift in the negative direction as reported by other groups [7-9]. In the case of combined irradiation and electrical stress, both of the mechanisms (state creation in a-Si:H channel and generation of holes) affect the electrical behavior of the TFT simultaneously. These two effects tend to negate each other, depending on the circuit activity factor and irradiation dose rate. The creation of states results in a positive shift in threshold voltage with stress time. Whereas the later results in a negative

threshold-voltage shift and the net result is a lower threshold-voltage shift when compared to the “irradiation only” case. As shown in Fig. 6.7, for combined radiation and electrical stress test, the average threshold voltage shift is ~ –1 V as compared to ~ –2.1 V when irradiated without bias.

To further interpret these findings, sub-threshold swing values are extracted for each of the cases. Fig. 6.8 shows the variation of sub-threshold swing (*S*) with exposure time for each case. The *S*-value is affected by both deep localized states in the a-Si:H channel layer and the interface states at the a-Si:H/SiN_x interface [10]. The interface trap density (N_{it}) at the semiconductor/insulator interface is estimated by [11]

$$N_{it} = \frac{C_{ox}}{q}\left(\frac{qS\log(e)}{kT} - 1\right) \tag{2}$$

Since,

$$S = 2.3\frac{kT}{q}\left(1 + \frac{qN_{it}}{C_{ox}}\right) \tag{3}$$

where q is the carrier charge, and C_{ox} is the oxide capacitance per unit area. The stable sub-threshold swing with stress time for the electrical bias stress case indicates a negligible degradation of the properties at the

interface. The degradation of the sub-threshold behavior for irradiation and electrical bias stress during irradiation implies damage to the interface. With long exposure to gamma radiation more interface states are produced. The N_{it} values range from 5 to 6 × 10^{11} cm^{-2} for only electrical stress bias case. For "irradiation only" case, the N_{it} value increases from 5×10^{11} cm^{-2} to 2×10^{12} cm^{-2} after 3 hours of gamma radiation exposure, whereas it increases from 5×10^{11} cm^{-2} to 4×10^{12} cm^{-2} for "combined gamma and electrical stress". Based on these values, we propose that the interfacial quality of these devices degrades with exposure to gamma radiation.

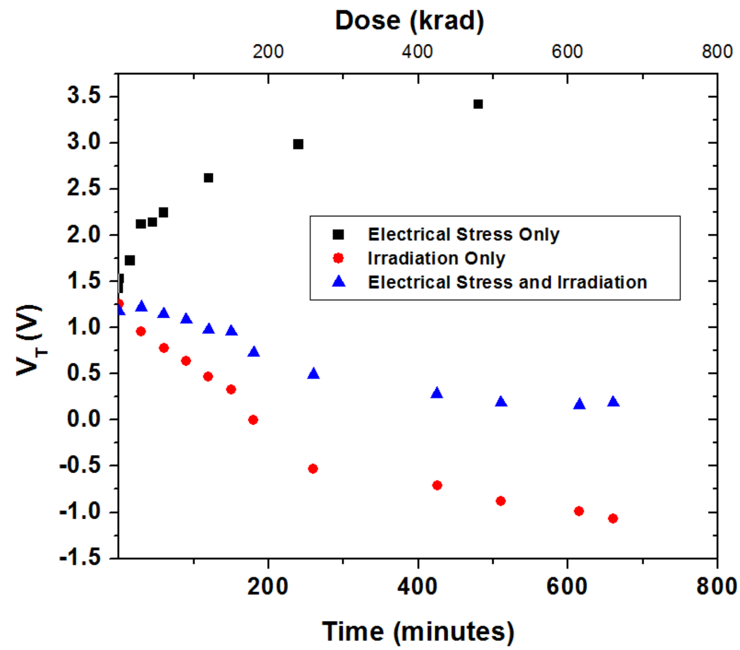


Figure 6.7 Threshold voltage as a function of time and accumulated dose for various devices in different tests.

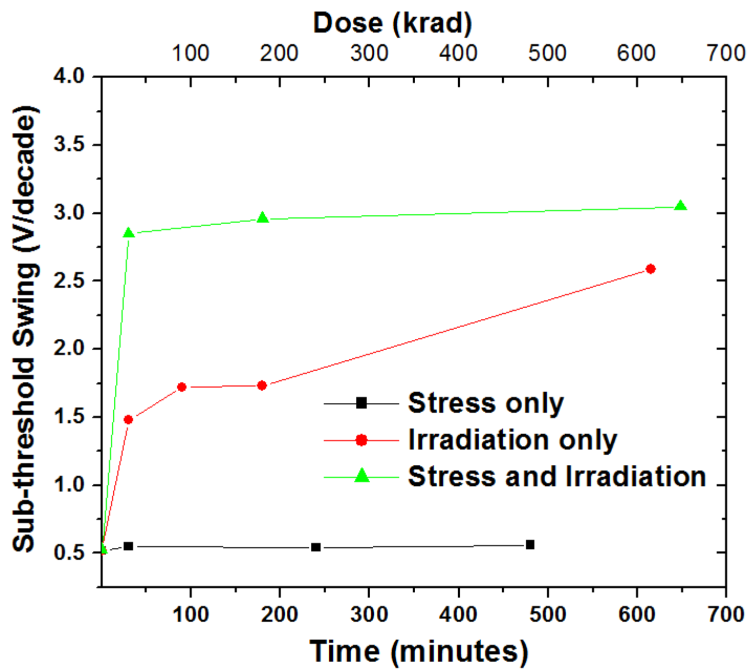


Figure 6.8 The sub-threshold swing as function of time and dose for various devices in different tests.

6. 5. CONCLUSION

From this study, we determined the threshold voltage shift and mobility behavior for a-Si:H TFTs fabricated on a low-temperature process amenable to flexible substrates when electrical gate stress and/or irradiation are applied. The threshold voltage shift due to a V_{GS} electrical stress rises as a power-law (Eq. 6.1) while the shift due to irradiation decreases with increasing dose. The combined effect of applying both the electrical stress (which follows a power-law V_T increase) and the irradiation (which imparts a V_T decrease) shows a threshold voltage that initially increases but then decreases with time and radiation dose. These effects are due to a combined creation of defect states, interface states and electron-hole pair generation in the insulating layer.

Chapter 7

CONCLUSION

7. 1. SUMMARY OF RESEARCH

In this dissertation, ITO-Ag-ITO multilayer transparent conductive oxide (TCO) system and low temperature fabricated thin film transistor (TFT) on flexible substrate has been investigated. Excellent electrical and optical properties have been obtained with figure of merit comparable to commercial TCO systems. The performance and reliability of the flexible a-Si:H and a-IZO TFTs has been investigated.

The first study was on the electrical and optical properties of ITO-Ag-ITO multilayer system on PEN flexible substrate. We have obtained excellent photopic average transmittance (~ 88 %), resistivity (~ 2.7×10^{-5} Ω-cm) and has the best Hackee figure of merit (41.0×10^{-3} Ω^{-1}) for the multilayer with optimum Ag (8 nm) thickness. The electrical properties (such as carrier concentration, mobility, and resistivity) changed significantly with incorporation of Ag between the ITO layers. Comparison of sheet resistance of the multilayers and the calculated sheet resistance of the Ag mid-layer indicates that most of the conduction is through the Ag mid-layer. The critical thickness of Ag to form a continuous conducting layer was found to be 8 nm using electrical and optical analysis. A conduction mechanism has been proposed to elucidate the mobility variation with increased Ag thickness. Carrier transport was found to be

limited by either interface scattering or grain-boundary scattering depending on the thickness of the Ag mid-layer. Interface scattering was dominant for thinner (5.5 - 7 nm) Ag and grain-boundary scattering was dominant for thicker (8 – 10.5 nm) Ag mid-layers. In addition, the effect of varying Ag mid-layer thickness on the optical properties has also been discussed. A figure of merit was used to compare performance of the IMI multilayer systems as a function of Ag thickness.

We have studied the effect of low temperature long anneals on the performance and stability of low temperature fabricated a-Si:H TFTs on PEN substrates. The TFTs were annealed in 5 % H_2/Ar (reducing atmosphere) at 150 °C for different times (4, 8, 24, 48, and 96 h) before any application of electrical stress. The bias-stress measurements are performed for up to 10^4 seconds and interrupted at regular intervals to measure the transfer characteristics. The source and the drain electrodes were grounded during the stress experiments. The stability and transfer characteristic of these TFTs were studied at temperatures ranging from room temperature to elevated temperatures as high as 125 °C. For TFTs annealed for 96 h, the sub-threshold slope and off-current were reduced by a factor ~ 3 and by 2 orders of magnitude, respectively when compared to unannealed TFTs. Also, longer annealed TFTs showed a significant improvement in their stability when compared to unannealed TFTs. Life-time values for the 48 h, and 96 h annealed TFT improved by a factor of ~ 3 compared to unannealed TFTs when threshold voltage shift is

extrapolated to 10 V. Stability at high temperatures with better life times for the longer annealed TFTs is due to improvement in the a-Si:H/SiN_x interface quality by the reduction of trapped charges inside the insulator. For all the TFTs at positive gate bias ΔV_t follow a power law-dependence with time indicating state creation. A low β value (0.6 for unannealed to 0.37 for 96 h annealed TFTs) indicates a good quality a-Si:H channel and/or the a-Si:H/insulator interface after longer anneals. Based on the variations of sub-threshold slope, mobility, and hysteresis with temperature; it has been inferred that the improvement in the stability is due to the reduction of interface trap density and good quality a-Si:H/insulator interface with anneal time.

We have performed similar low temperature long anneal study on a-IZO TFTs on PEN. This system has better mobility compared to a-Si:H TFTs. For this study the IZO TFTs have been annealed in air at 150 °C for different times (24, 48, 72, and 96 h) before any application of an electrical stress. The stability and transfer characteristic of these TFTs were studied at temperatures ranging from room temperature to elevated temperatures as high as 125 °C on an array of TFTs with *W/L* of 96/9. The TFTs were stressed with a positive gate bias of 20 V for up to 10^4 seconds. The source and the drain electrodes were grounded during the stress experiments. All the measurements were done in the dark using a HP4155B semiconductor parameter analyzer. Transfer characteristics were measured at source-drain voltage of 10 V and gate voltages from -20

V to 30 V. We have found that there is an optimum annealing time of 48 hours for the best performance and elevated temperature stability. The 48 hour annealed TFTs showed a stable turn-on voltage, and sub-threshold swing with operation temperatures when compared to the as-fabricated TFTs. The performance/stability improvements are attributed to the reduction in trap-state-density at the semiconductor/insulator interface, and curing of the defects states in the band-gap of IZO.

We also investigated the effects of mechanical and combined electro-mechanical stress on the IZO TFTs. The processed TFTs on PEN were cut into cylindrical shape and were later rolled around various radii tubes. All the measurements were made with a HP 4155B semiconductor parameter analyzer. Since all bending was done on cylindrical surfaces, the stress was essentially uniaxial. Tensile stress was obtained by bending the devices outward; while, compressive stress was obtained by bending them inward. For electromechanical stress the flexible substrate with TFTs were rolled around the cylindrical surface and taped at the ends while taking the measurements. The largest and smallest diameters in our experiment were 11.4 and 1.5 cm, respectively. All I-V characteristics were measured with gate to source bias (V_{GS}) varying from - 20 to 20 V at a constant drain to source bias (V_{DS}) = 10 V and 1 V. The off state current (I_{off}) was calculated as the least current value for V_{DS} = 10 V. The TFTs were subjected to both tensile and compressive stress, parallel and perpendicular to the conducting channel length. The mobility increased

while sub-threshold swing decreased with tensile stress and reverse changes were observed with compressive stress, both being parallel to the channel length. Almost no changes were observed for perpendicular stress, within experimental errors. The magnitude of change also depended on the time duration of strain. None of the changes were catastrophic to cause complete failure of the devices.

Finally, the a-Si:H TFTs were exposed to gamma radiation to test their radiation resistance. Three different tests on a total of 12 TFTs were performed: 1) positive V_{GS} electrical stress only, 2) Co-60 irradiation only, and 3) irradiation combined with positive V_{GS} electrical stress. Multiple TFTs were tested under each condition, and the current-voltage characteristics were measured. The results show the gate bias stress increasing the threshold voltage (V_T) with power law time dependence while the gamma irradiation decreases threshold voltage. When both the irradiation and gate bias stress were applied simultaneously, the V_T initially increased with electrical stress dominating and then decreased as the gamma radiation dominated. Changes in effective mobility were also extracted, and detailed analysis of the current-voltage characteristics indicated that the gamma radiation creates interface traps and electron-hole pairs whereas the gate stress produces defect states in the amorphous silicon.

7. 2. FUTURE WORK

It would be very interesting to integrate the ITO-Ag-ITO multilayer system in some device, such as organic light emitting diodes, flat-panel displays and photovoltaics, and investigate the device performance. The novel low temperature long anneals has a significant impact on the performance and their stability which is mostly due to improvement in the interface quality. Quantification of these interface states for each of the annealing case would definitely strengthen the point. Also, it would be interesting to investigate effect of different annealing ambience on the performance and stability of both a-Si:H and IZO TFTs. Lastly, modeling and simulation of the transfer characteristics would immensely advance the elucidation of the device physics of metal oxide TFTs, as device simulation is the fundamental tool for analyzing the activities of trap states and their effects on TFT performance.

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APPENDIX A

LIST OF PUBLICATIONS

JOURNAL PUBLICATIONS

1. **Indluru**, and T. L. Alford, "Effect of Ag thickness on electrical transport and optical properties of indium tin oxide–Ag–indium tin oxide multilayers," Journal of Applied Physics **105**, 123528 (2009).
2. **Indluru**, E. Misra, and T. L. Alford, "Current-density dependence on Ag eFUSEs With TiN Underlayers," IEEE-Electron Device Letters **30** (11), 1134 (2009).
3. **Indluru**, and T. L. Alford, “High temperature stability and enhanced performance of a-Si:H TFT on flexible substrate due to improved interface quality,” IEEE-Transactions on Electron Devices **57** (11), 3006 (2010).
4. **Indluru**, S. M. Venugopal, D. R. Allee, T. L. Alford, “Effect of anneal time on the enhanced performance of a-Si:H TFT's for future display technology” *accepted (in press)* IEEE – Journal of Display Technology.
5. **Indluru**, T. L. Alford, “Improvement in electrical stress stability of indium zinc oxide TFTs after low temperature annealing,” Electrochemical and Solid-State Letters **13** (12) H464 (2010).
6. **Indluru**, T. L. Alford, “Enhanced performance and thermal stability of a-Si:H TFTs,” Electrochemical and Soild-State Letters **13** (12), H467 (2010).
7. Dey, **A. Indluru**, S. M. Venugopal, D. R. Allee, T. L. Alford, “Effect of mechanical and electro-mechanical stress on IZO TFTs,” IEEE – Electron Device Letters **31** (12),1416 (2010).
8. **Indluru**, N. D. Theodore, and T. L. Alford, “Improved Electrical Conductivity and Optical Properties of ITO/Ag/ITO Thin Films for Flexible Electronics,” *under review* Applied Physics Express.
9. Edward H. Lee, **A. Indluru**, David R. Allee, Lawrence T. Clark, Keith E. Holbert, and Terry L. Alford, “Effects of gamma irradiation and voltage gate stress on performance and lifetimes of a-Si:H thin film transistors for flexible electronics and displays,” *accepted* (*in press)* IEEE – Journal of Display Technology.

CONFERENCE PRESENTATIONS AND PROCEEDINGS

1. **Indluru**, S. M. Venugopal, D. R. Allee, and T. L. Alford, “Threshold voltage shift variation of a-Si:H TFTs with anneal time,” MRS Spring 2010 Conference Proceedings, San Francisco, California, USA.
2. **Indluru**, T. L. Alford, “Improved thermal stability of indium zinc oxide TFTs by low temperature post annealing,” Electrochemical Society Transactions, 2010.
3. **Indluru**, T. L. Alford, “Enhanced performance and thermal stability of a-Si:H TFTs,” Electrochemical Society Transactions, 2010.
4. T. L. Alford, K. Sivaramakrishnan, N. D. Theodore, **A. Indluru**, I. Ahmad, and B. Hubbard, “Low temperature dopant activation using variable frequency microwave annealing,” MRS Spring 2010 Conference Proceedings, San Francisco, California, USA.
5. **Indluru**, and T. L. Alford, “Improved Thermal Stability of Indium Zinc Oxide TFTs by Low Temperature Post annealing,” Oral presentation, Electrochemical Society conference, 11-13th Oct. 2010, Las Vegas, Nevada, USA.
6. **Indluru**, and T. L. Alford, “Enhanced Performance and Thermal Stability of a-Si:H TFTs,” Oral presentation, Electrochemical Society conference, 11-13th Oct. 2010, Las Vegas, Nevada, USA.
7. **Indluru**, S. M. Venugopal, D. R. Allee, T. L. Alford, "Effect of anneal time on the performance of a-Si:H TFT's on flexible substrates," poster presentation, Flexible Electronics & Displays Conference 1-4th Feb 2010, Phoenix, Arizona, USA.
8. **Indluru**, N. D. Theodore, and T. L. Alford, "Effect of Ag thickness on electrical transport and optical properties of ITO/Ag/ITO multilayers for flexible electronics," poster presentation, Flexible Electronics & Displays Conference 1-4th Feb 2010, Phoenix, Arizona, USA.
9. **Indluru**, S. M. Venugopal, D. R. Allee, and T. L. Alford, “Threshold Voltage Shift Variation of a-Si:H TFTs With Anneal Time,” poster presentation, MRS spring conference, 5-9th April 2010, San Francisco, California, USA.
10. **Indluru**, S. M. Venugopal, D. R. Allee, and T. L. Alford, “Elevated temperature stability and enhanced performance of a-Si:H thin-film transistors on flexible substrates,” 7-10th Feb 2011, Phoenix, Arizona, USA

11. **A. Indluru,** and T. L. Alford**, "**Electrical, mechanical, and electro-mechanical stability of IZO thin-film transistors on flexible substrates," 7-10th Feb 2011, Phoenix, Arizona, USA

12. Edward H. Lee, **A. Indluru**, David R. Allee, Lawrence T. Clark, Keith E. Holbert, and Terry L. Alford, "The electrical reliability of a-Si:H TFTs with gamma radiation and electrical stress," poster presentation, Flexible Electronics & Displays Conference 1-4th Feb 2010, Phoenix, Arizona, USA.