Kinetics of Programmable Metallization Cell Memory

by

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ABSTRACT

Programmable Metallization Cell (PMC) technology has been shown to possess the necessary qualities for it to be considered as a leading contender for the next generation memory. These qualities include high speed and endurance, extreme scalability, ease of fabrication, ultra low power operation, and perhaps most importantly ease of integration with the CMOS back end of line (BEOL) process flow. One area where detailed study is lacking is the reliability of PMC devices. In previous reliability work, the low and high resistance states were monitored for periods of hours to days without any applied voltage and the results were extrapolated to several years ($>$10) but little has been done to analyze the low resistance state under stress. With or without stress, the low resistance state appears to be highly stable but a gradual increase in resistance with time, less than one order of magnitude after ten years when extrapolated, has been observed. It is important to understand the physics behind this resistance rise mechanism to comprehend the reliability issues associated with the low resistance state. This is also related to the erase process in PMC cells where the transition from the ON to OFF state occurs under a negative voltage. Hence it is important to investigate this erase process in PMC cells under different conditions and to model it.

Analyzing the programming and the erase operations separately is important for any memory technology but its ability to cycle efficiently (reliably) at low voltages and for more than 10^4 cycles (without affecting the cells performance) is more critical. Future memory technologies must operate with the low power supply voltages ($<$1V) required for small geometry nodes. Low voltage programming of PMC memory devices has previously been demonstrated using slow voltage sweeps and small numbers of fast pulses. In this work PMC memory cells were cycled at low voltages using symmetric pulses with different load resistances and the distribution of the ON and OFF resistances was analyzed. The effect of the program current used during the program-erase cycling on the resulting resistance distributions is also investigated.

Finally the variation found in the behavior of similar resistance ON states in PMC cells was analyzed more in detail and measures to reduce this variation were looked into. It was found that slow low current programming helped reducing the variation in erase times of similar resistance ON states in PMC cells. This scheme was also used as a pre-conditioning technique and the improvements in subsequent cycling behavior were compared.

To my parents, friends and the lovely Saranya.

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INTRODUCTION

1.1 Motivation

For years it was Dynamic Random Access Memory (DRAM) that was thought of for fast random access memory like the caches and Random Access Memories (RAM) in computers and it was magnetic storage memory that dominated the mass memory (but slower) storage like the computer hard disks and external storage. Magnetic storage memory falls into a class of memory technology called the Non-Volatile Memory (NVM). NVM functionality refers to the ability of a memory system to maintain stored information even if the power to the system is turned-off. NVM functionality is provided by a range of devices like hard disk drives, discrete NVM ICs and NVM blocks embedded in system-on-chip. Common examples of discrete NVM blocks used are in computer motherboards, serial memory chips, code storage chips and mass storage like USB drives and cards. Embedded NVM chips are used in microcontrollers, digital signal processors and programmable logic devices. FLASH memory is the mainstream of NVM technologies and it is considered a major break through in the semiconductor memory industry for more than a couple of reasons. First it marked the beginning of an improved age of hand held storage devices and consumer electronics like the memory sticks, smart phones, memory cards, mp3 players and now even ultra-portable computers. Also the entire outlook of having two different technologies, one for smaller but faster applications and another for slower but larger applications is beginning to fade and the quest for an universal memory is surfacing and this is the second most important impact of FLASH on the memory industry.

1.2 Introduction to FLASH memory

A FLASH cell is simply a floating gate MOS transistor (Fig. 1.1) or a transistor with a gate completely isolated by dielectrics, the Floating Gate (FG) and governed electrically by a capacitive coupled Control Gate (CG). FG acts as a storage bin for electrons

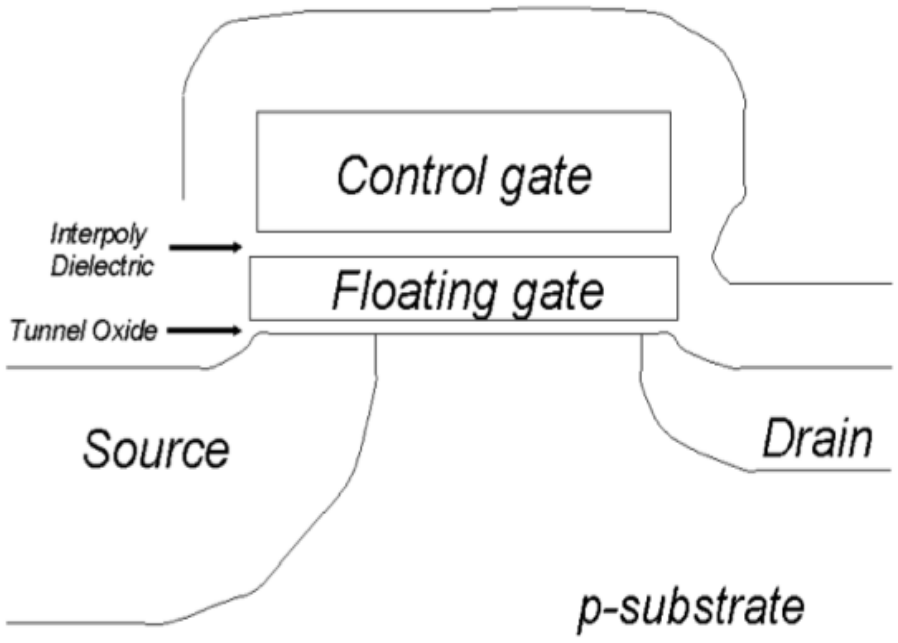

Figure 1.1: Schematic cross section of a Flash cell. The floating-gate structure is common to all the nonvolatile memory cells based on the floating-gate MOS transistor [1]

as it is isolated and charge injected into it modulates the threshold voltage of the transistor allowing for discrete memory levels. The electrons are forced to tunnel into the FG by applying appropriate bias to the CG, the source and drain terminals of the FG MOS to achieve very high electric fields across the thin FG gate oxide. The non-volatility depends on the quality of the dielectrics (and hence on the charge leakage to and from the FG). The gate dielectric between the FG and the channel is thinner as it allows the carriers (electrons) to tunnel in and out of the FG and the dielectric between the FG and the CG is thicker.

Fig. 1.2 shows the band diagram of a FG MOS assuming ideal behavior of the dielectrics. The neutral state is associated with the logic level '1' and the negatively charged state (with electrons in the FG) with logic level '0'. With the electrons in the FG the threshold voltage (V_T) increases positively and this can be sensed (read operation) by applying a bias between the source and the drain of the FG MOS. The erase operation is achieved by forcing the electrons out of the FG through either FN

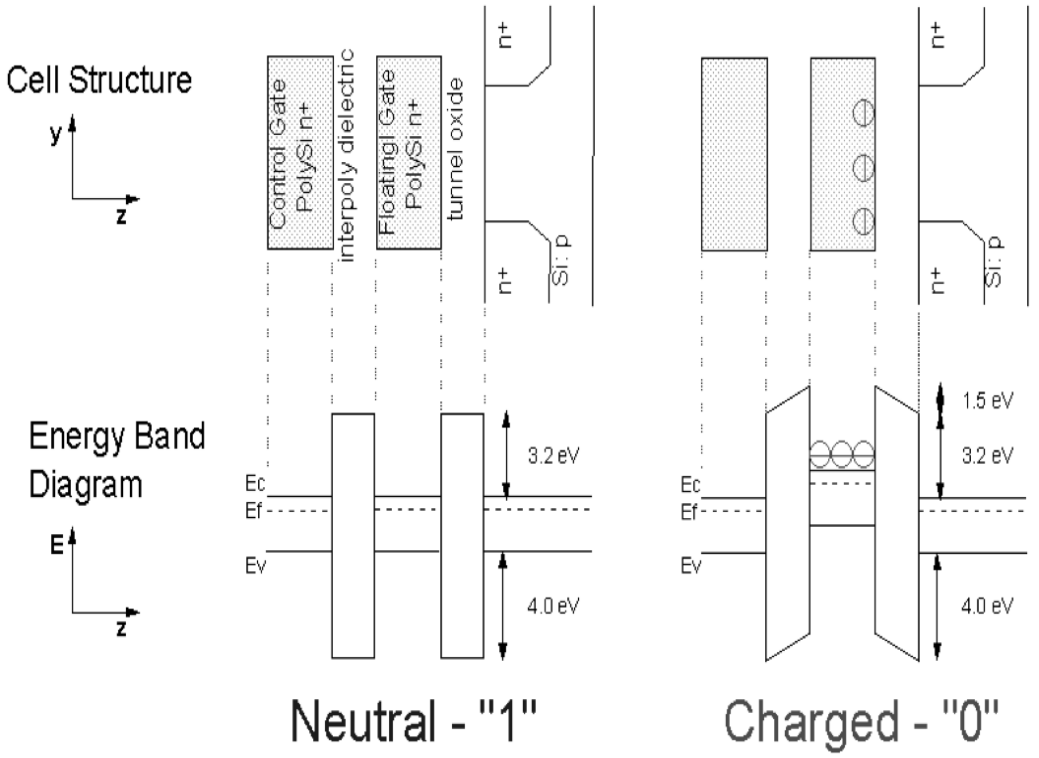

Figure 1.2: Schematic energy band diagram (lower part) as referred to a floating gate MOSFET structure (upper part). The left side of the figure is related to a neutral cell, while the right side to a negatively charged cell [1]

tunneling or UV radiation. Data retention in FLASH is specified to be more than 10 years and this means that the charge leakage from the FG is very minimal [1].

However FLASH has its set of limitations as a solid-state memory technology [10, 11]. It is prone to charge leakages, which reduces the number of write-erase cycles drastically and limits its scalability. The practical limit in thickness of the oxide layer (8 nm) below which oxide leakage current is intolerable is also fast approaching. A typical FLASH cell has an endurance of up to 10^5 cycles, above which the memory states lose their identity. Even with a lot of innovations being done in the control circuitry of these devices to improve its endurance, a permanent solution has not been reached yet [12, 13]. Another factor that cannot be overlooked is the cost of memory. The approximate cost of FLASH memory for portable devices is many times higher than the traditional rotating magnetic memory drives.

Today though FLASH (or its variations) dominate the Non-Volatile Memory (NVM) devices and the embedded memory applications and this NMV market is growing rapidly [14], all of these NVM devices in production require high voltages in excess of 5-8 V for operation primarily due to their fundamental operating principles. This is very different from the power requirements of the CMOS logic transistors used with the NVM devices that require less than 1 V to operate. Hence combining power hungry NVM devices with ultra-low power transistors poses a huge challenge for any improvement in embedded memory applications. Further, the need for future ultra-low power and sub-threshold CMOS applications, such as wireless sensor networks, biomedical devices, and portable electronics [15, 16], that require operating voltages less than 500 mV, is also ever growing.

Thus the whole industry is on the lookout for a universal memory that is much more scalable, reliable, cheap, ultra power efficient, simple and that can be easily integrated in to our current process flow without significant changes. It is a well-known fact that the innovation in new materials and technology is necessary for satisfying the fore mentioned requisites particularly as the physical limits of scaling are fast approaching. There are several key emerging memory technologies are under development for next-generation NVM technologies and storage applications [17, 18, 19]. Some of the main contenders are briefly discussed below.

1.3 Contenders for future memory technology

MRAM

In Magnetic storage RAM (MRAM) [19, 20, 21] data is stored by magnetic storage elements. The elements are formed from two magnetic plates, each of which can hold a magnetic field, separated by a thin insulating layer. One of the two plates is a permanent magnet set to a particular polarity, the other's field can be changed to match that of an external field to store data. The simplest way of reading a cell is achieved by measuring the electrical resistance of the cell as the electrical resistance of the cell changes due to

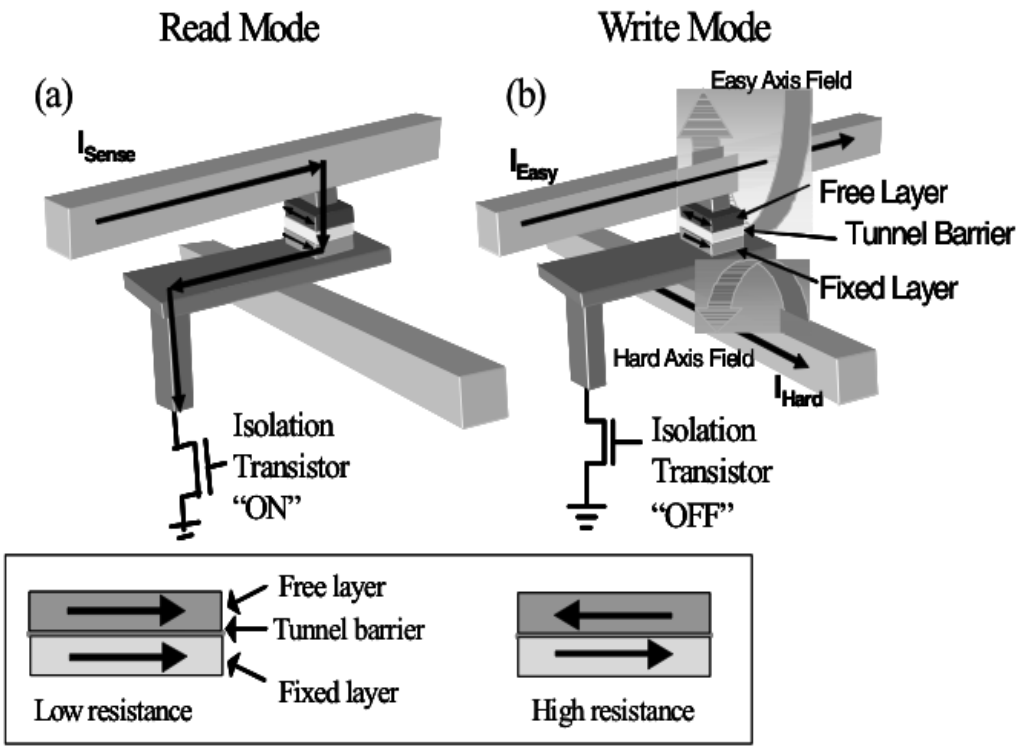

Figure 1.3: Illustration of a field-switched MRAM cell undergoing a) read and b) write operations. The inset shows the magnetic configuration of the layers in the MTJ for the two resistance states [2]

the orientation of the fields in the two plates as a result of the magnetic tunnel effect. Fig. 1.3 shows a MRAM memory cell based on a 1-transistor, 1-MRAM memory cell.

The key advantage of MRAM is its performance and endurance, but its cost structure is seen as the major disadvantage of the technology. The relatively small dynamic range of MRAM cell's ON and OFF states (< 50 [22, 23]) result in much larger cell designs which also affect their adaptation into multilevel applications. Also practical implementations of MRAM require very high write currents ($> 500\ \mu$A [24]), which is a disadvantage for use in ultra low power applications and in compatibility with sub-threshold CMOS. Hence such limitations still pose significant challenges in implementing MRAM for future memory applications. [20]

FeRAM

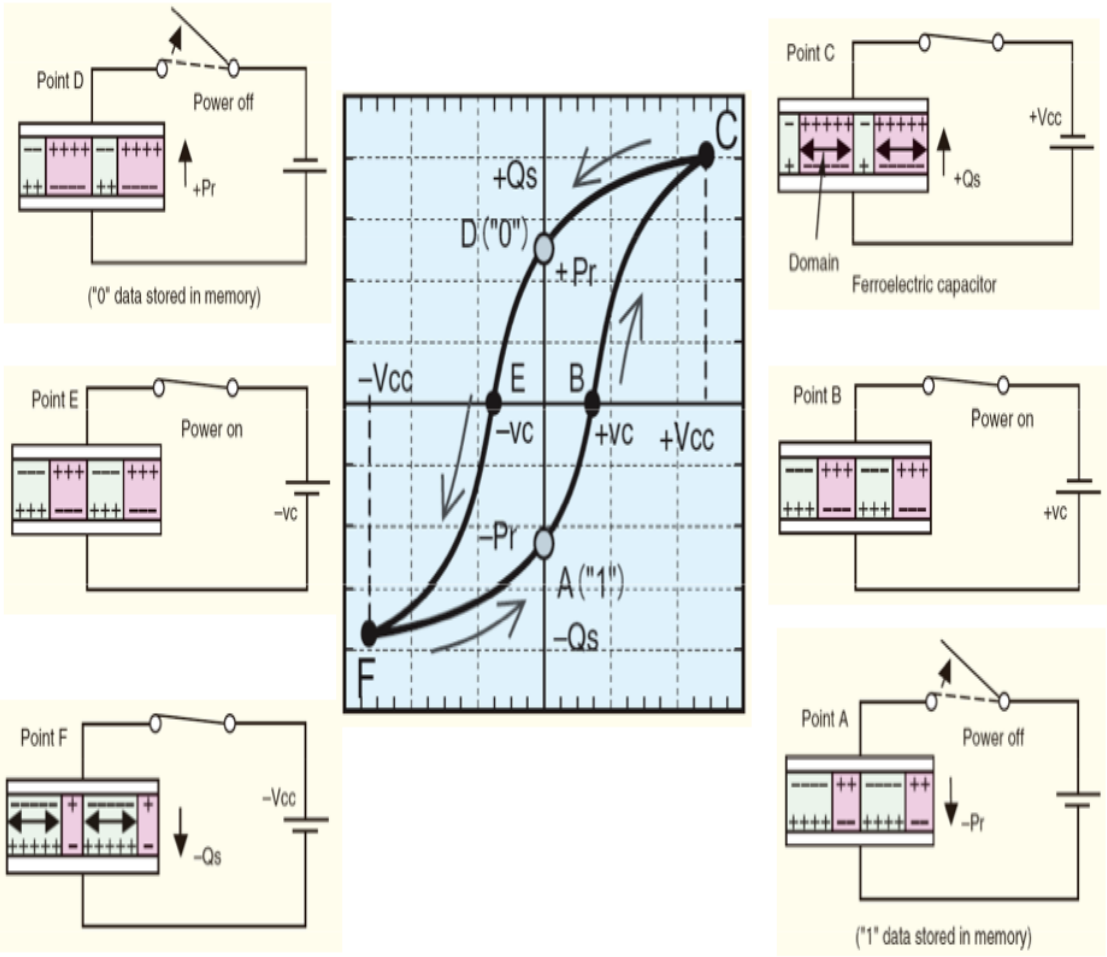

Figure 1.4: Illustration of polarization in a ferroelectric material and basic operation of FeRAM [3]

Ferroelectric RAM or FeRAM [25, 26, 27] is similar in construction to a DRAM but uses a ferroelectric layer instead of a dielectric layer to achieve non-volatility. A FeRAM cell also contains a capacitor and a transistor with the exception that in the FeRAM capacitor, the dielectric structure includes a ferroelectric material, like lead zirconate titanate. A ferroelectric material has a nonlinear relationship between the applied electric field and stored charge or the ferroelectric characteristic has a hysteresis loop as shown in Fig. 1.4. When an external electric field is applied across the ferroelectric material, the dipoles tend to line up in the direction of the applied field, due to small shifts in the positions of the atoms in the crystal structure of the material. This change is retained even after the field is removed making the memory cell non-volatile. Typically binary ”0”s and ”1”s are stored as one of two possible electric polarizations in each data storage cell.

The operational conditions of FeRAM result in low power consumption compared to MRAM and its high speed of operation also adds to lower write energy (100x - 1000x lower than FG NVM cells [24]). However the disadvantage with FeRAM technology is its characteristic wear out mechanism that limits the endurance of the cell in terms of program-erase cycles, high temperature operation and large cell size. Also another key scaling challenge of FeRAM technology has been the requirement for annealing the ferroelectric films at temperatures in excess of 600 ^{o}C which are not compatible for sub 90 nm CMOS back end of line processing temperatures. [28]

PCRAM

Phase Change RAM or PCRAM [29, 30, 31] uses the unique property of some chalcogenide glasses to switch between two resistance states (crystalline and amorphous) upon application of heat. In the amorphous state these materials are highly disordered and there is no regular order to the lattice. In this phase the resistivity is high and in contrast, the crystalline state of these materials exhibit low resistivity and ordered crystal lattice. This difference in resistivity is exploited in PCRAM and the phase change

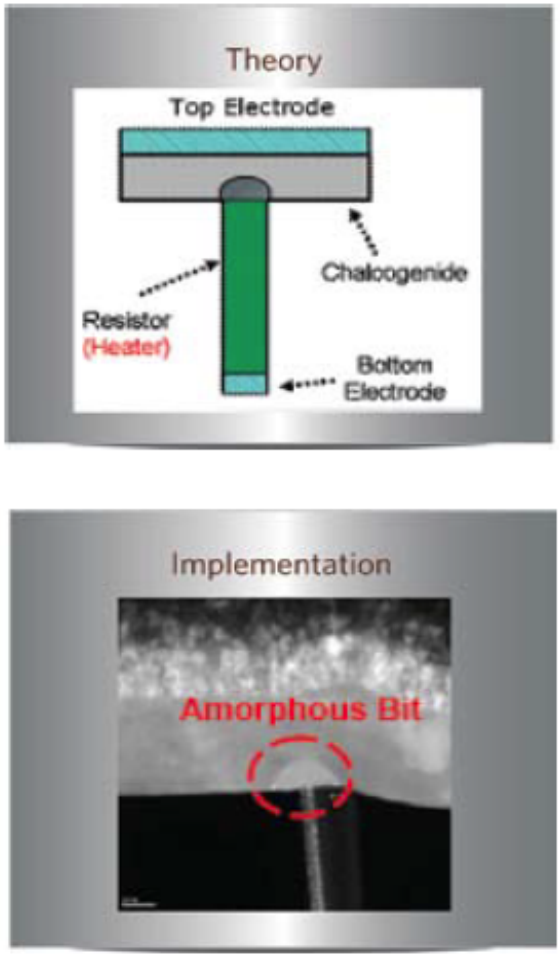

Figure 1.5: Example phase change storage element [4]

is achieved through localized joule heating caused by current injection. The end phase of the material can be adjusted through the injected current, applied voltage and the time of operation. As shown in Fig. 1.5 a layer of chalcogenide is sandwiched between two electrodes. A resistive heating element extends from the bottom electrode and contacts the chalcogenide layer. Current injected through this heating element induces phase change in the resistive switching element and different resistance phases of this material are used to represent different logic levels.

PCRAM technology based on GST chalcogenide resistive alloys has produced the densest of memory devices (512 Mb) utilizing emerging memory technologies [32]. Unlike MRAM and FeRAM the dynamic range between the ON and OFF states in

PCRAM is higher than 100x and hence simple cell architectures are possible. The write speeds in PCRAM ($<$ 500 ns [24]) are also impressive and better than the previously discussed NVM technologies. However the currents required to switch between the two states in the materials are very high ($>$ 500 μA [24]) and this limits the use of smaller access transistors and hence scaling in this technology.

The fourth technology that is a major contender for future memory applications is PMC. Many advantages like small cell sizes ($8F^2$ [33]), wide dynamic range between the ON and OFF state ($> 10^8$ [24]), fast write speeds ($<$ 100 ns [24, 34]), modulation of ON resistance with write current aiding in multilevel applications [5], sub 500 mV and sub 100 nA [24] operation are some of those advantages. But of the four technologies discussed PMC possesses the least history. Next section introduces more about PMC and its basic operation.

1.4 Programmable Metallization Cell (PMC) technology

Programmable Metallization Cell (PMC) technology has been shown to posses the necessary qualities for it to be considered as a leading contender for the next generation memory. These qualities include high speed and endurance [35, 36], extreme scalability, ease of fabrication, ultra low power operation, and perhaps most importantly ease of integration with the CMOS back end of line (BEOL) process flow [37]. It works by modifying the resistivity of a glass layer that is sandwiched between two metals, by electrochemically growing and dissolving a thin electrodeposit/Conductive Filament (CF) between the two metals. A metal doped (typically silver or copper) glass layer (germanium selenide/sulfide or recently SiO_2 [38]) that has very high resistivity inherently [34], has an anode (silver or copper) on top and an electrochemically indifferent cathode (typically tungsten) at the bottom.

When a positive bias that is greater than the threshold voltage ($\sim$ 450 mV) of the device, is applied between the anode and the cathode, silver from the anode is oxidized and migrates towards the cathode under the influence of the electric field and

gets reduced once it reaches the cathode with the help of the electron current form the cathode. Once the growth of the conductive filament initiates, the subsequent silver ions migrating towards it prefer to get deposited at the tip of the growing filament, as the electric field is highest at that point. As this process continues the area between the two electrodes is bridged by a silver electrodeposit after some time ($<$ 100 ns [34]) and the resistance now is very low. This silver electrodeposit remains unaffected even after the voltage supply is cut off and hence the device can works as a non-volatile memory by switching between these two very stable high and low resistance states repeatedly.

Since information is stored in the form of an electrochemically grown metallic filament rather than charge, the leakage is very negligible and hence the reliability is very high. Also irrespective of the device dimensions the diameter of the grown electrodeposit (depends only on the programming current) is only a few tens of nanometers ($<$ 100 nm) making it is ultra scalable [7], hence combining small footprint with non-volatility, unlike the DRAM which has a small footprint but needs to be constantly refreshed to retain its logic state. Also the write voltage is less than 1V and the erase voltage is less than 0.5 V and hence it consumes ultra low power [36]. Since the processing steps are very simple it can be integrated to the current technology with ease as well [39]. Moreover the process of electrodeposition and the erase mechanism together take only a few nanoseconds ($<$ 100 ns), as the ion mobility in these glasses is very high. Hence the devices are also extremely fast [34].

A lot of work relating to the above mentioned characteristics of PMC technology has already been done and it is an established fact that programmable metallization cell memory is indeed superior to the current memory technologies and its contenders for the spot of the next generation memory [40, 41, 42]. Fig. 1.6 shows the technology performance evaluation for Nanoionic memory (under which PMC memory technology falls) in ITRS 2009 and it has impressive ratings in all areas except reliability. This is due to the fact that detailed work is lacking in this area.

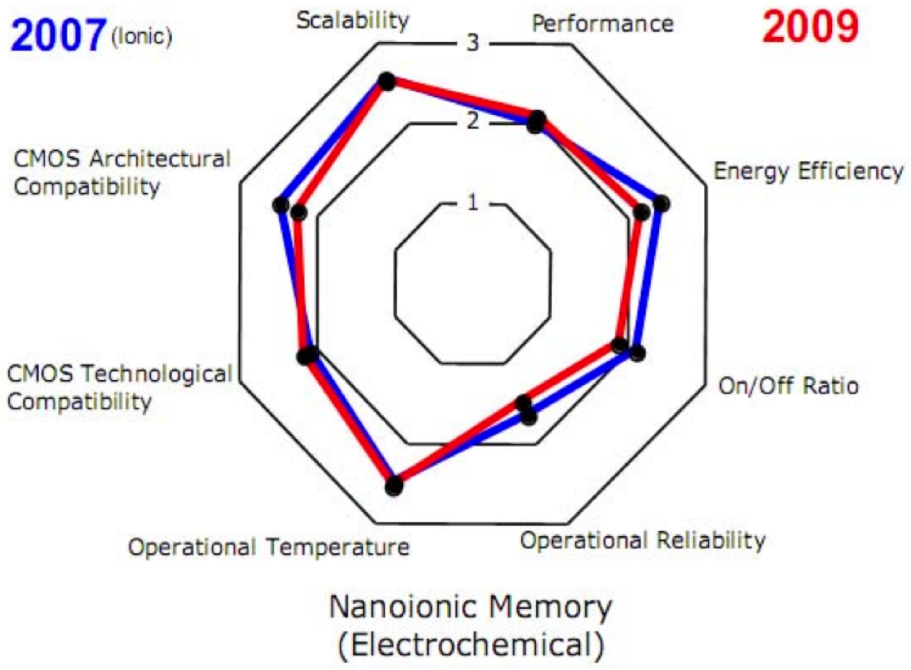

Figure 1.6: Technology performance evaluation for Nanoionic memory in ITRS 2009 [5]

1.5 Solid electrolyte layer in PMC memory cells

Previous section briefly explained the principle behind the PMC memory technology and before explaining the objective of this work it is important to discuss a few considerations on the material selection in PMC memory cells. PMC memory cells fall into a category called Resistive Random Access Memory (RRAM) as they use resistance change in a material (solid electrolyte) to store information (they are also sometimes classified into the Ionic Memory category). Materials for ionic memories generally include a reactive ion and a solid electrolyte layer. The reactive ion in the most common ionic memories is either silver (Ag) or copper (Cu). Many different types of solid electrolytes like metal sulfides, germanium rich solid electrolytes, oxides, etc. [43] have been used. This section mentions briefly about a few common types of electrolyte + reactive ion systems experimented so far.

Silver doped germanium selenide (Ag-Ge-Se)

The most common approach to form a solid electrolyte to be used in a PMC memory cell is to combine chalcogens with germanium and to dissolve Cu or Ag into it. The most common and one of the earliest ternaries formed this way is $Ag_{0.33}Ge_{0.20}Se_{0.47}$, that is essentially a glassy germanium rich backbone mixed with an Ag_2Se phase in the form of dispersed nanoscale superionic regions. The nanostructure of this material leads to a highly stable solid electrolyte that not only has high ion mobility (upto 10^{-3} cm^2/Vs) but also a high resistivity (> 100 Ωcm) [44]. PMC cells formed with silver and this germanium selenide solid electrolyte have been shown to possess impressive memory qualities like ultra-low voltage operation (< 0.5 V), fast switching speeds ($<$ 100 ns), high endurance ($> 10^{11}$ cycles), high dynamic range between the ON and OFF states (10^4 - 10^7), etc., [45].

However though high ion mobility is important for fast device operation, memory cells formed from this material system cannot tolerate processing conditions greater than 200 ^{o}C, since the hosting chalcogenide glass may crystalize in this range [42]. This means that relatively low temperature BEOL processing is necessary for integration with CMOS. Although this is possible with the latest advancements in materials and processing conditions, it adds to the cost of fabrication of these devices. It also poses certain restrictions on their operating temperatures when compared to other material systems.

Silver doped germanium sulfide (Ag-Ge-S)

Another material system similar to the silver doped germanium selenide system discussed in the previous section is silver doped germanium sulfide or $Ag_{0.33}Ge_{0.20}S_{0.47}$. Studies have shown that the mass transport and the internal structure of silver germanium sulfides are similar to that of silver germanium selenides with minor differences [46]. Memory cells based on this material system have been shown to possess excel-

lent thermal stability and be able to withstand the elevated temperatures used in many BEOL processes [39].

Ag-Ge-S devices have also been shown to possess impressive switching characteristics even after processing at 300 ^{o}C in an ambient that has considerable amounts of oxygen. Other characteristics that these devices exhibit are high OFF resistance ($> 10^{11}$ Ω) but very low ON resistance (depending on the current used while programming), and operating voltage < 1 V. Also the switching threshold (~ 450 mV) of these devices were found to be greater than that of selenide based devices (~ 250 mV), yielding a better noise margin. Though the ion mobility in these devices were a factor of 10 lower [46] than their selenide counterparts, their switching speeds have been shown to be < 100 ns [39]. Hence all the above mentioned qualities have made the silver germanium sulfide based PMC cells the most popular of the other systems used so far.

Copper doped silicon-di-oxide (Cu-SiO_2)

Recently copper doped silicon-di-oxide based PMC cells have generated a lot of interest as they have shown similar switching behavior to the Ag-Ge-Se and Ag-Ge-S (or metal-doped chalcogenide) based devices. Oxide based memory cells are of particular importance as SiO_2 based solid electrolytes are highly compatible with the BEOL processing in CMOS integrated circuits where SiO_2 already plays an important role as a dielectric. Also SiO_2 processing techniques are highly compatible with semiconductor processing and include Chemical Vapor Deposition (CVD) and Physical Vapor Deposition (PVD). Moreover copper is widely used in many integrated circuits as an interconnect material and combining this with SiO_2 leads to an inexpensive solid electrolyte material system that can be readily integrated with the CMOS circuitry [47].

Though the exact composition of the conducting pathway in Cu-SiO_2 PMC cells is unknown, electrical measurements and cross-section images have shown that the switching is similar to the metal-doped chalcogenides and that the ON resistance is ohmic in nature. These cells have also been shown to possess promising retention char-

acteristics, switching speeds and the ability to be used in multilevel applications based on the programming currents used [47]. They have also been shown to possess impressive endurance qualities with more than 10^7 cycles [38]. Another interesting ability of these cells is the bipolar switching characteristics they have been shown to possess which the metal-doped chalcogenides do not exhibit. Hence, though a great deal of material and electrical optimization is still required, copper doped silicon-di-oxide devices are promising for CMOS integration as they are based on existing materials in the CMOS process line [47].

Silver and copper doped tungsten oxide (Ag-WO_3 and Cu-WO_3)

Tungsten is a popular material in CMOS integrated circuit industry as tungsten plugs provide the required vertical connection between the horizontal running wiring that is made of copper [48]. Hence memory cells made of tungsten provide an excellent opportunity for higher density memory in a typical CMOS BEOL process. Initial results showed that structures based on WO_3-Cu sandwiches provided a strong medium for preparation of PMC memory cells [49]. A transition metal like tungsten (W) can be reacted with oxygen to form a base glass for the solid electrolyte [50] and if the formed tungsten oxide is porous in the trioxide (WO_3) form then the silver or copper ions can form electrodeposits in it, to function as a PMC memory cell.

Various quasi-static measurements have shown the potential of both Ag-WO_3 and Cu-WO_3 to be successfully used as PMC memory devices. Though the electrical behavior of these cells differed slightly from the metal-doped chalcogenide devices discussed previously, the basic underlying switching mechanism was found to be electrochemical in nature. These devices exhibited high OFF resistance ($> 10^{10}$ Ω) and ON resistance close to 10^5 Ω for a programming current of 1 μA [51].

There are other material systems that are also being investigated for similar electrochemical switching behavior such as Ag-Cu_2S [52], Cu-Cu_2S [53], Cu-GeS [39], Cu-Ta_2O_5 [54], Ag-TiO_2 [55] and Ag/Cu/Zn-ZnCdS [56], but as mentioned previously

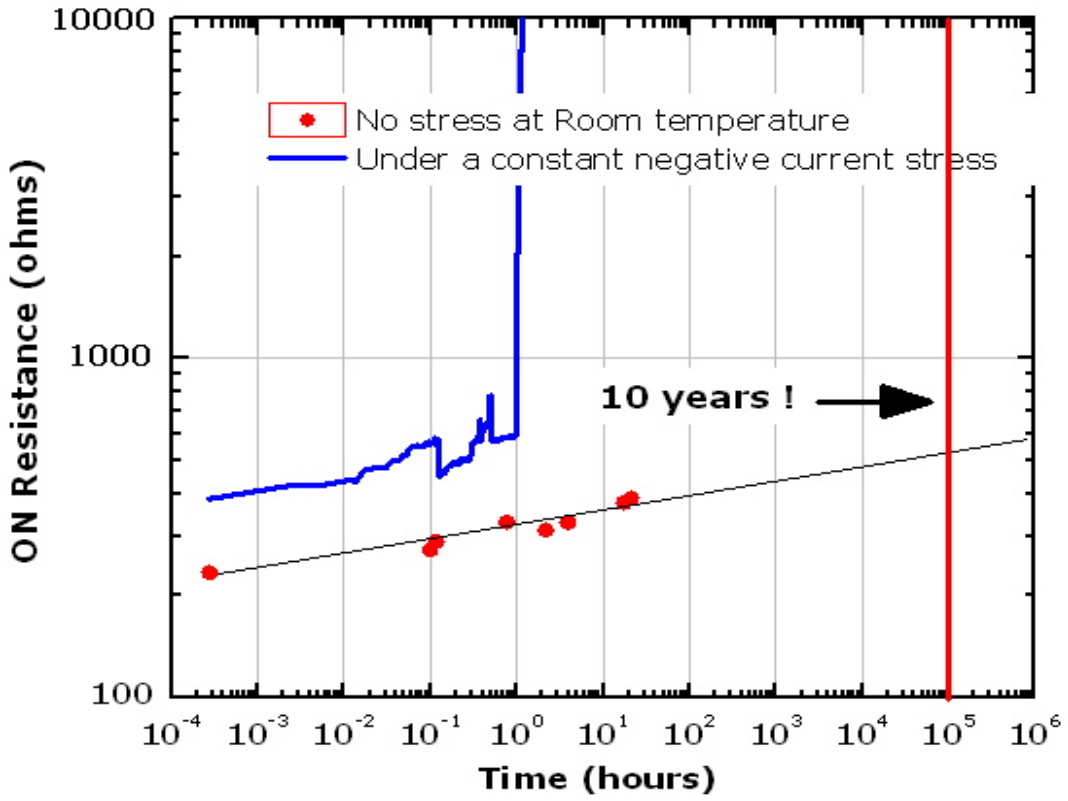

Figure 1.7: Stability of the low resistance state measured for around twenty hours and extrapolated to more than ten years and the effect of constant negative current stress on the low resistance state

metal-doped chalcogenides have gained the most attention of all these systems. This work concentrates on PMC memory cells based on silver germanium sulfide or Ag-Ge-S material system and all the results shown in this work are from experiments on devices based on this material system.

1.6 Reliability of PMC devices

Fig. 1.7 shows the low resistance state of a Ag-Ge-S PMC cell programmed at 1 mA compliance current. The low resistance state was monitored (using a read voltage of less than 50 mV in amplitude) for around twenty hours at room temperature and then extrapolated to ten years as shown. The low resistance state hardly changed and was less than three times the initial resistance at the end of ten years when extrapolated. However there was a gradual increase in the low resistance with time. Though projec-

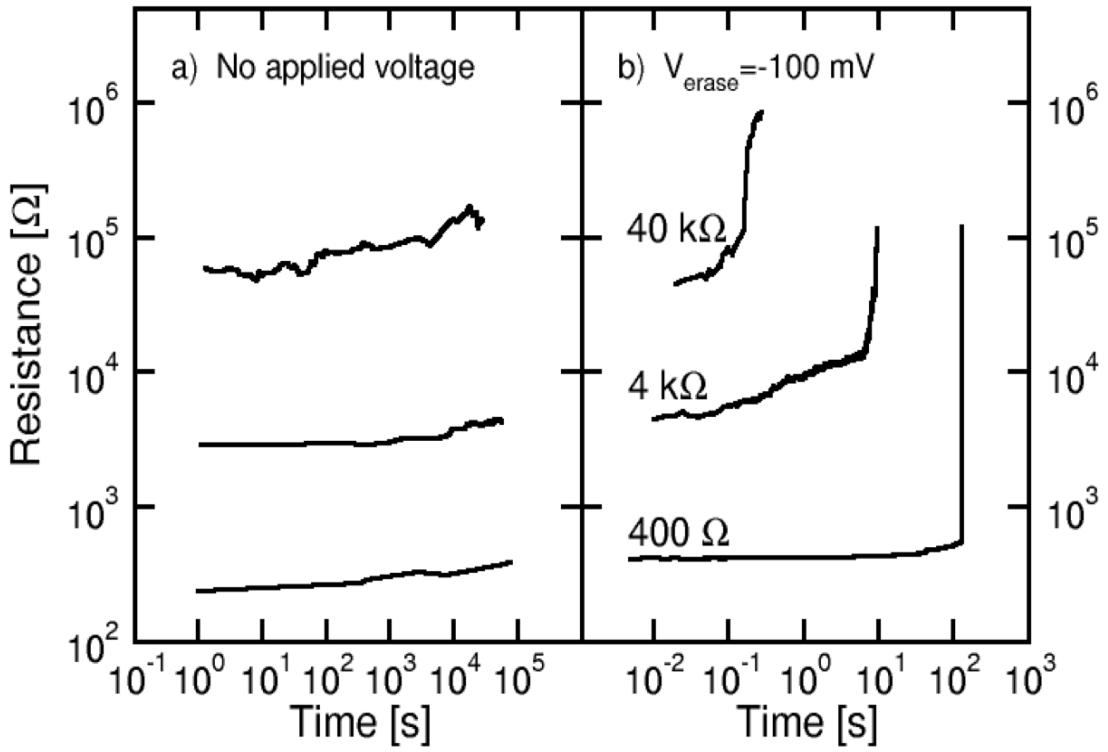

Figure 1.8: Measurements of different programmed states at room temperature (a) under no stress, (b) under a negative voltage stress of 100 mV. For the ON states, R_{ON} values of 400 Ω, 4 kΩ and 40 kΩ were obtained with compliance currents of 1 mA, 100 μA and 10 μA, respectively.

tion by extrapolation is a common practice in the memory industry as it is impossible to measure a resistance state up to ten years, it is not accurate as seen from the other plot in the same figure, which shows the low resistance state under a constant negative current stress. After some time under constant negative current stress the resistance of the device increases by several orders of magnitude to a higher value, to its OFF state from the low resistance ON state. Hence this device was noted to have failed under a constant negative current stress for almost an hour and in this work any change in the resistance state (that was being monitored for stability) by one order of magnitude or a factor of ten was considered to be a failure. Fig. 1.7 also shows that failure does not occur as gradually as in the case under no stress and it occurs rather abruptly.

The resistance vs time behavior is also consistent for different levels of ON

states. Fig. 1.8 illustrates the measured PMC cell resistance R_{ON} (ON state resistance) as a function of time at room temperature, (a) without and (b) with an applied bias V_{erase} = -100 mV, as measured with a semiconductor parameter analyzer. Three different levels of R_{ON}s are compared, which were obtained by tuning the compliance current during the programming operation [5]. For a 2 bit multilevel cell, the fourth level corresponds to the OFF state, whose resistance is stable and larger than 1 MΩ. From the figure, the ON state R_{ON} slightly increases for increasing time. It can be seen than the behavior of different ON states with and without stress is different. Hence though the increase in low resistance state under no stress (when extrapolated) was much less than half an order of magnitude from the initial resistance state, it is important to understand the underlying physical mechanism behind this increase in the low resistance state under no stress and also the effect of stress on the low resistance state.

1.7 Thesis outline

This work investigates resistance stability by means of monitoring different resistance states under normal and under extreme stress conditions (temperature and electrical). It also investigates resistance stability by means of voltage-accelerated measurements in particular, where a (range of) constant voltage stress (like V_{erase} = -100 mV in Fig. 1.8b) is applied to the Ag electrode, i.e. in the direction of erasing the device. Voltage-accelerated tests are also useful to assess the feasibility of PMC devices as signal path elements in programmable logic array (PLA) applications [57, 58].

With the stability of different resistance states analyzed under both (normal and) extreme stress conditions and developing a model for both program [6] and erase [59] process the next step was to investigate the Program Erase (PE) cycling of PMC cells. In particular emphasis is laid on ultra low voltage operation during cycling under different currents for more than 10^4 cycles. The trade-offs involved in using higher currents and a significant margin between the ON and the OFF states during cycling is also analyzed in this work.

Hence the purpose of this work is to 1) identify the possible mechanism(s) in PMC devices that cause the gradual increase in the low resistance state under no stress with time, 2) Identify the failure mechanism(s) under different types of stress and to investigate the stability of different low resistance states in PMC devices which is essential to establish their ability to be successfully used in multilevel programming applications and to 3) Investigate the feasibility of low voltage cycling of PMC cells.

The initial part of this work introduces the PMC technology, the basic science and the processing involved, followed by a detailed qualitative discussion of the working of PMC devices, which is necessary for the other part of the work. Various electrical results and discussions of various stressing experiments under different conditions are presented thereafter.

Chapter 2

DEVICE STRUCTURE, FABRICATION AND OPERATION

2.1 Device structure

A simple structure of a PMC device is shown in Fig. 2.1. It consists of a stack of three primary layers, the anode, the cathode and a sandwiched solid electrolyte on a silicon substrate insulated by a dielectric.

The thickness of the silver doped glass was ∼60 nm and that of the top electrode silver was ∼35 nm. The dimension of the devices varied from 5 μm to ∼ 100 nm. However the devices used in this work were restricted to dimensions greater than 500 nm. The basic test structures with the vias defined on the dielectric with the tungsten bottom electrode on a silicon substrate, were provided by Qimonda (a memory company split out of Infineon Technologies Ltd.). The cathode contact and the glass stack deposition with the top electrode were done at the Center for Solid State Electronics Research (CSSER) in Arizona State University (ASU). Fig. 2.2 shows the top view

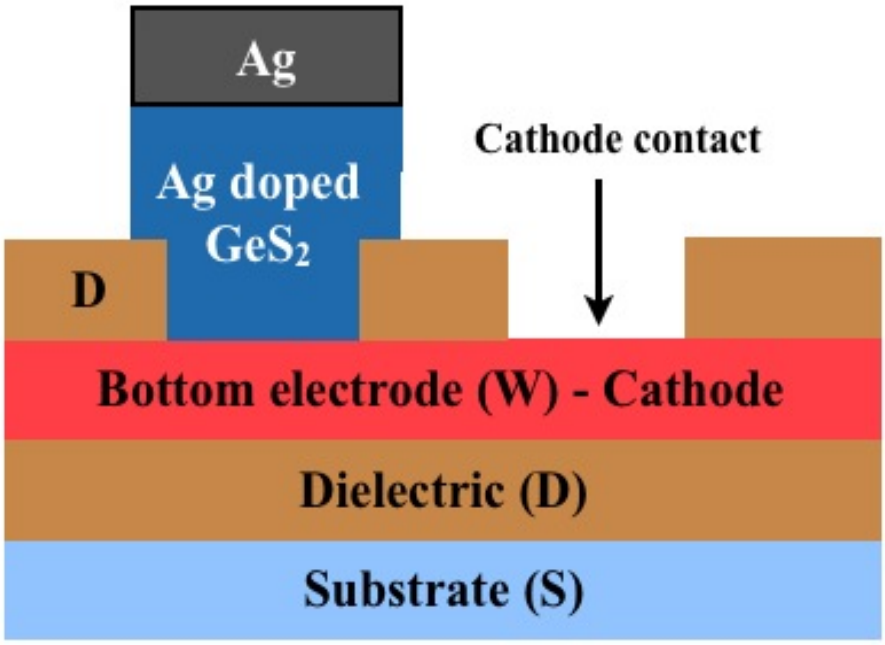

Figure 2.1: Simple layered structure of a PMC memory device

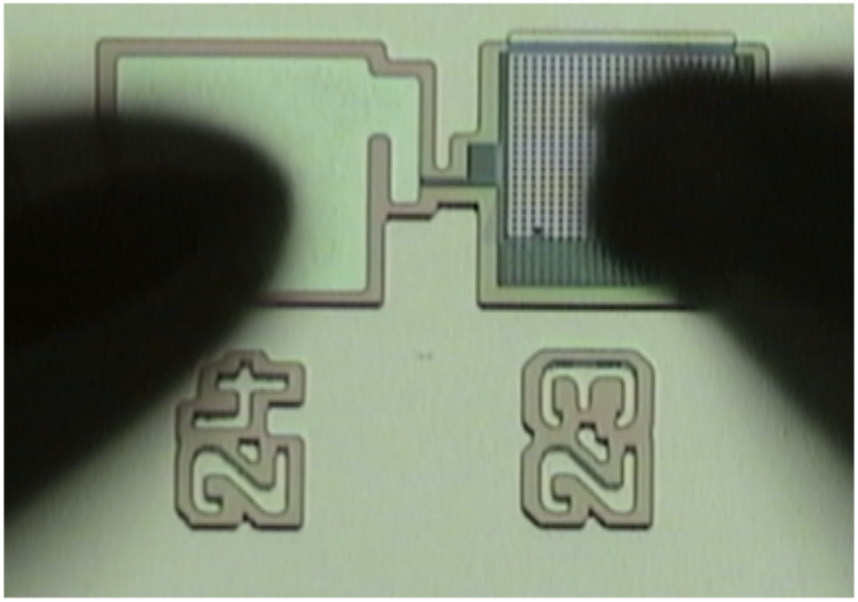

Figure 2.2: Top view of a PMC test structure with both electrodes contacted with tungsten probe tips

of a PMC test structures used in this work. Pad on the left is the anode pad and was covered with silver and the pad on the right is the cathode pad (tungsten). The area of intersection of these two is the active device region.

2.2 Process steps

After depositing the tungsten bottom electrode and the overlying silicon nitride layer (done by Qimonda) there are three main phases in fabricating a PMC device; cathode lithography, anode lithography and the glass stack deposition (done at CSSER in ASU).

Cathode lithography

This phase began with spinning Hexamethyldisilazane (HMDS adhesion promoter) and AZ 3310 at 3500 rpm for thirty seconds each to get a resist layer of thickness of around 2 μm. The wafer was then soft baked at 100 ^{o}C for sixty seconds. The resist was patterned using the karl suss aligner by exposing it for fifteen seconds at 4 - 5 mW/cm^2. Then the resist was developed with AZ 300 MIF for thirty-five seconds. The exposed silicon nitride layer was etched to make contact to the underlying tungsten layer by

reactive ion etching in fluorine ambient for seven minutes at approximately 250 $\mathring{A}$/s Finally the remaining resist and adhesive were stripped off using acetone.

Anode lithography

Anode lithography began with the same procedure as the cathode lithography where the adhesion promoter and the resist were spun at 3500 rpm for thirty seconds and the sample was then soft baked. The resist was patterned for glass stack deposition using the karl suss aligner by exposing it for fifteen seconds at 4 - 5 mW/cm^2. After developing the resist, the sample was loaded into Edwards I, a thermal vapor deposition system for the glass stack deposition, without stripping it.

Glass stack deposition

This stage began with the deposition of a 60 nm of Germanium Sulfide (GeS_2) layer at a rate of $\sim$ 1 $\mathring{A}$/s. This was followed by an in-situ deposition of a 30 nm layer of silver again at the same rate. The sample was then radiated with UV rays of $\sim$5 mW/cm^2 for twenty minutes to drive silver into the glass to form conductive nano-phases that are separated by $<$ 1 nm from each other [34]. The sample was again loaded into the thermal vapor deposition chamber of Edwards I for depositing a 35 nm silver top electrode layer. Finally the resist and the remaining HMDS were lifted off using acetone. This was followed by a fifteen minutes annealing at 300 ^{o}C in nitrogen ambient as annealing has been found to improve the performance of the germanium sulfide based devices particularly their retention capability [40]. Fig. 2.3 to Fig. 2.9 explains the fabrication steps involved in processing PMC devices discussed so far.

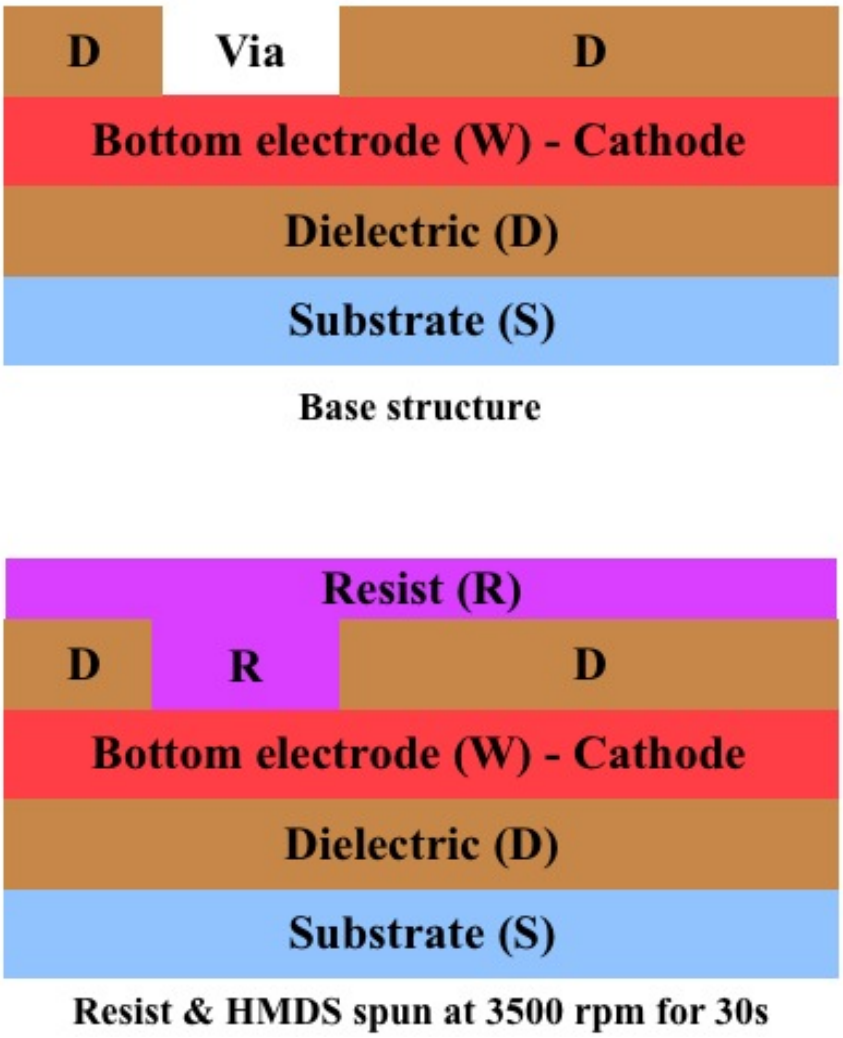

Figure 2.3: Process steps in PMC fabrication: Starting base structure provided by Infineon technology Ltd. is shown on the top

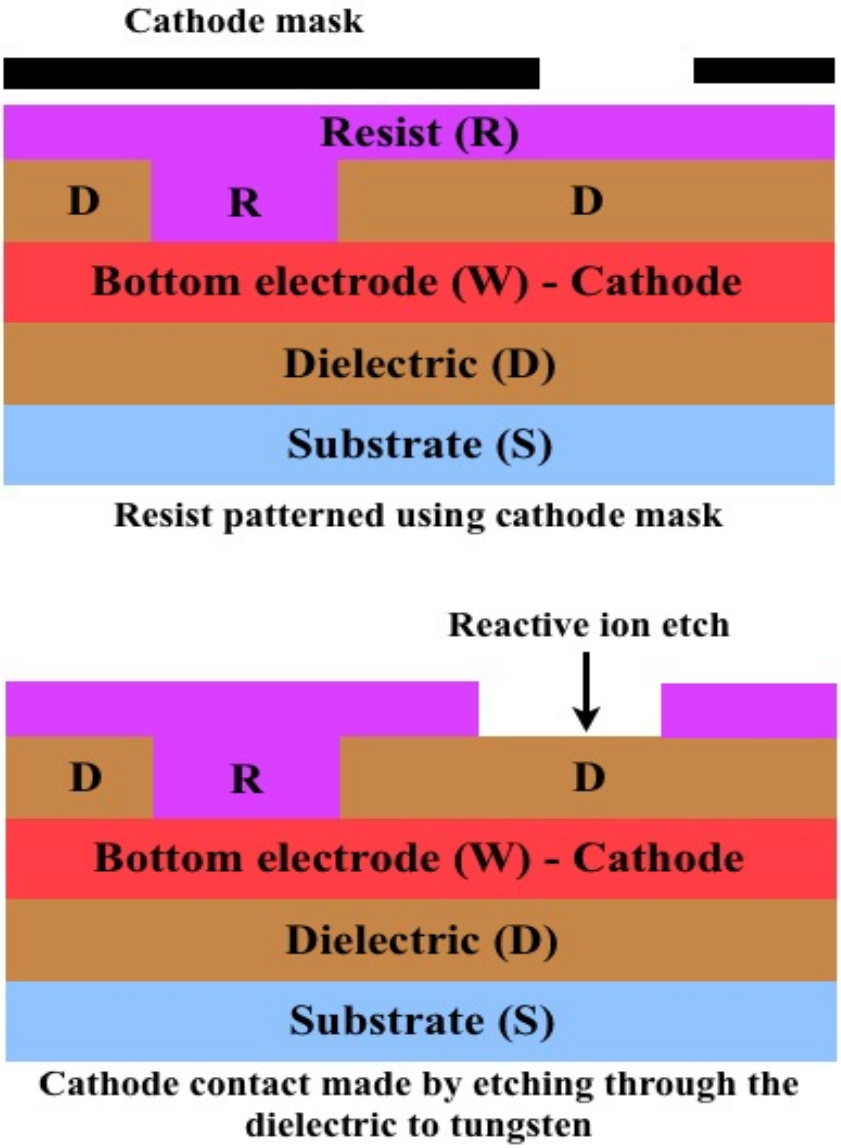

Figure 2.4: Process steps in PMC fabrication (cont.): Cathode lithography proceeds

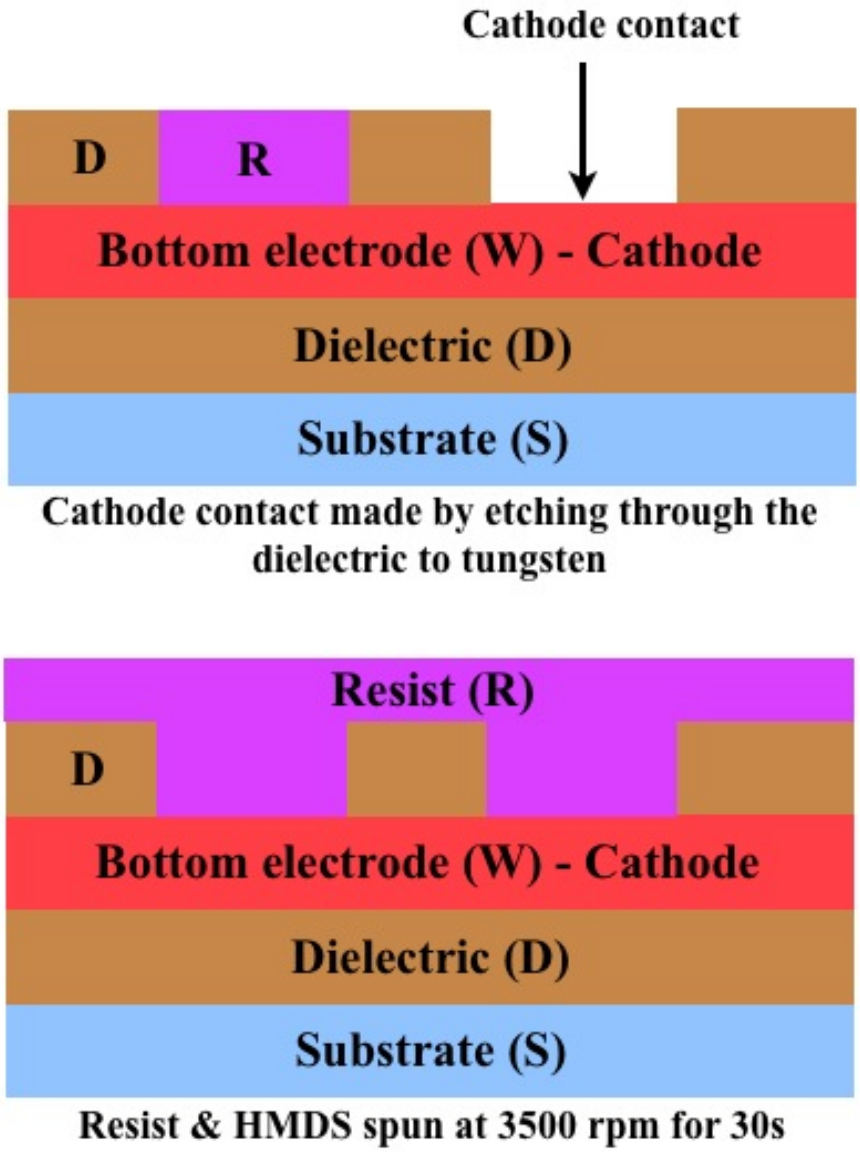

Figure 2.5: Process steps in PMC fabrication (cont.): Anode lithography begins

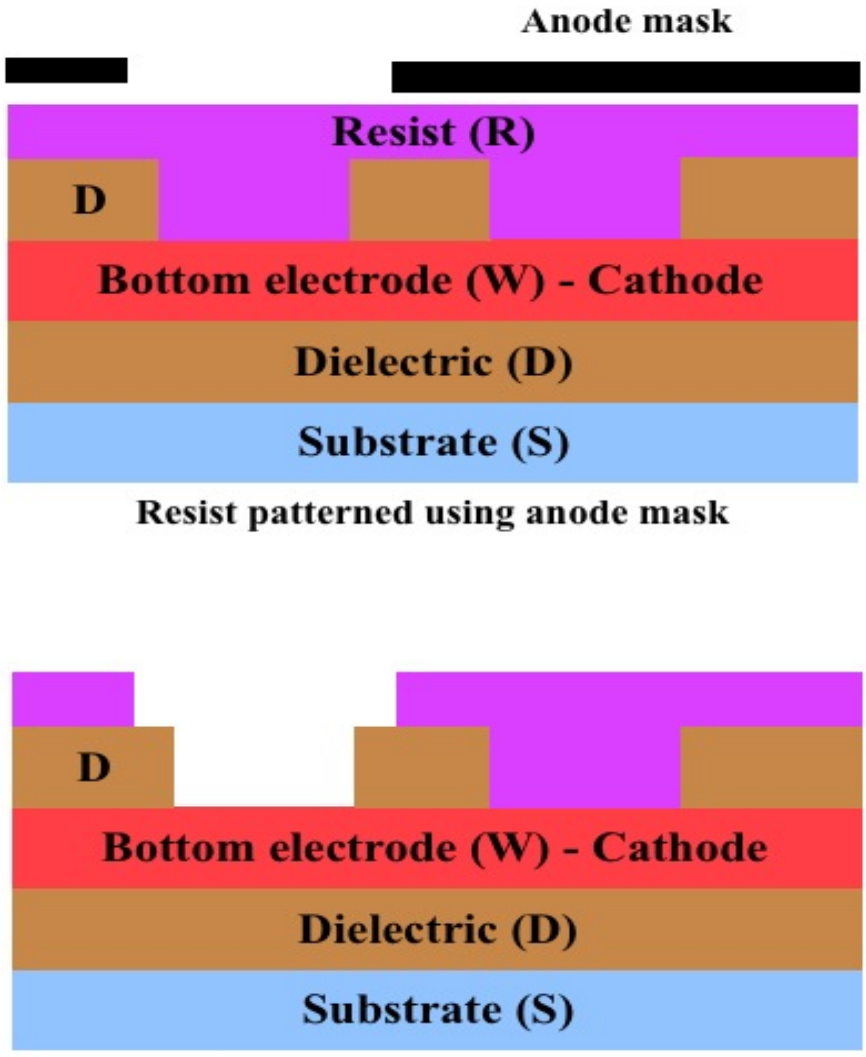

Figure 2.6: Process steps in PMC fabrication (cont.): Anode lithography proceeds

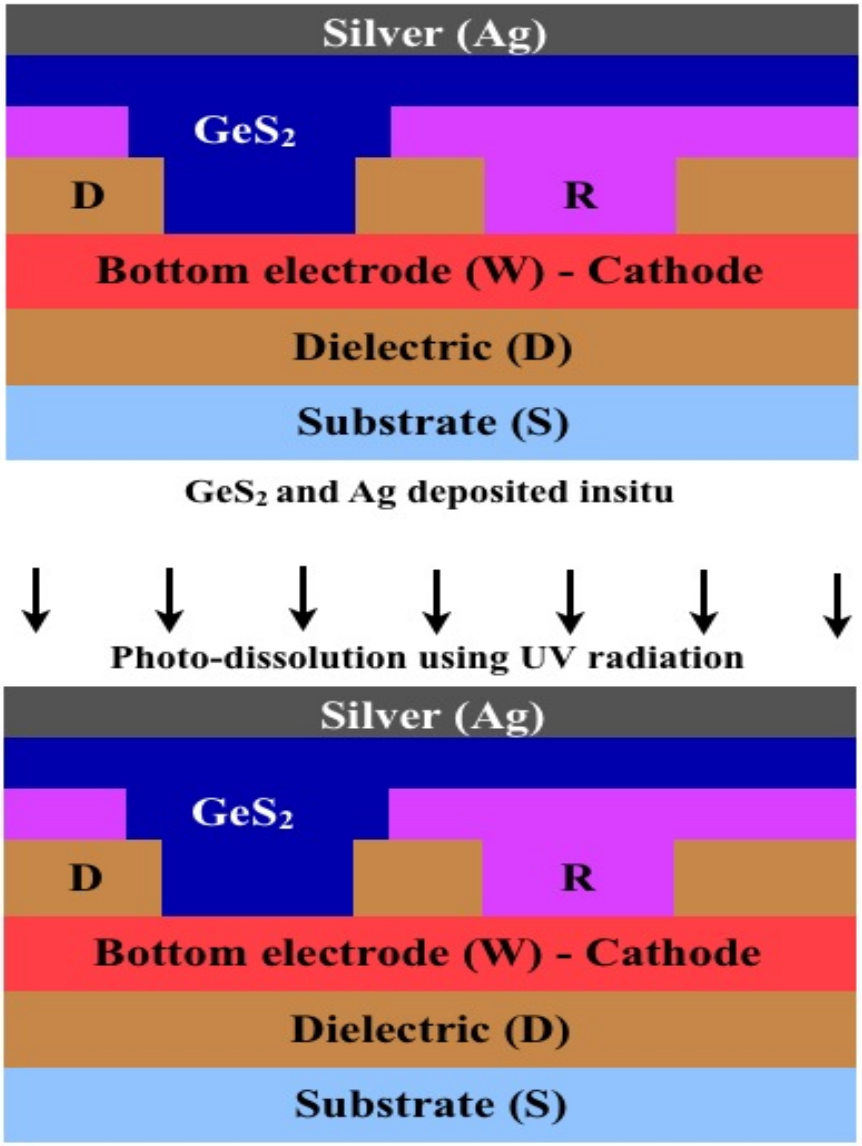

Figure 2.7: Process steps in PMC fabrication (cont.): Glass and silver in-situ deposition

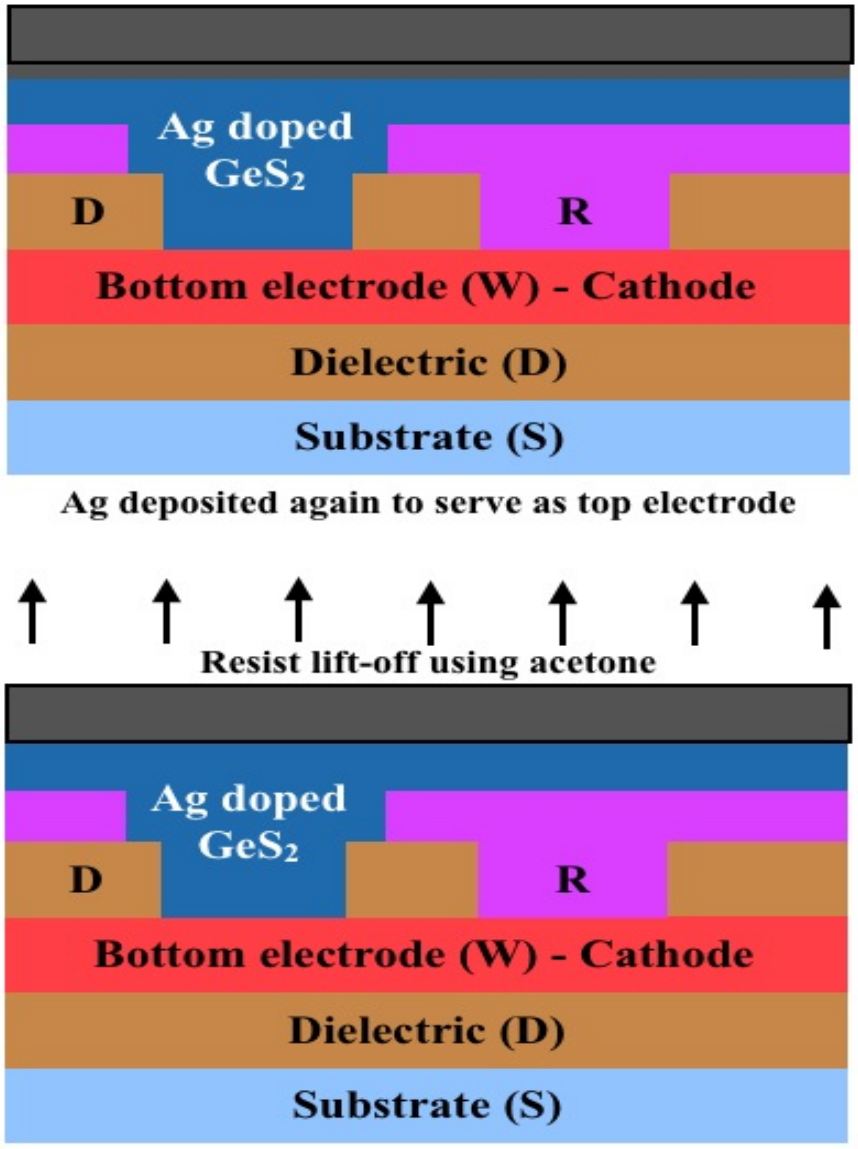

Figure 2.8: Process steps in PMC fabrication (cont.): Top electrode deposition

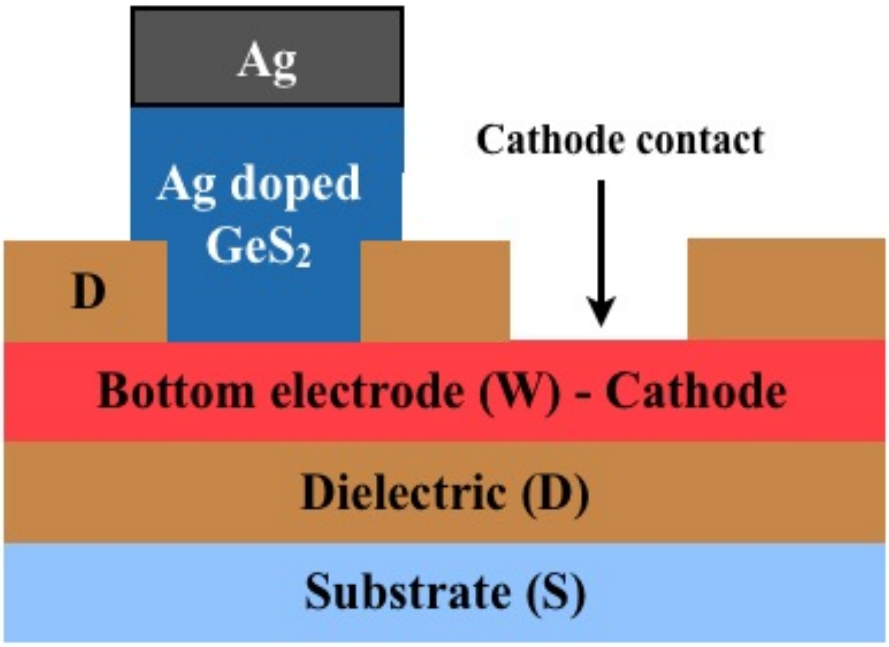

Figure 2.9: Process steps in PMC fabrication (cont.): Final structure after resist lift-off

2.3 Device operation - Basic

The operation of a PMC memory cell is based on the electrochemical rearrangement of nanoscale quantities of metal through a solid electrolyte sandwiched between two different metals. The two metals (in devices used in this work) are silver and tungsten and the electrolyte is silver doped, sulfur rich germanium sulfide, $\sim Ag_{40}$ $(Ge_{33}$ S_{67} $)_{60}$.

When no bias is applied across the two electrodes, since the conductive nanophases of doped silver in the solid electrolyte are discontinuous, the resistivity of the electrolyte is very high and the read voltage of a few tens of millivolts (< 50 mV) results in negligible current flow or very high off state resistance (> 1 GΩ) that depends inversely on the cell area [41].

When a positive voltage of few hundreds of millivolts (~ 450 mV for Ag-GeS devices) is applied across the two electrodes, silver ions from the oxidizable anode get oxidized and start drifting towards the cathode through the solid electrolyte, under the influence of the electric field. Once the silver ions enter the solid electrolyte, they move in coordinated motion as shown in Fig. 2.11 and Fig. 2.12 and the silver ion closest to the cathode where the electric field is the highest accepts an electron provided by the cathode to get reduced and gets deposited on the cathode as a silver atom. This process continues till a metallic electrodeposit is formed in the electrolyte bridging the two electrodes. Now the resistance falls drastically to a low value (depending on the compliance current set for protecting the device), giving rise to the low resistance or the ON state Fig. 2.13.

To erase the device an erase voltage of a few hundreds of millivolts ($\sim$150 mV for Ag-GeS devices) is applied in the opposite polarity (cathode being more positive with respect to the anode). The silver atoms in the conductive filament get oxidized and drift to the anode through the solid electrolyte under the erase electric field and get reduced and deposited on the anode (Fig. 2.14 and Fig. 2.15) giving back the initial high

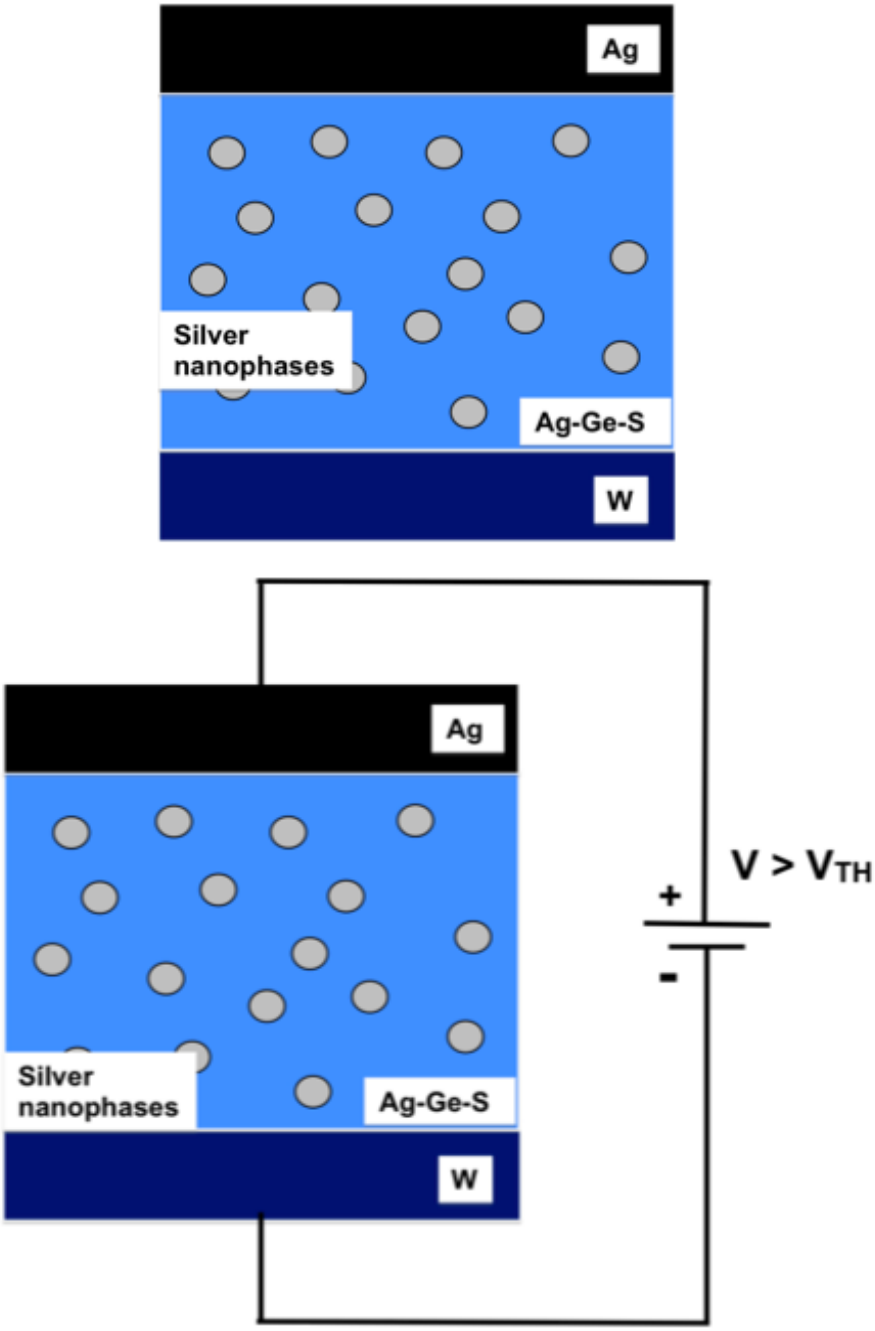

Figure 2.10: Operation of PMC devices

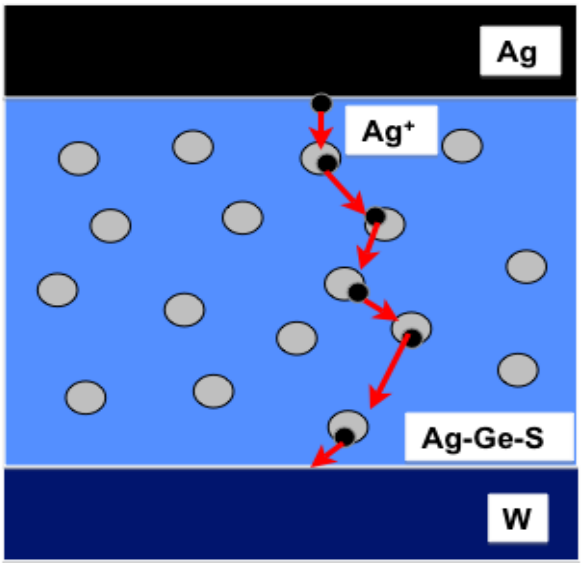

Figure 2.11: Operation of PMC devices (cont.); Silver ions from the nanophases separates out and moves towards cathode to get reduced, as the silver ions came in from the anode and they move in a coordinated fashion.

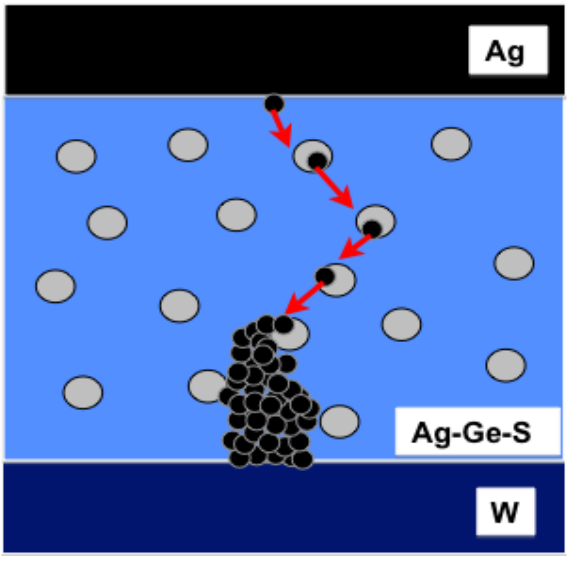

Figure 2.12: Operation of PMC devices (cont.); Once the electrodeposit starts growing the in- coming silver ions reduce and deposit at the tip of the growing electrodeposit as the electric field is most favorable there, aiding in the growth of a single continuous electrodeposit.

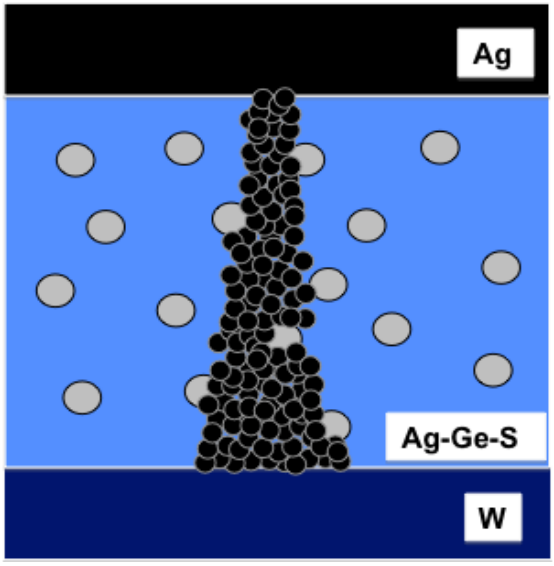

Figure 2.13: Operation of PMC devices (cont.); A metallic bridging electrodeposit that remains even after the voltage source is removed.

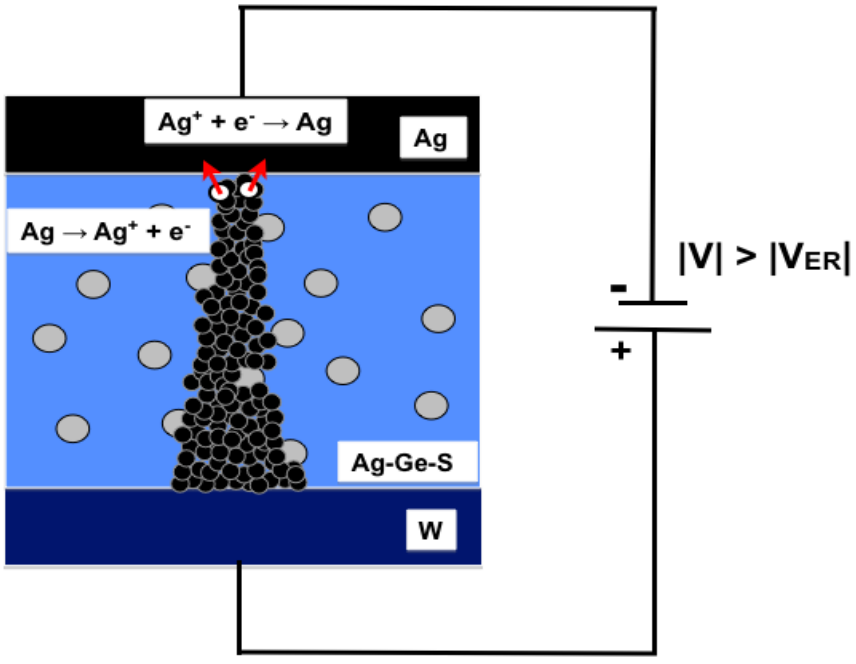

Figure 2.14: Operation of PMC devices (cont.); Silver atoms from the electrodeposit start get oxidized and drift towards the anode, where they combine with electrons to get reduced.

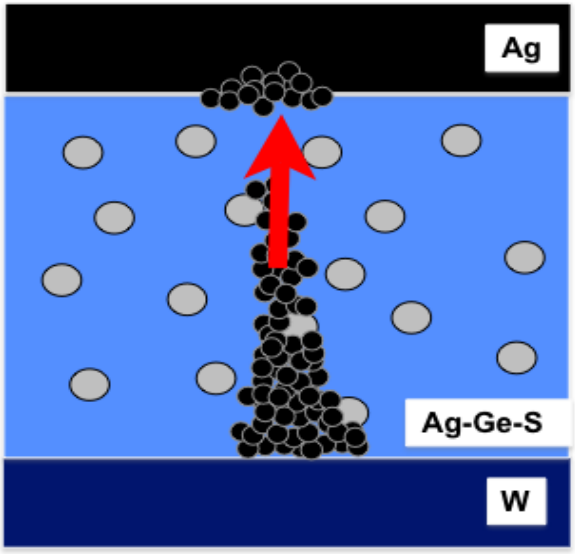

Figure 2.15: Operation of PMC devices (cont.); This process continues till all silver in the electrodeposit has been re-deposited at the anode.

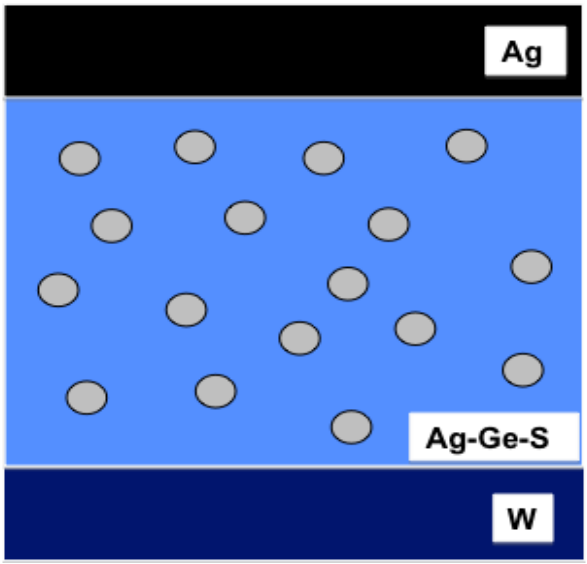

Figure 2.16: Operation of PMC devices (cont.); The high resistive state is restored at the end of the erase process.

resistive state. An important consideration for the device to not to re-write under the erase voltage is that the cathode has to be relatively indifferent (electrochemically) with respect to the anode (as tungsten is with respect to silver). This ensures the termination of the erase process as soon as all the silver from the conductive filament is deposited back at the anode and no more deposition of the cathode metal occurs.

2.4 Device operation - Ion conduction

As shown in Fig. 2.11 and Fig. 2.12, once a silver ion enters the solid electrolyte, it does not have to travel the entire depth of the electrolyte layer (600 $\mathring{A}$). The flow of ions happens in a coordinated motion as one ion replaces another in a vacancy as it becomes available. And when the electrodeposit starts growing towards the anode, the highest electric field is between the tip of the growing electrodeposit and the anode and hence further deposition takes place at the tip enhancing the electrodeposit growth. Also since the metal doping of the solid electrolyte is not subtle and is almost 50% by atomic weight [60] the ion mobility in the electrolyte is very high and hence these devices are extremely fast.

Ion conduction in solid most electrolytes occurs through defects. Similar to electronic conduction there are two energy levels, normal and interstitial that are separated by an energy gap. No conduction occurs in the solid electrolyte if all the normal energy level sites are filled with ions. At room temperature some of the ions occupy the interstitial energy levels by acquiring enough energy to overcome the energy gap. Conduction now occurs through the ions hopping over the barriers to move through different interstitial states [61]. Fig. 2.17 shows the qualitative energy diagram for ion conduction in most solid electrolytes. When there is no external energy ions occupy energetically most stable states with the lowest energy. When an external voltage is applied, the slope (or the electric field) tends to decrease the barrier to the ions and the ions migrate according to the applied electric field [61].

From this simple model the dependence of ion conduction on the applied volt-

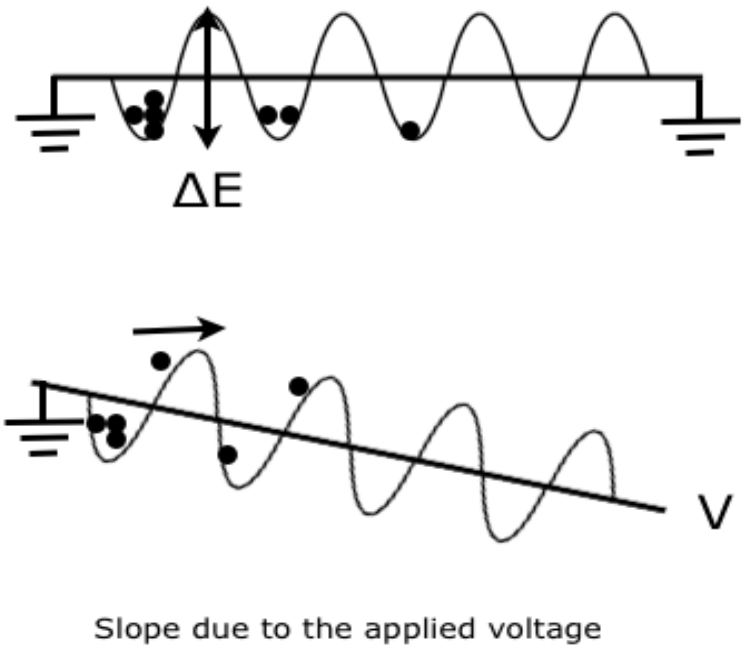

Figure 2.17: Qualitative diagram of ion conduction mechanism in most solid [6]

age is exponential of the form $e^{-\alpha V/kT}$, where α is a correction factor, V is the applied voltage and T is the temperature. Fig. 2.18 shows the dependence of the time for a PMC device to be programmed with voltage pulses of different magnitudes. It can be seen that this dependence is exponential and is in correlation (to the first order) to the fore mentioned theory and hence ion migration under applied electric field was found to be the most significant mechanism responsible for the write process [6].

An approximate model of the write process in PMC devices suggests two distinct stages in the growth of the conductive filament; build up and radial growth. Fig. 2.19 shows the voltage developed across the PMC devices as a function of time during the programming process, where there is a sudden drop in the voltage (due to the decrease in resistance) initially followed by a more gradual drop [6]. Since it is already known that devices programmed with higher compliance currents yield lower ON state resistances [5], from Fig. 2.19 it is fair to conclude that conductive filament formed with a high compliance current is thicker (comprising of more silver) than one written with a lower compliance current.

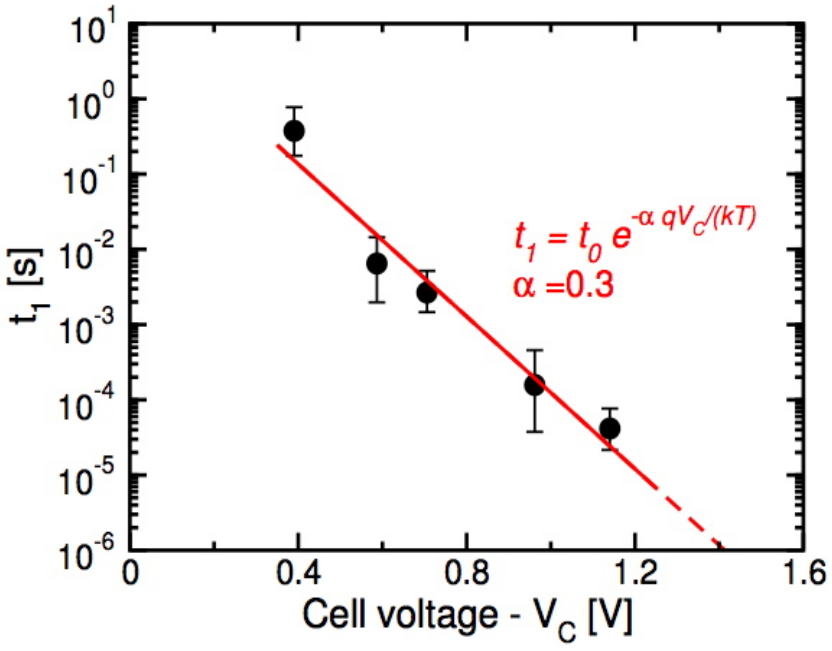

Figure 2.18: Dependence of the time for the device to be written with voltage pulses of different magnitudes [6]

Fig. 2.20 shows a voltage sweep used to electrically characterize PMC devices. The voltage across the two electrodes was swept from -1 V to +1 V and back to -1 V and the current and from it the resistance were monitored. When the voltage was less than the threshold voltage (0.45 V in Ag-GeS) the resistance was very high (of the order of 10^{11} Ω); this was the high resistance or the OFF state. When the applied voltage was greater than the threshold voltage, the device switched to a low resistance state (of around 10^{5} Ω) and the current reached the compliance (here 10 μA); this was the ON state. While the OFF resistance depends on the dimensions of the device (based on the equation R = ρD/A, where ρ is the resistivity, D the depth of the cell, A the area of the cell), the ON resistance depends on the compliance set based on $R_{ON} = V_{TH} / I_{COMP}$, where V_{TH} is the threshold voltage and I_{COMP} the compliance current. This threshold voltage, called the secondary threshold was lesser than the primary threshold and was found to be the minimum voltage required to sustain electrodeposition. For example in the above case the compliance current was 10 μA and hence the R_{ON} was

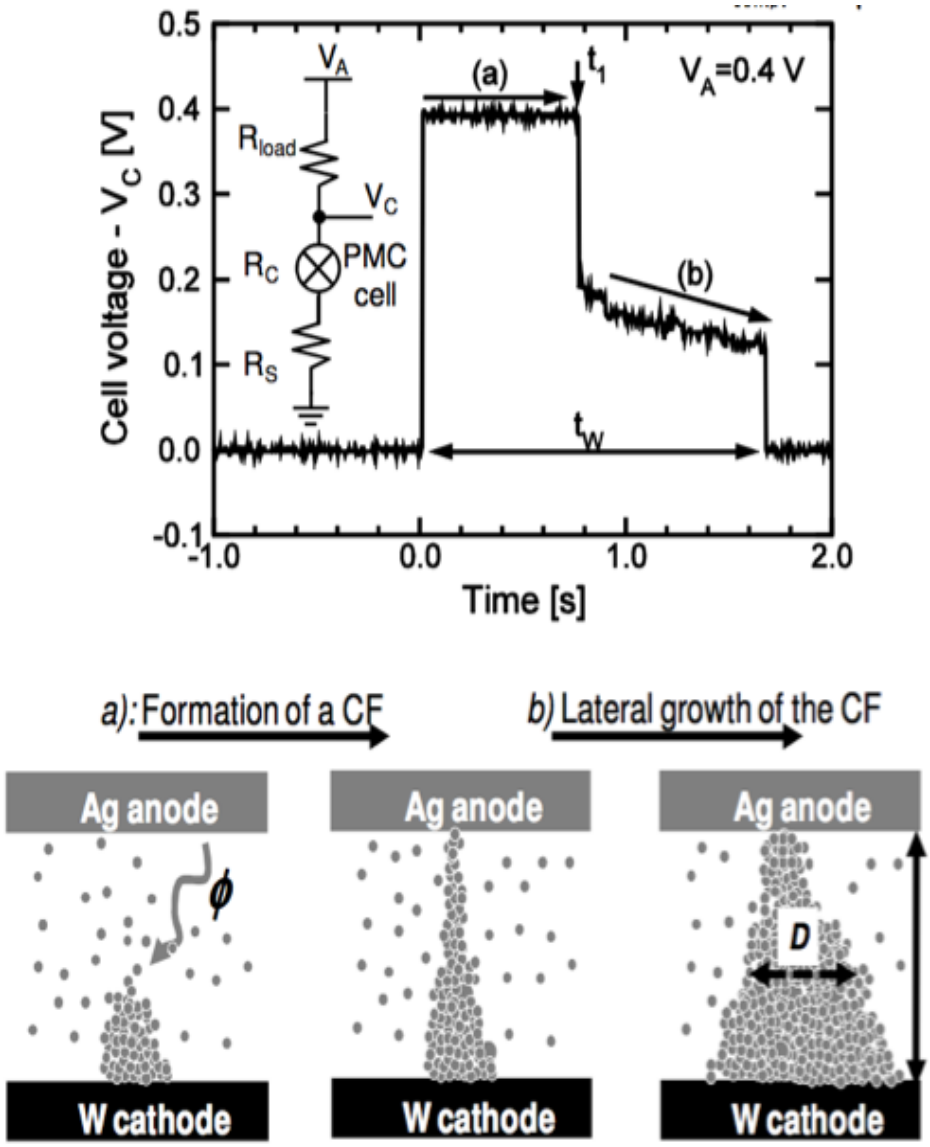

Figure 2.19: Voltage developed across the PMC devices as a function of time during a write process, where there is a sudden drop in the voltage (due to the decrease in resistance) initially followed by a more gradual drop [6]

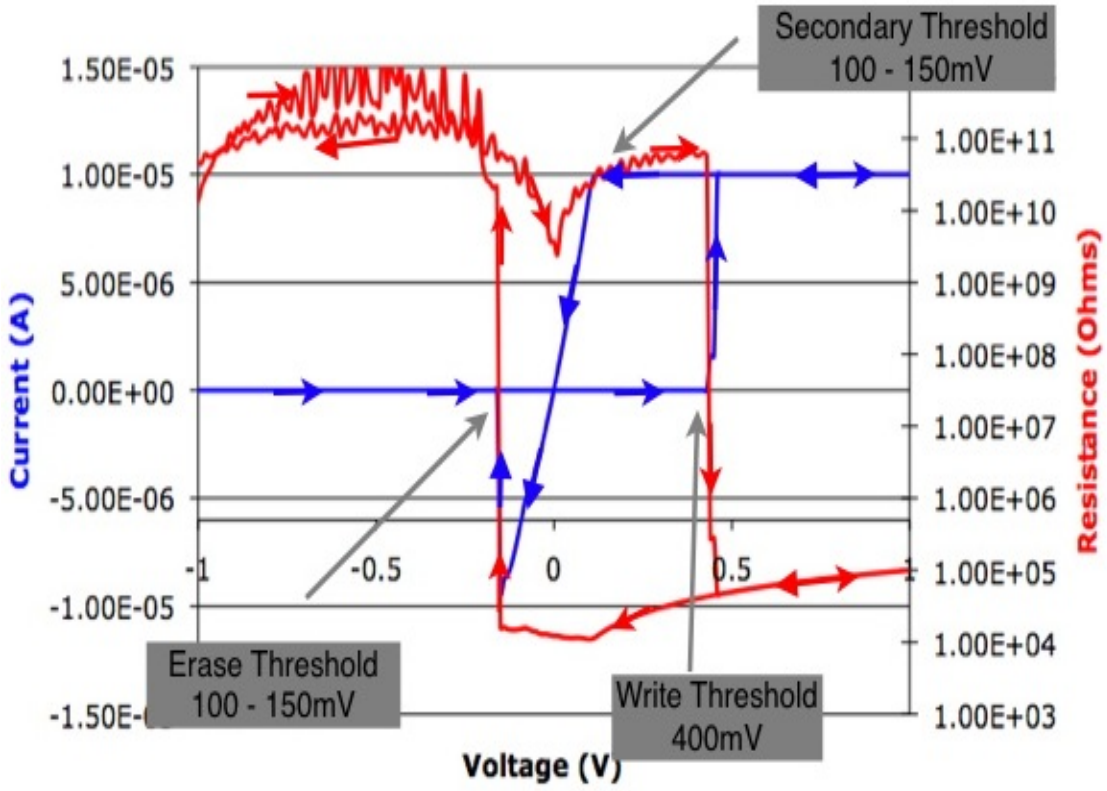

Figure 2.20: Current and resistance variation with a double voltage sweep from -1 V to 1 V.

$<$3 kΩ (0.2 / 10 μA). The erase voltage was $\sim$150 mV in the reverse direction.

Chapter 3

RETENTION TESTS

3.1 Introduction

An important property of any memory device is its ability to retain its logic state under both normal and abnormal conditions such as under a read disturb/noise in the control circuits. Normal conditions here refer to situations where no electrical stress is applied across the device (in any logic state) other than the read voltage, which is set low enough to not to affect the state of the device. Typically in a memory device this voltage is periodically pulsed to sense the state of the device by measuring its resistance. However the major part of this chapter concentrates on constant current/voltage stress at both room and elevated temperatures. This is unusual for memory arrays as the voltage is always pulsed for write, erase or read operations and constant current/voltage stress at elevated temperatures are abnormal conditions for the working of memory arrays. While endurance of a memory device can be tested by repeated programming and erasing at high frequencies, retention testing takes longer times and since it is not practical to measure the logic state of device for years (to establish the retention capability), the failure/aging mechanism under analysis is generally accelerated by stress (electrical, mechanical or thermal, depending on the technology). Hence the harsh stressing conditions used in this work were more a tool to assess the stability and to accelerate the failure mechanism(s) to allow them to be seen in a more reasonable timeframe.

Accelerated failure analysis is very common in memory industry and a lot of work related to FLASH in analyzing its Stress Induced Leakage Currents (SILC) have been done and are in progress. Since the gate is insulated from the channel in a FLASH cell the applied stress has to be a voltage stress that accelerates the tunneling mechanism increasing the leakage currents with thinner oxides [62, 63, 64]. Another class of emerging non-volatile memory technology, Phase Change Memory (PCM) also has a lot of work related to accelerated failure tests. Temperature plays the most important

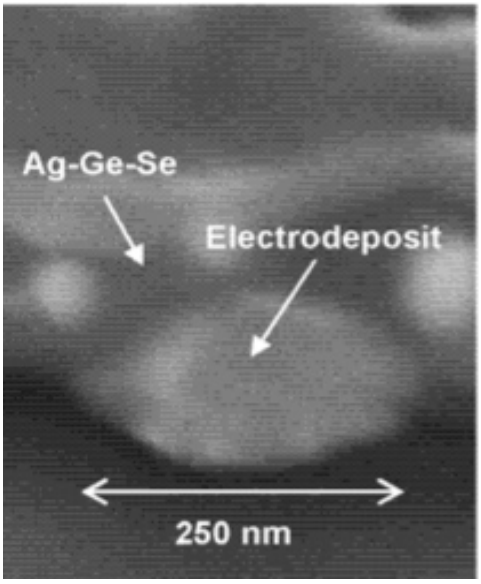

Figure 3.1: An SEM image of the cross section of a PMC device showing the conical electrodeposit [7]

role in a PCM device, i.e, for programming it by varying the physical nature of the active chalcogenide layer involved (temperatures greater than 1000 K are required for reset programming). Hence program disturb issues have been a major concern in the reliability of these devices where the temperature increase in one cell (used to program it) could cause a spurious write in an adjacent cell. A lot of work related to temperature accelerated failure mechanisms and read disturbs in these devices have been published [65, 66].

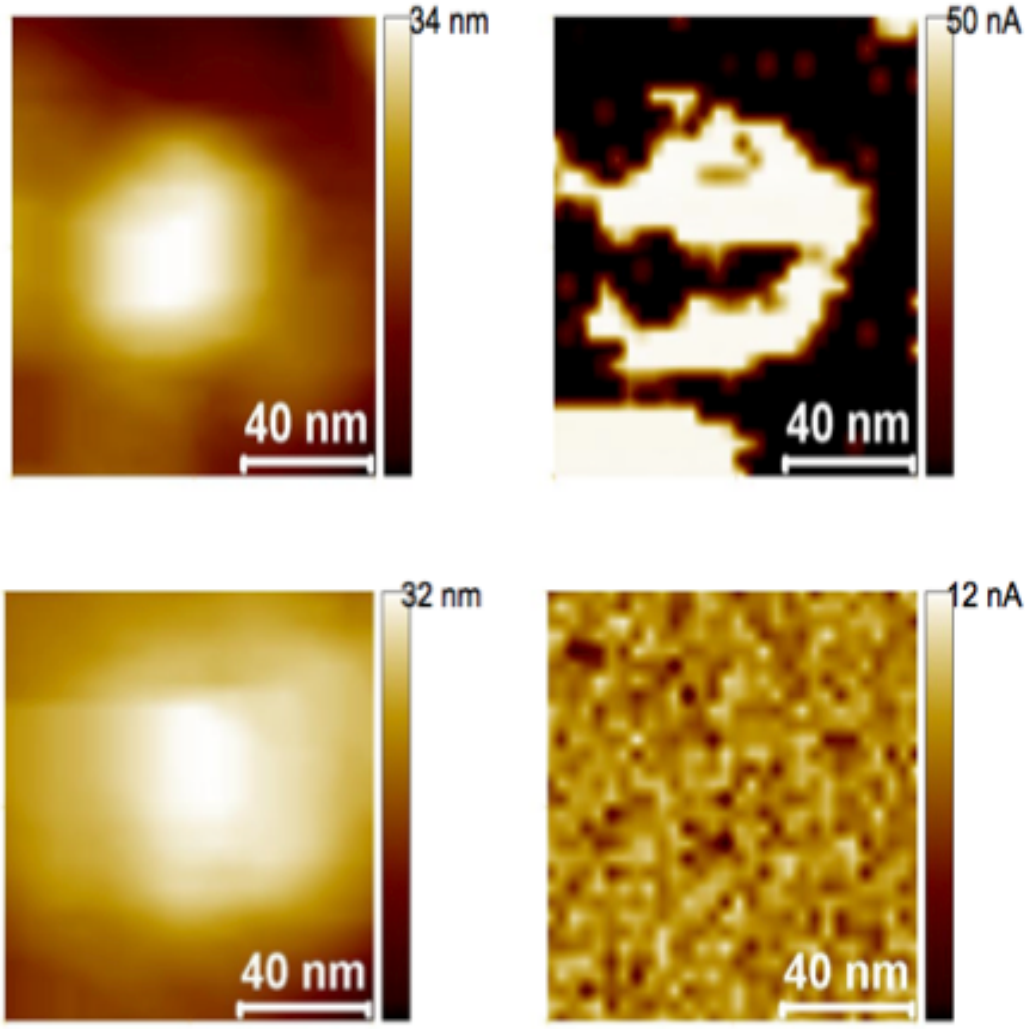

Figure 3.2: A conductive atomic force microscopy image of a nanoscale PMC device after write (top) and erase(bottom) process [8]

Fig. 2.10 in chapter 2 discussed the basic working of a PMC memory cell. The information is stored as a conductive filament grown electrochemically between two different metal electrodes and ultra scalability of PMC devices can be mainly attributed to the dimension of this filament. Scanning electron microscope images of the cross-section of programmed cells (prepared using Focused Ion Beam) shed some light on the approximate dimension of the filament and as shown in Fig. 3.1 it is approximately a few tens of nanometers in diameter ($<$ 100 nm) [7]. However since silver tends to nucleate under intense electron beam used in the SEM, the actual dimension of the filament is expected to be relatively much lesser. Fig. 3.2 that shows the conductive atomic force microscopy image of a nanoscale PMC device after write (top) and erase (bottom) process [8] aids in further understanding of both the dimension and the conductivity distribution of the grown filament. Hence though the devices in the test structure were a between 500 nm and 5 μm in size, the actual size needed for a PMC cell to work successfully is much lesser. Also the OFF resistance tends to decrease as the device dimension shrinks though the ON resistance is strictly dependent only on the compliance current.

Fig. 3.1 also provides insight into the structure of the grown filament, which is conical in shape, broader at the base near the cathode, tapering towards the anode. This is a result of the deposition process during the programming operation which initiates at the cathode and proceeds towards the anode [7]. Another observation from Fig. 3.2 that is significant for this work is the non-uniformity of the conductive path(as seen from the bright areas on the top-right figure). During the programming cycle the conductive filament grows in such a way that it encompasses some of the non-conducting phases (typically germanium rich) resulting in a filament that is not entirely metallic. To summarize the conductive filament responsible for the low resistance state in PMC devices is about a few tens of nanometers ($<$ 100 nm) in diameter at the base and roughly resembles a cone and has non-uniform silver distribution.

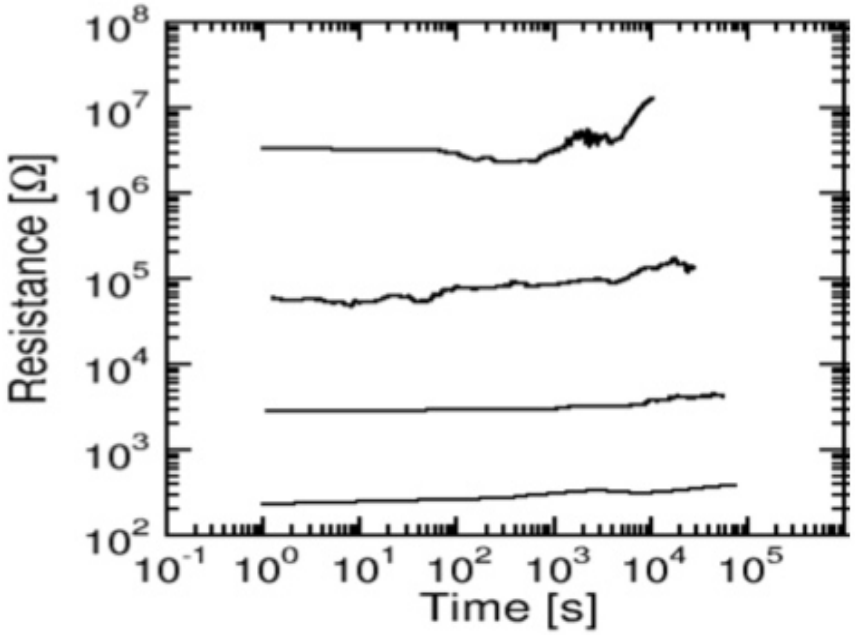

Figure 3.3: Different resistance states under no stress at room temperature monitored for around twenty four hours

Since a metallic interconnect bridges the two electrodes, the programmed/low resistance state is expected to be very stable with or without stress. Fig. 3.3 shows the behavior of different resistance states under room temperature monitored for around twenty four hours. The resistance states are very stable but with a gradual increase in the low resistance. The conductive filament is not entirely metallic as mentioned before and it is surrounded by a non-conducting solid electrolyte. This could lead to setting up of concentration gradients aiding in diffusion of silver from the conductive filament and temperature could accelerate this process. Hence thermal diffusion could be the reason for the gradual increase in the low resistance states under no stress. Also since silver when exposed to sulfur even at room temperature has a tendency to sulfurdize and hence some chemical reactions could also be responsible for the gradual loss of silver in the conductive filament.

Fig. 3.4 shows two different low resistance states monitored for more than an hour at two different temperatures, 25^{O}C and 125^{O}C. The role of temperature in accel-

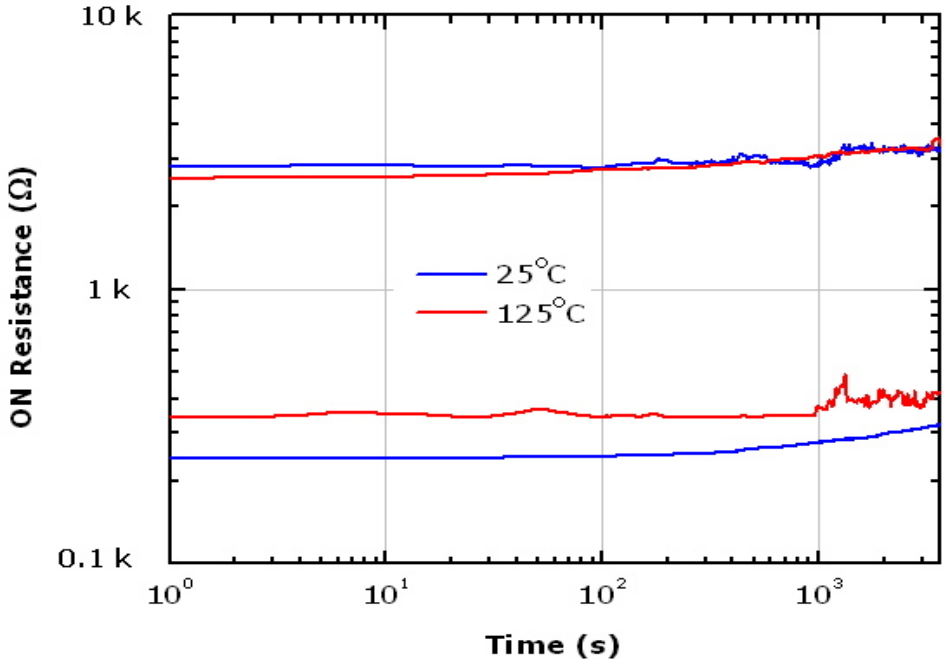

Figure 3.4: Two low resistance states monitored over time at two different temperatures, 25 ^{o}C and 125 ^{o}C

erating the gradual increase in the low resistance state is not clearly evident. Though temperature might play an important role in increasing the low resistance, its effect in isolation was hard to establish as a result of the gradual pace of the mechanism.

Now when a current/voltage stress is forced on the low resistance state a variety of possible failure mechanisms could come into play with electromigration, joule heating assisted thermal diffusion and voltage driven dissolution/ ion migration being the most significant of them. Any of then, (individually or in combination with another) could be the cause of the failure of the low resistance state in PMC devices under stress. The rest of this chapter discusses the accelerated current/voltage stressing experiments in further detail.

3.2 Test setup

All the electrical characterization tests were done using Agilent semiconductor parameter analyzer 4155B/C. Two micro-manipulators with tungsten probe tips ($\sim$ 10 μm diameter) were used to contact the two electrodes of the cells as shown in Fig. 3.5.

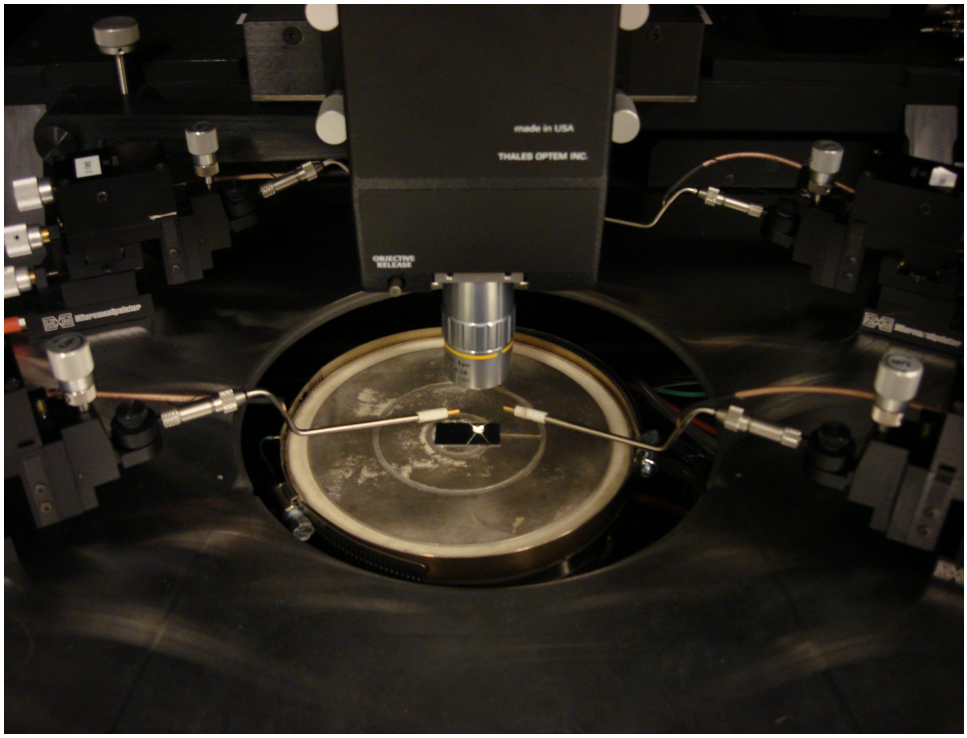

Figure 3.5: Test setup under the probe station with the micro-manipulator arms and the die with test structures

The procedure for accelerated failure tests was as follows. To begin with a few (< 3) Program-Erase (PE) cycles were carried on to make sure that the cell had the right threshold voltage and the ON/OFF resistances. A pulse of sufficiently long time period ($\sim$ 50 ms) or a voltage sweep (0 - 1 V) was applied at the required compliance current level to program the cells. This was followed by a read voltage of a $\sim$ 50 mV to make sure that the desired stable low resistance state was obtained. Finally voltage/current stress was forced on the low resistance state and the voltage/current stress was used to monitor the resistance with time till the cell switched off or till a relative high/low resistance state (for it to considered as a failure) was reached. A variation of 10x from the initial ON resistance was considered to be a failure and the time was taken as the failure time. Around ten trials were performed in each case and a normal probability plot was used on the failure times to obtain the mean time to failure for each case.

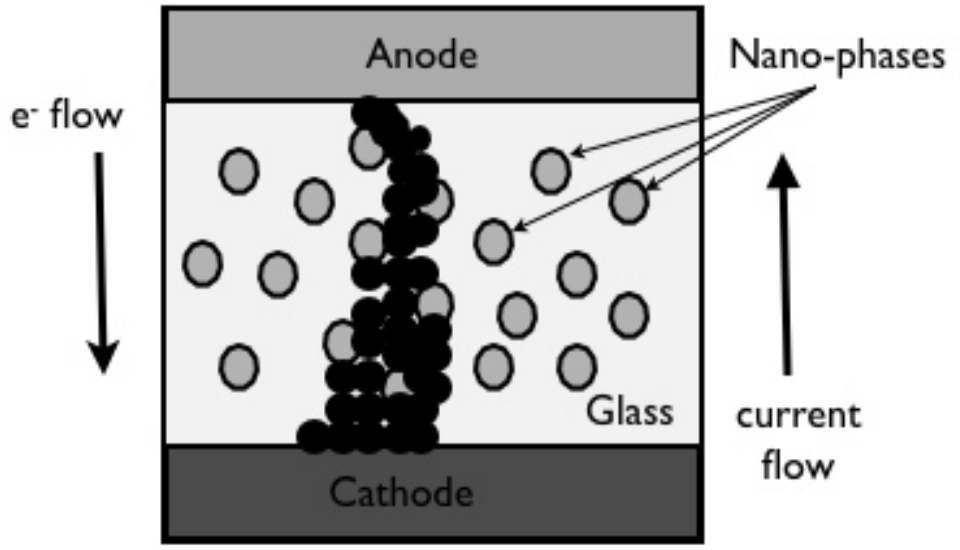

Figure 3.6: A programmed PMC cell with current stressing in the negative direction

3.3 Current stress

Typical current stress experiments are carried out by forcing a current through an interconnect (both at normal temperatures and elevated temperatures to accelerate failure) to maintain high constant current densities till failure. Failure times are then fit into the Black's equation (in case electromigration failures) [67] and one or more variables (like the activation energy and order, 'n' for the material) are calculated from the known parameters, like current density and temperature. Similar stressing tests on the low resistance states of PMC devices under constant current stress monitored till failure are presented in this chapter. Both negative and positive stressing currents of different magnitudes were used. Fig. 3.6 shows a qualitative picture of a programmed PMC cell with a negative current stress forced on it.

Negative current stressing refers to forcing a current through the device from the cathode to the anode till failure. The polarity of this current is opposite to the direction in which the device was programmed, i.e. it is in the erase direction (electrons flow from the anode to the cathode). It is important to note that a programmed cell is erased by applying a low negative voltage $\sim$150 mV for a short time. This negative voltage

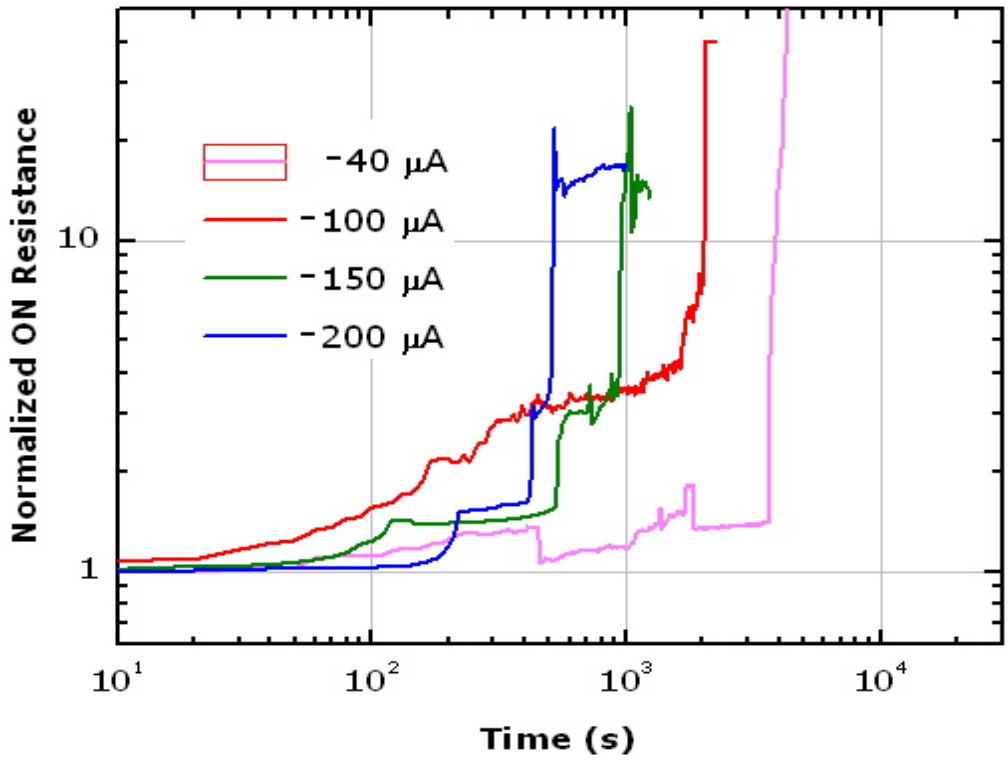

Figure 3.7: Variation in the normalized low resistance state ($R_{ON}/R_{ON-INITIAL}$) monitored till failure for different constant current stress on cells programmed with 1 mA compliance current

initiates the dissolution of the electrochemically grown filament by oxidizing the silver atoms constituting it and depositing them on the anode [68] depleting the conductive filament of the comprising silver and restoring the high resistance OFF state.

Negative current stress

Constant negative currents of different magnitudes were forced on the programmed low resistance states and the failure times were noted. A statistically significant number of trials were performed on each stressing current level and the mean time to failure (MTTF) was extracted from the normal probability plot of these times by taking the failure time at the 50% point (called the t_{50} point). Fig. 3.7 shows the variation in the normalized low resistance state ($R_{ON}/R_{ON-INITIAL}$) monitored till failure for different constant current stress on cells programmed with 1 mA compliance current (an ON resistance of about 500 Ω). Fig. 3.8 shows the normal probability plot for different

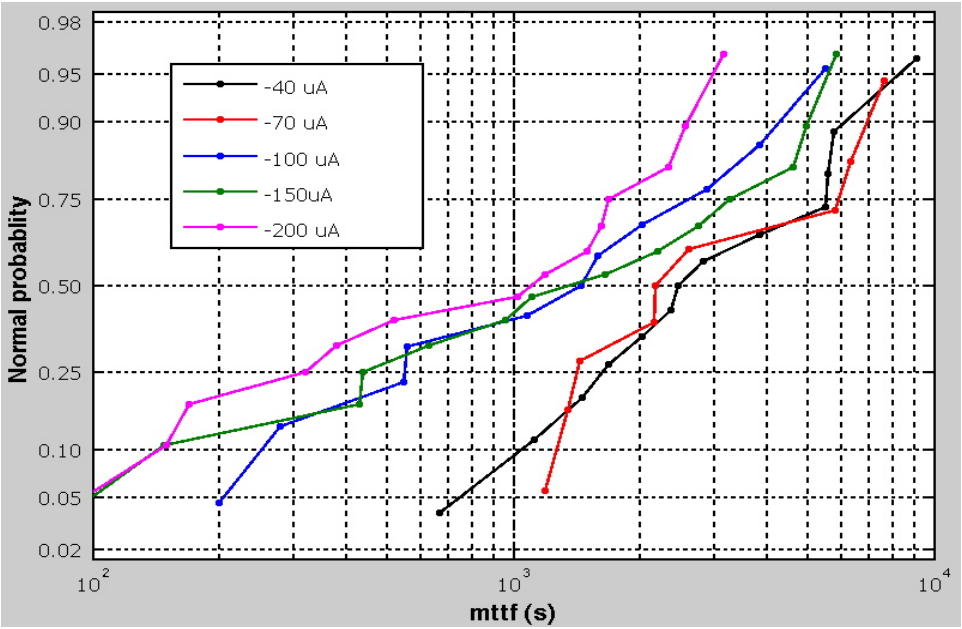

Figure 3.8: Normal probability plot for different constant negative current stress for devices written with 1 mA compliance current

constant current stress used to extract the mean times to failure at different currents.

Failure times decreased consistently with higher stressing currents as shown in Fig. 3.9. Linearity of the obtained experimental results (as seen from the straight line superimposed in Fig. 3.9) on a semi-log plot suggests an exponential dependence of the times to failure on the stressing currents. However for electromigration this dependence is expected to follow a power law (typically of the order 2) [69] as mentioned previously. The exponential dependence is also in close agreement with the theory discussed in chapter 2 about the ion conduction in solid electrolytes during the programming operation, suggesting that the failure under current stress could also be caused by ion migration under the reverse electric field developed due to the applied stress.

Also from Fig. 3.7 it can be seen that though failure occurred after some time from the beginning of the trial, the resistance started increasing almost immediately after the current stress was forced. This implies that the conductive filament started weakening or losing its constituent silver immediately (but not sufficient enough to cause failure), reducing the area of cross-section. Therefore though constant current

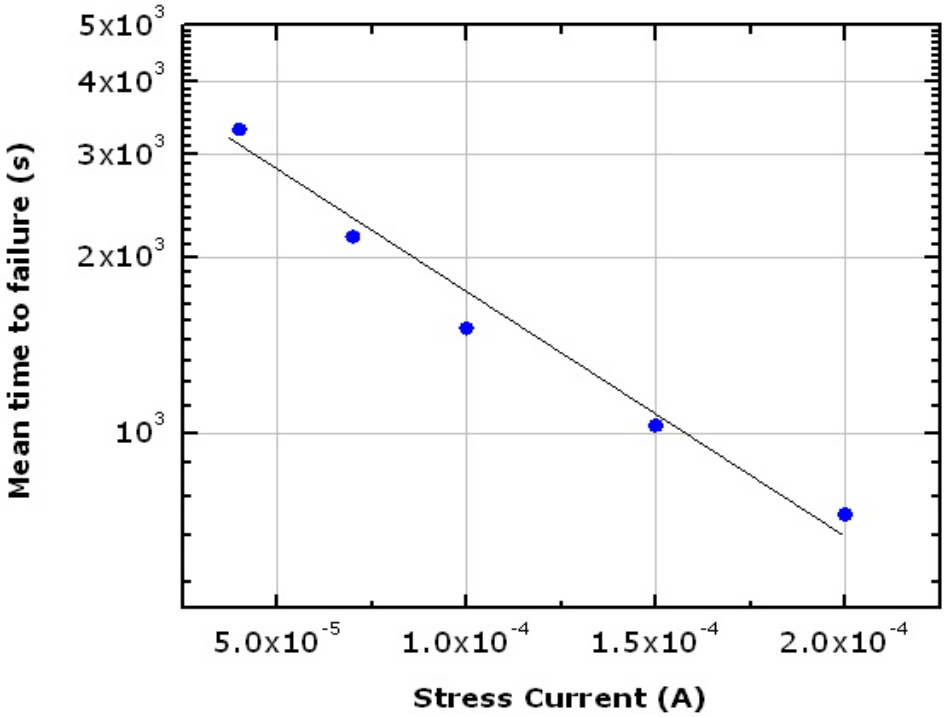

Figure 3.9: Mean time to failures for different stressing currents for devices programmed at resistance of around 500 Ω with the exponential fit shown as a the black line

was forced across the device, the current density was not uniform and started to increase as the area for current flow started to decrease. Hence the current density term in the Black's equation, mttf(s) = $AJ^{-n}\exp(E_a/kT)$ is not constant and this additional variable complicated the fitting analysis. Since the resistance change was instantaneous and continuous with time, the voltage developed across the conductive filament was also not constant. Hence under constant current stress both the current density and the voltage across the low resistance cell were non-uniform making both electromigration and ion migration analysis difficult.

A consistent trend noticed during the stressing trials discussed here and in succeeding chapters is the variation noticed in the time to failure for similar cells programmed and stressed with the same source. Though this could be attributed to some processing and testing condition variations, there is a strong possibility that this could be physical. Since the basic working of a PMC device involves forming and dissolv-

ing a conductive filament repeatedly, the statistical variations amongst different cells might result in filaments with different structures even under the same programming conditions. This variation could be both in terms of the shape of the resulting filament and conductivity distribution. This could lead to differing behavior of the similar low resistance cells under identical stress. Hence it is extremely important to be careful while processing these devices as uniformity amongst different cells is very important.

Positive current stress

When a high current is forced through a metallic interconnect the direction of the current is immaterial for the interconnect to fail by electromigration or joule heating as current in either direction will displace the atoms (electromigration) and/or cause self heating inducing thermal diffusion (joule heating). If devices fail under both positive and negative current stress the failure mechanism can be isolated to either electromigration or joule heating as ion migration in the positive direction will not result in an increase in the low resistance states as the developed voltage is in the direction of programming the device [57].

Positive stressing currents of different magnitudes were forced on devices programmed with a compliance of 100 μA to investigate the above discussed theory. Fig. 3.10 shows the variation in the low resistance states with time for different positive currents and the result from previous section, a -25 μA stress for comparison. PMC devices operate at ultra low power and their threshold voltage is less than 0.5 V. Hence before any failure mechanism could increase the low resistance state to failure, the cells re-programmed themselves more strongly as there was no dramatic increase in resistance under positive current stress but there was a decrease in the low resistance that was more predominant under higher positive stress. The cells were repairing themselves by growing a thicker (or multiple) filament(s) to accommodate more current. After the initial drop in the low resistance under +25 μA stress at $\sim$ 300 s, the resistance again started to increase gradually. There were two competing mechanisms

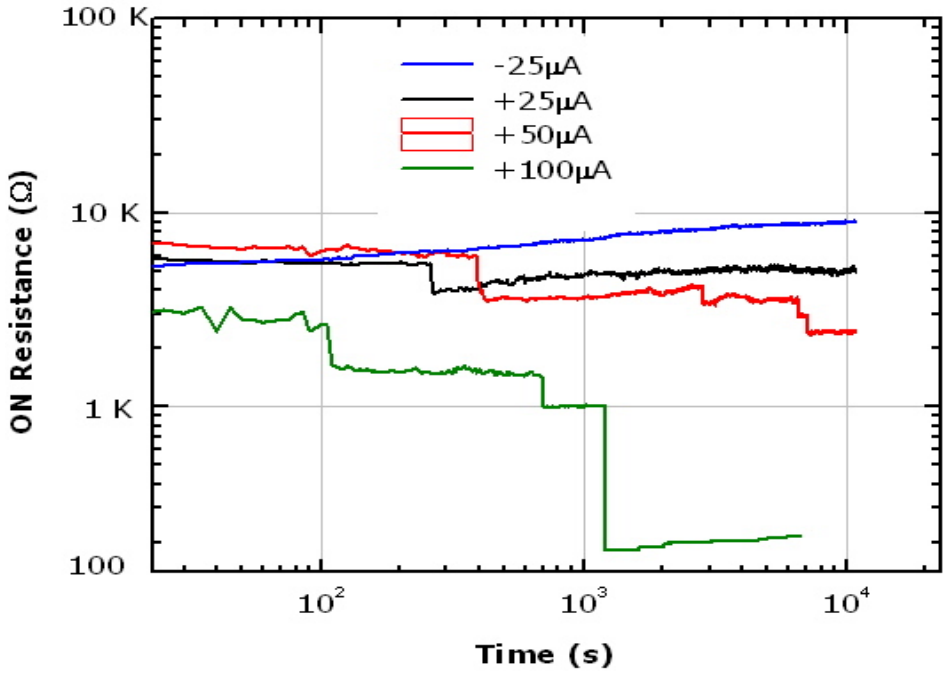

Figure 3.10: Variation in the ON resistance with time for different positive stressing currents on devices written with 100 μA compliance

present with one of them being the rewriting process (that dominated), the other one could have been thermal diffusion assisted by joule heating (which caused the increase in resistance). It was hence not possible to isolate electromigration and joule heating as the programmed cells rewrote themselves under positive current stress and the effect of failure mechanism(s) that result in the increase in the low resistance was overshadowed.

Bi-polar current stress

Under constant negative current stress, ion migration seemed to play the most significant role in failure, evident from the exponential dependence of the failure times on the stressing currents. However both current density and the voltage developed across the device were not constant due to the instantaneous and the continuous resistance change noticed in the low resistance states with time much before failure making electromigration analysis more complicated. However to further distinguish between electromigration and ion migration similarly programmed ON states (similar R_{ON}s) were stressed with unipolar and bipolar currents of similar magnitudes for equivalent stressing times.

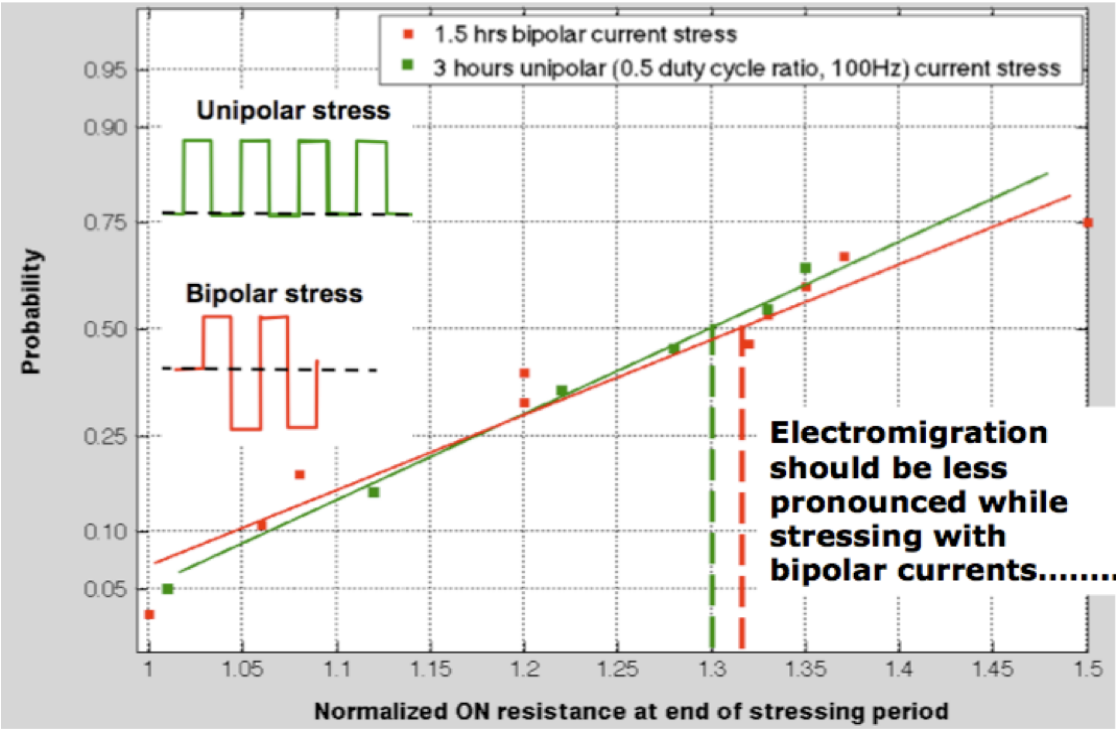

Figure 3.11: Distribution of the normalized ON resistance at the end of stressing period of similar R_{ON} states under unipolar and bipolar current stress

Normalized R_{ON}s at the end of stressing period ($R_{ON-FINAL}/R_{ON-INITIAL}$) were plotted and are shown in Fig. 3.11 and as seen from the figure there is no change in the $R_{ON-FINAL}/R_{ON-INITIAL}$ between two types of negative stressing currents.

Electromigration is a phenomenon where atoms in the crystal lattice of a conductor get displaced due to electrons at high current densities. When a DC high current is forced through a conductor for a prolonged time in one direction, the electrons displace the atoms and the resistance of the conductor starts increasing till it eventually fails. However when a bipolar (AC) stress current is used, since the direction of the current changes every half cycle, there should not be any net displacement of atoms (by electrons) in one direction and hence the effect of electromigration should be significantly lesser [70]. But from Fig. 3.11 it can be seen that there was no difference in behavior in the resistance increase in similar ON states under unipolar and bipolar current stress. This further suggests that electromigration does not play a significant

role in the resistance increase phenomenon in PMC cells under stress./par

3.4 Voltage stress

Negative voltage stress

Ion migration was found to have played a significant role in failure under current stress from the previous section. However as discussed previously neither the current density nor the voltage could be maintained constant across the conductive filament (due to instantaneous and continuous increase in the resistance). For analyzing the role of the applied voltage on a low resistance state, it is suitable to stress the cell with a constant voltage to verify the dependence of failure times according to the expression mentioned previously, MTTF (due to ion migration) = $Ce^{-\alpha V/kT}$, where C is a constant. The current density is also maintained relatively constant as the current reduces as soon as the resistance increases, stabilizing the current density.

The erase threshold voltage of PMC cells is $\sim$-150 mV as discussed from chapter 2. However a voltage sweep was used in that case and every increment of the voltage was applied across the device for a definite period depending on the integration time, i.e. when the voltage was swept from 0 to 1 V with a 10 mV increment every voltage step (10 mV, 20 mV, 30 mV, ... ,1 V) was applied across the device for $\sim$ 100 ms. But as seen from the current stressing results in the previous chapter the initiation of the erase process not only depends on the magnitude of the voltage but also on the time for which it is applied.

Fig. 3.12 shows the behavior of the low resistance state monitored till failure for different negative stressing voltages on cells programmed with 1 mA compliance (ON resistance of around 500 Ω). Failure was accelerated with increasing negative stressing voltages as in the case of negative stressing currents normal probability plots were used to extract the MTTFs for different stress voltages. Fig. 3.13 shows the exponential dependence of the times to failure on the stressing voltage again similar to the dependence observed in case of current stress. This further strengthens the claim made

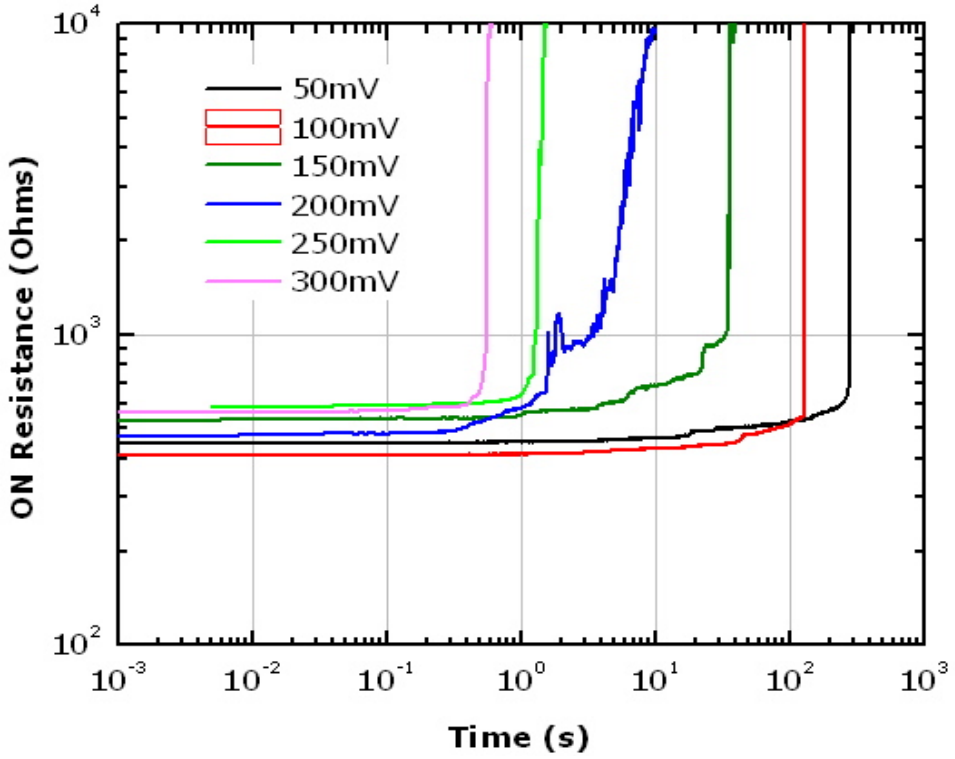

Figure 3.12: Behavior of the low resistance state monitored till failure under different negative stressing voltages on cells programmed with 1 mA compliance (ON resistance of around 500 Ω)

in the previous chapter about ion migration being responsible for failure under negative stress.

To address the dependence of initial ON resistance on the time to failure and to investigate the stability of multiple low resistance states under stress, the fore mentioned tests were carried on two more resistance levels, cells programmed with 100 μA and 10 μA compliance (On resistance of around 5 kΩ and 50 kΩ respectively). Fig. 3.14 shows the dependence of the failure times on the negative stress voltages for this low resistance state and the failure times were again found to be exponentially dependent on the stress voltages.

The voltage stress range for 50 kΩ state (25 mV to 100 mV) was different from the 500 Ω state (50 mV to 300 mV). This was because cells programmed at 50 kΩ cells switched off at higher voltages at times that were too small for the resolution of the test

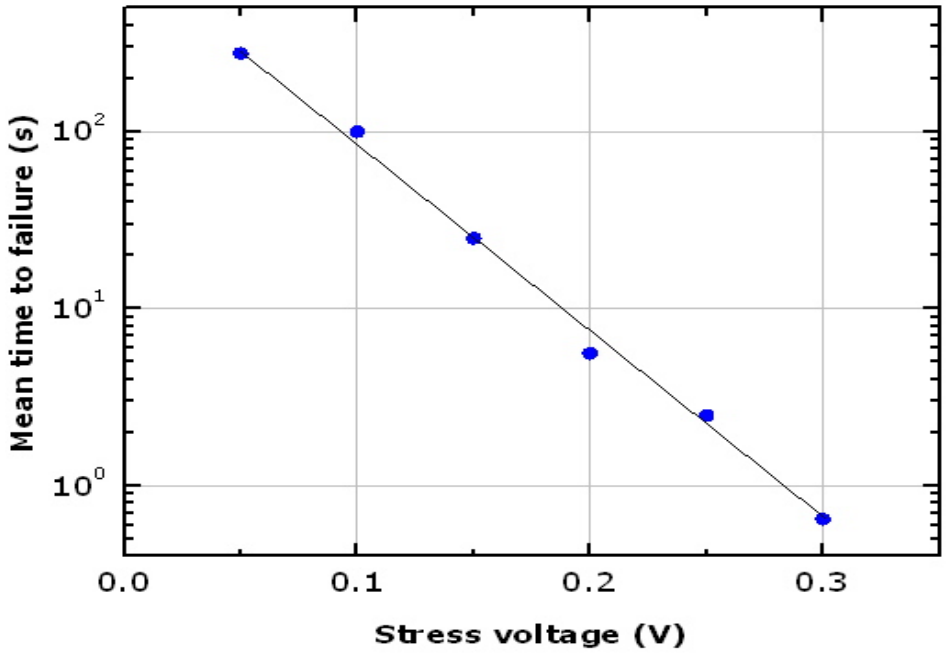

Figure 3.13: Exponential dependence of the times to failure on the stressing voltage on cells programmed with 1 mA compliance (ON resistance of around 500 Ω)

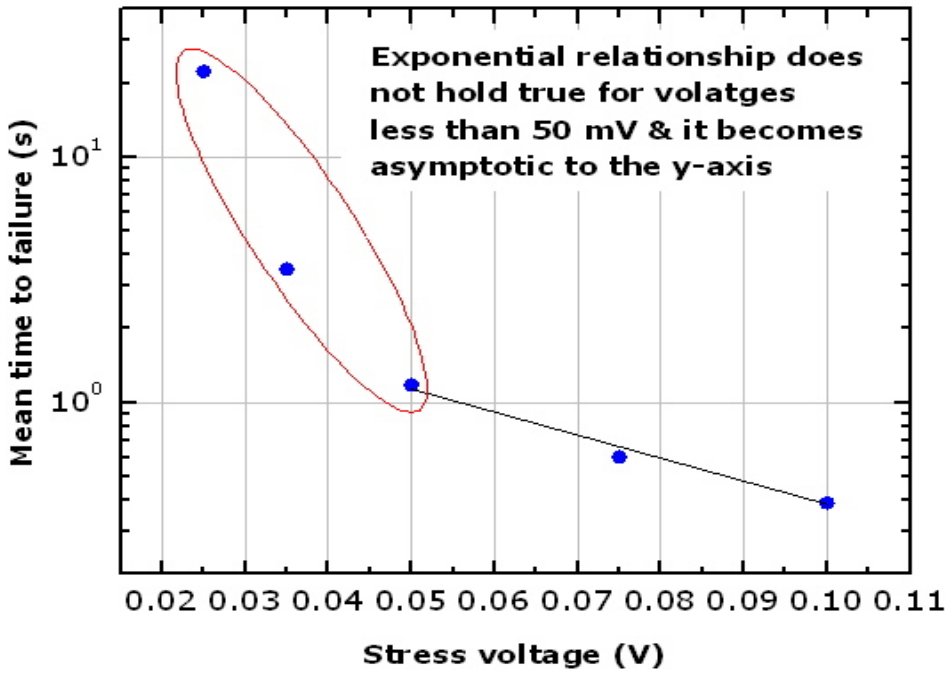

Figure 3.14: Dependence of the failure times on the negative stress voltages for the cells programmed at 50 kΩ

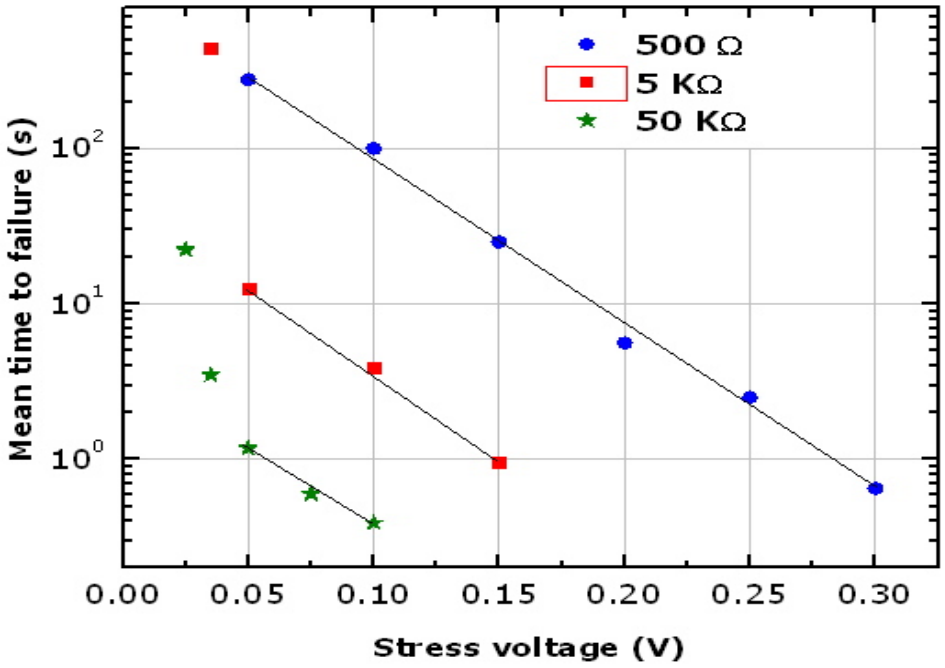

Figure 3.15: Cumulative results of mean times to failure under different negative stress voltages for three different initial resistance levels

equipment used. Also cells programmed at 500 Ω did not switch off for hours under negative voltages less than 50 mV.

Fig. 3.15 shows the cumulative results of mean times to failure under different negative stress voltages for three different initial resistance levels. The mean times to failure for any particular resistance level were exponentially dependent on the applied voltage stress and the slopes of the curves were fairly constant. This further suggests that the failure under both voltage and current stress was mainly due to ion migration.

It is evident from Fig. 3.14 that the exponential fit does not hold good for very low voltage stress (the two points on the curve, 25 mV and 35 mV). Also again in the 5 kΩ resistance level in Fig. 3.15 it can be seen that the exponential fit holds good only up to 50 mV. This is in agreement with the discussion in chapter 2 (as shown in Fig. 2.17) where in the absence of any applied stress the ions can move randomly in either direction of the barrier and ideally there is no net ion flow in any one direction. The curves in Fig. 3.15 are expected to be asymptotic to the time axis proceeding lower

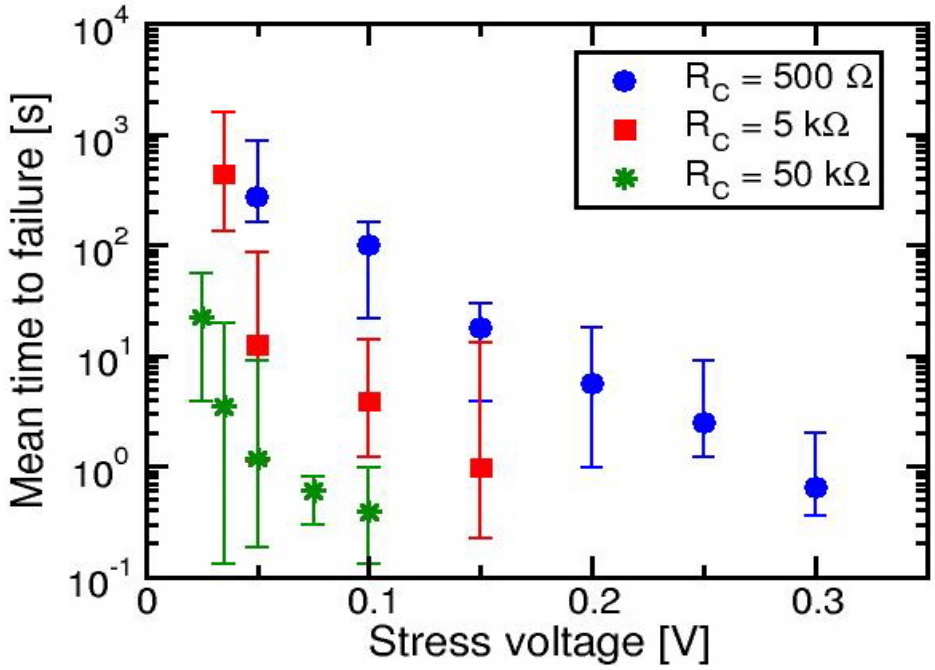

Figure 3.16: Variation in the failure times for similar stressing conditions

in the voltage scale as it was already seen in Fig. 1.7 and Fig. 3.3, that under no stress there is hardly any change in the resistance level (implying very high failure times) except for diffusion which occurs even in the absence of stress voltage.

As mentioned previously, considerable variation (spanning an order in magnitude) was noticed in the failure times for similar stressing currents and this was evident form Fig. 3.16 which shows error bars fitted on the points shown in Fig. 3.15. Error bars are particularly large for the higher resistance levels as seen from the figure. Thus uniformity amongst the devices that can be achieved by precisely controlling the processing and testing conditions is very important and this also affects the behavior of similar resistance ON states in PMC cells.

Positive voltage stress

Fig. 3.17 shows the low resistance state monitored over time for different positive voltage stress on devices programmed with 10 μA compliance. Fig. 3.18 shows the dependence of mean time to failure on the stress voltage. Similar to constant current stress

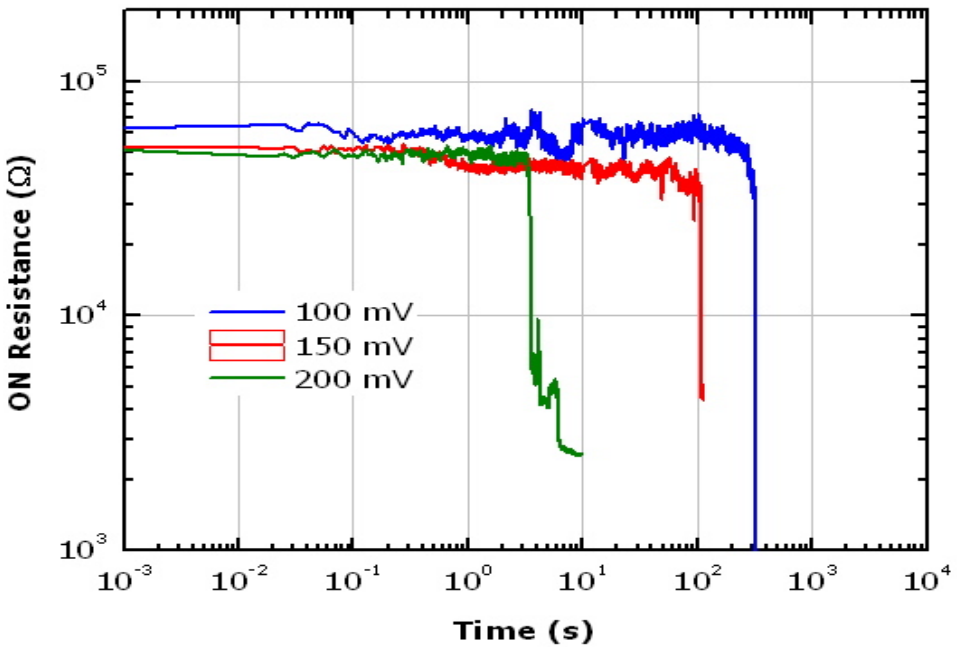

Figure 3.17: Low resistance state monitored over time for different positive voltage stress on devices programmed with 10 μA compliance

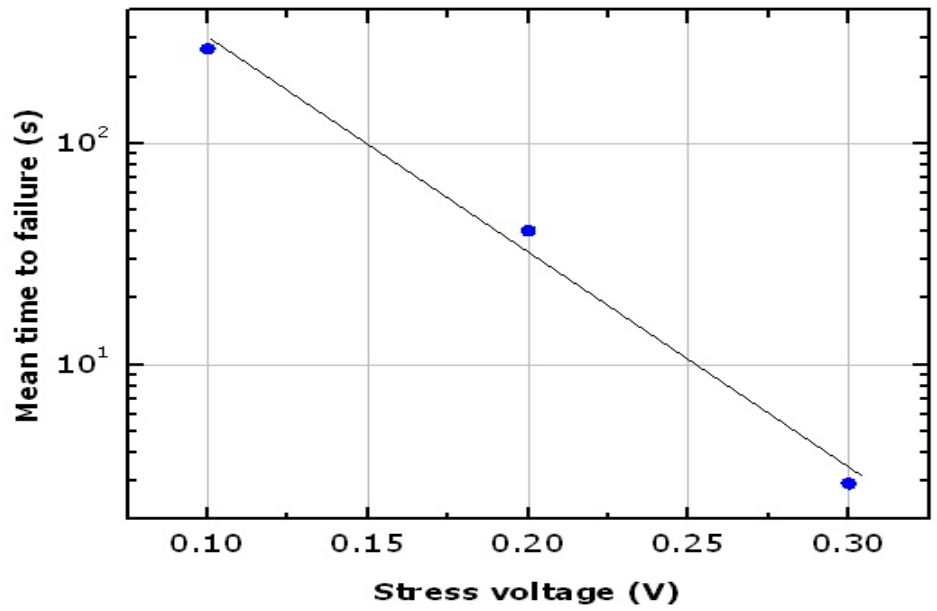

Figure 3.18: Cumulative results of mean times to failure under different positive stress voltages on devices written with 10 μA compliance

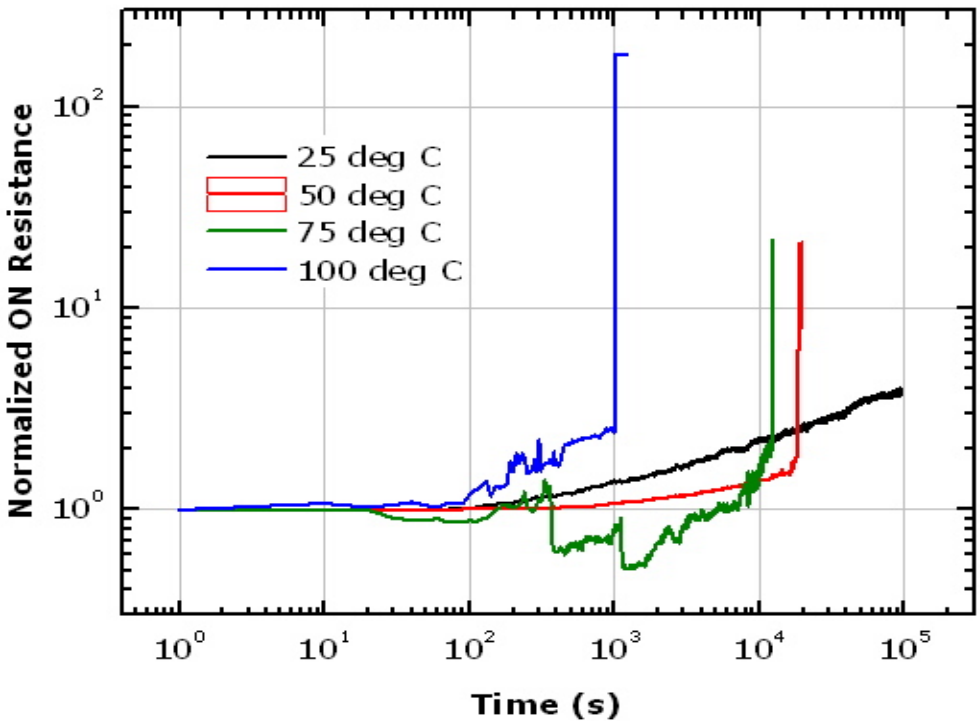

Figure 3.19: Variation in the normalized ON resistance with time while stressing with -25 μA constant current on cells programmed with 100 μA compliance current (ON resistance of around 5 kΩ)

in previous sections, the programmed cells reprogrammed themselves to accommodate more current under positive voltage stress. A decrease in the low resistance state by a factor of ten was considered failure in this case. This failure times were found to decrease with increasing applied positive stress voltages and the dependence was exponential as seen from Fig. 3.18, implying ion migration under the applied electric field to be most significant mechanism involved.

3.5 Current/Voltage stress at elevated temperatures

Current stress at elevated temperature

Since temperature accelerates any failure mechanism its role in failure of the low resistance states in PMC devices is critical. Fig. 3.19 shows the variation in the normalized low resistance states with time under a constant current stress of -25 μA on cells programmed with 100 μA compliance current. Failure times decreased with rising temperature as expected. Hence though the role of temperature in isolation was difficult

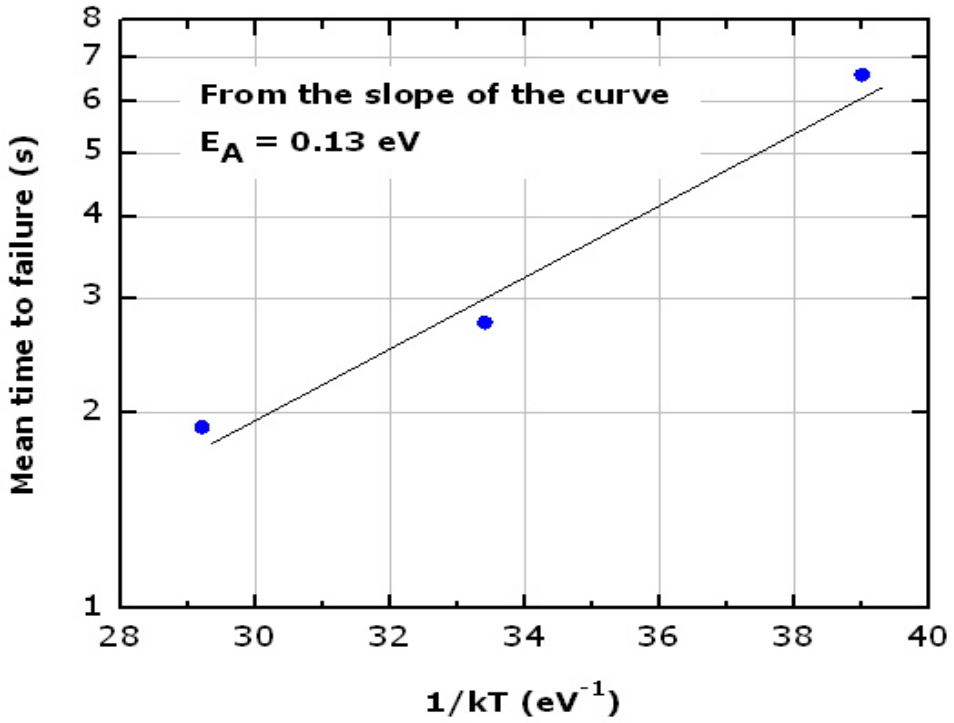

Figure 3.20: Variation of the mean time to failure at different temperatures for the same negative voltage stress

to extract, its combined role with a current stress is evident from these results. Earlier work on the combined effect of temperature and current stress on the low resistance states also showed similar trend and the activation energy for failure was calculated to be approximately 0.5 eV [58].

The unexpected variation in the resistance (drop in resistance under negative current stress and higher temperature) could not be attributed exclusively to the physics of the devices as an excessive amount of vibration was noticed on the temperature chuck during the high temperature measurements (possibly due to the pressure of the nitrogen flow used to regulate the temperature and reduce water condensation on the samples at low temperatures).

Voltage stress at elevated temperature

To see the interplay between temperature and negative voltage stress, devices programmed with 1 mA compliance were stressed with a negative voltage of 200 mV

at three different temperatures; 25 ^{O}C, 75 ^{O}C and 125 ^{O}C. Fig. 3.20 shows the dependence of failure times (extracted from more than ten trials in each temperature level) for the same negative voltage stress. The decrease in failure times at higher temperatures was similar to the results obtained for current stress at different temperatures and in previous work [58]. The dependence of failure times on temperature was found to be Arrhenius in nature as shown in Fig. 3.20 with the slope of the plot giving the activation energy for failure.

Activation energy from the graph was found to be $\sim$ 0.13 eV, which is in close agreement to the value that was calculated in an earlier work [51], 0.2 eV for Ag-GeSe devices under no electrical stress but with thermal stress at 70^{O}C. However activation energy from a previous work where a combination of current and temperature stress was used was 0.5 eV [58]. It is important to note that the number of trials used in that work for each current level were significantly much lesser and with the large statistical variations seen in the failure times under stress it is fair to conclude that 0.5 eV value of the activation energy was approximate. Also the theoretical value of the activation energy for silver is 0.3 eV [71]. The difference in the activation energy calculated here and in theory stems from the structure of the conductive filament in PMC devices. As discussed in chapter 2 the filament is not entirely metallic and is prone to possess voids and other defects. The 0.3 eV activation energy is for crystalline silver that is much more tougher than the conductive filament in PMC devices and the activation energy is expected to decrease as the interconnect becomes less crystalline as it is easier to cause failure.

3.6 Summary of accelerated failure tests

From the results so far on stability of PMC states under different stress conditions, it was also found that the transition from different ON states to a 10x increase did not result in a permanent failure or in other words it was not a hard failure. All the cells could be programmed again after a stress test without any loss of functionality. This

indicated that this transition under different electrical stressing conditions was similar to a typical erase process in a PMC device operation. To further analyze this, the behavior of PMC ON states under higher negative voltages had to be investigated. But higher the negative voltage, the transition time from ON state to a 10x higher resistance state was too small for accurate DC measurements and hence pulse measurements were required. Also since there was no clear difference in behavior of ON states under current and voltage stress, for the pulse measurements, only negative voltages were used (and not negative currents) for the rest of this work.

Chapter 4

VOLTAGE DRIVEN ON-OFF TRANSITION

4.1 Introduction

From the results discussed in chapter 3, it was clear that under constant current/voltage stress the PMC ON states behaved in a manner similar to their erase process. Also the transition from the low resistance ON state to a higher resistance OFF state (termed as a 'failure' so far) was not a permanent failure, in the sense the cells behaved normally even after this transition, emphasizing the fact that the transition was only an erase and not a failure. Hence this chapter details more results and discussions on the erase process of the PMC cells.

PMC cells work as a memory elements by repeatedly growing and dissolving a CF in the solid electrolyte (chalcogenide) layer sandwiched between two metal electrodes. The switching ON (or growing the CF) is due to electrochemical formation of a silver CF in the ion-conducting chalcogenide glass bridging the two electrodes with a low resistance path to allow sufficient current (as programmed) to flow through. The switching OFF is due to the dissolution of this CF to gain back the original high resistance OFF state. While the switching ON (program) mechanism in PMC cells has been analyzed and understood quite well [6] there are few un-answered questions about the switching OFF (erase) mechanism.

The CF in a PMC cells can be thought of as a silver interconnect bridging the two metallic electrodes. When a high current flows through this CF that is very small in diameter (< 100 nm), many failure mechanisms could be involved. Electromigration could play a major role in disrupting the CF [69, 67] or with the high current flowing through the metallic CF the local temperature rise could result in joule heating assisted CF disruption [72, 73]. Or the erase process could be similar to the program process in PMC but with reversed polarity and could be a result of electrochemical reactions assisted by ion migration under the applied electric field.

Though erase process in PMC cells have not been characterized extensively, previous work on lateral devices [68] and similar solid electrolyte switches [57] have shown that the erase of a CF starts with the oxidation of silver in the CF and in particular near the neck of the CF or the intersection of the CF and the silver electrode (anode). This has been shown to be due to the large potential drop across this interface due the vast difference in curvature between the CF and the electrode. This subsequently leads to dissolution of the CF initiating at the tip of the CF and gap between the retreating CF and the silver electrode widens as the erase electric field is maintained. This process continues till the majority of CF is re-deposited back to the silver electrode. However before the CF is dissolved, the current density may reach very high values and thermal effects and electromigration could play a role in aiding the erase process.

This chapter addresses the dependence of the transition time from the ON (low-resistance) to the OFF (high-resistance) state or the erase time in PMC cells. The ON-OFF transition time defines on one hand the stability of the ON state on the long-term scale, and on the other hand the erase operation time. Experimental data are explained in terms of dissolution of the CF, which sets the ON resistance and is dissolved during erase as a result of electrochemical reactions and ion hopping through the solid electrolyte [6]. No clear impact of electromigration was found, in agreement with previously reported results in [68] and [57].

From previous characterization work on program operations in PMC cells [6] it was shown that the thickness of the CF varies with the current used to program it. There were two distinct stages in the growth of a CF namely formation and the radial growth of the CF. The second stage in this CF growth process was shown to be effectively controlled by the current compliance set during programming. This is an important property of any memory technology for it to be successfully used in Multi-Level (ML) applications. However while programming PMC cells to different levels of ON resistances in a controlled manner is important, investigating the reliability and the

behavior of these (different resistance) ON states is also significant. Hence this chapter also investigates the ON-OFF transition of different ON states and the choice of the programmed ON resistance is shown to be critical for an optimum tradeoff between data-retention and program/erase performances, particularly for ML applications.

Finally having analyzed the CF with respect to the erase process, the role of the chalcogenide or the electrolyte layer thickness in data-retention and program/erase kinetics in PMC cells is also briefly discussed in this chapter.

4.2 Experimental Setup

Unlike the stress tests in chapter 3 the measurements in this chapter were done using the voltage pulses (instead of constant voltage sources) due to the smaller times involved at higher erase voltages. Fig. 4.1 shows the measurement setup used in pulse measurements in this work. The PMC test device was connected in series with a current-limiting resistor (R_L) and a Sony Tektronix AWG2021 Pulse Generator Unit (PGU) was connected across this series combination. An Agilent Technologies Digital Oscilloscope DSO7032 (DO) was used to monitor both the input to the circuit from the PGU (OSC2) and the output voltage drop across the PMC cell (OSC1). This was the same setup used for both program and erase speed measurements in this chapter.

Fig. 4.2 shows an erase time (t_E) measurement in which the dotted line is the input and the solid line is the output voltage across the PMC cell as seen on the DO. When the voltage across the cell (negatively) increases abruptly (to $\sim$ input voltage), the cell is erased and the time from this event to the falling edge of the input pulse is termed the erase time (t_E or t_{erase}). However it should be noted that this erase does not refer to a complete erase of the device, but to the time taken for a 10x increase in the ON resistance from its initial value, as this choice allowed for a fair comparison of resistance stability in different levels of R_{ON}.

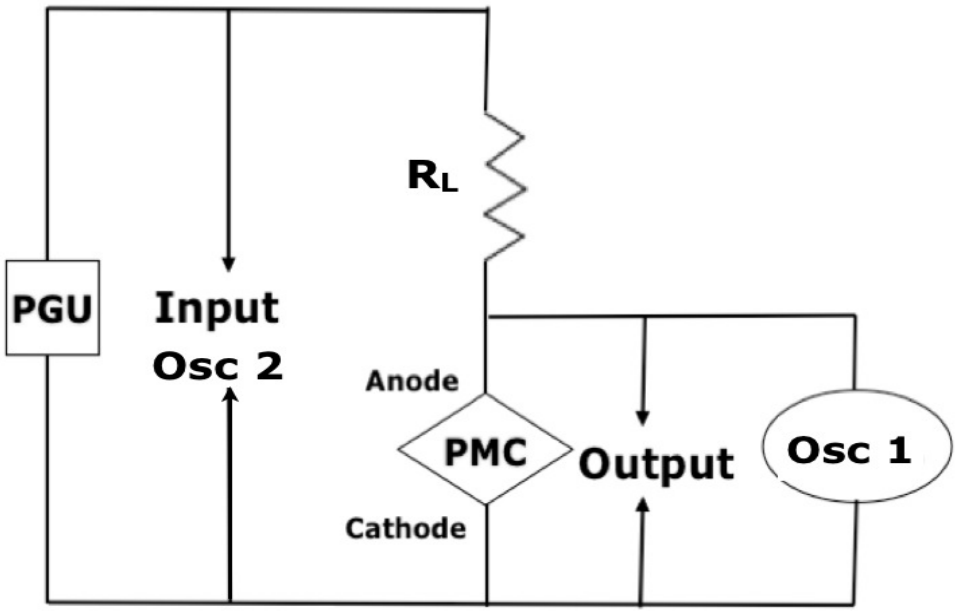

Figure 4.1: Setup used during pulse measurements of PMC cells in this chapter

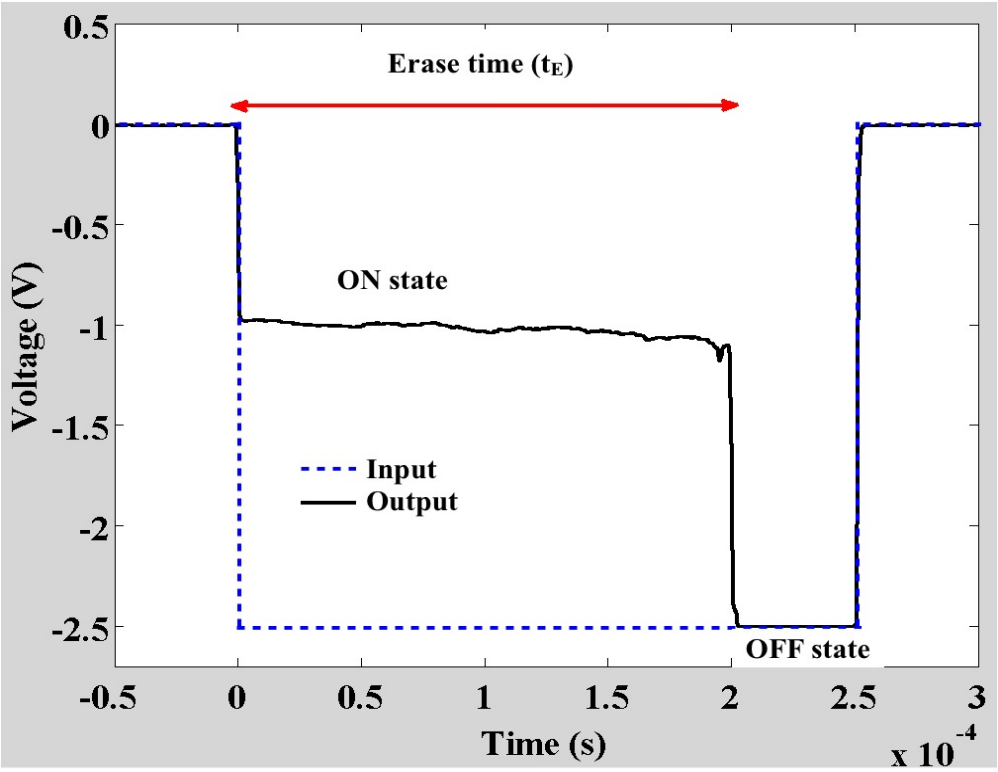

Figure 4.2: An erase time (t_E) measurement

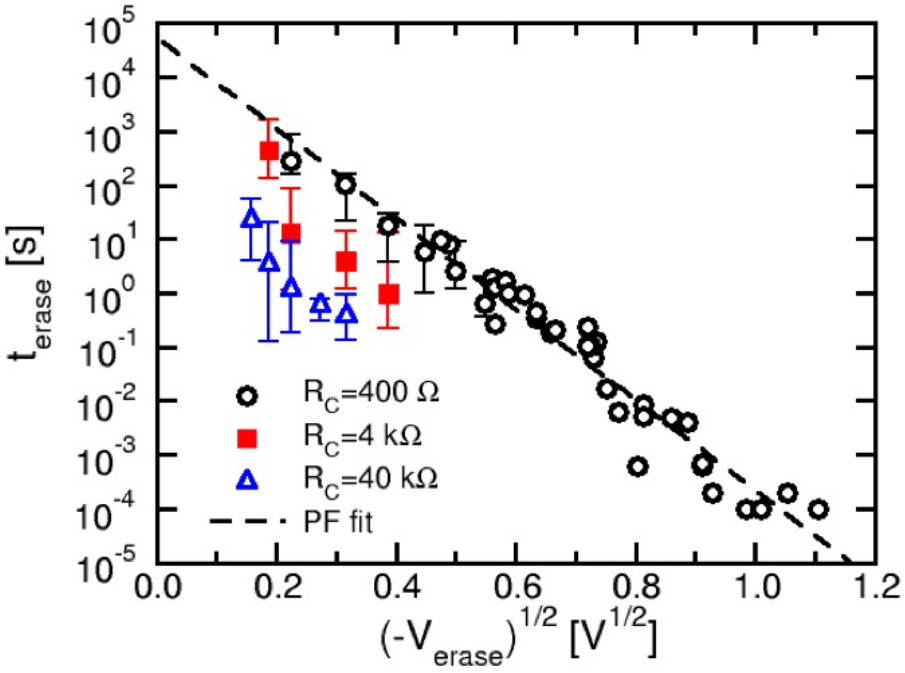

Figure 4.3: Measured erase times as a function of the square root of erase voltage, for R_{ON} = 400 Ω, 4 kΩ and 40 kΩ

4.3 Results

The stability/erase of PMC cells in this chapter were investigated by applying erase/ negative voltage pulses of different magnitudes to cells programmed to similar R_{ON} ($\sim$ 400 Ω) and measuring the time taken for a 10x increase in resistance from the initial low resistance state (t_E). Fig. 4.3 shows the measured t_{erase} as a function of the square root of V_{erase}, for initial R_C values of 400 Ω, 4 kΩ and 40 kΩ (from chapter 3), which were obtained with compliance currents of 1 mA, 100 μA and 10 μA, respectively. Clearly, statistical data confirm the inverse relationship between R_C (or R_{ON}) and t_{erase} (or t_E).

To study the voltage dependence on a wider timescale, Fig. 4.3 also shows results from pulse-mode experiments, with R_C = 400 Ω. For these measurements, fast negative voltage pulses were applied to the Ag electrode through a load resistance (R_L=1 kΩ) and the corresponding cell voltage V_C was traced to extract t_{erase} (Fig. 4.2).

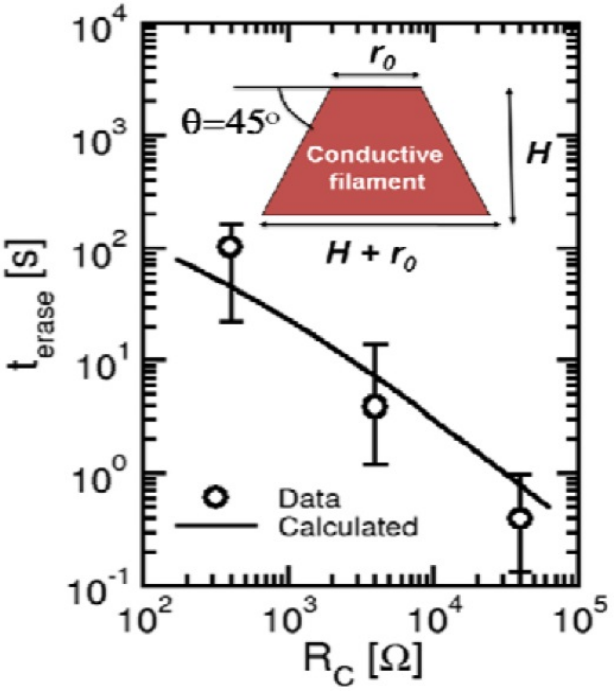

Figure 4.4: Trade-off between the long-term erase time (representative of retention time) and Inset: schematic drawing of a conical CF

The data align on the plot in the range from 100 μs to 1 s, suggesting that Poole Frenkel (PF) transport of ions (which is characterized by the square root dependence on electric field) mainly controls the erase operation. In particular, we propose that Ag ions are released by oxidation of the CF and then they migrate toward the negatively-biased Ag electrode by PF. This is in agreement with previous observations of PF ion conduction in glasses [74] and that the erase operation in PMC is controlled by ion migration, rather than electromigration [58].

4.4 Modeling erase process

The experimental results from Fig. 4.3 can be explained on the basis of a simple model for CF dissolution in PMC. To this purpose, Fig. 4.4 summarizes the dependence of t_E on R_C, for V_E = -100 mV. An assumption that the CF shrinks uniformly and at constant velocity v_D when a constant voltage is applied, then t_E will depend on the minimum CF radius r_0 as

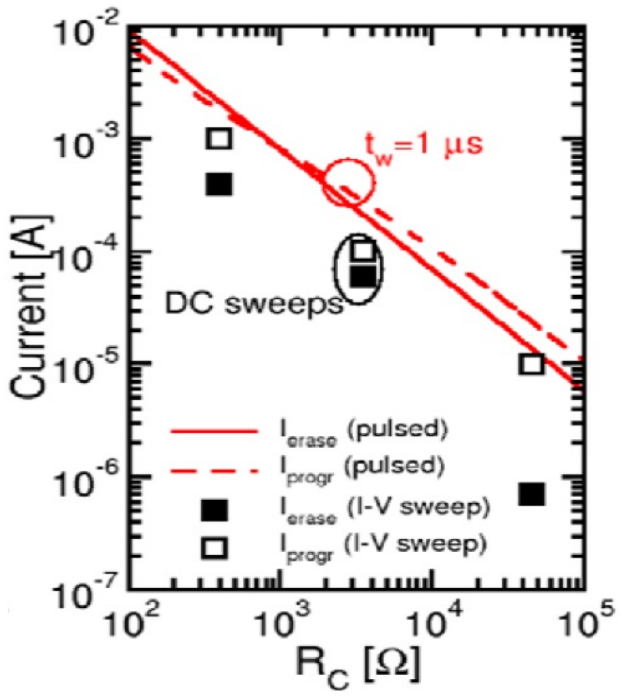

Figure 4.5: Current needed for programming/erasing the device as a function of R_C. Symbols refer to experimental data, lines to calculations or extrapolations

$$t_E = r_0/v_D \tag{4.1}$$

where r_0 controls the CF resistance through geometry and v_D depends on applied voltage as a result of ion migration. By assuming a truncated-cone shaped CF, as depicted in the inset of Fig. 4.4 [7], R_C can be calculated as [75]:

$$R_{PMC} = \rho \frac{H}{\pi r_0 (r_0 + H)} \tag{4.2}$$

where ρ is CF resistivity and the geometrical parameters are defined in the inset of Fig. 4.4 (where θ =45 ^{o}, for the sake of simplicity). Finally, the dissolution velocity can be modeled with the PF dependence on erase voltage V_E

$$v_D = v_{D0}\, e^{(\beta\sqrt{V_E})} \tag{4.3}$$

where β was extracted from Fig. 4.3 and v_{D0} is a fitting parameter. Results

from Eqs. (4.1 - 4.3) are reported in Fig. 4.4, for ρ = 10 mΩ cm, H = 60 nm and r_0 ranging from 2 nm to 200 nm. Note that ρ is to be considered an effective value for the CF resistivity, whose composition and electrical properties are likely to be not homogeneous; for the sake of simplicity, any possible dependence of ρ on CF size, hence on R_C, was neglected. Clearly, the calculations can account for the experimental data and allow studying the stability of low R_C ON states from retention measurements on higher R_C (i.e. less stable) ones.

4.5 Trade-off between data retention and program/erase current

We finally address the impact of R_C or R_{ON} on the current needed for programming (I_{prog}) and erase (I_{erase}). Fig. 4.5 shows I_{prog} and I_{erase} as a function of R_C, as obtained from experiments (voltage sweeps) or from calculations/extrapolations where voltage pulses of 1 μs were assumed. I_{erase} was determined at the ON-OFF transition during the erase sweep (or pulse), while I_{prog} corresponds to the compliance current used during the programming sweep (or pulse). The compliance current was shown to control R_C with good accuracy [5, 45] in fact, a smaller compliance current inhibits CF growth after its initial formation, thus imposing a higher R_C state. Calculations in Fig. 4.5, which were performed on the basis of a previously developed model [6], confirm the trend noted for I_{prog} data. However larger current is needed for fast operation in pulse mode, as already experimentally demonstrated for NiO-based resistive memories [76].

Erase data in Fig. 4.5 indicate that I_{erase} decreases for increasing R_C. This is because, according to Eq. (4.3), V_{erase} depends only logarithmically on R_C for a given t_{erase}, thus I_{erase}=V_{erase}/R_C decreases roughly linearly for increasing R_C. This is confirmed by the calculations shown in the figure, which were obtained for t_{erase}=1 μs. On the basis of the results in Fig. 4.4 and Fig. 4.5, it is clear that PMC retention properties have to be carefully traded-off with program/erase current requirements when choosing the R_C value to be programmed. Such a choice will depend on the final application and will be particularly critical for multilevel storage, where more than two R_C values have

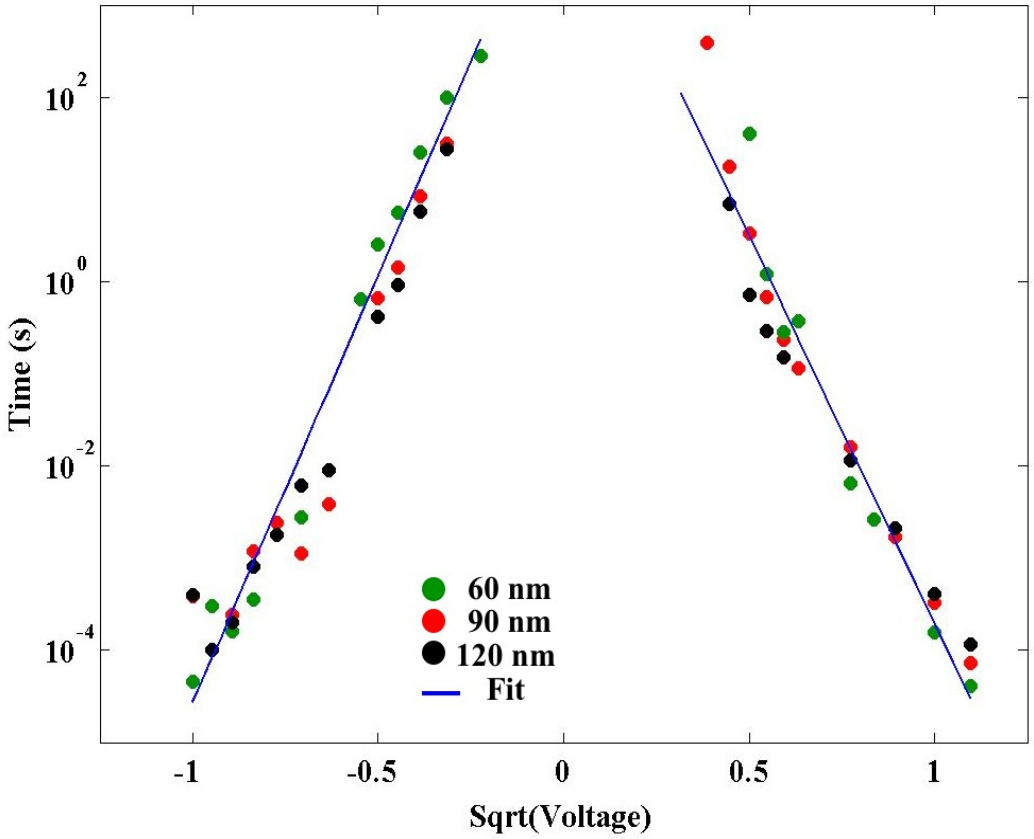

Figure 4.6: Effect of different electrolyte thickness on program and erase time dependence on erase voltage

to be located in the available resistance window.

4.6 Effect of electrolyte thickness on data-retention and program/erase kinetics in PMC cells

With programming kinetics in PMC cells explored in already published work [6] and having identified the physical mechanism behind the erase process in PMC cells in this chapter so far, it is important to analyze the effect of different electrolyte thickness on the data-retention and the program/erase kinetics. Fig. 2.1 showed a simple layered structure of a PMC device. The silver doped solid electrolyte layer is the most important layer in the device where the conductive filament is grown and erased repeatedly aiding in the successful operation of the device as a non-volatile memory with two stable resistance states (very high resistance OFF state and a low resistance ON state).

Since the conductive filament bridges the high resistance gap (in the electrolyte) between the top and the bottom electrodes, the nature of the grown conductive filament might be affected by the thickness of the electrolyte layer. Three samples having different electrolyte layer thickness ranging from 60nm to 120nm were prepared. Process conditions were varied slightly for different thickness samples in order to obtain similar electrolyte doping conditions for the three thicknesses. Times for programming (t_P) and erase (t_E) operations were obtained for different voltages from -1V to +1.2V. All the trials had similar initial resistance levels, i.e., for the erase operation all the devices were programmed with 1mA compliance current yielding an initial ON resistance of around 400 Ω and during the programming operation all devices were initially in the high OFF resistance state.

Fig. 4.6 shows the variation of program and erase times on different voltages for three different electrolyte thicknesses. There is no remarkable variation in these times with the electrolyte thickness. To verify if the actual thickness of the three samples were different another set of experiments were carried out. The leakage current of a device depends on its OFF resistance, which is proportional to the length of the conductor. Hence during the OFF state the leakage currents of the three different samples must be different if the thickness of the three samples was different.

To analyze the leakage currents in these three samples, current was plotted as the voltage was swept from 0 V to 250 mV. Since the threshold voltage of the particular batch of PMC devices used for this work was around 150 - 200 mV, current at voltage less than 100mV should be due to leakage charge through the electrolyte. Fig. 4.7 shows the current-voltage (IV) plots for different electrolyte thickness (but 5 μm lateral dimension devices). It is important to note that these IV sweeps were done on fresh cells from each sample. Before reaching the threshold voltage (showed in the figure), the leakage current of 60 nm sample is much higher than the 90 nm one, which is higher than the 120 nm sample. This clearly suggests a different electrolyte thickness in the

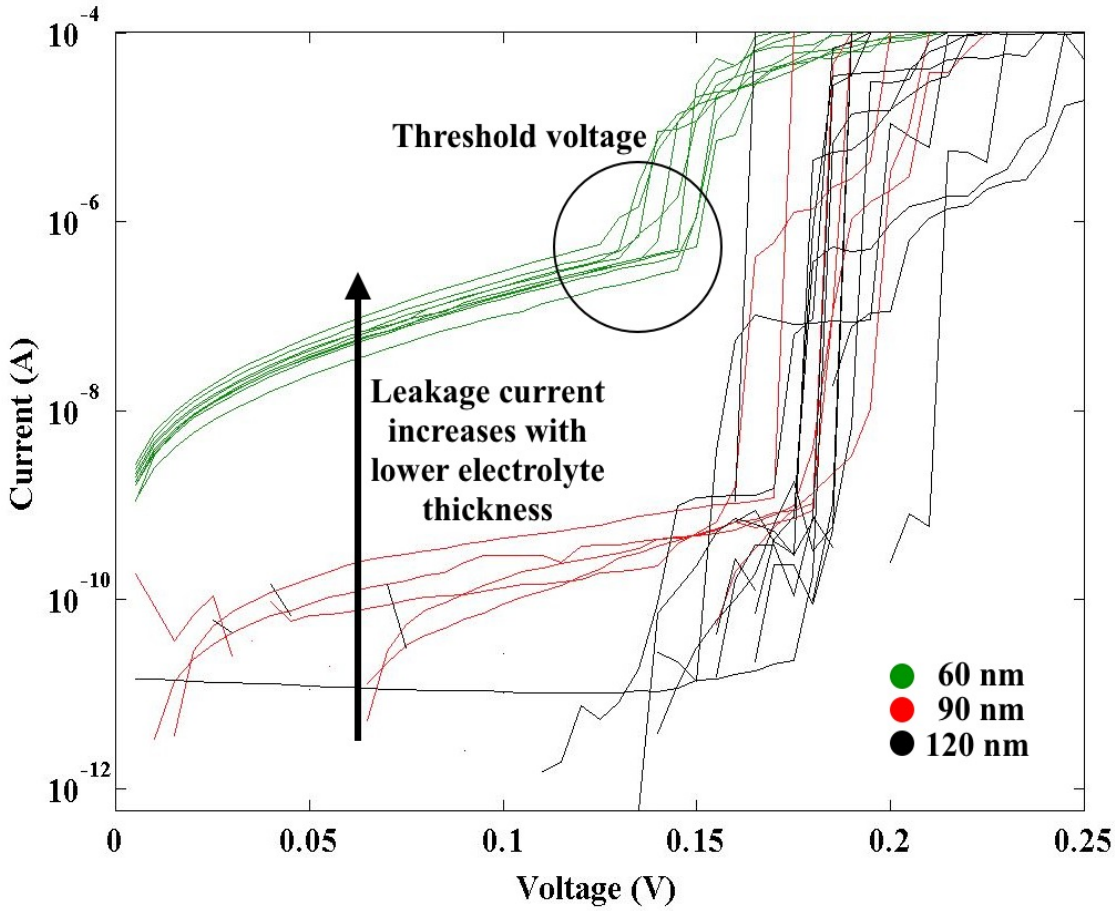

Figure 4.7: Leakage current measurements to verify the actual electrolyte thickness of different samples

three samples. The difference in the leakage currents however is larger than expected. This might be due to the different doping levels of these samples as silver penetration during photo dissolution process during the fabrication of these devices depends on the electrolyte thickness. Silver can penetrate to only around 50 nm depth into the electrolyte irrespective of how much silver is available for doping. This could lead to a lower number of available conductors (ions/electrons) in the electrolyte in the OFF state, reducing the leakage current [40, 60, 77].

Hence though the physical thickness of the different samples was different there was no noticeable change in the erase/program times amongst these samples. This could be explained as follows. All the devices were cycled (programmed and erased)

2-3 times before they were subjected to the tests mentioned in Fig. 4.6 to make sure the devices are in proper initial states before the tests. When the device is programmed or a positive voltage above the threshold voltage is applied the silver ions from the anode penetrate into the electrolyte and migrate towards the cathode where they reduce to a silver atom and eventually many such atoms contribute to the formation of a conductive filament. Hence after the first programming enough silver has actually entered the electrolyte though (as mentioned previously) due to higher thickness the amount of silver in the electrolyte was initially lesser. So after 2-3 program/erase cycles the electrolyte doping is similar in all the three samples. These 2-3 program/erase cycles led to an 'electrical forming' process, resulting in similar electrolyte conditions in the three samples. Also since the same compliance current was used to program the devices the amount of silver in a programmed device was the same and hence the time required for dissolving (during erase operation) this amount did not vary with the electrolyte thickness.

4.7 Summary of voltage-driven ON-OFF transition

The erase process in PMC devices was studied to address the ON state stability and the erase operation in pulse mode. The dependence of erase time on voltage and on the ON state resistance was characterized and modeled on the basis of by CF oxidation and Ag ion migration. Finally, the tradeoff between stability and the current needed for program and erase operations, was analyzed, allowing for design guidelines of multi-level PMC devices. Also there was no dependence of program and erase times on the electrolyte thickness and this was attributed to electrical forming that occurred in the first 2-3 PE cycles of the fresh PMC cells.

Chapter 5

LOW VOLTAGE CYCLING

5.1 Introduction

Programming kinetics in PMC cells, which occurs by voltage-driven electrochemical reactions and ion migration were characterized and modeled recently [6]. It was also shown in this work that a load resistor could be effectively used to tune the programmed resistance in pulsed mode, as it actively controls the program kinetics by reducing the cell voltage while the electrical pulse is maintained. The description was also verified with a semi-analytical model that accounted for the experimental data and could be used for multilevel programming applications.

The retention of various memory states in PMC cells and the effect of different types of stressing conditions on these states were analyzed in detail in chapter 3. The underlying mechanism behind the low resistance to high resistance transition (and vice-versa) was identified to be electrochemical in nature (thermal diffusion aided) rather than electromigration. The retention capabilities of different low resistance states were also determined to be significantly different (both with and without stress). Also the transition from low to high (er) resistance was found to be similar to a typical erase in PMC cells and was not a permanent failure.

Chapter 4 analyzed the erase process in PMC to address the ON state stability and the erase operation in pulse mode. The dependence of the erase time on the voltage and the ON state resistance was characterized and modeled on the basis of CF oxidation and Ag ion migration (electrochemical). The trade-off between stability and the current needed for program and erase operation, was analyzed, allowing for design guidelines of multilevel PMC cells. Having looked in individual operations of the PMC memory cells the next step was to study their cycling performance.

Future memory technologies must operate with the low power supply voltages, well below 0.9 V and eventually closer to 0.6 V, required for small geometry nodes.

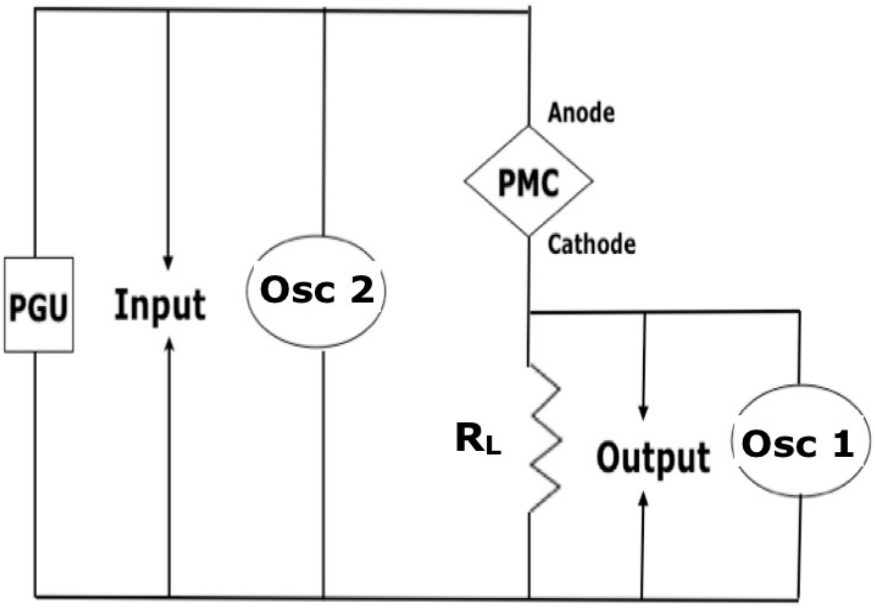

Figure 5.1: Setup used in program-erase (P-E) cycling and program speed determination of PMC devices in this chapter

Low voltage programming of PMC memory devices has previously been demonstrated using slow voltage sweeps [45] and small numbers of fast pulses [24]. However the reliability of the programmed and the erased states have to be analyzed at such low operating voltages. This chapter describes an investigation of low voltage time-symmetric programming and erasing of PMC devices for a significant number of write-erase operations (10_4 or more) over a range of programming currents from less than 1 μA to several hundred μA.

It is also a known fact that repeated cycling of any memory device would affect the future performance of the cell (insert reference). The deterioration in a memory cell will also depend on the cycling conditions like programming currents, erasing voltages, PE cycles, temperature of operation, etc (insert reference). It is important to analyze the effect of such cycling parameters on the memory cell and be able to predict any possible deterioration of the cell. This chapter also addresses a few of the afore mentioned cases in terms of cycling conditions in PMC cells.

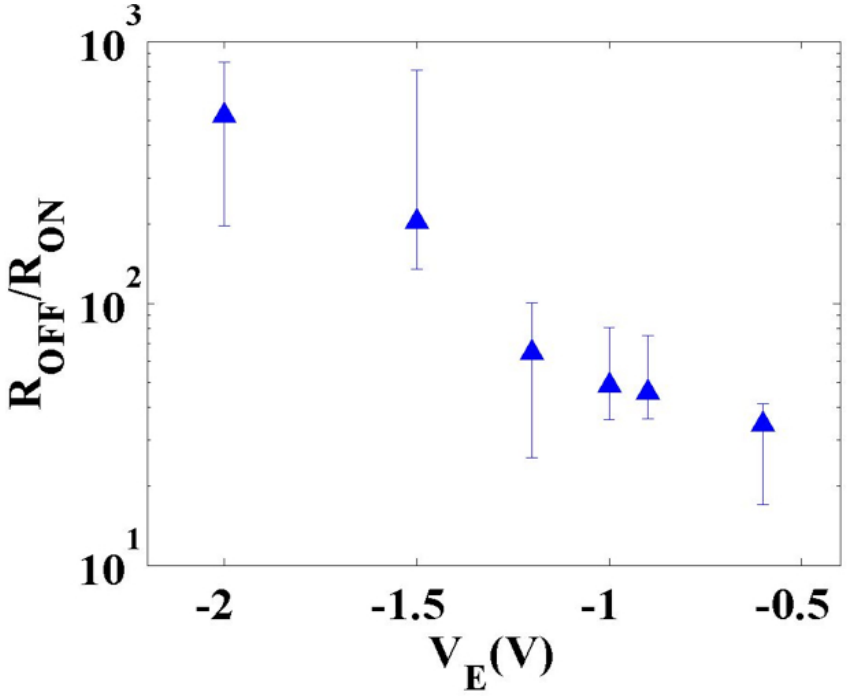

Figure 5.2: Ratio of R_{OFF}/R_{ON} for devices programmed to R_{ON} = 750 $\pm$ 250 Ω and erased with voltages from -0.6 V to -2.0 V

5.2 Experimental setup

Fig. 5.1 shows the measurement setup used in program-erase (P-E) cycling and program speed determination of PMC devices in this chapter. The PMC test device was connected in series with a current-limiting resistor (R_L) and a Sony Tektronix AWG2021 Pulse Generator Unit (PGU) was connected across this series combination. An Agilent Technologies Digital Oscilloscope DSO7032 (DO) was used to monitor both the input to the circuit from the PGU (OSC2) and the output voltage drop across R_L (OSC1). This setup is not the same as the setup used in the previous chapter (Fig. 4.1) as the DO (OSC1) was connected across the PMC cell in the previous setup, instead of R_L. This minor modification allowed the devices to switch considerably faster than in previous setups [6, 59], due to the reduced parasitics and by avoiding the loading of the PMC cell by the input impedance of the DO.

5.3 Low voltage erase

The programming characteristics of PMC devices have been extensively studied [6] and it is known that R_{ON} is inversely proportional to the programming current limit, and that programming time is dependent on voltage by an inverse exponential function. To complement this knowledge and assess the effects of low erase voltage on the R_{OFF}/R_{ON} ratio, a number of devices were programmed to similar values of R_{ON}, 750 $\pm$ 250 Ω, and then erased with 5 ms pulses of different voltage magnitude, V_E. It is known from previous studies [35, 36, 37, 45] that this 5 ms pulse width is much longer than the typical erase time in PMC cells, but this relatively long pulse width was chosen to ensure that the cell had settled to a stable OFF state before measuring it. The ratio of R_{OFF} to R_{OFF} was plotted with respect to V_E and this relationship is shown in Fig. 5.2. For the above conditions, average R_{OFF}/R_{ON} decreased with decreasing V_E,from a maximum of 520 at V_E = -2V to around 33 at -0.6 V. Note that the resultant R_{OFF} values obtained by these pulsed erase at low voltage, ranging from around 25 kΩ at - 0.6 V to 390 kΩ at -2 V, were very much smaller than the resistance of fresh (un-cycled) devices or even cells that were erased with long (DC) voltage sweeps of around -1 V. However it is important to note that this maximal R_{OFF} that is typically in the order of 100 MΩ or more [78], is characteristic of a device whose solid electrolyte contains only the Ag added during the processing steps involved in fabrication of PMC cells. The lower R_{OFF} seen in this experiment (and rest of this chapter) was most likely due to the additional silver that was added during the programming but not fully removed as a result of smaller erase voltages or shorter erase pulses (compared to DC sweeps). Nevertheless, even with a reduced R_{OFF}, the R_{OFF}/R_{ON} ratios are still sufficiently large even at the lowest programming voltage to permit simple sensing schemes to be employed.

5.4 Low voltage cycling

The program and erase voltage magnitudes used in this chapter, during cycling were adjusted in order to obtain steady cycling throughout the test period and 550 mV was found to produce consistent cycling results, thereby fulfilling the desire to operate below 0.6 V as mentioned before. Long (1 ms) programming and erase pulses that were symmetrical in pulse widths, were used to ensure that the devices switched and stabilized during each half-cycle to allow accurate measurements of both R_{ON} and R_{OFF} to be taken for every programming and erase operation. The cell resistance in the program (R_{ON}) and erase (R_{OFF}) half-cycles of the cycle can be determined by applying the simple voltage divider rule shown below.

$$R_{ON,OFF} = R_L \left(\frac{V_{INPUT}}{V_{OUTPUT}} - 1\right) \tag{5.1}$$

Fig. 5.3 shows typical cycling voltage traces as seen on the two channels of the DO for a programming voltage (V_P) of 550 mV and an erase voltage (V_E) of -550 mV. The dashed line is the input signal from the PGU and the solid line is the voltage trace across R_L. R_L was fixed, at 10 kΩ in this case and hence the symmetric voltages led to peak (while the device was in its ON state) program and erase current magnitudes that were approximately equal in each PE cycle. As seen in Fig. 5.3, the voltage drop across R_L in the case of the device programmed at 550 mV is approximately 0.36x the input voltage, resulting in an average R_{ON} that is around $1.8R_L$. Similarly, the voltage drop across R_L following the sharp erase event after the application of -550 mV is less than 1/10th the applied voltage, resulting in a R_{OFF} that is greater than $10R_L$ during the erase cycle ($R_{OFF}/R_{ON} > 10$). The R_{OFF}/R_{ON} ratio following the erase pulse is consistent with the results shown in Fig. 5.2.

Devices were subjected to 10^4 PE cycles with V_P = +550 mV, V_E = -550 mV, with R_L values of 1 kΩ, 10 kΩ, 100 kΩ, and 500 kΩ to determine the influence of cycling current on R_{ON} and R_{OFF}. Long (1 ms) program and erase pulses were again

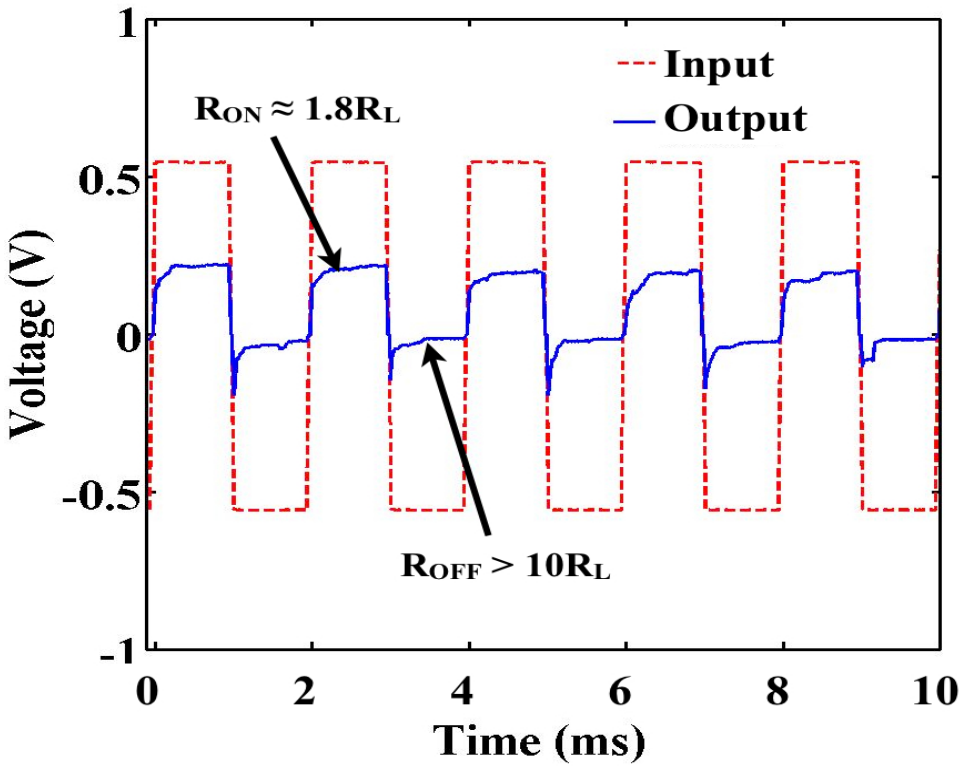

Figure 5.3: Voltage trace observed across the two channels of the DO (input and output) during the low voltage cycling of a PMC device with R_{ON} = 10 kΩ

used to allow accurate measurements of both R_{ON} and R_{OFF} to be taken for each cycle. With R_L = 500 kΩ, the largest value used in this chapter, the PMC device was programmed to an average R_{ON} in the order of 1.5 MΩ or $3R_L$, limiting the average peak program (I_P) and erase (I_E) currents to $I_P = I_E$ 0.27 μA. Similarly with R_L = 1 kΩ, the smallest value used in this analysis, the device was programmed to an average $R_{ON} \sim$ 1.5 kΩ (1.5 R_L) yielding a peak $I_P = I_P \sim 220$ μA. The measured median (t_{50}) R_{ON} and R_{OFF}, R_{OFF}/R_{ON} ratio, and the peak current attained for all R_L values used during 10^4 PE cycles are shown in Table. 5.1. Also shown in this figure is the ratio of the standard deviation of R_{ON} (STD) to the median value of R_{ON}, which will be discussed in more detail later.

The variation of R_{ON} and R_{OFF} with the peak current used during cycling (from Table. 5.1) is shown in Fig. 5.4 and the ratios: R_{ON}/R_L, R_{OFF}/R_L, and R_{OFF}/R_{ON} as a function of R_L are shown in Fig. 5.5. R_{ON} decreases with increasing programming

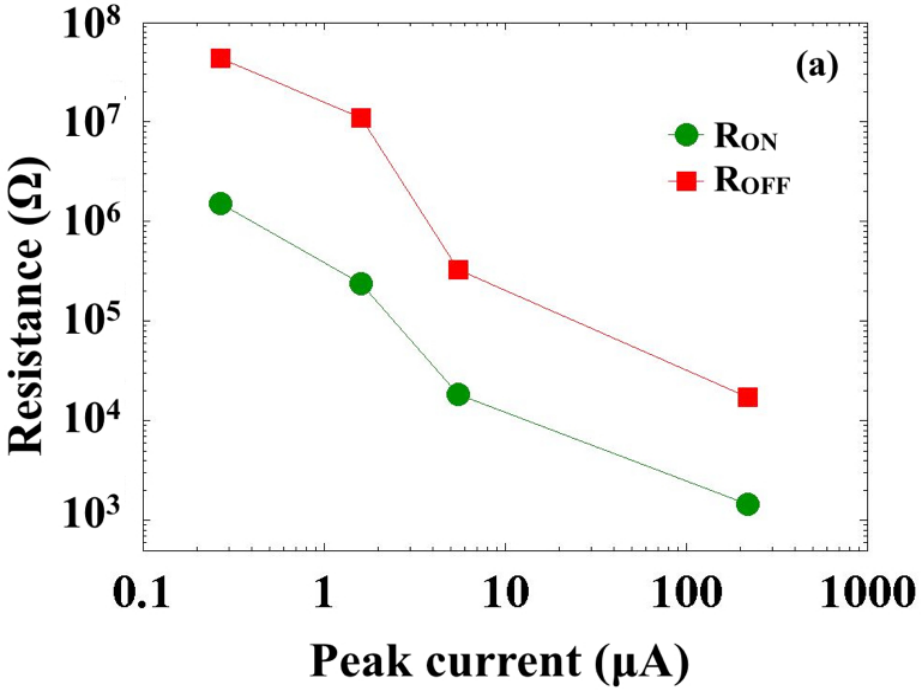

Figure 5.4: Variation of R_{ON} and R_{ON} with peak current

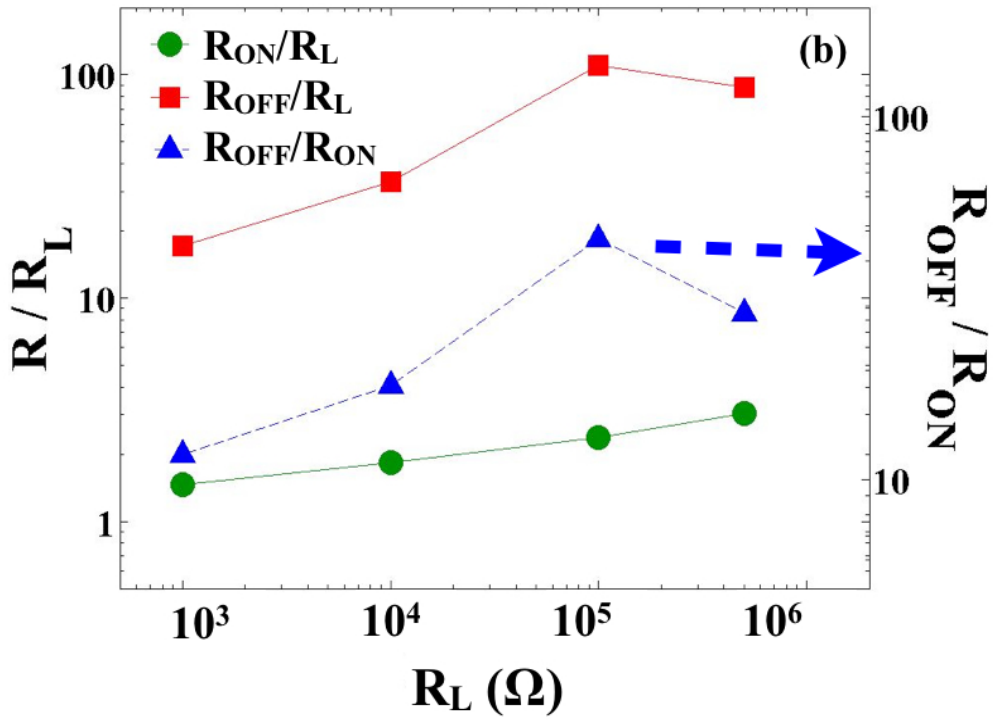

Figure 5.5: Variation of the ratios: R_{ON}/R_L, R_{OFF}/R_L, and R_{OFF}/R_{ON} as a function of R_L with low voltage cycling

R_L (kΩ)	R_{ON} (kΩ)		R_{OFF}	Peak current (μA)	R_{OFF} / R_{ON}
	Median	STD / Median	Median		
1	1.46	0.074	17.08 kΩ	220	11.7
10	18.27	0.278	332.8 kΩ	55	18.2
100	238.5	0.291	10.98 MΩ	1.6	46
500	1520	0.33	43.67 MΩ	0.27	28.8

Table 5.1: Median (t_{50}) R_{ON} and R_{OFF}, R_{OFF}/R_{ON}, and peak current for different R_L during 10^4 PE cycles

current as expected from the results of previous work [6] on PMC programming, but in this case, R_{ON} becomes higher for increasing R_L than would be predicted by a simple inverse linear relationship between R_{ON} and I_P. Hence the cell either undergo softer programming at higher R_L than expected, possibly due to the increased effects of parasitics at such high resistances, or that the programming is slightly harder at lower R_L, possibly due to thermal effects (Joule heating) caused by the high current flow for the relatively low ON and OFF state resistances. More work is required to determine the exact cause of this non-linearity, although a similar effect has been noted in previous PMC programming studies at higher voltage [6].

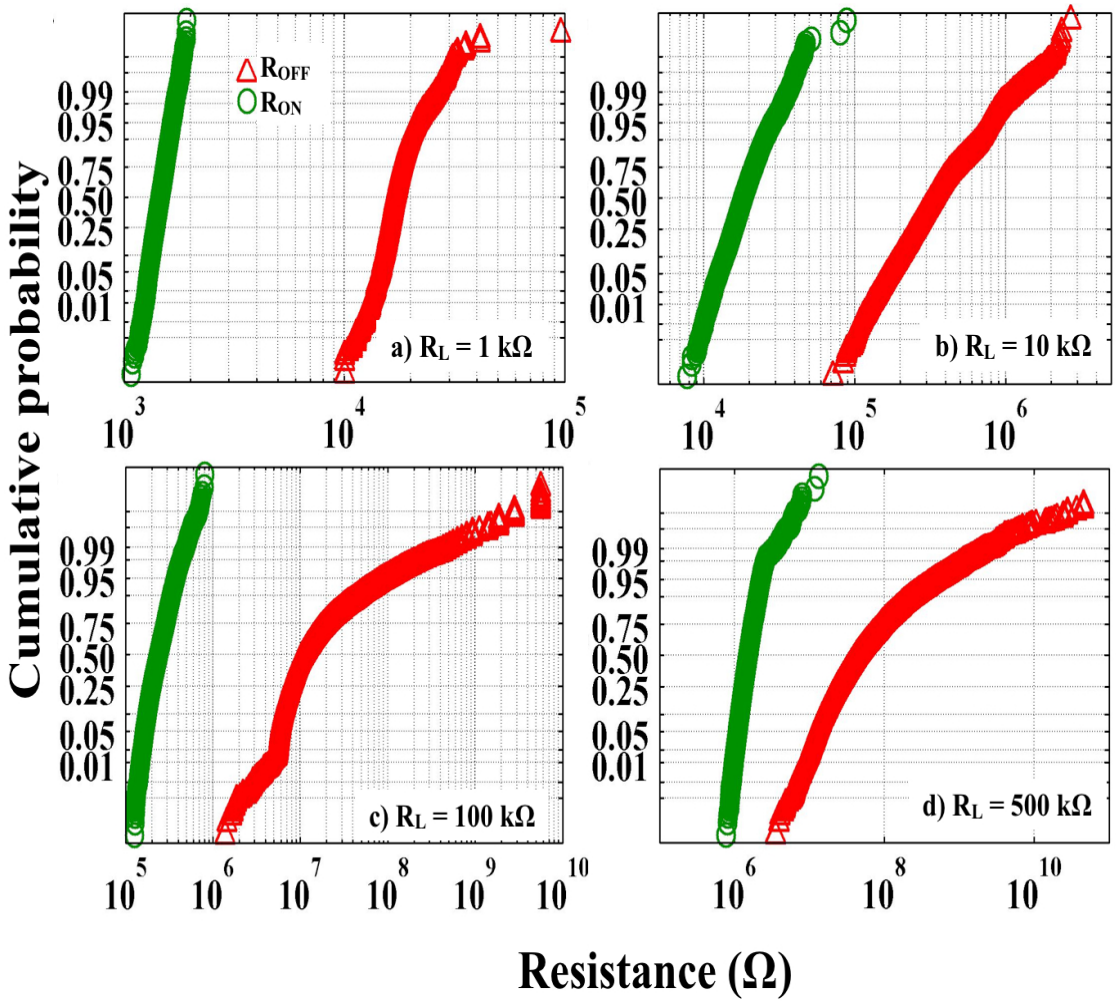

Figure 5.6: R_{ON} and R_{OFF} distributions (cumulative probability) of devices cycled for 10^4 cycles with R_L values of 1 kΩ, 10 kΩ, 100 kΩ, and 500 kΩ with V_P = 550 mV, V_E = -550 mV

Fig. 5.6 shows the R_{ON} and R_{OFF} distributions (cumulative probability vs. resistance) for the same devices cycled with the four different R_L values (1 kΩ, 10 kΩ, 100 kΩ, and 500 kΩ) for 10^4 PE cycles (V_P = +550 mV for 1 ms and V_E = -550 mV for 1 ms). Importantly R_{ON} and R_{OFF} were measured for every cycle to produce these cumulative probability plots. The high resistance distributions of the R_{OFF} plots above the 10^7 Ω range are artificially wide due to the limitations of the measurement setup. It is evident from the plots (and from Table. 5.1) that the distributions of R_{ON} and R_{OFF} are narrowest for the lowest R_L/ highest I_P and I_E (ignoring the artificial broadening of the resistance ranges in the high resistance regions), leading to the widest margin between the ON and OFF tail states, i.e., those with cumulative probability > 0.99 for R_{ON} and < 0.01 for R_{OFF}. But the margin between ON and OFF states clearly decreases with increasing R_L. There is no overlap between the R_{ON} and R_{OFF} distributions for R_L = 1 kΩ to 100 kΩ, except two (out of 10^4 programmed states) high resistance outliers In case of R_L = 10 kΩ, allowing such low voltage and low current cycling to be employed with adequate differentiation between the stored states. However, approximately 1 of the programmed states overlap in the case of R_{ON} = 500 kΩ, making it unacceptable for data storage.

5.5 Effect of cycling on program kinetics

In order to study the effect of cycling on the programming time (t_P), devices were cycled as before (V_P = +550 mV for 1 ms and V_E = -550 mV for 1 ms) for different numbers of cycles and with different R_L values (1 kΩ, 10 kΩ, 100 kΩ, and 500 kΩ), and t_P was determined after cycling using the DO to measure the time between the input pulse rising edge (V_P = 1V) and the rise in output voltage. Comparison of post-cycled device t_P to that of a fresh device (approximately 100 μs for these test conditions) was the main objective of this section.

Five to ten t_P measurements were made on ten different devices after 5 x 10^4 cycles with different R_L and the ratio of post-cycling t_P to the t_P of the fresh (un-

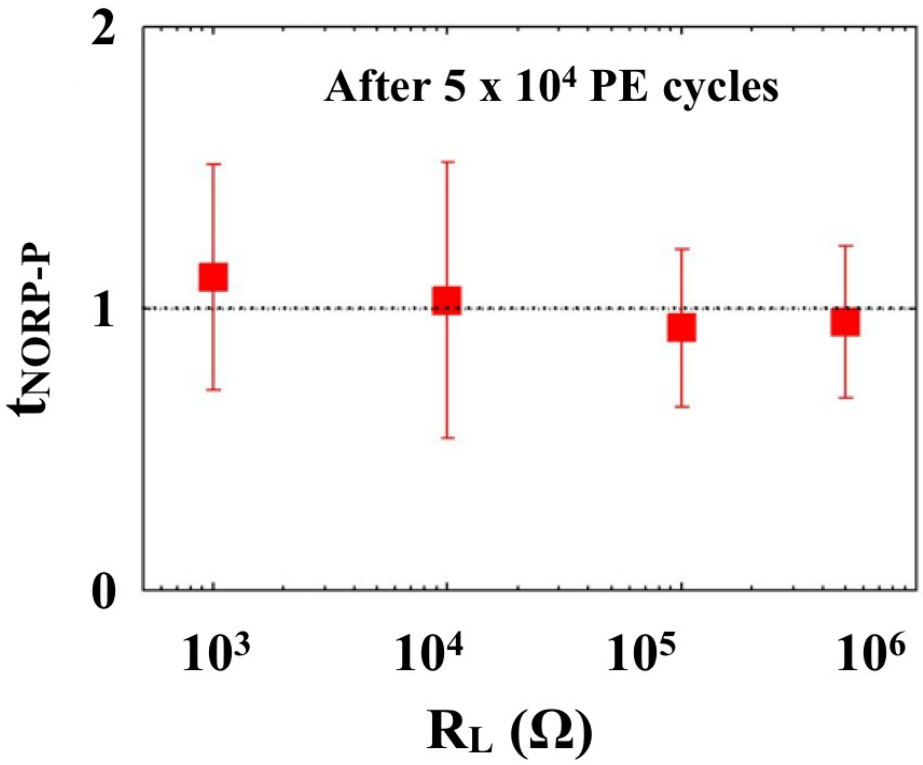

Figure 5.7: Ratio of post-cycling t_P to t_P (t_{NORM-P}) of a fresh device after 5 x 10^4 cycles vs. R_L

cycled) device, termed normalized t_P (t_{NORM-P}), was calculated for this analysis. It is important to note that a normalized value of 1 implies that there was no change in program time after cycling. The results of this analysis are shown in Fig. 5.7, which gives the distribution of t_{NORM-P} vs. R_L after 5 x 10^4 cycles. It is evident from the plot that there is no significant difference in t_P following cycling for higher R_L values but there appears to be a slight upward trend in t_{NORM-P} for lower R_L, indicating that the devices are moderately slower following cycling.

Next, five to ten t_P measurements were made on ten different devices after different number of PE cycles, from 10^3 to 1.5 x 10^6 cycles, with R_L = 100 kΩ (I_P = I_E = 1.6 μA) to further analyze the performance of PMC cells after cycling them at low currents. The t_P obtained after a particular number of cycles was normalized to the t_P of the same device before it was cycled (fresh device) as before and Fig. 5.8 shows the results of this analysis. There was no clear relationship between the t_{NORM-P} and the

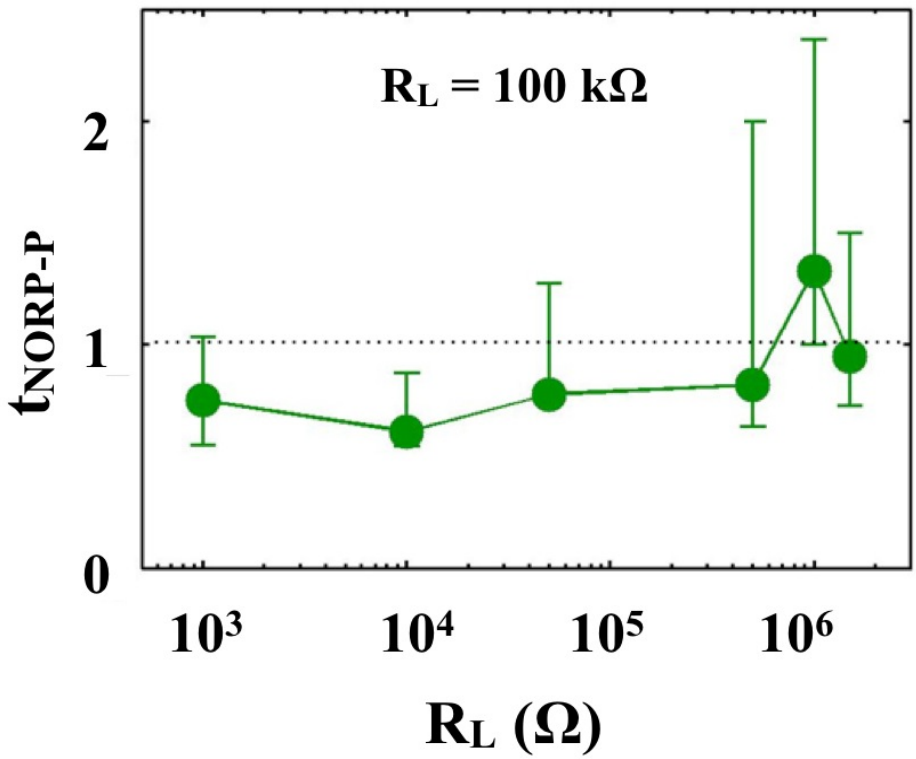

Figure 5.8: Ratio of post-cycling t_P to t_P (t_{NORM-P}) of a fresh device cycled with R_L = 100 kΩ vs. number of cycles

number of cycles, and their values remained close to or slightly less than 1 after 1.5 x 10^6 cycles. This confirmed that the programming time of the devices is not affected by high numbers of cycles with low I_P and I_E.

5.6 Discussion

The low voltage symmetric cycling conditions selected for these experiments led to stable PE cycling but the value of the current limiting series resistor had a significant effect not only on R_{ON} but also on R_{OFF} and on the distributions of these parameters. The relationship between R_{OFF}/R_{ON} and the erase voltage for single pulse erase, as shown in Fig. 5.2, combined with the data of Fig. 5.4, Fig. 5.5 and Fig. 5.6, suggest that a low voltage erase as part of low voltage cycling scheme will result in an OFF state resistance that is not necessarily the same as a fresh (unwritten) or deeply erased device but is actually only a few multiples of 10 higher than the R_{ON} ($\sim$ 10x - 50x) of

the device. As mentioned previously, this strongly suggests that the maximum current limit created by R_L sets R_{ON} as expected, albeit in a somewhat non-linear fashion which must be investigated further, but that the erase conditions during the dissolution of the filament result in incomplete removal of electrodeposited Ag in the electrolyte. Previous work on PMC cells regarding their erase process [59] determined that the dissolution process has a strong electrochemical character, i.e., the conducting filament created by reduction of Ag ions during the programming step is oxidized and the ions so created removed from the filamentary region by the electric field. A limited current and limited bias will therefore result in limited oxidation and transport of the filamentary silver.

In devices programmed to low R_{ON} with a high programming current, the initial filament will be relatively thicker [6] and partial dissolution will likely result in a residual but still largely intact filament, hence the low R_{OFF} values obtained. As R_{ON} becomes higher with lower I_P, the partial dissolution of the narrower filament will likely result in a more fragmented OFF state pathway and consequently higher R_{OFF}. This more fragmented filament is likely to result in a larger spread in R_{OFF}, which is what is seen in the results of Fig. 5.6 for the higher values of R_L (noting that the resistance values over 10^7 Ω are not accurate due to measurement limitations). However, the distributions in Fig. 5.6 of the 10^4 R_{ON} and R_{OFF} states in the case of R_L = 1 kΩ ($I_P = I_E$ = 220 μA) are near-Gaussian (straight line in the cumulative probability plot) and with a relatively small standard deviation, as indicated by the high slope of the lines and the data shown in Table. 5.1. This suggests that both the ON and OFF states are well defined. The R_{ON} distributions remain somewhat Gaussian until they reach very high values in the case of R_L = 500 kΩ but the standard deviation increases with increasing R_L or decreasing I_P (Table. 5.1). This increase in standard deviation is expected as the filaments that constitute the higher resistance ON states are thought to be thinner, less well defined, and more fragile (more susceptible to thermal diffusion)

and hence the range of resistances they produce, even for near identical programming conditions, will tend to be larger.

It was noted during this work that there is no obvious change in programming time for lower programming currents, even after 1.5 million cycles, but there would appear to be a slight increase in t_P following cycling at the highest currents. It can be seen that the ratio of R_{OFF} to R_L decreases with decreasing R_L from Fig. 5.5. Hence when a voltage is applied across both the PMC cell and R_L, the voltage drop across the PMC element is proportionally less for the low R_L case than for the high R_L case. Again from previous work [6] on PMC erase operation, it is clear that t_P increases exponentially with decreasing voltage across the device. Hence, the slight increase in t_P noted after 5 x 10^4 cycles with lower R_L is due to the reduction in the voltage across the PMC element and not due to the deterioration of the device due to cycling at high currents.

5.7 Summary of low voltage cycling on PMC devices

This chapter demonstrated that it is possible to utilize symmetric program-erase cycling for PMC devices at voltages that are within the specification of the nanoscale geometry devices at the end of the current version of the International Technology Roadmap for Semiconductors ($<$0.6 V) [79]. Single pulse erasing of devices programmed to a low R_{ON} suggested that the average R_{OFF}/R_{ON} ratio decreased with decreasing erase voltage, from a maximum of 520 at V_E = -2 V to around 33 at -0.6 V. This indicated that a low cycling voltage was probably less effective at removing the electrodeposited silver which had been added during the programming cycle but that the R_{OFF}/R_{ON} ratios were still sufficiently large ($>$10) to permit simple sensing schemes to be employed. The maximum current limit during cycling set by series resistance R_L defines the ON state resistance of the device and the symmetric low voltage erase conditions result in an OFF state resistance that is a few multiples of ten ($\sim$ 10x - 50x) higher than the ON state resistance for a wide range of program/erase currents (0.27 to 220 μA).

The distributions of R_{ON} and R_{OFF} are narrowest for the lowest R_L, leading to the widest margin between the highest ON and lowest OFF (tail) states, however, the margin between these states clearly decreases with increasing R_L even though the average R_{OFF}/R_{ON} ratio generally increases with increasing R_L. There was little or no overlap between the R_{ON} and R_{OFF} distributions for R_L = 1 kΩ to 100 kΩ, which would allow low voltage and low current cycling to be employed with adequate differentiation between the stored states, but significant tail state overlap occurs in the case of R_L = 500 kΩ. We believe that the wide resistance distributions in both the ON and OFF states at lower programming currents are due to less well-defined or fragmented residual filaments following program and erase operations respectively. Finally, there is no significant change in switching speed with the number of low voltage symmetric program-erase operations up to 1.5 x 10^6 cycles but lower values of R_L tend to lead to slightly slower switching speed due to the lower voltage drop across the device in its relatively low resistance off state.

Chapter 6

SWEPT COMPLIANCE PROGRAMMING AND PRE-CONDITIONING OF PMC CELLS

6.1 Introduction

Programmable metallization memory cell is also referred as Conductive Bridge Random Access memory (CBRAM) sometimes [80]. Fig. 6.1 shows a schematic of 1T1R CBRAM cells used in this chapter. The construction shown in Fig. 6.1 provides more control on the CBRAM cell as it allows easy dynamic modulation of current through the memory element by controlling the word line of the access transistor. The process steps for the cells used in this chapter were similar to the basic processing steps previously discussed in chapter 2 of this work.

Chapters 3 to 5 discussed in detail the retention, erase process and cycling behavior of PMC cells. All the chapters discussed the variations found in the experiments in PMC cells, particularly the variation in the behavior of PMC ON states. Or simi-

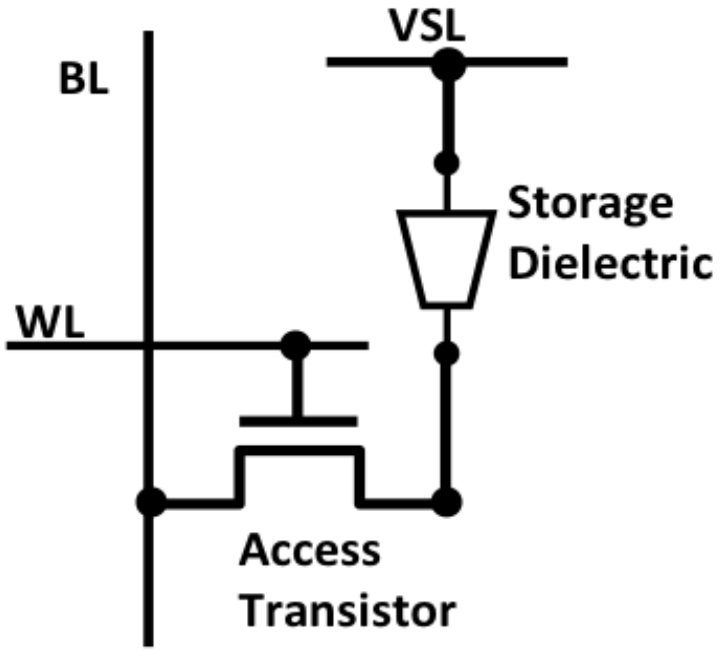

Figure 6.1: Schematic of 1T1R CBRAM cells used this chapter [9]

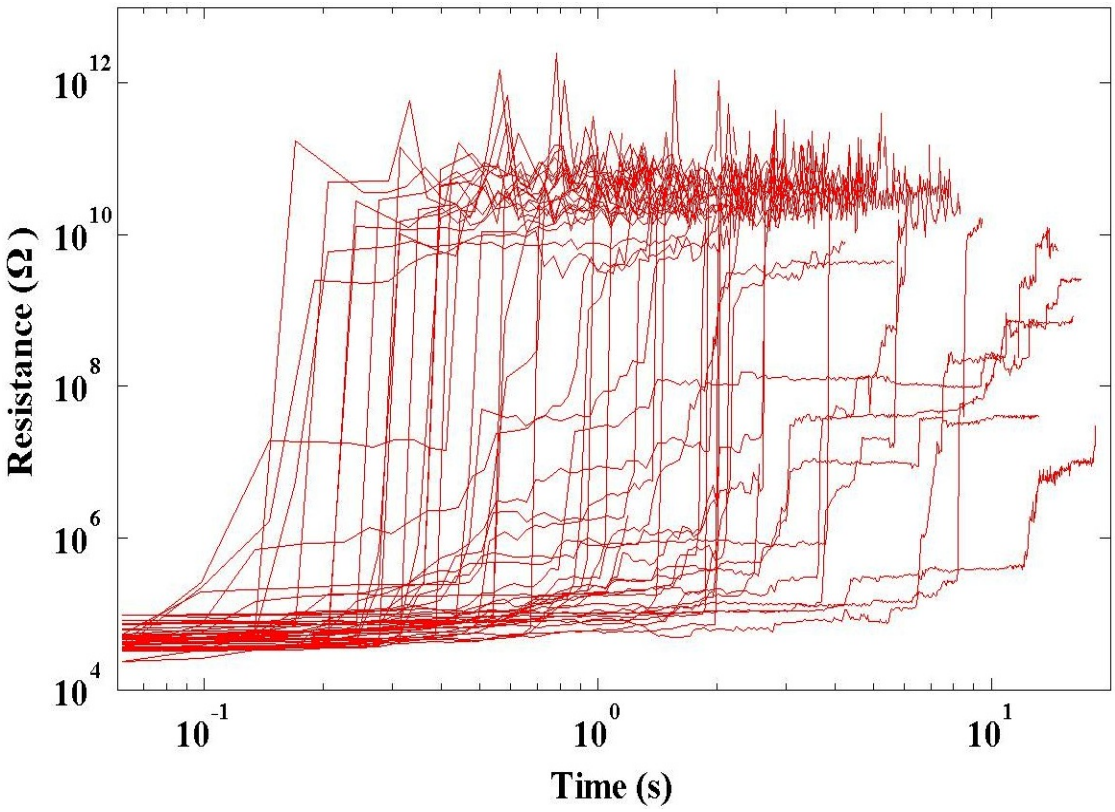

Figure 6.2: Variation of R_{ON} with time for 50 states on one CBRAM cell programmed (to similar R_{ON} in every trial) and stressed with a constant stress voltage V_{STRESS} = -75 mV

lar resistance PMC ON states behaved differently under similar stress/erase conditions (Fig. 3.16 for example). This was attributed to variation in process conditions and experimental setups involved. These tests were performed on test cells fabricated at ASU on base wafers provided by Qimonda. These test devices were discrete test devices that were not in arranged large arrays with access transistors. They were processed in a class 100 cleanroom and hence variations in materials, equipment and procedures were expected [81]. So it was difficult to identify the reason behind the variation (whether it was inherent to the cells or was due to non-ideal external conditions) found in the experiments so far.

Fig. 6.2 shows the variation of R_{ON} with time for 50 states on one CBRAM cell programmed (to similar R_{ON} in every trial) and stressed with a constant stress voltage V_{STRESS} = -75 mV. The cell was programmed with a current limit set by the word line

of the access transistor (V_{WL} = a high constant voltage to allow the flow of sufficient programming current) to achieve a $R_{ON} \sim 50$ kΩ every trial with V_{SL} - V_{BL} (= V_{CELL}) maintained at constant bias voltages (DC programming). After programming the cell, a constant negative stress voltage (-75 mV in Fig. 6.2) was forced across the cell and its resistance was monitored. As seen in chapter 3, the ON states remained relatively stable (with a gradual increase) for a certain time and transitioned to the OFF state abruptly after a certain time (called t_E as before). The cell was then reprogrammed with similar current limit and stressed again. This process was repeated 50 times on the same cell. As seen from the figure, t_E varied from around 0.1 s to 10 s for 50 states programmed with similar bias conditions and on the same cell. Hence though the cell was programmed to similar R_{ON} ($R_{ON-INTIAL}$) in every trial, the variation of t_E under the same negative voltage varied almost between two orders of magnitude. Since these cells were fabricated under much better processing conditions, not all of this variation could be attributed to the process. As mentioned previously since a CBRAM cell works as a memory element by repeatedly growing and dissolving a CF, a significant amount of statistical variation could be inherent to the device. Though variation in parameters is acceptable in any memory technology, it makes the optimization of cycling conditions for a particular application more challenging and more so in Multi-Level (ML) applications.

6.2 Swept compliance programming
Non-similar programming energy

In Fig. 6.2 the cell was programmed with a constant bias to all the three terminals, V_{BL}, V_{WL} and V_{SL} or the cell was programmed with a Constant Compliance (CC) current (since V_{WL} was constant). Fig. 6.3 shows the variation of R_{ON} with time for 50 states on one CBRAM cell programmed (to similar R_{ON} in every trial) and stressed with a constant stress voltage V_{STRESS} = -75 mV, but programmed with Swept Compliance (SC) programming. Or V_{WL} of the access transistor was swept from zero to its final

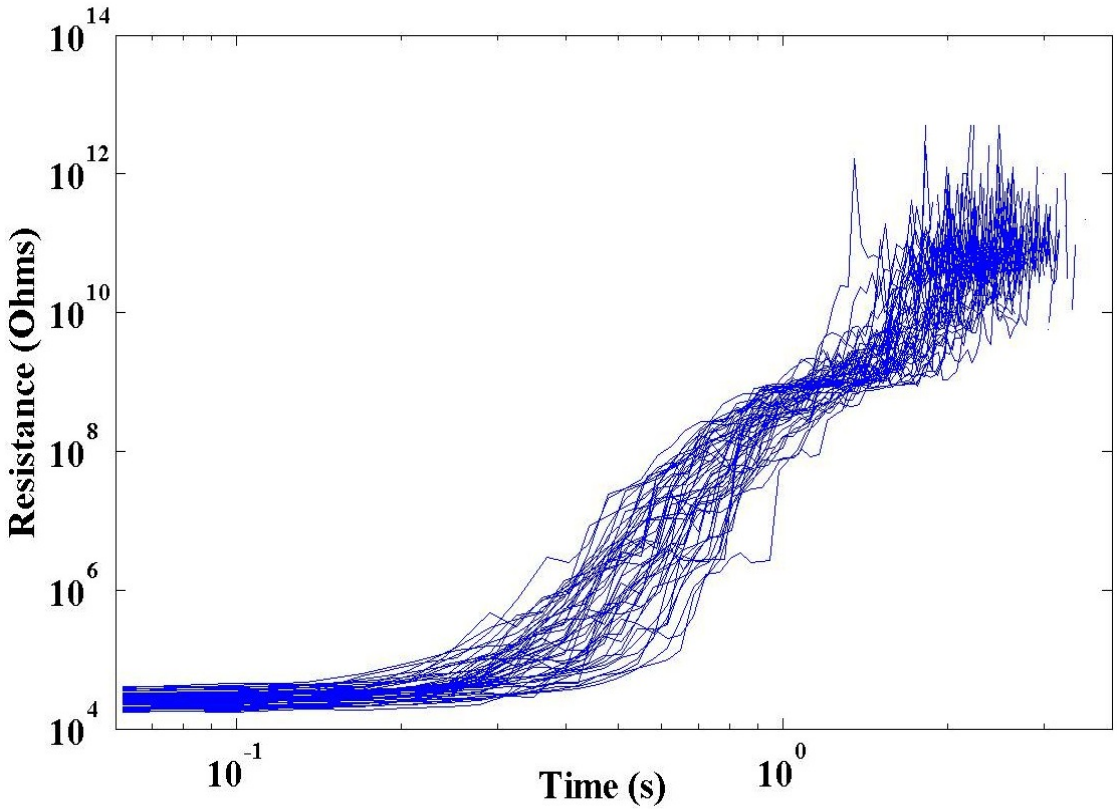

Figure 6.3: Variation of R_{ON} with time for 50 states on one CBRAM cell programmed (to similar R_{ON} in every trial) and stressed with a constant stress voltage V_{STRESS} = -75 mV, but programmed with swept compliance

(high) value (final value was the same as in Fig. 6.2) in around 100 DC steps during the programming operation, while V_{BL} and V_{SL} were maintained at the same constant voltage as before. Since the gate voltage of the access transistor or V_{WL} determines the current flow in through the CBRAM cell, if V_{WL} is swept instead of being held constant, the current limit is also varied from zero to a final (high) value during the programming operation of the cell. This current sweep (achieved through V_{WL} sweep) is shown in Fig. 6.4 for CC and SC programming. The y-axis shows the current flowing through the CBRAM cell during the programming operation and the x-axis shows the step number of the DC voltage sweep of V_{WL}. In CC programming the current remains fairly constant during the programming operation (though in CC, V_{WL} was swept in a small range close to the final value in order to keep the number of DC sweep steps

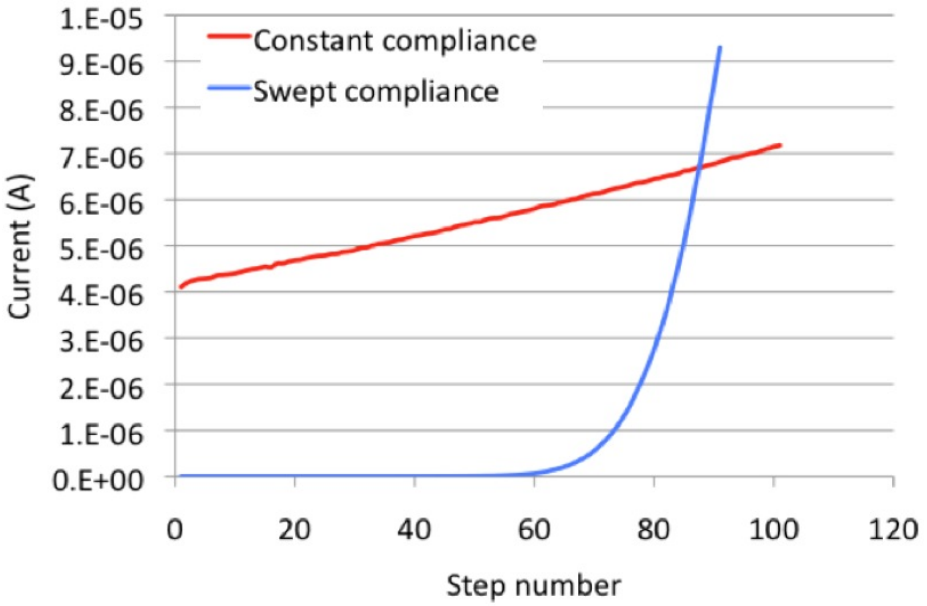

Figure 6.4: Current sweep (achieved through V_{WL} sweep) for constant compliance and swept compliance programming. The y-axis shows the current flowing through the CBRAM cell during the programming operation and the x-axis shows the step number of the DC voltage sweep of V_{WL}

similar to SC programming) while in SC programming the current varies continuously from 0 to a maximum current in $\sim$ 100 steps (V_{WL} sweep steps). The maximum final current ($I_{COMP-PROG}$) was maintained the same in both cases.

Comparing Fig. 6.2 and Fig. 6.3 it can be clearly seen that the ON states programmed with SC behaved differently than states programmed with CC. Though the $R_{ON-INITIAL}$ of the states programmed with SC were similar ($\sim$ 50 kΩ) to the ones programmed with CC, their behavior with time under the same negative voltage stress (V_{STRESS} = -75 mV) was much more similar to each other than the ones programmed with CC or the variation in t_E of the 50 states programmed with SC was very minimal. Another observation from Fig. 6.3 is that the transition from the ON to OFF state of the states programmed with SC is gradual and not abrupt as in case of the states programmed with CC.

Fig. 6.5 shows the variation of t_E as a function of trial number for states programmed with CC and SC. This figure again emphasizes the fact that the variation in

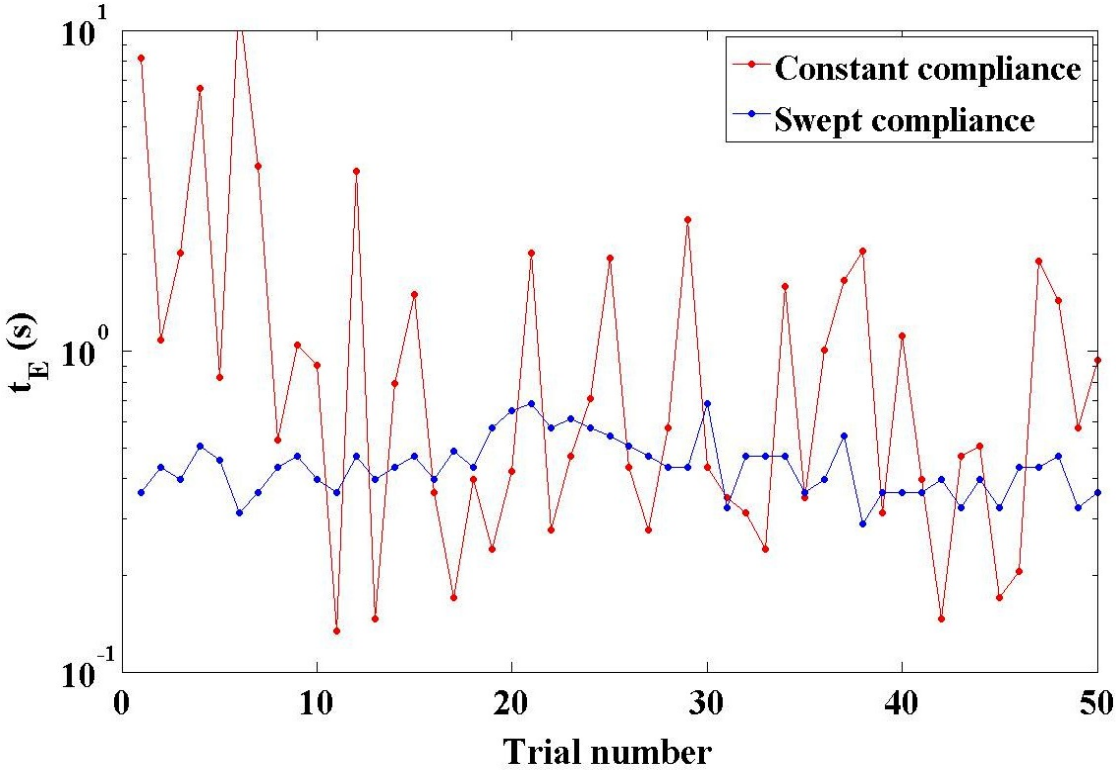

Figure 6.5: t_E of 50 states programmed with SC and CC

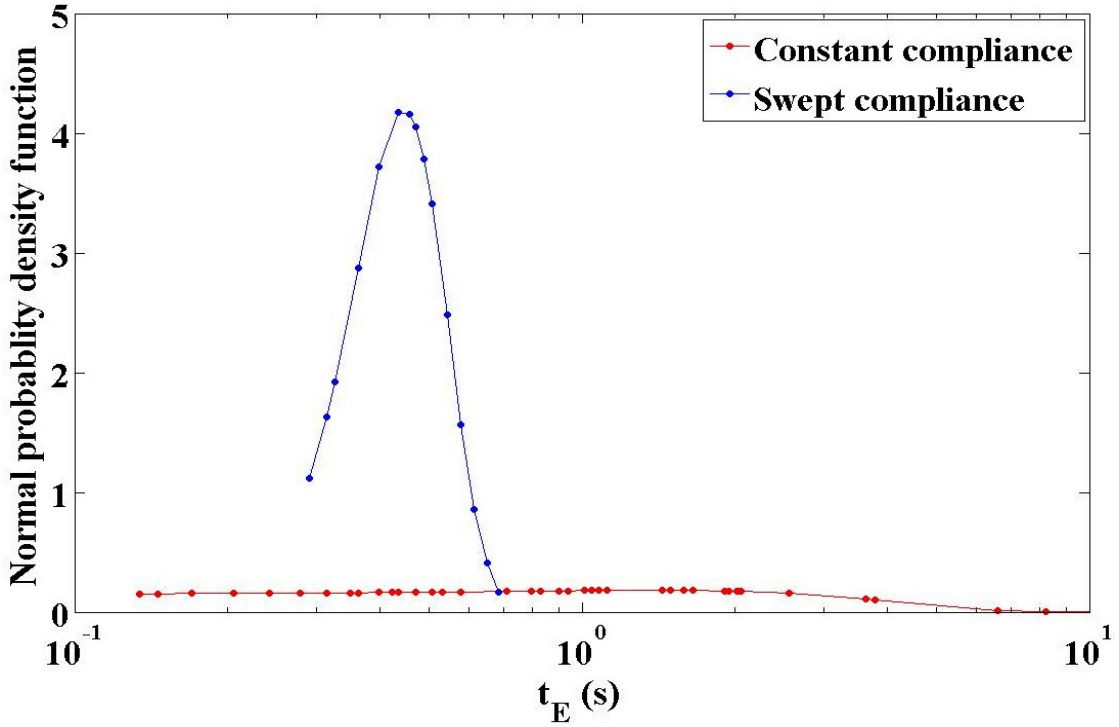

Figure 6.6: Variance of t_E of 50 states programmed with SC and CC

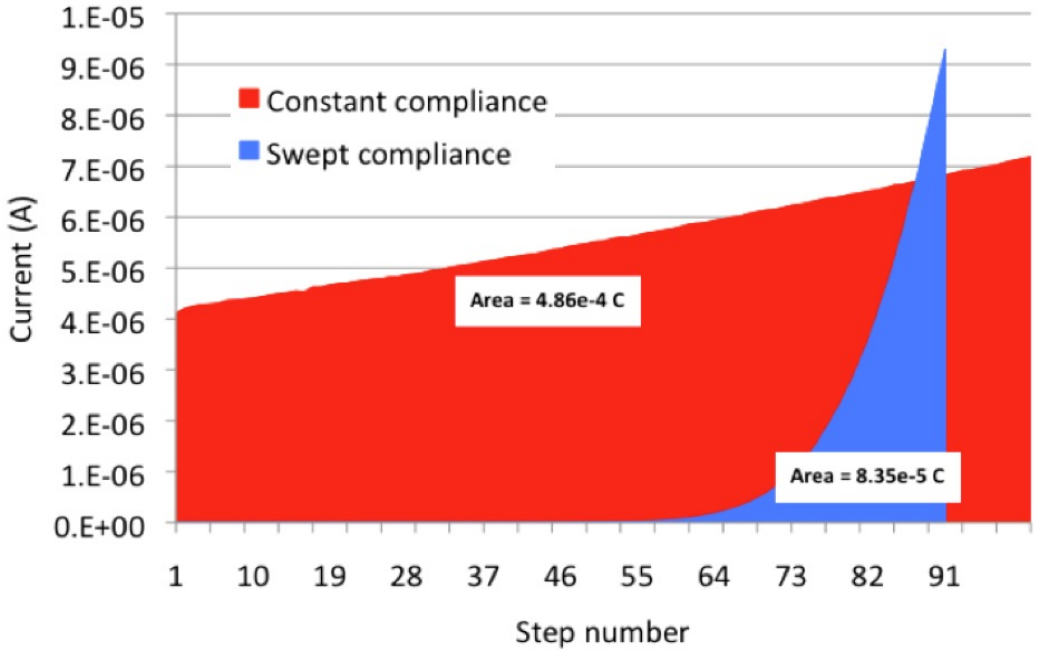

Figure 6.7: Current variation with sweep step number during a CC and a SC programming operation (same as in Fig. 6.4) but with areas under the curve (programming energies) for the two types of programming

t_E for states programmed with SC is much smaller than the ones programmed with CC. Fig. 6.6 shows the variance of t_E of 50 states programmed with SC and CC. The t_E of states programmed with SC fall into a much smaller window than the ones programmed with CC, indicating that the states programmed with SC behave more uniformly than the ones programmed with CC under negative stress.

Similar programming energy

Fig. 6.7 shows the program current ($I_{COMP-PROG}$) evolution with step number during a CC and a SC programming operations (same as in Fig. 6.4) but with areas under the curve for the two types of programming as well. Since the DC sweep step number is equivalent to the sweep time (as 1 DC sweep step $\sim$ 1 s), the area under the curves for the two types of programming is equivalent to the programming energy used in each case. It can be seen from the plot that the energies are not equivalent in both the cases. To allow for a more fair comparison of t_E in the two types of programming, this sec-

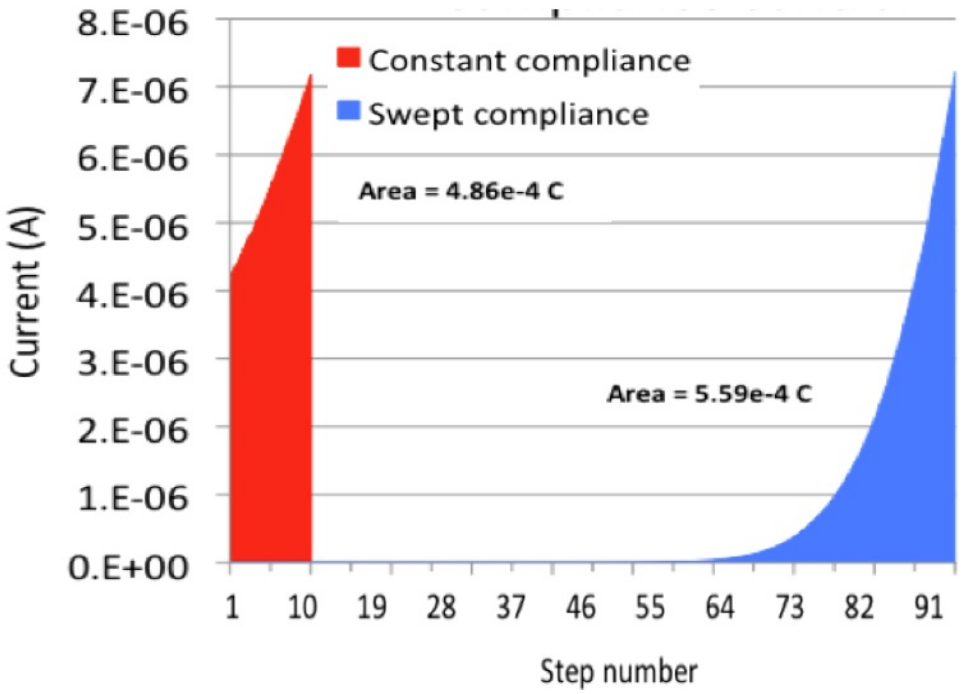

Figure 6.8: Current variation with sweep step number during a CC and SC programming operation with sweep steps adjusted to achieve similar programming energies in both types of programming for a more fair comparison of t_E variation

tion details the results of SC and CC programming with similar programming energies as shown in Fig. 6.8. The sweep steps were adjusted during SC (while the maximum current compliance was maintained the same) to achieve similar programming energies in both cases and the experiments detailed in the previous section were repeated. Fig. 6.9, Fig. 6.10 and Fig. 6.11 show the results of these experiments and it can be seen that the behavior of the ON states pre-conditioned with SC (with programming enegry made equal to CC) is similar to the ones obtained in the previous section (lower programming energy used in SC, compared to CC) and SC programming does indeed improve the behavior of similar ON states by reducing the variation in t_E under the same negative voltage stress.

6.3 Discussion on swept compliance programming

It was clear from the previous section that SC programming improved the performance of similar resistance ON states in CBRAM cells under stress by reducing the variation

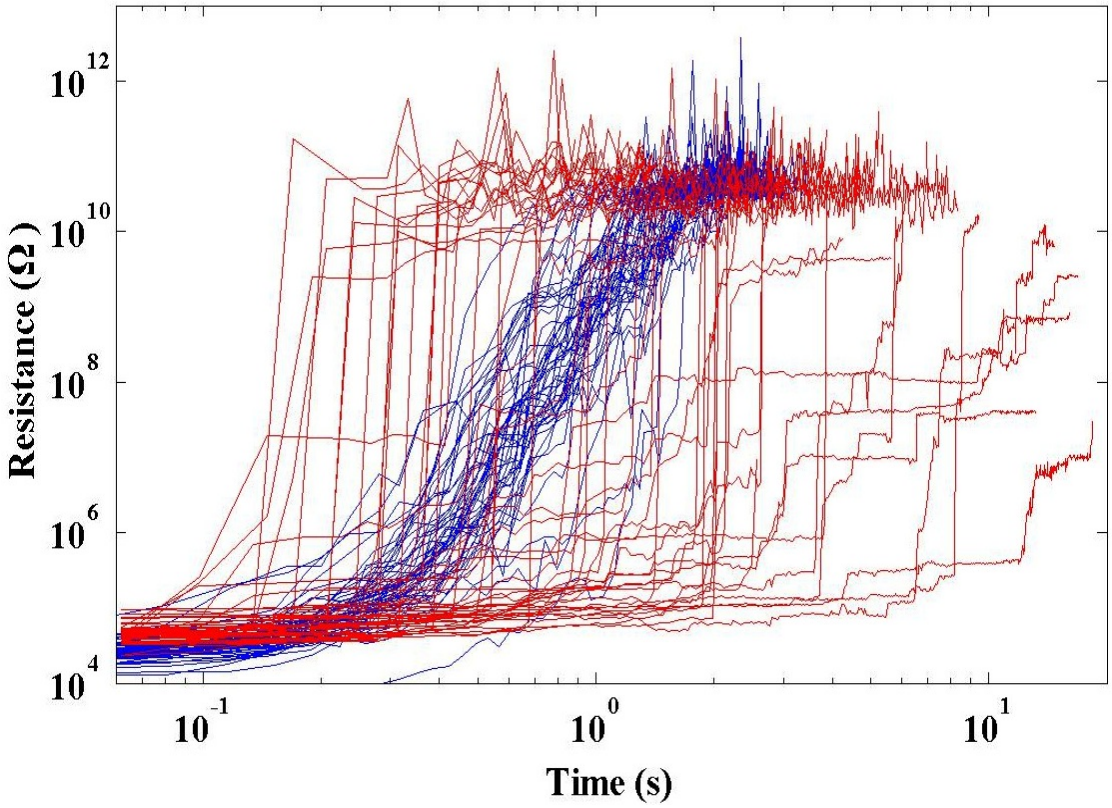

Figure 6.9: Variation of R_{ON} with time for one CBRAM cell programmed (to similar R_{ON}s) and stressed, for 50 trials with a constant stress voltage V_{STRESS} = -75 mV, programmed with CC (RED) and SC (BLUE) when similar programming energies were used

in t_E. It is important to note that the current limit is gradually increased during SC programming while it is maintained fairly constant during CC programming with the other parameters identical in both cases. It is a known fact that the erase process in a memory cells similar to PMC cells depends on the programmed CF as the erase initiates at the neck of the CF, at its intersection with the top electrode due to its difference in curvature compared to the top electrode [68] . If the grown CF is identical in every cycle, then its erase behavior in every cycle will also be similar and hence the variation in t_E will be minimal. Hence to achieve a better erase performance, programming operation must be optimized. From previous programming work [6], it was shown that the programming process in CBRAM cells has two stages, the formation and the growth of the CF. The idea behind SC programming is that by maintaining a low current during

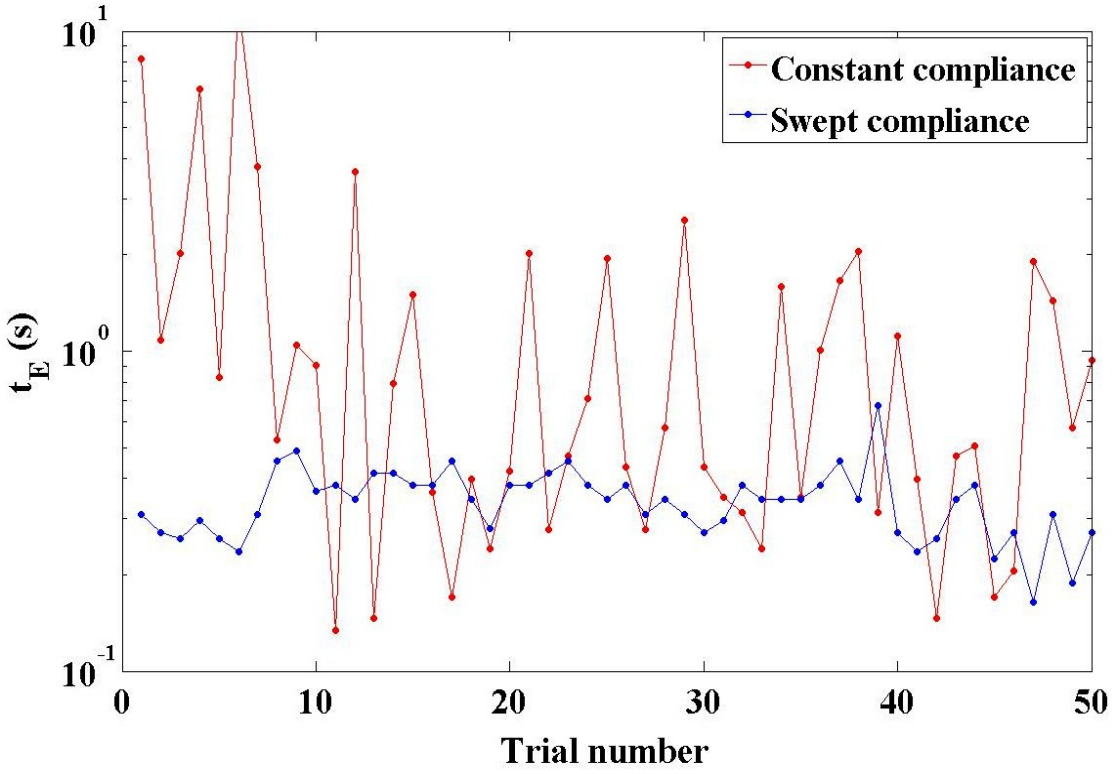

Figure 6.10: t_E of 50 states programmed with SC and CC when similar programming energies were used

the initial stage of the formation of the CF, the CF growth can be controlled better or that a low current programming (during the first stage) will create a conductive pathway in the solid electrolyte layer, that will ensure the growth of CF (approximately) in the same location in the electrolyte in every cycle, analogous to an some kind of 'electrical forming' of the electrolyte. In CC programming, since the current limit is held constant at a high value from the beginning of the programming operation, the growth of the CF is more abrupt and hence the location and the size of the grown CF in every cycle is prone to statistical variations, resulting in a higher variation in t_E. However the results discussed so far were experiments performed with DC voltages and on 1T1R CBRAM cells. Next section in this chapter discusses the pulse cycling (AC) results on a bigger population of CBRAM cells with the SC programming used for pre-conditioning cells to improve their Program-Erase (PE) cycling performance.

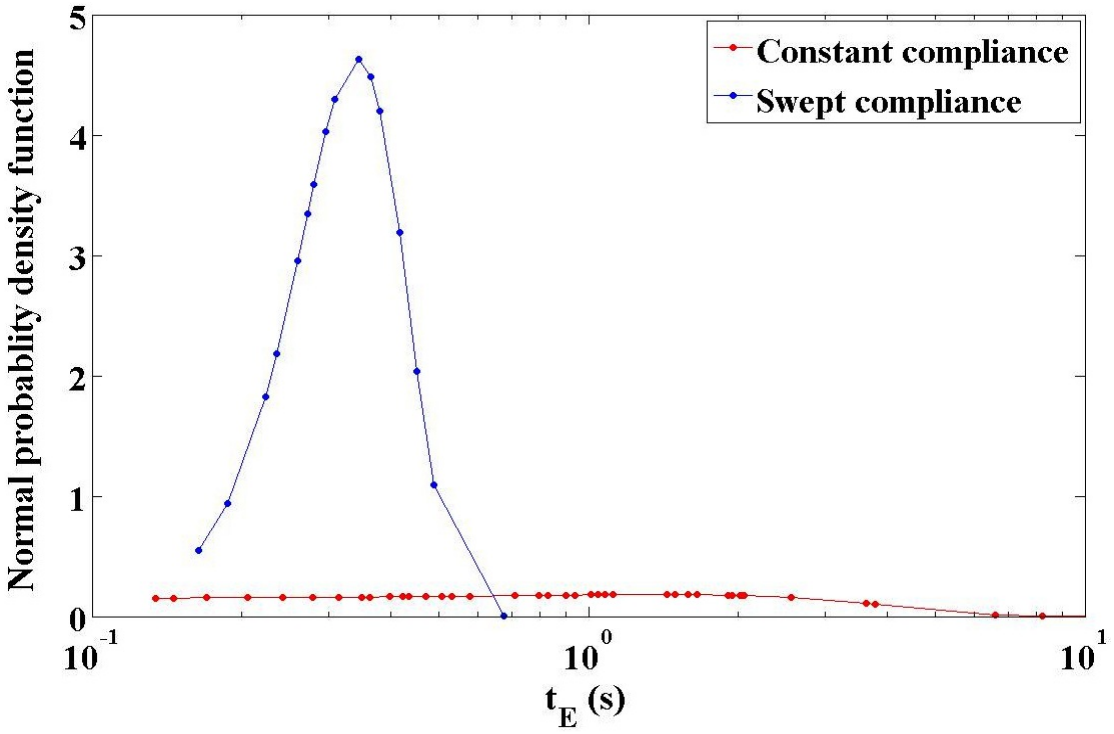

Figure 6.11: Variance of t_E of 50 states programmed with SC and CC when similar programming energies were used

6.4 Pre-conditioning

Pre-conditioning is a general concept in which an entity is exposed to a form of some stress or stimulus in order to prepare that entity to be more resilient against the stimulus when and if the stimulus is encountered in the future [82]. Pre-conditioning is a common practice in memory industry where a memory device is subjected to some kind of electrical or thermal treatment to ensure better performance when it is subjected to its actual use. It could be a thermal bake, a few strong PE cycles, a long voltage forming step, etc. In general pre-conditioning is aimed at improving the future cycling operation in a memory cell. For example in CBRAM, pre-conditioning is used to improve PE cycling yield, resistance distributions, etc. During the pre-conditioning operation, the memory cells are subjected to a few PE cycles (< 10) with more severe programming (and erase) conditions than what they might encounter during their cycling and this is expected to improve their cycling performance.

From the last section in this chapter it was found that maintaining a low current compliance (by sweeping V_{WL} instead of using a constant V_{WL}) improved the erase performance of similar resistance ON states. This section details the use of SC programming during the pre-conditioning process instead of the strong pre-conditioning traditionally used. However SC programming used DC conditions and 1T1R cells. Cells used in this section were constructed in bigger arrays and all the experiments detailed here had a sample size of 210 cells (referred as 210 bits) providing a bigger sample for a more careful statistical analysis. Fast voltage pulses were used for the results in this section instead of DC voltages. However due to the complexity of the cell architecture and some measurement setups involved, sweeping V_{WL} was difficult and hence instead of sweeping V_{WL} it was maintained constant but at a low voltage (lowest possible) to allow very minimal current flow during the pre-conditioning step.

Table. 6.1 summarizes briefly the pre-conditioning and cycling parameters used in this section. Table. 6.1(a) shows the conditions for High Current Pre-Conditioning (HCPC). Table. 6.1(c) is the Standard Compliance (Std-C) cycling condition used in this section. It is important to notice the difference in the programming current (I_{PROG} or $I_{COMP-PROG}$), voltage across the CBRAM cell (V_{SL}-V_{BL}) and the Pulse Width (PW) used during HCPC and Std-C. During HCPC, I_{PROG}, V_{CELL} and PW_{PROG} are much higher than the ones in Std-C. 210 CBRAM bits (sample size) were pre-conditioned using HCPC and then are cycled using Std-C (this sample is called the control sample) and their cycling performance was analyzed.

6.5 Low current pre-conditioning

Low Current Pre-Conditioning (LCPC) refers to a few PE cycles (< 10) used before cycling the memory cells to improve their cycling performance. Table. 6.1(b) shows the parameters used during LCPC and comparing it with Table. 6.1(a), it can be seen that I_{PROG} and V_{CELL} are much lower in LCPC than HCPC and this is to ensure that no significant programming occurs in the programming half-cycle of LCPC. Also the

(a) HCPC (Pre-condition)			
PROG		ERAS	
I_{COMP}	> 150 µA	I_{COMP}	NONE
PW	> 1 ms	PW	> 1 ms
V_{CELL}	> 2 V	V_{CELL}	< - 1.5 V

(b) LCPC (Pre-condition)			
PROG		ERAS	
I_{COMP}	< 6 µA	I_{COMP}	NONE
PW	> 100 ms	PW	> 1 ms
V_{CELL}	< 1 V	V_{CELL}	< - 1.5 V

(c) Std-C (Cycling)			
PROG		ERAS	
I_{COMP}	< 100 µA	I_{COMP}	NONE
PW	< 100 µs	PW	< 100 µs
V_{CELL}	< 2 V	V_{CELL}	> -2 V

Table 6.1: Various parameters used during pre-conditioning and cycling of CBRAM cells in this section

PW_{PROG} of LCPC is much greater than HCPC and this is to replicate the DC conditions that caused the 'electrical forming' effect that was found during SC programming in the previous section of this chapter. It is important to notice that the erase half-cycle of both LCPC and HCPC were similar. Hence another 210 CBRAM bits were pre-conditioned using LCPC and cycled with Std-C and their cycling performance was compared to the control sample. The rows highlighted in yellow in Table. 6.1 show the parameters that differ between LCPC and HCPC. From Table. 6.1(c) there are three important parameters during pre-conditioning and cycling; Maximum current allowed during the programming operation ($I_{COMP-PROG}$), cell voltage (V_{CELL}) and pulse width used during the programming operation (PW_{PROG}). To optimize the conditions in LCPC these three parameters, $I_{COMP-PROG}$, V_{CELL} and PW_{PROG} were varied and results were compared to the control sample.

Three types of plots/parameters were used to compare the performance of LCPC with HCPC; Cumulative Yield (CY), Per-cycle Yield (PY) and the resistance distribution (R_{ON} and R_{OFF}). PY refers to the number of bits passing in that cycle given either in % or in number of bits. CY refers to the number of bits that have passed till that

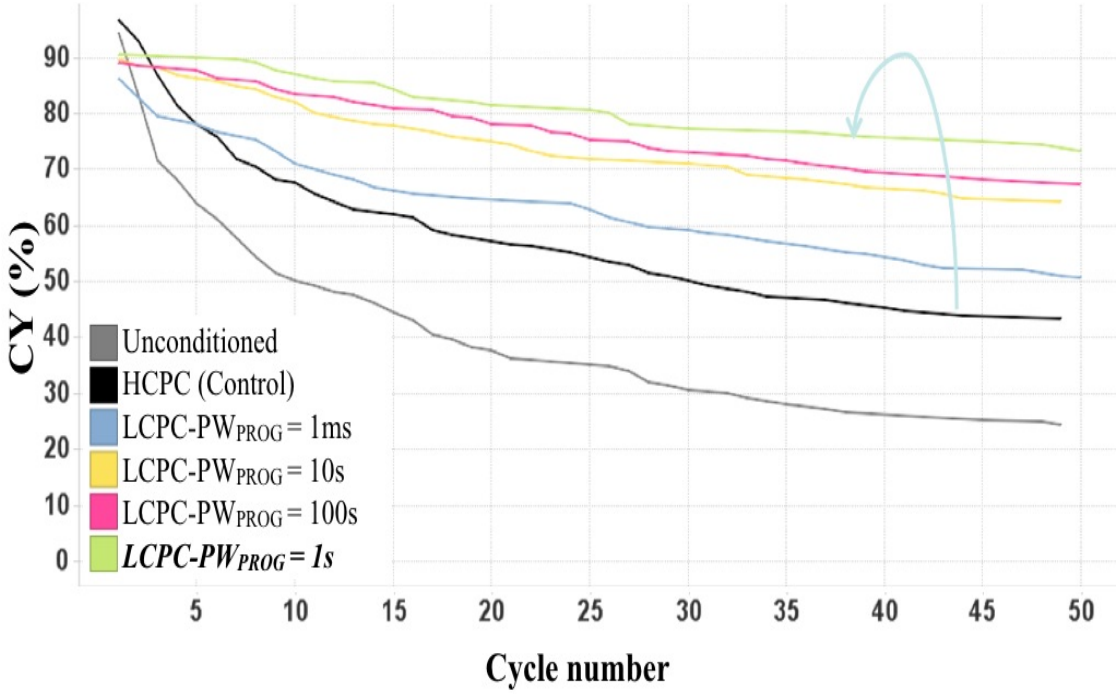

Figure 6.12: Variation of CY of the control sample and LCPC with four different LCPC-PW$_{PROG}$ with number of PE cycles, with $I_{PROG-COMP} < 6\ \mu$A and V_{CELL} = 0.9 V

cycle or it is the accumulation of the number of passed bits till that cycle. For example if the PY at cycle number 35 is 90 %, then 10 % of the bits failed in cycle 35. However if the CY at cycle 35 is 90 %, then 10 % of the bits have failed at least once in some cycle before 36.

$$LCPC\text{ - }PW_{PROG}$$

It was seen from the first section of this chapter that sweeping V_{WL} or the compliance current slowly during the programming operation improved the erase performance of the CBRAM cells. To replicate this effect on a bigger array of cells (instead of 1T1R), LCPC - PW$_{PROG}$ was varied between 1 ms to 100 s and the CY and PY were compared with the control sample. Fig. 6.12 shows the CY of the control sample (always shown in black) and LCPC with four different PW$_{PROG}$. For these experiments the other two LCPC factors were fixed at $I_{PROG-COMP} < 6\ \mu$A and V_{CELL} = 0.9 V. Also shown in the figure is another sample that was not pre-conditioned using HCPC or LCPC (un-

conditioned), but only cycled using Std-C. Most importantly, it can be seen from the figure that HCPC improved the performance of CBRAM cells, by improving the CY $\sim$ 20 % by the end of 50 PE cycles or CY for the sample pre-conditioned using HCPC was 20 % higher than the CY for the sample that was un-conditioned (shown in grey color), emphasizing the importance of pre-conditioning in CBRAM cells. However it can also be seen that the cycling performance of CBRAM cells pre-conditioned with LCPC (all four LCPC-PW$_{PROG}$) was much better than the ones pre-conditioned with HCPC, with the sample pre-conditioned with LCPC-PW$_{PROG}$ = 1 s yielding the best CY improvement at the end of 50 PE cycles, of $\sim$ 30 % when compared to the control sample (this improvement is shown with the blue colored arrow in the figure). The sample pre-conditioned with LCPC that yielded the most improvement in CY at the end of 50 PE cycles (compared to the control sample) is shown in 'bold' in the legend of the figures.

Fig. 6.13 shows the variation of PY of the control sample and LCPC with four different LCPC-PW$_{PROG}$ with number of PE cycles. The y-axis of the figure shows the number of bits that passed programming and erase in that cycle (out of the 210 bits used), hence if 210 bits passed in a cycle, the PY of that cycle is 100 %. Again the improvement in cycling performance for cells pre-conditioned with all LCPC-PW$_{PROG}$ is clearly seen from the figure, with LCPC-PW$_{PROG}$ = 1 s, yielding the best PY ($>$ 99 %) through out the cycling period. Hence LCPC helped improving the cycling performance of CBRAM cells, similar to SC (noticed previously), and it was found that a LCPC-PW$_{PROG}$ = 1 s yielded the best performance.

LCPC-V_{CELL}

With the programming pulse width during LCPC optimized in the previous section, the next parameter that was varied was the cell voltage or V$_{CELL}$ which is essentially the voltage across the series combination of the CBRAM cell and the access transistor (Fig. 6.1). Fig. 6.14 shows the CY of the control sample and LCPC with four differ-

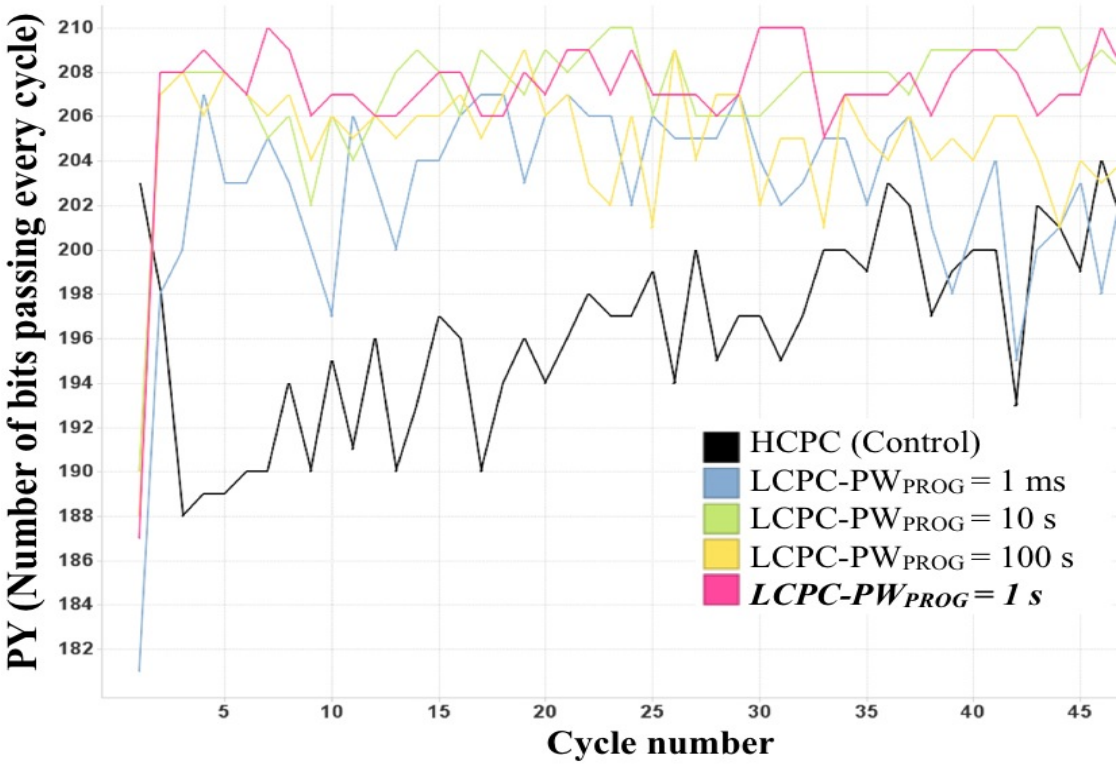

Figure 6.13: Variation of PY of the control sample and LCPC with four different LCPC-PW_{PROG} with number of PE cycles

ent LCPC-V_{CELL}, with $I_{PROG-COMP} < 6\ \mu A$ and PW_{PROG} = 1 s (best condition from Fig. 6.12 and Fig. 6.13). It is clear from the figure that there is a definite improvement in the cycling performance of CBRAM cells pre-conditioned with all LCPC-V_{CELL}, except for the highest value of V_{CELL} = 1.3 V (discussed later). Also again the best yield is from the sample pre-conditioned with LCPC-V_{CELL} = 0.9 V.

Fig. 6.15 shows the variation of PY of the control sample and LCPC with four different LCPC-V_{CELL} with number of PE cycles. The y-axis of the figure shows the number of bits that passed programming and erase in that cycle (out of the 210 bits used). Again the improvement in cycling performance for cells pre-conditioned with all LCPC-V_{CELL} is clearly seen from the figure, with LCPC-V_{CELL} = 0.9 V, yielding the best PY ($\sim$ 100 %) through out the cycling period.

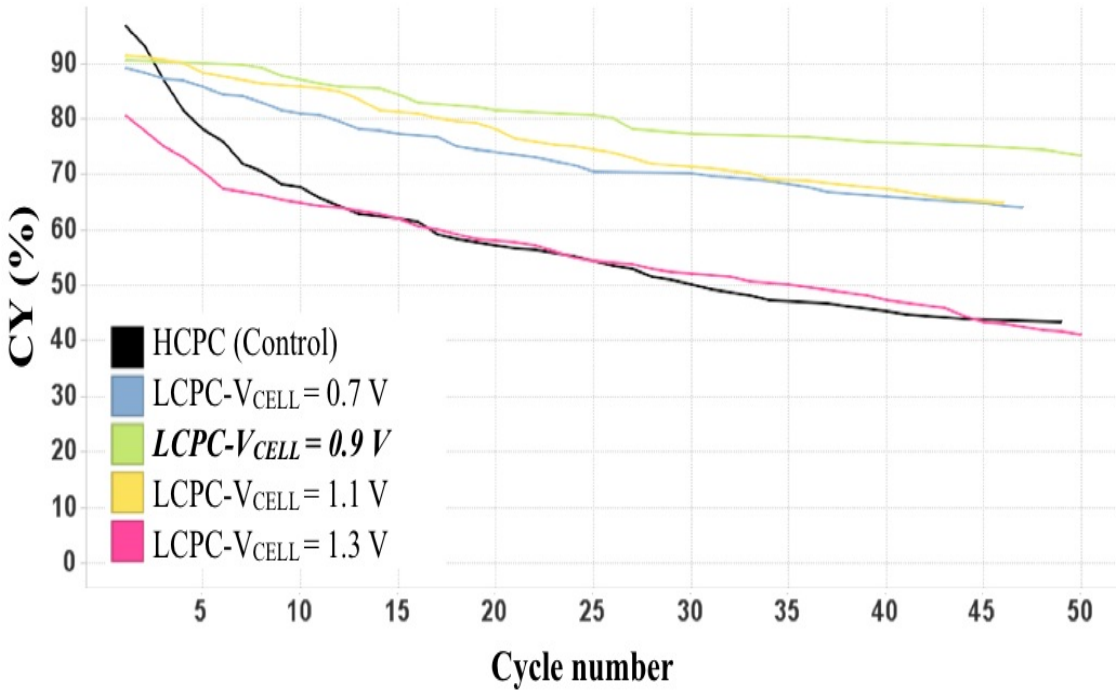

Figure 6.14: Variation of CY of the control sample and LCPC with four different LCPC-V_{CELL} with number of PE cycles, with $I_{PROG-COMP} < 6$ μA and PW_{PROG} = 1 s (best condition from Fig. 6.12 and Fig. 6.13)

LCPC-I_{PROG}

The last of the three parameters in LCPC that was optimized was $I_{COMP-PROG}$ and for these experiments the other two parameters were set at their optimized values from Fig. 6.12 and Fig. 6.14 at PW_{PROG} = 1 s and V_{CELL} = 0.9 V. LCPC-$I_{COMP-PROG}$ was varied from 6 μA to 24 μA and the results were compared with the control sample. Fig. 6.16 shows the CY and Fig. 6.17 shows the PY of the control sample and LCPC with three different LCPC-$I_{COMP-PROG}$.

Results in Fig. 6.16 differ from previous results in Fig. 6.12 and Fig. 6.14 where irrespective of the parameter values, LCPC improved the CY and the PY over the control sample. It can be seen from Fig. 6.16, that except for LCPC-$I_{COMP-PROG} < 6$ μA, the cycling performance of the samples pre-conditioned with the other two LCPC-$I_{COMP-PROG}$ was worse than the control sample. However the improvement in CY in the sample pre-conditioned with LCPC-$I_{COMP-PROG} < 6$ μA over the control sample

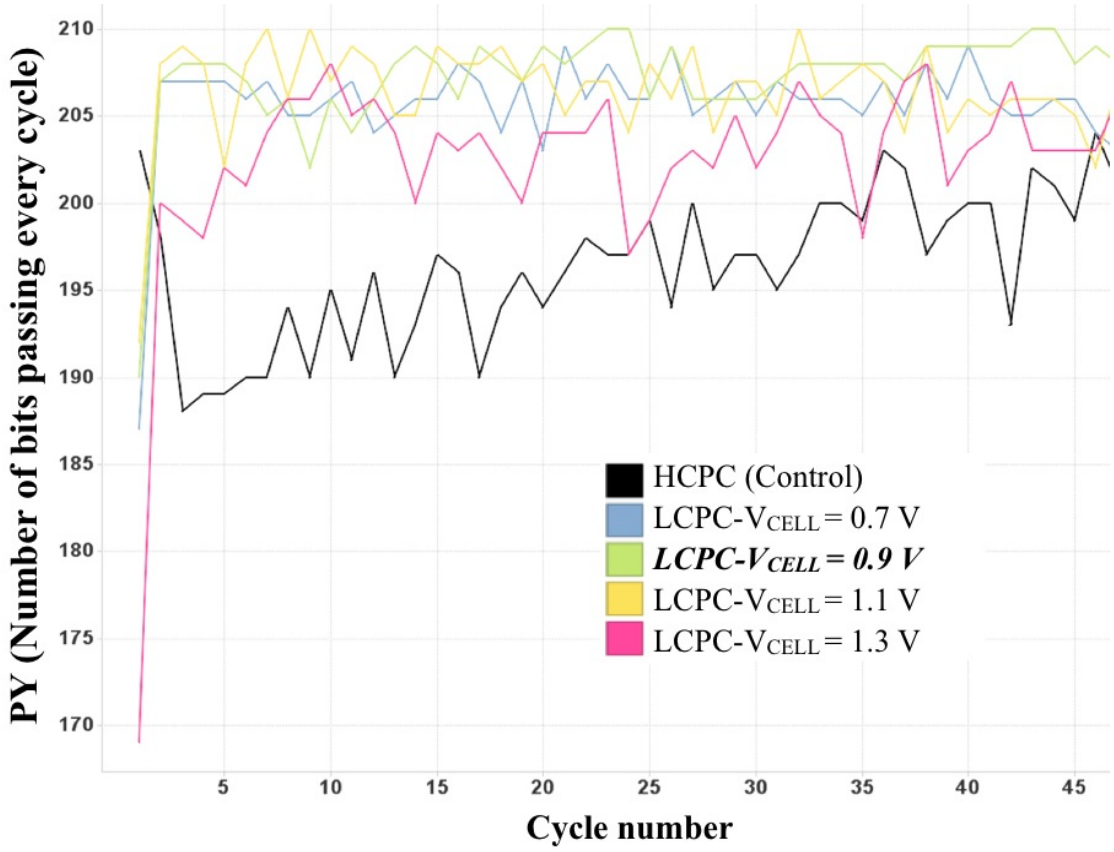

Figure 6.15: Variation of PY of the control sample and LCPC with four different LCPC-V_{CELL} with number of PE cycles, with $I_{PROG-COMP} < 6\ \mu$A and PW_{PROG} = 1 s (best condition from Fig. 6.12 and Fig. 6.13)

was significant, $\sim$ 30 % by the end of 50 PE cycles. Also Fig. 6.17 suggests that PY improvement was seen only in the sample pre-conditioned LCPC-$I_{COMP-PROG} < 6\ \mu$A.

To summarize the observations from Fig. 6.12 - Fig. 6.17, CBRAM cells pre-conditioned with LCPC showed significant improvement in cycling performance (CY and PY) over those pre-conditioned with HCPC (control sample). PW_{PROG} = 1 s, V_{CELL} = 0.9 V and $I_{COMP-PROG} < 6\ \mu$A were found out to be the best LCPC parameters for maximum improvement in cycling performance over the control sample. Fig. 6.14 and Fig. 6.16 suggested that this improvement due to LCPC ceased to exist when V_{CELL} or $I_{COMP-PROG}$ was too high.

6.6 Discussion on LCPC

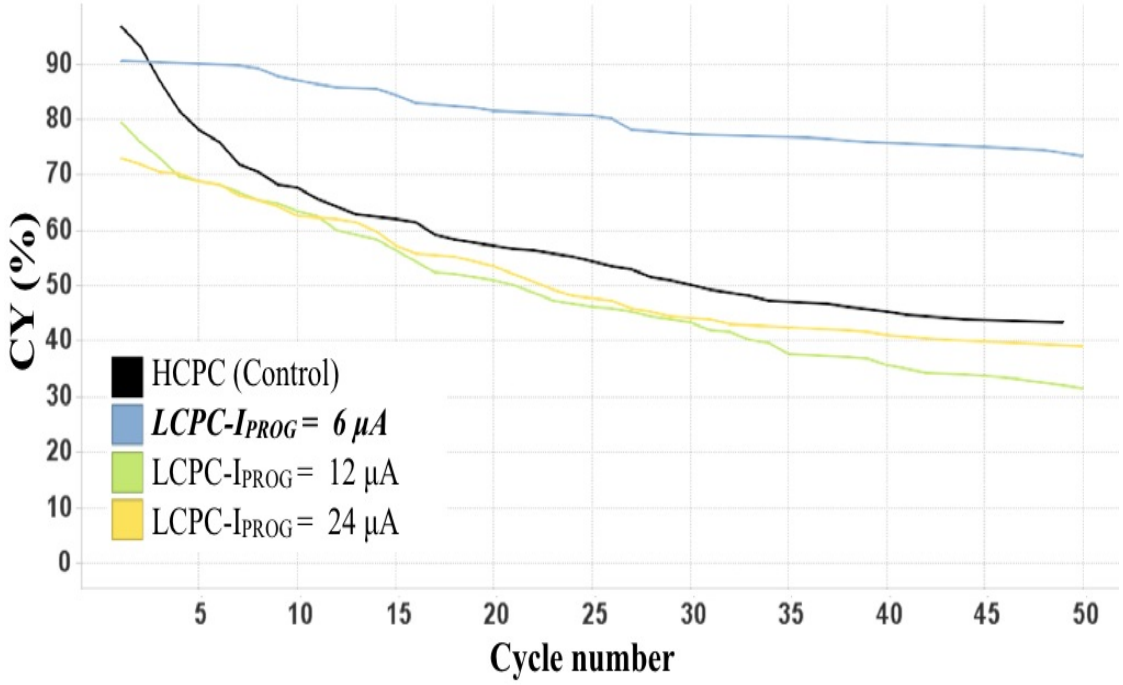

Figure 6.16: Variation of CY of the control sample and LCPC with four different LCPC-$I_{COMP-PROG}$ with number of PE cycles, with V_{CELL} = 0.9 V and PW_{PROG} = 1 s (best condition from Fig. 6.12 and Fig. 6.14)

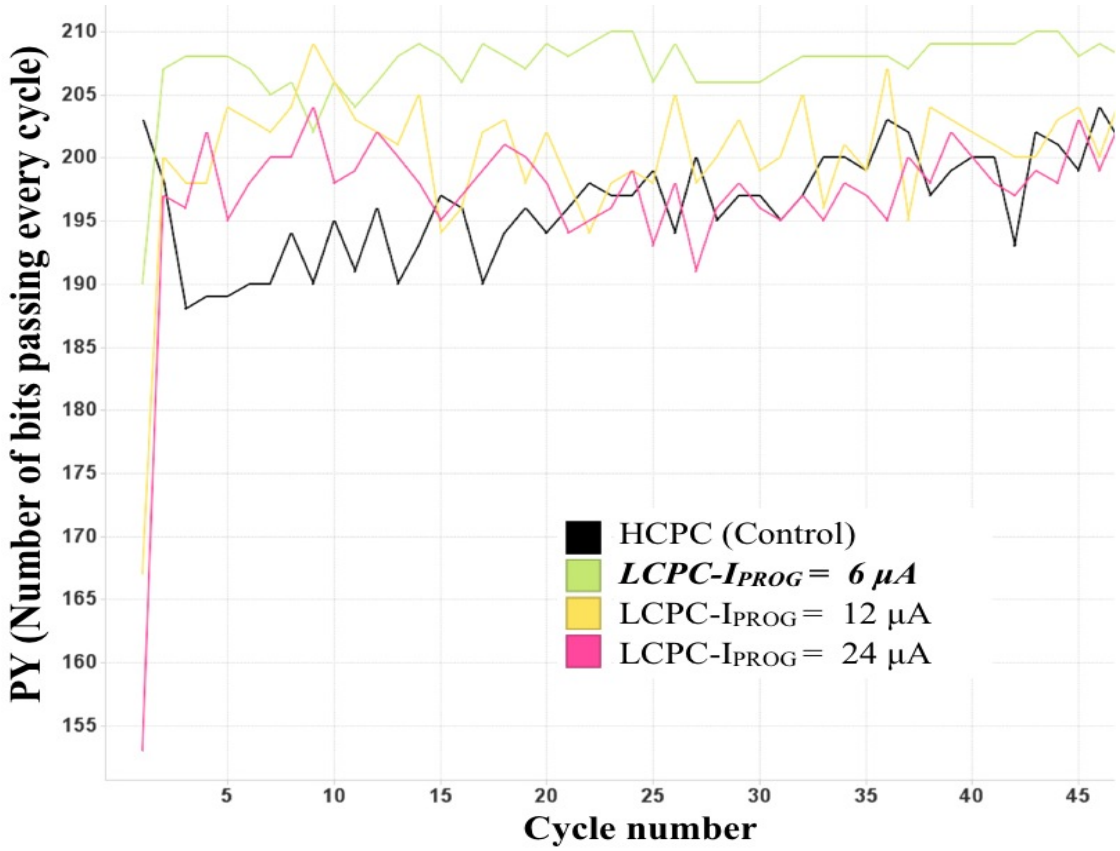

Figure 6.17: Variation of PY of the control sample and LCPC with four different LCPC-$I_{COMP-PROG}$ with number of PE cycles, with V_{CELL} = 0.9 V and PW_{PROG} = 1 s (best condition from Fig. 6.12 and Fig. 6.14)

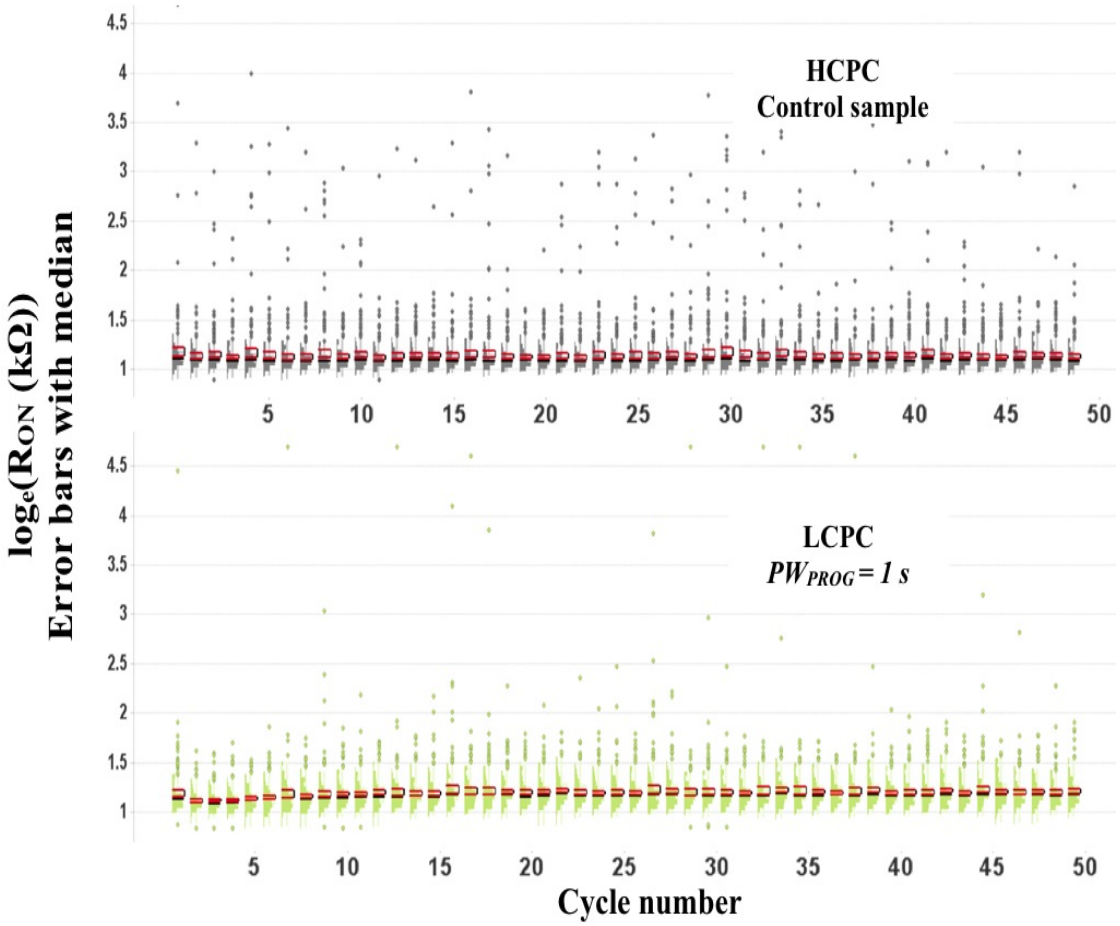

Figure 6.18: Variation of the median-R_{ON} with the error bars (median shown as black lines and the error bars shown as washed out grey and green solid bars) of the two samples (pre-conditioned with HCPC and LCPC) over the number of PE cycles

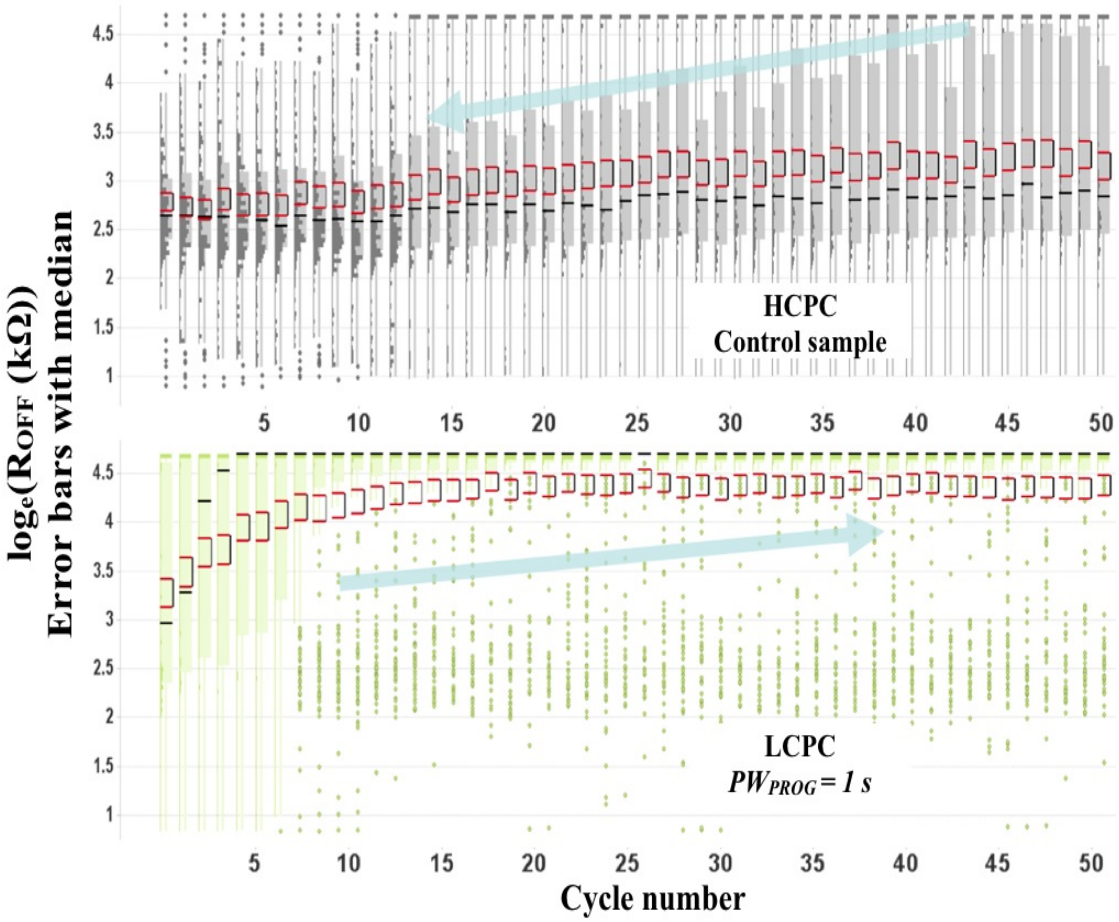

Figure 6.19: Variation of the median-R_{OFF} with the error bars (median shown as black lines and the error bars shown as washed out grey and green solid bars) of the two samples (pre-conditioned with HCPC and LCPC) over the number of PE cycles

From the results in the previous section, it was found that LCPC indeed improved the cycling performance of CBRAM cells as expected based on the results of swept compliance programming in this first section of this chapter. This improvement was not subtle, but $\sim$ 30 % in all the best cases. This further suggest that a few cycles (< 10) of low current pre-conditioning helped improve subsequent cycling performance of CBRAM cells up to 50 PE cycles (maximum PE cycles used in this work). Similar to the theory suggested previously for the swept compliance programming, the cells appeared to have undergone some kind of 'electrical forming' process due to LCPC that improved their program and/or erase behavior during their subsequent cycling.

To analyze this theory further, the resistance distribution (over number of PE cycles) of the cells pre-conditioned with HCPC (control) and LCPC (best condition: PW_{PROG} = 1 s, V_{CELL} = 0.9 V and $I_{COMP-PROG} < 6\ \mu$A) was compared. Fig. 6.18 and Fig. 6.19 show the variation of median-R_{ON} and median-R_{OFF}, respectively with the error bars (median shown as black lines and the error bars shown as washed out grey and green solid bars) of the two samples with the number of PE cycles. From Fig. 6.18 it can be seen that there was no noticeable difference in R_{ON} distribution between the two samples pre-conditioned with HCPC and LCPC. However the R_{OFF} distribution was significantly different for the sample pre-conditioned with LCPC compared to the sample pre-conditioned with HCPC as seen in Fig. 6.19. The median-R_{OFF} for the sample pre-conditioned with LCPC increased to $>$ 10 MΩ in a few PE cycles ($\sim$ 5) and the distribution became tighter with increasing number of PE cycles. In contrast, the median-R_{OFF} for the sample pre-conditioned with HCPC remained close $<$ 1 MΩ, but the distribution widened with increasing PE cycles, suggesting that the variation in the erase performance of the cells in the sample pre-conditioned with HCPC increased significantly with cycling. Hence LCPC improved the erase performance of CBRAM cells during PE cycling, similar to what was observed with swept compliance programming in Fig. 6.3 and Fig. 6.5.

6.7 Summary of Swept compliance programming and pre-conditioning of PMC cells

The variation found in the behavior of similar resistance ON states in PMC or CBRAM cells was analyzed more in detail and measures to reduce this variation were looked into. It was found that sweeping the compliance current (instead of maintaining it at a constant high value) during the programming operation ensured similar behavior of CBRAM ON states under stress/erase. However to control the programming current during the programming operation, cells with an access transistor (Fig. 6.1) or 1T1R cells were used. Initial tests on 1T1R cells showed marked improvement in terms of reduced variation in erase times (t_E) of similar resistance CBRAM ON states that were programmed with swept compliance current programming.

To further investigate this effect, a larger cell population (210 bits per sample) or cells constructed in arrays were used. However due to some restrictions in the cell architecture and the available measurement setups, the programming current could not be swept and was chosen to be maintained at the minimum possible value. Also this setup was used to pre-condition (not to cycle) the CBRAM cells to investigate their subsequent cycling performance and this pre-conditioning scheme was termed as Low Current Pre-Conditioning (LCPC). CBRAM cells pre-conditioned with LCPC showed marked improvements in their cumulative yield and per-cycle yield for up to 50 PE cycles when compared to the cells that were pre-conditioned with the (traditional) High Current Pre-Conditioning (HCPC). Various LCPC parameters like PW_{PROG}, V_{CELL} and $I_{COMP-PROG}$ were optimized to yield the best improvements in cycling performance over the control sample. Analyzing and comparing the resistance distribution of samples pre-conditioned with HCPC and LCPC, it was found that LCPC improved the erase performance during cycling of CBRAM cells, while not affecting their programming performance during cycling. This was in agreement with the improvements seen previously in the erase behavior of the cells programmed with swept compliance currents.

Chapter 7

CONCLUSIONS

Reliability is one the most significant properties of any non-volatile memory technology and the purpose of this work was to analyze the reliability of different low resistance states in PMC devices both under normal operating conditions and under extreme stress. The stability of low resistance states under no stress and the effect of temperature on these states were discussed. The kinetics of the erase process in PMC cells was analyzed and modeled. The feasibility of using PMC cells reliably as memory elements or PE cycling was investigated.

The low resistance states of PMC devices were found to be very stable at room temperature but with a gradual increase in resistance with time. The role of temperature in accelerating the gradual increase in the low resistance state was not clearly evident and its effect in isolation was hard to establish as a result of the gradual pace of the mechanism.

Accelerated failure tests with current and voltage stress of different magnitudes were conducted. Under negative current/voltage stress the low resistance ON state was lost after some time and the mean times to failure were exponentially related to the applied field, suggesting that the failure mechanism under stress was caused by ion migration under the influence of electric field. Failure times (for 10x decrease) in this case were again exponentially dependent on the applied stress, indicating ion migration to be the most significant effect causing failure. It was also found that the transition from different ON states to a 10x increase did not result in a permanent failure or in other words it was not a hard failure. All the cells could be programmed again after a stress test without any loss of functionality. This indicated that this transition under different electrical stressing conditions was similar to a typical erase process in a PMC device operation. The erase process in PMC devices was studied to address the ON state stability and the erase operation in pulse mode. The dependence of erase time on

voltage and on the ON state resistance was characterized and modeled on the basis of by CF oxidation and Ag ion migration.

It was also demonstrated that it is possible to utilize symmetric program-erase cycling for PMC devices at voltages that are commensurate with the nanoscale geometry devices at the end of the current version of the International Technology Roadmap for Semiconductors (<0.6 V). Single pulse erasing of devices programmed to a low R_{ON} revealed that the average R_{OFF}/R_{ON} ratio decreased with decreasing erase voltage, from a maximum of 520 at V_E = - 2 V to around 33 at - 0.6 V. This indicated that a low cycling voltage was probably less effective at removing the electrodeposited Ag which had been added during the programming cycle but that the R_{OFF}/R_{ON} ratios are still sufficiently large (> 10) to permit simple sensing schemes to be employed. The maximum current limit during cycling set by series resistance R_L defines the ON state resistance of the device and the symmetric low voltage erase conditions result in an OFF state resistance that is a few multiples of ten ($\sim$ 10x - 50x) higher than the ON state resistance for a wide range of program/erase currents (0.27 to 220 μA). The distributions of R_{ON} and R_{OFF} are narrowest for the lowest R_L, leading to the widest margin between the highest ON and lowest OFF (tail) states, however, the margin between these states clearly decreases with increasing R_L even though the average R_{OFF}/R_{ON} ratio generally increases with increasing R_L. Indeed, there is little or no overlap between the R_{ON} and R_{OFF} distributions for R_L = 1 kΩ to 100 kΩ, which would allow low voltage and low current cycling to be employed with adequate differentiation between the stored states, but significant tail state overlap occurs in the case of R_L = 500 kΩ. The wide resistance distributions in both the ON and OFF states at lower programming currents could be due to less well defined or fragmented residual filaments following program and erase operations respectively.

The variation found in the behavior of similar resistance ON states in PMC or CBRAM cells was analyzed more in detail and measures to reduce this variation were

looked into. It was found that sweeping the compliance current (instead of maintaining it at a constant high value) during the programming operation ensured similar behavior of CBRAM ON states under stress/erase. However to control the programming current during the programming operation, cells with an access transistor (Fig. 6.1) or 1T1R cells were used. Initial tests on 1T1R cells showed marked improvement in terms of reduced variation in erase times (t_E) of similar resistance CBRAM ON states that were programmed with swept compliance current programming.

To further investigate this effect, a larger cell population (210 bits per sample) or cells constructed in arrays were used. However due to some restrictions in the cell architecture and the available measurement setups, the programming current could not be swept and was chosen to be maintained at the minimum possible value. Also this setup was used to pre-condition (not to cycle) the CBRAM cells to investigate their subsequent cycling performance and this pre-conditioning scheme was termed as Low Current Pre-Conditioning (LCPC). CBRAM cells pre-conditioned with LCPC showed marked improvements in their cumulative yield and per-cycle yield for up to 50 PE cycles when compared to the cells that were pre-conditioned with the (traditional) High Current Pre-Conditioning (HCPC). Various LCPC parameters like PW_{PROG}, V_{CELL} and $I_{COMP-PROG}$ were optimized to yield the best improvements in cycling performance over the control sample. Analyzing and comparing the resistance distribution of samples pre-conditioned with HCPC and LCPC, it was found that LCPC improved the erase performance during cycling of CBRAM cells, while not affecting their programming performance during cycling. This was in agreement with the improvements seen previously in the erase behavior of the cells programmed with swept compliance currents.

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