Design of a Continuous Time Sigma Delta Analog-to-Digital Converter for Operation in Extreme Environments

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved February 2011 by the
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May 2011

ABSTRACT

In this work, a high resolution analog-to-digital converter (ADC) for use in harsh environments is presented. The ADC is implemented in bulk CMOS technology and is intended for space exploration, mining and automotive applications with a range of temperature variation in excess of 250°C. A continuous time (CT) sigma delta (ΣΔ) modulator employing a cascade of integrators with feed forward (CIFF) architecture in a single feedback loop topology is used for implementing the ADC.

In order to enable operation in the intended application environments, an RC time constant tuning engine is proposed. The tuning engine is used to maintain linearity of a 10 ksps 20 bit continuous time sigma delta ADC designed for spectroscopy applications in space. The proposed circuit which is based on master slave architecture automatically selects on chip resistors to control RC time constants to an accuracy range of ±5% to ±1%. The tuning range, tuning accuracy and circuit non-idealities are analyzed theoretically. To verify the concept, an experimental chip was fabricated in JAZZ .18µm 1.8V CMOS technology. The tuning engine which occupies an area of .065mm^2 consists of only an integrator, a comparator and a shift register. It can achieve a signal to noise and distortion ratio (SNDR) greater than 120dB over a ±40% tuning range.

ACKNOWLEDGMENTS

I am deeply indebted to Dr. Hugh Barnaby and Dr. Bert Vermeire, for their continuous guidance and constant support which made this work possible. Beyond offering me a research assistantship, I always found Dr. Vermeire willing to assist and guide me technically and professionally with his typical pleasant and helpful nature. I sincerely thank Dr. Barnaby for his invaluable guidance and boundless technical suggestions during the course of this project. It was also a tremendous pleasure to be his teaching assistant.

I would also like to thank Dr. Junseok Chae and Dr. Gennady Gildenblat for serving on my committee and for their thoughtful comments on the manuscript.

I would like to thank the staff at Connection One research center and particularly Mr. James Laux for being there, for the students, all the time. His tremendous help with Cadence is gratefully acknowledged. I spent a great time with my fellow graduate students at ASU, to avoid missing any name, I would like to say thank you all.

Finally, I would like to thank my family for their endless patience and unwavering support.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Many applications currently exist that require analog and mixed signal circuits to operate at temperatures well beyond commercial (0 °C to 70 °C), industrial (−40 °C to 85 °C) and even military (−55 °C to 125 °C) specifications. In oil and gas mining applications for example, numerous down hole measurements gathered by permanently installed sensors, form important parameters for seismic prognosis and well management. However, with the harsh conditions present down hole, electronic systems must cope with high temperatures (175 °C to 225 °C), pressures, vibration, shock, etc. Additionally, electronic circuits must have long life reliability and stability since replacement or maintenance is either impossible or extremely expensive.

Space-bound and automotive control microelectronics can also involve operation at temperatures in excess of 200 °C [8]. Automotive applications particularly represent a large market for high temperature electronics with potential benefits such as improved fuel economy, safety, and exhaust emissions control.

On the low end of the temperature spectrum, applications such as X-ray and far-IR imaging and spectroscopy for space exploration and particle experiments require operation at cryogenic temperature typically below 100K [10]. Major applications for extreme temperature circuits are summarized in Table 1.

Table 1: Key application areas with extreme temperature operation requirements.

Application		Temperature Range
Automotive industry	Compartment	-40°C to 85°C
	Engine/gear box	-40°C to 165°C
	Brakes	-40°C to 250°C
Avionics	Aircraft Surface	-40°C to 80°C
	Engine intake	-40°C to 185°C
	Jet Engine	-40°C to 320°C
Satellites		-150°C to 200°C
Space exploration		-150°C to 450°C
Oil exploration		-40°C to 175°C
Geothermal exploration		-40°C to 320°C

Due to noise and interference considerations, interface electronics must be located in close proximity to the sensors; therefore, ADCs capable of operation at extreme temperature would improve signal integrity substantially. Traditional approaches for preserving electronics in harsh environments usually include shielding, insulation and redundancy, at the expense of cost, power and weight. Therefore, design solutions that can offer an alternative to these approaches are desirable.

Despite the number of applications, few ADCs for extreme temperatures currently exist. For cryogenic temperatures, the only available ADCs are

superconductive circuits (Josephson junctions) [11], whose working temperature is limited to a maximum temperature of 10K. Therefore, testing of the sensor system at warmer temperatures is impossible. A cryogenic ADC, operating from room temperature (at the start of the cooling process) down to below 10K would overcome this problem. As to ADCs for extremely high temperatures only one is commercially available [9]. This converter provides 12 bits of resolution at 225 °C and uses a nonstandard silicon-on-insulator (SOI) CMOS process.

At high temperature, Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) in conventional bulk CMOS have several drawbacks, that include increased junction leakage, unstable threshold voltages, and reduced mobility [6], [7]. Among these drawbacks, excess leakage current at high temperature is the most critical, and can reduce circuit performance due to loss of bias current or cause the loss of charge stored across a capacitor, or result in higher susceptibility to latch-up [7]. Despite these issues, an instrumentation amplifier in bulk CMOS has been demonstrated at temperatures as high as 300 °C [4], and a switched capacitor (SC) 14-bit sigma-delta modulator has been shown to be functional at 255 °C [5].

Silicon on insulator (SOI) technology offers a significantly reduced leakage current by eliminating the reverse-biased diodes between source/drain region and substrate/well, and can achieve higher switching speeds due to the reduced gate capacitance. SOI CMOS analog circuits, reported in [1], [2], [3], have demonstrated that the elimination of junction leakage can enable the operation of a variety of analog circuits at temperatures near 300 °C or above. The

downside of SOI is that it is much more expensive compared to bulk CMOS technology.

At low temperatures on the other hand, performance of CMOS circuits is enhanced due to lower leakage current, improved mobility and decreased thermal noise. However, at temperatures below 10K several low-temperature-induced abnormalities occur as shown in Figure 1.

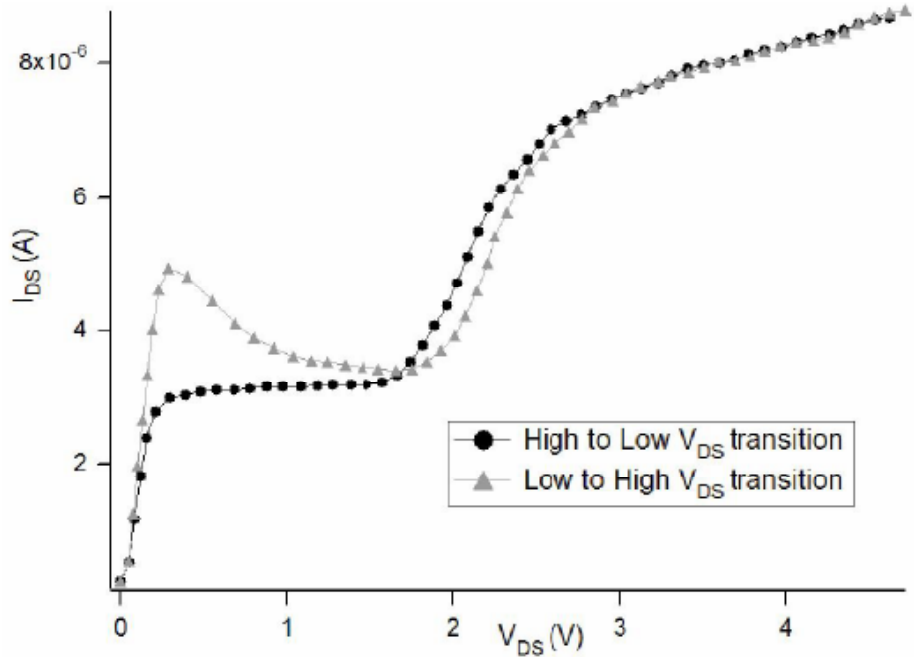


Figure 1: IV behaviour of a standard 0.7µm NMOS at 4.2K[11].

Obvious irregularities in the IV characteristic are the negative transconductance region located at the transition linear-saturation with clockwise hysteresis, the associated current overshoot in the time domain, and the kink at VDS mid-supply with counterclockwise hysteresis. These phenomena can deteriorate performance at 10K (-264 °C) and below. Key factors to cryogenic CMOS design are proper biasing and switching schemes.

This work addresses the design of a high resolution A/D converter able to operate across a range of temperature extending from -200 °C to above 225 °C in a standard CMOS process. Design specifications are summarized in Table 2

Table 2: ADC design specifications

Parameter	Value	Unit
SNR	≥122	dB
SNDR	≥120	dB
BW	0 - 10	ksps
Temperature range	-200 - 250	ºC
Input Signal Range	-1.5 – 1.5	V

1.2 MOSFET Operation in Extreme Temperatures

The operational characteristics of CMOS devices in extreme temperatures can be described by examining the effect of temperature on the key device parameters such as mobility, threshold voltage, noise and subthreshold slope. The drain current of a MOSFET in saturation is given by (1)

$$I_D = \frac{\mu}{2} C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \tag{1}$$

Where μ is the mobility of charge carriers, C_{OX} is the oxide capacitance, V_{GS} and V_{DS} are the voltages from the gate and the drain to the source, μ is the channel length modulation parameter, and V_{TH} is the threshold voltage. High-temperature operation of a standard CMOS transistor introduces several impairments. These include decreased carrier mobility, decreased threshold voltage and an exponentially increasing junction-to-substrate (reverse-biased diode) leakage current [12], [13], [14].

1.2.1 Mobility

Carrier mobility in silicon is influenced by two major scattering mechanisms: lattice scattering and impurity scattering. In lattice scattering, a carrier traveling through the crystal is scattered by the vibration of the lattice. As temperature increases, the mobility from the lattice scattering decreases with a temperature dependence of $T^{3/2}$ [16]. On the other hand, impurity scattering is scattering from crystal defects such as ionized impurities, and it has temperature dependence of $T^{3/2}$ [16]. Impurity scattering becomes less significant at higher temperature because the carriers are moving faster and exposed to impurities for a shorter time. Carrier mobility at 250 °C is less than one half the mobility at 25 °C [15]. A plot of measured mobility versus temperature is shown in Figure 2.

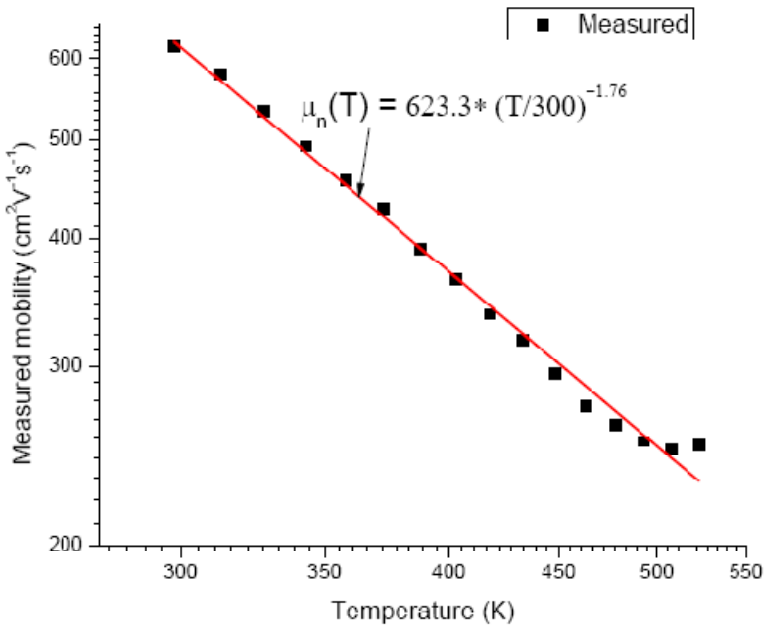


Figure 2: Measured mobility vs. temperature for a 50µm x 50µm NMOS in .35 µm technology [15].

The most significant advantage of low-temperature MOSFET operation is increased mobility. The increase of mobility and saturation velocity contributes to an increased current driving capability. Temperature dependency of the mobility can be modeled with

$$\mu = \mu_o \left(\frac{T}{T_o} \right)^{-\alpha} \tag{2}$$

Where μ_o is the mobility at the nominal operating temperature, T_o is the nominal operating temperature, and α is a constant that describes the temperature dependence. At 77 K, mobility increases by a factor of 4 to 6 [17].

1.2.2 Threshold Voltage

The zero bias threshold voltage is given by

$$V_{To} = V_{FB} + 2|\phi_F| + \frac{\sqrt{2q\varepsilon_{si} N_{SUB} 2|\phi_F|}}{C_{OX}} \tag{3}$$

Where V_{FB} is the flat band voltage, Φ_f is the strong inversion surface potential, ε_{si} is the dielectric constant of silicon, C_{OX} is the oxide capacitance per unit area, q is the electronic charge. N_{SUB} is the substrate doping concentration. The threshold voltage is given by

$$V_T = V_{To} + \gamma \left[\sqrt{2|\phi_F| + v_{sb}} - \sqrt{2|\phi_F|} \right] \tag{4}$$

Where γ is the body effect parameter and v_{sb} is the source bulk voltage. The flat band voltage is given by

$$V_{FB} = \frac{KT}{q}\left(\ln \frac{n_i}{N_{SUB}} - \ln \frac{N_{GATE}}{n_i} \right) - \frac{qN_{ss}}{C_{OX}} \tag{5}$$

Where N_{SS} is the effect of surface charge, n_i is the intrinsic carrier concentration and N_{GATE} is the gate doping concentration. The strong inversion surface potential is

$$\phi_F = \frac{KT}{q} \ln \left[\frac{N_{SUB}}{n_i} \right] \tag{6}$$

N_{SUB} has no dependent of temperature, whereas n_i decreases at lowered temperatures as follows

$$\frac{n_i(T_i)}{n_i(295K)} = \left[\frac{T_i}{295K} \right]^{1.5} e^{\left\{ -\left(\frac{qE_g}{2k} \right) \left[\frac{1}{T_i} - \frac{1}{295K} \right] \right\}} \tag{7}$$

Where E_g is the energy gap. Therefore, as the temperature is lowered, the magnitude of Φ_f and V_{Th} increases. V_{Th} can be optimized by adjusting either the doping concentration or the forward-bias voltage v_{sb}. The resulting forward current is negligible at 77 K because of the decrease in the n_i [18], [19].

Temperature dependence of the threshold voltage for an NMOS device can be given by [12]

$$\frac{\partial V_T}{\partial T} = \frac{\phi_{ms}}{T} + \frac{2\phi_F}{T} + \frac{\gamma_n}{\sqrt{2\phi_F}} \frac{\partial \phi_F}{\partial T} \tag{8}$$

At 300 K, the first term in (8) is -3.10 mV/ °C, the second is 2.70 mV/ °C and the last term is approximately -0.4 mV/ °C [13]. For a PMOS device, threshold voltage temperature dependence is given by

$$\frac{\partial V_T}{\partial T} = \frac{\phi_{ms}}{T} - \frac{2\phi_F}{T} - \frac{\gamma_n}{\sqrt{2\phi_F}} \frac{\partial \phi_F}{\partial T} + \frac{1}{T}\left(\frac{E_g}{q} + \frac{3kT}{q} \right) \tag{9}$$

Compared to (8), the magnitude of first term in (9) decreases to be about -0.5 mV/°C [13], the signs of second and third terms become negative and one more term is added with a value of about 4.3 mV/°C at 300 K. Therefore, as temperature increases, the threshold voltage of NMOS becomes more negative and that of PMOS becomes more positive, in addition, the change of PMOS threshold voltage is faster than NMOS. Experimental result shows a half-volt change of threshold voltage from 25 °C to 250 °C for a typical CMOS process for both NMOS and PMOS [13].

1.2.3 Subthreshold Current

The time required to turn transistors on and off is referred to as the switching speed of the device. In the off state, the MOSFET operates in the subthreshold region; therefore, the subthreshold slope is important. The slope of the subthreshold curve increases at low temperatures. This results in a decrease in junction leakage by many orders of magnitude, which in turn enables the use of smaller threshold voltages.

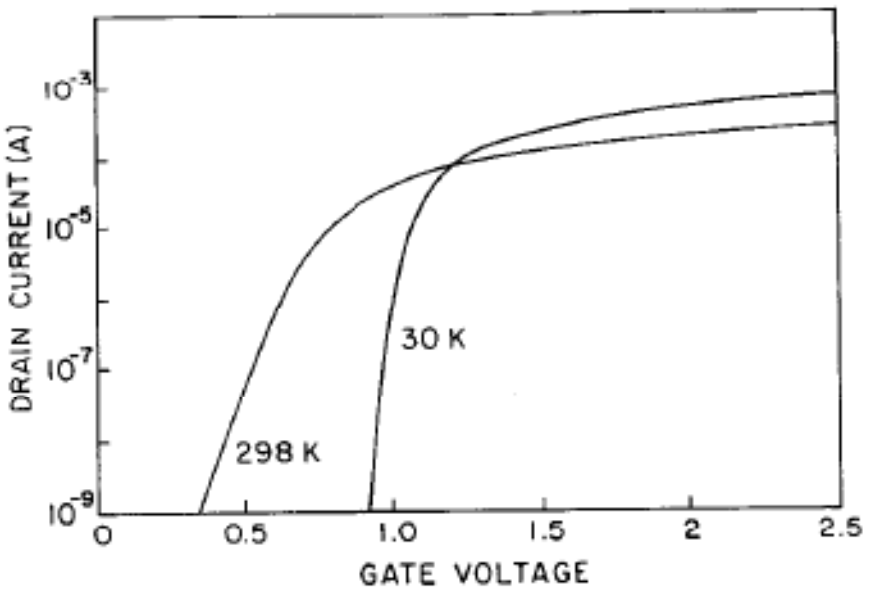


Figure 3: Transfer characteristics of n-channel MOSFET [19].

1.2.4 Leakage Current

In bulk CMOS technology, reverse biased diodes, as shown in Figure 4, exist between the source and drain diffusion regions and the substrate. Leakage currents from these two diodes are typically the limiting factor for high temperature operations.

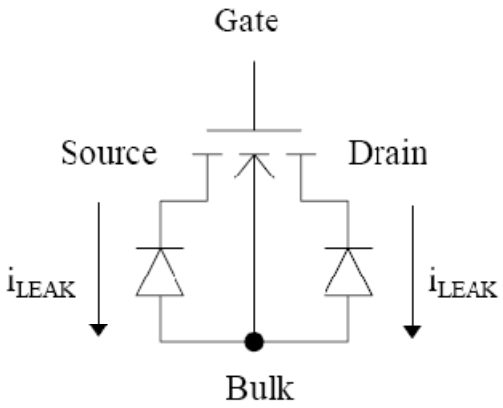


Figure 4: NMOS device with parasitic diodes

At room temperature, the leakage current is very small, usually on the order of pA. As temperature rises, two effects cause an increase of the junction leakage current [13]. First, a drift current will flow due to thermally generated electron-hole pairs in the depletion region. Generated carriers will be swept across the junction by the electric field. This effect which is proportional to the intrinsic carrier concentration usually dominates to temperatures up to 100–150 °C.

At higher temperatures, the junction leakage is dominated by diffusion of thermally generated minority carriers farther away from the junction area, which is proportional to the square of the intrinsic carrier concentration. When these carriers reach the edge of the depletion region, they are swept across the junction by the electric field. The concentration of minority carriers is a strong function of the temperature but is inversely proportional to the doping concentration. Therefore, PMOS transistors have much less leakage current than NMOS in an N-well process, as shown in Figure 5.

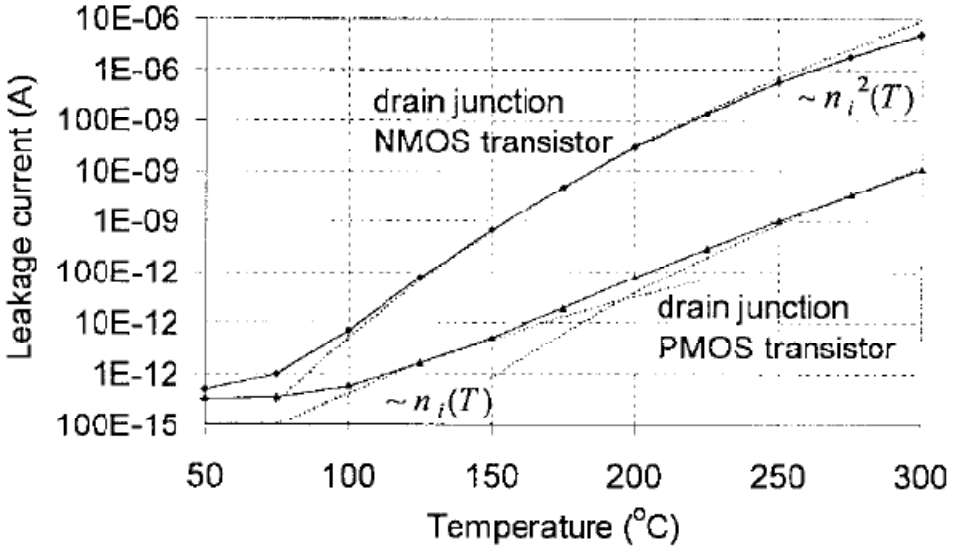


Figure 5: leakage currents of drain junctions of an NMOS and a PMOS transistor respectively. The p-type epitaxial layer has a doping concentration NA = 10^{15}cm^{-3} and the n-well doping concentration is ND = 4 x 10^{16}cm^{-3}. The area of both junctions is 2 x 20 mm^2 [4].

The total leakage current of a reverse biased diode is given by

$$I_L = I_{L,diff} + I_{L,gen} = qAn_i\left[\frac{n_i}{N_D}\sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau}V_A\right]\left(e^{\frac{qV_A}{kT}} - 1\right) \tag{10}$$

where A is the area of the p-n junction, V_A is the voltage applied to the diode, N_D is the n type doping density, W is the width of the junction depletion region at applied voltage V_A, D_P is the minority carrier diffusion constant, and τ is the minority carrier lifetime. For negative V_A (reverse bias) greater than a few tenths of a volt at temperatures below 1000 °C, the exponential terms are insignificant compared to –1, so that (10) simplifies to

$$I_L \cong -qAn_i\left[\frac{n_i}{N_D}\sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau}V_A\right] \tag{11}$$

As temperature increases beyond 25 °C up to 250 °C, the junction leakage current can rise by ~5 orders of magnitude [13].

Excess leakage currents lead to self-heating of the circuit; shifting in the operating points of analog circuits, lowering of the output resistance of high-impedance nodes, and leakage of stored charge on capacitive nodes. Leakage currents can also lead to latchup as well as a significant increase in offset among matching devices, [12]. Therefore, leakage currents constitute the most significant challenge in bulk CMOS high temperature circuits.

1.3 Organization

The remainder of this thesis is organized as follows: In chapter II an overview of ΣΔ ADCs is provided with a discussion on ADC performance metrics. Chapter III introduces the system level design of the ADC, while chapter IV discusses the proposed tuning engine and circuit implementation. Simulation and measurement results are presented in chapter V. Finally, chapter VI ends with the conclusions drawn from this work.

CHAPTER 2

OVERVIEW OF ΣΔ A/D CONVERTERS

This chapter provides an overview of some of the fundamental issues in the design of sigma delta modulators. The discussion begins with a variety metrics used to evaluate modulator performance. The basic operation of sigma-delta modulators is described subsequently, followed by a review of the quantizer linearized model as related to performance issues. Tradeoffs among a variety of sigma-delta architectures suitable for extreme temperature applications are explored.

2.1 ADC performance metrics

ADC characteristics are classified into two categories: static and dynamic performance metrics. The former include monotonicity, offset, gain error, differential nonlinearity (DNL), and integral nonlinearity (INL), whereas the latter implies signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise plus distortion ratio (SNDR), dynamic range (DR), spurious free dynamic range (SFDR), idle channel noise and the overload level (OL). A brief introduction concerning the static characteristics is given in [22]. In general, the overall performance of a $\Sigma\ \Delta$ modulator is characterized by the dynamic metrics, which can be subdivided into spectral and power metrics.

2.1.1 Spectral Metrics

When considering the spectral metrics of a ΣΔ modulator, two primary aspects must be considered:

- Total harmonic distortion (THD) is the ratio of the sum of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency. The *x*th harmonic itself is the ratio between the signal power and the power of the distortion component at the *x*th harmonic of the signal frequency [22].
- Spurious free dynamic range (SFDR) is the ratio of the signal power to the power of the strongest spectral tone [22]. Figure 6 illustrates both spectral metrics.

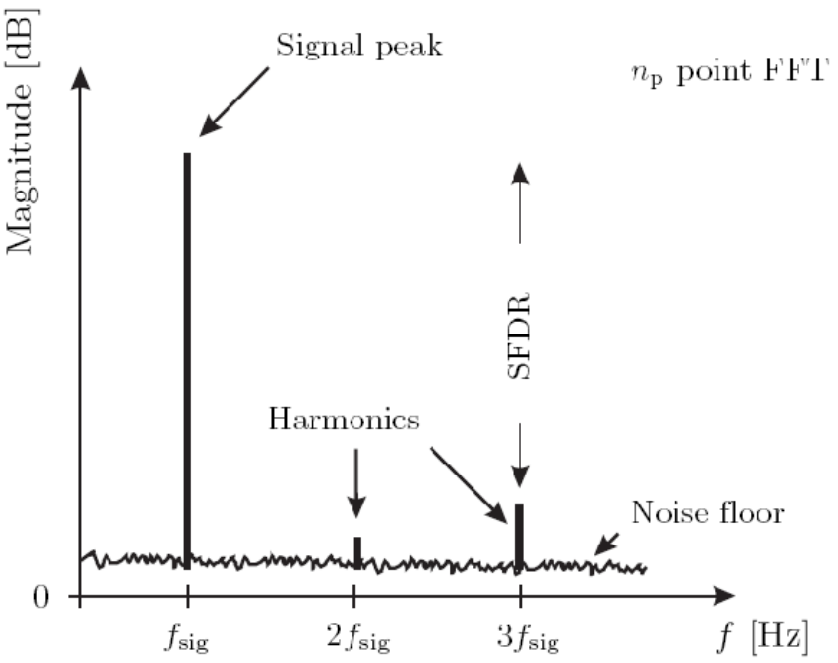


Figure 6: Typical spectrum with signal peak and harmonics.

2.1.2 Noise and Power metrics

These are commonly the most important measures, when ΣΔ ADCs are described or compared. All of these measures are obtained from the output spectrum by integration, or by inspection, these metrics include:

- In-band noise: The integrated in-band noise (IBN) is a common ΣΔ modulator measure, because it gives the total output noise in the band of interest and thus the minimum resolvable signal power. In spite of its little importance as a real ADC performance metric in terms of number of bits, it gives direct insight into the influence of architectural alternatives, nonideal behavior and so on. The IBN contains all in-band power

including noise, distortion or other tones. Only the signal itself is subtracted.

- Signal-to-noise ratio: The SNR of a converter is the ratio of the signal power to the noise power at the output of the converter, specified for a certain input amplitude. Most often, the maximum SNR is pointed out. In this work, the SNR is obtained by applying a signal at a frequency fsig > $f_B/2$, i.e., no signal distortion will appear in the band of interest (when no intermodulation occurs).
- Signal-to-noise and distortion ratio (SNDR): The SNDR is the ratio of the signal power to the noise and all distortion power components. Thus, the corresponding spectra are obtained by applying a signal at fsig ≤ $f_B/3$ to include at least the second and third harmonic inside the band of interest.
- Overload level (OL): also known as maximum stable amplitude is defined as the maximum input sinusoidal signal, for which the modulator still operates correctly. The input signal level for which the SNR falls 6dB below the peak value SNRp is considered the OL.
- Dynamic range (DR): The DR is defined as the ratio of rms value of the maximum input sinusoidal signal, for which the modulator operates correctly, to the rms value of the smallest detectable input sinusoidal signal.

For ΣΔ modulators most of these power measures are collected in a plot as shown in Figure 7.

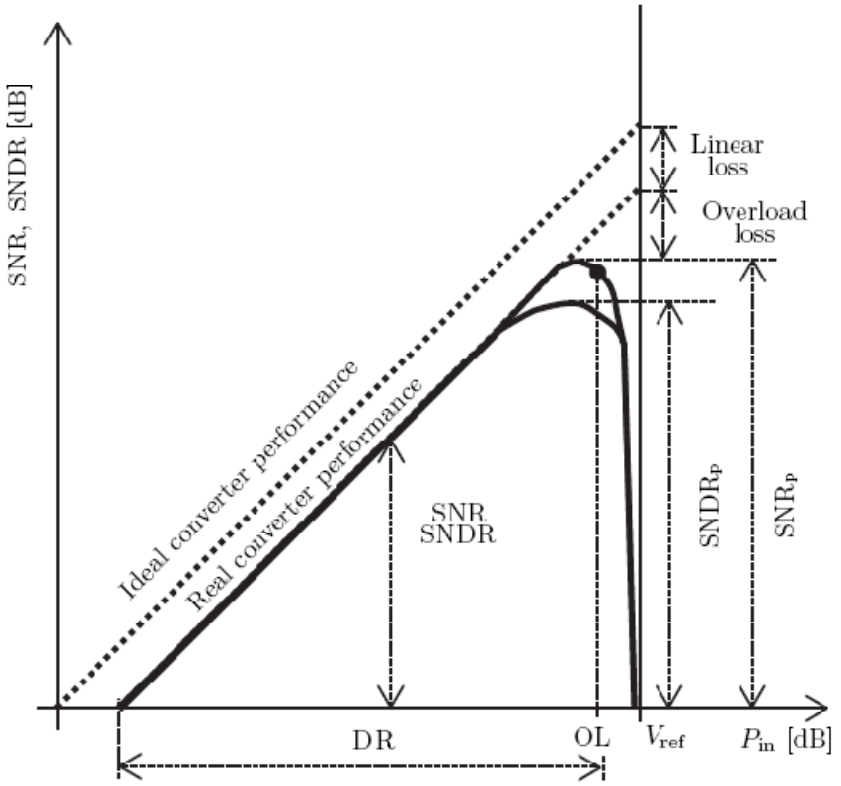


Figure 7: Power and noise performance characteristic of a ΣΔ converter

2.2 Nyquist-rate A/D Converters

Analog-to-digital conversion is the process of encoding an analog signal that is continuous in time and amplitude into a signal that is discrete with respect to time and quantized in amplitude. The fundamental operations comprising A/D conversion are illustrated in Figure 8.

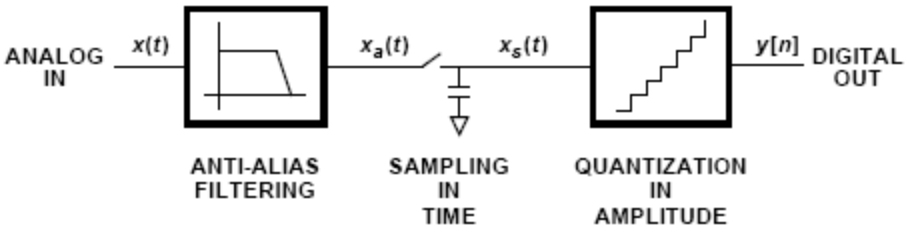


Figure 8: Fundamental operations comprising analog-to-digital conversion.

The analog input signal, $x(t)$, first passes through a band limiting lowpass filter, removing the signal components that lie above one-half of the sampling rate of the subsequent sampler. Otherwise, from the Nyquist sampling theorem [21], high frequency components of $x(t)$ would alias into the passband upon sampling, causing distortion that cannot be filtered or even distinguished from the original signal. Following the antialiasing filter, the bandlimited signal, $xa(t)$, is sampled, thus yielding the discrete-time signal, $xs(t) = xa(nTs)$, which is still continuous in amplitude. The sampled-data analog signal is then quantized in magnitude by the ensuing quantizer before being encoded into the output data signal, $y[n]$.

2.2.1 Sampling

From the Nyquist sampling theorem, if there is to be no loss of information or aliasing distortion upon sampling, *x(t)* must be sampled at a frequency higher than twice the baseband cutoff frequency, f_b, which is defined as the cutoff frequency for the antialiasing filter as shown in Figure 3.2. In the frequency domain, the spectrum of the sampled signal, $x_s(t)$, is

$$X_S(f) = \frac{1}{T_S} \sum_{k=-\infty}^{\infty} X_a(f - kf_S) \tag{12}$$

If the sampling frequency, f_s, is chosen to be at, or slightly higher than, the Nyquist rate, $2f_b$, then the converter is said to be a *Nyquist-rate converter*. However, the sampling rate can deliberately be chosen to greatly exceed the Nyquist rate in order to exploit the benefits of oversampling, described later in

this chapter. In this case, the converter is referred to as an *oversampling converter*. When the passband extends from dc to f_b, the oversampling ratio, M, is defined as $M = f_s /(2xf_b)$, with $M = 1$ for a Nyquist-rate converter. The two classes of sampling are depicted in Figure 9.

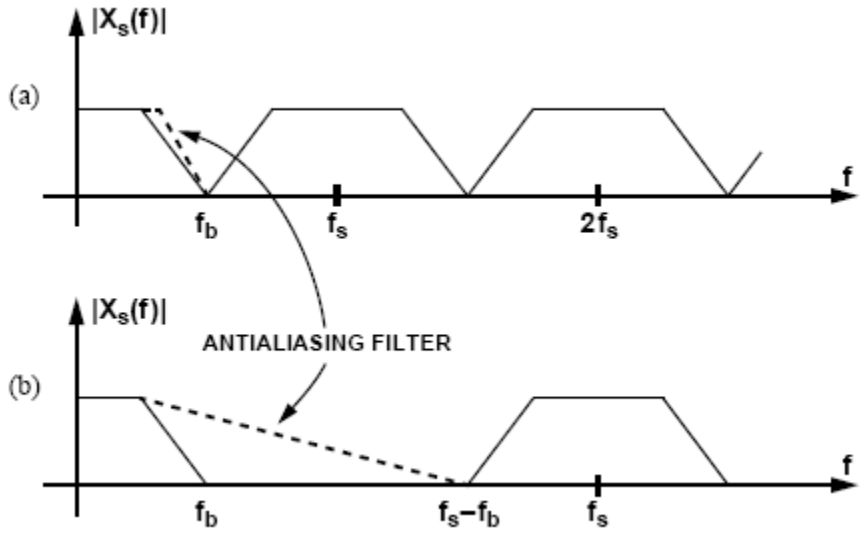


Figure 9: An analog signal (a) sampled at the Nyquist rate, and (b) oversampled.

2.2.2 Quantization

In principle, the sampling process does not result in any loss of information, provided that the sampling rate exceeds the Nyquist rate. However, this is not true of the quantization of the sampled signal because, in this non-reversible operation, a continuous range of amplitudes is mapped into a finite set of digital output codes. The transfer characteristic of a uniform quantizer with a gain of unity is illustrated in Figure 10(a), and the resulting saw-tooth quantization error is illustrated below in Figure 10(b).

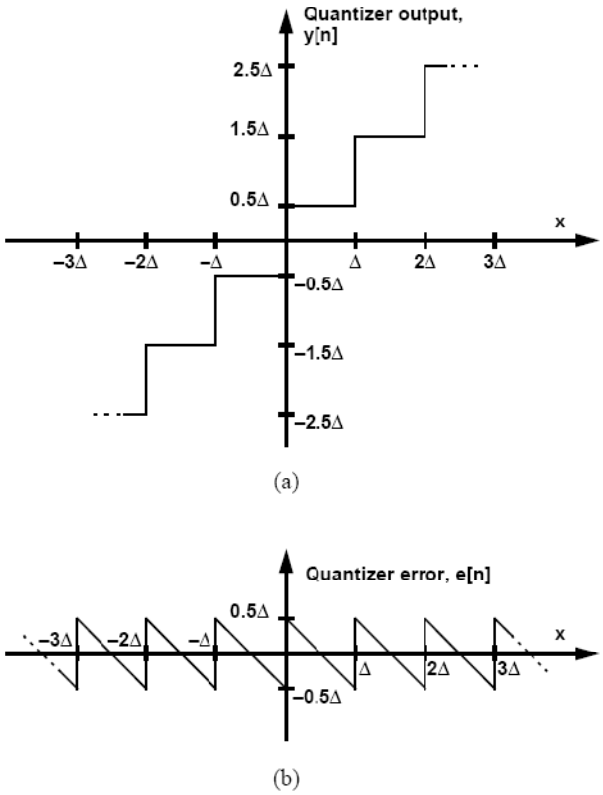


Figure 10: (a) Transfer characteristic and (b) error characteristic of a uniform quantizer.

A unity-gain, uniform N-bit quantizer has 2N quantization levels, and the step size, D, between quantization levels is

$$\Delta \equiv \frac{V_{REF}}{2^N - 1} \tag{13}$$

where V_{REF} is the full-scale input and output range of the quantizer.

The output of the quantizer can be written as a sum of the input signal, $x[n]$, with the quantization error, $e[n]$, which is the result of a nonlinear operation, $q\{\cdot\}$, on $x[n]$:

$$y[n] = x[n] + e[n] = x[n] + q\{x[n]\} \tag{14}$$

However, it is difficult to analyze the effect of the quantizer using (14) because of the nonlinear and signal-dependent nature of the quantization error. To

simplify the analysis, the quantization error, e[n] = q{x[n]}, is often approximated as additive white noise, and the quantizer is analyzed using statistical methods. Despite the deterministic nature of the quantizer error, it can be shown that the white noise approximation is valid if the following conditions are satisfied [22]:

1) The input signal should not exceed the full scale range of the quantizer.
2) The quantizer has sufficient number of quantization levels.
3) The input signal range spans many quantization levels.
4) The joint probability density of any two quantizer input samples is smooth.

It is permissible under these conditions to assume that the quantization error, $e[n]$, is distributed uniformly across its entire range, $-\Delta/2$ to $\Delta/2$, with the rectangular probability density function shown in Figure 11. The quantizer can then be replaced with the linearized stochastic model of Figure 12. The variance of the quantizer error, $e[n]$, is

$$\sigma_e^2 = \frac{1}{\Delta}\int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12} \tag{15}$$

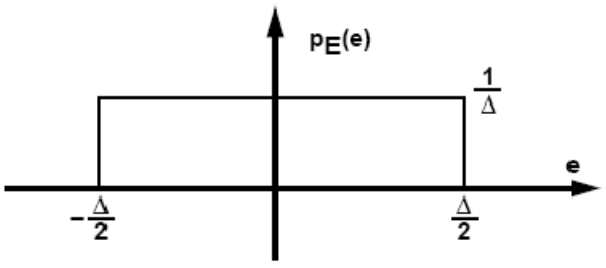


Figure 11: Probability density function of additive, white quantization noise.

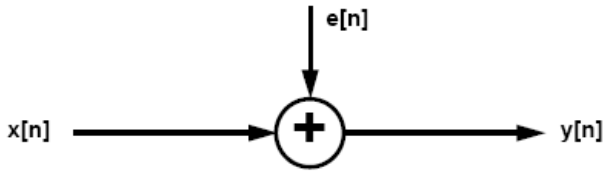


Figure 12: Linearized, stochastic model of quantizer.

DR can be shown to be equal to

$$DR = \frac{3}{2}2^{2N} \tag{16}$$

The familiar expression relating the dynamic range to the number of bits of a uniform *N*-bit quantizer is found by taking the *log* of (16), which leads to

$$10\log DR = 6.02 \times N + 1.76dB \tag{17}$$

Therefore, if the resolution of an A/D converter is limited by quantization noise, then its dynamic range increases by approximately 6 dB with every additional bit of resolution. In practical implementations, the minimum resolvable signal is limited by thermal noise rather than quantization noise. Nevertheless, in such cases, the dynamic range is defined similarly, with the lower limit established by an input signal level that yields a signal-to-noise ratio of one.

2.2.3 Limitations of the Additive White Noise Model

Due to the fact that the quantization noise is actually correlated with the input signal, the spectrum of the quantizer output can contain discrete tones that are not predicted by the white noise model [22]. This correlation is particularly strong in the case of 1-bit quantizers used in first order ΣΔ modulators and leads

to tonal components at the modulator output [23]. However, it is nevertheless useful to model the quantizer in this manner to predict the performance of an A/D converter. Even though the 1-bit quantizer violates the conditions of the model, the white noise quantizer model still allows for an accurate estimate of the dynamic range of a modulator that is comprised of a 1-bit quantizer embedded in a feedback loop. In such cases, the only justification for modeling the quantizer as an additive white noise source is that behavioral simulations of the system confirm the estimate of the dynamic range arrived at with the use of this model.

2.3 Oversampled A/D Converters

Data converters can be grouped according to their sampling rate into two categories, Nyquist rate and oversampling converters. Nyquist rate converters, include successive approximation register, pipeline and double integration sample analog signals with a maximum frequency less than the Nyquist frequency $f_N \leq f_s/2$, where f_s is the sampling frequency. Oversampling converters perform the sampling process at a much higher rate, $f_N << Fs$ where Fs denotes the input sampling rate. For a B bits quantizer and step size q, the noise power is spread equally over the entire frequency range. For a Nyquist rate sampler (Figure 13), the level of the noise power spectral density N(f) can be expressed as

$$N(f) = \frac{q^2}{12 f_s} \tag{18}$$

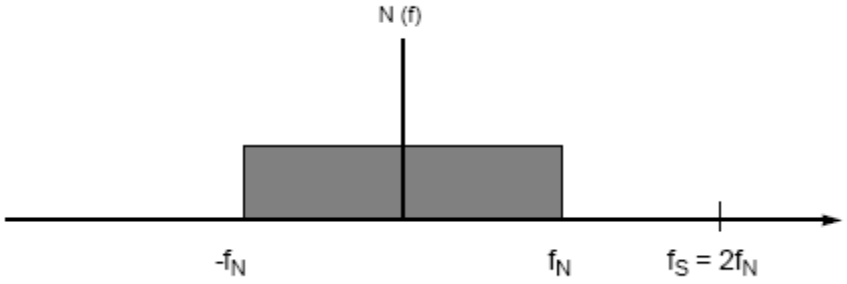


Figure 13: Noise Spectrum of Nyquist Samplers.

For the oversampling A/D (Figure 14), the level of the noise power spectral density N(f) can be expressed as

$$N(f) = \frac{q^2}{12F_s} \tag{19}$$

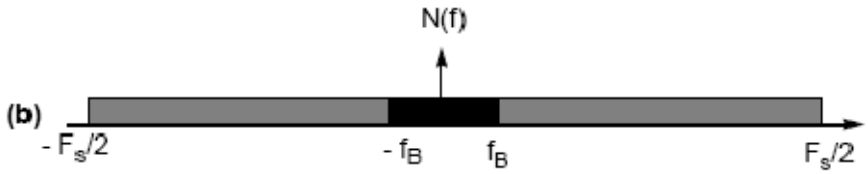


Figure 14: Noise spectrum of oversampling converters.

The in-band noise level is therefore

$$N_B = \int_{-f_B}^{f_B} N(f)df = \frac{2q^2 f_B}{12F_s} \tag{20}$$

It is obvious that oversampling results in a reduction of the in-band noise level, therefore an increase in the signal to noise ratio (SNR). Additionally, the inclusion of an analog loop filter can further reduce the in-band quantization noise at the expense of a larger noise power outside the band. This is the concept of noise-shaping. Sigma delta modulators (ΣΔ) make use of both oversampling and noise

shaping to achieve a high SNR in the band of interest. Figure 15 illustrates the main components of a ΣΔ A/D converter

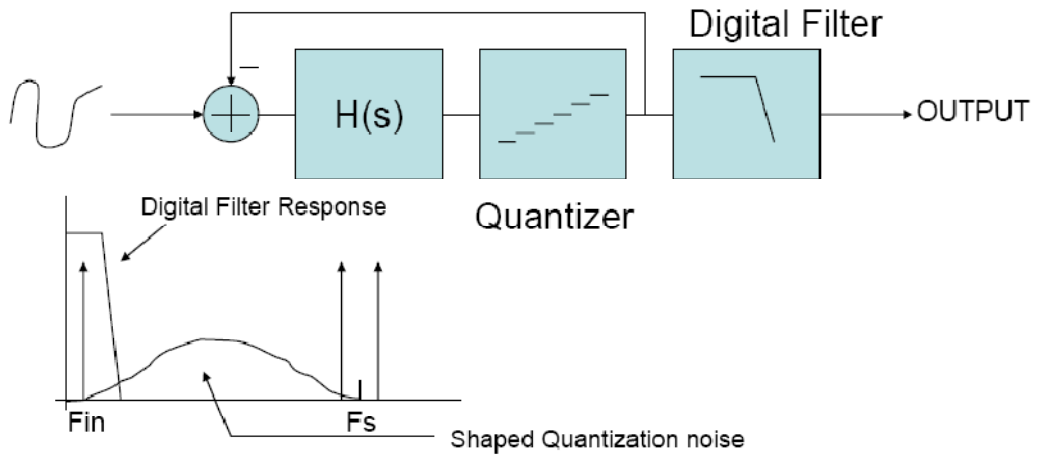


Figure 15: Generalized sigma delta modulator.

To understand why this works quantitatively, the quantizer is replaced with its linearized model. The quantizer is assumed to have unity gain with an added noise source N_Q as shown in Figure 16

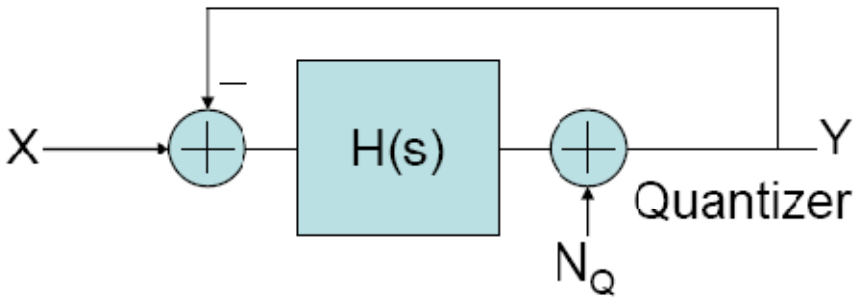


Figure 16: Modulator with linear quantizer model.

The transfer function is given by

$$Y = \frac{H(s)X}{1+H(s)} + \frac{N_Q}{1+H(s)} \tag{21}$$

$$Y = STF(s)X + NTF(s)N_Q \tag{22}$$

where STF(s) and NTF(s) are the signal transfer function and noise transfer functions respectively. For the frequency range where H(s) is large, N_Q is attenuated, and the output Y is a close approximation of the input X.

2.4 Discrete-Time and Continuous-Time ΣΔ Modulators

ΣΔ ADCs have been typically implemented using Discrete-Time (DT) circuits which are switched-capacitor (SC) based circuits. This is because SC circuits can be easily designed with high linearity. However, the bandwidth of DT ΣΔ ADCs is limited to a few MHz because they are power hungry. Design of high gain bandwidth product (GBW) and slew rate (SR) OTAs is prohibitive [32].

As demands of lower power consumption and greater integration increased, continuous-time (CT) ΣΔ ADCs emerged as a more desirable solution because of the relaxed GBW and SR requirements of OTAs. In addition, CT ΣΔ ADCs have an inherent anti-aliasing filter (AAF) which can relax the design requirements of an additional AAF or even eliminate it, resulting in lower system complexity and power consumption [31]. Table 3 summarizes advantages and disadvantages of DT and CT modulators.

Table 3: Comparison of DT and CT ΣΔ modulator.

	Advantages	Disadvantages
DT	• Insensitive to clock jitter • Insensitive to exact shape of OTA's settling waveforms • Accurate pole-zero locations	• Large capacitors for high performance • Requires an AAF • Large spike and glitch current drawn by capacitors • Susceptible to high leakage currents and voltage errors at high temperatures
CT	• High-speed operation • SNR is not limited by cap size • Low power consumption • High temperature operation	• Requires linear resistor • RC-time constant variation • Sensitive to clock jitter • Loop filter does not scale with sampling frequency

CHAPTER 3

SYSTEM DESIGN OF THE THIRD ORDER CT ΣΔ MODULATOR

This chapter presents system-level design of the continuous-time ΣΔ modulator for use in extreme temperature environments. The choice of modulator architecture is discussed. A single-bit single-loop third-order continuous-time ΣΔ modulator with an OSR of 400 is designed. The effects of circuit non-idealities on the performance of the ΣΔ modulator are studied. Design solutions are proposed to diminish their effect.

3.1 CT ΣΔ Modulator Architecture

A single-loop topology was chosen instead of a MASH design in order to avoid the complexity resulting from the additional circuitry needed to match the NTF and the digital noise-cancellation filter. This is particularly critical for operation at extreme temperatures, since mismatches between the two filters on the order of 1% could result in SNR loss at the output around 10dB or more [21]. A third-order NTF was chosen so that a peak signal-to-quantization- noise ratio (SQNR) well above the 120 dB SNR (in a 10 kHz signal bandwidth) required of the modulator could be achieved at a low sampling frequency. This way, the design requirements on the analog blocks of the loop filter are relaxed and the performance of the design would be limited by thermal noise alone. Additionally, having the circuit thermal noise dictate the limits on the modulator SNR performance has the added benefit of adding a random dithering signal to the

embedded quantizer, thereby decorrelating the quantization error from the input signal. A justification of the other architectural choices made in the converter is now further discussed.

3.1.1 Topology

A single-loop topology was chosen over a cascaded (MASH) design, because proper operation of the MASH modulator would require perfect matching between analog loop filters and the digital noise cancellation filter. Due to operation in extreme temperatures, analog loop filter coefficients would vary considerably leading to significant mismatch with the noise cancellation digital filter coefficients and an eventual loss of SNR.

A Cascaded Integrators with Feed Forward summation (CIFF) topology was selected to implement the loop filter. This topology offers several advantages compared to the conventional Cascaded Integrators with Multiple Feedback (CIMFB) topology. Firstly, a significant area reduction can be achieved in the CIFF topology, especially for the case of resistive feedback DAC implementation, which occupies a large chip area even with the use of high-resistivity poly resistors with a sheet resistance of about 1kΩ square. A multiple-feedback loop filter would need three DACs. Typically, the impedance levels in the second and third integrators are chosen to be several times those in the first integrator to reduce power dissipation by reducing the capacitor sized in those stages. This means that the feedback DACs feeding into the second and third integrators would be much larger and occupy an even larger area.

Another factor in favor of using a CIFF architecture instead of one that has multiple-feedback loop filter is best explained with the aid of Figure 17, where the block diagrams of modulators with an OBG of 1.5 and a sampling rate of 1 Hz are shown. Part (a) of the figure shows a feedforward design, where the integrator unity gain frequencies are scaled so that the peak signal swing of the first integrator (the one with a unity gain frequency of) is one half that of the other two integrators. This way, the first integrator limits the last, thereby aiding recovery of the modulator from overload. No additional provisions were made to reset the integrating capacitors.

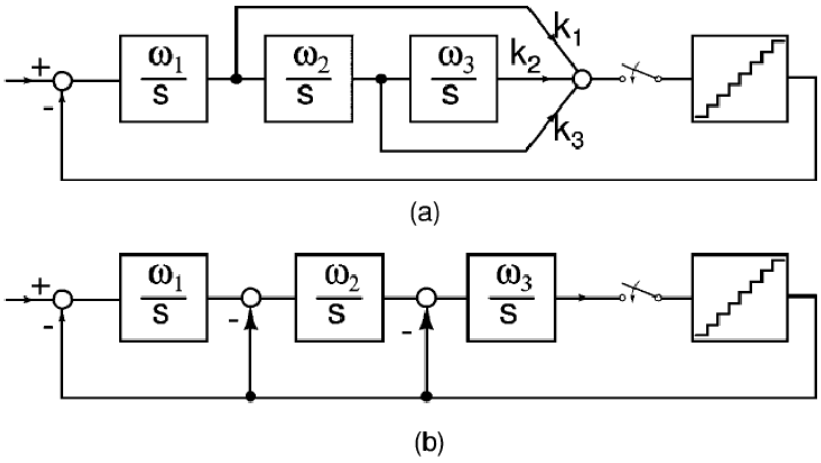


Figure 17: CIFF and CIFB modulators—the out-of-band gain of 1.5 and sampling rate of 1 Hz. (a) $\omega_1 = 2.77$, $\omega_2 = 2.0$, $\omega_3 = 0.06$. (b) $\omega_1 = 0.30$, $\omega_2 = .80$, $\omega_3 = 1.2$

Figure 17(b) demonstrates the unity gain frequencies for a CIFB design. The value of the integration resistor in the first integrator in both designs is set by the thermal noise limit. The second and third integrators can be implemented with smaller capacitors and much larger resistors. We note that the first integrator has

the widest bandwidth in a feedforward design, while in a multiple-feedback modulator, the first integrator has the smallest bandwidth. Thus, the integration capacitor of the first integrator in a feedforward loop filter will be much smaller than that in a multiple-feedback modulator.

It is also worthy to note that since the overall ADC resolution is limited by the input noise to the first stage integrator, and that the distortion characteristics of the first stage also limit the overall harmonic distortion at the output of the modulator, a large DC gain and bias current are often required in the first integrator. This is conducive to the first integrator having the largest bandwidth in the loop filter.

A third reason for favoring a CIFF architecture over a CIFB is that feedforward paths in a CIFF modulator aid in modulator recovery from an overload condition. This is due to the fact that the first integrator in a CIFF modulator has the widest bandwidth in the loop filter and therefore it saturates last, whereby the third integrator would overload first followed by the second integrator. This leads to a reduction of the overall order of the loop filter from a third order to a first order in the case of an overload, but it would not necessitate further remedial action such as a full system rest.

3.1.2 Number of Quantizer Levels

Although a multibit implementation offers several advantages over a single bit modulator such as a reduction of in-band quantization noise, reduced clock jitter noise and relaxation of slew rate requirements for the loop filter, a

multibit implementation adds substantial complexity and area requirements as well as incompatibility with operation at extreme temperatures.

Firstly, the feedback DAC must meet the overall linearity requirements and distortion requirements of the entire ADC. This implies an SNR of a 120 dB or more at the output of the DAC as well as a SFDR in excess of 120dB. Since the ΣΔ modulator is a continuous time implementation. A capacitive feedback DAC is not an option, thus leaving resistive or current mode DACs as the only viable solutions. Several matching and linearity enhancing techniques (dynamic element matching) have been previously proposed in literature [22], [23], however, ADC resolution was limited to 12 bits. This is due to the limitation of achieving a 20 bit linear continuous time feedback DAC. Additionally, dynamic element matching linearization techniques add significant power consumption, circuit complexity and an area overhead. A single bit DAC implementation is inherently linear, thereby alleviating the need for further linearization techniques [20], [21], [23].

Another important reason for using a single bit DAC over a mulitbit implementation is the low tolerance of the latter to operation at extreme temperatures. This is due to the susceptibility of the multibit continuous time DAC linearity to temperature variations which in our case are well in excess of 200°C. This implies that even a multibit DAC with dynamic element matching implementation will have a strong temperature dependency and lead to significant loss of resolution depending on the particular temperature.

A single bit resistive DAC's linearity is not a function of temperature, however, the feedback coefficient formed by the DAC resistor and the first stage

integrator capacitor is a strong function of temperature. Design solutions are proposed to remedy this problem further on.

3.1.3 Loop Filter and OSR

The ΣΔ modulator composed with 1-bit internal quantizer and a third-order single loop filter in CIFF configuration is shown in Figure 18.

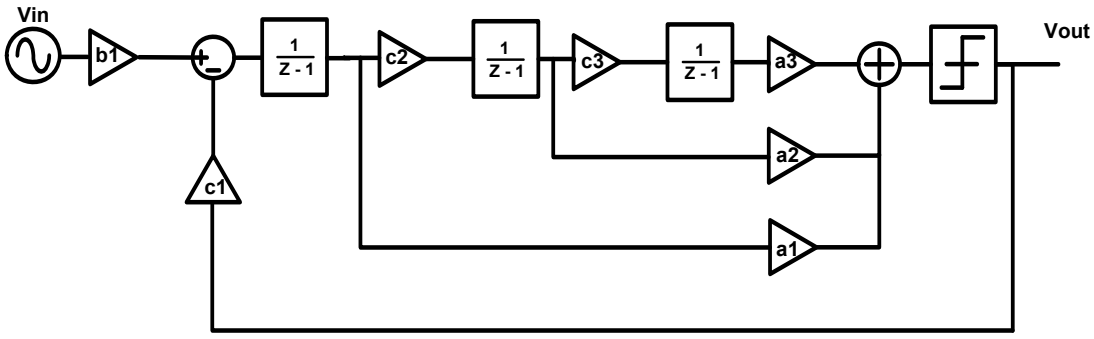


Figure 18: Discrete time model of the third order modulator

The STF is given by

$$STF = \frac{a1b2(z-1)^2 + a2b1c2(z-1) + a3b1c2c3}{(z-1)^3 + a1c1(z-1)^2 + a2c1c2(z-1) + a3c1c2c3} \tag{23}$$

The NTF is given by

$$NTF = \frac{1}{(z-1)^3 + a1c1(z-1)^2 + a2c1c2(z-1) + a3c1c2c3} \tag{24}$$

The STF and NTF are plotted in Figure 19.

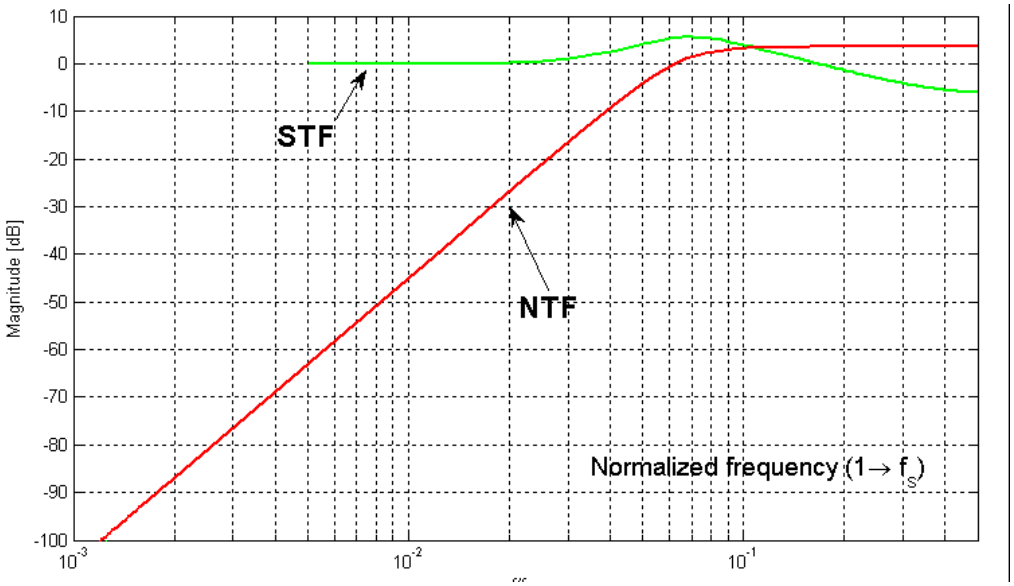


Figure 19: ΣΔ modulator STF and NTF vs. normalized frequency.

Following the application of the impulse invariant transformation and signal scaling, the CT ΣΔ modulator coefficients are provided in Table 4.

Table 4: CT ΣΔ modulator coefficients.

Coefficients	Values
a1	.2
a2	.5
a3	.08
b1	.1
c1	.1
c2	.3
c3	.5
k_{dfb}	.4

Peaking in the signal transfer function (STF) at high frequencies is inherent in the filter characteristic and could lead to an overload. This is particularly critical in wireless applications where the presence of an out-of-band blocking signal could cause the modulator to overload. A low pass filter can be used to limit the frequency of the signal at the input in such applications. In our case, blocker signals are not expected at the input.

For ΣΔ modulators with signal bandwidths up to tens of kHz, a large oversampling ratio (OSR) is usually used with high order noise shaping to achieve high resolutions. System tradeoffs were made regarding the modulator order (L), quantizer resolution (B), sampling frequency (Fs) and OSR in order to meet the 20 bit resolution according to

$$SNR = \frac{3\pi}{2} \cdot \left(2^B - 1\right)^2 \cdot (2L+1) \cdot \left(\frac{OSR}{\pi}\right)^{2L+1} \tag{25}$$

The theoretical SQNR calculation of 1 bit SD ADC converters can be seen in Figure 20. It can be seen that as the order is increased there is a dramatic increase at the SQNR. On the other hand, higher order modulators over 2nd order are vulnerable to instability. In order to resolve this, the NTF should be chosen carefully, which reduces the SQNR of this theoretical calculation.

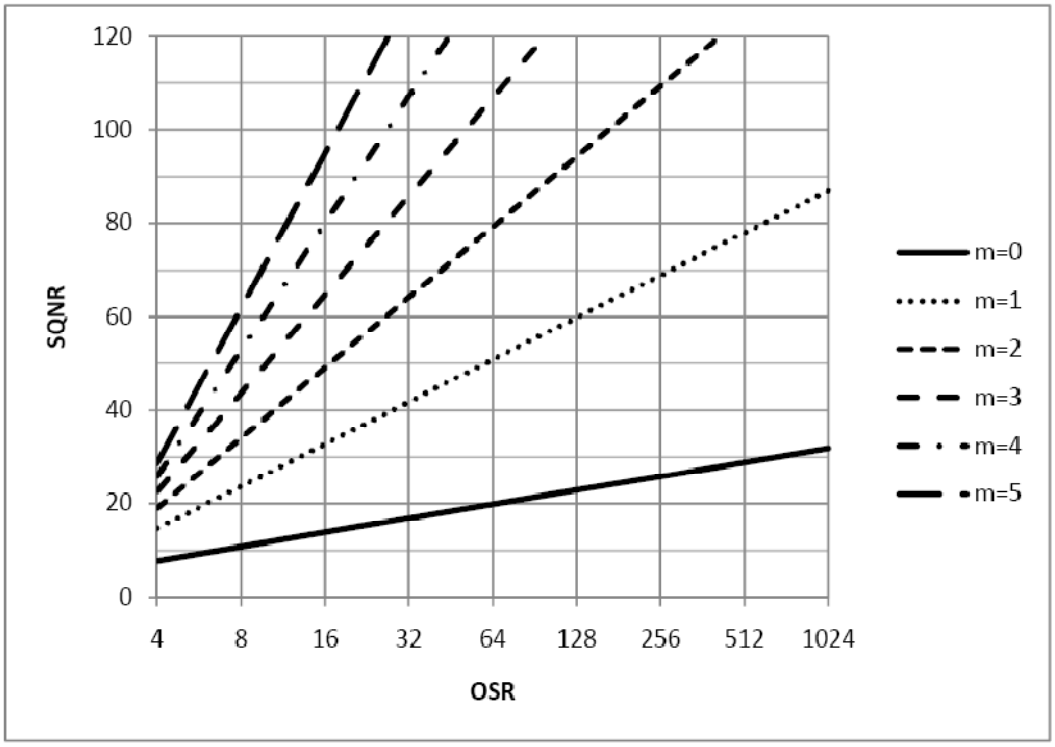


Figure 20: Theoretical SQNR of m^{th} order single bit ΣΔ Modulator [25].

3.1.4 Ideal Model Behavioral Simulations

The proposed modulator was simulated with ideal building blocks by using a Matlab Simulink ideal model as shown in Figure 21.

Figure 22 shows the simulated output power spectrum density (PSD) of the ideal model and 130 dB SQNR is achieved. Figure 23 shows the simulated histograms of each integrator's output. From this simulation, output swing requirements for each integrator can be determined. The first stage integrator should have at least a 0.3Vpk-pk output swing range to avoid signal clipping and a 1Vpk-pk swing range is required for the second stage. Finally, the third stage must have a 1Vpk-pk output swing range.

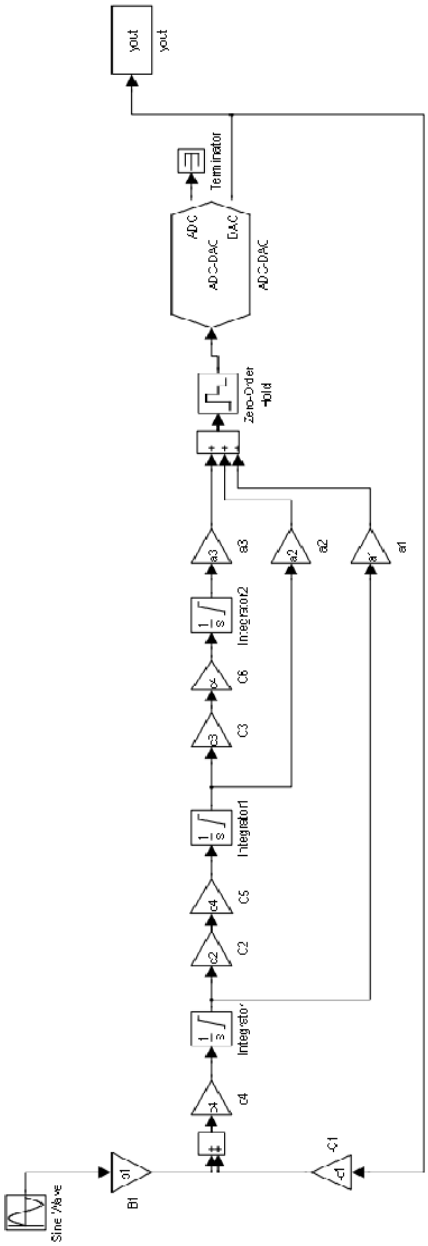


Figure 21: Simulink behavioral model of the ideal third order, single bit CT modulator.

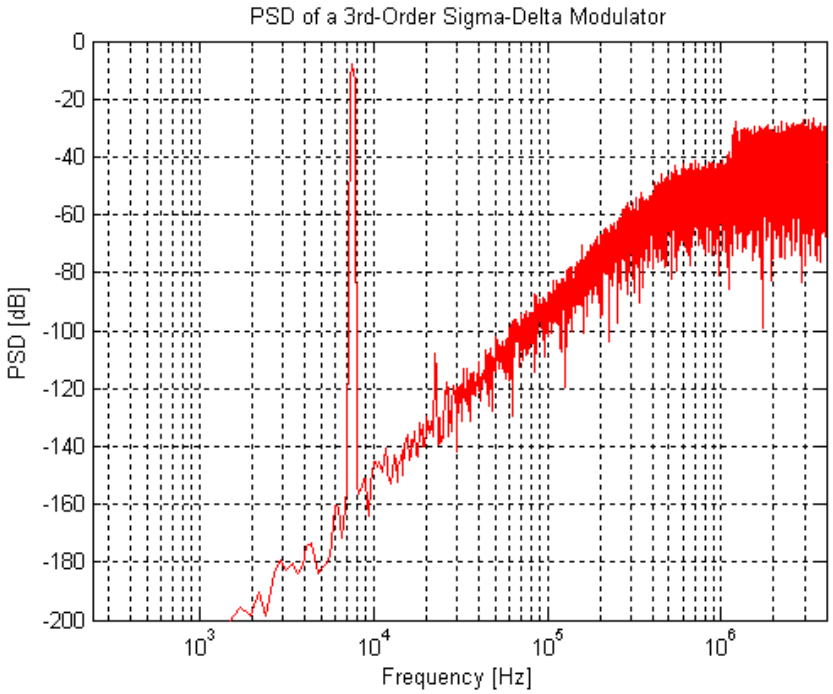


Figure 22: PSD of the ideal CT modulator Simulink model for a 1V peak input signal at 7.5 kHz.

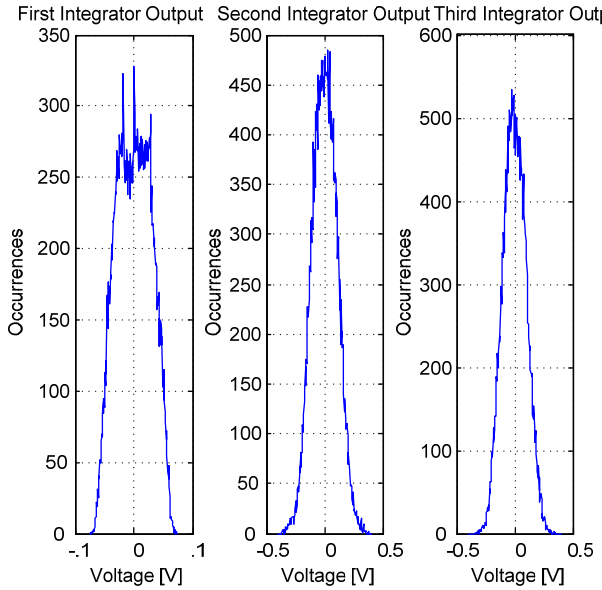


Figure 23: Histograms for the integrator outputs in the ideal modulator model.

3.2 Modulator Non-idealities

The effect of multiple modulator non-idealities on the performance of the modulator is studied next.

3.2.1 Finite DC gain and GBW in an Op-Amp

In Figure 24 an n-input path active-RC integrator with a single pole amplifier is shown. The single pole amplifier can be modeled as:

$$A(s) = \frac{A_{dc}}{\frac{s}{\omega_p} + 1} \tag{26}$$

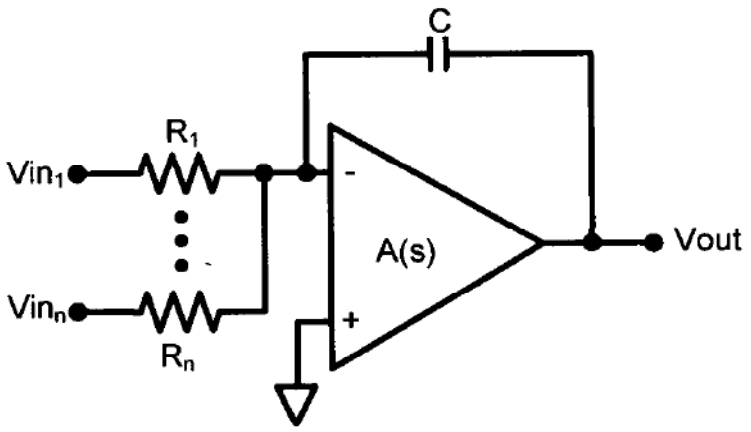


Figure 24: An n input path active-RC integrator with a single pole amplifier.

where A_{dc} is the DC gain and ω_p is the dominant pole of the amplifier in the integrator. The transfer function from the *ith* input to the output is therefore given by [30]:

$$I_i(s) = \frac{k_i f_s}{s\left(1 + \frac{1}{A(s)}\right) + \frac{1}{A(s)} \sum_{i=1}^{n} k_i f_s} \tag{27}$$

For simple calculation, the finite DC gain and GBW can be considered separately. If the finite DC gain is accounted for alone, the equation (27) can be modified as:

$$I_i(s) \cong \frac{k_i f_s}{s + \frac{1}{A_{dc}} \sum_{i=1}^{n} k_i f_s} \tag{28}$$

Hence, the integrator becomes leaky. This effect reduces quantization noise shaping strength at low frequencies. If only the finite GBW is considered, the transfer function is given by

$$I_i(s) \cong \frac{k_i f_s}{s} \frac{GE_{GBW}}{1 + \frac{s}{\omega_x}} \tag{29}$$

$$GE_{GBW} = \frac{GBW}{GBW + \sum_{i=1}^{n} k_i f_s} \tag{30}$$

$$\omega_x = GBW + \sum_{i=1}^{n} k_i f_s \tag{31}$$

Finite GBW not only affects an integrator coefficient error but also creates a 2nd pole reducing the filter phase margin. Therefore, finite DC gain and GBW have significant impact on modulator performance. For MASH architecture, the performance reduction is even worse. This is yet another reason why a single loop modulator topology is favorable in comparison to cascaded architectures for extreme temperature operation. Finite DC gain and GBW should be determined during the initial design phase and iterative behavioral simulations should be

performed to define the minimum specifications. In order to do that (27) is modified to

$$I_i(s) = \frac{1}{1+\frac{s}{k_i f_s}} \frac{A(s)}{1+A(s)\beta(s)} \tag{32}$$

Where β is given by

$$\beta(s) = \frac{\frac{s}{k_i f_s} + \frac{1}{A(s)} \frac{\sum_l k_{l,l\neq i}}{k_i}}{1+\frac{s}{k_i f_s}} \tag{33}$$

Therefore the integrator with the finite gain and bandwidth can be modeled as shown in Figure 25.

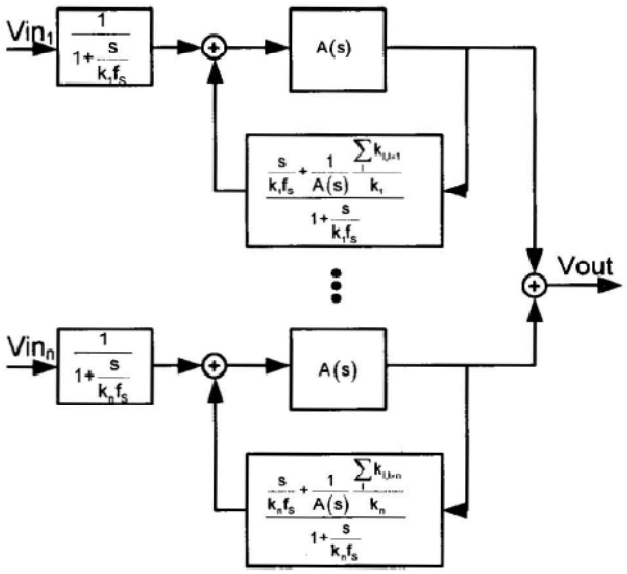


Figure 25: behavioral model of the n-input active-RC integrator in figure 21.

Figure 26 and Figure 27 show the SNR degradation resulting from Operational Transconductor Amplifier (OTA) gain and bandwidth variations. Since the first stage has a dominant impact on the modulator's performance, the effect of the first OTA's functional variation is simulated alone. Figure 26 shows that the gain of the first stage should be above 60 dB. The SNR starts to fall below 120 dB if the OTA gain is lower than 50 dB. Also, the modulator is robust to wide variation of the OTA bandwidth, as long as the GBW is above 8Mhz, little SNR degradation is observed. Figure 27 shows that the SNR is similarly robust with respect to the second and third stage OTAs their gain and bandwidth variations.

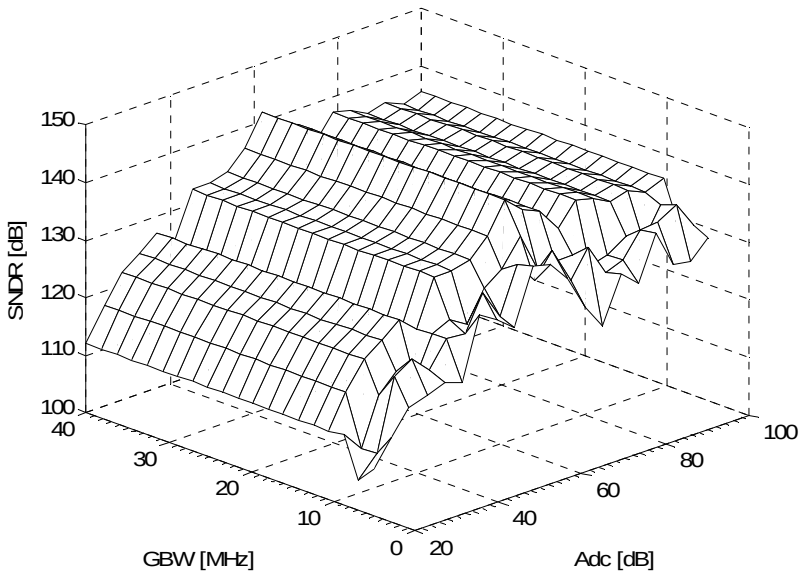


Figure 26: SNR versus gain and bandwidth variations for the first integrator.

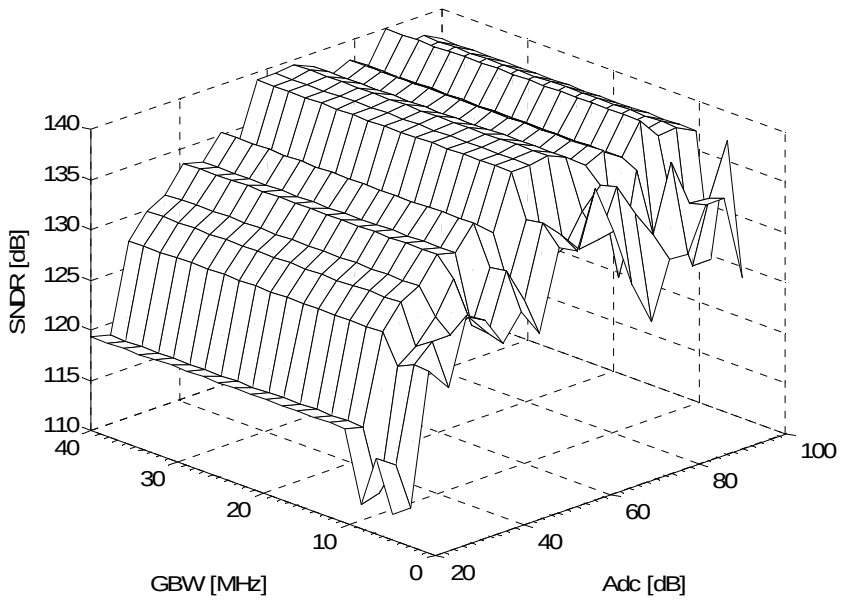


Figure 27: SNR versus gain and bandwidth variations for the second and third integrators.

It should be noted that the above analysis and Simulink models do not include temperature. However, the results can be used to predict the deterioration in modulator performance due to the operation in extreme temperatures. Therefore, suitable values for gain and bandwidth can be selected with adequate margin such that acceptable performance is guaranteed across all temperatures. The ultimate test of the modulator performance across all corners is best done using circuit level simulations in Cadence.

3.2.2 Excess Loop Delay

Figure 28 shows a discrete time SD modulator and its continuous time counterpart. The discrete time modulator and continuous time modulator are equivalent if the error signal e[n] in both modulators is equivalent. This equivalency in the signal path is satisfied only when an impulse-invariant transformation is used to calculate the continuous time transfer function H(s).

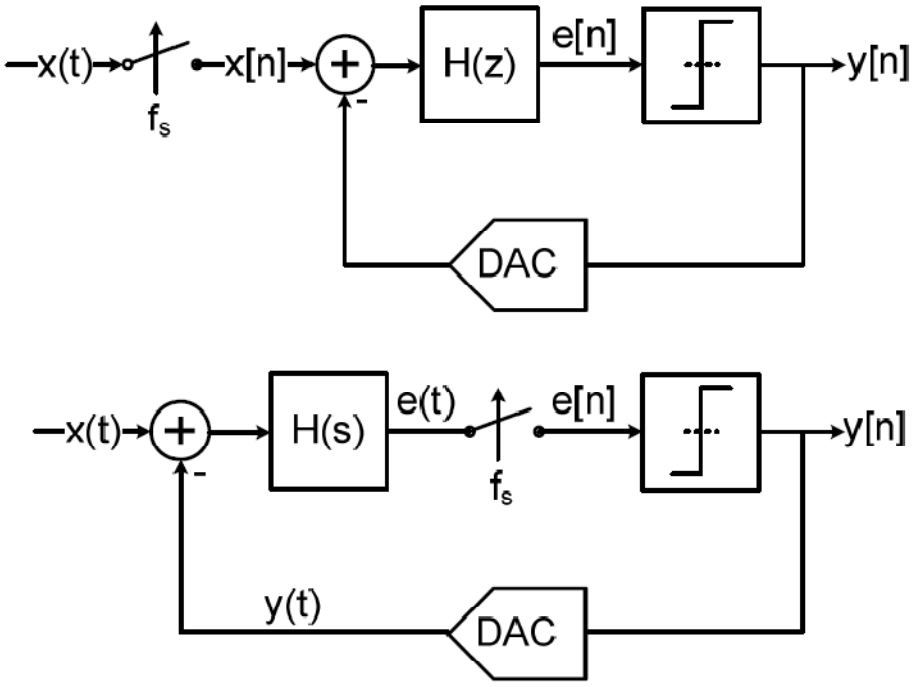


Figure 28: Block model of a discrete time ΣΔ modulator and it's equivalent CT implementation.

In a practical continuous-time ΣΔ modulator, there exists a loop delay between the sampling clock and DAC feedback pulse due to the nonzero switching time of the transistors in the feedback path. This undesired loop delay results in the DAC pulses getting extended into the subsequent clock cycle, therefore causing a change in the modulator's pulse response (e[n] and y[n]) at the

following sampling instant. As a result, the actual discrete-time domain loop transfer function is shifted away from the desired loop filter response. The order of actual noise transfer function is increased by one compared to the transfer function obtained from the ideal DAC pulse [40]. Excess loop delay is detrimental to the performance of high-order modulators. The maximum achievable SNR as well as the maximum stable amplitude will decrease with increasing loop delay, as shown in Figure 29.

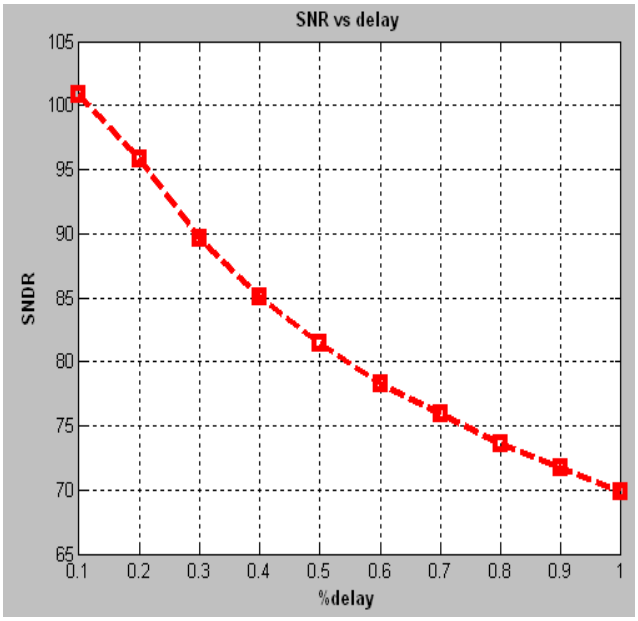


Figure 29: Peak SNDR with excess loop delay for the third order CT ΣΔ modulator.

Performance deterioration due to excess loop delay can be also eliminated by using return-to-zero DAC pulses or by the inclusion of half a clock cycle delay using the method outlined in [30]. In this design, the latter solution was used due to its simpler implementation and lower power consumption. The direct feedback coefficient k_{dfb} in Figure 30 is included so that a quantizer delay of up to half a

clock cycle ($T_s/2$, where T_s is the clock period) is tolerated without degradation in SNR [30].

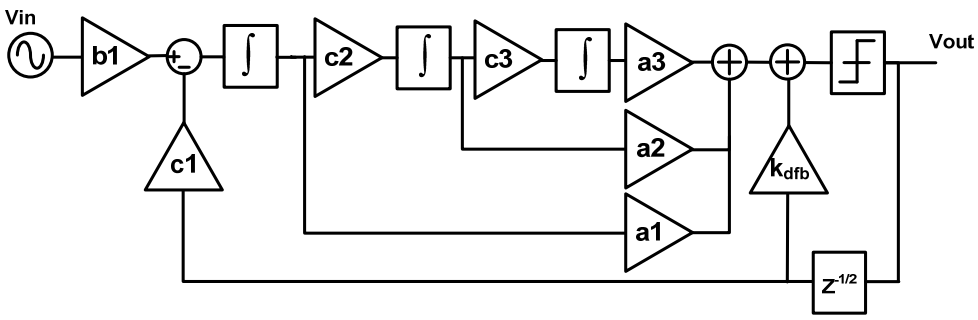


Figure 30: CT modulator with direct feedback coefficient k_{dfb} for excess loop delay compensation.

3.2.3 Clock Jitter

Clock jitter has a different influence over the performance of DT modulators compared to CT ΣΔ modulators. This is because jitter manifests as a source of error in different parts of the modulator. Figure 31 shows typical block diagrams of a DT and a CT ΣΔ modulator with respect to the influence of clock jitter [30], [22].

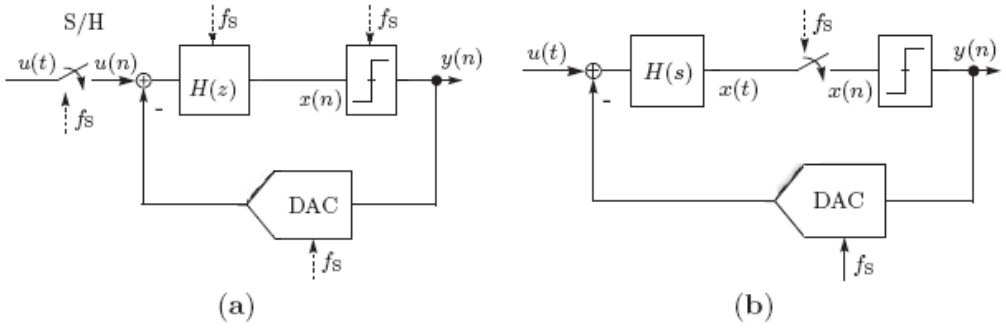


Figure 31: Jitter error sources in typical DT and CT ΣΔ modulators [40]. (a) DT modulator; (b) CT modulator.

In the case of a nonuniform sampling takes place, the decision of the quantizer in DT modulators remains correct to first-order approximation, because the integrators are designed to settle to a given accuracy within half the sampling period [22]. Therefore, the performance degradation due to clock jitter is primarily caused by errors in the front-end S/H circuit, where jitter caused sampling misalignment produces an equivalent amplitude error that degrades the SNR. Nevertheless, the introduced noise is uncritical for most applications [22],

[23], [30], [40], and the increase of the IBN due to clock jitter is proportional to OSR^{-3}.

Clock jitter affects CT modulators through two sources. First, the internal quantizer is prone to jitter affected sampling errors. But these errors enter the system at the point of maximum error suppression, i.e., at the quantizer, and are noise shaped and suppressed by the NTF. Second, clock jitter in CT implementations appears through errors resulting from the feedback DAC, this is because a CT ΣΔ modulator integrates the feedback waveform over time. Thus, a statistical variation of the feedback waveform results in a statistical integration error and consequently in increased noise.

The effect of jitter is modeled as an additive sequence at the input of a jitter-free modulator. For the case of NRZ feedback DACs, the error sequence is given by [30], [40].

$$e_j(n) = [y(n) - y(n-1)]\frac{\Delta T_s(n)}{T} \tag{34}$$

where $y(n)$ is the nth output sample of the modulator, T is the sampling time, and $\Delta T_s(n)$ is the clocking uncertainty of the nth edge of the feedback DAC. Since the difference between successive outputs of the modulator is smaller with a multibit quantizer, the sensitivity to clock jitter is reduced when compared with a single-bit design. The noise spectral density of clock jitter with NRZ DAC pulse is given by

$$P_n = \left(\frac{1}{OSR}\right)\left(\frac{\sigma_J}{T_s}\right)^2 P \tag{35}$$

where σ_J is the variance of the uncertainty in the DAC and $P_{\delta y}$ is the power of the quantizer's output samples difference ($y(n)$ - $y(n-1)$). Using the model in Figure 32, the behavioral model for the modulator is modified to include the clock jitter effect on the feedback DAC as shown in Figure 33.

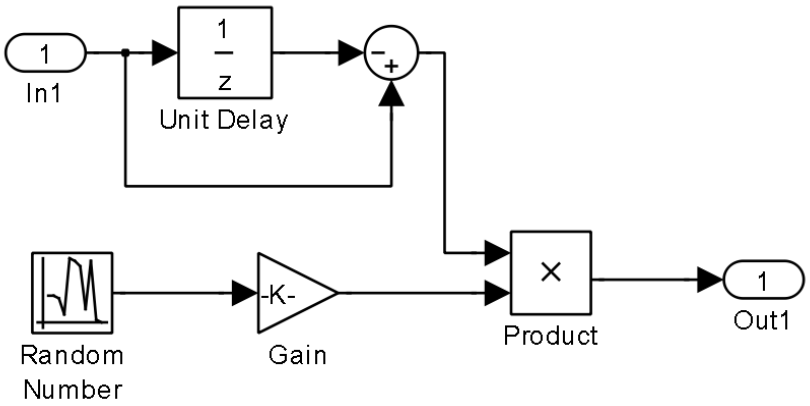


Figure 32: A simulink model for the expression in (21).

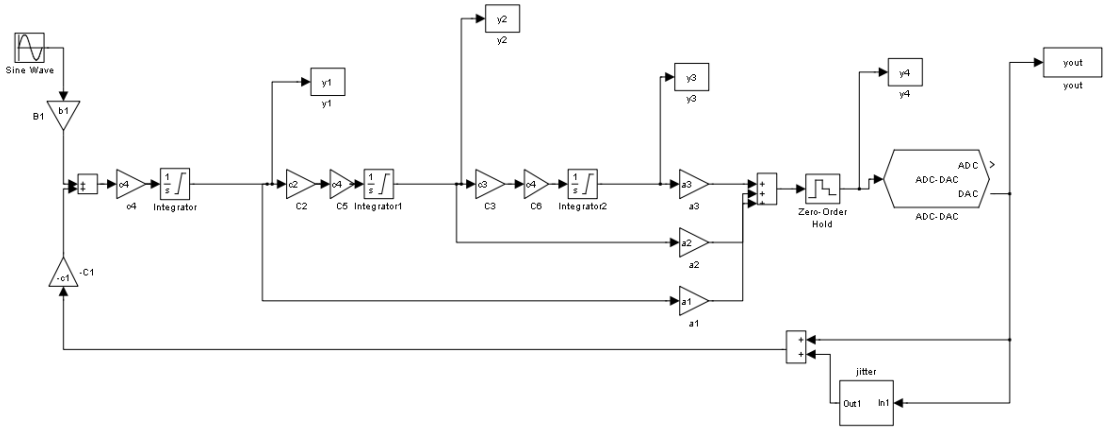


Figure 33: CT modulator behavioral model with clock jitter effect included in the DAC feedback.

Behavioral simulations (Figure 34) for this design reveal that in order to maintain 100 dB SNDR, clock jitter should be less than $5x10^{-5}$Ts which is equal to 53psec. This is a moderate requirement for the clock jitter. Analog Devices'

AD9540 clock generator and synthesizer exhibits a 100MHz clock having only 700fs rms of jitter. Nonetheless, attention should be given to clock distribution and layout of the clock on chip so that the added jitter is also minimized.

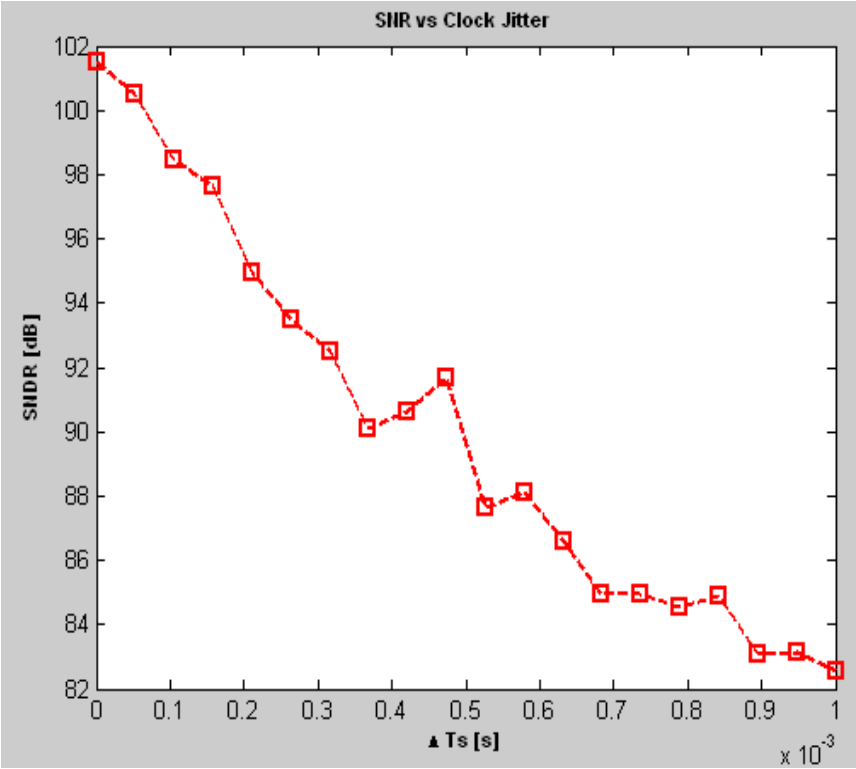


Figure 34: SNDR as function of DAC feedback clock jitter.

3.2.4 Sensitivity to RC-Product Variation

For DT modulators implemented using Switched Capacitors, the integrator coefficients are determined by the sampling clock frequency and the capacitor ratios, which can be made precise in a CMOS process. In contrast, loop filter coefficients in CT modulators are mapped into resistor-capacitor products, which vary largely over process and temperature. The absolute value of passive components can vary by as much as 10-20% from lot to lot, leading to combined

RC-product process variations exceeding 35% [34], [35], [36]. With the addition of wide changes in the ambient temperature, uncertainty in the RC time constants becomes even larger. The following equations model the RC-integrator transfer function when a variation (δ_{RC}) is present in the time constant.

$$I_i(s) = \frac{1}{s \cdot R_i C_i (1 + \delta_{RC})} \tag{36}$$

where

$$k_i^{-1} = R_i C_i (1 + \delta_{RC}) \cdot F \tag{37}$$

The transfer functions of an ideal continuous time integrator given by

$$I_i(s) = \frac{k_{i,i=1,2,3\ldots}}{sT_s^{`}} \tag{38}$$

where $T_s^{`}$ has a nominal value of $T_s$, the clock period of the system. If the integrator time constants $k_i/T_s^{`}$ deviate from their nominal values by δ_{RC}, the modulator's performance can degrade. Figure 35 shows the simulated SNR performance of the modulator with -3dB input signal (quantization noise only) versus the normalized *RC* time constant associated with the loop filter.

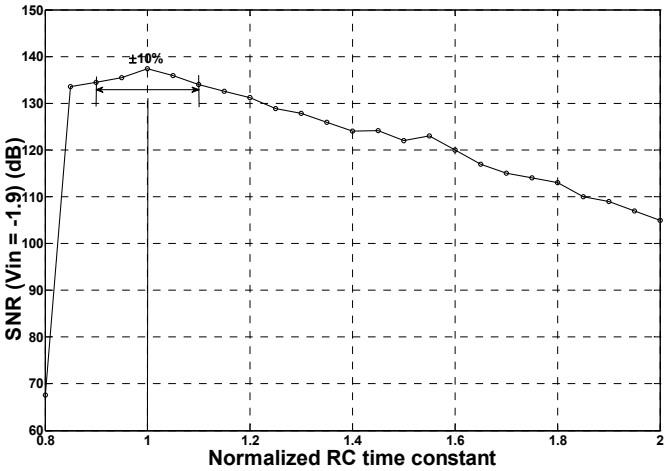


Figure 35: Simulated SNR of the ∑Δ modulator versus normalized RC time constant Ts`/ Ts.

The equivalent NTF is simulated with different values of RC. When the RC time constants decrease ($\delta_{RC} < 0$), then the in-band quantization noise decreases while the out-of-band gain increases (Figure 36). Therefore, a better SNDR is achieved at the expense of reduced maximum stable amplitude (MSA). The system becomes unstable when the normalized RC time constant decreases to approximately 0.88. If the RC time constant is increased beyond the nominal value ($\delta_{RC} > 0$), then the in-band quantization noise increases while the out-of-band gain decreases. This results in less efficient noise shaping, and hence a degraded SNR performance while MSA of the modulator is increased, resulting in better stability. Figure 35 also reveals that the time constant of the modulator can deviate as much as ±10% from its nominal value without degrading the signal-to-noise ratio (SNR) by more than 2 dB. Therefore, a ±10% variation in the integrator time constant is tolerable. The integrators in the loop filter, must be highly linear to maintain a 120 dB modulator SNDR [35]. Since CMOS technologies usually do not have tight enough control over absolute values of

resistors and capacitors, an *RC* time constant tuning circuit is needed to achieve assured performance without any in-factory trimming or calibration. A time constant tuning circuit also allows the correct value to be maintained over wide temperature swings.

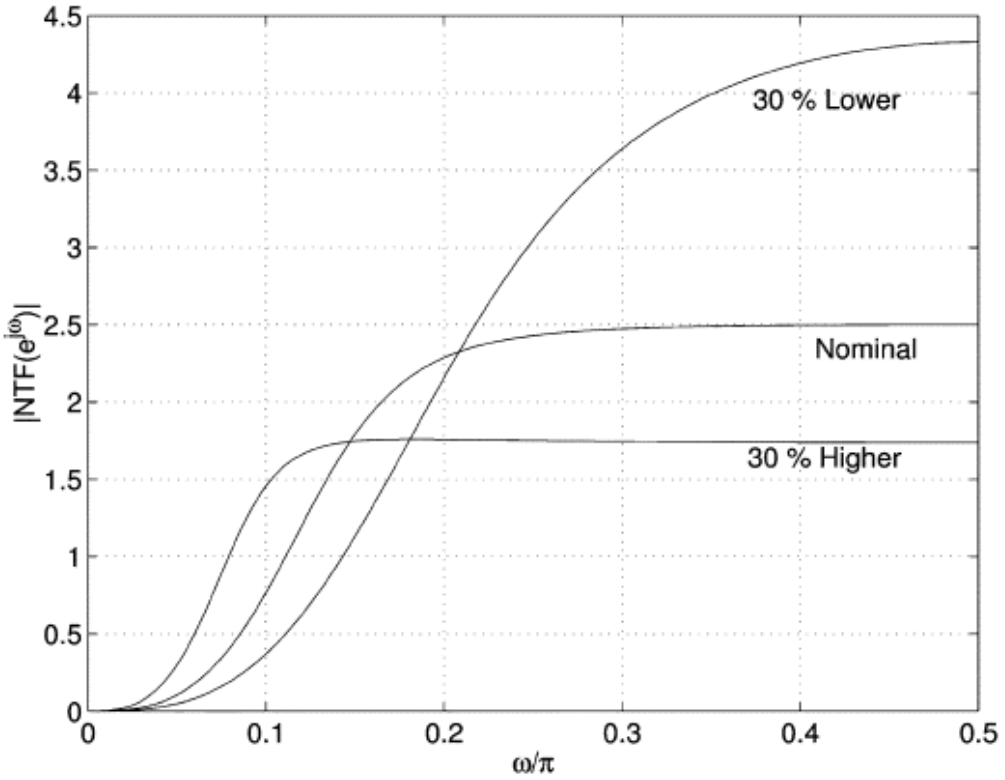


Figure 36: Noise transfer function for different RC product variations.

CHAPTER 4

RC TIME CONSTANT TUNING CIRCUIT

4.1 Introduction

As discussed in the previous chapter, extreme temperature operation brings the added requirement of ensuring that the loop filter response does not deviate by more than 10% from the desired filter response.

In this chapter, two RC time constant tuning engines are proposed for high linearity, continuous time active RC circuits, for use in harsh environments. The tuning circuits are used to maintain the required linearity of the 10 ksps 20 bit continuous time ΣΔ modulator. The proposed circuits which are based on master slave architecture automatically select on chip resistors to control RC time constants to an accuracy of ±5% in the first design, and 1% in the second. The tuning range, tuning accuracy and circuit non-idealities are analyzed theoretically. To verify the concept, an experimental chip was fabricated in.18µm 1.8V CMOS technology to test the first circuit. The tuning engine which occupies an area of .065mm^2 consists of only an integrator, a comparator and a shift register. It can achieve a signal to noise and distortion ratio (SNDR) greater than 120dB over a ±40% tuning range. The second circuit addresses the design limitations of the first design and offers greater tuning accuracy, reduced complexity and smaller die area.

4.2 Background

There are two possible methods to tune RC time constants; active and passive components tuning. Active tuning generally changes the transconductance (g_m) in an operational transconductance amplifier (OTA) using a control voltage V_{ctrl}. Figure 37 shows two g_m tuning implementations.

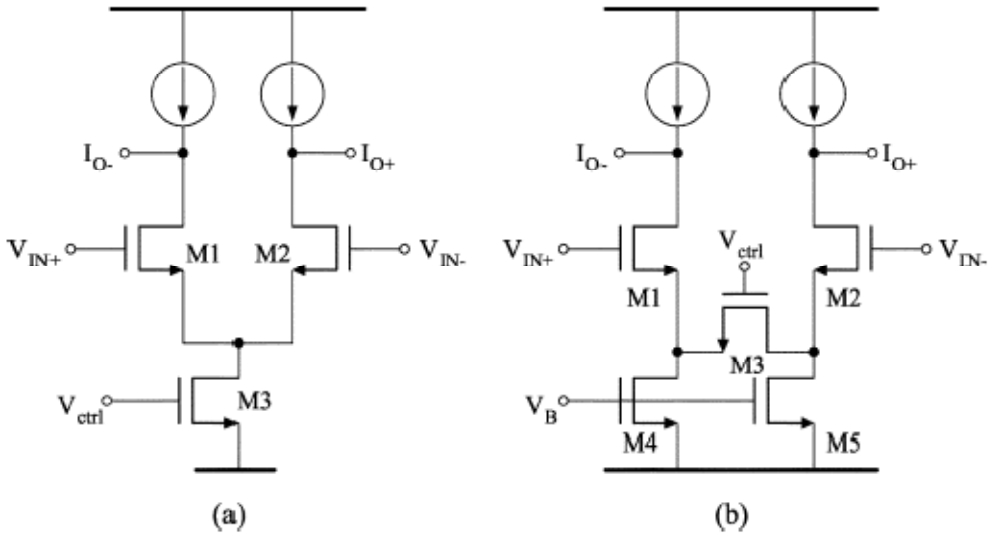


Figure 37: OTA gm tuning (a) via tail current source, and (b) via source degeneration resistance.

In Figure 37(a) [27], [28], tuning of gm is achieved by controlling the tail current source, which is governed by the gate voltage of M3. Figure 37(b) shows another popular gm tuning approach [27], [29]. The OTA small-signal transconductance is tuned by adjusting the gate voltage of transistor M3, which operates in the triode region therefore changing the degeneration factor. In both methods, g_m changes with the input signal common mode voltage, which limits the linearity of the OTA. In practical designs, g_m is chosen to achieve the required

linearity. However the tuning process varies g_m and its linear range, thereby degrading the linearity of the system [33]. Furthermore, the requirement to keep the transistors in their intended region of operation confines the OTA tuning range to a maximum of 30% of its nominal value [34]. Previously introduced active time constant tuning schemes were aimed at a tuning accuracy as high as 1% [37], [38], [39], [40], but involve complicated circuit structures such as phase-locked loops (PLLs) [26], [28], [32], [35], [39] necessary to obtain V_{ctrl}. Consequently, implementation cost is significantly increased. Some of these tuning circuits consume equal or more silicon area and power than the circuit-to-be-tuned [36].

Passive components tuning involves adjusting the capacitance or resistance within a set of discrete values by applying a digital control word [35]. Therefore, tuning accuracy is limited by the available resolution. Unlike active g_m tuning, passive tuning schemes do not degrade the linearity of the system because the change in the resistance or capacitance value does not change the operating points of the transistors.

Since only a 10% tuning accuracy is required for our application, degradation in linearity, added circuit complexity and power consumption resulting from g_m tuning become unjustifiable. Moreover, we require 40% tuning range. Unlike active tuning, the tuning range of the resistance value is limited only by the number of bits in the control word rather than the operating region of the transistors. A larger tuning range can be achieved by adding more bits in the control word if necessary, albeit at an increasing cost in silicon area. Therefore a

passive resistance tuning scheme for the active-RC integrators of the loop filter is adopted. The concept of the resistor tuning is illustrated in Figure 38.

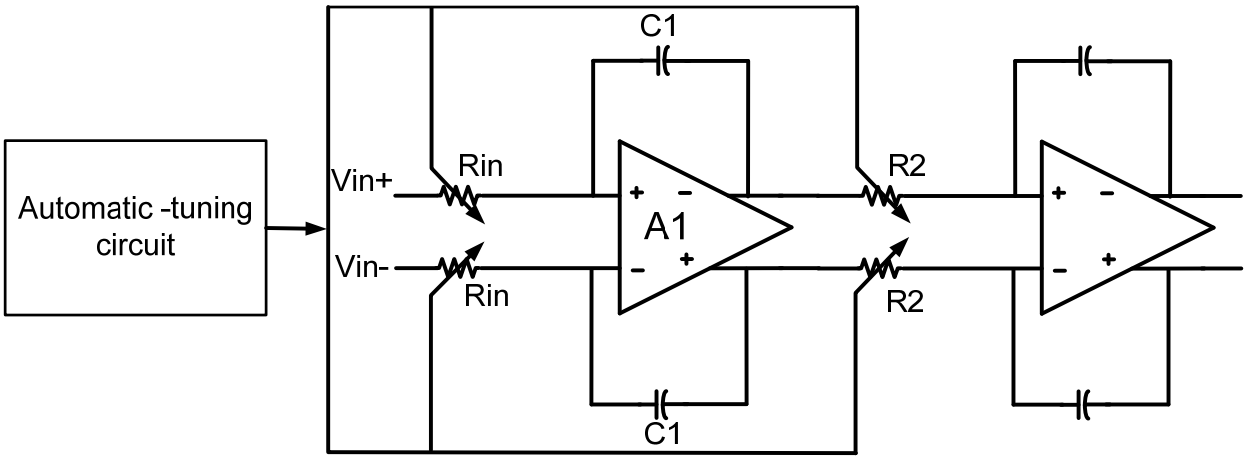


Figure 38: Active-RC integrator with discrete tuning approach (resistor tuning).

4.3 Prior Work on Tuning Circuits

Several methods for the tuning of on chip RC time constants have been reported in literature and patents. These vary with respect to accuracy, reliance on precision components and references, implementation complexity and power consumption.

4.3.1 Current Integrator Capacitive Bank Tuning

In this configuration [35], a fixed current source is used to charge a capacitive bank. The voltage at node V_O (Figure 39) is a function of the control word and integration time T which is held fixed. In order to tune the capacitive bank, V_O is compared to a certain voltage VREF2. The control logic decides in which direction the capacitive bank should be adjusted until V_O (T) falls below

VREF2. The scheme has from multiple drawbacks. These include the use of a fixed reference voltage to achieve the desired time constant value as well as the precondition that this reference voltage be held constant during the tuning period. This means that such a scheme would provide different results at different temperatures. Also, $V_O(T)$ is a function of the supply voltage Vdd, therefore, any fluctuations on the power lines will directly impact the tuning operation. Additionally, in order to insure that this tuning scheme settles to the desired design value, an accurate external R_{REF} is required.

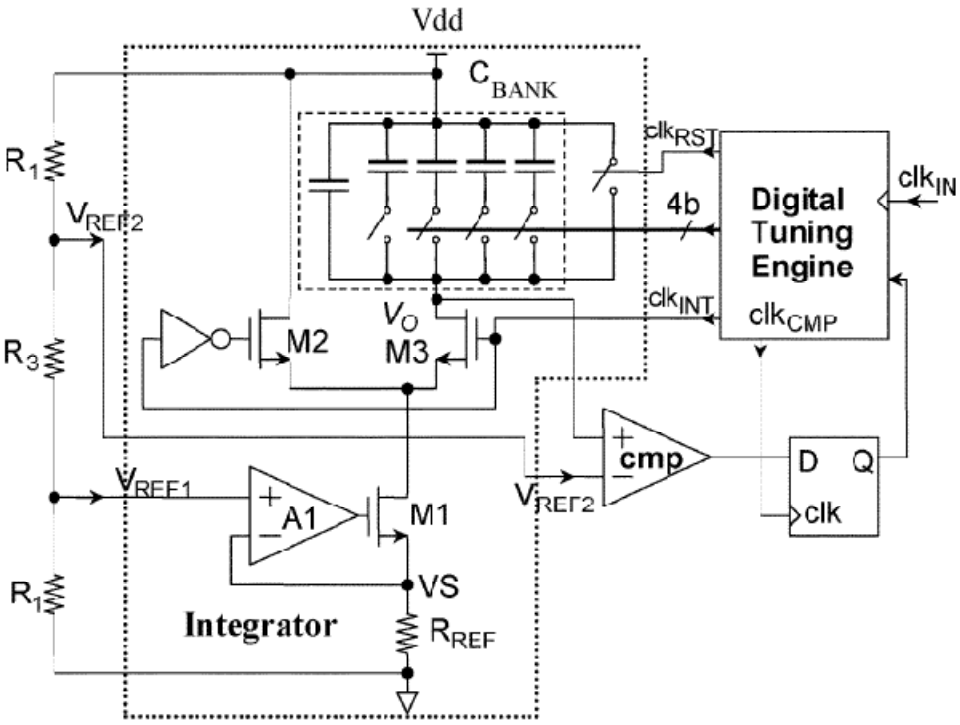


Figure 39: Capacitive tuning architecture [35].

4.3.2 Resistive Ladder tuning Using Digital DLL

Figure 40 shows the digital DLL tuning architecture [36]. In this scheme, a reference clock is generated using an on chip DLL and passed through a reference filter composed of a resistive ladder and a capacitor. The output signal VOUT, is delayed in accordance to the drift in resistor and capacitor values of the filter. VOUT is digitized using the comparator, which uses a reference voltage Vref. For Vref = .5VDD, the comparator output D is delayed by T1 which is directly proportional to R_{ref} $C_{ref.}$. The latch receives a reference LATCH CLK which is preselected to match the desired time constant. Adjustment of the resistor bank is based on the temporal relation of D and LATCH CLK.

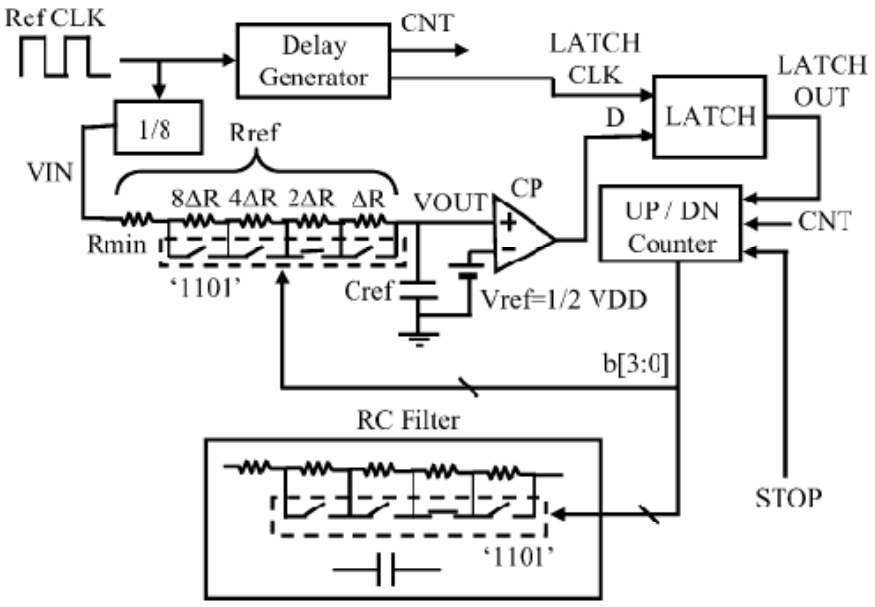


Figure 40: DLL RC tuning architecture.

This scheme renders its self unfitting for operation in a wide temperature environment because it relays directly on the reference voltage being held at a

constant value, in addition to the generation of a reference clock signal. The delay generator used in the circuit will also experience drift in the delay time with temperature, albeit minimal in value.

4.3.3 Current Reference Capacitive Bank Tuning

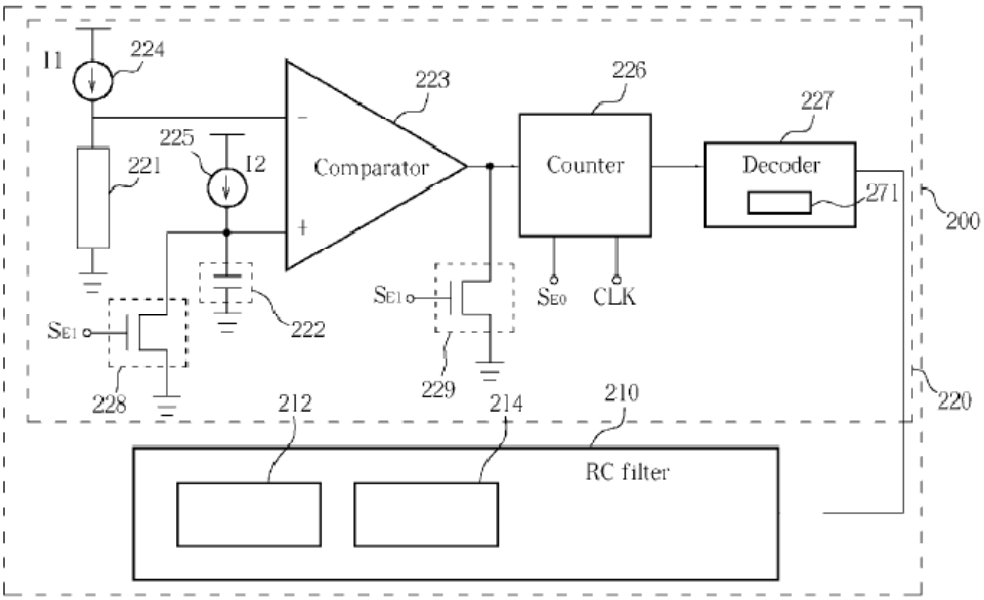


Figure 41: Current reference capacitive bank tuning [37].

In this tuning architecture [37], a capacitive bank is tuned by comparing the charging times of an accurate external reference resistor and the capacitor bank using on chip current references (Figure 41). The capacitor is charged until a stop signal is sent to the counter when the result of the comparison conforms to a predetermined rule. The decoder then decides which number of capacitors should be utilized by the RC filter according to the number of the clock cycles received by the counter.

The main drawbacks of the scheme are the use of precision external components like the reference resistor and its use of current references which should remain steady and stable during the tuning process and across all temperatures. If the current references drift with temperature and process mismatch, the result of the tuning process will be different; hence this scheme is not useful for operation in a wide temperature environment.

4.3.4 Two Step, RC Tuning

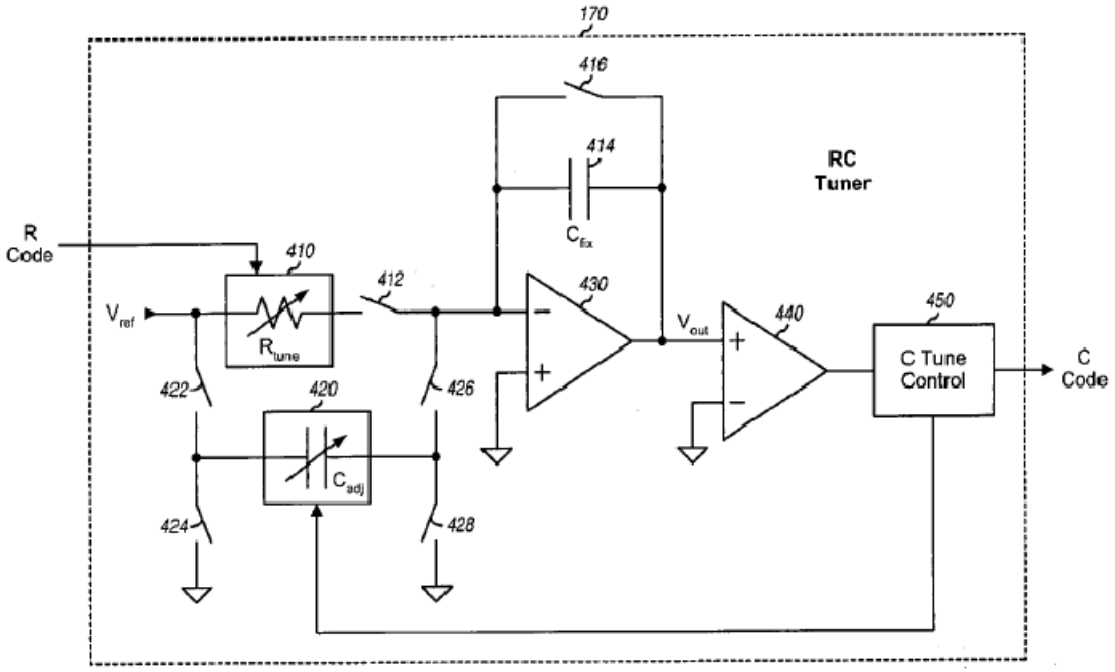


Figure 42: Two step RC tuning scheme [38].

This architecture (Figure 42) involves tuning of both resistive and capacitive banks separately [38]. First, the resistive bank is tuned by passing a current through an external resistor and passing a current through an adjustable

resistor. Voltages on the external and adjustable resistors are compared and the adjustable resistor is varied based on the comparison in order to obtain a tuned resistor.

Second, the tuned resistor is used in an RC integrator arrangement which includes capacitor C_{fix} to integrate Vref for a predetermined time. Afterwards, the charge on C_{fix} is discharged via C_{adj} during M clock cycles. The tuning control adjusts the capacitive bank based on the duration required to discharge C_{fix} completely.

This arrangement relies on having a fixed reference voltage and precision external resistor to carry out the tuning operation; therefore it is not suitable for our purposes.

4.4 PROPOSED SYSTEM ARCHITECTURE

In this section, we describe the proposed system's principal of operation and system components at the block level. Next section will introduce the schematic details for these components.

4.4.1 Principle of Operation

A single ended implementation of the proposed tuning architecture is shown in Figure 43. An identical resistor bank to the one used in the main circuit is adopted in the tuning circuit. The desired control word is determined by a zero crossing detector formed by the subtractor-integrator A1, comparator, and the

digital tuning engine. The N-bit control word is then applied to the resistor bank of the circuit-to-be-tuned.

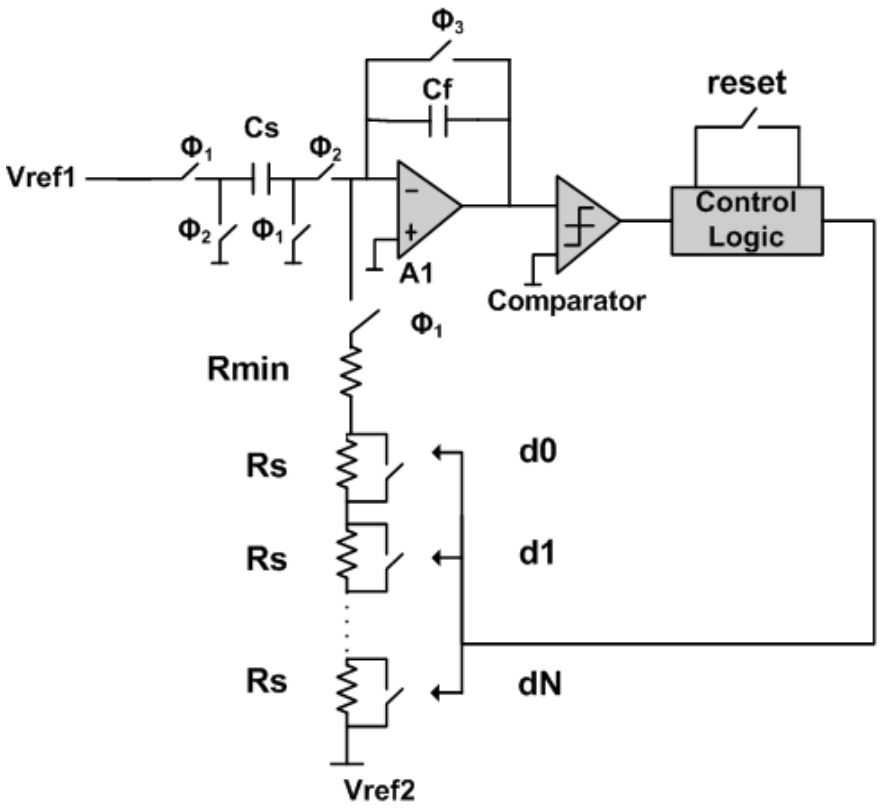


Figure 43: A single ended version of the proposed tuning architecture.

The programmable resistor bank in Figure 43 can be implemented either as binary weighted ladder or decimal ladder as shown in Figure 44.

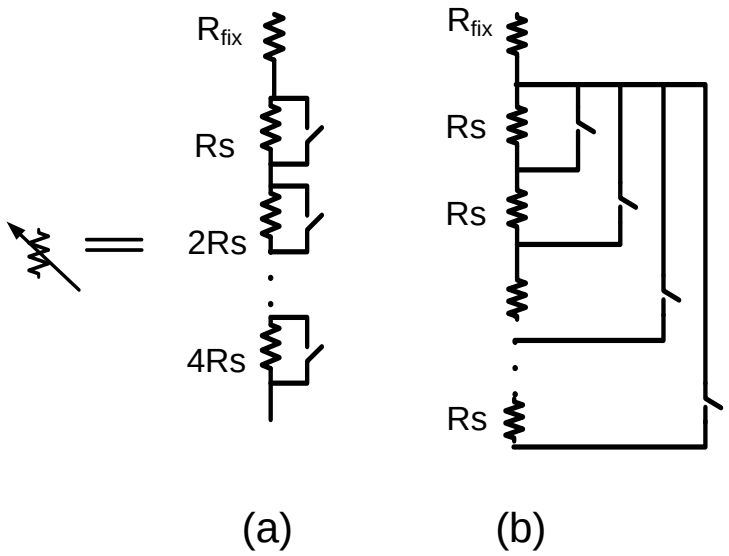


Figure 44: Tunable resistor implemented as binary weighted ladder (a) and decimal ladder (b).

Each step resistor R_s can be connected or disconnected to the amplifier by shorting/opening its corresponding switch accordingly. The resistance of the resistor bank R_{BANK} is determined by a digital control word. It can be tuned to a set of discrete values. For the binary weighted resistive ladder, R_{BANK} is given by

$$R_{BANK} = R_{fix} + R_s \sum_{i=0}^{N-1} 2^i b_i + R_{sw} \sum_{i=0}^{N-1} \overline{b_i}, b_i \in \{0,1\} \tag{39}$$

For a decimal ladder R_{BANK} is given by

$$R_{BANK} = R_{fix} + R_s \sum_{i=0}^{N-1} b_i + R_{sw} \sum_{i=0}^{N-1} \overline{b_i}, b_i \in \{0,1\} \tag{40}$$

where $[b_{N-1}\ldots b_1 b_0]$ is the N-bit control word, and R_{sw} is the resistance of the switch in the on state. Several methods for obtaining the control word have been reported in the literature, such as using a ramp generator [32], [34] or counter [36].

At the beginning of the tuning operation, the resistive ladder switches are open and ladder resistance (R_L) is at its maximum value. Operation of the tuning circuit begins with Φ_1. At the end of this phase, sampling capacitor C_s is charged to V_{ref1}. The voltage at the output of the opamp V_{out} is given by

$$Vout_{\Phi 1} = V_{ref\,2}\frac{T_{\Phi 1}}{2R_L C_{fb}} \tag{41}$$

where $T_{\Phi 1}$ is the duration of Φ_1, and C_{fb} is the feedback capacitor. On Φ_2, the voltage on C_{fb} is subtracted from the voltage on C_s, and V_{out} is then given by

$$Vout_{\Phi 2} = V_{ref\,1}\frac{C_s}{C_{fb}} - V_{ref\,2}\frac{T_{\Phi 1}}{2R_L C_{fb}} \tag{42}$$

An early version of Φ_3 triggers the comparison between $V_{out\Phi 2}$ and ground followed by Φ_3 which resets the comparator. Digital control increments the control word since the stop criterion is not met. The tuning process reverts to Φ_1, and successive control words that close switches in the resistor ladder one bit at a time are generated until $V_{ref2}T_{\Phi 1}/(2R_{eq}C_{fb})$ becomes bigger than $V_{ref1}C_s/C_{fb}$ and a reversal in the polarity of V_{out} occurs. Assuming V_{ref1} is equal to V_{ref2}, for the case that $V_{out} = 0$

$$R_L = \frac{T_{\Phi 1}}{2C_s} \tag{43}$$

Since the resistive ladder has discrete steps, V_{out} cannot exactly become zero. Therefore, the tuning operation is completed once a zero crossing has been detected. In the circuit-to-be-tuned, the capacitance values in each of the integrators are designed to keep the resistance values the same or integer multiple among the stages [22], [35]. The uniform resistance in each stage ensures a better matching performance and allows the same digital control word to be applied throughout the circuit-to-be-tuned without the need to tune each time constant individually, therefore saving silicon area. Once the resistance in the tuning circuit is tuned to the desired value, the tuning circuitry is disabled to reduce power consumption [31], [35]. The control word is latched and applied to the resistor banks in the loop filter. The tuning procedure can be re-activated when a recalibration permit is granted to compensate the possible time constant drift caused by temperature variation or aging. Since the same resistive ladder and unit capacitance are used in the tuning circuit as well as the circuit being tuned. A good RC time constant matching property between the master and slave circuits is guaranteed.

4.4.2 Design Details

In this section, the implementation of a fully differential version of the proposed tuning circuit is presented. Figure 45 demonstrates the tuning circuit including the decimal resistive ladder-to-be-tuned, the subtractor-integrator that generates the output voltage difference, the comparator and the logic circuit to

decide the control word. Figure 46 depicts the control clock diagram and integrator output waveform as a tuning operation proceeds.

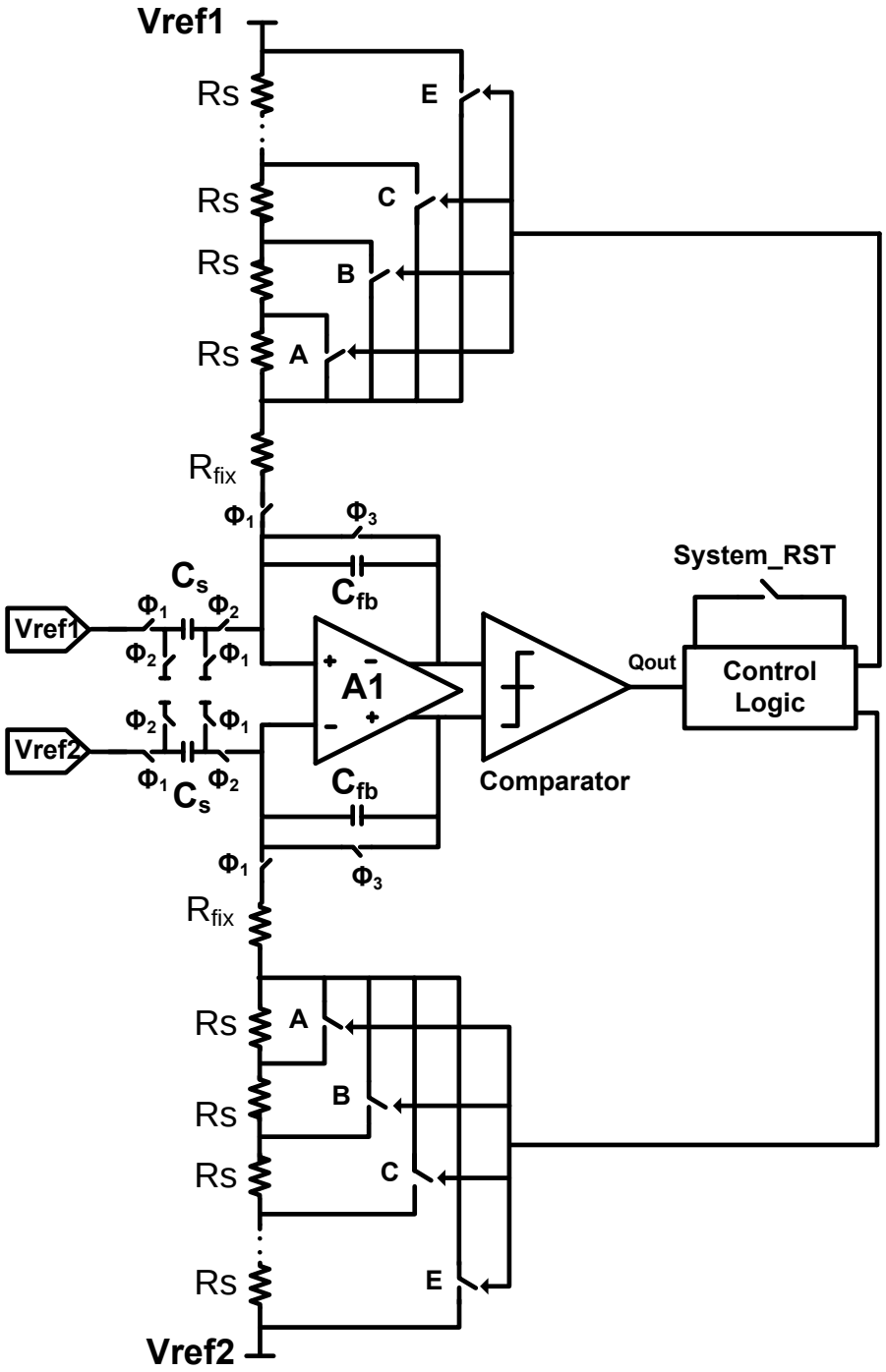


Figure 45: The Proposed tuning circuit including the decimal resistive ladder.

Figure 46 depicts the control clock diagram and integrator output waveform as a tuning operation proceeds.

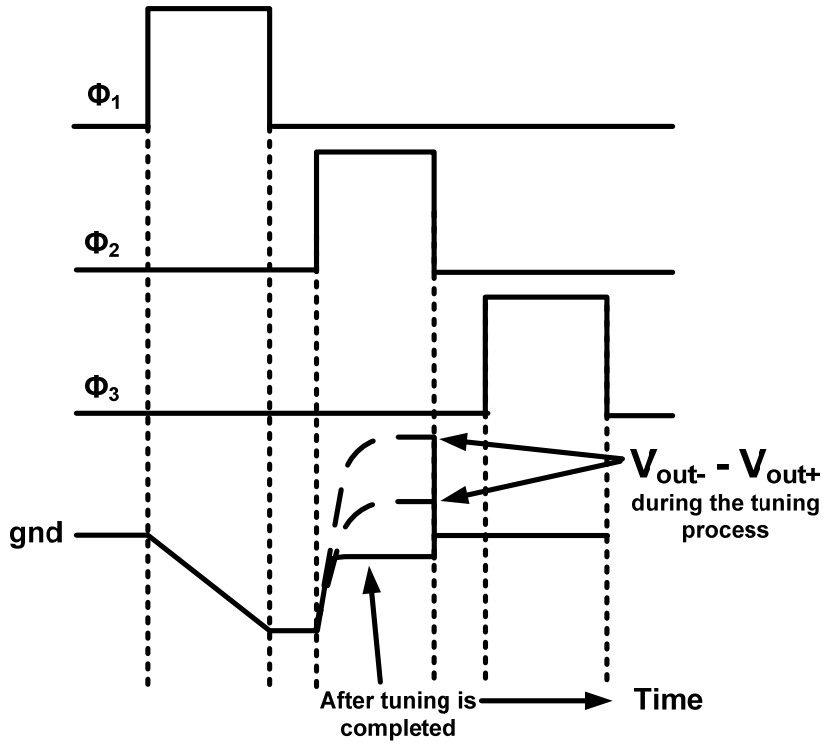


Figure 46: Timing diagram demonstrating the three phase clock along with the integrator/subtractor output waveform.

4.4.2.1 Resistive Ladder

Equation (40) shows the resistance of an N-bit binary-weighted resistive ladder with a fixed resistance R_{fix} and step resistance R_s. R_s is chosen as a compromise between area and good matching and R_{on} of the CMOS switch parallel to it. N and R_{fix} are determined by the nominal value and the

programmable range. Given the nominal value R_{nom} and a tuning range of (*1-a%,1+b%*) around the nominal value, we can have

$$R_{fix} = R_{nom} + R_s(1-a\%), N \geq \log_2\left[\frac{(b\%+a\%)R_{nom}}{R_s}\right] \tag{44}$$

$$R_{fix} = R_{nom} + R_s(1-a\%), N \geq \frac{R_{nom}(b\%+a\%)}{R_s} \tag{45}$$

Where equation (44) and equation (45) are for binary weighted and decimal ladder configurations respectively. The programmable resistor ladders must include the desired tuning value for the maximum process variations that occur during the fabrication over the entire range of ambient temperatures. The total worst-case deviation of the integrated RC time constant can be calculated from the values of component tolerances (±20% and ±15% for resistors and capacitors, respectively) and their temperature dependence (1000 ppm/ °C and 25 ppm/ °C, respectively). Using a nominal temperature of 0°C and an operating temperature range of -200°C-120°C, the worst-case deviation in time-constant which must be corrected by tuning is -50% to +40%. Therefore, a 4 bit ladder is required for a binary weighted ladder. For the decimal ladder, a smaller number or resistors than the power of 2 can be used to meet the design range.

4.4.2.2 Integrator

Opamp A1 and capacitors C_s and C_{fb} in Figure 45 form a discrete time integrator while the resistive ladder with capacitor C_{fb} form a continuous time

integrator. Opamp A1 in Figure 45 is a conventional single stage folded cascode op-amp, as shown in Figure 47. Over 80 dB dc gain is achieved to suppress the accuracy degradation caused by the non-ideality in the circuit.

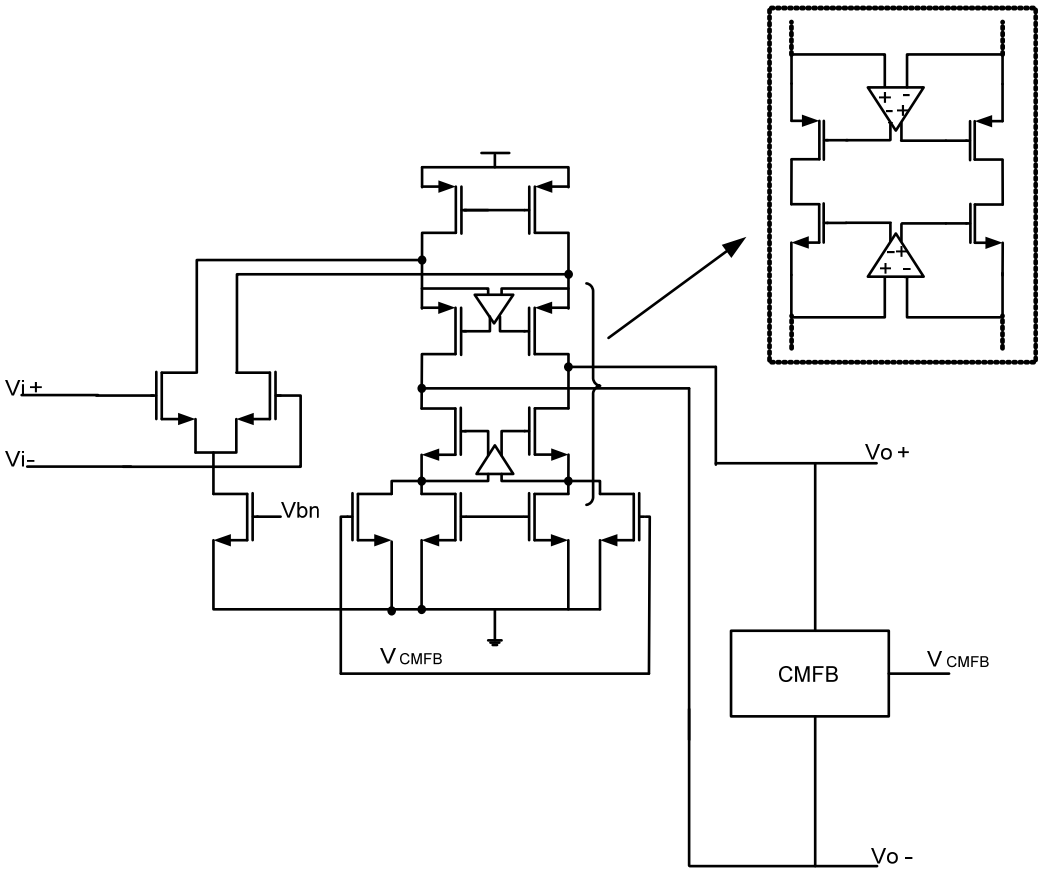


Figure 47: Schematic diagram of the operational amplifier used in the tuning circuit's integrator/subtractor stage.

4.4.2.3 Comparator

The comparator following opmap A1 is used to provide a 1-bit flag to the tuning logic to decide the control word. The comparator contains 3 stages: pre-amplifier, latch comparator and RS latch. The RS latch is added to the comparator to drive the following digital circuit. Inverters can substitute the RS latch.

Figure 48 depicts the circuit architecture. Since the tuning circuit operates at a low frequency, the speed requirement of the comparator is not a major concern.

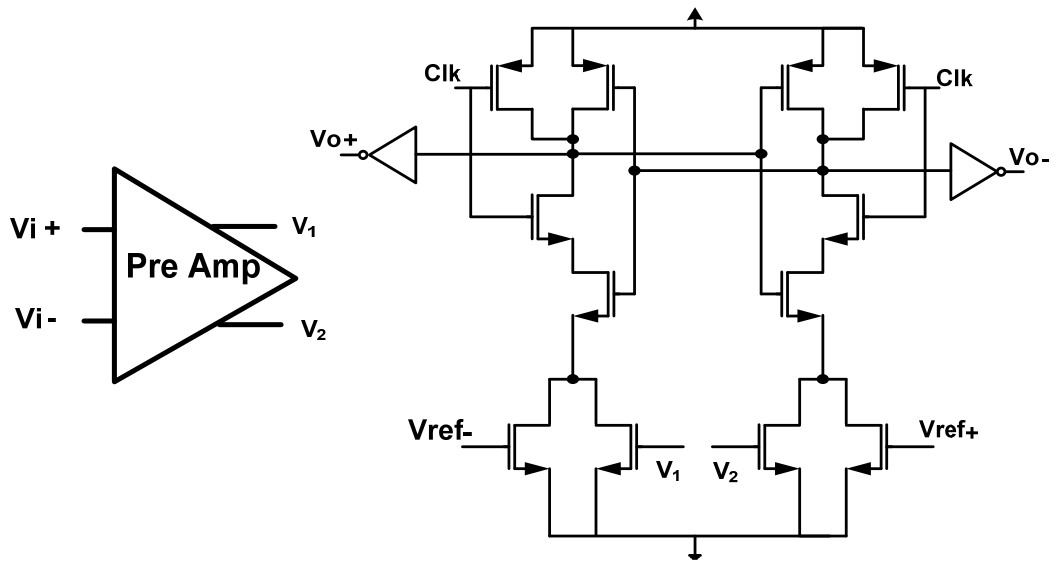


Figure 48: Latched comparator used in the tuning circuit and ΣΔ modulator.

4.4.2.4 Clock and Tuning Logic

The state chart of the digital tuning logic is shown in Figure 49(a). On power up or when a re-calibration signal is given, the tuning logic is activated. At the beginning of a tuning operation, the pre-set control word is reset to all zeros, opening all the switches in the ladder. As the tuning operation proceeds, the value of the control word is incremented if the comparator output is positive. This process continues until the stop criterion is met (comparator output is negative). Figure 49(b) shows the circuit block diagram of the tuning logic. Depending on the particular choice of the resistive ladder, the core of the digital tuning logic can

either be a full adder which increments the control word based on the comparator decision for the case of the binary ladder or it can be implemented with a shift register for the decimal ladder.

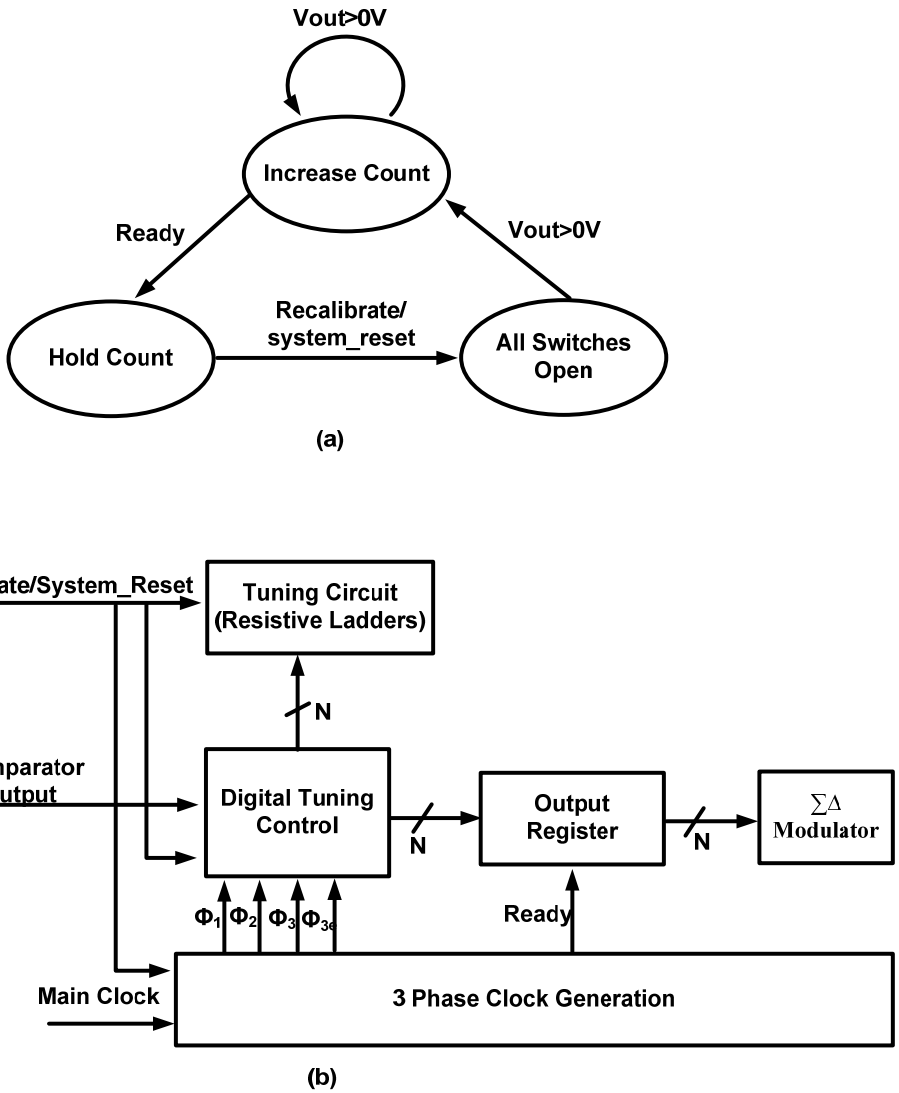


Figure 49: Tuning logic (a) state chart (b) block diagram.

The tuning control block in Figure 45 can be implemented with a simple shift register that is triggered by Φ_3 as shown in Figure 50. Once the control block's

Ready signal is high, the output registers are updated and the results are latched to the ladder in the slave circuit. The state of the output registers remains the same until a new tuning request has been made and a new *Ready* signal generated.

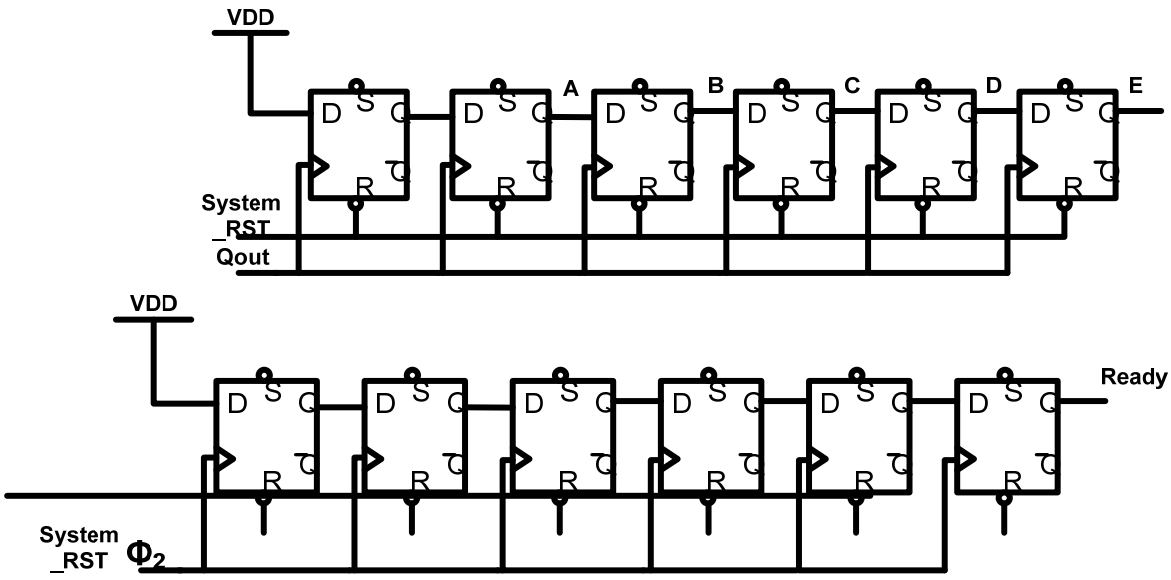


Figure 50: Tuning logic control unit.

The tuning circuit should not be sensitive to the duty cycle of the reference clock. Therefore a three phase clock that is only sensitive to the reference clock period and not the duty cycle is needed. The clock generation circuit is illustrated in Figure 51. The input latches in the circuit are clocked with the rising edge of the clock, therefore, only changes in the reference clock's period can affect the durations of $T_{\Phi i, i=1,2,3}$.

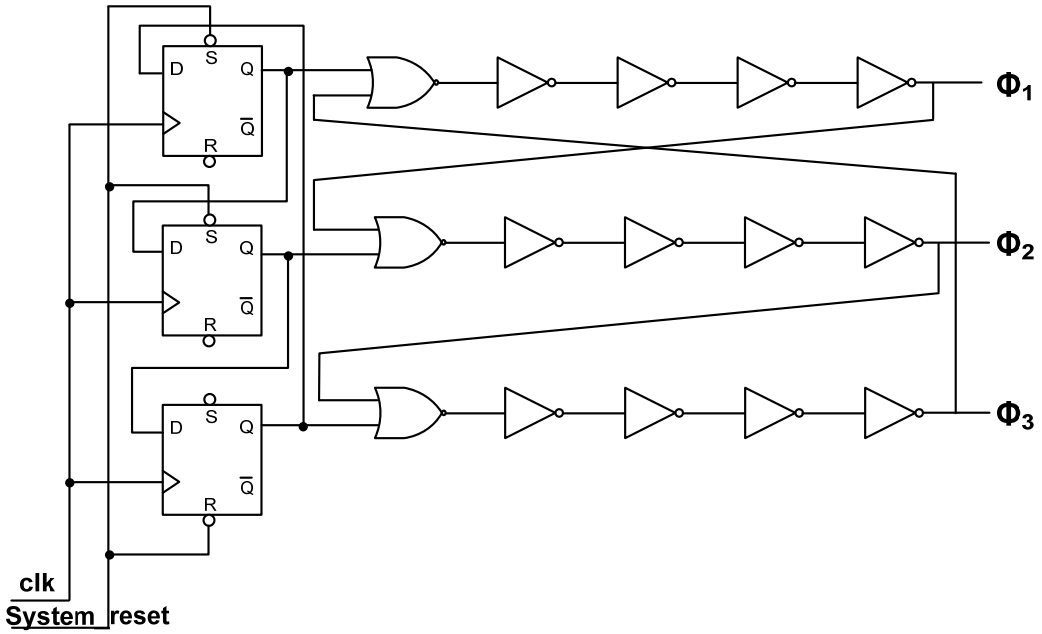


Figure 51: Three phase clock generation circuit.

4.4.3 Circuit Non-Idealities

The accuracy achieved by the proposed tuning circuit is dominated by the quantization error due to the discrete approach, and comparator offset. Measures were taken in the circuit implementation to meet the accuracy requirement even in the worst case. The following are the main non-idealities.

4.4.3.1 Quantization Error of the Ladder

The maximum relative *RC* time constant quantization error for an *RC* tuning range from (*1-a %)* to *(1+b%*) is given by

for a binary weighted ladder

$$\varepsilon_Q = \pm \frac{b\% + a\%}{2^N (1 - a\%)} \tag{46}$$

for a decimal ladder

$$\varepsilon_Q = \pm \frac{b\% + a\%}{N(1 - a\%)} \tag{47}$$

To achieve the same accuracy using the decimal ladder, more resistors and switches are required.

4.3.3.2 Non-Ideality of the Active Switches

Wide CMOS switches were used in the ladders to minimize the switch resistance. The CMOS switches introduce nonlinear on-resistance (R_{on}) and parasitic capacitance (C_p) to the resistive ladder. These parasitic elements have a limiting effect on the frequency response and linearity of the circuits in which they are being used. The maximum degradation in frequency response occurs for the condition of all switches being closed. Following the derivation methodology in [32], the maximum corner frequency is given by

for the binary weighted ladder

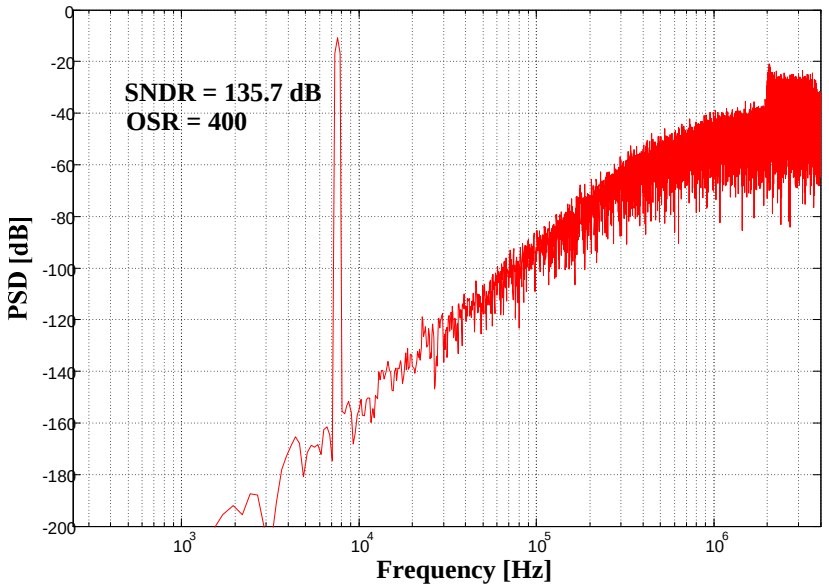
$$f_{co} = \frac{1}{2\pi N^2 2^{2N} \tau_{on}} \tag{48}$$

for decimal ladder

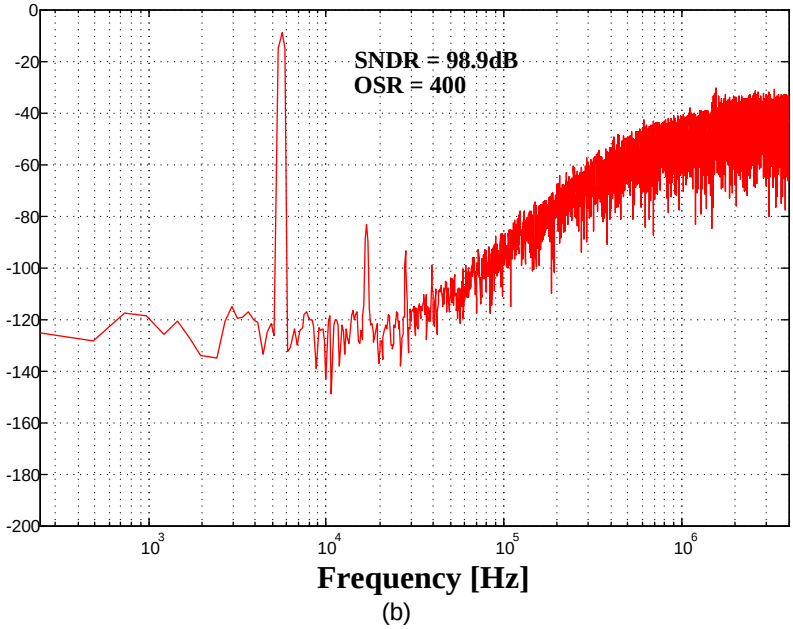
$$f_{co} = \frac{1}{2\pi N^2 \tau_{on}} \tag{49}$$

The nonlinearity of the switch resistances in the first integrator is of primary concern, because it leads to harmonic distortion at the output of the modulator and is not attenuated by the loop filter as is the case for the second and third integrators.

Figure 52 demonstrates the effect of switch nonlinearity on the overall performance of the modulator for an input signal of 600 mV. The advantage of using the decimal ladder is evident from these results as a higher corner frequency is possible and linearity is not compromised as result of increased switching elements.



(a)



(b)

Figure 52: Odd harmonics are observed in the simulated modulator output for the case of the binary weighted ladder (b) as compared to the decimal ladder (a).

4.3.3.3 Offset Voltages of the Amplifier and Comparator

The input referred offset of the amplifier A1 ($\nu_{iof,A1}$) and the input offset voltage of the comparator ($\nu_{iof,comp}$) can degrade the tuning accuracy if the sum of these offsets referred to the input of the comparator is high enough to cause the wrong decision at the output of the comparator during the final tuning step. Based on the expressions (44) - (47), (a = 50%, b= 40%, N = 3, Rs = 2.9kΩ) were chosen for our implementation. This allows for a design margin in excess of 100mV of total offset. Assuming that $\nu_{iof,A1}$ and $\nu_{iof,comp}$ are not correlated to each other, a value of 50mV for both can be tolerated.

4.3.3.4 Component Mismatches

Component mismatch may affect the tuning accuracy in two ways. First, in a fully differential implementation of the tuning circuit, mismatch between the R ladders and sampling and feedback capacitors of the opamp positive and negative terminals results in a deviation of the resultant voltage difference at the output of the opamp. Second, the mismatch between the ladder and capacitors in the tuning circuit and those in the integrators can also degrade tuning accuracy. Resistor matching can be improved by using the same unity resistor in the ladders and using layout techniques like common centroids. Capacitor matching is usually

as good as .1% with careful layout. For 10% tuning accuracy, component matching is not a concern.

4.4.4 Modified Tuning Circuit

The tuning engine and circuit implementation presented above provide an adequate solution to the time constant variability with temperature. However, the performance of the tuning engine can be improved by noting some observations related to the functionality circuit.

4.4.4.1 Performance Limitations of the First Tuning Circuit

The tuning engine and circuit implementation presented above provide an adequate solution to the time constant variability with temperature. However, two observations regarding its operation can be made that are utilized to improve its functionality.

First, from the analysis above, it is clear that the primary limitation on the tuning resolution of the circuit is due to the finite resolution of the resistive ladder. The lower limit of the ladder step size and therefore, resolution, is set by the opamp and comparator offset errors. Hence, the lowering or elimination of the offset of both opamp and comparator will allow the designer to increase the tuning resolution by decreasing the resistive ladder's step size.

The second observation is that due to the sequential operation of the tuning circuit, the opamp and comparator operate during certain clock phases and are idle in others. The opamp samples and carries out the continuous time

integration through the resistive ladder during Φ_1. During Φ_2, subtraction is carried out after which the opamp does nothing in Φ_3. As for the comparator, it is only active during Φ_3 and idle during Φ_1 and Φ_2. This observation is exploited to minimize power consumption and circuit complexity in the modified tuning engine.

4.4.4.2 Improved Architecture

The modified circuit is shown in Figure 53.

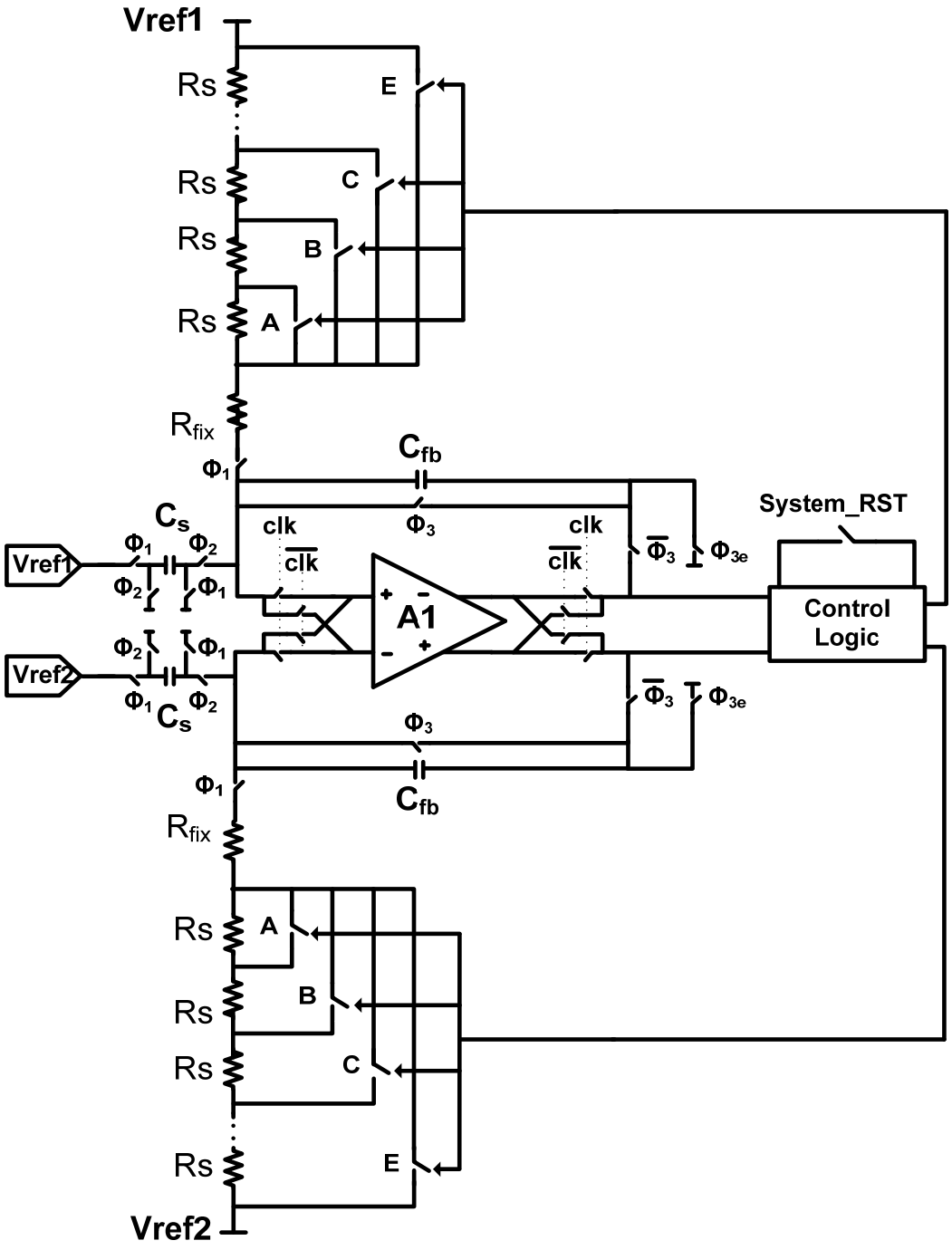


Figure 53: Improved tuning circuit.

In this circuit, opamp A1 is used to carry out integration, subtraction as well as comparison functions. This is done in the following way, during Φ_1, the reference voltages Vref1 and Vref2 are sampled on capacitors C_s, and C_{fb}. During Φ_2

subtraction occurs followed by a reversal of the residual voltage polarity across C_{fb} by connecting the bottom plate of the capacitor to ground in Φ_{3e} (early clock). The opamp in this phase is connected in open loop configuration and serves as a comparator. In addition, the offset of the opamp is eliminated throughout operation using chopper switches with chopping frequency (clk) of 6 MHz. Therefore the two critical performance observations made earlier are remedied. Additionally, fully differential operation in this circuit is not necessary, however, DC offset error generated from charge injection of the switches (sampling and chopper switches) would not be cancelled in a single ended implementation, hence, a fully differential operation results in complete elimination of the charge injection errors.

CHAPTER 5

TEST IC AND MEASUREMENT RESULTS

5.1 First Tuning Circuit Test IC

The tuning circuit was fabricated using the Jazz Semiconductor 0.18µm CMOS technology. It uses a supply voltage of 1.8 V. Figure 54 shows a die photo of the chip. The tuning circuit occupies 320µm*300µm. An on chip integrator was used to test the performance of the tuning circuit at run time. It includes tunable resistive ladders that are updated from the tuning circuit. As Figure 55(a) demonstrates, the slope of the integrator output increases with the progression of switches being turned on. Table 5 lists the values of this slope.

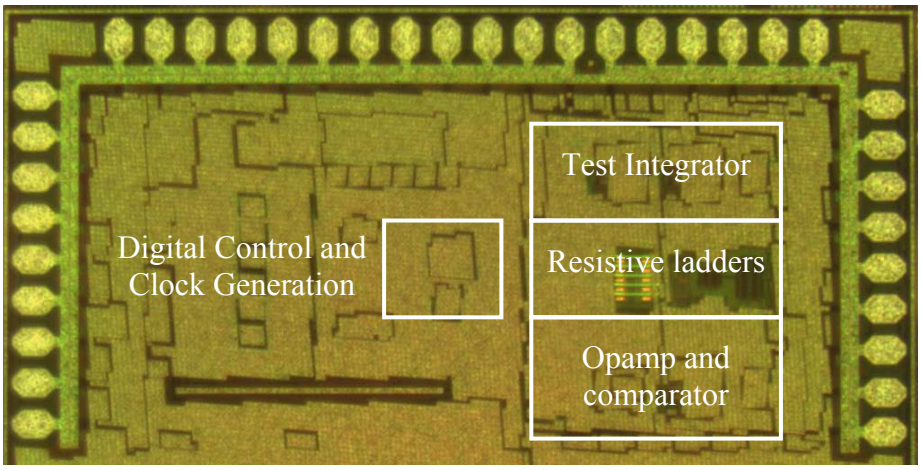


Figure 54: Tuning circuit test ic die photo.

The equivalent resistance value acquired by the tuning circuit (Req) versus $T_{\Phi 1}$ across a 260°C temperature range is presented in Figure 56 measured R_{eq} versus $T_{\Phi 1}$ at different temperatures. As the temperature increases/decreases, the resistance of the ladder decreases/increases accordingly. The tuning engine selects

the most appropriate resistive step, ensuring that the acquired resistance falls within the design margin irrespective of the temperature. Figure 57 demonstrates this for a desired resistance value of 27kΩ. $R_{acquired}$, is the resistance achieved by the tuning circuit.

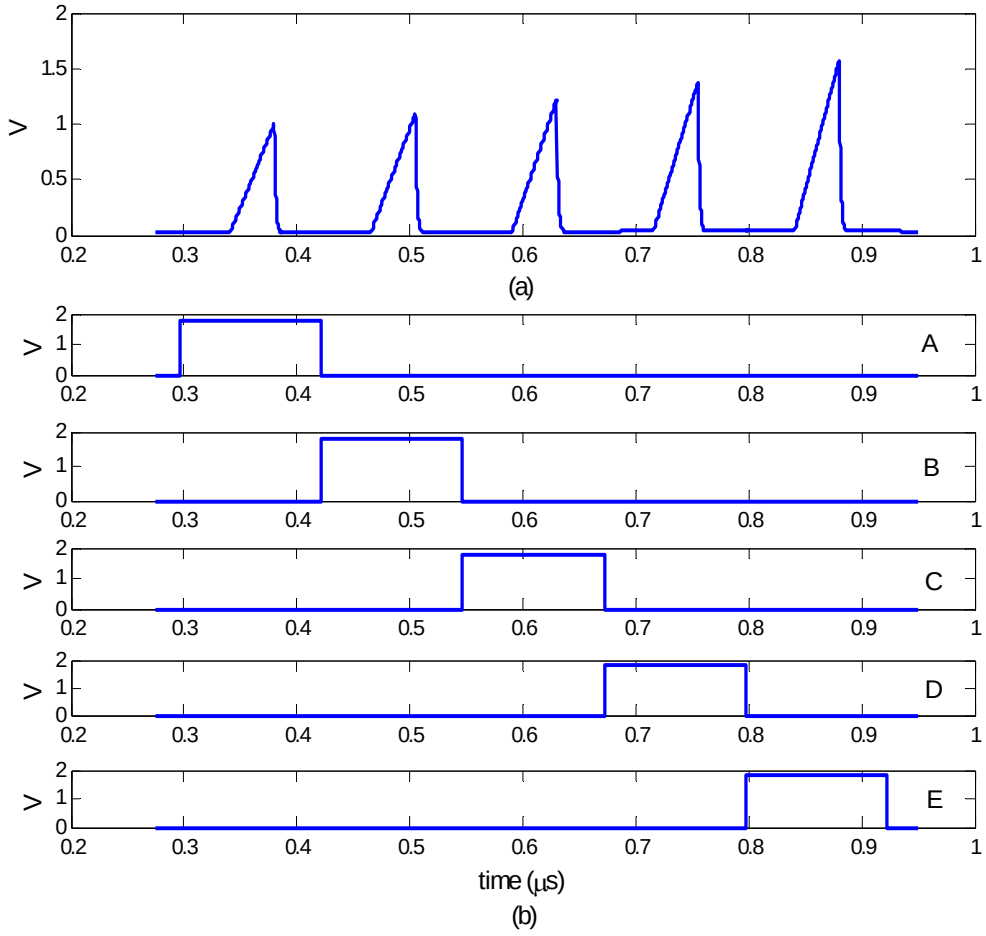


Figure 55: Transient response of the tuning circuit. (a) Transient response of the test integrator output. (b) Changes in the resistive bank control word.

Every measurement was reproduced using different reference voltages ranging from .1V to .8V differential. No differences in the code transitions were observed proving that the proposed circuit is independent of the reference voltage variations.

Table 5: Test integrator slope for different test codes generated by the tuning engine.

Code	Measured Slope x 10^7	Expected Slope x 10^7
A	1.56	1.557
B	1.71	1.712
C	1.90	1.901
D	2.14	2.139
E	2.44	2.439

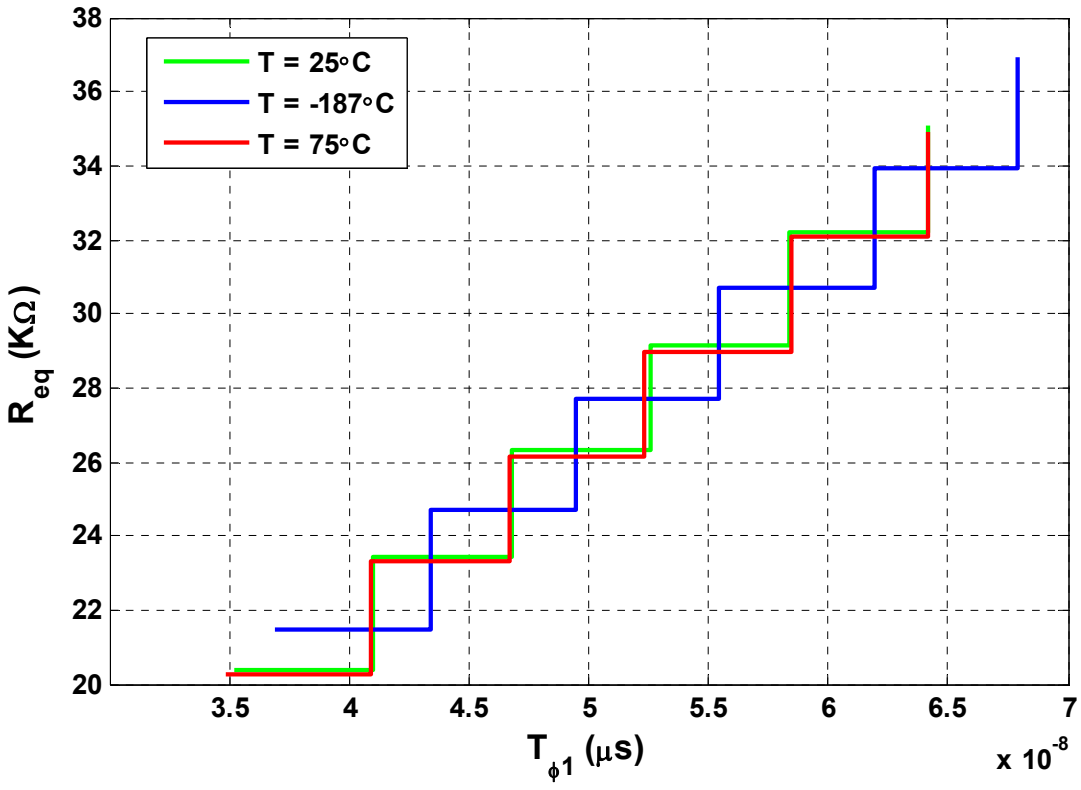


Figure 56: Measured Req versus $T_{\Phi 1}$ at different temperatures.

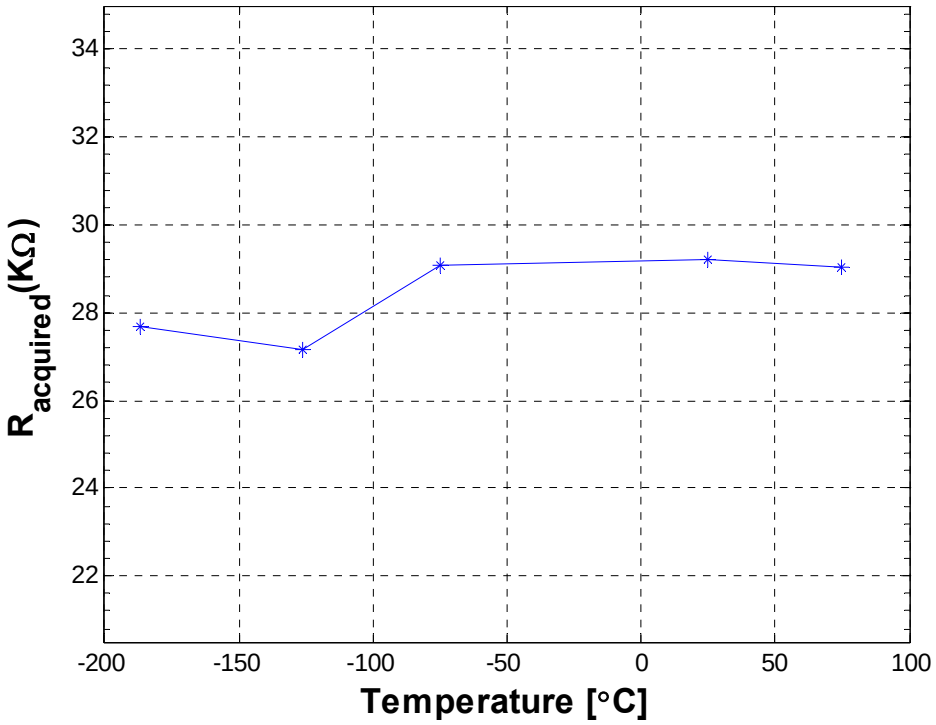


Figure 57: Measured $R_{acquired}$ versus temperatures.

In total, four test ICs were characterized across a wide range of temperatures and reference clock frequencies. A scatter plot of the acquired resistance by the tuning engine ($R_{acquired}$) is presented in Figure 58. The acquired resistance value has been normalized to the target resistance value (R_{target}). It is clear from this figure that all acquired measurements fall within the accuracy ±5% range as intended by the design.

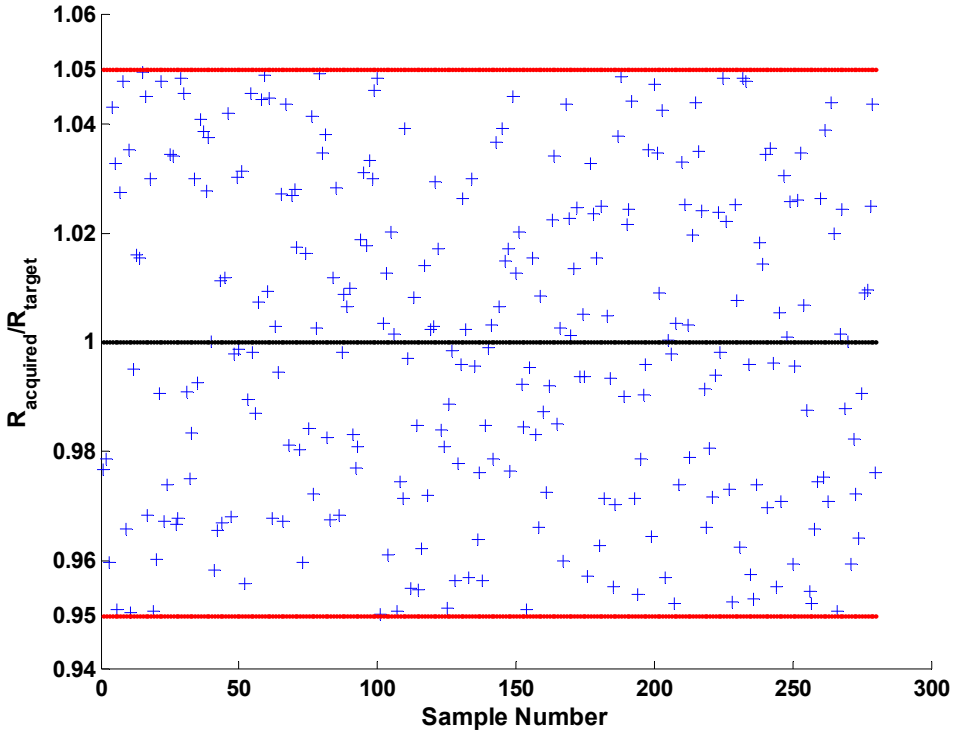


Figure 58: A scatter plot of the acquired resistance $R_{acquired}$ by the tuning engine after normalization to the target resistance R_{target}.

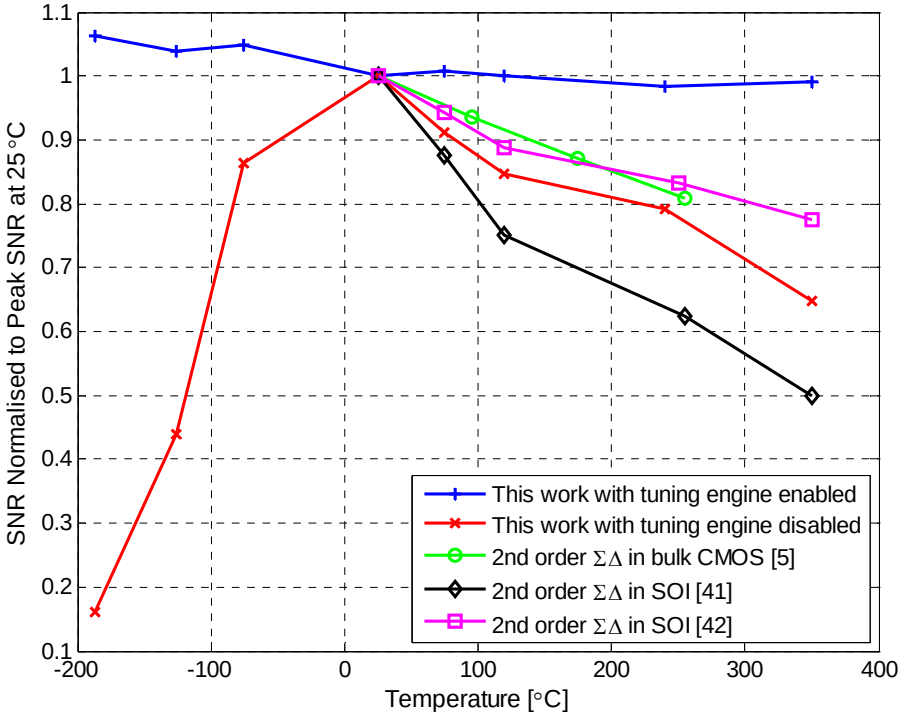


Figure 59: Comparative performance of state of the art extreme temperature A/Ds against this work. The SNR performance of each A/D is normalized to its peak at 25°C.

Figure 59 presents the SNR performance of several state of the art extreme temperature A/Ds compared to this work. The SNR of each converter has been normalized to its peak SNR at 25ºC. With the tuning engine disabled, the SNR of the ΣΔ modulator drops rapidly with increasing/decreasing temperature.

It is evident that tuning engine ensures that the ΣΔ modulator maintains the required SNR across the entire temperature range.

5.2 ΣΔ Modulator Test IC

The complete modulator (Figure 60) was implemented in in.18μm 1.8V CMOS technology. Floor plan of the test IC is shown in Figure 61. Circuit level simulated SNDR versus input signal amplitude of the modulator including the tunable resistive ladders is shown in Figure 62. The simulations in this figure were carried out for different temperatures.

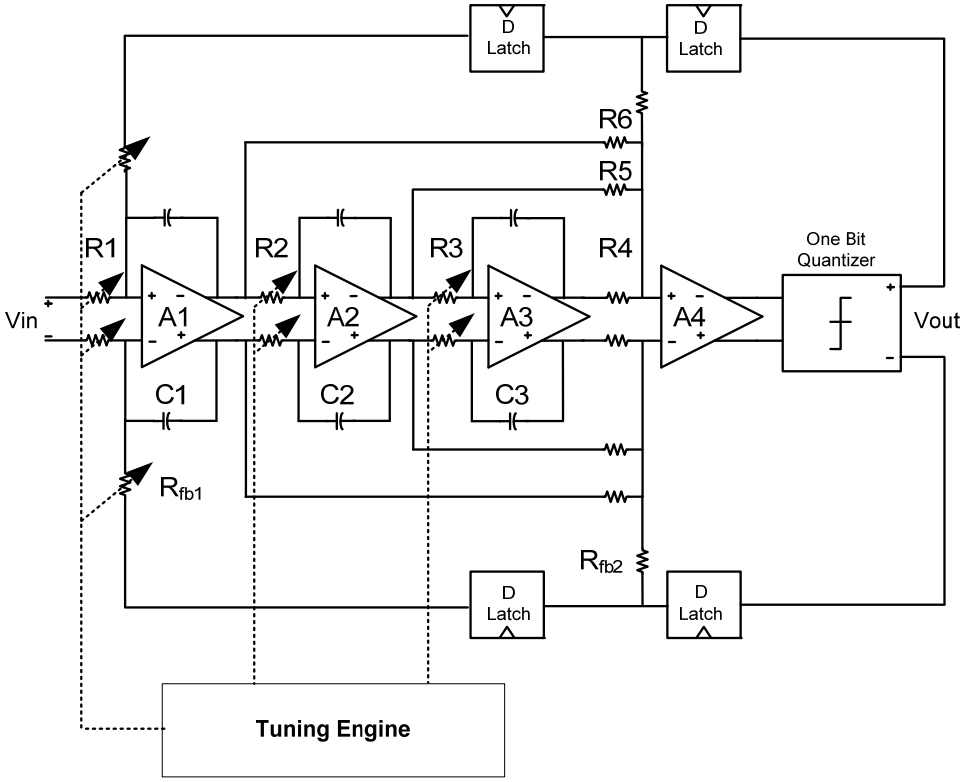


Figure 60: Full modulator with tunable resistive ladders circuit schematic.

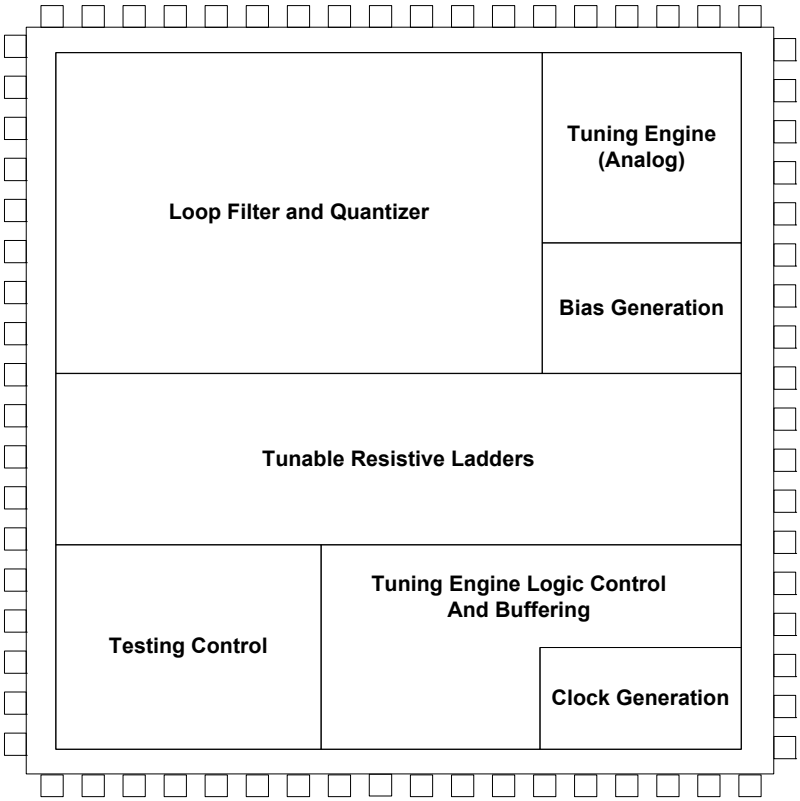


Figure 61: Full IC floor plan.

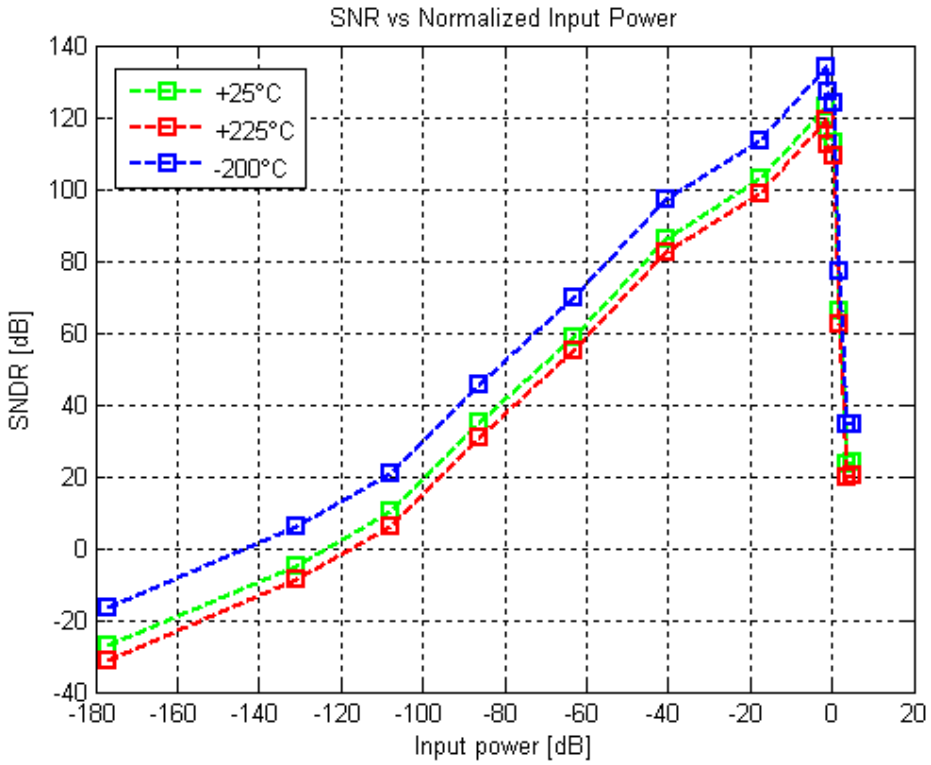


Figure 62: Simulated SNDR vs. input signal amplitude of the circuit level modulator including the tuning engine.

CHAPTER 6

CONCLUSIONS

In this thesis, a 20 bit continuous time ΣΔ modulator for extreme temperature applications was presented. A key contribution of this research is the development of an RC time constant tuning engine, for high linearity, continuous time active RC circuits. The tuning circuit is used to maintain the required linearity of the 10 ksps 20 bit continuous time ΣΔ modulator intended for space spectroscopy applications. The proposed circuit which is based on master slave architecture automatically selects on chip resistors to control RC time constants to an accuracy of ±5%. The tuning range, tuning accuracy and circuit non-idealities were analyzed theoretically. To verify the concept, an experimental chip was fabricated in.18μm 1.8V CMOS technology. The tuning engine which occupies an area of .065mm^2 consists of only an integrator, a comparator and a shift register. It can achieve a signal to noise and distortion ratio (SNDR) greater than 120dB over a ±40% tuning range.

A second improved version of the tuning engine was also presented, whereby limitations of the first engine are eliminated. The entire modulator was implemented in.18μm 1.8V CMOS technology. Circuit level simulation results show that the modulator achieves an SNDR of 120dB across a temperature range from -200°C to 225°C.

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