Cost-Effective

Integrated Wireless Monitoring of

Wafer Cleanliness Using SOI Technology

by

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ABSTRACT

The thesis focuses on cost-efficient integration of the electro-chemical residue sensor (ECRS), a novel sensor developed for the in situ and real-time measurement of the residual impurities left on the wafer surface and in the fine structures of patterned wafers during typical rinse processes, and wireless transponder circuitry that is based on RFID technology. The proposed technology uses only the NMOS FD-SOI transistors with amorphous silicon as active material with silicon nitride as a gate dielectric. The proposed transistor was simulated under the SILVACO ATLAS Simulation Framework. A parametric study was performed to study the impact of different gate lengths (6 μm to 56 μm), electron motilities (0.1 cm^2/Vs to 1 cm^2/Vs), gate dielectric (SiO_2 and SiN_x) and active materials (a-Si and poly-Si) specifications. Level-1 models, that are accurate enough to acquire insight into the circuit behavior and perform preliminary design, were successfully constructed by analyzing drain current and gate to node capacitance characteristics against drain to source and gate to source voltages. Using the model corresponding to SiN_x as gate dielectric, a-Si:H as active material with electron mobility equal to 0.4 cm^2/V-sec, an operational amplifier was designed and was tested in unity gain configuration at modest load-frequency specifications.

Dedicated to:

My parents, and brothers Viraj - Aneesh

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CHAPTER 1

INTRODUCTION TO PASSIVE WIRELESS IN-SITU MONITORING OF WAFER CLEANLINESS

The monitoring methodology under study is the Electro-Chemical Residue Sensor (ECRS) developed by X. Zhang, J. Yan, B. Vermeire, F. Shadman and J. Chae [1]. Because this sensor, which primarily serves as a load, is an integral part of the system, it is important to understand both the basic working principle of the sensor and the parasitics associated with the sensor.

Basic Principle of Operation

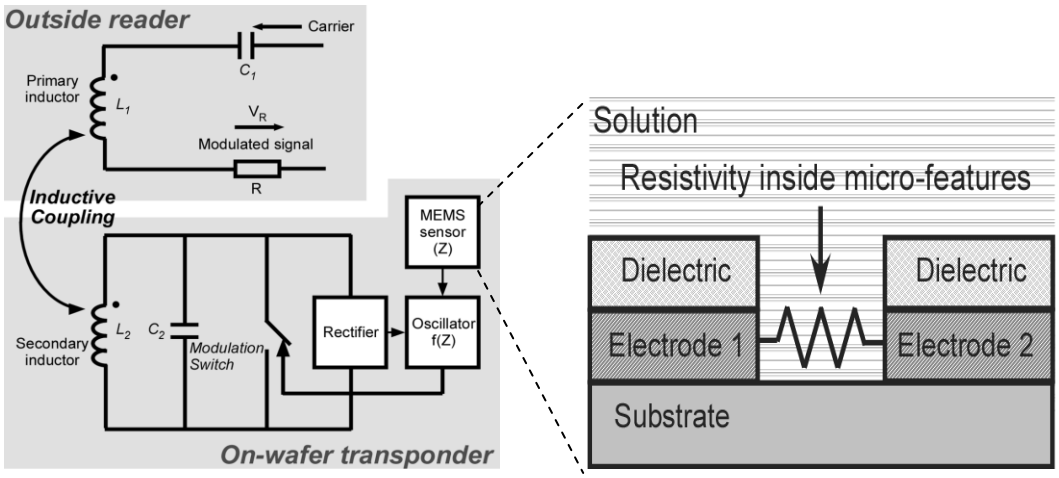


Fig.1.1 (a) Monitoring system prototype (b) Sensor structure

With thick dielectric layer covering the electrodes, the ECRS measures the impedance of fluid inside high aspect ratio micro-features which mimics the cleanliness of patterned wafers. The output of the ECRS is converted to a frequency via an on-wafer oscillator and transmitted to a data processing unit by passive transponder circuitry via inductive coupling. Since the electrical wires, connectors and batteries do not survive the cleaning chemistries used during

semiconductor manufacturing, it is preferable to have the monitoring system to be wireless, passive (remotely powered) and fully integrated. The ECRS wafer also needs to have form factor same as that of ordinary wafer so that it doesn't affect the fluid flow in the wafer-rinsing tool. This requirement also makes sure that the ECRS wafer can easily be manipulated using the same robotic wafer handlers that are under use for handling other ordinary wafers.

Modeling of ECRS and Equivalent Impedance:

The ECRS measures the impedance of fluid inside high aspect ratio trench, where the reduced concentration of contaminants will reduce the fluid conductivity, thus increasing the impedance

There exist several parasitic components. The Randles cell is one of the simplest and most common models to model these effects. It takes into account a solution resistance, a double layer capacitor and a charge transfer resistance. Additionally, there are capacitances associated with dielectric layers above and below the electrodes.

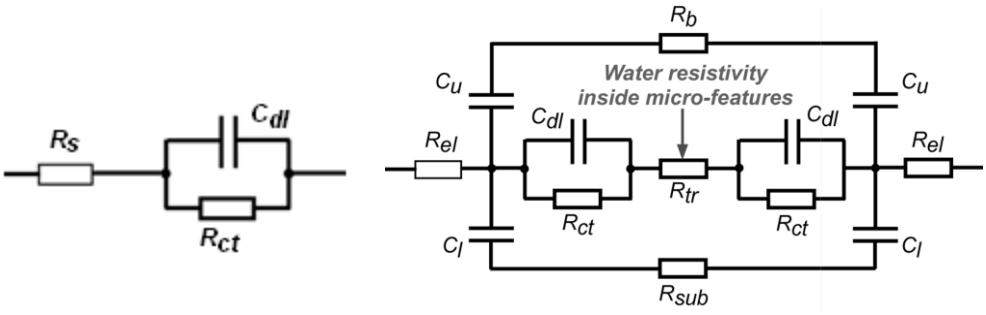


Fig.1.2 (a) The Randles cell (b) Model with all the parasitics included

Table1.1

ECRS parastitics

Symbol	The parameter
R_{el}	Electrode resistance
C_{dl}	Double layer capacitance. Whenever a conducting material (e.g. electrode) is kept in contact with electrolyte there is a formation of opposite charges across the electrode-electrolyte interface. This charge separation acts like a parallel plate capacitor.
R_{ct}	Charge transfer resistance. The metal molecules can electrolytically dissolve into the electrolyte, according to equation: $Me \overset{eq}{\Leftrightarrow} Me^{n+} + ne^{-}$.
R_b	Resistance of the bulk solution
R_{sub}	Resistance of substrate (very large, substrate is a dielectric material)
C_u, C_l	Capacitors formed due to dielectric layers above and below the electrodes

Sensor impedance, Z, is therefore:

$$Z = 2R_{el} + \left\{\left(\frac{2}{jwC_u} + R_b\right) || \left(\frac{2}{jwC_l} + R_{sb}\right) || \left[2\left(\frac{1}{jwC_{dl}} || R_{ct}\right) + R_{tr}\right]\right\}$$

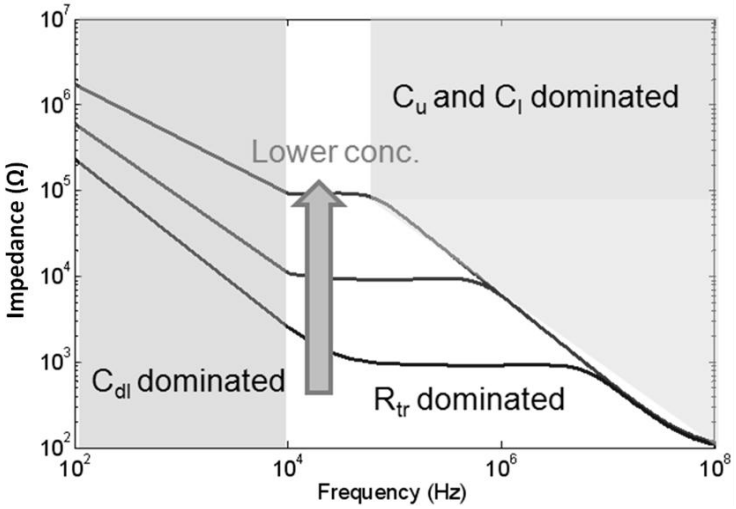


Fig.1.3 ECRS impedance versus frequency

C_{dl} dominates the impedance at low frequency, while at high frequency it is dominated by C_u *and* C_l. At intermediate frequency, it is dominated by the solution concentration sensitive term, R_{tr}. Even though, C_{dl} dominated impedance (i.e. impedance at low frequency) is solution concentration dependent, we observe that sensitivity to solution concentration is low. It is, therefore, in our interest to work in the intermediate frequency band where sensor impedance is R_{tr} dominated. To maximize width of this region, C_{dl} must be increased and C_u and C_l must be decreased. C_{dl} is increased by increasing liquid-metal interface by elongating sensor in serpentine pattern. The sensor was reported to have working frequency range from few hundred hertz to few tens of kHz.

Impedance to Frequency Conversion:

To perform real-time, in-situ measurement of sensor impedance wirelessly, it is necessary to perform impedance to frequency conversion. The oscillator does this job of converting sensor impedance into oscillation frequency.

Frequency of oscillation is related to sensor impedance by equation:

$$f(Z) = {}^{1}/_{2\tau(z)\ln 2}$$

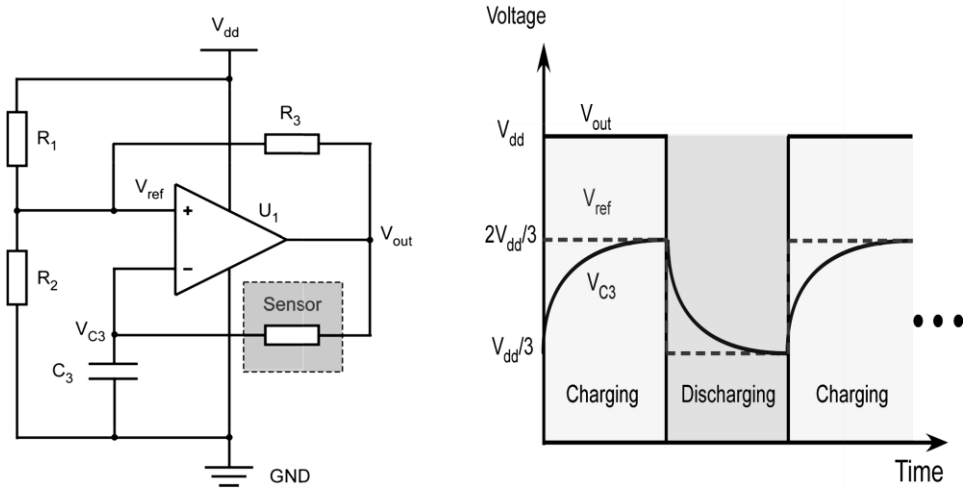


Fig.1.4 (a) Oscillator circuit (b) Output waveform

Required Op-Amp Specifications:

The op-amp needs to drive 1kΩ to 100kΩ resistive load at low frequencies, say few hundreds of hertz. Gain at these frequencies under given load conditions needs to be at least 10dB for successful operation of the oscillator circuit. Also, PSRR needs to be very high because op-amp will be remotely powered via rectification of the input RF power. Because what we are interested in is not high-speed operation, a-Si:H TFT technology could be a promising solution for cost-effective integration of the system in place, as will be explained in the next chapter.

CHAPTER 2

CHOICE OF TECHNOLOGY

The first task is to choose a technology that is most appropriate for the given task, i.e. cost-effective integration of ECRS and wireless transponder. Amorphous silicon (a-Si:H) thin film transistor (TFT) seems to be an excellent choice mainly because it is a low-cost technology, and ideal for large area applications where it is not crucial to consider speed of operation [2].

Inherent to our sensor, there is a technology requirement that the sensor need to be manufactured on a highly resistive substrate, as we are primarily interested in resistance of the trench with high aspect ratio which is in parallel with the substrate resistance as shown in figure 1.2 (b). This requirement makes sure that there is reduced parasitic coupling between the two electrodes, and measured impedance sensitivity with respect to contamination concentrations is high. Hence SOI is a good choice for the ECRS.

It is also good choice from performance stand point as SOI devices and circuits to perform better than their bulk counterparts thanks to inherent reduced parasitic components (dielectric instead of PN junctions are in use for isolation), improved trans-conductance, sharper sub-threshold slope, high temperature operation, and radiation hardness[3].

The technology is superior from fabrication point of view as well, as the technology not only involves fewer processing steps than the bulk, it also suppresses some yield hazard factors present in bulk CMOS. Since the circuit needs to be cost-effective, targeted device needs to be manufactured with as less

number of process steps as possible, in the micro-technology regime, with amorphous silicon as active material.

Because the device is in micro-technology regime, effects like impact ionization, hot carrier transport, narrow channel effect, could be neglected more or less. For the same reason, BSIM level 1 model -originally developed to describe MOS device with a channel length of 2 μm or more, is sufficiently accurate enough for our purpose. [4]

Self heating problem inherent to SOI circuits may not be as critical. The reason for this is that the mobility of a-Si is low, and hence currents will be small. Also, since high speed of operation is not required, large currents are not needed.

Next step is to decide whether to use fully depleted (FD) SOI or partially depleted (PD) SOI. FD SOI has some advantages over PD SOI, most important one being FD SOI devices have the highest gains in circuit speed, reduced power requirements. FD devices operate faster because of a sharper sub-threshold slope, and a reduced threshold voltage that allows for faster switching of the MOS transistors. Also, Fully-depleted SOI devices are naturally free from kink effect and have better sub-threshold swing. [2]

Now, for making the technology cost-effective, it is desirable that there are as less number of fabrications steps as possible. Because use of complimentary configuration will only increase number of mask steps, we may either use PMOS based circuitry or NMOS based ciruit. For amorphous silicon hole mobility is about more than an order of magnitude less than electron mobility, the most obvious choice is therefore to use NMOS only.

We therefore propose a-Si:H FD-SOI nMOS TFT technology for this ECRS system. For this, first literature survey focusing a-Si:H technology fabrication constraints, process variations and effects was done. This is because the ultimate goal is to build a robust circuit that would work over a range of device parameter variations. This should cut down our production costs too, as we can then work our way around with less control on our process steps. For this, device structures with different densities of defect states, mobility, gate lengths etc. need to be characterized to understand the performance window. With understanding of the fabrication constraints in place, a fabrication methodology for the device is proposed, detailing processing steps and suggesting typical layout rules.

We propose bottom gate configuration for the TFT. This is because polycrystalline silicon gate metal needs to be deposited first, prior to active amorphous silicon deposition as amorphous silicon cannot withstand high temperatures. n+ poly-Si deposition is a high temperature process and such high temperatures re-crystallize amorphous silicon. This introduces grain boundaries in the active channel region which is not desired.

Now that the technology has been proposed, to check feasibility of the technology for the application we are interested in, device design and modeling was done through a stepwise process. First, device level simulations were performed in SILVACO. Next, characterization/performance parameter extraction was done using MATLAB and by aiding the process with development of own

software tool. Lastly, verification of the analytical model was done using Cadence Spectre Virtuouso simulator.

Now, with corresponding level-1 SPICE models in place, the next step was to build test circuits in a circuit simulator (an op-amp and the rectifier circuit) and analyze the circuit performance to verify that the technology can be used to meet the circuit goals.

Final step is to build and test actual device characteristics and remodel the model file if necessary. In such a case, we may need to te-design the circuit with updated model and test the circuits for the system in place.

CHAPTER 3

A-SI:H TECHNOLOGY FABRICATION CONSIDERATIONS

The a-Si:H TFT is a low mobility transistor. It can therefore be used only for applications that require a transistor but do not have a very short response-time constraint. Mobility is not the only limitation that this technology faces. The performance of these transistors is dependent on large number of factors such as the design of the transistor, the etch methods, influence of the various process steps e.g. power specification for the PECVD process, properties of the dielectric used, thickness of the conducting thin film, structural properties the composing thin films etc. [2] Such considerations are primary focus of this chapter. The cited compilation [2] served as a good source of the literature survey for a-Si:H considerations, as it neatly explains all of the results noted in this chapter in detail and in depth.

Lithography Considerations:

Generally it is desired that the fabrication process should involve fewest lithography steps (or masks). This helps especially where mass production is desired, for which high throughput and low costs are a necessity. The minimum mask-count has been reduced from 7-8 previously to 4-5 today. This has been made possible thanks to technology solutions that involve low-mask count processes, which usually combine two or three steps into one step, for example: non-conventional back-light exposure, a multiple etch process, novel lithography etc.

Quality of Amorphous Silicon:

Crystalline silicon (c-Si) has a well-defined tetrahedral lattice structure with a bond length of 0.35 nm between adjacent atoms and a corresponding bond angle (θ) of 109°. For amorphous silicon, this tetrahedral structure of the silicon network is preserved for only short length scales (up to ~1nm), while there is little or no long range order. The amorphous nature therefore introduces a degree of disorder into the system so that there is a range of bond lengths (Δa) and bond angles (Δθ) around the crystalline case. For device quality a-Si:H, $\Delta a \leq 2\%$ of the crystalline bond length (a) and $\Delta\theta \leq 10\%$ of the crystalline bond length (θ) is typically desired.

Bulk Density of States (DOS) and Hydrogen Passivation:

Bonding deviations give rise to perturbation of energies for bonding and anti-bonding states, smearing out the band-edges, thereby giving rise to localized "band-tail" electron states. Quite obviously, width of these band-tails is measure of disorder/bonding deviations in the network. When a bond gets highly deformed, it becomes very weak –breaking of which leads to two dangling bonds/co-ordination defects that correspond to electron state distribution around the middle of the band-gap, each state having capacity to occupy two electrons.

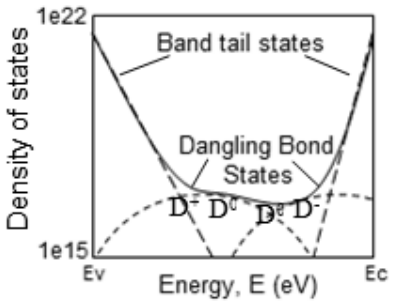


Fig. 3.1 Density of states diagram

Dangling bonds lying significantly below Fermi level get doubly occupied (D^- states), those well-above Fermi level are empty (D^+ states), those around Fermi level are single occupied (D^0 states). These defect states bring about scattering effects which effectively reduce carrier mobility. Lower density of these defects states is, therefore, always desired.

Lower defect densities are brought about by a process called hydrogenation where hydrogen "passivates" defects by forming Si-H bond at a silicon dangling-bond site. As the number of dangling bonds is reduced, local stress in the network gets reduced thereby reducing the number of weak bonds. This way band tail width gets reduced, and the band gap appears to widen because of this hydrogenation.

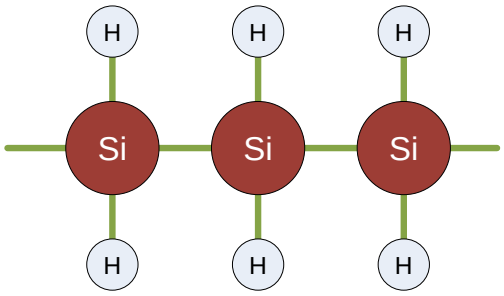


Fig.3.2 Alkane-like polymeric structure

However, it must also be remembered that very high a concentration of hydrogen is not desired as well. Not only does it increase the optical gap, but if the hydrogen content is increased above 10%, polymeric material gets formed, where its structure is analogous to alkane chains in carbon systems (fig3.2). Further increase in hydrogen content can segregate out hydrogen from silicon to form clusters. a-Si:H with high hydrogen content is very porous, has high defect

density and poor electronic properties. Parameter that controls the hydrogen content is the deposition temperature. The higher the substrate temperature during deposition, the lower is the hydrogen content of the a-Si:H produced .

Doping of a-Si:H

Even the most basic semiconductor devices rely on the ability to control precisely the position of the Fermi level within the band gap with doping. Particular to a-Si:H TFT, a highly n-type doped (n+) a-Si:H layer is required between metallic source and intrinsic a-Si:H channel layer in order to provide a non-rectifying ohmic contact. Without this layer, current crowding is observed at the source and drain which drastically reduces source-drain current in the channel.

However, we it is difficult to control "equivalent" doping density which corresponds to desired level of carrier concentration. This is because, when an impurity is added to amorphous silicon, there is no constraint on the number of bonds that impurity can form. Again, this is because, unlike the crystalline silicon case, silicon atoms in a-Si:H network do not have to form four bonds with four other silicon atoms. With addition of impurities, the local silicon network is able to adjust itself so that the impurity is assimilated into the bulk without having to donate or accept any carriers. This occurs as dopants form three (for acceptor type dopants) or five (for donor type dopants) bonds instead of forming four bonds and then accepting (for acceptor type dopants) or donating (for donating type dopants) the extra electron into the conduction band. Doping efficiency is therefore very low, and is related to concentration of dopant gas during deposition.

Fermi energy shifting also takes place through alternate process, as it occurs with creation of dangling bonds. The process of doping adds approximately one dangling per activated dopant. On account of equilibrium between dangling bonds and hydrogen atoms, this does not affect mid-gap states, but the process does increase band-tail width. Additionally, the ion implantation step requires a high temperature dopant-activation annealing that removes hydrogen, but the step also re-crystallizes low temperature deposited a-Si:H and changes dielectric films which is definitely not desired. For these reasons, Use of an ion implantation process is impractical and undesirable.

The most common method to solve the problem of doping a-Si:H is to directly deposit the doped film by PECVD. The process parameters are same as those for a-Si:H, with doping component such as PH_3 or B_2H_6 being added to supply the dopant atoms. Another method to dope a-Si:H is to use the non mass-separation ion doping method, where low ion acceleration energy is used for a short time (acceleration voltage less than few kilovolts) to shallowly dope the film using dopant containing gas.

In summary, thin film d**eposition rate** and the material properties namely activation energy, interface characteristics, bulk defect density, mobility which directly affect transistor performance are dependent on various depositions process factors e.g. type of process used, whether amplitude modulated RF plasma or frequency modulated RF plasma was used, Silane content of the feed-gas, plasma RF frequency, substrate temperature, **plasma condition, thin film**

depositions sequence, bombardment energy, interface **dielectric characteristics,** thin film thickness.

Dielectric growth considerations

Severe temperature restrictions for process steps make standard thermal growth of native oxide impractical. Alternately, solution is to develop novel low temperature process to grow conventional choice i.e. SiO_2 or to explore growth of other dielectric materials.

Novel technologies that rely on oxidization of the thin film, viz. high pressure oxidation, laser or excimer lamp oxidation, plasma anodization, have proved impractical because of inherent problems of low oxide growth rates, lack of success history for industrial applications, and incompatibility with large area production etc. Low temperature deposition of insulators is a better alternative., Insulator films produced using Physical Vapor Deposition (PVD) have been found to be more porous, more strained, more reactive and less stoichiometric than those produced using Chemical Vapor Deposition (CVD). Clearly, CVD is an obvious choice so far as deposition technology is concerned.

Silicon nitride is being used extensively for a-Si:H TFT technology. It is very crucial to make gate dielectric interface smooth as this interface directly influences transistor characteristics through surface scattering. In selecting a process choice, another important key points to consider is N/Si ratio. Higher nitrogen content increases the optical band gap for nitride layer and decreases density of defect states i.e. density of both fast states (interfacial traps with fast re-emission times) and slow states (interfacial and bulk traps with slow re-emission

times). This in turn improves threshold voltage stability, ΔV_T. The N/Si ratio affects band-bending, therefore threshold voltage (V_T) and electron mobility. The optimized range for N/Si ratio from V_T and electron mobility point of view is between 1 and 1.1, while for best TFT characteristics and reliability, the gate SiN_x should be slightly nitrogen rich, resulting in layers with low compressive stress and with high optical gap. N/Si ratio may be controlled by controlling plasma power. The ratio decreases with increase in plasma power, film stress changes from tensile to compressive which is consistent with change in N concentration of the film.

Etching selectivity:

High a-Si:H/SiN_x etch selectivity can be obtained by selectively forming a Teflon-type polymer residue on a-Si:H surface by including hydrogen in the fluorocarbon stream. Etch ratio could also be increased by increasing Cl content in the feed gas (i.e. Cl_2, HCl or $SiCl_4$ can be added to fluorocarbon or SF_6). Similarly, high SiN_x/ a-Si:H etch selectivity is obtained by increasing F content.

High n+ versus undoped a-Si:H etch selectivity is particularly difficult to accomplish high n+ versus undoped a-Si:H etch selectivity, mainly because both their etch chemistry and mechanism are similar. End-point of n+ etch process could either be detected from optical emission spectroscopy (which has its own limitations), or by counting the etch time, or by monitoring the process visually. Only for electrically activated doped film, etch rate ratio greater than 4 could be obtained using CF_3Cl or CF_2Cl_2 gas.

Metallization:

Metal choices include Ta, Cr, Mo (or its Alloy), Al (or its alloy), Ag, Cu. When choosing a metallization scheme, most important material properties that one needs to consider are: resistivity, contact to silicon, interfacial thermal oxide, adhesion, heat-resistance, chemical durability and etchabiliy. Ideal choice will be a material that has low resistivity, has good contact and adhesion properties, is resistant to surroundings, heat, chemicals and that can be easily etched to form interconnection as desired.

Table 3.1

Metals and their properties:

Properties		Materials					
		Ta	Cr	Mo (Mo Alloy)	Al (Al alloy)	Ag	Cu
Crystal Structure		BCC	BCC	BCC	FCC	FCC	FCC
Resistivity μΩ cm	Bulk	5.5	12.7	5.5	2.7	1.6	1.7
	Film	25	18-20	12-20	4-10	2-4	2-4
Contact (to Si, ITO)		G	G	G	NG	NG	NG
Adhesion		G	G	F	G	NG	NG
Heat-resistance		G	G	G	NG	NG	NG
Chemical-durability		G	G	NG	NG	NG	NG
Etchability		G (dry)	G (wet)	G (wet/dry)	G (wet)	NG	NG

(G=Good, F= Fair, NG= Not Good)

Now, with this table in place, one should also know metal specific concerns:

- To form a Ta film, an underlayer such as Mo,Nb or TaN, is required.
- Cr exhibits all good properties as those for Ta. However, sputter-deposited Cr film has high tensile stress that may lead to cracking of underlayer and glass substrate. NiCr is another interesting option. Mo has slightly lower resistivity than that for Ta and Cr, however adhesion property is worse. For Al, hillocks formation during CVD of the gate insulator is a serious problem. Also oxide of Al metal is a good insulator. [30]
- Cu and Ag suffer from poor non-electrical properties (table above)

TFT structure:

To manufacture a-Si:H TFT, multiple structural configurations are possible. Most predominant are the top-gate staggered, the simply staggered structure and the inverted-staggered structure. Of these, the inverted-staggered structure has better device characteristics because it has a superior a-Si:H/dielectric interface. This results in a lower interface density of states, therefore low threshold voltage. This seems to be excellent choice for our purpose because low-temperature process requirement as explained in chapter2.

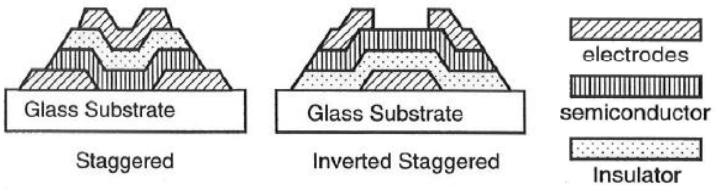


Fig. 3.3 Staggered and Inverted staggered structures

FABRICATION STEPS

The following process flow was developed to manufacturing the ECRS and the circuits needed to wirelessly read out the data. Masks with test structures to accurately characterize the technology were designed and are described in chapter 12.

Transistor fabrications steps:

(1) Gate Metal Deposition on glass substrate:

Material being deposited: n+ poly-silicon, thickness = 3 μm

(2) Pattern gate metal:

Steps in patterning:

1: Apply photoresist

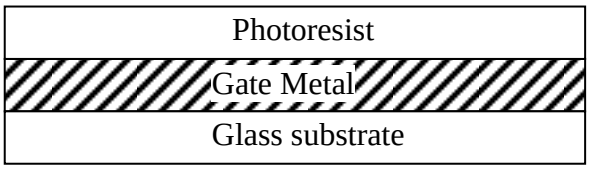


Fig 4.1 Cross-sectional view after applying photoresist

2: Use photomask to etch away part of photoresist.

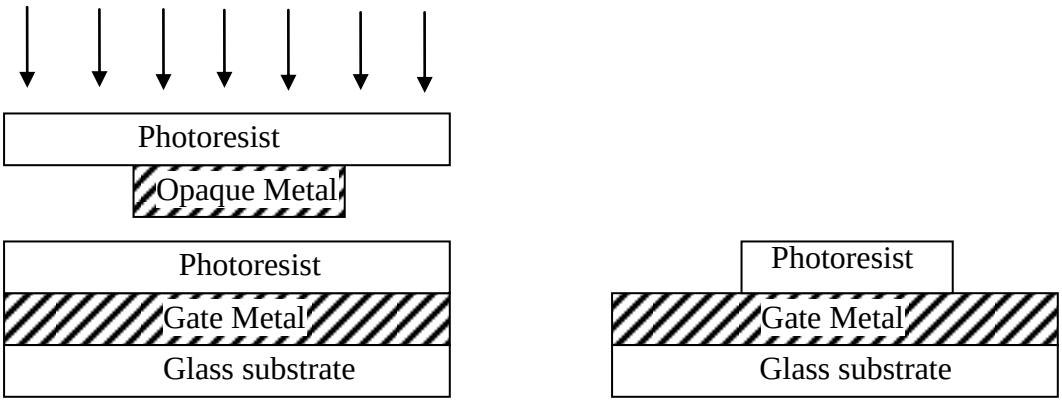


Fig 4.2 Cross-sectional view after etching away photoresist

3: Etch away gate metal not covered by photoresist.

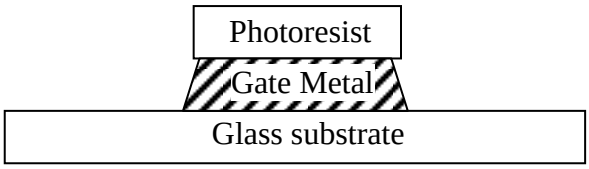


Fig 4.3 Cross-sectional view after etching away metal

Masks used and the end structure:

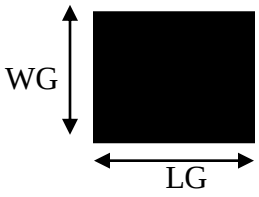


Fig 4.2 (a) "GATE" Mask (b) Cross-sectional view after patterning gate

(3) Deposit Gate dielectric

Material being deposited: Silicon Nitride, thickness = 30nm

Fig. 4.3 Cross-sectional view after depositing gate dielectric

(4) Deposit channel (active area)

Material being deposited: intrinsic a-Si:H, thickness = 100nm

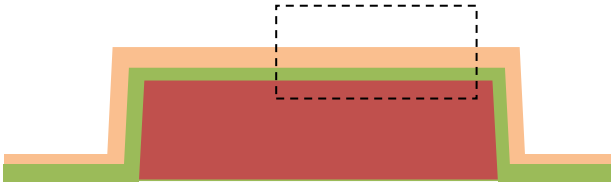


Fig. 4.4 Cross-sectional view after depositing active channel

(5) Pattern active area (mask name: Active)

Process similar to one described in step 2, high Si/SiN_x selectivity is required.

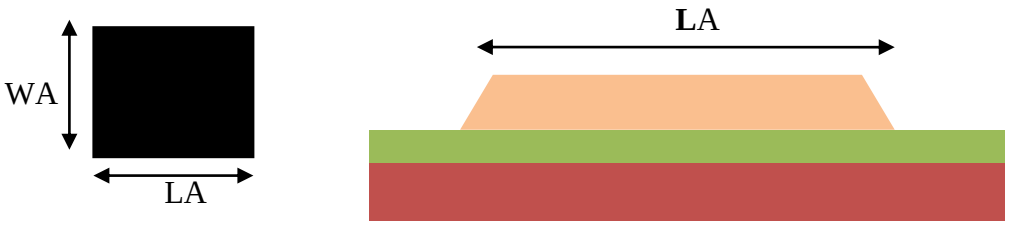


Fig. 4.5 (a) "ACTIVE" Mask (b) Cross-sectional view after patterning active area (Zoomed-in to dotted region in fig.43)

(6) Deposit dielectric material:

Material being deposited: SiN_x or SiO_2, thickness = 2 μm

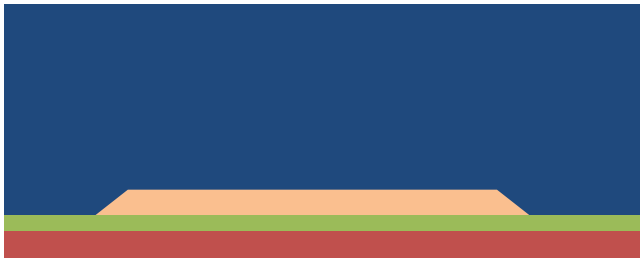


Fig. 4.6 Cross-sectional view after depositing dielectric over active region

(7) S/D opening:

Using mask "SDO", etch away dielectric and open up active regions and gate metal, so that terminal connections could be made.

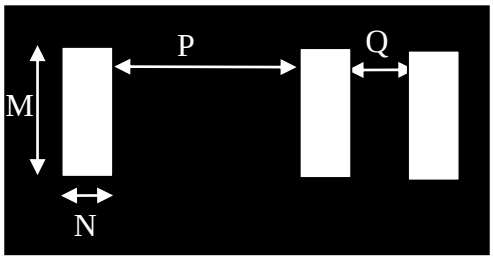


Fig. 4.7 (a) "SDO" Mask

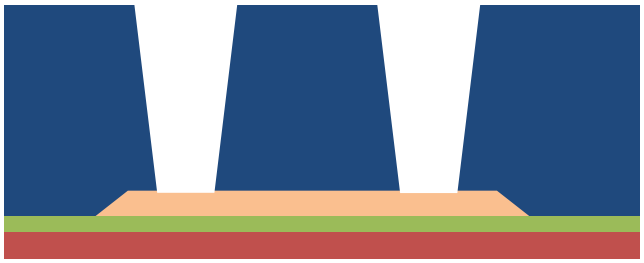


Fig. 4.7 (b) Cross-sectional view after opening SDO

(8) Deposit n+ a-Si:H

Material being deposited: n+ a-Si:H, thickness = 1 μm

Fig. 4.8 Cross-sectional view after depositing contact a-Si:H

(9) Contacts Isolation (“SDI” Mask)

Fig. 4.9 (a) “SDI” Mask (b) Cross-sectional view after contacts isolation

(10) Deposit Isolation dielectric again:

Material being deposited: SiNx or SiO2, thickness = 1 μm

Fig. 4.10 Cross-sectional view after deposition of dielectric over terminals

(11) Selectively etch dielectric over silicon using “CONTACT” mask.

Fig. 4.11 Cross-sectional view after using “CONTACT” mask

(12) Contact Metal deposition (Material: Al, thickness: 0.3 μm)

Fig. 4.12 Cross-sectional view after deposition of metal over contact regions

(13) Contact Metal Patterning, use “METAL” mask

Fig. 4.13 Cross-sectional view after using “METAL” mask

This process flow does make sure that we can fabricate ECRS sensor described in chapter 1. In other words, this process is compatible for the desired sensor structure. Process flow for the sensor is as follows:

ECRS sensor fabrication:

GATE MASK patterns out an electrode pair per sensor in a serpentine pattern. Serpentine pattern is desired because of the reasons explained in the first chapter. Corresponding GATE mask will be similar to the one below.

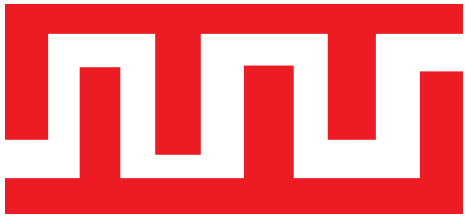


Figure 4.14 GATE mask for sensor

Sensor fabrication is a slightly tricky process as we need to create a trench between the two electrods. Therefore, so far as mask steps after GATE mask are concerned, every step etches out everything inside these trench regions completely. Also from cross-sectional view of the sensor, we know that there is only dielectric present on top of the electrodes, and no amorphous silicon or metal. ACTIVE, SDI and METAL masks therefore need to etch away amorphous

silicon and metal over the electrodes as well, except where contacts are to be made. SDO and CONTACT masks etch away dielectric material in the trench and also where terminal contacts are made.

For almost every microelectronic circuit design, resistors, capacitors and diodes are required as well. Fabrication methodology for each of these is given below in reference with transistor fabrication process flow.

Resistor Fabrication:

If no electrical contact to bottom- gate is made, source and drain contacts would serve as electrical terminals of the resistors.

Capacitor Fabrication:

Gate contact will serve as one of the terminals, the other terminal being a metallic contact that shorts source and drain terminals in the transistor design. To reduce parasitic resistance, source-drain shorting may begin at the SDO mask step itself. If ACTIVE step etches away all of the amorphous silicon for the capacitor structure, even lesser resistive parasitic component may be expected.

Diode Fabrication:

Because the transistor structure we have is nMOSFET, a diode may be realized by shorting gate terminal and one of the source and drain terminals, the left alone terminal being cathode terminal of the diode.

Conclusion:

All of the devices that are necessary as a building block of any standard circuit design may be realized using this proposed technology.

CHAPTER 5

DEVICE LEVEL SIMULATIONS

Technology Computer Aided Design (TCAD) is the branch of computational electronics that models semiconductor fabrication and semiconductor device operation. The simulators solve discretized equations that describe the physics involved, putting appropriate values for the relevant material parameters (viz. permittivity, conductivity) where required, thus reproducing the results one would expect from real-life fabricated device. For successful simulations to be obtained, a number of constraints need to be understood well.

EDA basics:

The majority of the simulators make use of the Finite Element Method (FEM). The structure to be simulated is broken down into a mesh, and numerical methods are applied to solve the discretized differential equations on the mesh points.

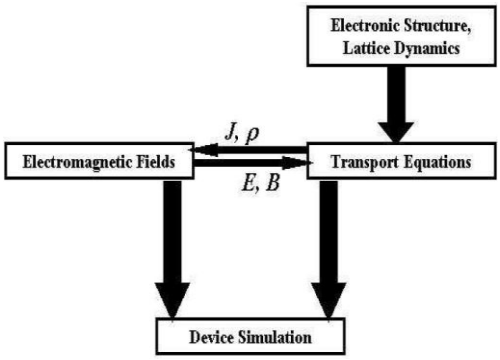


Fig.5.1Working of a device simulator [5]

For each well defined material configuration, the simulator first solves the band structure. In simple terms, it assigns values for parameters such as band gap, trap levels, position of Fermi energy by reading the library lookup tables and user

definitions. Boundary conditions are then applied and the transport module is coupled to the electromagnetic field solver to determine the device fields and currents under the stated conditions. The solver solves the discretized differential equations that describe the material physics using iterative methods and obtains a self-consistent solution.

To simulate a TFT, the equations that need to be solved are:

1. Poisson's equation, $\nabla^2\varphi = \frac{-\rho}{\varepsilon}$

   Where φ=electrostatic potential, ρ=charge density, ε=permittivity

2. Two continuity equations, one for each of the carriers namely electrons and holes, of form:

$$\frac{\delta n(x,t)}{\delta t} Adx = \left(\frac{J_n(x)}{-q} - \frac{J_n(x+dx)}{-q}\right) A + (G_n(x,t) - R_n(x,t))Adx$$

   where $n(x,t)$ is the carrier density, A is the area, $G_n(x,t)$ is the generation rate and $R_n(x,t)$ is the recombination rate. [6]

Equations that model physical phenomena, such as velocity overshoot, mobility degradation, thermal conduction, drain induced barrier lowering, short channel effects, narrow channel effects, channel length modulation, tunneling, generation/recombination are coupled with the Poisson and continuity equations. The final solution-set, includes electron concentrations, net generation rate, current magnitudes, carrier mobilities, and electric field at each point around the mesh. The solution needs to be consistent with all of the equations at every point to a specified accuracy. It is indeed a complex process; but fortunately computers today have enough computational strength to carry out these simulations within a

reasonable time frame. In order that these simulations give us realistic results, there are few things that must be kept in mind, as explained in the next section.

Guidelines on writing the simulation code:

The mesh definition plays a very crucial role in convergence of the simulator to an accurate solution. The denser the mesh is, the better is the spatial resolution. However, a denser mesh requires more computation effort since more equations need to be solved. A good compromise between accuracy and computation time is an ideal mesh choice. Such a mesh is always denser around a region where there is a steep gradient in the configuration, e.g. material boundaries, a sudden change in the doping level, near fixed sheets of charge.

A sample mesh for a-Si:H FD-SOI nMOSFET is shown below. We observe that mesh gets denser at every material boundary, every ohmic contact and where charge concentration is likely to get changed drastically under possible biased conditions e.g. gate dielectric-active silicon interface where inversion/accumulation charges accrue.

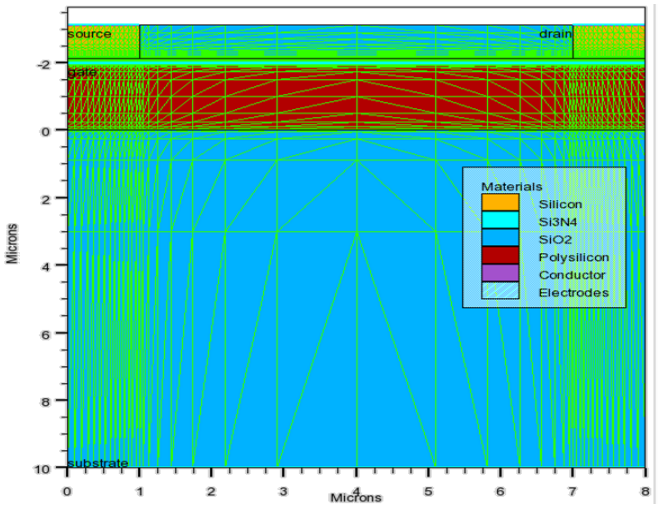


Fig.5.2 Sample mesh

Also, boundary conditions, like charge distributions, terminal electrostatic potentials, definition of ohmic contacts, light beam exposure, should be accurately specified.

Particular to SOI technology, because the channel region/body of SOI devices is floating, convergence problems may arise for increased bias conditions if the initial guess is poor. To avoid this problem, use of Newton Gummel method is recommended to obtain a more accurate initial solution [7].

Particular to a-Si:H technology, where electron mobility as low as 0.1 cm^2/V-sec needs to be defined, one cannot use concentration dependent mobility models (CONMOB, ANALYTIC, ARORA, KLA). These models overwrite the low field mobilities set in the MATERIAL statement [7].

The quality of the materials directly affects the device performance. To capture this dependency and obtain understanding of the performance window one is working in, a parametric study needs to be performed. It can be done through a set of simulations where a single material property is changed at a time. For example, band gap, density of trap states and layer thickness are varied within a reasonable range of values. Studying the resulting simulation results gives insight into the impact the materials choices, layer thicknesses and material quality have on the resulting TFT device characteristics.

CHAPTER 6

DEVICE SIMULATIONS FOR PARAMETRIC STUDIES

Device level simulations were done using SILVACO products and tools. As was explained in the earlier chapter, the software works with the internal physical models, and attempts to solve the set of multiple discretized differential equations over the entire device, under specified boundary conditions through an iterative process.

Simulation flow and SILVACO tools:

DevEdit and Deckbuild are the tools where various aspects of the device structure namely materials, material properties, dimensions, contact terminals, doping levels, simulation meshes etc. are defined. DevEdit can be used as a simulator under DeckBuild, or through a Graphical User Interface (GUI). GUI makes the process of construction of the device easier and interactive. One can literally draw the regions, assign library materials to these regions, set impurity levels and other specifications, and also do the optimal meshing quickly. In summary, the tool is used to generate a new mesh on an existing structure and can be used to create or modify a device. Devices can then be used by Silvaco 2-D and 3-D simulators. DeckBuild is an interactive runtime and input file development environment within which all Silvaco's TCAD and several other SIMUCAD products can run.

ATLAS is a device simulation framework. ATLAS enables device technology engineers to simulate the electrical, optical, and thermal behavior of semiconductor devices. ATLAS provides a physics-based, easy to use, modular,

and extensible platform to analyze DC, AC, and time domain responses for all semiconductor based technologies in 2 and 3 dimensions. ATLAS features comprehensive set of physical models, powerful numerical techniques, and it works well with other software from SILVACO. ATLAS is used to predict the electrical behavior of specified semiconductor structures and provide insight into the internal physical mechanisms associated with device operation, as it conveniently captures the theoretical knowledge. [6]

TonyPlot is a graphing tool . It is a powerful tool designed to visualize TCAD 1D and 2D structures produced by Silvaco TCAD simulators. TonyPlot provides visualization and graphic features such as pan, zoom, views, labels and multiple plot support. TonyPlot also provides many TCAD specific visualization functions such as 1D cut lines from 2D structures, animation of markers to show vector flow, integration of log or 1D data files and fully customizable TCAD specific colors and styles. Plotting engine supports all common 1D and 2D data views

The procedure:

1. Construct the device structure in DevEdit, with region-material specifications, appropriate doping, and meshing specifications. Save the structure file as with .str extension. Though saving command file is optional (.de extenstion), but it is advisable for any potential future modifications to the structure, especially the impurity specifications.
2. Use DeckBuild as text editor for real time program development.

a. The statement “go atlas” in effect asks DeckBuild to shut down the current simulator and activate the ATLAS module. Structure file might as well be created without using DEVEDIT, i.e. using ATLAS alone.
b. Modify the active region to take up amorphous silicon material properties using “material” statement.
c. In order that low mobility set in the “material” statement is not ignored, make sure “model” statement is not forcing ATLAS to use any of the concentration dependent models -namely CONMOB, ANALYTIC, ARORA, KLA.
d. Record/log effect of gate voltage change on device properties for low drain voltage (less than 100mV)
e. Log effect of drain voltage change on device properties for fixed gate voltage, for a set of values of gate voltage.

Analyze current and capacitance plots versus gate-to-source and drain-to-source voltages and extract of level-1 BSIM model parameters.

Device Structure:

As was explained in chapter 2, the device under consideration is a-Si:H FD SOI nMOSFET (refer to fig. 5.2). It is a bottom-gate MOSFET, because deposition of the gate metal -polycrystalline silicon is a high temperature process and a-Si:H active channel region cannot outlive such a high temperature process. At high temperatures, amorphous silicon crystallizes to polycrystalline silicon with huge number of grain boundaries, which is not what is desired. The following figure is a zoomed-in version of fig. 5.2, cropping off substrate portion

from the original figure. This is the section we are primarily interested in, and where electrical performance of the device is investigated.

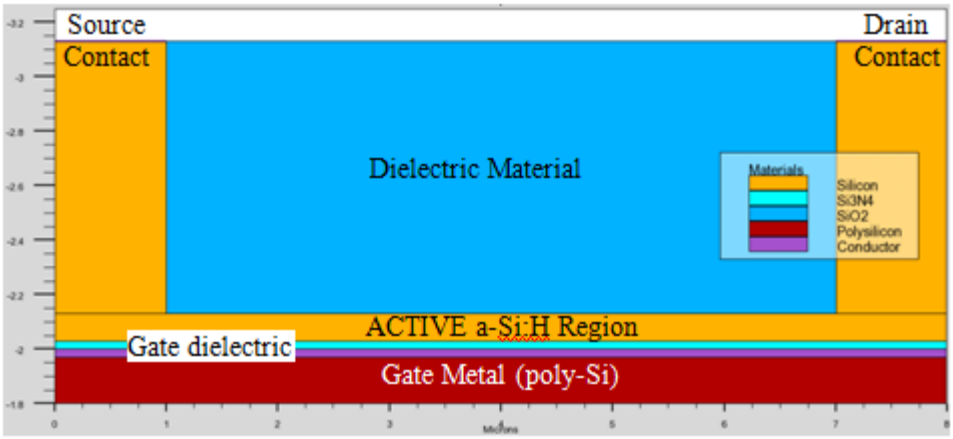


Fig.6.1 Simplified structure for simulation in Silvaco

Simulated variations:

Purpose of this section is to discuss each of the device parameters that are likely to change in real-life scenario and give their significance in brief.

Device performance is strongly dependent on the material quality. Because active region is of amorphous silicon, density of bulk trap states in amorphous silicon may potentially affect device performance. This effect was studied by varying every associated parameter, one at a time. Because device under study is nMOS, variations in the acceptor bulk traps affected device performance the most.

For amorphous silicon, electron mobility varies between 0.1 to 1cm^2/V-sec. Also, it degrades with time. It is important to investigate effect of this degradation on the device performance. Simulations were carried out at μ_n = 0.1,

0.3, 0.5, 0.7 and 1 cm^2/V-sec. Only current scaling was observed, and no change in threshold voltage, capacitances etc. other parameters was observed as expected.

Use of silicon nitride instead of silicon dioxide –as a potential gate dielectric material was investigated. Because silicon nitride has a higher dielectric constant (about twice), increase in both drain current and the parasitic capacitances was observed.

Typically, transistors with different aspect (W/L) ratios are used for a practical circuit realization. This is because a circuit designer expects a different set of performance parameters (trans-conductance, current drive, on-resistance for example) from different transistors in the circuit, as every transistor serves a different role in the overall system. It is therefore crucial to simulate devices with different gate lengths and develop compact model/models that can effectively be used for circuit designing purpose. Device gate length was varied from 6 μm to 56 μm, with very typical amorphous silicon material parameters.

CHAPTER 7

VARYING DENSITY OF BULK TRAP STATES

As was explained in the chapter "a-Si:H Technology Fabrication Considerations", bonding deviations inherent to the amorphous nature of amorphous silicon give rise to number of mid-gap trap levels. Typically these defect states lie in the forbidden gap of the semiconductor and act as emission-recombination centers changing the density of space charge in the bulk silicon and at interfaces directly influencing performance of the device. Hydrogen is used to passivate defects by forming a-Si:H bond, reducing density of active defect states.

Classification of traps can be done based on their corresponding energy levels. Typically, the density of defect states near band edges decays exponentially versus energy, while the distribution is Gaussian for trap levels around middle of the band-gap. Donor-like traps, similar to ionized donor impurities N_D^+, are positively charged and therefore can only capture an electron. This means that donor-like traps are positive when empty of an electron but are neutral when filled. Similarly, acceptor-like traps (N_A^-) are negative when filled but are neutral when empty.

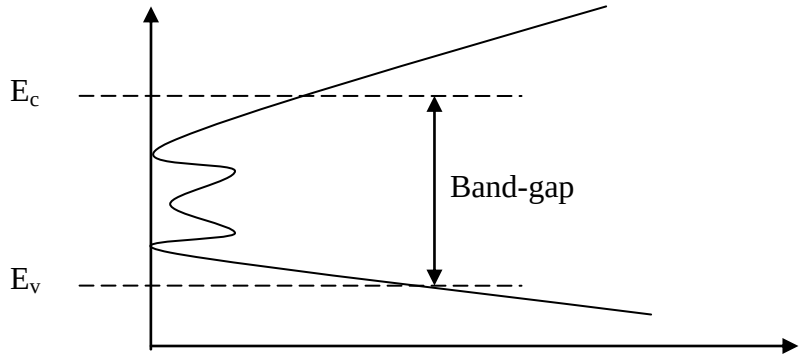


Fig. 7.1 Density of states

DEFECT statement:

In SILVACO, the density of states can be defined using the DEFECT statement with handful of parameters

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \qquad [7]$$

This is the energy distribution model that was first proposed by Davis and Mott [8]. The energy dependence of each of these components is described by following equations:

$$g_{TA}(E) = NTA \times \exp\left(\frac{E - E_c}{WTA}\right)$$

$$g_{TD}(E) = NTD \times \exp\left(\frac{E_v - E}{WTD}\right)$$

$$g_{GA}(E) = NGA \times \exp\left[-\left(\frac{E - E_c}{WGA}\right)^2\right]$$

$$g_{TA}(E) = NGD \times \exp\left[-\left(\frac{E - E_v}{WGD}\right)^2\right]$$

The most typical trap state distribution for passivated a-Si is chosen as the starting point of the parametric study. Defining parameters are assigned values under the "DEFECTS" statement as follows (with reference to the equations above):

DEFECTS CONTINUOUS \

NTA=1.E21 NTD=1.E21 WTA=0.033 WTD=0.049 \

NGA=1.5E15 NGD=1.5E15 WGA=0.15 WGD=0.15 \

EGA=0.62 EGD=0.78 \

SIGTAE=1.E-17 SIGTAH=1.E-15 SIGTDE=1.E-15 SIGTDH=1.E-17 \

SIGGAE=2.E-16 SIGGAH=2.E-15 SIGGDE=2.E-15 SIGGDH=2.E-16 \

"SIG" parameters are carrier capture cross sections pertaining to different defect states. (T=Tail states, G=Gaussian distribution, A=Acceptor, D=Donor, E=Electron, H=Hole).

Probabilities of occupation for the tail and Gaussian acceptor trap states, net recombination/generation rate, therefore the trapped carrier density are all functions of these capture cross-section values. For steady-state conditions, the net recombination/generation rate is identical for electrons and holes i.e. instantaneous equilibrium.

Following table is a summary of everything explained so far in this section:

Table 7.1

Parameters defined by DEFECT statement

	Description	Units	Default value	Example plot (Fig. 7.2)
NTA	Conduction band edge intercept density (acceptor tail)	cm^{-3}	1.12e21	1e21
NTD	Valence band edge intercept density (donor tail)	cm^{-3}	4e20	1e21
NGA	Peak density of states (acceptor Gaussian distribution)	cm^{-3}	5e17	1.5e15
NGD	Peak density of states (donor Gaussian distribution)	cm^{-3}	1.5e18	1.5e15
EGA	Energy corresponding to the Gaussian peak from conduction band (acceptor Gaussian distribution)	eV	0.4	0.68

EGD	Energy corresponding to the Gaussian peak from valence band (donor Gaussian distribution)	eV	0.4	0.72
WTA	Characteristic decay energy (spread) of the acceptor band-tail	eV	0.025	0.033
WTD	Spread of the donor band-tail	eV	0.05	0.049
WGA	Spread of the acceptor Gaussian distribution	eV	0.1	0.15
WGD	Spread of the donor Gaussian distribution	eV	0.1	0.15

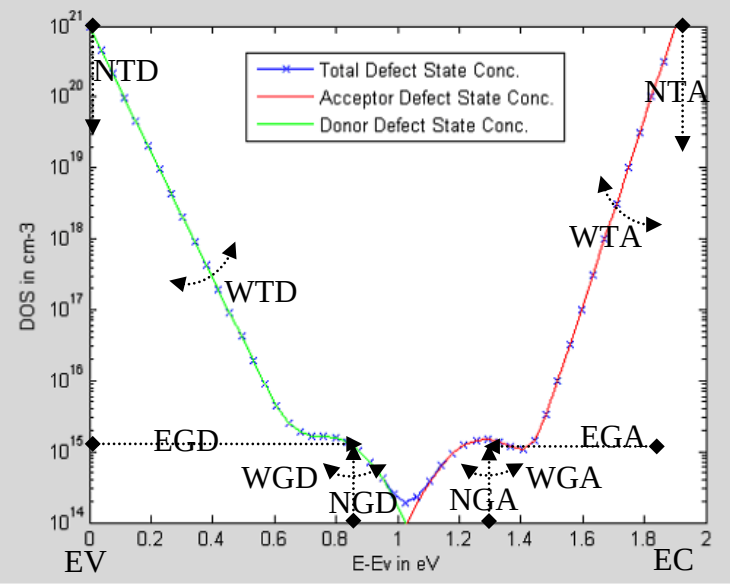


Fig.7.2 Density of states in SILVACO –an example plot

Methodology employed for the study:

Because TFT is n-MOS, current conduction will be primarily affected by acceptor type trap levels. This is because the bulk trap acceptor states lie closer to the conduction band than the donor states. This effect was studied by altering the parameters from the set NGA, WGA, WTA, EGA, one at a time. EGD and WGD

too were varied to effectively change Gaussian distribution of the deep level donor traps, only to observe no change in device characteristics despite choosing the values that may potentially maximize their effect as will be explained in the corresponding results section.

Mathematical analysis and extraction of parameters:

The results were analyzed mathematically, so as to get quantitative understanding of the device performance as well. This was done by extracting performance parameters such as threshold voltage, k-factor, parasitic resistances.

V_{TH} and A factor are extracted from $I_D/\sqrt{g_m}$ versus V_G plot at low V_D, where A= $A = \sqrt{\mu_n C_{ox} W V_D / L}$

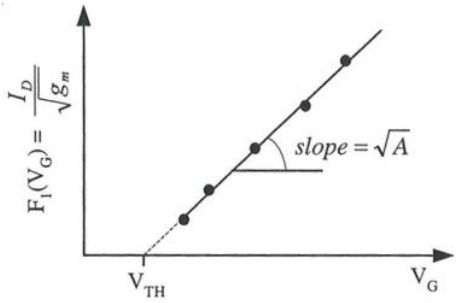


Fig.7.3 Parameter extraction [3]

Current degradation is analyzed and is modeled as an increase in drain resistance, and accordingly value of R_{SD} is computed using MATLAB with model as described here:

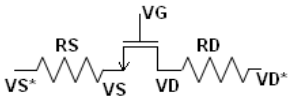


Fig.7.4 R_{SD} modeling

Let $R_S = R_D = R_{SD}/2$ and K = $\frac{u_n C_{OX} W V_D}{L}$ = A^2/V_{DS}*.

Therefore, $V_{GS}=V_{GS}^{*}-I_D R_{SD} / 2$ and $V_{DS} = V_{DS}^{*} - I_D R_{SD}$

$I_D = Kp(V_{GS}-V_T-V_{DS}/2)(V_{DS})$

$= Kp(V_{GS}^{*}-I_D R_{SD}/2-V_T-V_{DS}^{*}/2+I_D R_{SD}/2)(V_{DS}^{*}-I_D R_{SD})$

Therefore,

$I_D = KV_D/(1+KR_{SD})$, where $K= Kp(V_{GS}^{*}-V_T-V_{DS}^{*}/2)$

To extract mobility degradation factor, following equation was used:

$I_D = \frac{A(V_G - V_{TH})}{1+\theta(V_G - V_{TH})}$ (for small V_D).

We observe that I_D dependence on θ and R_{SD} is similar, both of the form y=m/(1+px).

Results:

(I) EGD variation at NGA=1.5 $x10^{15}$, EGD = [0.78, 1]

Reducing value of EGD below 0.78 will not affect total DOS. EGD was therefore increased to the value=1, where its contribution to DOS is potentially maximum. However, as we know for an n-MOS, acceptor traps are the ones that determine the device performance and not the donor traps. This was verified from the simulation results, where no change in IV characteristics was observed.

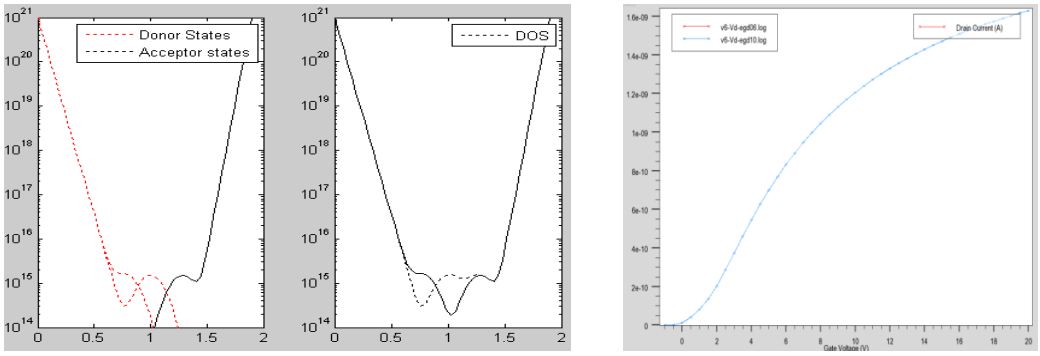
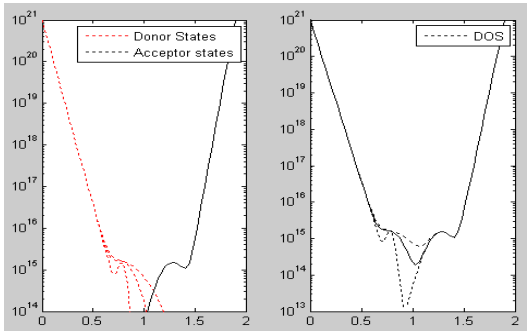


Fig.7.5 (a) Effect of EGD variation on DOS (b) I_D-V_G plots with EGD varied

(II) WGD variation at NGA=1.5 x10^{15} , WGD=[0.05, 0.15, 0.25]

As expected, WGD variation does not affect device performance for NGA=1.5e15.



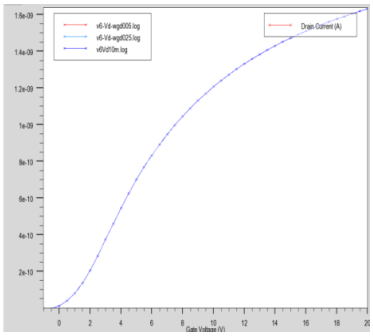
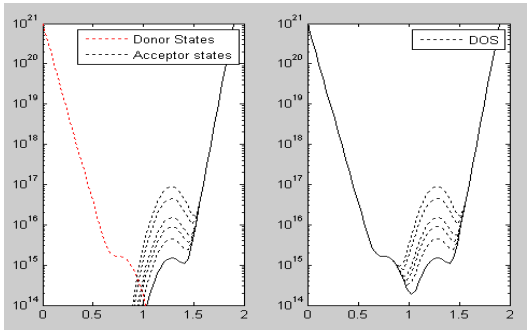


Fig.7.6 (a) WGD variations and DOS (b) I_D-V_G plots with WGD varied

(III) NGA variation: NGA = [1.5e15, 4.5e15, 9e15, 1.5e16, 4.5e16, 9e16]



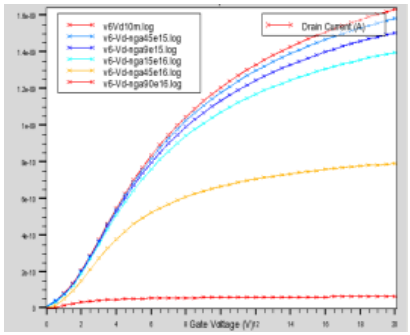
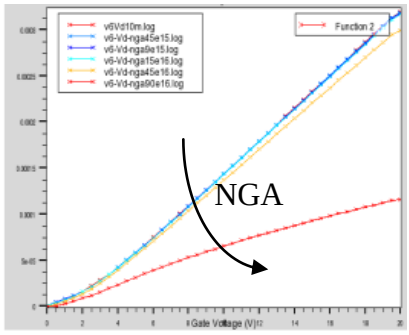
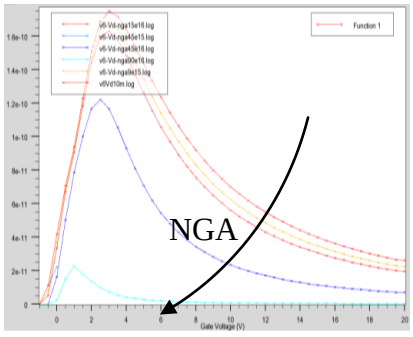


Fig.7.7 (a) NGA variations and DOS (b) I_D-V_G plots with NGA varied

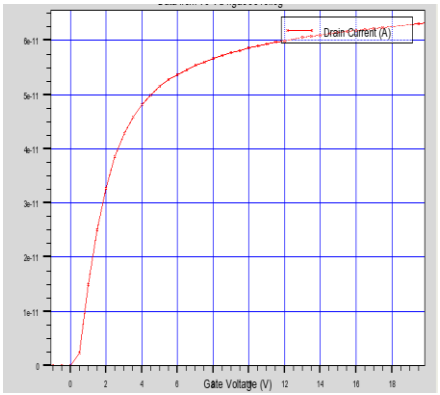




(c) $\sqrt{\frac{I_D}{g_m}}$ -V_G plots with NGA varied (d) g_m-V_G plots with NGA varied

We observe that:

1. Mobility and V_T remain unaffected for NGA < $4.5x10^{16}$ /cm^3.
2. However, we observe significant mobility degradation for each increased value of NGA.
3. Mobility degradation is more sensitive to NGA variations at higher values of NGA.
4. For NGA=$9x10^{16}$/cm^3, $\sqrt{\frac{I_D}{g_m}}$ plot is no longer linear, but a slight bump is observed. This is because the increased scattering brings about significant degradation in current, making V_{TH} extraction process spurious, and it under-predicts the V_{TH} e.g. extracted V_{TH}=0.5 V in Fig.7.6(f)



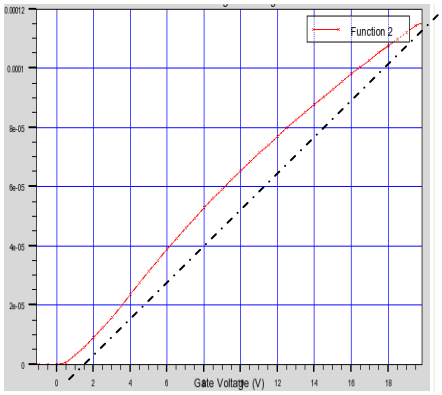
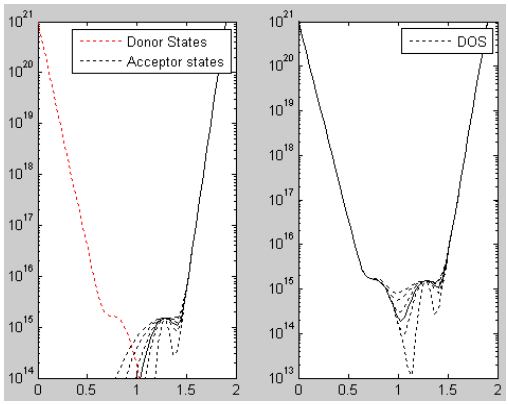


Fig.7.7 (e) I_D for NGA=$9x10^{16}$/cm^3 (f) $\sqrt{I_D/g_m}$ for NGA=$9x10^{16}$/cm^3

(IV) WGA variation at NGA=1.5 x10^{15}, *WGA = [0.06, 0.15, 0.3]*



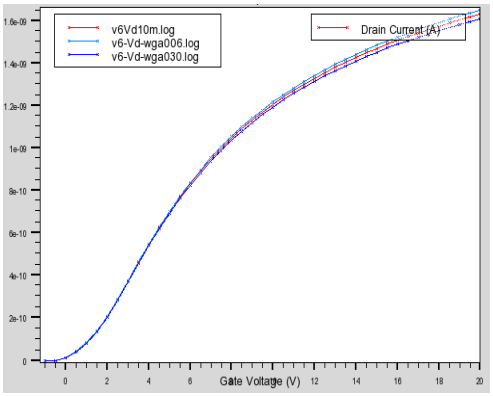
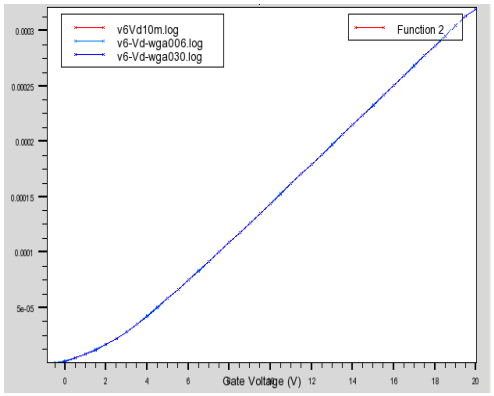


Fig.7.8 (a) WGA variations and DOS (b) ID-VG plots with WGA varied



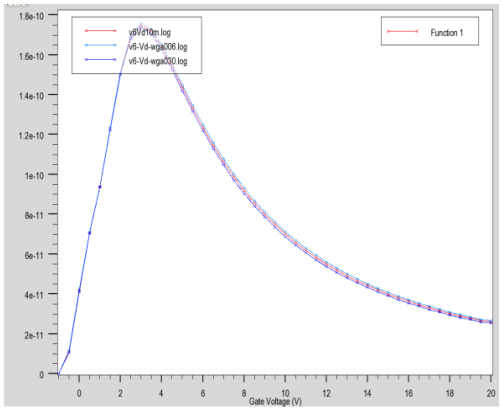


Fig.7.8 (c) $\sqrt{\frac{I_D}{g_m}}$ -V_G plots with WGA varied (d) g_m plots with WGA varied

We observe that:

1. WGA defines the spread for the Gaussian distribution of acceptor traps
2. Mobility remains unaffected by WGA variation for NGA =1.5x10^{15}/cm^3
3. Threshold voltage remains unaffected (1.66 V) for NGA=1.5x10^{15} /cm^3
4. However, from the inspection of DOS plot, we can expect more pronounced effect of WGA at higher NGA.

(V) WGA variation at NGA=1.5 x10^{16} *WGA = [0.06, 0.15, 0.3]*

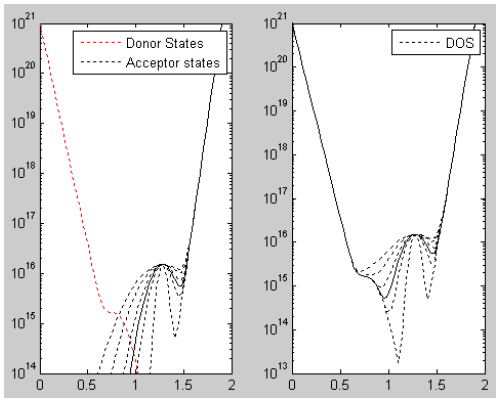
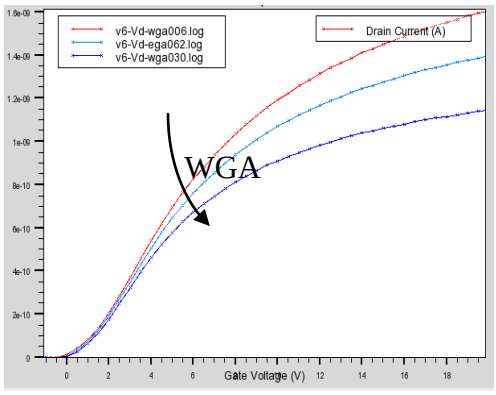


Fig.7.9 (a) WGA variations and DOS



(b) I_D plots with WGA varied

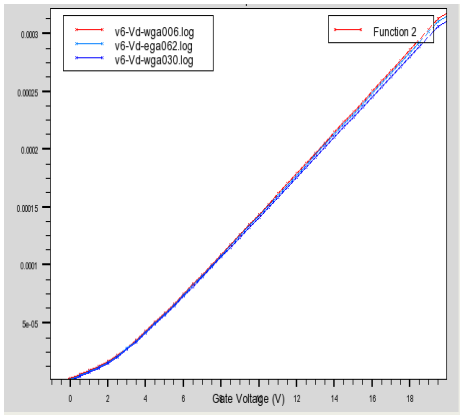
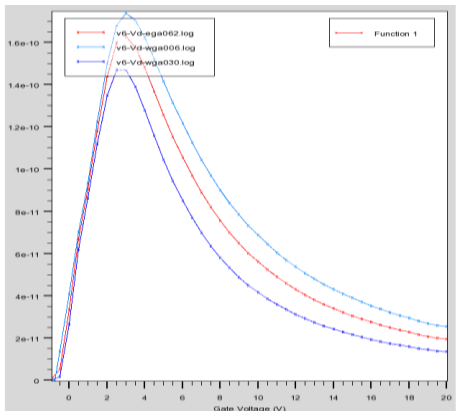


Fig.7.9 (c) $\sqrt{\frac{I_D}{g_m}}$ plots with WGA varied



(d) g_m plots with WGA varied

We observe that:

1. Kp (=3x10^{-9} A/V) stays more or less the same even for NGA=1.5x10^{16}/cm^3 i.e. low-field mobility remains unaffected.
2. Similarly V_{TH} also stays the same (1.66 V).
3. However, mobility degradation with increased Gaussian spread is much more for this value of NGA as expected.
4. This mobility degradation is effectively modeled by introducing non-zero R_D=R_S in the simplified drain current equation. Value of R_D is found for

the best fit using MATLAB code using equation $I_D = KV_D/(1+KR_{SD})$ where K= Kp (V_G-V_{TH}-V_D/2), and V_{TH}, Kp have already been extracted from $\sqrt{I_D/g_m}$ plot. Interestingly, R_{SD}=R_S+R_D was found to be a perfectly linear function in terms of WGA.

5. For WGA=[0.06 0.15 0.3],R_{SD}=[4.3e8 5.3e8 6.9e8]
6. R_{SD} in itself describes mobility degradation coefficient θ, where I_D= $KV_D/(1+ \theta(V_G-V_{TH}-V_D/2))$ as explained earlier.

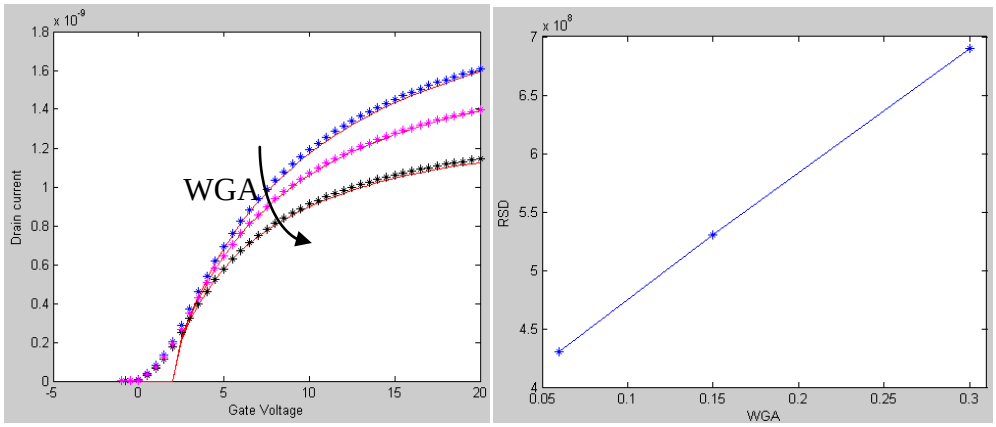


Fig.7.9 (e) R_{SD} model performance (f) R_{SD} versus WGA plot

(VI) WTA variation at NGA=1.5 x10^{16} *WTA = [0.015 0.024 0.033 0.040 0.045]*

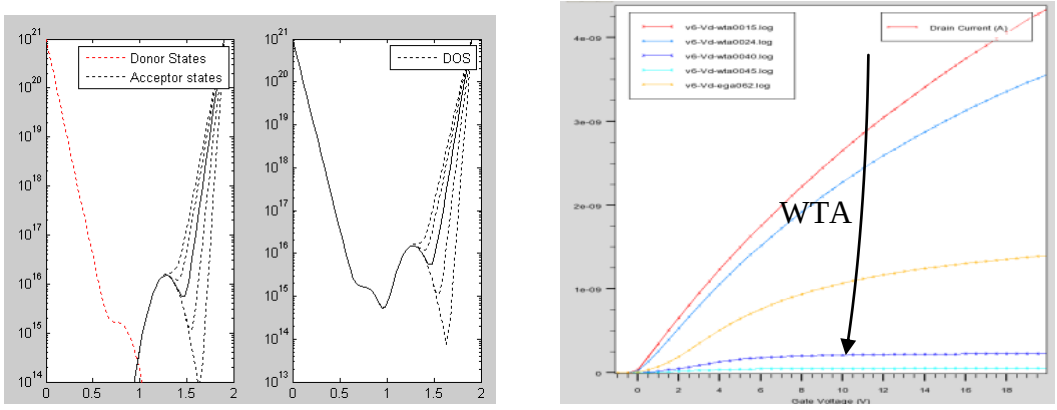
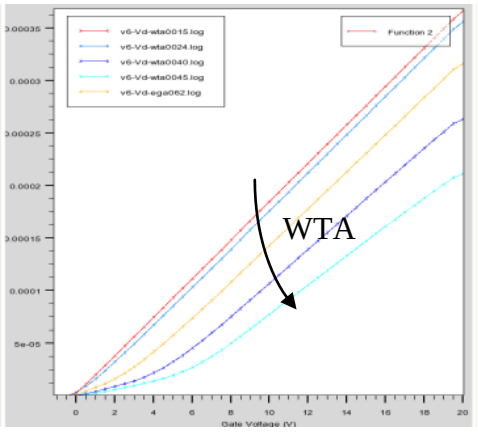


Fig.7.10 (a) WTA variations and DOS (b) I_D plots with WTA varied



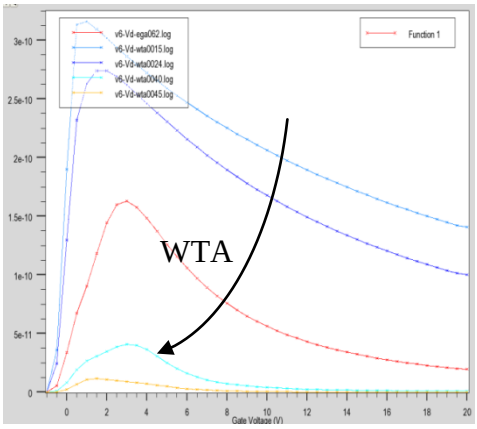


Fig.7.10 (c) $\sqrt{I_D/g_m}$ plots with WTA (d) g_m plots with WTA varied varied

We observe that:

1. WTA increment increases density of tail band acceptor traps drastically as can be seen on the plot above (Fig.7.9(a)). Because tail band acceptor traps are very close to conduction band, there is more frequent electron trapping, carrier low-field mobility is therefore reduced drastically (Fig.7.9(c)). "A" factor decreases.

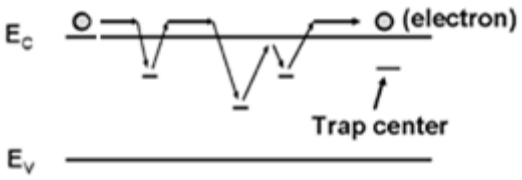


Fig.7.10 (e) Electron trapping and WTA

2. V_{TH} goes on increasing with increase in WTA. This is again because of the increased tail band trap levels.
3. High-field mobility degradation is more pronounced for wider spread of the tail band states, as expected.
4. V_{TH} is very close to 0 for WTA=0.015, Vth versus WTA was found to be approximately parabolic in shape.

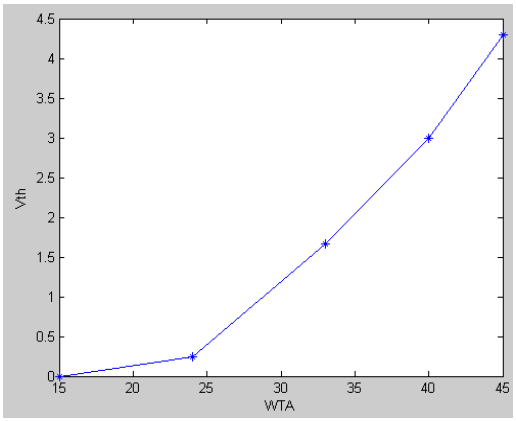


Fig.7.10 (f) Threshold voltage as a function of WTA

From the results obtained, it may be inferred that:

1. Device performance degrades as density of acceptor trap states is increased.
2. Performance degradation is more sensitive to variations in trap state density, at higher density of acceptor traps. Mathematically, $\left|\frac{\delta\, ID}{\delta NGA}\right|, \left|\frac{\delta\, ID}{\delta WGA}\right|, \left|\frac{\delta\, gm}{\delta NGA}\right|, \left|\frac{\delta\, gm}{\delta WGA}\right|, \left|\frac{\delta\, VTH}{\delta WGA}\right|, \left|\frac{\delta\, VTH}{\delta NGA}\right|$ etc. get larger for large values of NGA
3. Spread of the deep level states begins to manifest itself into the device performance only for significantly high density of deep level states.
4. Tail band acceptor trap states are the most crucial traps for n-MOS SOI. The tail states not only change the mobility-factor, but also cause a shift in threshold voltage. Device performance is therefore very much sensitive to the parameters associated with tail band acceptor traps states, namely WTA, NTA, EG300 (defining E_C).

Conclusion:

The quality of a-Si:H material directly determines the TFT device performance. As was explained in chapter for “a-Si:H Technology Considerations”, it is very important to carefully choose process conditions such as ambient temperature for deposition, pressure, feed gas composition, process sequence, plasma power and frequency to optimize the electrical device performance by reducing the density of states.

CHAPTER 8

MOBILITY VARIATION

The most common problem that a-Si:H TFT technology faces is mobility degradation with time. Simulations were carried out by varying low field mobility (mun) parameter alone, keeping all other material parametersconstant. As mentiioned in earlier chapters, the most common values for electron mobility in the case of amorphpus silicon falls in the range 0.1 cm^2/V-sec to 1 cm^2/V-sec. Following drain current characteristics were obtained for mun = 0.1, 0.3, 0.7, 1 cm^2/Vsec.

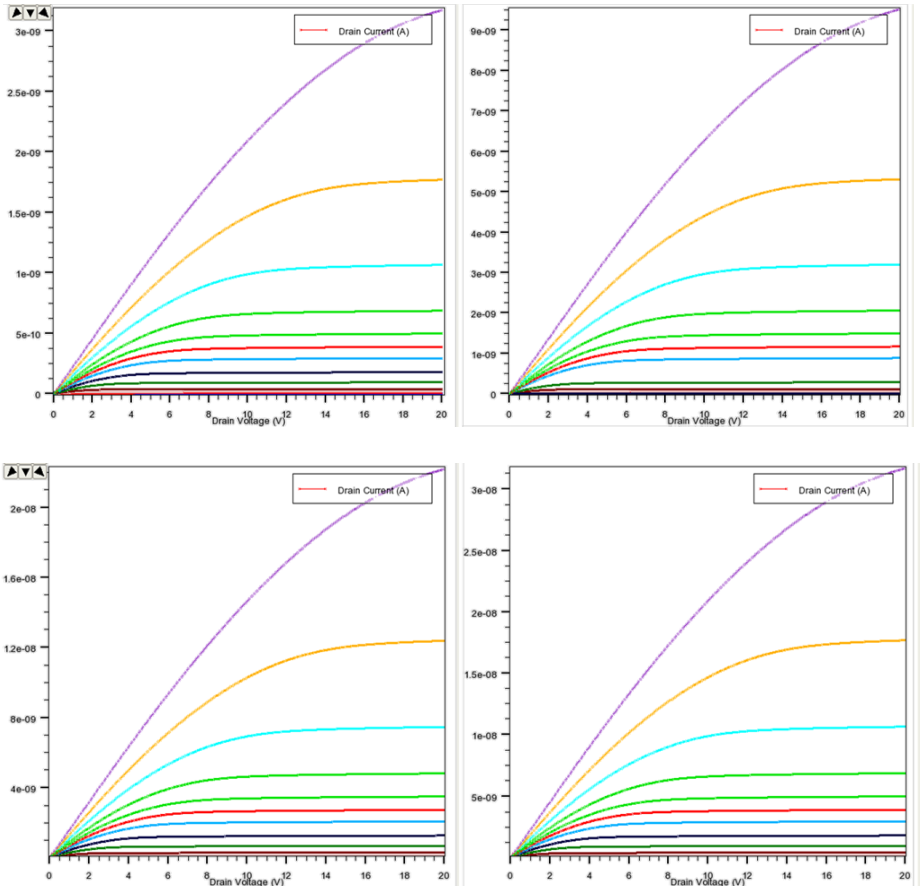


Fig. 8.1 I_D versus V_{DS} for mun= (a) 0.1 (b) 0.3 (c) 0.7 (d) 1 cm^2/Vsec

For V_{GS} varied= [0 1.2 2 2.8 3.6 4.8 6 7.2 8 8.8 10 12 15 20] V, L=16 µm

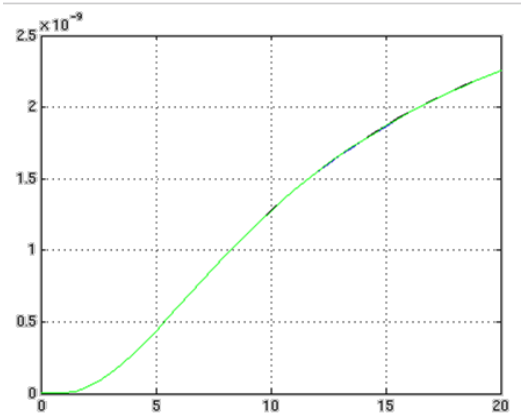


Fig. 8.2 $10I_D$, $3.33I_D$, $1.43I_D$ and I_D versus V_{GS} at V_{DS} = 1 V

for μ_n = 0.1, 0.3, 0.7, 1 cm^2/Vsec respectively

Mobility variation is not expected to change parasitic capacitance values much. With higher μ_n however, it is easier for electrons to respond to applied changes in the terminal voltage, which will increase capacitance values slightly.

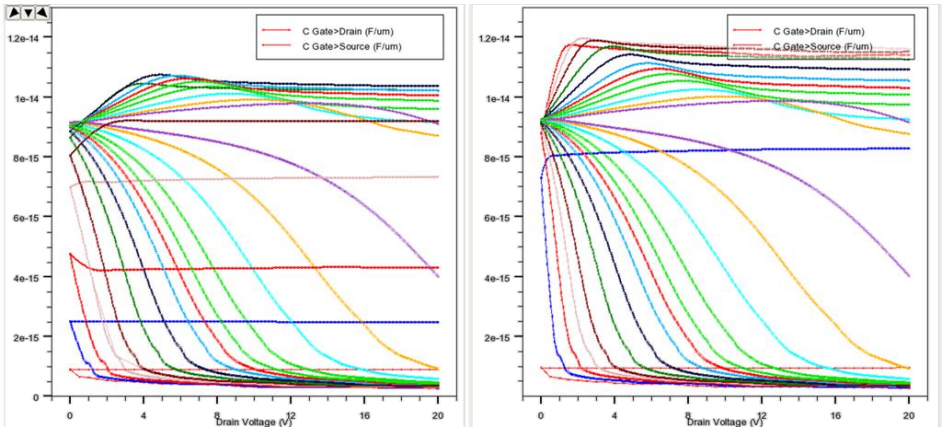


Fig. 8.3 C_{GS},C_{GD} versus V_{DS} for μ_n=0.1 and 1cm^2/Vsec

For V_{GS} varied as [0 1.2 2 2.8 3.6 4.8 6 7.2 8 8.8 10 12 15 20] V, L=16 µm

Conclusion:

Simulation results showed only the scaling of the drain current as one would expect, and no other change in terms of device performance.

CHAPTER 9

USE OF SILICON NITRIDE AS A DIELECTRIC MATERIAL

Use of silicon nitride as the gate dielectric material is very common in a-Si:H TFT technology for reasons explained in chapter four "a-Si:H Technology Fabrication Considerations". Silicon nitride also possesses an advantage over silicon dioxide in terms of dielectric constant. It has a relative permittivity (~7.6) which is almost twice as large as that of silicon dioxide (~3.7). The higher dielectric constant leads to higher drain currents for the same gate thickness. Higher drain currents were observed in the simulation results as one would expect from the Pao-Sah model for drain current.

The device definition:

Structurally the device will be similar to the one in figure 6.1, gate dielectric material being silicon nitride instead of silicon dioxide.

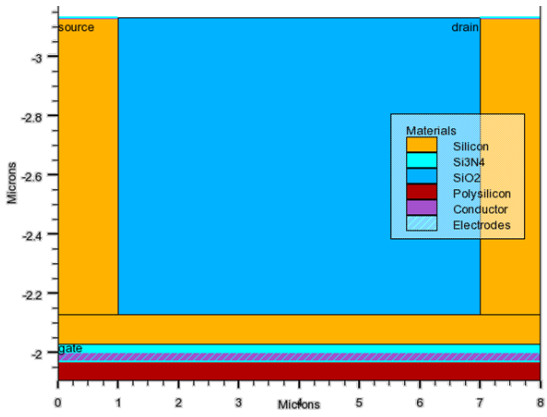


Fig.9.1 The device structure

By default, device in Silvaco has width=1 μm. Gate lengths were varied from 6 μm to 16 μm to 56 μm. Gate dielectric thickness (t_{ox}) chosen for simulations was 30nm, while thickness of the active area (t_{Si}) was chosen to be

100nm. n+ doping for S/D contacts was chosen to be $10^{17}cm^{-3}$. So for as definition of a-Si:H is concerned, most commonly used values were used as shown below (from the literature survey):

Material properties: mun=0.4 mup=0.05 nc300=2.5e20 nv300=2.5e20 eg300=1.9

Defect density: nta=1e21 ntd=1e21 wta=0.033 wtd=0.049 nga=1.5e15

ngd=1.5e15 ega=0.62 egd=0.78 wga=0.15 wgd=0.15

sigtae=1e-17 sigtah=1e-15 sigtde=1e-15 sigtdh=1e-17

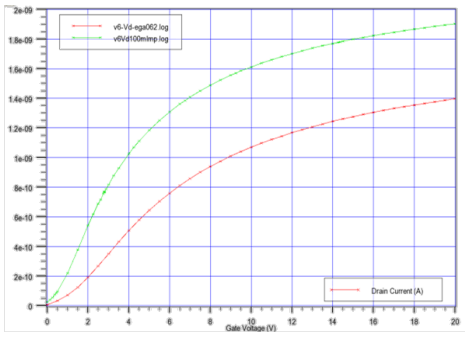
siggae=2e-16 siggah=2e-15 siggde=2e-15 siggdh=2e-16

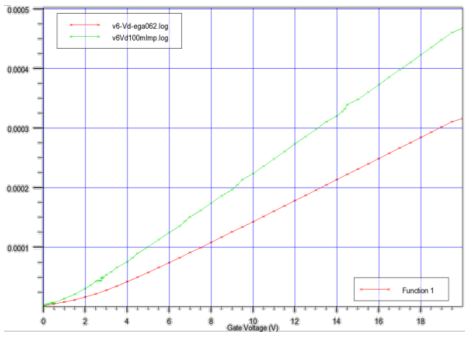
Simulations:

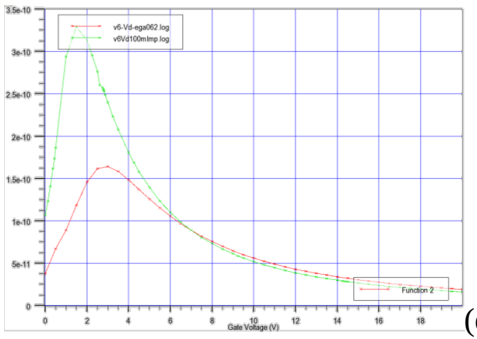
V_{GS} was swept from 0 to 20V for V_{DS} = 10, 50, 100 and 500 mV to extract and re-check V_T. To make sure the model works for range of biasing conditions, V_{DS} was swept from 0 to 20V at discrete values of V_{GS} in the range 0-20V.

Results:

Drain current, trans-conductance and parasitic capacitances increase as we use silicon-nitride instead of silicon-dioxide as a gate dielectric.

(a) 

(b) 

(c) 

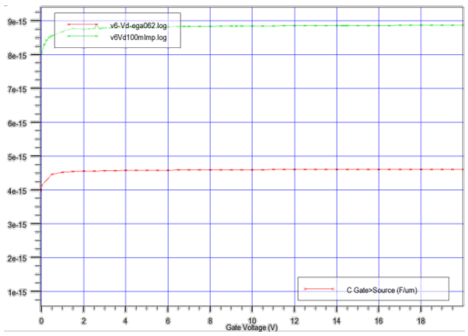
(d) 

Fig. 9.2 (a) I_D and (b) $I_D/\sqrt{g_m}$ (c) g_m (d) C_{gs} versus V_{GS} plots for L = 6 µm, V_{DS}=100mV for silicon-nitride (Green) and silicon-dioxide (red) as gate dielectric

Following plots (figures 9.3 to 9.8) correspond to devices with different device gate lengths, with silicon-nitride as gate dielectric for each.

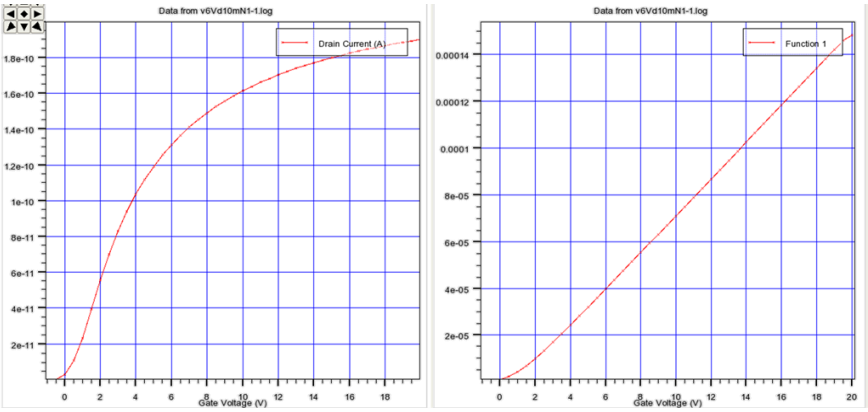


Fig. 9.3 (a) I_D and (b) $I_D/\sqrt{g_m}$ versus V_{GS} plots for L = 6 µm, V_{DS} = 10 mV

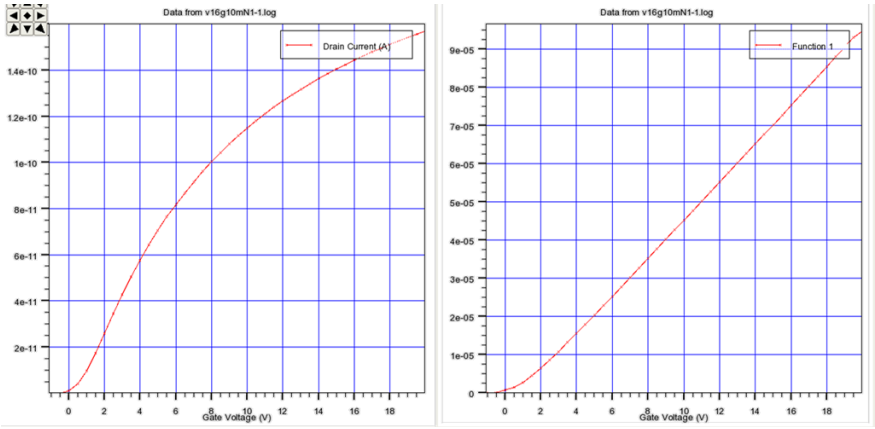


Fig. 9.4 (a) I_D and (b) $I_D/\sqrt{g_m}$ versus V_{GS} plots for L = 16 µm, V_{DS} = 10 mV

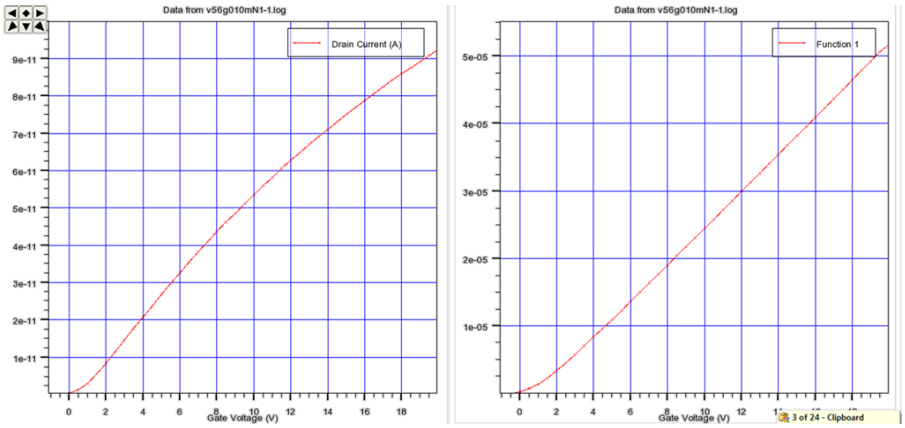


Fig. 9.5 (a) I_D and (b) $I_D/\sqrt{g_m}$ versus V_{GS} plots for L= 56 µm, V_{DS} = 10 mV

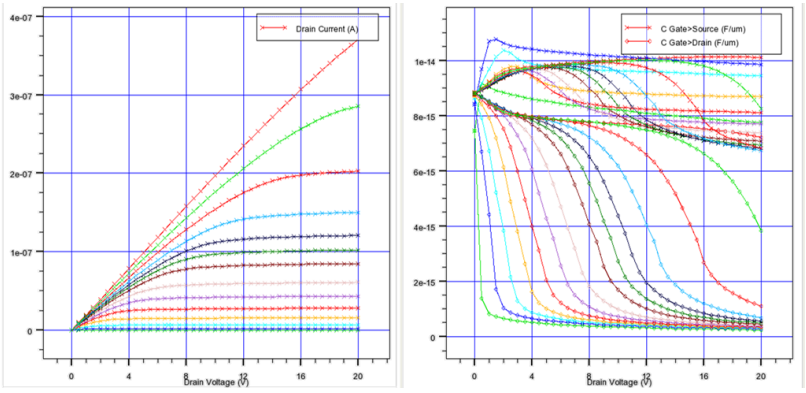


Fig. 9.6 (a) I_D (b) C_{GS},C_{GD} versus V_{DS} plots

for L = 6 µm, V_{GS} varied as [0 1 2 3 4 5 6 7.2 8 8.8 10 12 15 20] V

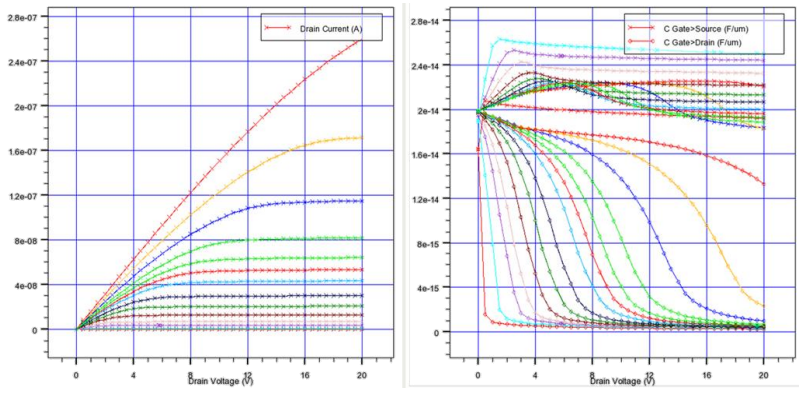


Fig. 9.7 (a) I_D (b) C_{GS},C_{GD} versus V_{DS} plots

for L=16 µm, V_{GS} varied as [0 1 2.2 3 4 5 6 7.2 8 8.8 10 12 15 20] V

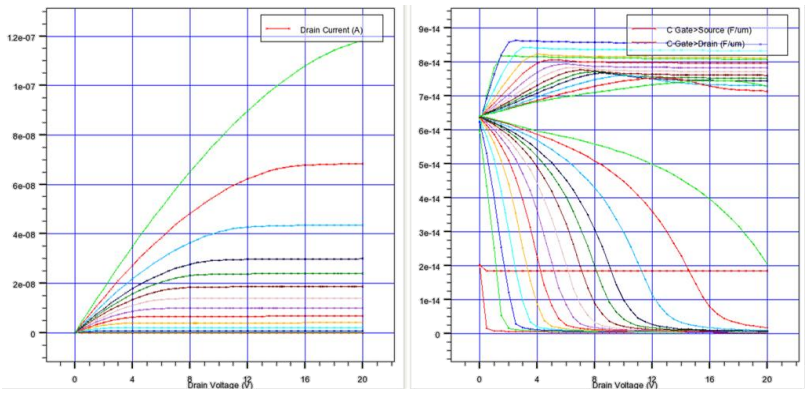


Fig. 9.8 (a) I_D (b) C_{GS},C_{GD} V_{GS} plots

for L= 56 μm, V_{GS} varied as [0 1.2 2 3 4 5 6 7 8 9 10 12 15 20] V

These device characteristics were further used to extract of compact model parameters.

CHAPTER 10

CADENCE-COMPATIBLE MODEL DEVELOPMENT

Simulating an integrated circuit to first verify its successful operation at the transistor level before committing it to the manufacturing is an industry-standard because it is not possible to breadboard the integrated circuit for testing purposes before the manufacture. Also, the high costs of manufacturing processes make it essential to design the circuit to be as close to perfect as possible before the integrated circuit is first built, and use of Electronic Computer Aided Design (ECAD) tools therefore becomes indispensable. ECAD tools use simplified analytical models to estimate the key circuit related parameters such as the circuit operating point and gain/bandwidth. This enables the circuit designer to concentrate on the bigger picture without having to bother about intricate device physics involved saving computational efforts and time.

Berkeley SPICE Models

Use of models developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley has become a common standard. Berkeley SPICE has four different MOSFET models of varying complexity (and thus simulation time) and accuracy. The Level 1 model, also called the Shichman-Hodges model, is a first order model suitable for device with a channel length of greater than 2 μm. The Level 2 model includes the second-order effects including lateral and vertical field dependent mobility model which become important for devices smaller than 2 μm. The Level 3 model, which is a semi-empirical model, has a better mobility

model. Following these models are the second generation BSIM and BSIM2, and third generation BSIM3. These different models can be activated by a parameter called LEVEL. [9]

A Cadence-compatible model was developed to allow rough estimation of circuit operation. Sufficiently accurate characteristics were achieved using level 1 Model. For this, it is important to understand role that every model parameter plays first.

Parameter name in the text	SPICE parameter name	Parameter description	Default value	Units
Level			1	
V_{To}	VTO	Zero-bias threshold voltage	0.0	V
κ	KP	Transconductance parameter	$2 \cdot 10^{-5}$	A/V^2
γ	GAMMA	Body factor	0.0	
μ_0	UO	Low field mobility	600	$cm^2/V \cdot S$
$2\phi_f$	PHI	Surface potential in strong inversion	0.1	V
λ	LAMBDA	Channel length modulation factor	0.0	V^{-1}
N_b	NSUB	Substrate Doping	0.0	m^{-3}
t_{ox}	TOX	Gate oxide thickness	10^{-7}	m
N_{ss}	NSS	Surface state density	0.0	cm^{-2}
—	TPG	Type of the gate material	1	—
I_s	IS	Bulk junction saturation current	10^{-14}	A/m^2
J_s	JS	Bulk junction saturation current per sq-meter of the junction area	10^{-14}	A
R_s	RS	Source ohmic resistance	0.0	Ω
R_d	RD	Drain ohmic resistance	0.0	Ω
ρ_s	RSH	Source, Drain diffusion sheet resistance	∞	Ω/□
—	CBS	Zero-bias B-S junction capacitance	0.0	F
—	CBD	Zero-bias B-D junction capacitance	0.0	F
C_{jo}	CJ	Zero-bias bulk junction capacitance per sq-meter of the junction area	0.0	F/m^2
m_j	MJ	Bulk junction bottom grading coefficient	0.5	—
ϕ_{bi}	PB	Bulk junction potential	0.8	V
C_{jswo}	CJSW	Zero-bias bulk junction side-wall capacitance per meter of the junction perimeter	0.0	F/m
m_{jsw}	MJSW	Bulk junction side wall grading coefficient	0.5	—
C_{gso}	CGSO	Gate-source overlap capacitance per meter channel width	0.0	F/m
C_{gdo}	CGDO	Gate-drain overlap capacitance per meter channel width	0.0	F/m
C_{gbo}	CGBO	Gate-bulk overlap capacitance per meter channel length	0.0	F/m
—	KF	Flicker noise coefficient	0.0	—
—	AF	Flicker noise exponent	1	—

Figure 10.1 SPICE Level 1 Model Parameters [4]

Equations for Level-1, Meyer Model)

1. DC Model equations:

$$V_{th} = V_{TO} + \gamma(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f})$$
$$V_{dsat} = V_{gs} - V_{th}$$

$$I_{ds} = \beta_0 \left[(V_{gs} - V_{th} - \tfrac{1}{2}V_{ds})V_{ds}\right](1 + \lambda V_{ds})$$

Linear region, $V_{gs} > V_{th}$ and $V_{ds} \leq V_{dsat}$

$I_{ds} = 0.5\beta_0 (V_{gs} - V_{th})^2 (1 + \lambda V_{ds})$ Saturation region, $V_{gs} > V_{th}$ and $V_{ds} \leq V_{dsat}$

$I_{ds} = 0$ Subthreshold region, $V_{gs} \leq V_{th}$

Where $\beta_0 = k(W/L)$ and $k = \mu_0 C_{ox}$

2. Capacitance Model equations:

$$C_{BS} = \frac{C_{j0}}{\left(1 - \frac{V}{\phi_{bi}}\right)^{m_j}} + \frac{C_{jsw0} P_s}{\left(1 - \frac{V}{\phi_{bi}}\right)^{m_{jsw}}}$$

where A_s and P_s are area and periphery of the source-to-bulk junction, C_{j0} and C_{jsw0} are junction capacitance per unit area and per unit periphery respectively at zero back bias. Similar equation holds for C_{BD}.

1. Strong Inversion Region ($V_{gs} > V_{th}$)

   a. Linear Region: In this case, $V_{gs} > (V_{th} + V_{ds})$

$$C_{GS} = \frac{2}{3} C_{oxt} \left[1 - \frac{(V_{gd} - V_{th})^2}{(V_{gd} + V_{gs} - 2V_{th})^2}\right]$$

$$C_{GD} = \frac{2}{3} C_{oxt} \left[1 - \frac{(V_{gs} - V_{th})^2}{(V_{gd} + V_{gs} - 2V_{th})^2}\right]$$

$$C_{GB} = 0$$

b. Saturation Region: In this case, $V_{gs} > (V_{th} + V_{ds})$

$C_{GS} = \frac{2}{3} C_{oxt}$

$C_{GD} = 0$

$C_{GB} = 0$

where $C_{oxt} = WLC_{ox}$

2. Weak Inversion Region ($V_{gs} < V_{th}$)

a. When $(V_{th} - \phi_f) < V_{gs} < V_{th}$

$C_{GS} = \frac{2}{3} C_{oxt} \left(\frac{V_{gs} - V_{th}}{\phi_f} + 1 \right)$

$C_{GD} = 0$

$C_{GB} = C_{oxt} \left(1 + \frac{4}{\gamma} (V_{gb} - V_{fb}) \right)$

b. When $V_{gs} < (V_{th} - 2\phi_f)$

$C_{GS} = 0$

$C_{GD} = 0$

$C_{GB} = C_{oxt}$

The overlap capacitances C_{GSO},C_{GDO} and C_{GBO} are then added to C_{GS}, C_{GD} and C_{GB} respectively, and are calculated from following equations.

$C_{GSO} = C_{gso} W$,

$C_{GDO} = C_{gdo} W$

$C_{GBO} = C_{gbo} L$

The procedure

Parasitic capacitances, and drain current versus V_{GS} plots at V_{DS} =100mV were analyzed and basic model parameters were extracted. Parameters were extracted using the procedure explained in chapter 7. Performance of the model, thus obtained, was assessed by comparing model-generated plots and SILVACO-generated plots. Performance assessment was done on parasitic capacitances, and drain current v/s V_{DS} plots at discrete V_{GS} values in the range 0V to 20V.

.MODEL V6SIN NMOS (level=1

+uo=0.4	Vto=1	lambda=0.005	
+Rs=21e6	Rd=21e6	nsub=1e13	tox=30e-9
+capmod=2	cgbo=0	cgso=1e-9	cgdo=1e-9)

Performance Assessment of the Model V6SIN

The model file was tested against observations from SILVACO simulation results. The model is reasonably accurate for a range of device lengths, from 6 microns to at least 56 microns as shown. This is sufficient to perform rudimentary circuit design.

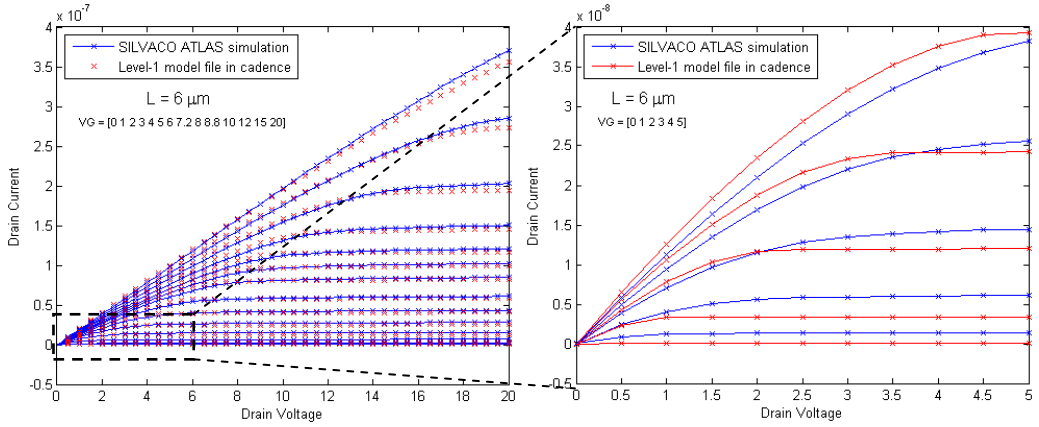


Fig.10.2 Model performance for L= 6µm (Test conditions specified on the plots)

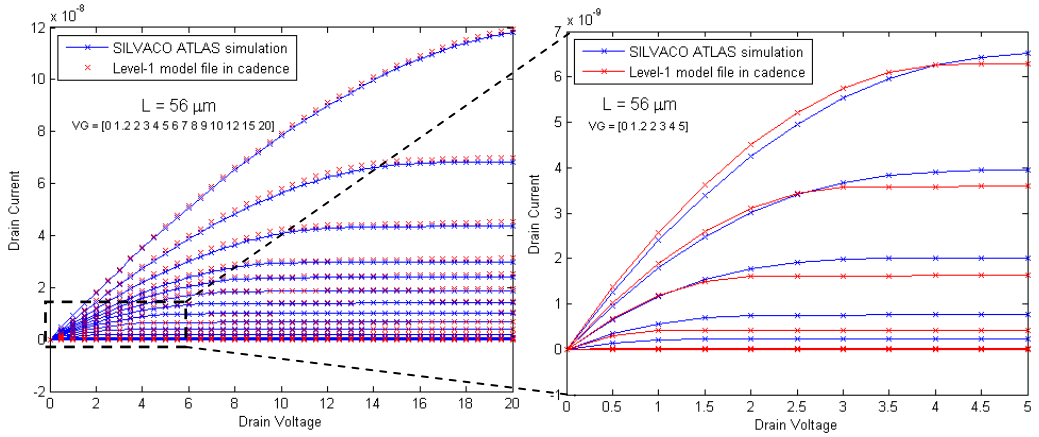


Fig.10.3 Model performance for L= 56µm (Test conditions specified on the plots)

CHAPTER 11

OP-AMP DESIGN

Because a-Si:H TFT is a low mobility transistor, the technology has rarely if ever been applied for core analog circuits like operational amplifiers. An attempt was made to design an op-amp that can drive the load resistance and capacitance of the ECRS. It is a two-stage operational amplifier based on the NMOS model (V6SIN.m) corresponding to the device with low field electron mobility = 0.4 cm^2/Vsec.

The Design:

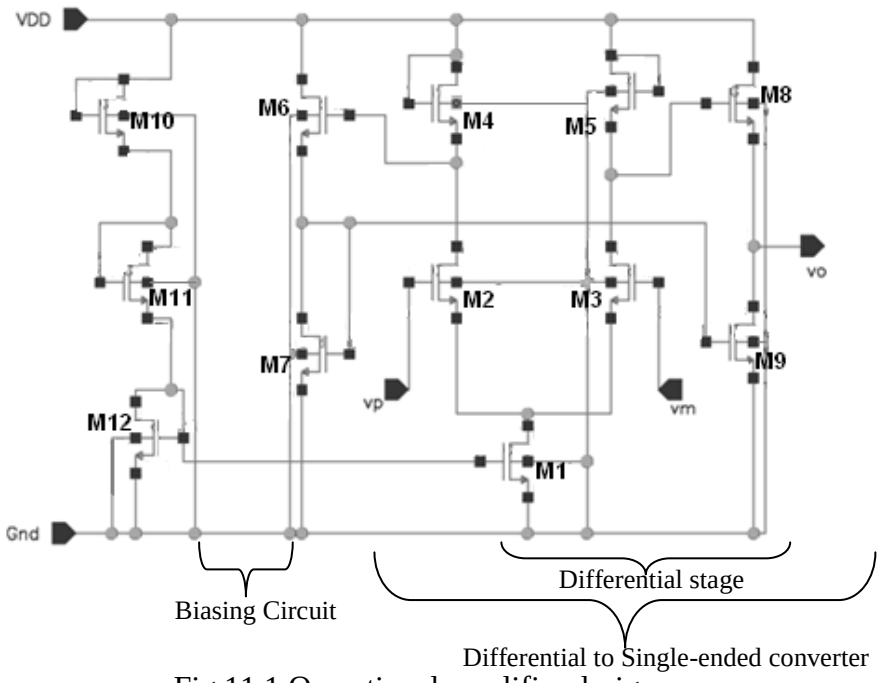


Fig.11.1 Operational amplifier design

As described in the circuit diagram above, leftmost stage provides biasing to the tail current supply transistor M1 which drives the first stage which is differential input stage. Second stage carries out differential to single ended conversion also improving output driving capability.

Sizing constraints:

For the differential stage, differential gain A_{dm1}, is given by $A_{dm1}=g_{m2}/g_{m4}$, and common mode gain A_{cm1} is given by $(2r_{O1}\, g_{m4})^{-1}$. For the second stage, differential to single ended gain is $A_{dm2} = \frac{g_{m8}r_{O9}}{2(1+g_{m8}r_{O9})}\left[1+\frac{g_{m6}g_{m9}}{g_{m8}(g_{m6}+g_{m7})}\right]$, while common mode gain A_{cm2} being $\frac{g_{m8}r_{O9}}{(1+g_{m8}r_{O9})}\left[1-\frac{g_{m6}g_{m9}}{g_{m8}(g_{m6}+g_{m7})}\right]$ [10]. We size transistors in our design so as to have overall maximum differential gain and low common mode gain. While doing this, a care must be taken so as to have high phase (possibly greater than 45^o) and high gain margins so that the amplifier output is stable.

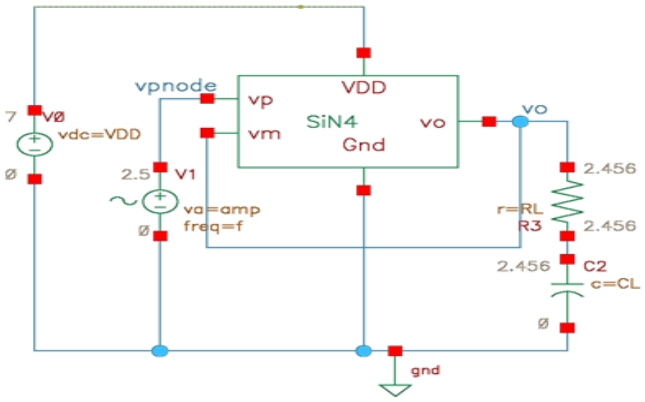
Other sizing constraints have to do with current drive capability of the stages and parasitic capacitances affecting frequency response of the amplifier. To increase load driving capability of the last stage, we need to increase W/L for M8 and M9. This is because, larger the load (i.e. smaller the resistance), more amount of current needs to be supplied. However, W/L cannot be increased to a very high value, as capacitive parasitics associated with this stage load the differential stage affecting its frequency response.

Similarly, we have restriction on W/L ratio of M2 because of the capacitive parasitics associated with M2. On account of these parasitics, we cannot increase gain of the first stage ($A_{dm1}=g_{m2}/g_{m4}$) by simply increasing size of M2 indefinitely. Instead, trans-conductance of M2 is increased by forcing higher amount of current by increasing W/L ratio for M1.

Also, to increase A_{dm1}, W/L for M4 cannot be decreased to a too low value, bias point for the second stage, correspondingly output swing and associated non-linearity considerations must be taken into account.

Test Bench:

The performance of op-amp was tested in the test bench shown in Figure 11.2 by connecting it in unity follower configuration. The output is shown in Figure 11.3. It can be concluded from this simulation amplifier thus built is stable for these specified load and input frequency conditions.



R_L = 20Mohms

C_L = 1nF

V_{DD} = 7V-8V

V_{CM} range = 2V-3.5V

Fig.11.2 Test bench

Output:

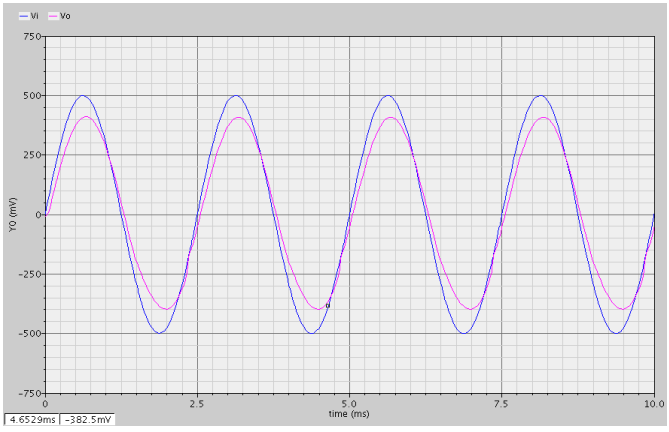


Fig.11.3 Output for the voltage follower

CHAPTER 12

MASK DESIGN

A mask set incorporating a large number of test devices and circuits was designed using AutoCAD software. Purpose of fabricating these test structures is to characterize and assess performance of the simulated devices and circuits real-time and develop more realistic compact models for later use. The files were saved in DXF file format that is compatible with Heidelberg Laser Writer at Center for Solid State Electronics Research (CSSER) at Arizona State University. These designs were drawn as parametric drawings in AutoCAD with appropriately specified geometric constraints (e.g. equality, colinearity, orthogonality, parallels etc.) and parametric dimensional specifications. This grows into a long list of parameters, and it is better to stick to some nomenclature scheme to avoid ambiguity. Nomenclature scheme is explained in the following section.

Nomenclature for dimensional parameters:

1. Typically, L is a dimension along x axis, W along Y axis, subscript indicates a specific layer (indexed by a number) or a specific functionality.

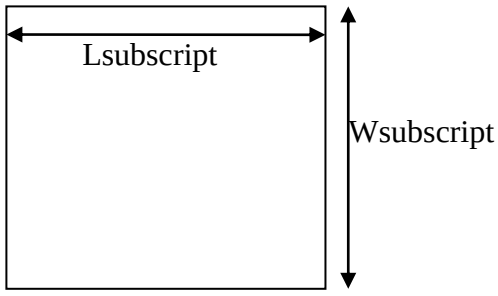


Figure 12.1 Illustration of the naming convention followed-1

2. For layer overlaps, L stands for the word “layer”.
    - x1,y1 => spacing between left bottom corners
    - x2,y2 => spacing between right top corners
    - To differentiate between the dimensions specific to contacts, letter c is used, with appropriate subscript from G, D and S.

For example,

For m=2 (Active Mask), n=1 and For m=4, n=3, c=S (i.e. source in SDI Mask)

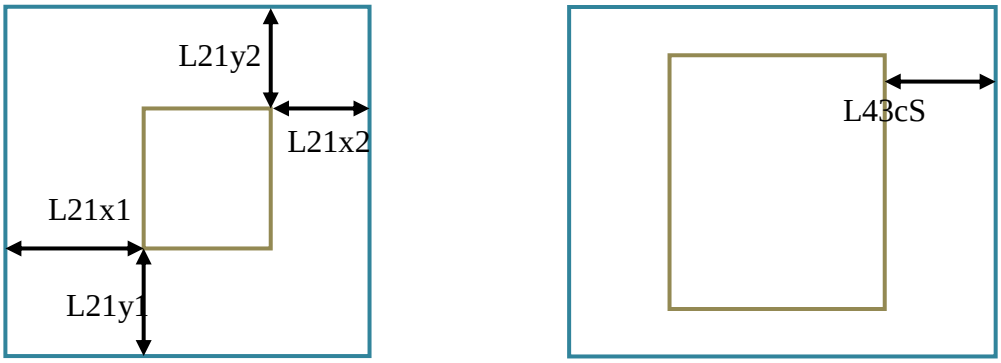
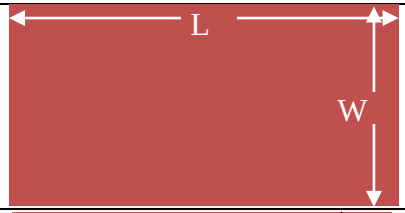
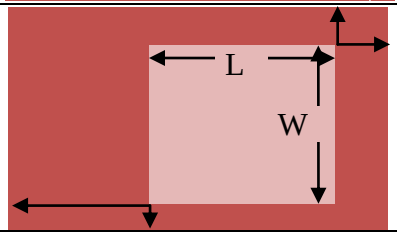
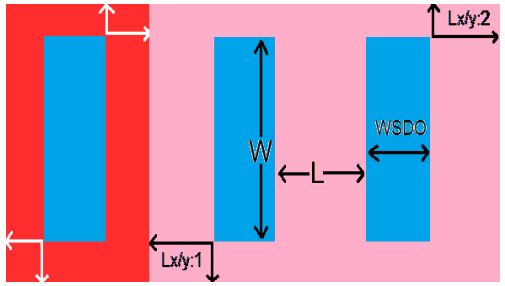


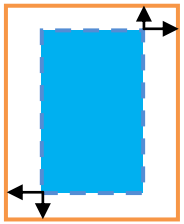
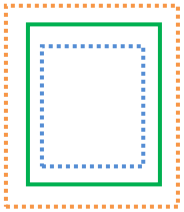
Figure 12.2 Illustration of the naming convention followed-2

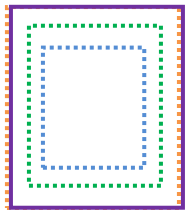
With this nomenclature in place, next few page should help better understand flow of parametric mask designing explained in the introduction above, combined with fabrication steps explained in chapter 4. The process flow described in this table corresponds to fabrication of transistor using our proposed technology.

LAYERS CHART

Table 12.1

Layer	Function	Comments	Independent variables	Driven variables	Figure 12.3 Mask designs
1GATE	Pattern gate terminal: Poly-Si	4-5 μm thick		WG, LG	
2ACTIVE	Pattern active channel: a-Si	100nm thick	L12(x/y)(1/2)=5 μm	WA, LA	
3SDO	Etch away dielectric and form openings for G,S,D	2 μm thick SiO_2/SiN_x, stop at a-Si:H	• DeviceW/DeviceL = (W/L here)=100/10 • WSDO=5 μm • L23(x/y)(1/2)=5 μm	None, we define device from here	

4SDI	Isolate G,S,D by etching away n+ a-Si:H	1.5 µm thick, stop at SiO_2/SiN_x dielectric.	L34(x/y)(1/2)c(GDS) =2µm	Spacing between SD Si regions (LGD4,LDS4)	For each of the terminals, dimensions marked by arrows are nothing but independent variable here L34(x/y)(1/2)c(G/D/S) 
5CONTACT	Etch contacts to SD regions through dielectric	1 µm thick, stop at a-Si:H	This mask falls between mask3 and mask4 dimensionally, see figure. L45(x-y)(1-2) c(GDS)=L34/2	Spacing between SD CONTACT regions (LGD5,LDS5)	

6METAL	Pattern G/S/D metal to avoid terminal shorts	0.5 μm thick, stop at dielectric	L56(x-y)(1-2) c(GDS) so that *mask 4 and 6 are aligned here.* Even if slightly misaligned, we expect no device failure. Misalignment Margin=4 μm	Spacing between SD CONTACT regions (LGD6,LDS6= LGD4,LDS4 respectively)	

These steps lead us to different layout designs in AutoCAD corresponding to different test structures as shown on the next few pages.

Overall layout of MOSFET:

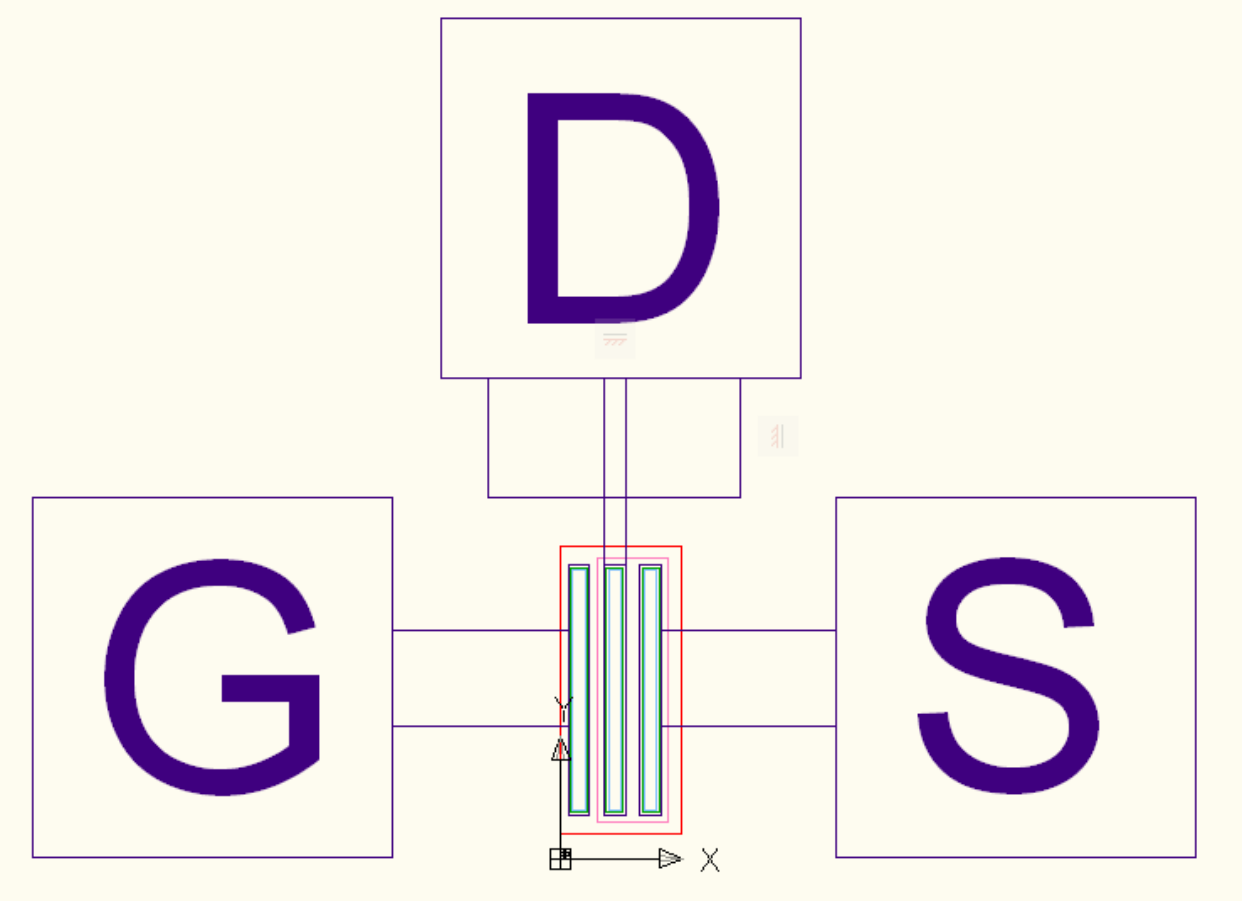


Figure 12.4 Overall Layout

MOSFET layers with dimensional constraints:

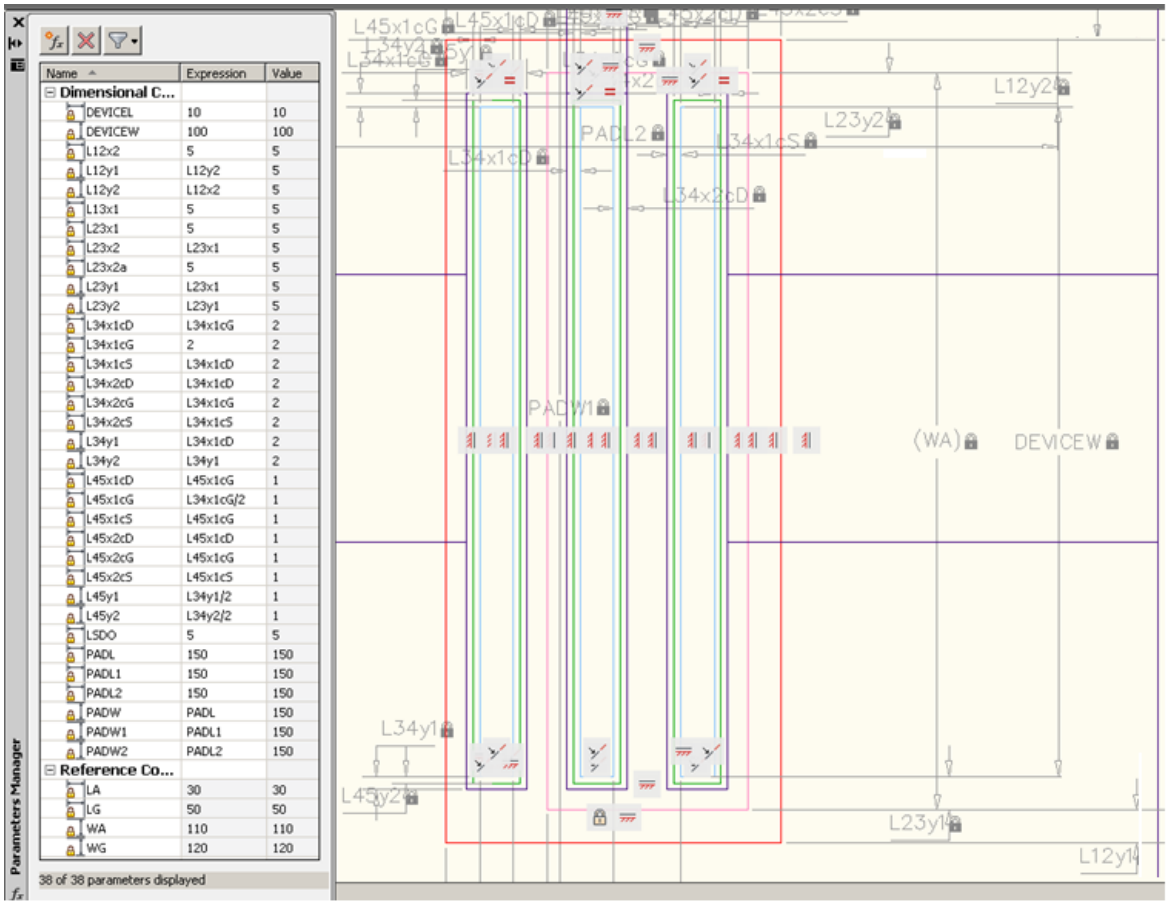


Figure 12.5 AutoCAD Screen shot depicting the MOSFET layers with dimensional constraints

Clean view of the MOSFET:

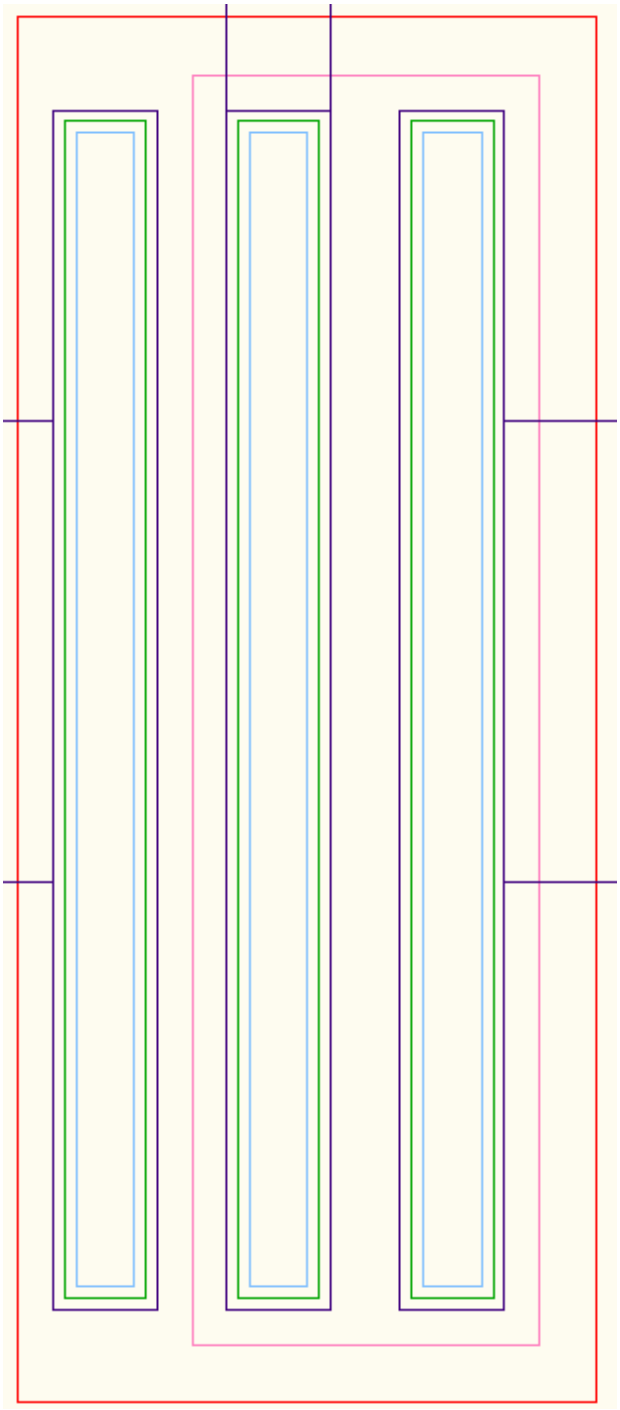


Figure 12.6 Clean view of the MOSFET

Resistor Layout:

1. Essentially, it is a transistor without a contact to the gate
2. SDO mask will have only two windows, and similarly for rest of the masks down the line i.e. SDI, CONTACT and METAL.
3. Single SDO window results in a less resistive resistor, bypassing ACTIVE region.

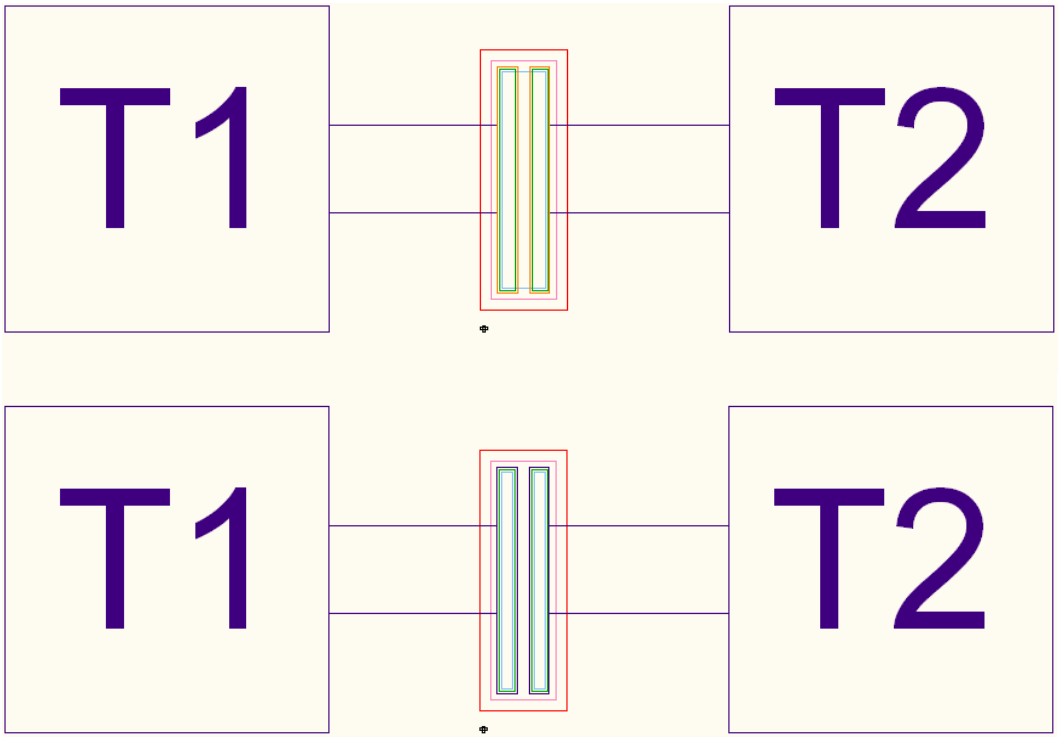


Fig. 12.7 Clean view of the resistor (a) Less resistive bypassing ACTIVE region (b) More resistive where ACTIVE region is in series connection

Capacitor Layout:

1. Source and drain are essentially shorted; other terminal is the gate terminal.
2. ACTIVE mask may pattern active area or etch it away completely.

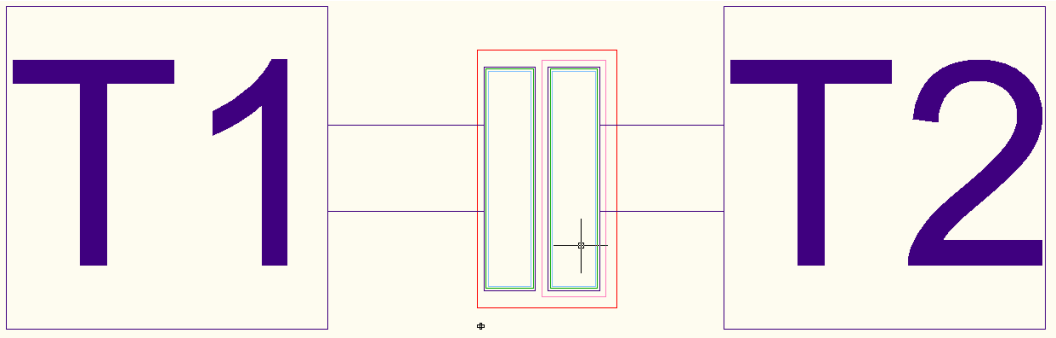


Fig. 12.8 Clean view of the capacitor

Sensor Layout:

1. GATE mask patterns out gate metal in the serpentine pattern
2. ACTIVE and SDI mask etches all of a-Si:H and stop at dielectric material
3. SDO, CONTACT and METAL etches away all the dielectric in the trench and also where terminal contact needs to be made.

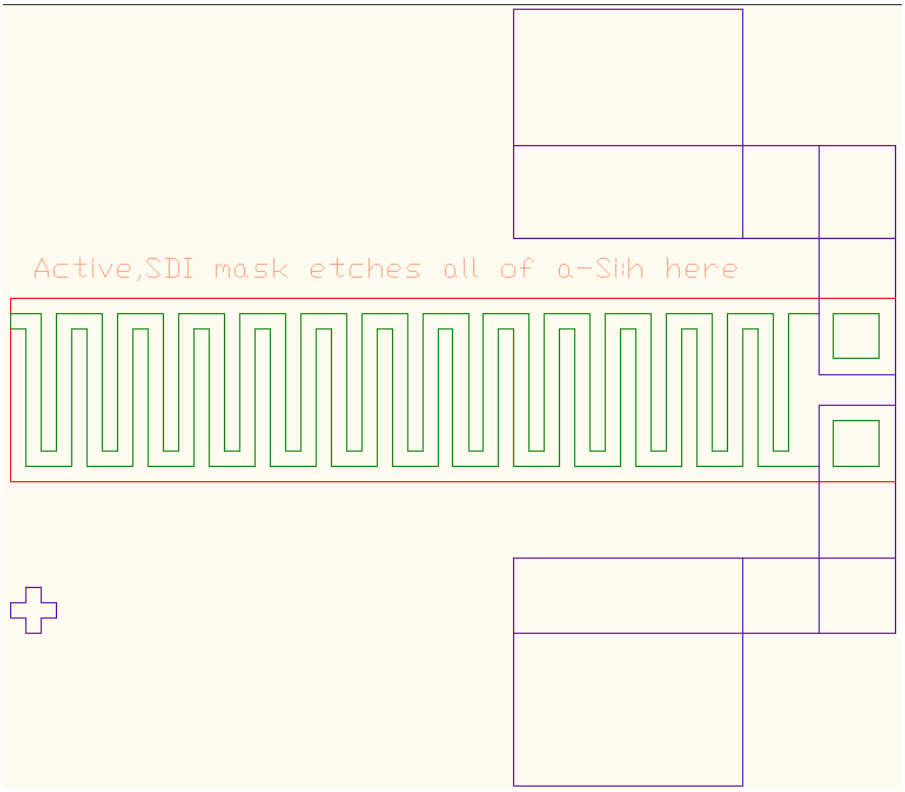


Fig. 12.9 Clean view of ECRS

File hierarchy system:

Once a parametric drawing is drawn, entire drawing is saved as an AutoCAD block using "block" command. Purpose of using block here is to create file-hierarchy within our design. File-hierarchy helps us make minor modifications to an individual design.

Every single change made to an individual blocks gets implemented for all of the instances of that block all over the wafer. Different structures with varying dimensions are saved as different blocks, with characteristic names given to each of them. Each of these blocks is then arrayed and these arrays are placed next to each other into wafer level AutoCAD design file.

CHAPTER 13

FUTURE WORK

With mask designs ready and the fabrication process considerations charted out, the next step is to fabricate the test structures. These structures need to be probed for range of measurements that characterize the device under different biasing and environment conditions. If necessary, remodeling needs to be done such that analytical expressions corresponding to these models fit the actual measured data. Sensor impedance frequency response as a function of contamination levels, drain current-gate/drain bias characteristics, C-V curves etc. are of primary interest here.

Robust circuit designing for the application in focus and testing the overall system is the conclusive step. With new technologies emerging in ever-growing semiconductor industry, it may also be of interest to see whether further cost cutting is possible through reliable fabrication in reduced number of process steps, or through use of processes that do not require fancy expensive control systems.

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