Adhesion in a Copper-Ruthenium Multilayer Nano-scale Structure and the Use of a Miedema Plot to Select a Diffusion Barrier Metal for Copper Metallization

by

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ABSTRACT

Miedema's plot is used to select the Cu/metal barrier for Cu metallization. The Cu/metal barrier system selected should have positive heat of formation (H_f) so that there is no intermixing between the two layers. In this case, Ru is chosen as a potential candidate, and then the barrier properties of sputtered Cu/Ru thin films on thermally grown SiO_2 substrates are investigated by Rutherford backscattering spectrometry (RBS), X-ray diffractometry (XRD), and electrical resistivity measurement. The Cu/Ru/SiO_2 samples are analyzed prior to and after vacuum annealing at various temperatures of 400, 500, and 600 ^oC and at different interval of times of 0.5, 1 and 2 hrs for each temperature. Backscattering analysis indicate that both the copper and ruthenium thin films are thermally stable at high temperature of 600 ^oC, without any interdiffusion and chemical reaction between Cu and Ru thin films. No new phase formation is observed in any of the Cu/Ru/SiO_2 samples. The XRD data indicate no new phase formation in any of the annealed Cu/Ru/SiO_2 samples and confirmed excellent thermal stability of Cu on Ru layer. The electrical resistivity measurement indicated that the electrical resistivity value of the copper thin films annealed at 400, 500, and 600 ^oC is essentially constant and the copper films are thermally stable on Ru, no reaction occurs between copper films and Ru the layer. Cu/Ru/SiO_2 multilayered thin film samples have been shown to possess good mechanical strength and adhesion between the Cu and Ru layers compared to the Cu/SiO_2 thin film samples. The strength evaluation is carried out under static loading conditions such as nanoindentation testing. In this study, evaluation and comparison is done

based on the dynamic deformation behavior of $Cu/Ru/SiO_2$ and Cu/SiO_2 samples under scratch loading condition as a measure of tribological properties. Finally, the deformation behavior under static and dynamic loading conditions is understood using the scanning electron microscope (SEM) and the focused ion-beam imaging microscope (FIB) for topographical and cross-sectional imaging respectively.

DEDICATION

To my parents and husband

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Chapter 1

INTRODUCTION

A. Diffusion Barrier

Recently the functionality and complexity of circuit components in integrated circuits have increased rapidly. The complex features have been achieved by reduction in the dimensions of both the devices and wiring [1]. This indicates scaling of interconnects. Interconnects are metal lines used to connect various devices on a semiconductor chip and the current flows through them. An ideal interconnect should have the least possible electrical and thermal resistance, adequate thermal stability preventing any phase change and reactivity to the substrate detrimental to the device, no diffusion into the substrate, minimal RC delay, no cross talk, high electromigration resistance, good wettability and adhesion to the substrate or underlying layers, low interfacial stress, compatibility with the process steps such as lithography and etching [2].

The need to reduce circuit delays resulted in the replacement of Al alloy with lower resistivity Cu. To achieve high speed and low power consumption, interconnects must be reliable because the decrease in cross-sectional area of the interconnect line and the increase in frequency cause the current density of interconnects to increase. Because electromigration failure is due to atomic diffusion caused by high electrical current density, the replacement of Al alloy with Cu was expected to enhance to electromigration resistance by the higher

melting point of Cu compared to Al alloy, and thus higher activation energy for diffusion [3].

Current semiconductor technology demands the use of low-resistivity metal layers for integrated circuit conduction lines and contact structures. Penetration of metal layers in Si is, however, deleterious to device properties. For this reason there is an increasing interest in the use of thin conducting layers between Si and metals as diffusion barriers. Many studies have been concerned with preventing interaction between aluminum and silicon. Metallurgical differences in the stability of a barrier with aluminum, which is highly reactive, and copper, which is more noble, may be expected. Al often induces failure by reacting with the barrier layer, forming aluminides. Copper is quite mobile at elevated temperatures, and may penetrate through a barrier layer without reacting with it [4, 5].

Copper has attracted much attention in deep submicron multilevel interconnection applications because of its low bulk resistivity, excellent electromigration resistance. But, Cu diffuses fast in silicon as well as oxide, and forms Cu-Si compounds at temperatures as low as 200°C, resulting in degradation of device. Also, it has poor adhesion to dielectric and drifts through oxide under field acceleration. Therefore, a diffusion barrier between Cu and its underlying layers is necessary for Cu to be useful in silicon integrated circuit applications [6].

To overcome these difficulties of the metal interconnects, a diffusion barrier is often deposited between interconnect and the substrate. The characteristics of an ideal barrier include effectively prevents Cu diffusing into

dielectrics and other adjacent materials, provide good adhesion to both Cu and dielectrics which is critical to resist delaminating during the subsequent processing and thermal stressing. Good adhesion can also help to improve copper electromigration resistance, inertness towards the metal and substrate, low electrical resistivity, thermal stability, and low interfacial stress to prevent delamination [2, 7].

In general practice, it is very difficult for any barrier layer to meet all the qualities of an ideal barrier. Hence, some of the criteria can be relaxed as long as the specific requirements of the final product can be reached safely. Various materials have been studied as a diffusion barrier between Cu and Si substrate, as well as Cu and dielectric layer. Refractory metals have been recognized as an attractive class of materials because of their high thermal stability and good electrical conductivity. Sputtering of nitride-based diffusion barriers, such as W-N, W-Ti, Ti-N, TaN, Ti-O-N, Ti-Si_x-N_y, Ru and more, to be used in Cu/barrier/Si and Cu/barrier/SiO_2, structures, has attracted extensive attention [8].

Ruthenium is selected as diffusion barrier for Cu metallization because Ru is an air-stable transition metal with a high melting point (2310°C) and is nearly twice as thermally and electrically conductive of 7.6 μΩcm as Ta. Additionally, Ru shows negligible solubility in Cu even at 900°C, and based on the binary phase diagram, there are no intermetallic compounds between Cu and Ru. These properties of Ru show that Ru may be a good candidate for Cu glue layer and also for a Cu diffusion barrier layer [9].

B. Electromigration

The most important concern with interconnects in integrated circuits is electromigration. It contributes to the premature failure of the interconnect. Electromigration is the mass transport in a diffusion controlled process under electrical driving force. This electrical driving force consists of electrical wind force and direct field force. The electrical wind force is associated with the effect of momentum exchange between the moving electron and the ionic atoms when electric current is applied to a conductor. With high current density, the momentum transfer effects significantly and a noticeable mass transport is observed. Being positively ionized, ions also tend to move in the direction of electric field, while they move in the direction of momentum impulse. Hence, a balance between the two forces determines the movement of ions [10].

Selection of metallization is one of the moat important parameter for the control of electromigration. Various metals have different electromigration resistance because of the difference in microstructure, chemical nature, texture orientation, alloying behavior and interaction with ambient. In general, it has been investigated that higher electromigration resistance is achieved with bigger grain size [11].

C. Miedema's Plot

According, to Miedema the ambiguity in discussing binary phase diagrams is the relative importance of enthalpy and entropy dominated processes. Miedema overcomes this problem to a certain extent by examining only the signs of heat of formation (ΔH_f). If the ordered phase exists in an alloy system and persists to low

temperature, then the ΔH_f is assumed to have negative sign. If no ordered phase exists and the solubility is not extensive (i.e., less than 10 at %), then ΔH_f is assumed to have positive sign [12]. Miedema reduces a vast, complex, phase-diagram compilation to a data formed by binary set of signs. Miedema's scheme works exceptionally well in ascertaining the signs for ΔH_f. It is more effective for transition-transition metal systems and non-transition-transition metal system than for non-transition to non-transition metal system. This scheme is restricted in that it predicts only signs for heat of formation with a high degree of accuracy. Miedema's work prevents its direct application to solubility problems. Miedema's scheme fails to describe systems in which structural or covalent energies play a significant role [13].

D. Adhesion

Adhesion is an important thin film technology because the thin films are fragile and must be supported by substantial substrates and the degree to which the film can share the strength of the substrate depends upon the adhesion between the metal layer and the substrate. Adhesion is important in determining the durability of thin film devices and also, plays an important role in governing the kinetics of the growth and structure of the films, with the result that performance of thin films is dictated by adhesion forces. Film structure will be aggregated when the cohesion energy exceeds the energy of adhesion. This dependence of film integrity upon adhesion forces is important for performance of such films and has a basic scientific import. The durability and longevity of thin

films are dependent upon their adhesion to the substrate since this determines the ease of removal [14].

Adhesion is the mechanical strength joining two different objects or materials. Adhesion is a fundamental requirement of most deposited film/substrate systems. In PVD technology, adhesion occurs on the atomic level between atoms and on the macroscopic level between the substrate surface and the deposited film. The apparent adhesion is usually measured by applying an external force to the thin film structure to a level that causes failure between the film and substrate, or in material near the interface. Scratch test is used to give a measure of the adhesion of a range of coatings/metal layer [14]. In this test a diamond stylus is drawn across the coated surface under an increasing load until some well-defined failure occurs at a load which is called the critical load, L_c. If this test is to be used to assess adhesion then this failure must occur as a result of coating detachment which is not always easy to identify. The types of failure which are often observed in the scratch test depend critically on the properties of both substrate and coating/metal layer. If the metal layer is very soft compared to the substrate, plastic deformation will occur within it and the scratch test critical load may be defined as the load at which the coating is scraped off exposing the substrate [15, 16]. It is not always easy to determine when this has occurred and quantification of the failure mode is difficult. For a hard coating on a softer substrate spallation and buckling failure modes result from interfacial detachment. But a range of other cracks and deformed regions can be observed. For hard coatings on hard substrates the chipping observed in the scratch test is almost

identical to the lateral fracture observed in the scratch testing of bulk ceramics. This failure is occasionally observed to coincide with the coating-substrate interface but this is not always the case making the results of the test difficult to interpret. Thus if scratch testing is to be used for adhesion assessment only the spallation and buckling failure modes are really useful [16].

E. Overview

In this study Ru is selected as a diffusion barrier for the Cu/Metal barrier system using the Miedema plot. Here Cu/Ru system was selected because Ru shows negligible solid solubility with Cu even at 900 °C. This implies Cu/Ru system would be stable at conventional operation temperature as well as typical diffusion barrier evaluation temperature. Therefore here we restrict our temperature to 600 ^{o}C. Chapter 2 discusses the experimental setup that is employed during the investigation. Chapter 3 discusses the Ru as a potential diffusion barrier in Cu metallization. Backscattering analysis indicates that both the copper and ruthenium thin films are thermally stable at high temperature (600 ^{o}C) for 2 hr annealed without any interdiffusion and chemical reaction between Cu and Ru thin films. The XRD analysis indicates no new phase formation in any of the annealed Cu/Ru/SiO_2 samples. The XRD data also confirmed excellent thermal stability of Cu on Ru layer. The electrical resistivity measurements indicate that the electrical resistivity value of the copper thin films annealed is essentially constant and the copper thin films are thermally stable on Ru and no reaction occurs between copper films and Ru layers. Chapter 4 discusses Cu/Ru/SiO_2 multilayered thin film samples possess good mechanical strength and

adhesion between the Cu and Ru layers compared to the Cu/SiO_2 thin film samples. The strength evaluation is carried out under static loading conditions such as nanoindetation testing. Then, we evaluate and compare the dynamic deformation behavior of $Cu/Ru/SiO_2$ and Cu/SiO_2 samples under scratch loading condition as a measure of tribological properties. The deformation behavior under static and dynamic loading conditions is understood using scanning electron microscope and focused ion-beam imaging microscope for topographical and cross-sectional imaging respectively.

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Chapter 2

EXPERIMENT

A. Sample Preparation

Thin films of copper were deposited on ruthenium using Magnetron sputtering technique. The sputtering technique used was an ion sputtering technique in an argon discharge tube. The phenomenon of sputtering takes place due to material erosion from a target (copper) on an atomic scale and the formation of a thin layer of the extracted material (copper) on a suitable substrate (ruthenium on SiO_2). The process is initiated in a glow discharge procedure in a vacuum chamber under the pressure-controlled gas flow. The Target erosion occurs due to the bombardment of energetic particles by reactive or non-reactive ions procedure in the discharge. Bilayer system consists of 200 nm Cu on 20 nm Ru. Compositions and thickness were verified by Rutherford Backscattering Spectrometry.

The furnace utilized for the anneals consisted of a quartz boat attached to a glass rod. The boat assembly was enclosed in A 19 mm Pyrex tube which was attached to a gas inlet on one end and a vacuum/glass outlet on the other. The entire system was close looped allowing the sample to be loaded and then vacuum was used to remove oxygen and other contaminants. The boat was transferred in and out of the furnace region by a circular magnet enclosed around the Pyrex tube.

To ensure removal of contaminants a three step procedure was used prior to annealing the samples. The first step consisted of a two minute evacuation followed by a two minute purge. Then, step one is repeated. The final step consisted of a five minute evacuation followed by a five minute purge.

The samples were annealed from 400-600 ^{o}C for 0.5, 1, and 2 hours. A 99.99% electronic grade Ar/H_2 (5%) forming gas was used for the anneals to minimize oxygen contaminants within the furnace. Annealing temperatures were chosen based on preliminary results which revealed a reaction at the SiO2/metal interface occurred at ~ 927 ^{o}C. During the actual annealing, the flow rate was monitored by an oil bubbler. The flow rate was calculated to be 1 litre per minute and was chosen to minimize the oxygen partial pressure in the furnace chamber.

B. Sheet resistance

Sheet resistance of the sample is measured using a typical in line four-point probe configuration as shown in fig. 2.1. In this method there are totally four probes. The spacing between the probes is 2 nm. Current passes through the outer probes in order to avoid contact resistance and the two inner probes sense the voltage and voltage drop between the two inner probes is measured. Each probe has probe resistance R_p, a probe contact resistance R_{cp} and a spreading resistance R_{sp} associated with it. However, these parasitic resistances can be neglected for the two voltage probes because the voltage is measured with high impedance voltmeter, which draws very little current. Thus the voltage drops across these parasitic resistances are insignificantly small. The voltage reading from the voltmeter is approximately equal to the voltage drop across the material

sheet resistance. The sheet resistance is calculated from the measured values of the voltage and the current by dividing the voltage by the current and multiplying this by the correction factor which depends on the probe spacing, film thickness and the probe distance from the edge of the sample. The sheet resistance expressions can be expressed as follows:

$$R_s = (V/ I) \times CF$$

Where CF = Correction factor

V/ I = Reading from the monitor

V = Voltage reading from the voltmeter

I = Current that passes through two probes

The resistivity of the material is calculated by using the following expression:

$$\rho = R_s \times t$$

Where t = thickness of the material. This measurement was of particular interest to verify that the resistance of the alloy films after annealing was comparable to that of the as-deposited sample.

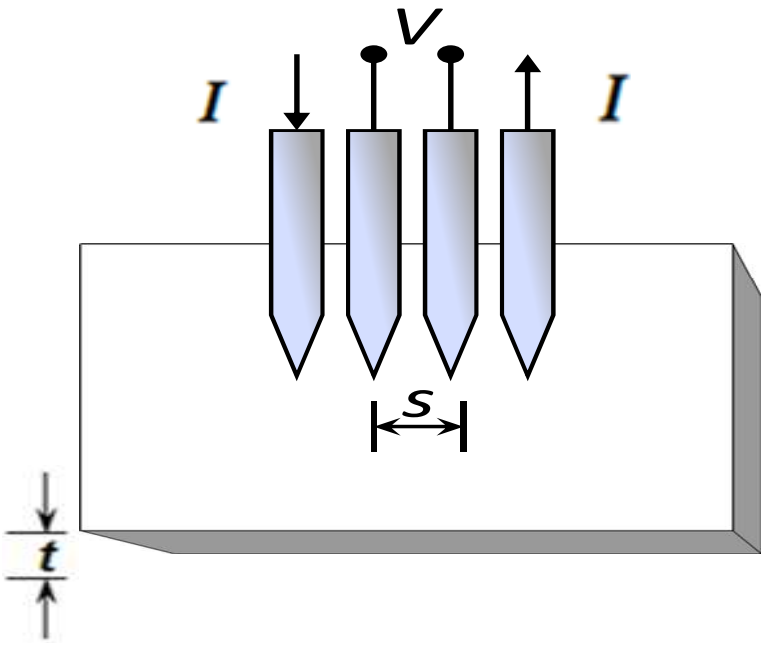

Figure 2.1: Layout of atypical four-point probe setup. Measurements taken at ASU had a probe spacing of 2 mm. Where S = spacing between the probes, and t = thickness of the sample.

C. X-ray Diffraction

X-ray diffraction analysis is a non destructive technique to obtain the crystallographic information and thus investigate the phrases formed in a solid sample. It reveals the lattice information from the near surface of the substance.

A crystal sets of parallel planes constituted by atoms. When monochromatic beam of X-rays of wavelength (λ) is directed towards the crystal at an angle (θ) to the atomic planes, diffraction occurs only when the distance traveled by the X-rays reflected from the successive planes differs by an integer number *n* of wavelengths. If *d* is the interplanar spacing, the path difference is twice the distance $d\sin\theta$. The Bragg's law which is the governing law for X-ray diffraction can be thus written as [1]:

$$n\lambda = 2d\sin\theta$$

Figure 2.2 shows the schematic of a typical X-ray diffractometer. In X-ray diffraction analysis, various analytical techniques can be applied to characterize a sample. A brief introduction of these techniques, which are being used, is provided below.

Bragg- Brentano Scan analysis is most commonly used in phase identification and stress analysis for crystalline materials, also known as (θ-2θ geometry scan). In this technique, the incident and the diffracted beams from the planes parallel to the sample's surface satisfies Braggs Law simultaneously. This provides the information about all the phases present in the sample within specific angle range selected. Figure 2.3 shows the schematic for the Braggs-Brentano

scan analysis. However, to confirm the extent of texturing completely, pole figure analysis is necessary.

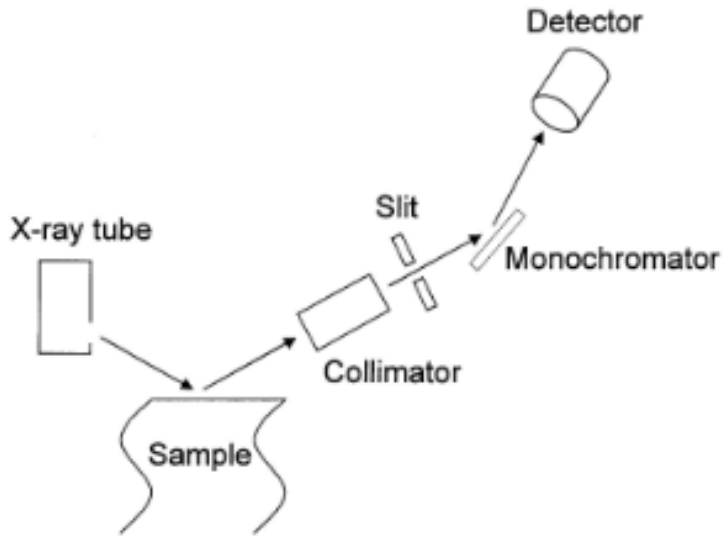

Figure 2.2: Schematic representation of X-ray diffractometer

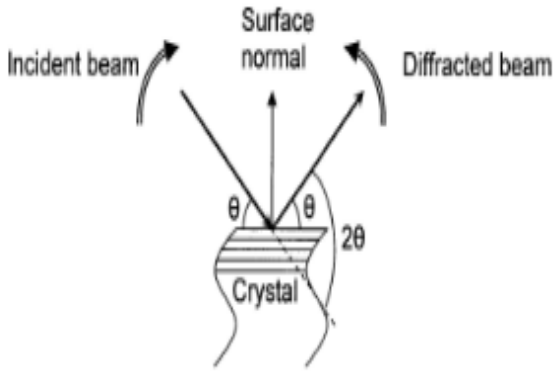

Figure 2.3: Schematic representation of Bragg-Brentano scan analysis.

Glancing incident X-ray diffraction is used to identify the phases in the polycrystalline thin film layers (minimum thickness ~10 nm), as well as measurement of thin film thickness using interferometry. It differs from the Bragg-Brentano scanning technique in the fact that, in the present case, the angle of the source from the sample surface is fixed at the lower value while the detector moves in the usual manner. In a θ-2θ geometry scan, the angle of the incidence is always equal to angle of exit. Hence, at higher angles to detect higher plane reflections, the penetration depth of x-rays may be greater than the thickness of the thin film, resulting in unwanted substrate peaks and noise. Glancing angle X-ray diffraction reduces this to a significant extent. It provides a larger interaction volume within the sample as compared to θ-2θ geometry scan. Therefore, to achieve less noise and precise position of peaks, this technique is used.

Pole figure analysis is one of the most robust tools to investigate the texturing or preferred orientation in the crystalline samples. Pole figure in the form of stereographic projections are used to represent the orientation distribution of lattice planes in crystallography and texture analysis. In this technique, detector and sample geometry are set so that the incident and diffracted beam make a specific angle with the sample surface. This angle is same as the angle necessary to satisfy the Bragg condition for a specific set of {*hkl*} planes in crystalline sample.

Analysis through one dimensional pole figure measures the intensity of X-rays diffracted from the sample as a function of tilt angle (ψ), with rotation about

an axis perpendicular to the sample surface. The results of one dimensional pole figure measurement are shown in the form of intensity versus tilt angle (ψ) plots. In two dimensional or three dimensional pole figure analysis, the tilting angle is first fixed, then the intensity is measured as a function of the rotation of sample (ψ) about an axis perpendicular to the surface of the sample. The sample is rotated from 0^o to 360^o. After completing one full rotation, the tilt angle changes and the process is repeated again. This process is repeated for the entire range of desired rotation and tilt angles.

D. Rutherford Backscattering Spectrometry

Rutherford backscattering spectrometry (RBS) is a non-destructive characterization technique. It is used to analyze the atomic composition of the sample like diffusion and interaction between the copper and ruthenium thin films and to estimate the sample thickness using very high energy (MeV) beam of low ion mass. It is also used for quantitative depth profiling, areal density measurements, and determination of crystal lattice quality. RBS utilizes Tandetron accelerator to generate a MeV ion beam. After entering the evacuated beam line, the ions are then collimated and focused. There are bending magnets which after mass selection geometrically disperse ions according to their mass. Finally the beam raster-scans over the specimen and back scattered ions are analyzed by a Si barrier detector. The electronic pulses are then amplified and sorted according to the voltage amplitude by a multichannel analyzer to yield the resulting RBS spectrum [2]. RBS was performed using a General Ionex 1.7 MV

tandem accelerator with He^{2++} ions at energy of 2.8 or 3.5 MeV as shown in fig. 2.4.

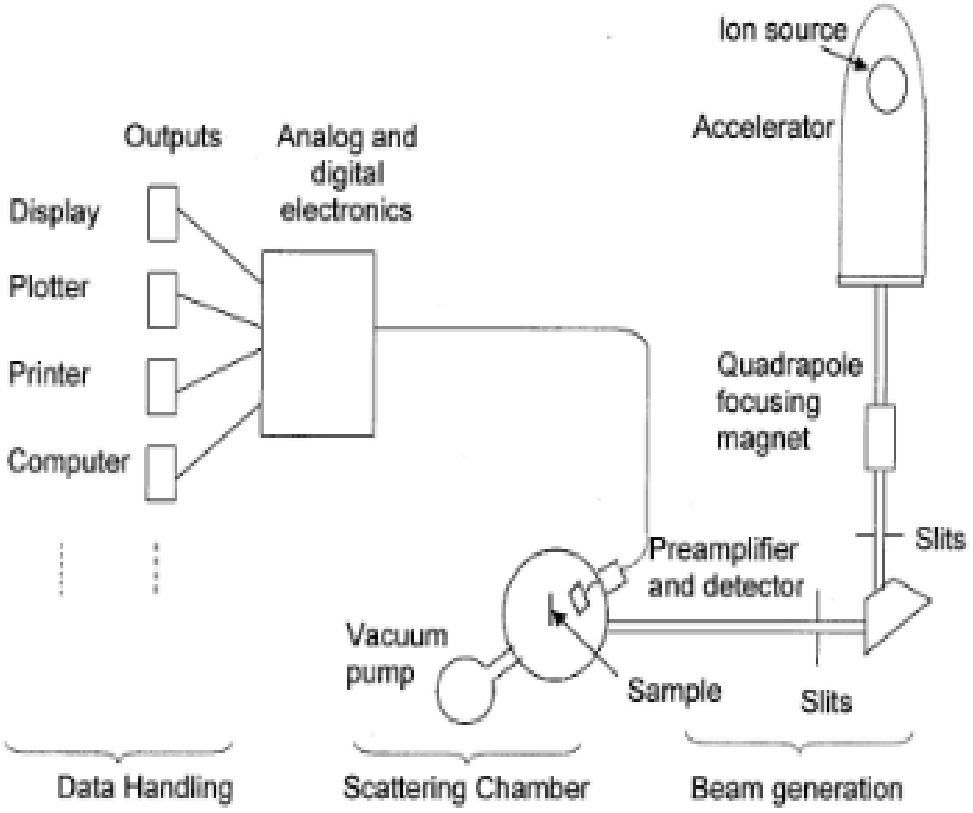

Figure 2.4: Schematic of a typical Rutherford backscattering system. A General Ionex 1.7 MV Tandetron accelerator was used for RBS at ASU.

F. SEM and FIB analysis

A dual-beam system is a combination of focused ion beam (FIB) with a scanning electron microscope (SEM). Both beams can operate independently or simultaneously and focus on the same point of the specimen. Imaging with the ion beam damages the specimen, the electron beam allows non-destructive observation. This combination of an ion beam with an electron beam allows extensive analysis of the surfaces or the interiors of materials. This combination is useful for cross-section sample preparation using the electron beam to view the cross-section faces as the ion beam mills normal to the sample surface. This monitoring allows the milling to be stopped precisely when the features of interest is exposed [3].

On a single beam FIB, a series of tilting and beam current changes would normally be required to monitor the cross-section face position in this way is time consuming process. A typical dual column configuration is a vertical electron column with a tilted ion column. The configuration has an ion beam at 52^{o} tilt to the vertical column. The sample is tilted to 52^{o} for milling normal to the sample surface. An alternate geometry is FIB column vertical and SEM at an angle. The advantage of this is sample tilt is not required to be tilted for milling normal to the sample, potentially simplifying the system operation. Using a tilted SEM column is not a typical configuration for most of the electron, so this would need to be considered [4].

To enable ion milling and electron imaging of the same region, dual beam has a coincident point where both the beams intersect with the sample. This is

normal operating position for the system. Options such as gas injector and EDS are also aligned for optimum at the same operation. SEM can be used to monitor the cross-section face as the FIB mills [4].

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Chapter 3

USE OF MIEDEMA PLOT TO SELECT DIFFUSION BARRIER METAL FOR COPPER METALLIZATION

A. Introduction

Rapid increase in the functionality and complexity of components in integrated circuits (ICs) has resulted in reduction in the dimensions of both the devices and wiring [1]. Aluminum (Al), copper and their alloys are widely used as interconnect material [2]. Al is replaced by copper as an interconnect material in advanced integrated circuit technology [3]. The need to reduce circuit delays prompted the replacement of Al alloy with lower resistivity copper (Cu). To achieve high speed and low power consumption, interconnects must be reliable because the decrease in device sizes in ICs has led to interconnect being subjected to high current densities and thermal stresses [4]. Electromigration, which is a current induced mass transport phenomena is one of the major cause for premature interconnect failure in ICs [5]. Because electromigration failure is due to atomic diffusion caused by high electrical current density, the replacement of Al alloy with Cu was expected to enhance to electromigration resistance by the higher melting point of Cu compared to Al alloy, and thus higher activation energy for diffusion. The interface between Cu and the barrier is the main path for electromigration. Copper metallization has been chosen for large scale integration because of its lower resistivity (1.6 μΩ-cm), better electromigration resistance, better stress voiding resistance and higher melting point than Al [6,7]. But copper

has some drawbacks such as fast diffusion into Si and SiO_2 [8, 9], even at temperatures below 200 °C and thus forming deep traps in silicon which reduces the electrical devices performance [8]. Copper also shows poor adhesion to SiO_2. Therefore, an adequate Cu diffusion barrier metal layer is required between Si and Cu to prevent the degradation of devices caused by the diffusion of Cu [10]. This problem can be overcome by insersion of a barrier layer between Cu and the Silicon substrate in Cu metallization. The basic requirements for a diffusion barrier layer are its stability, chemical inertness towards the metal contact or underlying substrate, low electrical resistivity for reducing overall resistance of the conductor and good adhesion to both the layers in contact [11]. Some of the diffusion barriers for copper metallization are transition metal barriers (Ta, W), transitional metal nitrides (Ti-N, Ta-N and W-N) and transitional metal boride (TiB_2) [12]. Some of the other metals and their alloys that are being researched for interconnect application include Ag, Au, Ti, and W [2].

In this study, our approach is to use Miedema's plot to select the Cu/metal barrier for Cu metallization. The Cu/metal barrier system should have positive heat of formation (ΔH_f) so that there is no intermixing between the two layers. One of the ambiguities in discussing Cu/metal binary phase diagram is the relative importance of enthalpy and entropy dominated processes. Miedema overcomes this problem to a certain extent by considering the signs of heat of formation (ΔH_f). If the ordered phase exists in an alloy system and persists to low temperature, then ΔH_f is assumed to be a negative sign. If no ordered phase exists and the solubility is not extensive (*i.e.*, less than 10 at. %), then ΔH_f is assumed to

have positive sign [13]. One of the potential candidate which satisfies the above condition is ruthenium (Ru) as shown in fig 3.1.

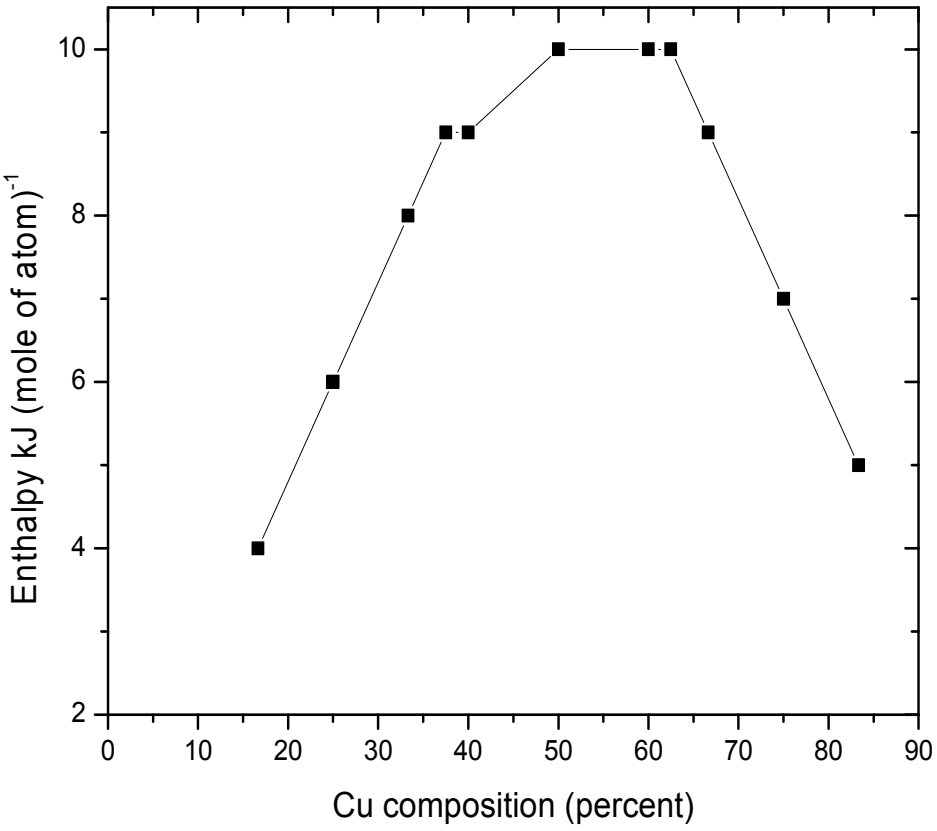


Figure 3.1: Heat of mixing of Cu and Ru as function of Cu composition.

Recent research show that Ru as an intermediate layer serves two purposes: (i) as an exchange barrier between the soft under layer (SUL) and a hard magnetic layer and, (ii) as a crystalline template for development of texture in the recording layer. The reduction in *c*-axis dispersion of Ru layer has resulted in improving the structural and magnetic properties of the recording layer [19]. All of the above benefits make Ru a very attractive barrier material. Ru has also

received a lot of attention in research as diffusion barrier for Cu in IC fabrication [14]. Ru is an air-stable transition metal with high melting point (2310 °C) and has an electrically resistivity of 7.6 μΩ-cm, which is one-half of that of Ta. Ru as a barrier layer adheres well to Cu [15]. More importantly Ru, like Ta, shows negligible solid solubility with Cu even at 900 °C [16,17]. Based on the literature data of the Cu-Ru binary phase diagram which indicates negligibly low solubility of Ru in copper (not exceeding 0.06 at. % Ru) and the immiscibility in the copper based alloys with ruthenium content of up to 18 at %. This is due to the fact that metals of the IB group, when alloyed with transition metals, form phase diagrams with immiscibility of components in a liquid state [18].

Based on Miedema's plot, we have selected Ru as a barrier layer between Cu and SiO_2 substrate. We then evaluate Cu/Ru barrier layer properties in Cu metallization using four-point probe, Rutherford backscattering spectrometry, and X-ray diffraction techniques.

B. Experimental Details

Thin films of Cu/Ru were deposited on the thermally oxidized silicon substrate using direct-current (dc) and radio-frequency (rf) sputtering using a magnetron gun. The base pressure prior to deposition was approximately $1x10^{-7}$ Torr. Substrate to target distance was 6 cm and was maintained at the same value for all experiments. Ruthenium layer of 20 nm thickness was deposited on Si wafers by radio-frequency (rf) magnetron sputtering. Then without a vacuum break, Cu thin films of 200 nm thickness was sputtered using direct current (dc) magnetron sputtering at a pressure of 1m Torr and 40 W power. After deposition,

the samples were annealed in a modified Lindberg vacuum anneal furnace (base pressure of 10^{-8} Torr) for each combination of time and temperatures, 0.5, 1, and 2 hr, and 400, 500, and 600 ^{o}C in order to investigate the changes in Cu/Ru stack behavior.

Backscattering analysis was used for thickness determination and atomic composition of the as-deposited films. It was also used for studying changes brought about by annealing the Cu/Ru/SiO_2/Si thin film layers. Rutherford backscattering spectrometry (RBS) analysis was performed in a vacuum of 10^{-6} Torr using a 4.3 MeV He^{++} ion beam and total accumulated charge of 20 μC in a General Ionex Tandetron accelerator. Sample and detector were in the Cornell geometry such that the backscatter detector is directly below the incident beam. The samples were tilted to 7^{o} off normal incidence to increase the depth resolution. Energy spectra were obtained using a surface-barrier detector and were analyzed using the RUMP computer simulation program [20].

To identify the phases formed due to annealing and crystallographic orientation of as-deposited and annealed thin films, X-ray diffraction analysis (XRD) was performed using a Philips X'pert MPD system with glancing angle (1^{o}) scan geometry to obtain more information from the thin films. Cu $K\alpha$ radiation was used as the incident X-ray beam and operation voltage and filament were 45 kV and 40 mA, respectively. The glancing angle configuration is used to limit X-ray penetration to the thin film mostly, thus reducing the occurrence of substrate peaks and background noise. The texture evolution of the Cu/Ru films

was investigated by pole figure analyses. Texture along the <111> and <200> poles was measured with the sample tilt ψ that varied from 0° to 85°.

Electrical resistivity of the $Cu/Ru/SiO_2$ was measured by four-point probe technique in order to analyze the thermal stability of thin film stack. For the sheet resistance measurement, a typical in-line configuration of the four probes was used. Current flows through two probes and the voltage is measured through other two probes [21].

C. Results

The copper diffusion into the barrier layers at different temperatures between the $Cu/Ru/SiO_2$ thin film layers is evaluated RBS, XRD, and electrical resistivity measurements. Backscattering plots convey information about the roughness and composition changes at interfaces as a function of temperature. The RBS data for as-deposited overlayed on a 600 ^oC for 2 hr annealed samples is shown in fig. 3.2. In order to elucidate the copper diffusion phenomena into the Ru thin film, we focus on the ruthenium and copper backscattered signals for as-deposited sample and 600 ^oC annealed sample for 2 hr. This is done by overlaying the spectrum of annealed sample over that of as-deposited sample. The overlayed copper and Ru backscattered signals of as-deposited and annealed samples did not show and changes in the width (thickness), the height of the peak (composition) and their positions at the *x*-axis (energy function) as shown in fig. 3.2. This is also consistent with all annealed samples overlayed the as-deposited sample. This indicates that both the Cu and Ru thin films are thermally stable at high

temperature (600 ^{o}C) for 2 hr annealed without any interdiffusion and chemical reaction between Cu and Ru thin films.

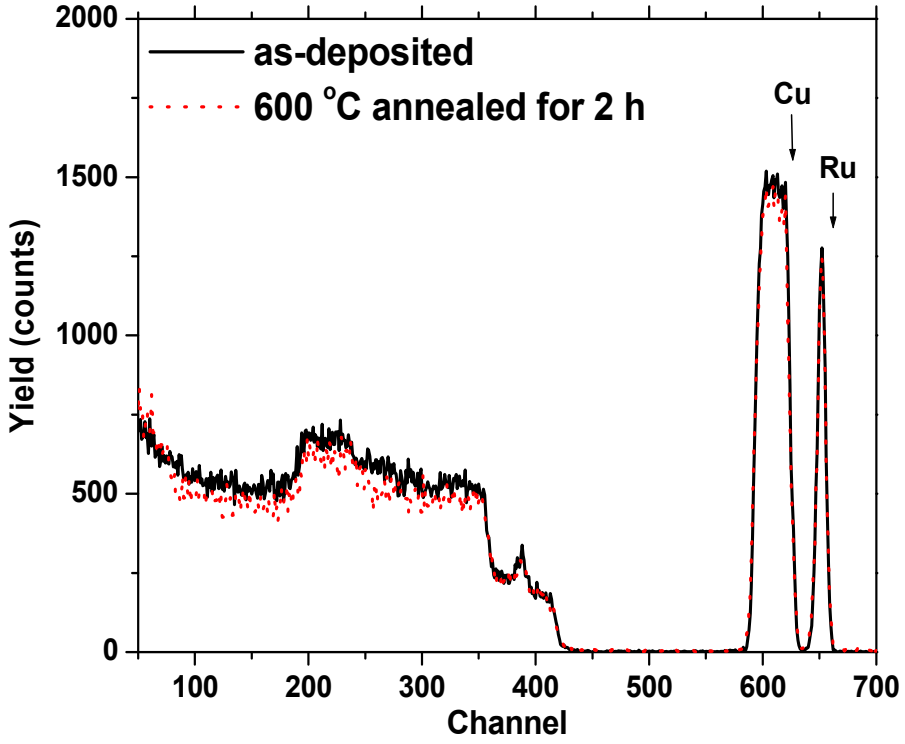


Figure 3.2: The RBS spectra of as-deposited sample overlayed on a 600 ^{o}C at 2 hr with an energy of 2 MeV and 7^{o} tilt.

The XRD data for Cu/Ru/SiO_2 samples vacuum annealed at 400, 500, and 600 ^{o}C for 2 hr and as-deposited sample is shown in fig. 3.3. A glancing angle scan (1^{o}) scan configuration is used to collect the diffraction peaks of copper films and to inspect any phase changes in copper after annealing compared to copper thin film layer in as-deposited sample as shown in fig. 3.3. The plot shows that all expected peaks of Cu and Ru are present. Within the detection limit of XRD,

there is no detected formation of any new peaks in the plot which indicates the absence of any new phase formed during annealing in any of the $Cu/Ru/SiO_2$ samples. Cu diffraction peaks are seen in all the samples and have same 2θ value in all the XRD spectra generated for samples annealed at different temperature. Only the peak heights of the annealed $Cu/Ru/SiO_2$ sample increases compared to the as-deposited $Cu/Ru/SiO_2$ sample. This is due to the crystallization of Cu thin film at higher temperature [22]. XRD data also confirmed excellent thermal stability of Cu on Ru layer. There is an exception to the general trend that increasing annealing temperature increases the <111> intensity, *i.e.,* the 500 ^oC annealed sample has slightly lower <111> intensity than the 400 ^oC. This may be due to the multiple twinning of the <111> grain in the 500 ^oC annealed sample. Pole figure XRD was used to investigate the texture of Cu films deposited on Ru layer. The <111> and <200> pole figure analysis of Cu/Ru thin film layers did not show any texture evolution nor secondary phase for both as-deposited as well as 600 ^oC for 2 hr annealed samples. The Cu films deposited on Ru showed no evidence of pronounced <111> or <200> texture. The texture dependences can be explained if the texture of the barrier is taken into account [22]. This suggests that Cu film texture has an underlayer dependence on the crystal structure and process conditions of the under metal Ru. Ruthenium has hcp structure and its interatomic spacing is 0.271 nm on the basal phase. Whereas Cu has fcc structure and its interatomic spacing is 0.361 nm on the {111} plane. It is evident that relatively large lattice mismatch and thus a high interfacial energy would result if a <111> and <200> oriented Cu film were deposited on Ru. For this reason, the Cu film

tends to grow on Ru film surface with random grain orientation. The XRD data in fig. 3.3 shows increased crystallinity of samples when annealed at high temperature compared with as-deposited thin film since the increase in of intensity of diffracted X-ray means enhancement of crystallinity of material.

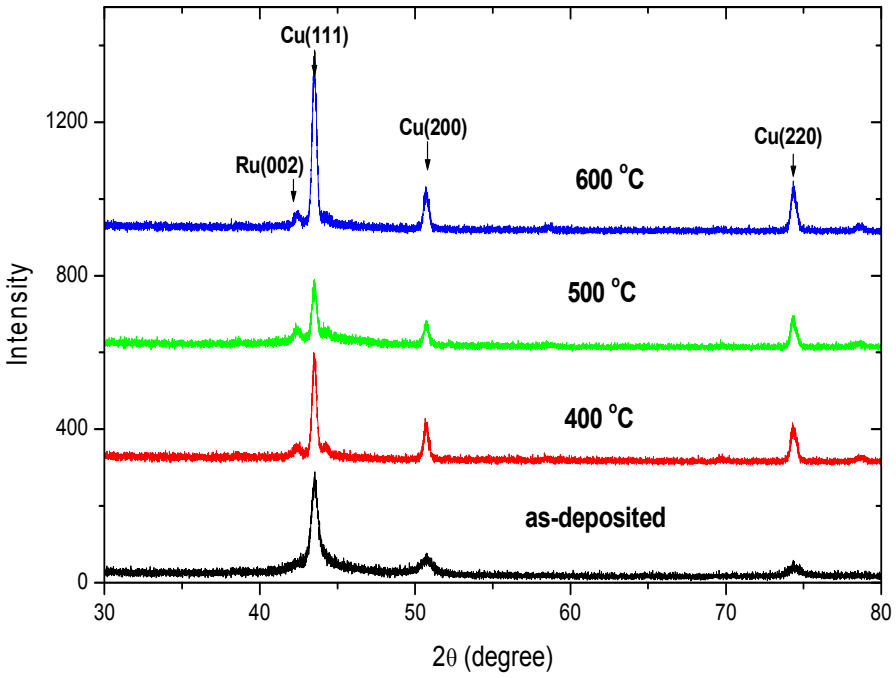


Figure 3.3: The XRD plot of as-deposited, 400, 500, 600 ^{o}C annealed sample.

The electrical sheet resistance of the Cu/Ru layers is measured by four-point probe technique prior to and after vacuum annealed at different temperatures. The resistivity of Ru thin film layer is very high (~7.1μΩ-cm), it is assumed that the resistivity value of Ru thin film layer does not contribute to the electrical resistivity value of Cu/Ru thin film layer. As shown in the fig. 3.4, the electrical resistivity value of as-deposited copper thin film is 4.7 μΩ-cm-5.2 μΩ−cm and that of the vacuum annealed copper thin film varies from ~2.5 μΩ-cm-3.2 μΩ-cm. This decrease in resistivity value for annealed copper thin film with respect to the resistivity of as-deposited sample is due to the increase in crystallinity of copper thin films. The enhancement of crystallinity results in increase of the mean free path of the carrier by reduction of electron scattering in ordered structure [23]. The electrical resistivity value of copper thin films annealed at different temperature and at different interval of time is as shown in fig. 3.4, and indicates that the electrical resistivity is essentially constant and the copper thin film is thermally stable at 600 ^{o}C for 2 hr vacuum annealed on ruthenium thin film layer and no reaction occurs between Cu/Ru thin film layers.

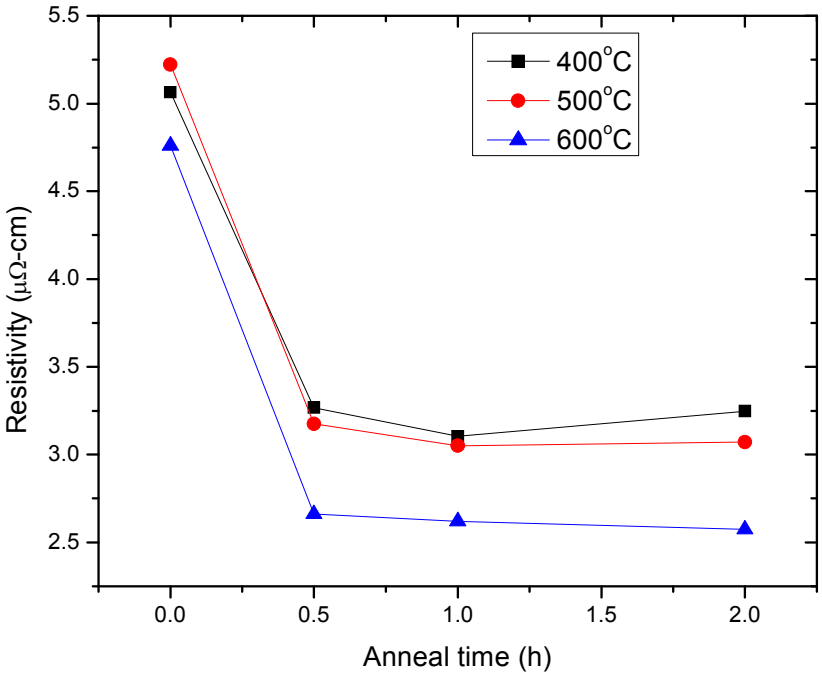


Figure 3.4: The resistivity measurements for as-deposited, 400, 500, 600 ^{o}C

Table 3.1: Resistivity measurement of all the samples by four-point probe method.

Samples annealed		Sheet resistance(Ω/sq)	Thickness Cu+Ru(nm)	Resistivity μΩ-cm/sq
Sample 400°C	0.5hr	0.1485	220	3.267
	1hr	0.1411		3.1042
	2hr	0.1476		3.247
	as-dep	0.2302		5.0644
Sample 500°C	0.5hr	0.1443	220	3.1746
	1hr	0.1387		3.051
	2hr	0.1396		3.071
	as-dep	0.2374		5.222
Sample 600°C	0.5hr	0.1210	220	2.662
	1hr	0.1191		2.620
	2hr	0.117		2.574
	as-dep	0.2165		4.76

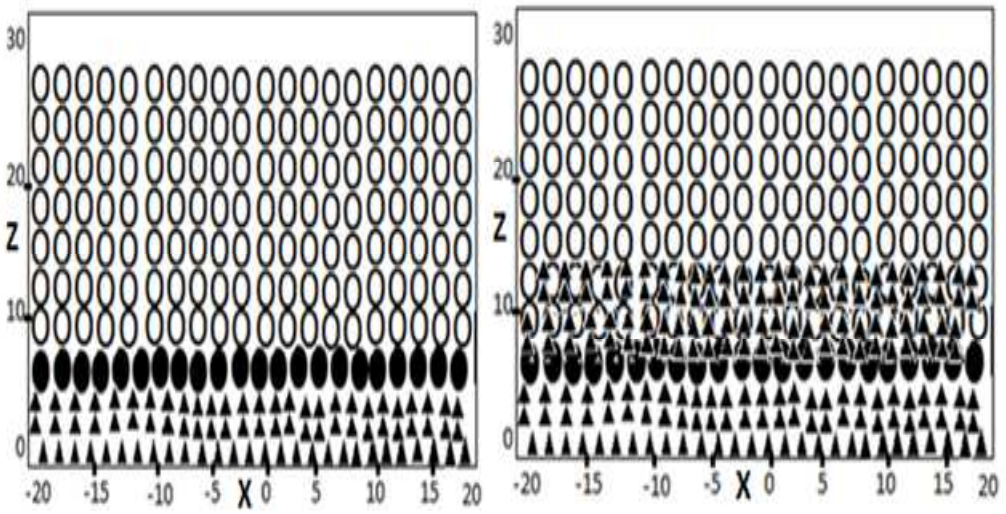
D. Discussion

Previous studies have shown that Cu starts diffusing into Si substrate at temperatures 200 °C and higher in absence of any barrier layer [24,25]. Hence the use of barrier layer to prevent the degradation of Cu into the Si substrate. Chan *et al.* showed that the interface between Cu/Ru(20 nm)/Si can be stable after annealing at 450 ^{o}C and also Cu/Ru has excellent adhesion stability [16]. Arunagiri *et al.* showed 5 nm Ru film can function as directly plateable Cu diffusion barrier up to at least 300 ^{o}C vacuum anneal for ten minutes [26]. At longer times or higher temperatures, copper starts to agglomerate and hence the film becomes discontinuous with the formation of voids. Until this temperature range the reaction between the interconnect layer and Si is prevented by the barrier layer.

In case of Cu-Ru system which is immiscible is characterized with positive heat of formation (ΔH_f) of 0.11 eV/atom [32]. This can also be confirmed from Miedema's plot as shown in Fig. 3.1. The interfacial bonding shows strong adhesion between Cu/Ru layers at elevated temperatures [28]. Kwon *et al.* has showed that the interfacial amorphization at the nanometer scale occurs in a thin interfacial layer of the immiscible binary systems [29], and the interfacial stability of multilayers actually depends on the value of the interface energy [30]. The interfacial free energy of the multilayer samples is increased with nanometer thickness of the Cu(200 nm)/Ru(20 nm)/SiO_2 samples. The interfacial energy is the major driving force for interfacial reaction between the Cu/Ru layers and results in spontaneous solid-state amorphization as shown in fig 3.5. When the

interfacial energy is completely consumed, the reaction terminates. Kinetic studies reveal that the growth of amorphous layer shows an asymmetric growth behavior as the disorder layer extends faster toward the Cu lattice than towards the Ru direction [27]. This is because the cohesive energy of Ru is larger than the Cu. Also, Ru lattice is more stable than Cu lattice which makes Ru lattice difficult to turn into disordered state. The critical solubility of Ru in Cu (10 at. %) which is smaller than that of Cu in Ru (20 at. %).

The main drawback of Cu metallization is that it copper easily reactive with substrate and high diffusivity through many diffusion barriers. The study of Ru diffusion barrier property for Cu metallization showed Cu did not show any signs of diffusion through the Ru barrier to form copper silicide ($CuSi_3$) at 600 ^oC. Based on the RBS analysis shown in Fig. 3.2, it is confirmed that copper atoms are not diffused through Ru barrier because no change in shape of the Cu peaks occurs at temperature upto 600 ^oC for 2 hr. Diffraction spectra did not show any evidence of new phase formation at elevated temperature. The electrical resistivity of Cu thin film initially decreases and then does not change when annealed. The decrease in the sheet resistance can arise due to grain growth, defect and impurity annealing [31].



(a) (b)

Figure 3.5: (a) Cu-Ru multilayers configuration of the initial state with disordered interlayer between Cu and Ru, and (b) The state after solid-state amorphization. Open circle symbols represent Cu and filled triangles represent Ru.

E. Conclusion

We have used Miedema's plot for the selection of Cu/Ru barrier system in Cu metallization. Miedema's plot illustrates a positive heat of formation which is evident of no intermixing between the Cu/Ru thin film layers. In the current study the requirements for Ru diffusion barriers layer for copper metallization was investigated. Thermal anneals up to 600 ^{o}C showed no signs of degradation/agglomeration and had good thermal stability. No evidence of Si was found on the top surface of the copper film and hence no interaction between copper and Si was observed, within the detection limit of RBS. Based on these results Ru diffusion barriers have the potential to increase the longevity of the films and can be used for high temperature electronics and integrated circuits.

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Chapter 4

ADHESION IN Cu/Ru/SiO_2/Si MULTILAYER NANO-SCALE STRUCTURE FOR COPPER METALLIZATION

A. Introduction

Recent advance in nanotechnology had lead to the fabrication of thin nano-scale films with distinct material properties such as optical, electrical, or magnetic. The multilayers are particularly simple systems wherein nano-scale control of the structure in one direction is easily attainable [1]. Mechanical properties of thin films have been a major concern over the reliability of metallization used for integrated circuits interconnections. The mechanical strength used for these interconnections is essential to understand the failure mechanism and to obtain appropriate solutions [2]. Multilayer coatings have shown to possess good mechanical and tribological properties [3,4] when compared with monolithically layer grown coatings/layers [5]. To study failure mechanisms and to characterize mechanical properties of coated systems, nanomechanical techniques such as nanoindentation [7-9] and nanoscratching [6] have widely been accepted as effective experimental methods.

Current semiconductor technology uses low resistivity metal lines for multilayer interconnect devices [10]. Copper (Cu) has considerably lower bulk resistivity and higher electromigration resistance than that of aluminum (Al) [11]. Both these traits are favorable and complement each other to allow higher current densities through Cu lines. Thin layers of copper films of nano-scale thickness on

SiO_2 substrate is an important structure in electronic devices [12]. If Cu does not bond well to the dielectric, it would lead to adhesion and agglomeration problems, when a high current density is passing through the Cu wire [13]. Failure due to delamination at the Cu/SiO_2 interface is a major drawback strongly related to device reliability [14,15]. Hence it is required to use a thin metal layer to serve as an adhesion promoter as well as diffusion barrier between Cu and the dielectric layer. Also to maintain the microstructure of nano-multilayers at high temperature, interdiffusion as well as interface phase transformation should be prevented. It is preferable that two coupled layers are immiscible, form coherent interfaces, and have different lattice structures [16,17]. By adding ruthenium (Ru) as a glue layer between the copper film and underlying SiO_2, it not only improves the adhesion [13]; but, it also satisfies the above requirement of an efficient barrier layer.

Adhesion is very important in thin film technology because the thin films are fragile and need to be supported by a substantial substrate and mechanical strength of the films depends on the adhesion between the film and the substrate [1]. A strong adhesion between Cu and Ru barrier films is critical for the fabricated Cu interconnects microstructures to withstand the demanding chemical mechanical planarization process currently used in integrated circuit fabrication [18]. The intrinsic adhesion energy for Cu/SiO_2 interface is 0.2-0.3 Jm^{-2} and for Cu/Ru interface is 4.6 Jm^{-2} [12]. Hence Cu/SiO_2 sample has weaker adhesion compared to $Cu/Ru/SiO_2$ thin film samples.

A wide range of methods is used to assess to adhesion of the coating. These methods include the peel method (*i.e.* `Scotch tape test'), the direct pull-off method, measurement of the abrasion resistance, and the scratch test [19]. The scratch test is widely used to quantitatively evaluate the adhesion of coatings to substrates. In this method a stylus having a well-defined tip is moved into the substrate film layer (laminates), while at the same time the tip is moved tangential to the surface. The normal force at which `failure' occurs is called the critical load. The critical load is used to qualitatively discriminate between differences in adhesion. Apart from the adhesion between substrate and coating, the critical load also depends on a large number of parameters including the tip radius, loading rate, mechanical properties of the substrate and coating, the thickness of the coating, and the friction between indenter and coating [20-23]. The understanding of deformation behavior in the multilayered material is restricted to the static loading conditions such as nanoindendation testing. This method provides a good understanding of mechanical response and deformation mechanism in the materials. Nanoindendation is one of the methods used to measure the delamination strength of the thin film structure because of the simplicity of sample preparation and applicability to small scale materials [24].

In this study, we evaluate the scratch resistance of Cu/SiO_2 and $Cu/Ru/SiO_2$ thin film samples. Post-scratch fracture analysis is done using scanning electron microscopy and focused ion beam microscopy to understand the deformation mechanism in the materials under dynamic scratch contact.

B. Experimental Details

Magnetron sputtering was used in the preparation of the samples. The base pressure prior to deposition was approximately $1x10^{-7}$ Torr. Substrate to target distance was 6 cm and was maintained at the same value for all experiments. Thin film layer of films were deposited by sputtering. Ruthenium layer of 20 nm thickness was deposited on Si wafers by radio-frequency (rf) magnetron sputtering at a pressure of 3 mTorr and 150 W power. Then without a vacuum break, Cu thin films of 200 nm thickness were sputtered using direct-current (dc) magnetron sputtering at a pressure of 3 mTorr and 50 W power. Similarly Cu thin films of 200 nm thickness were sputter deposited onto the SiO_2/Si substrate. The four samples that were used for the study were Cu/Ru/SiO_2 as-deposited and 600 ^oC annealed for 2 hr, and Cu/SiO_2 as-deposited and 600 ^oC annealed for 0.5 hr.

Scratch testing was performed using a Berkovich tip in a commercially available MTS nonoindenter. Multiple scratches were performed in each of the samples under load controlled conditions. A constant loading rate of 2.5 mN/s and a sliding velocity of 10 μm/s were used for all samples. The scratches were performed in two orientations of the Berkovich indenter tip-edge forward and face forward in the direction of scratching. A typical scratch procedure is shown in fig. 4.1, and consists of 4 segments. In the first segment, the indenter profiles the surface at a very small load of 100 μN to account for the slope and curvature of the sample surface. This is followed by the second load-ramped scratch segment performed near the profiling trace to avoid debris from the profiling trace. After the scratching segment the indenter traces back the scratch length with a small

load (100 μN) to estimate the residual deformation in the scratch. This measures the gross-plastic deformation at any point in the scratch. Finally in the fourth segment, a cross profile is carried out perpendicular to the scratch direction using a load of 100 μm to estimate the width and profile of the scratch track. The cross-profile was carried out at a distance where the film had not failed (below the critical load). This is chosen to be 10 mN for all samples. Post scratch testing, the scratches were analyzed under the scanning electron microscope (SEM) to analyze scratch profile and to identify the critical load for film failure. The deformation under the scratch was analyzed by performing cross-section analysis using a dual beam focused ion-beam (FIB) microscope.

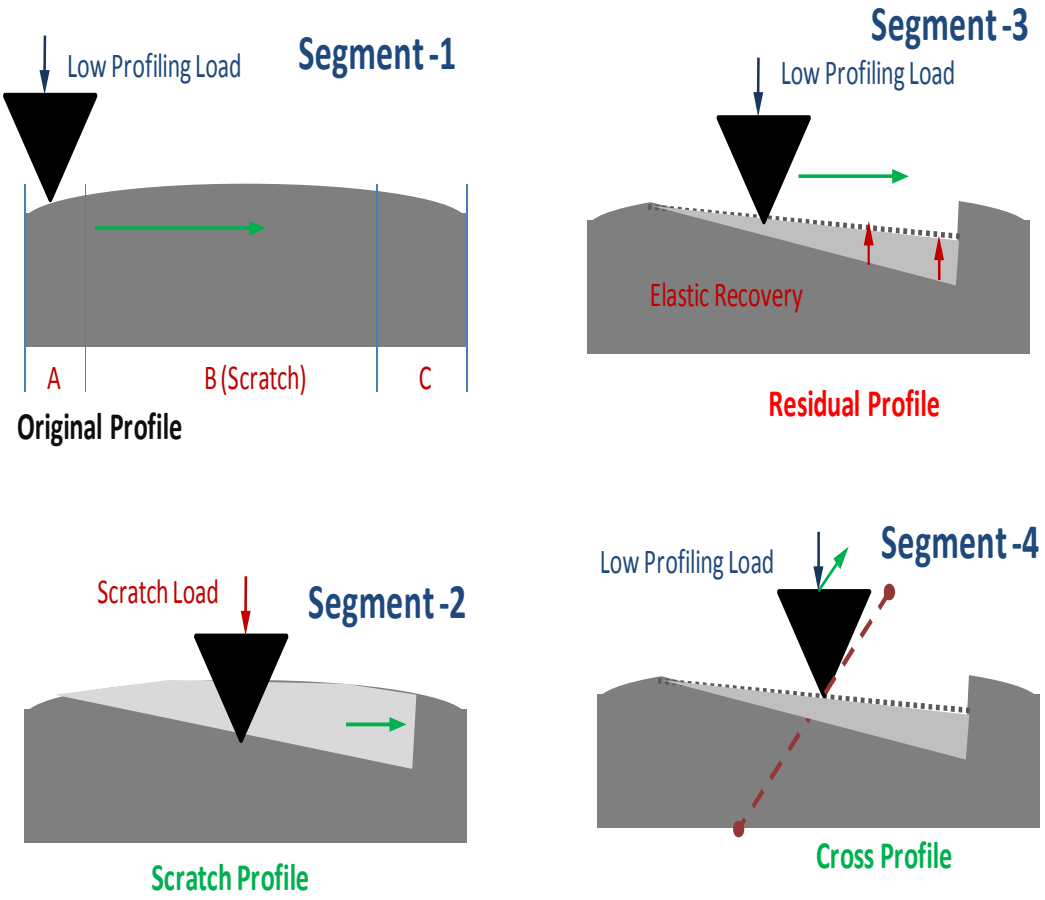
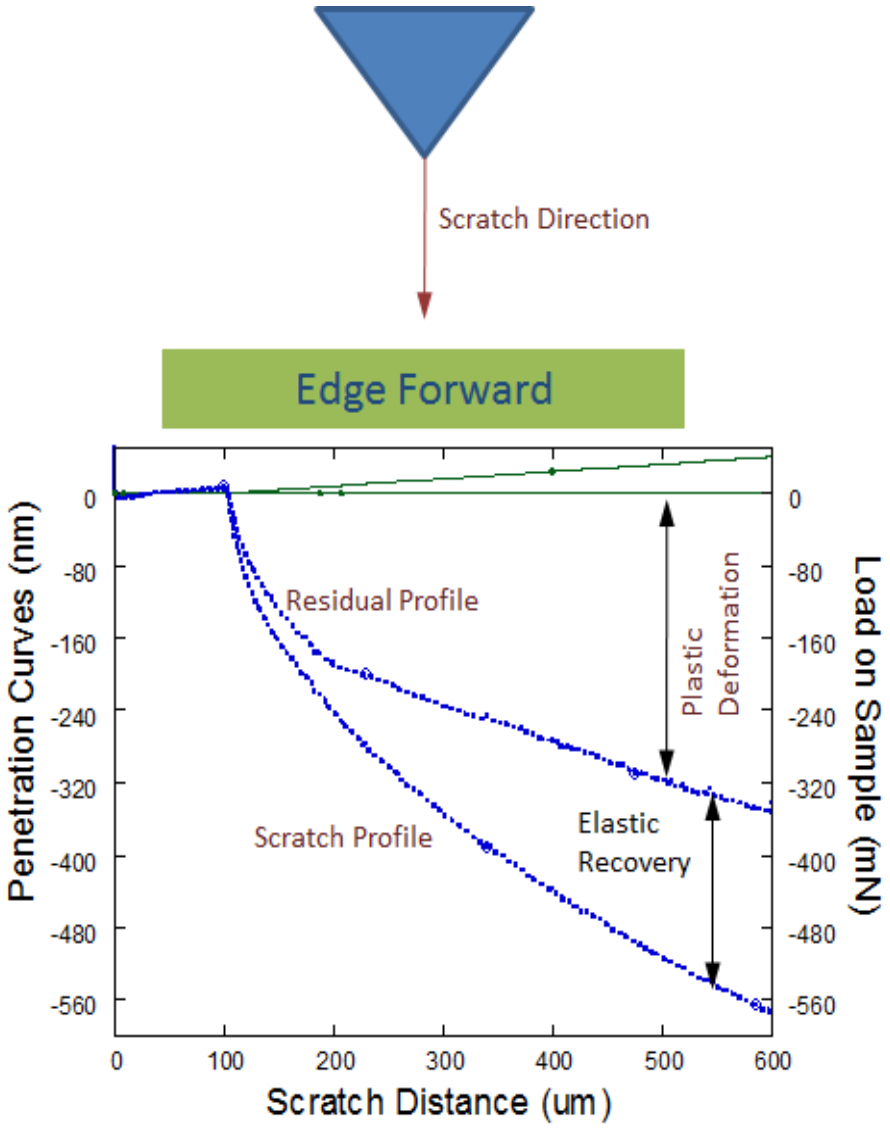


Figure 4.1: Schematic representation of scratch test.

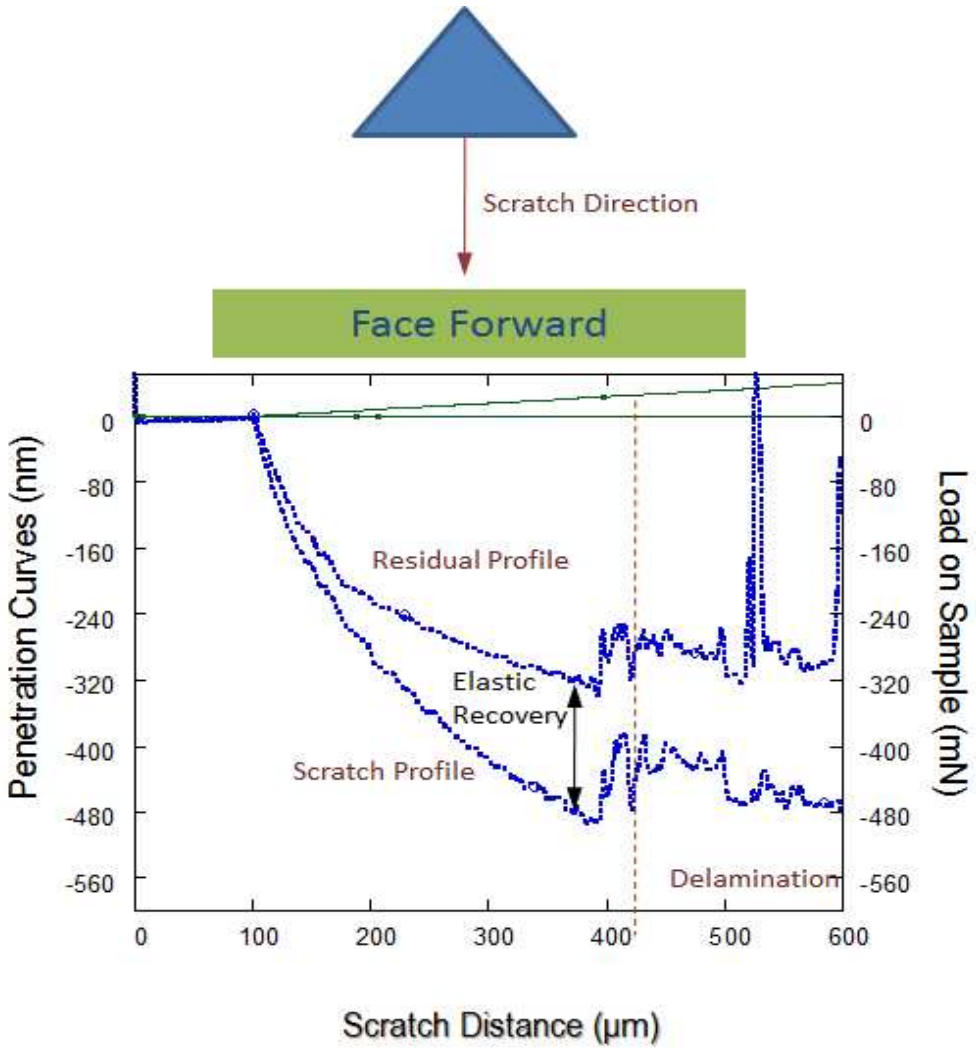
C. Results and Discussion

Scratch analysis was done with both edge and face forward conditions of Berkovich tip. However, edge forward condition did not result in delamination for any of the samples. As a result the following study is focused on analyzing the scratch resistance in a harsher face forward scratching condition. The edge forward condition and face forward condition scratch test for 600 ^{o}C, 2 hr annealed Cu/Ru/SiO_2 is shown in fig. 4.2 (a) and (b) respectively.

Scratch analysis of as-deposited $Cu/Ru/SiO_2$ overlayed on Cu/SiO_2 thin film samples is shows in fig. 4.3. Note that the scratch and residual profile for face forward scratch condition for the Cu(200 nm)/Ru(20 nm)/SiO_2 and Cu(200 nm)/SiO_2 thin films samples. It can be seen that there is higher elastic recovery and hardness in as-deposited $Cu/Ru/SiO_2$ samples compared to as-deposited Cu/SiO_2 samples. Also there is no delamination observed in $Cu/Ru/SiO_2$ sample and delamination is observed in Cu/SiO_2 samples. The critical load occurs at a load of about 9 mN for $Cu/Ru/SiO_2$ sample and about 4 mN Cu/SiO_2 sample as seen from the fig. 4.4. The critical load represents the point at which the diamond indenter has penetrated through the film thickness and hits the Si substrate. Hence the critical load that the $Cu/Ru/SiO_2$ sample can take is higher than that of Cu/SiO_2 sample. The critical point can also be seen from SEM micrograph of scratch fig. 4.5.


Scratch Direction
Edge Forward
Residual Profile
Plastic Deformation
Scratch Profile
Elastic Recovery
Penetration Curves (nm)
Load on Sample (mN)
Scratch Distance (um)
0
-80
-160
-240
-320
-400
-480
-560
0
100
200
300
400
500
600

(a)



(b)

Figure 4.2: The scratch test results for 600 ^{o}C annealed at 2 hr Cu/Ru/SiO_2 sample (a) Edge forward, and (b) Face forward condition.

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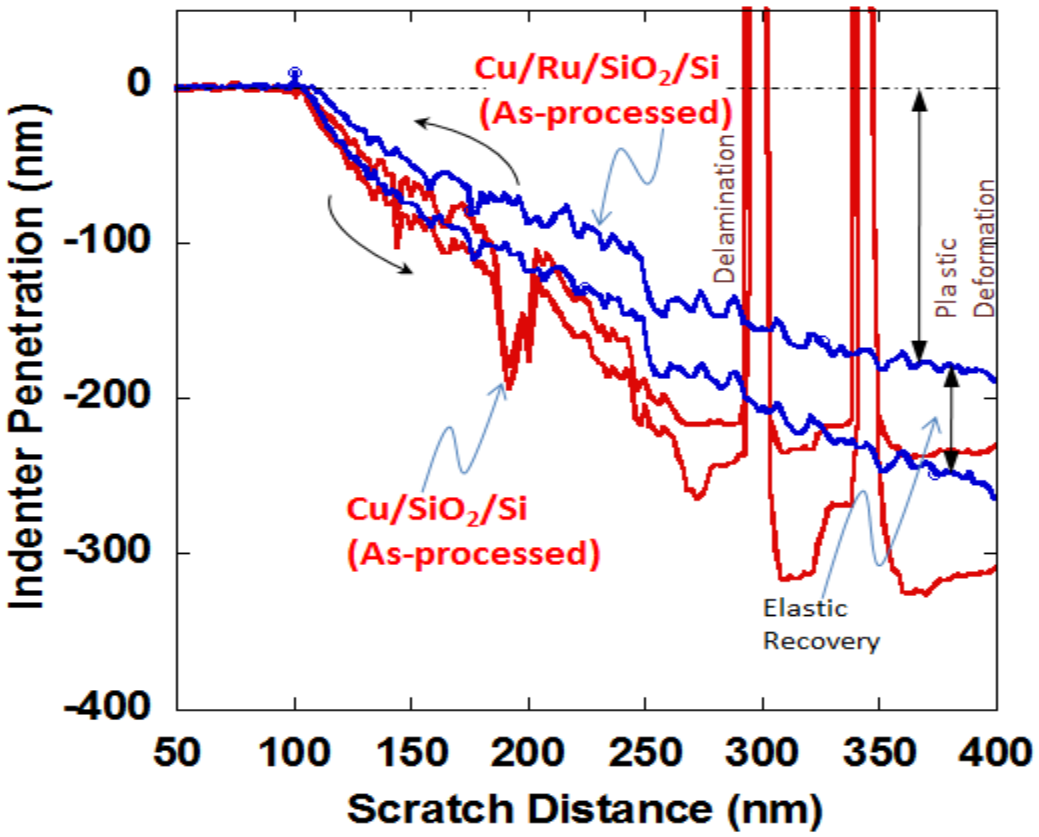


Figure 4.3: Scratch test analysis of as-processed $Cu/Ru/SiO_2$ overlayed on Cu/SiO_2 thin film samples in face forward scratch condition

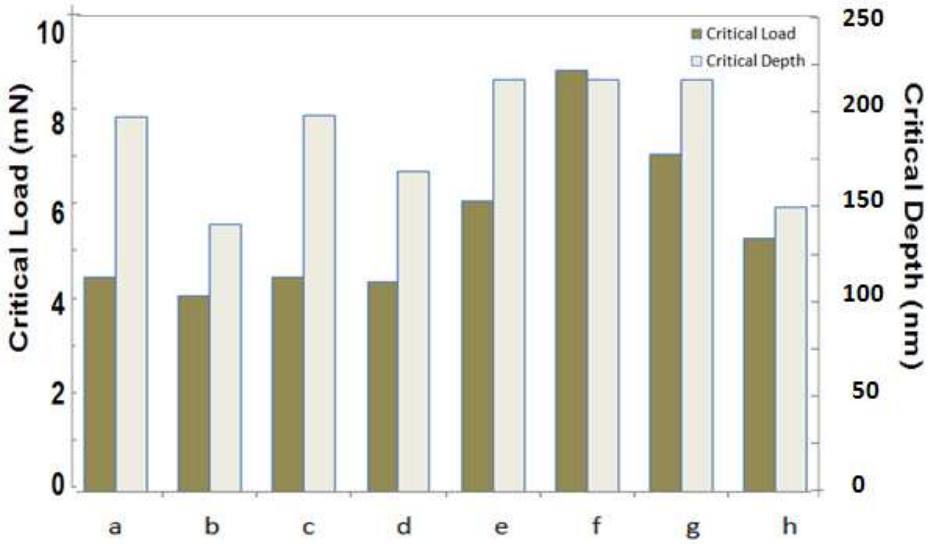
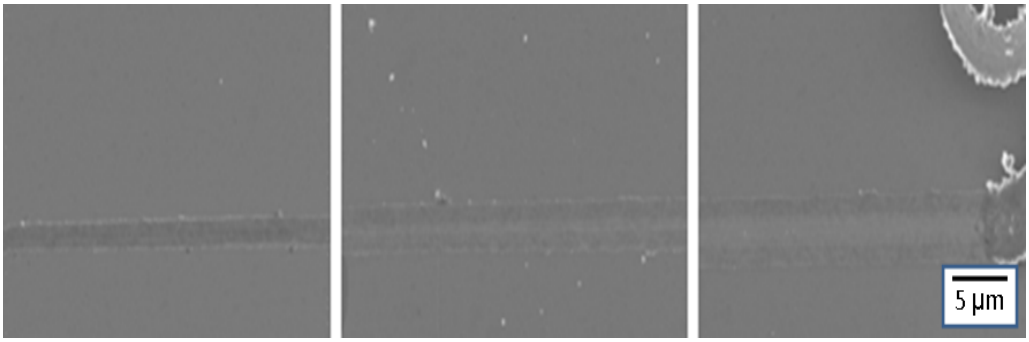
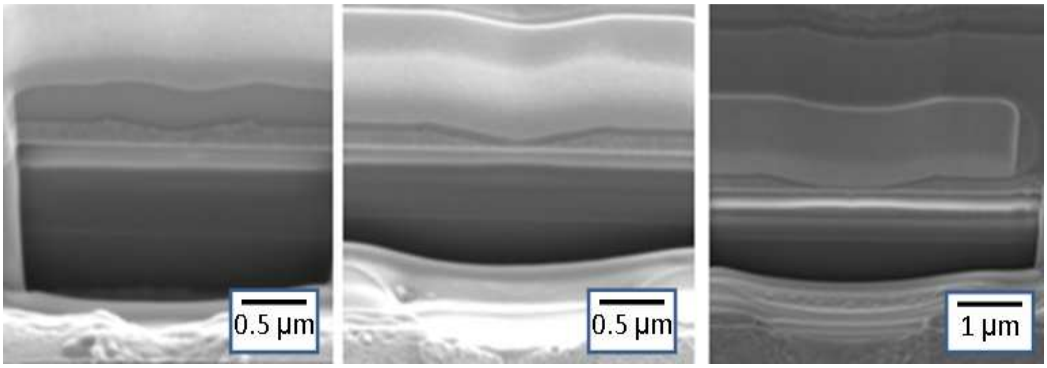


Figure 4.4: Critical load and critical depth for $Cu/Ru/SiO_2$ and Cu/SiO_2 thin film samples in face forward scratching condition



(a)



(b)

Figure 4.5: Post Scratch surface and cross section morphology of scratches in as-deposited Cu/Ru/SiO_2 sample imaged using (a) SEM and, (b) FIB analysis respectively.

The scratch analysis of 600 ^oC, 2 hr annealed Cu/Ru/SiO_2 overlayed on 600 ^oC, 0.5 hr annealed Cu/SiO_2 thin film samples are shown in fig. 4.6. Note that the scratch and residual profile for face forward scratch condition for 600 ^oC, 2 hr annealed Cu(200 nm)/Ru(20 nm)/SiO_2 and 600 ^oC, 0.5 hr annealed Cu(200 nm)/SiO_2 thin films samples. It can be seen that there is higher elastic recovery and hardness in annealed Cu/Ru/SiO_2 samples compared to annealed Cu/SiO_2 samples. There is no delamination in both the annealed samples. The critical load

occurs at a load of about 5.5 mN for Cu/Ru/SiO_2 sample and about 4.5 mN for Cu/SiO_2 sample can be seen from the Fig 3. The critical load represents the point at which the diamond indenter has penetrated through the film thickness and hits the Si substrate. The critical point can also be seen from the SEM micrograph of scratch fig. 4.7, and fig. 4.8.

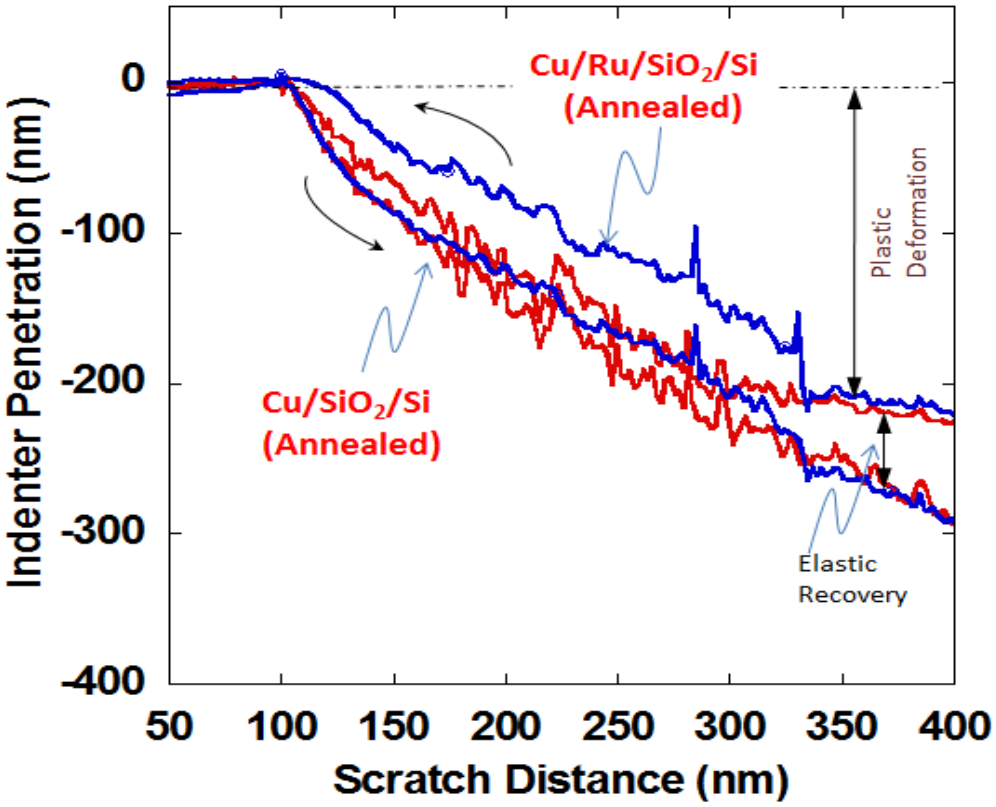
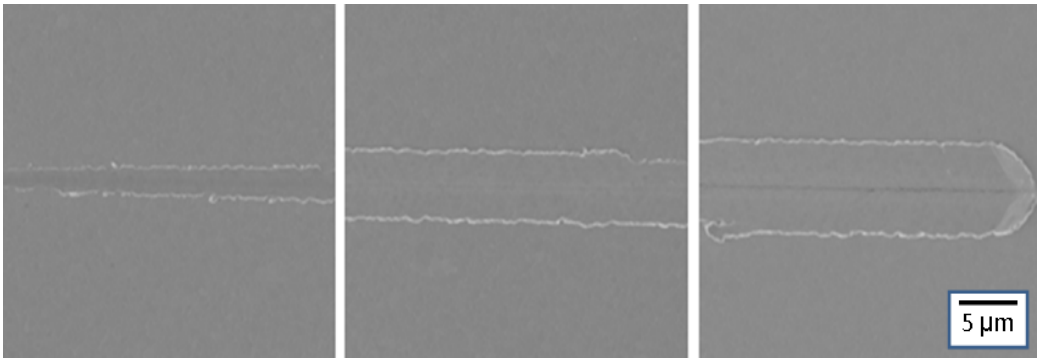
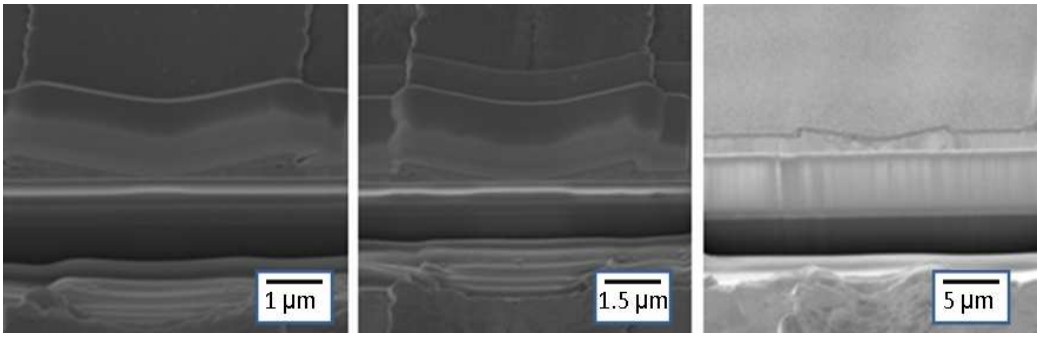


Figure 4.6: Scratch test analysis for 600 ºC annealed Cu/Ru/SiO_2 overlayed on Cu/SiO_2 thin film samples in face-forward scratch condition

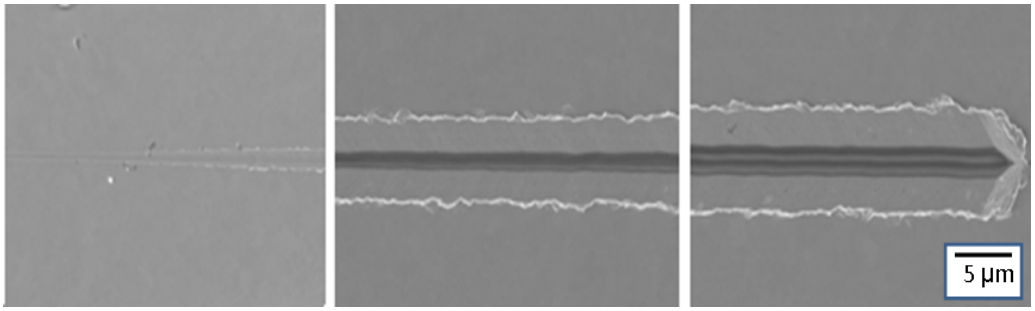


(a)

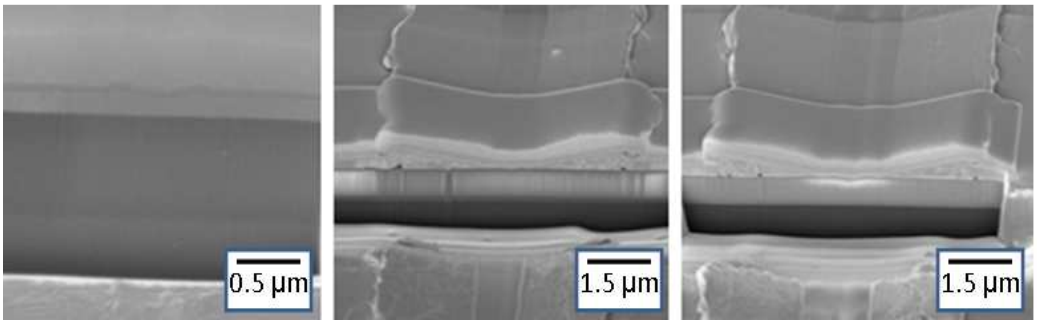


(b)

Figure 4.7: Post Scratch surface and cross section morphology of scratches in 600 ºC 2 hr annealed Cu/Ru/SiO_2 sample imaged using (a) SEM and, (b) FIB analysis respectively



(a)



(b)

Figure 4.8: Post Scratch surface and cross section morphology of scratches in 600 ºC 0.5 hr annealed Cu/SiO_2 sample imaged using (a) SEM and, (b) FIB analysis respectively.

From the FIB cross-sections, it is observed that no delamination of the film takes place in as-deposited and annealed $Cu/Ru/SiO_2$ samples implying that the film substrate adhesion is good. Deformation in $Cu/Ru/SiO_2/Si$ samples proceeds by ploughing through [25] and dragging of material and scraping occurs. Scratch response beyond the critical load is dominated by the underlying Si substrate and elastic recovery beyond the critical load is significant. Whereas, in case of Cu/SiO_2 samples there is delamination of the film seen at small critical load and only significant elastic recovery of the thin film sample. Also, the film debonds from the substrate easily.

The scratch analysis of $Cu/Ru/SiO_2$ samples showed higher elastic recovery and hardness in face forward scratch condition. Even at peak load the indenter does not penetrate through the film and suggests the strong scratch resistance of the $Cu/Ru/SiO_2$ multilayer. Whereas the Si substrate can be seen in the Cu/SiO_2 sample this implies no strong resistance to scratch is observed. In the face forward condition, the deformation proceeds in a distinctive manner.

The scratch resistance of the four samples can be compared in face forward condition based on critical load as shown in fig. 4.4. Note that the as-deposited $Cu/Ru/SiO_2$ sample represents higher critical load of 9 mN compared to 4.5 mN for as-deposited $Cu/Ru/SiO_2$ samples in the face forward scratch condition. This implies good scratch resistance of as-deposited $Cu/Ru/SiO_2$ sample when compared to as-deposited Cu/SiO_2 sample. The $Cu/Ru/SiO_2$ samples benefits from a stronger interface between Cu/Ru and later with the Si Substrate.

The presence of Ru layer (barrier layer) helps to increase the scratch resistance of the multilayered $Cu/Ru/SiO_2$ thin film samples.

The samples can also be compared base on the elastic and plastic work done on the samples during scratching before film failure (critical load) occurs. The plastic and elastic work plot of $Cu/Ru/SiO_2$ and Cu/SiO_2 samples is shown in fig. 4.9. The work done before the films fail there is greater elastic recovery in face forward scratching conditions and the deformation of the film is by plastic deformation and not delamination in case of $Cu/Ru/SiO_2$ thin film samples. Also, $Cu/Ru/SiO_2$ samples show higher elastic recovery and hardness at 10 mN load. Unlike in case of Cu/SiO_2 samples, the scratch does not penetrate through the film thickness to affect the underlying substrate at a load equivalent to the critical load in $Cu/Ru/SiO_2$ samples. The scratch width and depth as shown fig. 4.10 are also compared below the critical load (10 mN) as an indicator of scratch resistance.

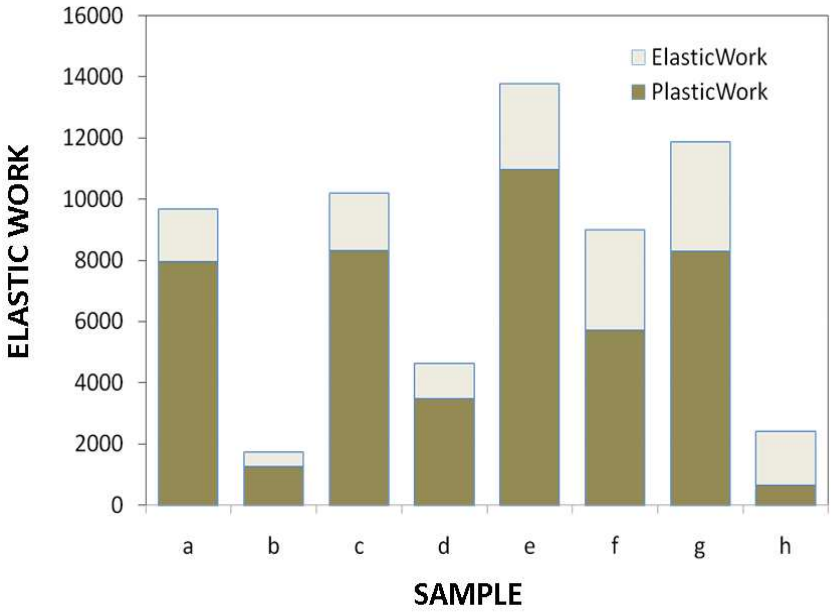


Figure 4.9: Plot of elastic and plastic work done on the Cu/Ru/SiO_2 and Cu/SiO_2 thin film samples

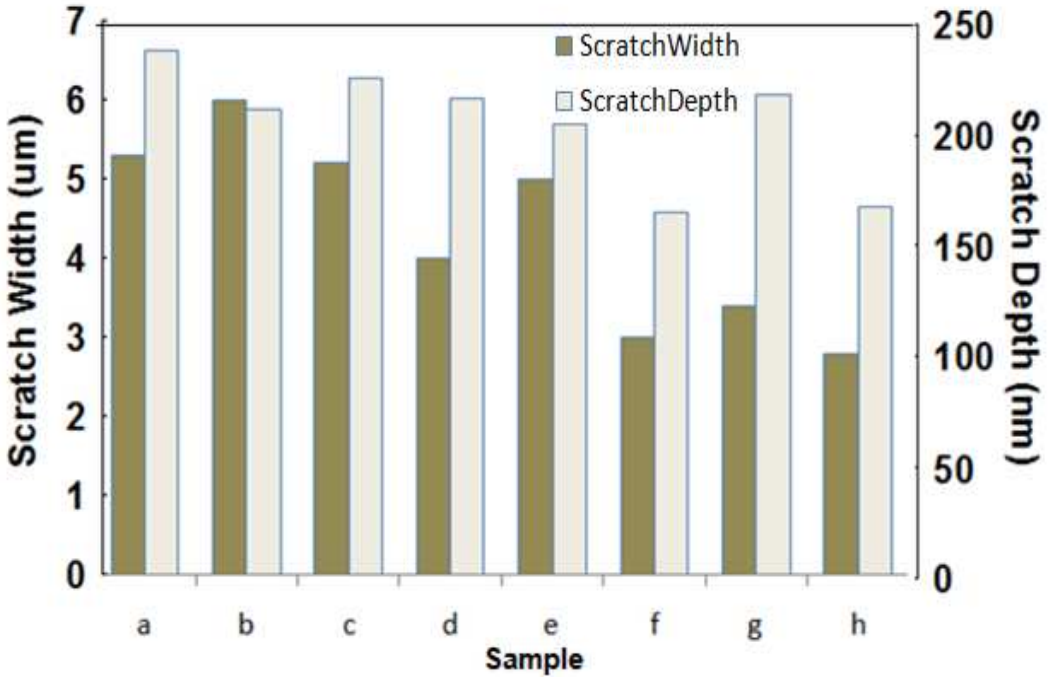


Figure 4.10: Comparision of scratch resistance of $Cu/Ru/SiO_2$ and Cu/SiO_2 samples in terms of scratch width and scratch penetration measured at scratch load of 10 mN.

The hardness of the thin films depends on the indentation depth [26,27]. The hardness is seen to increase as the depth of indendation approaches that of the film thickness due to the presence of harder substrate. Annealing the samples result in decrease of hardness. This decrease in hardness is significant at small depths where the hardness of the film is not influenced by the substrate. The presence of an oxide layer is indicated by sudden increase in depth of indenter due to the penetration of the indenter through the oxide layer which is indicative of the decrease in hardness [27]. Annealing the samples help to relieve stresses, increase softness, ductility and toughness and produce a specific microstructure [28].

In case of plastic deformation, when the stress (due to application of load) is removed, the material does not return to its previous dimensions but there is a permanent, irreversible deformation. With the increase in the compressive stress, the film begins to deform plastically. This stress level decrease slightly with the increasing temperature. When the material is taken beyond the yield point, it is deformed plastically and the stress is released, the material ends up with a permanent strain. If the stress is reapplied the material again responds elastically at the beginning upto a new yield point higher than the original yield point. This is strain hardening [29]. The strain hardening strengthens the material by plastic deformation. The amount of strain that the material will take before reaching the yield point is called elastic strain recovery. The magnitude of strain is limited by the difference in the thermal expansion of the substrate and the film and the temperature range used. The hardness is defined as the resistance to plastic deformation due to scratch testing. Thus it is the measure of plastic deformation.

The scratch resistance of the annealed $Cu/Ru/SiO_2/Si$ higher compared to annealed Cu/SiO_2 samples. This is due to the presence of Ru layer between Cu and SiO_2 which has better hardness and lower compressibility compared to copper. Also the FIB analysis of $Cu/Ru/SiO_2$ samples indicates no delamination which implies that Ru serves as a good adhesion layer between Cu layer and SiO_2 substrate.

D. Conclusion

In this study, we have evaluated the response of $Cu/Ru/SiO_2$ and Cu/SiO_2 thin film samples under dynamic scratch loading conditions as a measure of its

tribiological properties and nanoindendation to evaluate the mechanical strength. It was found that the $Cu/Ru/SiO_2$ samples showed higher elastic recovery and hardness compared to the Cu/SiO_2 samples. In case of Cu/SiO_2 as-deposited samples, there is poor adhesion between the Cu and the SiO_2/Si substrate as Cu does not adhere well to SiO_2 substrate and in case of Cu/SiO_2 annealed samples, fast diffusion of Cu into Si substrate at temperature below 200 ^oC forming Cu silicides leads to the degradation of the Cu film. In the case of $Cu/Ru/SiO_2$ samples Ru acts as a glue layer between the Cu and the SiO_2 substrate providing both strength and toughness against dynamic loading. Hence critical load for delamination is higher for $Cu/Ru/SiO_2$ samples compared to Cu/SiO_2 samples. Thus from the above analysis we can conclude that $Cu/Ru/SiO_2$ thin film samples present significant potential to be used in Cu metallization.

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Chapter 5

SUMMARY

Miedema's plot is used in the selection of Cu/Ru barrier system in Cu metallization. Miedema's plot illustrates a positive heat of formation which is evident of no intermixing between the Cu/Ru thin film layers. In the current study the requirements for Ru diffusion barriers layer for copper metallization was investigated. Thermal anneals up to 600 ^{o}C showed no signs of degradation/agglomeration and had good thermal stability. No evidence of Si was found on the top surface of the copper film and hence no interaction between copper and Si was observed, within the detection limit of RBS. Based on these results Ru diffusion barriers have the potential to increase the longevity of the films and can be used for high temperature electronics and integrated circuits.

Evaluation of Cu/Ru/SiO_2 and Cu/SiO_2 thin film samples under dynamic scratch loading conditions as a measure of its tribological properties and nanoindentation to evaluate the mechanical strength. It was found that the Cu/Ru/SiO_2 samples showed higher elastic recovery and hardness compared to the Cu/SiO_2 samples. In case of Cu/SiO_2 as-deposited samples, there is poor adhesion between the Cu and the SiO_2/Si substrate as Cu does not adhere well to SiO_2 substrate and in case of Cu/SiO_2 annealed samples, fast diffusion of Cu into Si substrate at temperature below 200 ^{o}C forming Cu silicides leads to the degradation of the Cu film. In the case of Cu/Ru/SiO_2 samples Ru acts as a glue layer between the Cu and the SiO_2 substrate providing both strength and toughness against dynamic loading. Hence critical load for delamination is higher

for $Cu/Ru/SiO_2$ samples compared to Cu/SiO_2 samples. Thus from the above analysis we can conclude that $Cu/Ru/SiO_2$ thin film samples present significant potential to be used in Cu metallization.

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