The Use of Voltage Compliant

Silicon on Insulator MESFETs for High Power and High Temperature

Pulse Width Modulated Drive Circuits

by

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ABSTRACT

Silicon Carbide (SiC) junction field effect transistors (JFETs) are ideal for switching high current, high voltage loads in high temperature environments. These devices require external drive circuits to generate pulse width modulated (PWM) signals switching from 0V to approximately 10V. Advanced CMOS microcontrollers are ideal for generating the PWM signals but are limited in output voltage due to their low breakdown voltage within the CMOS drive circuits. As a result, an intermediate buffer stage is required between the CMOS circuitry and the JFET.

In this thesis, a discrete silicon-on-insulator (SOI) metal semiconductor field effect transistor (MESFET) was used to drive the gate of a SiC power JFET switching a 120V RMS AC supply into a 30Ω load. The wide operating temperature range and high breakdown voltage of up to 50V make the SOI MESFET ideal for power electronics in extreme environments. Characteristic curves for the MESFET were measured up to 250°C. To drive the JFET, the MESFET was DC biased and then driven by a 1.2V square wave PWM signal to switch the JFET gate from 0 to 10V at frequencies up to 20kHz. For simplicity, the 1.2V PWM square wave signal was provided by a 555 timer.

The JFET gate drive circuit was measured at high temperatures up to 235°C. The circuit operated well at the high temperatures without any damage to the SOI MESFET or SiC JFET. The drive current of the JFET was limited by the duty cycle range of the 555 timer used. The SiC JFET drain current decreased

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with increased temperature. Due to the easy integration of MESFETs into SOI CMOS processes, MESFETs can be fabricated alongside MOSFETs without any changes in the process flow. This thesis demonstrates the feasibility of integrating a MESFET with CMOS PWM circuitry for a completely integrated SiC driver thus eliminating the need for the intermediate buffer stage.

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CHAPTER 1

INTRODUCTION

The increasing demand for electronics that can operate in high temperature environments has led to the commercial emergence of silicon carbide (SiC) and silicon on insulator (SOI) technologies. Due to the unique advantages of SiC, SiC junction field effect transistors (JFETs) provide an attractive solution for switching high current, high voltage loads in high temperature environments. To control the switching of the SiC JFETs a pulse width modulated (PWM) signal is required at the gate. An external circuit must be used to provide the gate control. For the SemiSouth power JFET used in these experiments the PWM signal is required to swing from 0V to approximately 10V [1]. Ideally a CMOS microcontroller would be used to provide the PWM gate control signal. However, the output voltage of a CMOS microcontroller is limited due to the low breakdown voltages of most CMOS technologies. To implement a CMOS microcontroller for SiC gate control an intermediate buffer stage is required between the CMOS circuitry and the JFET resulting in a more complicated gate control circuitry.

SOI metal semiconductor field effect transistors (MESFETs) provide an attractive solution to the gate control circuitry issue. Due to their ability to block large voltages and their wide operating temperature range they can replace the buffer stage previously required. Since the MESFETs can be fabricated on commercial SOI they can be implemented alongside an SOI CMOS microcontroller creating a single chip solution for the gate control circuitry of the

SiC power JFET. This allows for the simplification of the gate control circuitry and for the possibility of packaging it with the SiC JFET. To test the feasibility of this solution a SOI MESFET was used to drive the gate of a SiC power JFET which was switching a 120V$_{RMS}$ AC supply into a 30Ω load. Characteristic curves for the SOI MESFET were measured up to 250°C to demonstrate its ability to operate at high temperatures. To drive the JFET, the MESFET was DC biased and driven by a 1.2V square wave PWM signal to switch the JFET gate from 0V to 10V at frequencies up to 20kHz. This thesis is broken up into 3 main areas of discussion followed by a conclusions chapter. Chapter 2 is a literature review that discusses the problems presented by high ambient temperatures and the proposed solutions. Chapter 3 discusses in detail SOI MESFETs and presents the test results for the SOI MESFET at high temperatures. Chapter 4 describes the SiC JFET gate switching setup and the test results of the circuit are presented. Lastly Chapter 5 provides conclusions and ideas for future research.

CHAPTER 2

OVERVIEW OF HIGH TEMPERATURE ELECTRONICS

The demand for electronics capable of operating at high temperatures, greater than 125°C, has steadily increased over the past few decades. Industries including automotive, aerospace, nuclear environments, space exploration, deep-well drilling, and power semiconductors require certain electronics to operate at high ambient temperatures and in some cases high power as well. For example, electronics are often used to monitor and/or control subsystems that reside in hot spots such as combustion engines [2]. Without devices capable of withstanding high ambient temperatures the electronics must be placed far away from the subsystem or must be actively cooled. This results in additional overhead which can offset the benefits of the electronics from a system standpoint [3].

Bulk silicon processes in general are unable to operate reliably at high ambient temperatures much above 150°C. This has driven the development of new technologies to meet the extreme temperature demands. Silicon on insulator (SOI) processes have been successfully developed over the past two decades and are considered the best solution for low power applications up to 300°C [3]. For temperatures above 300°C wide bandgap semiconductors or vacuum electronics must be used for reliable operation. Wide bandgap semiconductors include SiC, GaAs, and GaAs heterostructures. This chapter provides an overview of high temperature electronics including technological challenges required for high temperature operation, Silicon and SOI operations and solutions, and wide-bandgap semiconductors.

Uunderstanding the need for specialized processes such as wide bandgap semiconductors requires first that the temperature effects internal to the semiconductor are characterized. Semiconductor device characteristics degrade as the ambient temperature increases, eventually reaching a point where they no longer provide the desired functionality for the circuit application [4]. There are four main areas of interest to focus on when discussing semiconductor temperature dependence; intrinsic carrier concentration, p-n junction leakage currents, thermionic leakage, and carrier mobility.

The concentration of free carriers within a device is largely temperature dependent. Semiconductor device operation is dependent upon the control of majority and minority carriers which is primarily accomplished in device fabrication through the introduction of dopants. For silicon at room temperature, the electron concentration in an n-type doped region is approximately equal to the concentration of n-type dopants introduced. Similarly, the hole concentration in the p-type doped region is approximately equal to concentration of p-type dopants. A lightly doped region within a device generally has a dopant concentration of 10^{14} to 10^{17} atoms per cubic cm. However, dopants are not the only source of free carriers within a device. Every semiconductor has thermally generated holes and electrons within the crystal. These free carriers are an intrinsic property of the semiconductor and therefore are referred to as intrinsic carriers. The intrinsic carrier concentration (n_i in cm^{-3}) is a strong function of

temperature as seen in Equation (2.1) [2]. N_C, N_V, and E_g are crystal properties and are relatively independent of temperature compared to the exponential term $E_g/2kT$.

$$n_i = \sqrt{NcNv} * e^{\frac{-Eg}{2kT}} \qquad (2.1)$$

where

N_C = electron density of states

N_V = hole density of states

E_g = bandgap energy of semiconductor

k = Boltzmann constant

T = temperature

Intrinsic carrier concentration, n_i, of silicon is approximately 10^{10} cm^{-3} at room termperature. This is insignificant when compared to the lightly doped regions with dopant concentrations of at least 10^{14} cm^{-3}. However, as the intrinsic carrier concentration increases with temperature they can become a significant percentage of the total carriers present. At approximately 300°C (573K) the intrinsic carrier concentration will reach the levels of the doped carrier concentrations. The electron concentration and temperature relationship can be seen in the graph shown in Fig. 21. The extrinsic (dopant) electron concentration is significantly larger than the intrinsic electron concentration until the temperature begins to approach 600K. As n_i approaches the dopant concentration, semiconductor junctions can become "washed out" losing their beneficial

characteristics. This effect can be reduced by increasing the doping density but is limited by reverse breakdown at p-n junctions.
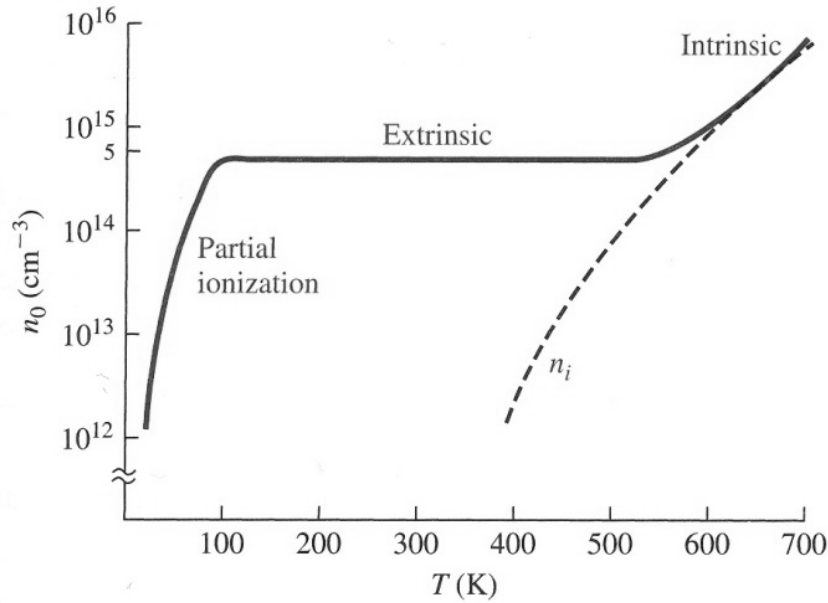
Fig. 1: Graph depicting the relationship between electron concentration and temperature in Kelvin [5].

Another area of concern in semiconductor devices as temperature increases is the reverse leakage current of p-n junctions. Rectifying junctions, such as p-n junctions, are essential to most semiconductor device operations such as diodes, MOSFETs, and BJT's. P-N junctions allow current to flow when a forward biased voltage is applied across the junction and block current flow when a reverse biased voltage is applied. The p-n junction consists of n-type and p-type doped regions which creates a depletion region at the junction. The depletion region has an inherent electric field which is why a forward biased voltage greater than the electric field is required for the junction to conduct. Even though under reversed bias conditions the junction blocks current flow, a small amount of

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current, called the reverse bias current, flows across the junction. In most circuit applications p-n junction reverse bias currents should be kept negligible with respect to the forward biased current. The behavior of p-n junctions is well understood. Equation (2.2) describes the voltage and current relationship across a p-n junction.

$$I = q * A * n_i^2 * \left(\frac{D_p}{L_p * N_D} + \frac{D_n}{L_n * N_A} \right) * \left[\exp\left(\frac{q * V_A}{2 * k * T} \right) - 1 \right] \qquad (2.2)$$

$$I_S = -q * A * n_i^2 * \left(\frac{D_p}{L_p * N_D} + \frac{D_n}{L_n * N_A} \right) \qquad (2.3)$$

where

N_A = acceptor doping density

N_D = donor doping concentration

L_p = diffusion length of p-type

L_n = diffusion length of n-type

D_p = hole diffusion constant

D_n = electron diffusion constant

V_A = applied voltage

A = cross-sectional area of the device

When a p-n junction is forward biased (V_A is positive) the exponential term in equation (2.2) is generally much larger than unity and the 1 can be dropped from the equation. When a p-n junction is reverse biased (V_A is negative) the exponential term becomes much smaller than unity. Thus equation (2.3) can be used to approximate the reverse bias leakage current. The equation

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for I_S shows that it has a large dependence on n_i and, as stated previously, n_i becomes very large as temperature is increased significantly. The other factors in equation (2.3) do not change with temperature as significantly as n_i and thus the reverse bias leakage current will increase with temperature with the square of the intrinsic carrier concentration. When the reverse bias leakage current becomes comparable to the magnitude of the forward bias current in a device, it may become harmful to device and circuit operation. Wide bandgap semiconductors generally have lower intrinsic carrier concentrations than silicon reducing the reverse bias leakage current by orders of magnitude.

Thermionic leakage can become troublesome as temperature increases. Thermionic leakage is when carriers gain enough energy to tunnel through or jump over energy barriers [6]. As temperature increases, carriers gain more energy which increases the chances of thermionic leakage, also referred to as emission. This effect can be greatly reduced with increased barrier heights, an advantage that wide bandgap semiconductors have over the conventional silicon based devices. Carrier mobility is also negatively affected with increasing temperature. As temperature increases significantly above room temperature a carrier's ability to move through a semiconductor crystal degrades. This is caused by increased collisions between atoms and carriers due to the increased thermal vibrations within the crystal lattice. This results in a decrease in the amount of current that a diode or transistor can carry. All semiconductors suffer from the issues described in this chapter. However, some semiconductors are more resilient

to the negative effects of temperature than others. The remainder of this chapter will investigate the different semiconductor processes.

2.2.   *SILICON AND SILICON ON INSULATOR PROCESSES*

Bulk silicon is currently by far the most widely used semiconductor process for many reasons. Silicon is an abundant element making it cheap as well as easy to use with many positive properties. Silicon grows a natural insulating oxide on its surface when exposed to oxygen. This provides a key element for the construction of metal oxide semiconductor field effect transistor (MOSFET) devices. MOSFETs, in turn, are the most popular and widely used devices in silicon processes. The current flow within a MOSFET is controlled by the density of carriers within the MOSFET's channel. The channel is formed when a voltage is applied to the MOSFET's gate causing charge to build up on the opposite side of the silicon dioxide insulator.   While bulk silicon MOSFETs have many advantages over other semiconductor devices for most moderate temperature applications (below 150°C), circuit and device damage or failure can occur as the ambient temperature increases to significantly higher levels. Equation (2.4) is the drain current equation for a MOSFET.

$$I_D = \mu * C_0 * \frac{W}{L} * (V_G - V_T)^2 \qquad (2.4)$$

where

I_D=drain current

μ=electron channel mobility

C_0=insulator capacitance per unit gate area

W=transistor gate-width

L=transistor gate-length

V_G=applied gate voltage

V_T=threshold voltage

As previously stated, the carrier mobility decreases as the ambient temperature increases. Equation (2.4) shows that as the carrier mobility decreases the on-state drain current decreases. The threshold voltage of the MOSFET also decreases with increasing temperature. This is an undesired effect that can lead to difficulty in turning off the device and even circuit failure. The sub threshold current, i.e. the current flowing through the device in the off-state, increases with temperature. The minimum obtainable off-state current is limited by the reverse leakage current of the p-n junction within the MOSFET. It was shown in the previous section that the leakage current through a p-n junction increases as n_i increases with temperature. Leakage currents can cause increased heat dissipation within the device as well as latchup issues. In CMOS integrated circuits the main path for leakage current occurs across the drain-substrate and well-substrate junctions [6]. Well substrate leakage occurs in PMOS devices where it is necessary to implant an n-type well into the p-type substrate. This creates a large amount of p-n junction area where leakage can occur. The drain substrate leakage is illustrated in Fig. 2. This current occurs deeper in the p-type substrate.
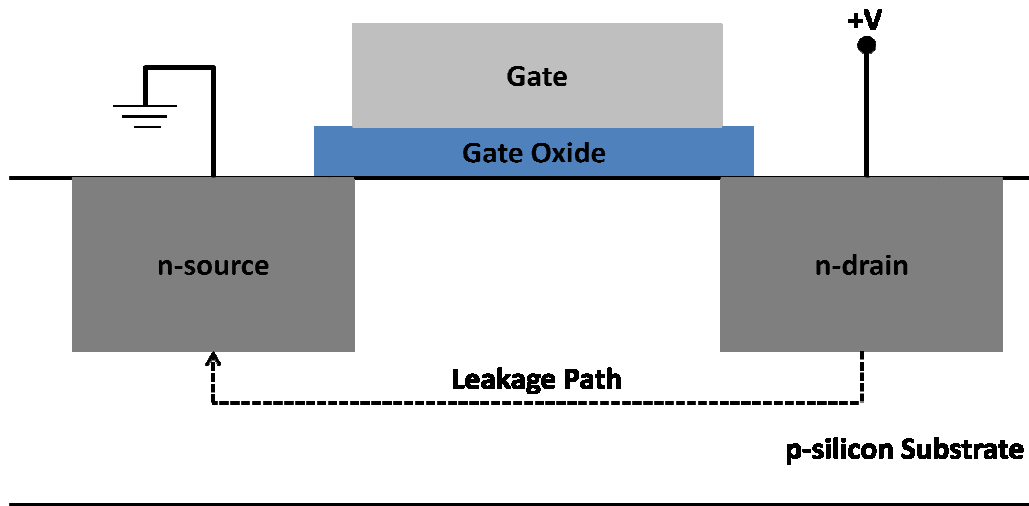
Fig. 2: Cross-section of a bulk silicon MOSFET illustrating the leakage path for the off-state leakage current.

As the ambient temperature is increased much above 150°C the different current issues can become very limiting to device operation. The on-state drain current to off-state leakage current ratio (I_{ON}/I_{OFF}) becomes unacceptable for many circuit applications. Circuit failure due to excessive junction leakage current is a common problem to all silicon processes operating at high ambient temperatures. This limits silicon devices in general to below 300°C [6]. Wide bandgap semiconductors have much lower reverse bias leakage currents which allows them to operate better at higher temperatures well above 300°C. Bulk silicon has many issues when operating at temperatures much higher than 150°C. However, if the off-state leakage current is reduced, silicon MOSFETs can operate closer to the theoretical limit of silicon (300°C).

Silicon on insulator (SOI) technologies were developed, in part, to increase the temperature operation range of silicon devices. In an SOI technology individual devices are isolated from the substrate and other devices due to the

addition of a SiO_2 insulating layer. This is illustrated in Fig. 3. A large SiO_2 layer is grown on top of the p-type silicon substrate which isolates the n-type source and drain regions and the p-type channel region from the substrate. SiO_2 blocks are also inserted around the device to completely isolate it from neighboring devices. With the additional isolation of the devices, SOI technologies reduce the p-n junction area on both the source and the drain. This decreases the leakage area of the junctions. The drain-substrate leakage is greatly reduced and the well-substrate leakage is almost completely eliminated. The bottom SiO_2 insulator greatly reduces the off-state leakage current between the source and drain because this typically occurs deeper in the p-type substrate. Comparing Fig. 3 to Fig. 2 it is apparent that the main path of leakage current from the drain to source is no longer available.
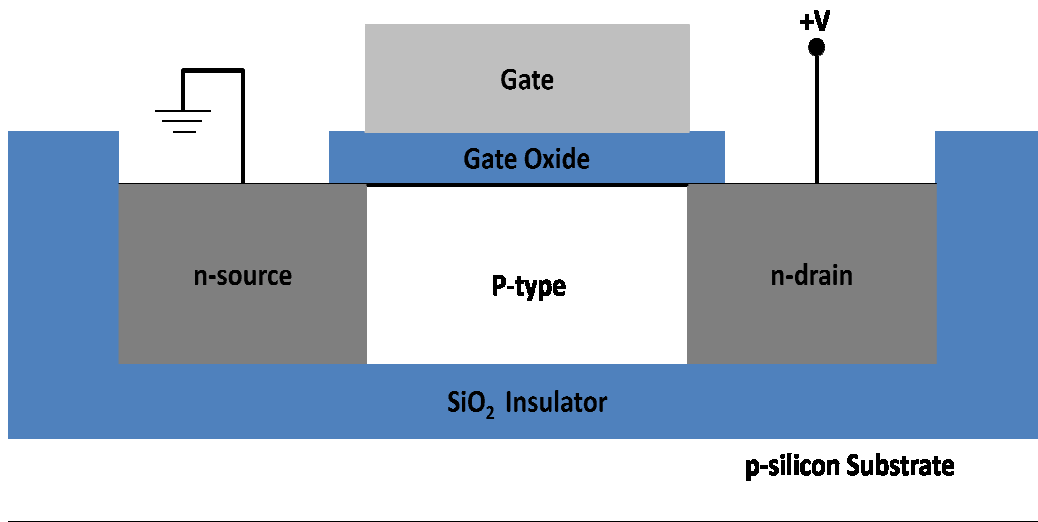
Fig. 3: Cross-section of a SOI MOSFET illustrating the isolation of the devices with respect to the p-type substrate and neighboring devices.

SOI devices are capable of operating in the 200°C to 300°C temperature range. Certain SOI processes have demonstrated MOSFETs used for small signal applications up to 300°C for extended periods of time (> 1000 hours) [6]. SOI does have some drawbacks when compared to bulk silicon processes. It is more difficult and costly to implement than bulk processes. Gate oxide degradation can still occur at high temperatures. This is caused by charges becoming trapped in the gate oxide and at the oxide/semiconductor interface. Trapped charges occur when carriers become energized enough due to increased temperature and large electric fields, causing these energized carriers to jump over or move around the insulator. Some charges become trapped in the SiO_2 during this process. This can lead to undesired shifts in a MOSFETs threshold voltage which can result in circuit failure. There are SOI technologies that are designed to ensure lower electric fields at the gate to avoid oxide degradation. Electro-migration in the aluminum interconnections at high temperatures can also limit high temperature operations.

SOI is currently well commercialized for certain applications such as high temperature operation up to 300°C; however it is not ideal for high power applications much above 150°C. In high power electronics there are large currents flowing through the devices which increase the internal power dissipation. During switching there are brief periods (microseconds) where both the current and voltage are very high causing large spikes in the power dissipation. All power dissipation within a device increases its temperature. As the temperature increases the leakage current increases raising the devices

temperature further creating a positive feedback loop for temperature increase. Due to the increased operating temperature of the devices, unacceptable leakage currents occur at much lower temperatures compared to low power SOI devices. In summary, SOI processes work well at temperatures up to 300°C for low power applications. At temperatures above 300°C and high power operation above 150°C a different semiconductor solution is needed. Wide bandgap semiconductors have been researched and many show promise for high temperature and/or high power applications.

2.3. *WIDE BANDGAP SEMICONDUCTORS*

Wide bandgap semiconductors have been targeted for use in high temperature environments above 300°C, and for power electronic applications, above 150°C [7]. As discussed in section 2.1, materials with higher bandgap energies should suffer less from junction leakage currents and intrinsic carrier problems. Equations (2.1), (2.2), and (2.3) all attest to this. This section will discuss GaAs, GaAs heterostructures and their advantages and disadvantages for high temperature electronics. SiC is another promising wide bandgap semiconductor that will be discussed further in section 2.4.

GaAs is the next most commonly used semiconductor material next to silicon. It has a bandgap energy of 1.34eV where silicon's bandgap energy is 1.1eV [7]. The higher bandgap energy should allow for higher temperature operation than silicon technologies. However, there are many drawbacks to using GaAs. GaAs does not have an adherent oxide like silicon making it impossible to construct MOSFETs. Instead, MESFETs are the most common device in GaAs

(more information on MESFETs will be provided in Chapter 3). The Schottky barriers at the gate of the MESFETs have large leakage currents at high temperatures. Leakage current across the drain junction also increases significantly with temperature. Electro migration causes the interconnections to degrade limiting the circuits to 300°C. The theoretical temperature limit for GaAs is 400°C based upon junction leakage, but to achieve temperatures much higher than 250°C to 300°C improved ohmic contacts and interconnections are needed. Other wide bandgap semiconductors show more promise for high temperature operation.

GaAs heterostructures are another possible solution for high temperature electronics. III-V materials can be grown on GaAs substrates to create heterostructures which offer many potential advantages. Heterojunction process advantages include reduced contact problems, reduced forward voltage drops across p-n junctions, and reduced resistive parasitics. The above mentioned advantages exist without compromising high temperature junction performance. GaAs heterostructures have been shown to operate at temperatures up to 550°C [6]. However, like GaAs, high temperature capable contacts are still needed. One popular heterostructure uses AlGaAs. AlGaAs has a wider bandgap than GaAs with the same crystal lattice. GaAs/AlGaAs/GaAs heterojunctions have lower reverse leakage currents when compared to GaAs. Heterostructures avoid the generally large resistive contacts associated with wider bandgap materials by using the lower ohmic contact to GaAs.

2.4. SILICON CARBIDE

SiC is the most mature wide bandgap semiconductor material that is well suited for high temperature operation [8]. Furthermore it is more commercially available than the other wide-bandgap semiconductors and has the ability to grow a thermal oxide which is useful in fabrication and gate dielectrics. There are an infinite number of SiC polytypes, currently 6H-SiC and 4H-SiC are the only two polytypes commercially available. Table 1 shows the basic electrical properties for different semiconductor materials including the 6H and 4H polytypes.

Table 1: Semiconductor properties of different semiconductor materials [8].

Material	E_g (eV)	n_i (cm^{-3})	ε_r	μ_n ($cm^2/V \cdot s$)	E_c (MV/cm)	v_{sat} ($10^7 cm/s$)	λ ($W/cm \cdot K$)	Direct/ Indirect
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8×10^6	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7×10^{-1}	11.1	350	1.3	1.4	0.8	I
InN	1.86	$\sim 10^3$	9.6	3000	1.0	2.5	-	D
GaN	3.39	1.9×10^{-10}	9.0	900	3.3	2.5	1.3	D
3C-SiC	**2.2**	**6.9**	**9.6**	**900**	**1.2**	**2.0**	**4.5**	**I**
4H-SiC	**3.26**	**8.2×10^{-9}**	**10**	**720^a 650^c**	**2.0**	**2.0**	**4.5**	**I**
6H-SiC	**3.0**	**2.3×10^{-6}**	**9.7**	**370^a 50^c**	**2.4**	**2.0**	**4.5**	**I**
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20	I
BN	6.0	1.5×10^{-31}	7.1	5	10	1.0*	13	I
AlN	6.1	$\sim 10^{-31}$	8.7	1100	11.7	1.8	2.5	D

Note: a — mobility along a-axis, c — mobility along c axis, * — estimate.

Among its advantageous properties over silicon, SiC has a wider bandgap energy (E_g), a lower intrinsic carrier concentration, a larger saturated drift velocity (v_{sat}), a higher electric breakdown field (E_c), and a higher thermal conductivity (λ) [9]. The wide bandgap energy of the 4H and 6H polytypes (3eV to 3.26eV) is approximately three times larger than the 1.1eV of silicon. The electric

breakdown field is an order of magnitude larger than silicon's allowing for a reduction in drift layer thickness. The thermal conductivity of SiC is three times larger than that of silicon which allows for more power efficient high temperature operation [10]. 6H-SiC has lower electron mobility (μ_n) than 4H-SiC which is why 4H-SiC is the more commonly used polytype. SiC does have some issues associated with it. The defects which occur most often are screw dislocations called micropipes which have negative effects on devices and limit the SiC's effective wafer size [11].

Many of the devices created in silicon can be fabricated in SiC and have advantages over their silicon counterparts. An example is the Schottky barrier diode (SBD), or metal semiconductor diode. It can be built to withstand high voltages in SiC, which is not feasible in silicon due to the lower barrier heights between the metals and silicon. The SiC SBD also has much lower reverse currents then the silicon SBD. SiC transistors include both unipolar and bipolar. The bipolar transistors include bipolar junction transistors (BJT) and the insulated gate bipolar transistor (IGBT). However since the IGBT has an odd number of p-n junctions in the current path, there is a large junction voltage drop (approximately 3V) which directly adds to the power dissipation. The unipolar transistors include MOSFETs and junction field effect transistors (JFET). SiC MOSFETs have yet to meet the full expectations of an efficient high power and high temperature device mostly due to the low mobility issues in the inversion layer. The SiC JFET has high input impedance and avoids issues associated with the MOSFET due to the lack of a gate oxide. JFET devices with superior

properties have been successfully fabricated and are currently in use in industry [12].

2.5. CONCLUSION

Due to the increasing demand for high temperature electronics, the different semiconductor solutions were discussed in this chapter. The short fallings of bulk silicon technologies were discussed, and it was concluded that bulk silicon cannot operate reliably much above 150°C. SOI technologies were discussed and shown to be one of the best options for high temperatures (below 300°C) and low power. The isolation from the substrate and other devices reduced the issues such as junction leakage seen with bulk silicon. However, SOI is more costly than bulk silicon and still suffers from gate oxide degradation at high temperatures. SOI is also not ideal for high power applications at increased temperatures. For temperatures above 300°C and for high power applications above 150°C wide bandgap semiconductors showed promising results. Their bandgap energies above that of silicon give them an advantage for these areas of operation. The advantages and disadvantages of GaAs, GaAs heterostructures, and SiC were discussed. SiC shows the most promise of the wide bandgap semiconductors and is a more mature process. It is also the most commercially available wide bandgap semiconductor.

CHAPTER 3

SOI MESFETS

MESFETs have been used in many different applications for decades with their inherent robustness making them ideal candidates for these applications. MESFETs created on silicon substrates have been attempted with mixed results in the past. The inherent properties of silicon on insulator (SOI) technologies allow for successful fabrication of silicon MESFETs. SOI MESFETs have been constructed by researchers at ASU on multiple processes showing some significant advantages over traditional MOSFETs for certain circuit applications. They can be designed to withstand large blocking voltages without damage to the device and operate well over a wide temperature range. This makes them a logical choice for use in the SiC JFET gate drive circuit described in chapter 4. This chapter will begin with a discussion of the background of MESFETs and basic MESFET operation. Following this is a description of the fabrication process for SOI MESFETs and the careful considerations that need to be taken. The next section describes the high breakdown voltage of SOI MESFETs. The last two sections are about the SOI MESFET used in the SiC JFET gate drive circuit showing the MESFETs physical characteristics and high temperature performance.

3.1. MESFET OPERATION AND BACKGROUND

Metal semiconductor field effect transistors (MESFETs) are majority carrier devices that have certain advantages over MOSFETs and can be used for a variety of purposes. The MESFET does not have an insulating gate like the

MOSFET; instead it uses a Schottky barrier gate to control the conductivity within the channel. They were previously manufactured using compound semiconductor processes such as GaAs. Compound semiconductors provide increased mobility among other advantages. However, there are not many examples of MESFETs successfully constructed on a silicon substrate. The inherent properties of a MESFET such as majority carrier conduction and the lack of a gate oxide can be positive attributes compared to the MOSFET. Due to the absence of an insulating gate, the MESFET has some different characteristics. There is gate current present and the gate capacitance is reduced. Also, the oxide interface states are eliminated. Since the MESFET is a majority carrier device, theoretically the mobility is capable of reaching bulk values.

Previously, for both MESFETs and MOSFETs to be combined on the same chip, the use of two separate substrates was needed. In the past MESFETs fabricated on silicon substrates have been attempted with varying degrees of success. However, the lack of an insulating layer makes it difficult to control the conduction area within the channel. There have been a few different methods to confine the channel conduction such as silicon on sapphire, the use of a doped well or a molecular beam epitaxial layer. Recently MESFETs have been fabricated using silicon on insulator (SOI) technologies and have demonstrated promising results [13]. The buried oxide in any SOI technology allows for decent control of the channel conduction area within a MESFET.

SOI MESFETs are 4 terminal majority carrier devices compared to GaAs MESFETs which are 3 terminal devices due to the thicker insulating layer. This

allows for control of the body in SOI MESFETs [14]. To create MESFETs in SOI technologies a self aligned silicide (salicide) step is used to create the near ideal Schottky gate. The current in the channel is controlled by the width of the depletion region under the Schottky contact. This in turn is controlled by the voltage applied at the gate of the device. Even though a significant amount of gate current is drawn (when compared to a MOSFET), the SOI MESFET is in fact a voltage controlled device not a current controlled device. For an n-type MESFET the channel is lightly doped n-type and the source and drain are heavily doped n-type. The lightly doped gate region is isolated from the heavily doped source and drain regions by a source access region and a drain access region respectively. The length of the source access region (L_{aS}) and the length of the drain access length (L_{aD}) determine the performance of the MESFET. A cross section of the SOI MESFET displaying source access and drain access regions can be seen in Fig. 4. Another important parameter for MESFET operation is the thickness of the silicon channel defined between the bottom junction of the silicide gate and the buried oxide layer. If the channel is too thin the device will have low current drive. If the channel is too thick it becomes difficult to fully deplete and thus difficult to turn of the device. The ideal thickness of the SOI MESFET channel is between 100nm and 200nm resulting in a reasonable threshold voltage between -0.5V and -1.5V [15]. The necessity of a relatively thin channel for MESFET operation is what makes SOI technologies such an attractive solution for silicon MESFETs.
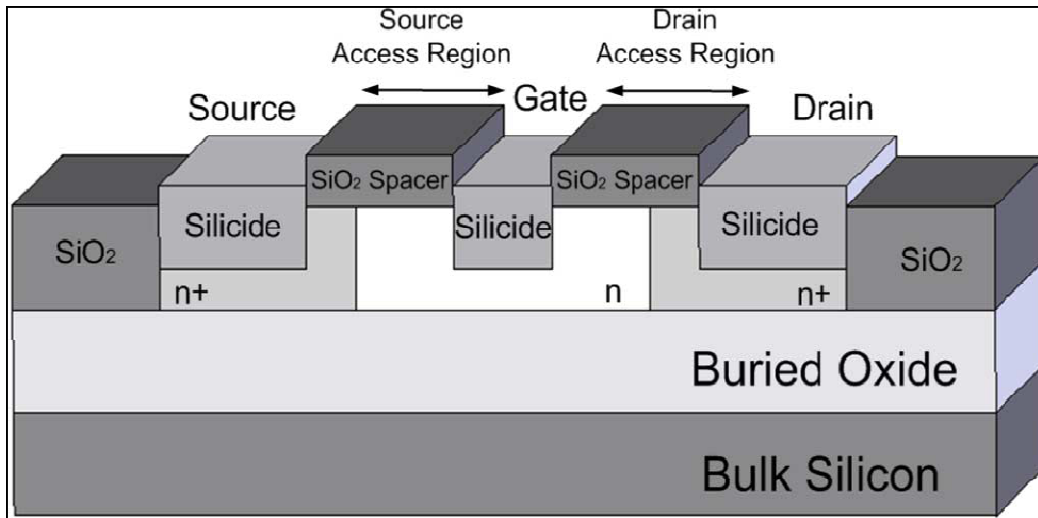
Fig. 4: SOI MESFET cross section showing the oxide spacers that define the source and drain access lengths and the silicide blocks that are used for the Schottky gate and the source and drain contacts [16].

The material used in the construction of the MESFET gate is critical for improving MESFET performance. Metal silicon junctions have been used to create the Schottky barrier gate. However, the use of silicide to form the gate is also a viable option. It requires a more complex fabrication process but it is found in many CMOS processes. To form a silicide, metal is deposited on a silicon surface and heated (the exact temperature depends on the metal used). The metal and silicon react forming a silicide. The metal silicon compounds that are most often used are platinum, titanium, cobalt, and nickel. The most important physical attributes of silicides are barrier height, temperature formation, and resistivity.

The use of platinum as a silicide has its advantages and disadvantages. It is an expensive choice. The platinum barrier height for n-type is approximately 0.85eV which is relatively high. Its p-type barrier type is much lower at

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approximately 0.21eV [13]. Thus platinum works well for n-type MESFETs but not for p-type MESFETs. Silicidation occurs at a lower temperature of 550°C. This can have an impact on process steps that follow the silicidation step because temperatures need to be kept below 550°C. Platinum silicidation also requires a clean silicon interface since it cannot silicide through SiO_2. The next option for silicide is titanium which can silicide through SiO_2. Titanium requires a two step anneal process to achieve low resistivity of the silicide [13]. To create the low resistivity form of titanium silicide ($TiSi_2$) the material must be brought above 750°C. Titanium silicide can interact with the dopants present resulting in a larger doping at the junction. This can degrade the junction resulting in a poor Schottky gate. Titanium is also not a good option for small feature sizes. Below approximately 0.5µm it becomes difficult to convert $TiSi$ to $TiSi_2$. The barrier heights are approximately equal, 0.58eV for n-type and 0.47eV for p-type, making the construction of both n-type and p-type MESFETs possible [13].

The next option for a silicide gate is cobalt. Cobalt, like titanium, requires a two step anneal process with an anneal temperature between 600°C and 800°C [13]. The barrier height is approximately 0.64eV. Cobalt silicide has a very low resistivity and is scalable to 0.2µm making it useful for smaller feature length technologies. Like titanium, it is sensitive to SiO_2 on the interface so a clean interface is needed. Cobalt also consumes a lot of silicon during the silicidation process which can result in rough junctions and high mechanical stress. A newer metal used for silicidation that has many positive qualities is Nickel. It can be used with feature sizes less than 100nm, allowing for MESFETs to be constructed

in cutting edge technologies. Nickel is a mobile species which reduces voids during silicidation. Nickel silicide's low resistivity form is NiSi so it consumes less silicon during silicidation. The interface created at the junction is smooth lowering the reverse bias current. The anneal temperature is between 200°C and 600°C so backend processing must be kept below 600°C which is a limitation. The barrier heights for n-type and p-type are 0.67eV and 0.43eV respectively allowing for the construction of both n-type and p-type MESFETs. It has no interaction with the dopants avoiding the issues associated with that.

Due to the widespread popularity of SOI CMOS the commercial production of MESFETs is possible. SOI substrates are widely used for advanced USLI logic and have shown many advantages for analog applications due to reduced parasitics and low substrate losses. Declining CMOS voltages have limitations on certain circuits such as voltage controlled oscillators. SOI MESFETs can be designed to have high breakdown voltages greater than 60V which will be discussed in section 3.3. SOI MESFETs demonstrating the feasibility and advantages of the devices have been constructed in SPAWAR, Peregrine, Honeywell and MIT-Lincoln Labs device process technologies.

3.2. *SOI MESFET FABRICATION*

The complex geometry of SOI MESFETs requires careful consideration during fabrication. All three dimensions of the device must be taken into account when constructing the MESFET. Also, important layers that are critical to MESFET operation may not be critical in CMOS processes meaning the level of precision needs to be taken into account. The SOI MESFET structure is shown in

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Fig. 4. As previously described, L_{aS} and L_{aD} are defined by the oxide spacers and the area between these oxide spacers is the silicide gate. The silicide layer is key for SOI MESFET fabrication since it is used in the source, drain and gate. As previously described, the choice of silicide is important for MESFET operation. The width of the depletion region must be able to reach the buried oxide to turn off the device. Since the silicidation process consumes silicon in the channel, the channel thickness can be controlled. SiO_2 spacers are used for patterning and creating the source and drain access regions. By using a normally critical layer for the SiO_2 spacers such as the gate stack for a MOSFET, more precision can be achieved. When considering fabrication in a CMOS process the order of the silicide block layer step with respect to the source and drain implant step needs to be known. If the silicide block layer is before the source/drain implant the access length can be defined by the implant mask. If it is after, the access length is defined by the silicide block layer. The source and drain access length is important for isolation of the gate as well as increasing the breakdown voltage of the device. Other parameters that should be considered during fabrication are the threshold voltage adjust and edge implants.
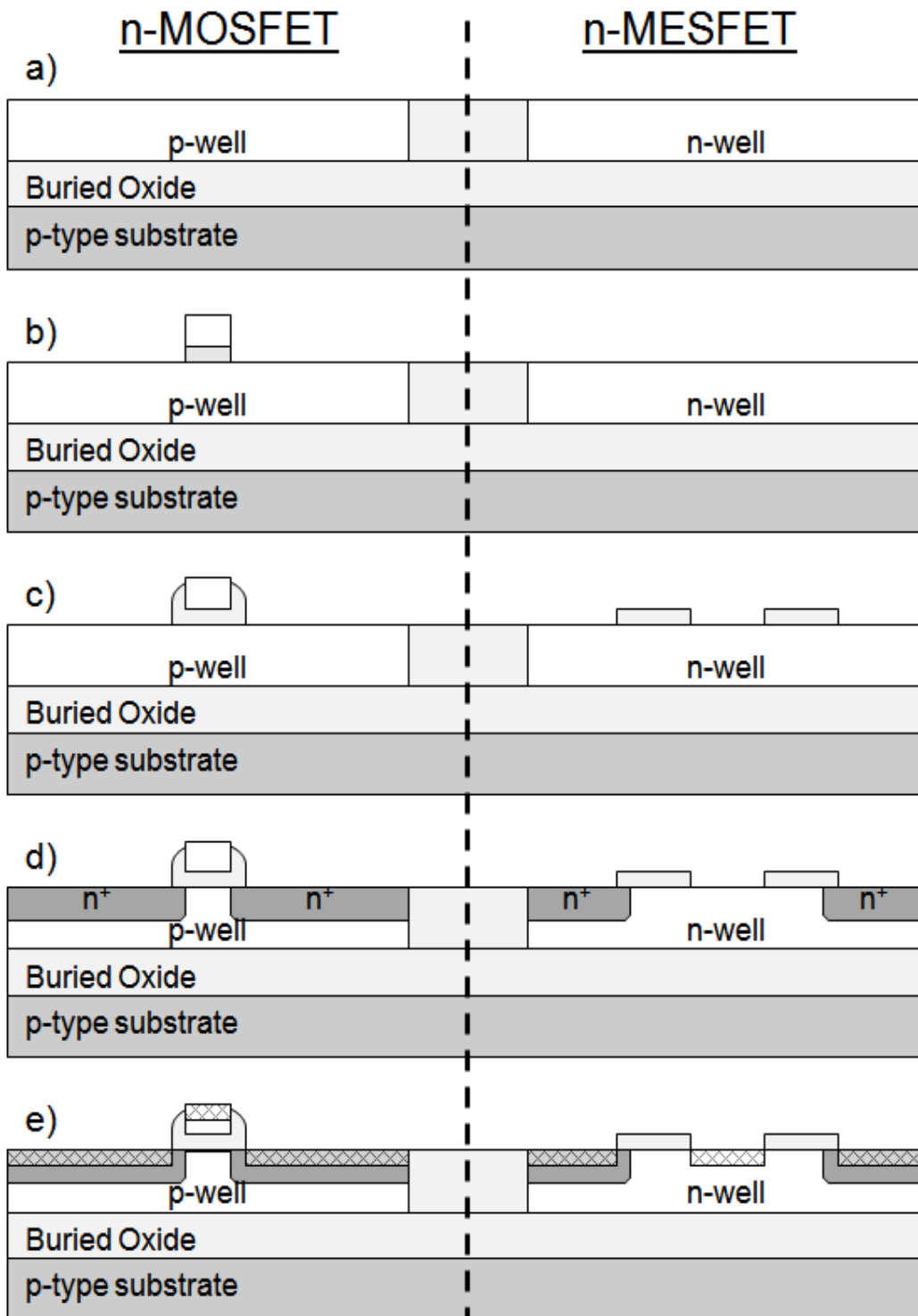
n-MOSFET | n-MESFET

a)

p-well | n-well

Buried Oxide

p-type substrate

b)

p-well | n-well

Buried Oxide

p-type substrate

c)

p-well | n-well

Buried Oxide

p-type substrate

d)

n^+ | n^+ | n^+ | n^+

p-well | n-well

Buried Oxide

p-type substrate

e)

p-well | n-well

Buried Oxide

p-type substrate

Fig. 5: Comparison of fabrication steps for n-type MOSFETs and MESFETs for an SOI CMOS process [17].

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The fabrication of SOI MESFETs follows the same steps as the fabrication of a MOSFET through the local oxidation of silicon (LOCOS) step. Fig. 5 shows the fabrication steps of a MESFET and a MOSFET simultaneously. First the active layers for both the MESFET and MOSFET are formed. In the second step the MOSFET gate stack is patterned. Following this, oxide is deposited across the wafer via plasma enhanced chemical vapor deposition. The Schottky gate formation is started with the patterning of SiO_2 via the silicon block (SB) layer. This is a critical step for MESFETs because it creates the access regions that isolate the gate from the source and drain. The oxide not covered by SB is etched away. In the fourth step the source and drain regions of the MESFET and MOSFET are heavily doped. A layer of photoresist is needed over the channel to keep it lightly doped and is removed afterwards. Then cobalt (or nickel) is deposited on the wafer and the exposed silicon will react during annealing to create the silicide. Lastly, the non reacted cobalt (or nickel) is removed and the MESFET continues through the rest of the process steps that are common to CMOS. It must be noted that MESFETs are not self aligned. L_{aS} and L_{aD} are slightly smaller than the SB layer because of the lateral growth of the silicide contacts. This limits the minimum size of the access regions and can cause possible misalignment. This also results in a gate length that is slightly larger than SB spacing (limits minimum gate length).

3.3.   *SOI MESFET BREAKDOWN VOLTAGE*

CMOS voltages have seen a steady decline as feature sizes continue to decrease which has caused many limitations in newer technologies. The

maximum voltages for CMOS technologies are determined by the MOSFET's ability to handle applied voltages. MOSFET breakdown usually occurs at the gate oxide. With each new technology's reduced feature sizes the thickness of the gate oxide decreases. With the reduced oxide thickness the electric field across it becomes very high even when low voltages are applied. The gate leakage current increases which can result in the destruction of the oxide providing a low resistive path between the gate and source/drain. These issues are what leads to reduced operating voltages. However, there is still a need for higher voltage tolerances in certain circuits. Inductive load circuits such as voltage controlled oscillators, DC-DC converters and certain types of power amplifiers can exceed the process voltage limits.

There have been multiple proposed solutions to the issue of reduced process voltages. One of the more popular solutions are laterally diffused MOSFETs (LD-MOSFETs). To create an LD-MOSFET a lightly doped region is placed between the heavily doped drain contact and the gate oxide region. This effectively reduces the electric field across the gate oxide to the channel since some of the electric field is reduced over the lightly doped region. LD-MOSFETs with breakdown voltages greater than 100V have been constructed. The drawback of LD-MOSFETs is that they require extra processing steps for CMOS processes leading to increased cost. On the other hand, SOI MESFETs can be constructed to withstand large voltages without any changes to the CMOS process. The access regions in a MESFET act much like the lateral drift region in the LD-MOSFET reducing the electric field at the gate. SOI MESFETS are

majority carrier devices and lack a gate oxide. This eliminates some of the breakdown mechanisms that are associated with MOSFETs such as electric field gate oxide breakdown and snapback [18]. The MESFET gate is also tolerant to current flow in both directions making it much more robust. The lack of a gate oxide improves the MESFETs ability to operate at higher temperatures which will be shown in the next two sections [19].

3.4.   *SOI MESFET DEVICE CHARACTERISTICS*

Due to the high breakdown voltage and temperature robustness of SOI MESFETs they were chosen for the SiC gate drive circuit described in chapter 4. The specific SOI MESFET chosen for the circuit application has a gate length of 0.6µm, a drain access length (Fig. 4) of 2.2µm, and a channel width of 100µm. The device was bonded into a high temperature package. A HP4155B Semiconductor Parameter Analyzer was used to measure the MESFET and obtain the graphs shown in Fig. 6 and Fig. 7. Fig. 6 shows the Gummel plot for the SOI MESFET. The gate current never exceeds approximately 10µA while the drain current increases into the mA range. The threshold voltage was extracted from this data using IC-CAP and was found to be -0.65 V [20]. Fig. 7 shows the family of curves plot for the MESFET at room temperature. The drain voltage was raised to 12V without showing indications of a soft breakdown, demonstrating the ability to withstand large blocking voltages. A breakdown voltage greater than 12V is relatively large compared to typical CMOS processes which generally have breakdown voltages less than 3.3V. The JFET gate drive circuit only requires the MESFET to handle a maximum drain voltage of 10V. The drain

current exceeded 2mA for a 0.5V gate voltage which is sufficient for driving the

JFET gate circuitry.

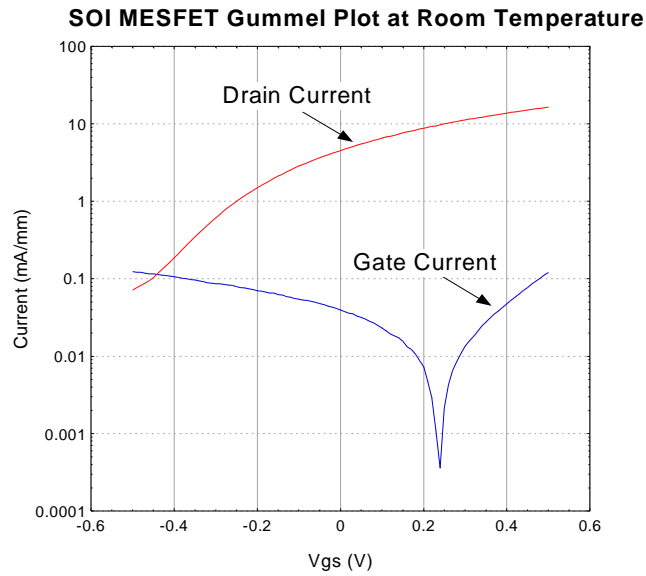**SOI MESFET Gummel Plot at Room Temperature**

Fig. 6: Gummel plot of the magnitude of the gate and drain current vs. gate-to-source voltage for a SOI MESFET at room temperature with the drain voltage held at 2V and the source voltage held at 0V.
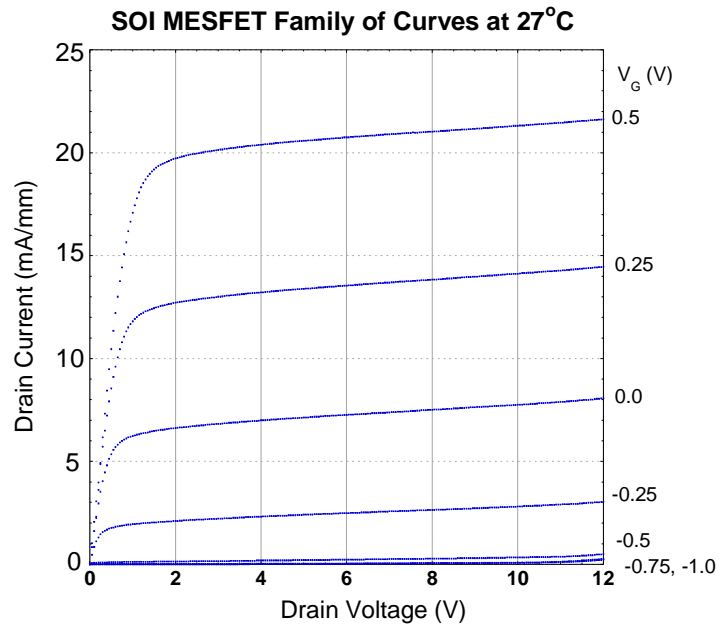
SOI MESFET Family of Curves at 27°C

Fig. 7: Family of curves for a SOI MESFET at room temperature.

If the MESFET is to properly drive a JFET device as well as other SiC devices, it needs to operate properly within the required temperature range. The SOI MESFET was measured over a range of temperatures to determine its robustness and temperature dependence. The packaged MESFET was placed in a convection oven and measured over a temperature range of 27°C to 250°C. Fig. 8 shows the family of curves for the MESFET at 250°C. Comparing Fig. 7 and Fig. 8, at 250°C the devices drain current has a larger slope. This indicates that the output resistance (R_O) of the device may decrease with increasing temperature. The drain current for $V_g = 0.5$ V never reaches 2 mA and is about 0.5 mA lower than the drain current ($V_g = 0.5$ V) at room temperature (Fig. 7).
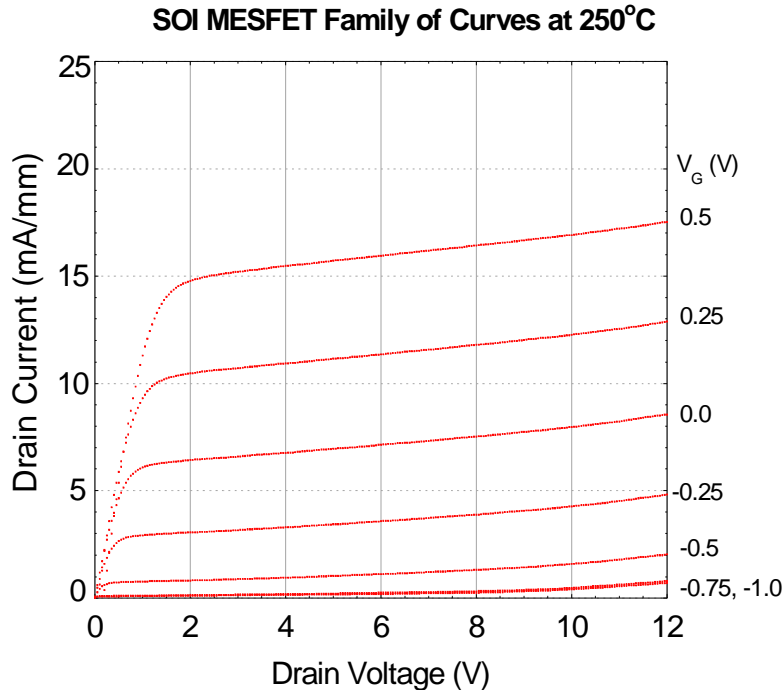
SOI MESFET Family of Curves at 250°C

Fig. 8: Family of Curves for an SOI MESFET measured at 250°C.

Fig. 9 displays the saturated drain current taken at V_{ds} = 4 V as it varies with temperature. The drain current increases for all the gate voltages and peaks around 150°C and then begins to decline with increased temperature. For V_g = 0.25 V and V_g = 0.5 V the drain current decreases below its value at room temperature. This means the MESFET cannot sink as much current at the highest temperatures when turned fully on due to an increase in parasitic source and drain resistances. However, the levels of drain current at these high temperatures are still adequate for switching the JFET. For V_g = -0.5 V at 250°C the drain current is larger than at room temperature. This causes the MESFET to not turn fully off requiring a larger negative voltage to be applied.

Fig. 10 is a graph of the gate current as a function of gate-to-source voltage with the drain and source both held at 0 V and the temperature raised from 100°C to 250°C. The graph illustrates how the gate current of the MESFET increases with rising temperature. For V_{gs} less than 0 V there is almost an order of magnitude increase from 100°C to 250°C. The increase in gate current for V_{gs} = 0.5V is smaller than the previous case. This indicates that the gate leakage current will not be as problematic when the device is switched on. Since the MESFET gate is a Schottky diode, increased leakage currents at higher temperatures are expected.
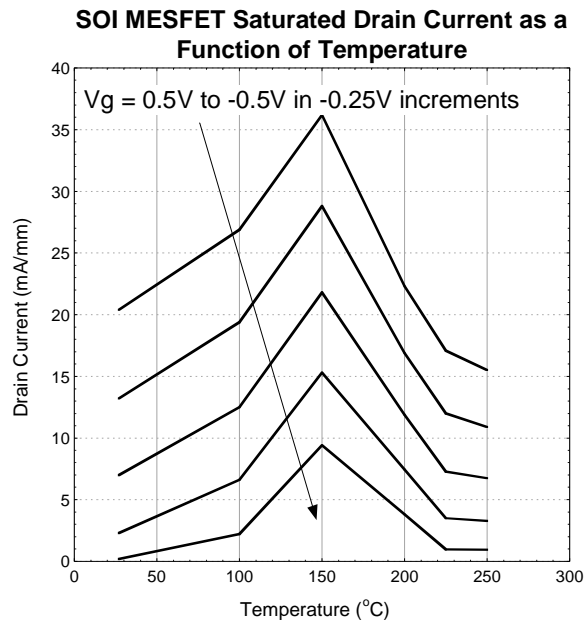
SOI MESFET Saturated Drain Current as a Function of Temperature

Vg = 0.5V to -0.5V in -0.25V increments

[Chart: Drain Current (mA/mm) vs Temperature (°C)]

Fig. 9: SOI MESFET drain current taken at V_{ds} = 4V for varying gate voltages over the temperature range of 27°C to 250°C.

Gate Current vs. Gate-to-Source Voltage

250°C

200°C

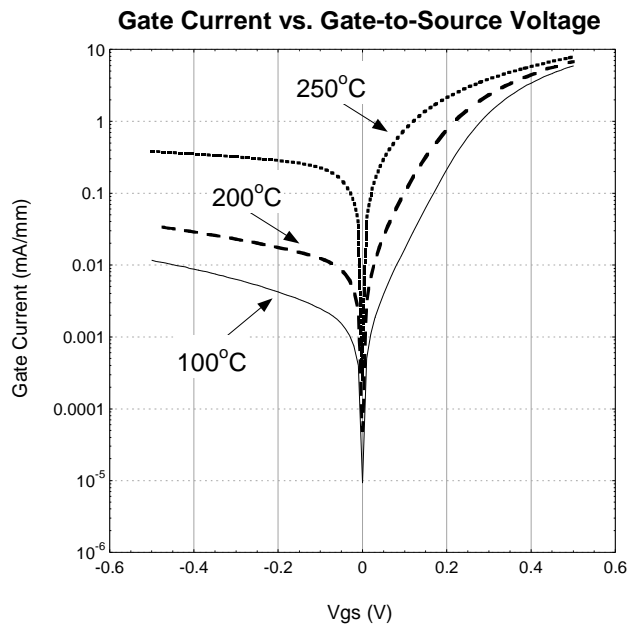100°C

[Chart: Gate Current (mA/mm) vs Vgs (V)]

Fig. 10: Gate current of the SOI MESFET measured as a function of gate-to-source voltage with the gate and the drain held at 0 V for a temperature range of 100°C to 250°C.

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3.6. CONCLUSIONS

As it has been shown in this chapter, SOI MESFETs are a realistic option for certain circuit applications. They allow for both MESFETs and MOSFETs to be combined on the same chip where before separate substrates had to be used to accomplish this. SOI MESFETs can be fabricated in many CMOS processes without the addition or change of any processing steps. The main requirement is that a silicide block step be present in the process. Multiple options for the silicide material were discussed and cobalt and nickel were shown to be the best options for forming the MESETs Schottky gate. The source and drain access regions of a MESFET have the inherent property of increasing the breakdown voltage of the device. This can be controlled during fabrication to create devices with very high breakdown voltages greater than 50V. The MESFETs lack of a gate oxide and majority carrier characteristics make it a robust device for extreme temperature environments. The room temperature and high temperature measurement results for the SOI MESFET device used in the SiC JFET gate drive circuit discussed in chapter 4 were displayed confirming the devices robustness.

CHAPTER 4

SiC GATE DRIVE CIRCUIT UTILIZING AN SOI MESFET

SiC, as previously discussed, has shown much promise for high temperature and high power applications. SiC junction field effect transistors (JFET) in particular are useful robust devices. They are the ideal choice for switching high current and high voltage loads in high temperature environments such as geothermal wells, satellites, space exploration and aerospace applications. The SiC JFET device requires a 0V to 10V pulse width modulated (PWM) signal to control the gate. The ideal source of the PWM signal is a CMOS microcontroller but due to the low breakdown voltages of CMOS discussed earlier it cannot provide a 0V to 10V signal. To make use of the CMOS microcontroller an intermediate buffer stage is required between the microcontroller and the SiC JFET. SOI MESFETs are an attractive solution due to their high temperature capabilities. By using a SOI MESFET the microcontroller and MESFET are integrated onto the same chip creating a single chip solution that is packaged with the SiC JFET. To demonstrate the feasibility of the solution this chapter shows the results of a SiC test circuit consisting of a 555 timer driving a SOI MESFET to switch a SemiSouth SiC JFET. First the device characteristics of the SiC JFET used in this experiment will be discussed followed by a description of the SiC JFET suggested gate drive circuit. In the next section the description of the SOI MESFET SiC gate drive circuit is provided and the room temperature and high temperature results are displayed. The last

section verifies the test results with circuit simulations using Agilent's Advanced Design System (ADS).

4.1. SIC JFET DEVICE CHARACTERISTICS

For the demonstration of a MESFET's ability to switch high temperature, high power devices, a SemiSouth SJEP120R125 enhancement mode SiC vertical JFET was chosen [21]. The JFET is a 1200V 15A device that is optimized for high voltage, high power, high frequency and high temperature applications [1]. A cross-section of the JFET is shown in Fig. 11. The device has a recessed gate which causes the JFET to be normally off. This is due to the width of the depletion region created by the implanted p-type gate which effectively pinches off the n-type channel. By applying positive charge to the gate the width of the depletion region is reduced allowing current to flow in the n-type channel. This means the JFET has a positive threshold voltage (approximately 1V) and does not require a negative bias on the gate for full blocking.
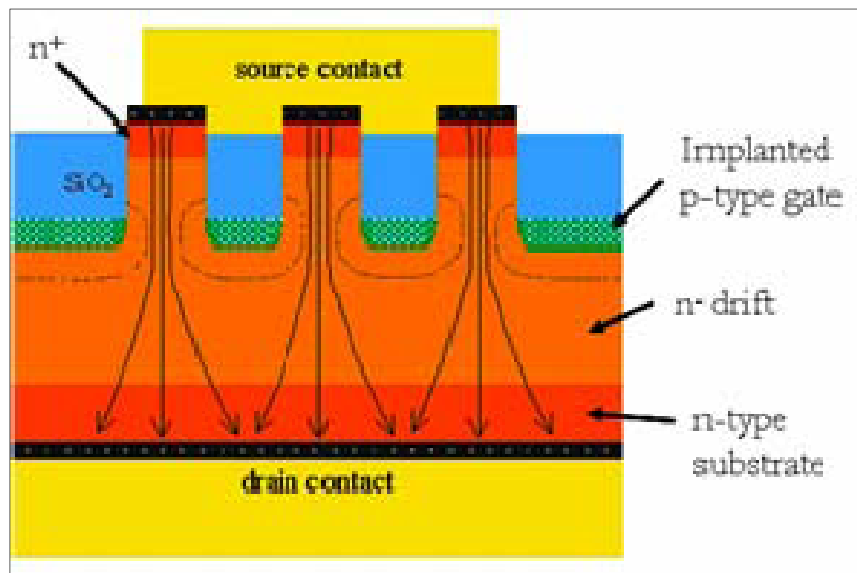

Fig. 11: Cross-section of a SemiSouth SJEP120R125 JFET [1].

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The SemiSouth vertical JFET structure is unique in that the channel is completely vertical between the recessed trench gate regions. This eliminates issues caused by lateral current flow in power transistor structures allowing for very high current densities to be achieved [22].
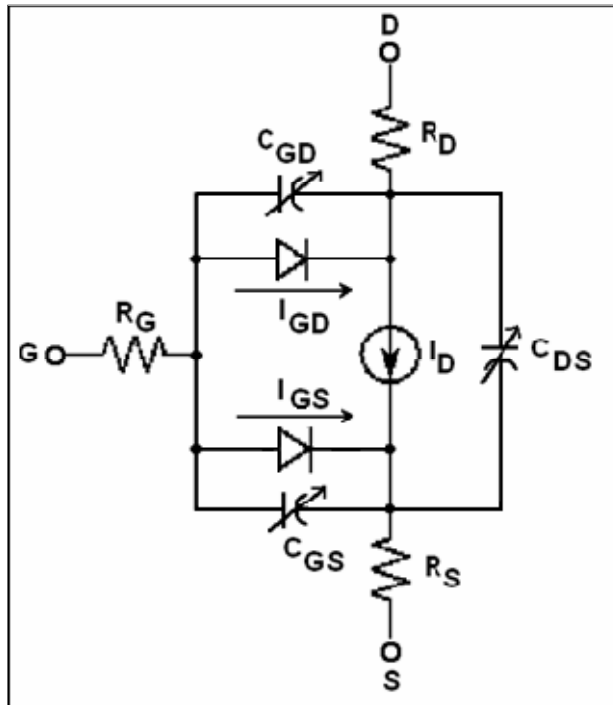

Fig. 12: Schematic model for the parasitics of the vertical JFET [1].

Fig. 12 shows the equivalent circuit for the parasitic impedances of the SiC JFET. There is no p-n junction between the drain and source so there is no intrinsic body diode. The gate-source junction is comprised of a p-n diode, like a BJT, and a variable capacitance, much like a MOSFET. There are two requirements for switching the JFET gate: dynamic charge to charge and discharge the gate capacitance and a steady state voltage and current for the gate-source diode. However the SiC JFET is not a current controlled device, the voltage difference between the gate voltage and threshold voltage controls the

channel width. Since the gate-to-source voltage is applied over a p-n diode a forward current is created, but it is significantly lower than the current required for a power BJT [1].

4.2. *SIC JFET GATE DRIVE CIRCUIT*

The gate drive circuit for the SiC JFET has to accomplish two things. First it has to be able to quickly deliver and remove the required charge for the gate-to-source capacitance and Miller capacitance. Secondly it needs to provide a steady state voltage and current to satisfy the forward bias gate-source diode and maintain a minimum drain-source on resistance ($R_{DS(ON)}$). To accomplish this SemiSouth recommends the AC coupled drive circuit shown in Fig. 13. The gate driver consists of an RC network between the JFET gate and the PWM signal generator. R_{CL} acts as a current limiting resistor. It sets the DC operating point in the on-state by dropping the potential difference between V_{CC} and the required gate-to-source voltage creating a gate current I_{GFWD}. The bypass capacitor C_{BP} provides the dynamic charge required by the gate. It also overdrives the gate during the turn off by causing the voltage to temporarily swing negative achieving a "hard" turn off. The resistor R in series with C_{BP} can be placed in the circuit to reduce ringing at the gate.
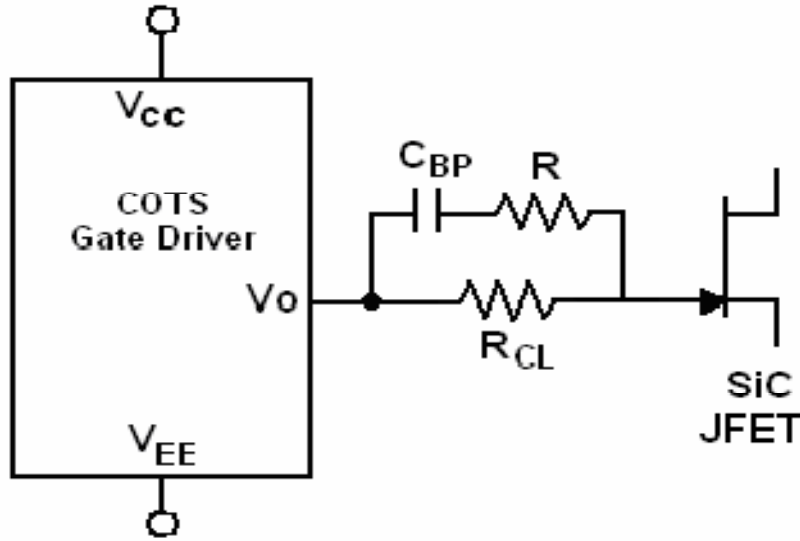
Fig. 13: AC coupled gate driver for the SemiSouth SJEP120R125 SiC JFET [22].

$$\frac{2*Q_g}{V_{CC} - V_{GS}} \leq C_{BP} \leq \frac{4*Q_g}{V_{CC} - V_{GS}}$$

(4.1)

$$R_{CL} = \frac{V_{CC} - V_{GS}}{I_{GFWD(@V_{GS})}}$$

(4.2)

where

Q_g = charge required by gate-to-source capacitance

V_{cc} = high voltage output of PWM gate drive circuit

V_{GS} = gate-to-source voltage

Equations (4.1) and (4.2) show the derived method for choosing the appropriate values of C_{BP} and R_{CL} [21]. Equation (4.1) is derived from the charge voltage relationship where Q_g is the charge required by the gate-to-source capacitance, V_{CC} is the positive high output of the PWM gate drive circuit, and V_{GS} is the desired gate-to-source voltage in the on state. A range is given because

the parasitic circuit effects differ for different circuit design choices. Equation (4.2) is simply Ohms Law. The value for I_{GFWD} can be found in the data sheet for the device from the I_G vs. V_{GS} graph.

This AC coupled gate drive circuit is driven by a PWM signal that has a 0V to 10V output, represented in Fig. 13. The ideal solution for a PWM signal generator is a CMOS microcontroller because of its functionality and small size. As stated previously, advanced CMOS processes are limited in supply voltage due to low breakdown voltages. Thus a buffer stage external to the CMOS microcontroller is needed to obtain the 0V to 10V signal. It will be shown that MESFETs can be used to replace the buffer stage because of their high breakdown voltages and wider operating temperature range. They can also be fabricated in an SOI CMOS process and integrated alongside the CMOS microcontroller.
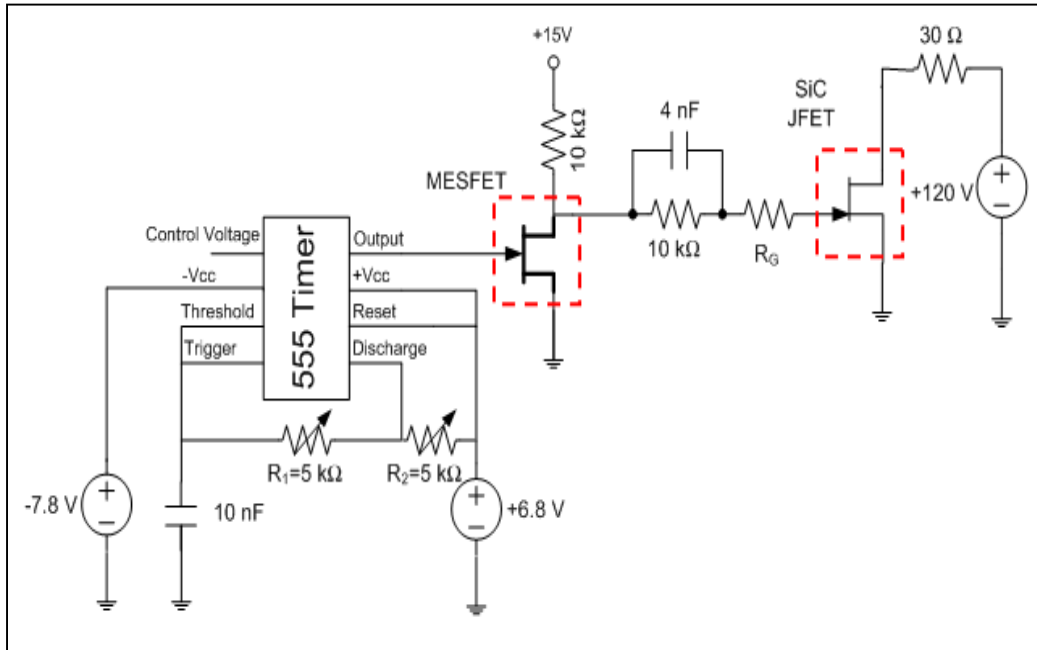
Fig. 14: Circuit Schematic for the PWM controlled SOI MESFET gate drive circuit for the SJEP120R125 SiC Power JFET. The MESFET and the JFET, indicated by the dashed boxes were placed in a convection oven separate from the rest of the circuitry.

To test the SiC JFET gate switching circuit the JFET and a packaged SOI MESFET were mounted on a copper block and placed inside a temperature controlled convection oven. Fig. 14 shows the circuit schematic of the switching circuit. The SiC Power JFET is connected to a half-wave rectified $120V_{RMS}$ AC signal through a 30Ω load to control the power flow. The AC coupled gate drive components presented previously (Fig. 13) are represented by the 4 nF capacitor and the 10 kΩ resistor in parallel. These values were chosen using equations (4.1) and (4.2). The MESFET was used to drive the AC coupled gate circuit in the range of 0 to 10 V. To drive the MESFET and thus the JFET a PWM signal needs to be applied to the gate of the MESFET. Out of convenience a 555 timer

was used to supply the PWM signal. The 555 timer has a limited output duty cycle range of 50% to 100%. This limited the achievable current drive range of the JFET. It is noted that the use of a microcontroller without a limited duty cycle would provide a wider current drive range for the JFET

The resistors and capacitors of the gate drive circuit and load circuit along with the 555 timer and its associated circuitry were not placed inside the temperature controlled convection oven since they were not rated for high temperature operation. Only the MESFET and JFET were placed inside the oven. The results of the experiment are still valid for demonstrating a MESFET driven SiC power JFET since all the parts that are not temperature rated can be implemented in a high temperature SOI process.

The 555 timer is controlled using an RC network represented in Figure 10 by R_1, R_2 and the 10nF capacitor. These elements control the frequency and duty cycle of the timer. Both resistors were variable resistors so the duty cycle could be adjusted to achieve multiple data points at the different temperatures. Since the duty cycle and frequency had to be adjusted together the frequency varied from 10 kHz to 15 kHz to achieve varied load currents. The voltage output of the 555 timer was 0.5 V high to -0.7 V low.
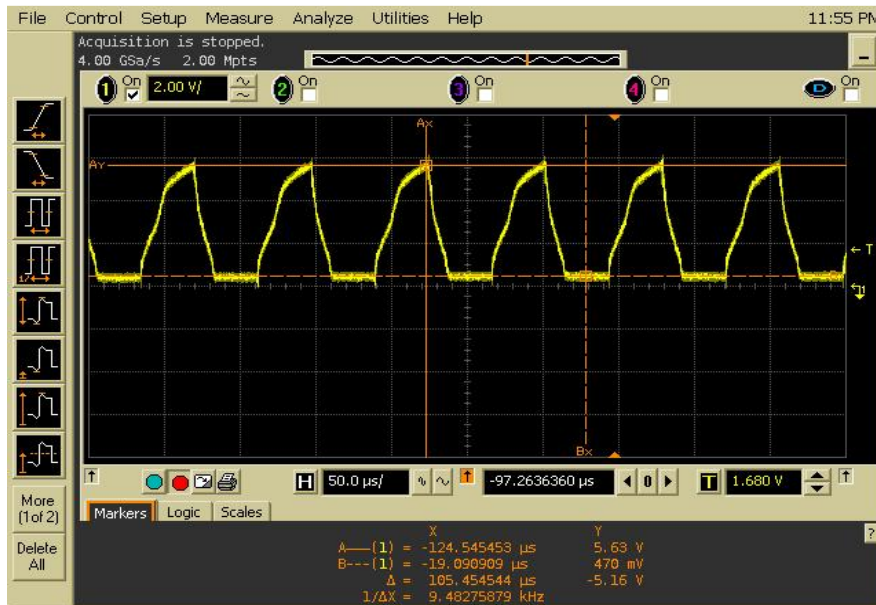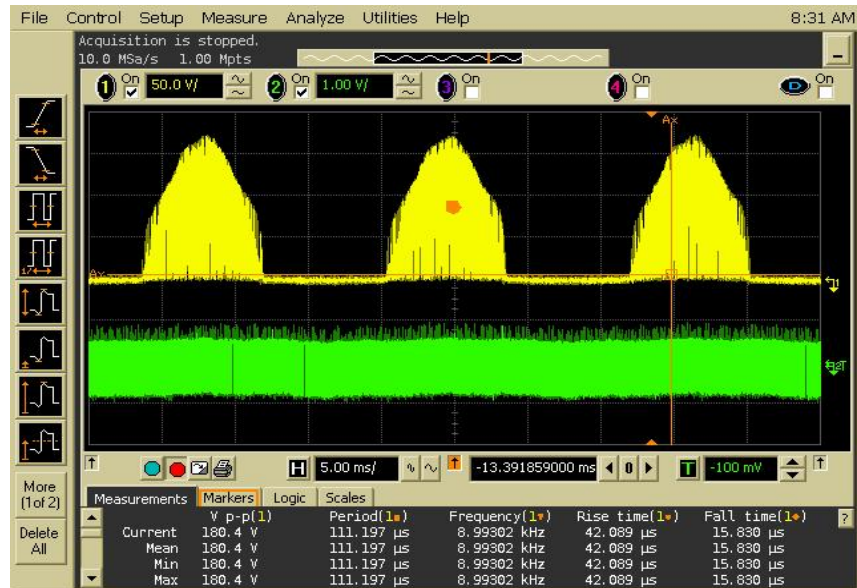
Fig. 15: Voltage waveform taken at room temperature at the MESFET drain for a 50% duty cycle signal supplied by the 555 at the gate. The voltage swings from 0 to 6 V.

The circuit voltages were measured using a digitizing oscilloscope and the temperature was increased from 27°C (room temperature) to 235°C. Data was taken for three different load currents at each temperature; 1.4A$_{RMS}$, 1.75A$_{RMS}$, and 2A$_{RMS}$. Fig. 15 shows the voltage waveform taken at the drain of the MESFET at room temperature for a 50% PWM 0.5V to -0.7V signal applied to its gate. The drain of the MESFET switches from 0 - 6V which is adequate for the desired load currents of the JFET. Fig. 16 shows room temperature voltage waveforms taken at the drain of the JFET. The duty cycle of the 555 timer was set to produce a 1.75A$_{RMS}$ load current. This shows the ability of the MESFET to provide good control of the JFET gate at room temperature. Fig. 17 further illustrates this showing the JFET switching with a load current of 1.4 A$_{RMS}$ and 2

A$_{RMS}$. The load current range (1.4 – 2 A) was limited by the duty cycle range of the 555 Timer.
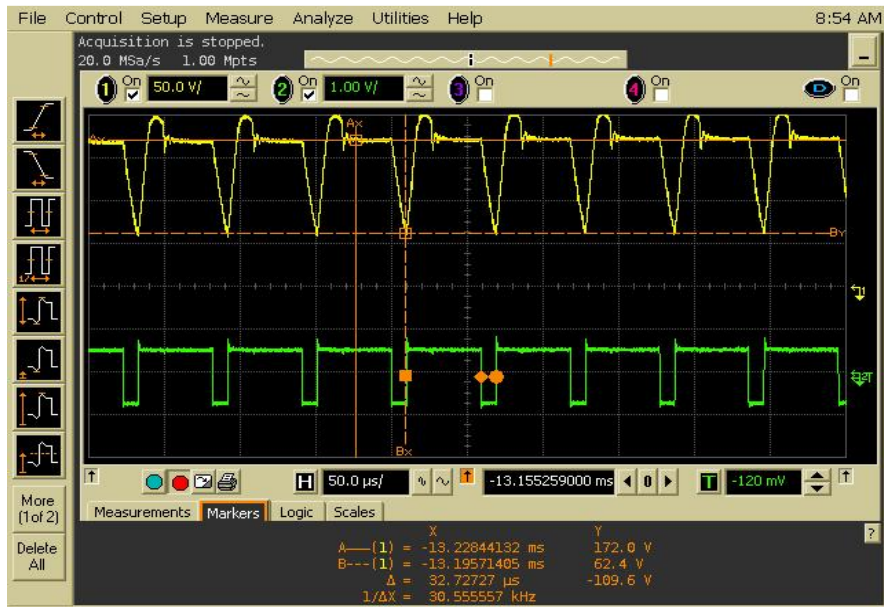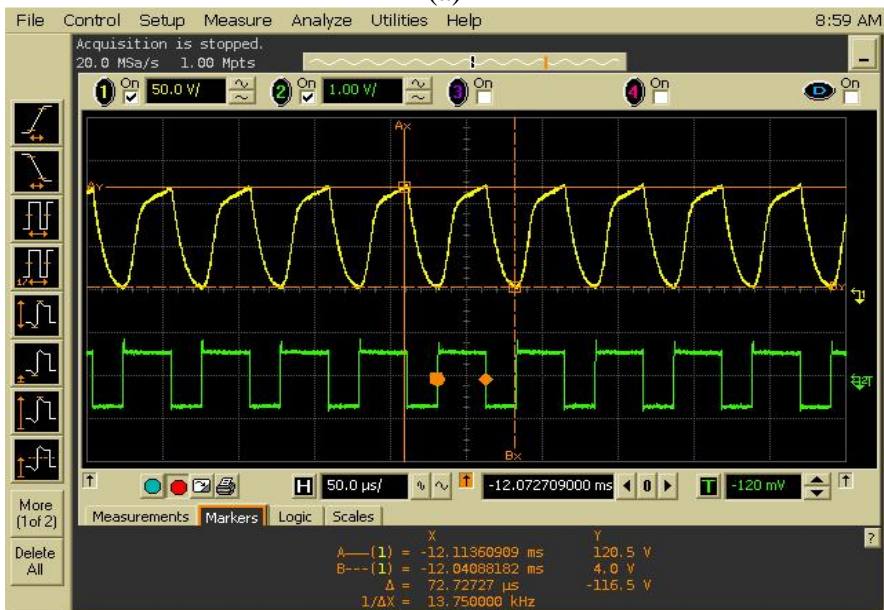

(a)

(b)

Fig. 16: Voltage waveforms at the drain of the JFET taken at room temperature for a 1.75 A$_{RMS}$ load current. Waveform (a) shows the PWM 60 Hz Half-wave rectified signal in yellow (50 V/div) and the 555 timer circuit PWM signal in green (1 V/div). Waveform (b) is the same waveform zoomed in to show the switching behavior of the JFET (0 – 170 V).

(a)

(b)

Fig. 17: Voltage waveforms captured at the drain of the JFET (yellow, 50V/div) and the gate of the MESFET (green, 1V/div) taken at room temperature. Waveform (a) has a load current of 1.4 A_{RMS} and (b) has a load current of 2 A_{RMS}.

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Voltage waveforms were captured at the MESFET gate and JFET drain at temperatures of 100°C, 175°C, and 235°C. The waveforms are presented in Fig. 18, Fig. 19, and Fig. 20. The duty cycle of the PWM signal was adjusted at each of the temperatures to produce an average load current of 1.75A$_{RMS}$. This demonstrates the MESFETs ability to provide good gate control of the JFET over a wide range of temperatures. It can be seen by comparing Fig. 19 and Fig. 20 that as the temperature increases it becomes increasingly harder to achieve the higher load currents. The duty cycle, of the JFET, in Fig. 19 is 28% (72% duty cycle at MESFET gate) and the duty cycle in Fig. 20 is 53% (47% duty cycle at MESFET gate). The frequencies are approximately equal but the duty cycle to achieve the same load current is almost double. This is due to an increased difficulty in switching on the JFET at higher temperatures.
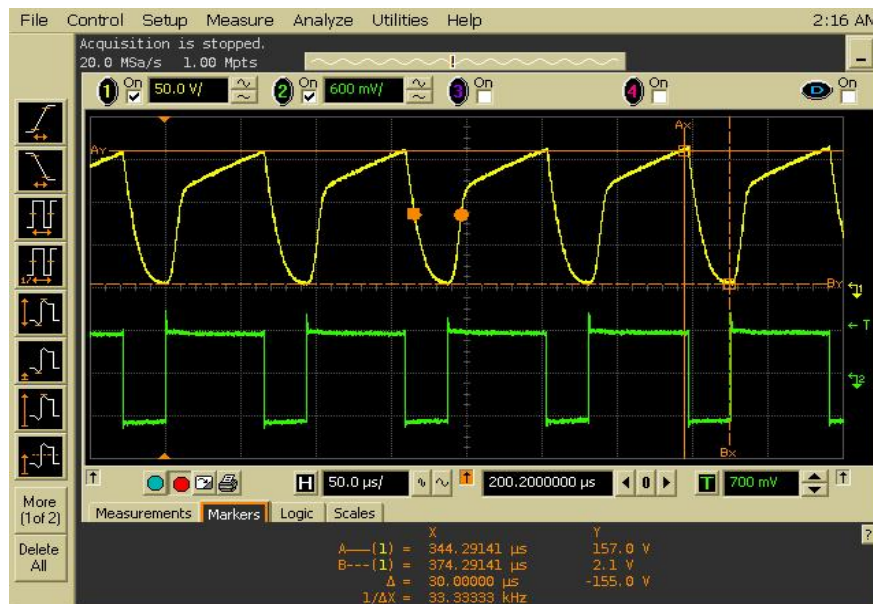

Fig. 18: Voltage Waveform for the JFET drain (yellow, 50V/div) and MESFET gate (green, 600mV/div) for a load current of 1.75 A$_{RMS}$ and a temperature of 100°C.

Fig. 19: Voltage Waveform for the JFET drain (yellow, 50V/div) and MESFET gate (green, 600mV/div) for a load current of 1.75 A$_{RMS}$ and a temperature of 175°C.
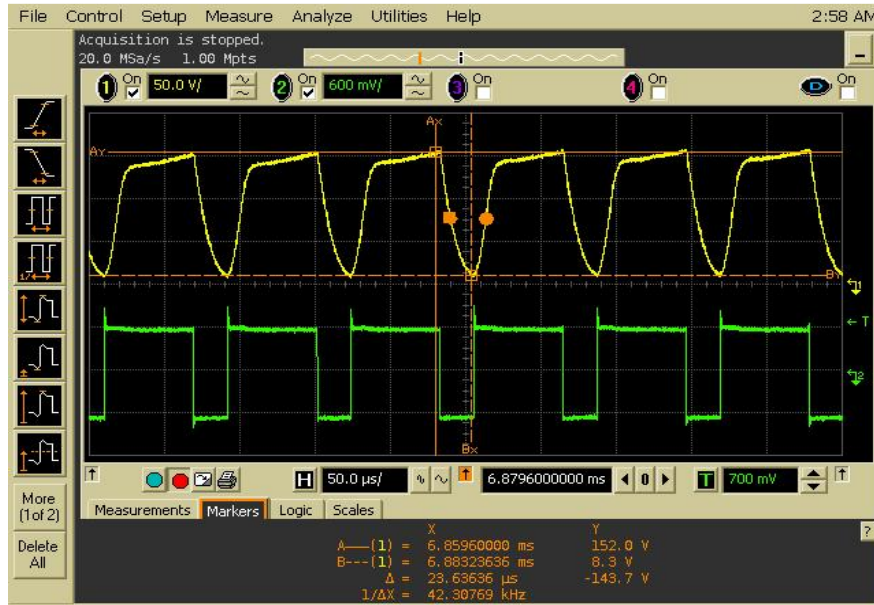

Fig. 20: Voltage Waveform for the JFET drain (yellow, 50V/div) and MESFET gate (green, 600mV/div) for a load current of 1.75 A$_{RMS}$ and a temperature of 235°C.

There are a couple reasons why it might be harder to turn on the JFET at higher temperatures. There could be an increase in parasitic resistances of the

JFET's source and drain contacts or the channel resistance, limiting the load current. To overcome this, the JFET could be turned on harder by raising the gate voltage or a JFET with a larger current drive could be used. Also, an increase in gate leakage current with increasing temperature would also limit the load current. Increasing the JFET's gate voltage should compensate for the increased leakage current. The MESFET also has larger leakage currents at high temperatures. This could also contribute to the difficulty of turning on the JFET.

Fig. 21 shows a graph of the measured load current as a function of the duty cycle for room temperature, 150°C, and 235°C. As described above, this illustrates the diminishing current drive of the JFET for increased temperatures. At 235°C the JFET can no longer sink a load current of $2A_{RMS}$ with the limited duty cycle range. The slight discrepancies in the graph are most likely due to the slight change in frequency between measurements to obtain the same load current. As mentioned previously, the 555 timer can be replaced with a high temperature microcontroller to produce a duty cycle range of 0 – 100%.
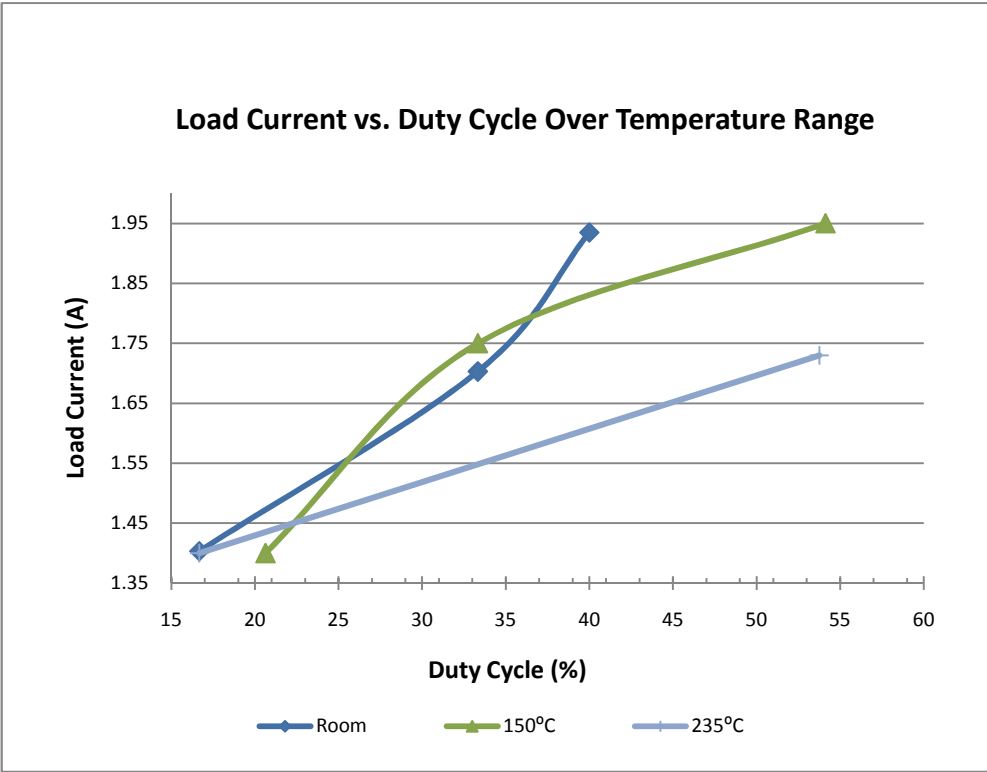
Fig. 21: A graph of the load current vs. duty cycle of the JFET measured at room temperature, 150°C, and 235°C.
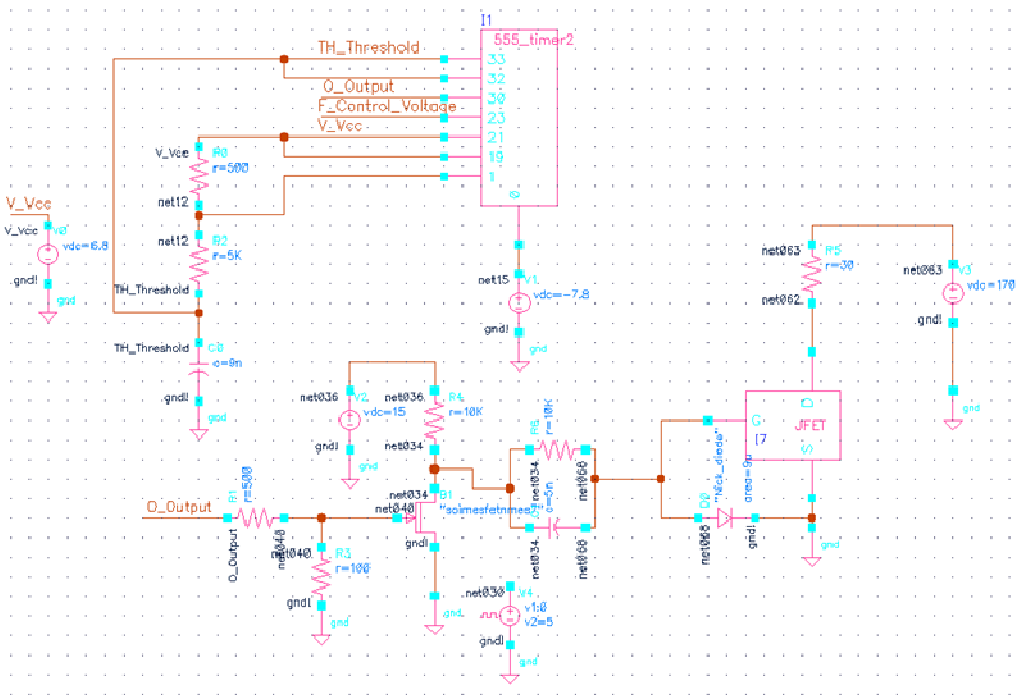
Fig. 22: Screen capture of the circuit schematic used in Advanced
Design Systems to simulate the SiC JFET gate switching circuit.

To model the room temperature data results presented in section 4.3 the

SiC JFET gate switching circuit was simulated using Advanced Design System

(ADS) software.   The ADS simulation used a generic 555 timer circuit, a

calibrated SOI MESFET model, and a level 2 JFET model. The SOI MESFET

model is a TOM3 model that was developed by previous students at ASU [23].

The Level 2 JFET model was a generic JFET model tuned to the specific

parameters of the SemiSouth JFET.   This was accomplished by matching the

family of curves plot and Gummel plot of the JFET models simulated results to

the SJEP120R125. The screen capture of the ADS circuit schematic is shown in

Fig. 22. The 555 timer switching frequency was set to 15 kHz with a 50% duty
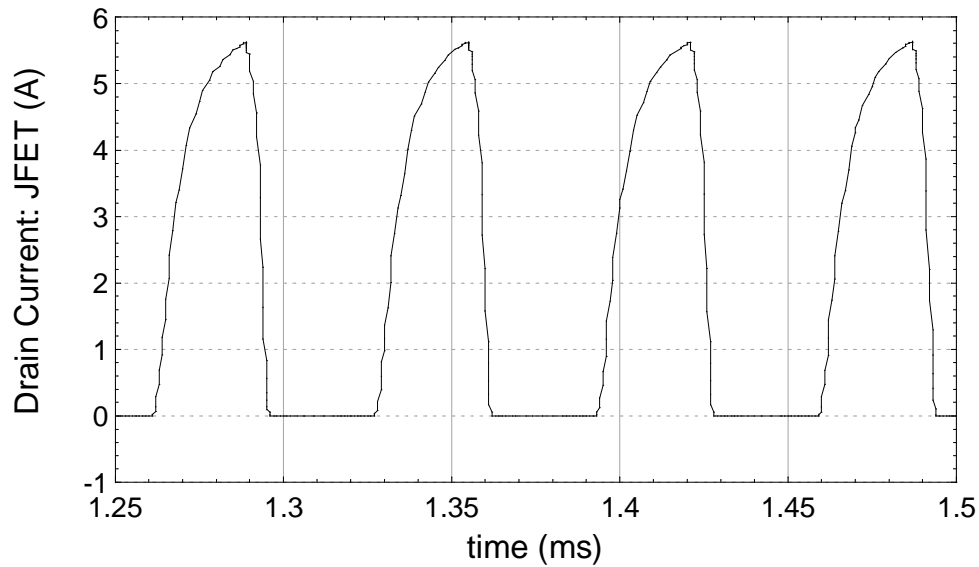
cycle. The JFET level 2 model was extracted at room temperature and is not a viable model for increased temperatures. This limits the simulations of the circuit to room temperature simulations only.

(a)

(b)
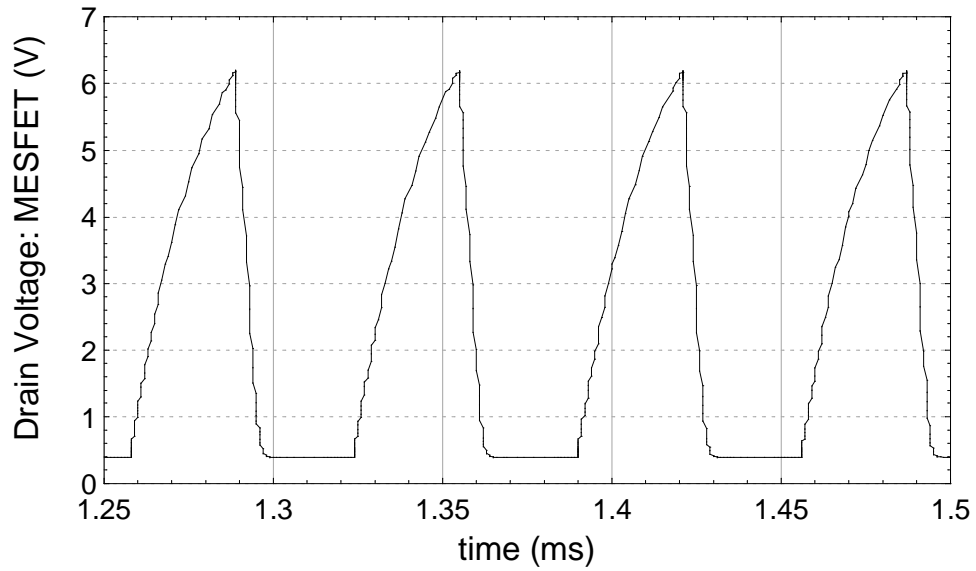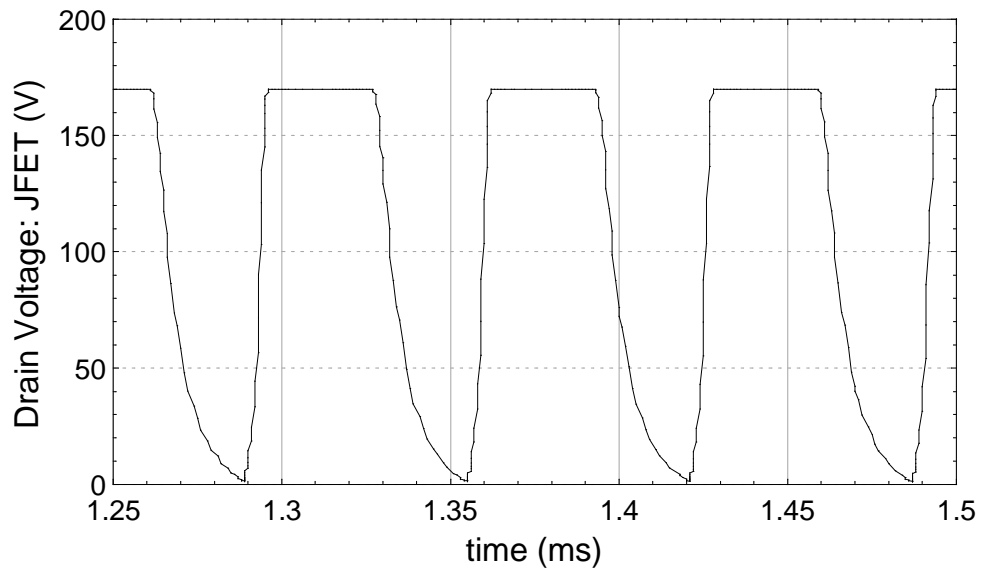
Fig. 23: Room temperature SiC JFET gate switching circuit simulation results from ADS. Graph (a) is the drain voltage of the MESFET, graph (b) is the drain voltage of the SiC JFET, and graph (c) is the instantaneous drain voltage of the JFET.

Simulation results from the circuit schematic shown in Fig. 22 are displayed in Fig. 23. The results displayed in Fig. 23 are for a duty cycle of 50%. The simulated results are very similar to the measured results displayed in section 4.3 with the MESFET drain voltage swinging from 0 – 6 V (Fig. 23a) and the SiC JFET drain voltage swinging from 0 – 170 V (Fig. 23b). The shape of the waveforms are very similar to the measured results. Comparing Fig. 23a to Fig. 15 and Fig. 23b to Fig. 16b confirms this. Reproducing the measured results with a simulated circuit model ensures that the data presented is well understood, and that the next phase of the SiC gate switching circuit can be designed optimally using simulated results before new devices are manufactured.

4.5. CONCLUSIONS

It has been shown that a SOI MESFET gate drive circuit can successfully control the switching of a SiC power JFET. This was demonstrated with the active components, MESFET and JFET, located in a temperature controlled convection oven with the temperature raised to 235°C. The current drive of the JFET was seen to decrease at higher temperatures. The SOI MESFET operated well under high temperatures up to 250°C and can be designed to withstand blocking voltages in excess of 60V making it a good solution for low-side driver circuits, especially in extreme temperature environments. The SiC gate drive circuit including the SOI MESFET was modeled in Agilent's ADS environment. The simulation results were consistent with the test results of the actual circuit presented.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

As it was shown in Chapter 2, there is an increasing demand for electronics to operate in high temperature environments. Of the silicon and wide bandgap technologies discussed, SiC and SOI technologies show the most promise. SiC was shown to operate well for high power applications and high temperature applications that exceed 300°C where SOI was shown to be ideal for low power applications below 300°C. The SOI MESFET was discussed thoroughly in Chapter 3. Its robust characteristics allow for operation at very high temperatures up to 250°C without damage to the device or a serious decrease in performance. Due to the access regions present in the device it is also capable of blocking high voltages. This coupled with the ease of integration into many CMOS processes make it an intriguing option for certain applications. These properties also give it an advantage over similar MOSFET solutions such as the LD-MOSFET.

Chapter 3 discussed one such application for SOI MESFETs. By using the SOI MESFET to drive the gate of the SiC JFET the JFET's gate drive circuitry can be significantly simplified into a single integrated component. SiC JFET switching circuits are used in numerous extreme environment applications including well drilling. The test results show that the SiC gate drive circuitry with the SOI MESFET operated well up to temperatures of 235°C. There were some issues discovered from the test results. It was observed that the JFET drain current diminished with increasing temperature. The JFET drain current range

was ultimately limited by the available duty cycle range of the gate drive circuitry which in turn was limited by the use of the 555 timer.

Improving upon the SOI MESFET used for the SiC gate drive circuit would improve the overall circuit operation. The SOI MESFET used in the circuit had a drive current of a little over 1mA which limited the switching frequency of the gate. This low drive current caused a slow discharge of the bypass capacitor in the gate drive circuit. The effects of this are shown in Fig. 15. By designing the SOI MESFET to handle a much higher drain current the MESFET would be able to pull its drain voltage to zero over a much shorter time period. Fig. 15 also shows that the charging of the bypass capacitor when the MESFET is turned off also takes a long period of time. This was limited by the 10kΩ load resistor shown in Fig. 14. The resistor size was limited by the low drive current of the SOI MESFET and could not be sized any smaller. By increasing the drive current of the MESFET for future tests the load resistor value could be decreased resulting in a quicker charging of the bypass capacitor. These improvements would not only allow for higher switching frequencies at the gate of the SiC JFET but also a smoother switching waveform at the drain of the MESFET. This in turn would cause the JFET to switch its load in a smoother fashion.

5.1. FUTURE WORK

For future implementation and testing of the SiC gate drive circuit the improved SOI MESFET needs to be integrated with a SOI CMOS microcontroller. The use of a CMOS microcontroller would allow for greater

control of the gate drive circuit. The duty cycle range of the 555 timer was limited to between 50% and 100%. A CMOS microcontroller would be able to produce waveforms with a full range of duty cycles, 0% to 100%, allowing for greater control of the SiC JFET drain current. Also, by integrating the appropriately sized SOI MESFET with the CMOS microcontroller, proper demonstration of a single on-chip solution could be shown. Lastly, a better understanding of temperature effects on the SiC JFETs performance can lead to a solution for the diminished current of the JFET at high temperatures.

5.2. CONCLUSION

This thesis has shown the viability of using SOI MESFETs for high temperature applications especially where higher voltages are required. This was successfully demonstrated in the SiC JFET gate drive circuit. SOI MESFETs easy integration with CMOS can allow for simplified solutions for the gate control of power transistors. With further research and development of MESFETs in SOI technologies being conducted at ASU, the commercial viability for these circuit applications will only increase.

REFERENCES

[1] "Silicon carbide enhancement-mode junction field effect transistor and recommendations for use," ed. SemiSouth Labs: Application Note AN-SS1, pp. 1-9.

[2] R. Johnson*, et al.*, "The changing automotive environment: high-temperature electronics," *IEEE Transactions on Electronics Packaging Manufacturing,* vol. 27, pp. 164-173, July 2004.

[3] P. G. Neudeck, "High-temperature electronics - a role for wide bandgap semiconductors?," *Proceedings of the IEEE,* vol. 90, pp. 1065-1075, June 2002 2002.

[4] B. Draper and D. Palmer, "Extension of high temperature electronics," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology,* vol. CHMT-2, pp. 399-404, December 1979.

[5] D. A. Neamen, *Semiconductor physics and devicers, basic principles*, 3rd ed. New York: McGraw-Hill, 2003.

[6] P. L. Dreike, "An overview of high-temperature electronic device technologies and potential applications," *IEEE transactions on components, packaging, and manufacturing technology,* vol. 17, December 1994.

[7] P. Chalker, "Wide bandgap semiconductor materials for high temperature electronics," *Thin Solid Films,* pp. 616-622, 1999.

[8] A. Elasser, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE,* vol. 90, pp. 969-984, June 2002.

[9] J. A. Cooper and A. Argarwal, "SiC power switching devices - the second electronics revolution," *Proceedings of the IEEE,* vol. 90, pp. 956-967, June 2002.

[10] J. B. Casady, "Status of silicon carbide (SiC) as a wide bandgap semiconductor for high temperature applications: a review," *Solid State Electronics,* vol. 39, pp. 1409-1422, 1996.

[11] R. Singh, "Reliability and performance limitations in SiC power devices," *Microelectronics and Reliability,* vol. 5, pp. 713-730, June 2006.

[12]   J. Zolper, "A review of junction field effect transistors for high temperature and high power electronics," *Solid-State Electronics,* vol. 42, pp. 2153-2156, 1998.

[13]   J. Ervin, "Fabrication and characterization of SOI MESFETs," Ph.D Thesis, Arizona State University-Tempe, 2007.

[14]   J. Yang*, et al.*, "Silicon-based integrated MOSFETs and MESFETs: a new paradigm for low power, mixed signal, monolithic systems using commercially available SOI," *Int. J. of High Speed Electronics and Systems,* vol. 16, pp. 723-732, 2006.

[15]   W. Lepkowski, "Optimizing the design of partially and fully depleted MESFETs for low dropout regulators," Ph.D Thesis, Arizona State University, Tempe, 2010.

[16]   J. Ervin*, et al.*, "CMOS-compatible SOI MESFETs with high breakdown voltage," *IEEE Transactions on Electron Devices,* vol. 53, pp. 3129-3135, 2006.

[17]   W. Lepkowski*, et al.*, "Scaling SOI MESFETs to 150 nm CMOS technologies," *submitted to IEEE Transactions on Electron Devices,* 2010.

[18]   J. Vanderstand*, et al.*, "CMOS compatible SOI MESFETs for extreme environment applications," *IEEE Transactions on Electronic Devices,* vol. 53, pp. 3129-3135, December 2006.

[19]   A. Balijepalli*, et al.*, "Compact modeling of a PD SOI MESFET for wide temperature designs," *Microelectronics Journal,* vol. 40, pp. 1264-1273, 2009.

[20]   (2000, May, 2009). *Agilent Technologies*. Available: http://www.home.agilent.com/agilent/home.jspx?cc=US&lc=eng

[21]   Datasheet, "SJEP120R125," ed: SemiSouth Labs.

[22]   "Optimized gate driver for enhancement-mode SiC JFET," ed. SemiSouth Labs: Application Note, pp. 1-6.

[23]   A. Balijepalli*, et al.*, "High-voltage CMOS compatible SOI MESFET characterization and SPICE model extraction," in *Microwave Symposium Digest, 2006. IEEE MTT-S International*, 2006, pp. 1335-1338.