

Total Dose Effects and Hardening-by-Design Methodologies
for Implantable Medical Devices

by

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ABSTRACT

Implantable medical device technology is commonly used by doctors for disease management, aiding to improve patient quality of life. However, it is possible for these devices to be exposed to ionizing radiation during various medical therapeutic and diagnostic activities while implanted. This commands that these devices remain fully operational during, and long after, radiation exposure. Many implantable medical devices employ standard commercial complementary metal-oxide-semiconductor (CMOS) processes for integrated circuit (IC) development, which have been shown to degrade with radiation exposure. This necessitates that device manufacturers study the effects of ionizing radiation on their products, and work to mitigate those effects to maintain a high standard of reliability. Mitigation can be completed through targeted radiation hardening by design (RHBD) techniques as not to infringe on the device operational specifications.

This thesis details a complete radiation analysis methodology that can be implemented to examine the effects of ionizing radiation on an IC as part of RHBD efforts. The methodology is put into practice to determine the failure mechanism in a charge pump circuit, common in many of today's implantable pacemaker designs, as a case study. Charge pump irradiation data shows a reduction of circuit output voltage with applied dose. Through testing of individual test devices, the response is identified as parasitic inter-device leakage caused by trapped oxide charge buildup in the isolation oxides. A library of compact models is generated to represent isolation oxide parasitics based on test

structure data along with 2-Dimensional structure simulation results. The original charge pump schematic is then back-annotated with transistors representative of the parasitic. Inclusion of the parasitic devices in schematic allows for simulation of the entire circuit, accounting for possible parasitic devices activated by radiation exposure. By selecting a compact model for the parasitics generated at a specific dose, the complete circuit response is then simulated at the defined dose. The reduction of circuit output voltage with dose is then re-created in a radiation-enabled simulation validating the analysis methodology.

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CHAPTER 1 INTRODUCTION TO IMPLANTABLE MEDICAL DEVICES

1.1 Historical Perspective

In the last 60 years, the world has seen development of implantable medical devices that serve to improve patient quality of life. This has led to the development of a multi-billion dollar industry. Through collaboration between medical professionals and engineers, implantable device technology has evolved into complex systems capable of such activities as patient monitoring, drug delivery, neurological stimulation and support of heart function through artificial pacing and defibrillation [1]. These devices currently serve to treat a wide array of diseases, and continued breakthroughs in the medical and engineering fields will expand their usage going forward [2-4].

The origin of the implantable medical device industry was the development of the artificial pacemaker, which is used to treat heart arrhythmia through electrical stimulation. Early research of the effects of electricity on the human heart began in the late eighteenth and early nineteenth centuries as scientists attempted to observe the effects of electrical stimulation on recently deceased combatants of the French Revolution. Although crude, these tests did reveal that electricity could produce muscle contraction, including in the heart. Such results lead researchers into exploring electricity as a treatment for cardiac-related problems through localized stimulation and through full body electrification, which yielded poor clinical results [5]. Considered the first pacemaker, Hyman's external electro-mechanical pacemaker was invented in 1932. The device delivered an induction shock by way of a hand-wound, spring-driven generator

that was capable of providing six minutes of pacing between windings [6]. Pacing stimulation was delivered via a needle injected into the right atrium of the heart. The device was capable of producing a pulsed current at 30, 60 or 120 beats per minute. The device was first tested on animals, then later humans but was quickly abandoned amid controversy. In 1952 Zoll succeeded in pacing the heart of a patient who had suffered cardiac arrest. This was done with two external electrodes on the chest surface connected to an external pacemaker [7]. 1958 saw many developments, first, Fruman successfully introduced an electrode into the right ventricle of a patient's heart and was effective in pacing the heart for 96 days [8]. Secondly, Lillegel and Bakken created a transistor-based, battery-powered, external pacemaker for which was put in use successfully for 18 patients [9].

The foundation for modern pacemakers was established in October 8th, 1958 in Sweden with the advent of the first fully implantable pacemaker. The device was designed by Rune Elmqvist and implanted by surgeon Åke Senning. The device used a nickel-cadmium battery that required frequent transcutaneous (through unbroken skin) recharging [10]. This first device only lasted 3 hours, and was replaced by a second device on October 9th, 1958 which subsequently failed. Throughout the rest of the first patient's lifetime he received another 21 pacemaker implantations [11].

The first fully implantable pacemaker in the United States was designed by engineer Wilson Greatbatch and cardiologist W.M. Chardack, developed in 1959. The device, designed to deliver single-chamber ventricular pacing, measured 6 cm

in diameter and was 1.5 cm thick and weighed in at 180 grams. The circuit generated 10 mA current pulses, 1-ms wide, at a rate of 60 beats per minute. The pacemaker drained an average standby current $12\mu\text{A}$ from the mercury-zinc battery. This gave the implantable pacemaker an estimated battery life of 5 years, but was almost always replaced after 1 year [9], [12]. On June 6th, 1960 Chardack completed the first successful application of this pacemaker design when he implanted their device into a 77 year old man at Millard Fillmore Hospital in Buffalo, New York [13]. This new design showed significant improvement in durability and battery life from the Elmqvist-Senning pacemaker and allowed for widespread clinical usage of this new treatment [10].

With the acceptance of the implantable pacemaker as a viable heart therapy option, more research and development lead to numerous advancements to the device technology in the subsequent decades. In the 1970's pacemakers advanced to become smaller in size by moving away from discrete components. Additionally designs began to include circuitry protection and the introduction of hermetic sealing technology prevented device contamination. A major progression in device development was the switch from bipolar to complementary metal oxide semiconductor (CMOS) technology during the 1980's. This enabled design of circuits with a much lower current drain.

The present day advancement and shrinking of CMOS technology has allowed for the expansion of pacemaker functionality, as circuits could be designed with more features without sacrificing overall device size. Further advancements included the addition of telemetry through skin, allowing doctors to

program pacemakers remotely and adjust pacing as needed. Additionally, increases in circuit sophistication allowed pacemakers to sense the patient's activity level and adjust pacing accordingly [9]. Current designs are expected to last more than 10 years before needing to be replaced. Future work in the field serves to increase the pacemaker feature set, boost battery life and improve reliability. Currently the effects of electromagnetic interference (EMI) and radiation exposure on pacemakers are issues of concern for medical professionals and engineers [14-24].

As of 2006, around 40% of all human deaths are related to cardiovascular diseases. However, contemporary pacemakers have evolved in complexity from early devices, and continue to play a crucial role in treatment, with more than 250,000 pacemakers implanted every year [12].

1.2 Key Electronic Design Considerations for Medical Devices

All electronics designed for medical devices are constructed with the primary goal of increased battery life through ultra-low power consumption while maintaining a high standard of reliability. In fact, reliability and device lifetime are the primary product differentiation factors [4]. Today, the U.S. Food and Drug Administration (FDA) regulate medical devices to ensure quality and protect patients. Field failures of implanted devices are unacceptable, as a fault could require device replacement involving surgery or, in extreme cases, put the patient's life in danger. Great care is taken in the front-end design and qualification process to ensure a reliable product.

Since the medical device market is rather low volume in comparison to the commercial electronics industry, medical device companies have employed a “fast follower” approach by leveraging new integrated circuit (IC) processes only after they have been developed by higher volume industries such as consumer electronics. This approach allows for medical device companies to have a better understanding of product reliability and reduce development times. Ultimately, the market would like to draw investment from commercial foundries and fabless companies to provide solutions specifically designed for medical devices; however this has yet to come to fruition.

IC designs are primarily fabricated in silicon based CMOS processes due to the low standby power consumption and high device reliability. The continued tracking of CMOS technology with Moore’s Law has allowed designs to increase the complexity of systems without gains in power consumption or device size. Additionally the integration of multiple functional blocks into a single system-on-a-chip (SOC) serves to further limit current draw in comparison to older designs, which relied on inter-chip communication in the system requiring more power. As device feature size shrinks at each successive technology node, overall maximum supply voltage shrinks as well. However, with decreased supply voltage, the device threshold voltage is also lowered. This is undesirable as reduction in threshold voltage leads to increased off-state leakage. So selection of the CMOS process must balance the benefits of shrinking feature size with the requirements of ultra-low power consumption.

Another undesired aspect for the medical device industry in relation to shrinking geometries is the reduction in standard gate oxide thickness. Most if not all pacemaker designs require the use of large output voltage (5-10V) for pacing, for which the newest technology nodes' ultra-thin gate oxides cannot reliably support. To solve this issue many companies employ technologies that provide devices of different gate oxide thicknesses within the standard process. This allows circuit designers the option to use transistors with thicker oxides for use in high voltage output sub-circuits while still having the opportunity to employ thin gate oxide transistors in lower voltage digital sub-circuits. The requirement of thicker oxides and high circuit voltages is deleterious when considering susceptibility to ionizing radiation, as will be shown and discussed throughout this thesis.

A key design consideration to be considered in technology selection is transistor matching. The scaling to smaller geometry processes has improved matching but again must be balanced with the drawback of reduced threshold voltages and the resulting increase in off-state current. To accomplish this, medical device companies employ the newer processes but require foundries to implement threshold-adjust implants to increase device threshold voltages and improve matching.

A typical pacemaker device uses a non-rechargeable battery as the system's sole power source. Battery supply voltage is usually targeted near 3V with design considerations made to accommodate an end-of-life battery voltage reduced as low as 1.7V. To maximize battery life, all systems operate at currents as low as

10 μ A and a leakage for off-state transistors targeted to be less than 1pA per micrometer of gate width. This is a difficult task as system designs often include a microcontroller IC, on-chip read only memory (ROM) with static random access memory (SRAM), a mixed-signal IC for biological sensing and generating output signals, a protection IC to shield against interference, a large SRAM for storage of diagnostic data and possibly very-high voltage electronics for generation of defibrillation signals [25]. As an example, a cardiac pacemaker system showing the device's connection to the heart, and a top level block diagram of a sample pacemaker circuit are shown in Fig. 1.1 and Fig. 1.2 respectively. This diagram can be divided into four areas of operation [26].

1. Input – Biological sensing circuits consisting of amplifiers and filters, physiologic sensor and the telemetry circuit.
2. Output – High voltage multiplier circuit and the high voltage output generator.
3. Circuit Control – Battery management, bias and reference generators.
4. Logic – Memory for diagnostic information storage and programmable logic for therapy controls and oscillators.

With consideration to the inflexible battery lifetime requirements, the most critical sub-blocks are the circuit control and output sub-blocks, as there efficiency most affects the battery drain of the circuit. Of specific interest is the high voltage multiplier circuit, which is responsible for DC-DC voltage multiplication to achieve voltages greater than available directly from the battery.

This circuit is often implemented through a highly efficient charge pump topology. As will be discussed in the next section, these circuits are also of critical concern when considering ionizing radiation tolerance of the complete system.

1.3 Reliability Concerns Related to Radiation Exposure

The main figure of merit for implantable medical devices, specifically pacemakers, is the device's expected lifetime and reliability. Many of the reliability concerns of implantable device designers are not exclusive to the medical device field. These include the deleterious device effects of gate-induced drain leakage (GIDL), stress-induced leakage current (SILC), negative-bias temperature instability (NBTI) as well as other material and packaging related reliability concerns [4, 25, 27, 28]. However, many of these concerns are well monitored and are of utmost consideration during the front-end design process. Additionally, all devices undergo stringent qualification and "burn-in" testing to check for defects before reaching doctors and surgeons for use in patients.

However one area of medical device reliability that has not been significantly explored by device engineers is the effects of radiation on implanted devices. Exposure of implanted devices to ionizing radiation is possible during diagnostic x-rays or through the use of radiation therapy for cancer treatment. Traditionally, the effects of ionizing radiation in semiconductor devices and integrated circuits were of concern for engineers designing for space and nuclear applications only. However, as implantable devices continue to grow in usage, there is a need to address radiation effects in these devices in more depth.

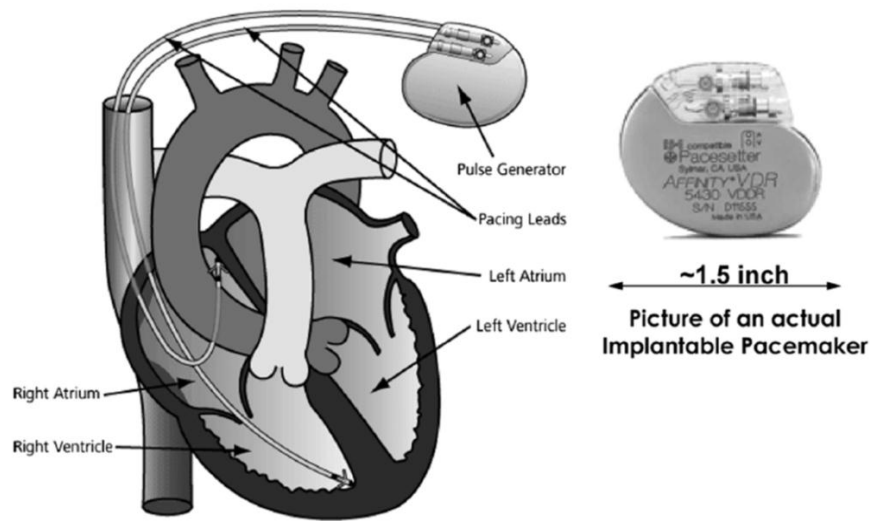


Fig. 1.1 Depiction of the pacemaker's connection to the human heart and a picture of a pacemaker showing device scale [26].

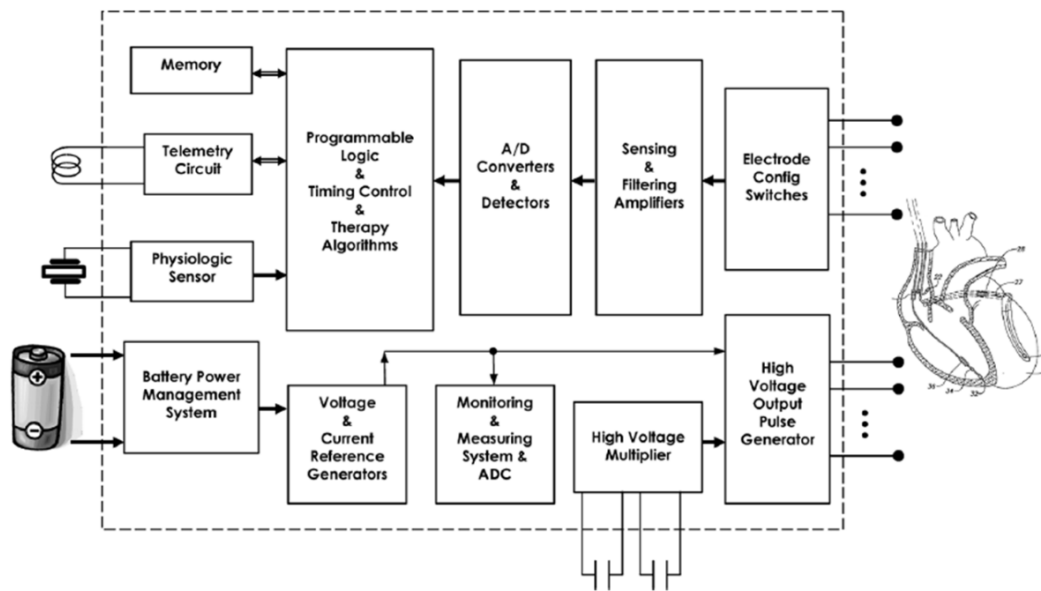


Fig. 1.2 Example block diagram of the pacemaker circuit [26].

Currently, some pacemaker device manufacturers list relatively low thresholds (1-5 Gy) for acceptable device exposure levels, with some manufacturers stating that no level of exposure is acceptable [23]. Therapeutic dose for tumor treatment can range from 10 to 70 Gy, although it is assumed that the pacemaker device will see only a fraction of the total dose, thus should maintain full functionality [20]. However, it is considered “best practice” to avoid directly exposing the device to radiation during cancer therapy, with many recommendations going as far to say that patients with implantable medical devices need to have their pacemakers relocated or that the plan of cancer therapy should be re-evaluated to avoid radiation exposure [17-19]. Numerous clinical studies which test commercial pacemaker devices for their radiation tolerance report mixed results [15, 21, 23, 24].

One specific case study of interest details a 64-year old woman with an implantable pacemaker who was diagnosed with breast cancer [17]. The case presented is particularly challenging due to the location of the cancerous tumor in proximity to the pacemaker. The study reports that the pacemaker received an estimated total dose of 4.3 Gy during cancer therapy, and reported normal operation of the device following treatment. The study concluded that the use of radiation therapy for patients with implantable devices is safe, but only if extreme caution is taken. Additionally recommendations are made to a) consider other treatment options, b) surgically relocated the device, c) attempt to exclude the pacemaker from the radiotherapy portal and d) attempt to calculate dose to the

pacemaker. The study concludes by recommending that device manufactures to make radiation tolerance data for their devices more readily available.

The drawback of these types of clinical studies is that they all approach the problem from a medical perspective. The studies focus on a “pass/fail” methodology for device performance post-irradiation, only monitoring external electrical signals as would be seen by the heart. As such, they do not explore radiation effects on internal circuitry to analyze the true effect of ionizing radiation and consider if latent reliability issues exist, or if the expected device lifetime has been significantly reduced. If design specifications such as current draw are affected and exceed specification after exposure, battery life would be reduced and surgical replacement of the pacemaker could potentially be needed years earlier than originally predicted.

As the medical technology, surgical techniques and device designs advance the likelihood that implanted devices will see increased exposure levels during therapy could increase. This necessitates preemptive steps be taken to improve device radiation tolerance. The primary reason ionizing radiation effects warrant serious consideration in implantable electronics is the nature of device designs, specifically:

- Medical devices must utilize technologies with thicker dielectrics and lower doping levels. It is well known that these properties make high voltage MOS technologies more susceptible to ionizing radiation [29].

- Higher voltage requirements of pacemaker sub-blocks such as voltage multiplication circuitry and high voltage output generators result in larger electric fields throughout the circuit, particularly in the device oxides, which will enhance radiation-induced defect buildup [30, 31].
- Ionizing radiation is known to cause increases in off-state currents, reduce threshold voltage in n-channel devices and cause parasitic inter-device leakage [29], all of which are damaging to the low-power consumption design goals.
- Tolerance of field failures of implantable devices is unacceptable and the consequences are severe. Radiation induced failures, or even battery life degradation, could result in surgical replacement of devices and put patient health in jeopardy.

The mechanisms of ionizing radiation effects in CMOS integrated circuits are explored in detail in Chapter 2, while the remainder of this thesis elaborates on a methodology to analyze ionizing radiation effects at the device and circuit levels, with the end result being a circuit simulation capturing radiation response. The capability for predictive radiation effect simulation allows designers to examine sensitive circuitry, and enables design changes to be made early in the product development process that would serve to increase radiation tolerance.

1.4 Goals and Approach

This thesis is divided into five chapters, with the early chapters serving to motivate investigation ionizing radiation effects in implantable medical devices.

The latter chapters then provide an analysis methodology to address the radiation effects issues. A case study is then presented implementing the analysis technique, which results in a circuit simulation capable of reproducing radiation-induced circuit failure seen in experimental irradiation testing.

Chapter 2 provides background into ionizing radiation damage in silicon dioxide (SiO_2). This includes some basic discussion into the history of ionizing radiation effects research. The chapter then details the physical nature of ionizing radiation interaction with dielectrics, with an explanation of the radiation induced defects and their effect on device and circuit operation. This chapter then concludes by relating the radiation-induced non-idealities to medical device circuit design concerns and also considers how traditional radiation hardening approaches fit within the medical device development framework.

In Chapter 3, the high voltage charge pump circuit, one of the most common and radiation sensitive sub-circuits used in medical devices, is described. Then a theory of operation is presented for a charge pump along with experimental data exhibiting output voltage collapse due to total dose exposure. Using the charge pump collapse as motivation, a failure analysis methodology is presented, which allows investigation and reconstruction of the radiation-induced degradation.

Chapter 4 provides the result of the charge pump analysis. Each step of the methodology and the resulting outcomes are described. Results of the analysis support the final determination that charge pump voltage collapse is the result of inter-device leakage currents due to radiation degradation of isolation oxides in the circuit. These conclusions are supported through individual test device

characterization, TCAD modeling, and the development of a radiation-enabled simulation of the charge pump that recreates voltage collapse seen in experiment.

The final chapter summarizes the thesis, reviews my contributions, and recommends future work. With respect to my contributions, the primary goals are to:

- Provide a reproducible procedure for radiation-enabled simulation that can be applied to other circuits and technologies.
- Qualify the need for predictive engineering of integrated circuit radiation response. Such capabilities allow design changes to improve radiation tolerance to be made early in the design development process.

By systematically approaching radiation effects issues in medical devices, non-idealities can be effectively managed or mitigated. Since exposure to ionizing radiation is sporadic, unlike electronics designed for space or nuclear applications, it would be imprudent to make radiation effects mitigation the central reliability concern of device designers. The ultimate goal is to balance the aim of improved radiation tolerance without having to perform major modifications to existing process and design procedures that would disrupt device design efficiency and efficacy.

CHAPTER 2 RADIATION EFFECTS BACKGROUND

2.1 Historical Perspective

The field of ionizing radiation effects research has been active for more than 60 years, studying the consequences of exposing electronics to the harsh environments in space and nuclear applications. Research on radiation effects in microelectronics began after the failure of seven satellites in 1963. On July 9th, 1962 the Atomic Energy Commission (AEC) and Defense Atomic Support Agency detonated a thermonuclear warhead above Johnson Island in the South Pacific Ocean. This experiment, in addition to similar nuclear tests by the Soviet Union, is attributed to increasing the amount of nuclear particles in the Earth's Van Allen belt [32-35].

It was later determined that the failure mechanism for the satellites could be attributed to the ionization of particles in the bipolar transistors leading to trapping of charged particles in the silicon surface. This resulted in increased leakage currents causing circuit failure [33]. It was then believed that CMOS transistors would be more radiation tolerant than bipolar transistors, due to the fact their transfer characteristics are not dependent on minority carrier lifetime [35]. However, testing of CMOS device radiation sensitivity at the Naval Research Laboratory (NRL) in 1964 revealed otherwise. It was reported that both n- and p-channel MOS devices exhibited sensitivity, which was linked to buildup of oxide-trapped charge and interface traps in device oxides [36, 37]. These results motivated the federal government to fund multiple research groups to investigate radiation effects and their impact on military space systems.

The 1970's saw the establishment of programs to develop radiation hardened CMOS integrated circuits. Sponsored by the Defense Nuclear Agency, these programs focused on modify gate dielectrics through oxide growth techniques, anneal conditions and doping conditions [36]. Additionally during this time, electronic spin resonance (ESR) on CMOS silicon dioxide films at NRL helped identify the root damage mechanism relationship to oxygen vacancy defects in the oxide [36, 38].

Due to the desire to increase component density on chip during the 1980's, local oxidation of silicon (LOCOS) replaced direct moat hardened isolation oxide as the isolating dielectric. The disadvantage to LOCOS was lateral intrusion of the so called "birds beak" into the active device channel width, which leads to increased radiation sensitivity [39]. As technology advanced, LOCOS was replaced by shallow trench isolation (STI) which allowed for increased component density. These isolations are preferable due to less lateral intrusion, better surface planarity and allowed for the continual increase in on-chip component density [39, 40].

The scaling of state-of-the-art digital technologies has reduced gate oxide thicknesses to less than 4 nm, and in doing, has made gate threshold voltage shifts due to ionizing radiation in these technologies less of a concern in comparison to isolation oxide damage. However for designs that require thicker gate oxides such as mixed-signal, power CMOS and Flash Memory, threshold voltage shifts are still a major concern [41-43]. Additionally it is seen that STI oxides are still significantly affected by ionizing radiation in modern CMOS devices, making

inter-device leakage and so-called device “edge” leakage a continued hindrance to radiation hardening commercial processes [29, 44, 45].

2.2 Total Dose Effects

Ionization is the process for which exposure to radiation in solid state materials causes electrons to be liberated from atoms in the material. This occurs due to the contact of charged particles (i.e., electrons, protons, alpha particles, and heavy ions) and/or high energy photons with the atoms of the material [46]. Energetic particles passing through electronic materials convert some quantity of the particle energy to ionization in the material. The quantity of energy converted into ionization can be determined by the linear energy transfer (LET) function, which gives the energy loss per unit length (dE/dx) of a particle. LET is a function of the mass and energy of the particle as well as the target material density. The LET is expressed in units of MeV-cm²/g, or in simple terms, the energy loss per unit length normalized to the density of the material of interest [46, 47]. Fig. 2.1 illustrates the LET in SiO₂ versus particle energy for electrons, protons, and secondary electrons generated by 10 keV x-rays and 1.25 MeV ⁶⁰Co γ -rays [48].

Interaction between charged particles and the material serves to generate electron-hole pairs (ehps) that lead to direct ionization damage. Alternatively, ionizing radiation damage due to photons is caused by indirect ionization. This process is started when ehps are created along the track of secondary electrons emitted during the photon interaction with the material. In both indirect and direct ionization, the density of ehps generated along the tracks of the charged particles is proportional to the energy transmitted to the material [49].

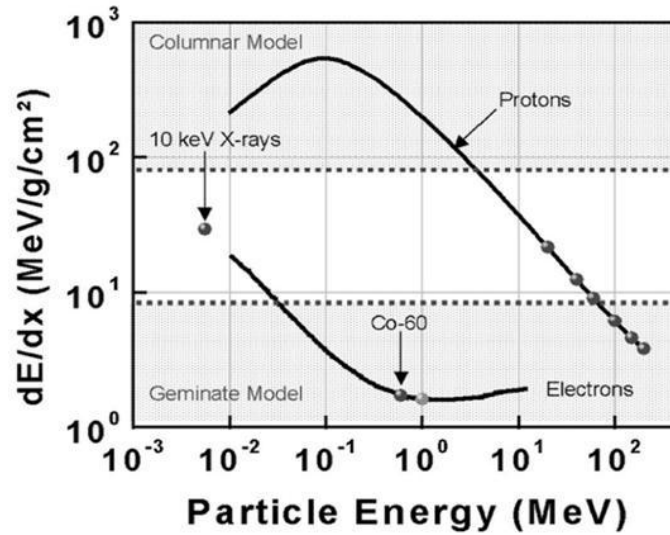


Fig. 2.1 LET vs. particle energy for electrons, protons, and secondary electrons generated by 10 keV x-rays and 1.25 MeV ^{60}Co γ -rays [48].

Energetic secondary electron generation from photon exposure occurs through three different processes. The dominant process depends on the photon energy and the material of interest. For low-energy photons interacting with Silicon (10-100keV), the photoelectric effect dominates as a photon serves to excite an electron to a high enough state to be emitted free of the atom. For higher energy photons in Silicon (0.1-10MeV) the Compton effect dominates. Similar to the photoelectric effect, a photon serves to excite an electron to a higher, free state. However, with Compton scattering, a lower energy photon is also created, which is free to interact with other atoms. Pair production occurs only at very high photon energies in silicon ($>3\text{MeV}$). In this process the high energy photon serves to create an electron-positron pair. The positron has the same properties as an electron, except that the charge is positive [31].

The total amount of energy deposited by a particle that causes the generation of an ehp is quantified as total ionizing dose (TID). A typical unit of TID is the rad (radiation absorbed dose), which signifies the energy absorbed per unit mass of a material ($1 \text{ rad} = 100 \text{ ergs absorbed per gram}$) [47]. The SI unit for TID is a gray ($1 \text{ Gy} = 100 \text{ rad}$). Gray is the commonly used while discussing ionizing radiation in medicine; however the rad is the conventional unit used by the radiation effects community.

Immediately after the generation of electron-hole pairs due to ionizing radiation, many of the electrons rapidly transport out of the dielectric leaving behind the slower holes. Depending on the electric field in the oxide during exposure, some electrons will recombine with holes. The fraction of the holes that do not recombine is known as the fractional hole yield. These remaining holes will transport along localized states in the oxide. During this transport process, some of the holes will be trapped, forming positive oxide-trapped charge, primarily near the $\text{SiO}_2\text{-Si}$ interface. Additionally, during the hole hopping and the charge trapping processes, hydrogen ions (protons) can be released. These ions can also drift or diffuses to the interface where they can cause the formation interface traps in the silicon bandgap. These four processes are illustrated in Fig. 2.2 [31, 46].

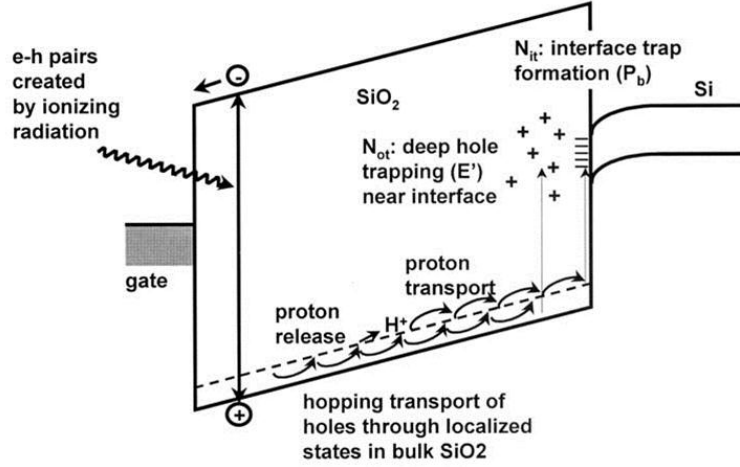


Fig. 2.2. Energy band diagram of MOS capacitor which illustrates the main processes for radiation induced charge generation [31][46].

2.2.1 Charge Yield

The four processes of radiation induced charge generation due to radiation exposure are all the result of conversion of dose (energy absorbed per unit mass of the material) into the generation of ehps. The amount of carrier generation can be expressed analytically using the following formula [31, 50]:

$$N_h \left[\frac{\# \text{ehp}}{\text{cm}^2} \right] = f_y(E_{ox}) g_o D t_{ox} \quad (2.1)$$

This gives the total number of holes generated per unit area of the material, N_h , as a function of the charge (or hole) yield, $f_y(E_{ox})$, the pair density conversion factor, g_o , the dose, D , and the oxide thickness in centimeters, t_{ox} . This equation is can be easily understood when related to qualitative description four processes given previously and illustrated in Fig. 2.2.

As described before, part of the energetic particle's kinetic energy is transferred to the material for ehp generation. The minimum energy required for creating an electron-hole pair, E_p , depends on the bandgap of the material. The

pair density conversion factor, g_o , which relates ehps generated to total dose can be calculated using following formula [51]:

$$g_o \left[\frac{\# \text{ehp}}{\text{cm}^3 \cdot \text{rad}} \right] = 100 \left[\frac{\text{erg}}{\text{g}} \right] \left[\frac{1}{\text{rad}} \right] \cdot \frac{1}{1.6 \times 10^{-12}} \left[\frac{\text{eV}}{\text{erg}} \right] \cdot \frac{1}{E_p} \left[\frac{\# \text{ehp}}{\text{eV}} \right] \cdot \rho \left[\frac{\text{g}}{\text{cm}^3} \right] \quad (2.2)$$

The relationship between ionization energy, material density, and generated carriers are listed in Table 2.1 for GaAs, Si, and SiO₂, respectively [31, 50].

Table 2.1 Minimum electron-hole pair creation energy, density and pair density generated per rad for a given material [31]

Material	E _p (eV)	Density (g/cm ³)	Pair density, g_o (ehp/cm ³ ·rad)
GaAs	~4.8	5.32	~7×10 ¹³
Silicon	3.6	2.328	4×10 ¹³
Silicon Dioxide	17	2.2	8.1×10 ¹²

Once generation of ehps has occurred, a fraction of the ehps are almost immediately annihilated through either columnar or geminate recombination [49]. The fraction of ehps that avoid initial recombination is the charge yield, f_y . If an electric field is present during this process, it serves to separate electrons and holes and reduce recombination. It then follows that charge yield is dependent on the magnitude of the local electric field in the material. The charge yield can then be approximated as

$$f_y(\vec{E}) \approx \left(\frac{|\vec{E}|}{|\vec{E}| + E_0} \right) \quad , \quad (2.3)$$

where \vec{E} is the local field vector and E_0 is the threshold field constant ($= 5.5 \times 10^5$ V/cm) [51, 52]. For two common radiation sources used for experimental testing, ⁶⁰Co gamma rays and 10 keV x-rays, $f_y(\vec{E})$ can be expressed as [53],

$$f_y(\vec{E})_{Co-60} = \left(\frac{0.55}{|\vec{E}|} + 1 \right)^{-0.7} \quad (2.4)$$

$$f_y(\vec{E})_{x-ray} = \left(\frac{1.35}{|\vec{E}|} + 1 \right)^{-0.9}, \quad (2.5)$$

where the local field vector (\vec{E}) is expressed in units of MV/cm. The charge yield is plotted for various radiation sources in Fig. 2.3 [31, 51, 52].

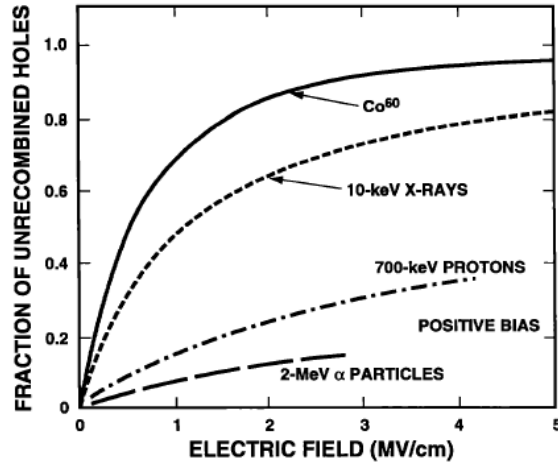


Fig. 2.3. Fraction of uncombined holes vs. electric field for various incident particles [31, 51, 52].

It is of note that the fractional hole yield seen in Fig. 2.3 actually increases with decreased energy of the incident particle. This can be explained by observing that a strongly ionizing particle forms dense columns of charge, in which the ehp recombination rate is high because of the decreased average spacing between pairs [31]. It is also obvious in Fig. 2.3 that with increased electric field the probability of recombination decreases.

2.2.2 Hole Transport

After ehp generation and initial recombination, the holes and electrons that do not recombine can transport through the silicon dioxide due to the local electric field. Since electrons have a high mobility (e.g., $\mu_n = \sim 20 \text{ cm}^2/\text{Vs}$ at 300K) they are able to transport out of the oxide, on the order of picoseconds [46, 47, 54]. However holes have a lower mobility ($\mu_p = \sim 1.6 \times 10^{-5} \text{ cm}^2/\text{Vs}$ at 300K), and consequently remain in the oxide. Holes then can transport through the oxide, some toward the SiO₂-Si interface. This process is a great deal slower than the electron transport, and is temperature and field-dependent [51].

As the hole transports through the oxide, it causes a distortion of the localized potential field in the lattice due to the hole's charge, as described by the continuous-time-random-walk (CTRW) hopping transport formalism [55, 56]. This model suggests that holes move by hopping between localized shallow trap states in the oxide. As a charged hole transports through the oxide, it causes distortion of the local lattice in the SiO₂ layer. This distortion also serves to increase the effective mass of the hole and decrease its mobility. The combination of the charged hole and its strained field is known as a polaron, and it is said that hole transport occurs through the lattice via "polaron hopping" [51, 56].

Once the trap depth increases past a certain limit, there is a possibility the hole could become trapped. Part of these transporting holes could also become trapped at sites near the SiO₂-Si interface, where they form the previously mentioned positive oxide-trapped charge (N_{ot}). These trapping sites are thought to be the result of neutral oxygen vacancies in the SiO₂ (E' centers) [57, 58],

although other work has proposed that hydrogen containing defects in the oxide may also trap holes [59, 60]. Reactions between holes and defects in the oxide can also lead to the creation of interface traps (N_{it}) [61]. The nature of positive oxide-trapped charge and interface traps generated due to ionizing radiation will be discussed further in sections 2.2.3 and 2.2.4.

2.2.3 Positive Oxide Trapped Charge

Holes generated via ionizing radiation can transport toward the SiO₂-Si interface in the presence of a positive gate bias. Due to lattice mismatch and the out-diffusion of oxygen, there are a large number of oxygen vacancies near the interface [62]. These vacancies can also be thought of as “excess” silicon at the interface that did not completely oxidize during fabrication. As the holes approach the interface, these vacancies trap some fraction of the holes. This fraction is a function of the capture cross section near the interface. The capture cross section depends highly on the device fabrication process, as fraction of trapped holes can vary from >3% for radiation hardened processes to as high as 50-100% for soft oxides [31].

Two oxygen vacancy defect types play a role in the transportation toward the interface and subsequently trapping of the hole as positive oxide-trapped charge. These defects, or E' centers, are classified as either E'_δ or E'_γ centers [29]. The E'_δ center is a shallow trap that impacts hole transport, as most of the E'_δ centers have energies located in the SiO₂ bandgap less than 1.0 eV from the oxide valence band. Alternatively, the E'_γ center is a deep trap, located at energy levels greater than 3 eV above the oxide valence band, and is responsible for charge buildup in

the near the interface [50]. Fig. 2.4 illustrates an energy band diagram of SiO_2 showing of the main E' centers and the relative position in the oxide.

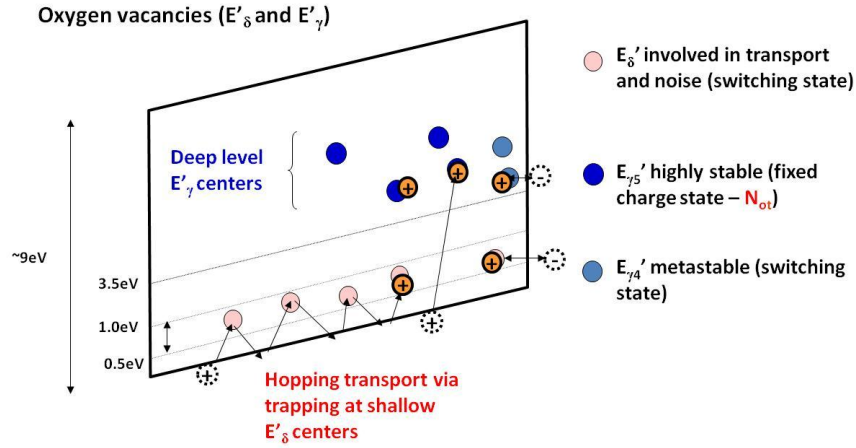


Fig. 2.4. Band Diagram of SiO_2 illustrating possible oxygen vacancies [50].

Following the trapping of charge in the oxide, neutralization of the charge can occur. The rate for which charge neutralization occurs has been shown to exhibit a time, temperature and electric field dependence. It is found experimentally that the voltage shift due to oxide-trap charge (ΔV_{ot}) exhibits logarithmic decrease in magnitude as a function of time during post-irradiation anneal. Additionally this logarithmic decrease is shown to be independent of the irradiation dose rate, however the magnitude of total recovery (total decrease in magnitude of ΔV_{ot}) is highly process dependent with some commercial processes exhibiting little charge neutralization [31, 63]. It is also found that for some technologies, elevated temperature anneals indicate that neutralization is a strongly thermally activated process, with time to 50% neutralization varying by approximately an order of magnitude between anneal temperatures of 25°C to

125°C [31]. Finally charge neutralization shows a strong bias dependency, with experimental data indicating that it is possible for charge neutralization under a large positive bias during anneal to be double that of neutralization seen in an unbiased anneal [31, 64].

It has also been illustrated in experiments that some of the charge neutralization seen is reversible by switching to a negative anneal bias. This indicates that the defect centers associated with the oxide-trapped charge are still present after anneal, and some of the appeared neutralization is actually just charge compensation [31]. There are two physical mechanisms that are used to describe the time, temperature and bias dependence of charge neutralization seen in experiment. Charge neutralization can occur from the tunneling of electrons from the silicon and the thermal emission of electrons residing in the oxide valance band to the oxide traps as illustrated in Fig. 2.5. The resulting effects on transistor operation due to positive-oxide trapped charge will be discussed further in section 2.3.

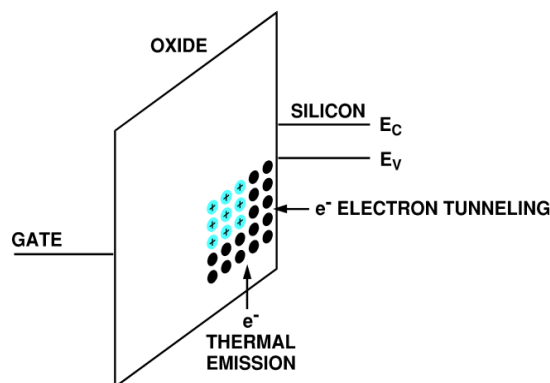


Fig. 2.5 Energy band diagram of a MOS Capacitor under positive gate bias which illustrates the are two oxide trapped-charge neutralization [31].

2.2.4 Interface Traps

Ionizing radiation also produces interface traps which form in the silicon bandgap. Since the radiation induced traps are developed physically at the SiO₂-Si interface, the traps can either be positive, neutral or negative as it easily donates or accepts electrons from the silicon, subject to the trap location in the bandgap and the applied external bias. Interface traps that fall in the upper half of the silicon bandgap, i.e., above the intrinsic Fermi energy, are generally considered acceptor-like. For these defects, if the Fermi level is above the trap energy level, the defect accepts an electron from the silicon and is negatively charged. If the trap energy falls in the lower half of the bandgap, i.e., below the intrinsic Fermi energy, the defects are typically denoted as donor-like. For these interface traps, if the Fermi level is below the trap level an electron is donated to the silicon, leaving behind a positive charge. If the intrinsic Fermi energy is equal to the Fermi level at the interface (a midgap voltage is applied to the gate), there is no net charge contributed by the interface traps [31].

Interface states resulting from ionizing radiation exposure are identified as dangling bond defects called P_b centers [50, 65]. These P_b defects are classified by two center types, P_{b0} and P_{b1} . P_{b0} centers are common to the (111) silicon surface, with the dangling bond defect extending normal to the oxide. The P_{b1} center is closely related to the P_{b0} defect but common to (100) silicon [50]. A graphical representation of the two common defect centers is provided in Fig. 2.6.

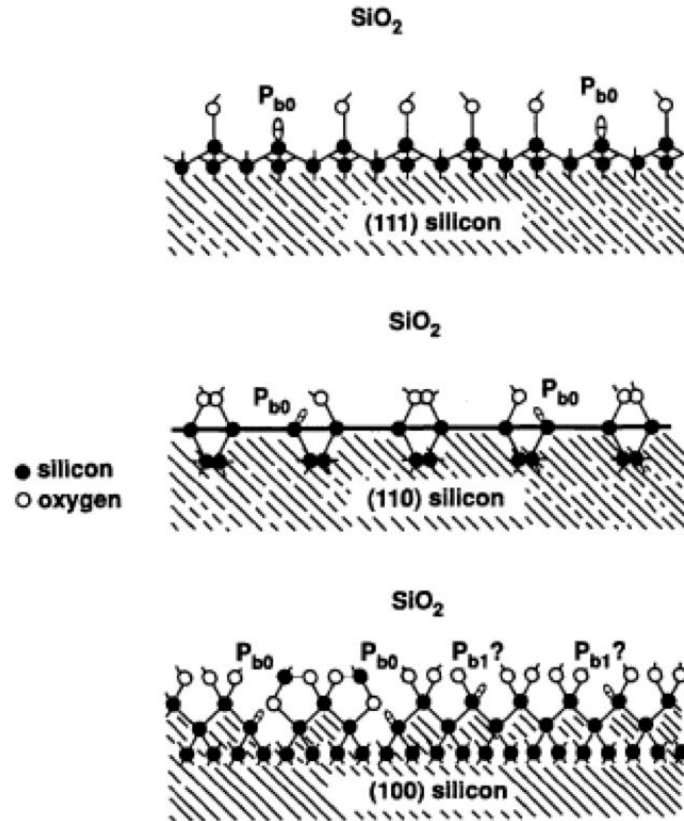


Fig. 2.6. Model of P_{b0} and P_{b1} interface trap centers on (111), (110) and (100) silicon [50, 66].

Accumulation of interface traps following irradiation is a relatively slow process, with trap generation occurring seconds to thousands of seconds after exposure. It is believed trap formation occurs by way of a two-step process. The process begins in a similar fashion to that of the oxide-trapped charge formation, with the ehf generation due to ionization. Again, the fraction of holes that do not immediately recombine are capable of transport through the oxide. As previously discussed, the hole can be trapped, or alternatively, it may interact with oxide defect centers containing hydrogen (DH centers). These defect centers are found to be naturally occurring in the oxide or formed during fabrication processing.

This results in the release of positively charged hydrogen atoms, also known as protons (H^+) [59, 67]. It is thought that the majority of the protons are released when a hole is captured or released from a hydrogen-passivated oxygen vacancy during the hole hopping process [67]

The released proton (H^+) can now transport toward the interface in a manner similar to the hole hopping process under the influence of a positive electric field. At the interface the protons can serve to break the Si-H bonds, form in H_2 and a dangling Si-bond. This reaction can be expressed as [50, 61],



The product of this reaction is an interface trap defect (D^+). As discussed previously, the interface traps (N_{it}) can interchange charge with the silicon due to the close proximity of the trap at the interface, leaving no barrier to charge movement. The use of hydrogen is prevalent during CMOS processing thus the possibility of hydrogen-passivated silicon dangling bonds is highly likely. The resulting effects on transistor operation due to interface trapping will be discussed further in section 2.3.

2.3 Device Response Considerations – Effects on Gate Oxides

Both positive oxide-trapped charge and interface traps resulting from ionizing radiation can be seen manifested in the CMOS DC characteristics as a reduction of the threshold voltage and decrease in the subthreshold slope. This is illustrated by example in Fig. 2.7 and Fig. 2.8.

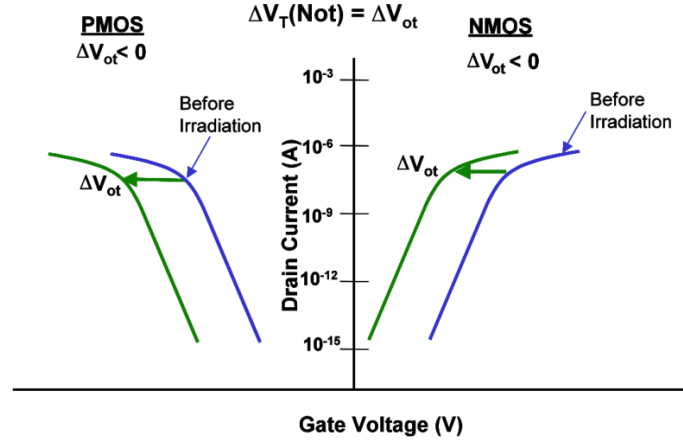


Fig. 2.7 Illustration of the shift in the drain current vs. gate voltage characteristics of n- and p-channel MOSFETs as a result of positive oxide-trapped charge [50].

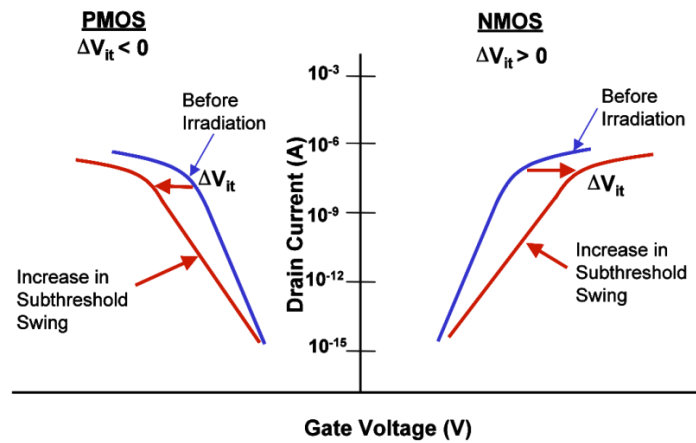


Fig. 2.8 Illustration of the shift in the drain current vs. gate voltage characteristics of n- and p-channel MOSFETs as a result of interface traps [50].

As seen in Fig. 2.7 the buildup of positive oxide trapped charge in the gate oxide serves to reduce the threshold voltage for both n and p-channel MOSFETs. Additionally the shift in threshold voltage for n-channel MOSFETs results in an increase in off-state and drive currents, while in p-channel MOSFETs off-state and drive currents are reduced. As seen in Fig. 2.8 interface trap buildup serves to decrease the subthreshold slope, or as it is often described increase the

subthreshold swing, of a CMOS device. Additionally an increase in threshold voltage is seen for n-channel MOSFET while the threshold voltage of a p-channel MOSFET is reduced (becomes more negative) with the increased presence of interface traps. The bias dependence of the trapping or de-trapping of charge at the interface in the created trap states can explain this shift in current-voltage due to interface trapping. During the current-voltage characterization the silicon surface at the Si-SiO₂ interface is swept from accumulation to inversion by the gate voltage. Increased interface trapping inhibits the gate's ability to invert the silicon surface.

It is seen in equation (2.1) that the magnitude of holes generated due to ionizing radiation shows a linear dependence on oxide thickness (t_{ox}). The amount of holes generated directly determines the amount of oxide-trapped charge (ΔN_{ot}) and interface traps (ΔN_{it}) generated in the oxide as discussed in sections 2.2.3 and 2.2.4. This indicates that the magnitude ΔN_{ot} and ΔN_{it} will both decrease with decreased oxide thickness due to device scaling. Additionally, it is understood that the magnitude of the radiation induced voltage shift (ΔV_{ot}) due to oxide-trapped charge (ΔN_{ot}) can be calculated using the following formula [29]:

$$\Delta V_{ot} = -\frac{t_{ox}}{k_{ox}\epsilon_o}q\Delta N_{ot} \quad (2.7)$$

Equation 2.7 includes constants for elementary charge (q), dielectric constant for SiO₂ (k_{ox}) and permittivity of free space (ϵ_o). Considering the ΔN_{ot} dependence on oxide thickness in equation (2.7) indicates that negative threshold

voltage shifts caused by fixed oxide trapped charge buildup is proportional to the square of oxide thickness, as seen in,

$$-\Delta V_t(\Delta N_{ot}) = -\Delta V_{ot} \propto t_{ox}^2 \quad (2.8)$$

This indicates that device scaling, and the reduction of gate oxide thicknesses in a given technology will serve to limit the effect of oxide trap charge on threshold voltage. In effect device scaling has increased the radiation hardness in the most state of the art technologies making threshold voltage shifts due to gate oxide degradation a minimal issue, as verified through experiment [45].

2.4 Effects on Isolation Oxides

While the hardness of gate oxides to ionizing radiation has been greatly increased due to device scaling, isolation oxides still remain relatively soft. In both older (LOCOS) and later (STI) isolation technologies, the buildup of oxide-trapped charge resulting parasitic leakage current is shown to be an issue [29, 31, 38-40, 44, 46, 49]. Possible leakage current paths are exemplified in Fig. 2.9. Intra-device drain-to-source (so called “edge”) leakage in n-channel MOSFETs can result from buildup of oxide-trapped charge near the active device edge, as seen in Fig. 2.10. This edge leakage can be thought of as a separate parasitic edge transistor acting in parallel with the gate oxide transistor. This is illustrated in current-voltage characteristics of Fig. 2.11.

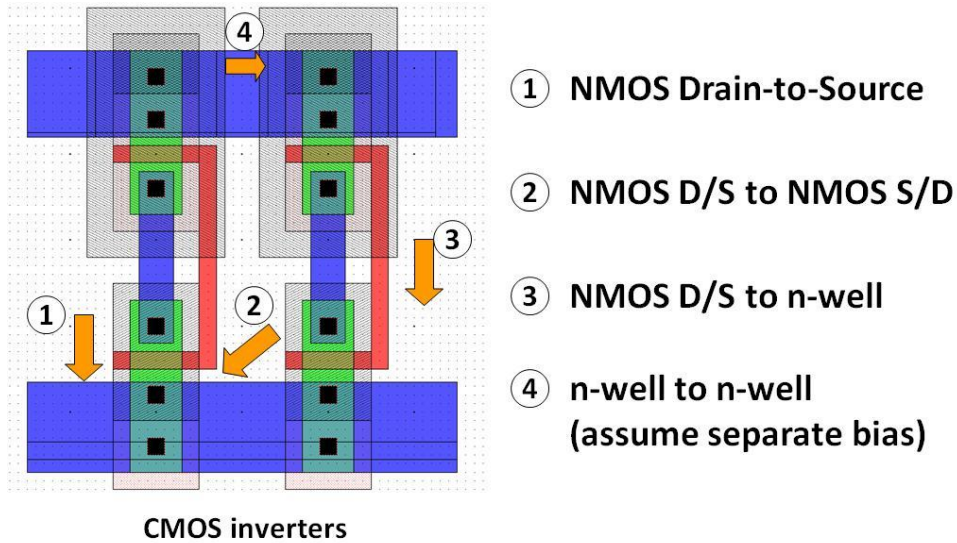


Fig. 2.9 Possible intra- and inter-device leakage current path resulting from oxide trapped charge buildup in LOCOS or STI isolation oxides [50].

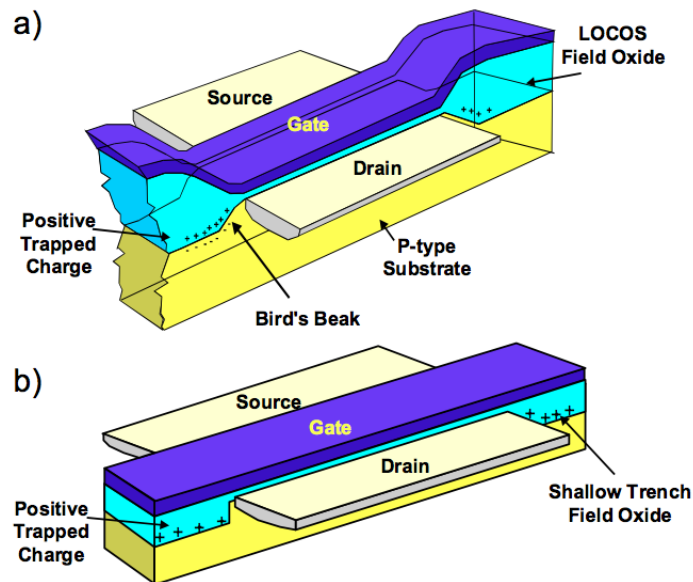


Fig. 2.10 Cross section of a) LOCOS isolated and b) STI isolated transistor showing trapped-charge location corresponding with intra-device edge leakage current [31, 68].

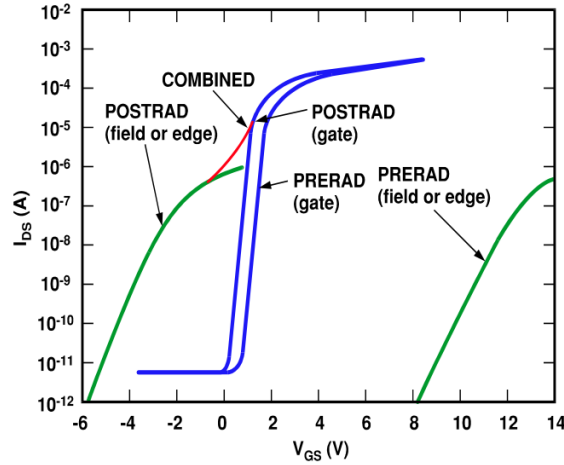


Fig. 2.11 Current-voltage characteristics of gate-oxide and a parasitic "edge" transistor showing increase in current post-irradiation due to the parasitic edge transistor [31].

Additionally the buildup of oxide-trapped charge in the base of the isolation oxide can result in inversion of silicon causing inter-device leakage current (paths 2 to 4 of Fig. 2.9). Oxide trapped-charge buildup is enhanced by the presence of a local electric field in the isolation oxide. High bias voltages on polysilicon and metal device interconnections on top of isolation oxides serve to generate this field. Parasitic current between active transistors can result in loss of device isolation, increased drain on voltage supplies, and the collapse of desired node voltages [29, 31, 34, 39, 44].

2.5 Radiation Hardening for Implantable Medical Device Electronics

Integrated circuit manufactures designing products for space and nuclear applications desire extremely radiation tolerant circuits. As such, radiation mitigation strategies have been developed including the use of "rad-hard" foundry processes, use of state-of-the-art technologies shown to be more radiation tolerant,

and specialty transistor geometries shown to mitigate edge leakage [44, 45, 69, 70]. However these options are often impractical for manufacturers of integrated circuits for implantable medical devices. Due to the low-volume nature of “rad-hard” foundries, they are often highly cost prohibitive for all except cases where extreme radiation tolerances are required. Since medical device radiation exposure levels are expected to be low, rad-hard processing is not a prudent option. As described previously, current commercial state-of-art technologies have been shown to be more radiation tolerant than older processes. However, medical device designs require high device reliability and ultra-low power consumption, as described in chapter 1. Due to these stringent requirements, medical device manufacturers adopt a “fast follower” approach to new technologies, and will not adopt new process unless thoroughly vetted [4, 25, 28].

Because of these reasons, medical device manufacturers are best implement radiation hardening by design in a strategic and measured fashion. By making the most minimally invasive design and layout changes, while working within current circuit design goals and constraints, a targeted level of radiation tolerance can be achieved. The rest of this thesis focuses on the development of radiation-enabled circuit simulation methodology (Chapter 3). This methodology is put into practice to model the voltage collapse of a charge pump circuit common to implantable pacemaker devices (Chapter 4). The capability for predictive engineering of a given circuit or technology’s radiation response allows for design changes to be made early in the development process to improve radiation tolerance.

CHAPTER 3 FAILURE ANALYSIS METHODOLOGY

3.1 Case Study

To develop and validate the failure analysis methodology as part of a radiation hardening by design strategy, an integrated circuit which is part of an implantable pacemaker design is chosen as a case study. The IC of study is used to provide electrical impulses, delivered by electrodes contacting the heart muscles, to regulate the beating of the heart. The IC has multiple functional digital and analog blocks used to provide multi-chamber pacing and recharge support for the pacemaker device. However the focus of this study is on a single block of the IC, the negative supply pumps. The choice to investigate the negative supply pumps, implemented as a charge pump topology, makes is particularly appropriate as a) charge pumps are widely used in implantable device and medical applications for voltage generation and b) high circuit bias conditions serve to enhance ionizing radiation damage potential in device oxides.

To understand the negative supply pumps, the first half of Chapter 3 provides some charge pump background information and common implementations for context. Then the theory of operation for the charge pump of study is detailed, which is critical in understanding the failure mode shown. Finally the experimental irradiation results showing collapse of the charge pump output with applied dose is shown as motivation. The second half of Chapter 3 details the failure analysis approach taken to identify and simulate the cause of voltage collapse.

3.1.1 Charge Pump Background

High voltage switched capacitor charge pump topologies are becoming increasingly implemented in such applications as non-volatile memory and medical devices to generate a range of potentials from a single battery voltage [71-73]. In many cases, existing supply voltages in low power ICs are insufficient for some application specific operations, such as floating gate programming, as an LCD driver or simply to generate battery-multiplied supply rails on chip. Charge pumps used in these types of applications are particularly susceptible to radiation-induced degradation because their higher voltage specifications typically require the utilization of devices manufactured with thicker dielectrics and lower doping levels. It is well known that these properties make high voltage CMOS technologies more susceptible to TID damage than advanced low power CMOS processes [29]. Moreover, the higher voltage requirements result in larger electric fields, particularly in isolation (field) oxides, which will enhance radiation-induced defect buildup [30, 31]. The combined impact of lower doping and high electric fields leads to greater levels of field oxide leakage that, as will be shown, increases current draw at the charge pump output.

3.1.2 Theory of Operation

For the IC design studied here it is desired to have to large negative voltage rails, equal to $-1 \times V_{DD}$ and $-3 \times V_{DD}$, with respect to ground that can be used throughout the circuit. Since the circuit is implemented as part of an implantable pacemaker, only two supply voltage rails (V_{DD} and GND) are available

externally from the device battery. This necessitates the implementation of a dual-charge pump topology, capable of internally generating the required voltages.

The $-3\times V_{DD}$ supply is predominantly used in the circuit as a gate voltage for large p-channel transistors implemented as switches. By using a large negative voltage on the p-channel gate permits an elevated gate to source voltage V_{gs} . Larger V_{gs} translates into a smaller “on” resistance per gate width for the large p-channel switches. The generated $-1\times V_{DD}$ voltage is used predominantly as the “off” state gate voltage for switches throughout the design. Additionally both the generated negative voltages are used as supply voltage rails for other sub circuits such as amplifiers and comparators.

Fig. 3.1 illustrates the charge pump implementation in the overall integrated circuit scheme. The charge pump block contains the $-1\times V_{DD}$ pump, $-3\times V_{DD}$ pump and the non-overlapping clock generation circuit.

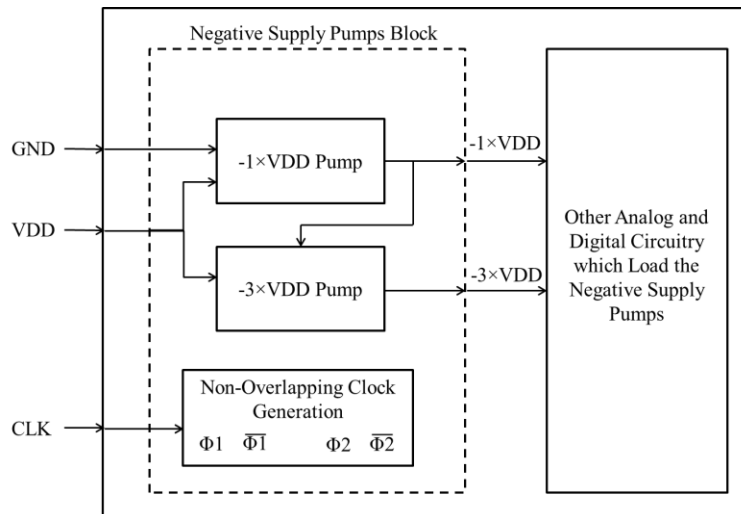


Fig. 3.1 Simplified block diagram of integrated circuit implementation of Negative Supply Pumps.

The Non-Overlapping Clock Generation circuit uses the external clock (CLK) to create two non-overlapping clocks ($\Phi1$ and $\Phi2$) and their complements ($\overline{\Phi1}$ and $\overline{\Phi2}$). The external clock (CLK) is set for a 50% duty cycle and a frequency of ~500Hz in normal mode and can increase to a boost mode frequency ~4kHz for use during higher demand for negative supply pump current drain functions. Internally generated clock $\Phi1$ is high when CLK is low and $\Phi2$ is high when CLK is high. The non-overlap period for the generated clocks is set to ~50ns. This must be maintained to prevent opposing switches to be “on” at the same time which would result in power supply crowbar current.

These generated clocks are used to open and close switches within the $-1\times VDD$ and $-3\times VDD$ supply pumps, as shown schematically in Fig. 3.2. Negative supply pump operation can be characterized by two phases, “charge” and “pump”, for each of the two generated voltages, as shown in Fig. 3.3. During the $-1\times VDD$ node “charge” phase, the $-1\times VDD$ pump capacitor (C1) is connected between the VDD node (anode) and GND node (cathode) supplies, which results in the pump capacitor being charged up to approximately the VDD voltage. During the $-1\times VDD$ node “pump” phase, the $-1\times VDD$ pump capacitor is connected from GND node (anode) to $-1\times VDD$ node (cathode), which results in the hold capacitor (C2) being pumped down to approximately a $-1\times VDD$ voltage.

During the $-3\times VDD$ node “charge” phase, the $-3\times VDD$ pump capacitor (C3) is connected between the VDD node (anode) and $-1\times VDD$ node (cathode) supplies, which results in the pump capacitor being charged up to approximately $(VDD - (-1\times VDD))$ or approximately $2 \times VDD$ in voltage. During the $-3\times VDD$

node “pump” phase, the $-3\times VDD$ pump capacitor is connected from $-1\times VDD$ node (anode) to $-3\times VDD$ node (cathode), which results in the hold capacitor (C4) being pumped down to approximately a $-3\times VDD$ voltage.

The switching frequency of the charge pump is set such that the output voltage magnitudes builds up properly on the hold capacitors at start up and is short enough to prevent RC decay of the voltage during standard operation due to current loading from the rest of the circuit. Changes in the switch operation in the negative supply pumps, or in the loading on the output nodes could adversely affect the circuit’s ability to generate and then hold the desired negative voltages.

The two supply pumps contain four capacitors total; two 39 nF pump capacitors (C1 and C3) and two hold capacitors (C2 and C4) of capacitances of $0.47\mu F$ and $0.10\mu F$ respectively. The two pumps also contain eight MOSFET switches, two p-channel FETs (S1 and S5) and six n-channel FETs (S2-S4 and S6-S8).

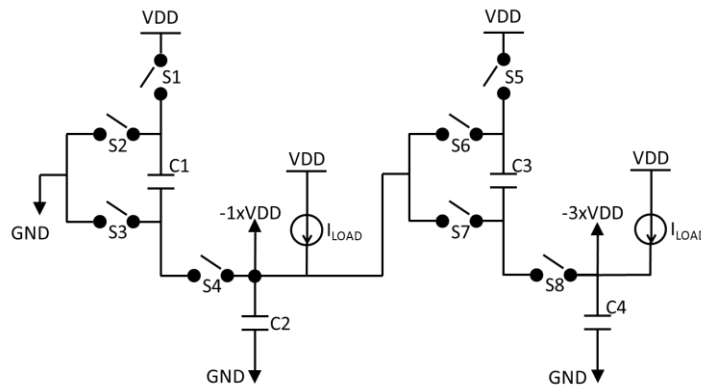
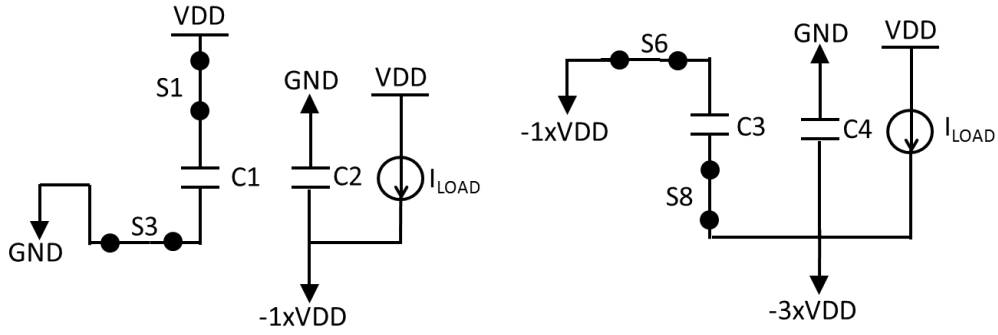
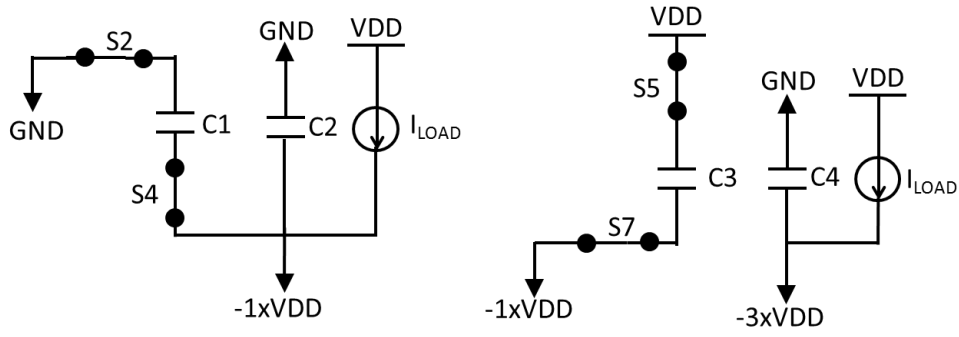


Fig. 3.2 Dual charge pump configuration implemented to generate $-1\times VDD$ and $-3\times VDD$ from the externally available VDD and GND voltages.



(a)



(b)

Fig. 3.3 Configuration for (a) ϕ_1 phase. $-1 \times V_{DD}$ is in “charge” phase, and $-3 \times V_{DD}$ is in “pump” phase. (b) ϕ_2 phase. $-1 \times V_{DD}$ is in “pump” phase, and $-3 \times V_{DD}$ is in “charge” phase.

3.1.3 Experimental Irradiation Results

For the radiation failure analysis of the charge pump, the focus was on degradation in the high voltage $-3\times VDD$ output node. The radiation response of the $-3\times VDD$ with applied total dose is shown in Fig. 3.4. It is seen that at 1 krad(Si) of total dose exposure, the output has reduced by more than 1V, and after 2 krad(Si) total dose exposure the output has reduced 50% from the operation specification. Such a reduction in the charge pump output is considered unacceptable for the integrated circuit design. These results serve as motivation for the failure analysis case study, and represent the dataset that is to be recreated via a radiation-enabled simulation.

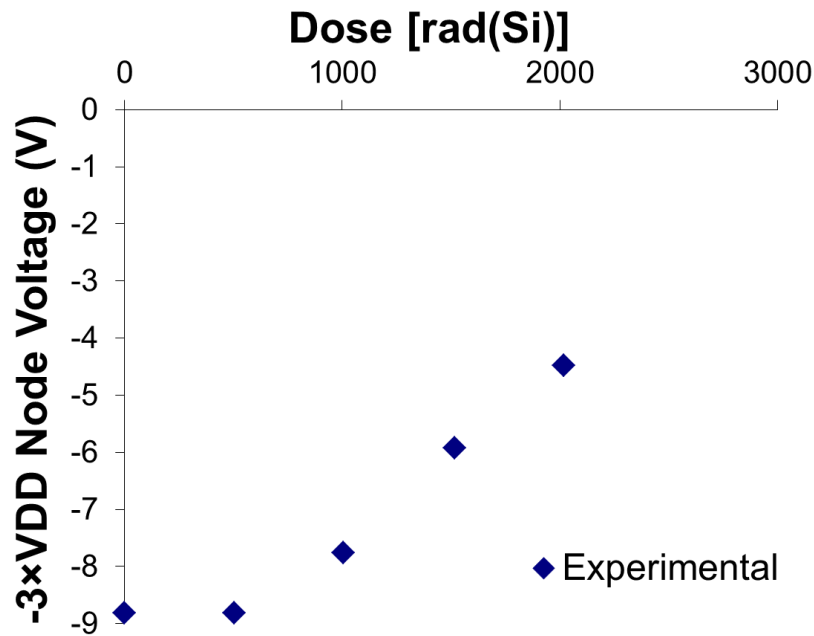


Fig. 3.4 Experimental Data showing voltage collapse of the $-3\times VDD$ charge pump output versus applied total dose.

3.2 *Failure Analysis Approach*

Determining the root cause of failure of any medium-to-large scale integrated circuit is not a trivial task. Correlating non-ideal device effects studied by device and process engineers to the simulations and layout work of the circuit designers is a critical link necessary to maintain circuit reliability. This connection is often not as strong as needed as designers must see the circuit from a top-down, system perspective, while device engineers are concerned about the characteristics of the individual transistors. The best way device engineers communicate and influence designers is through the compact models used for circuit simulation, and the setting of design rules as part of the process design kit used for circuit layout.

In this study, the link is made to communicate radiation effects by giving designers the capability to see the possible degradation of their circuits in their current simulation tools. We achieve this through the creation of radiation-enabled compact models that, when implemented in circuit simulations, can provide instant feedback to the designers. Simulating with these compact models allows the designers to see the impact of radiation immediately, allowing circuit changes to be made early in the design process to lessen the non-ideal effects on the finished integrated circuit.

The goal of the failure analysis case study is to explain the degradation exhibited as a collapse of the $-3\times VDD$ charge pump output with increasing total dose exposure. To accomplish this, extensive experimental work, device modeling and circuit and layout analysis is needed. The process taken is shown graphically in Fig. 3.5 and detailed throughout the rest of Chapter 3.

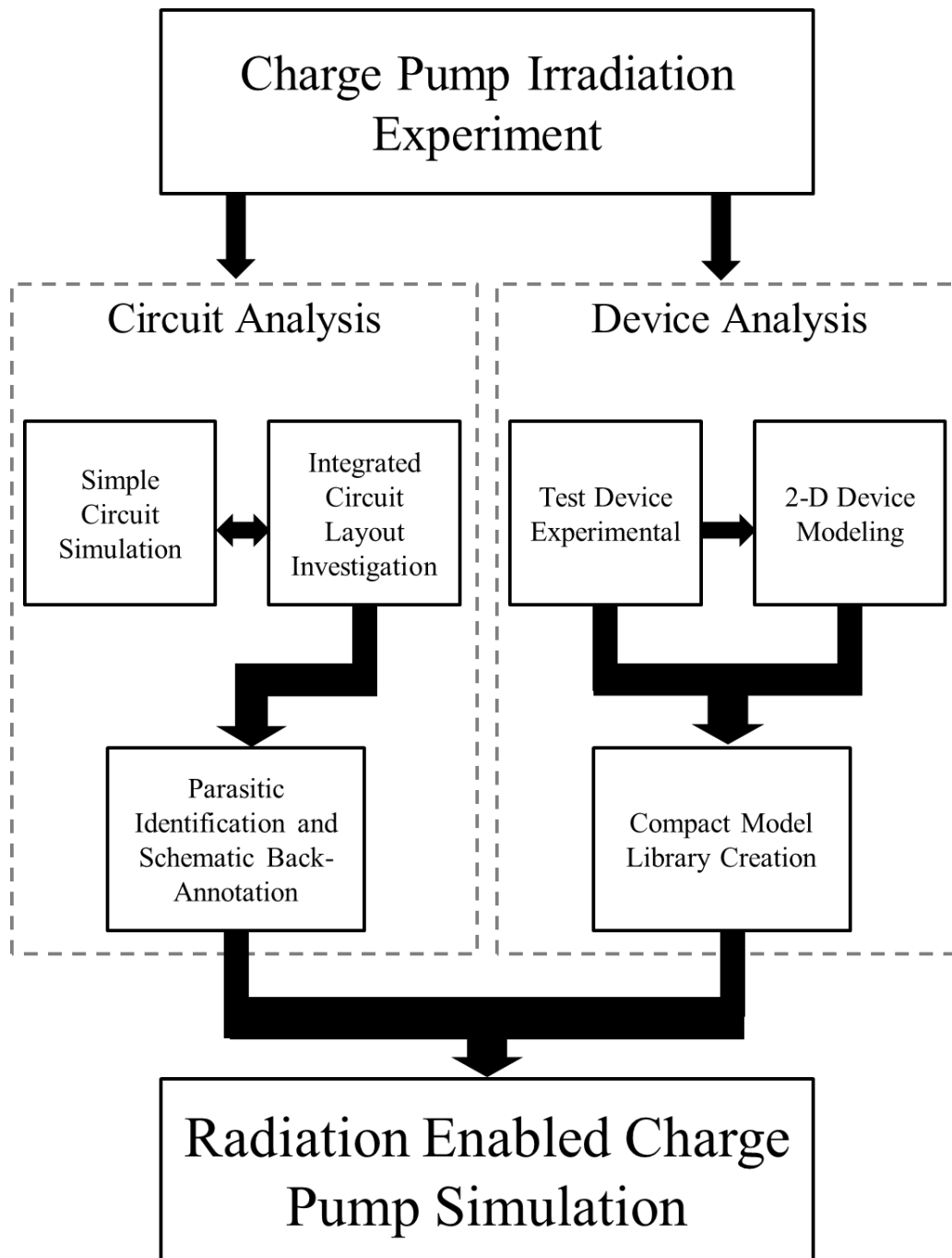


Fig. 3.5 Flowchart outlining the failure analysis case study.

3.2.1 *Experimental Testing*

To characterize the total dose radiation response of the charge pump circuit, the complete integrated circuit was irradiated. The integrated circuit was operating in its standard mode during irradiation; with the charge pump outputs set to $-1 \times VDD$ ($\sim -3V$) and $-3 \times VDD$ ($\sim -9V$). Radiation exposure of the charge pump IC was performed in an x-ray irradiator (110 kV, 6 mA source with a 230 mm source-to-surface distance). Circuit irradiation results $-3 \times VDD$ node voltage collapse as previously presented in Fig. 3.4.

To understand the effects of ionizing radiation on gate and isolation oxides, it is necessary to characterize test devices pre- and post-irradiation to determine sensitive circuit elements. For the case study, a process monitor (PM) test chip was available that included standard two-edge MOSFETs of various width/length ratios (i.e., “as designed” transistors) as well as specialized field oxide FETs (FOXFETs) representative of the isolation oxide structures separating the “as-designed” transistors on the chip. The isolation oxides in this technology are conventional local oxidation of silicon (LOCOS) structures, with average thickness of 1,000 nm. Radiation exposures of the PM devices were performed at room temperature in the ^{60}Co Gammacell irradiator at Arizona State University. Both irradiations were completed using the step stress approach in accordance with MIL STD 883 1019.4 with corrective calculations made to ensure corresponding dosimetry between sources.

The two-edge n-channel MOSFETs were irradiated with a gate bias of VDD (3.2V) and with all other terminals grounded while two-edge p-channel

MOSFETs were configured with zero bias (all terminals grounded) during irradiation. The n-channel FOXFET devices were biased with a gate potential of $4 \times V_{DD}$ (12.8V) with all other terminals grounded. Irradiation biases were chosen to match conditions in the charge pump circuit and provide a realistic bias scenario with electric fields present that would maximize TID damage to the oxides.

Three different DC current-voltage measurements were performed prior to irradiation, and then after three irradiation stress steps of 0.3k, 0.9k and 3.0krad (Si), to generate data suitable for compact model creation: drain current vs. gate voltage sweep with drain voltage held low (100 mV), drain current vs. gate voltage sweep with drain voltage held high (3.2 V) and a drain current vs. drain voltage sweep with gate voltage stepped by 1 V. All electrical measurements were made within 10 minutes after completion of irradiation to limit the effect of annealing in the measurement.

3.2.2 Device Modeling

While experimental data is highly valuable in the failure analysis process, it is often highly beneficial to supplement with data obtained through device modeling. This is particularly evident while studying the effects of ionizing radiation, as experimental data costs time and money. Getting experimental time with a radiation source is not always easy, and generating the test periphery (packaging die, PCB boards, biasing connections, etc.) is time consuming. Additionally, since the radiation physically alters the silicon dioxide properties, irradiated devices are basically destroyed following radiation characterization. For

every irradiation and characterization performed, a new set of devices must be used. Limiting the wasted die by coordinating limited and focused testing is good strategy.

Device modeling is achieved by way of 2-D computer simulation in Silvaco ATLAS. Silvaco allows for creation of 2-D structures via a graphical user interface, and allows for device simulation for electrical characterization. Additionally the radiation effects module (REM) for Silvaco is employed. REM is a self-consistent field/charge-trapping module, which models ionizing radiation-induced transport and non-uniform trapping of charge in the oxide. REM allows simulation of the radiation response for the modeled device at user-defined dose stress step points and bias conditions. The process to calibrate the 2-D ATLAS structure with the REM module is outlined in Fig. 3.6.

Device models are generated using process information such as doping densities and device geometry information. The model is then calibrated against pre-irradiation experimental data to provide authenticity to the modeled output. Once a pre-irradiation structure is calibrated, further REM calibration is realized by fine-tuning REM radiation parameters such that the Silvaco simulation matches closely to the known experimental electrical characteristics for the pre-irradiation dataset and one of the post-irradiation datasets. Then simulating with the tuned REM parameters at other dose levels achieved in experiment the model fit can be verified against experiment. By showing good agreement at multiple dose levels, a calibrated TCAD model is achieved.

The combination of data obtained through experiment and through device modeling simulation allows for the creation of multiple compact models for pre and post-irradiated devices. A compact model library can be developed in the BSIM3v3 modeling framework from the merged datasets.

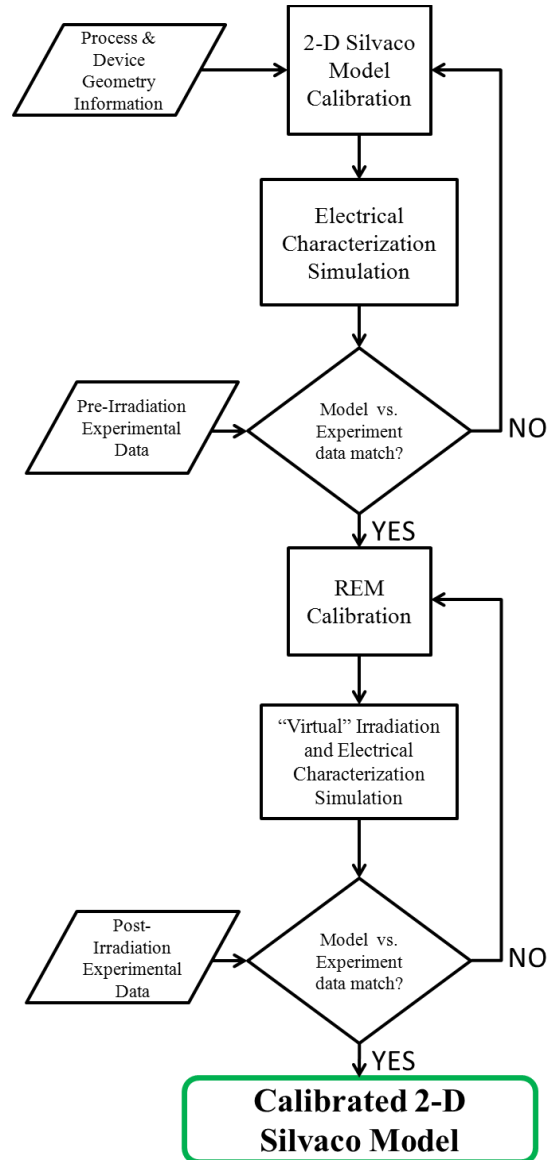


Fig. 3.6 Process flowchart outlining the calibration of the 2-D structure in Silvaco ATLAS with the radiation effects module (REM) implemented.

3.2.3 *Circuit Analysis*

In order to relate the results found in individual device testing and modeling to the output voltage collapse seen by complete circuit testing, detailed circuit and layout analysis is needed. This is analogous to the previous discussion about connecting the work of design and device engineers. The process began with a top-down analysis, using simple circuit simulation to motivate targeted investigation of possible sensitive parts of the design.

As discussed in the radiation effects background of Chapter 2, many of the device effects related to ionizing radiation lead to increased current flow through as-drawn devices, and inter-device current flow under isolation oxides. By combining the possibility of radiation-induced leakage to a single ideal leakage current in between nodes for a simplified simulation can be highly beneficial early in the failure analysis. To do this, simulation of the charge pump circuit can be performed with the insertion of a current source into schematic. By simple circuit analysis of the effects of the ideal leakage current on different nodes in the schematic, we can try and recreate the failure mode seen in the experimental voltage collapse. Successful recreation of the voltage collapse with the current source directs the analysis toward possible sensitive regions in the integrated circuit. Combining the knowledge gained from simple circuit analysis with device degradation uncovered by test device experimental data and computer modeling serves to point at the primary mechanism leading to circuit failure.

The most radiation sensitive circuit elements are identified by the previous steps in the process and then chosen for compact model creation. For the sensitive

as-drawn devices new compact models, which are a direct replacement for original design compact models, can be generated. However, when the concern is creation of inter-device leakage paths due to damage in isolation oxides, we must introduce new schematic symbols and connections in schematic to properly simulate these devices. This identification of inter-device parasitics and schematic back-annotation is the final step needed to support radiation-enabled simulation.

3.2.4 Radiation Enabled Circuit Simulation Methodology

To validate the failure analysis conclusions it is necessary to recreate the ionizing radiation degradation in simulation. For the purposes of the charge pump case study, the goal is to recreate the collapse of the $-3\times VDD$ voltage node. This required the design of a new simulation methodology allowing for radiation enabled circuit simulation. Understandably, the capability to plot the change in a circuit parameter (in the case study $-3\times VDD$ node voltage) versus total dose is not a standard part of production circuit simulation tools. To do this, a transient simulation of the charge pump output voltage can be run multiple times, and during each simulation a new set of compact models is used. The process of selecting a compact model set can effectively set the dose level of the circuit simulation, as the compact model itself was created at a certain exposure level. This process implemented for simulation of the charge pump is represented graphically in the flowchart of Fig. 3.7.

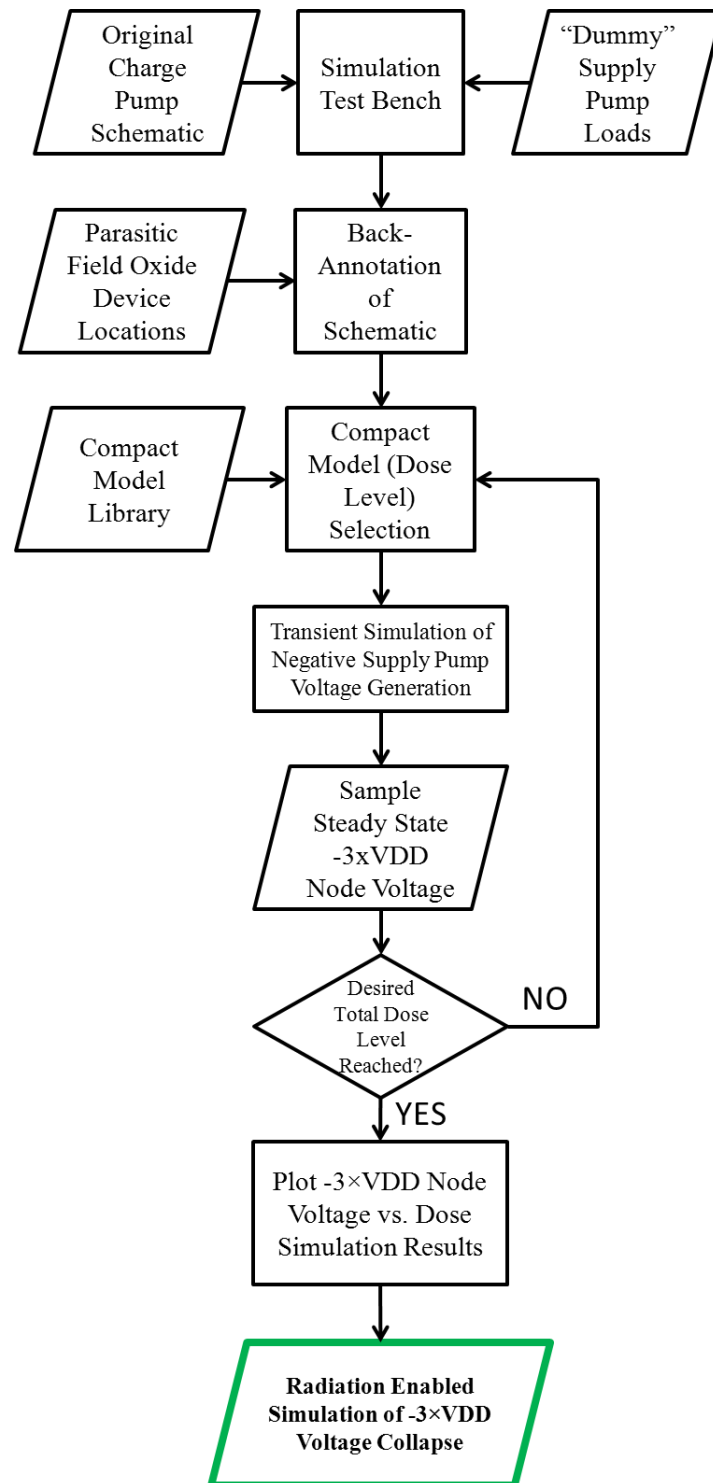


Fig. 3.7 Flowchart detailing steps to generate the $-3\times VDD$ collapse vs. dose via radiation enabled simulation.

For the initial setup of the simulation test bench, it was necessary to extract the charge pump and non-overlapping clock generation sub-circuits from the original top level schematic. Since the rest of the integrated circuit for which the $1\times VDD$ and $-3\times VDD$ are used serve to load the charge pump, it must be represented in the test bench. This is done by insertion of “dummy” loads onto the charge pump output, as used by the designers during circuit development. Now that all “as-drawn” devices have been placed in the test bench, it is also necessary to determine if any parasitic devices that could be activated via radiation exposure should be added to the schematic. As we “virtually irradiate” the circuit in simulation these devices must be considered as part of the response.

The full simulation schematic is now established in the test bench, and now to choose our simulation dose level, we reference the established compact model library. Since the models were created after a specific dose exposure level, the model represents the device’s operation at that exposure level. By selecting a particular exposure level (compact model set) for all devices in schematic, we then simulate the circuit at that exposure level.

For the charge pump circuit we run a transient simulation of the pump operation as the $-3\times VDD$ node voltage builds up on the hold capacitor. We then note the final steady state voltage for the node at the chosen simulated exposure level. Next we re-select our compact model library set at the next exposure level, and repeat the simulation. Parametrically running in the simulation and substituting compact model sets effectively increases total dose exposure.

Once the final total dose exposure level is reached, we now have a dataset of samples of the steady state $-3\times VDD$ node voltage for each of the simulations run. By plotting that dataset of node voltage versus total dose for the simulations, we then recreate the experimental collapse due to irradiation.

CHAPTER 4 ANALYSIS AND SIMULATION RESULTS

To investigate the collapse of the $-3\times VDD$ voltage node due to ionizing radiation, the failure analysis methodology of Chapter 3 is employed. By following the failure analysis process and constructing a radiation-enabled simulation that successfully recreates the voltage collapse seen in experiment, the root cause of failure is found and the methodology is validated. Chapter 4 summarizes results obtained using this failure analysis methodology, presents the results of the radiation-enabled circuit simulations and discusses the implications for targeted radiation hardening of integrated circuits.

4.1 Test Device Characterization

To investigate the effect of ionizing radiation on MOSFETs within the charge pump integrated circuit, process monitor test devices are characterized as a suitable substitute. Use of test devices allows for device terminal bias conditions during irradiation to be easily controlled, and simplifies post-irradiation current-voltage characterization. To understand the full effect of ionizing radiation in the gate oxide of the n- and p- channel MOSFETs, devices were irradiated with “worst-case” bias conditions that would maximize charge yield in the gate oxides, within the constraints of realistic bias conditions of the charge pump circuit.

It is seen that the NMOS (Fig. 4.1) and PMOS (Fig. 4.2) current-voltage characteristics are minimally affected by dose after irradiation to 3.0 krad(Si). It is seen that both devices exhibit minimal buildup of oxide-trapped charge (N_{ot}) and almost no interface trap (N_{it}) accumulation in the gate oxide. Additionally, the radiation induced-voltage shifts still fall within the acceptable process model

corners (Slow-Slow and Fast-Fast) as used by circuit designers. Conversely the full circuit irradiation data illustrates the collapse of the output voltage at the same level of total dose. Based on this result, degradation of “as-drawn” transistors due to ionizing radiation was discounted as the primary mechanism leading to the collapse in the charge pump.

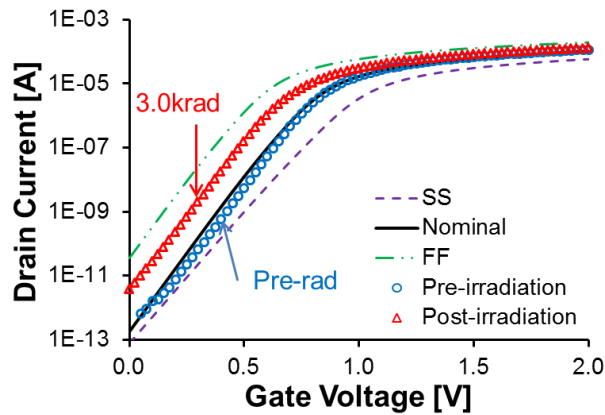


Fig. 4.1 Current-voltage characteristics for the 50/3 μ m NMOS transistor. Additionally, model corners (SS, FF and nominal) are provided for comparison.

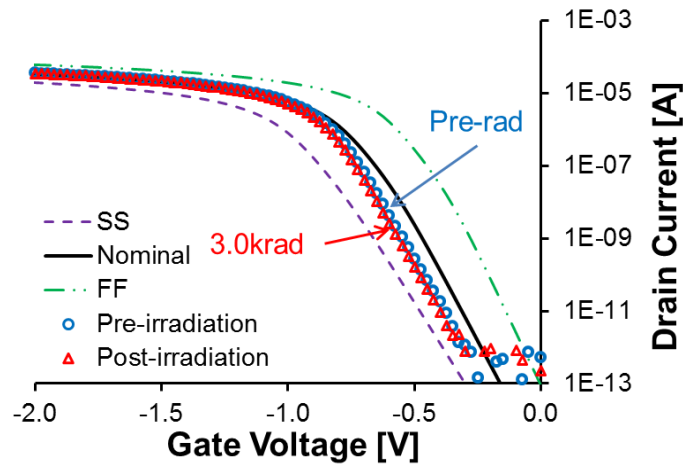


Fig. 4.2 Current-voltage characteristics for the 50/3 μ m PMOS transistor. Additionally, model corners (SS, FF and nominal) are provided for comparison.

With MOSFET test results exhibiting minimal ionizing radiation degradation in gate oxides, it is then necessary to investigate degradation in isolation oxides. Also available were process monitor field oxide (FOX)FETs, which are useful in characterizing the isolation oxides for the technology. For this technology, LOCOS is used as the isolation oxide structure. The FOXFET structure is similar to a standard MOSFET structure, with highly-doped n+ drain and sources and a single polysilicon stripe acting as a control gate. However in the FOXFET, the “gate” oxide is actually the thick LOCOS oxide giving the test device a very high threshold voltage.

By irradiating and characterizing the FOXFET, the radiation hardness and potential for inter-device leakage current under isolation oxides is known. Again, bias conditions for the FOXFET structure were chosen to maximize the charge yield by generating a high electric field in the oxide. Since the FOXFET is actually a parasitic transistor (i.e. not part of the schematic design of the circuit) the bias conditions of interest in the charge pump is actually the maximum voltage seen on device interconnect that route over the isolation oxides. By replicating this “worst-case” condition in the FOXFET, the potential for radiation induced damage in these sensitive regions is known.

Results of the n-channel FOXFET irradiation are shown in Fig. 4.3. These results illustrate significant buildup of oxide trapped charge (N_{ot}) in the LOCOS base, as seen by the large reduction in FOXFET threshold voltage. Additionally some accumulation of interface traps (N_{it}) is also shown, with minor increase in the subthreshold swing. From these results it can be determined that exposure to

ionizing radiation results in parasitic inter-device leakage currents due to isolation oxide degradation from oxide-trapped charge buildup. In fact, at the highest dose level achieved, off-state current (e.g. gate voltage=0V) is approximately 10nA. This is a multiple order of magnitude increase in comparison to the pre-irradiation characteristics. From these results, it is reasonable to infer that inter-device leakage is the primary mechanism resulting in voltage collapse in the integrated circuit. To validate this hypothesis, further work is needed via device modeling, layout investigation and circuit simulation.

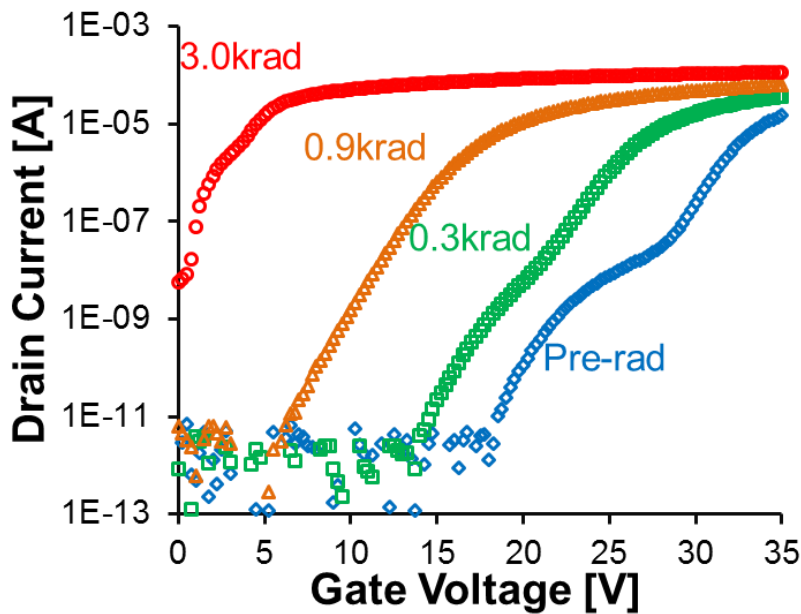


Fig. 4.3 Gate Voltage versus Drain Current for the 50/3μm n-channel FOXFET pre-irradiation and at total ionizing dose (TID) levels of 0.3k, 0.9k and 2.7krad(Si).

It is theorized that the non-linearity in the subthreshold region of three of the four dose levels shown in Fig. 4.3 are the result of a secondary parasitic FET structure, with less drive current and a lower threshold voltage, in parallel with

the primary FOXFET structure that has a greater drive current and higher threshold voltage. The radiation then alters these parallel devices at slightly different rate, causing the threshold voltage shifts toward 0V separately. However, this hypothesis was not fully validated in experiment. Subsequently, for the purposes of the failure analysis and modeling, the approximation is made that the only parasitic of concern is primary FOXFET due to the high drive current which would have a more deleterious effect on the output node. Thus the secondary parasitic is neglected in all further modeling and simulation work.

4.2 Device Modeling

To further investigate the effects of ionizing radiation on the isolation oxides, 2-D computer modeling was employed. By generating a Silvaco model of the parasitic FOXFET structure and simulating with the Radiation Effects Module (REM) within the Silvaco ATLAS simulator the experimental FOXFET results can be validated. Additionally the development of a calibrated 2-D FOXFET structure allows for the generation of additional current-voltage data suitable for compact model generation.

A 2-D TCAD structure representative of the FOXFET tested in experiment previously, with n+ drain and source regions (n+ to n+), was constructed as shown in Fig. 4.4. Inputting process technology information and adjusting the virtual FOXFET structure to match pre-irradiation data enables proper calibration of the parasitic device. Once a pre-irradiation structure is calibrated, REM was employed. Using REM inside of ATLAS allows further calibration of the 2-D

structure using FOXFET data for dose step stress levels and bias conditions achieved in experiment.

REM calibration is realized by fine-tuning radiation parameters such that the Silvaco simulation matches closely to the known experimental electrical characteristics for the pre-irradiation dataset and one of the post-irradiation datasets. Then simulating with the tuned REM parameters at remaining dose levels the model fit can be verified against experiment. By showing good agreement at all dose levels, a calibrated TCAD model is achieved. REM parameters used in simulation can be found in Table 4.1. Simulation results of the 2-D n+ to n+ FOXFET structure are compared to experimental data in Fig. 4.5.

Table 4.1 Parameters used for Radiation Effects Module (REM) simulation in Silvaco ATLAS

Radiation Effects Module (REM) Parameter	Representative Symbol	Value for Simulation
Initial Density of Hole Traps	N_t	$2.8 \times 10^{18} \text{ cm}^{-3}$
Hole Capture Cross Section for Hole Traps	σ_{tp}	$1 \times 10^{-14} \text{ cm}^2$
Hole Capture Cross Section for Electron Traps	σ_{pn}	$3 \times 10^{-12} \text{ cm}^2$
Lifetime of Hole Traps	t_p	$1 \times 10^{30} \text{ sec}$ (neglecting hole trap annealing)

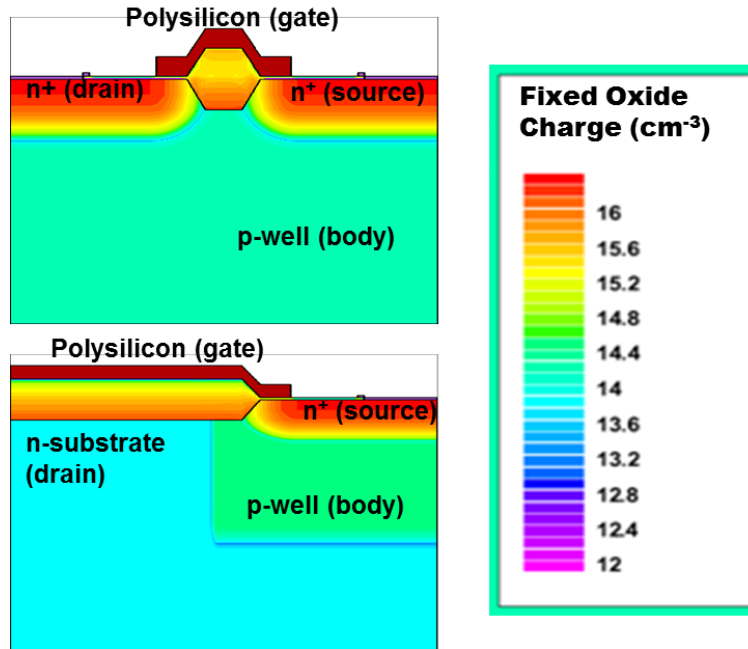


Fig. 4.4 2-D structures for the n+ to n+ (top) and the n+ to n-substrate (bottom) FOXFETs. Plot shows charge buildup modeled with REM at 0.9krad(SiO₂).

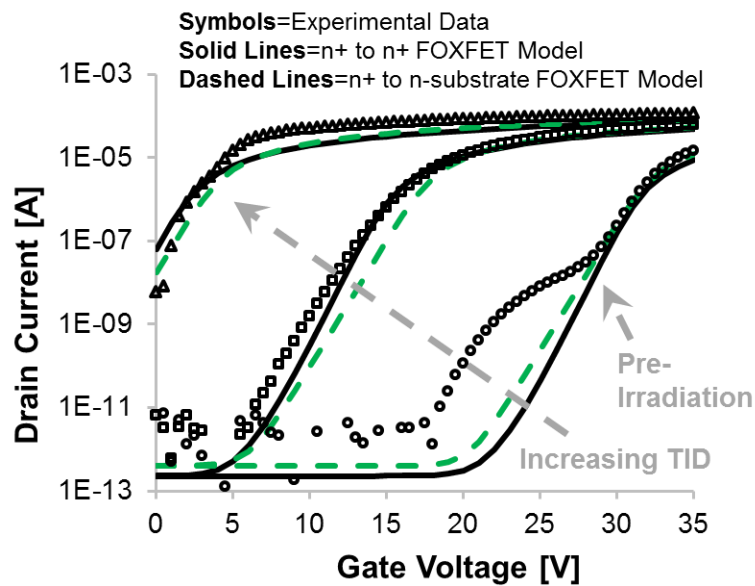


Fig. 4.5 Gate Voltage versus Drain Current for the 50/3μm n-channel FOXFET pre-irradiation and at total ionizing dose (TID) levels of 0.9k and 3.0krad(Si).

Layout investigation of the charge pump integrated circuit found that no parasitic inter-device regions exist in layout similar to that of the test FOXFET with n+ source and drains (n+ to n+). However, since the circuit was developed in a n-substrate/p-well technology, numerous FOXFET-like parasitics exist with an n-substrate drain and a n+ source. The formation of this region in layout will be discussed further in section 4.3.

Since a fully calibrated 2-D ATLAS structure with REM simulation has been achieved for the n+ to n+ FOXFET structure, it is now possible to generate a new n+ to n-substrate structure (as seen in Fig. 4.4) and assume the same REM parameters (listed in Table 4.1) controlling fixed oxide charge buildup. Generation of the new n+ to n-substrate FOXFET structure and subsequent simulation shows good agreement with experimental data and simulation performed on the n+ to n+ FOXFET, as seen in Fig. 4.5. These results confirm the use of current n+ to n+ FOXFET datasets and new n+ to n-substrate FOXFET datasets as suitable representations of the on-chip parasitic.

Achievement of a fully calibrated n+ to n-substrate FOXFET now allows accurate extraction of electrical characteristics based on the proper description of charge buildup as a function of dose. By utilizing REM again for simulation, one is able to increase the radiation response resolution across the dose range of interest. Fig. 4.6 shows the reduction threshold voltage of the n+ to n-substrate FOXFET as simulated in ATLAS using REM. Threshold voltage shifts extracted from the experimental n+ to n+ FOXFET are also plotted in Fig. 4.6. The plot indicates excellent agreement between the radiation-enabled device simulations

and experiments. Therefore, it is seen that the ATLAS structures with REM simulation serves as a capable supplement to “fill in” the FOXFET dataset at additional total dose levels, not achieved in experiment. The calibrated structure is used to generate data suitable for compact modeling at additional total dose levels of 1.16k, 1.66k, and 2.33krad(SiO₂), which was not available via experimental irradiations.

Based on the results of Fig. 4.5 and Fig. 4.6, it is reasonable to assume that electrical characteristics taken from ATLAS simulations on the generated 2-D FOXFET structure will accurately represent the actual parasitic FOXFET structure found in layout at the simulated dose. Using electrical characteristics from the 2-D TCAD simulation allows for creation of a comprehensive compact model library for the FOXFET structures as will be discussed in section 4.5.

The final BSIM3 compact models were created using data from the Silvaco REM simulations exclusively. The advantage being that compact models are more easily fit to the simulated data, and a high level of agreement is obtained between simulation and the compact models. The disadvantage to this strategy is there is exhibited mismatch in the shape of the subthreshold slope between the Silvaco simulation and experimental data. However, as mentioned previously in section 4.1, the non-linearity seen in the subthreshold slope is neglected.

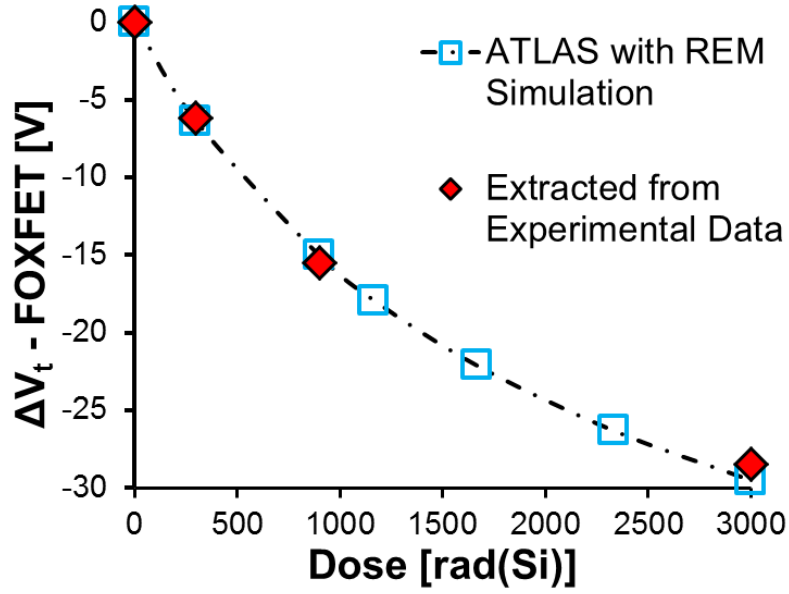


Fig. 4.6 Change in threshold voltage of the FOXFET versus applied total dose showing good agreement experimental irradiation and ATLAS simulation data.

4.3 Layout Investigation

FOXFET experimental data and modeling results illustrate significant degradation of isolation oxides due to ionizing radiation, it is then necessary to verify if integrated circuit layout conditions exist that are conducive to inter-device leakage. For such parasitic currents to occur, it is necessary to have separate n-type regions of different biases, separated by p-type region. Additionally, polysilicon routed over isolation (LOCOS) oxide above the p-type region acts as a biased gate. This would serve to aide in the inversion of the p-type region and increase radiation-induced damage in the oxide by providing vertical electric field.

Review of the charge pump and non-overlapping clock generation circuit layouts reveals numerous possible parasitic FOXFET-like structures. The

integrated circuit is designed in an n-type substrate/p-well technology, thus parasitic FOXFETs structures occur at the edges of p-wells in the design, as shown in Fig. 4.7 and Fig. 4.8.

The n- substrate, held at VDD, forms the drain while an n+ diffusion region forms the source. The n+ diffusion can be biased as low as $-3\times VDD$, depending on circuit state. The p-well, which makes up the body of the parasitic, is biased at the most negative potential (i.e., $-3\times VDD$). The gate of the parasitic is a polysilicon interconnect line, biased as high as VDD, which runs over isolation field oxide at the p- well edge. The circuit bias conditions result in a $4\times VDD$ (FOXFET polysilicon gate to p-well body) voltage across the field oxide, providing high electric field to enhance TID degradation. This worst case bias condition was replicated in the individual PM FOXFET irradiation bias conditions as described in the experimental details.

This type of parasitic FET structure is found to occur 51 times within the charge pump and non-overlapping clock generation circuitry, thus it is reasonable to assume radiation-enabled activation of these parasitic would be the root cause of failure. By simulating circuit operation with the addition of the parasitic FOXFETs back-annotated into the schematic, this conclusion can be confirmed.

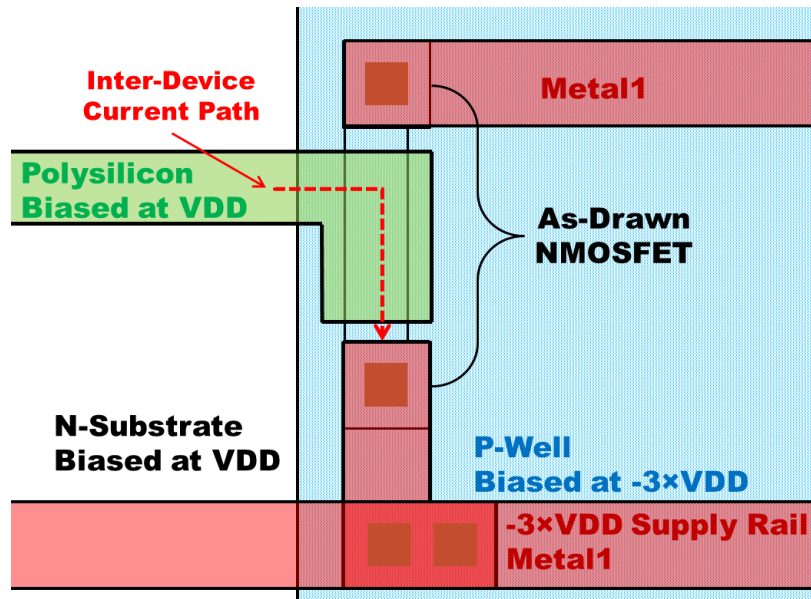


Fig. 4.7 Layout example of the parasitic FET structure with inter-device current path from the n-substrate to the n+ diffusion.

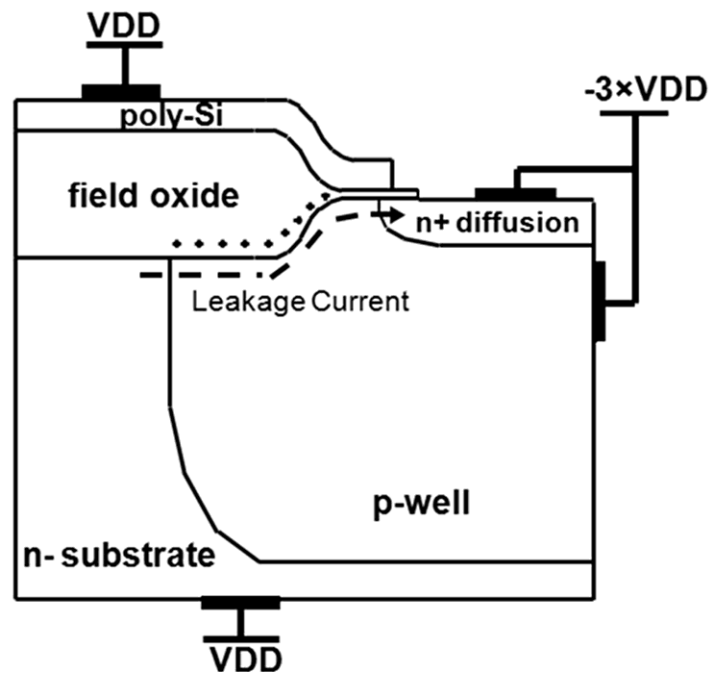


Fig. 4.8 Cross-section of the parasitic FOXFET structure occurring in layout. Also indicated are typical bias configuration for each region.

4.4 Simple Circuit Simulation

Examination of the circuit schematic and layout of the dual charge pump design revealed the existence of numerous potential inter-device parasitic leakage paths under isolation oxides, with regions in the layout similar to that of the FOXFET test structure. Among the most critical potential paths are those formed between the fixed VDD supply voltage and the charge pump floating $-3\times VDD$ output. Leakage current between these two nodes will charge the output node, thereby causing the voltage to collapse. This leakage path is shown schematically in Fig. 4.9.

To analyze the circuit-level effects of leakage from VDD to the $-3\times VDD$ output of the charge pump, simulations were performed with a parasitic leakage source between those nodes. Fig. 4.10 shows how the charge pump output voltage collapses as a result of the increased leakage current. From the graph it is evident that, as leakage increases past approximately $1\ \mu A$, the output voltage begins to drop significantly. The output voltage reduces almost entirely to 0 V once the total parasitic current reaches $100\ \mu A$. The collapse exhibited with increasing leakage current can be considered a full failure of the charge pump circuit. If we consider that the leakage current is the summation of contributions from numerous parasitic inter-device FOXFET leakage currents, it can be understood that the activation of these devices would cause the output voltage collapse.

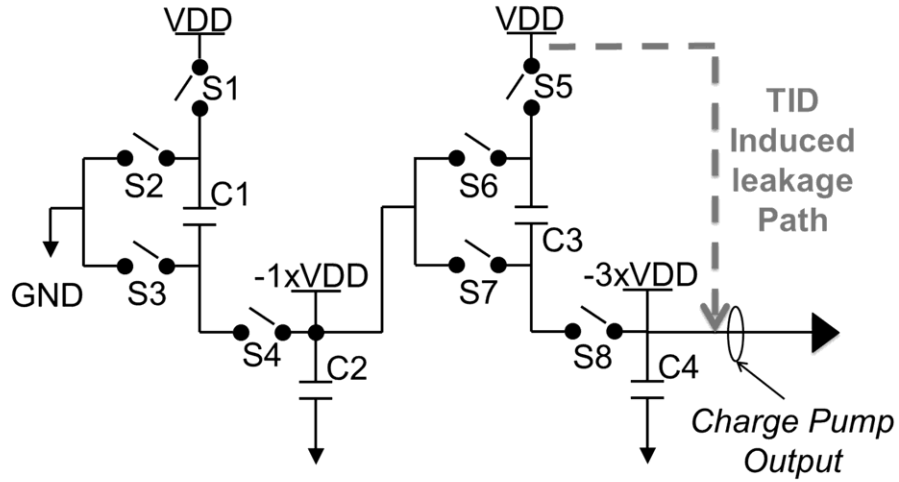


Fig. 4.9 Simplified charge pump schematic illustrating the radiation induced leakage path associated with the activation of parasitic FOXFET devices.

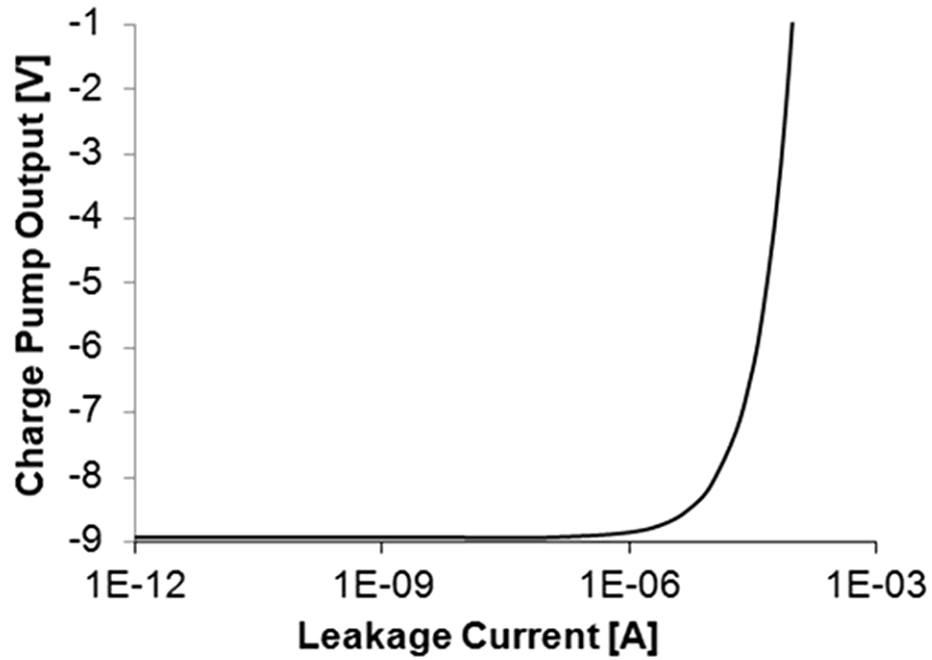


Fig. 4.10 Simulation of -3xVDD charge pump output reduction due to radiation as modeled by leakage current from the VDD to -3xVDD node.

4.5 Compact Model Library

In order to implement the radiation-enabled simulation strategy outlined in Chapter 3, it is necessary to generate a radiation-enabled compact model library. Since the compact model selected for simulation is equivalent to selecting a dose level for our methodology, multiple compact models for the same device type must be generated. With the experimental and modeling results, it is determined that inter-device leakage currents cause the voltage collapse. To capture this in simulation, we can generate compact models of the parasitic FOXFET structure and implement it into schematic.

Compact models for the FOXFET parasitic device were generated in the BSIM3v3 compact modeling framework. Using the combined dataset from experimental testing and computer modeling, seven separate compact models were created representing total dose exposure levels of 0k (pre-irradiation), 0.30k, 0.90k, 1.16k, 1.66k, 2.33k and 3.00krad(SiO_2). Implementing each compact model to represent the parasitic devices in allows for effective full circuit simulation at each dose step listed.

4.6 Radiation Enabled Circuit Simulation

To recreate the voltage collapse failure mechanism seen in experiment, a test bench was developed to allow for radiation-enabled simulation. The test bench included the original charge pump and non-overlapping clock generation circuits as well as dummy capacitive and resistive loads to represent the rest of the integrated circuit for which the pumps supply. Also, the 51 parasitic FOXFETs

had to be back-annotated into schematic based the results of the layout investigation.

By successive Cadence AMS simulations of the charge pump circuitry with back-annotated parasitic FOXFETs at all of the dose stress levels for which the compact models were created, we are now able to model the complete charge pump response with increasing dose. Fig. 4.11 illustrates the charge pump output voltage simulated with parasitic FOXFETs back annotated. As seen in the simulation results, as we model increased total dose (interchange FOXFET compact models), the output voltage collapses in a similar fashion as that observed in experiment.

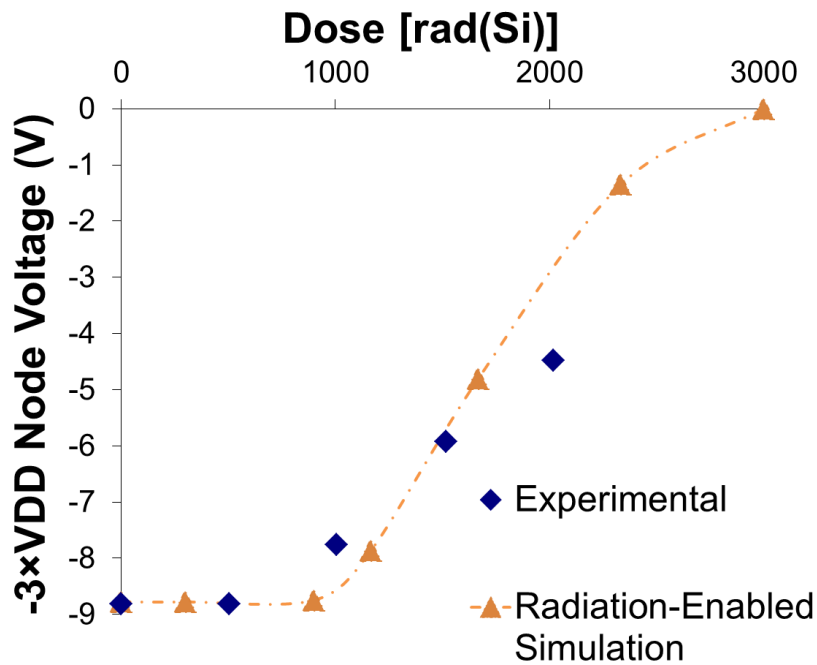


Fig. 4.11 Radiation-enabled circuit simulation of the charge pump output voltage ($-3 \times V_{DD}$) compared against experimental test data.

One notable consideration to understand when comparing experiment to simulation in Fig. 4.11 is that the parasitic FOXFETs in the charge pump IC have irradiation biases controlled internally by the circuit state conditions during irradiation. This is important because, as we apply dose and begin to collapse the output voltage, the irradiation biases (specifically the p-well voltage of $-3\times VDD$) of the FOXFETs are reduced. Thus the FOXFETs in the charge pump experimental data encounter a dynamic bias condition during irradiation. This decreasing bias leads to reduced damage in the FOXFET, somewhat slowing the collapse of the output.

In the presented radiation enabled circuit simulation approach, the test device dataset along with Silvaco simulation is used for compact model creation, with a particular compact model selected for each dose point in the circuit simulation. These datasets taken on individual FOXFET irradiations are taken using a static bias during irradiation as specified in the experimental details section. In individual device testing external supplies fix bias conditions. Correlating this information with the known bias dependency of oxide trapped charge buildup, it is expected that the modeled/simulated damage would be greater than that of the full charge pump irradiation due to reduction in irradiation bias at upper dose levels of the experiment. This correlation is illustrated in the results of Fig. 4.11, as simulated collapse in the output voltage is more severe than that of the experiment at the higher total exposure levels.

The ability to accurately predict, or in the case of this analysis re-create, the radiation response of a given circuit is valuable in attempts at front-end mitigation

of ionizing radiation effects. By analyzing the results of a radiation-enabled simulation, targeted and measured design changes can be implemented as part of a radiation hardening by design strategy within the context of other medical device design goals.

CHAPTER 5 CONCLUSIONS AND FUTURE WORK

5.1 Summary and Conclusions

Implantable medical device technology will continue to advance in its complexity and grow as a prevalent option in disease management practices. Furthermore, the likelihood of patient exposure to ionizing radiation will remain typical during cancer therapies and other standard medical procedures. As such, ionizing radiation effects will continue to be a serious threat to device reliability and lifetime. To effectively understand and diminish possible device degradation, device manufactures must develop mitigation methods that are implemented into their front-end design process.

This thesis presents a methodology to examine radiation effects of any integrated circuit through test device characterization, computer modeling and full circuit simulation. The methodology is validated by the discovery of the root cause failure for a charge pump circuit case study. It is concluded that the output voltage collapse with increasing total dose is the result of inter-device leakage currents under isolation oxides onto the output node. This is validated by radiation-enabled circuit simulation that recreates the failure mode seen in experiment.

Implementation of radiation-enabled simulation during product development can allow for measured increases in radiation tolerance to be gained through radiation hardening by design strategies. In the case of the charge pump, all design and development work is complete, so hardening of the design is not an option. However, knowledge gained through the failure analysis process and

radiation-enabled simulation results are applicable to new designs and revisions in the future.

5.2 *Future Work*

Possibilities for expansion of this work include:

- Apply and refine methodology in other circuits and more advanced technologies.
- Implement methodologies into front-end design process to harden new circuit designs.
- Develop tools for circuit simulation that can quickly and automatically select between radiation enabled compact models for the purposes of radiation enabled simulation.
- Create experimental testing and modeling studies to investigate the degradation of oxides under switched bias conditions. Currently models represent damage in test devices at static bias conditions, while integrated circuit field exposures occur during normal operation with dynamic electric field conditions.
- Explore parasitic FOXFETs with irregular gates to develop analytical model that accurately describes a device width and length for use in circuit simulations.

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