Hierarchical Fault Response Modeling of Analog/RF Circuits

by

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ABSTRACT

In this thesis two methodologies have been proposed for evaluating the fault response of analog/RF circuits. These proposed approaches are used to evaluate the response of the faulty circuit in terms of specifications/measurements. Faulty response can be used to evaluate important test metrics like fail probability, fault coverage and yield coverage of given measurements under process variations. Once the models for faulty and fault free circuit are generated, one needs to perform Monte Carlo sampling (as opposed to Monte Carlo simulations) to compute these statistical parameters with high accuracy. The first method is based on adaptively determining the order of the model based on the error budget in terms of computing the statistical metrics and position of the threshold(s) to decide how precisely necessary models need to be extracted. In the second method, using hierarchy in process variations a hybrid of heuristics and localized linear models have been proposed. Experiments on LNA and Mixer using the adaptive model order selection procedure can reduce the number of necessary simulations by 7.54x and 7.03x respectively in the computation of fail probability for an error budget of 2%. Experiments on LNA using the hybrid approach can reduce the number of necessary simulations by 21.9x and 17x for four and six output parameters cases for improved accuracy in test statistics estimation.

ACKNOWLEDGMENTS

Although this thesis book lists only one author, in reality the ideas it molds together were contributed and refined by many extraordinarily insightful colleagues. My first thanks go to the almighty for directing me to Prof. Sule Ozev to conduct this masters research. On most days I leave her office after the meeting wondering if I have really got the benefit of my 18 years of science education. My interactions with her have proved time and again that learning is a continuous process and this gives me great deal of enthusiasm to delve deep into new and obscure topics. I thank her for all the guidance during this enduring period of research. I would also like to thank Prof. Yu(Kevin)Cao and Prof. Jennifer Blain Christen for promptly agreeing to serve on the defense committee.

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Chapter 1

INTRODUCTION

There is a continuous push for reducing the test time/cost and test development time of analog circuits. Over the years, a plethora of approaches have been proposed in the literature to automatically generate test measurements [1-2], to find alternate ways of measuring/guaranteeing the specifications [3-4], to reduce the test set [5-7], or to conduct measurements on-chip [8-9]. However once one deviates from full specification testing, it is essential that the new test technique be evaluated under process variations and fault scenarios.

With such a diverse variety of test approaches, an efficient and accurate way of evaluating the fault response under process variations is needed. Existing fault simulation approaches require injecting the faults into the circuit specifications and simulating the resulting circuit to evaluate the fault response [2, 10-11]. With the continuous nature of circuit parameters and presence of process variations, each fault simulation takes on a statistical nature and may require statistical analysis. One easy way of conducting this statistical analysis is to use Monte-Carlo simulations for each fault, which is computationally too expensive.

A. Problem Statement

Ideally each circuit instance can be classified as passing/failing by making a decision on the process parameters without the need for circuit

simulations. Since, circuit response is a complex non-linear function, making such an evaluation not possible. Our goal is to make this decision with the least possible computational burden.

The goal of the fault simulation is to statistically evaluate the response of a list of faults under a set of given test stimuli. These responses are then compared with test limits to determine the likelihood of a faulty circuit passing/failing. These statistical analysis are used to predict important test metrics, such as fault coverage, defect parts per million (DPPM), and yield loss. Since there are many faults in the circuit and they have to be evaluated for various distinct input conditions, fault simulation is computationally very expensive. This computational cost has been a major burden preventing analog fault based simulations from becoming an industry practice. This work aims at developing computationally efficient as well as accurate methods for analog fault simulation.

B. Prior Work

In order to tackle the problem of computational complexity of fault simulation, simple circuit approximations, such as linear modeling [10, 12-13] and worst case approximation [14] have been proposed. In [14], the authors present a technique for quickly estimating the worst case tolerance band of a given circuit. While this technique provides useful insight during the design optimization process, it tends to overestimate the bounds on response parameters and provides no information about the nature of the

distribution, which is needed to compute the test metrics. In [10], the authors make use of a linear modeling approach for the circuit and use analytical relations to compute a Gaussian approximation for the response distribution. While computationally efficient, this technique may result in larger errors, particularly when the circuit behavior is highly non-linear. In [15], the authors extend these models to include quadratic modeling, only in the diagonal elements.

A common thread in prior work is to start from a particular modeling perspective (worst case, linear and quadratic) and optimize on computation time [14-17]. However, in such approaches, the final accuracy is dictated bottom up, with no way of controlling or trading it off with computational complexity. One has to take the final goal of the modeling process into account when deciding what form of modeling needs to be used. Stratigopoulous *et. al* [31] proposed a method to evaluate the joint probability density function (JPDF) of specifications based on the adaptive kernel density estimation. Once JPDF of the specifications are evaluated, we need to simply do a Monte Carlo sampling from the JPDF. The downside with this technique is sampling from a complex JPDF is inefficient especially when the number of specifications are large. The final goal of all these techniques (including the one in this thesis) is to compute various test metrics such as fault coverage, yield coverage and detectability etc [18].

C. Proposed techniques in a nutshell

In this thesis, we rely on polynomial modeling of the output response of the faulty and the fault free circuits to enable fault simulation. In order to judiciously use simulations, we present two methods. The first technique basically follows a top-down approach for constructing the model. We start from the error budget on the test metric and determine the minimum model order that will keep the overall error within this budget. We perform a certain number of simulations and check if a linear model would meet the accuracy requirement. If not, we consider a second order model and check for its suitability. If the second order model does not satisfy the error budget, we may need to resort to higher order modeling or Monte Carlo simulations.

In order to save on simulation time for second order models, we propose a procedure which takes the error budget and the threshold(s) into account to approximately estimate the coefficients of the second order model with O(n) simulations. This procedure regresses the response of significant coefficients, and non significant terms are derived from solving systems of linear equations. Solving this equation yields a set of solution vectors. A solution set selection methodology is used to choose the non-significant terms that would best fit the model. Monte-Carlo sampling and analytical computation, as opposed to Monte-Carlo simulations, can be used to calculate important test metrics, such as fault coverage and fail probability.

However, even with non-linear models, it is possible that errors in computing certain test metrics such as DPPM may not meet the industry standard. As an example let us assume that error in computing the probability of test escape for a circuit is 1% and the probability of having fault in the circuit is 10%. This results in an uncertainty of 1000 in the estimated DPPM which is not acceptable.

In our second method, we make an effort to reduce this uncertainty to allowable proportions by constructing localized linear models. We exploit the hierarchical nature of process variations and use Design of Experiments (DOE) sampling strategy for high level variations. We then localize small random variations around the important samples stemming from high level variations. The method follows a two phase procedure where during the first phase the circuits are classified into three sections namely certainly passing, certainly failing and ambiguous. Initially, we use heuristics based on levels for DOE to perform the initial evaluation of the status of the circuit instances. In the second phase, we try to reduce the instances in the ambiguous lot by constructing linear models around certain input regions. Since we are constructing first order models over a localized region in input space, the accuracy is guaranteed to be much better, unlike in the previous method where we model the response as a function of entire input space. Guard bands around specification thresholds are invoked to improve the accuracy of the status evaluation procedure.

The major contributions of the first method in this thesis are the top-down approach based on the accuracy requirement in computing the test metrics, adaptive model order selection based on the threshold(s), the error budget requirement, and a mathematical procedure for approximating a second order model using O(n) simulations. The contributions of the second method include a heuristic approach based on Design of Experiments to classify the circuits in a coarse manner, construction of first order models around localized input regions both eventually lead to better accuracy in test metric computation.

Figures 1, 2 and 3 illustrate the basic difference between our approaches when compared with the traditional Monte-Carlo simulations. Figure 1 shows the traditional Monte Carlo approach wherein the circuit instances are fed to a simulation engine to obtain the response distribution. Figure 2 displays the Monte-Carlo sampling procedure wherein we perform few number of Monte-Carlo simulations to model the response. Once we derive the model coefficients, we simply do a Monte Carlo sampling (as opposed to Monte Carlo simulation) to compute the approximate response distribution. Figure 3 illustrates a modified Monte Carlo sampling procedure wherein we use DOE and heuristics to do a coarse evaluation of the test statistics and fine tune the accuracy based on modeling and Monte Carlo sampling.

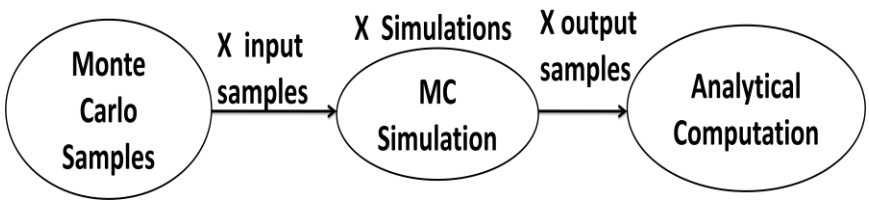

Fig. 1. Traditional Monte Carlo Analysis

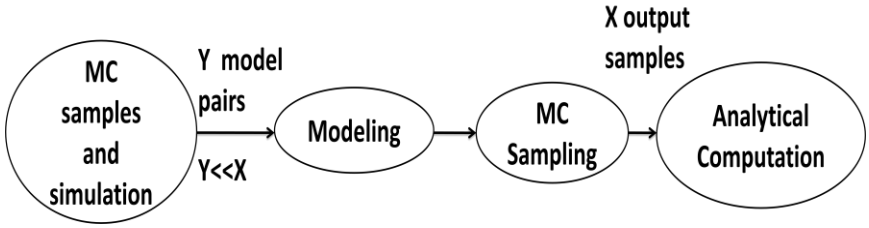

Fig. 2. Monte Carlo sampling based approach

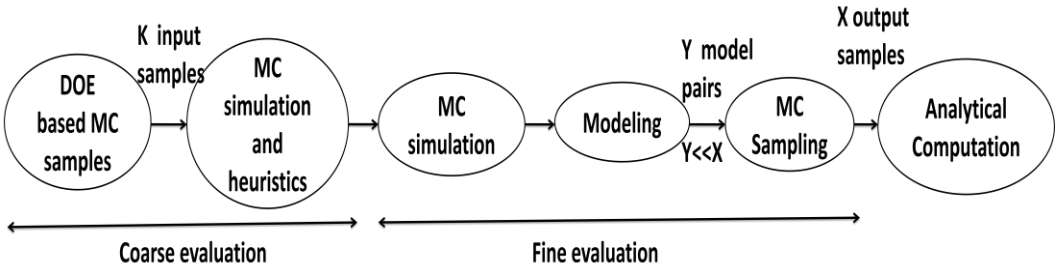

Fig. 3. Modified Monte Carlo sampling based approach

D. Thesis Outline

Chapter II discusses the importance of computing test metrics and also explains the tradeoff between choosing model order and accuracy. Chapter III deals with non-linear coefficient approximation and outlines the advantages of using robust regression techniques over the traditional least squares method. Chapter IV lists the proposed top down approach for fault response evaluation. Then in chapter V, we propose an improved method that uses DOE, heuristics and hierarchy in process variations to evaluate the

test statistics with better accuracy. Chapter VI proves the effectiveness of our proposed approaches with help of test circuits simulated in ADS. Chapter VII concludes the thesis with summary and future directions for research.

Chapter 2

COMPUTATION OF TEST METRICS

We develop our modeling approach with the specific goal of computing various test metrics for analog/RF circuits. In general, most test metrics such as fault and yield coverage [15], pass/fail probability and detectability [19-20] are statistical in nature due to the effect of process variations.

A. Definition of Test Metrics for Analog circuits

Digital manufacturing test quality has been assessed by the definition of quantitative parameters such as fault coverage and test escape. Unfortunately, the direct application of these metrics (defined for digital circuits) to the analog domain bears little hope. This is due to the statistical and continuous nature of fault and fault responses, as well as the fact that each fault may not be equally likely. As a result in analog domain, a statistical framework for fault response evaluation is necessary.

In the analog domain, faults can be classified as catastrophic faults or parametric faults. Catastrophic faults cause a drastic failure at the fault location changing the circuit structure. Examples are opens and shorts in interconnects. Parametric faults are unexpectedly high deviations in circuit parameters such as width of the transistor or threshold voltage. Typically, catastrophic faults cause a complete failure in the circuit functionality and are easy to classify without the need to resort to statistical simulations. However, parametric faults are much harder to classify since in most cases the circuit still functions, but with

potentially degraded specifications. Parametric faults may stem from direct physical defects, such as an open in a finger of the transistor, or may stem from unexpected local or global process variations such as spike in the threshold voltage. Existence of a fault, however, does not necessarily mean the circuit will fail its specifications. Similarly, a fault-free circuit does not necessarily satisfy all of its specifications due to process variations. The test metrics that we use are based on the specifications of the circuit:

- **Yield**: It is defined as ratio of number of devices satisfying all the specifications(good devices) to the total number of manufactured devices

$$\boldsymbol{Yield} = \frac{\boldsymbol{\#devices\ passing\ all\ the\ specifications}}{\boldsymbol{\#manufactured\ devices}} \tag{1}$$

  Figure 4 shows the response distribution for a two parameter case. Using the position of both the thresholds yield can be computed by integrating the suitable area under the curve.

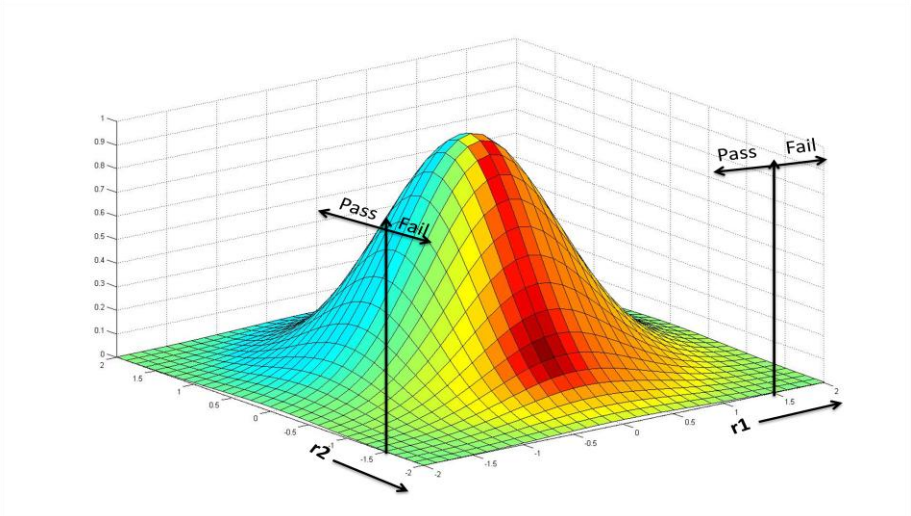

Fig. 4. Yield for a two parameter case

- **Yield Loss**: It is defined as the ratio of the number of good devices failing the test to the total number of good devices

$$\textbf{\textit{Yield Loss}} = \frac{\textbf{\textit{\# good devices failing the test}}}{\textbf{\textit{\#good devices}}} \tag{2}$$

Ideally, we would expect yield loss of 0%. Conceptually, yield coverage and yield loss depend on the statistical distribution of circuit specifications, the errors made in the measurement or estimation of the specifications, and the limits on the specification. These concepts are illustrated in Figure 5. The red curve is the actual distribution we would expect for a response parameter *r*. Due to accuracy limitations in the measuring equipment and inconsistencies in the load board circuitry, we obtain a blue distribution. Yield loss is the difference in the area past the specification limit.

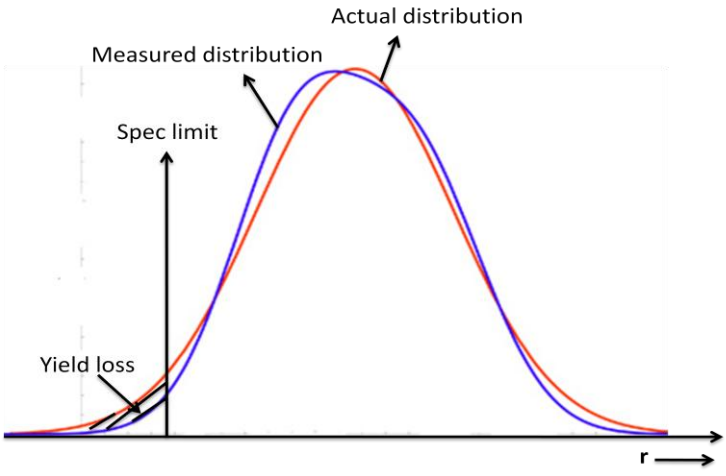

Fig. 5. Yield loss due to a particular parameter

- **Test Escape**: It is defined as the number of bad devices passing the test to the total number of faulty devices.

$$\textbf{\textit{Test escape}} = \frac{\textbf{\textit{\# bad devices passing the test}}}{\textbf{\textit{\#bad devices}}} \tag{3}$$

This is an important measure from an economic and customer perspective. Ideally we would expect a test escape of 0%. However, due to incomplete or indirect testing some level of test escape is inevitable.

- **Fail Probability**: It is the ratio of the number of devices failing a particular specification to the number of devices in the distribution.

$$\textbf{\textit{Fail probability}} = \frac{\textbf{\textit{\# devices failing a particular specification}}}{\textbf{\textit{\#devices in the distribution}}} \tag{4}$$

It is generally defined for a particular circuit structure; could be faulty or fault free. Figure 6 illustrates fail probability computation for a parametric fault scenario.

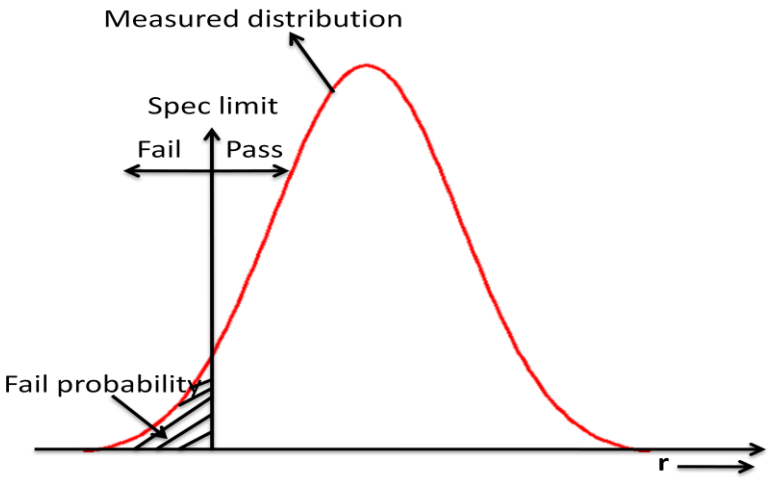

Fig. 6. Fail probability for a particular specification

- **Defective parts per million (DPPM)**: It is defined as the average number of defects in an average production run scaled by one million. It can be calculated using the following formula.

$$\boldsymbol{DPPM = \frac{\#defective\ devices}{\#shipped\ devices} * 10^6} \tag{5}$$

This is an extremely important indicator of the quality of the production line. Different applications require different DPPM levels based on their criticality. For example, applications related to aerospace, automobiles and medical require near 0 DPPM levels, while other applications which are not very critical such as garage door openers can tolerate higher DPPM levels.

B. Process variations and Test Metrics

Due to process variations, the evaluation of test statistics may depend on how the rest of the parameters will play out as illustrated in Figure 6. It shows the gain histogram of an LNA when the fault is injected in the width of the input transistor. The fault coverage of this measurement/threshold pair for the injected fault is the probability that the response falls to the left of the threshold. Thus, the first step in computing this (and many other similar) test metrics is to approximate the statistical distribution of the faulty circuit response. The next step is to compare it with the pass/fail threshold and find the probability of pass or fail.

It is clear that in order to compute the test metric accurately, one has to estimate the distribution of the faulty response accurately. However, there is another factor to take into account. For the example in Figure 7, any error in estimating the distribution will reflect into the fault coverage computation. Suppose that the threshold line was further away from the faulty circuit distribution. Then, the error in estimating the distribution would have a smaller impact on the overall accuracy. Thus, the accuracy with which we need to approximate the circuit behavior is not a pre-determined fixed value and this effect should be taken into account when constructing a model.

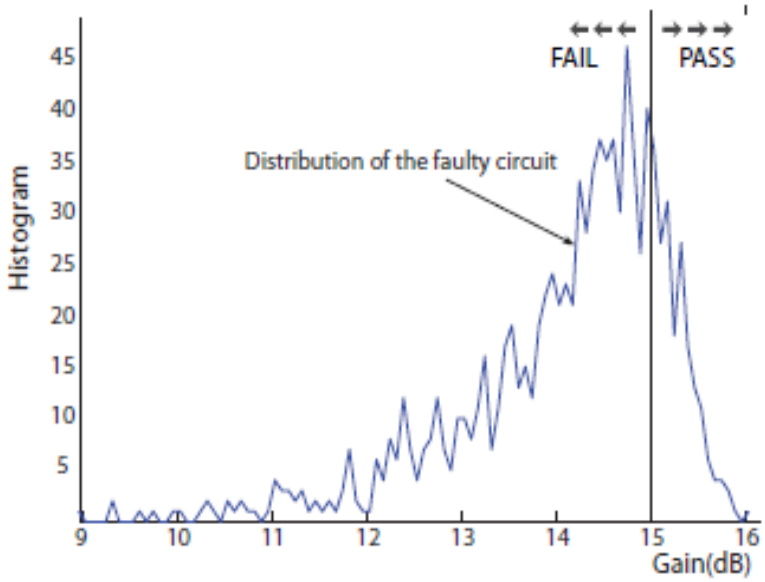

Fig. 7. Distribution of faulty LNA

C. Why Non linear models may be necessary?

While the order of the model should be dictated by the desired final accuracy, we first would like to show why non-linear models are generally needed to achieve reasonable accuracy. Modeling circuit behavior is a

challenge due to the non-linear nature of analog circuits and the implicit relations that arise from the circuit equations. A common thread in modeling is therefore to use a known polynomial approximation for the circuit behavior, which is a non-linear function of unknown form. Thanks to the results proposed by Taylor, polynomial models are effective to approximate any generic function as long as the deviation from the fixed point is not excessive.

The simplest form of polynomial modeling is to use a linear approximation, which is also called as *sensitivity analysis*. It has been used as a first-hand analysis tool for many problems ranging from circuit optimization to fault response analysis [10, 21]. Linear models basically linearize the function around the point of interest, thus approximating the neighborhood by a straight line. As the process variations increase and the processing technology are pushed towards its limits, the circuit response becomes highly non-linear when deviations in process and layout parameters are taken into account.

A linear model would work well only if the nominal point of the process/layout parameter is on a stable part of the curve that represents the overall function. However, this may not be true especially when process and layout parameters are taken into consideration. As an example, Figure 8 shows the response of noise figure versus transistor length for an amplifier. It illustrates how a higher order model approximates the response better

than a simple linear model around the region spanned by the process variations.

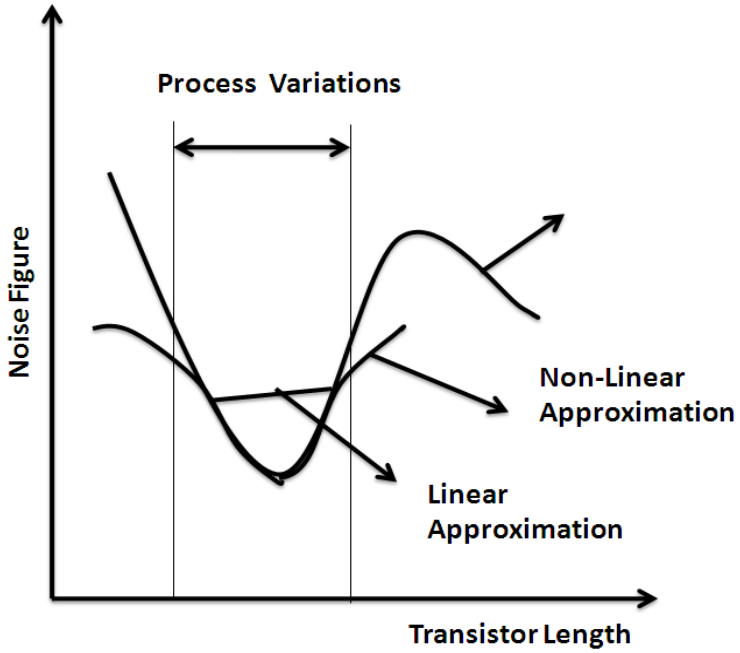

Fig. 8. Linear and higher order models under process variations

Perhaps a more telling illustration is based on how linear models impact the distribution of the faulty circuit response. Figures 8 and 9 represent the gain distribution under a fault injection scenario for an LNA. The distance between the vertical lines represent the shift in the mean. Figure 9 compares the gain distribution obtained through Monte Carlo Simulations and the distribution obtained through a first order approximation. It is clear that when the decision threshold is not far from this distribution, we may incur a large error in the computation of the test metric. Most of this error stems from the mean, as mean errors shift the complete distribution and thus detrimental to achievable accuracy. In Figure

9, the mean difference between the two curves is 6%. Comparatively, Figure 10 shows the distributions obtained by SPICE and through second order modeling. While there is still some mismatch in the histogram, the mean error is much smaller. The mean error in this case was found to be only 0.6%. In comparison, we see that the second order model always performs better than its linear counterpart. If this accuracy is not satisfactory we need to resort to higher order modeling.

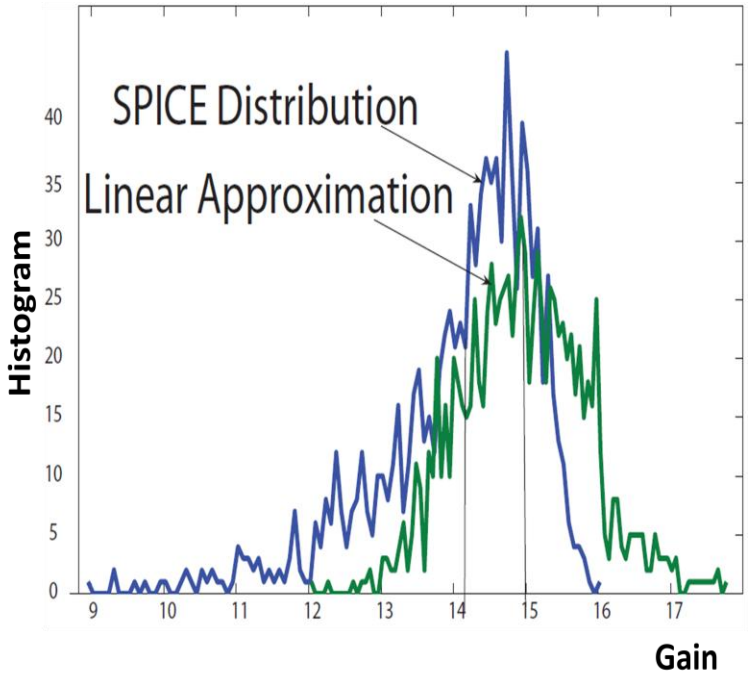

Fig. 9. Error in first order modeling

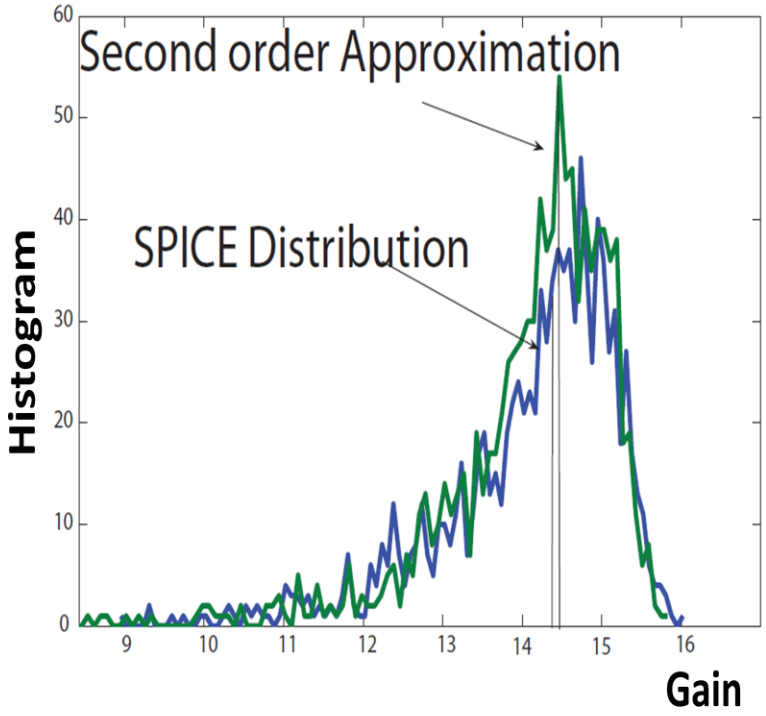

Fig. 10. Error in second order modeling

D. Choosing the optimal order

It is obvious that using higher order polynomials for circuit behavior approximation provides added accuracy benefits. Nonetheless, the computational cost of higher order polynomials grow exponentially as the order grows. Therefore, it is essential that one selects the lowest order of polynomial approximation that provides the desired level of accuracy.

Choosing an optimal order with the careful consideration of the trade-off between accuracy and simulation overhead is very important. We will address the issue of choosing an optimal order below. Consider the following arguments,

- A model of order p would be more accurate than a model of order m, where $m < p$
- Evaluation of a model of order m would require order of $O(n^m)$ simulations as against $O(n^p)$ for a model of order p

From these arguments it is obvious that it is impossible to have a highly accurate model and a reduced simulation overhead simultaneously. To evaluate this trade-off, one needs to take into consideration the accuracy boost in the response and the number of simulations that would be required to construct the model. Figures 11 and 12 highlight the standard deviation of the modeling error and the corresponding simulation overhead for evaluating the response of an analog/RF circuit.

From Figure 11, we observe that the improvement in the accuracy is considerable when we move from a linear to a second order model. But thereafter, moving to a third order model is a case of diminishing returns, since the boost in accuracy is not worth the extra simulation overhead. Indeed, it may be computationally more efficient to conduct a full blown Monte-Carlo simulation compared to the extraction of a third order model. Thus, we restrict ourselves to second order modeling and revert to Monte-Carlo simulations if the overall accuracy is not adequate. From Figure 11, we also observe that the number of simulations to completely evaluate a second order model is in the order of $O(n^2)$ where n is the number of input parameters. We make an effort to evaluate an approximate second order

model using reduced number of simulations *ie.,* of O(n) as illustrated in Figure 12. In the next section, we describe some important mathematical background required for our coefficient estimation algorithm.

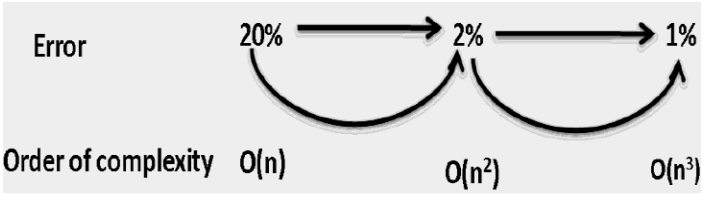

Fig. 11. Computational cost and accuracy trends with increase in model order

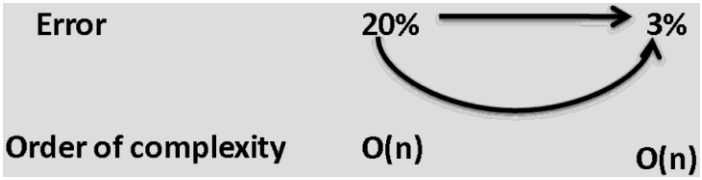

Fig. 12. Our goal is to compute the second order model with reasonable accuracy without boosting the computational cost

Chapter 3

NON-LINEAR COEFFICIENTS APPROXIMATION

Reducing the order of a highly non-linear function by fitting higher order models (predominantly second order) around a specific region in the input space are of interest to the modeling and optimization community [22-23].

The input region around which a model is valid, is often quantified by what is called as the trust region radius which is a common nomenclature in optimization problems. These problem solving techniques make use of the second order multi-variable Taylor series expansion around the point of interest to evaluate the model. One of the classical ways of fitting a model is through regression. Instead of using the normal least squares regression (LS), we resort to robust regression techniques such as the least median of squares (LMS) or the Least Trimmed Squares (LTS). LMS and LTS are resistant to the presence of outliers as they minimize a different cost function than its LS counterparts. In the next few sections, we explain these techniques and justify the need for using them as against the traditional Least squares approach.

A. Concept of Robust regression

Robust regression refers to a class of methods proposed for fitting models that are resistant to outliers. In a statistical sense, the outlier is an observation that lies at an abnormal distance from other values in a random sample from the population. Outlier may occur due to noise in the observation or due to highly non-linear nature of the model.

In multivariate regression, the input variables are (x_{i1},...x_{ip}) where *i* runs from 1 to *n*, and *n* is the number of variables that lie in a space with *p* dimensions (which is sometimes called the factor space). A leverage point is defined as a point (x_{k1},...,x_{kp}, y_k) for which (x_{k1},...,x_{kp}) is outlying with respect to (x_{i1},...x_{ip}) in the data set. One cannot detect the outliers by analyzing the residual of the least squares this is since the residuals are sensitive to leverage points which will lead to misclassification of the good and the bad points [24]. A special class of robust modeling technique called the Reweighted least squares (RLS) identifies the outliers using the robust regression techniques, and applies LS method on the "clean" samples obtained. This kind of modeling technique would be more suitable in the analog domain because of the highly non-linear nature of its response. Since our understanding of the faulty circuit response under process variations for different operating conditions is not very clear, it would be best to leave the outlier classification problem to the discretion of the algorithm.

B. Robust regression estimators

Roussew proposed two robust regression estimators namely the Least Median of Squares (LMS) and the Least Trimmed Squares (LTS). He modified the cost function in the Least squares technique from

$$\arg_\theta \min \sum_i r_i^2 \tag{9}$$

to

$$\arg_\theta \min median(r_i^2) \tag{10}$$

where r_i^2 are the squared residuals, yielding the Least median of squares (LMS) estimator. The estimator is very robust with respect to outliers in y as well as in **x**. Unfortunately, the LMS performs poorly from the point of view of asymptotic efficiency. To remedy this problem another estimator called the Least trimmed squares (LTS) has been proposed [24].

$$\arg_\theta \min \sum_{i=1}^{h} (r^2)_{i:n} \tag{11}$$

where $(r^2)_{1:n} \leq \ldots \leq (r^2)_{n:n}$ are the ordered squared residuals.

In order to improve the crude LTS and LMS solutions, he proposed another scheme called the Reweighted least squares (RLS) whose estimator is given by

$$\arg_\theta \min \sum_i w_i r_i^2 \tag{12}$$

where,

$$w_i = \begin{cases} 1 & \text{if} |r_i/\sigma| \leq 2.5, \\ 0 & \text{if} |r_i/\sigma| \geq 2.5, . \end{cases} \tag{13}$$

In case of LMS,

$$\sigma = C1.\sqrt{med_i(r_i^2)} \tag{14}$$

In case of LTS,

$$\sigma = C2.\sqrt{(1/n)\sum_{i=1}^{h} r^2_{(i:n)}} \tag{15}$$

where C1 and C2 are correction factors. The value of 2.5 used in equation 13 is not rigid [24]; it is just a measure for classifying the outliers.

Figure 13 shows the linear fit obtained through LS and the LTS techniques for a certain set of observations. We see that the LS fit is more biased towards certain points (leverage points) in an attempt to minimize the squared sum of the residuals, eventually leading to a poor fit. On the other hand the LTS technique fits a linear model completely ignoring the outliers. It has been proven that the breakdown point of robust estimators to be 50% [25]. Breakdown point is defined as the maximum allowable contamination in the sample set. Theoretical maximum of breakdown point cannot be more than 50% since beyond that there won't be a distinction between good and bad points.

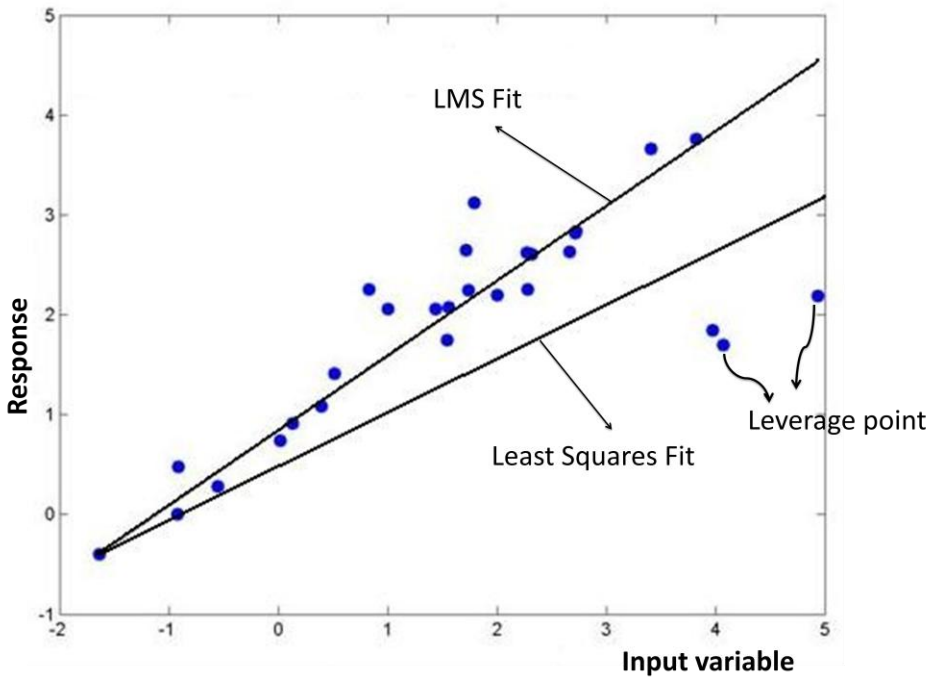

Fig. 13. Least median of squares Vs Least squares

Chapter 4

ADPATIVE MODEL ORDER SELECTION

The goal of our approach is to be able to approximate statistical test metrics such as detectability, fault coverage, fail probability.

A. Top down approach for Error Budget estimation

An interesting question in the modeling process is what approximation accuracy is indeed acceptable. Unfortunately, there is no generic answer to this question. The required approximation accuracy depends on three factors:

- The desired accuracy of computing the test metrics, such as the fault coverage, yield loss, DPPM etc.
- The distance between the threshold line and the mean of the statistical distribution
- The standard deviation of the statistical distribution

Clearly, once one specifies the accuracy for each test metric, it translates as different accuracy requirements for each fault and each response parameter that we are trying to model. Figures 14 and 15 illustrate the reason for this variation. In Figure 14, the response of the faulty circuit is close to the pass/fail threshold. A small error in the model may result in a large error in the computation of the *fail probability* metric (see Chapter2 section A for definitions). Comparatively in figure 15 (catastrophic case), the

response of the faulty circuit is far away from the threshold, and one can make larger errors in modeling without affecting the accuracy of the fail probability computation.

While this example is convincing that one needs to customize the error bounds for each case, it also raises a circularity problem. In order to translate the error budget given for the computation of the test metric to the error budget in the modeling process, we seem to need to know the actual distributions of the faulty circuits. Nonetheless, if we know the distribution, we would have done all the work already, and there would be no reason to continue with the modeling.

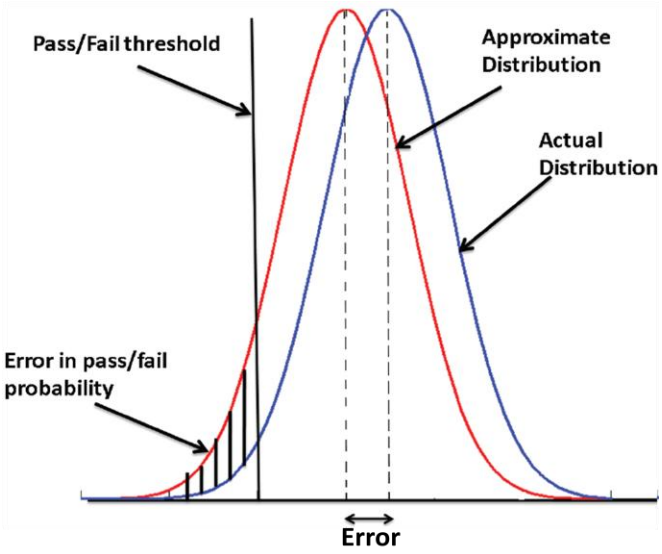

Fig. 14. Distribution of the faulty circuit close to the decision threshold

In order to break this circularity, we perform minimum number of simulations on the faulty circuit and try to predict beforehand what model order to choose. Using the error budget requirement and the threshold(s),

we evaluate the suitability of the modeled distribution. In other words, we determine if the model order that has been used for approximating the faulty distribution is good enough to meet the error budget requirement. The key issue here is that we let the final goal dictate the modeling process, rather than letting the modeling process dictate the final accuracy that we can obtain.

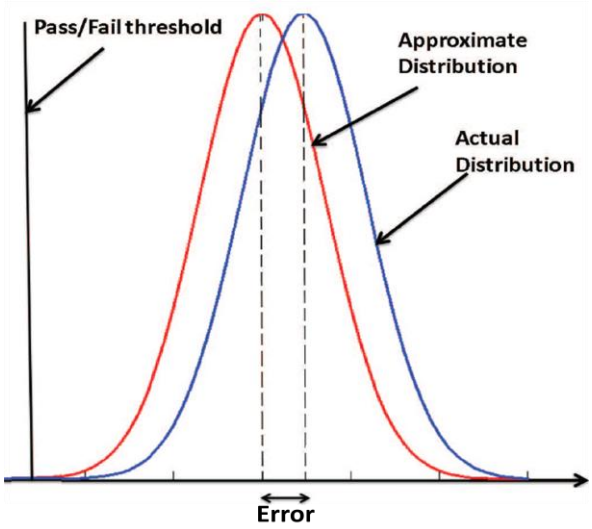

Fig. 15. Distribution of faulty circuit far from the decision threshold

B. Flow of the Non-Linear Modeling technique

Figure 16 represents the different steps involved in our adaptive model order selection procedure.

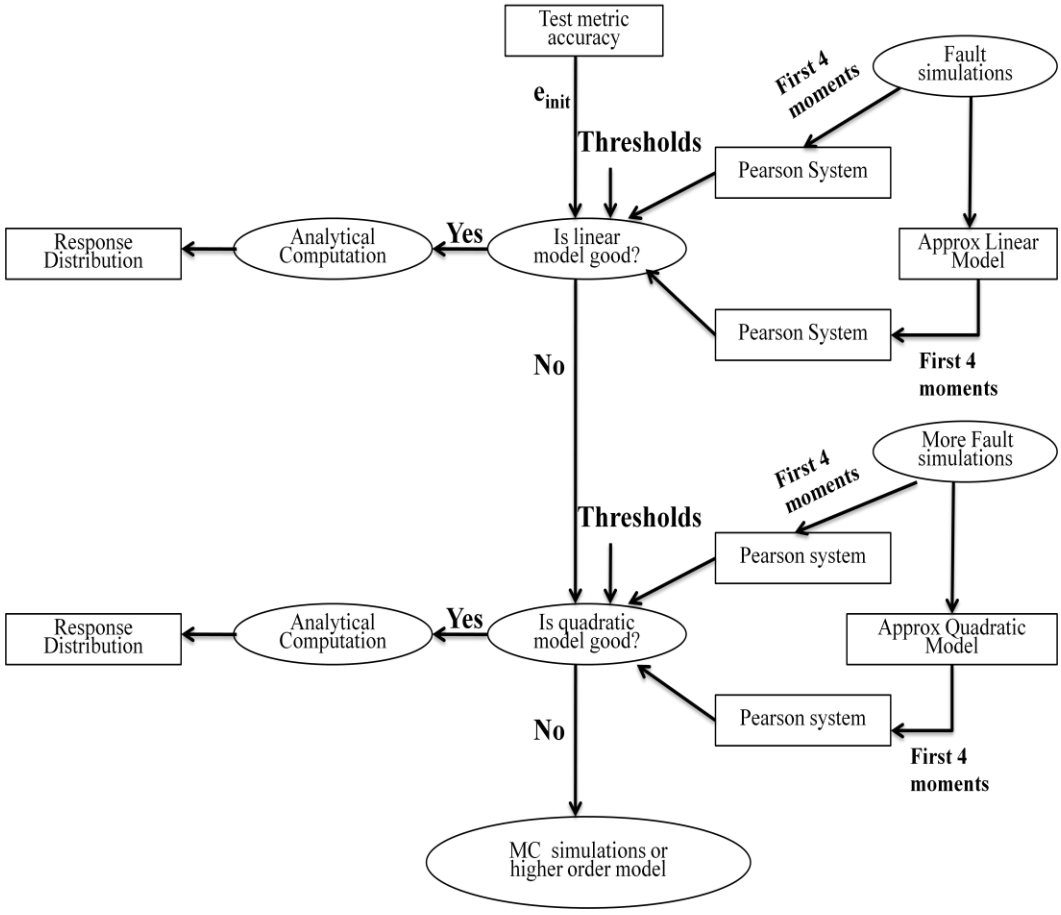

Fig. 16. Flow of the proposed modeling procedure

The inputs to the algorithm are the test metric accuracy (error budget) e_{init}, thresholds and the fault simulation data. First, we check if linear model meets the accuracy requirement. We perform *4n* fault simulations, *n* being the number of input parameters to compute the first four moments namely mean, standard deviation, skewness and kurtosis *ie.,* μ_{SP}, σ_{SP}, γ^1_{SP} and γ^2_{SP} of the response. Using the fault simulation data, we robustly regress the response in first order as a function of the input circuit parameters described before (see Chapter3, section B). Using the modeled responses, we calculate

the first four moments namely μ_{lin}, σ_{lin}, γ^1_{lin} and γ^2_{lin}. Approximate distributions are generated for SPICE and the linear model using Pearson system of statistical distributions. The Pearson system generates random data whose distribution follows the first four user defined moments [26]. The test statistics computed from these distributions are compared to determine the suitability of the model. If the linear model is deemed unfit, we repeat the same procedure for a second order model.

C. Pearson system of distributions

Once the first four moments of the circuit response are obtained, the proper member of the Pearson system can be identified and the probability of failure P_f is calculated as follows

$$P_f = \Pr[g(X) < 0] = \int_{g(X)<0} f_X(x)dx \tag{16}$$

where $f_X(x)$ is the joint PDF of the vector of random variables X and $f_{g(X)}(g(x))$ is the PDF of $g(X)$ identified by the Pearson system.

The Pearson system is an empirical system of distribution in which the PDF of a random variable is the solution of a differential equation,

$$\frac{1}{f(x)}\frac{df(x)}{dx} = -\frac{a+x}{c_0 + c_1 x + c_2 x^2} \tag{17}$$

here the coefficients a, c_0, c_1, c_2 are determined by the first four statistical moments of the random variable X and $f(x)$ is the PDF of X to be found by

solving the equation. The shape of $f(x)$ changes considerably with coefficients, and Pearson has classified the different shapes into seven groups according to the form of the solution of

$$c_0 + c_1 x + c_2 x^2 = 0 \tag{18}$$

More detailed explanations about the Pearson system can be found in [26].

D. Model coefficients determination

Instead of performing O (n^2) simulations for second order, we present a technique to obtain an approximation just by performing O (n) simulations. However, we need to perform another *4n* fault simulations (*n* being the number of inputs) to estimate the second order coefficients. Once the model is evaluated, we obtain Pearson distributions model and simulations to evaluate the accuracy that we can reach in calculating the test metrics. We resort to higher order modeling or Monte Carlo simulations (whichever is computationally feasible) if the accuracy does not meet the user defined requirement. The above procedure is repeated to model all the different responses of the circuit as a function of the circuit parameters.

Our coefficient determination model is mainly based on the observation that since the layout level parameters are uncorrelated, the contribution of the first order derivatives and the main body diagonal elements in the hessian is vital than the cross terms [16]. Any response can be approximated using the second order Taylor series around the nominal point as follows

$$f(x) \approx f(x_k) + \nabla f(x_k)^T (x - x_k) + \frac{1}{2!}(x - x_k)^T \nabla^2 f(x_k)(x - x_k) \qquad (19)$$

where $\mathbf{x}_k$ is the input point of interest, $\nabla f(x_k)$ is the gradient of the response function at $\mathbf{x}_k$ and $\nabla^2 f(x_k)$ is the Hessian of the response at $\mathbf{x}_k$.

Since the first order and the second order derivatives are the major contributors, we fit a second order model using a combination of reweighted least squares (RLS) and a proposed approach. As a rule of thumb, to select coefficients easily the, RLS technique needs 4*p* observations, *p* being the number of regression terms [24-25]. For a second order model *p*=2*n*, where *n* is the number of input parameters. Thus, we need 8*n* simulations to completely evaluate all the coefficients of the model. We incorporate a simulation reuse approach to compute the cross terms so that we won't need extra simulations.

For the case of Full Blown Simulation analysis (to obtain a complete second order model), the number of simulations required would be $\frac{4(n^2 + 3n)}{2}$. Thus, the number of simulation savings from our methodology to the Full Blown Simulation analysis is $\frac{(n + 3)}{4}$. RLS generally associates a weight of 0 for the outliers and 1 for the non outliers. RLS can be done using LMS or the LTS estimator for outlier classification. In this work, we use the LTS estimator because it can achieve better asymptotic efficiency. Since LTS consumes a lot of time, we use a fast LTS proposed by Rousseuw *et. al* based on approximation algorithms [28]. After the process of RLS, our model would contain approximations of 2*n*

derivatives (first and second order coefficients) and $\frac{n(n-1)}{2}$ unknowns (cross terms) since the total number of coefficients are $\frac{n(n+3)}{2}$. The regression model for the response can be represented as follows,

$$y = d + \sum_{i=1}^{n} a_i x_i + \frac{1}{2}\sum_{i=1}^{n} b_i x_i^{\,2} + \frac{1}{2}\sum_{i,j=1,i\neq j}^{n} c_{ij} x_i x_j \tag{20}$$

where d is the nominal circuit response, a_i's are the first order derivatives, b_i's are the second order derivatives and c_{ij}'s are the cross terms. After the RLS process, a_i's and b_i's would be known while the c_{ij}'s would be unknowns.

The cross terms can be computed by minimizing the following equation.

$$D = \sum_{l=1}^{t} (y_l - (d + \sum_{i=1}^{n} a_i x_{il} + \frac{1}{2}\sum_{i=1}^{n} b_i x_{il}^{\,2} + \frac{1}{2}\sum_{i,j=1,i\neq j}^{n} c_{ij} x_{il} x_{jl}))^2 \tag{21}$$

Here t is a variable that runs through the fault simulation space that we had generated earlier for modeling purposes. As described previously, RLS identifies the outliers and applies the Least squares model on the clean sample. We make use of the extra cross terms to make our model more generic to account for the cross correlations between process parameters. In an attempt to achieve it, we minimize the above estimator D over the entire sample space, thus allowing t to run from 1 to 8n. The values of the cross terms can be computed by equating the partial derivatives of the estimator D with respect to c_{ij}s shown in equation 22 to 0. This would yield a linear system of $\frac{n(n-1)}{2}$ equations as shown below

$$\begin{aligned} &\frac{\partial D}{\partial c_{12}} = 0 \\ &\frac{\partial D}{\partial c_{13}} = 0 \\ &\vdots \\ &\frac{\partial D}{\partial c_{nn-1}} = 0 \end{aligned} \tag{22}$$

Solving for the above partial derivatives and after rearranging them, we get the following set of equations.

$$c_{12}\sum_{l=1}^{t} x_{1l}{}^{2}x_{2l}{}^{2} + c_{13}\sum_{l=1}^{t} x_{1l}{}^{2}x_{2l}x_{3l} + \ldots + c_{nn-1}\sum_{l=1}^{t} x_{nl}x_{n-1l}x_{1l}x_{2l} + m_l\sum_{l=1}^{t} x_{1l}x_{2l} - \sum_{l=1}^{t} x_{1l}x_{2l}y_l = 0 \tag{23}$$

$$c_{12}\sum_{l=1}^{t} x_{1l}{}^{2}x_{2l}x_{3l} + c_{13}\sum_{l=1}^{t} x_{1l}{}^{2}x_{3l}{}^{2} + \ldots + c_{nn-1}\sum_{l=1}^{t} x_{nl}x_{n-1l}x_{1l}x_{3l} + m_l\sum_{l=1}^{t} x_{1l}x_{3l} - \sum_{l=1}^{t} x_{1l}x_{3l}y_l = 0 \tag{24}$$

$$\vdots$$

$$c_{12}\sum_{l=1}^{t} x_{1l}\,x_{2l}x_{nl}x_{n-1l} + c_{13}\sum_{l=1}^{t} x_{1l}\,x_{3l}x_{n-1l}x_{nl} + \ldots + c_{nn-1}\sum_{l=1}^{t} x_{n-1l}x_{nl} + m_l\sum_{l=1}^{t} x_{n-1l}x_{nl} - \sum_{l=1}^{t} x_{n-1l}x_{nl}y_l = 0 \tag{25}$$

c_{ij}'s are the cross derivatives to solve, y_l represents the l^{th} observation, m_l represents the estimated value of y_l from the RLS regression model and x_{li} represents the l^{th} observation of the i^{th} input parameter.

A solution set contains the 2*n* first and second order derivatives (obtained from RLS) and the cross terms (from the proposed approach). In each of the solution set, the first and second derivatives are the same, while the cross terms are different depending upon the index *t* that we have used in the summation in equation 21. As *t* varies from 1 to *8n,* we would have 8*n* sets of distinct model coefficients. We need to pick the "best coefficients set" that would come close to the SPICE results when it comes to computing different test metrics. In order to

compute the "best coefficients set", we calculate the error in test metric for each solution set. If there are multiple solution sets with the same least error in test metric computation, we choose the one with minimum sums of squares of residuals. Algorithm for best solution set selection is shown below

- Compute the error in test metric calculation for each solution set
- In case of multiple sets with the same least error, choose the coefficients with the least Sums of squares of errors (SSE)
- Solution set with minimum SSE contains the coefficients for the model

Chapter 5

HIERARCHICAL DOE BASED TEST STATISTICS EVALUATION

The method proposed in the previous chapter does not consider hierarchy in process variations. The results (see Chapter6) for the proposed adaptive method suggest good improvement in computational accuracy when compared to prior methods, such as worst case min-max analysis etc. However in some cases, the accuracy may not be adequate. In order to achieve even better accuracy for test metrics estimation, we propose a technique that exploits the hierarchical nature of process variations and uses DOE samples to localize the circuit instances in the process skew space.

A. Process variations model

In this section, we present our model for process variations. We consider two basic types of process variations in our analysis; inter die variations and intra-die variations. Intra die variations can be further divided into random variations and spatially correlated variations. Random variations have no dependence on the location of the devices, while intra die variations that are spatially correlated produce an increased likelihood of similar gate length for device that are closely spaced versus those that are placed further apart. In our model, we restrict ourselves to random intra die variations.

We use the following model [34], where the device length $L_{total,k}$ is the algebraic sum of nominal gate length, the inter die device length variation ΔL_{inter} and intra die device length variation $\Delta L_{intra,k}$.

$$L_{total,k} = L_{nom} + \Delta L_{inter} + \Delta L_{intra,k} \tag{26}$$

where ΔL_{inter} and $\Delta L_{intra,k}$ are random variables. L_{nom} represents the mean of the gate length across all possible dies. All devices on a die share one variable ΔL_{inter} for the inter die component of their total device length variation, which represents a variation of the mean of the gate length of a particular die. $\Delta L_{intra,k}$ represents the variations of individual gate from the mean gate length. In our procedure, each device is represented with a separate random variable $\Delta L_{intra,k}$, where all random variables $\Delta L_{intra,k}$ have identical probability distributions. For the purpose of our discussion we assume that both random variables ΔL_{inter} and $\Delta L_{intra,k}$ have a truncated Gaussian distribution. This reflects the fact that the gate length in an operational chip cannot be less than a finite minimum value and at the same time cannot be greater than a finite maximum value.

For our analysis, we use this process model for lengths and widths of all the transistors. Similar to the previous notation, the components of the device are W_{nom}, ΔW_{inter} and $\Delta W_{intra,k}$ where W_{nom} is the nominal value of width and ΔW_{inter} and $\Delta W_{intra,k}$ are random variables. Typically, these components are defined for unit elements such as a finger of the transistor. Statistical model for a multi-finger transistor is product of variations in single finger and number of fingers. In other words, for a '*m*' finger transistor, the process model for width would be

$$W = m(W_{nom} + \Delta W_{inter} + mean(\Delta W_{intra,k})) \tag{27}$$

We follow a similar procedure for modeling the length of the transistor.

B. Statistical tolerancing using Design of Experiments

In any Engineering design containing uncertainties, one of the key components of system evaluation is to analyze the uncertainties in performance to uncertainty in design. A wide variety of techniques in various Engineering fields have been proposed such as in structural reliability [35-37], stochastic mechanics [38-39] and quality engineering [40-42]. These include Taylor series based methods, Monte Carlo simulation (MC), numerical integration or design of experiments (DOE) based method. Often these analyses are carried out to compute the statistical moments of performance function, failure probability or other similar metrics.

Each of the above mentioned techniques have their own advantages and disadvantages in terms of computation accuracy, evaluation effort and applicability. It is generally accepted that computationally intensive brute force Monte Carlo simulations are correct indicators of system performance. Hence, they are used as a base for evaluating the accuracy of other proposed methods. In order to put things in a circuit's perspective, uncertainty in inputs is process variations in the length and width, modeled using the process model. Performances of the system are the output response of the circuit such as Gain, Noise Figure, IIP3, S-parameters and system evaluation is analogous to computing test statistics such as yield coverage, fail probability and test escape.

DOE can be used when the number of input parameters is low such that an exhaustive evaluation of the sampling points is possible. When one considers

overall variation parameters in the circuit, this is certainly not the case. Here, we make use of the hierarchical nature of process variations. If we focus only on the high-level variations (inter-die variations), the number of variation parameters is small (only four in our analysis) and does not increase with circuit complexity. To account for the inter-die variations therefore, we can make use of the DOE approach.

However, one cannot ignore the impact of inter-die variations in fault analysis. This would require a separate statistical analysis for each of the DOE samples, thus defeating the purpose of reducing the overhead. Here, we make use of two observations to make the computational complexity tractable. First, since intra-die variations are much smaller compared to the inter-die variations, it is possible to approximate the behavior of the circuit around each DOE sample with a linear function without much loss in accuracy. Second, since DOE output samples for a faulty circuit may fall far from the decision thresholds, we would have some knowledge about the nature of the circuit instances when seen relative to the DOE space. In such cases, even after the juxtaposition of the within die variations, no circuit instance around these DOE samples will cross the decision boundaries. If we can determine such cases, then we can determine the outcome of their simulation without conducting the simulation. Hence, our hierarchical analysis consists of three steps:

1. Evaluate the response of the DOE samples
2. Determine the DOE samples that fall far from the decision boundaries (these will be referred to as Group-I DOE samples)

3. Use Monte-Carlo sampling for within die variations and classify Monte-Carlo instances that fall around the group-I DOE samples wither pass or fail depending on the DOE outcome without conducting the circuit simulations.

The outcome of MC instances that cannot be classified in this manner will be determined either through simulations or through linear modeling.

The proposed method is developed based on experimental design technique for statistical moment analysis initially proposed by Taguchi [41]. He proposed a three-level factorial design with levels $\left\{\mu_{x_i} - \sigma_x i\sqrt{3/2}, \mu_{x_i}, \mu_{x_i} + \sigma_{x_i}\sqrt{3/2}\right\}$ where μ_{x_i} and σ_{x_i} are the mean and standard deviation of the i^{th} input random variable in the system and equal weights $\left\{\frac{1}{3}, \frac{1}{3}, \frac{1}{3}\right\}$. D'Errico and Zaino [43] modified the Taguchi method in order to improve the accuracy of moments calculation. They proposed levels $\left\{\mu_{x_i} - \sigma_x i\sqrt{3}, \mu_{x_i}, \mu_{x_i} + \sigma_{x_i}\sqrt{3}\right\}$ with corresponding weights $\left\{\frac{1}{6}, \frac{2}{3}, \frac{1}{6}\right\}$. It has been shown that the modified weights proposed are equivalent to nodes and weights of Gauss-Hermite quadrature method. These weights and levels are derived based on the assumption that the inputs are normally distributed.

C. Statistical analysis using DOE

In this section we briefly explain the theory behind statistical analyses using DOE.

C.1. Overall procedure for uncertainty analysis using DOE

For a random variable X, k^{th} order moment of the system response function g(X) is given by quadrature formula with m nodes.

$$E\{g^k\} = \int_{-\infty}^{\infty} [g(x)]^k f_X(x)dx \approx w_1[g(\mu+\alpha_1\sigma)]^k + w_2[g(\mu+\alpha_2\sigma)]^k + \cdots + w_m[g(\mu+\alpha_m\sigma)]^k \quad (28)$$

where $f_X(x)$ is the probability density function of X, μ and σ are the mean and standard deviation of X respectively. To estimate accurately up to 4th moment, which is often required by empirical statistics calculator such as Pearson's, we need at least a three node quadrature rule, and parameters α_i and w_i can be obtained by solving moment matching equations,

$$\mu_k = \int_{-\infty}^{\infty} (x-\mu)^k f(x)dx = w_1(\alpha_1\sigma)^k + w_2(\alpha_2\sigma)^k + \cdots + w_m(\alpha_m\sigma)^k \quad (29)$$
$$k = 0,1,2,\cdots,2m-1$$

where μ_k is the k[th] moment of the random variable X and *2m-1* is polynomial order of the quadrature rule. By making a substitution $l_i = \mu + \alpha_i\sigma$, the above equation can be rewritten in terms of l_i and w_i. There would be *2m* variables hence *2m* equations to solve for. Given *2m* different values of μ_k, the corresponding levels l_i and weights w_i can be calculated. Using the weights and levels, we compute the first *k* moments of the system response distribution g(X). It has also been proved that unique value of moments does not necessarily yield unique distribution. In simpler words, there can be many distributions with equal first *k* moments. Due to this limitation, we just use the levels obtained from

Gauss-Hermite quadrature formula for computation of input vectors to carry out DOE analysis. This would become clear in the subsequent sections.

C.2. Determination of levels for 7^n *DOE*

We resort to a 7^n *DOE* and use the levels obtained in the process to compute the input vectors for our method. Based on equation y, the equations for 7^n DOE are formulated as follows.

$$\begin{aligned}
&w1 + w2 + w3 + w4 + w5 = 1 \\
&w_1 l_1' + w_2 l_2' + w_3 l_3' + w_4 l_4' + w_5 l_5' = 0 \\
&w_1 l_1'^2 + w_2 l_2'^2 + w_3 l_3'^2 + w_4 l_4'^2 + w_5 l_5'^2 = \sigma^2 \\
&w_1 l_1'^3 + w_2 l_2'^3 + w_3 l_3'^3 + w_4 l_4'^3 + w_5 l_5'^3 = \sigma^3 \sqrt{\beta_1} \\
&w_1 l_1'^4 + w_2 l_2'^4 + w_3 l_3'^4 + w_4 l_4'^4 + w_5 l_5'^4 = \sigma^4 \beta_2 \\
&w_1 l_1'^k + w_2 l_2'^k + w_3 l_3'^k + w_4 l_4'^k + w_5 l_5'^k = \mu_k \\
&k = 5, \cdots, 13
\end{aligned} \tag{30}$$

In order to solve the above system of equations, the first thirteen statistical moments of a normally distributed random variable X should be provided. Solving the above system of equations yield levels as displayed in the table below.

TABLE I

7^n DOE levels for normally distributed inputs

Levels
$-2.65196135\sigma + \mu$
$-1.67355162\sigma + \mu$
$-0.81628788\sigma + \mu$
μ
$0.81628788\sigma + \mu$
$-1.67355162\sigma + \mu$
$-2.65196135\sigma + \mu$

D. Proposed Method

Figure 17 illustrates the flow of our proposed test statistics estimation engine.

Given the thresholds and MC input samples, the proposed methodology evaluates the status of each of the Monte Carlo (MC) circuit instance (pass/fail) with good amount of accuracy and an acceptable simulation overhead. Using the MC input samples and algorithm shown in Figure 17 we obtain density function (JPDF) of output parameters. This JPDF along with the position of the specification thresholds is used to calculate the test statistics.

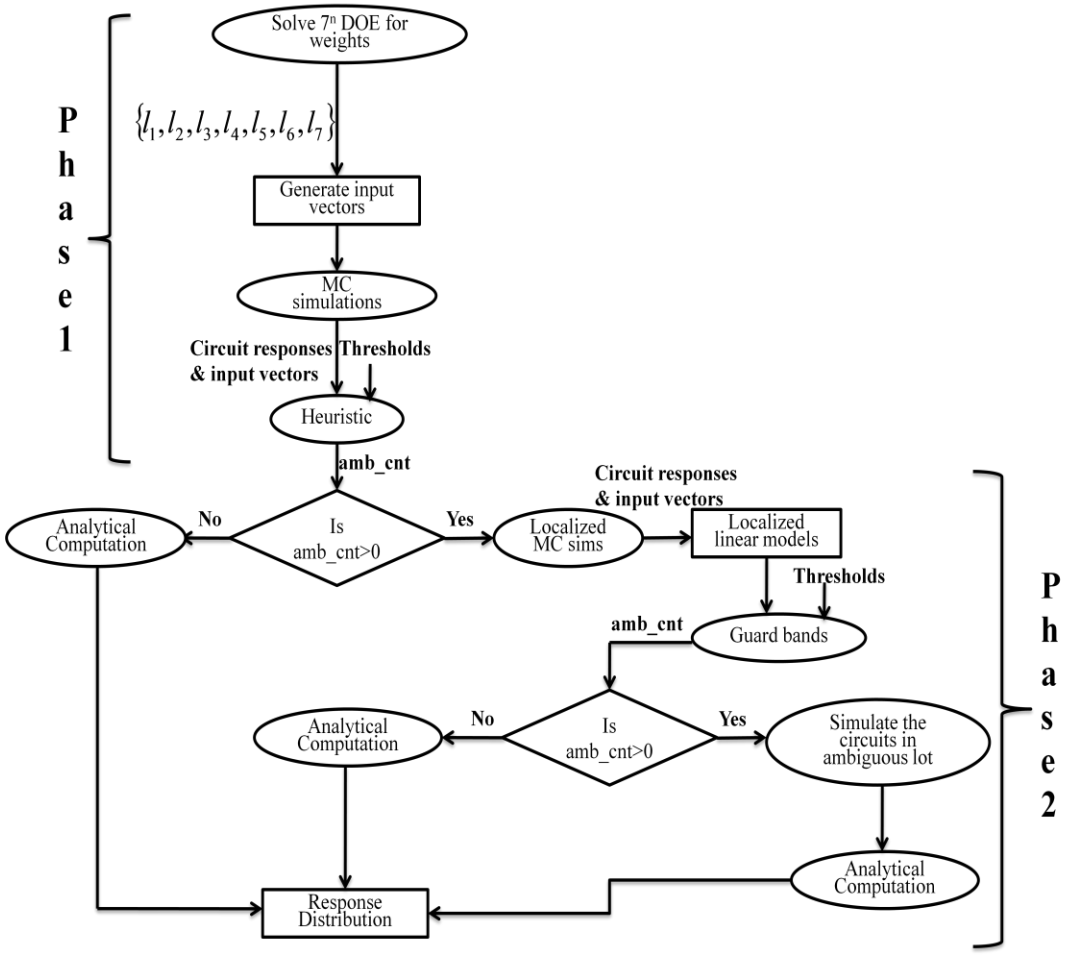

Fig. 17. Flow of our proposed hybrid procedure

In short, the methodology predicts the status of the MC circuit instances (pass/fail) with the help of heuristics and linear models, at the cost of reasonable simulation overhead. There are two phases in this procedure, Phase I invokes heuristics, on input vectors generated using levels obtained from solving 7^n DOE equations, to classify the status of the circuit instance as certainly passing/certainly failing/ambiguous. Phase II resolves the status of the circuits that are ambiguous using localized linear models, whose demarcation boundaries are set by the DOE levels. Based on the relative

position(s) of the specification threshold(s) and JPDF of circuit parameters, the need for a modeling phase may or may not arise. For example, if the JPDF is far away from the positions of the specification thresholds, the heuristic evaluates the status of most of the circuit instances, leaving very few of them in the ambiguous bin which can be simulated later. This would save considerable amount of simulation effort needed to construct models. On the other hand, if the JPDF of circuit parameters and the specification thresholds are nearby, which is quite often the case, use of the modeling phase becomes inevitable.

It should also be noted that unlike extracting a single linear model for the entire input space, which have often been found to be inadequate, we construct linear models in Phase II over localized input regions (the demarcations are dictated by the process model presented in section E of this Chapter). This gives us the advantage of increased accuracy in modeling the circuit output parameters. Even though the accuracy of localized linear models is good, they can never match SPICE simulations, we account for this limitation by applying guard bands around each specification threshold. These guard bands for a particular input space are developed based on the RMS error in modeling the output parameters for that input space. Once we apply models along with guard bands for the MC circuit instances, most of the circuits are resolved except for the circuit instances where at least one of the modeled specification falls in the guarded region. This reduced number of

circuits can be readily simulated. The next few sections explain the heuristics and modeling procedure in detail.

E. Phase I: Heuristic

As shown in Figure 17, the inputs to our heuristic are the DOE levels and the specification thresholds. To make things clear, let us explain our heuristic with a cascode LNA as example. Simple cascode architecture contains two transistors, 3 inductors and a load capacitor. The inputs to our algorithm are process variables namely, width, length, inductance and capacitance ie., four in this case. We construct 7^4 DOE input process vectors, whose positions are determined by the DOE levels in Table I and simulate them. From the simulation results and the position of specification thresholds, we pick out the combination of input vectors that pass, and the remaining ones fail. Using this knowledge, and the position of the MC circuit instance with respect to the DOE vectors, we propose a heuristic to evaluate the status of the circuit as **certainly passing**/**certainly failing** or **ambiguous**.

- **Certainly passing/failing**: A MC circuit instance whose status has been evaluated by the heuristic with complete certainty. Modeling is not applicable for this case.
- **Ambiguous:** A MC circuit instance whose status cannot be determined by the heuristic. Modeling/simulations are used to resolve the status of the circuit instances in this category.

Figure 18 highlights one possible scenario for an MC circuit instance. It shows the position of each of the input process parameters (W, L, ind, cap)

for a particular MC instance relative to the position of the DOE levels. In this Figure, we note that all the process parameters (both the widths and lengths, three inductors and a load capacitor) are bound between the same boundaries even in the presence of intra die variations. Based on our observations from pseudo randomly generated MC circuit instances, there is only 50% statistical chance for this to occur. The remaining 50% of the circuit instances fall directly into the ambiguous bin since the heuristic cannot handle it.

It takes quite a considerable simulation effort to construct models to resolve the status of the circuits in the ambiguity bin, which is worthwhile for a fault free circuit. But in the case of faulty circuit, such an elaborate analysis would generate unacceptable computational burden especially if the JPDF and specification thresholds are far. To account for this situation in the faulty circuits, we average out all the input parameters and present one width, one inductance, one length and one capacitance to our heuristic.

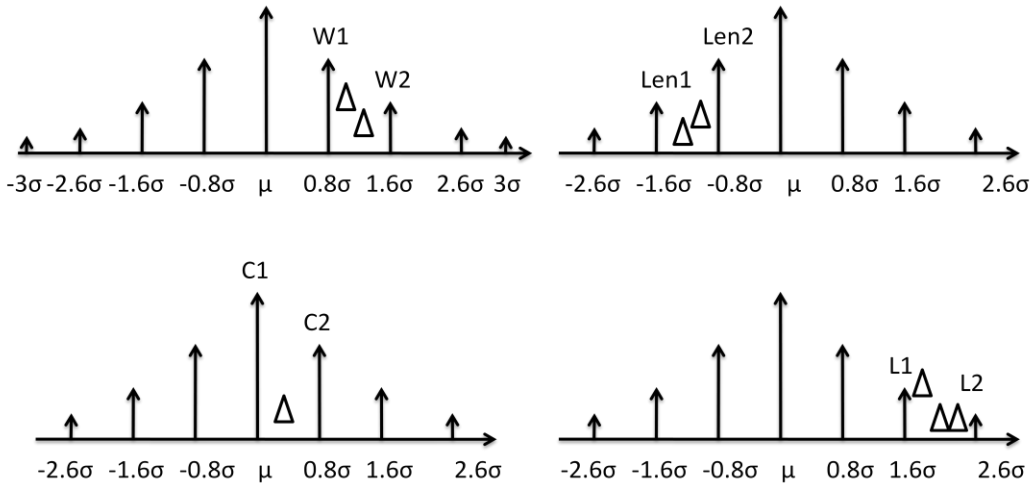

Fig. 18. Position of the process parameters with respect to the DOE levels at the beginning of Phase I

In the example figure, widths are bounded between (W1-W2), lengths between (Len1-Len2), inductances between (L1-L2) and capacitance between (C1-C2). Using these boundaries 2^4 different combinations are possible as shown below

$$\left\{\begin{array}{l} W1-Len1-L1-C1 \\ W1-Len1-L1-C2 \\ \vdots \\ W1-Len2-L2-C2 \\ W2-Len2-L2-C2 \end{array}\right\} \tag{31}$$

Using the pass/fail information from simulation of DOE vectors, the following rules apply in determining the status of the circuit.

- Circuit certainly passes if all the 16 combinations shown above pass
- Circuit certainly fails if all the above combinations fail

- Ambiguous otherwise

F. Phase II: Localized linear models

Status of the MC circuit instances in the ambiguous bin is resolved with the help of linear models around local input space. Figure 18 shows input space demarcation for the purpose of reducing the input span of the models. From the Figure, there are 8 different input regions across four distinct process parameters, resulting in 8^4 model possibilities. As a worst case scenario, we might even need 8^4 different models to resolve the status of the circuits in the ambiguous bin. However, based on our observations it does not happen, thanks to our heuristics for avoiding this mathematical possibility. As discussed previously, since 50% of the circuits does not fall within the bin boundaries (due to intra die component in process variation model), mean of all the process parameters are used to identify the appropriate model.

Let us assume that once we average out all the intra die process variations, the position of the process parameters relative to the DOE levels are shown in Figure 19. We sample from these bounded regions to compute models for circuit's output parameters. Using these models and the MC circuit instances, we compute the JPDF of all the circuit parameters which is used to evaluate the test statistics. As a rule of thumb in modeling, we use $4k$ simulations to construct linear models, 'k' being the number of input parameters ie.,8 in the case of an LNA. Even though, we are modeling a small portion of the input region, the accuracy of the models is limited and these would affect the results of the circuit instances whose responses fall near the specification thresholds.

In order not to compromise on the accuracy we use guard bands (regions of uncertainty around the specification thresholds) to simulate the few instances which cannot be evaluated after modeling. The positions of the guard band are computed for each output parameter based on the RMS error in modeling that particular parameter. Since the RMS error in modeling output parameters for a localized input space is small, the proportion of the circuits falling in guarded region is also small. These tiny circuit samples can be readily simulated to obtain their true status.

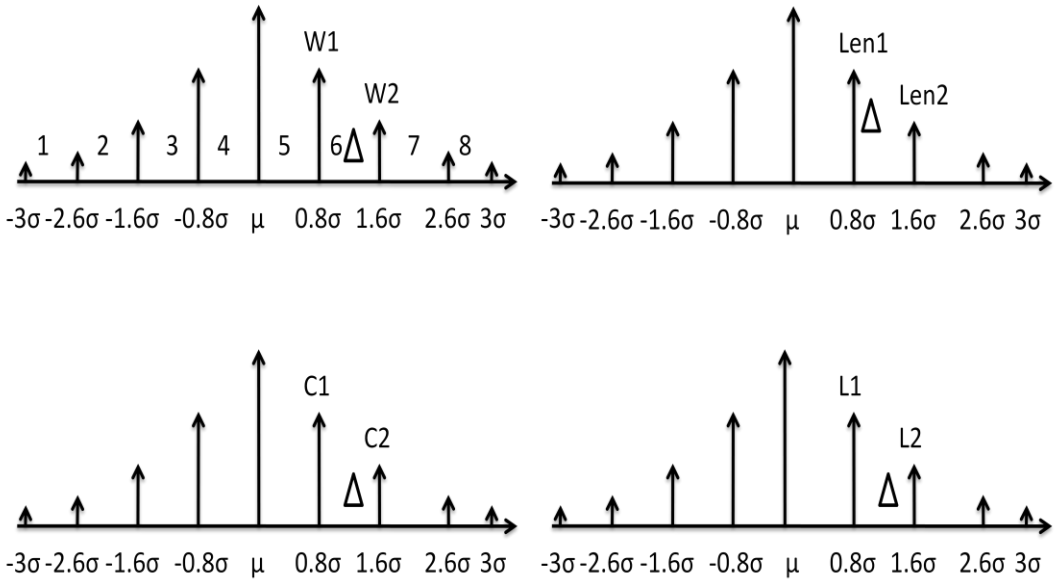

Fig. 19. Position of process parameters with respect to the DOE levels after averaging them out at the beginning of phase II

Chapter 6

SIMULATION RESULTS

This chapter contains simulation results for both the proposed methods *ie.,* adaptive model order selection method and the DOE based hierarchical test statistics evaluation method.

A. Adaptive model order selection method

We have applied our non-linear coefficients approximation algorithm to two experimental circuits, namely a cascode Low Noise Amplifier (LNA) and double balanced Gilbert Cell Mixer (Mixer) with a resistive load as shown in Figures 20 and 21. The input parameters for the model are the width and length of the transistors and the R, L and C components connected to the circuit. For the mixer, we exclude the matching network parameters for model computation. We consider both single fault and simultaneous fault injection: there can be one or multiple faults in each faulty instance of the circuit.

In this section, we show that the adaptive modeling procedure works well for both single and simultaneous fault injection scenarios. The circuit responses we model are gain, input impedance, output impedance, Noise Figure and IIP3 for the Low Noise Amplifier, and Conversion gain, IIP3, Noise Figure, LO-RF, RF-IF and LO-IF port isolation parameters for the Mixer. Gain and IIP3 are assumed to measured up to the accuracy of +/-0.1dB, while the

input and output impedance are assumed to be measured with an accuracy of about +/-5 ohms. Noise Figure is assumed to be measured with an accuracy of about +/-0.5 dB. Similarly for the mixer, the port isolation parameters are assumed to be measured with an accuracy of about +/-5 dB. These uncertainties in the measurement are incorporated to emulate the limitations of the ATE measurement.

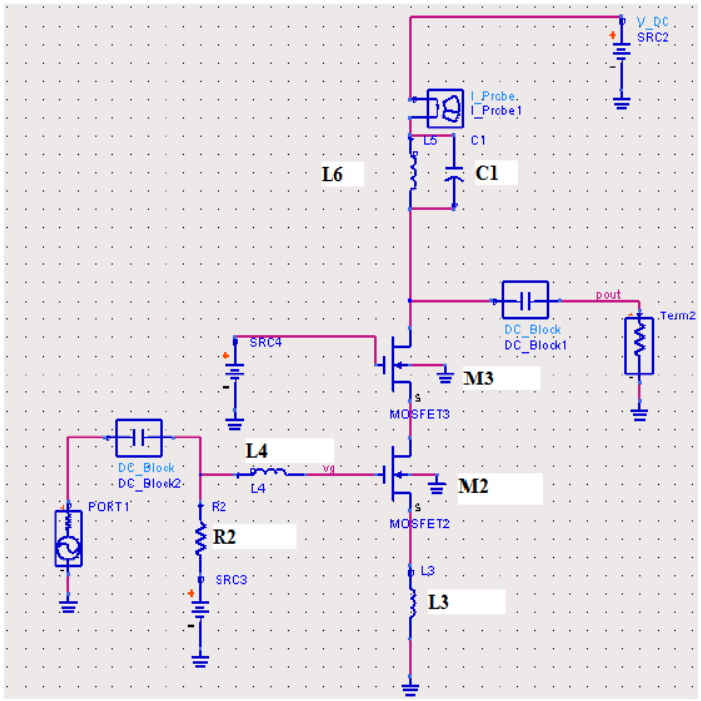

Fig. 20. Cascode Low Noise Amplifier

For the LNA, there are 2 transistors, 3 inductors, and a capacitor. We consider fault injection into each of the width and length of the transistor, 3 inductors and the capacitor, 8 faults in total. In our Mixer, there are 6 input transistors, 4 resistors and 2 inductors. The number of faults are 2 for each transistor, 1 for each resistor and inductor thus 18 faulty circuit instances in all. Apart from the single injected faults, we also consider two global faults

each for the Mixer and LNA. The global faults are V_{th} shift and simultaneous faults in the widths of the transistor. In case of these test circuits, not all fault injections cause a specification violation. In making a fault dictionary we consider only non-redundant faults i*e.*, faults that cause a specification violation. The fault dictionary for the LNA and Mixer is shown in Table II.

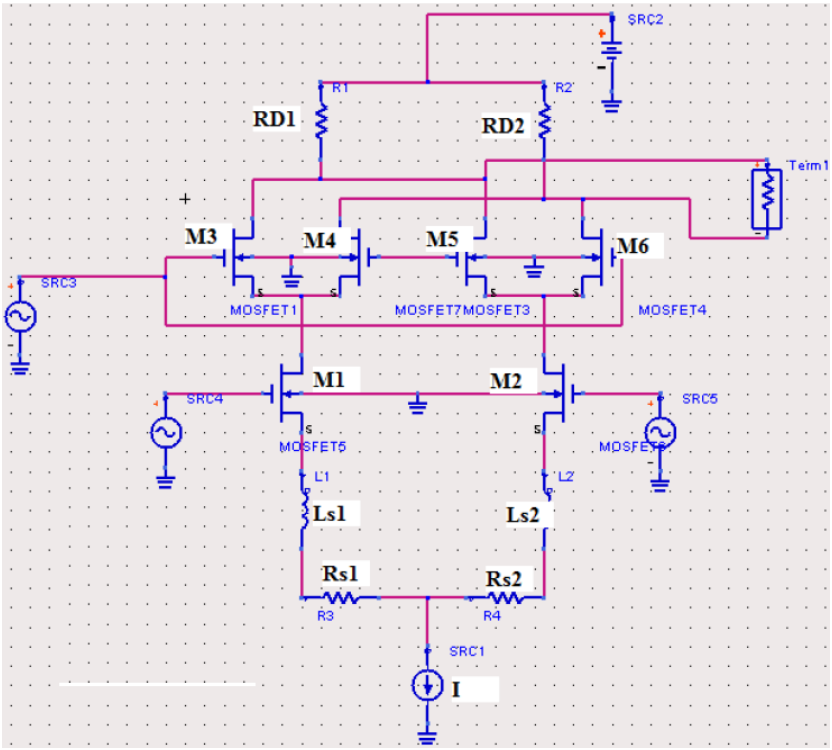

Fig. 21. Double balanced Gilbert cell mixer

TABLE II

Fault dictionary of LNA and Mixer

LNA		**Mixer**	
Fault	Fault location	Fault	Fault location
F1	W(M2)	G1	RD1
F2	L(M2)	G2	W(M1)
F3	L6	G3	L(M1)
F4	C1	G4	I_bias
F5	L4	G5	Rs1
F6	L3	G6	W(M3)
F7	W(M2) and W(M3)	G7	W(M1) and W(M2)
F8	V_{th}	G8	V_{th}

The transistors width and length are assumed to exhibit a variation of +/-10%, while variations in the passive components are set at +/-20%. These values correspond to the tolerance window of the process parameters which span for 3σ on either side. It is assumed that the injected faults cause a maximum deviation of up to 10σ from the nominal value. It should be noted that the amount of deviation we inject for faulty components has no effect on our modeling technique. We merely use this fault injection method as a conduit to evaluate the performance of our technique in terms of accuracy of computing a test metric, the probability of failing a specification, *fail probability*, in this case.

We performed 5000 MC simulations for each fault instance to form the baseline. In our experiment, we set the value of error budget for pass/fail probability computation to 2%. Threshold T1 is chosen such that the yield of the fault free distribution is 100%. As a first step, we obtain the first order coefficients using the RLS approach. We evaluate the suitability of this model

order by comparing the accuracy in test statistics that can be achieved. If the accuracy meets the user defined specification, we use it to compute the test statistics. In the case of tight threshold(s), where linear model may not be adequate, we perform extra 4*n* simulations and compute the second order coefficients. If second order model also proves to be inadequate, we need to resort to higher order modeling or Monte Carlo simulations whichever is computationally feasible.

Table III and Table IV show the results of our accuracy driven model order selection procedure for each of the faults in LNA and Mixer. We see that certain responses require higher order modeling in order to meet the error budget. Table V compares the number of simulations required to model the response parameters under all fault scenarios using the proposed approach against the conventional Monte Carlo simulations. The number of simulation setups required to evaluate the response parameters are different for the LNA and Mixer. For the LNA, gain, input impedance, output impedance and Noise Figure simulations require a single tone setup, while the IIP3 measurement requires a two tone setup, thus 2 distinct setups. For the case of mixer, we require one simulation setup for evaluating gain, port isolation parameters and Noise Figure, one setup for IIP3 computation needing 2 distinct setups. Since we use 5000 fault simulations for each fault as baseline to evaluate our method, we would need 10,000 simulations for LNA and Mixer respectively (2 distinct setups).

As there are eight faults in the dictionary, we require 80,000 simulations for the LNA and another 80,000 simulations for the mixer to evaluate our method. Based on the model order that we obtain, the number of simulations we require are either $4n$ (first order) or $8n$ (second order), n being the number of inputs. Nonetheless, in our experiments we have not used fault simulation techniques for estimating the first order model of the faulty circuits [29-30]. Using these techniques, we could potentially remove additional simulations that are required for the second order model. We assume that we resort to Monte Carlo simulations when the second order model does not meet the accuracy requirement. The simulation savings are expected to reduce with tighter thresholds as the required modeling order increases proportionally.

TABLE III

Model order selection for LNA

Output parameters	Faults	Model order
Gain	F1	2
	F2	2
	F3	1
	F4	2
	F5	>2
	F6	2
	F7	1
	F8	2
Zin	F1	1
	F2	2
	F3	1
	F4	1
	F5	2
	F6	2
	F7	1
	F8	2
Zout	F1	2
	F2	2
	F3	>2
	F4	1
	F5	2
	F6	1
	F7	1
	F8	2
Noise Figure	F1	1
	F2	1
	F3	1
	F4	1
	F5	1
	F6	1
	F7	1
	F8	1
IIP3	F1	1
	F2	1
	F3	1
	F4	1
	F5	1
	F6	1
	F7	1
	F8	1

TABLE IV

Model order selection for Mixer

Output parameters	Faults	Model order
RF-IF isolation	G1	2
	G2	>2
	G3	2
	G4	1
	G5	1
	G6	2
	G7	1
	G8	2
Conversion Gain	G1	2
	G2	2
	G3	1
	G4	1
	G5	2
	G6	2
	G7	1
	G8	2
IIP3	G1	1
	G2	1
	G3	>2
	G4	1
	G5	2
	G6	1
	G7	1
	G8	1
Noise Figure	G1	1
	G2	1
	G3	1
	G4	1
	G5	1
	G6	1
	G7	1
	G8	1
LO-RF isolation	G1	2
	G2	2
	G3	2
	G4	1
	G5	1
	G6	2
	G7	1
	G8	2
LO-IF isolation	G1	2
	G2	2
	G3	1
	G4	1
	G5	1
	G6	2
	G7	1
	G8	2

TABLE V

Simulation statistics for LNA and Mixer

Circuit	Monte Carlo	Proposed	Speedup
LNA	80,000	10,608	7.54x
Mixer	80,000	11,376	7.03x

Table VI and Table VII compares the fail probability computed from both the approaches for the base case of 5000 MC simulations for an LNA and Mixer respectively. Here, the table is tabulated based on the assumption that the maximum attainable fail probability is 100% for each fault. However, this is not true in reality, as we have to account for the probability of fault occurrence and the probability for each fault. If we assume that the probability of fault occurrence to be 10% and probability of a fault to be $\frac{1}{6}$, the accuracy boost in fail probability computation we get would be an increase in magnitude by two orders.

The fail probability is computed for each of the response parameters for all the fault scenarios in the dictionary. This table illustrates that our approach works well and satisfies the error budget for most of the cases except for a few. The error in test metric computation for some cases is more than 2%. These cases are depicted separately for each output parameter at the bottom. Our method predicts these inadequacies in the model beforehand by performing few faulty SPICE simulations. See the corresponding faults and parameters tables III and IV.

Table VIII compares the Test escape computed from SPICE and adaptive model order approach. To compute the test escape associated with an LNA we regard Gain, Zin1 and Zout to be the measured parameters from which one evaluates test metrics such as pass/fail statistics. The pass/fail statistics for the other 2 parameters namely IIP3 and Noise figure along with the test pass determine the overall pass/fail statistics. Similarly for the Mixer, Conversion gain, LO-IF, RF-IF and LO-RF port isolation parameters contribute to test pass/fail statistics while Noise Figure and IIP3 along with the test pass/fail statistics contribute to overall pass/fail statistics. Test escape is defined as the number of circuit instances that pass the test criterion but fail the overall criterion.

TABLE VI

Fail probability comparison for all faults in the dictionary of an LNA assuming a threshold T1

Output parameters	Faults	SPICE (in %)	Ours (in %)	Error (in %)
Gain	F1	58.98	59.66	0.68
	F2	0.12	0.02	0.1
	F3	43.32	44.72	1.4
	F4	24.65	23.95	0.7
	F6	34.65	34.76	0.11
	F7	0	0	0
	F8	22.79	23.76	0.97
	F5	**54.1**	**50.39**	**3.71**
Zin	F1	91	90.04	0.96
	F2	99.24	99.86	0.62
	F3	63.5	62.98	0.52
	F4	99.87	100	0.13
	F5	28.9	28	0.9
	F6	76.6	75.9	0.7
	F7	0	0	0
	F8	37.48	36.11	1.37
Zout	F1	99.78	98.7	1.08
	F2	0.76	0.02	0.74
	F4	43.7	43.11	0.59
	F5	99.2	98.98	0.22
	F6	99.65	99	0.65
	F7	0	0	0
	F8	19.28	20.05	0.77
	F3	**99.96**	**90.34**	**9.62**
Noise Figure	F1	0	0.12	0.12
	F2	99.98	100	0.02
	F3	0	0.16	0.16
	F4	0	0	0
	F5	0	0	0
	F6	0	0.83	0.83
	F7	0	0	0
	F8	68.79	68.17	0.62
IIP3	F1	100	100	0
	F2	100	100	0
	F3	100	100	0
	F4	99.08	98.58	0.44
	F5	100	100	0
	F6	100	99.34	0.66
	F7	100	100	0
	F8	37.63	37.17	0.46

TABLE VII

Fail probability comparison for all faults in the dictionary of a Mixer assuming a threshold H1

Output parameters	Faults	SPICE (in %)	Ours (in %)	Error (in %)
RF-IF isolation	G1	100	100	0
	G3	99.7	100	0
	G4	100	100	0
	G5	100	100	0
	G6	100	100	0
	G7	0	0	0
	G8	82.63	81.87	1.24
	G2	**96.7**	**100**	**3.3**
Conversion Gain	G1	61.9	62.08	0.18
	G2	45.34	46.56	1.22
	G3	38.4	39.7	1.3
	G4	99.94	99.98	0.04
	G5	1.36	2.13	0.77
	G6	99.91	99.53	0.38
	G7	2.76	2.53	0.23
	G8	48.91	47.5	1.41
IIP3	G1	0.06	0	0.06
	G2	55.67	56.23	0.56
	G4	1.38	0.66	0.72
	G5	100	99.73	0.27
	G6	91.5	91	0.5
	G7	97.34	98.11	0.77
	G8	42.63	42.65	0.02
	G3	**79.34**	**84.67**	**5.33**
Noise Figure	G1	23.76	98.7	1.08
	G2	0.76	0.02	0.74
	G3	43.7	43.11	0.59
	G4	99.2	98.98	0.22
	G5	99.65	99	0.65
	G6	0	0	0
	G7	19.28	20.05	0.77
	G8	**99.96**	**90.34**	**9.62**
LO-RF isolation	G1	93	91	2
	G2	78.45	79.16	0.71
	G3	99.67	99.93	0.26
	G4	100	100	0
	G5	100	99.98	0.02
	G6	99.3	99.65	0.35
	G7	0	0	0
	G8	58.63	57.65	1.02
LO-IF isolation	G1	100	100	0
	G3	99.7	100	0.3
	G4	100	100	0
	G5	100	100	0
	G6	100	100	0
	G7	0	0	0
	G8	82.63	81.87	1.24
	G2	**96.7**	**100**	**3.3**

TABLE VIII

Test escape comparison

Fault	SPICE	Ours
F1	55.36	55.76
F2	0.12	0.02
F3	36.92	35.02
F4	0	0
F5	35.78	37.99
F6	56.5	55.8
F7	0	0
F8	5.89	6.17
G1	61.84	62.08
G2	0	3.78
G3	45.87	43.94
G4	99.94	99.98
G5	0	0
G6	91.89	92.9
G7	0	0
G8	65.15	63.29

B. DOE based hierarchical process variations method

We use a cascode LNA, same as the one shown above to evaluate the efficiency of the DOE based method. The fault dictionary under which we analyze using our method is shown in the table below. We have evaluated only single fault injection scenario *ie*., only one fault in a circuit instance. Since our method is based on modeling, which has a strong mathematical foundation, we would expect our method to perform well for multiple fault injection scenarios as well. As described in the previous section, there are 8 possible faulty circuit instances and we choose only 6 among them that cause violation in at least one of the specifications. The tolerances and variations in the process parameters are exactly same as used in previous method to maintain consistency. Nonetheless, it

is assumed that the injected faults cause a maximum deviation of 6σ (unlike 10σ in the previous section) from the nominal value to be more realistic.

TABLE IX

Fault dictionary of LNA for DOE based method

Fault	Fault location
H1	Global inductance shift
H2	L6
H3	Global shift in V_{th}
H4	C1
H5	L(M2)
H6	W(M2)

50K Monte Carlo simulations for each of the faults in the dictionary are conducted to form the baseline for evaluating the efficiency of the proposed method. A notable feature of this method is the incorporation of process model (see Chapter 5, section E.) to form the 50K Monte Carlo samples. The 3σ tolerances for the inter die variations are +/-10% of the mean and the 3σ intra die variation is limited to +/-1% of the mean for the transistor process parameters such as Width and Length. For the case of resistances, inductances and capacitance, the inter die variations would be +/-20% and the intra die variations would be +/-2% of their mean values respectively. As in the previous method, we account for inaccuracies is the measuring equipment in our model. The approximation parameters are kept exactly the same as in the previous method.

As a first step, we use heuristics and DOE to classify the Monte Carlo circuit instances into three parts **certainly failing**, **certainly passing**, **ambiguous**. Then, we resolve the circuit instances in the ambiguous bin by using localized

linear polynomial models based on the process model. Guard bands are also used to account for inaccuracies in the models. The circuit instances falling in the guarded region are simulated readily to evaluate their status. Our proposed method is compared with the recently published work on test statistics estimation using kernel based non parametric density estimation techniques by Stratigopulous *et.al* [31]. For comparison purposes, four output parameters are used, namely gain, Noise Figure, IIP3 and S11.

It is reported in [31] that, the kernel based density estimation method for synthetic JPDF construction works well if the dimension of the JPDF is less. Our hierarchical DOE based method does not have any such constraint; we restricted our comparison to four dimensional case due to extensive computation time requirements of the density estimation method for higher dimensions. To show results on a higher dimensional JPDF, we also evaluated our technique for 6 output parameters. The two additional parameters apart from the previously mentioned four are the gain of the LNA at pass-band limits.

Table VIII shows the accuracy in estimating the test metrics of faulty instances for different guard banding situations for four parameter case. For certain fault cases such as (H_1, H_2) the nominal response of at least one of the output parameter is at least 10σ away from the mean of the fault free circuit. In such situations, we assume that all the circuit instances of that particular fault fail, thus avoiding the need to perform any complicated analysis. Column 1 shows different guard banding situations, column 2 comprises instances from the fault dictionary where FF indicates the fault free case. Columns 3, 4 and 5 show the

number of circuit instances that have been determined as passing, failing and doubtful respectively for each case in the dictionary. Column 6 contains the number of misclassified circuit instances in the end.

The misclassification count is a sum of two components: passing circuits classified as failing (YL) and failing circuits classified as passing (TE). This behavior is generally common among those circuit instances whose output parameter falls close to the specification threshold(s). In order to keep the misclassified circuits to a minimum, we associate guard bands based on the RMS error in modeling a particular output parameter around the specification threshold(s). One would expect the misclassified circuit instances to reduce and the simulation cost to increase with higher guard banding as illustrated in the Table X. Figure 22 displays the effect of guard banding and simulation savings on the misclassification number for the fault free circuit scenario with four output parameters.

TABLE X

Fail probability estimation for four parameter case

Guard band	Faults	Certain pass (out of 50K)	Certain fail (out of 50K)	Ambiguous(out of 50K)	Misclass(out of 50K)	Simulation count
5σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11015	35220	3765	11	98359
	H6	35930	11099	2971	13	82611
	FF	41478	5575	2947	46	94176
4.5σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11216	35394	3390	15	90859
	H6	11291	36066	2643	15	76051
	FF	41653	5637	2710	46	89436
4σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11410	35576	3014	19	83339
	H6	11456	36194	2350	21	70191
	FF	41843	5720	2437	51	83976
3.5σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11604	35755	2641	27	75879
	H6	11658	36313	1616	27	63771
	FF	42041	5777	2182	56	78876
3σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11791	35953	2256	33	68179
	H6	11828	36434	1738	32	57951
	FF	42275	5847	1878	63	72796
2.5σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	12001	36113	1886	38	60779
	H6	11992	36587	1421	38	51611
	FF	42485	5942	1573	80	66696

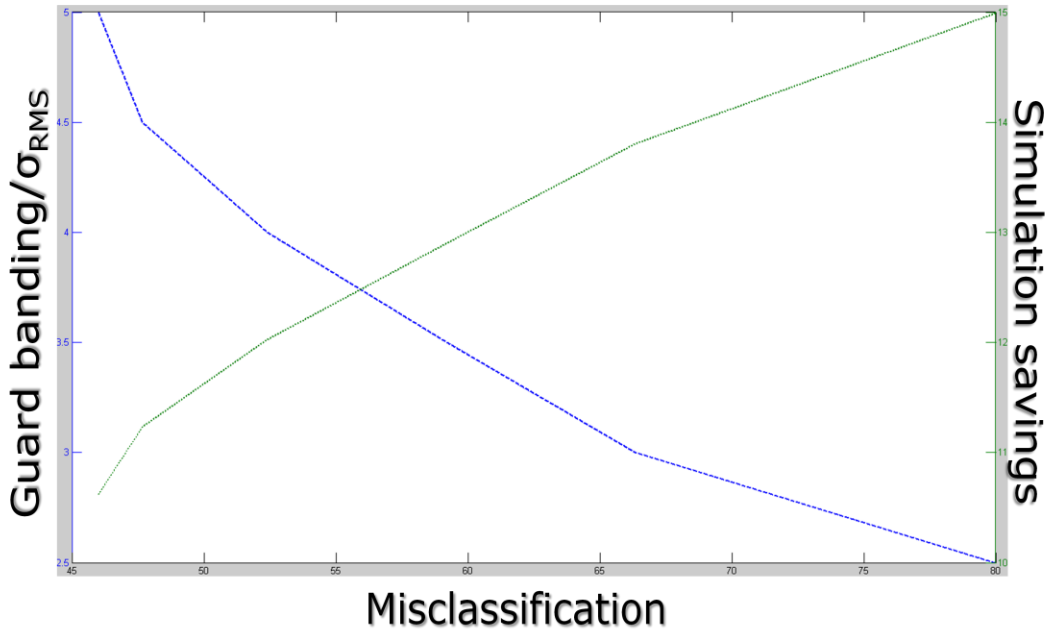

Fig. 22. Variation of Misclassification with guard banding and simulation savings

Simulation count shown in the last column of Table X is a sum of three components

1. 7^4 DOE simulations to classify the circuit as certainly passing/certainly failing/ambiguous
2. Number of simulations required to construct localized linear models to evaluate the status of the ambiguous circuit instances
3. Simulation of circuit instances in the guarded region

The total simulation count shown in column 6 is the number of simulations required to evaluate the status of 10^6 circuit instances. Table XI shows the test statistics evaluation for the case of six output parameters. Table XII shows the total savings in simulation for both the cases: four parameter and six parameter cases for different guard banding scenarios.

TABLE XI

Fail probability estimation for six parameter case

Guard band	Faults	Certain pass (out of 50K)	Certain fail (out of 50K)	Ambiguous(out of 50K)	Misclass(out of 50K)	Simulation count
5σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	10806	35645	3549	11	91638
	H6	11001	36039	2960	15	79990
	FF	36582	6783	6635	47	192026
4.5σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11001	35805	3194	15	84538
	H6	11188	36174	2638	15	73550
	FF	37209	6835	5956	47	178446
4σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11185	35974	2841	15	77478
	H6	11342	36306	2352	15	67830
	FF	37801	6917	5282	47	164966
3.5σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11368	36150	2482	15	70298
	H6	11547	36426	2027	15	61330
	FF	38434	6981	4585	47	151026
3σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11543	36630	2127	15	63198
	H6	11711	36551	1738	15	55550
	FF	39069	7054	3877	47	136866
2.5σ	H1	0	50000	0	0	1
	H2	0	50000	0	0	1
	H3	0	50000	0	0	2401
	H4	1	49999	0	0	3160
	H5	11742	36479	1779	15	56238
	H6	11876	36704	1420	15	49990
	FF	39662	7163	3175	47	122826

TABLE XII

Simulation savings for different guard band scenarios

No. parameters	Guard band/σ_{RMS}	Simulation savings
4	2.5	27.08
	3	24.45
	3.5	22.31
	4	20.57
	4.5	19.09
	5	17.81
6	2.5	21.38
	3	19.14
	3.5	17.35
	4	15.83
	4.5	14.62
	5	13.54

Figure 23 compares the error in fail probability comparison (50K MC simulation results as base) between proposed approach (guard band of $2.5\sigma_{RMS}$) and the method presented in [31] for all the fault scenarios in the dictionary and Fault free circuit. To ensure a fair comparison, the number of circuit simulations required to compute the JPDF for each fault in Kernel based density estimation approach is kept same as the number of simulations required by our method for that particular fault. The proposed method performs better than the kernel based density estimation for faulty scenarios and the difference is significant for the fault free case.

For fault scenarios H1 and H2, since the mean values of the response are more than 10σ from the nominal value of the fault free circuit, we directly classify all the circuit instances as failing. For these faults, both methods are very close to the classifications obtained through Monte-Carlo simulations. For faults H3, H4, H5, H6 our method performs slightly better than kernel density estimation. Even though the error is less than 0.7% in kernel based method, the number of

misclassified circuit instances is in the order of around 7,000 out of a million. For the fault free case our method offers higher accuracy and the error in the kernel based method is around 3%.

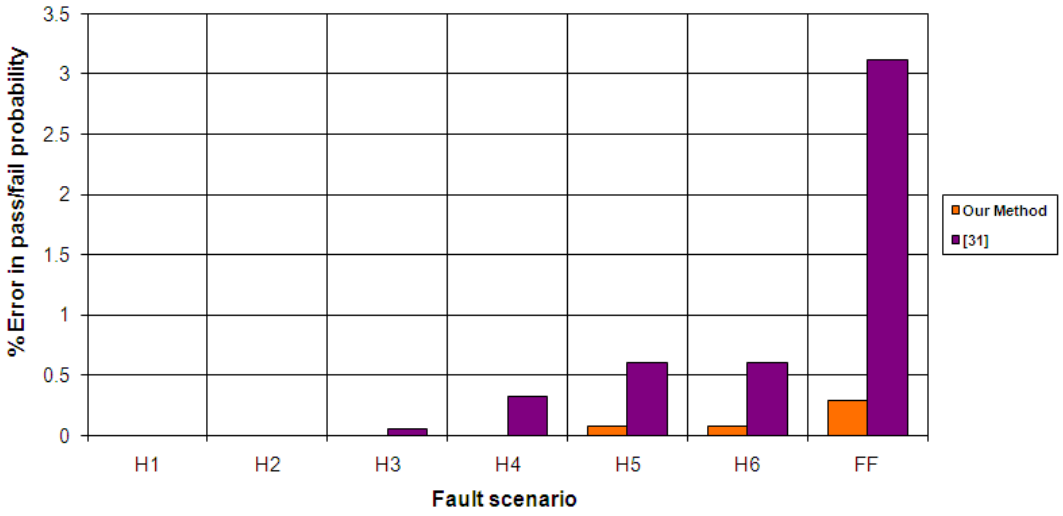

Fig. 23. Accuracy comparison between the proposed approach and method in [31] for four parameter case.

Chapter 7

CONCLUSION

Due to the increasing process variability with scaling technologies, the nature of the response of the analog/RF circuits has become probabilistic in nature. Monte Carlo analysis takes process variations into account but present a large simulation overhead. Our approach addresses this issue by taking process variations into account and constructs a suitable model based on the allowable error in test statistics computation. Some of the applications of this approach would be a quick and a firsthand estimation of the Yield and Fault coverage statistics that could be easily integrated into the design flow.

In this work we propose two approaches to evaluate the test metrics. The first method uses an adaptive model order selection technique with the model order determined by the error budget. The second method uses hierarchy in process variations and modeling to compute the test metrics with increased accuracy.

The first method uses a top down approach, where in we start with a required accuracy on test metric computation. Based on this error budget we estimate the coefficients in first order using robust regression techniques. In case the linear model does not satisfy the error budget, we move to second-order modeling and once again use robust regression techniques to obtain the coefficients. To compute the cross terms we solve a system of linear equations and choose the best coefficient set based on the proposed

methodology. Experiments on an LNA and a Mixer show that we could potentially obtain a speed up of 7.54x and 7.03x for a chosen threshold when it comes to the computation of the pass/fail probability.

The biggest limitation of the first method is the maximum achievable accuracy in terms of test statistics evaluation. The constraint on accuracy can be attributed to modeling the entire input space. We remedy this problem to a good extent by constructing localized linear models based on the hierarchy in process variations: die-to-die variations, where the number of variables is small and limited but the variation amount is large, and within die variations, where the number of variables is large and scales with circuit, but the variation amount is small.

We present a two step procedure based on DOE and first order models to response evaluation. The first step uses heuristics based on 7^n DOE levels to classify the circuit instance as certainly passing/certainly failing and ambiguous. The circuit instances in the ambiguous bin are evaluated by constructing localized linear models for within-die variations by using die-die variation instances as fixed points. The proposed method is compared against the recent work on test metrics computation based on adaptive kernel density estimation and our method has been found to perform better especially for the fault free case.

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