# Study of On-Chip Integrated Switched-Capacitor Voltage Regulator

by

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ABSTRACT

Power management circuits have been more and more widely used in various applications, while providing fully integrated voltage regulation remains a challenging topic. Switched-capacitor (SC) voltage converters have received attentions in integrated power conversion for fixed-ratio voltage conversions with good efficiency and feasibility of integration. During my PhD study, an on-chip current sensing technique is proposed to dynamically modulate both switching frequency and switch widths of SC voltage converters, enhancing fast transient response and higher efficiency across a wide range of load currents.

In conjunction with SC converters, a low-dropout regulator (LDO) is implemented which is driven by a push-pull operational transconductance amplifier (OTA), whose current is mirrored and sensed with minimal power and efficiency overhead. The sensed load current directly controls the frequency and width of SC converters through a voltage-controlled oscillator (VCO) and a time-to-digital converter, respectively.

Theoretical analysis and optimization for SC DC-DC converters have been presented in prior works, however optimization of different capacitors, namely flying and input/output decoupling capacitors, in SC voltage regulators (SCVRs) under an area constraint has not been addressed. A methodology to optimize flying and decoupling capacitance for area-constrained on-chip SCVRs to achieve the highest system-level power efficiency. Considering both conversion efficiency and droop voltage against fast load transients, the proposed model determines the optimal ratio between flying and decoupling.

Based on the previous design, a fully integrated switched-capacitor voltage regulator with voltage comparison and on-chip lossless current sensing control is proposed.

Based on the voltage comparison result and sensed current as the load current changes, the frequency of the SC converters is modulated for optimal efficiency.

In 65nm CMOS, the regulator is implemented with MIM-capacitor, targeting 2.1V input voltage and 0.9V output voltage. According to the measurement results, the proposed SC voltage regulator achieves 69.6% peak efficiency at 60mA load current, which corresponds to a 4.2mW/mm$^2$ power-area density and 12.5mW/nF power-capacitance density. The efficiency across 20mA to 92mA regulator load current range is above 62%. The steady-state output voltage ripple across 22x load current range of 3.5mA-76mA is between 50mV to 60mV.

DEDICATION

To my PhD advisor and committees

To my family

TABLE OF CONTENTS

Page

CHAPTER Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

Figure Page

# CHAPTER 1

# INTRODUCTION

## 1.1 The Applications of Power Management Integrated Circuits

Power management Circuits have been widely used in a wide variety of areas in industry and civil applications, such as high-performance servers, information security systems, vehicle electronic systems and all kinds of mobile electronic devices. For common electronic systems, there are different kinds of power management circuit providing power delivery, conversion and regulation function for battery, CPU, non-volatile memory, display, wireless adaptor, etc. Figure 1.1 shows some examples with the applications of power management ICs.

The general design considerations of power management IC include the input and output voltage, the load current, the power efficiency, the voltage ripple of the output voltage, the load transient and the chip area, etc.

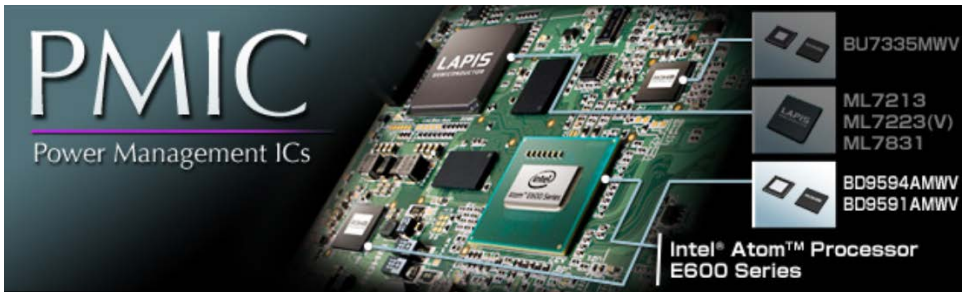





Figure 1.1 Applications of power management integrated circuit (the images are obtained from Google image search)

## 1.2 The Fundamentals of Integrated Switched-Capacitor Voltage Converters

Switched-capacitor voltage converters have been more and more widely applied in different kinds of power management circuits. The advantages of switched-capacitor voltage converters include feasibility of full integration, good efficiency at fixed conversion ratio, minimal radiated EMI, simpler implementation, low cost, compact, etc. Switched-capacitor voltage converters operation in voltage mode, in which the voltage of the capacitors does not change abruptly. The capacitor(s) are charged in a certain portion(s) of the clock period and are discharged the other(s), as shown in Figure 1.2. Due to such operation, the switched-capacitor voltage converters offer good performance at fixed conversion ratios.

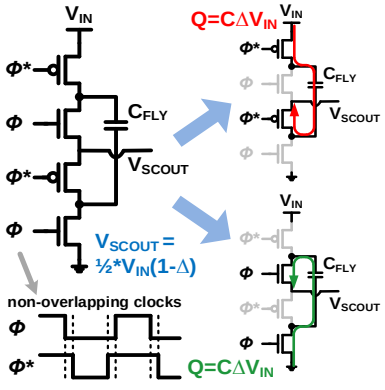



Figure 1.2. Basic operation of a 2:1 SC voltage

The common topologies of the switched-capacitor voltage converters include the ladder topology, the Dickson charge pump, the Fibonacci Topology, the series-parallel topology and the doubler topology, as shown in Figure 1.3.

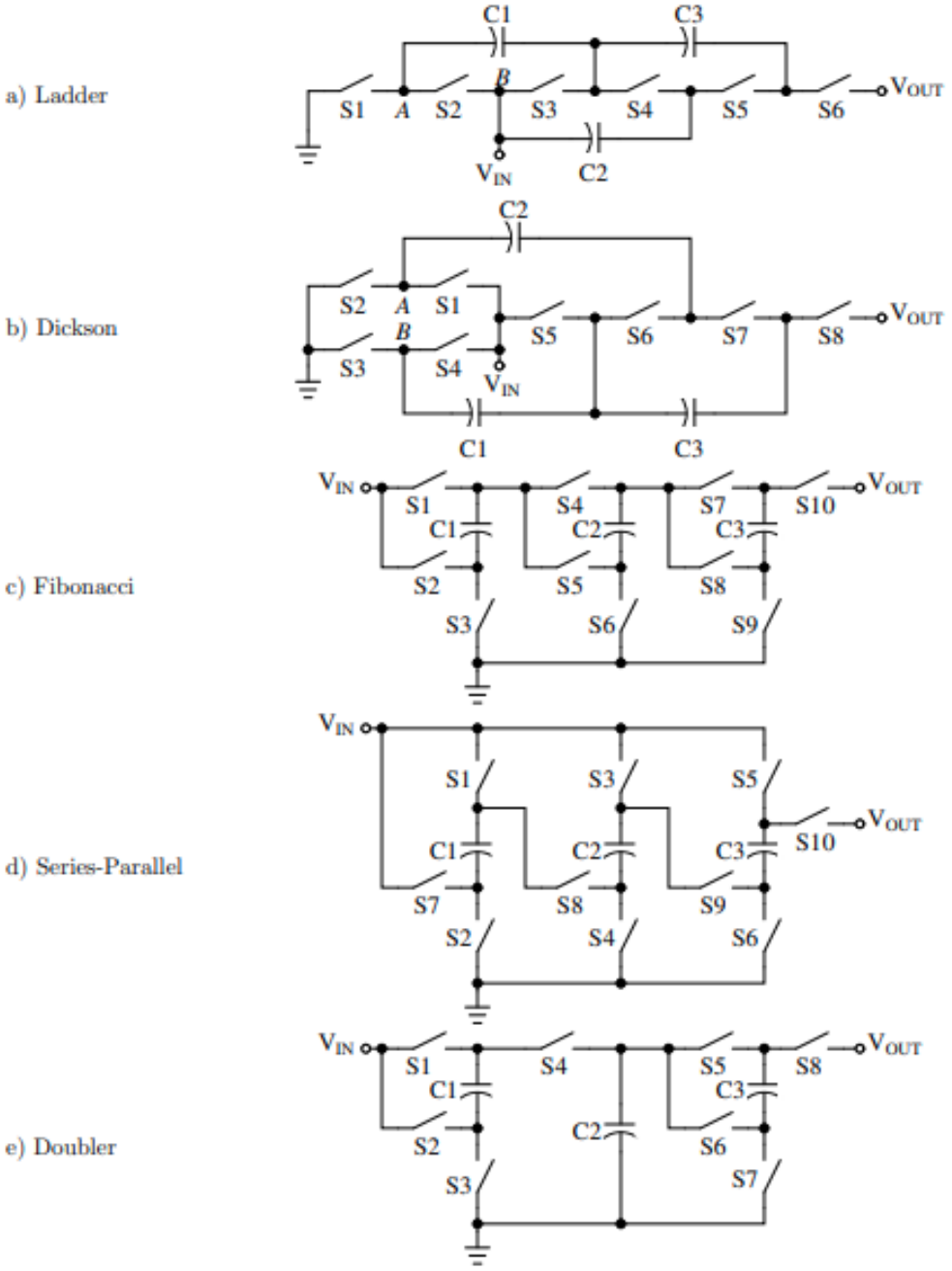



Figure 1.3. Common topologies of switched-capacitor voltage converters

The efficiency and power density of an integrated SC voltage converter is directly influenced by the capacitor technology of the CMOS process, besides the conversion ratio and topology. Different capacitor technologies, such as MIM (metal-insulator-metal), MOS (metal-oxide-semiconductor), and DT (deep trench) offer different trade-offs between efficiency and current density options for SC converter design. The sources of power loss in SC voltage converters include the following [10-12]:

(1) charging and discharging behavior of the flying capacitor causes slow switching loss (SSL) due to the voltage ripple at the output, which is inversely proportional to the switching frequency and flying capacitance.

(2) current through the on-resistance of the non-ideal switches results in fast switching loss (FSL), which is proportional to the switch width.

(3) parasitic capacitance of the flying capacitor causes bottom-plate loss, because it is charged from the supply in one phase and discharged to ground in the other phase. Such loss is proportional to the total bottom plate capacitance as well as the switching frequency.

(4) the parasitic capacitance of the SC switches causes switching loss due to its charging and discharging behavior, which is proportional to both the switch width and frequency.

# CHAPTER 2

## SURVEY OF SWITCHED-CAPACITOR VOLTAGE REGULATOR

## 2.1 Comparison of Different Topologies of Voltage Regulators

There have been a wide variety of power management circuits, such as non-isolated and isolated buck/boost voltage converters, linear voltage regulators, switched-capacitor voltage converters, etc.

Traditional buck/boost converters with high-quality off-chip or package-integrated inductors [1,2] can provide high power efficiency while on-chip buck converters [3,4] still suffer from limited efficiency due to low-quality inductors. Integrated linear regulators are usually applied on-chip and offer excellent regulation against load changes while the efficiency is intrinsically low when the input and output voltage has a larger difference [5,6]. In contrast, switched-capacitor converters can be fully-integrated [7-15] and achieve good efficiency at fixed conversion ratios even when the input and output difference is large. In addition, modern high-quality on-chip capacitors make on-chip SC converters have both high efficiency and power density.

## 2.2 Prior Works on Switched-Capacitor Voltage Regulators

### 2.2.1 "A Fully-Integrated Switched-Capacitor 2:1 Voltage Converter with Regulation Capability and 90% Efficiency at 2.3A/mm$^2$" by Leland Chang et al.

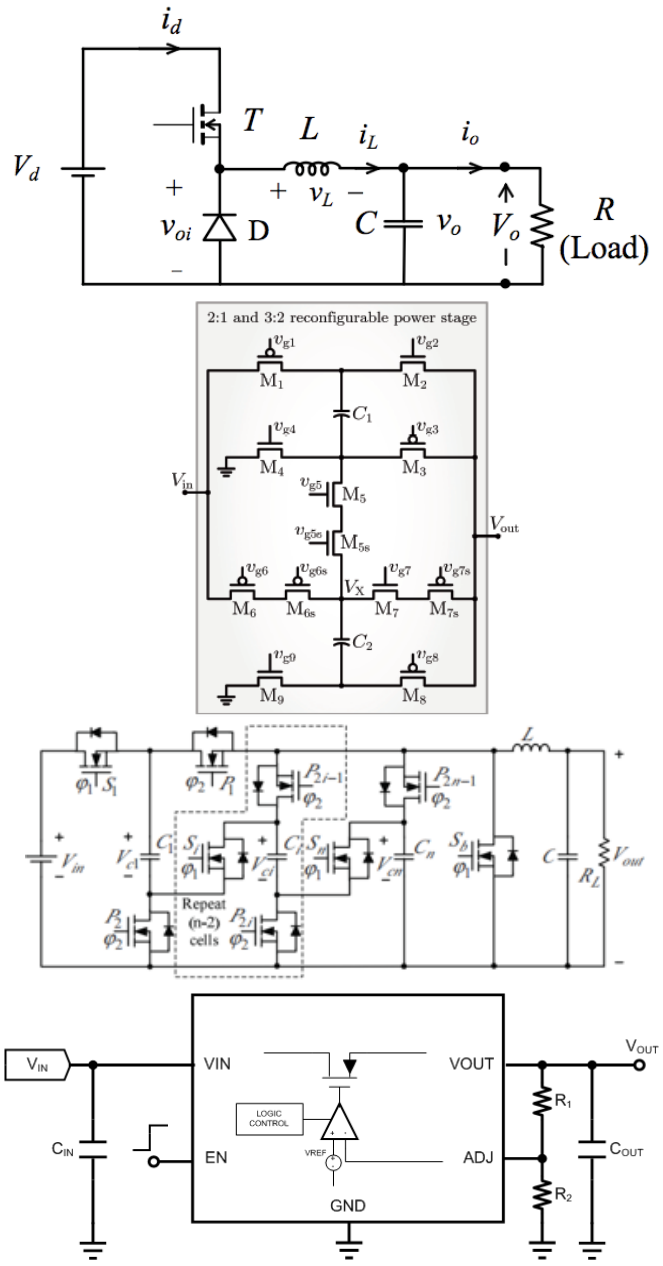
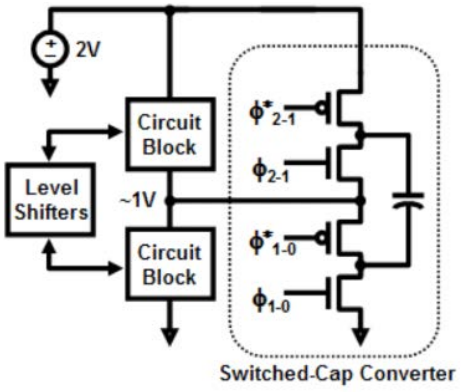
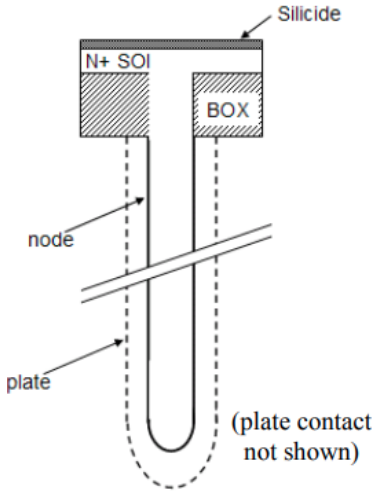



Figure 2.1 Different types of voltage regulators: (a) current mode buck converter (b) switched-capacitor voltage converter (c) Hybrid switched-capacitor voltage converter (d) Linear regulator

"This work has a 2V-to-0.95V 2:1 switched-capacitor design, which is implemented in 45nm SOI CMOS. The capacitor is on-chip deep-trench capacitor which has high quality and capacitance density. The SC converter operates at 100MHz frequency. This design had

achieved 90% efficiency with 2.3A/mm$^2$ power density. This design has self-regulation capability, which allows the proposed circuit to be combined with stacked voltage domain techniques to improve conversion efficiencies. At the cases that the loads are imbalanced, the SC converter provides mismatch current up or down the stack at ~90% efficiency. At the case of full mismatch (one load is off), the circuit behaves similarly to the step-down circuit at 100MHz. At the case that no mismatch current is needed, 96% efficiency is measured. At 20MHz, the efficiency at zero mismatch current is 99%; however, as the output current is reduced, the efficiency for maximum mismatch is degraded. When the frequency is regulated according to load, optimal average efficiency can be attained."



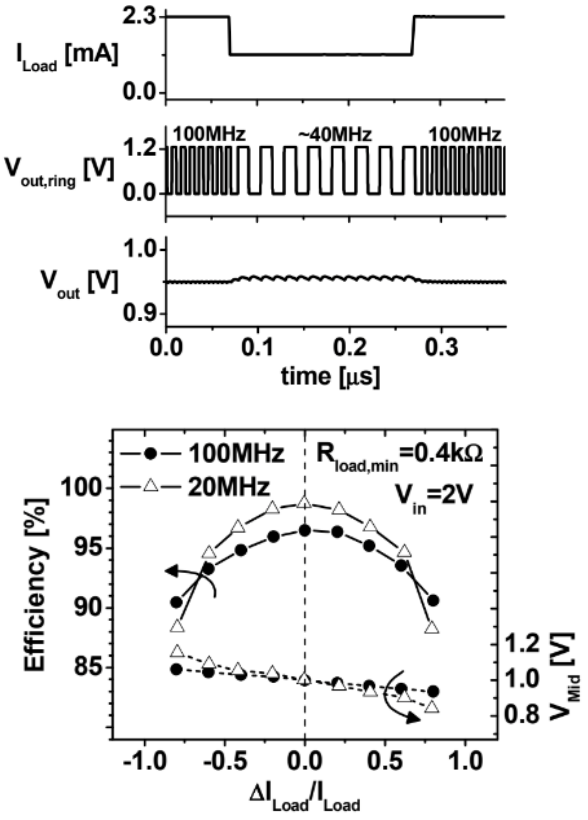


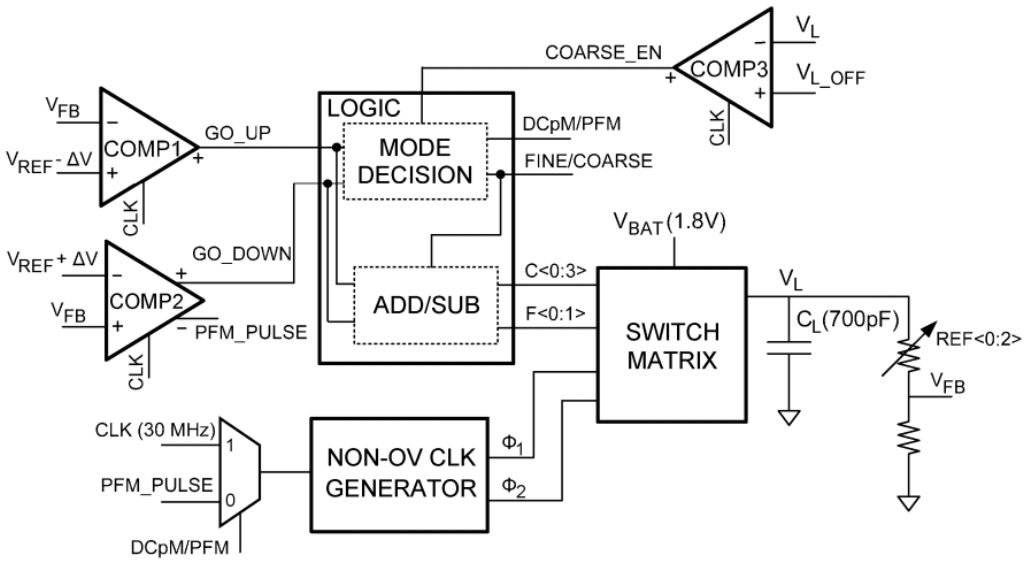

Figure 2.2 The circuit diagram, the capacitor structure the frequency response and efficiency plot of the design

## 2.2.2 "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS" by Yogesh K. Ramadass, et al.

"This work proposed a capacitor-based fully-integrated switching regulator in 45 nm standard CMOS technology to combine the advantages of the regulation techniques of the SC converter. The proposed design uses 30 MHz switching frequency. The capacitor is on-chip poly-Nwell capacitors for both the charge-transfer and the load capacitors. The design uses a digital capacitance modulation control mechanism to maintain regulation against

load current changes, which is a quite different scheme from the traditional PFM and PWM control methods. In this design, the frequency is kept constant, while due to the change of capacitance with load current, the switching and bottom-plate loss can be scaled. Thus the regulator achieves high efficiency across different load current levels while maintaining predictable switching noise behavior. This proposed switching regulator was designed as the power for mixed-signal modules inside a fully-integrated FM transceiver, which can be used for other applications as well.

This fully-integrated switched-capacitor DC-DC converter design is implemented in 45 nm digital CMOS technology. The converter chip area is only 0.16 $mm^2$ and delivered a programmable sub-1 V power supply with efficiency as high as 69% for load currents between 100 A and 8 mA. There are multiple modes of operation were within the converter to enable fast transient response, which can also keep the ability to settle within narrow hysteretic bands."



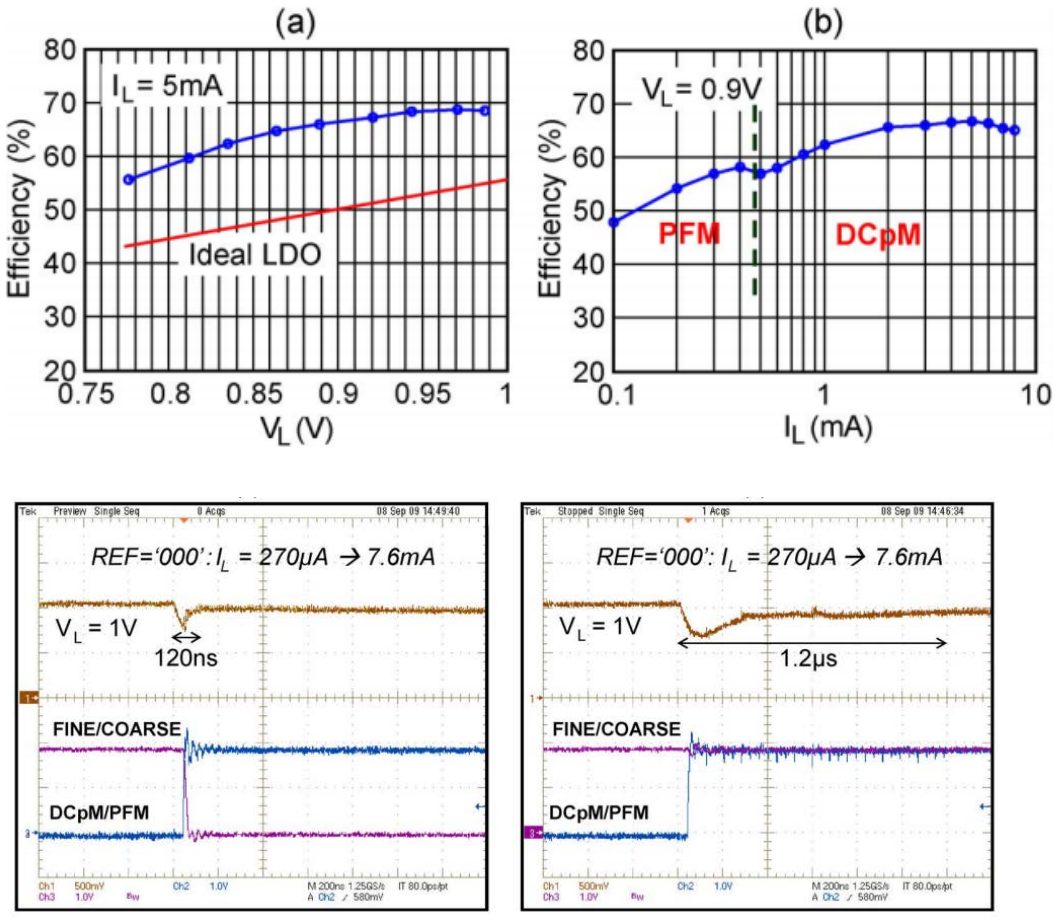



Figure 2.3 The circuit diagram, the efficiency, and load transient result of this work

## 2.2.3 "A Monolithic Current-Mode CMOS DC–DC Converter With On-Chip Current-Sensing Technique" by Cheung Fai Lee, et al.

"This work proposed a monolithic current-mode CMOS DC–DC converter with integrated power switches and on-chip current sensor for feedback control. The proposed accurate on-chip current sensor can sense the inductor current, and by combining with the internal ramp signal, it can be used for current-mode DC–DC converter feedback control. Moreover, there is no external components and no extra I/O pins used for the current-mode controller.

This design is fabricated in 0.6um CMOS process and the measured absolute error between the sensed signal and the inductor current is less than 4%. The converter with the on-chip current sensor operates from 300kHz to 1MHz frequency. The input voltage is from 3 to 5.2V and it is designed for single-cell lithium-ion battery supply applications. The measured output ripple voltage is about 20 mV with a 10-uF off-chip capacitor and 4.7-uH off-chip inductor. The power efficiency is over 80% for load current from 50 to 450 mA."

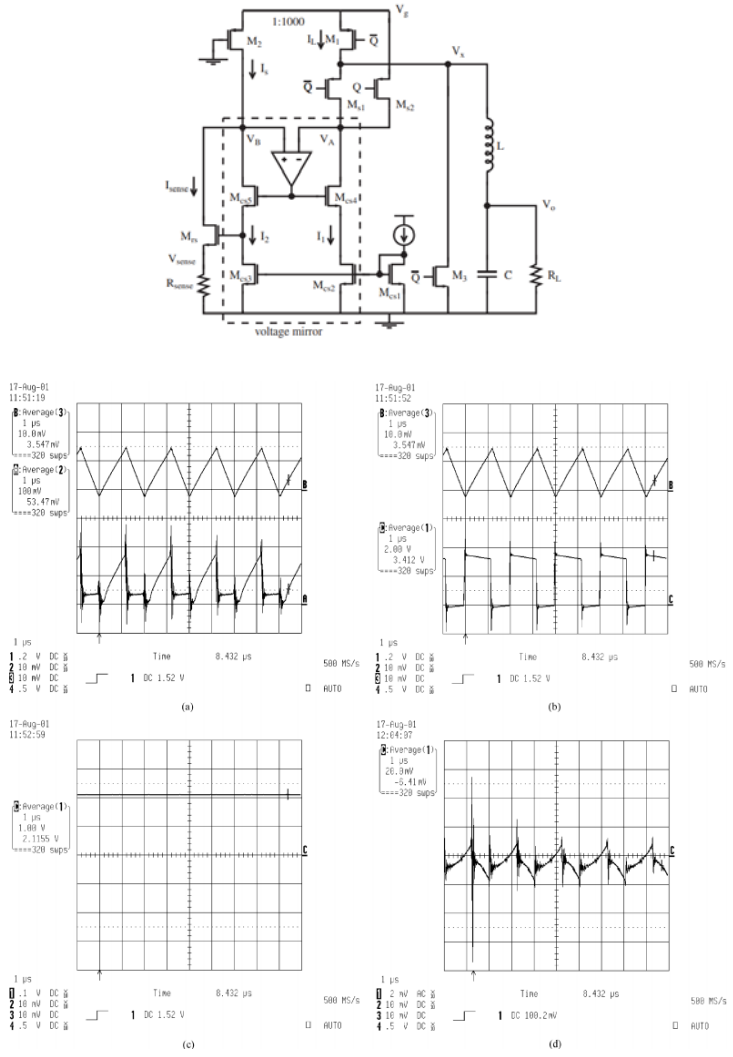



Figure 2.4 The circuit of the proposed regulator and the steady-state measurement results with 2.1-V output voltage (Duty ratio >0:5): (a) the inductor current (curve B) and the sensing voltage (curve A); (b) the inductor current (curve B) and V in Fig. 5 (curve C); (c) the DC output voltage; and (d) the output ripple voltage.

### 2.2.4 “A Low Ripple Switched-Capacitor Voltage Regulator Using Flying Capacitance Dithering”, by Suyoung Bang, et al.

“This work proposed a switched-capacitor voltage regulator (SCVR) that dithers flying capacitance to reduce output voltage ripple. The benefits of such ripple reduction are investigated. In the proposed technique, maximum frequency is applied to the SC converters. When the load current changes, the flying capacitance for different phases is adjusted through comparators and a digital controller. The proposed design is fabricated in 65nm process. The design consists of a 40-phase SCVR with 4b capacitance modulation (CM) and a 2:1 conversion ratio.

In this work, the number of phases for CM is adjusted in which the number of phases must be reduced to achieve a small flying capacitance, which can actually degrade output ripple. In order to optimize the regulator output ripple in closed-loop SC converters, this work proposes dithered-capacitance modulation (DCM). The flying capacitance is adjusted on-demand with a fixed frequency used for the SC converter. A delay-locked loop (DLL)Clocks is used to generate the clocks for 40 SC converter phases, so significant phase interleaving can be used to maximize temporal distribution of the flying capacitance charge transfer.

For ripple measurement, dedicated on-chip measurement circuits is used and the load performance monitoring were included to accurately assess the magnitude and impact of ripple reduction. According to the measurement results, the ripple magnitude at 2.3V input and 1V output is 6-16mV for 11-142mA load. The peak efficiency is 70.8% and the corresponding power density is 0.187W/mm$^2$.”

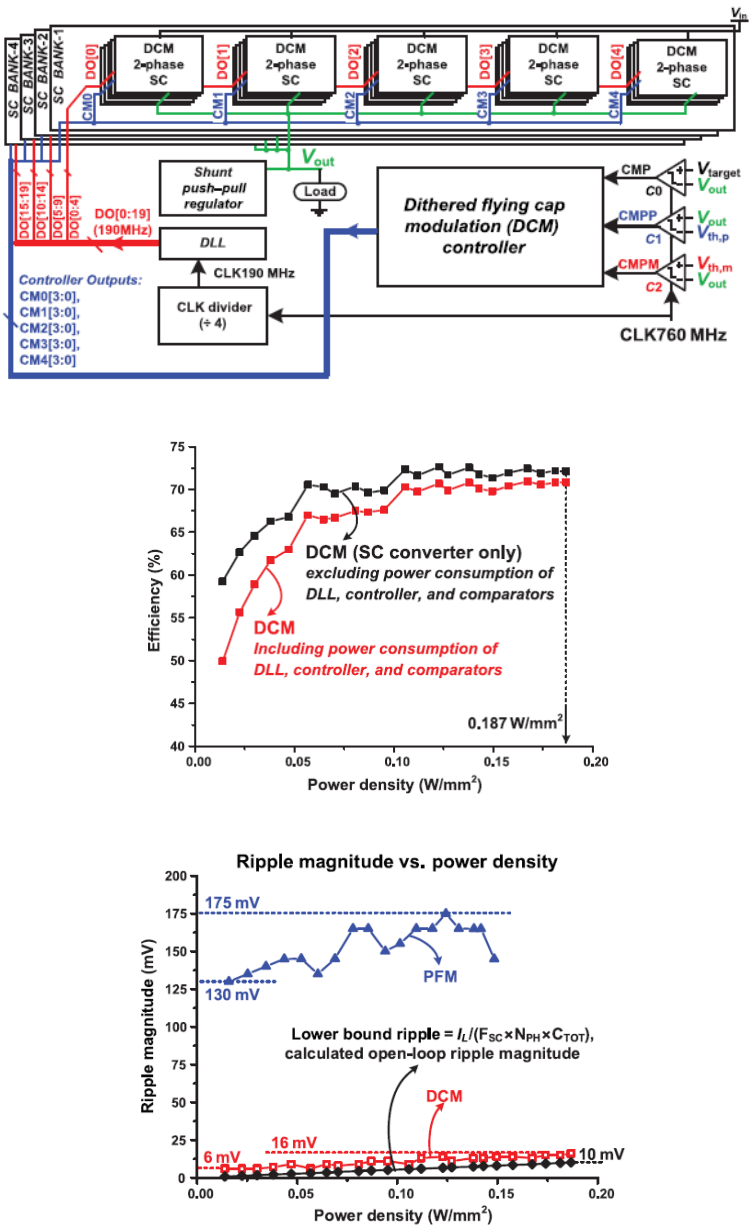



Figure 2.5 The circuit diagram, the measured efficiency and measured ripple magnitude

# CHAPTER 3

# ON-CHIP CURRENT-SENSING AND WORKLOAD OPTIMIZATION

## 3.1 Single-Phase Switched-Capacitor Voltage Converter Optimization

In this section, we investigate optimization of a single-phase 2:1 SC voltage converter. The results will be applied to the multi-phase interleaved SC converter design.

### 3.1.1 Operation of 2:1 Switched-Capacitor Converter

A 2:1 SC down-converter operates with non-overlapping clock signals applied at different switch devices [7, 11, 12], as illustrated in Figure 3.1(a). In one state, the top and bottom plate of the flying capacitor is connected to the input voltage (VIN) and the output voltage (VOUT), respectively. In the other state, the top and bottom plate of the flying capacitor is connected to the output voltage (VOUT) and ground, respectively. Continuously switching back and forth between the two states, the input voltage is effectively divided by half, providing a 2:1 down conversion. To maximize the conversion efficiency, the power loss due to switch devices, drivers, bottom-plate capacitance, and inherent ripple should be balanced and minimized based on load current (I_LOAD).

Our target load current is 1A, which would be similar to those of mobile application processors (AP). Assuming that leakage power could consume at least 10% of the total AP power, the SC converter should adapt to 10X range of current from 0.1A to 1A. With target load current at given VIN and VOUT voltages, the design parameters of the SC converter include switch width, switching frequency, and flying capacitance, which affect the overall efficiency and current density.

### 3.1.2 Optimal Efficiency and Power Density Trade-off

Assuming that 17 SC converter phases will be interleaved to reduce inherent ripple (detailed description in Section III), the single-phase SC converter should produce output current of 58.8mA (1A/17). With ideal voltage sources of 2.1V and 1V connected at VIN and VOUT, respectively, we performed a coarse three-dimensional sweep of switch width, switching frequency, and the flying capacitance (CFLY). For five CFLY values, both the switch width and frequency are swept in simulations using 32nm technology, where the flying capacitors are implemented with the deep trench capacitors. Conservatively, if 20% of the total regulator area is devoted to circuits other than CFLY, 6W/mm2 power density could be achieved at this design point.

### 3.1.3 Frequency and Width Optimization with Load Current

The authors in [7] showed that both the optimal switch width and switching frequency is proportional to (I_LOAD)^(2/3). More recently, it has been shown that in the case of output-resistance constrained 2:1 SC converters, switch-width and switching frequency should both scale linearly with target output resistance [21]. With the CFLY from Section II.B, we explored the two-dimensional design space of frequency and switch widths of the 2:1 SC converter in 32nm technology for load currents from 100mA to 1A (Figure 3.2), to quantify the importance of such co-optimization. As in Section II.B, VIN and VOUT are connected to voltage sources, and power losses for control or regulation were not considered.

We first found the optimal width and frequency for the maximum current of 1A, and the resulting width (Wopt@Imax) was used as the total width of the on-branch and off-branch of the switches (Figure 3.1(a)), such that the effect of parasitic capacitance is captured in

width modulation. Through stacking, since no transistor in the converter or driver sees voltage larger than (VIN-VOUT), only thin-oxide devices are used without reliability concerns.

The two design parameters were then swept to find out the optimal frequency and width that led to the best efficiency at different load current values, and the results are shown in Figure 3.1(b). Figure 3.1(c) shows the relative value of both switching frequency and switch width of SC converters for the 10X range of load currents, where 10-20X adaptation in frequency and width is shown to be necessary to optimize the efficiency across the target load range.

## 3.2 Fully-Integrated Switched-Capacitor Voltage Regulator with on-Chip Current Sensing

### 3.2.1 17-Phase SC Converter

Starting from the single-phase SC converter optimized in Section II, multiple-phase interleaving was adopted to reduce the inherent output voltage ripple and enhance response time [7, 10, 13]. The clock signals of multiple converter phases were driven by a 17-phase voltage-controlled oscillator (VCO), whose frequency is controlled by current-starved footers and headers. The number of phases was chosen as 17, since it showed a good trade-off between ripple reduction and converter design overhead. The number of configurable switch widths was chosen to be eight (with half-LSB switch always on), to balance width configurability and parasitics of the switch devices. Using eight discrete widths, there was

<0.3% efficiency degradation from the ideal achievable efficiency with continuous widths in Figure 3.1(b).

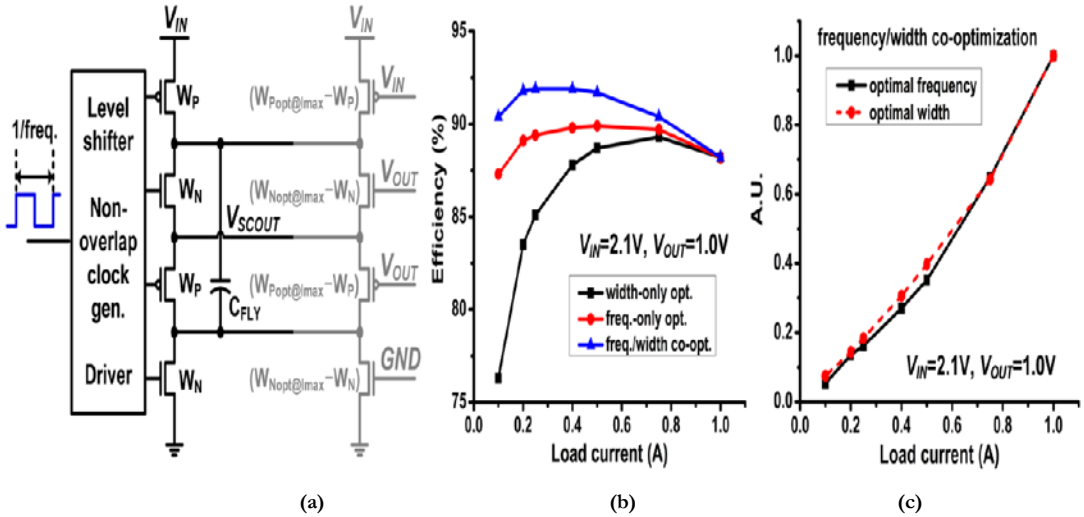



Figure 3.1. (a) 2:1 switched-capacitor converter schematic with on-/off-branch is shown. (b) Ideal efficiency comparisons with optimal frequency and/or width modulation for 100mA-1A load currents are shown. (c) Relative value of optimal frequency and width for 100mA-1A load currents

### 3.2.2 On-Chip Current Sensing and LDO Regulator

To sense the load current, we chose to use a LDO regulator in conjunction with step-down SC converters [9, 19], which also provide benefits such as fine-grain voltage output and ripple minimization. The current sensor is realized by a parallel PMOS transistor that is matched to the power PMOS transistor in the LDO regulator with a 1:1000 size ratio [18]. As shown in Figure 3.2, the error amplifier in the LDO regulator controls the strength of the power transistor such that the output voltage (VOUT) tracks the desired reference

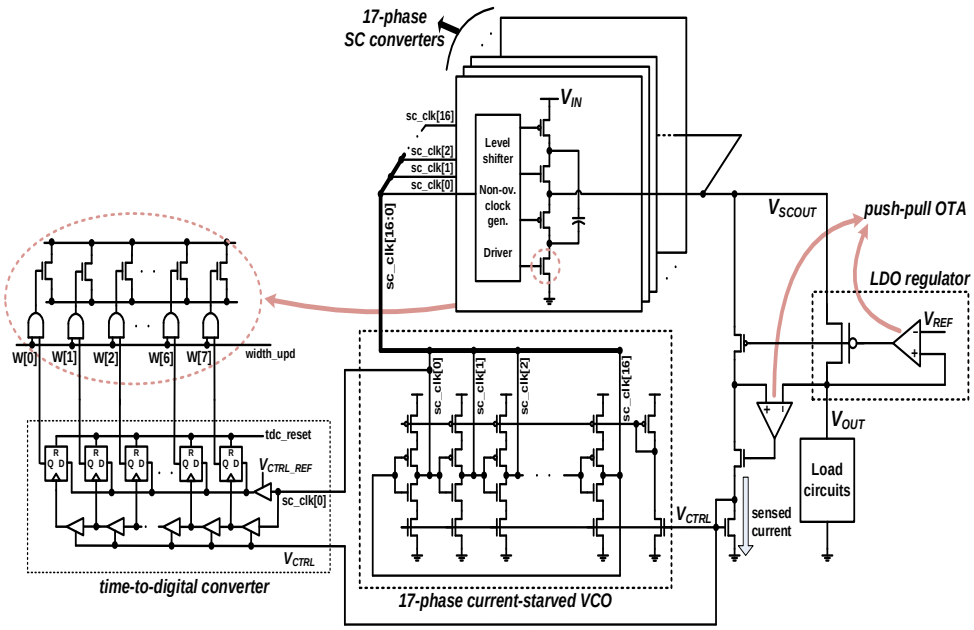



Figure 3.2 The circuit diagram of the proposed SC regulator

voltage (VREF). To accurately sense the load current with a linear ratio, another operational amplifier is employed to keep the drain voltages of the power and sensing PMOS transistors very close to each other. For the frequency modulation, the sensed load current directly controls the delay of the VCO, which modulates the frequency of the 17-phase switched-capacitor converters. For the width modulation, the sensed current goes through a time-to-digital converter that provides an 8-bit thermometer code that controls the switch widths of all 17 phases.

### 3.2.3 Push-pull OTA with Channel-Resistance-Insensitive Small-Gain Stages

The error amplifiers in the proposed design largely affects the performance of the voltage regulator, including DC error, voltage droop, and steady-state ripple of the regulator output. The short-channel effects in the 32nm process must be considered carefully in the operational amplifier design to ensure high specifications such as gain, bandwidth, and

phase margin. To that end, we present a differential operational transconductance amplifier (OTA) with a push-pull output stage. Differential implementation has been adopted in this design instead of conventional single-ended cascaded gain-boosting stages.

Figure 3.3 shows the proposed design of a push-pull OTA that provides gain boosting, wide output swing, as well as a push-pull output stage for symmetric ripple cancellation. In the differential input stage, negative-gm method is applied for gain-boosting by increasing the output resistance. The intermediate cascaded stages are channel-resistance-insensitive, which offers small gain and less-dominant poles and zeros to keep sufficient bandwidth while enhancing the DC gain [20]. Meanwhile cascode tail-biasing in these small-gain stages alleviates the, current mismatch issue in the SOI process.

Due to different emphasis on the two error amplifiers, trade-offs are made to properly design the two OTAs separately. First, the LDO error amplifier requires high DC gain, high bandwidth, and moderate phase margin to ensure output voltage accuracy and fast response to load transients. On the other hand, the error amplifier employed for current sensing requires higher phase margin to maintain the current sensing loop with minimal noise and ripple, especially on the feedback control voltage from the diode-connected NMOS transistor. To that end, the error amplifier for the LDO contains four cascaded small-gain stages while the error amplifier for current sensing was designed to have three small-gain stages, where the degraded loop gain due to less cascading still offers a current sensing accuracy of 97.3% to 100% across the load range, as shown in the experimental results. Bias currents of the push-pull output stage of the error amplifiers are set properly to satisfy the stability and dynamic performance requirements of both the LDO and the current sensing feedback loops.

### 3.2.4 Voltage-Controlled Oscillator

As shown in Figure 3.2, the sensed current is mirrored and directly drives the footer and header of the current-starved voltage-controller oscillator. Through this tight integration, the sensed current promptly modulates the SC converter frequency in a continuous fashion. The footers and header sizes determine the amount of starved current for charging and discharging the output capacitance of each inverting stage, and the inverters Push-pull OTA Performance that reside between the header and footer are sized accordingly to obtain the targeted frequency range with the feedback control voltage.

### 3.2.5 Time-to-Digital Converter

To perform the discrete switch width modulation, the time-to-digital converter shown in Figure 3.2 converts the sensed current into digital signals that turn the switches on or off. The chain of the eight delay stages are controlled by the same feedback voltage used in frequency modulation. Each delay stage is equivalent to a single VCO phase, varying with the load current through the feedback control voltage. This is compared with a reference delay and counts how many flip-flops the delay driven by current sensing will go through in a given time. Instead of converting linear delay into linear digital values, this design converts linear current, to which the corresponding delay is inversely proportional, into linear digital values.

## 3.3 Simulation Results

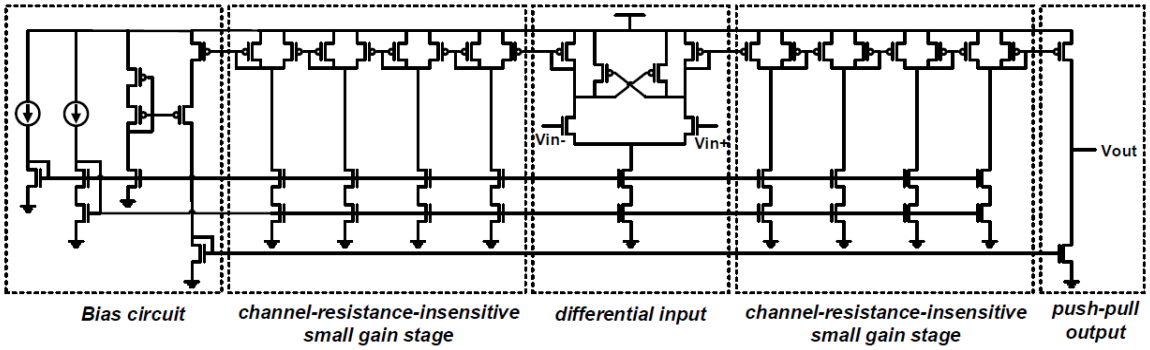



Figure 3.3. Push-pull OTA with channel-resistance-insensitive small-gain stages.

The proposed integrated SC voltage regulator with on-chip current sensing was designed and simulated in 32nm SOI CMOS with deep trench capacitors. We also implemented a baseline switched-capacitor voltage regulation scheme that performs pulse frequency modulation [10, 13] for comparison. Regulator efficiency, voltage droop against load transients, and steady-state ripple across 10X range of load currents will be reported in this section.

### 3.3.1 Push-pull OTA Performance

Figure 3.4 shows the stability simulation results of the proposed push-pull OTA connected to the LDO regulator for maximum and minimum load currents. The LDO error amplifier design achieves a DC gain of 57.2dB with 393.2MHz bandwidth, and 62 degree

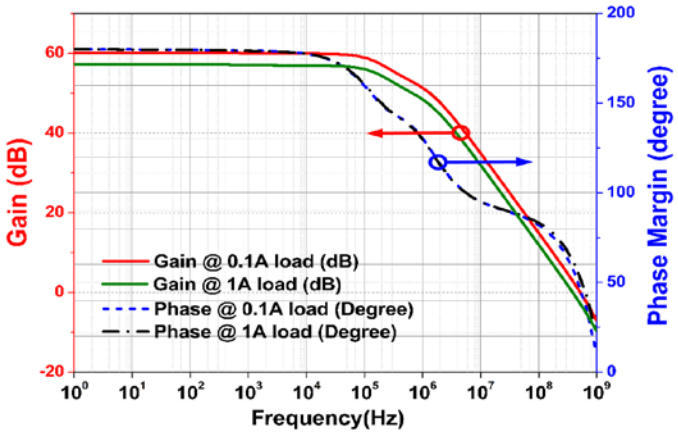



Figure 3.4. Loop stability simulation of the LDO push-pull OTA at 0.1A and 1A load currents.

of phase margin at 1A load current, while for 100mA load current, 60.2dB DC gain with 534.4MHz bandwidth, and 46 degree of phase margin are achieved. In the current sensing OTA, for 1A load current, the achieved bandwidth and phase margin are 307.4MHz and 78.5 degree, with a DC gain of 35.7dB, and for 100mA load current, these values are 579.0MHz and 52.8 degree, with a DC gain of 43.1dB. The power consumptions of the error amplifiers for the LDO and current sensing are 751µW and 622µW, respectively.

### 3.3.2 Regulator Efficiency Across a Wide Load Range

In Figure 3.5, the output voltages of the SC converter and the LDO regulator, as well as the efficiencies of the SC converter, LDO regulator, and the entire regulator are shown. Overall, a nearly constant efficiency of80% is demonstrated across load currents from 100mA to 1A. Targeting 0.95V, the average output voltage DC error of the regulator is kept under 1% across 10X load range.

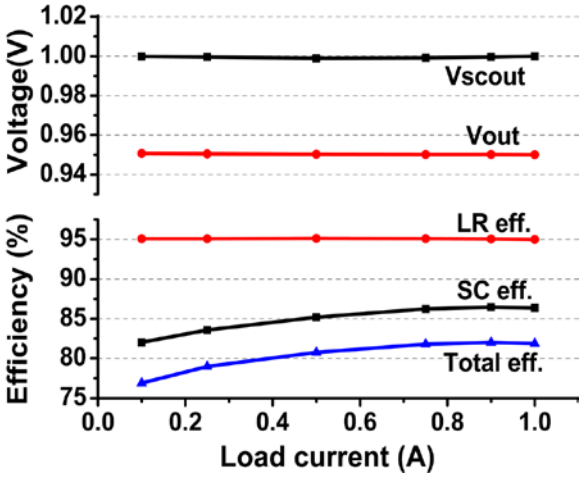



Figure 3.5. Output voltage and efficiency simulation results.

### 3.3.3 Load Transient and Steady-state Regulation

An abrupt load transient was simulated by transitioning the load current from 100mA to 900mA in 10ns (80mA/ns), and the simulation results are shown in Figure 3.6. For the width modulation, we assumed that an architectural preset signal could be provided to the regulator [5] earlier than the worst-case load transient, such that the switch widths are pre-configured to maximum width. The error amplifier output promptly tracks the load current change and the SC converter switching frequency is modulated instantaneously without a high-speed clock. As a result, the proposed SC voltage regulator achieves a fast and stable load transition with 33mV of output voltage droop. Without the architectural preset signal, the worst-case droop was 85mV for 80mA/ns load transient and was 28mV for 16mA/ns load transient. After the load transient occurs, the error amplifiers and the overall regulator promptly stabilize within 15ns.

Figure 3.7 shows the steady-state voltage waveforms from 100mA to 1A of load current in the steps of 100mA. Aided by the proper designs of the LDO and sensing push-pull OTAs, the steady-state output ripple, the feedback control voltage of the sensing circuitry, and the VCO switching frequency are regulated well with minimal noise and ripple. Across the

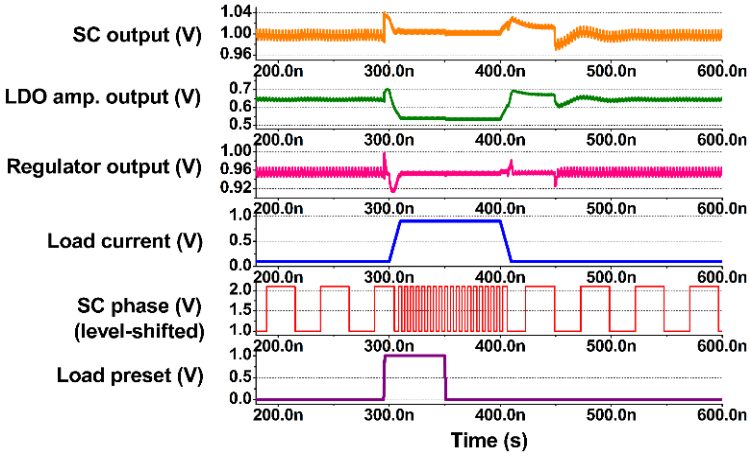



Figure 3.6. Transient response of the proposed SC voltage regulator against an 80mA/ns load transition (100mA to 900mA change in 10ns).

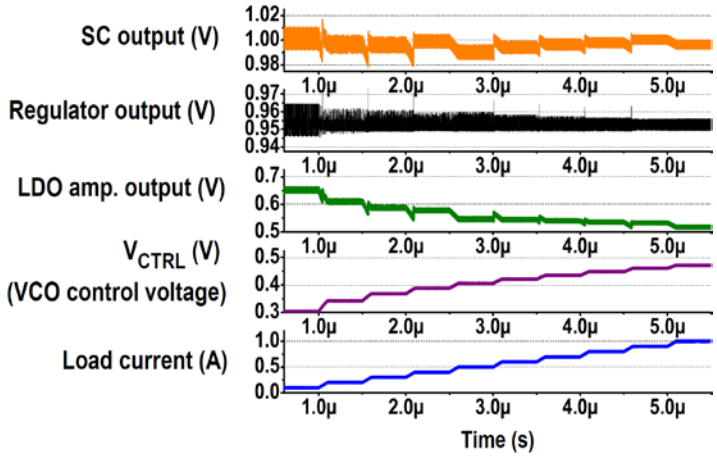



Figure 3.7. Steady-state simulation of the proposed SC voltage regulator. While load current is increased at a step size of 100mA from 100mA to 1A, output and intermediate voltage waveforms

10X range of load currents, the worst-case output voltage (VOUT) ripple is 20mV at 0.1A load.

### 3.3.4 Comparison with baseline SC regulator using PFM

A number of prior works in SC voltage regulation uses pulse frequency modulation (PFM) with a multi-GHz high-speed clocked comparator [8, 9, 10, 13], as illustrated in Figure 3.8(a), which either enables advancing the next SC converter phase or stall the phase operation until VOUT becomes smaller than VREF.

We employed an ideal 3.8GHz clocked comparator, which is equivalent to 17 times the maximum VCO frequency of the proposed design. Without the current sensing circuitry, the clocked comparison against VREF of 0.95V modulates only the switching frequency, while the switch widths are kept at maximum width. Targeting the same VIN and VOUT voltages with the proposed scheme, identical load transients were applied to the baseline PFM regulation scheme, and the simulation results are shown in Figure 3.8(b). The worst-case droop for 80mA/ns load transient is 75mV for the SC converter output, while the

worst-case ripple is 175mV at 0.1A load. Overall, the proposed scheme improved output voltage droop by 2.2X and the output ripple by 8.7X.

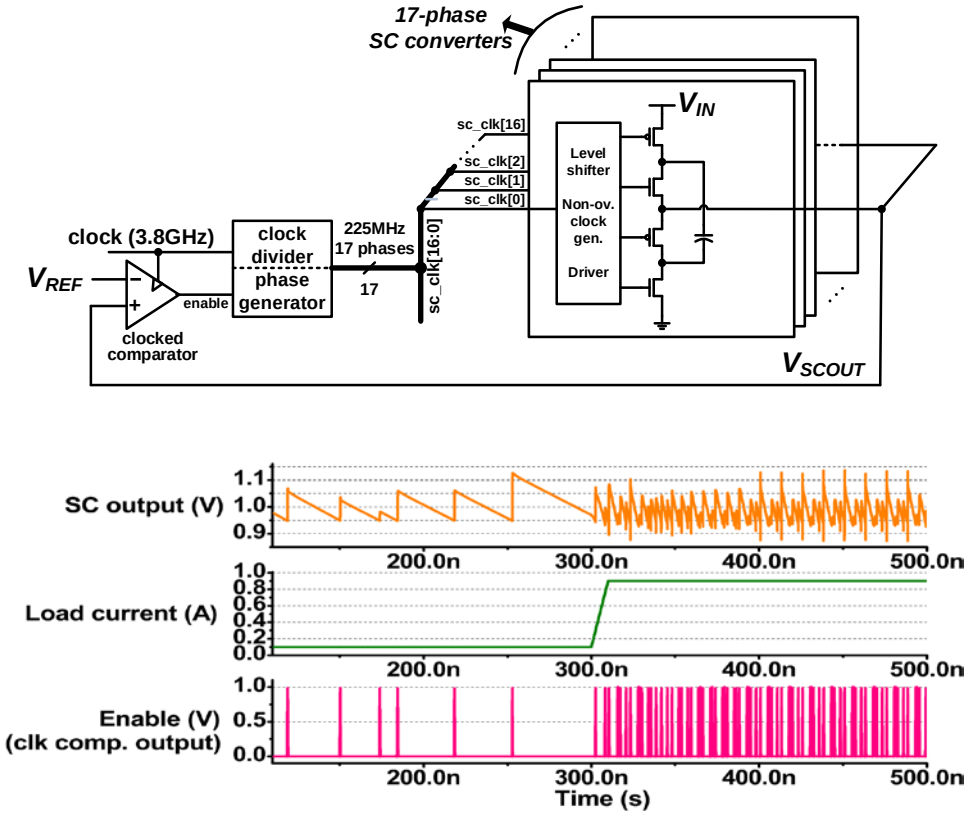



Figure 3.8. (a) Baseline SC regulator implementation using pulse frequency modulation (PFM). (b) Load-transient simulation results of the baseline PFM scheme.

## Summary

In this work, we proposed a fully-integrated switched-capacitor voltage regulator with deep trench capacitors that employs on-chip current sensing

to modulate switching frequency and switch widths simultaneously. Experimental results from 32nm simulation achieved 77-82% efficiency across a 10X range of load currents with 6W/mm2. Moreover, a fast and stable 80mA/ns load transition with 33mV droop voltage, and less than 20mV steady-state ripple across the 10X load range is obtained.

# CHAPTER 4

## FLYING AND DECOUPLING CAPACITANCE OPTIMIZATION WITH AREA CONSTRAINT

## 4.1 Design Considerations for Area-Constrained SCVR

On-chip power management has become increasingly important in modern processor designs for the pursuit of fine-grain dynamic voltage scaling, efficient power delivery, fast load regulation, and simpler package/board design. In order to address the challenges in power supply design, various power conversion circuits and regulation schemes have been proposed. Buck converters with high-quality off-chip or package-integrated inductors have been widely used in portable devices for their high power efficiency [22], but are limited by their on-chip integration capability due to a lack of high-quality on-chip inductors [23]. Linear regulators or low dropout regulators (LDO) with digital, analog, or mixed-mode schemes have also been well presented in recent years [24-25]; however, the linear dependence of efficiency on the input and output voltage values makes LDO an unfavorable choice for high step-down conversion. In comparison, SC voltage converters can offer a fully integrated solution with high-quality on-chip capacitors at integer conversion ratios [22-29]. Furthermore, recently proposed SC converter designs with binary and rational conversion ratios have largely enhanced the efficiency for a wide range of output voltages [29-30].

Theoretical analysis on efficiency and optimization of SC voltage converters have been conducted in several prior works [31-35]. The output impedance models of fast switching loss and slow switching loss conditions for different conversion topologies was proposed

in [31] to analyze the finite conductance of switches and the charging/discharging operations. In [32], the gate capacitance loss, CMOS capacitor bottom-plate loss, and the interleaving ripple-reduction technique were analyzed and optimized. The authors of [33] derived the converter output resistance and analyzed the switch width and switching frequency to achieve optimal efficiencies in SC converters. Regulation analysis of high-power SC converters is performed in [34] using a charge-balance transient-calculation modeling method, however closed-form analysis of droop voltage against abrupt load transients has not been presented. The trade-off of using flying capacitance and decoupling capacitance was analyzed in [35], but an integrated analysis considering both efficiency and droop is not presented.

Most standalone SCVRs in the literature are not designed with specific area constraints. While power densities are reported, more often than not, decoupling capacitance is not included in the overall area. However, in practical scenarios of SCVRs being employed in processors or embedded systems, strict area constraint usually exists, and the area of the SCVR plus the area of input/output decoupling capacitance need to fit in a given real estate. Considering that most of the SCVR area is devoted to capacitance [26-27], selection of appropriate flying capacitance versus decoupling capacitance directly affects the conversion efficiency, output current, and output droop voltage against load transients. The capacitors in SCVRs that will be investigated in this work are illustrated in Figure 4.1. Integrating the effects of both conversion efficiency and output droop into system-level power, we present an area-constrained analysis and optimization of flying and decoupling capacitors in on-chip SCVRs. The proposed work on modeling, analysis, and optimization of SCVRs has the following contributions:

- SC converter efficiency over a wide range of flying capacitance for two CMOS technology nodes (32nm and 65nm), as well as output voltage droop over a wide range of decoupling capacitance are modeled.
- We propose a new figure-of-merit for system-level power efficiency considering both conversion efficiency and minimum supply voltage of load circuits, to optimize the flying capacitance versus decoupling capacitance ratio of SCVRs under a fixed area constraint.
- The proposed models and figure-of-merit are validated for various load current values with an area constraint, in both 32nm and 65nm CMOS process, which show well-matched results with high accuracy.

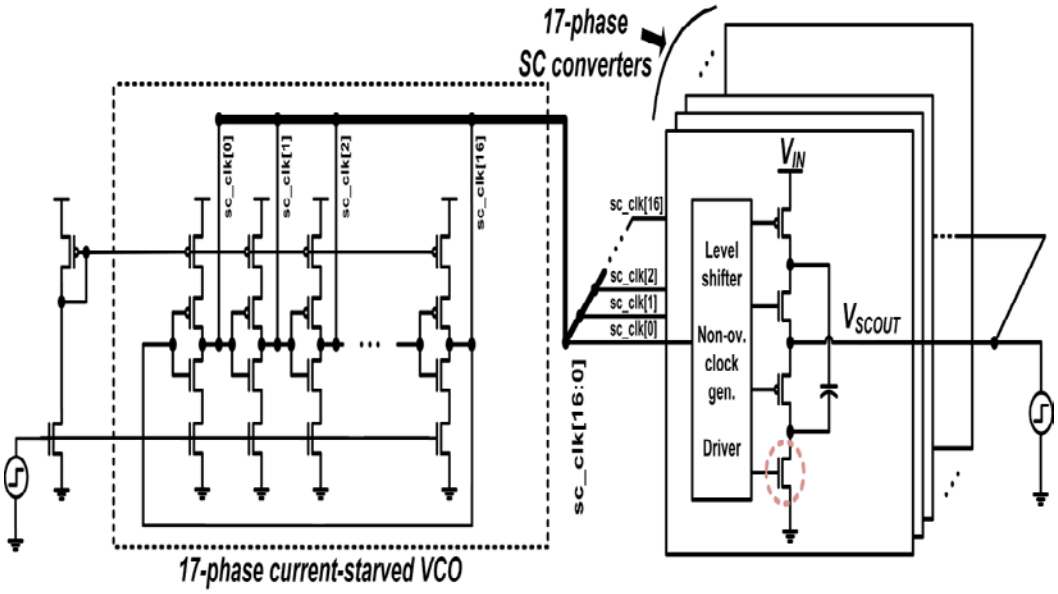



Figure 4.1. Schematic of SC voltage regulator used for droop analysis against load transients.

## 4.2 The Analysis and Optimization of Area-Constrained SCVR

In this section, we present the power loss analysis, conversion efficiency model and droop voltage model of SCVRs. We focus on 2:1 SC converters due to its prevalence in high-efficiency SC converter designs [26, 29], and their use in state-of-the-art binary and rational-ratio SC converters [30].

### 4.2.1 Analysis of Conversion Efficiency and Output Current

The efficiency and power density of an integrated SC voltage converter is directly influenced by the capacitor technology of the CMOS process, besides the conversion ratio and topology. Different capacitor technologies, such as MIM (metal-insulator-metal), MOS (metal-oxide-semiconductor), and DT (deep trench) offer different trade-offs between efficiency and current density options for SC converter design. The sources of power loss in SC voltage converters include the following [10-12]:

(1) charging and discharging behavior of the flying capacitor causes slow switching loss (SSL) due to the voltage ripple at the output, which is inversely proportional to the switching frequency and flying capacitance and is set by:

$$P_{SSL} = \frac{I_L^2}{N_{SSL} f_{sw} C_{fly}}, \quad (1)$$

where $I_L$ is the load current of the SC converter, $f_{sw}$ is the switching frequency, and $C_{fly}$ is the flying capacitance. $N_{SSL}$ is the coefficient depending on SC converter topology and $N_{SSL} = 4$ for a 2:1 SC converter.

(2) current through the on-resistance of the non-ideal switches results in fast switching loss (FSL), which is proportional to the switch width and is set by

$$P_{FSL} = I_L^2 \frac{R_{on}}{W_{sw}} N_{FSL}\,, \tag{2}$$

where $W_{sw}$ is the switch width of the SC converter, and $R_{on}$ is the on-resistance of the switch determined by the CMOS process. $N_{FSL}$ is the coefficient depending on SC converter topology and $N_{FSL} = 2$ for a 2:1 SC converter.

(3) parasitic capacitance of the flying capacitor causes bottom-plate loss, because it is charged from the supply in one phase and discharged to ground in the other phase. Such loss is proportional to the total bottom plate capacitance as well as the switching frequency and is set by:

$$P_{bott} = N_{bott} V_o^2 C_{bott} f_{sw}\,, \tag{3}$$

where $N_{bott}$ is the number of bottom plates, $C_{bott}$ is the bottom-plate capacitance, and $V_o$ is the SC converter output voltage.

(4) the parasitic capacitance of the SC switches causes switching loss due to its charging and discharging behavior, which is proportional to both the switch width and frequency and is set by:

$$P_{sw} = k_{drive} N_{sw} C_{sw} V_{sw}^2 f_{sw}\,, \tag{4}$$

where $k_{drive}$ is the constant of proportionality accounting for the pre-drivers [12], $C_{sw}$ is the parasitic capacitance of the switch, $N_{sw}$ is the number of switches that is conducting, and $V_{sw}$ is the supply voltage of the driver stages.

The total power loss of a SC converter is the sum of the four aforementioned loss terms:

$$P_{loss} = \frac{I_L^2}{N_{SSL} f_{sw} C_{fly}} + I_L^2 \frac{R_{on}}{W_{sw}} N_{FSL} + V_o^2 C_{bott} f_{sw} + k_{drive} N_{sw} C_{sw} V_{sw}^2 f_{sw} \quad (5)$$

The optimal conversion efficiency for different load currents with a given flying capacitance can be determined with the minimization of $P_{loss}$ by varying switching frequency and switch width of the SC converter:

$$\eta_{opt} = \left(1 + \frac{P_{loss\_min}}{P_{load}}\right)^{-1}, \quad (6)$$

where $P_{loss\_min}$ is the minimum value of $P_{loss}$ for a given load current and flying capacitance, and $P_{load}$ is the output power of the SC converter and is set by:

$$P_{load} = V_o I_L \quad (7)$$

Using the 'fmincon' optimization function in Matlab, the minimum power loss $P_{loss}$ is determined with interior-point algorithm for various load currents

and flying capacitance values, thereby obtaining the optimal efficiencies for 2:1 SC converters according to Eq. (6).

### 4.2.2 Analysis of Droop Voltage against Load Transients

The load transient behavior of a SCVR is determined by the operation of the SC converter, the input/output decoupling capacitance and the closed-loop regulation scheme. To analyze the effect of decoupling capacitance on SCVR output droop, we performed droop simulations in 65nm CMOS with MIM capacitors used for input and output decoupling capacitance. As shown in Figure 4.2, the 17-phase interleaved SC converters are driven by a voltage-controlled oscillator (VCO) that provides a frequency modulation scheme against a load transient from 102mA to 1.02A in 10ns. The droop voltage simulation results for 1nF-13nF of input and output decoupling capacitors are shown in Figure 4.3. As can be seen, for the same amount of capacitance (and thus area), the effect of input decoupling capacitance on the output droop is considerably weaker than that of the output decoupling capacitance. In addition, for certain types of capacitors, such as MOSCAP or DTCAP, there could be reliability issues when a high voltage, such as the input voltage, is applied across the capacitors. Due to these reasons, modeling the effect of the input decoupling capacitance on droop is not considered in this work.

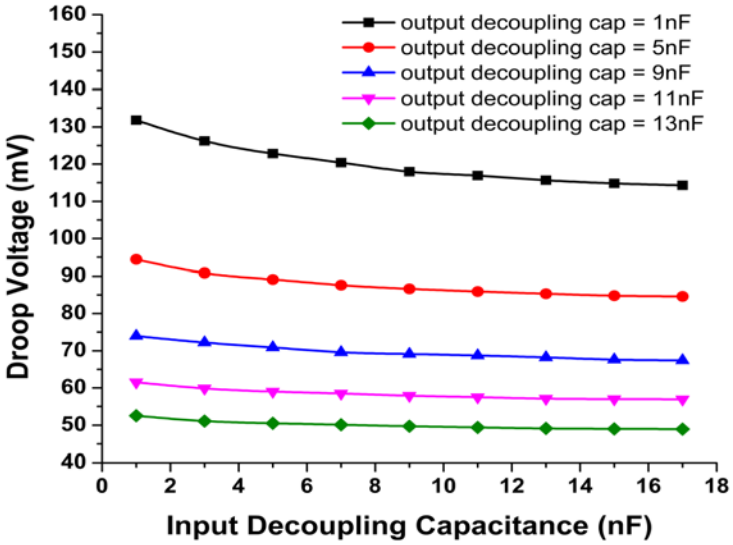



Figure 4.2 SCVR output droop voltage against fast load transients with MIM input and output decoupling capacitances from regulator simulation (Figure 4.1) in 65nm.

In the SCVR operation, the load current is equivalent to the sum of the SC output current and the current through the output decoupling capacitance. During the steady state of the SCVR, when the current, switching frequency, switch width and other modulated parameters are kept constant, the load current is mainly provided by the flying capacitor. The minimum output voltage value in continuous cycles of the switching clocks [11] is set by:

$$V_o\,(t) = \frac{V_i}{2} - \frac{i_{SC}(t)}{4C_{fly} \cdot f_{sw}} \tag{8}$$

Upon an abrupt load transient, the portion of current supplied by the output decoupling capacitor first instantaneously increases and then decreases

as the SC converter provides more output current with a particular regulation scheme. The current provided by the decoupling capacitor $i_{cp}\,(t)$ is set by:

$$i_{cp}\,(t) = C_{cp} \cdot \frac{d\,V_o(t)}{dt}\,, \tag{9}$$

where $C_{cp}$ is the decoupling capacitance. At the output node of the SCVR, three current paths exist: the SC converter current, the decoupling capacitor current and the load current. According to Kirchhoff's current law (KCL), the three current values have the following relationship during the load response:

$$N \cdot i_{SC}(t) + i_{cp}(t) = N \cdot\ i_L(t)\,, \tag{10}$$

where $N$ is the number of interleaved phases in the SCVR, $i_{SC}(t)$ is the single-phase SC converter output current and $i_L(t)$ is the load current.

With a specific regulation scheme, SC input voltage $Vi$, flying capacitance $C_{fly}$, switching frequency $f_{sw}$, decoupling capacitance $C_{cp}$, the number of interleaved phases $N$ and load current step $i_L(t)$ are already known. Then, a system of differential equations, Eqs. (6)-(8), is formed that has $V_o(t)$, $i_{SC}(t)$ and $i_{cp}(t)$ as unknown variables. Assuming that the load current increases from $I_0$ to $I_1$ in transient time of $\Delta t$, starting at time 0, the time-domain single-phase load current is expressed as:

$$I_L(t) = \frac{I_1 - I_0}{\Delta t} \cdot t + I_0 \tag{11}$$

The regulation scheme of the SCVR is modeled as a sudden increase of switching frequency from $f_{sw0}$ to $f_{sw1}$ at $\Delta t/2$, without losing generality. Substituting Eq. (11) into the system of equations Eqs. (6)-(8) leads to a single-variable differential equation as follows:

$$\frac{K_0 V_i}{2} - K_0 \cdot V_o(t) - C_{cp} \frac{d\, V_o(t)}{dt} = \frac{I_1 - I_0}{\Delta t} \cdot t + I_0 , \quad (12)$$

where $K_0 = 4C_{fly} \cdot f_{sw0}$ is a constant. The initial condition is:

$$V_o(0) = \frac{Vi}{2} - \frac{I_0}{K_0} \quad (13)$$

By solving the differential equation above, the output voltage equation can be derived as follows:

$$V_o(t) = \frac{C_{cp}\,(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot (1 - e^{-\frac{K_0}{C_{cp}} \cdot t}) - \frac{I_1 - I_0}{K_0 \cdot \Delta t} \cdot t + \frac{V_i}{2} - \frac{I_0}{K_0} , \quad (14)$$

As the output voltage before the load response is given by Eq. (11), the droop voltage of the SCVR at time $\Delta t/2$ is set by:

$$V_{droop\_sc} = -\frac{C_{cp}\,(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot (1 - e^{-\frac{K_0}{C_{cp}} \cdot t}) + \frac{I_1 - I_0}{K_0 \cdot \Delta t} \cdot t \quad (15)$$

The first term of in Eq. (15) represents the droop voltage contributed from the output decoupling capacitance, and the second term represents the output voltage decrease caused by the operation of the SC converter.

In realistic conditions, the SCVR input voltage $Vi$ is not constant due to the voltage drop $L \cdot di/dt$ caused by the package inductor. The relation between the off-chip supply voltage $V_{supply}$ and SCVR input voltage is set by:

$$V_i(t) = V_{supply} - \frac{L_{pck}}{2M} \cdot \frac{d\, i_{sc}(t)}{dt}\,, \qquad (16)$$

where $M$ is the number of I/O pins and $L_{pck}$ is the inductance of each pin.

For a load step from $I_{SC0}$ to $I_{SC1}$ in $\Delta t$, the additional amount of droop caused by the package inductor is set by:

$$V_{droop\_ind} = \frac{I_{sc1} - I_{sc0}}{2M} \cdot \frac{L_{pck}}{\Delta t} \cdot e^{-\frac{C_{cp}}{C_0}}\,, \qquad (17)$$

where is $C_0$ a fitting parameter obtained from simulation data. The package resistance can affect the DC error of the output voltage for different load currents, but its influence on load-response droop voltage is negligible when the DC error is small, which is the case for all the transient simulations analyzed in this work. Overall, the droop voltage of the on-chip SCVR is modeled as:

$$V_{droop} = -\frac{C_{cp}\,(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot (1 - e^{-\frac{K_0}{C_{cp}} \cdot t}) + \frac{I_1 - I_0}{\Delta t \cdot K_0} \cdot t + \frac{I_{sc1} - I_{sc0}}{2M} \cdot \frac{L_{pck}}{\Delta t} \cdot e^{-\frac{C_{cp}}{C_0}} \quad (18)$$

Proposed Figure-of-Merit for System-Level Power Optimization

In order to evaluate the proposed optimization for an area-constrained SCVR design, we hereby propose a figure-of-merit (FOM) for the system-level power, as shown below:

$$FOM = \frac{P_{out}}{P_{out} + P_{loss} + V_{droop} \cdot I_{avg}}\ , \quad (19)$$

where $P_{out}$ represents the output power at a target load current and $P_{loss}$is the corresponding power conversion loss. $I_{avg}$ represents the average current of the processor load, which depends on the workloads of different applications. Without losing generality, in this work, we assume $I_{avg}$ to be the average value of the maximum load current $I_{max}$ and the minimum load current of $0.1 \cdot I_{max}$, which becomes $0.55 \cdot I_{max}$. The minimum load current is set as 1/10 of the maximum load considering the leakage current of processors, and also serves as the initial current for the worst-case load step response.

The SCVR compares its output voltage to a target reference $V_{ref}$ and continuously modulates the converter to keep the output voltage as close as possible to $V_{ref}$. When abrupt load transients occur, the SCVR can experience

worst-case droop $V_{droop}$, which will bring down the output voltage to $V_{ref} - V_{droop}$. Since it is very difficult to precisely predict when the load transients will occur, to avoid any timing failure even when the droop occurs, $V_{ref} - V_{droop}$ needs to be the minimum supply voltage $V_{min}$ for the digital load circuits. This means that, in conditions without abrupt load transients, $V_{ref}$ needs to be positioned at $V_{min} + V_{droop}$ to prevent any timing failure considering potential droop. To that end, $V_{droop}$ becomes the supply voltage margin of the digital loads, and $V_{droop} \cdot I_{avg}$ represents the additional output power that needs to be provided to the load circuits considering that the SCVR output droop that can occur.

Assuming that a fixed die area is allocated to the total area of flying capacitors and decoupling capacitors, the ratio between the areas of the two capacitors that results in the highest figure-of-merit (FOM) can be obtained, which represents a system-level power-optimal design point for the SCVR. The modeling of FOM can be performed with a combination of the proposed efficiency model and droop voltage model as follows:

$$FOM_{cal} = \left(\frac{1}{\eta_{opt}} + \frac{0.55V_{droop}}{I_{max}}\right)^{-1}, \quad (20)$$

where $\eta_{opt}$ and $V_{droop}$ are the efficiency and droop values modeled in Section II.A and II.B, respectively.

## 4.3 Simulation Results

In this section, we provide experimental results obtained from circuit simulations in 65nm and 32nm CMOS and show the comparison with the model predictions. The flying capacitors and the decoupling capacitors are implemented with MIM capacitors in 65nm and with DT capacitors in 32nm.

### 4.3.1 Efficiency simulations

In order to validate the efficiency and current density trade-off relation of 2:1 SC converters, a set of SC converter designs were implemented in 65nm and 32nm CMOS using the simulation setup in Figure 4.2. Each SC converter phase is driven by four-stage buffers with four ideal non-overlapping clocks. For each flying capacitance value, the switching frequency and width are swept as design variables to obtain the optimal efficiency for different output currents. Then, this is iterated for a number of flying capacitance values to obtain the optimal efficiencies for different flying capacitance values. The comparison of the model calculation with the simulated results in 65nm

and 32nm are shown in Figure 4.4 and Figure 4.5, respectively, which includes multiple load current cases per SC converter phase across a wide range of flying capacitance values. The results show that the model is reasonably accurate and the maximum efficiency error is less than 1.4% for

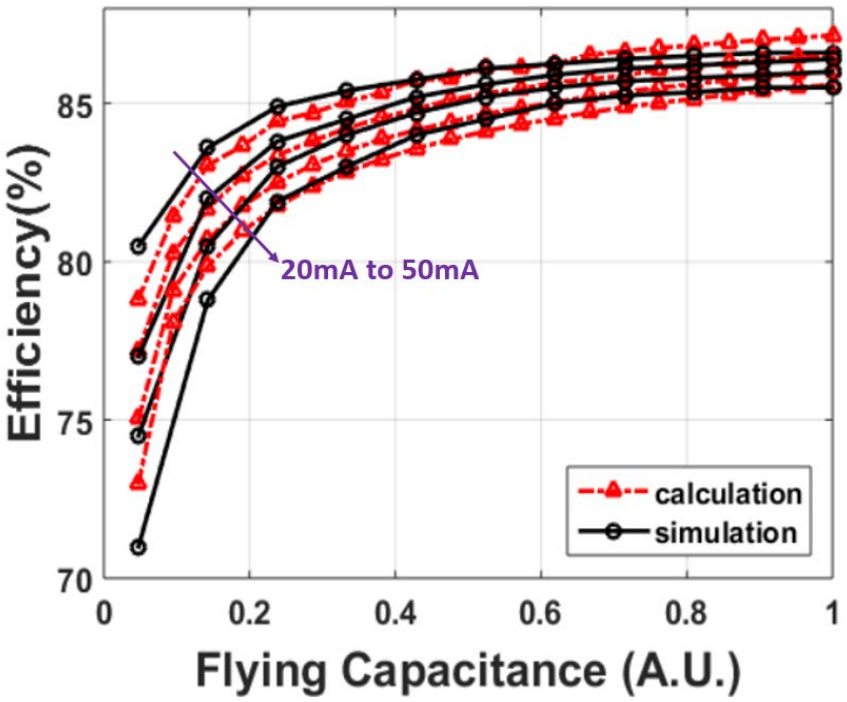



Figure 4.3. Simulated and calculated optimal efficiency values with different flying capacitances at 20mA, 30mA, 40mA and 50mA load currents (per converter phase) in 65nm CMOS.

a 21× range of flying capacitance in 65nm, and less than 0.4% for a 10× range of flying capacitance in 32nm.

### 4.3.2 Droop Voltage Simulations

To validate the accuracy of the droop voltage model for a wide range of decoupling

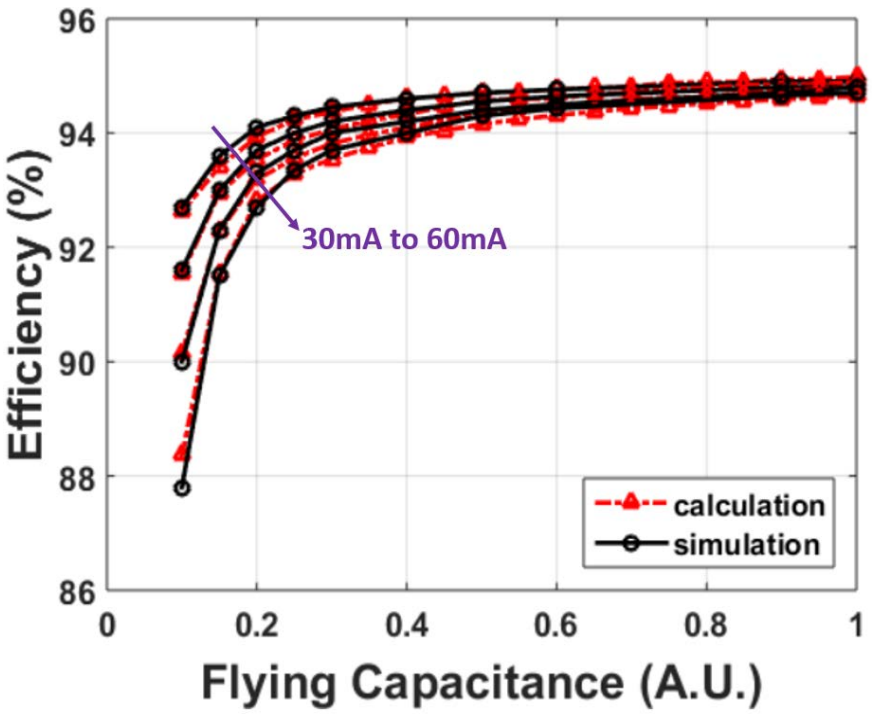



Figure 4.4. Simulated and calculated optimal efficiency values with different flying capacitances at 30mA, 40mA, 50mA and 60mA load currents (per converter phase) in 32nm CMOS.

capacitance, transistor-level simulations with regulation circuits are performed in both 65nm and 32nm CMOS. In the simulation setup (Figure 2), an output current source changes the load current from 51mA to 510mA in 10ns and a decoupling capacitance is set as a design variable. The output voltage regulation is implemented with a step increase in the control voltage of the VCO (left part of Figure 2) to provide an immediate increase of switching frequency so that the output voltage decrease is minimized. By sweeping the output decoupling capacitance value, different droop voltage values are obtained from simulations.

The comparison of the model calculation and the simulation results in 65nm and 32nm CMOS are shown in Figure 4.6 and Figure 4.7, respectively, to show the accuracy of the model prediction. The proposed model for droop voltage against load transients with different decoupling capacitance achieved good accuracy. In 65nm (Figure 6), the maximum and average prediction droop errors for decoupling capacitance up to 21× range is 8.4mV %) and 3.7mV (3.5%), respectively. In 32nm (Figure 4.7), the maximum and average droop errors are 15mV (11.9%) and 4.5mV (4.3%), respectively.

Flying and Decoupling Capacitance Optimization Based on Figure-of-Merit

Since the proposed figure-of-merit characterizes the performance of the SCVR, by varying the ratio between flying and decoupling capacitance with an area constraint, the FOM can be obtained through modeling calculation and simulations in 65nm and 32nm CMOS.

In the 65nm design, the total on-chip MIM capacitors occupy a fixed die area of 1.7mm2. The total flying capacitance is divided by 17 for a 17-phase interleaved SC converter, and the rest of the area is occupied by the decoupling capacitance. In the 32nm design, the total area of the DT capacitors is 0.32mm2. The design area overhead of the drivers and controlling circuits are relatively very small, thus omitted in this discussion. For different output current values of the SCVR, the optimal efficiencies with different flying capacitance percentage (P_FC) are obtained by sweeping the frequency and width of the SC converter, and the droop voltages are obtained by running transient simulations with load step from 0.1× to 1× current. The FOM for each different flying capacitance percentage is determined with Eq. (19) based on the simulation results, at different load current cases. The modeled FOM is calculated with Eq. (20) according to the efficiency and droop voltage formulas. The comparison of simulated and calculated FOM versus

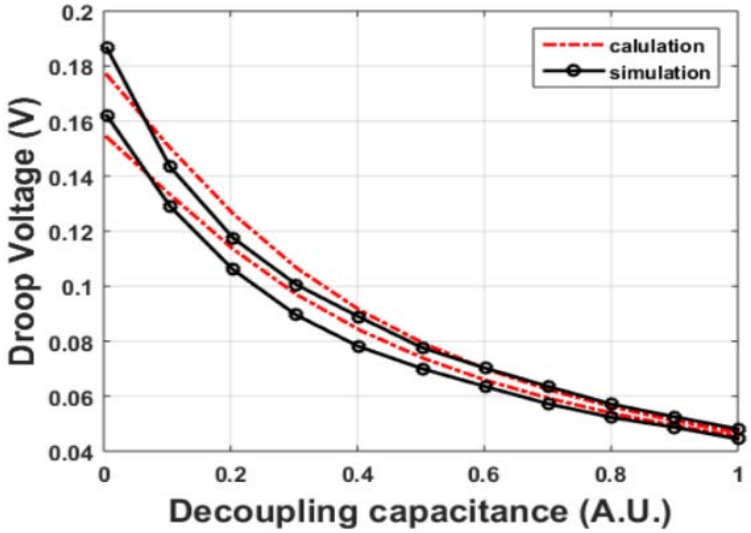



Figure 4.5. Simulated and calculated droop voltage of SCVR for 51-510mA, 10ns load step in 65nm CMOS for a 21X range of flying capacitance percentage for three different load current cases in 65nm and 32nm CMOS are shown in Figure 4.8 and Figure 4.9, respectively.

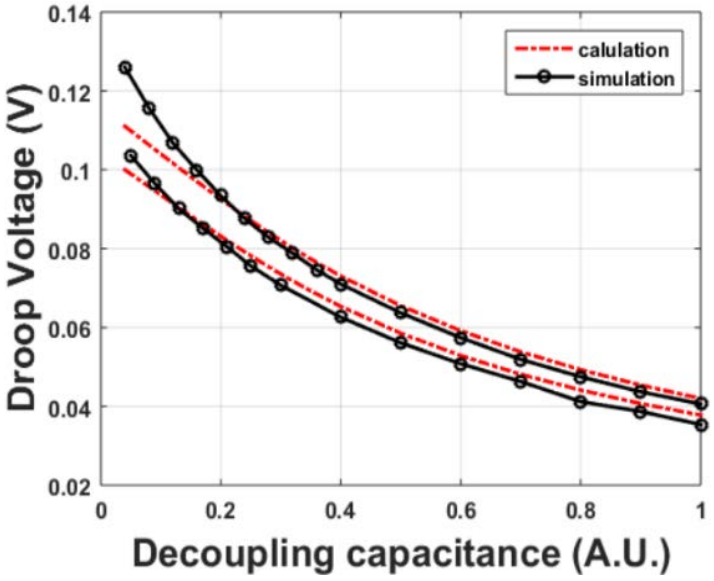



Figure 4.6. Simulated and calculated droop voltage of SCVR for 102-1020mA, 40ns load step in 32nm CMOS for a 21X range of decoupling capacitance.

Table I shows the simulated and modeled optimal flying capacitance percentage that offers the best system-level power efficiency for different load current cases, as well as the

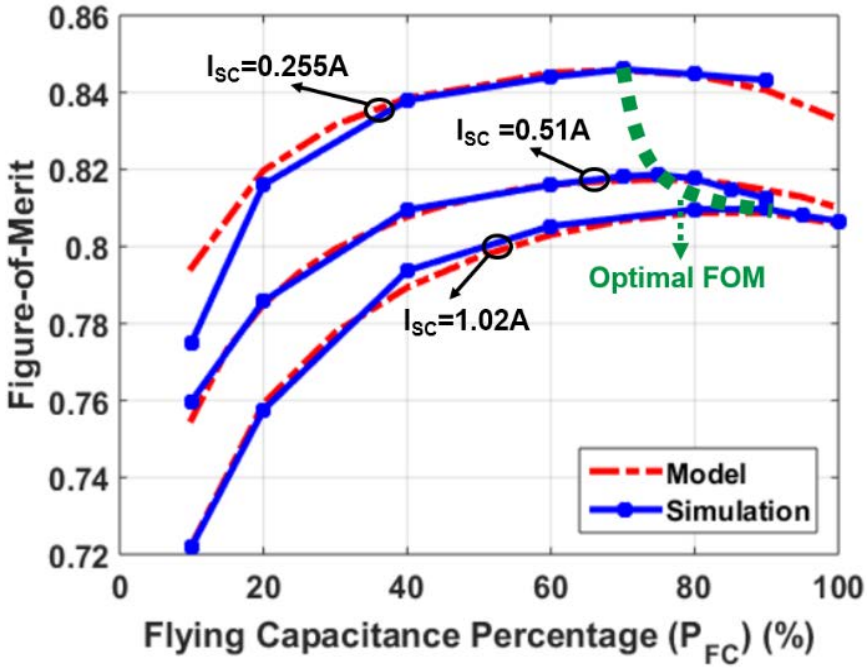



Figure 4.7. Simulated and calculated Figure-of-Merit for different flying capacitance percentage over total capacitance in 65nm CMOS at 0.255A, 0.51A and 1.02A SC current.

corresponding figure-of-merit, droop voltage and power efficiency in 65nm and 32nm, respectively. Compared to the simulation results where the smallest PFC step is 5%, the worst-case modeling error of PFC is 5%.

## Summary

In this work, we present an optimization methodology for flying and output decoupling capacitance of SCVRs under specific area constraints. The power efficiency and droop voltage against load transients are modeled with respect to flying capacitance and decoupling capacitance. Based on these models, we proposed a figure-of-merit that

represents system-level power efficiency, capturing both efficiency and droop. The proposed FOM allowed us to optimize the flying and decoupling capacitance values for area-constrained on-chip SCVRs. The models are validated with SCVR circuit simulations

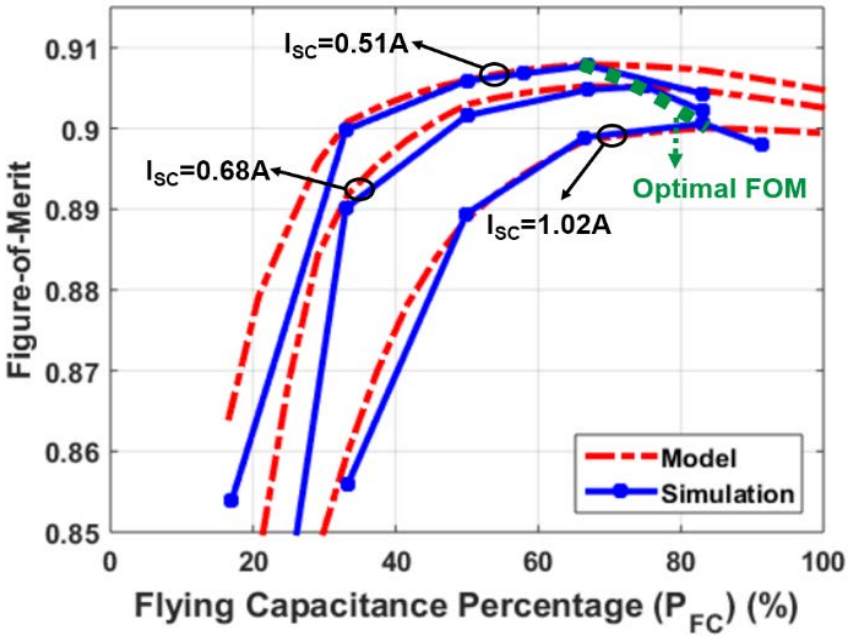



Figure 4.8. Simulated and calculated Figure-of-Merit for different flying capacitance percentage over total capacitance in 32nm CMOS with 0.51A, 0.68, and 1.02A SC current.

in 65nm and 32nm CMOS, showing good prediction accuracy.

**Table I. Optimal-FOM flying capacitance percentage and performance parameters in 65nm and 32nm CMOS from (m) modeling and (s) simulation results. Total area of flying and decoupling capacitance is 1.7mm2 and 0.32mm2, respectively, for both process technologies.**

| **Process** | | **65nm CMOS** | | | **32nm CMOS** | | |
|---|---|---|---|---|---|---|---|
| **SC current (A)** | | ***0.255*** | ***0.51*** | ***1.02*** | ***0.51*** | ***0.68*** | ***1.02*** |
| **Optimal PFC (%)** | ***m*** | **70** | **75** | **85** | **67** | **70** | **83** |
| | ***s*** | **70** | **75** | **90** | **67** | **75** | **83** |
| **Optimal FOM** | ***m*** | **0.846** | **0.817** | **0.809** | **0.908** | **0.905** | **0.900** |
| | ***s*** | **0.846** | **0.819** | **0.810** | **0.908** | **0.905** | **0.900** |
| **Efficiency (%)** | ***m*** | **86.0** | **84.5** | **83.0** | **94.0** | **93.7** | **93.3** |
| | ***s*** | **85.4** | **84.2** | **85.4** | **94.1** | **93.0** | **93.6** |
| **Droop voltage (mV)** | ***m*** | **40** | **48** | **83** | **34** | **45** | **69** |
| | ***s*** | **41** | **44** | **93** | **37** | **48** | **72** |

# CHAPTER 5

# PROTOTYPE OF A SC VOLTAGE REGULATOR

## 5.1 Fully-Integrated SCVR with V+I Sensing Control

We propose a 2.1V to 0.9V 17-phase 2:1 fully-integrated switched-capacitor voltage regulator with voltage comparison and lossless on-chip current sensing control for frequency modulation. the output voltage of the regulator is compared with a reference voltage to generate a binary signal, which controls the frequency of the VCO through footers/headers, which drives the SC converters through non-overlapping switch drivers. Moreover, the current sensing circuit parallelly mirrors the input current through the top PMOS transistor of the 2:1 SC voltage converter with a ratio of 1/150. The sensed current then goes through a diode-connected NMOS to generate a control voltage that is in positive correlation with the sensed current and load current. Then the control voltage modulates the VCO clock frequency. According to the measurement results, the proposed design achieves peak efficiency of 69.6% at 4.2mW/mm2 power-area density and 12.5mW/nF power-capacitance density, and the regulator output voltage ripple in a 3.5mA to 76mA load range is between 50mV to 60mV.

In this work we focus on 2:1 SC voltage converter design, and the voltage comparison and current sensing control can be applied to other integer voltage conversion ratios. Moreover, some state-of-art prior work on SC voltage converters focused on 2:1 converters in successive approximation  or in recursive manner , which makes our design optimization of 2:1 SC converter particularly relevant.

In this section, we will focus on the optimization of 2:1 single-phase switched-capacitor voltage converter as a representative of step-down SC converters for on-chip power management.

### 5.1.1 Operation of 2:1 Switched-Capacitor Converter

Switched-capacitor voltage converter operates in a voltage mode in contrast to traditional non-isolated buck converters. For 2:1 switched-capacitor voltage converter, flying capacitance is charged to pull current from the input voltage source to the output at half of the clock period and is discharged to pull current from ground to the output at the other half clock period. With continuous switching between the two states back and forth, the SC converter provides a down conversion of 2:1 ratio. The power loss of the switched-capacitor converters include the fast switching loss and slow switching loss.

The target load of our proposed 2:1 switched-capacitor voltage regulator is 80mA, which can be applied in various mobile electronic devices. Assuming the leakage power at minimum load of the mobile application processors is 10% of the maximum power, we design the regulator for a load range of 8mA to 80mA.

### 5.1.2 Efficiency Optimization and trade-off with Power Density

The authors in [8] showed that the optimal switching frequency and switch width is proportional to (I_LOAD)^(2/3). More-recent prior works have also showed close-to-linear relation between optimal frequency/width and load current. In addition, for a given load current, the increase of the flying capacitance offers higher optimal efficiency while decreasing its power density as the capacitor area increases, which is a trade-off between efficiency and power density. The targeted single-phase SC converter output current is

9.4mA in this design. In 65nm CMOS, we use metal-insulator-metal (MIM) capacitor as the flying capacitor due to its high quality, and high- Vt power switches to avoid current leakage. By running post-layout simulations, we picked 240pF flying capacitance, and 100um power switches as the optimal frequency and switch width for a 4.5mA single-phase SC converter output current.

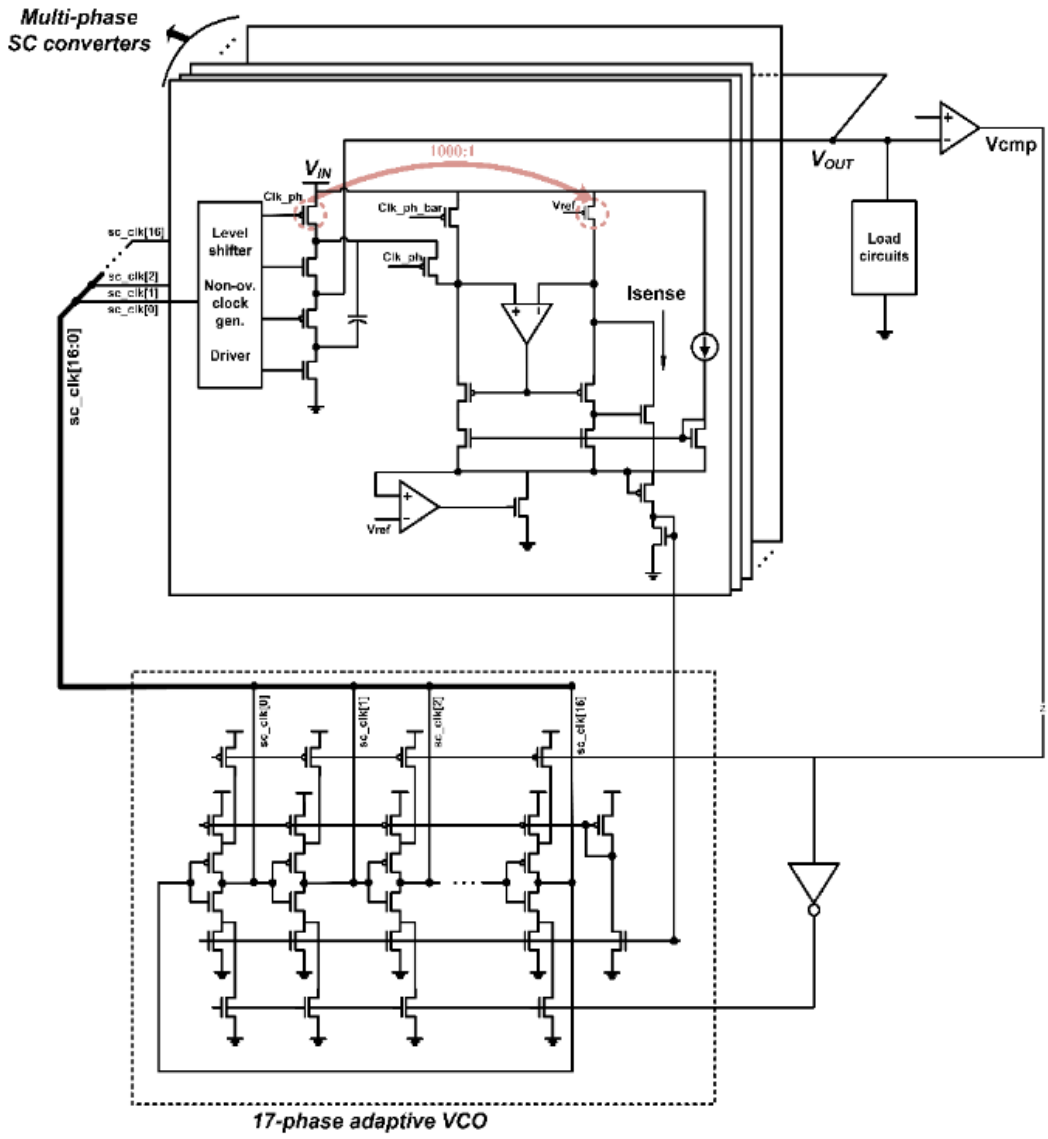



Figure 5.1. Circuit Diagram of the regulator with voltage comparison and current sensing control

### 5.1.3 Voltage Comparison and Current Sensing Control for Frequency Modulation

The overall circuit diagram of the proposed switched-capacitor voltage regulator with voltage comparison and current sensing control is shown in Figure 5.1, which will be described in detail in this section.

17-phase interleaved SC converter

Based on the single-phase 2:1 SC converter optimized in Section II, we adopt multiple-phase interleaved structure, where the converters' inputs and outputs are connected respectively, in order to reduce the intrinsic output voltage ripple and enhance response time[]. The number of SC phases was chosen as 17, as it shows a good trade-off between ripple reduction and converter design overhead. The clocks of the multi-phase converters are driven by 17-phase current starved voltage-controlled oscillator (VCO), whose control voltage is generated from the feedback circuitry. The VCO outputs are connected to the driver of the power switches, which consists of level-shifters and deadtime generators. The level-shifter provides clocks for the clocks between 0V and Vdd/2, as well as the ones between Vdd/2 and Vdd. The deadtime generators provides a short time interval within a clock period when all power switched are off, to avoid DC current leakage.

### 5.1.4 Adaptive Voltage-Controlled Oscillator

We use a current-starved VCO for this SC voltage regulator. Figure 5.2 shows the circuit diagram of this VCO design. In each stage, a PMOS header and NMOS footer is used to control the current through the inverting stage in the middle, the current of each branch is set by the VCTRL_N voltage for the NMOS footer as well as the VCTRL_P voltage for

the PMOS header. When the SC current increases, the VCTRL_N as well as the current increases for each stage of the VCO, the clock frequency then increases, which controls the SC converters in return. Moreover, there are additional footer and header whose gates are connector to binary signals from the output of the comparator, which compares the regulator output with a reference voltage during load transients. When the comparator output changes, these additional footer and header abruptly pump more current into each branch so that the SC converter frequency are also abruptly increased during load transient

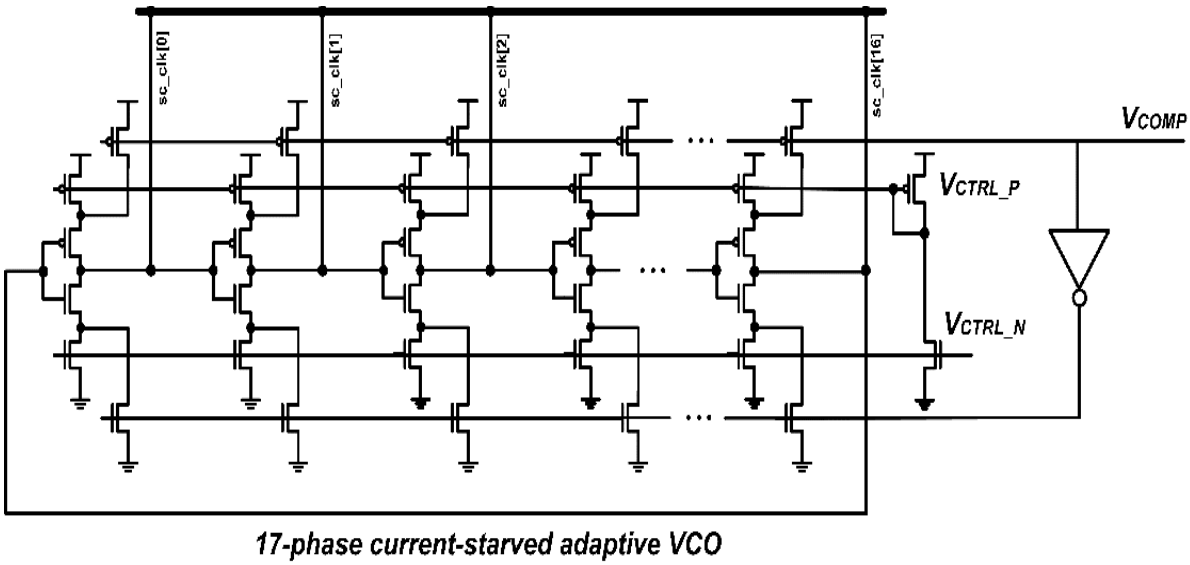



Fig 5.2. The circuit diagram of the current starved adaptive VCO

response. This scheme is used to reduce voltage droop.

### 5.1.5 Lossless On-Chip Current-Sensing Circuit

To sense the SC converter current with minimal power loss, a parallel current-sensing circuit is applied to the SC converter, which mirrors the input current of the SC converter,

as shown in Figure 5.3. The current sensing circuit is used in each phase of the SC converters to increase the sensing accuracy and response time of the feedback in case only some of the SC converter phases changes while other haven't change, at a certain time point of a clock period.

The input current of the SC converter goes through the top PMOS transistor, which is turned on at half clock period and is turned off at the other half. When the top PMOS is on, its current is mirrored with a transistor that has 1/150 of its width. The mirroring PMOS transistor M7 has the same source voltage with the power PMOS transistor M1 and its gate voltage is set to a DC reference voltage that is the same as that of M1, when the gate voltage is low. When M1 is turned on, its drain voltage is passed through a PMOS switched, to the input node of the operational amplifier. The drain voltages of M1 and M7 are then equalized with a negative feedback loop through the amplifier and a PMOS M8. By setting the current through M8 and M4 very small, the majority of the sensed current goes M10 instead of M8. As the SC converter input voltage VIN is twice the nominal voltage of the process, M1 to M8 operates between VIN and VIN/2. VIN/2 is supplied by a tail LDO, which provides current to all the sensing circuits of the regulator. The sensed current is then converted to a control voltage, VCTRL, which is connected to the input of the VCO. VCTRL is set between ground and VIN/2 by properly selecting the size of the diode-connected NMOS transistor M12. In the current branch of Isense, M10 and M11 could have their body-to-source voltage larger than the nominal voltage, so we uses deep-Nwell for M10 and M11, so that the transistor bodies are connected to the source instead of VDD or ground, which avoids the body-to-source voltage breakdown. The control voltage VCTRL for each of the 17-phases are connected to reduce its voltage ripple. The current

sensing circuit is turned off when the top PMOS transistor is off at half of the clock period by pulling the amplifier positive input to VIN with M2. The total power consumption of the current sensing circuit is 39uA, which is 0.4% of power for targeted 9.4mA current in each SC converter phase.

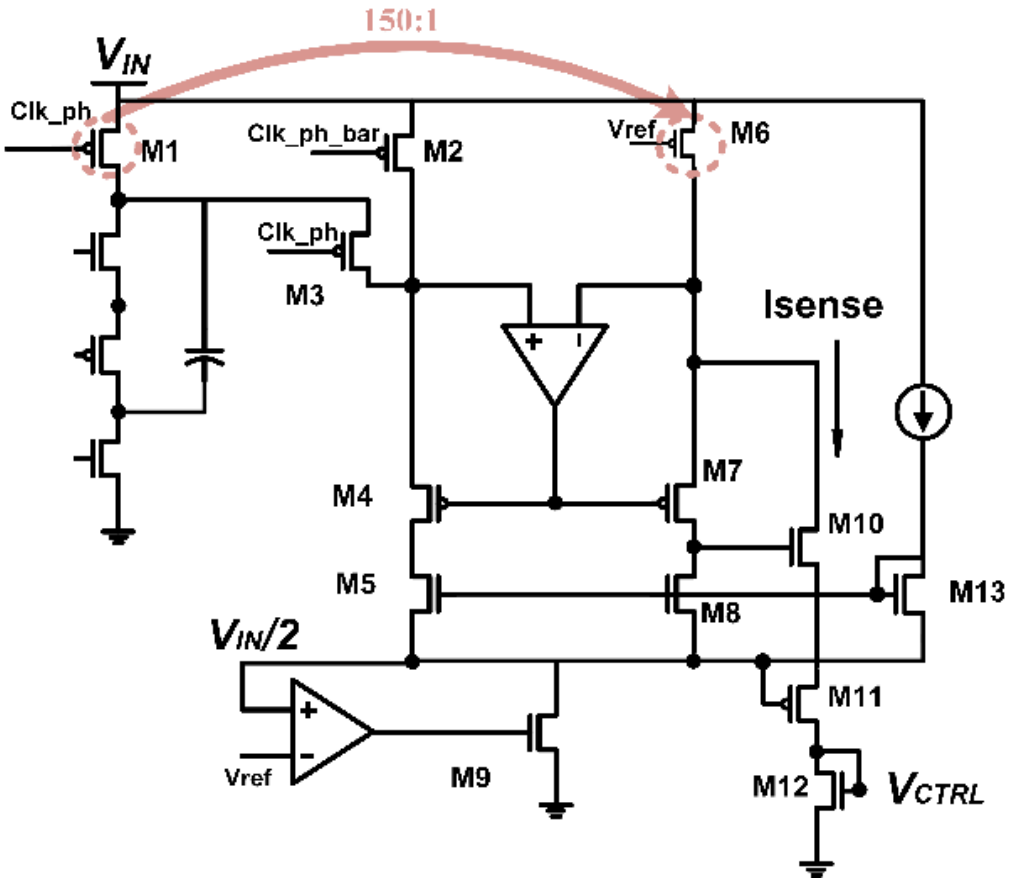



Fig. 5.3. The diagram of the current sensing circuit

### 5.1.6 SR-Latched Comparator

The design of the SC clocked-comparator design is shown in Figure 5.4, which utilizes a differential NMOS input structure together with cross-coupled inverters to drive the differential inputs to VDD or ground at each branch. Without the S-R latch, both the positive and negative outputs of the comparator stays at VDD when the clock signal is low,

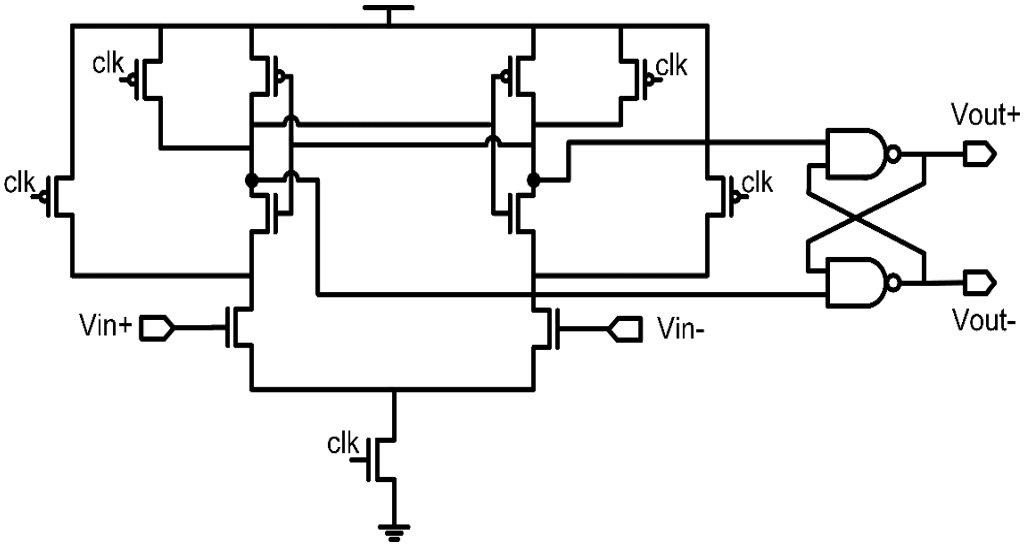



Figure 5.4. The clocked comparator with SR latch

and are evaluated to the corresponding voltage level when the clock signal is high. By the SR-latch as the second stage, the Vout+ and Vout- stay at the corresponding voltage level no matter how the clock signal changes, and only change the output voltage level when the inputs of the comparator change invert.

According to the post-layout simulation, the clocked-comparator works at least up to 2GHz clock frequency when the input voltage difference is 50mV. Figure5.5 shows the transient plot for the input and output voltages of the clocked-comparator, as well as the clock signal.

### 5.1.7 Two-stage Differential Operational Amplifier

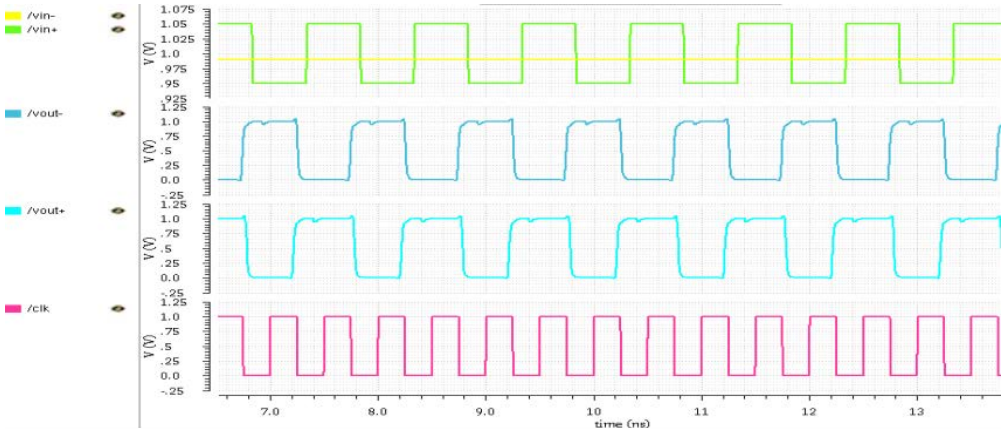



Figure 5.5 The input and output waveforms of the clocked-comparator

For the amplifier in the current sensing circuit, we uses a two-stage operational amplifier design, which is shown in Figure 5.6 . The first stage of the op-amp is a differential amplifier with NMOS input pairs as the input voltage is close to the input supply voltage. The second stage is a PMOS common-source amplifier. A compensation capacitor is used between the outputs of the two stages in order to splitting the poles and enhance the stability of the op-amp. Additionally the PMOS M9 provides zero nulling resistance with its source-to-drain resistance. As the current sensing circuit works on and off and only senses the current at half of the clock period for each converter phase, the bandwidth of the amplifier is enhanced so that the amplifier can respond fast during the short time intervals that the sensing circuit is on.

Since the op-amp in the current sensing circuit works between VIN and VIN/2, where VIN is twice the nominal voltage, the body-to-source voltage could exceed the nominal voltage for M3 and M4, deep-Nwell devices are also used to avoid Vbs breakdown.

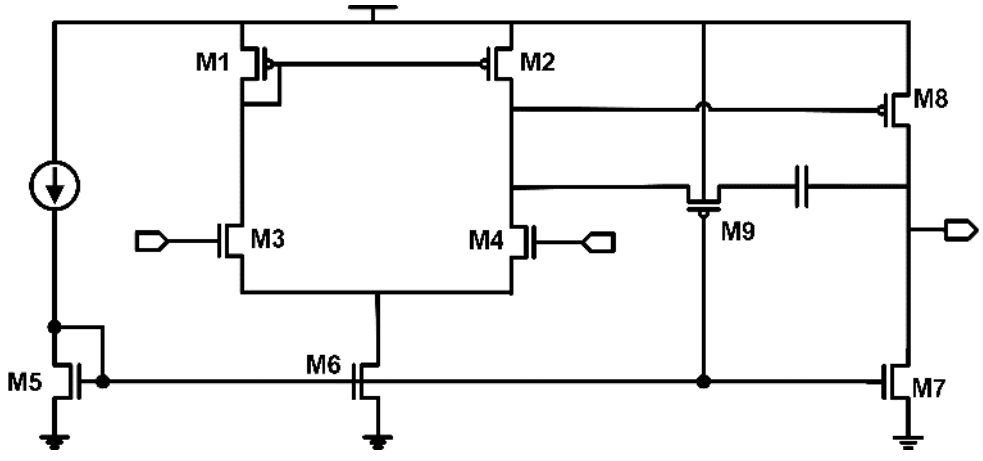



Figure 5.6. Circuit Diagram of the two-stage operational amplifier

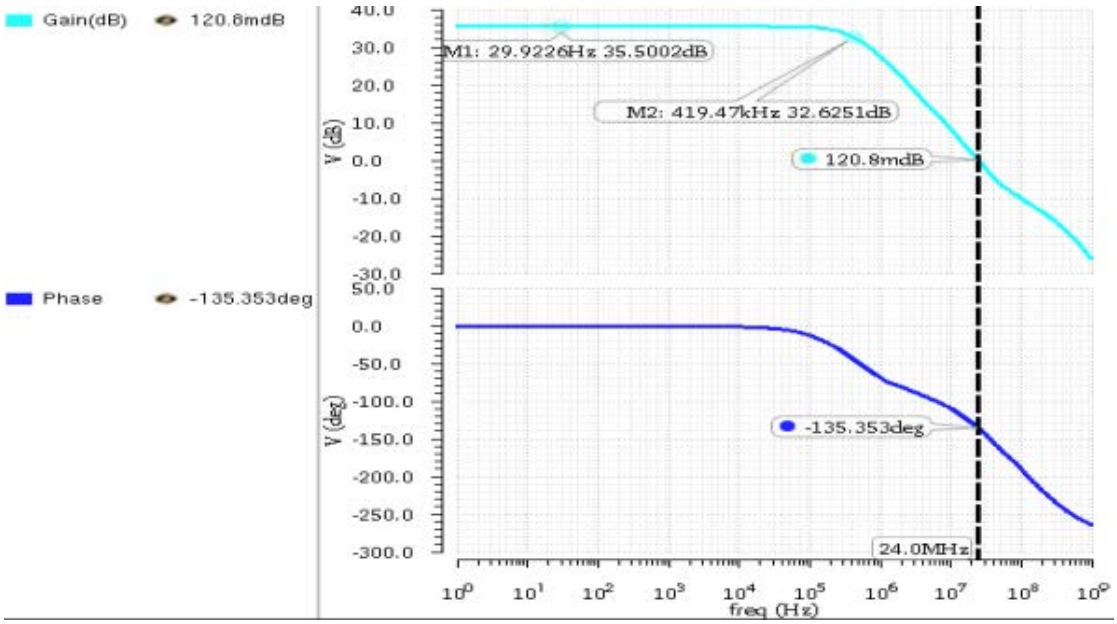



Figure 5.7 Frequency response bode-plot of the operational amplifier

The post-layout simulation for the frequency response bode-plot of the two-stage operational amplifier is shown in Figure 5.7 . The DC gain of the amplifier is 35.5dB and the dB-bandwidth is 420kHz with a current consumption of 29.6uA. The phase margin is 45 degree for this design.

### 5.1.8 Level-Shifter and Deadtime Generator

The driver circuit for the SC converters is shown in Figure 5.8. Starting from standard inverter sizing, M2 and M3 split the original NMOS with equal size. Similarly, M4 and M5 split the original PMOS with equal size. M2 and M5 are driven by a delay line which increase pull-down and pull-up delay respectively for the upper and lower sides. The.

upper side clock then has slightly lager than 50% duty cycle and the lower side clock has slightly smaller than 50% duty cycle. The upper side clocks drive the PMOS transistors of

SC converter and the lower side clocks drive the NMOS transistors. This setup generates deadtime between PMOS and NMOS on-time, which avoids DC current from the input to ground.

## 5.2 The Physical design of the 17-Phase Switched Capacitor Voltage Converter

The 17 phases of switched capacitor voltage converters are evenly distributed in the chip area. The large capacitors are put on the outer side of the chip and the main power lines are

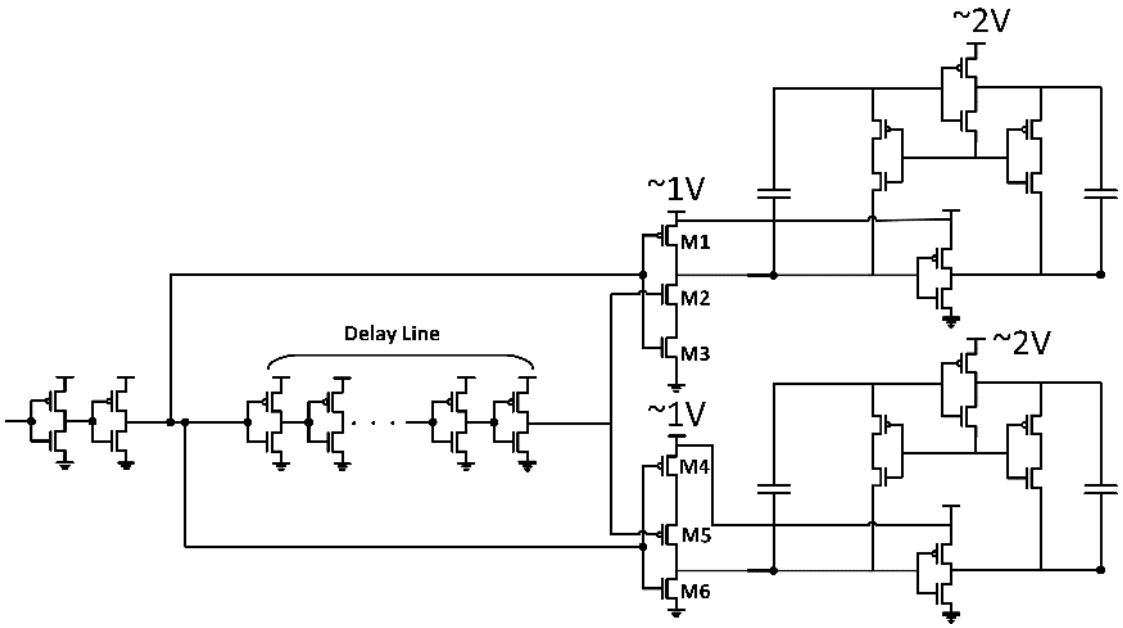



Figure 5.8 The circuit diagram of the driver for a SC converter

put in the middle of the chip, so that the IR drop through the main power line metals are reduced as much as possible.

The main control circuit locates close to the center of the chip and the all the clocks for the switches the power converters are distributed in an H-tree structure, so that delay from the VCO to SC converter is the same for all phases, as shown in Figure 5.9.

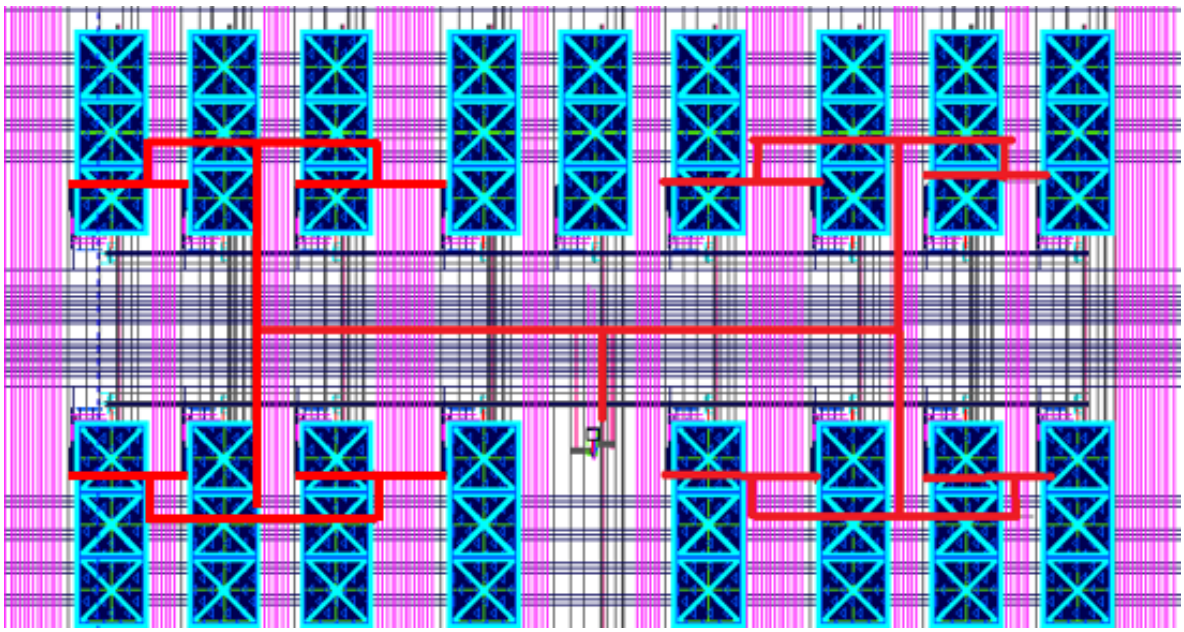


Figure 5.9. The clock distribution for the 17-phase switched-capacitor voltage regulator (The red lines traces the H-tree implementation)

## 5.3 Measurement Results

The design of the proposed SC voltage regulator is fabricated in 65nm CMOS. The flying capacitance is MIM capacitor. The chip area with IO pads is 2.6mm x 4.6mm. The chip micrograph is shown in Fig 5.10.

### 5.3.1 Power Efficiency and Power density of the Proposed SC Voltage Regulator

For the testing of the regulator chip, the input supply voltage is changed between 2.0V to 2.3V, and the current range is between 3.5mA to 92mA. The efficiency at different supply voltage for each load point is shown in Figure 5.11. The efficiency plot for different VCO supply voltage is shown in Figure 5.12.

Overall, the measured power efficiency and power density of the SC voltage regulator across 3.5mA to 92mA load range. The peak efficiency is 69.6% at 60mA load current with a 4.2mW/mm2 power-area density and 12.5mW/nF power-capacitance density. The efficiency across 20mA to 92mA load range is above 62%, as shown in Figure 13. In addition, the measured steady-state output voltage ripple value of the proposed SC regulator across 3.5mA to 76mA load ranges from 50mV to 60mV.

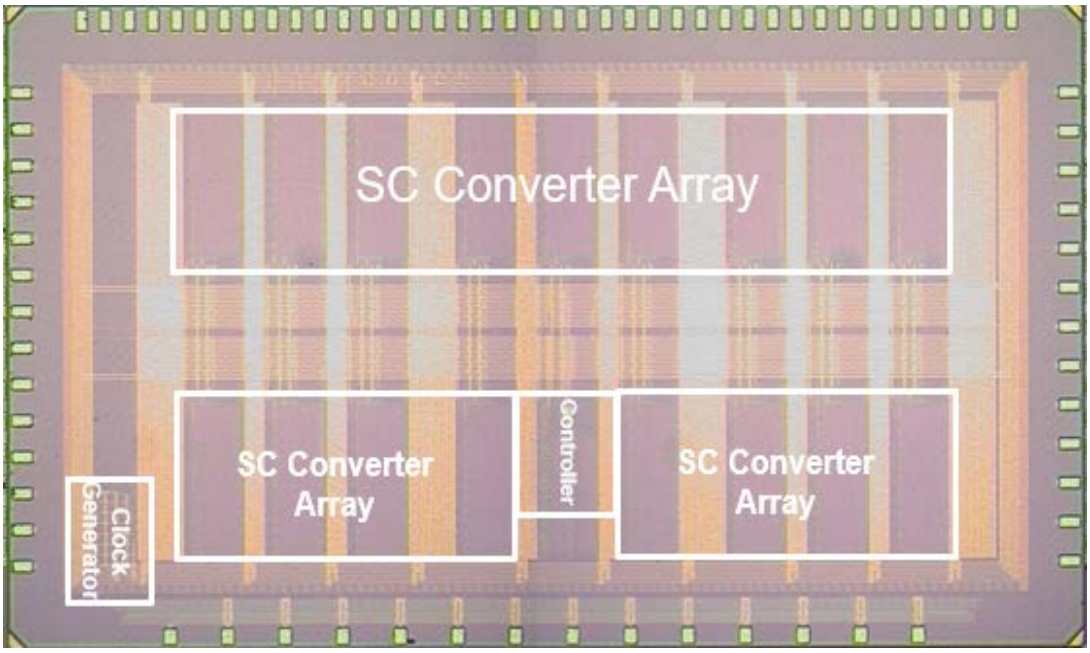



Figure 5.10 The chip micrograph of the SCVR

### 5.3.2 Load Transient of the Proposed SC Voltage Regulator

Figure 5.14 shows the regulator output voltage when the load current changes between 3.5mA to 70mA in 5kHz frequency. The blue line is the output voltage transient waveform; the purple line is the voltage across a small series resistor. The axis and tick label on the right side shows the value respectively.

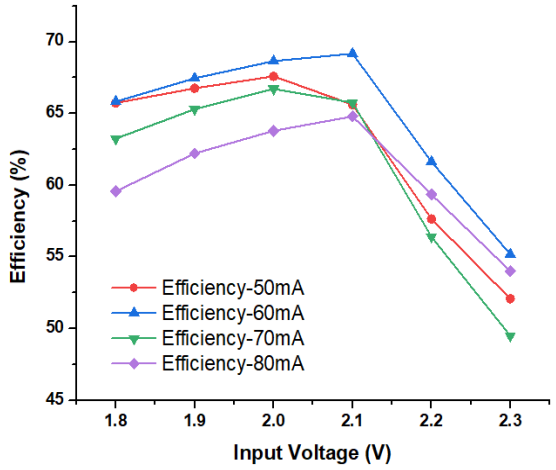



Figure 5.11. The regulator efficiency vs Input supply voltage at different load currents

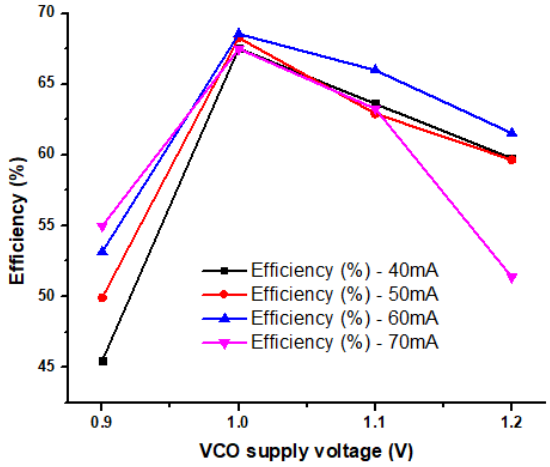



Figure 5.12. The regulator efficiency vs VCO supply voltage at different load currents

### 5.3.2 Load Transient of the Proposed SC Voltage Regulator

Figure 5.14 shows the regulator output voltage when the load current changes between 3.5mA to 70mA in 5kHz frequency. The blue line is the output voltage transient waveform; the purple line is the voltage across a small series resistor. The axis and tick label on the right side shows the value respectively.

Table II compares this work with the measured specifications of the SC voltage regulator works in recent years

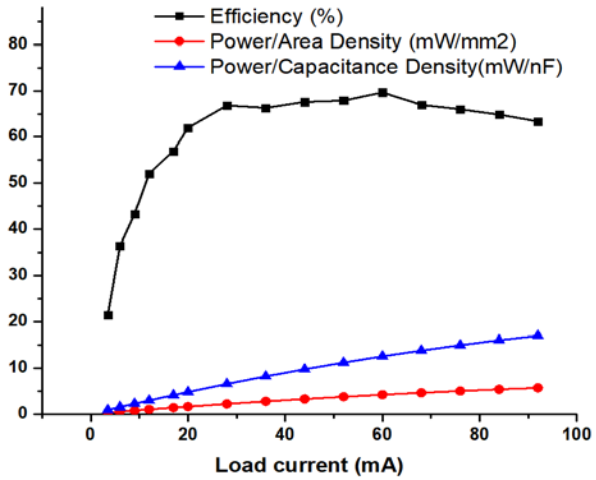



Figure 5.13. The measured efficiency and power density of the SC regulator across load current range

| Source | [36] | [37] | [38] | [39] | [40] | This work |
|---|---|---|---|---|---|---|
| Process | 65nm | 65nm | 130nm | 130nm | 40nm | 65nm |
| Capacitor Type | MIM+ MOS | MIM+ MOS | NA | MIM+ MOS | NA | MIM |
| Input voltage | 2.3 | 1.05-1.4 | 1.5 | 3.2-4 | 3.5-4 | 2.3-1.8 |
| Output voltage | 1 | 0.55,1 | 0.44, 0.88 | 1.07 | 0.75 | 0.9 |
| Peak efficiency (%) | 71 | 78 | 78 | 78 | 70 | 70 |
| Load current (mA)@ Peak efficiency | 142 | 0.35 | 12 | 27 | 20 | 60 |
| Current/capacitance Density (mW/nF) | 38.4 | 0.78 | 5.4 | 60 | 13.3 | 12.5 |
| Output ripple (mV) | 6-16 | 50-80 | NA | 30-50 | 60 | 50-60 |
| Chip area ($mm^2$) | 0.76 | 0.27 | 0.72 | 0.39 | 1.1 | 9.2 |

**Table II Comparison of measured specifications of the SC voltage regulator works in recent years with this work**

## Summary

In this work, a fully-integrated switched-capacitor voltage regulator with voltage comparison and current sensing control is proposed. The prototype chip is fabricated in 65nm CMOS. The measurement result shows that the SC voltage regulator achieves 69.6% peak efficiency at 60mA load current, which corresponds to 4.2mW/mm2 power-area density and 12.5mW/nF power-capacitance density. The efficiency across 20mA to 92mA

load range is above 62%. The steady-state output voltage ripple across 22x load current range of 3.5mA-76mA is between 50mV to 60mV.

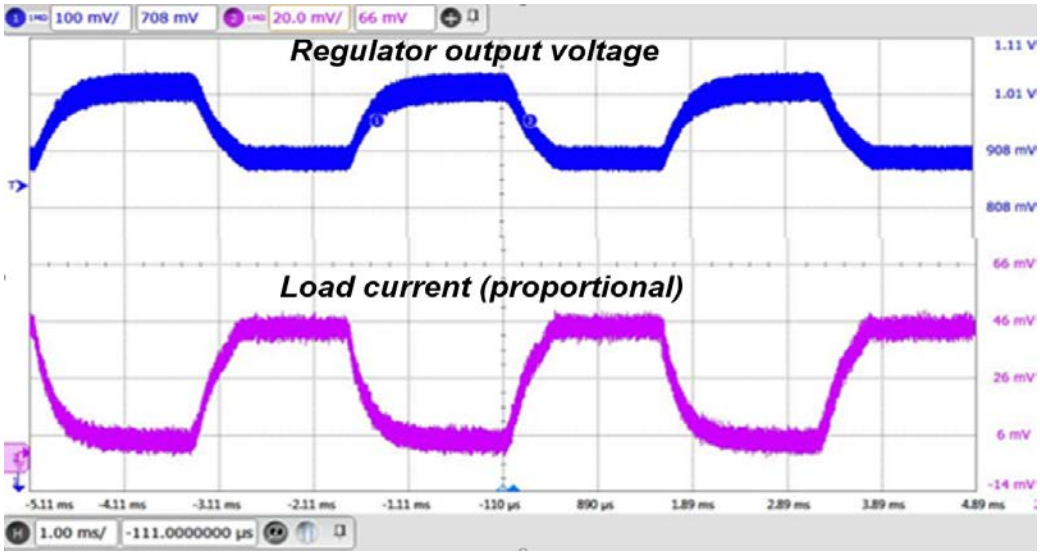



Figure 5.14. The regulator output voltage when the load current changes between 3.5mA to 76mA in 5kHz frequency

# CHAPTER 6

# CONCLUSION

As the power management circuits have been more and more important in a wide variety of fields, providing fully integrated voltage regulation is a challenging and promising research topic. Switched-capacitor (SC) voltage converters have received attentions in integrated power conversion for fixed-ratio voltage conversions with good efficiency and feasibility of integration.

During my PhD study, an on-chip current sensing technique is proposed to dynamically modulate both switching frequency and switch widths of SC voltage converters, enhancing fast transient response and higher efficiency across a wide range of load currents. The fully-integrated switched-capacitor voltage regulator design with deep trench capacitors employs on-chip current sensing to modulate switching frequency and switch widths simultaneously. Simulation results in 32nm SOI process shows that the design achieved 77-82% efficiency across a 10X range of load currents with 6W/mm$^2$. Moreover, a fast and stable 80mA/ns load transition with 33mV droop voltage, and less than 20mV steady-state ripple across the 10X load range is obtained.

On the mathematical modeling of the SC regulator, we propose a methodology to optimize flying and decoupling capacitance for area-constrained on-chip SCVRs to achieve the highest system-level power efficiency. Considering both conversion efficiency and droop voltage against fast load transients, the proposed model determines the optimal ratio between flying and decoupling capacitance for fixed total area at different load current cases. These models are validated with integrated 2:1 SCVR implementations in both 65nm

and 32nm CMOS. Simulations show high model accuracy on efficiency and droop modeling for a broad range of flying and decoupling capacitance.

In 65nm CMOS, we prototyped a fully integrated, 17-phase interleaved switched-capacitor voltage regulator with voltage comparison and current sensing control, to provide frequency modulation against fluctuating load current. The regulator is implemented with MIM-capacitor, targeting 2.1V input voltage and 0.9V output voltage. According to the measurement results, the proposed SC voltage regulator achieves 69.6% peak efficiency at 60mA load current, which corresponds to a 5.7mW/mm$^2$ power-area density and 12.5mW/nF power-capacitance density. The efficiency across 20mA to 92mA regulator load current range is above 62%. The steady-state output voltage ripple across 22x load current range of 3.5mA-76mA is between 50mV to 60mV.

In the past years, the research on integrated switched-capacitor voltage regulator has shown progress in the conversion efficiency, the input and output voltage range, the regulation across load current range, the response against load transients, the output voltage ripple, with the application of new conversion circuit topologies, new types of process and devices, as well as new regulation schemes, which are receiving continuing attention and effort.

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