Modeling, Control and Design of Modular Multilevel Converters for High Power Applications

by

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ABSTRACT

Modular multilevel converters (MMCs) have become an attractive technology for high power applications. One of the main challenges associated with control and operation of the MMC-based systems is to smoothly precharge submodule (SM) capacitors to the nominal voltage during the startup process. The existing closed-loop methods require additional effort to analyze the small-signal model of MMC and tune control parameters. The existing open-loop methods require auxiliary voltage sources to charge SM capacitors, which add to the system complexity and cost. A generalized precharging strategy is proposed in this thesis.

For large-scale MMC-embedded power systems, it is required to investigate dynamic performance, fault characteristics, and stability. Modeling of the MMC is one of the challenges associated with the study of large-scale MMC-based power systems. The existing models of MMC did not consider the various configurations of SMs and different operating conditions. An improved equivalent circuit model is proposed in this thesis.

The solid state transformer (SST) has been investigated for the distribution systems to reduce the volume and weight of power transformer. Recently, the MMC is employed into the SST due to its salient features. For design and control of the MMC-based SST, its operational principles are comprehensively analyzed. Based on the analysis, its mathematical model is developed for evaluating steady-state performances. For optimal design of the MMC-based SST, the mathematical model is modified by considering circuit parameters.

One of the challenges of the MMC-based SST is the balancing of capacitor voltages. The performances of various voltage balancing algorithms and different modulation methods have not been comprehensively evaluated. In this thesis, the performances of different voltage-balancing algorithms and modulation methods are analyzed and evaluated. Based on the analysis, two improved voltage-balancing algorithms are proposed in this thesis.

For design of the MMC-based SST, existing references only focus on optimal design of

medium-frequency transformer (MFT). In this thesis, an optimal design procedure is developed for the MMC under medium-frequency operation based on the mathematical model of the MMC-based SST. The design performance of MMC is comprehensively evaluated based on free system parameters.

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LIST OF SYMBOLS

Variable	
α	Initial switching angle of SM.
α_i	Initial switching angle of the i^{th} SM within an arm (i ranges from 1 to N_{SM}).
α_k	Initial switching angle of an SM during the k^{th} switching period of an alternating period (k ranges from 1 to N_{SM}).
B_{Larm}	Flux density of arm inductor.
C	Capacitance of SM capacitor.
f_{ac}	The fundamental frequency of ac-link voltage.
f_{SW}	Switching frequency of SM.
i_{arm}	Arm current.
i_{ci}	Capacitor current of the i^{th} SM.
i_x	AC-side current of phase x ($x = a, b, c,$ and d).
$i_{xu},\ i_{xl}$	Upper- and lower-arm currents of phase x ($x = a, b, c,$ and d).
i_{zx}	Circulating current of phase x ($x = a, b, c,$ and d).
L_{tot}	Total inductance including arm inductance and leakage inductance of ac-link transformer.
L_{arm}	Inductance of arm inductor.
L_{T}	Leakage inductance of ac-link transformer.
n_T	Turn ratio of ac-link transformer.
N_{BLK}	Number of blocked SM capacitors per arm.
N_C	Number of blocked capacitors per arm.
N_{insert}	Number of inserted SMs per arm.
N_{SM}	Number of SM per arm.
ω	Angular frequency equals to $2\pi f_{\mathrm{ac}}$.

Variable	
Φ	Phase shift angle for power regulation of MMC-based SST.
φ	Phase angle at time t, which equals to ωt.
P_{rate}	Rated power of MMC.
P_{con}	Conduction loss of semiconductor device.
P_{sw}	Switching loss of semiconductor device.
P_{conT}	Conduction loss of IGBT/MOSFET.
P_{conD}	Conduction loss of diode.
Q_c	Capacitor charge of an SM during a switching period.
Q_{ci}	Capacitor charge of the i^{th} SM within an arm (i ranges from 1 to N_{SM}).
Q_{ck}	Capacitor charge of an SM during the k^{th} switching period of an altenating period (k ranges from 1 to N).
R_{arm}	Winding resistance of arm inductor.
R_{T}	Winding resistance of ac-link transformer.
S_{SM}	Switching function of an SM.
θ_{R}	Ramping angle of ac-link voltage.
θ	Phase-shift angle bwteen adjacent SMs based on phase-shift modulation, which equals to $\frac{\theta_{\text{R}}}{N_{\text{SM}}}$.
$\tan\delta$	Tangent of loss angle.
T_{ac}	Period of ac-side voltage.
T_{SW}	Switching period of SM.
T_s	Simulation time step.
Δv_c	Variation of capacitor voltage of an SM induced from capacitor charge during a switching period.
$v_{\text{ac,pri}}$	Primary-side ac-link voltage.
$v_{\text{ac,sec}}$	Secondary-side ac-link voltage.

Variable

v_{ci}	Capacitor voltage of the i^{th} SM.
$V_{\text{dc,pri}}$,$I_{\text{dc,pri}}$	Primary-side dc-link voltage and current.
$V_{\text{dc,sec}}$,$I_{\text{dc,sec}}$	Secondary-side dc-link voltage and current.
v_{xu}, v_{xl}	Upper- and lower-arm voltages of phase x ($x = a, b, c,$ and d).
V_{LL}	Amplitude of the ac-side line-to-line voltage.
V_{dc}	DC-bus voltage.
V_C^{nom}	Nominal voltage of SM capacitor.
V_{arm}, v_{arm}	Voltage across each arm.
$V_C^{\text{I,SS}}$	Uncontrollable steady-state SM capacitor voltage during Stage I.
V_C^{ini}	Initial SM capacitor voltage for controllable startup.

LIST OF ABBREVIATIONS

Abbreviation	
3LX/5LX	Three-level/Five-level Cross Connected
AMBA	Alternate Modulation Balance Algorithm
BESS	Battery Energy Storage System
CD	Clamp Double
D-MPC	Direct Model Predictive Control
DAB	Dual-active Bridge Converter
DSM	Detailed Switching Model
ECM	Equivalent Circuit Model
EMT	Electromagnetic Transient
ESS	Energy Storage System
EV	Electric Vehicle
FB	Full Bridge
FBL	Fault Bocking
FCS-MPC	Finite Control Set Model Predictive Control
HB	Half Bridge
HVDC	High Voltage Direct Current
IM2DC	Isolated Modular Multilevel DC-DC Converter
LMMC	Lattice Modular Multilevel Converter
MFT	Medium-frequency Transformer
MMC	Modular Multilevel Converter
MPC	Model Predictive Control
MTDC	Multi-terminal Direct Current

Abbreviation	
NLC	Nearest-level Control
PHMMC	Parallel Hybrid Modular Multilevel Converter
PS	Phase Shift
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Source
RMS	Root Mean Square
RSF	Reduced Switching Frequency
SM	Submodule
SSC	Stacked Switched Capacitor
SST	Solid State Transformer
STATCOM	Static Synchronous Compensator
SV-PWM	Space Vector Pulse Width Modulation
UFB	Unipolar-voltage Full Bridge
VSC	Voltage Sourced Converter

Chapter 1

INTRODUCTION

1.1 Basics of Modular Multilevel Converter

The modular multilevel converter (MMC) is firstly proposed by R. Marquardt in 2003 [1], which became an attractive converter for high power applications due to its salient features: 1) its modularity and scalability to meet high voltage requirements, 2) reduced voltage ratings and dv/dt stress of switches and capacitors, 3) high efficiency, 4) improved power quality for filter-free applications, 5) inherent fault-tolerance capability and 6) fault-blocking capacity to improve fault interruption performance of the MMC-based high-voltage direct current (HVDC) systems. Therefore, the MMC has become the basic building block for multi-terminal direct current(MTDC) systems and DC grids [2].

Fig. 1.1 shows a schematic diagram of a three-phase MMC. The MMC consists of two arms per phase leg. Each arm comprises N series-connected submodules (SMs), and an arm inductor. The SMs in each arm are controlled to generate the required arm voltage. The arm inductor is utilized as an ac filter to suppress the high-frequency harmonics of the arm current.

1.1.1 Typical Applications

The MMC is initially proposed for the HVDC systems. Recently, it has been employed into various high power applications, including the grid integration systems of the renewable energy sources (RESs), the medium-voltage motor drive systems, energy storage systems (ESSs), the solid-state transformers (SSTs), etc.

- HVDC systems: The MMC is one of the competitive converters for the voltage

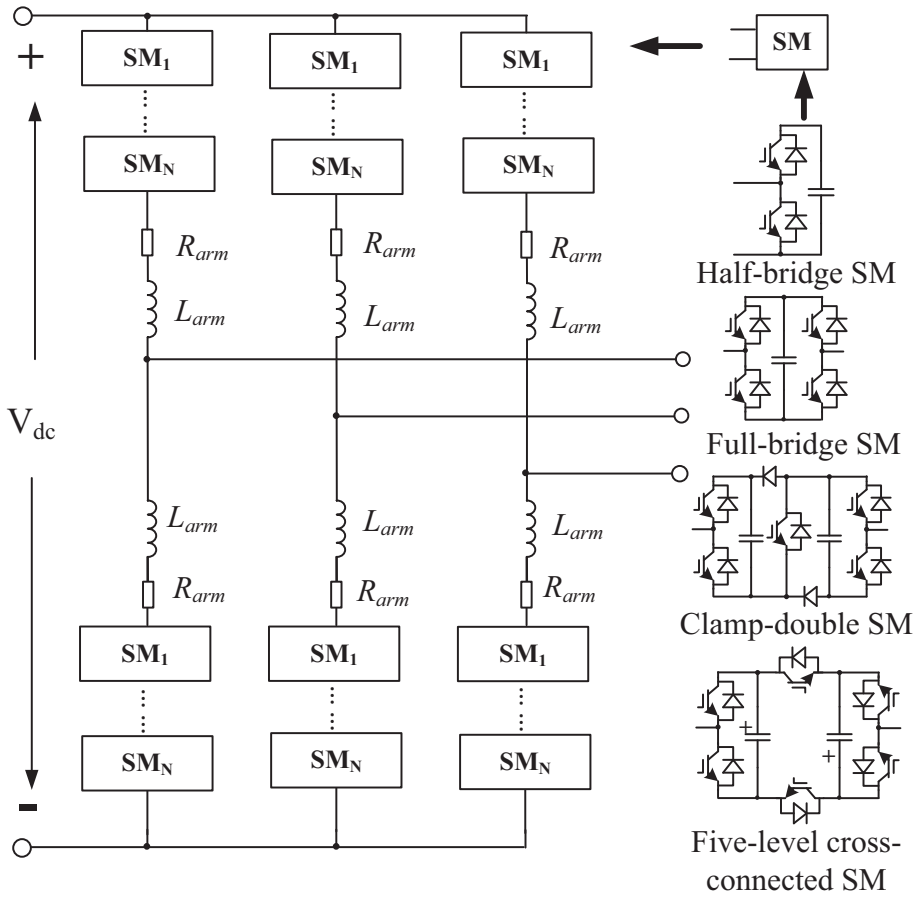


Figure 1.1. Schematic diagram of MMC with various SMs.

sourced converter (VSC) based HVDC applications [3–9]. The MMC has been employed into several practical HVDC systems, which are listed in Table 1.1 [10–15]. To improve the fault blocking capability of MMC, the fault-blocking SMs are proposed in [2, 16]. Several improved topologies are proposed in [17–19] to increase the voltage rating of dc side.

- Grid integration systems of RESs: During recent few years, the MMC is employed into grid integration systems of RESs, such as offshore wind farms and large-scale photovoltaic (PV) plants [20–31].

- AC motor drives: The MMC is also utilized as a medium-voltage motor drive. Under

low-speed operating condition, the low-frequency voltage fluctuation of capacitor is the main issue of the MMC-based medium-voltage motor drives. In [32–35], several circulating current injection methods have been presented to suppress the low-frequency voltage ripple of SM capacitor.

- Energy storage systems: During recent several years, the MMC is employed into grid-tied battery energy storage system (BESS) [36–44], as well as the small scale BESS in electric vehicle (EV) [45–47].

- Other applications: The MMC is also employed into other applications, such as STATCOM and SSTs [48–53].

Table 1.1
MMCs-Embedded HVDC Systems around the World [10–15]

	Terminals	Commissioning year	Rated capacity (MW)	DC voltage (kV)
Trans Bay Cable Project	2	2010	400	±200
INELFE, France-Spain,	2	2014	2×1000	±320
BorWin2 HVDC System	2	2015	800	±300
Nan'ao	3	2015	200/100/50	±160
Zhoushan	5	2016	400/300/100/100/100	±200
Zhangbei	4	Under construction	3000/3000/1500/1500	±500

1.1.2 Configurations and Topologies of Modular Multilevel Converters

A Submodule configurations and switching states

The SM is the basic building block of MMC. The half-bridge (HB) circuit is a dominant configuration of SM in MMC. However, in case of a dc-side fault, the MMC consisting of the HB SMs (HB-MMC) cannot block the fault currents fed from ac grid. Various SMs are investigated to improve the fault-blocking performance of MMC, such as full-bridge (FB), unipolar-voltage full-bridge (UFB), clamp-double (CD), and three-level/five-level cross-connected (3LX/5LX) SMs , which are denoted as fault-blocking SMs (FBL SMs) in the following part of this thesis [8, 16, 54]. The configurations of various SMs are shown in Fig. 1.2.

In [55, 56], for the HB SM, there are three operating state:

- Inserted: When the upper switch is turned on, while the lower switch is turned off, the capacitor is inserted into arm. The charging and discharging of capacitor is determined by the direction of arm current.

- Bypassed: When the lower switch is turned on, while the upper switch is turned off, the SM is bypassed.

- Blocked: When both switches are turned off, the arm current can only flow through the anti-parallel diodes of $S1$ and $S2$. When the arm current is positive, the capacitor is charged. While when the arm current is negative, the SM is bypassed.

The various SMs are equivalent to the series-connected/parallel-connected HB SMs. $S1$ is logically complementary with $S2$, while $S3$ is logically complementary with $S4$. For the UFB SM, when the conducting switch $S3$ is turned on, it operates as the HB SM. Similarly, for the FB SM, when the conducting switch $S4$ is turned on, it operates as the

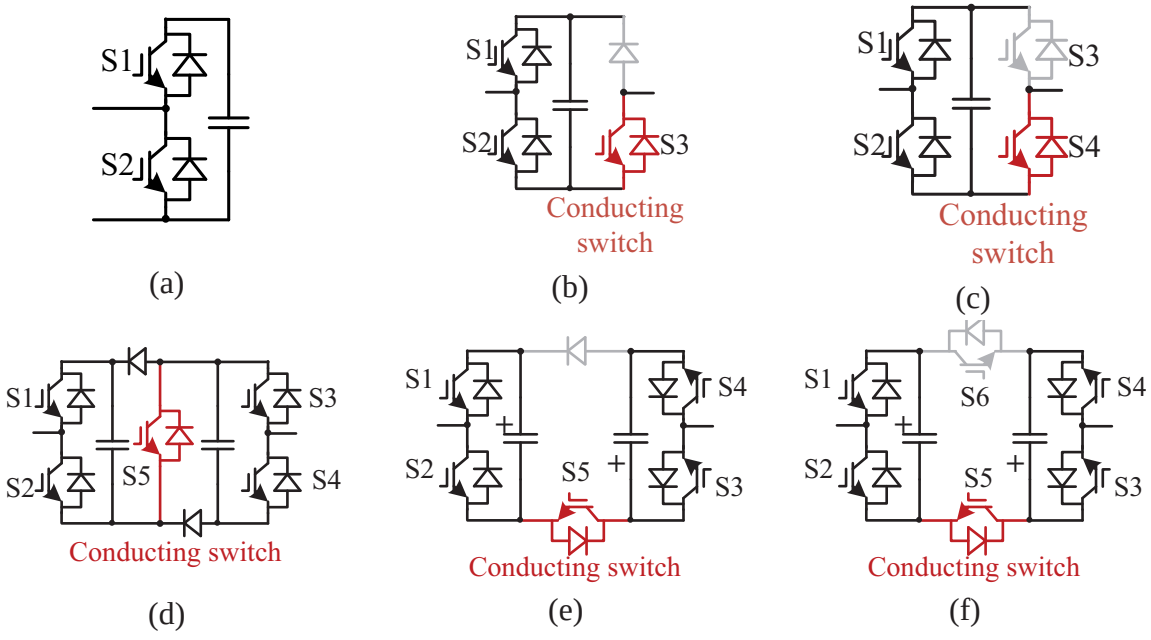


Figure 1.2. The configuration of various SMs: (a) HB SM, (b) UFB SM, (c) FB SM, (d) CD SM, (e) 3LX SM, and (f) 5LX SM.

HB SM. For the CD and 3LX SMs, when conducting switch ($S5$) is turned on, they are equivalent to two series-connected SMs. For the 5LX SM, when $S5$ is turned on, the two HB SMs are positively connected. When $S6$ is turned on, the two HB SMs are inversely connected.

B Topologies of MMCs

The HB-MMC is the dominant topology for high-power applications. The MMC consisting of FBL SMs are proposed for HVDC systems to improve the fault-blocking capability. By combining the HB SMs with FBL SMs in hybrid MMC, it can make a trade off among the dc fault-blocking capability, efficiency, and cost [16].

To improve the performance of MMC, various modified topologies are proposed for MMCs:

- Reduce capacitor size and voltage ripple: Generally, in traditional MMC, the bulky

Table 1.2
Switching States of the Fault-Blocking SMs Under Normal Operating Condition

	S1/S2	**S3/S4**	**S5/S6**	$\mathbf{v_o}$
UFB	1/0	1/-	-/-	v_c
	0/1	1/-	-/-	0
FB	1/0	0/1	-/-	v_c
	0/1	0/1	-/-	0
	1/0	1/0	-/-	0
	0/1	1/0	-/-	$-v_c$
CD	1/0	0/1	1/-	$2v_c$
	0/1	0/1	1/-	v_c
	1/0	1/0	1/-	v_c
	0/1	1/0	1/-	0
3LX	1/0	0/1	1/-	$2v_c$
	0/1	0/1	1/-	v_c
	1/0	1/0	1/-	v_c
	0/1	1/0	1/-	0
5LX	1/0	0/1	1/0	$2v_c$
	0/1	0/1	1/0	v_c
	1/0	1/0	1/0	v_c
	0/1	1/0	1/0	0
	1/0	0/1	0/1	0
	0/1	0/1	0/1	$-v_c$
	1/0	1/0	0/1	$-v_c$
	0/1	1/0	0/1	$-2v_c$

capacitors are required to suppress the voltage ripple. The large number of bulky capacitors increase the cost and volume of MMC, reduce the power density, and limit the widespread applications of MMC [57]. To reduce the capacitor size and voltage ripple, a modified MMC is proposed in [57], which adds a middle SM in each phase leg. Reference [58] proposed a new SM configuration integrated with the stacked

switched capacitor (SSC) energy buffer architecture, which allows larger capacitor voltage ripple and reduces the requirement of capacitor. Reference [59] proposed a flying-capacitor MMC, which is characterized by the cross connection of the upper and lower arms in one phase leg through a flying capacitor. The flying capacitor can redistribute the power between upper arm and lower arm, and hence it can mitigate the capacitor voltage ripple. To reduce the capacitor voltage ripple, an active power decoupling circuit is applied into the SM of MMC, as an active buffer to absorb the power ripple [60].

- Increase dc-link voltage: To increase the dc-link voltage rating and make the MMC more suitable for high voltage application, several modified topologies are proposed in [17, 19], in which the phase legs are connected in series.

- Reduce power losses: Due to the fewer SMs operating outside the main power path, the power losses of parallel hybrid MMC (PHMMC) can be potentially reduced, which have been investigated in [17, 18]. A lattice modular multilevel converter (LMMC) has been proposed in [61], in which the arm consists of two HB SMs combined with a cascade circuit. It provides lower power losses and fault-handling capability.

- Reduce common-mode voltage: For medium-voltage motor drive applications, the common-mode voltage is one concern, when designing the motor drive converters. To solve this problem, an active cross-connected MMC and a flying-capacitor MMC are proposed in [59, 62].

1.1.3 Control Strategies

A Normal operating condition and control strategies

The steady-state operational principles of MMC have been analyzed in [2, 63, 64]. Each arm can be equivalent to a voltage source. By controlling the arm voltages, the controlling purposes are achieved.

Under normal operating condition, the control strategies of MMC are classified as classical control strategies and model predictive control strategies [65]. The model predictive control strategies are classified as the finite control set model predictive control (FCS-MPC), direct MPC (D-MPC), indirect MPC, and dual-stage MPC [65]. The classical control strategies can be further classified as distributed control strategy and centralized control strategy.

To guarantee normal operating of MMC, the control strategy consists of modulation methods, the ac-side and dc-side currents controller, the circulating current control algorithms, and capacitor voltage-balancing algorithms.

- Modulation methods: The modulation methods for multilevel converters can be generally classified into carrier-based pulse width modulation (PWM), space vector PWM (SV-PWM) and staircase modulation methods [66–71]. The carrier-based PWM methods for multilevel converter can be divided into phase-shifted carrier-based PWM method [64, 72–74] and level-shifted carrier-based PWM methods [2, 69–71, 75–78].

- Circulating current control strategies: The internal circulating currents do not have impact on the ac-side voltages and currents. However, they can increase the peak and root-mean-square (RMS) value of the arm currents, which consequently increase the converter power losses as well as the ripple magnitude of the SM capacitor volt-

ages. To attenuate the impacts of circulating currents, the circulating current control strategies have been proposed, including passive filter-based methods [79–81], modulation-based methods [82], controller-based methods [40, 60, 83–91], and predictive model based methods [92, 93].

- Capacitor voltage-balancing algorithms: To guarantee the normal operating of MMC, the capacitor voltages should be balanced by the voltage-balancing algorithms [83, 94–101].

B DC Fault Condition

- Fault blocking: Under dc fault condition, the current paths of various SMs are shown in Fig. 1.3. Under this condition, the HB SM is naturally bypassed, while the capacitors in the FBL SMs are charged by the fault current. Figure 1.3 shows the current

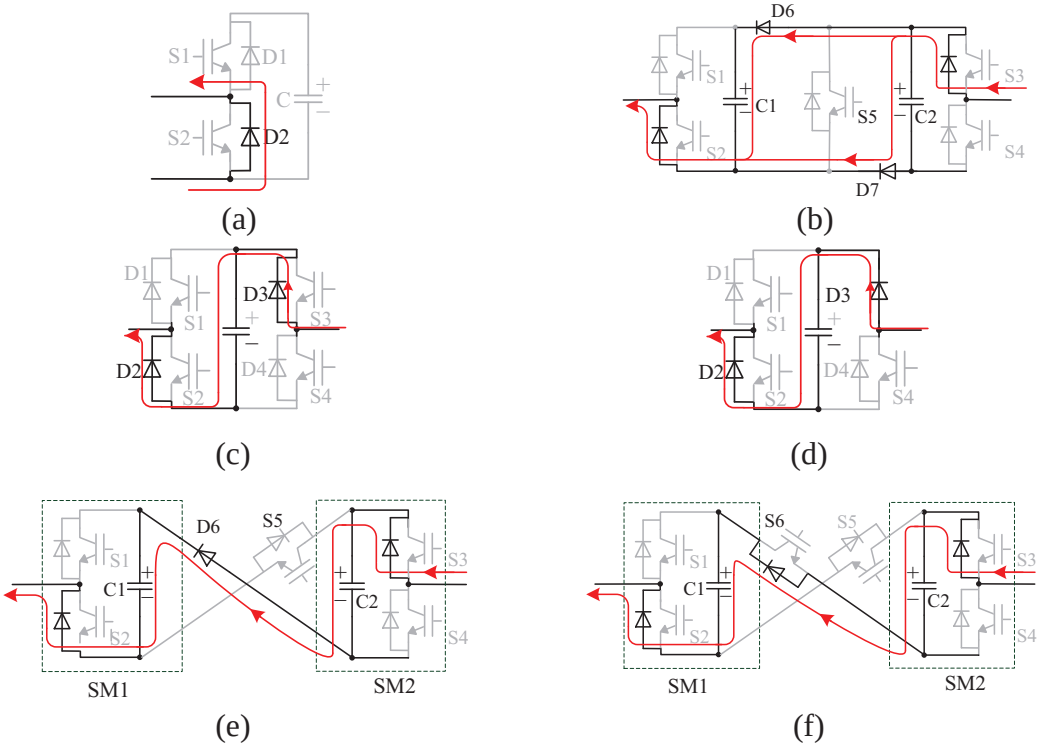


Figure 1.3. The fault current paths of various SMs: (a)HB, (b) CD, (c) FB, (d) UFB, (e) 3LX, and (f) 5LX SM circuits.

path of the hybrid MMC consisting of the HB SMs and the FB SMs. Under the dc fault condition, the HB SMs in each arm are bypassed, while the capacitors in the FB SMs are negatively inserted into the current loop and support the ac-side line-to-line voltage. In this way, the fault current can be blocked. For various MMC configurations, the current paths are similar. For the HB-MMC, the current flows through the diodes and bypassed all SMs. Thus, the HB-MMC cannot block the fault current. For the MMCs consisting of various FBL SMs, all capacitors support the ac-side line-to-line voltage to block the fault current.

- Fault-STATCOM operating mode: Under pole-to-pole dc fault condition, the MMC can provide reactive power to the ac grid when operating in the STATCOM mode. Based on the FBL SMs, the MMCs can produce bipolar arm voltages. Thus, the upper arms, the lower arms, or both lower and upper arms can perform STATCOM function similar to the cascaded H-bridge converters. The fault-STATCOM control

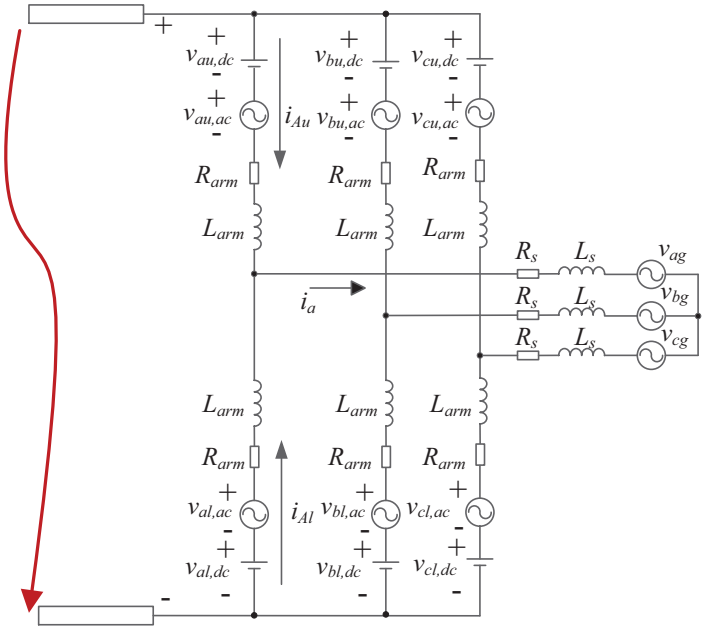


Figure 1.4. The equivalent circuit of fault-blocking MMC under fault-STATCOM condition.

strategy has been summarized in [50, 102]. Under fault-STATCOM condition, the equivalent circuit of the fault-blocking MMCs is shown in Fig. 1.4. The fundamental-frequency arm voltage is controlled to regulate the reactive power transfer. The reference of dc circulating current is set to be zero. The ac grid needs to compensate the power loss of MMC to maintain the capacitor voltage. The overall control is shown in Fig. 1.5.

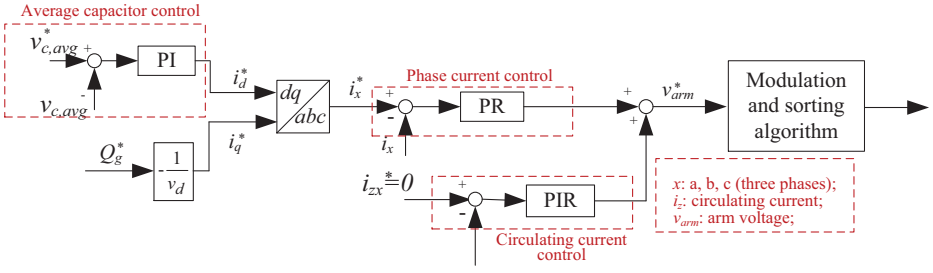


Figure 1.5. The block diagram of the control strategy for the fault-blocking MMCs under fault-STATCOM condition.

1.2 Literature Review and Statement of the Problem

1.2.1 Precharging Strategy of MMC-Based HVDC Systems

Before entering the normal operating condition, the SM capacitors in MMC should be smoothly precharged to their nominal voltages during the converter startup process. Otherwise, the inrush current might lead to the destroy of semiconductor devices and capacitors. The existing precharging methods can be classified as:

- Closed-loop methods: In [55, 103], the closed-loop startup control methods are applied to charge the SM capacitors from ac or dc side. Reference [104] investigates the startup issue of the CD SM-based MMC-HVDC system and proposes a grouping sequentially controlled charge method. However, the method is specifically applica-

ble to the MMC with the CD SMs and additional control effort is needed to group and charge the SM capacitors.

- Open-loop methods: In [105] and [106], an auxiliary voltage source is employed to charge the SM capacitors individually.

The closed-loop methods require additional effort to analyze the small-signal model of MMC and to tune parameters of digital controller. The existing open-loop methods require auxiliary voltage sources to charge the SM capacitors, which add to the system complexity and cost. In addition, the existing open-loop methods did not consider various configurations of SMs and topologies of MMC.

1.2.2 Equivalent Circuit Model of MMC

For large-scale MMC-embedded power systems, it is required to investigate dynamic performance, fault characteristics, protection, and stability [107, 108]. Modeling of the MMC is one of the main challenges associated with the study of the large-scale MMC-based power systems. On the other hand, for the purpose of designing an MMC station and its controller, highly efficient model is also needed with considering control parameters/strategies and accurate dynamics of arm voltage/current, dc current, and capacitor voltage. The detailed switching model (DSM) of the MMC for electromagnetic transient (EMT) simulation is time consuming due to large number of semiconductor switches. To address this challenge, several MMC models have been developed to accelerate the EMT simulation, including average-value models and equivalent circuit models (ECMs) [108–123]. The problems of these models are briefly summarized as follows:

- SM configuration: In [109, 110, 112, 114, 119, 120, 123], the ECMs only considered the HB SM, which are not capable of blocking fault current under dc-fault conditions.

In [116], the ECM was developed based on hardware-in-loop (HIL) platform, which considered the FB SM without verifying fault-blocking operations. In [113, 117], the real-time ECMs were implemented by digital controllers, which only considered the operating behaviors of the HB-MMC. In [118, 122], although the ECMs considered the FBL SMs, the arm circuits are not optimal.

- Operating mode: In [108, 111], although the ECMs considered the operating behavior of the FB SM, they did not consider fault-STATCOM operating conditions of the MMCs based on the FBL SMs.

Therefore, there is still a lack of comprehensive considerations of various SM circuits and different operating conditions.

In addition, the impacts of simulation time step on performances of simulation has not been comprehensively analyzed. In [115, 124, 125], the simulation time step is assumed to be equal to the sampling time step, which does not consider practical issues of an industrial controller. In the practical MMC-based systems, the sampling period (or control period) of an industrial controller depends on system requirements and limitations. When considering the requirements of practical system, the simulation time step may not be equal to the sampling period. When fixing the sampling period, the increased simulation time step will lead to additional error. To accurately simulate these MMC-based systems with considering the industrial controllers, the simulation time step must be properly determined, which significantly affects simulation accuracy and computational efficiency. Moreover, the impacts of the simulation time step on voltage-balancing strategies (e.g., sorting algorithm) have never been investigated before.

1.2.3 Control of Solid-State Transformer Based on MMC

The SST has been investigated for distribution systems to reduce the volume and weight of power transformer [126–130]. Recently, the MMC has been employed for SST applications (MMC-based SST) due to its salient features, such as modularity, scalability, high efficiency, and high reliability [53, 131–134]. For instance, the isolated modular multilevel dc-dc converter (IM2DC) is derived based on the dual-active bridge converter (DAB) and shown in Fig. 1.6. The MMC can generate an ac-link voltage with an arbitrary waveform to energize the medium-frequency transformer (MFT), which provides more flexibilities of controlling the SST while avoiding destructive dv/dt stress. To generate the multilevel ac-

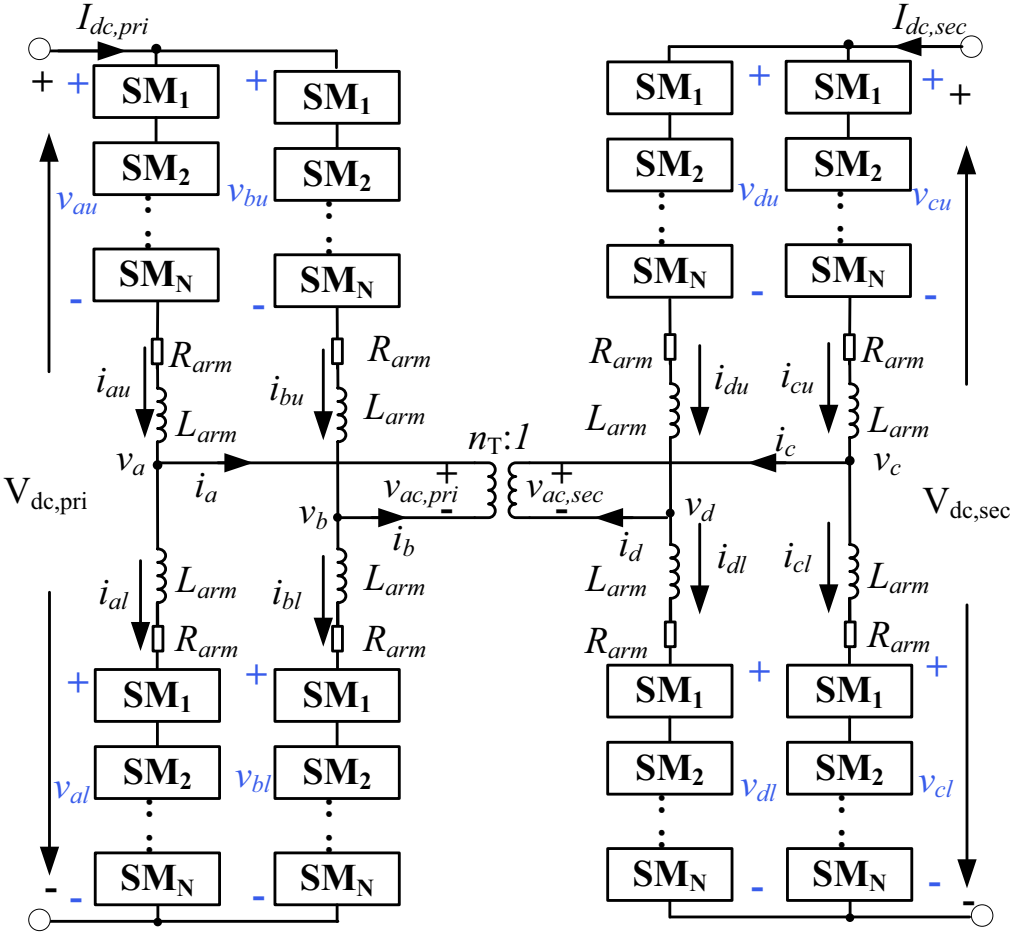


Figure 1.6. Schematic of MMC-based SST.

link voltage, the phase-shift (PS) modulation method has been employed and investigated [53, 133, 135]. However, the nearest-level control (NLC) modulation method, as one of the popular modulation methods, which has not yet been comprehensively studied for the MMC-based SST under medium-frequency operations.

One of the challenges of the MMC under medium-frequency operations for SST applications is capacitor voltage balancing. In [52], a single-step alternating voltage-balancing algorithm is proposed to balance capacitor voltages by alternatively rotating gating signals by one step in each switching period. This algorithm can be easily implemented without voltage and current feedback. However, this single-step alternating voltage-balancing algorithm leads to a low-frequency capacitor voltage ripple. When increasing the number of SMs per arm, the low-frequency ripple will increase. On the other hand, the conventional sorting algorithms in [97] have not been comprehensively investigated for MMC under medium-frequency operations. In summary, there are four control strategies, as listed in Table 1.3.

Table 1.3
Modulation Methods and Voltage-Balancing Algorithms for the MMC-Based SST

Modulation	**Voltage-balancing algorithm**	f_{ac}	References
PS	Single-step alternating	20 kHz	[53]
	Sorting with rearranged phase-shift angles	40 kHz	[136]
	Sorting with voltage deviations	20 kHz	[134]
NLC	Single-step alternating	-	-
	Conventional sorting	250-400 Hz	[131, 132]
Carrier-based PWM	-	10 kHz	[137]
Trapezoidal current modulation	Single-step alternating	3 kHz	[138, 139]

1.2.4 Modeling and Optimal Design of MMC-Based SST

Existing references about the optimal design of the MMC-based SST only focus on the optimal design of MFT [140–143]. However, for the MMC-based SSTs, due to large number of passive components including capacitors, arm inductors, and heat sinks, the volume of MMC dominates the total volume of the MMC-based SST. In addition, there are large number of semiconductor devices in MMC, which might lead to high power losses. For the optimal design of the MMC-based SST, the free system and circuit parameters include fundamental frequency (f_{ac}) and ramping angle (θ_{R}) of ac-link voltage, number of SMs per arm (N_{SM}). In addition, the various modulation methods and voltage-balancing algorithms are considered as free control options. However, their impacts on design of the MMC under medium-frequency operation have not been comprehensively investigated.

To conduct optimal design procedure of the MMC-based SST, the system should be solved by an efficient model with a high accuracy. Although the ECM is accurate and efficient, it is inconvenient for optimal design of MMC due to the need of manually setting free parameters. If the searching space contains a lot of combinations of free parameters, the ECM is not efficient for optimal design. Thus, modeling and formulating the MMC-based SST is an essential part of the optimal design procedure.

1.3 Thesis Objectives

The objectives of this thesis are:

- To develop the generalized precharge strategy for the MMC-based HVDC systems, which considers the various configurations of SMs and topologies of MMC.
- To develop the improved MMC equivalent circuit model, which considers the various SM configurations and operating conditions of MMC. In addition, the impact of

simulation step time is investigated for the MMC-based HVDC systems.

- To develop a mathematical model for optimal design of the MMC-based SST, which considers circuit parameters.
- To develop the voltage-balancing algorithms based on various modulation methods of the MMC-based SST to improve its operating characteristics, which is based on analyzing the operating characteristics of the MMC-based SST.
- To develop the optimal design procedure of MMC under medium-frequency operation for SST applications, which is based on the proposed mathematical model.

1.4 Thesis Outline

Chapter 2 proposes a generalized precharging strategy for the MMC-based HVDC system for the various SM configurations and topologies of MMC.

Chapter 3 proposes an improved equivalent circuit for modeling and simulation of the MMCs based on various configurations and different operating conditions. Moreover, the simulation time step is comprehensively investigated by considering the sampling period of the industrial controller, capacitor voltage-balancing strategies, errors of current and voltage level, and computational efficiency. The impacts of the simulation time step on simulation accuracy and efficiency are analyzed and discussed.

Chapter 4 develops a mathematical model for optimal design of the MMC-based SST based on detailed analysis of its steady-state operation.

Chapter 5 evaluates and develops various voltage-balancing algorithms based on P-S modulation and NLC modulation to improve performances and characteristics of the MMC-based SST.

Chapter 6 develops a systematically design optimization process for MMC under medium-frequency operation for SST applications. The impacts of free parameters are comprehen-

sively investigated.

Chapter 7 concludes this thesis and summarizes the contributions of this work. In addition, the future works are presented.

Chapter 2

PRECHARGING STRATEGY AND STARTUP PROCESS OF MODULAR MULTILEVEL CONVERTERS-BASED HVDC SYSTEMS

One of the main technical challenges associated with the control and operation of the MMC systems is to smoothly precharge the SM capacitors to their nominal voltage during the converter startup process. Otherwise, the inrush current might lead to the destroy of semiconductor devices and capacitors. The existing precharging methods can be classified as closed-loop methods [55, 103, 104] and open-loop methods [105, 106]. The closed-loop methods require additional efforts to analyze the small-signal model of MMC and to tune parameters of digital controller. The existing open-loop methods require auxiliary voltage sources to charge the SM capacitors, which add to the system complexity and cost. In addition, the existing open-loop methods did not consider various configurations of SMs and topologies of MMC.

2.1 The Proposed Generalized Precharging Strategy for MMC-Based HVDC Systems

Generally, the precharging process of MMC includes two stages:

- Uncontrollable precharging (Stage I): During this stage, the SMs are uncontrollable and all the switches are blocked. The charging current from either the ac or the dc side flows through the anti-parallel diodes to charge the SM capacitors to an uncontrollable steady-state voltage $V_C^{\mathrm{I,SS}}$. Since the system is uncontrollable, to limit the inrush charging current, a current-limiting resistor arranged in the dc side, ac side, or the arm loops is employed [55, 104, 144].

- Controllable precharging (Stage II): After Stage I, when an initial voltage built-up

across each SM capacitor, the SMs can be controlled to be in the inserted, bypassed, or blocked state.

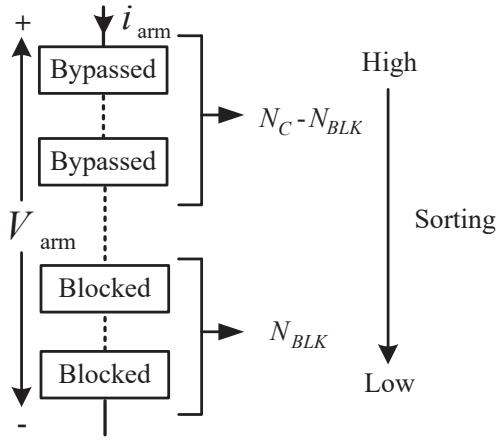


Figure 2.1. The proposed precharging strategy for an arm.

The idea of the proposed precharging strategy is based on control of the number of blocked and bypassed SM capacitors in conjunction with the conventional SM capacitor voltage sorting algorithm. In this way, all SM capacitors can be charged to their nominal voltage V_C^{nom}. When the MMC is connected to a dc voltage source at its dc side or to an ac voltage source at its ac side, a steady-state voltage V_{arm} is established across each arm, as shown in Fig. 2.1.

In detail, for the HB-MMC, during Stage I, the switches are uncontrollable. The capacitor is charged, when the arm current is positive. When the arm current is negative, the charging current flows through the anti-parallel diode of S2. During Stage II, when all SMs are controllable, N_{BLK} SM capacitors out of N_C SM capacitors of each arm are blocked and N_{BY} (where $N_{\text{BY}} = N_C - N_{\text{BLK}}$) SM capacitors are bypassed during startup process to charge the SM capacitors. N_C is the total number of SM capacitors in each arm, where $N_C = N_{\text{SM}}$ for the HB-MMC systems. The relationship between SM capacitor number N_C and SM

number N_{SM} of each arm is given by

$$N_C = \begin{cases} N_{\mathrm{SM}}, & \text{HB, FB, UFB,} \\ 2N_{\mathrm{SM}}, & \text{CD, 3LX, 5LX.} \end{cases} \tag{2.1}$$

During precharging process, the capacitor voltage is related to the number of blocked SMs. To charge capacitors to the nominal voltage V_C^{nom}, the corresponding reference value of N_{BLK} is given by

$$N_{\mathrm{BLK}}^{\mathrm{ref}} = \frac{V_{\mathrm{arm}}}{V_C^{\mathrm{nom}}}, \tag{2.2}$$

where V_{arm} depends on various operating conditions and will be discussed in the following sections. The corresponding $N_{\mathrm{BY}}^{\mathrm{ref}}$ is equal to $(N_C - N_{\mathrm{BLK}}^{\mathrm{ref}})$. To balance the capacitor voltages/energy during the startup precharging process, the conventional sorting algorithm is employed [145].

2.2 Startup Procedures for Various MMC Configurations

Considering various SM circuits, a general startup precharging procedure is developed and described in Fig. 2.2, in which V_C^{ini} is the initial voltage of SM capacitors for controllable startup. In case of the FBL SMs, the conducting switches are turned on. In this way, all SMs are equivalent to the HB SMs and the SM capacitors can be controlled as either in the blocked or the bypassed state. After all capacitor voltages reach their steady-state values, the current-limiting resistor is bypassed and the number of the blocked SM capacitors N_{BLK} is controlled from N_C to $N_{\mathrm{BLK}}^{\mathrm{ref}}$ smoothly in conjunction with the capacitor voltage sorting algorithm, while the number of bypassed SM capacitors is changed from zero to $N_{\mathrm{BY}}^{\mathrm{ref}}$.

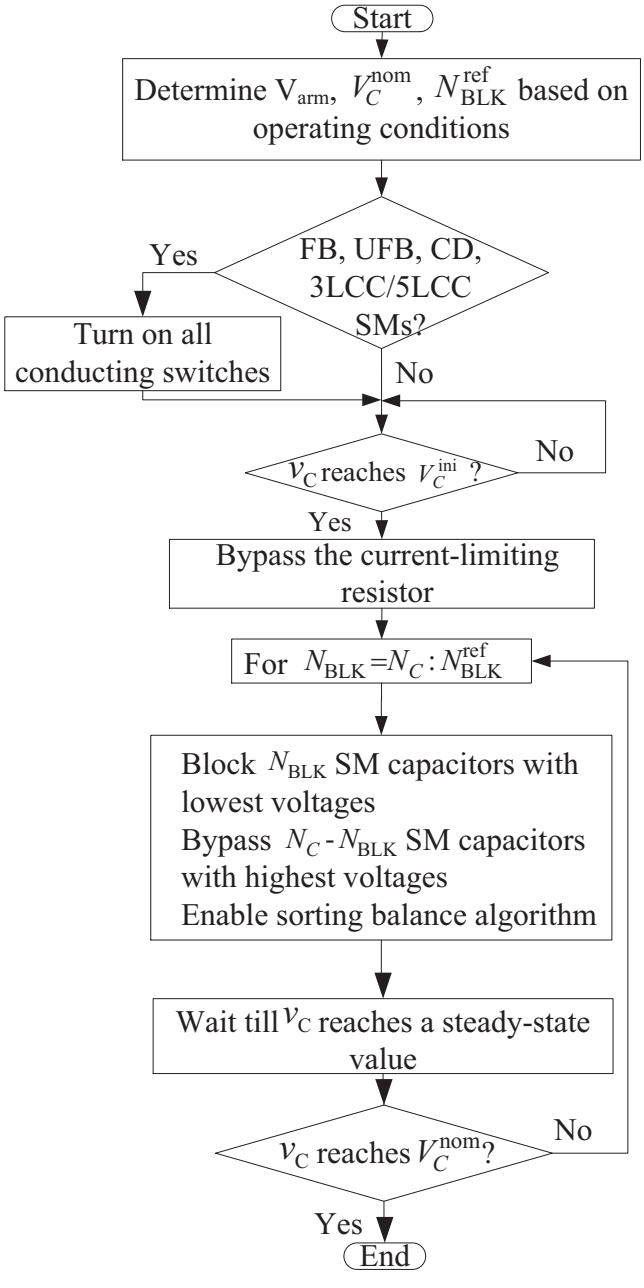


Figure 2.2. Flowchart of the proposed startup strategy of the MMC.

2.2.1 DC-Side Startup

Due to a positive dc-bus voltage on the dc side of the MMC, a positive arm voltage is generated and given by,

$$V_{\text{arm}} = \frac{V_{\text{dc}}}{2}. \tag{2.3}$$

Regardless of the SM circuit topology, the charging current is positive to charge the S-M capacitors. To charge the SM capacitors to their nominal voltage, the corresponding reference number of the blocked SM capacitors is

$$N_{\text{BLK}}^{\text{ref}} = \frac{V_{\text{arm}}}{V_C^{\text{nom}}} = \frac{V_{\text{dc}}}{2V_C^{\text{nom}}}. \tag{2.4}$$

Before starting up, during Stage I, all SM capacitors can be charged to the uncontrollable steady-state voltage $V_C^{\text{I,SS}}$. Then, when all SM circuits are controllable, the precharging process will enter into Stage II. Under this condition, the initial voltage of all SM capacitors for controllable startup (V_C^{ini}) is equal to $V_C^{\text{I,SS}}$, which is given by

$$V_C^{\text{I,SS}} = V_C^{\text{ini}} = \frac{V_{\text{dc}}}{2N_C}, \tag{2.5}$$

2.2.2 AC-Side Startup

When the ac side of the MMC is connected to an ac grid/voltage source, the arm voltage is determined by the ac-side line-to-line voltage and the SM circuit topologies.

- Startup Procedure for the HB-MMC: For the HB-MMC, the charging circuit can be regarded as an uncontrolled rectifier. When v_{ab} is positive, the current flows from phase-*a* upper arm to phase-*b* upper arm. Due to the HB SM circuit, the current flows through the anti-parallel diodes of the SMs in the phase-*a* upper arm, charging the SM capacitors of phase-*b* upper arm, as shown in Fig. 2.3. Thus, the maximum available charging voltage in each arm is $V_{\text{arm}} = V_{\text{LL}}$, where V_{LL} is the amplitude of the ac-side line-to-line voltage.

To charge the SM capacitors to their nominal voltage, the reference number of blocked SM capacitors is $N_{\mathrm{BLK}}^{\mathrm{ref}} = \dfrac{V_{\mathrm{LL}}}{V_C^{\mathrm{nom}}}$ based on (2.2). For the HB-MMC, before starting up, at the end of Stage I, all SM capacitors are charged to the uncontrollable steady-state voltage $V_C^{\mathrm{I,SS}}$. Under this condition, $V_C^{\mathrm{I,SS}}$ and the initial voltage of all SM capacitors for controllable startup (V_C^{ini}) are equal, which are given by

$$V_C^{\mathrm{I,SS}} = V_C^{\mathrm{ini}} = \frac{V_{\mathrm{LL}}}{N_C}. \tag{2.6}$$

By properly controlling N_{BLK} from N_C to $N_{\mathrm{BLK}}^{\mathrm{ref}}$, the SM capacitors can be smoothly charged to their nominal voltages.

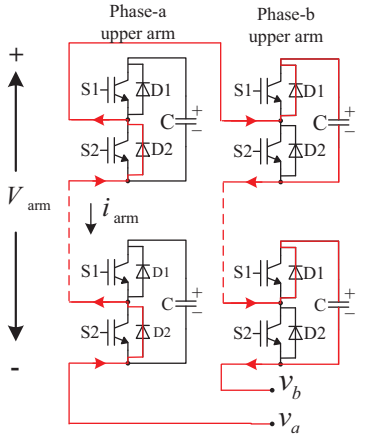


Figure 2.3. HB-MMC charged from ac side.

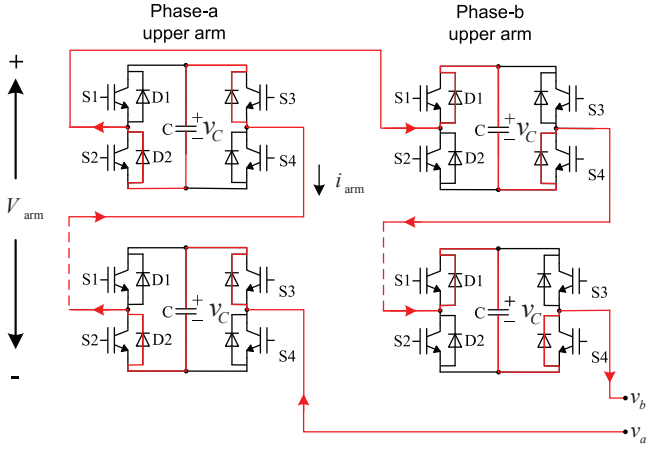


Figure 2.4. FB-MMC charged from ac side.

- Startup Procedure for the FB-MMC: For the FB-MMC, during Stage I, the ac-side

current uncontrollably charges the SM capacitors in both phase-*a* and phase-*b* arms, as shown in Fig. 2.4. Thus, during uncontrollable precharging stage, when blocking all SMs, the maximum available charging voltage across each arm is $\frac{V_{\mathrm{LL}}}{2}$. The steady-state SM capacitor voltage during Stage I is

$$V_C^{\mathrm{I,SS}} = \frac{V_{\mathrm{LL}}}{2N_C}. \tag{2.7}$$

After Stage I, when all SMs are controllable, the conducting switches (i.e., $S4$ in Fig. 2.4) are turned on. The ac-side current flows through the anti-parallel diodes of one arm and charge the SM capacitors in the other arm, which has similar charging behavior of the HB-MMC. The SM capacitors are charged to the initial voltage $V_C^{\mathrm{ini}} = \frac{V_{\mathrm{LL}}}{N_C}$ for controllable startup, which is the same as that of the HB-MMC. Thus, when all SM capacitors are charged to their nominal voltage, the corresponding reference number of the blocked SM capacitors is the same as that of the HB-MMC, i.e., $N_{\mathrm{BLK}}^{\mathrm{ref}} = \frac{V_{\mathrm{LL}}}{V_C^{\mathrm{nom}}}$. For the UFB, 3LX, and 5LX SMs in [16], similar procedures are applied.

- Startup Procedure for the CD-MMC: For the CD-MMC, during Stage I, when the arm current is negative, every two capacitors in each SM are charged in parallel, as shown in Fig. 2.5. When the arm current is positive, the two capacitors in each SM are in series. The equivalent number of SM capacitors in charging loop is $\frac{N_C}{2}+N_C = 1.5N_C$, which support the line-to-line voltage. Thus, at the end of Stage I, all SM capacitor voltages reach to the uncontrollable steady-state voltage

$$V_C^{\mathrm{I,SS}} = \frac{V_{\mathrm{LL}}}{1.5N_C}. \tag{2.8}$$

Subsequent to Stage I, when all SMs are controllable, all conducting switches (i.e., $S5$ in Fig. 2.5) are turned on, and the SM capacitors are charged to the initial voltage $V_C^{\mathrm{ini}} = \frac{V_{\mathrm{LL}}}{N_C}$ for controllable startup, which is the same as that of the HB-MMC. Therefore, the startup procedure for the CD-MMC is similar to that of the FB-MMC.

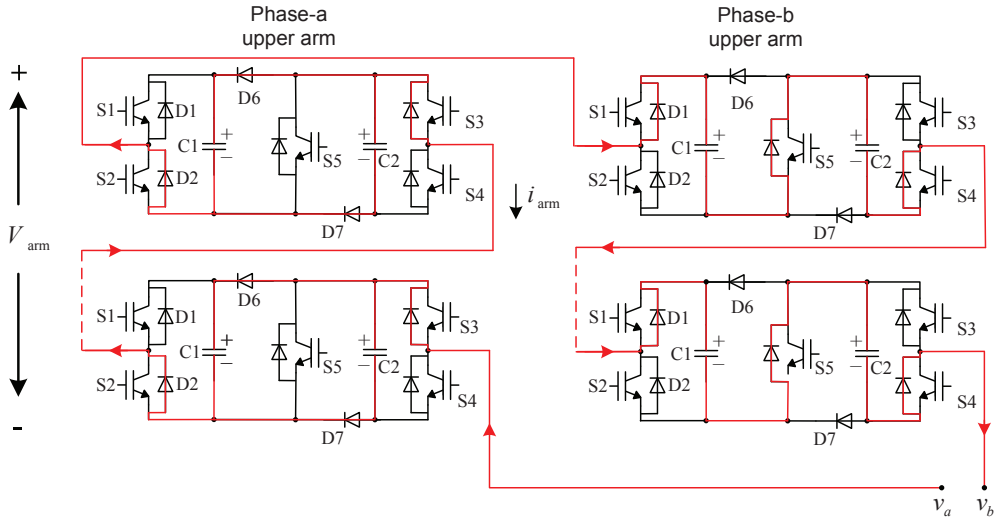


Figure 2.5. CD-MMC charged from ac side.

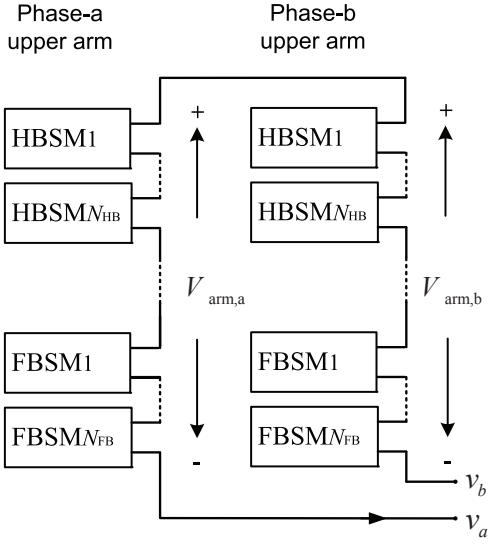


Figure 2.6. Hybrid MMC charged from ac side.

- Startup Procedure for the Hybrid MMC: As shown in Fig. 2.6, for a hybrid MMC consisting of N_{HB} HB and N_{FB} FB SMs in each arm [16, 146], the HB SMs are charged only when the arm current is positive while the FB SMs are charged when the arm current is either positive or negative during Stage I. Therefore, the capacitors in the FB SMs are charged doubled compared to the other capacitors in the HB SMs.

Consequently, the HB and FB SM capacitor charges are respectively expressed by,

$$Q_{\text{HBSM}} = Q_{p,\text{HB}} + Q_{n,\text{HB}}, \tag{2.9}$$

$$Q_{\text{FBSM}} = Q_{p,\text{FB}} + Q_{n,\text{FB}}, \tag{2.10}$$

where, Q_p and Q_n are the charges of the associated SM capacitor when the arm current is in its positive and negative half cycle, respectively. For the same positive arm current, $Q_{p,\text{HB}} = Q_{p,\text{FB}}$. Since the capacitor in the HB SM is bypassed when the arm current is negative, $Q_{n,\text{HB}} = 0$. Assuming that the charges of the HB and FB SM capacitors are the same during positive and negative half cycle, $Q_{p,\text{FB}} = Q_{n,\text{FB}}$. Therefore, the uncontrollable steady-state capacitor voltage during Stage I can be expressed by,

$$2V_{C,\text{HB}}^{\text{I,SS}} = V_{C,\text{FB}}^{\text{I,SS}}. \tag{2.11}$$

Considering the steady-state condition, when phase-*a* current is negative, the capacitors in the FB SMs of phase-*a* and those in the HB and FB SMs of phase-*b* support the line-to-line voltage V_{LL}. Similar situation happens when phase-*a* current is positive. Thus, the second relationship of uncontrollable steady-state capacitor voltage during Stage I is

$$N_{\text{HB}}V_{C,\text{HB}}^{\text{I,SS}} + 2N_{\text{FB}}V_{C,\text{FB}}^{\text{I,SS}} = V_{\text{LL}}. \tag{2.12}$$

Base on (2.11) and (2.12), the uncontrollable steady-state capacitor voltages of the HB and FB SMs are respectively described by (2.13) and (2.14)

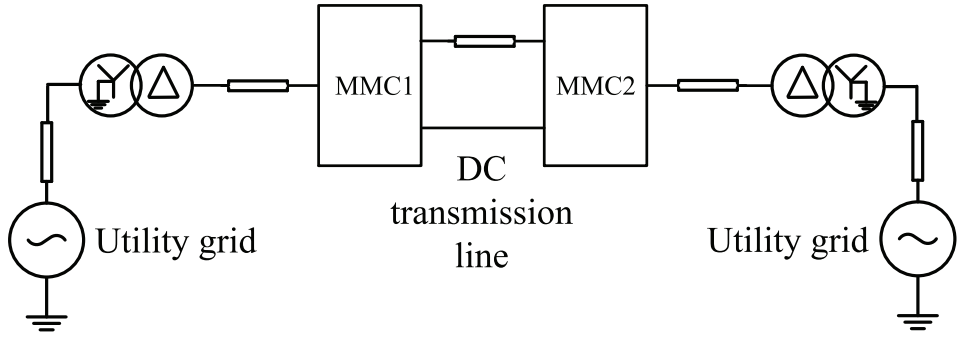
$$V_{C,\text{HB}}^{\text{I,SS}} = \frac{V_{\text{LL}}}{N_{\text{HB}} + 4N_{\text{FB}}}, \tag{2.13}$$

$$V_{C,\text{FB}}^{\text{I,SS}} = \frac{2V_{\text{LL}}}{N_{\text{HB}} + 4N_{\text{FB}}}. \tag{2.14}$$

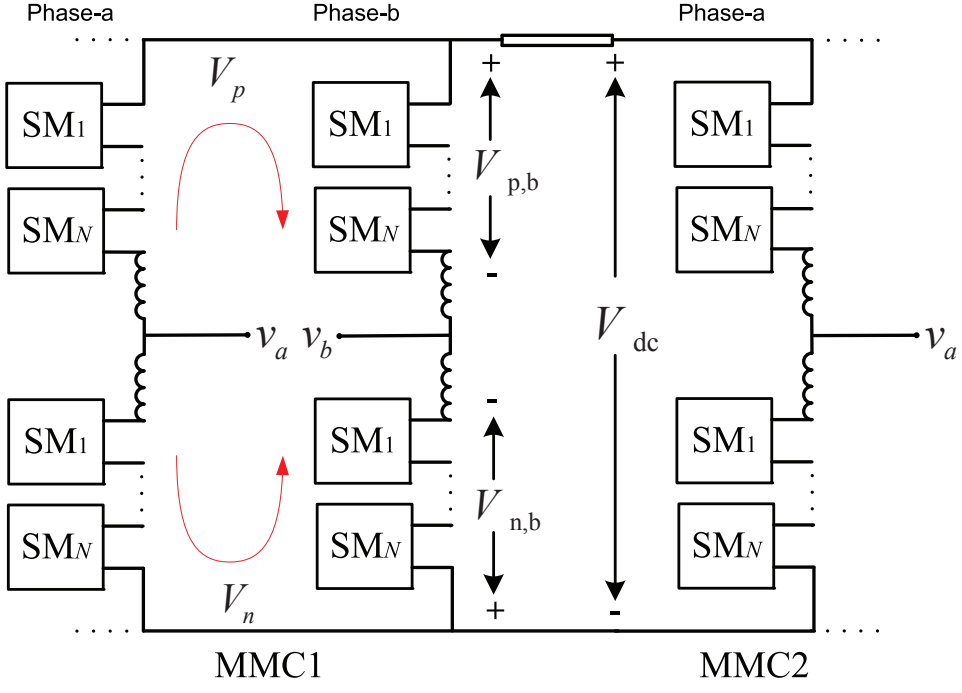
Subsequent to Stage I, when all SMs are controllable, all conducting switches in the FB SMs are turned on and, consequently, each SM capacitor can be charged to $V_C^{\text{ini}} = \frac{V_{\text{LL}}}{N_C}$, which is the same as that of the HB-MMC.

For other SM circuits, the startup procedure is similar to that of the HB-FB hybrid MMC. The only difference is the uncontrollable steady-state SM capacitor voltage $V_C^{I,SS}$ during Stage I, which depends on the number of various types of SMs and their circuit topologies.

2.3 Startup Procedures for the MMC-HVDC Systems



(a)



(b)

Figure 2.7. Schematic representation of the MMC-HVDC system: (a) single-line diagram and (b) circuit diagram.

In terms of the startup process of the MMC-HVDC systems, the ac side of MMC-1 is connected to an ac grid/voltage source, as shown in Fig. 2.7. Once MMC-1 starts up from its ac side and the dc-bus voltage is built up, MMC-2 can start up from its dc side. Thus, MMC-1 experiences an ac-side startup process while MMC-2 starts up from its dc side. A generalized startup procedure for various MMC-HVDC systems is proposed as follows:

- Step 1, when an ac grid is connected to MMC-1, the SM capacitors in MMC-1 are uncontrollably precharged to a steady-state voltage $V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}}$ during Stage I. At the same time, a dc-bus voltage $V_{\mathrm{dc}}^{\mathrm{I}}$ generated by MMC-1 can charge the SMs in MMC-2 to an uncontrollable steady-state voltage $V_{C,\mathrm{MMC2}}^{\mathrm{I,SS}} = \dfrac{V_{\mathrm{dc}}^{\mathrm{I}}}{2N_C}$ based on (2.5).
- Step 2, when the SMs in MMC-1 become controllable after the steady-state voltage $V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}}$ established, if there are FBL SMs in MMC-1, their conducting switches are turned on. Consequently, the new steady-state capacitor voltages of MMC-1 become $V_{C,\mathrm{MMC1}}^{\mathrm{ini}} = \dfrac{V_{\mathrm{LL}}}{N_C}$ and the steady-state dc-bus voltage becomes $V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}}$. The established dc-bus voltage charges the SM capacitors of MMC-2 to a new steady-state voltage $V_{C,\mathrm{MMC2}}^{\mathrm{ini}} = \dfrac{V_{\mathrm{dc}}^{\mathrm{II}}}{2N_C} = \dfrac{V_{\mathrm{LL}}}{2N_C}$ based on (2.5).
- Step 3, when all SMs of MMC-1 and MMC-2 are controllable and all conducting switches are turned on, the current-limiting resistor is bypassed and the number of blocked (bypassed) SM capacitors is controlled from N_C to $N_{\mathrm{BLK}}^{\mathrm{ref}}$ to charge the SM capacitors to their nominal voltages.

The uncontrollable steady-state capacitor voltage and dc-bus voltage during Stage I are determined by the types of SM circuits and discussed in the following.

As shown in Fig. 2.7, the steady-state dc-bus voltage is calculated by

$$V_{\mathrm{dc}} = V_{p,b} - V_{n,b}, \tag{2.15}$$

where, $V_{p,b}$ and $V_{n,b}$ are the sum of steady-state SM capacitor voltages within their corresponding arms.

For the HB-MMC-HVDC system, $V_{p,b} = V_{\mathrm{LL}}$ and $V_{n,b} = 0$ based on the current direction of Fig. 2.7. Thus, the dc-bus voltage during Stage I is $V_{\mathrm{dc}}^{\mathrm{I}} = V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}}$.

For the FB-MMC-HVDC system, when all conducting switches are off, $V_{p,b} = V_{n,b} = \frac{V_{\mathrm{LL}}}{2}$ and, consequently, $V_{\mathrm{dc}}^{\mathrm{I}} = 0$ based on (2.15). Thus, the SMs in MMC-2 cannot be charged due to the zero dc-bus voltage. Once all conducting switches in MMC-1 are turned on, a steady-state dc-bus voltage $V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}}$ is produced and the SMs in MMC-2 can be charged from its dc side, which is similar with the HB-MMC-HVDC system. Similarly, for the UFB, 3LX, and 5LX SMs, prior to turning on the conducting switches, $V_{\mathrm{dc}}^{\mathrm{I}} = 0$.

For the CD-MMC-HVDC system, as shown in Fig. 2.7, based on (2.15), the steady-state voltage generated by MMC-1 during uncontrollable stage is calculated by

$$V_{p,b} = N_C V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}} = N_C \frac{V_{\mathrm{LL}}}{1.5N_C}, \tag{2.16}$$

$$V_{n,b} = \frac{N_C V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}}}{2} = \frac{N_C}{2}\frac{V_{\mathrm{LL}}}{1.5N_C}, \tag{2.17}$$

$$V_{\mathrm{dc}}^{\mathrm{I}} = V_{p,b} - V_{n,b} = \frac{1}{3}V_{\mathrm{LL}}. \tag{2.18}$$

The steady-state values of the dc-bus voltage, capacitor voltages, and the number of blocked SM capacitors are summarized in Table 2.1.

For the hybrid MMC-HVDC system consisting of N_{HB} HB SMs and N_{FB} FB SMs, prior to turning on the conducting switches in the FB SMs, based on (2.15), the dc-bus voltage during Stage I is calculated by

$$V_{p,b} = N_{\mathrm{HB}} V_{C,\mathrm{HB}}^{\mathrm{I,SS}} + N_{\mathrm{FB}} V_{C,\mathrm{FB}}^{\mathrm{I,SS}}, \tag{2.19}$$

$$V_{n,b} = N_{\mathrm{FB}} V_{C,\mathrm{FB}}^{\mathrm{I,SS}}, \tag{2.20}$$

therefore,

$$V_{\mathrm{dc}}^{\mathrm{I}} = V_{p,b} - V_{n,b} = N_{\mathrm{HB}} V_{C,\mathrm{HB}}^{\mathrm{I,SS}}. \tag{2.21}$$

Table 2.1

The Steady-State Values for Various MMC-HVDC Systems

	HBSM	FB/UFB/ 3LX/5LXSM	CDSM
$V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}}$	$\frac{V_{\mathrm{LL}}}{N_C}$	$\frac{V_{\mathrm{LL}}}{2N_C}$	$\frac{V_{\mathrm{LL}}}{1.5N_C}$
$V_{C,\mathrm{MMC1}}^{\mathrm{ini}}$	$\frac{V_{\mathrm{LL}}}{N_C}$	$\frac{V_{\mathrm{LL}}}{N_C}$	$\frac{V_{\mathrm{LL}}}{N_C}$
$V_{\mathrm{dc}}^{\mathrm{I}}$	V_{LL}	0	$\frac{V_{\mathrm{LL}}}{3}$
$V_{\mathrm{dc}}^{\mathrm{II}}$	V_{LL}	V_{LL}	V_{LL}
$V_{C,\mathrm{MMC2}}^{\mathrm{I,SS}}$	$\frac{V_{\mathrm{LL}}}{2N_C}$	0	$\frac{V_{\mathrm{LL}}}{6N_C}$
$V_{C,\mathrm{MMC2}}^{\mathrm{ini}}$	$\frac{V_{\mathrm{LL}}}{2N_C}$	$\frac{V_{\mathrm{LL}}}{2N_C}$	$\frac{V_{\mathrm{LL}}}{2N_C}$
$N_{\mathrm{BLK,MMC1}}^{\mathrm{ref}}$	$\frac{V_{\mathrm{LL}}}{V_C^{\mathrm{nom}}}$	$\frac{V_{\mathrm{LL}}}{V_C^{\mathrm{nom}}}$	$\frac{V_{\mathrm{LL}}}{V_C^{\mathrm{nom}}}$
$N_{\mathrm{BLK,MMC2}}^{\mathrm{ref}}$	$\frac{V_{\mathrm{LL}}}{2V_C^{\mathrm{nom}}}$	$\frac{V_{\mathrm{LL}}}{2V_C^{\mathrm{nom}}}$	$\frac{V_{\mathrm{LL}}}{2V_C^{\mathrm{nom}}}$

The above analysis is applicable to the hybrid MMC-HVDC systems with other types of SM circuits. Once all conducting switches are turned on, the charging procedure becomes similar to that of the HB-MMC-HVDC system.

2.4 Study Results

In this section, performance of the proposed strategy for various MMC-HVDC systems with different SM circuits is evaluated based on simulation studies in the PSCAD/EMTDC software environment. The study system parameters are the same as those used in [16].

2.4.1 Startup Process of an MMC from the DC Side

Figure 2.8 shows the startup process of the HB-MMC system from its dc side. During Stage I, the SMs are uncontrollable and the current-limiting resistor is inserted to limit the

charging current. The SM capacitor voltages are charged to their uncontrollable steady-state voltage $V_C^{\mathrm{I,SS}} = \frac{V_{\mathrm{dc}}}{2N_C} = 1.5$ kV at $t = 0.5$ s. During Stage II, the SMs are controllable and the current-limiting resistor is bypassed. From $t = 0.5$ s, as shown in Figs. 2.8 (a) and (c), the number of blocked SM capacitors is dynamically controlled from $N_C = 20$ to $N_{\mathrm{BLK}}^{\mathrm{ref}} = \frac{V_{\mathrm{dc}}}{2V_C^{\mathrm{nom}}} = \frac{60kV}{2 \times 3kV} = 10$ to charge the SM capacitors to their nominal voltage. The arm currents are limited by the changing rate of N_{BLK}, as shown in Fig. 2.8 (b). As expected, the startup process of the MMCs and the hybrid MMCs based on the SMs with fault-blocking capability is similar to that of the HB-MMC.

2.4.2 Startup Process of an MMC from AC Side

In Fig. 2.9, the ac-side startup process of the HB-MMC system is shown. During Stage I (prior to $t = 1$ s), the current-limiting resistor is inserted to limit the charging current. The SM capacitor voltages are charged to their uncontrollable steady-state voltage $V_C^{\mathrm{I,SS}} = \frac{V_{\mathrm{LL}}}{N_C} = 2.1$ kV. After Stage I, the SMs are controllable and the current-limiting resistor is bypassed at $t = 1$ s. The number of blocked SM capacitors is changed from $N_C = 20$ to $N_{\mathrm{BLK}}^{\mathrm{ref}} = 14$ to charge the SM capacitors to their nominal voltage, as shown in Figs. 2.9 (a) and (d). The arm and ac-side currents are limited by the changing rate of N_{BLK}, as shown in Figs. 2.9 (b) and (c). After the startup process, the MMC starts to transfer power between ac and dc sides at $t = 2.5$ s.

The ac-side startup process of the FB-MMC system is illustrated in Fig. 2.10. During Stage I (prior to $t = 0.5$ s), the SMs are uncontrollable and the SM capacitor voltages are charged to their steady-state voltage $V_C^{\mathrm{I,SS}} = \frac{V_{\mathrm{LL}}}{2N_C} = 1.1$ kV. After Stage I, all conducting switches are turned on at $t = 0.5$ s. Consequently, the SM capacitors are charged to their new steady-state voltage $V_C^{\mathrm{ini}} = \frac{V_{\mathrm{LL}}}{N_C} = 2.1$ kV at $t = 1$ s, which is the same as that of the HB-MMC. At $t = 1$ s, the current-limiting resistor is bypassed, and the number of blocked SM capacitors is being dynamically controlled from $N_C = 20$ to $N_{\mathrm{BLK}}^{\mathrm{ref}} = 14$ to charge

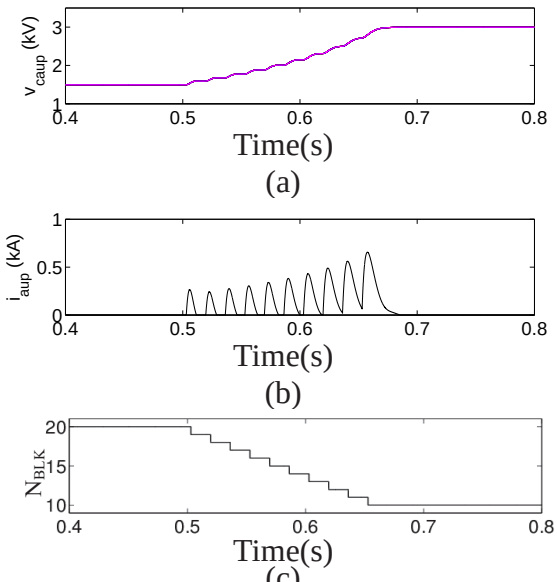


Figure 2.8. DC-side startup process of the HB-MMC system: (a) SM capacitor voltages of the phase-*a* upper arm, (b) phase-*a* upper arm current, and (c) the commanded number of blocked SM capacitors within each arm.

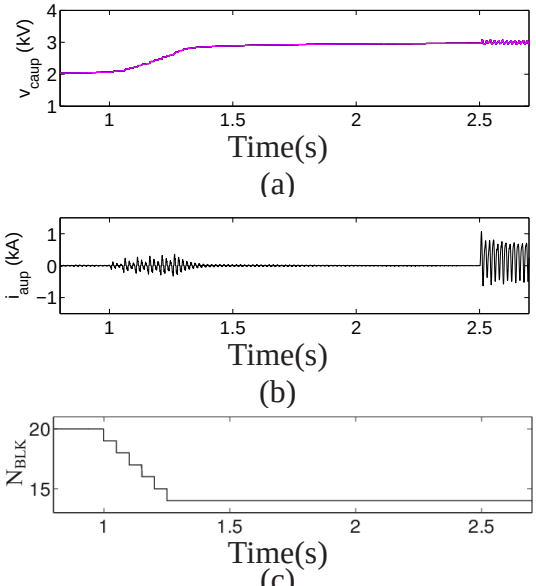


Figure 2.9. AC-side startup process of the HB-MMC system: (a) SM capacitor voltages of the phase-*a* upper arm, (b) phase-*a* upper arm current, and (c) the commanded number of blocked SM capacitors within each arm.

the SM capacitors to their nominal voltage, as shown in Fig. 2.10. The arm and ac-side currents are limited by the changing rate of N_{BLK}. After the startup process, the MMC starts to transfer power between its ac and dc side at t = 1.8 s. For the UFB, 3LX, and 5LX SM-based MMC systems, the startup process is similar to that of the FB-MMC.

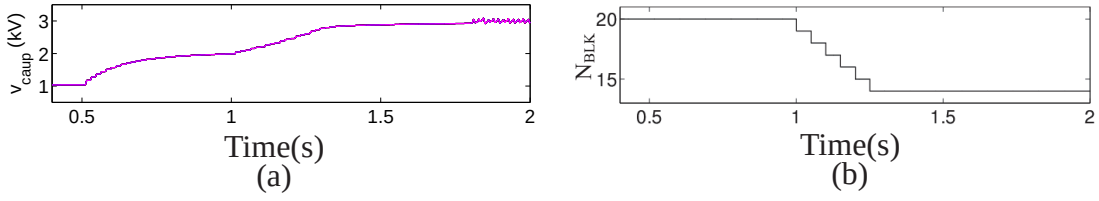


Figure 2.10. AC-side startup process of the FB-MMC system: (a) SM capacitor voltages of the phase-*a* upper arm and (b) the number of blocked SM capacitors per arm.

The startup process of the CD-MMC is also similar to that of the FB-MMC. However, the uncontrollable steady-state capacitor voltage during Stage I is different. For the CD-

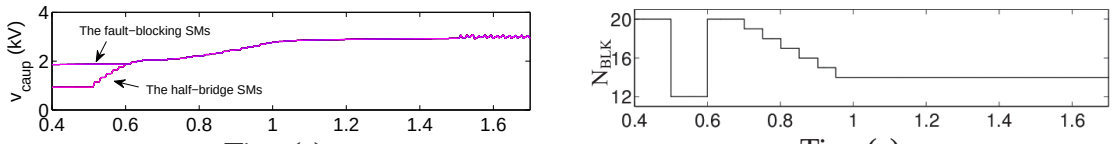


Figure 2.11. AC-side startup process of the hybrid MMC system based on HB SM ($N_{\mathrm{HB}} = 12$) and UFB SM ($N_{\mathrm{UFB}} = 8$): (a) SM capacitor voltages of the phase-*a* upper arm, and (b) the number of blocked SM capacitors per arm.

MMC, $V_C^{\mathrm{I,SS}} = \dfrac{V_{\mathrm{LL}}}{1.5N_C} = 1.4$ kV.

For the hybrid MMC consisting of $N_{\mathrm{HB}} = 12$ HB and $N_{\mathrm{UFB}} = 8$ UFB SMs in each arm, the uncontrollable steady-state voltages of the HB and UFB SMs respectively reach $V_{C,\mathrm{HB}}^{\mathrm{I,SS}} = 0.96$ kV and $V_{C,\mathrm{UFB}}^{\mathrm{I,SS}} = 1.9$ kV around $t = 0.5$ based on (2.13) and (2.14), as shown in Fig. 2.11. Subsequent to Stage I, when all conducting switches are turned on while setting $N_{\mathrm{BLK}} = N_{\mathrm{HB}} = 12$ between 0.5 s and 0.6 s, the SM capacitors of the HB and UFB SMs are charged to the same steady-state voltage $V_C^{\mathrm{ini}} = 2.1$ kV at $t = 0.6$ s. After the SM capacitor voltages reach the same value, the current-limiting resistor is bypassed and N_{BLK} is controlled from $N_C = 20$ to $N_{\mathrm{BLK}}^{\mathrm{ref}} = 14$ to charge the SM capacitors to their nominal voltage, as shown in Fig. 2.11.

2.4.3 Startup Process of the MMC-HVDC System

Figure 2.12 illustrates the startup process of the HB-MMC-HVDC system. Prior to $t = 0.6$ s, both MMC-1 and MMC-2 are in uncontrollable stage while $V_{\mathrm{dc}}^{\mathrm{I}} = V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}} = 42$ kV, in which the SMs of the two MMCs are charged to the uncontrollable steady-stage voltage $V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}} = \dfrac{V_{\mathrm{LL}}}{N_C} = 2.1$ kV and $V_{C,\mathrm{MMC2}}^{\mathrm{I,SS}} = \dfrac{V_{\mathrm{LL}}}{2N_C} = 1.1$ kV, respectively, as shown in Figs. 2.12 (a) and (e). After $t = 0.6$ s, both SMs are controllable and the current-limiting resistor is bypassed. The number of blocked SM capacitors is being changed from $N_C = 20$ to $N_{\mathrm{BLK}}^{\mathrm{ref}}$ ($N_{\mathrm{BLK}}^{\mathrm{ref}} = 14$ for MMC-1 and $N_{\mathrm{BLK}}^{\mathrm{ref}} = 7$ for MMC-2) to charge the SM capacitors to their nominal voltages, as shown in Figs. 2.12 (a), (d), (e), and (h). The arm and ac-

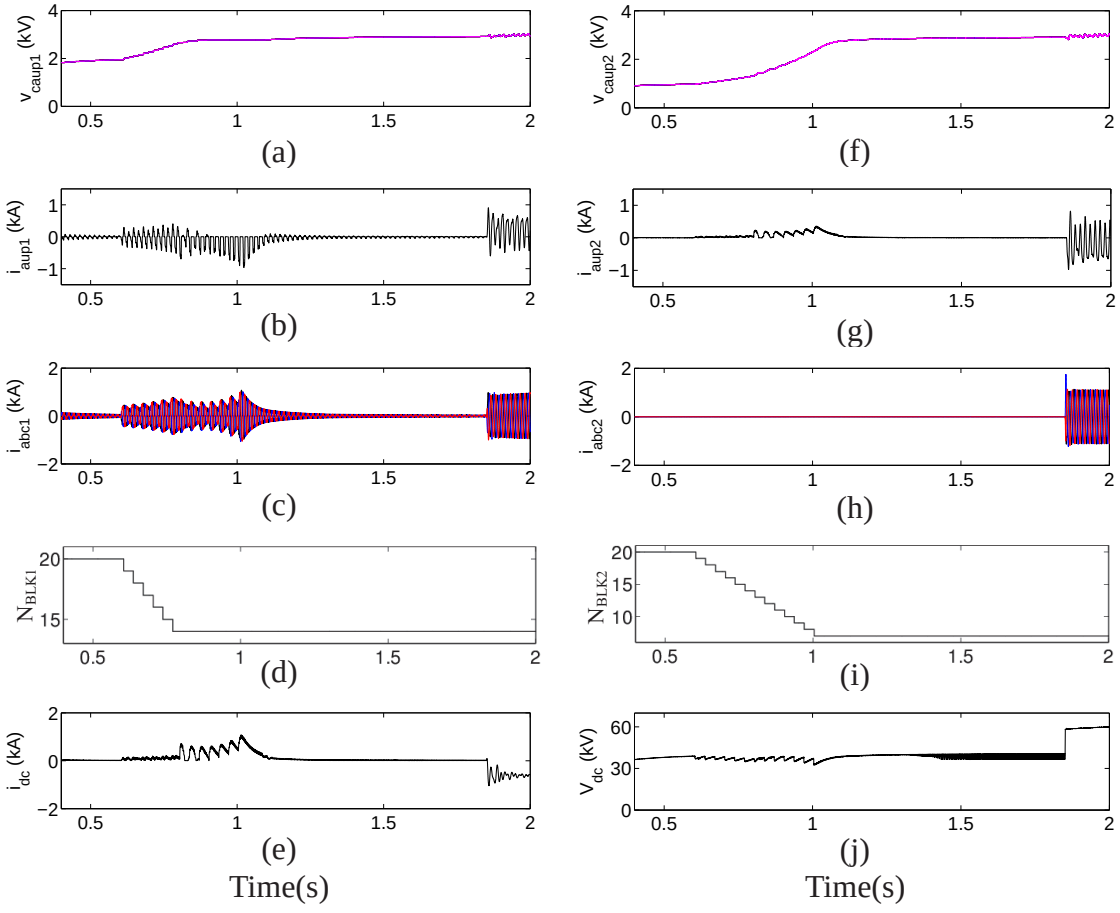


Figure 2.12. The startup process of the HB-MMC-HVDC system: (a) SM capacitor voltages of the phase-*a* upper arm of MMC-1, (b) and (c) phase-*a* upper arm and ac-side currents of MMC-1, (d) the commanded number of blocked SM capacitors of MMC-1, (e) dc current, (f) SM capacitor voltages of the phase-*a* upper arm of MMC-2, (g) and (h) phase-*a* upper arm and ac-side currents of MMC-2, (i) the commanded number of blocked SM capacitors of MMC-2, and (j) dc-bus voltage.

side currents are limited by the changing rate of N_{BLK}, as shown in Figs. 2.12 (b), (c), (d), (f) and (h). Subsequent to the startup process, the MMC-HVDC system starts to transfer power between two ac systems at t = 1.8 s.

In Fig. 2.13, the startup process of the FB-MMC-HVDC system is shown. As shown in Fig. 2.13 (a), the SMs in MMC-1 are precharged to the uncontrollable steady-state voltage $V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}}$ = 1.1 kV (prior to t = 0.2), while the steady-state voltage of the SMs in MMC-2 is zero due to $V_{\mathrm{dc}}^{\mathrm{I}}$ = 0. After t = 0.2 s, the conducting switches of the SMs in MMC-1

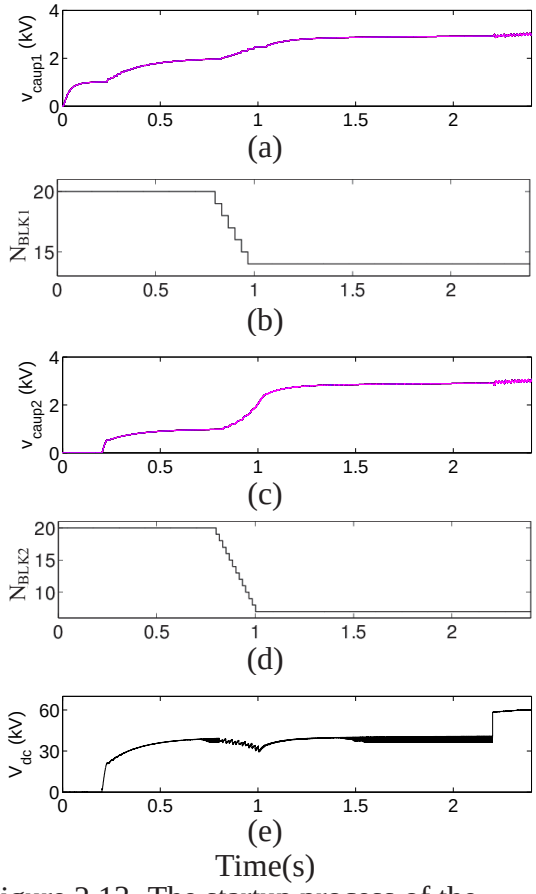


Figure 2.13. The startup process of the FB-MMC-HVDC system: (a), (b), (c), and (d) SM capacitor voltages and the commanded number of blocked SM capacitors of the phase-*a* upper arm of MMC-1 and MMC-2, and (e) dc-bus voltage.

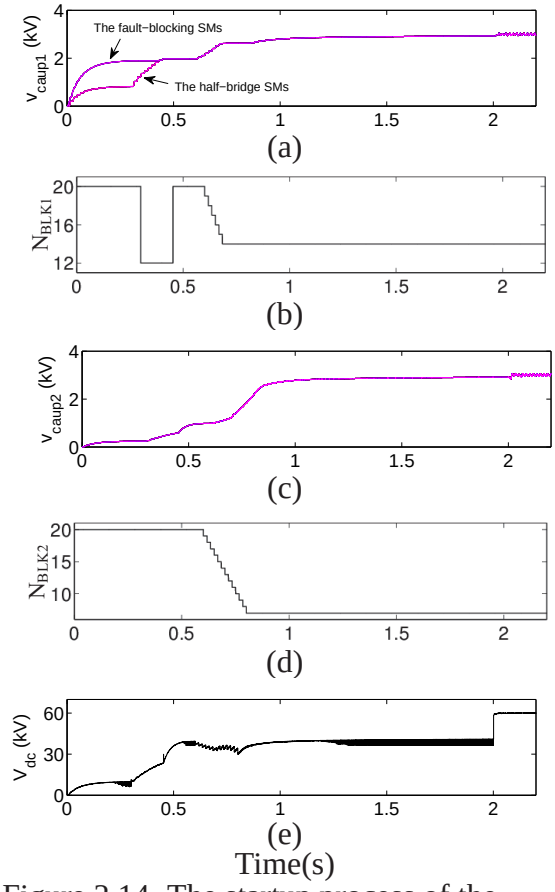


Figure 2.14. The startup process of the hybrid MMC-HVDC system with HB SMs (N_{HB} = 12) and UFB SMs (N_{UFB} = 8): (a), (b), (c), and (d) SM capacitor voltages and the commanded number of blocked SM capacitors of the phase-*a* upper arm of MMC-1 and MMC-2, and (e) dc-bus voltage.

are turned on and the SM capacitors of MMC-1 are charged to the new steady-state voltage $V_{C,\mathrm{MMC1}}^{\mathrm{ini}}$ = 2.1 kV around t = 0.8 s. At the same time, the steady-state dc-bus voltage rises up to $V_{\mathrm{dc}}^{\mathrm{II}}$ = V_{LL} = 42 kV, which charges the SMs in MMC-2 to the steady-state voltage $V_{C,\mathrm{MMC2}}^{\mathrm{ini}}$ = 1.1 kV around t = 0.8 s, as shown in Fig. 2.13 (c). After t = 0.8 s, the SMs in both MMCs are controllable and the current-limiting resistor is bypassed. The

number of blocked SM capacitors is being controlled from N_C to $N_{\mathrm{BLK}}^{\mathrm{ref}}$ to charge the SM capacitors to their nominal voltage, as shown in Fig. 2.13. For the UFB, 3LX, and 5LX SM-based MMC-HVDC systems, the startup process is similar to that of the FB-MMC-HVDC system.

In Fig. 2.14, the startup process of the hybrid MMC-HVDC system is shown, which consists of $N_{\mathrm{HB}} = 12$ HB and $N_{\mathrm{UFB}} = 8$ UFB SMs. At $t = 0.3$ s, the SMs in MMC-1 are precharged to the uncontrollable steady-state voltage $V_{C,\mathrm{HB}}^{\mathrm{I,SS}} = 0.96$ kV for the HB SMs and $V_{C,\mathrm{UFB}}^{\mathrm{I,SS}} = 1.9$ kV for the UFB SMs based on (2.13) and (2.14), while the uncontrollable steady-state voltage of the SMs in MMC-2 is $V_{C,\mathrm{MMC2}}^{\mathrm{I,SS}} = \dfrac{V_{\mathrm{dc}}^{\mathrm{I}}}{2N_C} = 0.29$ kV due to $V_{\mathrm{dc}}^{\mathrm{I}} = 11.5$ kV based on (2.21), as shown in Figs. 2.14 (a) and (e). From $t = 0.3$ s, all conducting switches of the SMs in MMC-1 are turned on and the number of blocked SM capacitors of MMC-1 is changed to $N_{\mathrm{BLK1}} = N_{\mathrm{HB}} = 12$ so that the SM capacitors of the HB and UFB SMs of MMC-1 are charged to the same steady-state voltage $V_{C,\mathrm{MMC1}}^{\mathrm{ini}} = 2.1$ kV, as shown in Figs. 2.14 (a) and (b). Once the capacitor voltages of the HB and UFB SMs in MMC-1 reach the same voltage 2.1 kV, $N_{\mathrm{BLK1}} = 20$. At the same time, $V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}} = 42$ kV and, consequently, $V_{C,\mathrm{MMC2}}^{\mathrm{ini}} = 1.1$ kV, as shown in Figs. 2.14 (c) and (e). Subsequent to $t = 0.6$ s, the current-limiting resistor is bypassed and the number of blocked SM capacitors is being changed from N_C to $N_{\mathrm{BLK}}^{\mathrm{ref}}$ to charge the SM capacitors to their nominal voltage.

Chapter 3

AN IMPROVED EQUIVALENT CIRCUIT MODEL OF MMC AND INFLUENCE ANALYSIS OF SIMULATION TIME STEP

In this chapter, an improved equivalent circuit is proposed for modeling and simulation of the MMCs based on various configurations and different operating conditions. Moreover, the simulation time step is comprehensively investigated by considering the sampling period of the industrial controller, capacitor voltage balancing strategies, errors of current and voltage level, and computational efficiency. The impacts of the simulation time step on simulation accuracy and efficiency will be analyzed and discussed.

3.1 Configurations and Operational Principles of the Proposed ECM

The proposed arm circuit and various SM circuit topologies are shown in Figs. 3.1 and 3.2, respectively. The operational principles of various SM circuits have been presented in [16]. The MMC's operating conditions mainly include precharing/startup process, normal operating condition, and fault condition. Under dc fault condition, the HB-MMC cannot block the fault currents fed from the ac grid. While the FBL SMs can block the fault currents. In addition, the MMC based on the FBL SMs can work as a STATCOM under dc fault conditions [50, 102].

3.1.1 Operational Principles of the Proposed Equivalent Arm Circuit

A The proposed generalized equivalent arm circuit

Under normal operating condition, the SM configurations of Fig. 3.2 can be equivalent to a single HB SM or combination of two individual HB SMs. The UFB SM has the same behavior as the HB SM, while the CD SM and 3LX SM are consisted of two series-

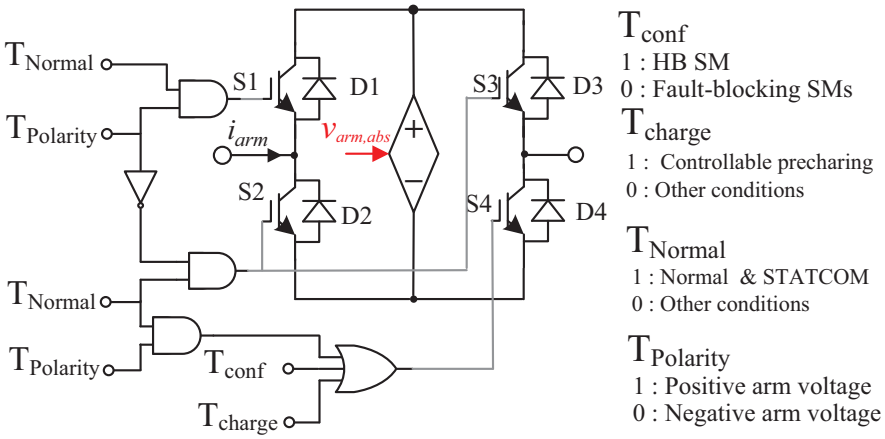


Figure 3.1. The proposed equivalent circuit of an arm.

connected HB SMs. The FB SM and 5LX SM have similar behaviors, which can generate bipolar voltage. Under blocked condition, the FBL SMs have the same behavior as the FB SM. Consequently, the FB circuit can be assumed as the generalized equivalent circuit.

B Switching states of the proposed equivalent arm circuit

The switching states of the proposed arm circuit of Fig. 3.1 depend on SM configurations and operating conditions, as listed in Table 3.1.

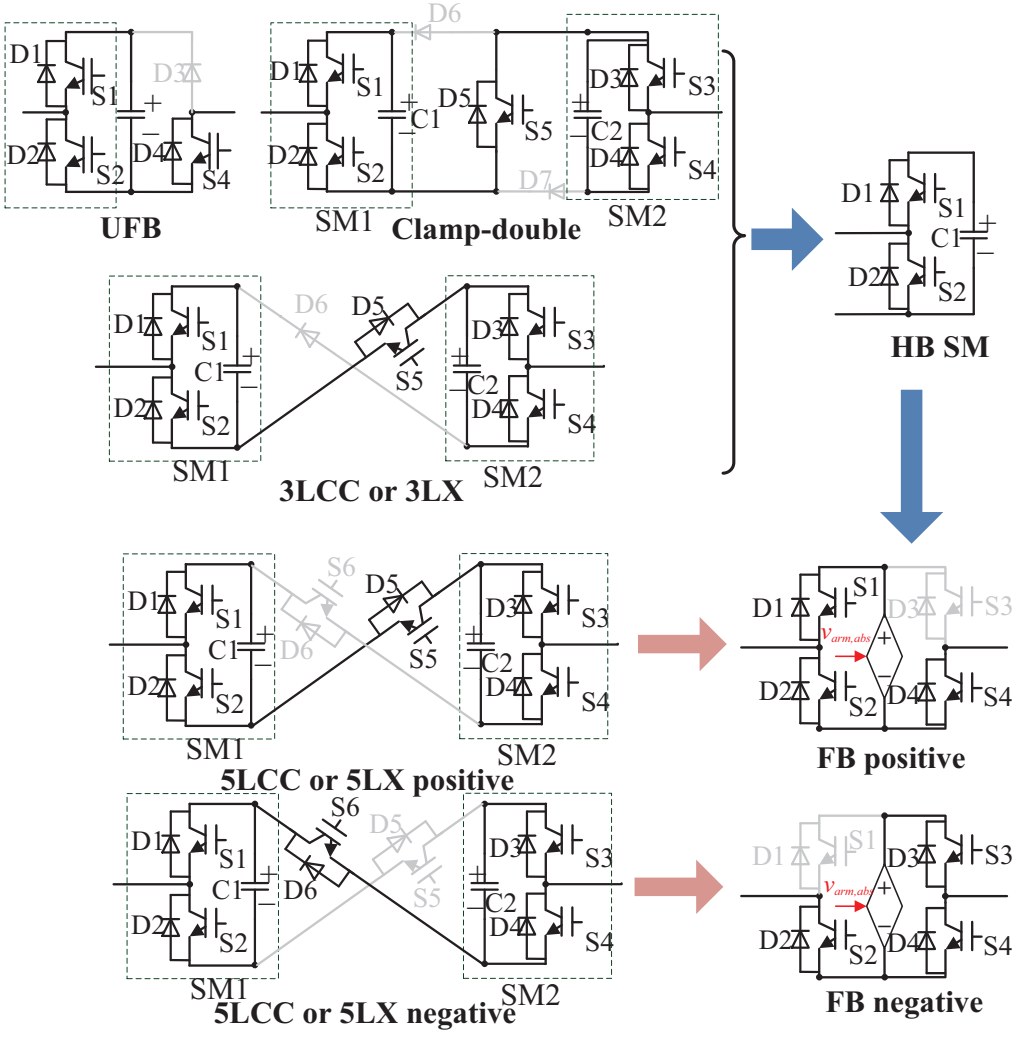


Figure 3.2. Various SM circuit topologies with fault-blocking capability.

Table 3.1

Switching States of the Proposed Equivalent Arm Circuit

SM configuration	**Operating conditions**		**Arm voltage polarity**	**S1**	**S2**	**S3**	**S4**
HB	**Precharging & DC fault**			0	0	0	1
$T_{\text{conf}} = 1$	**Normal** $T_{\text{Normal}} = 1$		positive	1	0	0	1
Fault-blocking $T_{\text{conf}} = 0$	**Precharging** $T_{\text{Normal}} = 0$	**Uncontrollable**		0	0	0	0
		Controllable		0	0	0	1
	Normal & Fault-STATCOM $T_{\text{Normal}} = 1$		positive	1	0	0	1
			negative	0	1	1	0
	Fault-blocking $T_{\text{Normal}} = 0$			0	0	0	0

The operating conditions include precharging, normal, fault-blocking, and fault-STATCOM conditions. For the HB-MMC, under normal operating condition, the S1 and S4 of Fig. 3.1 are turned on, i.e., $T_{\text{conf}} = 1$, $T_{\text{charge}} = 0$, $T_{\text{normal}} = 1$, and $T_{\text{polarity}} = 1$. Under other conditions, only S4 is turned on, i.e., $T_{\text{conf}} = 1$, $T_{\text{normal}} = 0$, and $T_{\text{polarity}} = 1$. For the MMCs based on the FBL SMs, the details are described as follows:

- Precharging condition: In [56, 103], the startup process can be divided into uncontrollable precharging stage and controllable precharging stage. Under uncontrollable precharging condition, $T_{\text{Normal}} = 0$. Under controllable precharging stage, the MMCs based on various SM circuits operate as the HB-MMC. Thus, the S4 should be turned on, and $T_{\text{charge}} = 1$.

- Normal and the fault-STATCOM conditions: $T_{\text{Normal}} = 1$ and $T_{\text{charge}} = 0$. The switching states of Fig. 3.1 are then determined by the arm voltage polarity, as listed in Table 3.1.

- Blocked conditions: The blocked conditions include the uncontrollable precharging condition and dc fault-blocking condition. Under these conditions, T_{Normal} and T_{charge} are set as 0.

After determining T_{conf}, T_{Normal} and T_{charge}, the switching states of Fig. 3.1 can be determined by the arm voltage polarity. For the MMCs based on the FBL SMs, under normal and fault-STATCOM conditions, the arm voltage can be positive and negative. To generate the positive voltage, the S1 and S4 are turned on, and $T_{\text{polarity}} = 1$. For the negative voltage, the S2 and S3 are turned on, and $T_{\text{polarity}} = 0$.

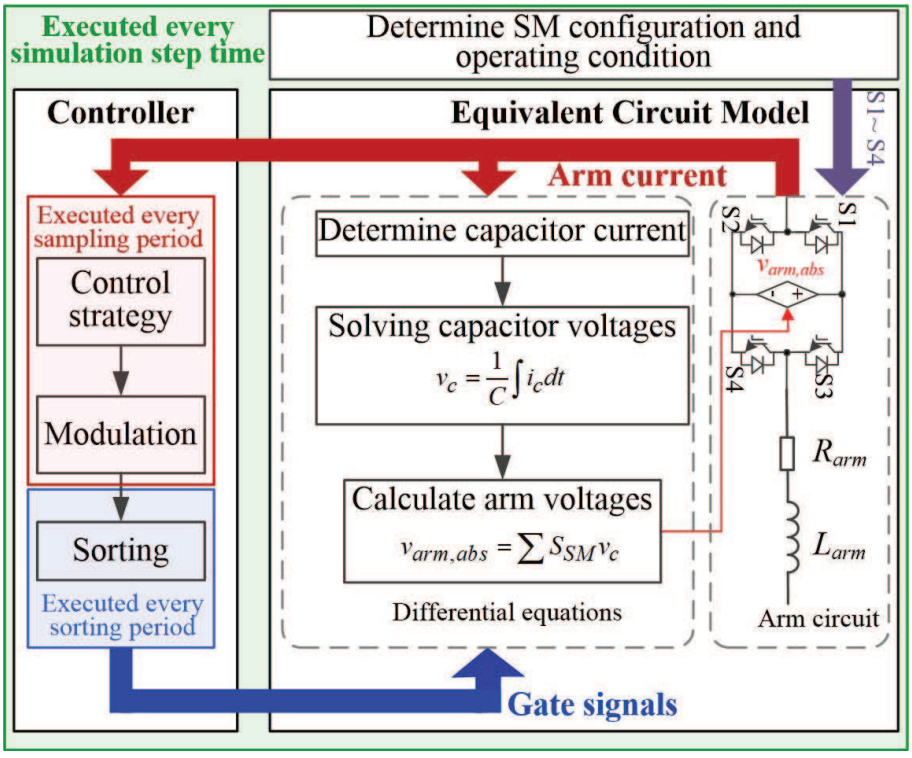


Figure 3.3. The MMC model with its controller based on the proposed equivalent arm circuit.

3.1.2 The Developed Detailed ECM

A Overview of the developed detailed ECM

Based on the proposed equivalent arm circuit, the detailed MMC model can be developed with considering an industrial controller, as shown in Fig. 3.3. When modeling the MMCs based on the proposed ECM, the simulation time step is set for the whole system. The control system can be divided into two parts: 1) the control strategy and modulation are executed every sampling (or control) period; 2) the capacitor voltage balancing algorithm (e.g., sorting) is executed every sorting period. The detailed steps are shown as follows:

- Step 1: Determination of simulation parameters: Firstly, the simulation parameters and MMC configurations should be determined. Based on these parameters, the switching states of Fig. 3.1 can be determined according to Section II(A).

- Step 2: Execution of control algorithms: In the detailed ECM, the controller performs the converter-level control algorithms, including capacitor voltage balancing, and reactive power control, and circulating current control. Then, it generates the gating signals to switch on/off the associated SMs.

- Step 3: Capacitor current calculation: The gating signals are used to derive the capacitor currents based on the arm current.

- Step 4: Capacitor voltage calculation: The capacitor voltages are derived based on the capacitor current and the differential equations.

- Step 5: Arm voltage calculation: The arm voltage (v_{arm}) is derived based on the gating signals and the capacitor voltages. The absolute value of arm voltage ($|v_{arm}|$) is the input of the controlled voltage source, as shown in Fig. 3.3.

B Capacitor current and voltage

The dynamics of each capacitor voltage is described by

$$i_{ci} = C\frac{dv_{ci}}{dt}, \tag{3.1}$$

where v_{ci} represents the capacitor voltage and i_{ci} refers to the capacitor current of the i^{th} SM.

The capacitor voltage at time t_k can be derived from (3.1), which is given by

$$v_{ci}(t_k) = v_{ci}(t_{k-1}) + \frac{1}{C}\int_{t_{k-1}}^{t_k} i_{ci}(\tau)d\tau. \tag{3.2}$$

The capacitor voltage can be solved by numerical methods. In this paper, the Simpson quadrature method is employed. To solve for the capacitor voltage, the capacitor current is required, which depends on the SM circuit, SM switching state (inserted or bypassed), and arm current.

For the HB SM, the capacitor current can be derived as follows:

- Blocked condition: When all switches of the HB SM are turned off, the capacitor current is determined by the direction of the arm current and given by

$$i_{\text{ci}} = \begin{cases} i_{\text{arm}}, & i_{\text{arm}} > 0, \\ 0, & i_{\text{arm}} < 0. \end{cases} \tag{3.3}$$

- Normal condition: i_{ci} depends on insertion and bypass of the SM, and can be expressed as

$$i_{\text{ci}} = S_{\text{HB}} i_{\text{arm}}, \tag{3.4}$$

where S_{SM} is the switching function of the HB SM and defined by

$$S_{\text{HB}} = \begin{cases} 1, & \text{inserted}, \\ 0, & \text{bypassed}. \end{cases} \tag{3.5}$$

For the FBL SMs, under normal operating conditions, they behave like the HB SM and i_{c} can be determined by (3.4), in which S_{SM} is their corresponding switching states. Under fault operating conditions, for the UFB, FB, 3LX, and 5LX SMs, when all switches are turned off, either positive or negative arm currents flow through the anti-parallel diodes to charge the capacitors, and $i_{\text{c}} = |i_{\text{arm}}|$.

For the CD SM, under blocked condition, when the arm current is positive, two HB SMs in the CD SM are connected in series. When the arm current is negative, two HB SMs are connected in parallel. Therefore, when the CD SM is blocked, the capacitor currents can be calculated by

$$i_{\text{c,1}} = i_{\text{c,2}} = \begin{cases} |i_{\text{arm}}|, & i_{\text{arm}} > 0, \\ 0.5\,|i_{\text{arm}}|, & i_{\text{arm}} < 0, \end{cases} \tag{3.6}$$

where $i_{\text{c,1}}$ and $i_{\text{c,2}}$ are the currents of two capacitors in the CD SM, respectively.

C Arm voltage

The voltage of the controllable voltage source ($v_{\text{arm,abs}}$) of Fig. 3.1 can be calculated based on the number of the inserted SM capacitors. The number of the inserted SM capaci-

tors is determined by SM circuits and switching states, arm current direction, and operating conditions.

- Normal operating condition: The UFB, 3LX, and 5LX SMs are equivalent to a single HB SM or two series-connected HB SMs. Then, the arm voltage is generally expresses as (3.7). The FB SM can be assumed as two parallel-connected HB SMs. The arm voltage is expresses as (3.8). $v_{\text{arm,abs}}$ is the input to the controllable voltage source, as shown in Fig. 3.4.

$$v_{\text{arm}} = \sum S_{\text{HBi}} v_{\text{ci}}, \tag{3.7}$$

$$v_{\text{arm}} = \sum \left(S_{\text{HBi1}} - S_{\text{HBi2}}\right) v_{\text{ci}}, \tag{3.8}$$

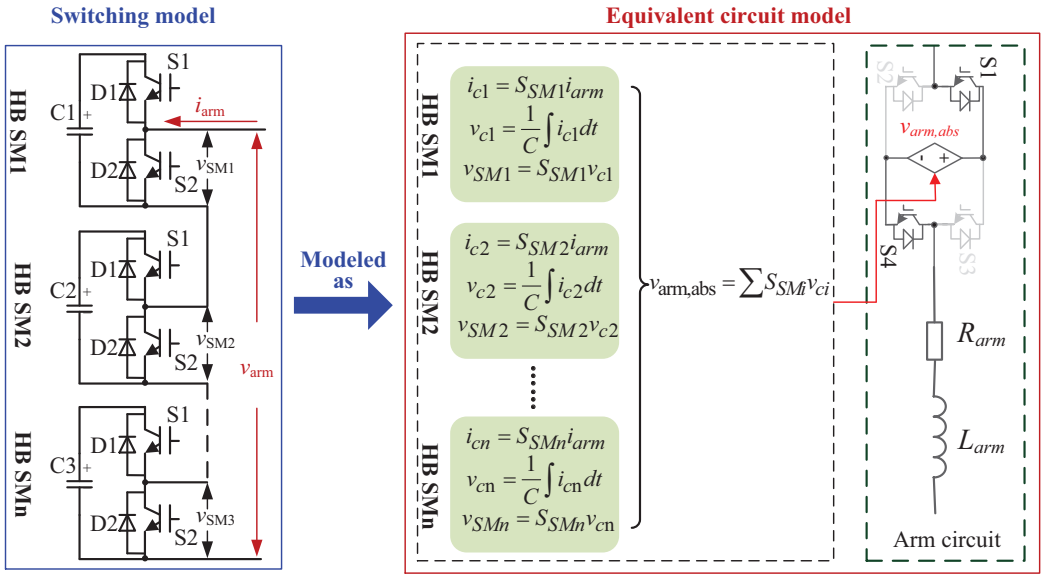
  where S_{HBi1} regulates the HB SM consisted of S1 and S2, while S_{HBi2} regulated the HB SM consisted of S3 and S4.

- Blocked conditions: For the HB-MMC, when the arm is positive, $v_{\text{arm}} = N_{\text{inserted}} v_{\text{ci}}$, where N_{inserted} is the number of capacitors in the blocked-state SMs per arm. Otherwise, the arm voltage is zero. For the fault-blocking MMCs, v_{arm} is the sum of the capacitor voltages in the blocked SMs regardless of the direction of the arm current, as shown in Fig. 3.5.

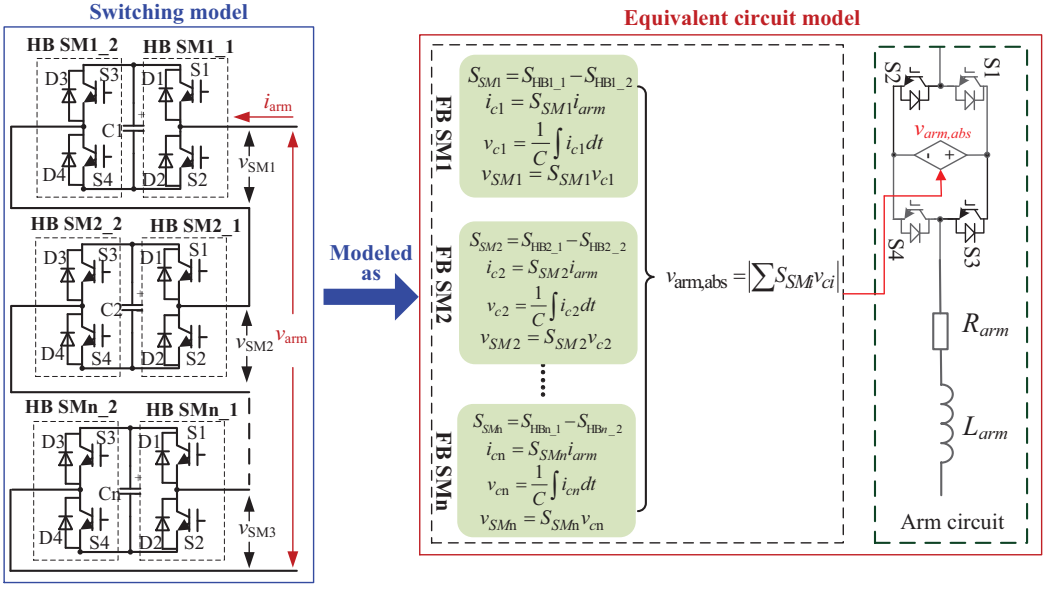
3.1.3 The Simplified ECM

To further improve the computational efficiency of the proposed ECM, the number of state variables (i.e., capacitor voltages) can be reduced. This simplified ECM assumes that all capacitor voltages are well balanced and only the average capacitor voltage of each arm is considered to calculate the arm voltage.

Under normal operating condition, as analyzed in [119], the average capacitor current is derived as



(a)

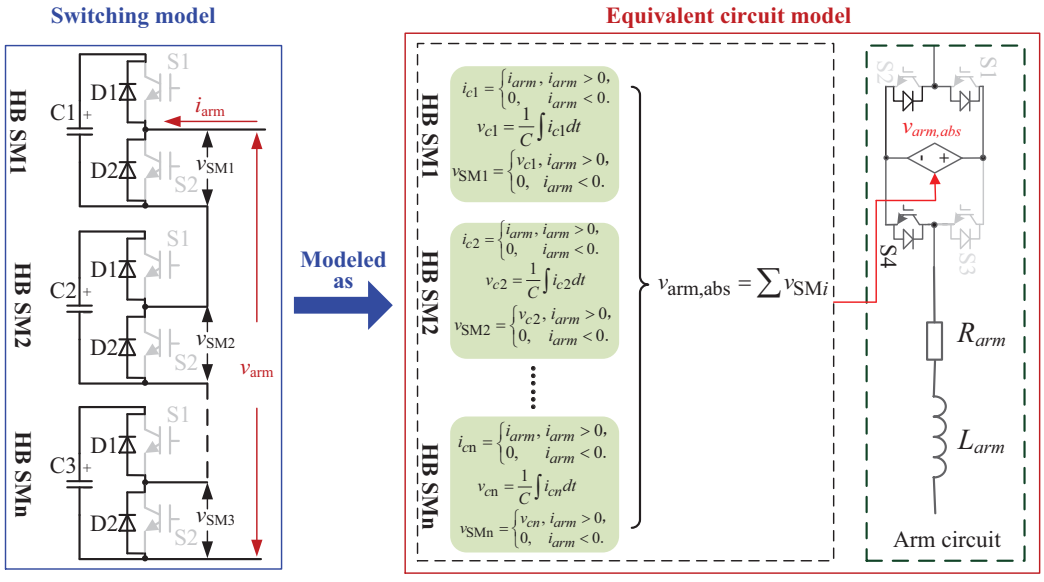


(b)

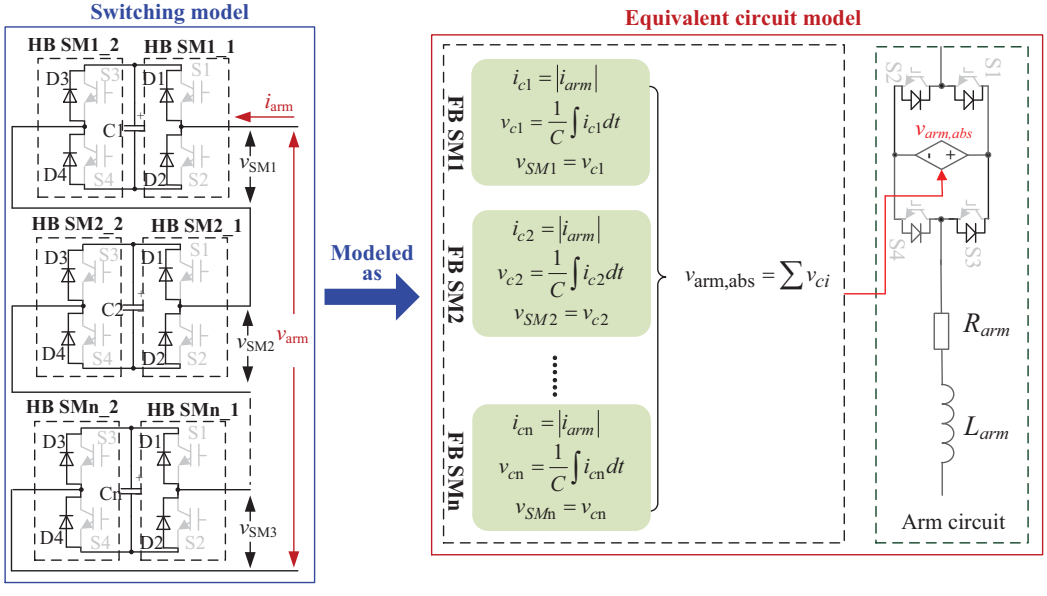
Figure 3.4. The schematic of (a) HB-MMC, and (b) FB-MMC under normal condition.

$$i_{c,avg} = \frac{1 + d_{arm}}{2} i_{arm}, \tag{3.9}$$

where d_{arm} is the modulation reference, which is derived from grid current controller and circulating current controller. The average capacitor voltage of an arm can be derived by



(a)



(b)

Figure 3.5. The schematic of (a) HB-MMC, and (b) FB-MMC under blocked condition.

(3.2) and (3.9). The arm voltage is determined by the number of the inserted SM capacitors, which is given by:

$$v_{\text{arm}} = N_{\text{insert}} v_{\text{c,avg}}, \tag{3.10}$$

where n_{insert} is the number of the inserted capacitors, and $v_{\text{c,avg}}$ is the average SM capacitor

voltage of an arm.

Under uncontrollable precharging and dc fault conditions, the capacitor currents of various SMs are still governed by (3.3) and (3.6). The arm voltage is determined by the SM circuit and number of capacitors. Under controllable precharging condition, the average capacitor voltage is determined by the equivalent capacitance per arm, which depends on the SM circuits and the number of the inserted capacitors and has been analyzed in [56].

Table 3.2

System Parameters of the MMC-HVDC System

Parameters	**Nominal Value**
Rated power	100 MW
DC link voltage	110 kV
AC grid line-to-line voltage	60 kV RMS
Number of SMs per arm, N_{SM}	20
Arm inductance	5 mH
Capacitance per SM	1000 μF
Rated capacitor voltage per SM	5 kV
DC line inductance	1 mH
DC line resistance	1 Ω
DC line capacitance	100 μF

3.2 Influence Analysis and Determination of Simulation Time Step

The proposed ECM can be used to evaluate the dynamic performance of the MMC with considering its industrial controller. However, the improperly selected simulation time step may lead to additional errors and low computational efficiency during simulation. Thus, the simulation time step t_{step} should be properly determined based on the sampling period or control period t_{sample}, capacitor voltage balancing period t_{sort}, and simulation accuracy and efficiency.

A point-to-point FB-MMC-HVDC system is selected as the study system and the sys-

tem parameters are listed in Table 3.2. Based on the DSM and proposed ECM technologies, the models of the MMC-HVDC system are built and compared in the PSCAD/EMTDC program environment. The simulation time step and sampling period of the DSM are set as 10 μs.

3.2.1 Influence of the Sampling Period

As shown in Fig. 3.6, the increased sampling period t_{sample} causes the increased time delay, loss of voltage level, and distortion in arm voltage, and consequently, leads to increased harmonics in arm current and dc current. The maximum sampling period has been investigated in [115, 124, 125], which is determined by the modulation index and the total number of SMs per arm, as expressed in (3.11).

$$t_{\text{sample}} = \frac{1}{\pi m f_0 N_{\text{SM}}}, \tag{3.11}$$

where m is the modulation index, f_0 is the fundamental frequency, and N_{SM} is the number of SMs per arm. When fixing the simulation time step at 10 μs, the modulated waveform is show in Fig. 3.7. The increased sampling period leads to increased distortion.

3.2.2 Influence Analysis of the Simulation Time Step

In [115, 124, 125], the sampling period equals to the simulation time step, which may not be proper when considering an industrial controller. The sampling period or controller

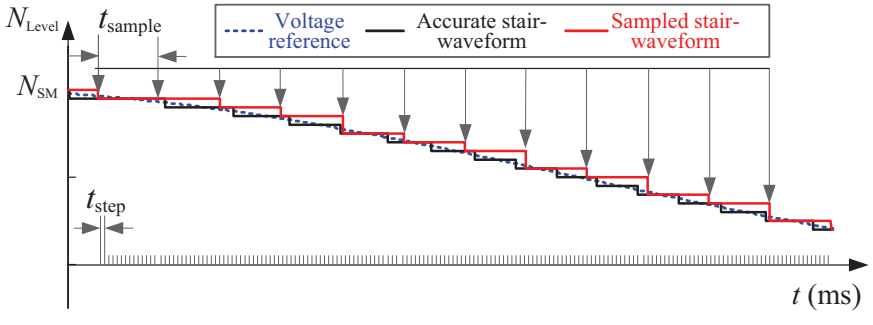


Figure 3.6. The voltage levels of the MMC with $t_{\text{sample}} = 200\mu s$.

period depends on the practical system specifications and limitations. When using the sampling period of the industrial controller for modeling and simulation, the simulation time step is flexible to choose. When fixing the sampling period, the increased simulation time step will lead to additional distortion. To ensure the system operating properly, the influence of the simulation time step should be investigated. When fixing the sampling period, the simulation time step should equal to or less than the sampling period, i.e.,

$$t_{\text{step}} \leq t_{\text{sample}}. \tag{3.12}$$

In this section, to investigate the influence of the simulation time step, t_{sample} is fixed at 100 μs based on (3.11).

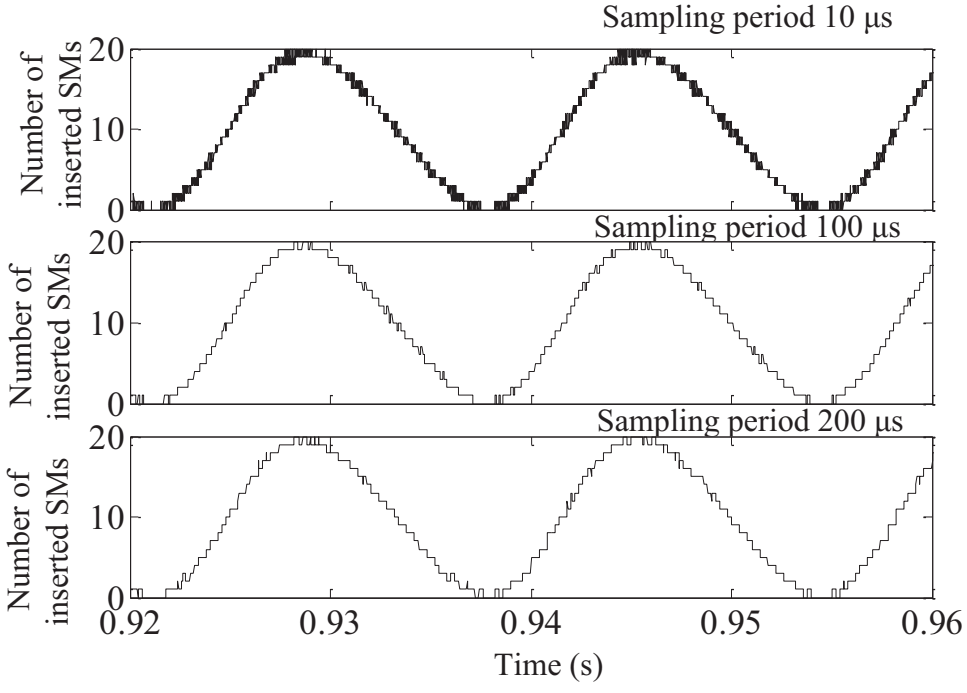


Figure 3.7. The modulated waveform when fixing the simulation time step at 10 μs.

A Influence of t_{step} on capacitor voltage balancing

Since the capacitor voltage balancing period t_{sort} will significantly affect the switching frequency of semiconductor devices and their power losses [97, 147]. To reduce power losses of the MMCs, the reduced switching-frequency balancing methods are preferred. Thus, the sorting period should be equal to or greater than the sampling period, i.e. [97, 147–150],

$$t_{sort} \geq t_{sample}. \tag{3.13}$$

For the given sampling period, if properly increasing the simulation time step, the performance of capacitor voltage balancing is not significantly affected, as shown in Fig. 3.8.

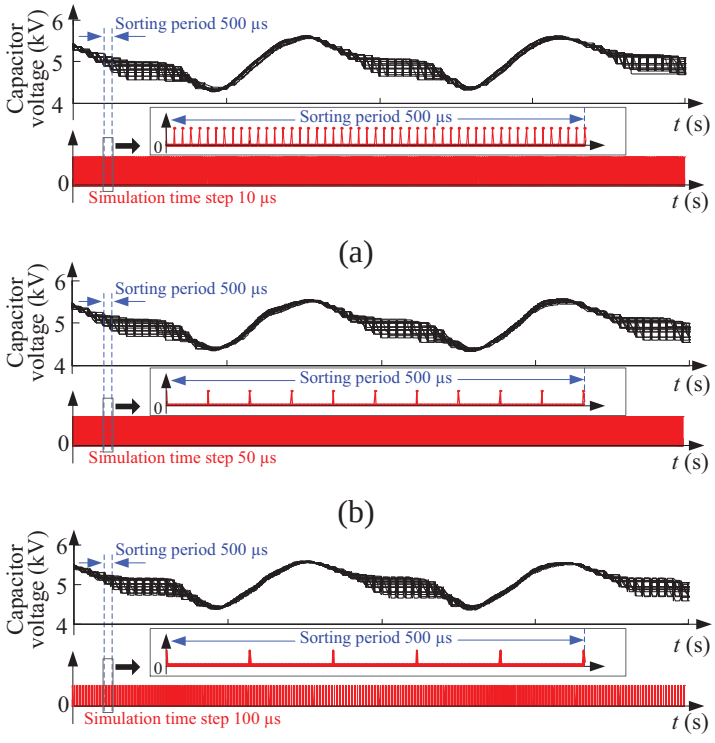


Figure 3.8. The capacitor voltages with $t_{sort} = 500\ \mu$s based on various simulation time steps: (a) $t_{step} = 10\ \mu$s, (b) $t_{step} = 50\ \mu$s, and (c) $t_{step} = 100\ \mu$s.

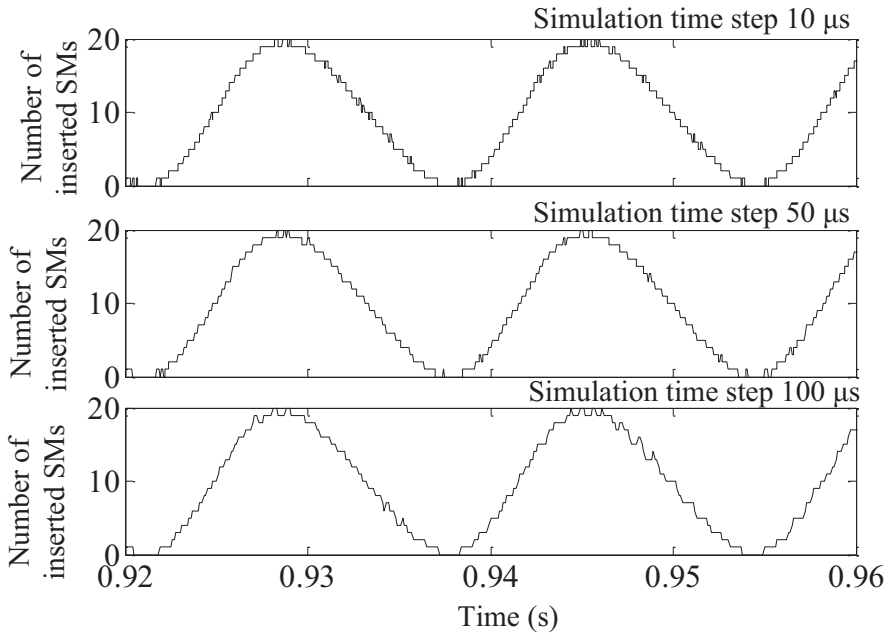


Figure 3.9. The modulated waveform when fixing the sampling period at 100 μs.

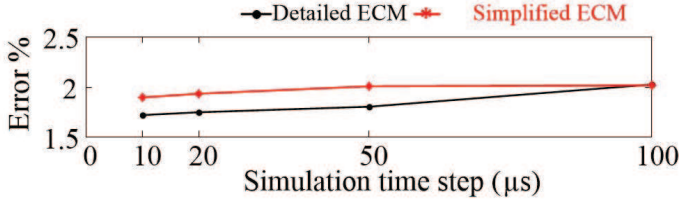


Figure 3.10. Errors of voltage level calculation for various simulation time steps.

B Influence of t_{step} on modulated arm voltage

As shown in Fig. 3.9, when fixing the sampling period at 100 μs, the increased simulation time step also leads to additional distortion. To evaluate simulation performance, the errors are calculated for arm and dc currents with various simulation time steps. The average error is calculated from *n*-point differences between the voltages and currents of the DSM and proposed ECMs, which is given by

$$e_{\text{ave}} = \frac{\sum_{i=1}^{n} |f_{\text{ECM}}(i) - f_{\text{DSM}}(i)|}{n \cdot max(f_{\text{DSM}})} \times 100, \tag{3.14}$$

where n is the number of the selected points, f_{DSM} and f_{ECM} denote the measured values of the DSM and ECMs, respectively. When the simulation time step is much smaller than

the sampling period, i.e., $t_{\text{step}} = 10\,\mu$s, the voltage levels can be precisely represented. However, when t_{step} increases, the lost voltage levels may lead to the increased errors in voltage level calculation, as shown in Fig. 3.10.

C Influence of t_{step} on arm current and dc current

When increasing the simulation time step, the lost voltage levels lead to increased pulse width of the arm inductor voltage, as shown in Fig. 3.11. Due to the increased simulation time step, the voltage of arm inductor has fewer switching actions than that of the DSM. Consequently, the increased simulation time step causes wider pulse of the inductor voltage, leading to the increased arm current ripple. In Fig. 3.11, V_{Lm} denotes the magnitude of the inductor voltage. The fast Fourier transform (FFT) spectrum of arm and dc voltages and currents are shown in Fig. 3.12 for various simulation time steps. The increased simulation time step introduces more low-order harmonics in arm and dc currents. This means that the equivalent switching frequency is reduced, and the distortion of arm voltage is increased. Based on Fig. 3.13, the increased simulation time step leads to the increased errors in arm current, while the dc current is slightly influenced.

In addition, based on the results shown in Fig. 3.12, more low-order harmonics are introduced by sorting algorithm. For the detailed ECM, since the gating signals are ultimately generated by the sorting algorithm, which increases arm current and voltage distortions. For the simplified ECM, the capacitor voltages are assumed to be well balanced, and the simulation results show lower distortions.

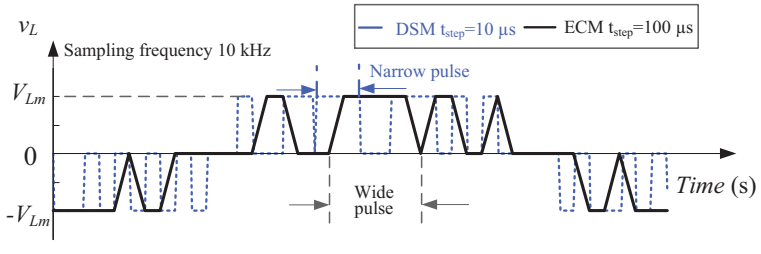


Figure 3.11. The arm inductor voltage.

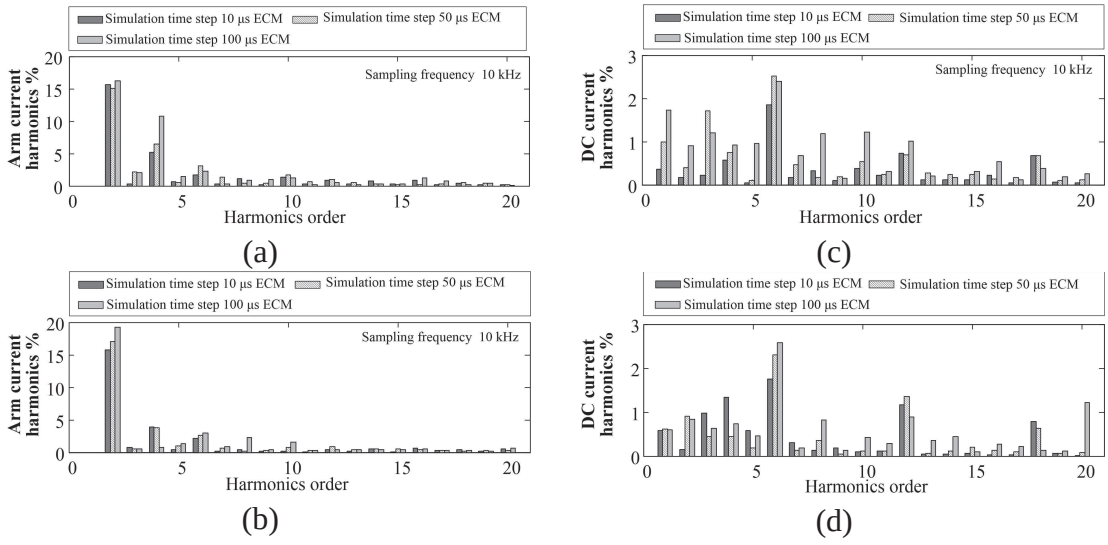


Figure 3.12. The FFT spectrum of (a) arm current of the detailed ECM, (b) arm current of the simplified ECM, (c) dc current of the detailed ECM, and (d) dc current of the simplified ECM.

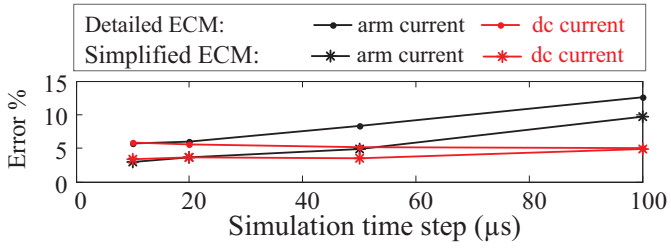


Figure 3.13. Average errors of arm current and dc current based on various simulation time steps.

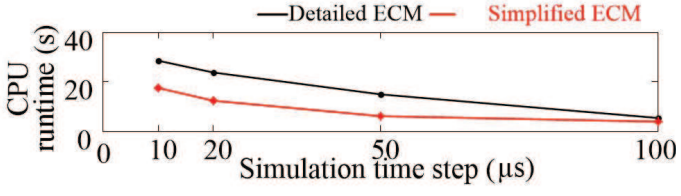


Figure 3.14. The total CPU runtime of the detailed ECM and simplified ECM based on various simulation time steps.

D Influence of t_{step} on performance evaluation of simulation efficiency

The system listed in Table 3.2 is used to evaluate the computational efficiency based on various simulation time steps. The sampling period and sorting period are fixed at 100 μs and the operating time is fixed at 1 s. Figure 3.14 shows the total CPU runtime of the detailed ECM and simplified ECM for various simulation time steps.

Based on the aforementioned analysis, the increased simulation time step leads to higher computational efficiency and lower accuracy. The selection of the simulation time step is a tradeoff between accuracy and computational efficiency. For the study system in this paper, the maximum simulation time step of the proposed ECM could be equal to the sampling period.

3.3 Performance Evaluation and Verification of the Proposed ECM

To verify and validate the proposed ECM, a point-to-point MMC-HVDC system is selected as the study system and built in the PSCAD/EMTDC program environment. The parameters are listed in Table 3.2. The simulation results of the proposed ECM are compared with those of the DSM for various SM configurations and operating conditions.

3.3.1 The Proposed Detailed ECM

An HB-MMC-HVDC system is modeled and simulated based on the DSM and the proposed detailed ECM, respectively. A dc fault occurs at 0.6 s and the HB-MMC cannot block the fault current fed from the ac grid. The waveforms of the phase-a arm currents, dc currents, and capacitor voltages are compared, which coincide and demonstrate the accuracy of the proposed ECM, as shown in Fig. 3.15.

The MMCs based on the FBL SMs, such as the FB, UFB, CD, 3LX, and 5LX SMs, have the similar behaviors under normal and fault operating conditions. Figure 3.16 shows the

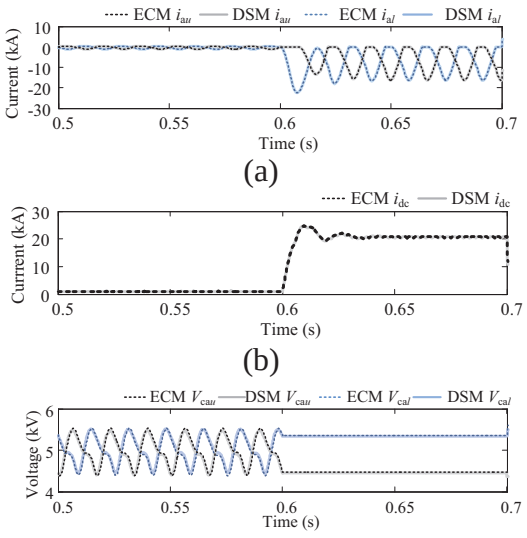


Figure 3.15. The simulation results of the HB-MMC-HVDC based on the DSM and the proposed detailed ECM with $t_{\text{step}} = 10$ μs: (a) arm currents, (b) dc currents, and (c) capacitor voltages.

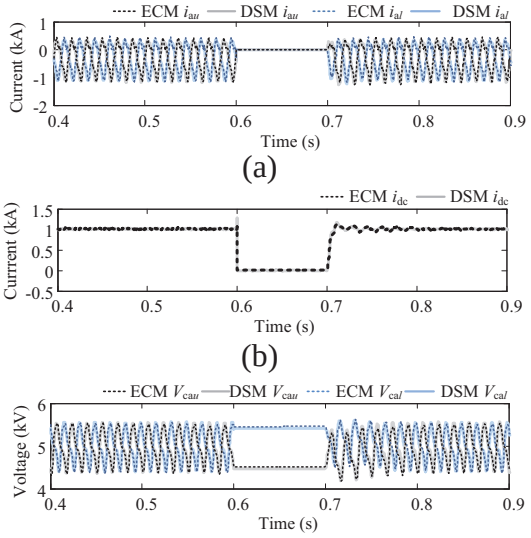


Figure 3.16. The simulation results of the FB-MMC-HVDC based on the DSM and the proposed detailed ECM with $t_{\text{step}} = 10$ μs: (a) arm currents, (b) dc currents, and (c) capacitor voltages.

phase-a arm currents, dc currents, and capacitor voltages of the FB-MMC-HVDC system modeled by the DSM and the proposed detailed ECM with $t_{\text{step}} = 10$ μs under various operating conditions. The simulation results demonstrate the effectiveness of the proposed ECM for various operating conditions. Figure 3.17 shows the dc current and capacitor voltages with $t_{\text{step}} = 100$ μs. Based on Figures 3.16 (b) and 3.17 (a), the larger simulation time step leads to the increased dc current ripple.

Under dc-fault condition, the MMCs based on the FBL SMs can operate in the STATCOM mode to produce reactive power. The simulation results of the FB-MMC operating in the STATCOM mode are shown in Fig. 3.18.

3.3.2 The Proposed Simplified ECM

The simplified ECM has better efficiency by considering the average capacitor voltage and neglecting the dynamics of each capacitor voltage.

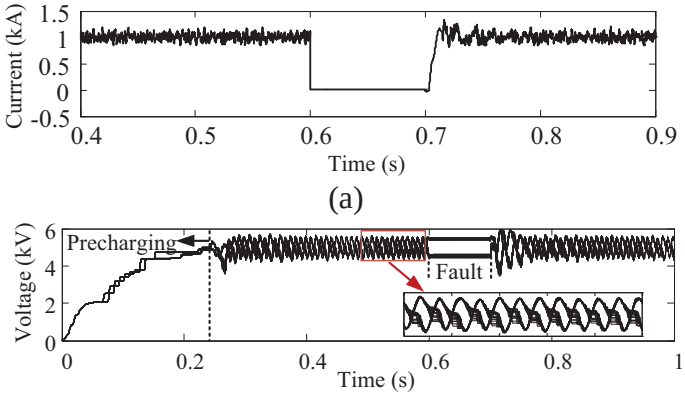


Figure 3.17. The simulation results of FB-MMC based on ECM with t_{step} = 100 μs: (a) dc current, and (b) capacitor voltages.

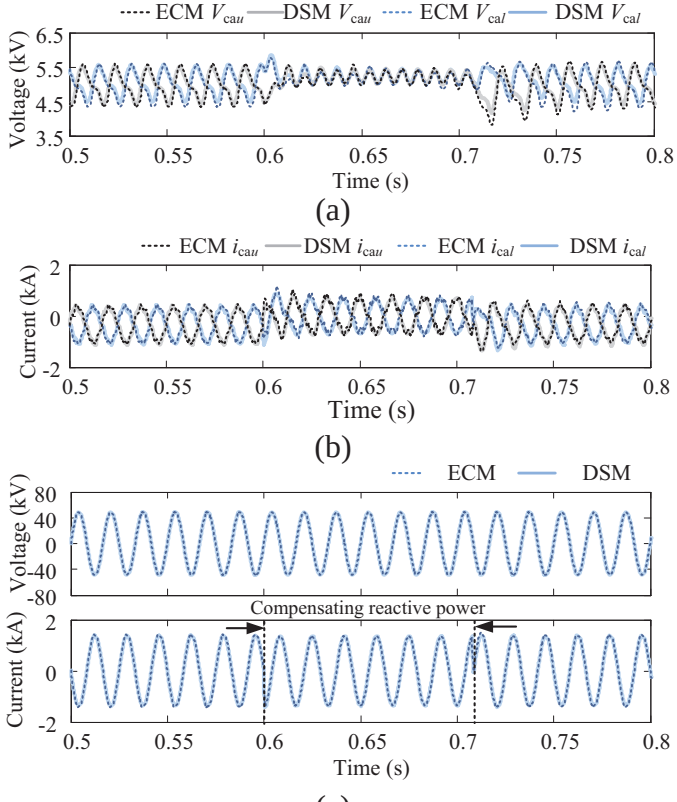


Figure 3.18. The simulation results of the FB-MMC in the STATCOM mode with t_{step} = 10 μs: (a) capacitor voltages, (b) phase-a arm currents, and (c) ac-side phase current and voltage.

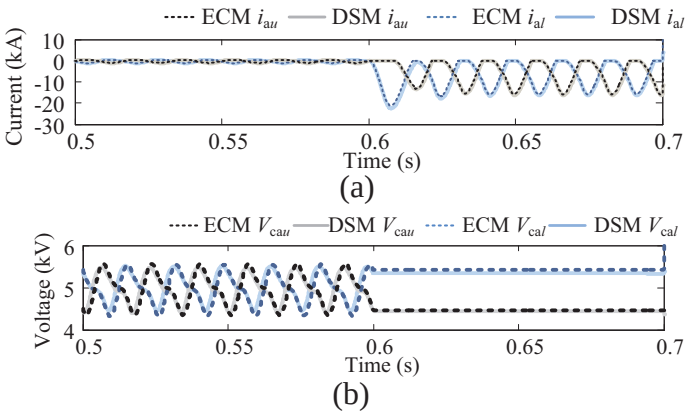


Figure 3.19. The simulation results of MMC1 of the HB-MMC-HVDC based on the DSM and proposed simplified ECM with t_{step} = 10 μs: (a) arm currents, and (b) capacitor voltages.

The phase-a arm currents and capacitor voltages of the HB-MMC-HVDC system based on the simplified ECM and DSM are compared and shown in Fig. 3.19. For the FB-MMC-HVDC, the arm currents and capacitor voltages under various operating conditions are shown in Fig. 3.20. Figure 3.21 shows the STATCOM operation of the FB-MMC during a dc fault. Figure 3.22 shows the dc current and capacitor voltages with t_{step} = 100 μs. Based on the simulation results, the voltage and current waveforms coincide and the proposed simplified ECM is applicable to various MMC configurations and different operating conditions.

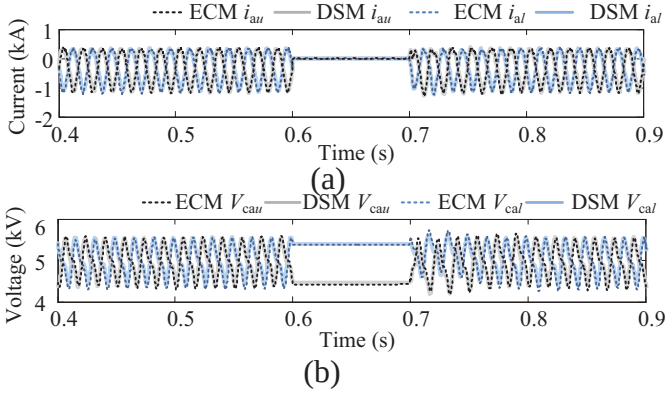


Figure 3.20. The simulation results of MMC1 of the FB-MMC-HVDC based on the DSM and proposed simplified ECM with t_{step} = 10 μs: (a) arm currents, and (v) capacitor voltages.

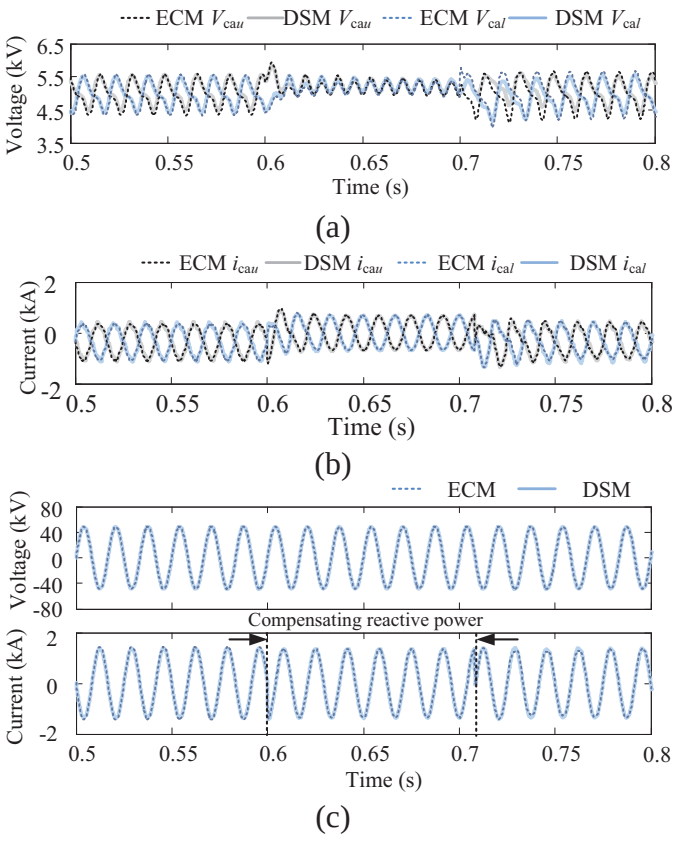


Figure 3.21. The simulation results of the FB-MMC in the STATCOM mode based on the simplified ECM with $t_{\text{step}} = 10\ \mu$s: (a) capacitor voltages, (b) phase-a arm currents, and (c) ac-side phase current and voltage.

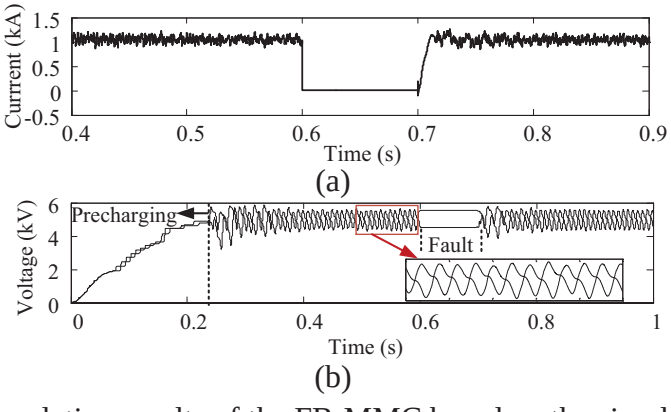


Figure 3.22. The simulation results of the FB-MMC based on the simplified ECM with $t_{\text{step}} = 100\ \mu$s: (a) dc current, and (b) capacitor voltages.

Table 3.3
Comparison of Simulation Runtime for Various MMC-HVDC Systems Based on the DSM and the Proposed ECM.

Simulation settings Simulation time step = 10 μs ; System operating time = 1 s.			
MMC configuration	**DSM runtime (s)**	**ECM runtime (s)**	
		Detailed	**Simplified**
HB	1656.21	30.67	11.52
FB	8512.72	31.34	11.73
CD	21877.39	30.31	12.38
3LX	29097.14	30.84	12.21
hybrid (HB and FB)	3179.83	30.56	11.94

3.3.3 Computational Efficiency

A The MMC-HVDC systems based on various SM circuits

To evaluate the efficiency of the proposed ECM, the simulation runtime for various MMC-HVDC systems based on the DSM, detailed ECM, and simplified ECM is listed in Table 3.3. The system operating time is 1 s and the simulation time step is 10 μs. The simulation is conducted on the operating system of Microsoft Windows 10 with a 2.60 GHz Intel Core i7-6700HQ CPU and 8 GB of RAM.

As shown in Table 3.3, the proposed ECM can significantly improve the computational efficiency as compared with the conventional DSM while keeping high accuracy. The increasing complexity of SM circuit topologies will severely reduce the simulation efficiency of the conventional DSM. However, the simulation efficiency of the proposed ECM is almost not affected by the complexity of SM circuit topologies.

Table 3.4
Comparison of Simulation Runtime of the MMC-HVDC Systems with Various Voltage Levels.

Simulation settings Simulation time step = 10 μs, System operating time = 1 s.		
Number of SMs per arm	**ECM runtime (s)**	
	Detailed	**Simplified**
20	31.34	11.73
40	37.11	12.03
60	43.89	12.45
80	47.80	12.71
100	54.62	13.12
200	96.56	16.29

B The high-level MMC-HVDC systems

Table 3.4 shows the simulation runtime for the MMC-HVDC systems with various voltage levels. As the increasing of the number of SMs, although the simulation runtime of the proposed ECM increases, it still much smaller than that of the conventional DSM.

3.4 Conclusion

In this chapter, a generalized ECM is proposed for modeling and simulating the MMCs based on various SM circuits under different operating conditions. The proposed detailed ECM considers internal state variables and can be used to evaluate the dynamic performance of an MMC with considering a practical industrial controller. To further improve simulation efficiency, the simplified ECM is derived by neglecting the dynamics of individual capacitor voltage. The study results show that the selection of the simulation time step influences simulation efficiency and accuracy. For the given study system, the maximum simulation time step could be equal to the sampling period (or control period) of

the practical controller for highest simulation efficiency while keeping good accuracy. The study results also show that the complexity of SM circuit topologies significantly affects the simulation efficiency of the conventional DSM. However, the proposed ECM can keep the same high-efficiency simulation for various SM circuits regardless of the complexity of SM circuit topologies.

Chapter 4

OPERATIONAL PRINCIPLES AND MATHEMATICAL MODEL OF MODULAR MULTILEVEL CONVERTER-BASED SOLID-STATE TRANSFORMER

To model the MMC-based SST, the operational principles of IM2DC are analyzed in this chapter. The IM2DC has similar operational principles with the DAB converter. The difference is that the MMC can generate a controllable multilevel voltage waveform.

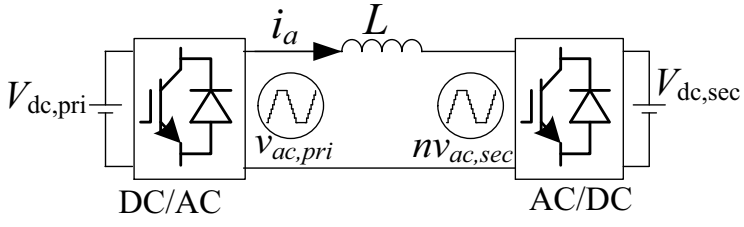


Figure 4.1. The equivalent circuit of IM2DC.

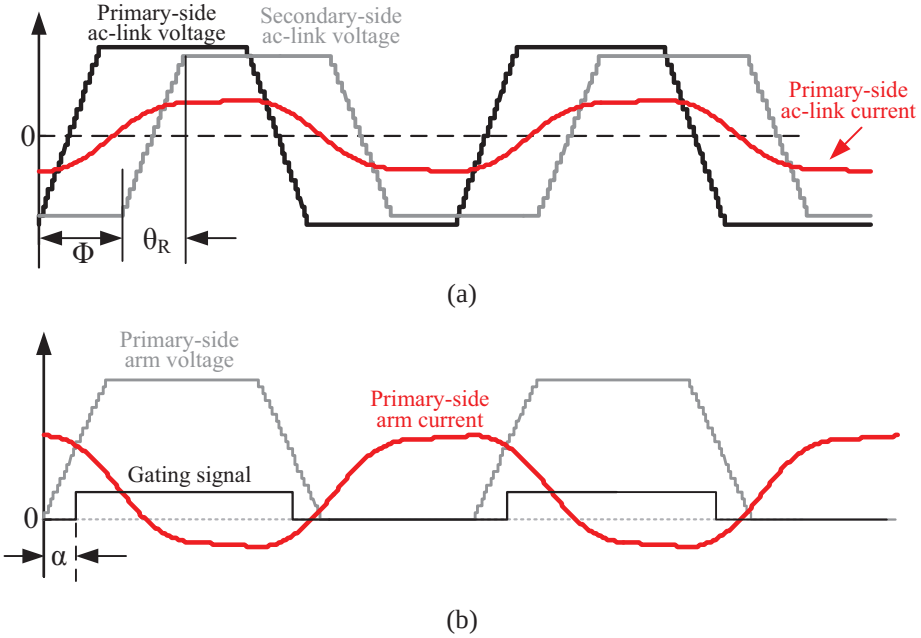


Figure 4.2. Theoretical waveforms of (a) primary-side and secondary-side ac-link voltages, and primary-side ac-link current, and (b) arm voltage, arm current, and SM gating signal.

Similar to the DAB converter, the IM2DC can be equivalent to a circuit shown in Fig.

4.1. The ac-link currents and the transmitted power of the IM2DC are determined by the phase-shift angle (Φ) between the primary- and secondary-side ac-link voltages. When the secondary-side ac-link voltage $v_{\mathrm{ac,sec}}$ lagging the primary-side ac-link voltage by Φ ($\Phi > 0$), the power flows from the primary side to the secondary side. When the secondary-side ac-link voltage $v_{\mathrm{ac,sec}}$ leading the primary-side ac-link voltage by Φ ($\Phi < 0$), the power flows from the secondary side to the primary side. The phase-shift angle should be less than $\pi/2$ ($|\Phi| \leqslant \pi/2$). The arbitrary ac-link voltages and current, as well as arm voltage and current are shown in Fig. 4.2.

4.1 Mathematical Model of Isolated Modular Multilevel DC-DC Converter

4.1.1 Arm Currents

The arm current can be derived from voltage drop on arm inductor. In this way, the arm currents are expressed in (4.1).

$$\begin{cases} R_{\mathrm{arm}} i_{xu} + L_{\mathrm{arm}} \dfrac{\mathrm{d}i_{xu}}{\mathrm{d}t} &= \dfrac{V_{\mathrm{dc}}}{2} - v_{xu} - v_x, \\ R_{\mathrm{arm}} i_{xl} + L_{\mathrm{arm}} \dfrac{\mathrm{d}i_{xl}}{\mathrm{d}t} &= \dfrac{V_{\mathrm{dc}}}{2} - v_{xl} + v_x, \end{cases} \tag{4.1}$$

where the subscript x represents phase-leg a, b, c and d. When $\{x = a, b\}$, the R_{arm} and L_{arm} represent resistance and inductance of primary-side arm inductor ($R_{\mathrm{arm,pri}}$ and $L_{\mathrm{arm,pri}}$). When $\{x = c, d\}$, the R_{arm} and L_{arm} represent resistance and inductance of secondary-side arm inductor ($R_{\mathrm{arm,sec}}$ and $L_{\mathrm{arm,sec}}$). Similarly, when $\{x = a, b\}$, the V_{dc} represents primary-side dc-link voltage ($V_{\mathrm{dc,pri}}$). When $\{x = c, d\}$, the V_{dc} represents secondary-side dc-link voltage ($V_{\mathrm{dc,sec}}$).

4.1.2 AC-Link and DC-Link Currents

Based on the basic operational principles of MMC, the upper- and lower-arm currents are expressed as (4.2), which contain a circulating current and equally share ac-side current.

$$\begin{cases} i_{xu} &= \dfrac{i_x}{2} + i_{zx}, \\ i_{xl} &= -\dfrac{i_x}{2} + i_{zx}. \end{cases} \tag{4.2}$$

When substitute (4.2) into (4.1), the dynamic performances of ac-link current and circulating current can be expressed as:

$$\begin{cases} R_{\text{arm}} i_x + L_{\text{arm}} \dfrac{\mathrm{d}i_x}{\mathrm{d}t} &= (v_{xl} - v_{xu}) - 2v_x, \\ R_{\text{arm}} i_{zx} + L_{\text{arm}} \dfrac{\mathrm{d}i_{zx}}{\mathrm{d}t} &= \dfrac{V_{\text{dc}} - v_{xu} - v_{xl}}{2}, \end{cases} \tag{4.3}$$

The primary- and secondary-side dc-link currents are derived from corresponding circulating currents, as expressed in (4.4), while (4.5) expressed the relationship between arm voltages and ac-link current.

$$\begin{cases} i_{\text{dc,pri}} &= i_{za} + i_{zb}, \\ i_{\text{dc,sec}} &= i_{zc} + i_{zd}. \end{cases} \tag{4.4}$$

$$\begin{aligned} &\frac{[(v_{al}-v_{au})-(v_{bl}-v_{bu})] - n_T\,[(v_{cl}-v_{cu})-(v_{dl}-v_{du})]}{2} \\ &= (R_T + R_{\text{arm,pri}} + n_T^2 R_{\text{arm,sec}}) i_a + (L_T + L_{\text{arm,pri}} + n_T^2 L_{\text{arm,sec}}) \frac{\mathrm{d}i_a}{\mathrm{d}t}, \end{aligned} \tag{4.5}$$

where R_{T} and L_{T} denote the winding resistance and leakage inductance of ac-link transformer.

4.1.3 Capacitor Voltage and Arm Voltage

Based on the above analysis, the arm currents, ac-link current, and dc-link current are regulated by arm voltages. The arm voltage is determined by voltages of inserted capacitors. In this way, to determine arm voltage, the capacitor voltage should be derived from arm current, as expressed in (4.6). The S_{SMi} represents the switching function of the i^{th} SM, which is defined in (4.7). Finally, the arm voltage is the capacitor voltages of on-state SMs.

$$\begin{cases} i_{\mathrm{ci}} = i_{\mathrm{arm}} S_{\mathrm{SMi}}, \\ v_{\mathrm{ci}} = \frac{1}{C} \int i_{\mathrm{ci}} \mathrm{d}t. \end{cases} \tag{4.6}$$

$$S_{\mathrm{SMi}} = \begin{cases} 1, & \text{inserted}, \\ 0, & \text{bypassed}. \end{cases} \tag{4.7}$$

$$v_{\mathrm{arm}} = \sum_{i=1}^{N_{\mathrm{SM}}} v_{\mathrm{ci}} S_{\mathrm{SMi}}, \tag{4.8}$$

where v_{SMi} are the switching function and capacitor voltage of the i^{th} SM in an arm, respectively.

4.1.4 Implementation of Simulation System Based on Mathematical Model

Compared with circuit-based simulation models, such as detailed switching model and equivalent circuit model mentioned in Chapter 2, the mathematical model or equation-based models are more suitable for optimal design of converters and controllers. Because the circuit parameters and controller parameters can be swept without frequently stop simulation and manually setting parameters.

To implement a simulation system of the MMC-based SST based on mathematical model, a flowchart is shown in Fig. 4.3. Firstly, the system parameters, circuit parameters, and simulation parameters are set for simulation model. Then, all variables are initialized. This is considered as the first iteration of simulation. After that, the switching sequences and gating signals are determined by voltage-balancing algorithms and modulation methods. The arm voltages are derived from switching functions and capacitor voltages, as expressed in (4.8).

The derived arm voltages are substituted into (4.5) and (4.10) to solve ac-link current

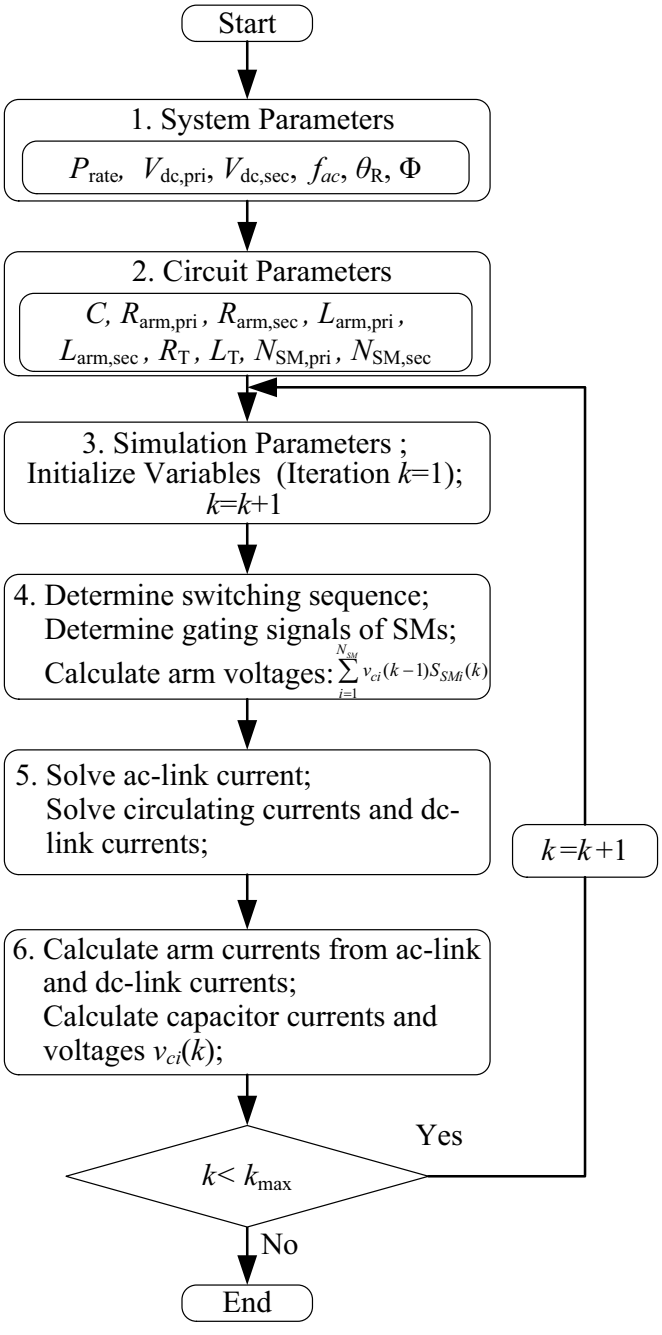


Figure 4.3. The flowchart of implementing mathematical model of MMC-based SST.

and circulating currents. Then, the dc-link current is derived from circulating currents.

$$i_a(k) = \frac{[v_{al}(k) - v_{au}(k) - v_{bl}(k) + v_{bu}(k)] - n_T\,[v_{cl}(k) - v_{cu}(k) - v_{dl}(k) + v_{du}(k)]}{2\left[(R_T + R_{arm,pri} + n_T^2 R_{arm,sec})T_s + (L_T + L_{arm,pri} + n_T^2 L_{arm,sec})\right]} T_s + \frac{(L_T + L_{arm,pri} + n_T^2 L_{arm,sec})}{(R_T + R_{arm,pri} + n_T^2 R_{arm,sec})T_s + (L_T + L_{arm,pri} + n_T^2 L_{arm,sec})} i_a(k-1), \tag{4.9}$$

where k represents the k^{th} simulation step.

$$i_{zx}(k) = \frac{L_{\text{arm}}}{R_{\text{arm}}T_s + L_{\text{arm}}} i_{zx}(k-1) + \frac{V_{\text{dc}} - v_{xu}(k) - v_{xl}(k)}{2\left[R_{\text{arm}}T_s + L_{\text{arm}}\right]} T_s. \tag{4.10}$$

Then, the arm currents are derived from ac-link current and circulating currents based on (4.2), and the capacitor currents and voltages are updated according to (4.6). To be clearer, a pseudo code of implementing MMC-based SST appears in Table 4.1.

Table 4.1

Pseudo Code of Implementing MMC-Based SST Based on Mathematical Model

Set System Parameters: P_{rate}, $V_{\text{dc,pri}}$, $V_{\text{dc,sec}}$, f_{ac}, θ_{R}, Φ;
Set Circuit Parameters: C, R_{arm}, L_{arm}, R_{T}, L_{T}, N_{SM};
Set Simulation parameters: number of simulation steps k_{max}, simulation time step;
Initialize Variables: phase currents, arm currents, dc-link currents, arm voltages, capacitor voltages, gating signals;
FOR k = 2 to k_{max}
  Voltage Balancing
  [$\text{ID}_{xu}(k)$]=Voltage balancing (Sorting options, $v_{c,xu}(k-1)$);
  % ID_{xu} is a vector containing index of SMs in phase-x upper arm
  [$\text{ID}_{xl}(k)$]=Voltage balancing (Sorting options, $v_{c,xl}(k-1)$);
  % ID_{xl} is a vector containing index of SMs in phase-x lower arm
  Modulation
  [$\text{S}_{xu}(k)$, $\text{V}_{xu}(k)$]=Modulation (Modulation options, $v_{c,xu}(k-1)$);
  % S_{xu} is a vector containing gating signals of SMs in phase-x upper arm
  [$\text{S}_{xl}(k)$, $\text{V}_{xl}(k)$]=Modulation (Modulation options, $v_{c,xl}(k-1)$);
  % S_{xl} is a vector containing gating signals index of SMs in phase-x lower arm
  Solve ac-link current and phase currents
  [$i_a(k)$]=Solve ac-link current($V_{au}(k)\sim V_{du}(k)$, $V_{al}(k)\sim V_{dl}(k)$, $i_a(k-1)$,
    R_{T}, L_{T}, n_{T}, R_{arm}, L_{arm}, T_s); % T_s is simulation time step
  $i_b(k) = -i_a(k)$, $i_c(k) = -n_{\text{T}} i_a(k)$, $i_d(k) = -n_{\text{T}} i_b(k)$;
  Solve circulating currents
  [$i_{zx}(k)$]=Solve circulating current($V_{\text{arm},xu}(k)$, $V_{\text{arm},xl}(k)$, $i_{zx}(k-1)$, R_{arm}, L_{arm}, T_s);
  Solve arm currents $i_{xu}(k) = 0.5i_x(k) + 0.5i_{zx}(k)$, $i_{xl}(k) = -0.5i_x(k) + 0.5i_{zx}(k)$;
  Update capacitor voltages
  [$v_{c,xu}(k)$]=Solve Capacitor Voltage(C, $i_{xu}(k)$, $i_{xu}(k-1)$, $\text{S}_{xu}(k)$, T_s);
  % $v_{c,xu}$ is a vector containing SM capacitor voltages of phase-x upper arm
  [$v_{c,xl}(k)$]=Solve Capacitor Voltage(C, $i_{xl}(k)$, $i_{xl}(k-1)$, $\text{S}_{xl}(k)$, T_s);
  % $v_{c,xl}$ is a vector containing SM capacitor voltages of phase-x lower arm
ENDFOR

4.2 Modified Mathematical Model Considering Parameter Design of MMC-Based SST

To implement the above detailed mathematical model, all circuit parameters should be provided in advance. However, for optimal design purpose, some circuit parameters, such as SM capacitance, arm inductance, and leakage inductance of ac-link transformer, should be determined based on system requirements. Thus, the mathematical model should be modified for the optimal design of the MMC-based SST.

4.2.1 Total Inductance of MMC-Based SST

The ac-link voltages can be expressed as piecewise-linear equations (4.11) and (4.12) based on the given system parameters, including rated power (P_{rate}), nominal dc-link voltages ($V_{\text{dc,pri}}$ and $V_{\text{dc,sec}}$), frequency of ac-link voltage (f_{ac}), phase-shift angle between primary-side and secondary-side ac-link voltages (Φ), and ramping angle of ac-link voltage (θ_R). In this section, the θ_R is assumed to be $0 \leqslant \theta_R \leqslant |\Phi| \leqslant \frac{\pi}{2}$. For other conditions and more detailed derivations are shown in Appendix 7.2.

$$v_{\text{ac,pri}}(\varphi) \approx \frac{(v_{al}-v_{au})-(v_{bl}-v_{bu})}{2} = \begin{cases} \dfrac{2V_{\text{dc,pri}}}{\theta_{\text{R}}}\varphi - V_{\text{dc,pri}}, & 0 < \varphi < \theta_{\text{R}}, \\ V_{\text{dc,pri}}, & \theta_{\text{R}} < \varphi < \pi, \\ -v_{\text{ac,pri}}(\varphi - \pi), & \pi < \varphi < 2\pi. \end{cases} \tag{4.11}$$

$$v_{\text{ac,sec}}(\varphi)' = n_T v_{\text{ac,sec}}(\varphi) \approx \frac{n_T\left[(v_{cl}-v_{cu})-(v_{dl}-v_{du})\right]}{2} = \frac{n_T V_{\text{dc,sec}}}{V_{\text{dc,pri}}} v_{\text{ac,pri}}(\varphi - \Phi), \tag{4.12}$$

where $v_{\text{ac,sec}}(\varphi)'$ is the reflected secondary-side voltage.

When ignoring winding resistances of arm inductor and ac-link transformer, the ac-link current is derived from ac-link voltages based on (4.5). The primary-side ac-link current (i_{a}) can be expressed as (4.13) when $\Phi > 0$ and (4.14) when $\Phi < 0$, respectively.

Then, the dc-link current can be estimated from average ac-link power, which derived from ac-link voltage and current, as expressed in (4.15). Based on (4.15), the total induc-

$$i_{\mathrm{a}}(\varphi)=\begin{cases}\dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\dfrac{\varphi^2}{\theta_{\mathrm{R}}}-\varphi+\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\Phi-\dfrac{\theta_{\mathrm{R}}}{2}+\dfrac{\pi}{2}\right), & 0<\varphi<\theta_{\mathrm{R}},\\ \dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\Phi-\dfrac{\theta_{\mathrm{R}}}{2}+\dfrac{\pi}{2}\right), & \theta_{\mathrm{R}}<\varphi<\Phi,\\ \dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(-\dfrac{(\varphi-\Phi)^2}{\theta_{\mathrm{R}}}+\varphi-\Phi-\dfrac{\theta_{\mathrm{R}}}{2}+\dfrac{\pi}{2}\right), & \Phi<\varphi<\Phi+\theta_{\mathrm{R}},\\ \dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(-\varphi+\Phi+\dfrac{\theta_{\mathrm{R}}}{2}+\dfrac{\pi}{2}\right), & \Phi+\theta_{\mathrm{R}}<\varphi<\pi,\\ -i_{\mathrm{a}}(\varphi-\pi), & \pi<\varphi<2\pi.\end{cases} \tag{4.13}$$

$$i_{\mathrm{a}}(\varphi)=\begin{cases}\dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\dfrac{\varphi^2}{\theta_{\mathrm{R}}}-\varphi+\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(-\varphi+\Phi+\dfrac{\theta_{\mathrm{R}}}{2}+\dfrac{\pi}{2}\right), & 0<\varphi<\theta_{\mathrm{R}},\\ \dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(-\varphi+\Phi+\dfrac{\theta_{\mathrm{R}}}{2}+\dfrac{\pi}{2}\right), & \theta_{\mathrm{R}}<\varphi<\pi+\Phi,\\ \dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left[\dfrac{(\varphi-\pi-\Phi)^2}{\theta_{\mathrm{R}}}-\varphi+\Phi+\dfrac{\theta_{\mathrm{R}}}{2}+\dfrac{\pi}{2}\right], & \pi+\Phi<\varphi<\pi+\Phi+\theta_{\mathrm{R}},\\ \dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(\varphi-\Phi-\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{3\pi}{2}\right), & \pi+\Phi+\theta_{\mathrm{R}}<\varphi<\pi,\\ -i_{\mathrm{a}}(\varphi-\pi), & \pi<\varphi<2\pi.\end{cases} \tag{4.14}$$

tance of the MMC-based SST can be determined from system parameters. The rated power corresponds to $|\Phi| = \dfrac{\pi}{2}$.

$$I_{\mathrm{dc,pri}}=\frac{\int_0^{2pi} v_{\mathrm{ac,pri}} i_{\mathrm{a}}\,\mathrm{d}\varphi}{2\pi V_{\mathrm{dc,pri}}}=\begin{cases}-\dfrac{n_T V_{\mathrm{dc,sec}}}{\pi\omega L_{\mathrm{tot}}}\left(\dfrac{\theta_{\mathrm{R}}^2}{6}+\Phi^2-\pi\Phi\right), & \Phi>0,\\ \dfrac{n_T V_{\mathrm{dc,sec}}}{\pi\omega L_{\mathrm{tot}}}\left(\dfrac{\theta_{\mathrm{R}}^2}{6}+\Phi^2+\pi\Phi\right), & \Phi<0.\end{cases} \tag{4.15}$$

4.2.2 Submodule Capacitance of MMC-Based SST

According to (4.6), the capacitor voltage is related to arm current. Based on the above analysis, the piecewise-linear equation of arm current can be derived from (4.13), (4.14), and (4.15). In addition, the (4.6) expresses relationship between capacitor voltage and capacitor charge (Q_c), where Q_c is defined as integral of capacitor current. In this way, the peak-peak ripple of capacitor voltage $\Delta V_{\mathrm{c,pp}}$ equals to $\dfrac{\Delta Q_{\mathrm{c,pp}}}{C}$, where $\Delta Q_{\mathrm{c,pp}}$ is peak-peak

ripple of capacitor charge. After determining $\Delta Q_{\mathrm{c,pp}}$, the SM capacitance can be determined by $\dfrac{\Delta Q_{\mathrm{c,pp}}}{\Delta V_{\mathrm{c,pp}}}$.

4.2.3 Arm Inductance of MMC-Based SST

In the analysis of Section 4.2.2, the circulating current only contains half of dc-link current. Theoretically, it also contains harmonics and current ripple. In this section, the peak-peak current ripple is estimated to determine arm inductance. In the following analysis, the circulating current is divided into two terms, the dc circulating current and harmonics as expressed in (4.16).

$$i_{zx} = \overline{i_{zx}} + \widetilde{i_{zx}} = \frac{I_{\mathrm{dc}}}{2} + \sum i_{zx,hn}, \tag{4.16}$$

where I_{dc} represents primary/secondary-side dc-link current, $i_{zx,hn}$ represents the n^{th} order harmonic of circulating current.

Similarly, the arm voltage is divided into two terms. One is derived from average value of capacitor voltage, while the other is derived from capacitor voltage ripple, which are defined in (4.17).

$$v_{\mathrm{arm}} = \overline{v_{\mathrm{arm}}} + \widetilde{v_{\mathrm{arm}}} = \sum_{i=1}^{N_{\mathrm{SM}}} \overline{v_{\mathrm{ci}}} S_{\mathrm{SMi}} + \sum_{i=1}^{N_{\mathrm{SM}}} \widetilde{v_{\mathrm{ci}}} S_{\mathrm{SMi}}, \tag{4.17}$$

where $\overline{v_{\mathrm{ci}}}$ denotes the average capacitor voltage of the i^{th} SM, while $\widetilde{v_{\mathrm{ci}}}$ represents capacitor voltage ripple of of the i^{th} SM.

When substituting (4.16) and (4.17) into (4.3), it can be modified as (4.18).

$$R_{\mathrm{arm}}\left(\overline{i_{zx}} + \widetilde{i_{zx}}\right) + L_{\mathrm{arm}} \frac{\mathrm{d}\widetilde{i_{zx}}}{\mathrm{d}t} = \frac{V_{\mathrm{dc}} - \overline{v_{xu}} - \overline{v_{xl}}}{2} - \frac{\widetilde{v_{xu}} + \widetilde{v_{xl}}}{2}. \tag{4.18}$$

In this way, the current ripple of circulating current is resulted from capacitor voltage ripple. The voltage ripple crossing arm inductor can be estimated by $\dfrac{V_{\mathrm{dc}} - v_{xu} - v_{xl}}{2} - R_{\mathrm{arm}} \dfrac{I_{\mathrm{dc}}}{2}$. When neglecting R_{arm}, the current ripple of circulating current can be expressed as

$$\widetilde{i_{zx}} = \frac{B_{\mathrm{Larm}}}{L_{\mathrm{arm}}} = \frac{1}{L_{\mathrm{arm}}} \int \frac{V_{\mathrm{dc}} - v_{xu} - v_{xl}}{2} - R_{\mathrm{arm}} \frac{I_{\mathrm{dc}}}{2} \mathrm{d}t, \tag{4.19}$$

where B_{Larm} is flux density of arm inductor. In this way, after determining peak-peak ripple of flux density $\Delta B_{\text{Larm,pp}}$, the arm inductance can be estimated as $\frac{\Delta B_{\text{Larm,pp}}}{\Delta i_{zx,\text{pp}}}$, where $\Delta i_{zx,\text{pp}}$ is peak-peak ripple of circulating current.

4.2.4 Implementation of Modified Mathematical Model Considering Parameter Design

According to analysis of Sections 4.2.1 to 4.2.3, all circuit parameters are determined based on given system parameters. In addition, some variables are initialized, including arm voltages and currents, capacitor voltages, and arm voltages. Then, these circuit parameters and initialized variables are substituted into mathematical model to solve steady-state conditions of the MMC-based SST, as shown in Fig. 4.4. To be clearer, a pseudo code of implementing the MMC-based SST appears in Table 4.2.

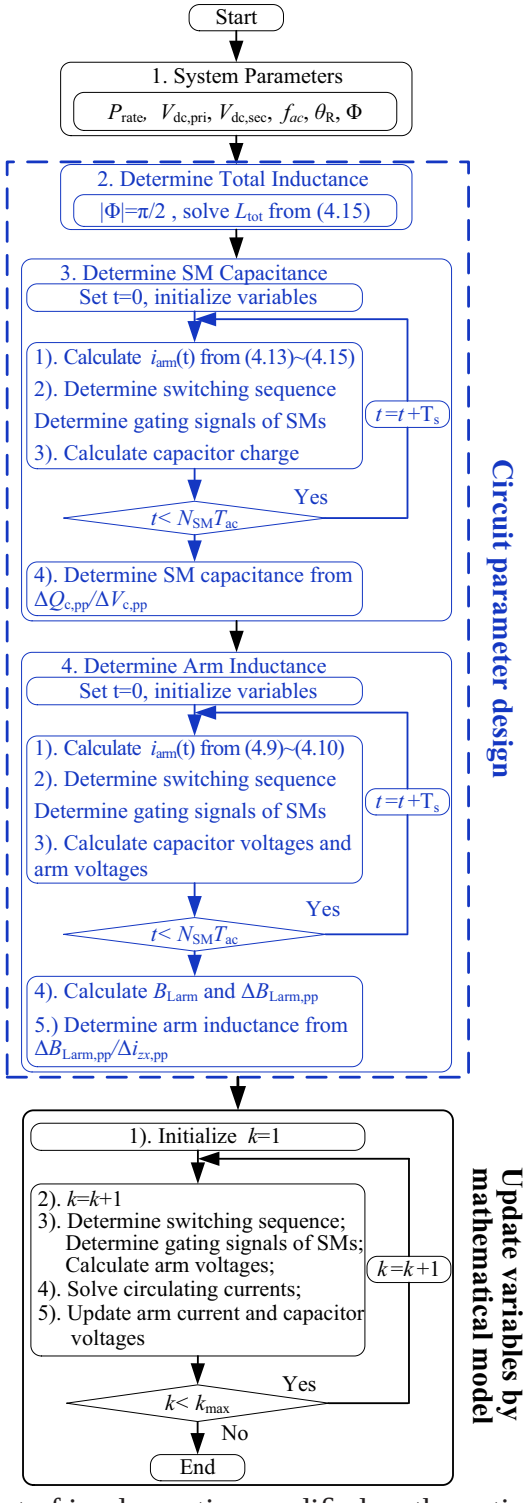


Figure 4.4. The flowchart of implementing modified mathematical model of the MMC-based SST considering circuit parameter design.

Table 4.2

Pseudo Code of Modified Mathematical Model for Optimal Design of MMC-Based SST

Set System Parameters: P_{rate}, $V_{\text{dc,pri}}$, $V_{\text{dc,sec}}$, f_{ac}, θ_{R}, Φ;

Set Circuit Parameters: N_{SM};

Set Limitations: $\Delta V_{\text{c,pp}}$, $\Delta i_{\text{zx,pp}}$;

Set Simulation parameters: number of simulation steps $k_{\max}$, simulation time step T_s;

Initialize Variables ($k = 1$**)**: phase currents, arm currents, dc-link currents, arm voltages, capacitor voltages, gating signals;

Determine L_{tot} **by** (4.15) ;

Determine SM capacitance

FOR k=2 to $N_{\text{SM}}N_{\text{samp}}$ % N_{samp} is number of sampling points per period $\frac{1}{f_{ac}T_s}$

solve $i_{\text{arm}}(k)$ from (4.13), (4.14), and (4.15);

$[\text{S}_{SM}(k)]$=Balancing (Sorting options, $Q_c(k-1)$);

solve capacitor charge by $Q_c(k) = Q_c(k-1) + \dfrac{i_{\text{arm}}(k)S_{\text{SM}}(k) + i_{\text{arm}}(k-1)S_{\text{SM}}(k-1)}{2}T_s$;

ENDFOR

Determine SM capacitance C by $\dfrac{\Delta Q_{\text{c,pp}}}{\Delta V_{\text{c,pp}}}$;

Determine Arm Inductance

FOR k=2 to $N_{\text{SM}}N_{\text{samp}}$

$[\text{ID}_{xu}(k)]$=Voltage balancing (Sorting options, $v_{c,xu}(k-1)$);

$[\text{ID}_{xl}(k)]$=Voltage balancing (Sorting options, $v_{c,xl}(k-1)$);

$[\text{S}_{xu}(k),\ \text{V}_{xu}(k)]$=Modulation (Modulation options, $v_{c,xu}(k-1)$);

$[\text{S}_{xl}(k),\ \text{V}_{xl}(k)]$=Modulation (Modulation options, $v_{c,xl}(k-1)$);

solve flux density B_{Larm} by $B_{\text{Larm}}(k) = B_{\text{Larm}}(k-1) + \dfrac{V_{\text{dc}} - \text{V}_{xu}(k) - \text{V}_{xl}(k)}{2}T_s$;

solve $i_{\text{xu}}(k)$, $i_{\text{xl}}(k)$ from (4.13), (4.14), and (4.15);

$[v_{c,xu}(k)]$=Solve Capacitor Voltage(C, $i_{xu}(k)$, $i_{xu}(k-1)$, $\text{S}_{xu}(k)$, T_s);

$[v_{c,xl}(k)]$=Solve Capacitor Voltage(C, $i_{xl}(k)$, $i_{xl}(k-1)$, $\text{S}_{xl}(k)$, T_s);

ENDFOR

Determine Arm Inductance L_{arm} by $\dfrac{\Delta B_{\text{Larm}}}{\Delta i_{\text{zx,pp}}}$;

Determine L_{T};

Update Variables

FOR $k = 2$ to $k_{\max}$

Voltage Balancing

[ID$_{xu}(k)$]=Voltage balancing (Sorting options, $v_{c,xu}(k-1)$);

[ID$_{xl}(k)$]=Voltage balancing (Sorting options, $v_{c,xl}(k-1)$);

Modulation

[$S_{xu}(k)$, $V_{\text{arm},xu}(k)$]=Modulation (Modulation options, $v_{c,xu}(k-1)$);

[$S_{xl}(k)$, $V_{\text{arm},xl}(k)$]=Modulation (Modulation options, $v_{c,xl}(k-1)$);

Solve ac-link current and phase currents

[$i_a(k)$]=Solve ac-link current($V_{\text{arm},au}(k) \sim V_{\text{arm},du}(k)$, $V_{\text{arm},al}(k) \sim V_{\text{arm},dl}(k)$, $i_a(k-1)$, R_{T}, L_{T}, n_{T}, R_{arm}, L_{arm}, T_s);

$i_b(k) = -i_a(k)$, $i_c(k) = -n_{\text{T}} i_a(k)$, $i_d(k) = -n_{\text{T}} i_b(k)$;

Solve circulating currents

[$i_{zx}(k)$]=Solve circulating current($V_{\text{arm},xu}(k)$, $V_{\text{arm},xl}(k)$, $i_{zx}(k-1)$, R_{arm}, L_{arm}, T_s);

Solve arm currents $i_{xu}(k) = 0.5 i_x(k) + 0.5 i_{zx}(k)$, $i_{xl}(k) = -0.5 i_x(k) + 0.5 i_{zx}(k)$;

Update capacitor voltages

[$v_{c,xu}(k)$]=Solve Capacitor Voltage(C, $i_{xu}(k)$, $i_{xu}(k-1)$, $S_{xu}(k)$, T_s);

[$v_{c,xl}(k)$]=Solve Capacitor Voltage(C, $i_{xl}(k)$, $i_{xl}(k-1)$, $S_{xl}(k)$, T_s);

ENDFOR

4.3 Verifications of Mathematical Model for MMC-Based SST

4.3.1 Simulation Verification

To verify the accuracy of the detailed mathematical model and the proposed modified mathematical model, an MMC-based SST is implemented based on different models. Firstly, the circuit parameters are designed by the proposed modified mathematical model from system requirements. Then, the MMC-based SST is implemented in PSCAD based on the equivalent circuit model. The MMC-based SST based on detailed mathematical model and proposed modified model are implemented in MATLAB. The system specifications are listed in Table 4.3, where the total inductance is determined by the proposed modified mathematical model according to (4.15).

Table 4.3
Parameters of the MMC-Based SST Simulation System Based on Different Models

Parameters	**Nominal Value**
Maximum power	1 MW
Primary-side dc-link voltage	10 kV
Secondary-side dc-link voltage	10 kV
Frequency of ac-link voltage	10 kHz
Turn ratio of isolated transformer, n_T	1:1
Number of SMs per arm	10
Ramping angle, θ_{R}	0.4π
Total inductance	1.06 mH

To verify the performance of the detailed mathematical model and the proposed modified mathematical model, both of the PS modulation and NLC modulation are considered, while only the single-step alternating voltage balancing algorithm is considered, which was proposed in [52]. Then, based on the above system parameters, the SM capacitance, arm inductance, and leakage inductance of ac-link transformer are determined by the proposed modified mathematical model according to analysis in Sections 4.2.2 and 4.2.3. When determining SM capacitor, the peak-peak ripple is limited to 2% of the nominal capacitor voltage. When determining arm inductance, only the fundamental-frequency and double-frequency circulating currents are considered, which limits the peak-peak ripple to 5% of dc circulating current. Based on PS modulation, the SM capacitance is 305 μF, while the arm inductance is only 88 μH. Based on NLC modulation, the SM capacitance is 213 μF, while the arm inductance is 137 μH.

Based on PS modulation, figure 4.5 shows the arm voltages, arm currents, and capacitor voltages of different models. In addition, figure 4.7 compares the Fourier spectrum of voltages and currents obtained from different models. Based on NLC modulation, the voltages, currents, and their spectrum are shown in Figs. 4.6 and 4.8. To further verify

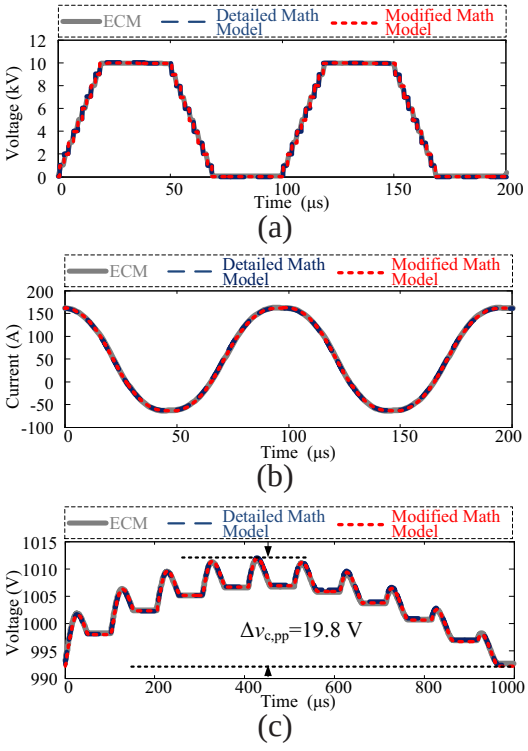


Figure 4.5. The simulation results of MMC-based SST based on PS modulation: (a) arm voltages, (b) arm currents, and (c) capacitor voltages.

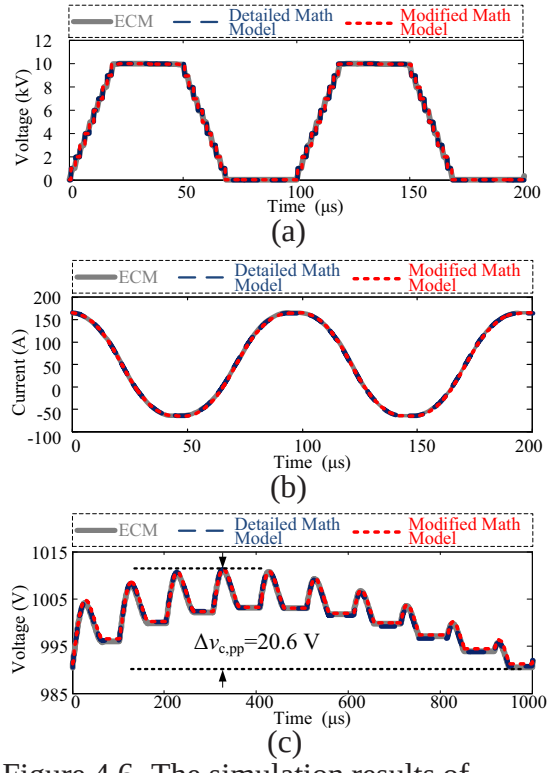


Figure 4.6. The simulation results of MMC-based SST based on NLC modulation: (a) arm voltages, (b) arm currents, and (c) capacitor voltages.

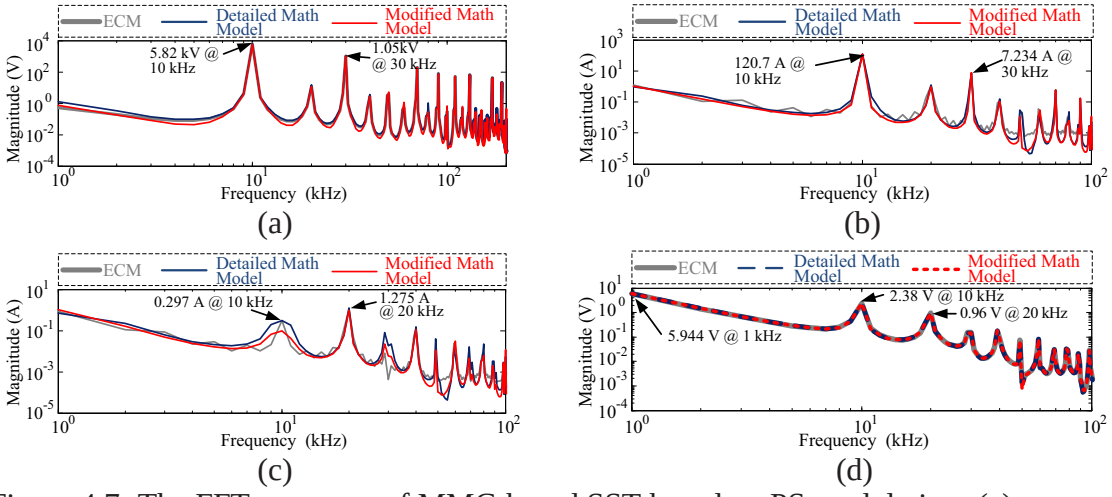


Figure 4.7. The FFT spectrum of MMC-based SST based on PS modulation: (a) arm voltages, (b) arm currents, (c) circulating current, and (d) capacitor voltages.

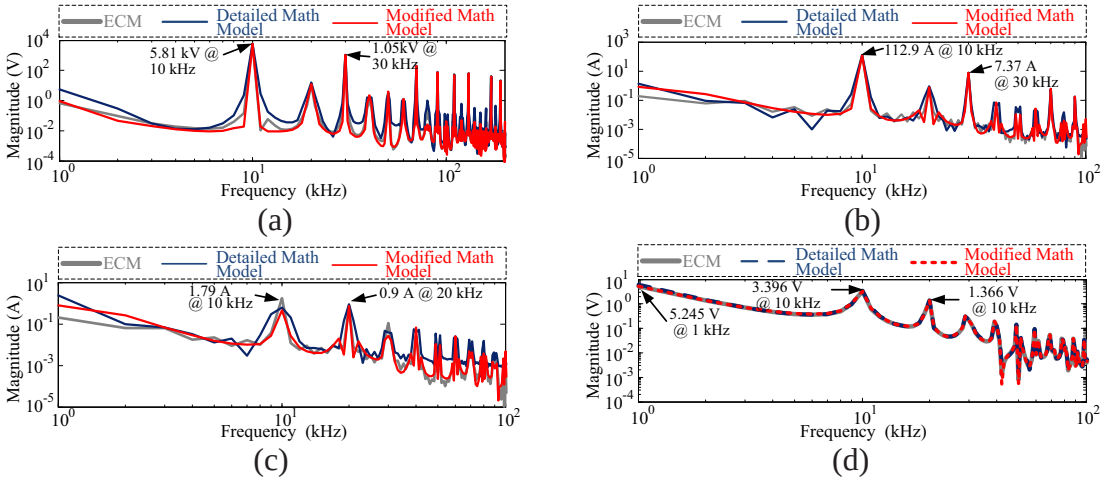


Figure 4.8. The FFT spectrum of MMC-based SST based on NLC modulation: (a) arm voltages, (b) arm currents, (c) circulating current, and (d) capacitor voltages.

performances of the MMC-based SST based on different models, the semiconductor losses are compared in Table 4.4, where the Infineon FF150R12RT4 is selected for calculating semiconductor losses.

Table 4.4

Semiconductor Losses of the Simulation System Based on Different Models and Different Modulations

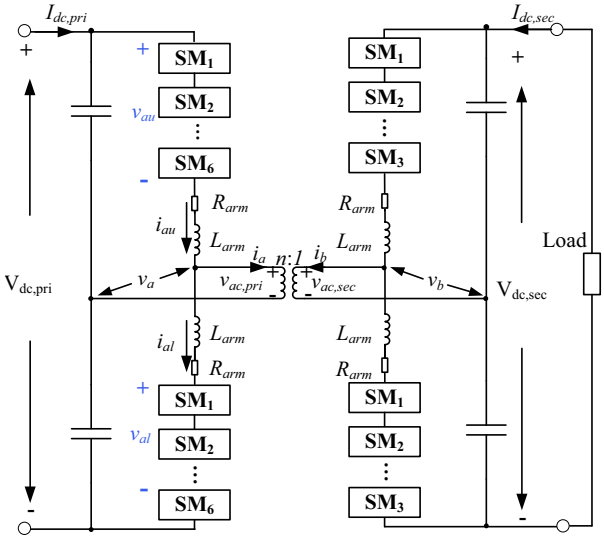
Model	**PS**		**NLC**	
	P_{SW} **(kW)**	P_{con} **(kW)**	P_{SW} **(kW)**	P_{con} **(kW)**
ECM	6.085	12.904	6.009	13.034
Detailed math model	5.984	12.945	5.999	12.979
Modified math model	6.004	13.055	5.998	12.975

P_{SW} is the switching loss of semiconductor devices;

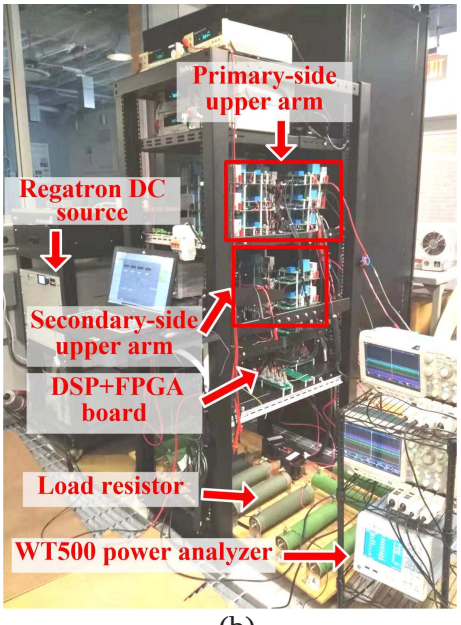
P_{con} is the conduction loss of semiconductor devices.

4.3.2 Experimental Verification

An experimental prototype of the single-phase MMC-based SST is built to evaluate its performances, as shown in Fig. 4.9. Its parameters are listed in Table 4.5. The ramping angle is fixed at $\theta_R = \pi/2$.



(a)



(b)

Figure 4.9. Experimental prototype: (a) schematic of experiment prototype, and (b) photograph of experiment prototype.

Based on PS modulation, figure 4.10 compares the arm voltages, arm currents, and capacitor voltages of mathematical models with experimental waveforms. In addition, figure 4.12 compares the Fourier spectrum of voltages and currents of mathematical models with those of experimental waveforms. Based on NLC modulation, the corresponding results are shown in Figs. 4.11 and 4.13.

Table 4.5
Parameters of the Experimental Prototype

Rated power, P_{rate}	2.5 kW
DC-link voltage, $V_{\text{dc,pri}}$	350 V
Frequency of ac-link voltage, f_{ac}	20 kHz
Primary-side number of SMs per arm	6
Secondary-side number of SMs per arm	3
DC-link capacitance	500 μF
SM capacitance, C	20 μF
Arm inductance, L_{arm}	20 μH
Load resistance	75 Ω
Semiconductor device	FGH40T65UQDF
Transformer turns ratio	1:1

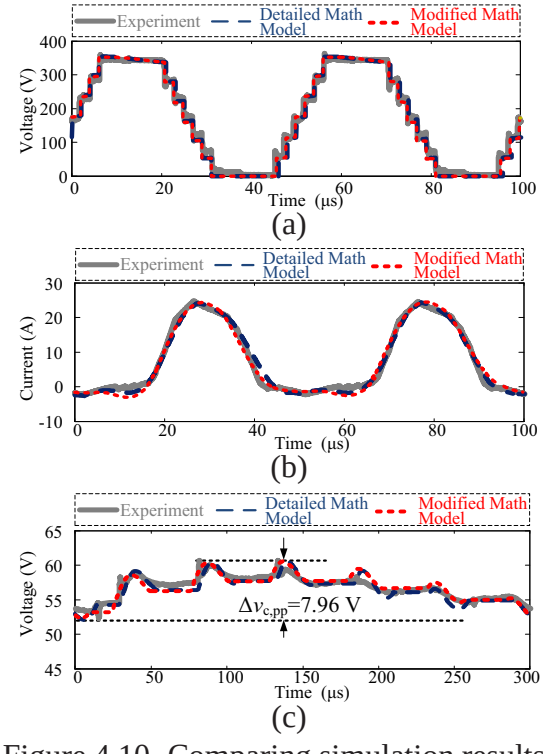


Figure 4.10. Comparing simulation results with experimental waveform of MMC-based SST based on PS modulation: (a) arm voltages, (b) arm currents, and (c) capacitor voltages.

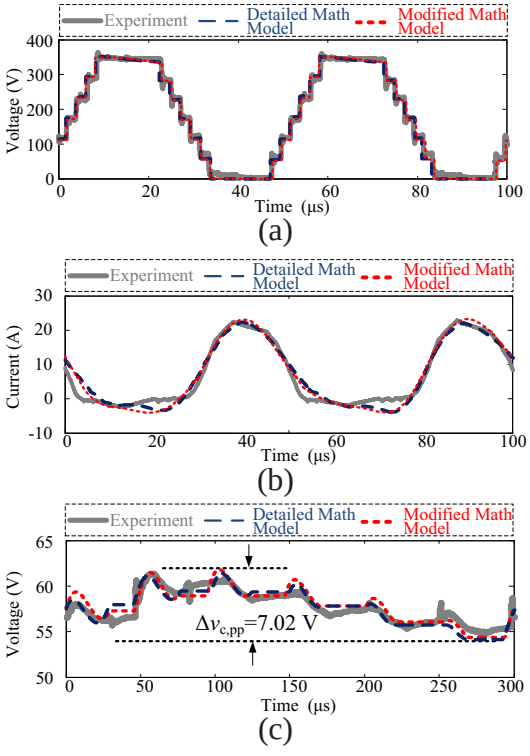


Figure 4.11. Comparing simulation results with experimental waveform of MMC-based SST based on NLC modulation: (a) arm voltages, (b) arm currents, and (c) capacitor voltages.

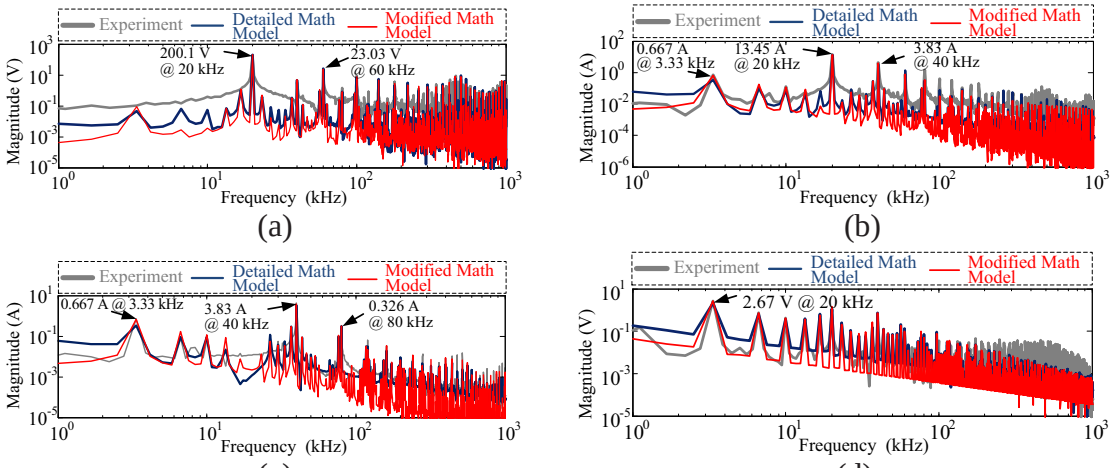


Figure 4.12. Comparing FFT spectrum of experimental prototype and simulation system based on PS modulation: (a) arm voltages, (b) arm currents, (c)circulating current, and (d) capacitor voltages.

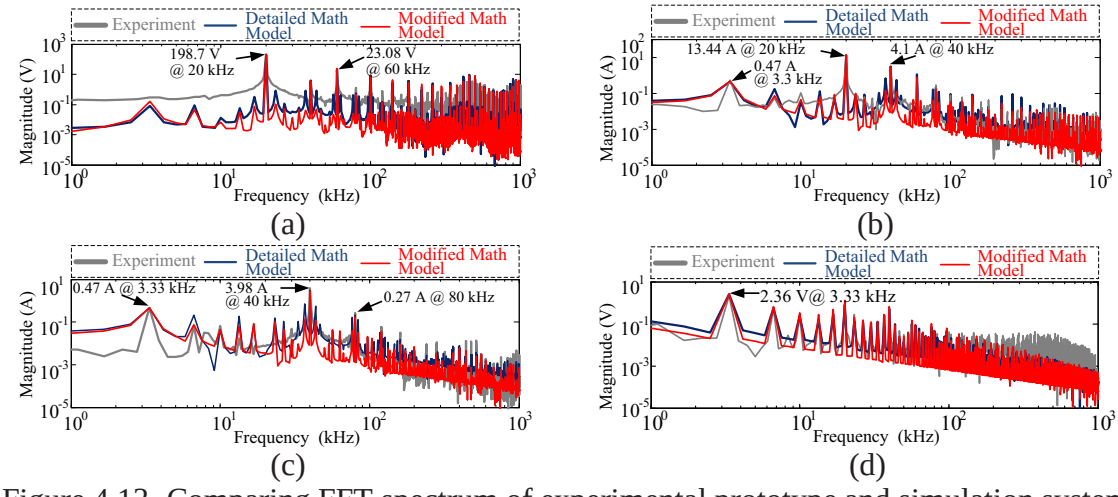


Figure 4.13. Comparing FFT spectrum of experimental prototype and simulation system based on NLC modulation: (a) arm voltages, (b) arm currents, (c)circulating current, and (d) capacitor voltages.

Chapter 5

VOLTAGE BALANCING ALGORITHMS OF MODULAR MULTILEVEL CONVERTER-BASED SOLID-STATE TRANSFORMER BASED ON DIFFERENT MODULATION METHODS

In this chapter, firstly, the performances of PS modulation and NLC modulation are analyzed and evaluated for IM2DC. Then, the performances of single-step alternating voltage-balancing algorithm and the conventional reduced switching-frequency (RSF) voltage-balancing algorithm [97] are analyzed for IM2DC. Based on these analyses, the problems of modulation methods and voltage-balancing algorithms are summarized. Finally, the improved voltage-balancing algorithms are proposed in this chapter by rearranging capacitor charging order.

5.1 IM2DC Operating Principle

According to analysis of Chapter 4, the IM2DC has similar operational principles with the DAB converter. The difference is that the MMC can generate a controllable multilevel voltage waveform. In this chapter, the trapezoidal ac-link voltage is employed for the analysis. The following analysis is performed for the primary-side MMC, which is also applicable for the secondary-side MMC.

5.1.1 Modulation Methods

To generate the multilevel ac-link voltages, the PS modulation is widely used in IM2DC, which has been analyzed in [52, 134]. The NLC modulation is also a popular method to generate the multilevel ac-link voltage. Based on NLC modulation, firstly, the ac-link voltage determines the number of inserted SMs (N_{insert}). Then, the gating signals are determined based on the switching sequence.

5.1.2 Characteristics of SM Capacitor Charging and Discharging

The SM capacitor charging and discharging performance varies with different modulations. Figures 5.1 and 5.2 show the theoretical waveforms of arm voltage, arm current, and gating signals of the MMC based on the PS and NLC modulation methods, respectively.

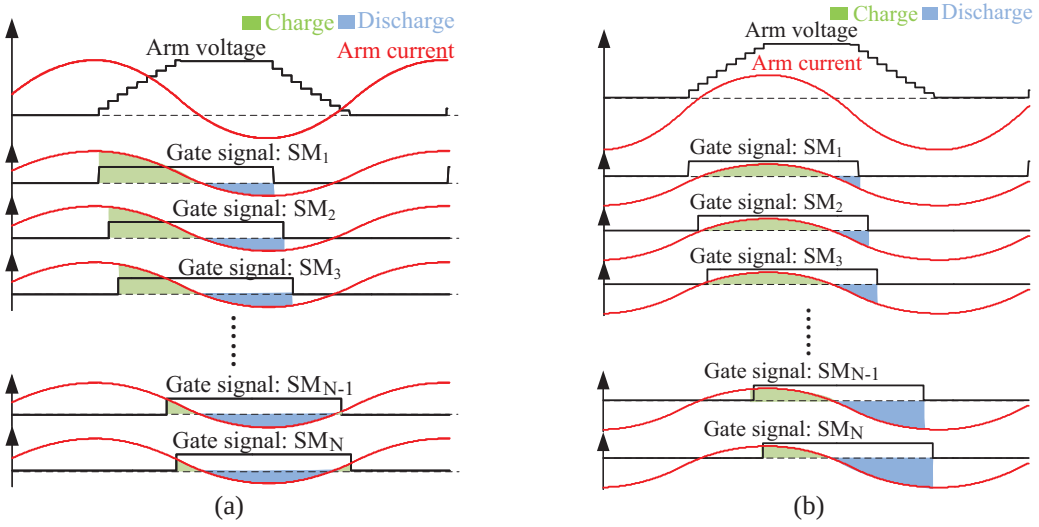


Figure 5.1. Arm voltage, arm current, and gating signals of SMs in primary-side MMC based on PS modulation: (a)$\Phi > 0$, and (b) $\Phi < 0$.

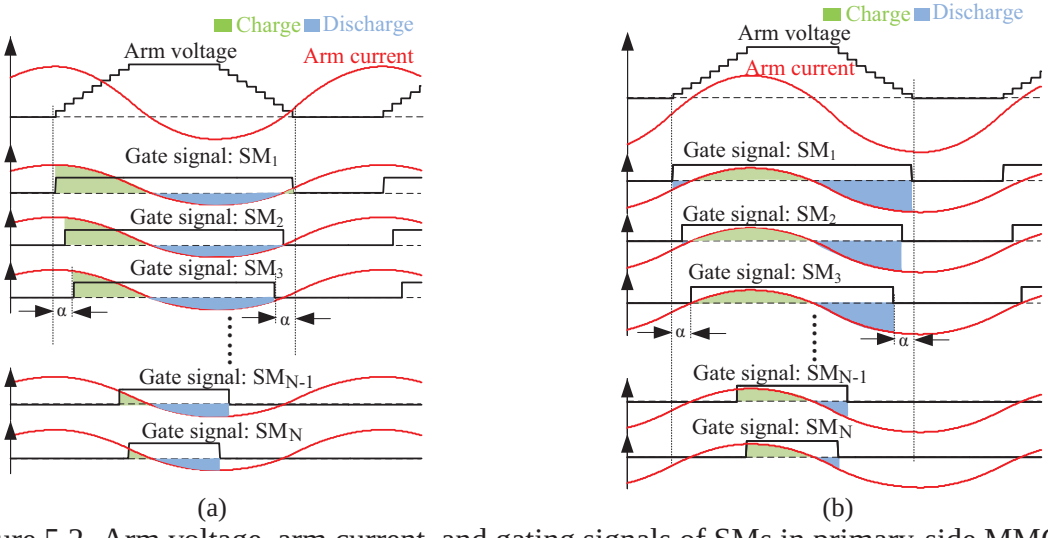


Figure 5.2. Arm voltage, arm current, and gating signals of SMs in primary-side MMC based on NLC modulation: (a) $\Phi > 0$, and (b) $\Phi < 0$.

During each switching period, the capacitor experiences both charging and discharg-

ing processes and the total charge for each SM capacitor depends on the switching angle (α) and ON-state time interval, as shown in Figs. 5.1 and 5.2. For different modulation methods, the switching angle and ON-state time interval vary. Without considering voltage-balancing algorithms, for the PS modulation, the switching angle of the i^{th} SM (α_i) is $\frac{(i-1)\theta_{\mathrm{R}}}{N_{\mathrm{SM}}}$, while the duty ratio is 50%. For the NLC modulation shown in Fig. 5.2, the switching angle of the i^{th} SM (α_i) is also $\frac{(i-1)\theta_{\mathrm{R}}}{N_{\mathrm{SM}}}$, but the ON-state time interval of the i^{th} SM is $\pi + \theta_{\mathrm{R}} - 2\alpha_i$. The capacitor charge can be calculated by (5.1) and (5.2) for the PS and NLC modulation methods, respectively.

$$Q_c = \int_{\alpha}^{\pi+\alpha} i_{\mathrm{arm}}(\varphi)d\varphi, \tag{5.1}$$

$$Q_c = \int_{\alpha}^{\pi+\theta_{\mathrm{R}}-\alpha} i_{\mathrm{arm}}(\varphi)d\varphi, \tag{5.2}$$

where Q_c is the SM capacitor charge during one switching period. α is the angle between the arm voltage and gating signal. i_{arm} is the arm current of the primary-side MMC. Therefore, the expression of the capacitor charge in terms of α is given by (5.3) and (5.4) for the PS and NLC methods, respectively.

$$Q_c(\alpha) = \begin{cases} \dfrac{V_{\mathrm{dc,pri}}}{\omega^2 L_{\mathrm{tot}}}\left(-\dfrac{\theta_{\mathrm{R}}^2}{6}+\dfrac{\pi\theta_{\mathrm{R}}}{4}+\dfrac{\alpha^3}{3\theta_{\mathrm{R}}}-\dfrac{\alpha^2}{2}+\dfrac{\theta_{\mathrm{R}}-\pi}{2}\alpha\right) \\ +\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega^2 L_{\mathrm{tot}}}\left(\dfrac{\theta_{\mathrm{R}}^2}{12}+\dfrac{2\Phi-\pi}{4}\theta_{\mathrm{R}}+\dfrac{\alpha^2}{2}+\dfrac{\pi-2\Phi-\theta_{\mathrm{R}}}{2}\alpha\right), & \Phi \geq 0, \\ \dfrac{V_{\mathrm{dc,pri}}}{\omega^2 L_{\mathrm{tot}}}\left(-\dfrac{\theta_{\mathrm{R}}^2}{6}+\dfrac{\pi\theta_{\mathrm{R}}}{4}+\dfrac{\alpha^3}{3\theta_{\mathrm{R}}}-\dfrac{\alpha^2}{2}+\dfrac{\theta_{\mathrm{R}}-\pi}{2}\alpha\right) \\ +\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega^2 L_{\mathrm{tot}}}\left(-\dfrac{\theta_{\mathrm{R}}^2}{12}-\dfrac{2\Phi+\pi}{4}\theta_{\mathrm{R}}-\dfrac{\alpha^2}{2}+\dfrac{\pi+2\Phi+\theta_{\mathrm{R}}}{2}\alpha\right), & \Phi < 0. \end{cases} \tag{5.3}$$

$$Q_c(\alpha) = \begin{cases} \dfrac{n_T V_{\mathrm{dc,sec}}}{\omega^2 L_{\mathrm{tot}}}\left(-\dfrac{\theta_{\mathrm{R}}^3}{12\pi}+\dfrac{\theta_{\mathrm{R}}^2}{12}-\dfrac{\Phi^2\theta_{\mathrm{R}}}{2\pi}+\dfrac{\Phi\theta_{\mathrm{R}}}{2}+\dfrac{\alpha^2}{2}+\dfrac{6\Phi^2+\theta_{\mathrm{R}}^2}{6\pi}\alpha-\dfrac{2\Phi+\theta_{\mathrm{R}}}{2}\alpha\right), & \Phi \geq 0, \\ \dfrac{n_T V_{\mathrm{dc,sec}}}{\omega^2 L_{\mathrm{tot}}}\left(\dfrac{\theta_{\mathrm{R}}^3}{12\pi}-\dfrac{\theta_{\mathrm{R}}^2}{12}+\dfrac{\Phi^2\theta_{\mathrm{R}}}{2\pi}+\dfrac{\Phi\theta_{\mathrm{R}}}{2}-\dfrac{\alpha^2}{2}-\dfrac{6\Phi^2+\theta_{\mathrm{R}}^2}{6\pi}\alpha-\dfrac{2\Phi-\theta_{\mathrm{R}}}{2}\alpha\right), & \Phi < 0. \end{cases} \tag{5.4}$$

The total charge of an SM capacitor during one switching period varies with the switching angle, as shown in Fig. 5.3. For the PS modulation, the SM capacitor is charged at a

smaller switching angle and discharged at a larger switching angle regardless of the direction of the power flow. For the NLC modulation, if $\Phi > 0$ (the power flows from the primary side to the secondary side), the capacitor is charged at a smaller switching angle and discharged at a larger switching angle. If $\Phi < 0$ (the power flows from the secondary side to the primary side), the charging and discharging pattern is reversed, as shown in Fig. 5.3.

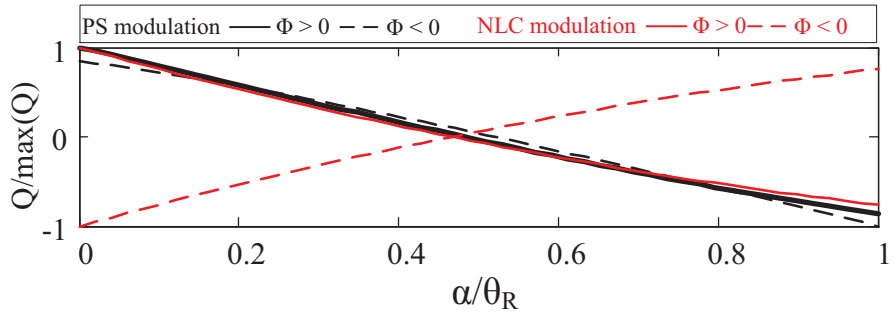


Figure 5.3. Capacitor charge of an SM for the PS and NLC modulation methods ($\theta_R = \pi/5$).

In addition, the capacitor charges calculated by the mathematical model are shown in Fig. 5.4 with changing the ramping angle θ_R from 0.2π to 0.5π. The increased θ_R will increase the net capacitor charges, resulting in larger voltage ripple. Comparing with the NLC modulation, the PS modulation has larger net capacitor charges.

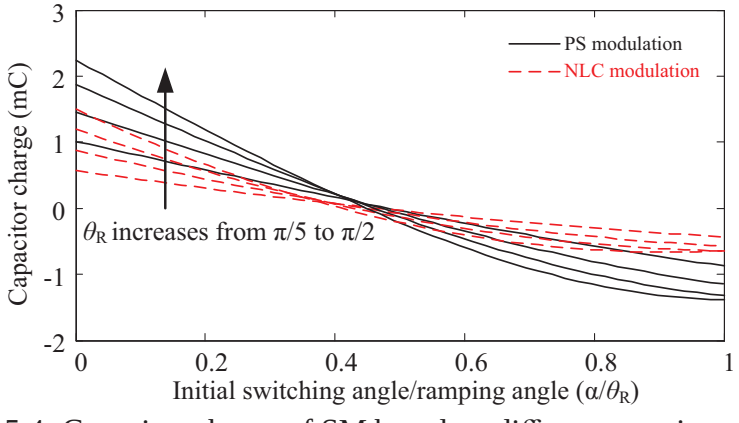


Figure 5.4. Capacitor charge of SM based on different ramping angles.

5.2 Analysis and Performance Comparison of Various Voltage-Balancing Algorithms and Modulation Methods

In this section, the charging and discharging performance of the single-step alternating voltage-balancing algorithm and the conventional sorting algorithm with the PS and NLC modulation methods are comprehensively analyzed and compared. Based on the analysis, the characteristics of SM capacitor voltage ripple will be derived.

To evaluate performances of varies voltage balancing algorithms based on different modulation methods, an IM2DC is built in PSCAD simulation environment. The system specifications are listed in Table 5.1. For all operating conditions, the absolute value of the phase-shift angle Φ is fixed at $\pi/2$.

Table 5.1
Parameters of the IM2DC Simulation System

Parameters	**Nominal Value**
Maximum power	1 MW
Primary-side dc-link voltage	10 kV
Secondary-side dc-link voltage	10 kV
Frequency of ac-link voltage	10 kHz
Turn ratio of isolated transformer	1:1
Number of SMs per arm	9
SM capacitance	50 μF
Arm inductance	50 μH
Transformer leakage inductance	1100 μH

5.2.1 Single-Step Alternating Voltage-Balancing Algorithm with the PS and NLC Modulation Methods

In [52], the single-step alternating voltage-balancing algorithm has been investigated based on the PS modulation, which alternatively changes the switching angle of each S-

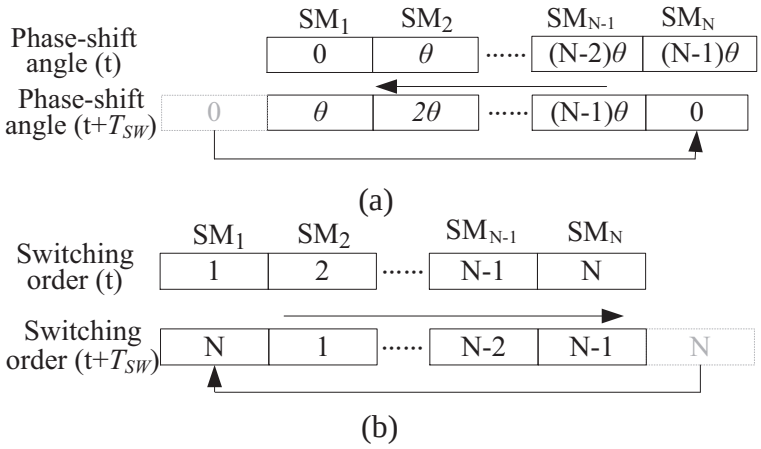


Figure 5.5. Implementation of the single-step alternating voltage-balancing algorithm based on: (a) the PS modulation, and (b) the NLC modulation.

M (α) step-by-step from 0 to $\frac{(N_{\mathrm{SM}}-1)\theta_{\mathrm{R}}}{N_{\mathrm{SM}}}$. However, the single-step alternating voltage-balancing algorithm can also be implemented based on the NLC modulation by rotating the switching order of the SMs, as shown in Fig. 5.5 (b). The switching order is changed by one step in each switching period. Thus, the charging-discharging period includes N_{SM} switching periods. The charging and discharging characteristics of an SM capacitor based on the single-step alternating voltage-balancing algorithm with the PS and NLC methods are shown in Figs. 5.6 and 5.7, respectively.

Based on the analysis in Section 5.1.2 and Figs. 5.6 and 5.7, the charging-discharging period is N_{SM} times the switching period $N_{\mathrm{SM}}T_{\mathrm{SW}}$. The capacitor is charged during the first half of the charging-discharging period and discharged in the last half period for the single-step alternating voltage-balancing algorithm with the PS modulation, as shown in Fig. 5.6. While the capacitor is charged during the last half period and discharged in the first half period for the single-step alternating voltage-balancing algorithm with the NLC modulation, as shown in Fig. 5.7. Therefore, for the single-step alternating voltage-balancing algorithm with either the PS or the NLC, there is a low-frequency capacitor voltage ripple with the period of $N_{\mathrm{SM}}T_{\mathrm{SW}}$.

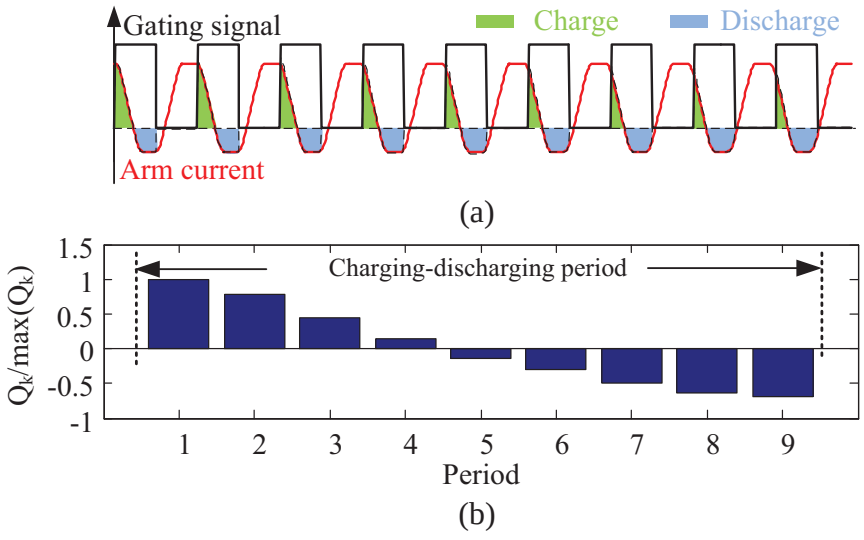


Figure 5.6. Charging and discharging characteristics of SM capacitor in the primary-side MMC based on the single-step alternating voltage-balancing algorithm with the PS modulation: (a) gating signal and arm current, and (b) capacitor charges.

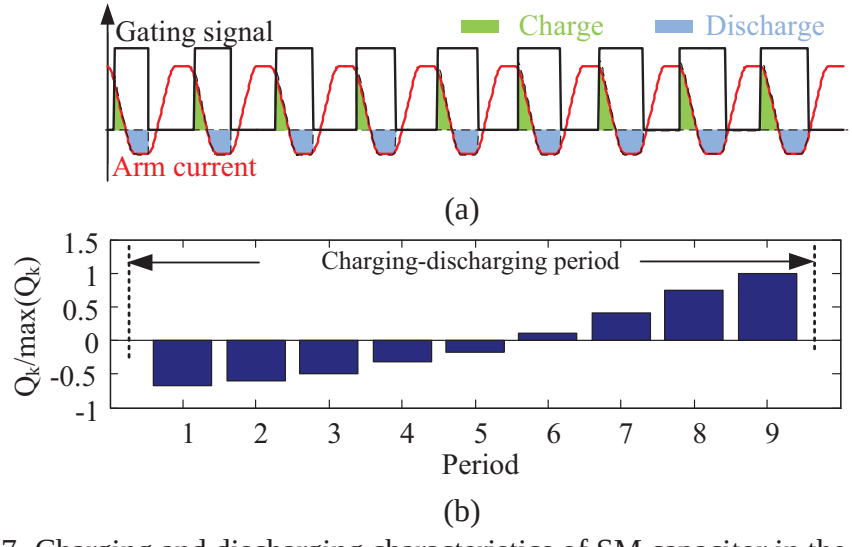
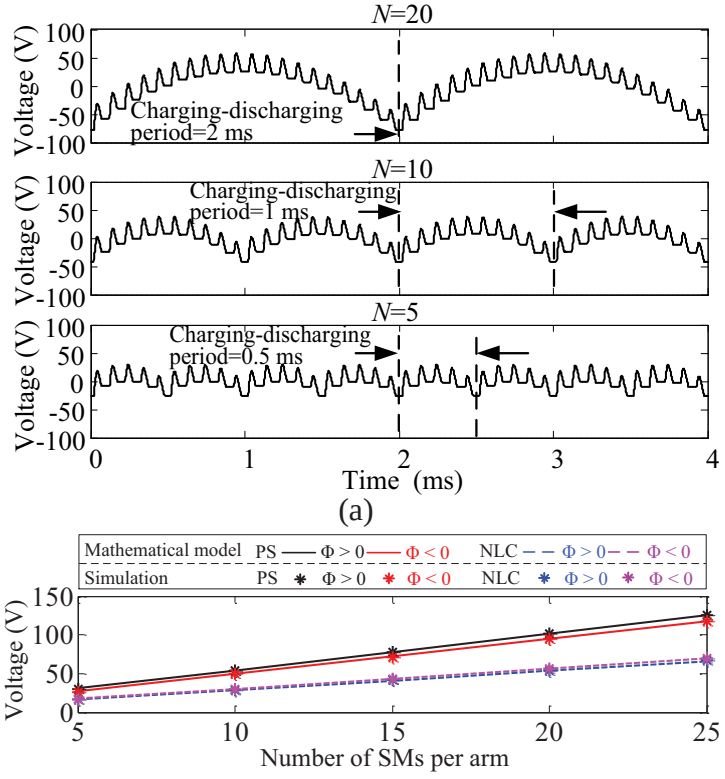


Figure 5.7. Charging and discharging characteristics of SM capacitor in the primary-side MMC based on the single-step alternating voltage-balancing algorithm with the NLC modulation: (a) gating signal and arm current, and (b) capacitor charges.

During the k^{th} switching period in the charging-discharging period, the SM capacitor voltage variation can be determined by ($Q_{ck} = C\Delta v_{ck}$). To evaluate the peak-to-peak value of the low-frequency capacitor voltage ripple ($\Delta v_{c,pp}$), all positive charges in a charging-discharging period are added and the total positive charges are expressed by (5.5). Figure

5.8 shows the capacitor voltage ripple based on the PS modulation. When fixing SM capacitance as 50 μF, the increased N_{SM} leads to linearly increased capacitor voltage ripple.

$$\Delta v_{\mathrm{c,pp}} = \frac{\sum_{k=1}^{N_{\mathrm{SM}}} |Q_c(\alpha_k)|}{2C}. \tag{5.5}$$



(a)

(b)

Figure 5.8. Capacitor voltage ripples for different N_{SM}s with $\theta_{\mathrm{R}} = \pi/5$: (a) capacitor voltage ripples from the simulation model based on the single-step alternating voltage-balancing algorithm with the PS modulation ($\Phi > 0$), and (b) the peak-peak values of the low-frequency ripple.

5.2.2 The Conventional Sorting Algorithm

The conventional sorting algorithms, i.e., the RSF voltage-balancing algorithms, have been investigated in the MMC-based systems under low-frequency operations [97, 149]. However, they have not yet been comprehensively investigated for the MMC under medium-frequency operation [134, 151].

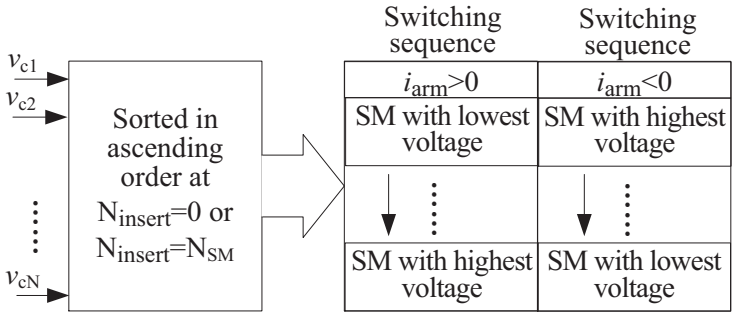


Figure 5.9. Implementation of the conventional sorting algorithm.

For the conventional sorting algorithm, the N_{insert} is determined by the reference arm voltage regardless of the modulation methods. When all SMs are inserted ($N_{\text{insert}} = N_{\text{SM}}$) or bypassed ($N_{\text{insert}} = 0$), the capacitor voltages are sorted in the ascending order, as shown in Fig. 5.9. The gating signals are determined by the polarity of arm current. When the arm current (i_{arm}) is positive, the SMs with the lowest voltages are inserted. When $i_{\text{arm}} < 0$, the SMs with the highest voltages are inserted. If the current direction changes at $N_{\text{insert}} = 0$ or $N_{\text{insert}} = N_{\text{SM}}$, the conventional sorting algorithm does not lead to additional switching actions. On the other hand, if the current direction changes at $0 < N_{\text{insert}} < N_{\text{SM}}$, the additional switching actions occur only when the direction of arm current changes. Since the capacitor voltages are sorted only once and the arm current direction only changes twice every switching period, there are no significantly additional switching actions.

Based on the simulation model with the parameters listed in Table 5.1, the arm voltage/current and gating signals of the IM2DC are shown in Figs. 5.10 and 5.11 for θ_{R} at $\pi/5$ and $\pi/2$, respectively. As shown in Figs. 5.10 and 5.11, the SM capacitors are charged and discharged alternatively in the switching cycles. In this way, there is no significant low-frequency ripple of the SM capacitor voltages.

Based on conventional sorting algorithm, when increasing N_{SM}, the peak-peak value of the low-frequency capacitor voltage ripple is just slightly increased, as shown in Fig. 5.12.

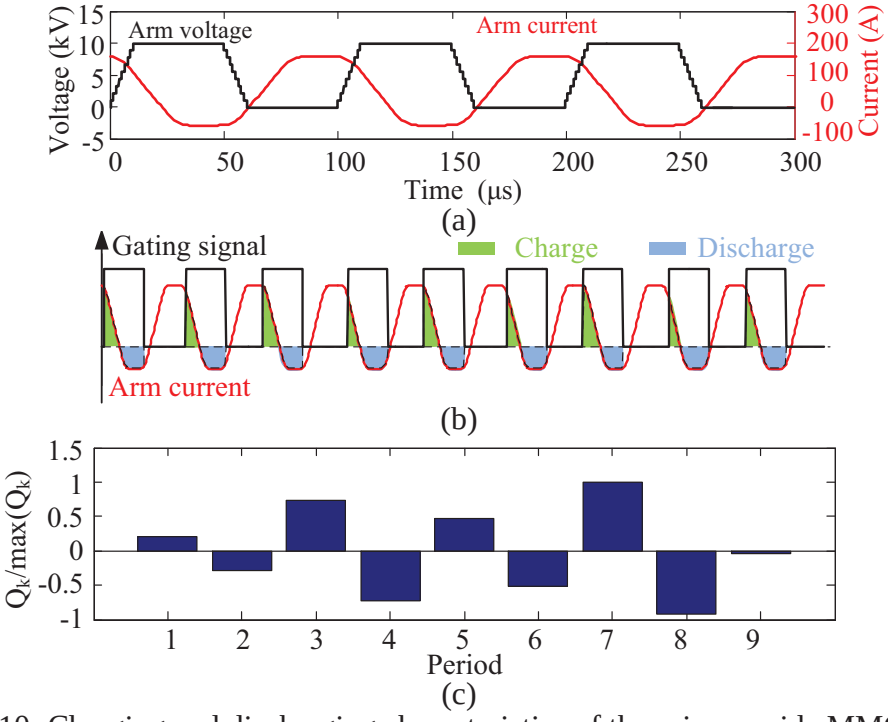


Figure 5.10. Charging and discharging characteristics of the primary-side MMC based on the conventional sorting algorithm ($\theta_R = \pi/5$ and $\Phi = \pi/2$): (a) arm voltage and current, (b) gating signal and arm current, and (c) capacitor charges of an SM.

5.2.3 Summary of Voltage-Balancing Algorithm

Based on the above analysis, the single-step alternating voltage-balancing algorithm is a sensor-less voltage-balancing algorithm, which does not need capacitor voltage feedback. However, the single-step alternating voltage-balancing algorithm has low-frequency ripple of capacitor voltage due to continuously charging or discharging SM capacitors for multiple switching cycles. If the number of SM capacitors is increased, the SM capacitance also needs to be increased to attenuate the voltage ripple.

For the conventional sorting algorithm, the arm current and capacitor voltages should be measured to perform the algorithm. However, there is no significant low-frequency capacitor voltage ripple since the SM capacitor is charged and discharged alternatively during switching cycles. However, the slightly additional switching actions occur due to the changing of arm current direction.

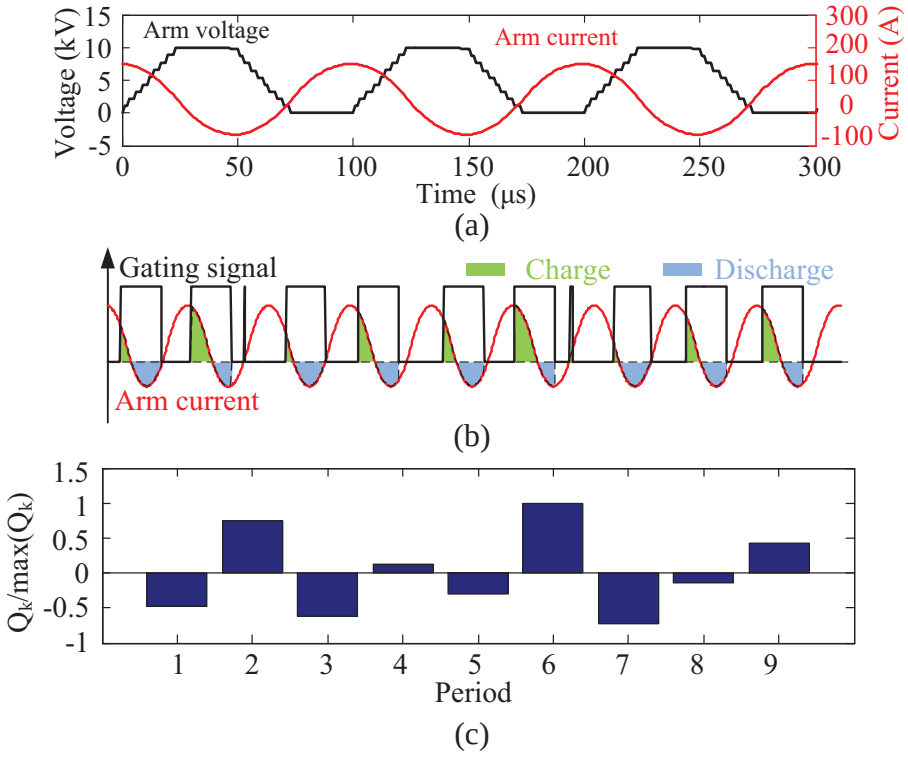


Figure 5.11. Charging and discharging characteristics of the primary-side MMC based on the conventional sorting algorithm ($\theta_R = \pi/2$ and $\Phi = \pi/2$): (a) arm voltage and current, (b) gating signal and arm current, and (c) capacitor charges of an SM.

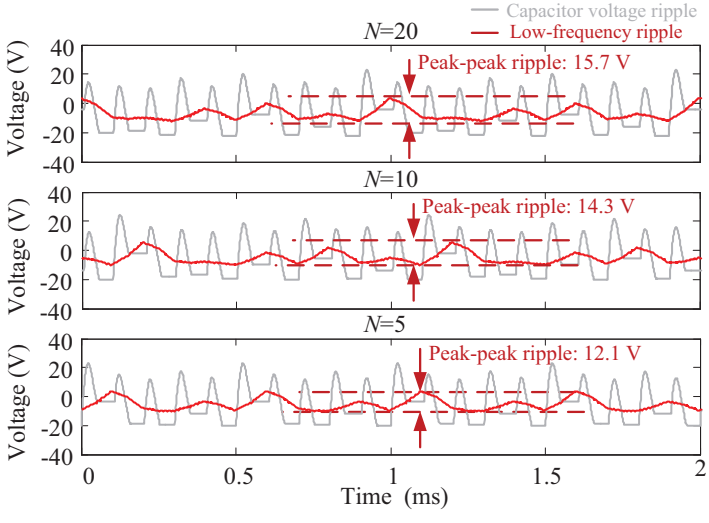


Figure 5.12. Capacitor voltage ripple based on conventional voltage-balancing algorithm for different N_{SM}s.

5.3 The Proposed Voltage-Balancing Algorithms

To attenuate the low-frequency voltage ripple and avoid the additional switching actions, two new voltage-balancing algorithms are proposed in this section.

5.3.1 The Proposed Multi-Step Alternating Voltage-Balancing Algorithm

According to [52], the single-step alternating voltage-balancing algorithm rotates the gating signals of each SM to its adjacent SM by one step in each switching period. However, this single-step method leads to the low-frequency voltage ripple. To attenuate this low-frequency ripple, a multi-step alternating algorithm is proposed, as shown in Fig. 5.13. Based on the analysis in Section 5.1, the SM capacitor is charged at the smaller switching angles and discharged at the larger switching angles, as shown in Fig. 5.3. To charge and discharge the capacitor alternatively, the switching angle should be changed between the smaller angles and the larger angles alternatively. Thus, the proposed method rotates the gating signals by N_{rot} steps in each switching period, as shown in Fig. 5.13. The switching order of the SMs depends on the index number. For example, the SM_1 is the first inserted SM and the index number is 1. During the next switching cycle, the switching sequence rotates by N_{rot} steps and the index number of SM_1 becomes $(N_{\text{rot}} + 1)^{th}$. The algorithm repeats for the following cycles. After N_{SM} switching cycles, the SM_1 will rotate back to its original position.

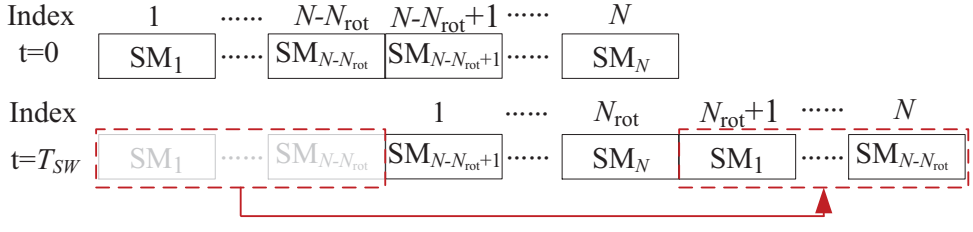


Figure 5.13. Schematic of the proposed multi-step alternating balancing algorithm.

In this section, one possible method to determine N_{rot} is presented and summarized by

(5.6). N_{rot} should be properly selected so that each SM experiences all switching angles from 0 to $\frac{(N_{\text{SM}}-1)\theta_{\text{R}}}{N_{\text{SM}}}$ after N_{SM} switching periods, which is important to maintain the average capacitor voltage [52]. In the first switching period, the switching angle vector rotates by N_{rot} steps. After k cycles, the total rotating steps are kN_{rot}. If the switching angle vector returns to its initial sequence after k cycles, the remainder of $\frac{kN_{\text{rot}}}{N_{\text{SM}}}$ should be zero. Only when $k = N_{\text{SM}}$, each SM experiences all switching angles from 0 to $\frac{(N_{\text{SM}}-1)\theta_{\text{R}}}{N_{\text{SM}}}$. Based on the proposed method of selecting N_{rot}, an SM capacitor can be charged and discharged alternatively so as to avoid continuously charging or discharging, and then suppress the low-frequency voltage ripple. Figure 5.14 shows an example of the switching sequences of the MMC with 8 SMs per arm. Based on Fig. 5.14, when selecting N_{rot} to be 5, each SM can experience all switching angles from 0 to $\frac{(N_{\text{SM}}-1)\theta_{\text{R}}}{N_{\text{SM}}}$.

$$N_{\text{rot}} = \begin{cases} \frac{N_{\text{SM}}-1}{2}, & N_{\text{SM}} \text{ is odd}, \\ \frac{N_{\text{SM}}}{2}+2, & N_{\text{SM}} \text{ is even and } \frac{N_{\text{SM}}}{2} \text{ is odd}, \\ \frac{N_{\text{SM}}}{2}+1, & N_{\text{SM}} \text{ is even and } \frac{N_{\text{SM}}}{2} \text{ is even}. \end{cases} \tag{5.6}$$

In practice, when implementing the proposed multi-step alternating voltage-balancing algorithm with the PS modulation, the initial switching angles are applied to the SMs based on the switching sequence. For instance, $\alpha_i = (i-1)\theta$ is applied to the i^{th} SM to be inserted. Similarly, for the NLC modulation, the SMs are inserted based on the switching sequence.

Figures 5.15 and 5.16 show the switching states and capacitor charges of the SMs in the primary-side MMC based on the proposed multi-step alternating voltage-balancing algorithm for the PS and NLC methods, respectively. The SM capacitor is not charged or discharged for several continuously switching cycles. Therefore, the capacitor voltage ripple can be reduced.

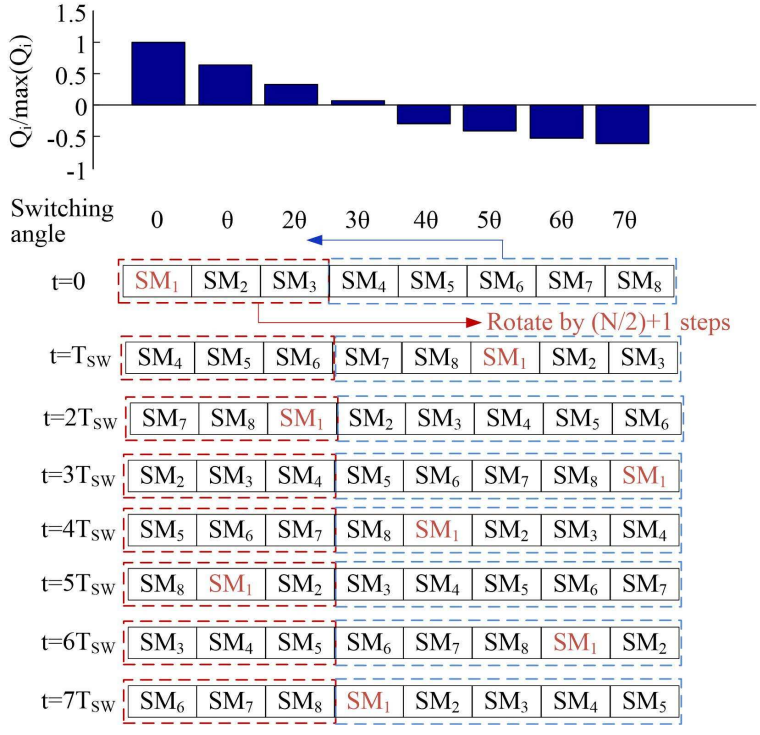


Figure 5.14. Switching sequence of MMC consisted of 8 SMs per arm based on multi-step alternating algorithm.

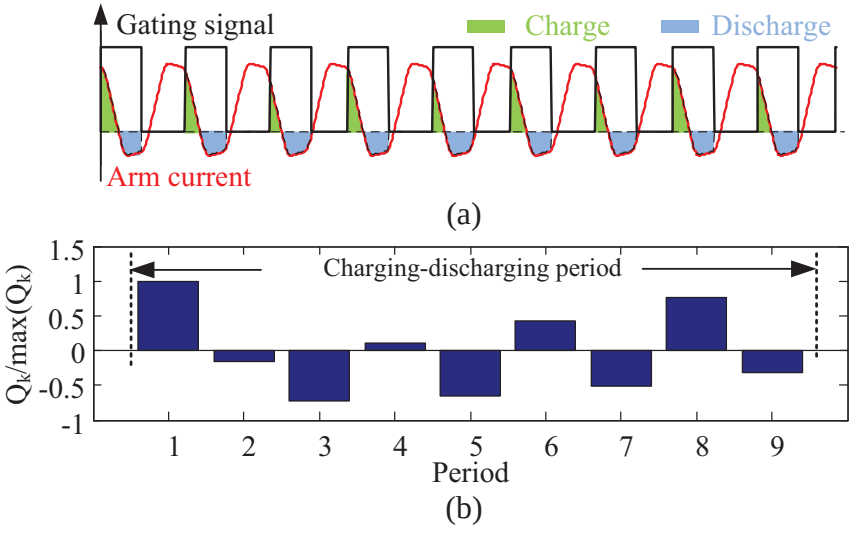


Figure 5.15. Charging and discharging performance of the primary-side MMC based on the proposed multi-step alternating voltage-balancing algorithm with the PS modulation: (a) gating signal and arm current, and (b) capacitor charges.

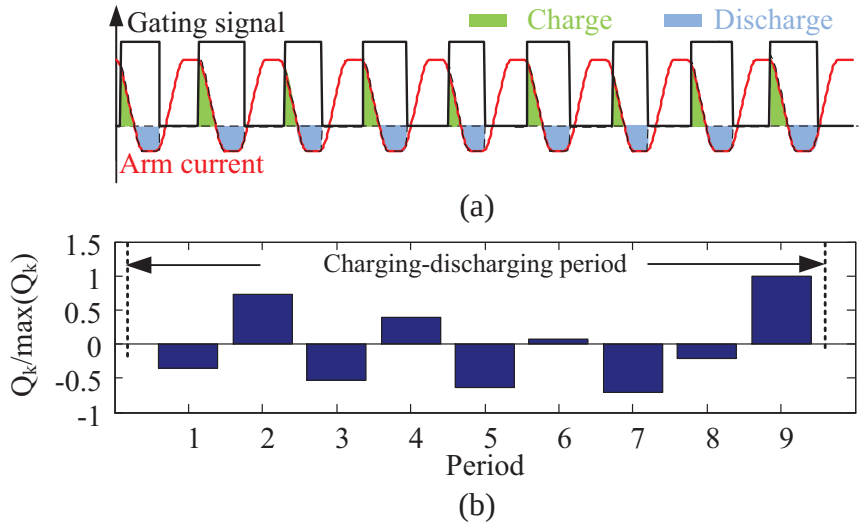


Figure 5.16. Charging and discharging performance of the primary-side MMC based on the proposed multi-step alternating voltage-balancing algorithm with the NLC modulation: (a) gating signal and arm current, and (b) capacitor charges.

5.3.2 Proposed Current-less Sorting Algorithm

The proposed algorithm is based on the analysis in Section 5.1. As shown in Fig. 5.3, the SM capacitor is charged at the smaller switching angle and discharged at the larger switching angle for the PS modulation. The proposed algorithm sorts the SMs in the ascending order when $N_{\text{insert}} = 0$ and assign the smaller switching angles to the low-voltage SMs and the larger switching angles to the high-voltage SMs, as shown in Fig. 5.17 (a). In this way, the SM capacitors can be charged at one switching cycle and discharged at the next cycle, as shown in Fig. 5.18. Therefore, the capacitor voltage ripple can be reduced.

For the NLC modulation, the SM capacitor is charged at either smaller or larger switching angle dependent on the phase-shift angle Φ, as shown in Fig. 5.3. The proposed method performs the conventional sorting algorithm at $N_{\text{insert}} = 0$, as shown in Fig. 5.17 (b). When the phase-shift angle (Φ) is positive, for the primary-side MMC, the SMs with the lowest voltages are inserted at first since the SM capacitors are charged at the smaller switching angles. While the SMs with the highest voltages are inserted at first when Φ is negative.

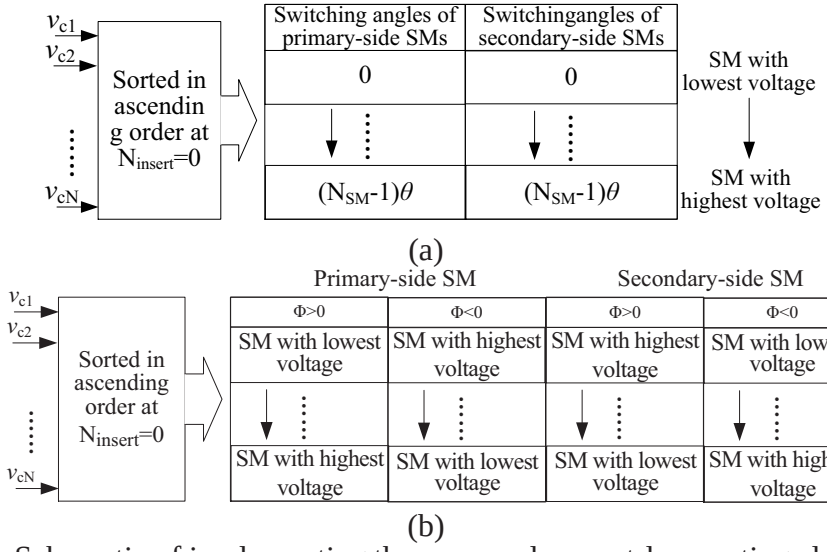


Figure 5.17. Schematic of implementing the proposed current-less sorting algorithm based on: (a) the PS modulation, and (b) the NLC modulation.

For the secondary-side MMC, the pattern is reversed. In this way, the proposed current-less sorting algorithm does not need to measure the arm-current direction so that there is no additional switching action. Moreover, the SM capacitors can be charged and discharged cycle by cycle, and then the capacitor voltage ripple is reduced, as shown in Fig. 5.19.

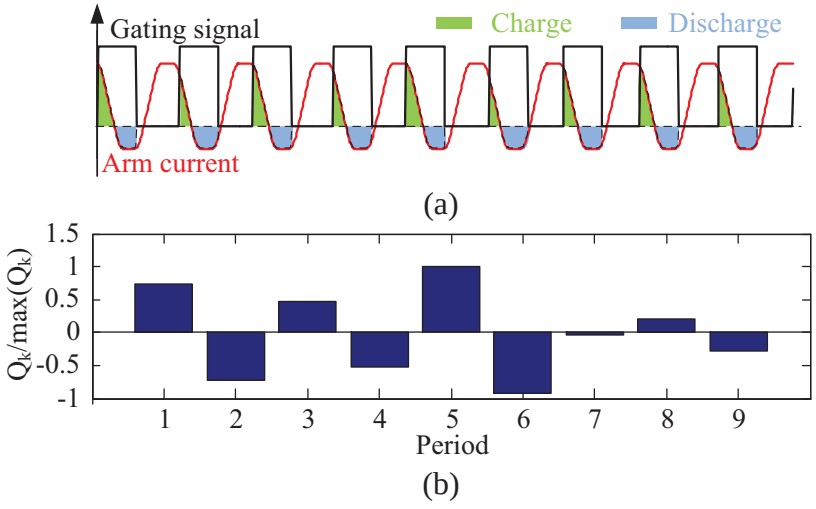


Figure 5.18. Charging and discharging performance of the primary-side MMC based on the proposed current-less sorting algorithm with the PS modulation: (a) gating signal and arm current, and (b) capacitor charges.

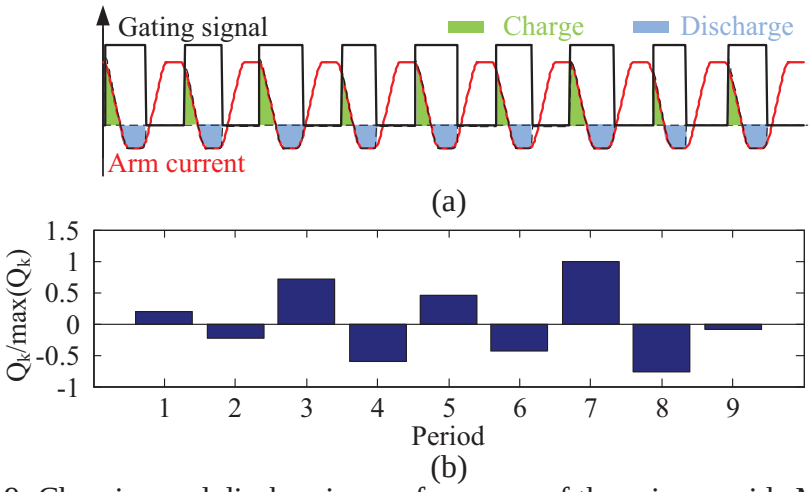


Figure 5.19. Charging and discharging performance of the primary-side MMC based on the proposed current-less sorting algorithm with the NLC modulation: (a) gating signal and arm current, and (b) capacitor charges.

5.4 Simulation and Experimental Verification

5.4.1 Simulation Results

To verify and evaluate the performances of various voltage-balancing algorithms, an IM2DC is built in PSCAD simulation environment based on the parameters listed in Table 5.1. The phase-shift angle Φ is fixed at $\pi/2$, while fixing the ramping angle (θ_R) at $\pi/2$.

Figure 5.20 shows the capacitor voltages of the primary-side MMC based on the conventional sorting algorithm. When N_{insert} reaches to zero, the capacitors are sorted by voltage in the ascending order. The capacitor voltages are well balanced with little low-frequency ripple.

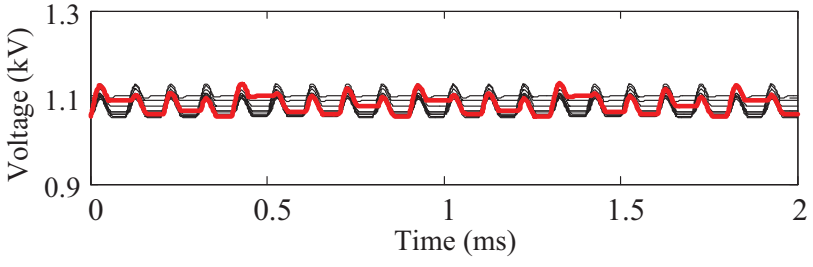


Figure 5.20. Capacitor voltages of the primary-side MMC based on the conventional sorting algorithm.

Figure 5.21 shows the capacitor voltages of the primary-side MMC based on the PS modulation, which are corresponding to different voltage-balancing algorithms. From Fig. 5.21, the single-step alternating voltage-balancing algorithm leads to the low-frequency ripple of capacitor voltage. For the proposed multi-step alternating voltage-balancing algorithm, the low-frequency capacitor voltage ripple is significantly reduced. For the proposed current-less sorting algorithm, the low-frequency ripple can be further reduced, which has the similar performance with the conventional sorting algorithm.

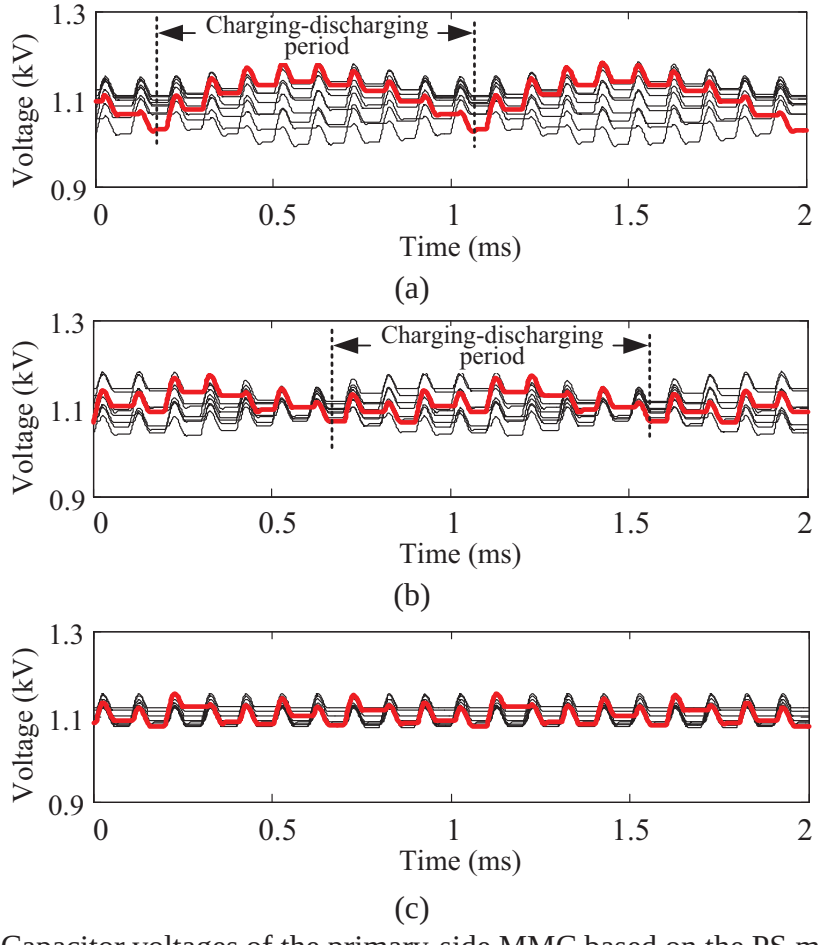


Figure 5.21. Capacitor voltages of the primary-side MMC based on the PS modulation: (a) the single-step alternating voltage-balancing algorithm, (b) the proposed multi-step alternating voltage-balancing algorithm, and (c) the proposed current-less sorting algorithm.

Figure 5.22 shows the capacitor voltages of the primary-side MMC based on the NLC modulation. The proposed multi-step alternating voltage-balancing algorithm and current-less sorting algorithm can significantly reduce the low-frequency ripple while keeping capacitor voltages balanced.

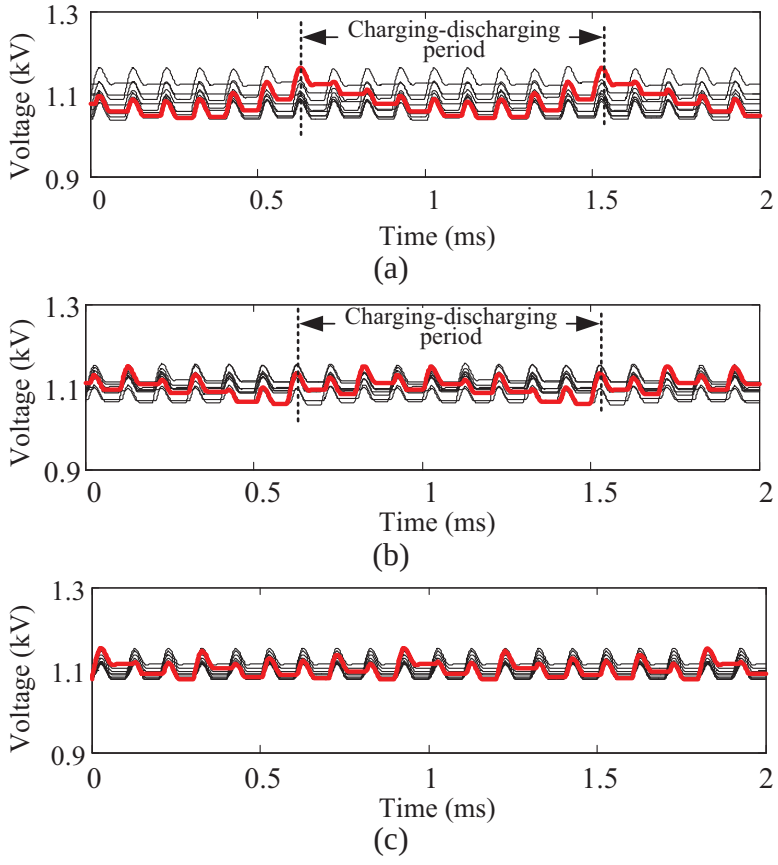


Figure 5.22. Capacitor voltages of the primary-side MMC based on the NLC modulation: (a) the single-step alternating voltage-balancing algorithm, (b) the proposed multi-step alternating voltage-balancing algorithm, and (c) the proposed current-less sorting algorithm.

The FFT spectrum of capacitor voltages are shown in Fig. 5.23 for different voltage-balancing algorithms and modulation strategies. The single-step alternating algorithm leads to large low-frequency ripple and its frequency is determined by $\frac{f_{ac}}{N_{\mathrm{SM}}} = 1.11$ kHz, where the fundamental frequency of ac–link voltage is $f_{ac} = 10$ kHz and the number of SMs per arm is $N_{\mathrm{SM}} = 9$. When employing other voltage-balancing algorithms, the low-frequency

ripple can be reduced, which demonstrates the aforementioned analysis. When increasing the N_{SM} to 20, the low-frequency voltage ripple further increases at 0.5 kHz, as shown in Fig. 5.23 (c).

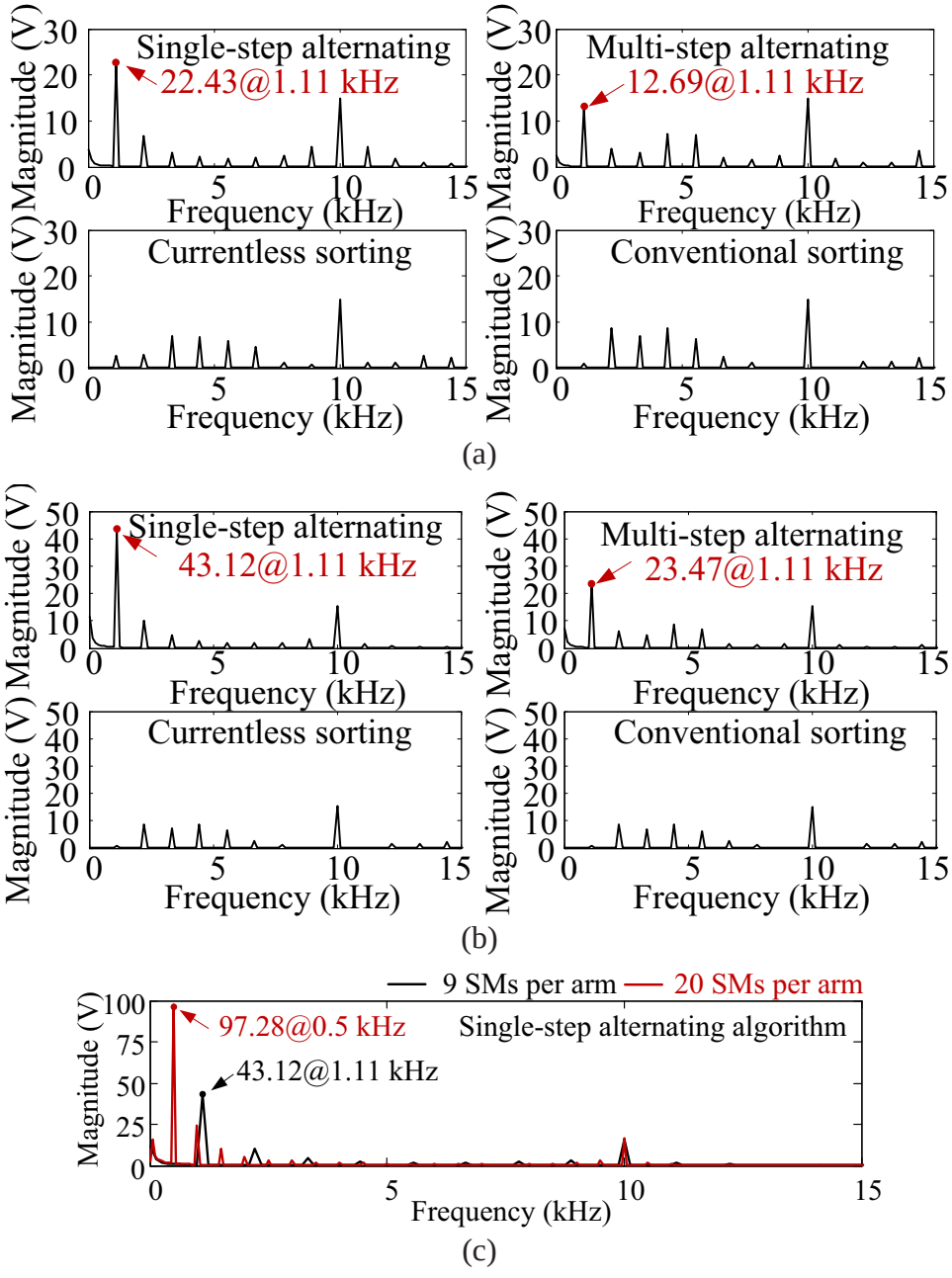
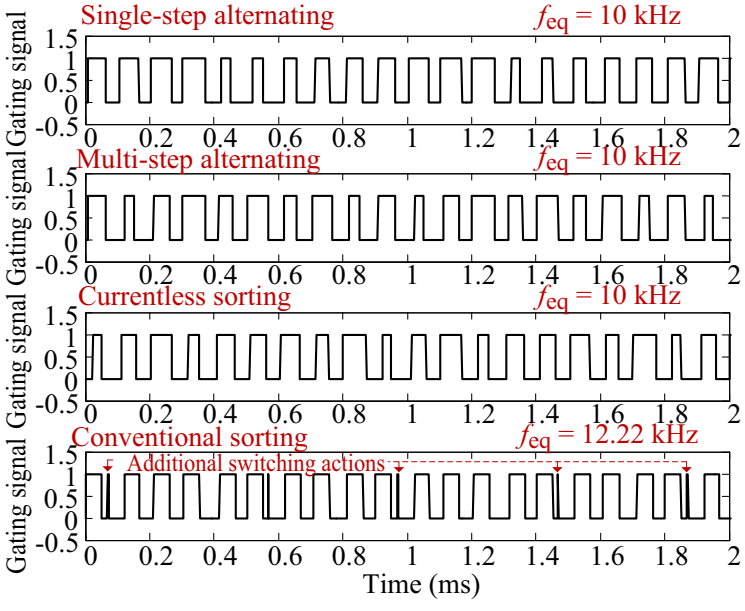
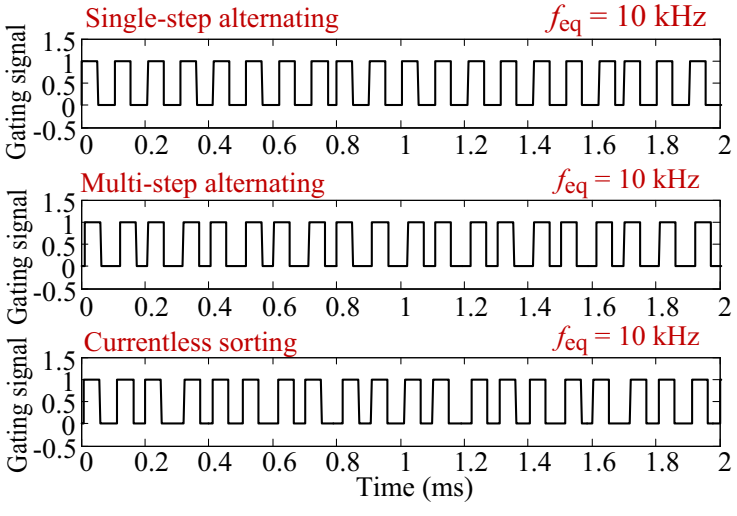


Figure 5.23. Spectrum of capacitor voltage based on: (a) the NLC modulation, (b) the PS modulation, and (c) different number of SMs per arm.

The SM gating signals as well as the equivalent switching frequency (f_{eq}) for various voltage-balancing algorithms and modulation methods are shown in Fig. 5.24. Based on Fig. 5.24, the conventional sorting algorithm has more switching actions than the others. In addition, the Infineon FF150R12RT4 is selected for the simulation model to estimate the conduction loss and switching loss. The estimated power losses are listed in Table 5.2.



(a)



(b)

Figure 5.24. Gating signals based on: (a) the NLC modulation, and (b) the PS modulation.

Table 5.2
Switching Frequency and Semiconductor Losses of the Simulation System Based on Different Modulation Strategies and Voltage-Balancing Algorithms

Modulation	**Balancing algorithm**	**Switching frequency**	$P_{\mathbf{SW}}$ **(kW)**	$P_{\mathbf{con}}$ **(kW)**
NLC	Single-step alternating	10 kHz	12.75	5.28
	Multi-step alternating	10 kHz	12.82	5.28
	Currentless sorting	10 kHz	12.94	5.28
	Conventional sorting	12.22 kHz	13.42	5.29
PS	Single-step alternating	10 kHz	13.13	5.37
	Multi-step alternating	10 kHz	12.92	5.35
	Currentless sorting	10kHz	12.98	5.36

P_{SW} is the switching loss of semiconductor devices;
P_{con} is the conduction loss of semiconductor devices.

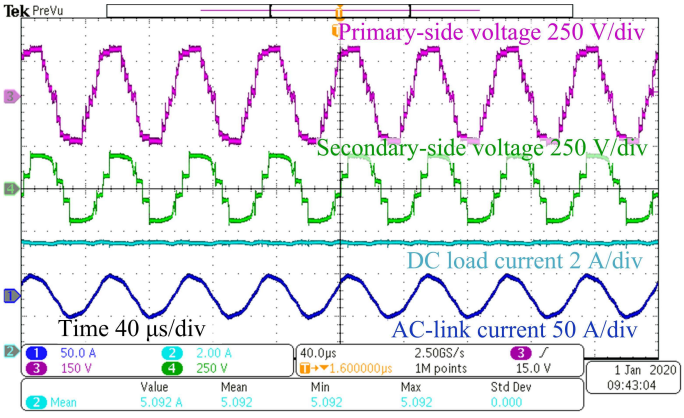
Based on Table 5.2, the conventional sorting algorithm has the highest switching loss due to the additional switching actions.

5.4.2 Experimental Results

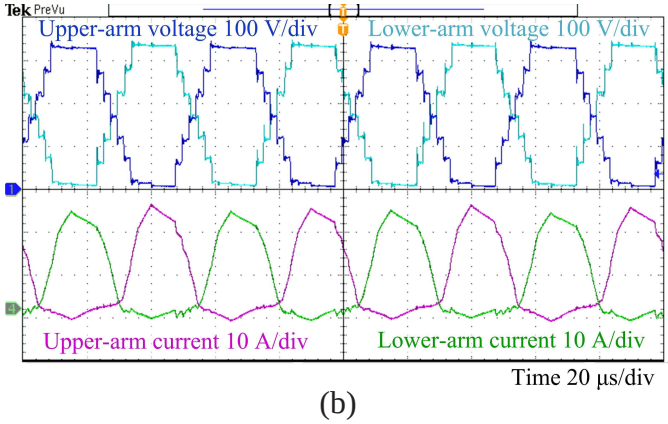
An experimental prototype of the single-phase MMC-based dc-dc transformer is built to verify the effectiveness of the proposed methods, as shown in Fig. 4.9. Its parameters are listed in Table 4.5. The ramping angle is fixed at $\theta_{\mathrm{R}} = \pi/2$.

Figure 5.25 shows the ac-link voltages, ac-link current, arm voltages, and arm currents. The phase-shift angle between the primary-side voltage and secondary-side voltage is $\Phi = \pi/2$.

Figure 5.26 shows the arm voltage, SM output voltage, capacitor voltages of the upper arm based on the conventional sorting algorithm. According to Fig. 5.26, the capacitor voltages are well balanced with low ripple but additional switching actions.



(a)



(b)

Figure 5.25. Experimental results of the single-phase MMC-based dc-dc transformer: (a) the primary- and secondary-side ac-link voltages, dc load current, and ac-link current (from top to bottom), and (b) the primary-side arm voltages and current.

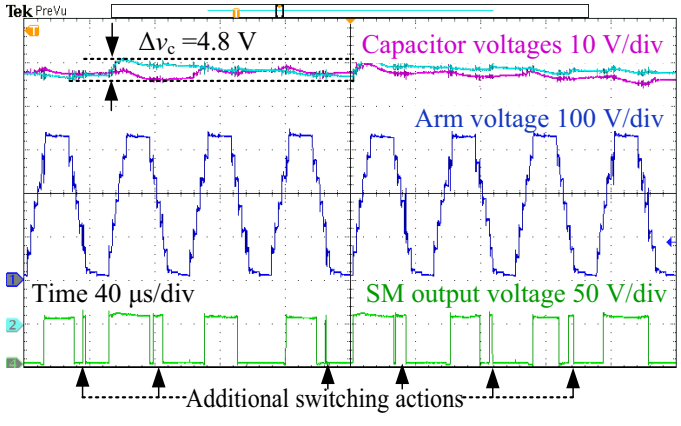


Figure 5.26. Experimental results of the conventional sorting algorithm: the capacitor voltages, arm voltage, and SM output voltage (from top to bottom).

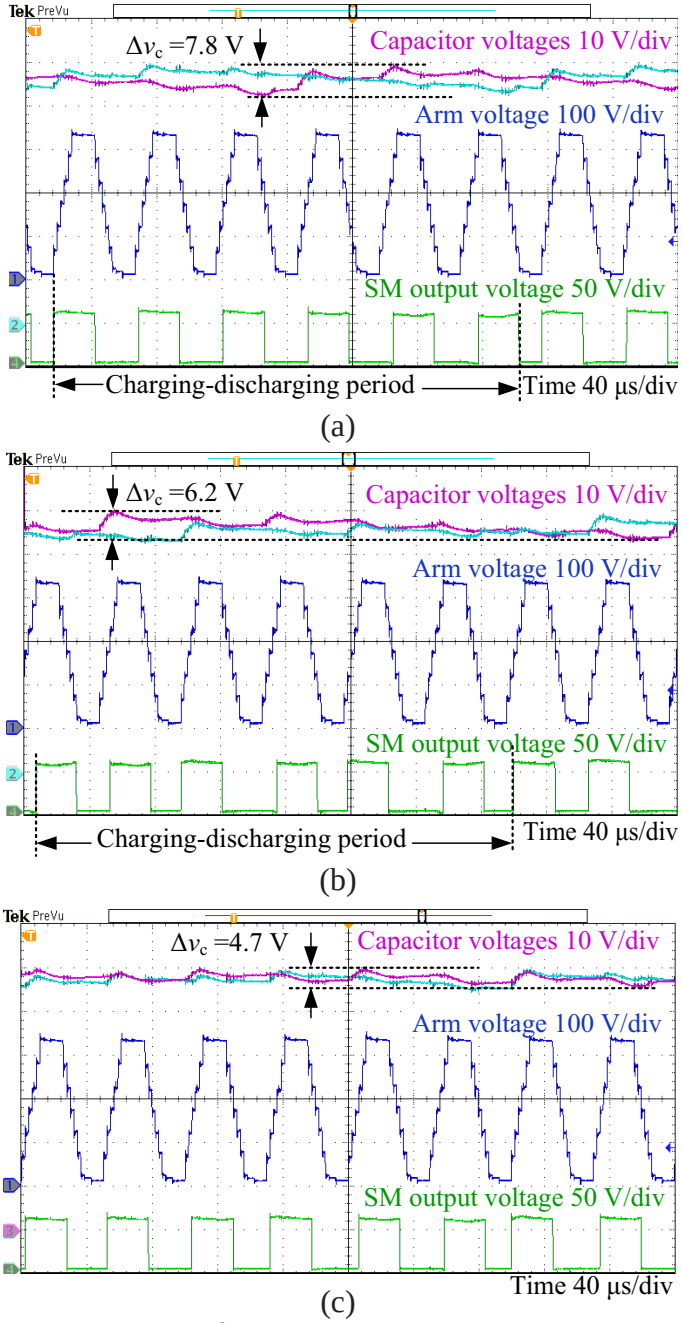
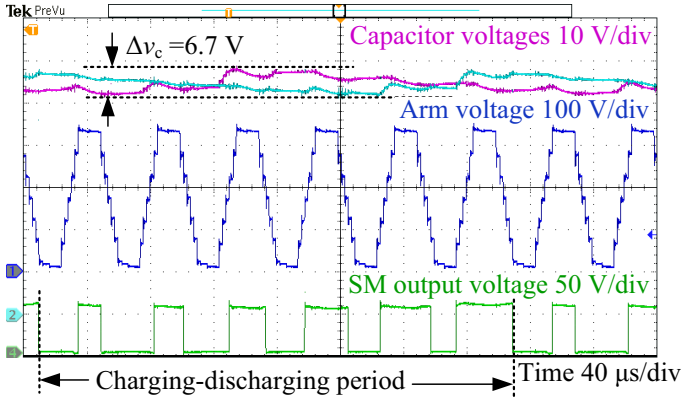
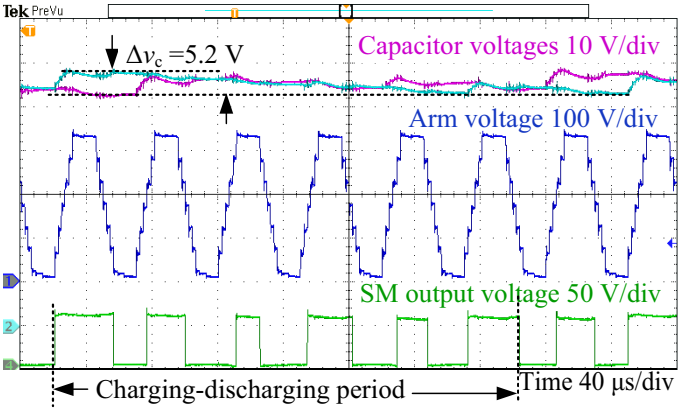


Figure 5.27. Experimental results of capacitor voltages based on the PS modulation: (a) the single-step alternating voltage-balancing algorithm, (b) the proposed multi-step alternating voltage-balancing algorithm, and (c) the proposed current-less sorting algorithm.

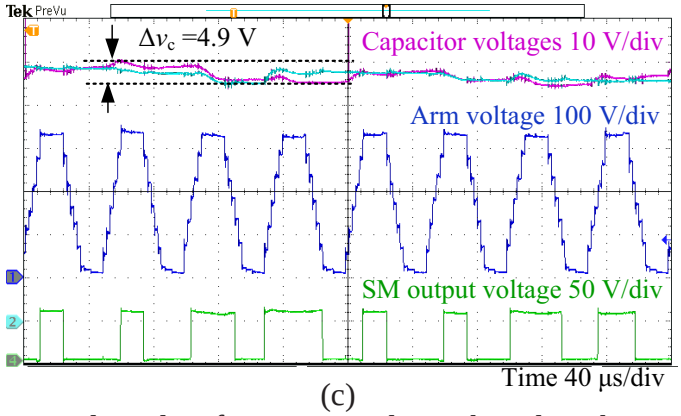
Figures 5.27 and 5.28 show the experimental results of the upper-arm voltages, SM output voltages, and capacitor voltages based on the PS and NLC modulation methods, re-



(a)



(b)



(c)

Figure 5.28. Experimental results of capacitor voltages based on the NLC modulation: (a) the single-step alternating voltage-balancing algorithm, (b) the proposed multi-step alternating voltage-balancing algorithm, and (c) the proposed current-less sorting algorithm.

spectively. Based on the experimental results, the single-step alternating voltage-balancing algorithm leads to the low-frequency ripple of capacitor voltage. While the proposed multi-step alternating voltage-balancing algorithm and current-less sorting algorithm can significantly reduce the voltage ripple. Figure 5.29 shows and compares the capacitor charges from the experimental test and the mathematical model. The proposed methods ensure to charge and discharge the capacitors cycle by cycle so that the continuous charging or discharging as well as the low-frequency ripple can be avoided, as shown in Fig. 5.30.

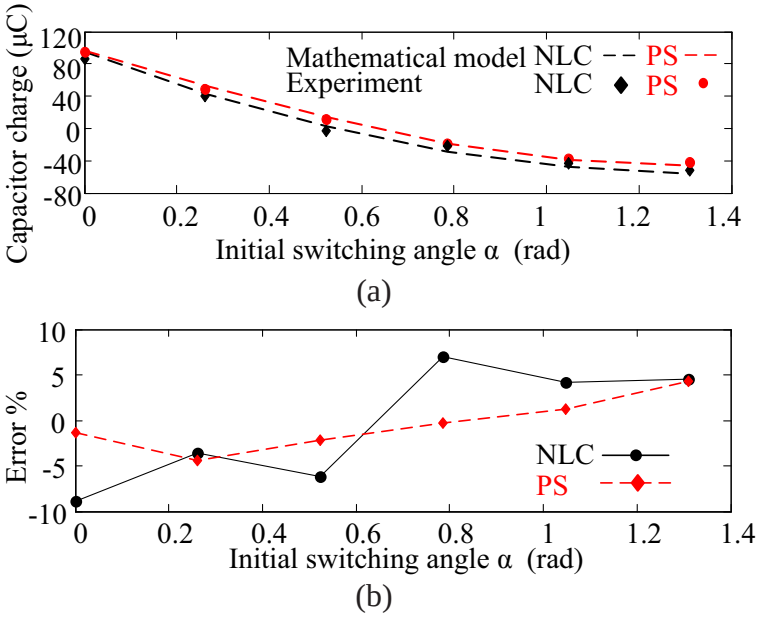


Figure 5.29. Error of capacitor charges based on the mathematical model and experimental test: (a) capacitor charges, and (b) errors of the capacitor charges.

Figure 5.31 shows the Fourier spectrum of capacitor voltages for various modulations and voltage-balancing algorithms based on the simulation and experimental studies. Comparing with the single-step alternating voltage-balancing algorithm, the proposed two methods can significantly reduce the low-order harmonics in the capacitor voltages. Furthermore, the proposed current-less sorting algorithm with the NLC modulation has the best performance in reducing the low-frequency ripple without introducing the additional switching loss.

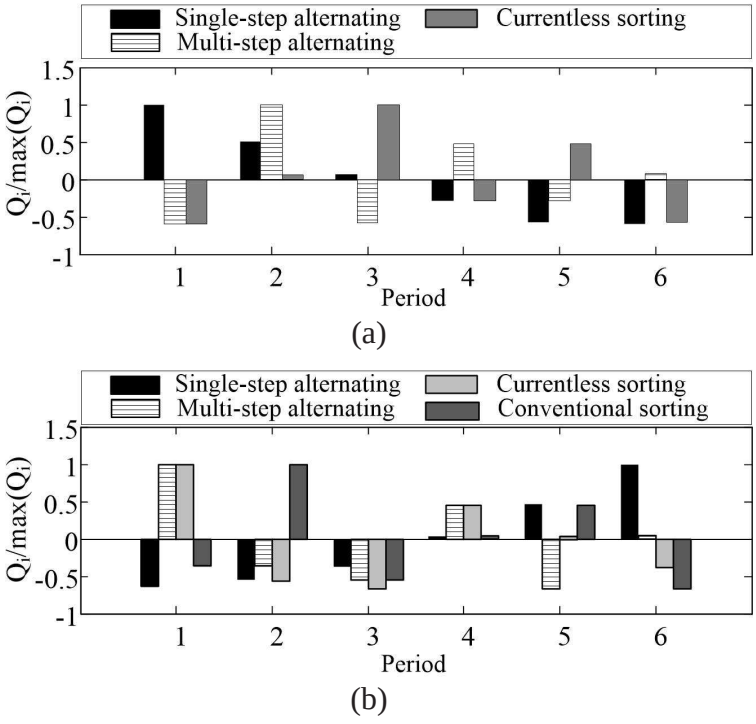


Figure 5.30. Capacitor charges based on: (a) the PS modulation, and (b) the NLC modulation.

Based on the experimental test, the equivalent switching frequencies and power losses for different modulation strategies and voltage-balancing algorithms are measured and shown in Table 5.3. As shown in Table 5.3 and Fig. 5.26, the conventional sorting algorithm has the additional switching actions and, consequently, the highest power losses as compared to other methods. The power loss is measured by WT500 power analyzer. The primary-side dc voltage and dc current are measured to obtain the primary-side dc power. The primary-side ac-link voltage and ac-link current are measured to obtain the average power at the ac side. Therefore, the power losses can be obtained by evaluating the difference between the measured dc-side power and ac-side power, which include semiconductor losses, arm inductor loss, SM capacitor loss, and filter capacitor loss. Since the dc/ac voltages and currents are very similar due to the same operating condition, the losses of arm inductor and filter capacitor are similar for different voltage-balancing algorithms. The SM capacitor loss is negligible due to the application of film capacitors with negligible equiva-

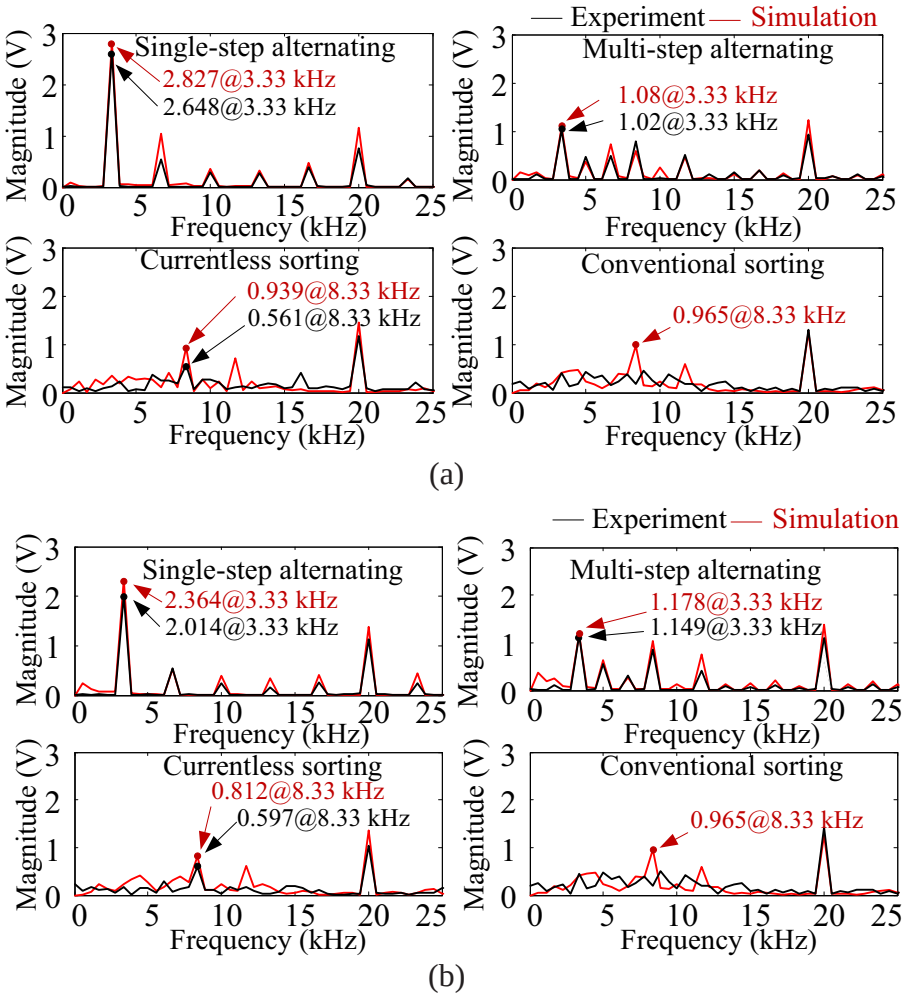


Figure 5.31. FFT spectrum of capacitor voltage based on : (a) the PS modulation, and (b) the NLC modulation.

lent series resistances (ESRs). Therefore, the differences of power losses between different algorithms are mainly caused by the switching loss of semiconductor devices.

5.5 Conclusion

This chapter investigated modulation methods and voltage-balancing algorithms of the MMC under medium-frequency operations for SST applications. The performance of various methods/algorithms is evaluated and compared theoretically and experimentally. Based on the analytical and experimental results, the existing single-step alternating voltage-

Table 5.3
Switching Frequency and Power Losses for Different Modulation Strategies and Voltage-Balancing Algorithms Based on the Experimental Test

Modulation	**Balancing algorithm**	**Switching frequency**	**Power loss (W)**
NLC	Single-step alternating	20 kHz	264.3
	Multi-step alternating	20 kHz	263.8
	Currentless sorting	20 kHz	264.9
	Conventional sorting	27.5 kHz	274.2
PS	Single-step alternating	20 kHz	262.2
	Multi-step alternating	20 kHz	260.2
	Currentless sorting	20kHz	260.8

balancing algorithm leads to a low-frequency capacitor voltage ripple and this issue will become worse when the number of SMs increases. While the conventional sorting algorithm has much smaller voltage ripple but introducing the additional switching actions as well as more switching loss. To reduce the low-frequency voltage ripple and avoid the additional switching actions and loss, two new voltage-balancing algorithms are proposed and investigated, i.e, the multi-step alternating voltage-balancing algorithm and the current-less sorting algorithm. The study results demonstrate satisfactory performance of the proposed capacitor voltage-balancing algorithms. Among the evaluated methods/algorithms, the proposed current-less sorting algorithm with the NLC modulation has the best performance in terms of reducing the voltage ripple and avoiding the additional switching actions.

Chapter 6

OPTIMAL DESIGN OF MODULAR MULTILEVEL CONVERTER FOR MMC-BASED SSTS

In this chapter, a procedure is developed for optimal design of the MMC under medium-frequency operation for SST applications. There are several free system parameters and circuit parameters providing more flexibilities for optimal design, which include frequency (f_{ac}) and ramping angle (θ_{R}) of ac-link voltage, and number of SMs per arm (N_{SM}). In addition, the modulation methods and voltage-balancing algorithms also impact the steady-state performance of the MMC-based SST.

- Number of SMs: In MMC, there are large number of SMs consisting of capacitors, semiconductor devices, and heat sinks. In this way, the volume of SM capacitors and heat sinks dominate the total volume of the MMC-based SST. In addition, due to the large number of semiconductor devices, the semiconductor losses might dominate the overall power loss of the MMC-based SST. Thus, the N_{SM} greatly influences design of MMC.

- Frequency of ac-link current: Theoretically, by increasing ac-link frequency, the SM capacitance and arm inductance are reduced, while the semiconductor losses and core loss of arm inductor are increased. In this way, by reducing SM capacitance, the volume of capacitor can be reduced. However, the increased semiconductor loss requires large heat sink to limit the maximum junction temperature.

- Ramping angle of ac-link voltage: By increasing θ_{R}, it avoids high dv/dt of ac-link transformer. However, it reduces the RMS value of ac-link voltage, hence increases

ac-link current. It will increase power loss of SM capacitor, conduction losses of semiconductor devices, and winding loss of arm inductor.

Thus, in this chapter, the impacts of free parameters are investigated for the optimal design of the MMC-based SST.

6.1 Overview of Optimal Design Procedure

In Section 4.2, a modified mathematical model has been developed for optimal design of the MMC-based SST, which considers the circuit parameter design of MMC. Figure 6.1 shows the optimal design procedure of the MMC-based SST based on the proposed modified mathematical model.

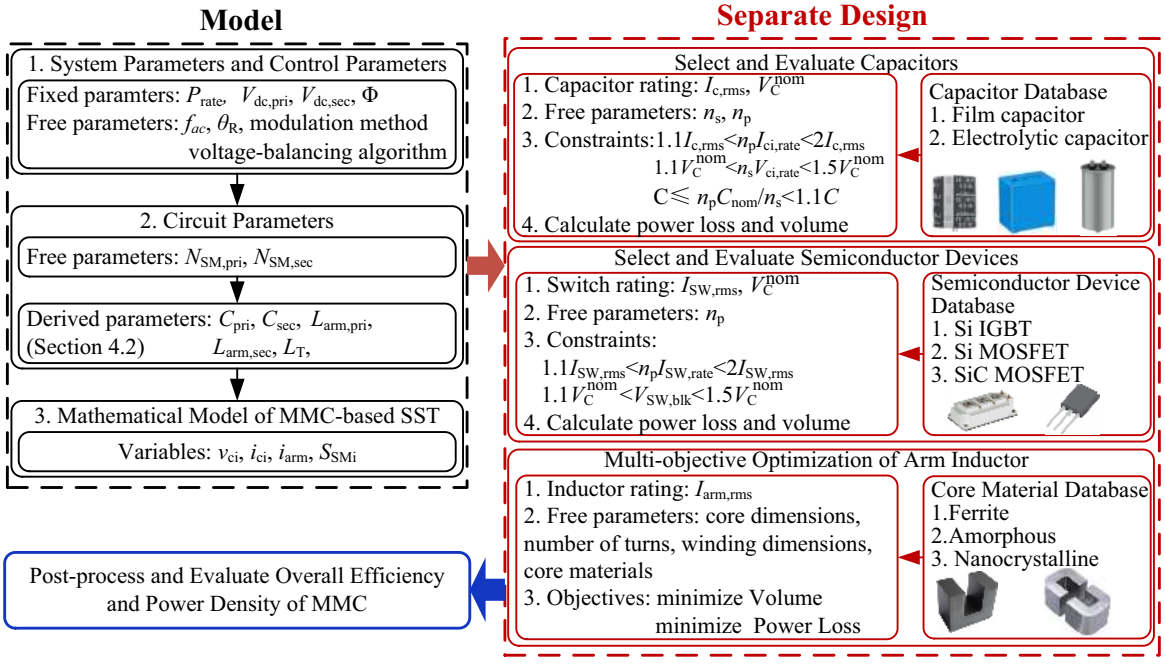


Figure 6.1. The flowchart of optimal design of MMC-based SST.

Firstly, all state variables are solved by the mathematical model based on system requirements. Then, the rated voltages and currents of main circuit components (including SM capacitors, arm inductors, and semiconductor devices) are derived from arm current, gating signals, and capacitor voltages. Based on design criteria and constraints, the ca-

pacitors and semiconductor devices are selected from database, while the arm inductor is designed by the elitist non-dominated sorting genetic algorithm (NSGA-II). Finally, the non-dominated solutions of each design are combined to evaluate overall efficiency and power density of MMC.

6.2 Capacitor Selection

Based on analysis of Section 4.2, the SM capacitance is estimated from peak-peak ripple of capacitor charge ($\frac{\Delta Q_{\mathrm{c,pp}}}{\Delta V_{\mathrm{c,pp}}}$), where $\Delta V_{\mathrm{c,pp}}$ is 2% of the nominal SM capacitor voltage ($V_{\mathrm{C}}^{\mathrm{nom}} = \frac{V_{\mathrm{dc}}}{N_{\mathrm{SM}}}$).

The SM capacitor is constructed by combinations of n_{s} series- and n_{p} parallel-connected capacitors to reach the required capacitance and rated current, while reducing volume and power losses (resulted from ESR) to optimize the design. Both film and electrolytic capacitors are considered. The rated voltage ($n_{\mathrm{s}} V_{\mathrm{ci,rate}}$) is 1.1 to 1.5 times of the nominal SM capacitor voltage, while the current ($n_{\mathrm{p}} I_{\mathrm{ci,rate}}$) of selected capacitor is 1.1 to 2 times of RMS current of SM capacitor, where $I_{\mathrm{ci,rate}}$ is the rated current of single capacitor.

To estimate power losses of SM capacitors, the ESR is estimated by (6.1) in terms of frequency and nominal capacitance.

$$\mathrm{ESR} = \frac{\tan\delta}{\omega C}, \tag{6.1}$$

where $\tan\delta$ is tangent of loss angle, which is available from datasheet. Then, the power loss and volume are evaluated to identify the non-dominated solutions of selected capacitors.

6.3 Semiconductor Devices

When selecting IGBT and MOSFET from database, the blocking voltage ($V_{\mathrm{SW,blk}}$) ranges from 1.1 to 1.5 time of the nominal SM capacitor voltage, while the current rating ($n_p I_{\mathrm{SW,rate}}$) is 1.1 to 2 times of required RMS current of semiconductor device ($I_{\mathrm{SW,rms}}$). To reach

required current rating, the SM is constructed by combinations of n_{p} parallel-connected IGBTs/MOSFETs, where n_{p} is no more than 4.

6.3.1 Power Losses

A Power losses of IGBT

The power losses of the semiconductor devices include the conduction loss of IGBT (P_{conT}) and diode (P_{conD}), the switching loss (E_{on}, E_{off}) of IGBT, and the reverse recovery loss (E_{rec}) of diode. Based on [152], the power losses of IGBTs can be estimated based on the parameters from datasheets, which are calculated by

$$\begin{cases} P_{\mathrm{conT}} = V_{\mathrm{ce}}\left(i_c\right) \cdot i_c = \left(c_0 + c_1 \cdot i_c + c_2 \cdot i_c^2\right) \cdot i_c, \\ P_{\mathrm{conD}} = V_{\mathrm{f}}\left(i_f\right) \cdot i_f = \left(d_0 + d_1 \cdot i_f + d_2 \cdot i_f^2\right) \cdot i_f, \end{cases} \tag{6.2}$$

$$\begin{cases} E_{\mathrm{on}} = \left(a_{\mathrm{on0}} + a_{\mathrm{on1}} \cdot i_c + a_{\mathrm{on2}} \cdot i_c^2\right) \frac{V_{\mathrm{C}}^{\mathrm{nom}}}{V_{\mathrm{CEN}}}, \\ E_{\mathrm{off}} = \left(a_{\mathrm{off0}} + a_{\mathrm{off1}} \cdot i_c + a_{\mathrm{off2}} \cdot i_c^2\right) \frac{V_{\mathrm{C}}^{\mathrm{nom}}}{V_{\mathrm{CEN}}}, \\ E_{\mathrm{rec}} = \left(a_{\mathrm{rec0}} + a_{\mathrm{rec1}} \cdot i_f + a_{\mathrm{rec2}} \cdot i_f^2\right) \frac{V_{\mathrm{C}}^{\mathrm{nom}}}{V_{\mathrm{CEN}}}, \end{cases} \tag{6.3}$$

where V_{ce} is the on-state collector-emitter voltage of IGBT; V_{f} is the forward voltage drop of anti-paralleled diode; the collector current (i_c) and free-wheeling diode current (i_f) are derived from the arm current and switching function; V_{CEN} is the rated V_{ce} under test condition; the coefficients $c_0 \sim c_2$, $d_0 \sim d_2$, $a_{\mathrm{on0}} \sim a_{\mathrm{on2}}$, $a_{\mathrm{off0}} \sim a_{\mathrm{off2}}$, and $a_{\mathrm{rec0}} \sim a_{\mathrm{rec2}}$ are extracted from datasheets using the curve fitting method.

B Power Losses of MOSFET

For MOSFET, equation (6.2) is still applicable for estimating conduction loss of MOSFET. However, most datasheets do not provide curves of E_{on}, E_{off}, and E_{rec}. Thus, the switching losses should be estimated from rise- and fall-time of current and drain-source

voltage (t_{ri}, t_{ru}, t_{fi}, t_{fu}), which are determined by drain-source voltage and gate-driver circuit parameters, including gate resistance R_g, gate threshold voltage $V_{\text{gs,th}}$, gate plateau voltage $V_{\text{gs,plat}}$, the on-state and off-state gate-driver voltages $V_{\text{dr,on}}$ and $V_{\text{dr,off}}$, MOSFET input capacitance C_{iss}, and MOSFET gate-drain capacitance C_{gd}. The MOSFET input capacitance C_{iss} is defined as the sum of gate-source capacitance and gate-drain capacitance ($C_{gs} + C_{gd}$) [153–155]. The E_{rec} of body diode is estimated by $Q_{rr}V_{\text{ds,off}}$, where Q_{rr} can be obtained from datasheet [154, 156].

$$\begin{cases} t_{ru} = & (V_{\text{ds,off}} - V_{\text{ds,on}})\dfrac{R_g C_{gd}}{V_{\text{gs,plat}} - V_{\text{dr,off}}}, \\ t_{fu} = & (V_{\text{ds,off}} - V_{\text{ds,on}})\dfrac{R_g C_{gd}}{V_{\text{dr,on}} - V_{\text{gs,plat}}}, \end{cases} \tag{6.4}$$

where $V_{\text{ds,off}}$ equals to nominal SM capacitor voltage.

$$\begin{cases} t_{ri} = & R_g C_{\text{iss}} \ln\left(\dfrac{V_{\text{dr,on}} - V_{\text{gs,th}}}{V_{\text{dr,on}} - V_{\text{gs,plat}}}\right), \\ t_{fi} = & R_g C_{\text{iss}} \ln\left(\dfrac{V_{\text{dr,off}} - V_{\text{gs,plat}}}{V_{\text{dr,off}} - V_{\text{gs,th}}}\right). \end{cases} \tag{6.5}$$

Then, the turn-on and turn-off energy are estimated as:

$$\begin{cases} E_{\text{on}} = & V_{\text{ds,off}} I_{\text{ds}} \dfrac{t_{ri} + t_{fu}}{2}, \\ E_{\text{off}} = & V_{\text{ds,off}} I_{\text{ds}} \dfrac{t_{fi} + t_{ru}}{2}, \\ E_{\text{rec}} = & Q_{rr} V_{\text{ds,off}}. \end{cases} \tag{6.6}$$

6.3.2 Thermal Analysis and Volume of Heat Sink

Based on the analysis proposed in [157, 158], the heat-sink volume can be estimated from its thermal resistance, as expressed in (6.7), where the cooling system performance index (CSPI) is assumed to be 3.0 (natural air cooling), V_{hs} is the estimated volume of heat sink. In this way, to estimate the volume of heat sink, the thermal resistance of heat sink should be estimated based on thermal analysis. In this chapter, an HB SM is assumed to be

mounted on one heat sink. The total loss of an HB SM is calculated to estimate the thermal resistance of heat sink. The ambient temperature is set as 40 °C.

$$V_{\text{hs}}\,[\text{litre}] = \frac{1}{R_{hs}\left[\frac{\text{K}}{\text{W}}\right]\text{CSPI}\left[\frac{\text{W}}{\text{K}\cdot\text{litre}}\right]}, \tag{6.7}$$

The thermal model of IGBT/MOSFET has been investigated in [159, 160], which is shown in Fig. 6.2. The thermal resistance of heat sink is determined by allowable heat sink temperature, which can be derived from semiconductor loss and maximum junction temperature. The maximum junction temperature is obtained from manufacturer datasheet of semiconductor devices.

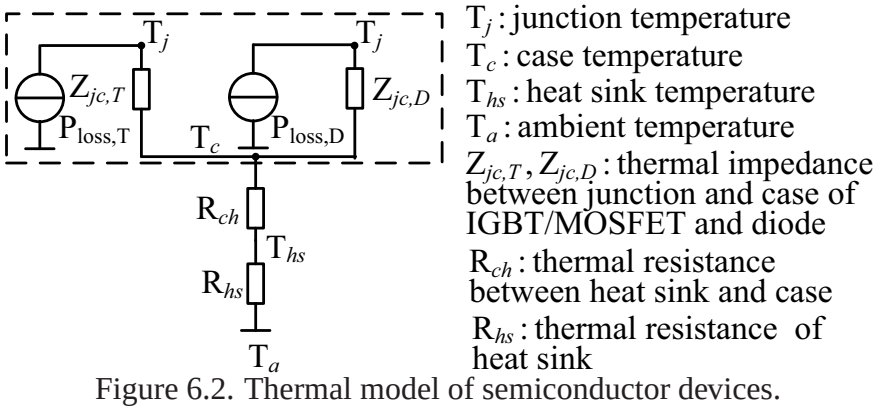


Figure 6.2. Thermal model of semiconductor devices.

$$T_{hs} = T_a + P_{loss}R_{hs}, \tag{6.8}$$

where P_{loss} is the power loss of a single semiconductor device. To determine the maximum R_{hs}, the maximum surface temperature of heat sink is estimated as:

$$T_{\text{hs,max}} = T_{\text{j,max}} - P_{\text{loss}}R_{\text{ch}} - \max\left\{P_{\text{loss,T}}Z_{\text{jc,T}}, P_{\text{loss,D}}Z_{\text{jc,D}}\right\}, \tag{6.9}$$

where $Z_{\text{jc,T}}$ and $Z_{\text{jc,D}}$ are junction-case thermal impedances of IGBT/MOSFET and body diode; R_{ch} is thermal resistance of thermal pad or thermal grease. Similarly, the power loss of semiconductor device P_{loss} can also be divided into power loss of IGBT/MOSFET $P_{\text{loss,T}}$ and that of body diode $P_{\text{loss,D}}$.

The dynamic variation of junction temperature is considered for thermal analysis [160, 161].

$$\begin{cases} \Delta T_j(t_{n-1}) = & P_{\text{loss}}(t_{n-1}) \sum R_{\text{th,i}} \left(1 - e^{-\frac{\Delta t}{\tau_{\text{th,i}}}}\right), \\ \Delta T_j(t_n) = & \sum \Delta T_j(t_{n-1}) e^{-\frac{\Delta t}{\tau_{\text{th,i}}}} + P_{\text{loss}}(t_n) \sum R_{\text{th,i}} \left(1 - e^{-\frac{\Delta t}{\tau_{\text{th,i}}}}\right), \end{cases} \tag{6.10}$$

where $R_{\text{th,i}}$ and $\tau_{\text{th,i}}$ are thermal resistance and time constant corresponding to the i^{th} element of chain-type thermal equivalent circuit (Foster network), which can be found from datasheet of semiconductor devices.

6.4 Arm Inductor Design

Based on the NSGA-II, the detailed multi-objective optimization procedure has been developed for dc inductor in [162]. In this section, similar design procedure is employed for designing arm inductor of the MMC-based SST. To formulate problem, firstly, the geometry of arm inductor is defined, and the magnetic equivalent circuit (MEC) is developed based on defined dimensions. Then, the winding loss and core loss are analyzed separately. Finally, an overview of design procedure is presented.

6.4.1 Geometry and Magnetic Equivalent Circuit of Inductor

In this section, the UI core is selected for arm inductor, as illustrated in Fig. 6.3. According to analysis in [162], its MEC is shown in Fig. 6.4, which can be solved by numerical method. The reluctances are defined as:

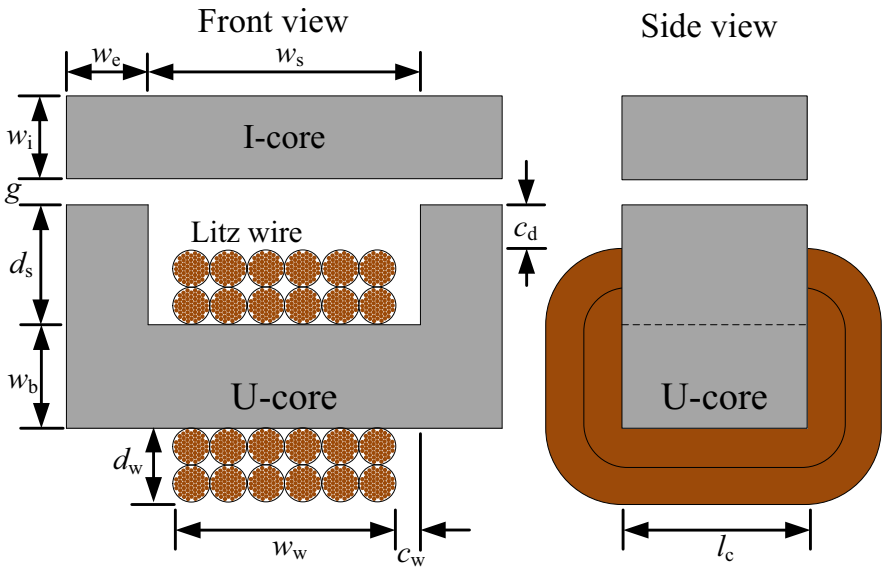


Figure 6.3. The architecture of UI-core inductor.

$$\begin{cases} R_{ic}(B_{ic}) = \dfrac{w_s + w_e}{w_i l_c \mu_0 \mu_r(B_{ic})}, \\ R_{buc}(B_{buc}) = \dfrac{w_s + w_e}{w_b l_c \mu_0 \mu_r(B_{buc})}, \\ R_{luc}(B_{luc}) = \dfrac{2d_s + w_b}{2w_e l_c \mu_0 \mu_r(B_{luc})}, \\ R_{gap} = \dfrac{g}{w_e l_c \mu_0}, \end{cases} \tag{6.11}$$

where R_{ic} is reluctance of I-core, R_{buc} is reluctance of base of U-core, R_{luc} is reluctance of a leg of U-core, R_{gap} is reluctance of air gap, μ_0 is the permeability of free space ($\mu_0 = 4\pi \times 10^{-7}$ H/m). In addition, reference [162] analyzed a more detailed MEC of UI-core by considering fringing flux and leakage flux linkage, which is not repeated in this section.

The volume of UI-core inductor is estimated by sum of core volume ($\mathrm{Vol_{core}}$) and volume of winding coil ($\mathrm{Vol_{wind}}$) laying outside of magnetic core, which is expressed as

$$\begin{aligned} \mathrm{Vol_{tot}} &= \mathrm{Vol_{core}} + \mathrm{Vol_{wind}} \\ &= [(w_\mathrm{i} + w_\mathrm{b})(w_\mathrm{s} + 2w_\mathrm{e}) + 2d_\mathrm{s}w_\mathrm{e}]\, l_\mathrm{c} + w_\mathrm{w} d_\mathrm{w}(\pi d_\mathrm{w} + l_\mathrm{c} + 2w_\mathrm{b}). \end{aligned} \tag{6.12}$$

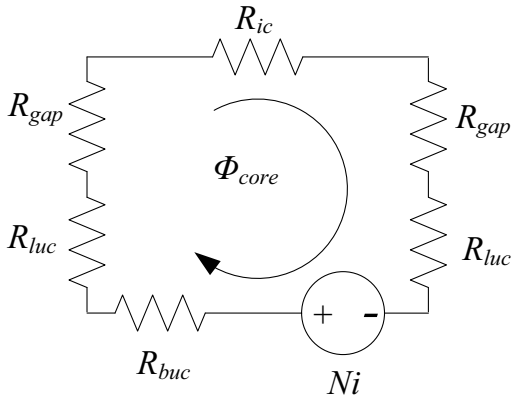


Figure 6.4. The magnetic equivalent circuit of UI-core inductor.

6.4.2 Winding Loss

In this section, when constructing arm inductor, the multi-strand wire or litz wire is considered. The essential dimensions of litz wire include cross-sectional area of single stand, number of strands, outer diameter, and length of lay (also known as pitch length).

A DC winding resistance and loss

To estimate dc resistance, the length of bundled wire is derived from UI-core dimensions, which is expressed as (6.13) [162].

$$l_{\text{wire}} = \frac{w_{\text{w}} d_{\text{w}} (\pi d_{\text{w}} + 2l_{\text{c}} + 2w_{\text{b}}) k_{\text{pf}}}{A_{\text{wire}}} = (\pi d_{\text{w}} + 2l_{\text{c}} + 2w_{\text{b}}) N_{\text{turn}}, \tag{6.13}$$

where k_{pf} and N_{turn} are packing factor and number of turns of winding coil, A_{wire} is cross-sectional area of bundled wire. The k_{pf} is defined as $\frac{N_{\text{turn}} A_{\text{wire}}}{w_{\text{w}} d_{\text{w}}}$.

To estimate A_{wire}, according to suggestions of litz wire manufacturer, the outer diameter of unserved litz wire (d_{wire}) is estimated from diameter of single strand (d_{str}) and number of strands (N_{str}) by $k_{\text{p}} \sqrt{N_{\text{str}}} d_{\text{str}}$, where k_{p} is the packing factor of litz wire. The k_{p} typically ranges from 1.25 to 1.28 depending on N_{str} [163].

As shown in Fig. 6.5, the single strand is similar to a helical coil. In this way, the length of single strand is longer than the length of bundled litz wire, which leads to increasing of

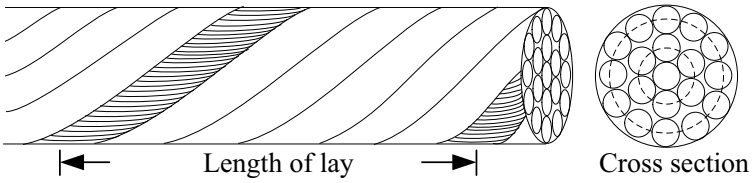


Figure 6.5. Diagram of litz wire.

dc winding resistance. To estimate the length of single strand, the length of lay describes the distance which a single wire needs for one complete rotation around the litz wire circumference [164]. In this section, the length of lay is estimated by $N_{\mathrm{str}}d_{\mathrm{str}}$. When assuming the length of bundled litz wire is l_{wire}, the length of single strand is estimated by (6.14) [165].

$$\begin{cases} l_{\mathrm{str}} = l_{\mathrm{litz}}, & N_{\mathrm{str}} = 1, \\ l_{\mathrm{str}} = \dfrac{l_{\mathrm{wire}}}{N_{\mathrm{str}}d_{\mathrm{str}}}\sqrt{(N_{\mathrm{str}}d_{\mathrm{str}})^2 + d_{\mathrm{wire}}^2}, & N_{\mathrm{str}} > 1. \end{cases} \tag{6.14}$$

Then, the dc winding resistance is expressed as

$$R_{\mathrm{wire,dc}} = \frac{l_{\mathrm{str}}}{N_{\mathrm{str}}A_{\mathrm{str}}\sigma_{\mathrm{w}}} = \frac{R_{\mathrm{str,dc}}}{N_{\mathrm{str}}}, \tag{6.15}$$

where A_{str} is cross-sectional area of single strand, σ_{w} is conductivity of conductor. The dc winding loss is calculated from dc current of inductor and dc winding resistance, which is expressed as

$$P_{\mathrm{wind,dc}} = I_{\mathrm{L,dc}}^2 R_{\mathrm{wire,dc}}, \tag{6.16}$$

where $I_{\mathrm{L,dc}}$ is dc current of inductor.

B AC winding resistance and loss

Based on analysis of [162], both skin effect and proximity effect lead to increased ac winding resistance, which can be analyzed separately.

- Skin effect: For single solid conductor or single strand of litz wire, the ac impedance caused by skin effect is estimated by (6.17) [162].

$$Z_{\mathrm{str,skin}} = -\frac{l_{\mathrm{str}}J_{\mathrm{B}}\left(\dfrac{d_{\mathrm{str}}}{2\kappa}\right)}{\pi d_{\mathrm{str}}\kappa\sigma_{\mathrm{w}}J_{\mathrm{B}}'\left(\dfrac{d_{\mathrm{str}}}{2\kappa}\right)}, \tag{6.17}$$

where J_B is Bessel function of order zero, κ is defined as $\sqrt{\frac{j}{\omega\sigma_w\mu_0}}$. Then, the ac impedance of bundled wire caused by skin effect is estimated as $Z_{wire,skin} = Z_{str,skin}/N_{str}$.

- Proximity effect: For single solid conductor, the ac resistance caused by proximity effect can be estimated by Dowell's formula [166–169]. When considering litz wire, the Dowell's formula is modified as (6.18) [170, 171].

$$F_{prox} = \frac{R_{str,prox}}{R_{str,dc}} = \Delta_{str}\frac{\sinh(2\Delta_{str}) + \sin(2\Delta_{str})}{\cosh(2\Delta_{str}) - \cos(2\Delta_{str})} + \Delta_{str}\frac{2\left(N_d^2 N_{str,lay}^2 - 1\right)}{3}\frac{\sinh(\Delta_{str}) + \sin(\Delta_{str})}{\cosh(\Delta_{str}) + \cos(\Delta_{str})} \tag{6.18}$$

  where the litz wire has multiple layers of strands and $N_{str,lay}$ is number of layers in bundled litz wire, N_d is the number of layers of winding coil. The Δ_{str} is normalized diameter respect to skin depth δ_w, which is defined as

$$\Delta_{str} = \left(\frac{\pi}{4}\right)^{0.75}\frac{d_{str}}{\delta_w}\sqrt{\eta}, \tag{6.19}$$

  where η represents the porosity factor typically ranging from 0.4 to 0.7. In this section, η is fixed at 0.7. The skin depth is estimated as $\delta_w = (\pi\mu_0\sigma_w f)^{-0.5}$.

  Then, the ac-resistance of bundled litz wire caused by proximity effect is estimated as

$$R_{wire,prox} = \frac{R_{str,dc}F_{prox}}{N_{str}} = R_{wire,dc}F_{prox}. \tag{6.20}$$

The ac winding loss is estimated from RMS value of n^{th} order harmonic and corresponding ac winding resistances caused by skin effect and proximity effect, which is expressed as

$$P_{wind,ac}(n) = I_{L,rms}^2(n)\left[R_{wire,prox}(n) + R_{wire,skin}(n)\right], \tag{6.21}$$

where $R_{wire,skin}(n)$ is ac winding resistance caused by skin effect of n^{th} order harmonic, which is real part of $Z_{wire,skin}(n)$. The $I_{L,rms}$ is RMS value of inductor current.

6.4.3 Core Loss

The improved General Steinmetz Equation (iGSE) is a popular method to estimate core loss induced from nonsinusoidal excitations, which is express as (6.22). The coefficients K_c, α, and β are obtained from datasheet.

$$P_v = \frac{1}{T}\int_0^T k_i|\Delta \mathrm{B}|^{\beta-\alpha}\left|\frac{\mathrm{dB(t)}}{\mathrm{d}t}\right|^{\alpha}\mathrm{d}t\ \frac{kW}{m^3} \tag{6.22}$$

where coefficient k_i is defined as (6.23).

$$k_i = \frac{K_c}{2^{\beta-1}\pi^{\alpha-1}\int_0^{2\pi}|\cos(\theta)|^{\alpha}\mathrm{d}\theta} \tag{6.23}$$

The core loss P_{core} is calculated by $P_v \mathrm{Vol}_{\mathrm{core}}$.

6.4.4 Optimal Design Based on Nondominated Sorting Genetic Algorithm

The optimization of arm inductor has two objectives, the minimizations of volume ($\mathrm{Vol_{tot}}$) and power loss ($\mathrm{P_{loss}}$). The NSGA-II algorithm is implemented by a MATLAB-based genetic optimization toolbox known as GOSET, which is provided by [162, 172].

$$\begin{cases} \min f_1 = \min \mathrm{Vol_{tot}}, \\ \min f_2 = \min \mathrm{P_{loss}}, \end{cases} \tag{6.24}$$

where $\mathrm{Vol_{tot}}$ can be solved by (6.12), while the total loss of design inductor is the sum of winding loss and core loss.

A Parameters for optimization

The first step of this optimization design is identifying proper free parameters. One choice of selected free parameters is listed in (6.25).

$$\text{Parameters} = \left[\mathrm{ID_{core}}\ \mathrm{ID_{cd}}\ \underbrace{g\ l_{\mathrm{c}}\ w_{\mathrm{e}}\ w_{\mathrm{i}}\ w_{\mathrm{b}}\ c_{\mathrm{d}}\ c_{\mathrm{w}}}_{\text{core dimensions}}\ \underbrace{N_{\mathrm{turn}}\ N_{\mathrm{d}}\ N_{\mathrm{w}}\ N_{\mathrm{str}}\ A_{\mathrm{str}}}_{\text{winding dimensions}}\right], \tag{6.25}$$

where $\mathrm{ID}_{\mathrm{core}}$ is the index of core material in database, $\mathrm{ID}_{\mathrm{cd}}$ is the index of conductor material, N_{w} is the number of bundled wires per layer of winding coil.

The variables are classified as:

- continuous: core dimensions are considered as continuous variables. The N_{turn}, N_{w}, N_{d}, N_{str} are regarded as continuous variables and then rounded to nearest integer [162]. The A_{str} is also a continuous variable, which is different from actual cross-sectional area of practical conductor. Hence, it is rounded to the closest available wire gauge from Standard Wire Gauge list, which determines d_{str}.

- discrete: the magnetic core materials and conductor materials in database are considered as discrete selections. In database,the magnetic materials include the magnetic materials include TDK N87 [173], Ferroxcube 3C90 [174], Metglas 2605-SA1 [175], and Hitachi FT-3M [176]. Informations of other ferrite materials are available in [162]. Only the copper material is considered for winding coil.

Then, other variables are derived from these parameters. The outer diameter of bundled wire is estimated from N_{str} and d_{str}, which determine dimensions of winding coil by

$$\begin{cases} w_{\mathrm{w}} = d_{\mathrm{wire}} N_{\mathrm{w}}, \\ d_{\mathrm{w}} = d_{\mathrm{wire}} N_{\mathrm{d}}. \end{cases} \tag{6.26}$$

Other dimensions of UI core are determined as

$$\begin{cases} w_{\mathrm{s}} = w_{\mathrm{w}} + 2c_{\mathrm{w}}, \\ d_{\mathrm{w}} = d_{\mathrm{w}} + c_{\mathrm{d}}. \end{cases} \tag{6.27}$$

B Inequality constraints for optimization

In this section, some inequality constraints are defined for optimization of UI-core inductor:

- inductance: The inductance of designed arm inductor should be higher than the required arm inductance. In this section, the incremental inductance is calculated from flux linkage around dc operating point, as expressed in (6.28).

$$L_{inc} = \frac{\lambda|_{i_{\text{arm,dc}}+\Delta i} - \lambda|_{i_{\text{arm,dc}}-\Delta i}}{2\Delta i}, \tag{6.28}$$

  where the λ is solved by MEC. Thus, the incremental inductance is limited by inequality constraint $L_{arm} \leq L_{inc}$.

- number of turns: The N_{turn}, N_{d}, and N_{w} are related to number of turns of winding coil. Theoretically, N_{turn} should equal to $N_{\text{d}}N_{\text{w}}$. In this section, it is limited by inequality constraint $N_{\text{turn}} \leq N_{\text{d}}N_{\text{w}}$.

- current density: The current density is estimated from RMS value of arm current rather than dc current, which is $J_{\text{w}} = \frac{I_{\text{arm,rms}}}{N_{\text{str}}A_{\text{str}}}$. Based on analysis of [162], the maximum current density of copper can reach to $7.5 \times 10^6 \ \frac{A}{m^2}$. Thus, the J_{w} is less than $7.5 \times 10^6 \ \frac{A}{m^2}$.

- flux density: To avoid saturation of magnetic core, the maximum flux density of magnetic core (B_{max}) is less than the saturation flux density of magnetic material (B_{sat}).

6.4.5 Case Study

In this chapter, the arm inductor is only designed to suppress circulating current harmonics at fundamental frequency and double frequency. Based on PS modulation, when fixing f_{ac} and θ_{R} at 10 kHz and 0.4π, the arm inductance is 88 μH.

A Evaluation of different core materials

Figure 6.6 compares core losses of arm inductors based on different magnetic materials. The parameters for estimation of core loss are listed in Appendix C, which are obtained by curve-fitting method. Based on these results, the nanocrystalline material (Hitachi FT-3M) causes lowest power loss and small volume of arm inductor. The amorphous material (Metgals 2605-SA1) leads to highest power loss due to its high saturation flux density. Although ferrite materials (3C90 and N87) also lead to acceptable core loss, the volume of arm inductor is larger than that based on nanocrystalline material.

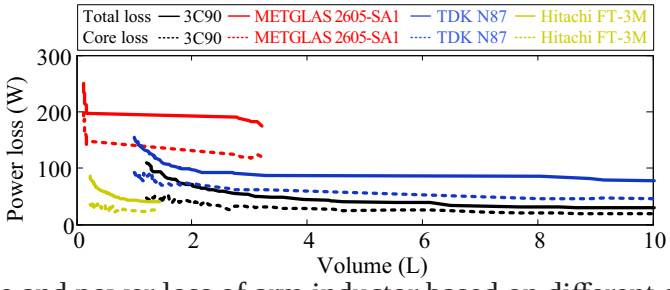


Figure 6.6. Volume and power loss of arm inductor based on different core materials (f_{ac} = 10 kHz, N_{SM} =10, $\theta_R = 0.4\pi$).

B Effects of stranded litz wire

When constructing winding coil by single solid wire, the ac winding loss is much higher than that of litz wire, as shown in Fig. 6.7. In this way, for medium-frequency or high-frequency operating conditions, the winding loss can be reduced by employing stranded litz wire into arm inductor.

6.5 Overall Optimization

For optimal design of the MMC-based SST, the fixed system parameters are listed in Table 6.1. In this design, the secondary-side MMC is assumed to have similar behavior with primary-side MMC. In this way, only the primary-side MMC is designed by the optimal

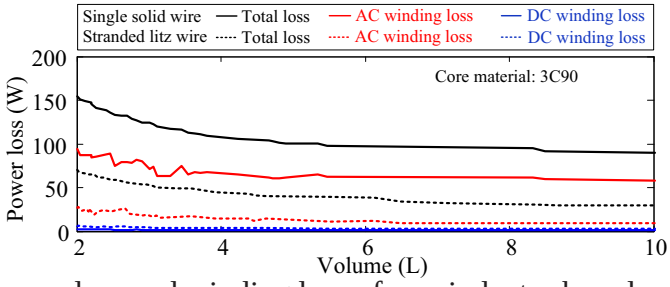


Figure 6.7. Total power loss and winding loss of arm inductor based on single solid wire and stranded litz wire (f_{ac} = 10 kHz, N_{SM} =10, $\theta_{\mathrm{R}} = 0.4\pi$).

design procedure. Then, the same procedure is also applicable for secondary-side MMC, which is not repeated. To evaluate impacts of various free parameters, under each condition, the non-dominated solutions are selected for each component. Figure 6.8 is an example of the non-dominated solutions of SM capacitors. Then, the overall efficiency and power density of the primary-side MMC are evaluated by combining the non-dominated solutions of designed capacitors, semiconductor devices, and arm inductors.

Table 6.1

Fixed Parameters for Optimal Design of the MMC-Based SST

Parameters	**Nominal Value**
Maximum power	1 MW
Primary-side dc-link voltage	10 kV
Secondary-side dc-link voltage	10 kV
Turn ratio of isolated transformer, n_T	1:1
Phase-shift angle for power regulation, Φ	$\frac{\pi}{2}$

6.5.1 Impacts of Number of SMs and Ramping Angle of AC-Link Voltage

To investigate impacts of N_{SM} and θ_{R}, other free parameters are fixed, where f_{ac} is 1 kHz. The single-step alternating algorithm and PS modulation are selected to generate switching signals of SMs.

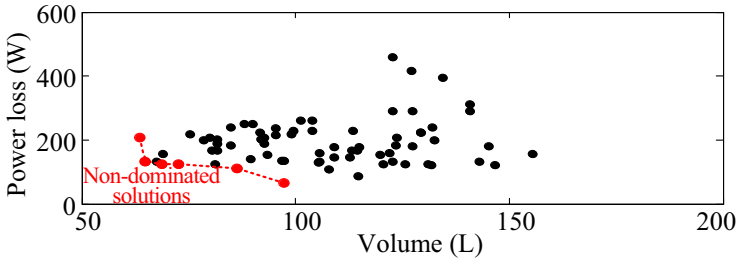


Figure 6.8. Diagram of non-dominated solutions of selected capacitors (f_{ac} = 1 kHz, N_{SM} = 10, and θ_R = 0.9π).

A SM capacitors

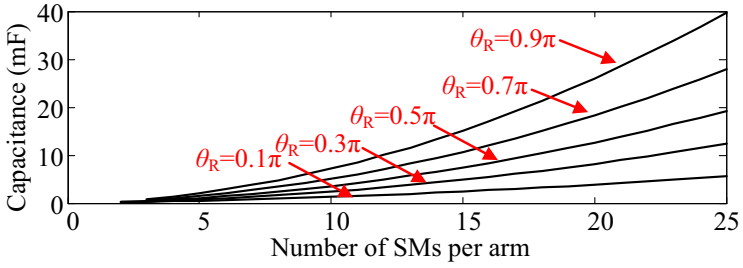


Figure 6.9. Capacitance based on various N_{SM} and θ_R (f_{ac} =1 kHz).

When fixing f_{ac} at 1 kHz, the SM capacitance is greatly increased by increasing number of SMs and ramping angles of ac-link voltage as shown in Fig. 6.9. When constructing the SM capacitors by film capacitors and electrolytic capacitors, the film capacitor is only available for low-capacitance and high-voltage designs, while the electrolytic capacitors are suitable for high-capacitance and low-voltage designs. Because, comparing with electrolytic capacitors, film capacitors have lower capacitance and higher voltage rating. When comparing their volume and power losses, the film capacitor results in low power losses due to low ESRs, while electrolytic capacitors lead to smaller volume of SM capacitor, as shown in Fig. 6.10.

B Semiconductor devices

Based on various number of SMs per arm, figure 6.11 shows the blocking voltages of available semiconductor devices. Figure 6.12 shows the semiconductor losses of silicon

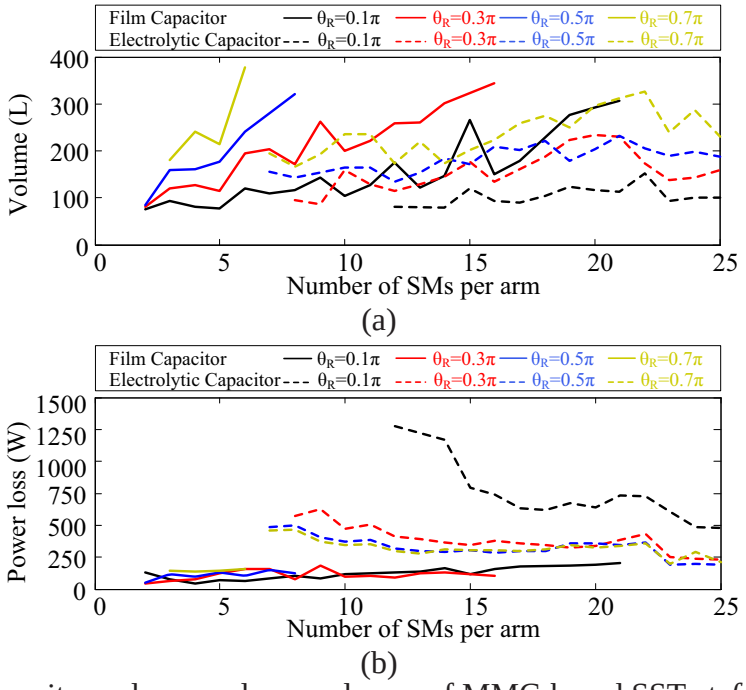


Figure 6.10. Capacitor volume and power losses of MMC-based SST at f_{ac} = 1 kHz: (a) volume, and (b) power losses.

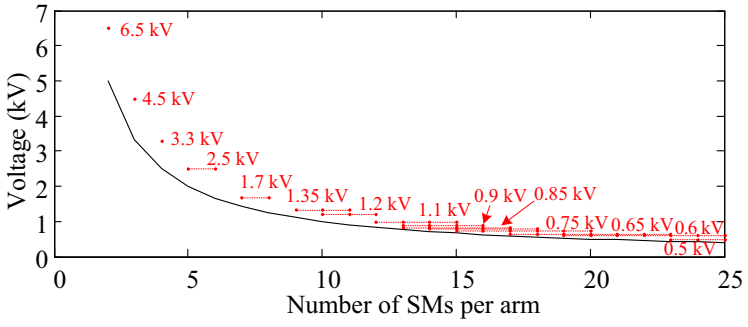


Figure 6.11. Blocking voltages of available semiconductor devices based on various number of SMs.

(Si) insulated gate bipolar transistor (IGBT) and metal-oxide-semiconductor field-effect transistor (MOSFET). Initially, when increasing N_{SM}, the semiconductor loss is reduced due to reduction of switching loss. Generally, the low-voltage semiconductor devices have better switching performances than high-voltage ones. However, when further increasing N_{SM}, the conduction loss is greatly increased due to increased number of semiconductor devices. Under low-frequency operating conditions, the hybrid IGBTs and the silicon car-

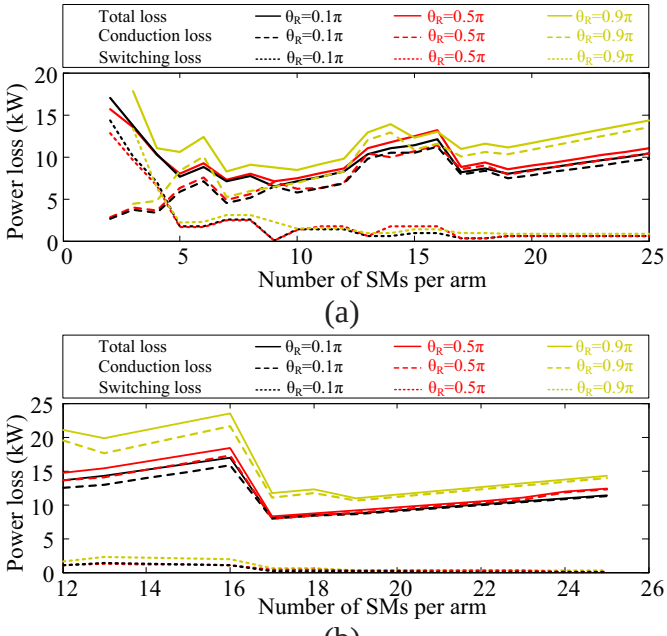


Figure 6.12. Semiconductor loss of Si devices at f_{ac} = 1 kHz: (a) IGBT, and (b) MOSFET.

bide (SiC) MOSFETs lead to limited reduction of switching loss, while even lead to higher conduction loss as shown in Fig. 6.13.

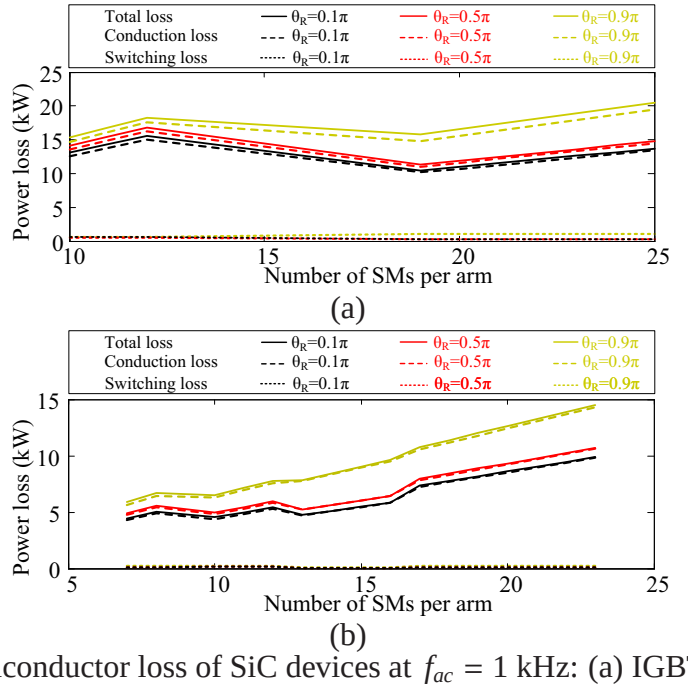


Figure 6.13. Semiconductor loss of SiC devices at f_{ac} = 1 kHz: (a) IGBT, and (b) MOSFET.

The high semiconductor loss requires large volume of heat sink to dissipate heat and

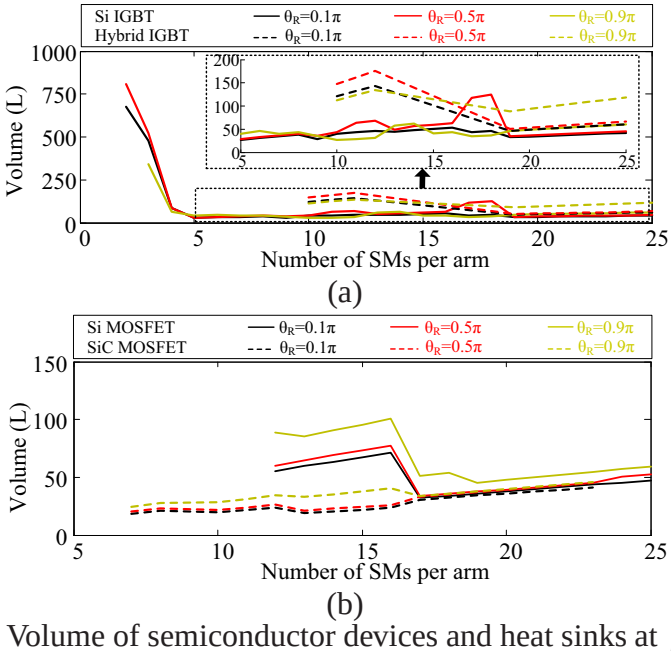


Figure 6.14. Total Volume of semiconductor devices and heat sinks at f_{ac} = 1 kHz: (a) IGBT, and (b) MOSFET.

limit junction temperature. Thus, it has similar trend as semiconductor loss, as shown in Fig. 6.14.

C Arm inductors

Based on the single-step alternating voltage-balancing algorithm, the increased N_{SM} leads to reduced arm inductance, as shown in Fig. 6.15(a). Because, based on single-step alternating voltage-balancing algorithm, when increasing N_{SM}, the greater SM capacitance is required to suppress low-frequency capacitor voltage ripple. At the same time, the fundamental-frequency and double-frequency capacitor ripples are further reduced, and hence could lead to lower circulating current ripple. Similarly, when increasing θ_{R}, the increased SM capacitance also help reduce circulating current ripple to reduce arm inductance. As shown in Fig. 6.15(b), the volume of inductor is reduced by increasing θ_{R}, while the power loss is not greatly reduced. Based on increased N_{SM}, the power loss can be reduced, while the volume is not obviously reduced.

D Total power loss and volume

Based on different N_{SM} and θ_R, the total power losses and volume of MMC are shown in Fig. 6.16. Under this condition, the semiconductor loss dominates the total loss, while the capacitor volume dominates the total volume. By increasing N_{SM}, initially the total power loss and volume are reduced. While, when further increasing N_{SM}, they are increased. In addition, as shown in Fig. 6.16, when increasing the θ_R from 0.1π to 0.9π, the power loss and volume are increased.

6.5.2 Impacts of Frequency on Design of MMC

In this subsection, the single-step alternating algorithm is still selected to balance capacitor voltages, which is based on PS modulation. The θ_R is fixed at 0.1π.

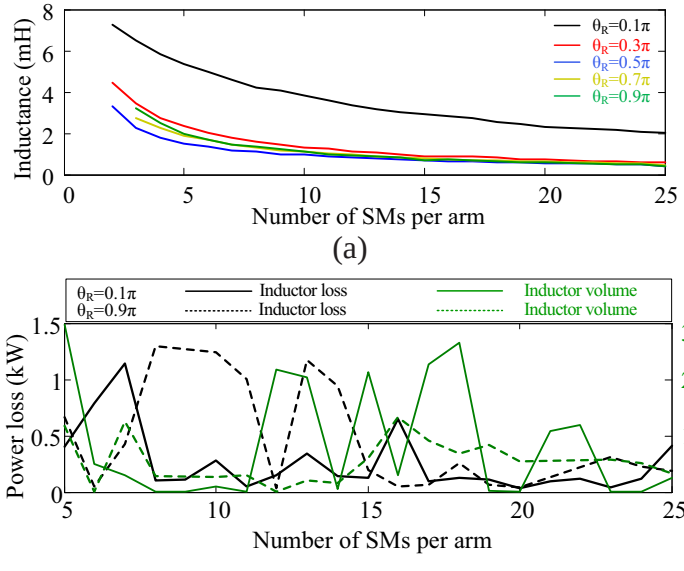


Figure 6.15. Arm inductances, power losses, and volume of inductors based on different number of SMs and ramping angles (f_{ac} = 1 kHz): (a) inductance, and (b) power loss and volume.

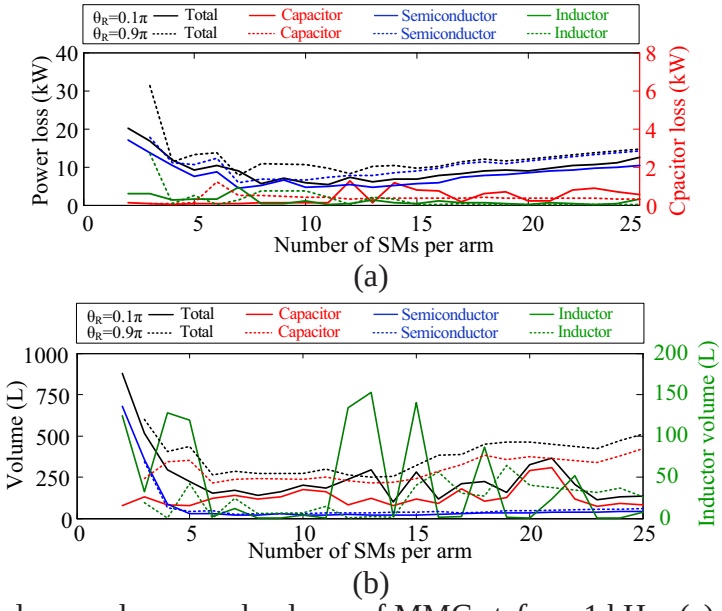


Figure 6.16. Total power losses and volume of MMC at f_{ac} = 1 kHz: (a) power losses, and (b) volume.

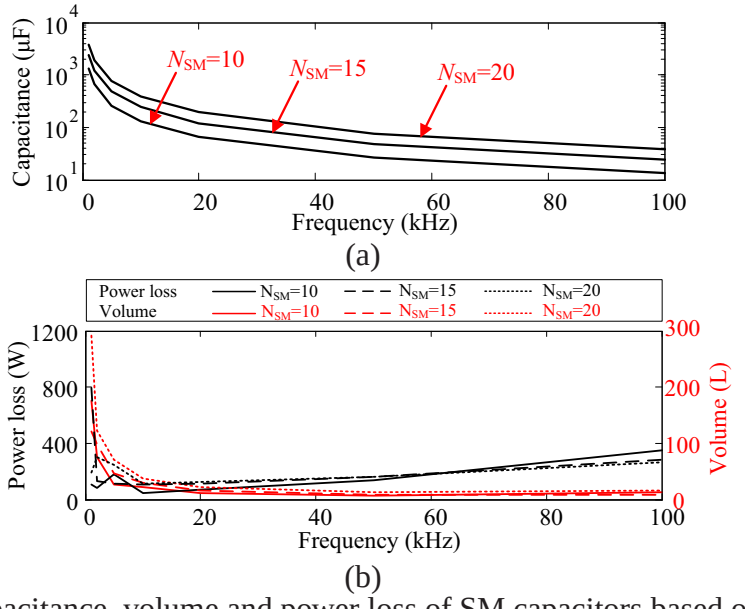


Figure 6.17. Capacitance, volume and power loss of SM capacitors based on various f_{ac} ($\theta_R = 0.1\pi$): (a) capacitance, and (b) power losses and volume .

A SM Capacitors

When increasing f_{ac} from 1 kHz to 100 kHz, the SM capacitance is greatly reduced, as shown in Fig. 6.17(a). However, this does not guarantee lower power loss and small-

er volume. Initially, when increasing f_{ac}, the reduced SM capacitance results in smaller volume and lower power loss, as shown in Fig. 6.17(b). When further increasing f_{ac}, the volume does not significantly reduce. However, the power loss is increased. Because, when increasing ac-link voltage frequency, the low-capacitance film capacitors are selected to construct SM capacitor. Generally, the low-capacitance film capacitor has high ESR, which leads to high power loss. For different N_{SM}, the trend is similar.

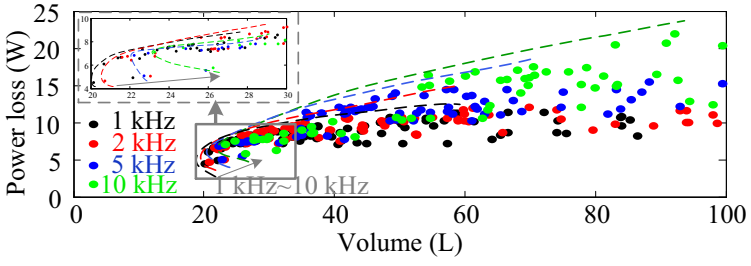


Figure 6.18. Total volume and power losses of semiconductor devices and heat sinks based on various frequencies ($N_{\mathrm{SM}} = 10$ and $\theta_{\mathrm{R}} = 0.1\pi$).

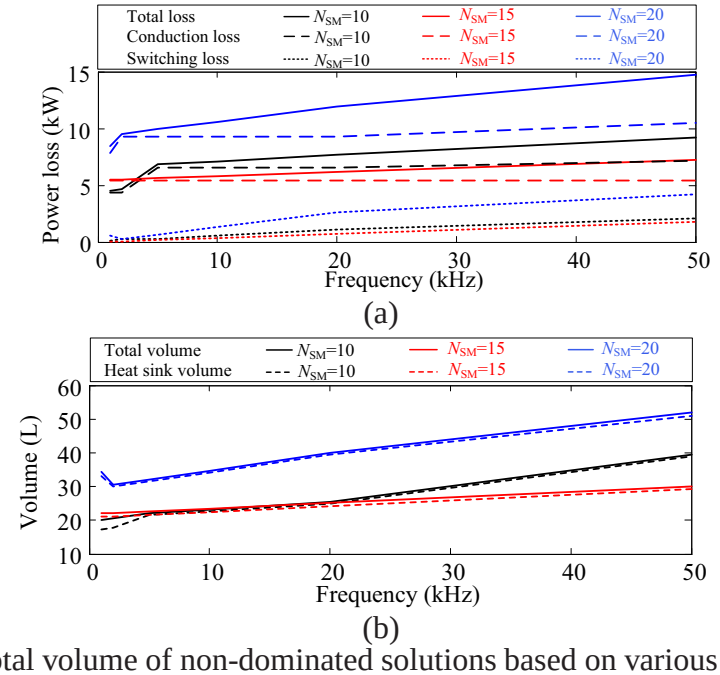


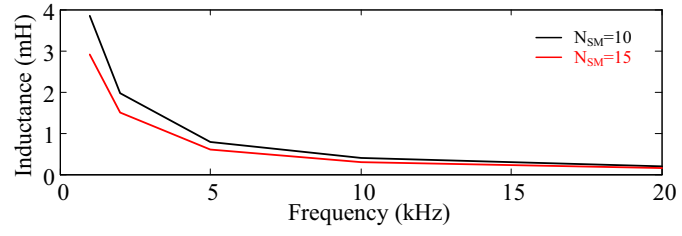
Figure 6.19. Total volume of non-dominated solutions based on various frequencies and number of SMs: (a) Power losses, and (b) volume ($\theta_{\mathrm{R}} = 0.1\pi$).

B Semiconductor devices

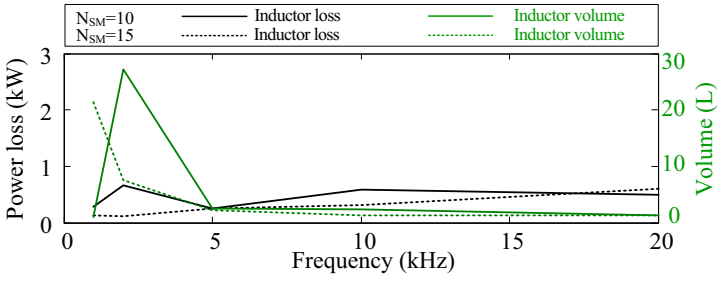
When increasing f_{ac} from 1 kHz to 10 kHz, the volume and power losses of selected semiconductor devices and heat sinks are compared in Fig. 6.18. The increased f_{ac} results in increased total volume of semiconductor devices and heat sinks, and increased power losses of semiconductor devices. In detail, the conductor losses and switching losses of non-dominated solutions are compared in Fig. 6.19(a). Based on increased frequency, the conduction loss is not greatly increased, while the switching loss is greatly increased. Thus, the increased heat sink volume is induced from increased switching loss, as shown in Fig. 6.19(b).

C Arm inductor

When increasing f_{ac} from 1 kHz to 20 kHz, the arm inductance is greatly reduced, as shown in Fig. 6.20(a). Initially, the power loss and volume of arm inductor are reduced. While, when further increasing f_{ac}, the power loss and volume are not greatly reduced.



(a)



(b)

Figure 6.20. Inductance, volume and power loss of an arm inductor based on various f_{ac} ($\theta_R = 0.1\pi$): (a) inductance, and (b) power losses and volume.

In detail, based on various f_{ac}, the core loss and winding loss are compared in Fig. 6.21. The increased f_{ac} greatly increases core loss of arm inductor, even though reduces volume magnetic core. The dc winding loss keeps low, while the ac winding loss is not greatly influenced by increased f_{ac} due to employment of litz wire.

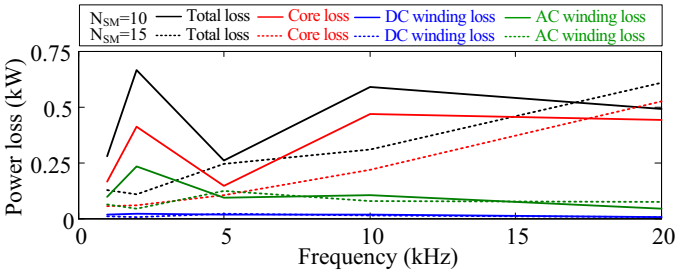


Figure 6.21. Power losses of an arm inductor based on various f_{ac} ($\theta_R = 0.1\pi$).

D Total power loss and volume

Based on different f_{ac} and N_{SM}, the total power losses and volume of MMC are shown in Fig. 6.22. Initially, the increased f_{ac} results in greatly reduced volume, while the total power loss is neither greatly increased nor reduced. When further increasing f_{ac}, the total volume is not greatly reduced, while the total loss is increased. Thus, the optimal frequency should be determined by trade-off between total volume and power loss.

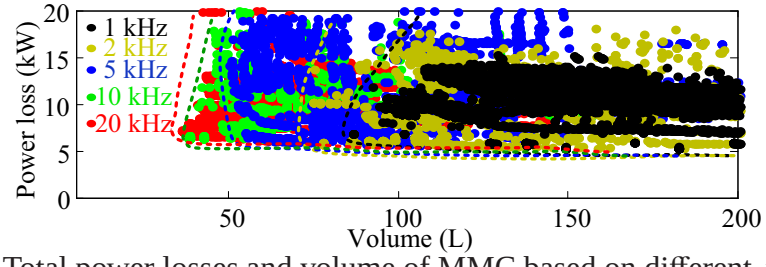


Figure 6.22. Total power losses and volume of MMC based on different f_{ac} ($\theta_R = 0.1\pi$).

In detail, the volume and power loss of selected components are compared in Fig. 6.23. Under all conditions, the semiconductor loss dominates total loss of MMC. Under low-frequency operating condition, the capacitor volume dominates the total volume. When

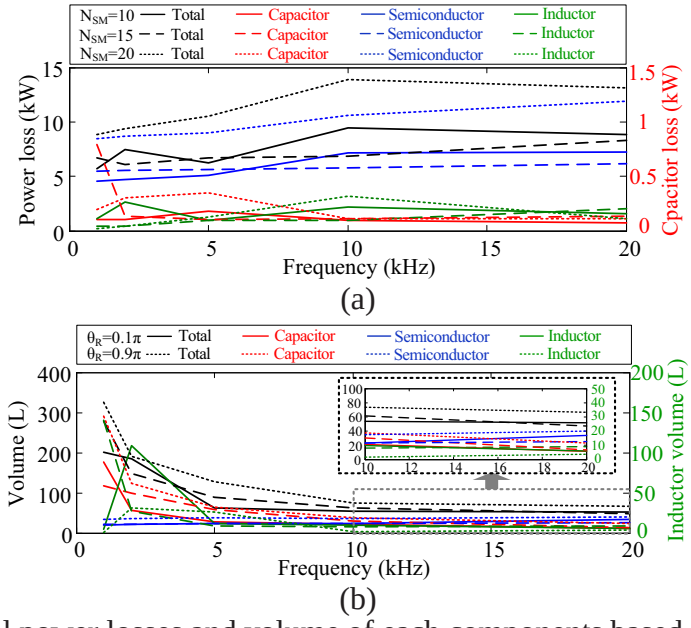


Figure 6.23. Total power losses and volume of each components based on various f_{ac} ($\theta_{\mathrm{R}} = 0.1\pi$): (a) power losses, and (b) volume.

increasing f_{ac}, the volume of SM capacitors is greatly reduced, while the volume of heat sinks increases and dominates the total volume.

6.5.3 Overall Power Loss and Volume of MMC in MMC-Based SST

Based on various f_{ac}, N_{SM}, and θ_{R}, the efficiency and power density of primary-side MMC are evaluated to identify the optimal solutions, as shown in Fig. 6.24. The non-dominated solutions can be regarded as optimal solutions. While among them, an optimal solution results in highest power density (27.65 kW/L) and acceptable efficiency (99.28%), where the total loss is 7.192 kW, and the volume is 36.17 L. The corresponding specifi-

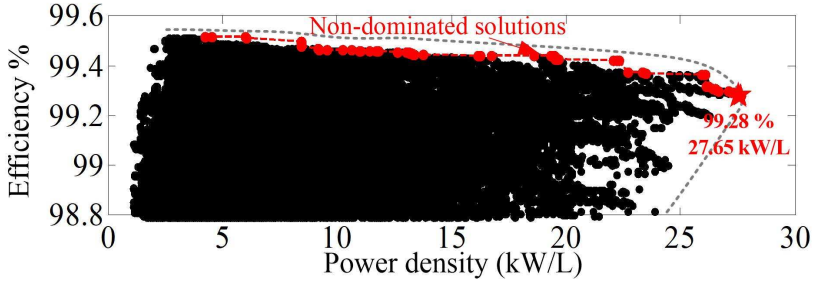


Figure 6.24. Efficiency and power density of primary-side MMC based on different f_{ac}, N_{SM}, and θ_{R}.

cations of selected components are listed in Table. 6.2. The corresponding f_{ac} and θ_{R} of ac-link voltage are 20 kHz and 0.1π. There are 13 SMs in each arm. The SM capacitor is constructed by 5 paralleled 20 μF film capacitors. The SiC MOSFETs are selected to construct SM. The arm inductor is designed based on the nanocrystalline material from Hitachi.

Table 6.2
Specification of Selected Components for Optimal Design of MMC

Parameters	Nominal Value
System Parameters	
Maximum power	1 MW
Primary-side dc-link voltage	10 kV
Secondary-side dc-link voltage	10 kV
Frequency of ac-link voltage, f_{ac}	20 kHz
Turn ratio of isolated transformer, n_T	1:1
Phase-shift angle for power regulation, Φ	$\frac{\pi}{2}$
Ramping angle, θ_{R}	0.1π
Circuit Parameters	
Number of SMs, N_{SM}	13
SM capacitance, C	97.42 μF
Arm inductance, L_{arm}	166.88 μH
Control Options	
Modulation	phase-shift modulation
Voltage-balancing algorithm	single-step alternating
Selected Capacitor	
Part No.	MKP1848C62090JP*
Number of series-connected capacitor, n_s	1
Number of paralleled capacitors, n_p	5
Total volume	11.53 L
Total loss	118.12 W
Selected Semiconductor Devices	
Part No.	C3M0030090K
Number of paralleled semiconductor devices, n_p	4
Total volume	22.16 L
Total loss	5.438 kW
Arm Inductor	
Core material	Hitachi FT-3M
Winding dimensions	N_d: 1, N_w: 7, N_{str} 3284, Strand AWG: 41, A_{str}: 0.00397 mm^2
Core dimensions	g: 0.765 mm, l_c: 28.2 cm, w_b: 12.84 mm, w_e: 16.35 mm, w_i: 12.38 mm, d_s: 4.89 mm, w_s: 33.98 mm
Total volume	2.48 L
Total loss	1.636 kW

Chapter 7

SUMMARY AND FUTURE WORK

7.1 Summary

The main focuses of this thesis are design, modeling and control of MMCs for high-power applications. The state-of-art of MMC-based applications and the objectives of this thesis are presented in Chapter 1.

The main contributions of this thesis are listed as follows:

- A generalized precharging strategy is proposed for the MMC-based systems built upon various SM circuits under ac- and dc-side startup conditions.

- An improved equivalent circuit model (ECM) of MMC is proposed for large-scale MMC-based HVDC or MTDC system, which improves the computational efficiency and considers the various SM configurations and different operating conditions of MMC. The impacts of simulation time step are also analyzed and determined for the proposed ECM.

- The operational principles and mathematical model of MMC-based SST are analyzed in this thesis. A modified mathematical model is proposed for optimal design of the MMC-based SST by considering circuit parameters. Then, the proposed mathematical models are verified by simulation results and experimental results.

- The performances of different modulation methods and voltage-balancing algorithms are comprehensively analyzed and evaluated for MMC-based SST. Based on the analysis, two improved voltage balancing algorithms are proposed for IM2DC or MMC-based SST. The proposed algorithms are verified by PSCAD simulation results and

experimental results.

- Based on the proposed modified mathematical model of MMC-based SST, an optimal design procedure is proposed for MMC in the MMC-based SST. The impacts of free system parameters on design performance of the MMC for SST applications have been comprehensively investigated. The overall efficiency and power density of MMC have been evaluated to identify the optimal solutions.

7.2 Future Work

The following items are suggested for the future research:

- In this thesis, only the MMC is optimized for the MMC-based SST. In the future, the optimal design of MFT should be embedded into optimal design procedure of the MMC-based SST. Then, the overall efficiency and power density of the MMC-based SST should be comprehensively evaluated by considering both of MMC and MFT.

- The performances of SSTs based on various topologies should be compared and evaluated to identify the optimal topology.

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APPENDIX A

DETAILED DERIVATIONS OF PIECE-WISE LINEAR EQUATIONS FOR MMC-BASED SST

A.1 Derivations of AC-Link Current and Transmitted Power

A.1.1 Condition of $0 < \Phi < \frac{\pi}{2}$ and $\theta_R < \Phi$

The primary-side ac-link voltage is expressed in (A.1). When reflecting secondary-side ac-link voltage to primary-side, it is expressed as $v'_{ac,sec}$ in (A.2).

$$v_{ac,pri}(\varphi) = \begin{cases} \dfrac{2V_{dc,pri}}{\theta_R}(\varphi - \Phi) - V_{dc,pri}, & 0 < \varphi < \theta_R, \\ V_{dc,pri}, & \theta_R < \varphi < \pi, \\ -v_{ac,pri}(\varphi - \pi), & \pi < \varphi < 2\pi. \end{cases} \tag{A.1}$$

$$v'_{ac,sec}(\varphi) = \begin{cases} -n_T V_{dc,sec}, & 0 < \varphi < \Phi, \\ \dfrac{2n_T V_{dc,sec}}{\theta_R}\varphi - n_T V_{dc,sec}, & \Phi < \varphi < \Phi + \theta_R, \\ n_T V_{dc,sec}, & \Phi + \theta_R < \varphi < \pi, \\ -v'_{ac,sec}(\varphi - \pi), & \pi < \varphi < 2\pi. \end{cases} \tag{A.2}$$

Then, the ac-link current is dominated by differential equation and is derived as

$$v_{ac,pri}(\varphi) - v'_{ac,sec}(\varphi) = \frac{L_{tot} \cdot di_a}{dt}. \tag{A.3}$$

$$\begin{aligned} i_a(\varphi) = & \begin{cases} \dfrac{1}{\omega L_{tot}} \displaystyle\int_0^{\varphi} \frac{2V_{dc,pri}}{\theta_R}\varphi - V_{dc,pri} + n_T V_{dc,sec} d\varphi + I_0, & 0 < \varphi < \theta_R, \\ \dfrac{1}{\omega L_{tot}} \displaystyle\int_{\theta_R}^{\varphi} V_{dc,pri} + n_T V_{dc,sec} d\varphi + I_1, & \theta_R < \varphi < \Phi, \\ \dfrac{1}{\omega L_{tot}} \displaystyle\int_{\Phi}^{\varphi} V_{dc,pri} + n_T V_{dc,sec} - \frac{2n_T V_{dc,sec}}{\theta_R}(\varphi - \Phi)\, d\varphi + I_2, & \Phi < \varphi < \Phi + \theta_R, \\ \dfrac{1}{\omega L_{tot}} \displaystyle\int_{\Phi+\theta_R}^{\varphi} V_{dc,pri} - n_T V_{dc,sec} d\varphi + I_3, & \Phi + \theta_R < \pi, \end{cases} \\ = & \begin{cases} \dfrac{V_{dc,pri}}{\omega L_{tot}}\left(\dfrac{\varphi^2}{\theta_R} - \varphi\right) + \dfrac{n_T V_{dc,sec}}{\omega L_{tot}}\varphi + I_0, & 0 < \varphi < \theta_R, \\ \dfrac{V_{dc,pri}}{\omega L_{tot}}(\varphi - \theta_R) + \dfrac{n_T V_{dc,sec}}{\omega L_{tot}}(\varphi - \theta_R) + I_1, & \theta_R < \varphi < \Phi, \\ \dfrac{V_{dc,pri}}{\omega L_{tot}}(\varphi - \Phi) + \dfrac{n_T V_{dc,sec}}{\omega L_{tot}}\left(\dfrac{(\varphi - \Phi)^2}{\theta_R} + \varphi - \Phi\right) + I_2, & \Phi < \varphi < \Phi + \theta_R, \\ \dfrac{V_{dc,pri}}{\omega L_{tot}}(\varphi - \Phi - \theta_R) + \dfrac{n_T V_{dc,sec}}{\omega L_{tot}}(-\varphi + \Phi + \theta_R) + I_3, & \Phi + \theta_R < \pi, \end{cases} \end{aligned} \tag{A.4}$$

where I_0 to I_3 are derived as:

$$\begin{cases} I_0 = \dfrac{1}{\omega L_{\text{tot}}}\left[V_{\text{dc,pri}}\left(\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\text{dc,sec}}\left(\dfrac{\pi}{2}-\Phi-\dfrac{\theta_{\text{R}}}{2}\right)\right], \\ I_1 = \dfrac{1}{\omega L_{\text{tot}}}\left[V_{\text{dc,pri}}\left(\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\text{dc,sec}}\left(\dfrac{\pi}{2}-\Phi+\dfrac{\theta_{\text{R}}}{2}\right)\right], \\ I_2 = \dfrac{1}{\omega L_{\text{tot}}}\left[V_{\text{dc,pri}}\left(\Phi-\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\text{dc,sec}}\left(\dfrac{\pi}{2}-\dfrac{\theta_{\text{R}}}{2}\right)\right], \\ I_3 = \dfrac{1}{\omega L_{\text{tot}}}\left[V_{\text{dc,pri}}\left(\Phi+\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\text{dc,sec}}\left(\dfrac{\pi}{2}-\dfrac{\theta_{\text{R}}}{2}\right)\right]. \end{cases} \tag{A.5}$$

In this way, when $\Phi > 0$, the ac-link current is expressed as (A.6).

$$i_{\text{a}}(\varphi)=\begin{cases} \dfrac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\dfrac{\varphi^2}{\theta_{\text{R}}}-\varphi+\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\left(\varphi-\Phi-\dfrac{\theta_{\text{R}}}{2}+\dfrac{\pi}{2}\right), & 0<\varphi<\theta_{\text{R}}, \\ \dfrac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\varphi-\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\left(\varphi-\Phi-\dfrac{\theta_{\text{R}}}{2}+\dfrac{\pi}{2}\right), & \theta_{\text{R}}<\varphi<\Phi, \\ \dfrac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\varphi-\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\left(\dfrac{(\varphi-\Phi)^2}{\theta_{\text{R}}}+\varphi-\Phi-\dfrac{\theta_{\text{R}}}{2}+\dfrac{\pi}{2}\right), & \Phi<\varphi<\Phi+\theta_{\text{R}}, \\ \dfrac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\varphi-\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\left(-\varphi+\Phi+\dfrac{\theta_{\text{R}}}{2}+\dfrac{\pi}{2}\right), & \Phi+\theta_{\text{R}}<\varphi<\pi, \\ -i_{\text{a}}(\varphi-\pi), & \pi<\varphi<2\pi. \end{cases} \tag{A.6}$$

The average power at dc-side can be derived from ac-link voltage and ac-link current.

$$P_{\text{dc}} = \frac{\int_0^{\pi} v_a(\varphi) i_a(\varphi)\mathrm{d}\varphi}{\pi}. \tag{A.7}$$

The detailed calculations of P_{dc} are as follow:

$$\begin{aligned} &\frac{1}{\pi}\int_0^{\theta_R} v_{\text{ac,pri}}(\varphi) i_a(\varphi)\mathrm{d}\varphi \\ &= \int_0^{\theta_{\text{R}}} \frac{V_{\text{dc,pri}}}{\pi}\left(\frac{2\varphi}{\theta_{\text{R}}}-1\right)\left[\frac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\frac{\varphi^2}{\theta_{\text{R}}}-\varphi\right)+\frac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\varphi+I_0\right]\mathrm{d}\varphi \\ &= \frac{n_T V_{\text{dc,pri}} V_{\text{dc,sec}}}{\pi\omega L_{\text{tot}}}\frac{\theta_R^2}{6}, \end{aligned} \tag{A.8}$$

$$\begin{aligned} &\frac{1}{\pi}\int_{\theta_R}^{\Phi} v_{\text{ac,pri}}(\varphi) i_a(\varphi)\mathrm{d}\varphi \\ &= \int_{\theta_{\text{R}}}^{\Phi} \frac{V_{\text{dc,pri}}}{\pi}\left[\frac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}(\varphi-\theta_{\text{R}})+\frac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}(\varphi-\theta_{\text{R}})+I_1\right]\mathrm{d}\varphi \\ &= \frac{\left(V_{\text{dc,pri}}^2 - n_T V_{\text{dc,pri}} V_{\text{dc,sec}}\right)\left(\Phi^2-\pi\Phi+\pi\theta_R-\Phi\theta_R\right)}{2\pi\omega L_{\text{tot}}}, \end{aligned} \tag{A.9}$$

$$
\begin{aligned}
&\frac{1}{\pi}\int_{\Phi}^{\Phi+\theta_R} v_{\mathrm{ac,pri}}(\varphi) i_a(\varphi)\mathrm{d}\varphi \\
&= \int_{\theta_\mathrm{R}}^{\Phi+\theta_\mathrm{R}} \frac{V_{\mathrm{dc,pri}}}{\pi}\left[\frac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}(\varphi-\Phi)+\frac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(-\frac{(\varphi-\Phi)^2}{\theta_\mathrm{R}}+\varphi-\Phi\right)+I_2\right]\mathrm{d}\varphi \\
&= \frac{V_{\mathrm{dc,pri}}^2\left(-\frac{\pi\theta_R}{2}+\Phi\theta_R\right)+n_T V_{\mathrm{dc,pri}} V_{\mathrm{dc,sec}}\left(\frac{\pi\theta_R}{2}-\frac{\theta_R^2}{3}\right)}{\pi\omega L_{\mathrm{tot}}},
\end{aligned}
\tag{A.10}
$$

$$
\begin{aligned}
&\frac{1}{\pi}\int_{\Phi+\theta_\mathrm{R}}^{\pi} v_{\mathrm{ac,pri}}(\varphi) i_a(\varphi)\mathrm{d}\varphi \\
&= \int_{\Phi+\theta_\mathrm{R}}^{\pi} \frac{V_{\mathrm{dc,pri}}}{\pi}\left[\frac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}(\varphi-\Phi-\theta_\mathrm{R})+\frac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}(-\varphi+\Phi+\theta_\mathrm{R})+I_3\right]\mathrm{d}\varphi \\
&= \frac{\left(V_{\mathrm{dc,pri}}^2+n_T V_{\mathrm{dc,pri}} V_{\mathrm{dc,sec}}\right)\left(-\frac{\Phi^2}{2}+\frac{\pi\Phi}{2}-\frac{\Phi\theta_R}{2}\right)}{\pi\omega L_{\mathrm{tot}}}.
\end{aligned}
\tag{A.11}
$$

Then, the P_{dc} is calculated by summing (A.8) to (A.11), which is expressed as:

$$
P_{\mathrm{dc}} = \frac{n_T V_{\mathrm{dc,pri}} V_{\mathrm{dc,sec}}\left(-\Phi^2-\frac{\theta_R^2}{6}+\pi\Phi\right)}{\pi\omega L_{\mathrm{tot}}}.
\tag{A.12}
$$

A.1.2 Condition of $-\frac{\pi}{2} < \Phi < 0$ and $\theta_\mathrm{R} < |\Phi|$

$$
v'_{\mathrm{ac,sec}}(\varphi) = \begin{cases}
n_T V_{\mathrm{dc,sec}}, & 0 < \varphi < \pi+\Phi, \\
-\frac{2n_T V_{\mathrm{dc,sec}}}{\theta_\mathrm{R}}(\varphi-\pi-\Phi)+n_T V_{\mathrm{dc,sec}}, & \Phi < \varphi < \Phi+\theta_\mathrm{R}, \\
-n_T V_{\mathrm{dc,sec}}, & \pi+\Phi+\theta_\mathrm{R} < \varphi < \pi, \\
-v'_{\mathrm{ac,sec}}(\varphi-\pi), & \pi < \varphi < 2\pi.
\end{cases}
\tag{A.13}
$$

$$
i_\mathrm{a}(\varphi) = \begin{cases}
\frac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\frac{\varphi^2}{\theta_\mathrm{R}}-\varphi\right)-\frac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\varphi+I_0, & 0 < \varphi < \theta_\mathrm{R}, \\
\frac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}(\varphi-\theta_\mathrm{R})-\frac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}(\varphi-\theta_\mathrm{R})+I_1, & \theta_\mathrm{R} < \varphi < \pi+\Phi, \\
\frac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}(\varphi-\pi-\Phi)+\frac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left(\frac{(\varphi-\pi-\Phi)^2}{\theta_\mathrm{R}}-\varphi+\pi+\Phi\right)+I_2, & \pi+\Phi < \varphi < \pi+\Phi+\theta_\mathrm{R}, \\
\frac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}(\varphi-\pi-\Phi-\theta_\mathrm{R})+\frac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}(\varphi-\pi-\Phi-\theta_\mathrm{R})+I_3, & \pi+\Phi+\theta_\mathrm{R} < \pi,
\end{cases}
\tag{A.14}
$$

where I_0 to I_3 are derived as:

$$\begin{cases} I_0 = \dfrac{1}{\omega L_{\text{tot}}}\left[V_{\text{dc,pri}}\left(\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\text{dc,sec}}\left(\dfrac{\pi}{2}+\Phi+\dfrac{\theta_{\text{R}}}{2}\right)\right], \\ I_1 = \dfrac{1}{\omega L_{\text{tot}}}\left[V_{\text{dc,pri}}\left(\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\text{dc,sec}}\left(\dfrac{\pi}{2}+\Phi-\dfrac{\theta_{\text{R}}}{2}\right)\right], \\ I_2 = \dfrac{1}{\omega L_{\text{tot}}}\left[V_{\text{dc,pri}}\left(\dfrac{\pi}{2}+\Phi-\dfrac{\theta_{\text{R}}}{2}\right)-n_T V_{\text{dc,sec}}\left(\dfrac{\pi}{2}-\dfrac{\theta_{\text{R}}}{2}\right)\right], \\ I_3 = \dfrac{1}{\omega L_{\text{tot}}}\left[V_{\text{dc,pri}}\left(\dfrac{\pi}{2}+\Phi+\dfrac{\theta_{\text{R}}}{2}\right)-n_T V_{\text{dc,sec}}\left(\dfrac{\pi}{2}-\dfrac{\theta_{\text{R}}}{2}\right)\right]. \end{cases} \tag{A.15}$$

$$i_{\text{a}}(\varphi)=\begin{cases} \dfrac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\dfrac{\varphi^2}{\theta_{\text{R}}}-\varphi+\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\left(-\varphi+\Phi+\dfrac{\theta_{\text{R}}}{2}+\dfrac{\pi}{2}\right), & 0<\varphi<\theta_{\text{R}}, \\ \dfrac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\varphi-\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\left(-\varphi+\Phi+\dfrac{\theta_{\text{R}}}{2}+\dfrac{\pi}{2}\right), & \theta_{\text{R}}<\varphi<\pi+\Phi, \\ \dfrac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\varphi-\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\left[\dfrac{(\varphi-\pi-\Phi)^2}{\theta_{\text{R}}}-\varphi+\Phi+\dfrac{\theta_{\text{R}}}{2}+\dfrac{\pi}{2}\right], & \pi+\Phi<\varphi<\pi+\Phi+\theta_{\text{R}}, \\ \dfrac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\varphi-\dfrac{\theta_{\text{R}}}{2}-\dfrac{\pi}{2}\right)+\dfrac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\left(\varphi-\Phi-\dfrac{\theta_{\text{R}}}{2}-\dfrac{3\pi}{2}\right), & \pi+\Phi+\theta_{\text{R}}<\varphi<\pi, \\ -i_{\text{a}}(\varphi-\pi), & \pi<\varphi<2\pi. \end{cases} \tag{A.16}$$

The detailed calculations of P_{dc} are as follow:

$$\begin{aligned} &\frac{1}{\pi}\int_0^{\theta_R} v_{\text{ac,pri}}(\varphi) i_a(\varphi)\mathrm{d}\varphi \\ &= \int_0^{\theta_{\text{R}}} \frac{V_{\text{dc,pri}}}{\pi}\left(\frac{2\varphi}{\theta_{\text{R}}}-1\right)\left[\frac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}\left(\frac{\varphi^2}{\theta_{\text{R}}}-\varphi\right)-\frac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}\varphi+I_0\right]\mathrm{d}\varphi \\ &= -\frac{n_T V_{\text{dc,pri}} V_{\text{dc,sec}}}{\pi\omega L_{\text{tot}}}\frac{\theta_R^2}{6}, \end{aligned} \tag{A.17}$$

$$\begin{aligned} &\frac{1}{\pi}\int_{\theta_{\text{R}}}^{\pi+\Phi} v_{\text{ac,pri}}(\varphi) i_a(\varphi)\mathrm{d}\varphi \\ &= \int_{\theta_{\text{R}}}^{\pi+\Phi} \frac{V_{\text{dc,pri}}}{\pi}\left[\frac{V_{\text{dc,pri}}}{\omega L_{\text{tot}}}(\varphi-\theta_{\text{R}})-\frac{n_T V_{\text{dc,sec}}}{\omega L_{\text{tot}}}(\varphi-\theta_{\text{R}})+I_1\right]\mathrm{d}\varphi \\ &= \frac{V_{\text{dc,pri}}^2}{\pi\omega L_{\text{tot}}}\left(\frac{\Phi^2}{2}+\frac{\pi\Phi}{2}-\frac{\Phi\theta_{\text{R}}}{2}\right)+\frac{n_T V_{\text{dc,pri}} V_{\text{dc,sec}}}{\pi\omega L_{\text{tot}}}\left(\frac{\Phi^2}{2}+\frac{\pi\Phi}{2}-\frac{\Phi\theta_{\text{R}}}{2}\right), \end{aligned} \tag{A.18}$$

$$\begin{aligned}
&\frac{1}{\pi}\int_{\pi+\Phi}^{\pi+\Phi+\theta_R} v_{ac,pri}(\varphi) i_a(\varphi)\mathrm{d}\varphi \\
&= \int_{\pi+\Phi}^{\pi+\Phi+\theta_R} \frac{V_{dc,pri}^2(\varphi-\pi-\Phi)}{\pi\omega L_{tot}} + \frac{n_T V_{dc,pri} V_{dc,sec}}{\pi\omega L_{tot}}\left[\frac{(\varphi-\pi-\Phi)^2}{\theta_R} - \varphi + \pi + \Phi\right] + \frac{V_{dc,pri} I_2}{\pi}\mathrm{d}\varphi \\
&= \frac{V_{dc,pri}^2}{\pi\omega L_{tot}}\left(\frac{\pi\theta_R}{2} + \Phi\theta_R\right) + \frac{n_T V_{dc,pri} V_{dc,sec}}{\pi\omega L_{tot}}\left(\frac{\theta_R^2}{3} - \frac{\pi\theta_R}{2}\right),
\end{aligned} \tag{A.19}$$

$$\begin{aligned}
&\frac{1}{\pi}\int_{\pi+\Phi+\theta_R}^{\pi} v_{ac,pri}(\varphi) i_a(\varphi)\mathrm{d}\varphi \\
&= \int_{\pi+\Phi+\theta_R}^{\pi} \frac{V_{dc,pri}}{\pi}\left[\frac{V_{dc,pri}}{\omega L_{tot}}(\varphi-\pi-\Phi-\theta_R) + \frac{n_T V_{dc,sec}}{\omega L_{tot}}(\varphi-\pi-\Phi-\theta_R) + I_3\right]\mathrm{d}\varphi \\
&= -\frac{V_{dc,pri}^2 - n_T V_{dc,pri} V_{dc,sec}}{\pi\omega L_{tot}}\left(\frac{\Phi^2}{2} + \frac{\pi\Phi}{2} + \frac{\pi\theta_R}{2} + \frac{\Phi\theta_R}{2}\right).
\end{aligned} \tag{A.20}$$

Then, the P_{dc} is calculated by summing (A.17) to (A.20), which is expressed as:

$$P_{dc} = \frac{n_T V_{dc,pri} V_{dc,sec}\left(\Phi^2 + \frac{\theta_R^2}{6} + \pi\Phi\right)}{\pi\omega L_{tot}}. \tag{A.21}$$

A.1.3 Condition of $0 < \Phi \le \frac{\pi}{2} < \theta_R$ and $\pi < \Phi + \theta_R$

$$v'_{ac,sec}(\varphi) = \begin{cases} -\dfrac{2n_T V_{dc,sec}}{\theta_R}(\varphi + \pi - \Phi) + n_T V_{dc,sec}, & 0 < \varphi < \theta_R + \Phi - \pi, \\ -n_T V_{dc,sec}, & \theta_R + \Phi - \pi < \varphi < \Phi, \\ \dfrac{2n_T V_{dc,sec}}{\theta_R}(\varphi - \Phi) - n_T V_{dc,sec}, & \Phi < \varphi < \pi, \\ -v'_{ac,sec}(\varphi - \pi), & \pi < \varphi < 2\pi. \end{cases} \tag{A.22}$$

$$\varphi_c = \frac{n_T V_{dc,sec}(\Phi - \pi)}{V_{dc,pri} + n_T V_{dc,sec}} + \frac{\theta_R}{2}. \tag{A.23}$$

$$
i_{\mathrm{a}}(\varphi)=\begin{cases}
\dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\dfrac{\varphi^2}{\theta_{\mathrm{R}}}-\varphi\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left[\dfrac{(\varphi+\pi-\Phi)^2}{\theta_{\mathrm{R}}}-\dfrac{(\pi-\Phi)^2}{\theta_{\mathrm{R}}}-\varphi\right]+I_0, & 0<\varphi<\varphi_c,\\
\dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\dfrac{\varphi^2}{\theta_{\mathrm{R}}}-\varphi-\dfrac{\varphi_c^2}{\theta_{\mathrm{R}}}+\varphi_c\right)\\
\quad+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left[\dfrac{(\varphi+\pi-\Phi)^2}{\theta_{\mathrm{R}}}-\dfrac{(\varphi_c+\pi-\Phi)^2}{\theta_{\mathrm{R}}}-\varphi+\varphi_c\right]+I_1, & \varphi_c<\varphi<\Phi+\theta_{\mathrm{R}}-\pi,\\
\dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left[\dfrac{\varphi^2}{\theta_{\mathrm{R}}}-\varphi-\dfrac{(\Phi+\theta_{\mathrm{R}}-\pi)^2}{\theta_{\mathrm{R}}}+(\Phi+\theta_{\mathrm{R}}-\pi)\right]\\
\quad+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}(\varphi+\pi-\Phi-\theta_{\mathrm{R}})+I_2, & \Phi+\theta_{\mathrm{R}}-\pi<\varphi<\Phi,\\
\dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}\left(\dfrac{\varphi^2}{\theta_{\mathrm{R}}}-\varphi-\dfrac{\Phi^2}{\theta_{\mathrm{R}}}+\Phi\right)+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left[-\dfrac{(\varphi-\Phi)^2}{\theta_{\mathrm{R}}}+\varphi-\Phi\right]+I_4, & \Phi<\varphi<\theta_{\mathrm{R}},\\
\dfrac{V_{\mathrm{dc,pri}}}{\omega L_{\mathrm{tot}}}(\varphi-\theta_{\mathrm{R}})+\dfrac{n_T V_{\mathrm{dc,sec}}}{\omega L_{\mathrm{tot}}}\left[-\dfrac{(\varphi-\Phi)^2}{\theta_{\mathrm{R}}}+\dfrac{(\theta_{\mathrm{R}}-\Phi)^2}{\theta_{\mathrm{R}}}+\varphi-\theta_{\mathrm{R}}\right]+I_5, & \theta_{\mathrm{R}}<\varphi<\pi.
\end{cases}
\tag{A.24}
$$

where I_0 to I_5 are derived as:

$$
\begin{cases}
I_0=\dfrac{1}{\omega L_{\mathrm{tot}}}\left[V_{\mathrm{dc,pri}}\left(\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\mathrm{dc,sec}}\left(\dfrac{(\pi-\Phi)^2}{\theta_{\mathrm{R}}}-\dfrac{3\pi}{2}+\Phi+\dfrac{\theta_{\mathrm{R}}}{2}\right)\right],\\
I_1=\dfrac{1}{\omega L_{\mathrm{tot}}}\left[V_{\mathrm{dc,pri}}\left(\dfrac{\varphi_c^2}{\theta_{\mathrm{R}}}-\varphi_c+\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\mathrm{dc,sec}}\left(\dfrac{(\varphi_c+\pi-\Phi)^2}{\theta_{\mathrm{R}}}-\varphi_c-\dfrac{3\pi}{2}+\Phi+\dfrac{\theta_{\mathrm{R}}}{2}\right)\right],\\
I_2=\dfrac{1}{\omega L_{\mathrm{tot}}}\left[V_{\mathrm{dc,pri}}\left(\dfrac{(\Phi+\theta_{\mathrm{R}}-\pi)^2}{\theta_{\mathrm{R}}}-\Phi-\dfrac{\theta_{\mathrm{R}}}{2}+\dfrac{\pi}{2}\right)+n_T V_{\mathrm{dc,sec}}\left(\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)\right],\\
I_3=\dfrac{1}{\omega L_{\mathrm{tot}}}\left[V_{\mathrm{dc,pri}}\left(\dfrac{\Phi^2}{\theta_{\mathrm{R}}}-\Phi-\dfrac{\pi}{2}+\dfrac{\theta_{\mathrm{R}}}{2}\right)+n_T V_{\mathrm{dc,sec}}\left(\dfrac{\pi}{2}-\dfrac{\theta_{\mathrm{R}}}{2}\right)\right],\\
I_4=\dfrac{1}{\omega L_{\mathrm{tot}}}\left[V_{\mathrm{dc,pri}}\left(\dfrac{\theta_{\mathrm{R}}}{2}-\dfrac{\pi}{2}\right)+n_T V_{\mathrm{dc,sec}}\left(-\dfrac{\Phi^2}{\theta_{\mathrm{R}}}+\Phi+\dfrac{\pi}{2}-\dfrac{\theta_{\mathrm{R}}}{2}\right)\right],\\
I_5=\dfrac{1}{\omega L_{\mathrm{tot}}}\left[V_{\mathrm{dc,pri}}\left(\dfrac{\pi}{2}-\dfrac{\theta_{\mathrm{R}}}{2}\right)+n_T V_{\mathrm{dc,sec}}\left(-\dfrac{(\pi-\Phi)^2}{\theta_{\mathrm{R}}}+\dfrac{3\pi}{2}-\Phi-\dfrac{\theta_{\mathrm{R}}}{2}\right)\right].
\end{cases}
\tag{A.25}
$$

The i_{dc} is expressed as (A.26).

$$
\begin{aligned}
i_{\mathrm{dc}}=\frac{n_T V_{\mathrm{dc,sec}}}{\pi\omega L_{\mathrm{tot}}}\Bigg(&\frac{\Phi^4-2\pi^3\Phi-2\pi\Phi^3+3\pi^2\Phi^2}{3\theta_{\mathrm{R}}^2}+\frac{\pi^4}{6\theta_{\mathrm{R}}^2}\\
&+\frac{6\pi^2\Phi-6\pi\Phi^2-2\pi^3}{3\theta_{\mathrm{R}}}+\pi^2+\Phi^2+\frac{\theta_R^2}{6}-\pi\Phi-\frac{2\pi\theta_{\mathrm{R}}}{3}\Bigg).
\end{aligned}
\tag{A.26}
$$

APPENDIX B

SELECTED CAPACITORS AND SEMICONDUCTOR DEVICES

Table B.1
Selected Capacitors

Manufacturer	Series/Type
TDK	B2562
	B2563
	B2568
	B2569
	B43541
	B43548
KEMET	C4AE
	C4AQ
	C44U
	C44P
Vishay	MKP1848
Nichicon	LGW
	LNC

Table B.2
Selected IGBTs

Manufacturer	Series/Type	Manufacturer	Series/Type
Infineon	FZ250R65KE3	IXYS	IXYL40N250CV1
	FF200R33KF2C		IXYL50N170CV1
	FF150R17KE4		IXYN30N170C1
	FF200R17KE3		IXYN50N170CV1
	FF200R17KE4		IXYK30N170CV1
	FF225R17ME4		IXGH32N90B2D1
	FF225R17ME4P		IXYH40N90C3D1
	FF50R12RT4		IXYN80N90C3H1
	FF75R12RT4		IXXX100N75B4H1
	FF100R12KS4		ITF48IF1200HR
	FF100R12RT4		IXA33IF1200HB
	FF150R12KE3G		IXA37IF1200HJ
	FF150R12KS4		IXA45IF1200HB
	FF150R12KT3G		IXA60IF1200NA
	FF150R12MS4G		IXGH40N120C3D1
	FF150R12RT4		IXGT30N120B3D1
	FF200R12KE3		IXGT40N120B2D1
	FF200R12KE4		IXYB82N120C3H1
	FF200R12KE4P		IXYH30N120C3D1
	FF200R12KS4		IXYH40N120B3D1
	FF200R12KS4P		IXYH40N120C3D1
	FF200R12KT3		IXYN82N120C3H1
	FF200R12KT4		IXYN100N120C3H1
	FF225R12ME4		IXYR50N120C3D1
	FF225R12ME4P		MII75-12A3
	FF225R12MS4		MII100-12A3
	IKQ40N120CH3		MII145-12A3
	IKQ40N120CT2		MII150-12A4
	IKQ50N120CH3		MII200-12A4

	IKQ50N120CT2
	IKQ75N120CH3
	IKQ75N120CS6
	IKQ75N120CT2
	IKW40N120CS6
	IKW40N120H3
	IKW40N120T2
	IKW40T120
	IKY40N120CH3
	IKY40N120CS6
	IKY50N120CH3
	IKY75N120CH3
	IKY75N120CS6
	AIKW40N65DF5
	AIKW40N65DH5
	AIKW50N65DF5
	AIKW50N65DH5
	IHW30N65R5
	IHW40N65R5
	IHW50N65R5
	AIKW30N60CT
	AIKW50N60CT
	AIKW75N60CT
	AUIRGP4063D
	AUIRGPS4070D0
	FF200R06KE3
	IKQ100N60T
	IKQ120N60T
	IKW30N60DTP
	IKW30N60H3
	IKW30N60T
	IKW40N60DTP
	IKW40N60H3
	IKW50N60DTP
	IKW50N60H3
	IKW50N60T
	IKW60N60H3
	IKW75N60H3
	IKW75N60T
Dynex	DIM100PHM33
	DIM125PHM33-TL
	DIM125PHM33-TS
	DIM200PHM33
ABB	5SNG0150P450300
	5SNG0150Q170300
	5SNG0200Q170300
Powerex	QIC6508001
	QID4515002
	QID4515004
	QID4520002
	QID3310006
	QID3320002
	QID3320004
	MII300-12A4
	IXXH30N65B4D1
	IXXH40N65B4D1
	IXXH40N65B4H1
	IXXH40N65C4D1
	IXXH60N65B4H1
	IXXH80N65B4D1
	IXXH80N65B4H1
	IXXN110N65B4H1
	IXXN110N65C4H1
	IXXR110N65B4H1
	IXXX110N65B4H1
	IXXX140N65B4H1
	IXYH40N65C3H1
	IXYH50N65C3D1
	IXYH50N65C3H1
	IXYH75N65C3D1
	IXYH75N65C3H1
	IXYN75N65C3D1
	IXYN100N65B3D1
	IXYN120N65B3D1
	IXYN120N65C3D1
	IXYQ30N65B3D1
	IXYQ40N65B3D1
	IXYQ40N65C3D1
	IXYX100N65B3D1
	IXYX100N65C3D1
	IXDH35N60BD1
	IXGH48N60C3D1
	IXGH60N60C3D1
	IXGN72N60C3H1
	IXGR72N60B3H1
	IXGX72N60B3H1
	IXXH30N60B3D1
	IXXH30N60C3D1
	IXXH50N60B3D1
	IXXH50N60C3D1
	IXXH75N60B3D1
	IXXH75N60C3D1
	IXXN200N60B3H1
	IXXN200N60C3H1
	IXXR100N60B3H1
	IXXX100N60B3H1
	IXYH50N120C3D1
	IXYN100N65C3H1
	IXGA30N60C3C1
	IXGH36N60B3C1
	IXGH48N60B3C1
	IXGH48N60C3C1
	IXGR60N60C3C1
SemiQ	GPA030A135MN-FDR

MITSUBISHI	CM200HG-130H	
	CM75DY-34A	
	CM75DY-34T	
	CM100DY-34A	
	CM100DY-34T	
	CM150DX-34SA	
	CM150DY-34A	
	CM150DY-34T	
	CM200DX-34SA	
	CM200DY-34A	
	CM200DY-34T	
	CMH100DY-24NFH	
	CMH150DY-24NFH	
	CMH200DU-24NFH	

Table B.3
Selected MOSFETs

Manufacturer	**Series/Type**	**Manufacturer**	**Series/Type**
Infineon	SPW55N80C3	IXYS	IXFB44N100Q3
	IPB65R050CFD7A		IXFB70N100X
	IPBE65R050CFD7A		IXFN70N100X
	IPP65R045C7		IXFX52N100X
	IPP65R050CFD7A		IXFB52N90P
	IPT65R033G7		IXFN56N90P
	IPW65R019C7		IXFB90N85X
	IPW65R035CFD7A		IXFN66N85X
	IPW65R037C6		IXFN90N85X
	IPW65R041CFD		IXFT50N85XHV
	IPW65R048CFDA		IXFX66N85X
	IPW65R050CFD7A		IXFB50N80Q2
	IPP60R040C7		IXFB60N80P
	IPT60R028G7		IXFB62N80Q3
	IPW60R017C7		IXFN50N80Q2
	IPW60R024CFD7		IXFN60N80P
	IPW60R024P7		IXFN62N80Q3
	IPW60R031CFD7		IXFX44N80Q3
	IPW60R037P7		IXFB150N65X2
	IPW60R040C7		IXFH46N65X2
	IPW60R040CFD7		IXFH60N65X2
	IPW60R041P6		IXFH60N65X2-4
	IPW60R045CPA		IXFH80N65X2
	IPW60R045P7		IXFH80N65X2-4
	IPW60R060P7		IXFN100N65X2
	IPW60R070P6		IXFN120N65X2
	IPZ60R017C7		IXFN150N65X2
	IPZA60R024P7		IXFN170N65X2
	AIMW120R045M1		IXFN90N170SK
	IMW120R030M1H		IXFN50N120SiC
	IMZ120R030M1H		IXFN70N120SK
	IMW120R045M1		IXFT60N50P3

	IMZ120R045M1	IXFX94N50P2
	IMW65R027M1H	IXFX80N50Q3
Cree	C2M0045170D	IXFT60N65X2HV
	CAS300M17BM2	IXFT80N65X2HV
	C2M0025120D	IXFX100N65X2
	C2M0040120D	IXFX120N65X2
	C3M0016120D	IXTH48N65X2
	C3M0021120D	IXTH52N65X
	C3M0021120K	IXTH62N65X2
	C3M0032120D	IXTH64N65X
	CAS120M12BM2	IXTH80N65X2
	C3M0030090K	IXTN102N65X2
	C3M0015065D	IXTR102N65X2
Rhom	BSM080D12P2C008	IXTX102N65X2
	BSM120D12P2C005	IXTX120N65X2
	BSM180D12P2C101	IXFX48N60Q3
	BSM180D12P2E002	IXFT50N60P3
	BSM180D12P3C007	IXFH60N60X
	BSM250D17P2E004	IXKH70N60C5
	SCT3022KLHR	IXFX80N60P3
	SCT3030KLHR	IXFX90N60X
	SCT3040KLHR	IXFB110N60P3
	SCT3040KR	IXFB132N50P3
	SCT3017ALHR	IXFB120N50P2
	SCT3022ALHR	IXFB100N50Q3
	SCT3030ALHR	
	SCT3030AR	

APPENDIX C

SELECTED MAGNETIC MATERIAL DATA

C.1 B-H Curve Fitting

To describe the characteristics of magnetic materials, an approach has been developed in [162]. The anhysteretic relationship between flux density B and field intensity H is expressed as a function of H or as a function of B.

$$\begin{aligned} B &= \mu_H(H)H \\ \mu_H(H) &= \mu_0 + \sum_{k=1}^{K} \frac{m_k}{h_k} \frac{1}{1+|H/h_k|^{n_k}} \end{aligned} \tag{C.1}$$

$$\begin{aligned} B &= \mu_B(B)H \\ \mu_B(B) &= \mu_0 \frac{r(B)}{r(B)-1} \\ r(B) &= \frac{\mu_r}{\mu_r - 1} + \sum_{k=1}^{K} \alpha_k |B| + \delta_k \ln\left(\varepsilon_k + \zeta_k e^{-\beta_k |B|}\right) \\ \delta_k &= \frac{\alpha_k}{\beta_k},\ \varepsilon = \frac{e^{-\beta_k \gamma_k}}{1+e^{-\beta_k \gamma_k}},\ \zeta_k = \frac{1}{1+e^{-\beta_k \gamma_k}}. \end{aligned} \tag{C.2}$$

Based on this method, the characteristic of Hitachi FT-3M is illustrated in Figs. C.1 and C.2. The parameters of TDK N87, METGLAS 26605-SA1 can be found in [177, 178]. More parameters are of ferrite materials available in [162], including MN8CX, MN60LL, MN67, MN80C. For other magnetic materials, the parameters are listed in Tables C.1 and C.2.

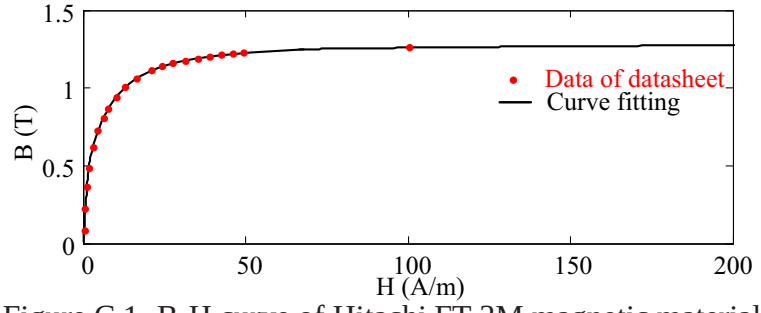
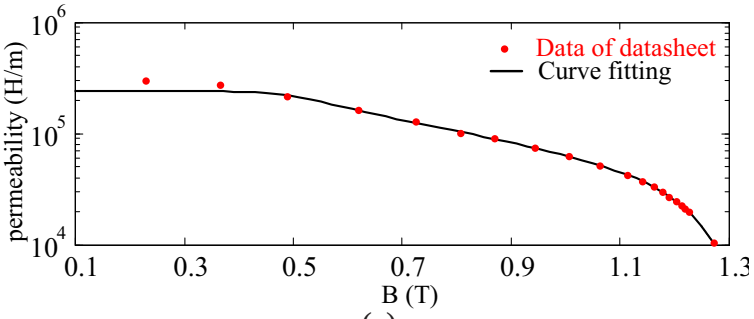


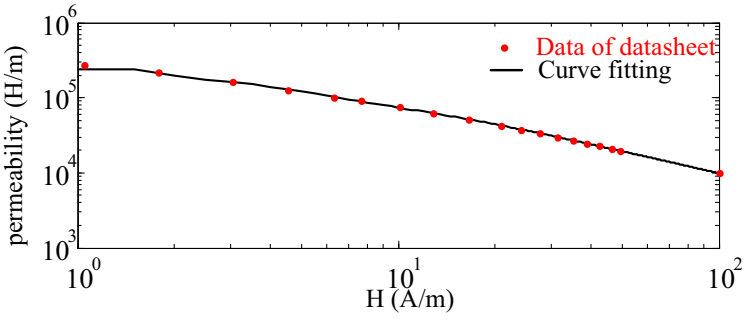
Figure C.1. B-H curve of Hitachi FT-3M magnetic material.

C.2 Steinmetz Equation Parameters

The parameters of Steinmetz equations are also available by curve fitting method, which are listed in Table C.3. More parameters are of ferrite materials available in [162], including MN8CX, MN60LL, MN67, MN80C.



(a)



(b)

Figure C.2. Permeability of Hitachi FT-3M magnetic material as function of (a) flux density *B*, and (b) field intensity *H*.

Table C.1

Parameters of Permeability (μ_H)

Magnetic Material	m_k	n_k	h_k
3C90	2.0019×10^{-6}	0.002	912.5709
	0.3274	2.2513	60.2897
	0.3525	0.0023	138.1937
	0.2734	2.2504	133.0681
FT-3M	1.4026	1.6163	13.4186
	0.4543	3.3356	4.3085
	1.268	1.0246	46.428
	0.1294	13.2479	1.8823

Table C.2

Parameters of Permeability (μ_B)

Magnetic Material	μ_r	α_k	β_k	γ_k
3C90	7828.1	0.00027312	0.0583	0.4246
		0.0024	12.8364	463.0486
		12.2122	27.6667	0.6858
		1.6423	0.0709	173.3499
FT-3M	242040	3.804	4.5276	38.132
		1.4566×10^{-5}	29.5438	0.4945
		2.6198	29.47267	1.5268
		10.7855	7.497	2.6978

Table C.3

Steinmetz Equation Parameters for Estimation of Core Loss

Magnetic Material	K_c	α	β
3C90	0.6415	1.566	2.7107
N87	60.0771	1.1299	2.3426
METGLAS 2605-SA1	0.8228	1.5353	1.7368
Hitachi FT-3M	3334.22	0.5012	2.1355