Measurements and Simulations of Self-Heating in 40nm SOI MOSFETs

by

Xiong Zhang

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved November 2020 by the
Graduate Supervisory Committee:

Trevor Thornton, Chair
Dragica Vasileska
Michael Goryll
Stefan Myhajlenko

ARIZONA STATE UNIVERSITY

December 2020

ABSTRACT

Combining the rapid development of semiconductor technologies, miniaturization of integrated circuits (ICs), and scaling down the device size is trending towards faster, cheaper, and more reliable components for low-power integrated circuits. Most research and development relate to efficiency, structure, materials, and performance. However, the thermal problem is also created and becomes more critical with shrinking device dimensions and increased integration densities, such that it affects the device performance and leads to degradation and damage. At the nanometer scale, the self-heating effect (SHE) is one of the main factors to degrade devices. Therefore, tracking and quantifying the SHE is important for reliability and efficiency issues. In this dissertation, engineers design two identical and closely spaced 40nm gate length silicon-on-insulator (SOI) n-channel metal-oxide-semiconductor-field-effect transistors (NMOSFETs) that share a common source with the same active silicon region. One of the MOSFETs acts as a heater to heat-up the active region, while the other one is a thermometer to evaluate the SHE and local temperature changes. The thermometer provides a method to calibrate the numerical models of self-heating and track the heat flow. Moreover, it also involves a trap-rich SOI wafer technology, in which a trap-rich layer, with higher resistivity and lower thermal conductivity compared to conventional bulk silicon substrates. The trap-rich SOI substrates can reduce the cross-talk and minimize the power consumption to increase the system performance. In particular, it offers a solution to radio frequency integrated circuits (RFICs) which require fast switching and low leakage. In high power amplifier (PA) applications, Watt-level PAs operates at less than 50% efficiency because of temperature limitations. The author uses experimental measurements of the local temperature changes, combined

with simulations to examine the heat flow and temperature distribution. The approach may be useful to build a self-test application, because it can quantify the temperature changes by putting one or multiple NMOSFET thermometers around a complementary metal-oxide-semiconductor (CMOS) power amplifier, while only adding minimum die area. It points to ways in which it can optimize the reliability of RFIC applications, which operate under high-temperature or high-power conditions to protect the device before it is overheated or damaged.

To my parents and my wife

I would express my deepest appreciation to my parents, Mr. Chaoming Zhang and Mrs. Shiqiong Peng, for their great encouragement and unconditional support during all my life. It is my pleasure and honor to be born in such a happy family. Then I would like to extend my heartfelt gratitude to my wife, Mrs. Huan Li, who always gives her generous support and never withdraw even when I was the hardest struggling time.

ACKNOWLEDGMENTS

Firstly, I would like to appreciate my adviser, Professor Trevor Thornton. Without his continued patience and kindly guidance, this project would never be finished by any possibility. During the past four years, his profound professional knowledge and patience let me redefine the word, ‘advisor’, he is not only caring the academic skills in research areas as a professor, but also concerning students’ daily lives as an eldership. He always tries to give his generous support to help me in a reliable and dependable position to continue my study. Moreover, he provides me a good experience with how to go through a completed project, from the basic background research to write a professional journal or a conference paper, includes how to describe texts and analysis figures to draw the conclusions. Truthfully, I really feel grateful for his everlasting investment and support of time and efforts in my research.

Then I would thank to my faculty committee members, Professor Dragica Vasileska, Professor Michael Goryll and Dr. Stefan Myhajlenko. I appreciate their constructive suggestions and comments, they teach me how to run a research project rigorously, and the target will be never achieved without strong volition and persistence. It would influence me all the time.

Last but not least, many thanks to members of our research group, Dr. Raymond Tsui, Dr. Som Dahal, Dr. Carrie Sinclair, Dr. Payam Habibi-Mehr, Muhammad Faizan Ahmad, and Vishal Jha, who are kindly to support me during my whole Ph.D. period. They let me feel that we are all in one group and fight for each small goal together. It is helpful for me to study and work with them as a team.

TABLE OF CONTENTS

Page

LIST OF TABLES vii

LIST OF FIGURES viii

CHAPTER

1 INTRODUCTION 1

1.1. Background Knowledge 3

1.2. Silicon-On-Insulator (SOI) MOSFETs 7

1.3. Self-Heating in SOI Devices 10

1.4. Trap-Rich, High Resistivity Substrates SOI MOSFETs 12

2 EXPERIMENTAL DETAILS AND METHOD 15

2.1.Device Use and Layout Details 16

2.2. NFET Heater Characteristics 18

2.3. NFET Thermometer Calibration 21

3. MEASUREMENT RESULT AND TWO DIFFERENT TYPES OF SOI SUBSTRATE COMPARISION 25

3.1. Self-Heating Characteristics 25

3.2. Trap-Rich, High Resistivity Substrate and Bulk Silicon Substrate SOI MOSFETs Performance Comparison 28

4. SILVACO SIMULATION 34

4.1. Overview 35

4.2. SOI MOSFETs Device Modeling 36

4.2.1. Three-Terminals Modeling 37

CHAPTER Page

4.2.2. Ion Implantation Model 42

4.2.3. Five-Terminals Modeling 44

4.3. Theoretical Model 46

4.3.1. Fourier Law of Thermal Conduction 47

4.3.2. Drift-Diffusion (DD) Transport Model 48

4.3.3. Hydrodynamic Transport Model 50

4.4. Temperature Distribution Comparison Between Trap-Rich, High Resistivity Substrate and Conventional Bulk Silicon Substrate SOI Device 51

5. DISCUSSION AND SUMMARY 55

5.1. Mesh Convergency 55

5.2. Metal Contact Material 58

5.3. Thermal Boundary 59

5.4. Summary and Further Plan 60

REFERENCES 64

APPENDIX

A SILVACO SIMULATION CODE 69

LIST OF TABLES

Table Page

4.1. Implantation Details for the Device Modeling in Athena 43

4.2. A Comparison Between the Temperature Captured on the Thermometer NFET Measurements and Simulation Results for Two Types of SOI Substrate Device without Thick Metal Contact 54

4.3. A Comparison Between the Temperature Captured on the Thermometer NFET Measurements and Simulation Results for Two Types of SOI Substrate Device with 2 μm Thick Metal Contact 54

5.1. Insulator Material Properties Comparison 62

LIST OF FIGURES

Figure Page

1.1. Energy Band Diagram for Insulators, Semiconductors, and Conductors 3

1.2. Direct and Indirect Bandgap Semiconductors 5

1.3. 2D Cross-section View for Comparison Between Bulk CMOS and SOI CMOS Device Structure 8

1.4. 2D Cross-section View for Comparison Between PD-SOI and FD-SOI Transistor Structure 9

1.5. The Path of Heating Flow Generating and Dissipating Through the Inside of Semiconductors by Optical and Acoustic Phonon Emission under Different Timing Window [7] 11

1.6. 2D Cross-section View for Trap-rich, High Resistivity Substrate SOI MOSFET Structure 13

2.1. Layout of the 40 nm Gate Length NFET Pairs Where the Gap Between the Gates is 150nm. The NFETs Pair Share a Common Source Contact and the Same Active Silicon Region with Area 500 nm x 470 nm 16

2.2. Pad Configuration of the 40 nm SOI Devices, Five Terminals to Contact Five Different Pads, and Each of the Bond Pads Size is 96 x 96 um^2 17

2.3. Cascade Microtech 11000 Probe Station with Five Probes 18

2.4. Device to Device Variation Comparison for Turn-on Characteristics Curve Based on a Same Die of Conventional Low Resistivity SOI Substrate Devices 19

Figure Page

2.5. Family-of-curves Comparison for the Conventional Low Resistivity SOI Substrates Devices of 40 nm Gate Length NFET with the Total Channel Width 500nm 20

2.6. Sub-threshold Slope (SS) as Defined in the Turn-on Characteristics Curve Using a Log Scale for the Current Drive 22

2.7. Gate Voltage Vs. Log Scale of Drain Current, Shows the Various Sub-threshold Slope (SS) Values Present under Different Temperatures Applied by the Hot Chuck of the Probe Station 23

2.8. SS Values of the Thermometer Increase with Chuck Temperature Increased. The Red Line Indicates a Polynomial Fit to the SS Values Used for the Thermometer Temperature Calibration 24

3.1. The Relationship Between the Thermometer Temperature Changes and the Heater Power Dissipated, The Red Line is a Quadratic Fit for All Different Gate Voltages Biased Under 0.5V (Solid Triangles), 0.75V (Open Squares), 1V (Open Circles), Respectively....................27

3.2. Comparison Between Trap-rich, High Resistivity SOI Substates with Conventional Bulk Silicon SOI Substrates for the Relationship Between Gate Voltage and Drain Current....................29

3.3. Sub-threshold Slope as a Function of Temperature Captured on the Thermometer, and the Device-to-device Variation Shown by Error Bars. The Open Red Squares Represent Trap-rich, High Resistivity SOI Substrates, and the Open Blue Circles Represent Conventional Bulk Silicon SOI Substrates 30

Figure Page

3.4. Family-of-curves for 40 nm Gate Length NFETs on SOI Substrates, the Curves Present Different Gate Voltage Conditions, from 0.2V to 1V with Step 0.1V, and the Error Bars Indicate the Difference Between Two Different Types of Substrate Devices 31

3.5 Changes in Temperature of The Calibrated Thermometer with Applied Heater Power for Both Trap-rich, High Resistivity SOI Substrates (Open Red Circles) and Conventional Bulk Silicon SOI Substrates (Open Blue Squares) 32

4.1. 3D Version of the NFET Pairs of Heater and Thermometer Structure with Interconnect Wiring up to Metal-2 Contact 37

4.2. 2D Cross-section of a 45-nm SOI CMOS Process Metal Stack-up. All Metal Layers are Copper, Except the Aluminum for the Top Metal [11].......................38

4.3. 2D Cross-section for a Three-terminal SOI Device with 40 nm Gate Length, 80 nm Active Silicon Region, and 225 nm for the Insulating BOX Layer, and More Mesh Points Distributed in Channel Area 39

4.4. Cutline Through the Gate to the Active Silicon Region. The Open Green Squares Present Active Phosphorus Doping Level, 2E14 cm^{-3}, and the Red Crossed Solid Line Presents the Active Boron Doping Level, 1E17 cm^{-3} in Active Silicon Region 40

4.5. Family-of-curves Comparison for Measurement and Simulation Results by Using the Exact Same Bias Voltage Condition. The Drain Voltage is Swept From 0 to1 V, and Bias Different Gate Voltages, 0.5V, 0.75V, 1V, Respectively 41

Figure Page

4.6. Comparison of the Turn-on Characteristics Measurement and Simulation Results by Using the Exact Bias Voltage Conditions. The Gate Voltage is Swept From -0.5V to 1V, and the Drain Voltage Bias is Set At 0.1V 42

4.7. Functions of Ion Implantation in a N-channel MOSFET....................................44

4.8. 2D Cross-section for Five-terminals SOI Device with 40 nm Gate Length, 225 nm Thickness for the Buried Oxide layer, and Both Devices Share an 80 nm Thick Active Silicon Region. The Red Bottom Region Indicates Polysilicon Formed by a Chemical Vapor Deposition Step with One-micron Thickness 45

4.9. Summary of Drift Diffusion (DD) Transport Mechanisms 48

4.10. Temperature Distribution for 40 nm Gate Length SOI NFET Pairs 52

4.11. A Closer Look at the Temperature Distribution, the Heat Transfer from High Temperature to Lower Temperature, and the Thermometer Temperature is Around 20-Degree Celsius Lower Compared to the Heater Temperature 52

5.1. Comparison Between Measurement and Simulation Results for Conventional Bulk Silicon Substrate with Mesh Convergency Problem for Vg=0.75V (Middle Open Black Square Curve) 56

5.2. Comparison Between Simulated Family-of-curves for Both Two Types of Substrate Under Various Gate Voltages, 0.5V, 0.75, 1V. The Open Black Squares Represent Conventional Bulk Silicon Substrate, While the Open Red Circles Present Trap-rich, High Resistivity Substrate Devices by Using 'Gummel Block Newton' Method 57

Figure Page

5.3. Comparison of Simulated Family-of-curves for Various Substrate Thickness. The Open Circles are for Substrate Thickness=0.1 μm, Squares for Substrate Thickness=1 μm, Triangles for Substrate Thickness=5 μm, Bias Under Different Gate Voltage, 0.5V, 0.75V, 1V, Respectively 59

5.4. Comparison of the Simulated Temperature Determined for Different Substrate Thickness. The Blue Solid Circles are for a Substrate Thickness=0.1 μm, Red Open Squares for Substrate Thickness=1 μm, and Black Open Triangles for Substrate Thickness=5 μm 60

CHAPTER 1

INTRODUCTION

In 1965, Gordon Moore published a prediction of the technology roadmap for semiconductors, projecting that the number of transistors will be doubled every eighteen to twenty-four months for integrated circuits, and the performance also gets doubled. It became the famous ‘Moore’s law’, but it is not a law of nature, only an observation of the outcome and a prediction of the future. But combined with both marketing demands and manufacturer supplications, Moore’s law is a dynamically balanced solution that leads to many useful predictions for the semiconductor field. For the last fifty years, the whole of semiconductor industries focuses to follow up and extend Moore’s law, and it leads to faster, cheaper, more integrated, and reliable integrated circuits with lower power consumption.

Nowadays, Moore’s law has transitioned to the “more than Moore” generation due to the increasingly stringent industrial demands. Manufacturing technologies require the fabrication of faster and smaller devices, with reduced leakage, higher efficiency, and that are more reliable in specific environments. Engineers follow three ways to extend and develop Moore’s law; the first one, continuing to shrink the dimensions of devices, for example, Taiwan Semiconductor Manufacturing Company (TSMC) is mass-producing a 5 nm technology in 2020 and is developing a 3 nm technology for release in 2021. However, with the continuous scaling-down of device size, there are more and more difficulties in technology development, and the need for high investment to reach smaller size with high levels of integration. The second approach involves the exchange of device materials, for example, from traditional group IV silicon to III-V groups materials, such as InGaAs,

because of the high carrier mobility and special optical properties. Other materials include GaN and group IV materials, SiC and diamond. Because of their higher energy bandgap, SiC and diamond can operate under higher temperature and higher power environments compared to traditional silicon devices. The third approach is to exchange the device structure. For example, the fin field-effect transistor (FINFET) exchanges the traditional planar metal-oxide-semiconductor field-effect transistor (MOSFET) in some applications. Due to the lower equivalent input capacitance and effect of channel quantization, it can provide higher output currents, higher switching speeds, and lower power consumption. At the moment, the FINFET structure technique becomes the main development path for under 20 nm technologies. Furthermore, the nanosheet and nanowire transistors moves towards the nanometer-scale due to their high aspect ratio, to obtain gate control over the channel more efficiently.

In this study, based on the basic complementary metal-oxide-semiconductor (CMOS) structure, the author uses the fundamental current-voltage curves under direct current (DC) conditions, to characterize factors such as the current drive (I_d), threshold voltage (V_{th}), transconductance (g_m), sub-threshold slope (SS) to explain the working functions of a MOSFET. Then there are comparisons for silicon-on-insulator (SOI) technologies, trap-rich, high resistivity substrates and conventional bulk silicon substrates, including FinFETs, nanosheet, and nanowire transistors. Then those mainstream technologies are used to describe the history of semiconductor manufacturing and future developments.

1.1. Background Knowledge

For the last several decades, silicon technology has grown from a single transistor to hundreds of millions of transistors embedded into highly integrated circuits, a process that has changed the entire world in different ways. It also becomes one of the most important inventions of the 20th century. Silicon, the fundamental material for semiconductor technology, has an energy band gap of 1.12ev at 300K. The energy band gap is the main difference between conductors, semiconductors, and insulators. Then energy band theory explains the ability for free electrons to move from the valence band to the conduction band, and the distance between the valence band and conduction band is called the band gap. Figure 1.1. shows there is no gap for conductors (i.e. ideal metal) and a small band gap for semiconductors, and a wide band gap for insulators. The Fermi level is related to the energy band diagram and is located at the half-way position in the band gap for pure (i.e. undoped) semiconductors. At the absolute zero of temperature all states below the Fermi level are filled with electrons and all states above are empty.

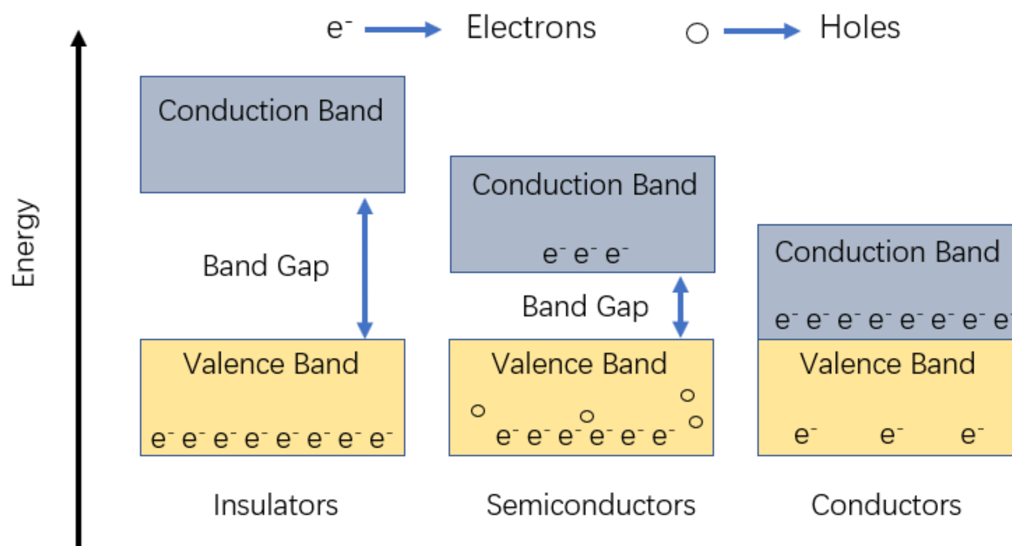

Figure 1.1. Energy band diagram for insulators, semiconductors and conductors.

Wide band gap materials are insulators but can conduct current under high-voltage or high-temperature conditions. Resistivity, and its inverse conductivity, describe the ability of materials to oppose or allow the flow of current generated by the flow of negatively charged electrons. The definitions of resistance, R, and conductance, G, in direct current (DC) conditions under uniform cross-section are described in equations 1.1. and 1.2. However, the equations may need to be adjusted because they assume uniform current density, and an alternating current (AC) condition may not be suitable for this equation, because the skin effect and the geometrical cross-section may be different with an effective cross-section for the actual current flow.

$$G = \sigma \frac{A}{\ell} \tag{1.1}$$

$$R = \rho \frac{\ell}{A} \tag{1.2}$$

where

ρ, rho,is the electrical resistivity and measured in Ohm meters [Ω·m]

L is the length and measured in meters [m]

A is the cross-section area of measured in square meters [m^2]

σ, sigma, is the electrical conductivity and measured in Siemens per meter [$S \cdot m^{-1}$]

Semiconductors can be divided into indirect band gap semiconductor (IBS) and direct band gap semiconductor (DBS) depending on the alignment of the conduction and valence bands in momentum space. If the minimum energy level of the conduction band and the maximum energy level of the valence band are aligned at k=0 in the Brillouin zone, we refer to a direct band gap semiconductor, otherwise, it is called an indirect band gap

semiconductor, as shown in Figure 1.2. For example, iIndium arsenide (InAs), and gallium arsenide (GaAs) are direct band gap materials, while crystalline silicon (Si) and germanium (Ge) are indirect band gap materials.

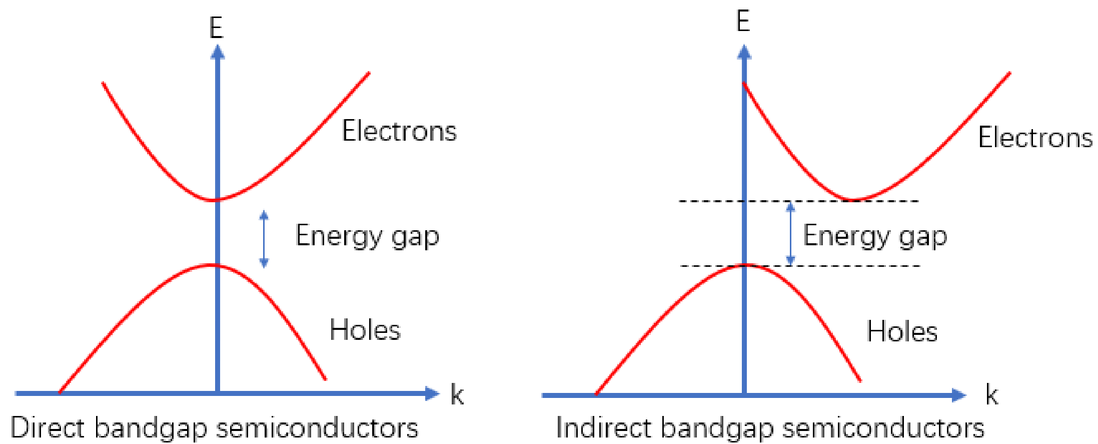

Figure 1.2. Direct and Indirect bandgap semiconductors

In addition, semiconductors also can be divided into intrinsic semiconductors and extrinsic semiconductors by the doping process, which can change the electrical, optical, and structural properties of materials, and a doped semiconductor is referred to as an extrinsic semiconductor. In semiconductors, there are two kinds of carriers, electrons and holes. At the absolute zero of temperature and no external energy excitation condition, the valence electrons are bound by covalent bonds and there are no free electrons in the crystal and the semiconductor cannot conduct electricity. However, when the temperature of the semiconductor increases or the external environment changes, such as light exposure, the valence electrons in some covalent bonds gain enough energy to move from the valence band to the conduction band, and become free electrons, also leaving the same number of free holes. Moreover, a hole is a unique particle in a semiconductor. It has a positive charge,

the same amount of charge as the electron. The transition process resulting from thermal excitation is called intrinsic excitation. Obviously, the number of free electrons and holes generated by the eigen excitations are the same. Then the concentration can be described as either highly or lightly doped for semiconductors, and equation (1.3) and equation (1.4) show the concentration relationship among electrons, holes and intrinsic carrier for intrinsic and extrinsic semiconductors under thermal equilibrium states, respectively.

$$n = p = n_i \tag{1.3}$$

$$n_0 \cdot p_0 = n_i^2 \tag{1.4}$$

where

n is electrons concentrations and measured in [cm^{-3}]

p is holes concentrations and measured in [cm^{-3}]

Finally, there is a significant thermal problem that arises from the continued shrinking of device dimensions due to self-heating. Any increased heat generated during the operating process will affect the device performance due to junction leakage and increased power consumption. In this study, measurements and a numerical simulation model are used to quantify and track the heat flow in nanoscale NMOSFETs. The results suggest a built-in-self-test (BIST) application for power amplifiers (PAs) that may be developed for future use.

1.2. Silicon-On-Insulator (SOI) MOSFETs

The fourth generation of cellular communications systems has been developed for the past years, and engineers are starting to think about the next generation for telecommunications. The so-called ‘5G’ or ‘further 5G’ naturally becomes the solution, and regulation and standardization identification also capture attention around the world. Based on the market investigation, the quantities of devices would increase exponentially, around tens or even hundreds of billions of devices will be needed when the 5G communication system has been built. Therefore, to meet the market demands and the high integration requirements, there is a need to develop more advanced and efficient technologies based on reality and reliability. The requirements for these technologies should allow for high data rate with low latency and energy cost. It indicates that the engineers should design the device by adding more nodes per unit area and Hz (more (bits/s)/Hz per node, more bits/s per unit area, also smaller size of cells), increasing bandwidth, and increasing spectral efficiency [1].

The silicon-on-insulator (SOI) technique fabricates an insulating layer between the silicon channel and the substrate as shown Figure 1.3. [4]. Typically, this layer is made of silicon dioxide or sapphire. The difference between using SiO_2 or sapphire depends on the application, where SiO_2 is more widely used to reduce short-channel effects for microelectronics devices, and sapphire trends to use for radiation-sensitive and high-performance radio frequency (RF) devices [2]. Compared to conventional bulk CMOS, the SOI technique offers higher device performance without continuing to shrink the channel length and gate oxide thickness. Due to the electrical insulator, SOI CMOS is fabricated to

reduce parasitic capacitance, soft-errors, short channel effects, power consumption with higher transistor packing density and circuit performance [3].

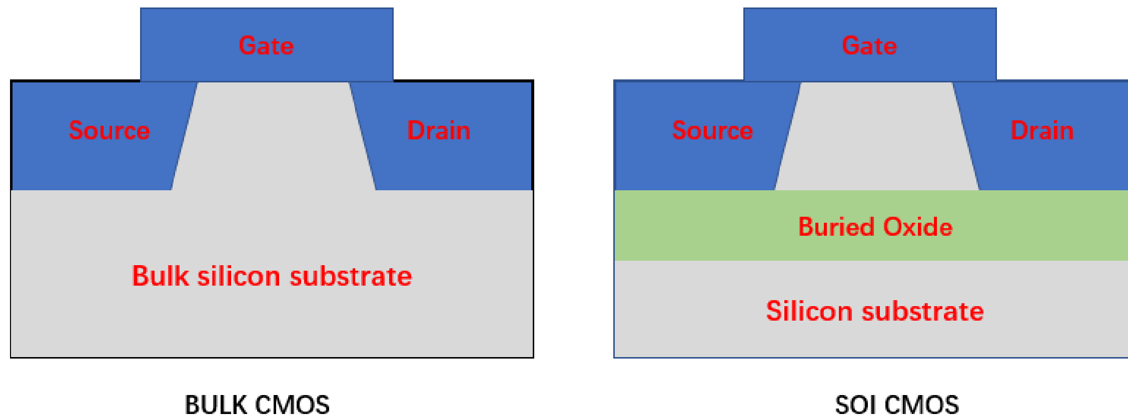

Figure 1.3. 2D cross-section view for comparison between bulk CMOS and SOI CMOS device structure.

There are two types of SOI wafers, partially depleted silicon-on-insulator (PD-SOI) and fully depleted silicon-on-insulator (FD-SOI). As shown Figure 1.4. [4] the main difference between PD-SOI and FD-SOI is the floating body, PD-SOI has a doped channel, the insulating buried oxide (BOX) layer is in the range 100-200 nm thick, and the silicon under the channel is partially depleted of mobile charges carriers leading to the floating body effect. Avalanche ionization at the drain area leads to charge accumulating in the quasi-neutral region. FD-SOI has an undoped or lightly doped channel, the insulating BOX layer is around 5-50 nm, and the ultra-thin body is fully depleted of mobile charges to waive the floating body effect. Both PD-SOI and FD-SOI are targeting high- performance microprocessors. PD-SOI is widely used for 180 nm to 22 nm high-performance applications and FD-SOI devices are more widely to be used in 22 nm and beyond for low-power electronics, because of the ultra-low leakage and power consumption.

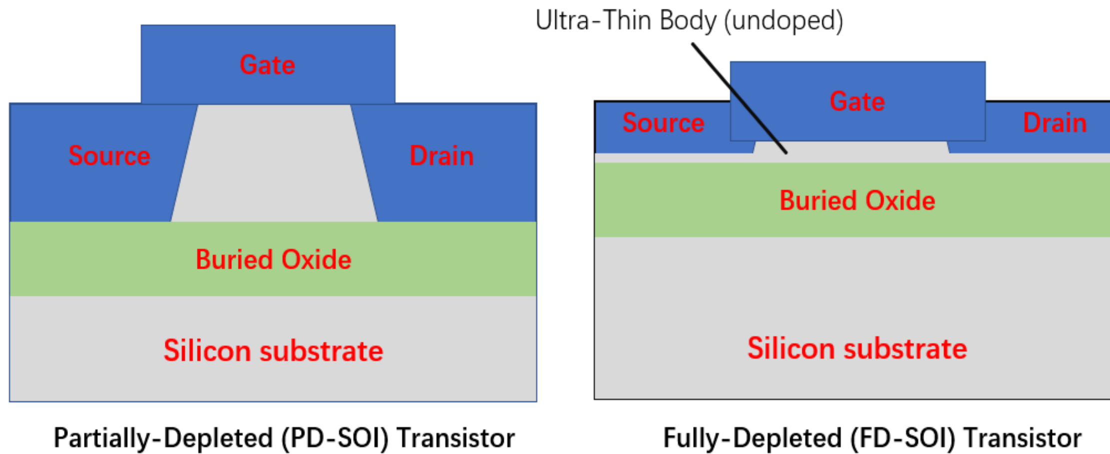

Figure 1.4. 2D cross-section view for comparison between PD-SOI and FD-SOI transistor structure.

In this study, the Global Foundries 45 nm RF silicon-on-insulator (SOI) technology has been used. The insulating BOX layer in the partially depleted SOI technique is around 200 nm thickness, and only contributes a small extra thermal resistance compared to bulk silicon substrates [5]. It comes from the previous IBM 12S0 process with high resistivity silicon (HR-Si) substrate and back-end-of-line (BEOL) thick metal options to get better performance at radio frequency (RF)/mm-Wave [6]. It has been optimized for high-performance and energy-efficient 5G mm-wave transceiver front-ends. As described, the 5G communication system has a higher data rate (>1 Gb/s) and lower latency (<1 ms). In other words, the SOI technique provides a solution to complementary metal-oxide-semiconductor (CMOS) processes because of decreased parasitic capacitance and leakage current, and higher current drive with a better sub-threshold swing. It benefits from the HR-Si substrate, especially for RF integrated circuits, for which it can reduce silicon substrate RF losses and crosstalk. The technology can be widely used for future 5G communication systems. It presents for advance manufacturing standards, low-cost, and

high-volume CMOS foundries [6]. Furthermore, a power amplifier (PA) is one of the most important parts in wireless communication front ends, as it determines the energy efficiency and quality-of-service. The efficiency of PAs depends to some degree on the thermal handling which can also impact reliability [6]. Especially for 5G, highly integrated, mm-Wave and massive multiple-input multiple-output (MIMO) systems [1], these properties require a complicated spectrum-efficient modulation schemes which demand high linearity and high-efficiency of PAs that are reliable and dependable.

1.3. Self-Heating in SOI Devices

As the dimensions of CMOS devices become smaller and smaller, there are more and more devices in a certain area to increase densities, and the resulting temperature increase leads to device degradation or efficiency decrease. Therefore, the self-heating effect (SHE) becomes a signification problem. It may affect device performance and damage the device by over-heating or cause degradation if the device operates under high temperature and high power conditions. Then quantifying and tracking the heating distribution also becomes important and helps to provide a solution about temperature distribution and heating transmission direction.

The heating distribution between devices is a dynamic balance because the heating would generate and dissipate at the same time, and the self-heating effect will affect the device performance due to the heat accumulation in a certain time window. If the rate of generating heat is faster than dissipating, the heating will accumulate in the device and increase the operating temperature, and the path and timing also need consideration as Figure 1.5. shows [7].

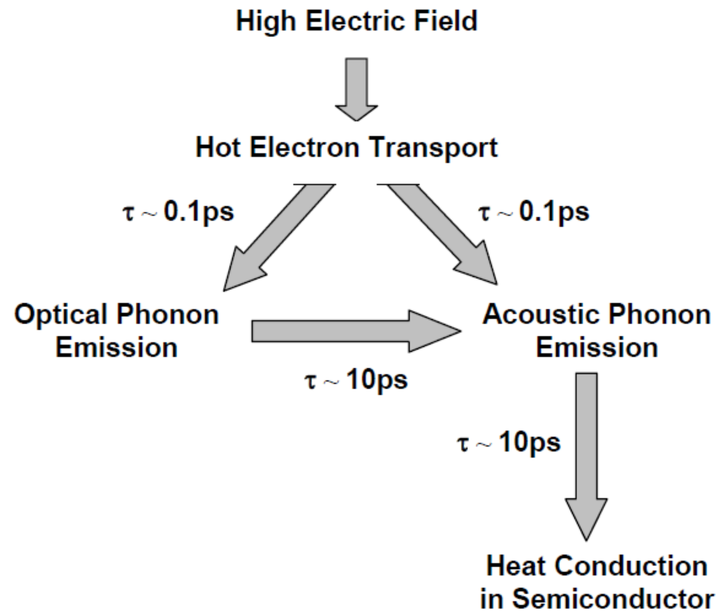

Figure 1.5. The path of heating flow generating and dissipating through the inside of semiconductors by optical and acoustic phonon emission under different timing window [7].

Thermal conductivity, k, units of $W.m^{-1}.K^{-1}$, is used to describe the ability of a material to conduct heat, which indicates the heat transfer faster in a material with a higher thermal conductivity than a material with lower thermal conductivity. Both types of material lead to different applications, for example, high thermal conductivity material can be used in a heat sink application and low thermal conductivity material can be used for thermal insulation. In SOI devices, the thermal conductivity of the buried oxide is only around 1 to 1.5 $W.m^{-1}.K^{-1}$ compared to the thermal conductivity of conventional bulk silicon substrates which is 140 $W.m^{-1}.K^{-1}$, approximately 100 times larger [8]. Therefore, the SOI technique offers better performance enhancement but the lower thermal conductivity of the buried oxide layer may also give more self-heating than bulk silicon substrate devices, and the increased temperature will affect the SOI device by increased junction leakage and power

consumptions. In this study, the author uses experimental and simulation methods to quantify how much self-heating is created in SOI devices and the resulting temperature distributions across the device.

1.4. Trap-rich, High Resistivity Substrate SOI MOSFETs

In the past years, engineers normally use silicon as the main material to make bulk silicon substrates for CMOS. This dissertation will focus on trap-rich, high resistivity silicon substrates as well. The trap-rich technique is important in CMOS radio frequency integrated circuits (RFICs) for reducing crosstalk between components and minimizing RF power loss in active and passive devices [9] [10]. In this study, a trap rich layer is introduced between the buried oxide layer and the silicon substrate as Figure 1.6. shows, and it consists of a high resistivity ($\rho \sim 1$–10 kΩ.cm) silicon substrate compared to the conventional bulk silicon substrate resistivity ($\rho \sim 13.5$ Ω.cm). A chemical vapor deposition process is used to insert several hundred nanometers to one micrometer thickness of poly-Si [11]. Without the trap-rich layer, the negative electrons attracted by the positive fixed charges between the buried oxide BOX layer and the bulk silicon substrate, generate a parasitic conduction channel, and this parasitic conduction path reduces the effective resistivity of the substrate at GHz frequencies. Therefore, by adding the trap-rich layer can eliminate the parasitic conduction path and increase the effective resistivity to optimize the device performance [5]. In this study, 45 nm SOI CMOS technology combines trap-rich, high resistivity substrate used to optimize RFIC applications, which can support the 5G communication band of 28-32 GHZ and beyond [6].

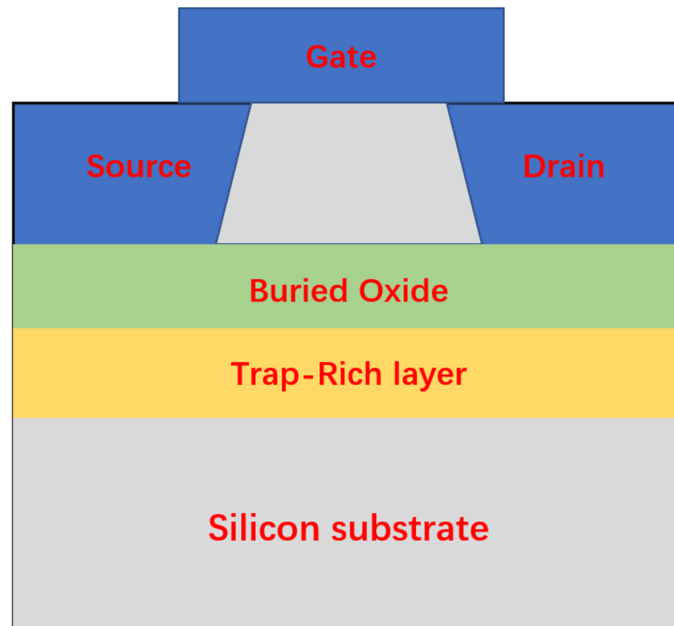

Figure 1.6. 2D cross-section view for trap-rich, high resistivity substrate SOI MOSFET structure.

However, the thermal conductivity of conventional bulk silicon substrates is around 140 W. m^{-1}. K^{-1} [8], and for the thermal conductivity of trap-rich layer in high resistivity SOI substrate for undoped poly-Si is around 10 W.m^{-1}.K^{-1} [12]. This indicates that the heat-conducting ability of poly-crystalline trap-rich layer is 10-15 times lower than bulk silicon, and will be worse for self-heating effects. Again, any increase temperature in self-heating will impact the performance of SOI RFICs by degrading carrier mobility, reduced drain saturation current, and increased power consumption and junction leakage. Therefore, it is important to understand the trap-rich technique and its contribution towards self-heating, especially for RF power amplifiers, which typically operate at ~ 50% efficiency are at risk of failing if operated at high temperatures and in stressful environments. In this study, a comparison between low resistivity and high resistivity silicon substrate uses

experimental data and simulation results to show the differences, and based on Silvaco TCAD simulation results, that explain the heat flow and temperature distribution. It provides a method to track and quantify the self-heating distribution. The approach can be used to as a thermometer tracker and placed nearby one or multiplied around a power amplifier (PA) for built-in self-heating test applications, for example, it can monitor the heating created and protect PAs operating high temperature stress conditions that might lead to damage [13].

CHAPTER 2

EXPERIMENTAL DETAILS AND METHOD

Trap-rich, high resistivity SOI silicon substrates offer performance enhancement for RFIC applications but also reduce the thermal conductivity due to increasing the phonon scattering compared to single crystal silicon, which means the self-heating effect becomes a more serious situation for SOI device at the nano-scale level. In order to track and quantify the self-heating effect and how much heat it generates. In this chapter, the DC experimental measurements are used to describe both trap-rich, high resistivity SOI substrate and bulk silicon substrate SOI devices under self-heating effect. The device is a combination of a heater and a calibrated thermometer, and the structure can be designed symmetrically. Indeed, a thermometer can track the heat accumulation and quantify the temperature, then in nano-scale devices, the heat flow will affect both heater and thermometer. To avoid the heat flow created by the thermometer itself, engineers can add a grounded dummy gate to isolate the thermometer from the heater minimizing the impact of parasitic leakage on the thermometer side for FinFET devices [14]. In this study, it focuses on SOI MOSFET on both high resistivity, trap-rich substrates and low resistivity substrate devices, it uses a common-source configuration without any dummy gate. Basically, there are two identical SOI MOSFETs put together and share one common source and the same active silicon region, one is called 'heater', another one called 'thermometer'. The basic working function is adding sufficient voltage bias to one of the devices above threshold voltage and into saturation so that it heats the active silicon region. The other MOSFET is biased in the sub-threshold regime to track and quantify the heat generated.

2.1. Device Use and Layout Details

The Global foundries 45 RFSOI CMOS technology [6] is used to fabricate both trap-rich, high resistivity SOI substrates and conventional SOI substrates with pairs of 40 nm gate length n-channel MOSFETs where the gap between two gates is 150nm and the total channel width is 500nm as Figure 2.1. shows [13]. Thickness of the insulating buried oxide (BOX) layer and the active silicon layer are 225 nm and 80 nm, respectively.

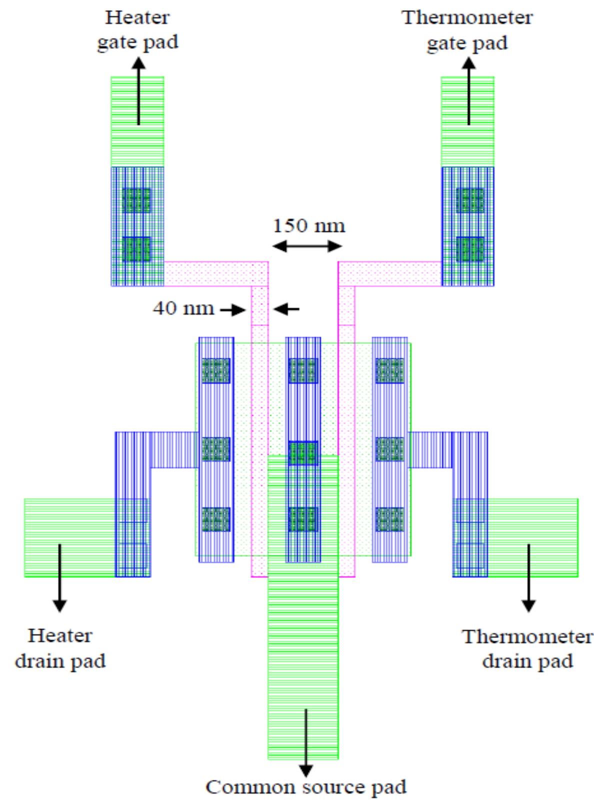

Figure 2.1. Layout of the 40 nm gate length NFET pairs where the gap between the gates is 150nm. The NFETs pair share a common source contact and the same active silicon region with area 500 nm x 470 nm.

In previous work, the gate length of the device is designed as 50 nm and 80 nm, and the device width is designed as 70nm, 200nm, and 500nm respectively. Typically, the series resistance for a wide and narrow device is around 350 Ohms to 600 Ohms [15]. As

a result, the common source needs a negative voltage to account for the voltage drop across the source contact. After optimization, the 40 nm gate length NFET is the Global Foundries 45 RFSOI process limitation for gate length with maximum of eight metal layers. This 40 nm gate length SOI device maximize the operating frequencies (f_{max}, greater than 300GHz) and minimizes the parasitic loss at radio frequencies because of the metal interconnects with low sheet resistance copper wiring [6]. Figure 2.2. shows, the pad configuration for the heater and thermometer pair [13]. Furthermore, the parasitic resistance from source or drain to the 96 x 96 um^2 pad can be determined as 5 to 6 Ohms by using caliber xRC parasitic extraction (PEX) tools. Compared to previous work, the parasitic resistance has decreased 60 to 100 times, and the voltage drop, which equals to parasitic resistance times the current drive through the channel, also decrease 60 to 100 times. As a result, the voltage drop across the source contact is negligible.

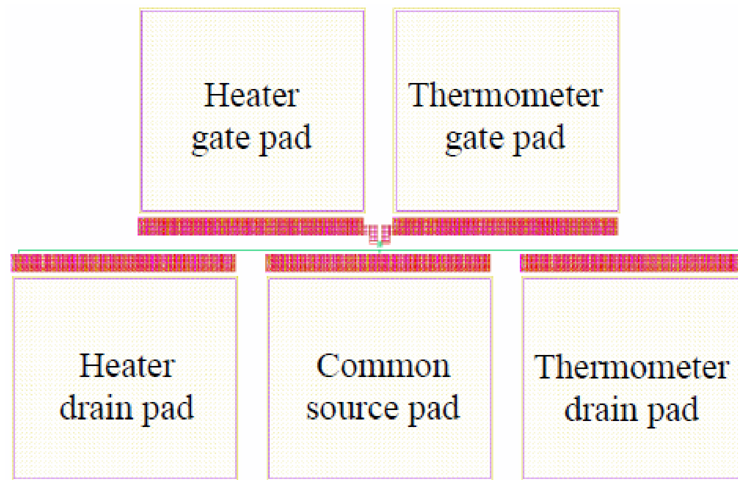

Figure 2.2. Pad configuration of the 40 nm SOI devices, five terminals to contact five different pads, and each of the bond pads size is 96 x 96 um^2.

2.2. NFET Heater Characteristics

For device characterization, the family-of-curves and turn-on characteristic curves (Gummel curve) are the most common ways to calibrate the performance of devices. They can provide the basic parameter information, for example, threshold voltage (V_{th}), current drive (I_d), transconductance (g_m), sub-threshold slope (SS) and so on. During the measurements, in order to reduce the experimental error and increase the accuracy of the data, such as the lab temperature, the probe station noise, and even the strength of the probing device, all of those factors can affect the measurement results and may lead the experimental conclusion to another direction. Therefore, repeating multiple identical measurements on different devices is recommended. In this study, a Cascade Microtech 11000 probe station as shown in Figure 2.3, has been used for all the measurements, and each measurement is repeated three times and uses the average results with calculated error bars.

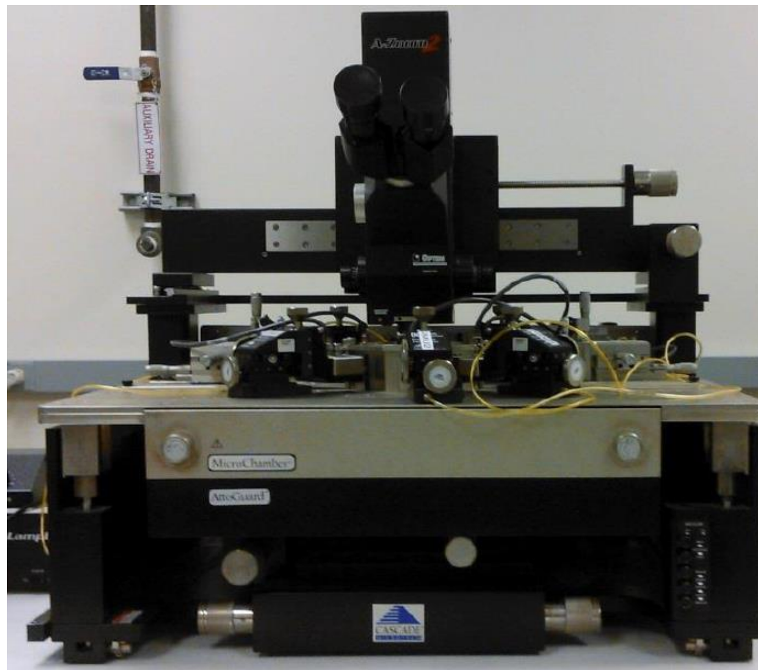

Figure 2.3. Cascade Microtech 11000 probe station with five probes.

As mentioned above, the device to device variation under the same measurement conditions (V_g swept from -0.5V to 1V, V_d=0.1V) have been repeated with two different devices (names as A1 and B6) in the same conventional low resistivity SOI substrate die as Figure 2.4. shows, and also indicates the importance of using average results.

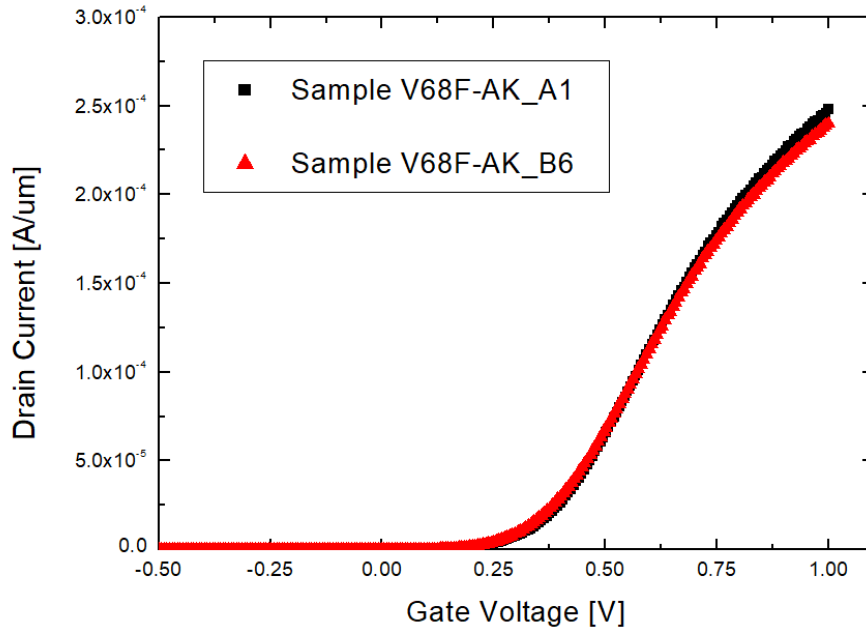

Figure 2.4. Device to device variation comparison for turn-on characteristics curve based on a same die of conventional low resistivity SOI substrate devices.

The Global Foundries 45 nm RFSOI technology has a nominal maximum operating voltage of 1V due to the process design kit, and to protect the device, the voltage used for all the measurements must be 1V or less [13]. And due to the fact that the total channel width is 500 nm, the current drive is doubled numerically when using standard units [A/um]. As Figure 2.5. shows the family-of-curves for the conventional low resistivity SOI substrates 40 nm gate length device (sweeps the drain voltage from 0V to 1V, with applied gate voltages of 0.5V, 0.75V, 1V, respectively), indicates the maximum current drive is around one milli-ampere per micrometer (mA/um), so the maximum current drive is around

0.5 mA through the whole device. The parasitic resistance from the source or drain to the contact pads is around 5 to 6 Ohms, so the total voltage drop from the pad to source or drain is 3 mV. The voltage applied at the common source contact on the active silicon region is only 3 mV higher than the probing connection from the source contact pad to the DC ground, which can be neglected when compared to the operating voltage. Therefore, the 40 nm gate length NFET pair of heater and thermometer can be described as two identical NFETs, and either one could be regarded as heater or thermometer, and the current flow through the heater is independent of the thermometer characteristics calibration.

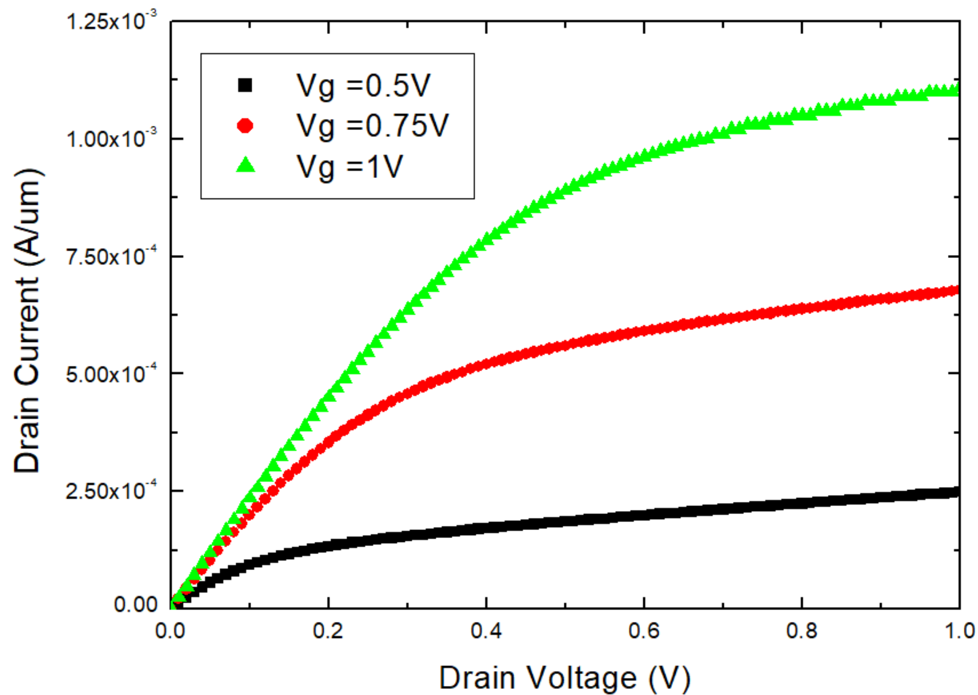

Figure 2.5. Family-of-curves comparison for the conventional low resistivity SOI substrates devices of 40 nm gate length NFET with the total channel width 500nm.

2.3. NFET Thermometer Calibration

As discussed above either one of the NFETs can be regarded as a heater and the other one as the thermometer. The heater NFET is biased above the threshold voltage and into saturation to heat up the active silicon region, while the thermometer NFET is biased into the sub-threshold regime. Equation (2.1) express the drain current, (I_D), in terms of the drain voltage, (V_{DS}), gate voltage, (V_{GS}), and threshold voltage, (V_{TH}) [16].

$$I_D = I_S' \, exp\left[\frac{V_{GS}-V_{TH}}{nU_T}\right]\left(1 - exp\left[-\frac{V_{DS}}{U_T}\right]\right) \tag{2.1}$$

In (2.1), U_T, is the thermal voltage, which presents as KT/q, n is the ideality factor, equals to 1.323 on average due to the device to device variation, and I_s' is a constant value for the reverse saturation current. In practice the drain voltage, V_{DS}, is chosen to be three times larger than U_T so that the drain current can be regarded as independent of V_{DS}. In addition, the sub-threshold slope, SS, which is equal to the inverse slope of the log scale of I_{DS} and V_{GS} in the turn-on characteristic of Figure 2.6, changes with temperature in the sub-threshold region, $V_{GS}<V_{TH}$. Therefore, the temperature can be extracted by measuring the sub-threshold drain current and using equation (2.2) which shows the SS value in terms of the temperature changes.

$$SS = \ln(10) * \left(\frac{\mathrm{KT}}{\mathrm{q}}\right) * \mathrm{N} = \frac{1}{\mathrm{slope}} \tag{2.2}$$

In equation (2.2)

K, Boltzmann constant, 1.3806e-23, ($J.K^{-1}$)

T, temperature, (K)

q, elementary electric charge, 1.6021e-19 (C)

N, ideality factor, 1.323 due to the specific device to device variation.

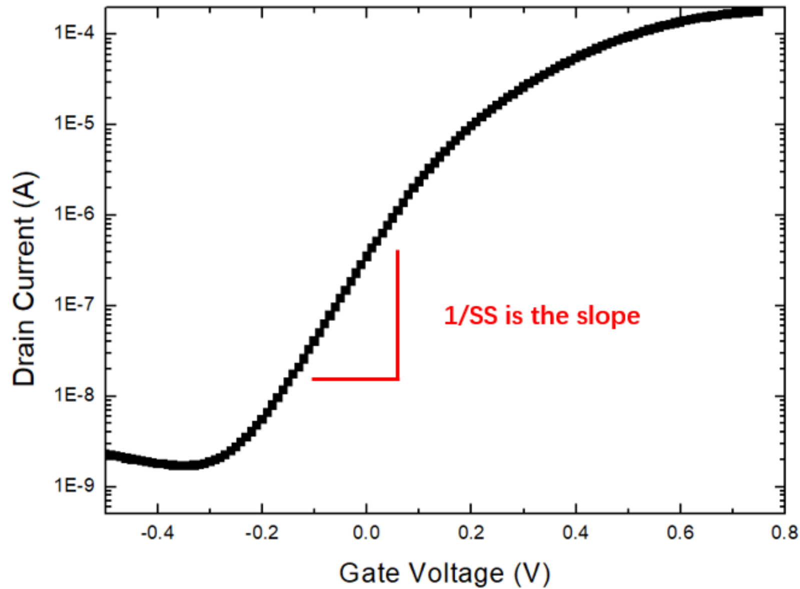

Figure 2.6. Sub-threshold slope (SS) as defined in the turn-on characteristics curve using a log scale for the current drive.

Also, the thermal voltage is $U_T = KT/q$, and equals to 0.02586V at 300K. The temperature can be determined using equation (2.3) which comes from equation (2.2). For the experimental measurements, a temperature-controlled hot chuck is used to calibrate the NFET thermometer, with the chuck temperature confirmed by an independent thermocouple measurement. As Figure 2.6. shows, the various SS values change in terms of the relationship between gate voltage and the log-scaled drain current under different temperature operating conditions controlled by the temperature of the hot chuck.

$$T = q\left(\frac{SS}{N*\ln(10)}\right)/K \quad (2.3)$$

Based on Figure 2.4, the threshold voltage for the 40 nm gate length NFET pairs of heater and thermometer SOI device is ~ 0.25V. Figure 2.7. indicates that the SS value can be extracted from the sub-threshold regime, where the drain current varies exponentially for gate voltages below the threshold voltage, until the leakage currents dominate for a gate voltage of less than approximately -0.2V [13]. With a drain voltage of 0.1V, the variation in drain current with gate voltage is highly repeatable and there is no significant delay for the given temperature range. Therefore, the variable SS value can be used as a valuable indicator to calibrate the device temperature changes. Moreover, the sub-threshold slope values increase when the chuck temperature increases as Figure 2.8. [13] shows, and all the SS values trend to a polynomial fit under different temperatures.

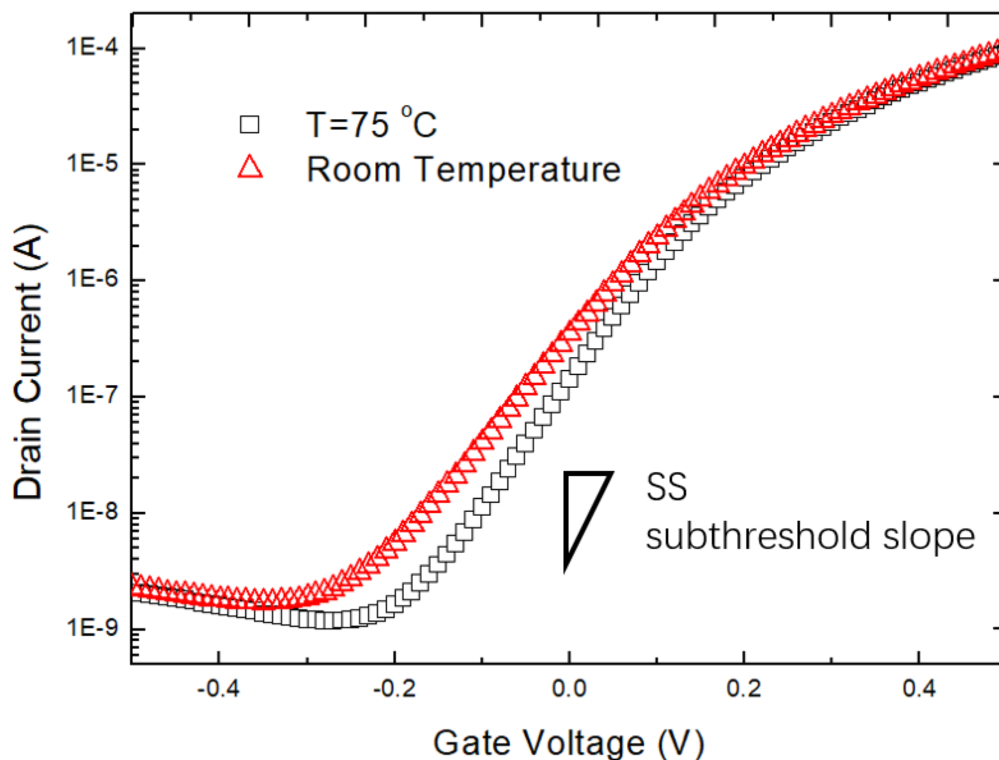

Figure 2.7. Gate voltage vs. log scale of drain current, shows the various sub-threshold slope (SS) values present under different temperatures applied by the hot chuck of the probe station.

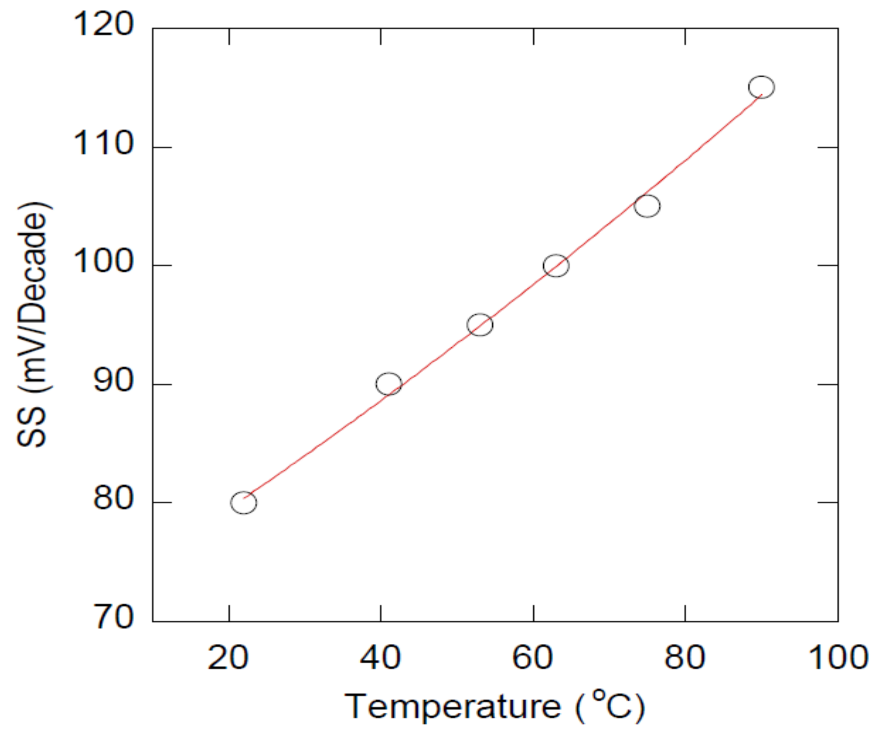

Figure 2.8. SS values of the thermometer increase with chuck temperature increased. The red line indicates a polynomial fit to the SS values used for the thermometer temperature calibration.

CHAPTER 3

MEASUREMENT RESULTS AND TWO DIFFERENT TYPES OF SOI SUBSTRATES COMPARISION

The self-heating effect (SHE) can be measured under DC conditions and used to quantify the increase in temperature. In this chapter, multiple measurements are averaged to calibrate how much heat is generated through the heater NFETs and used to compare the performance of NFETs on conventional silicon SOI substrates with trap-rich, high resistivity SOI silicon. Due to the structure difference, the trap-rich devices might be expected to have more heat generated during the voltage bias process because of the lower thermal conductivity compared to the bulk silicon substrate. However, the results show very similar heating for NFETs on both types of substrates.

3.1. Self-Heating Characteristics

Taking the product of the maximum current flow through the heater, 0.5mA, and nominal maximum voltage, 1V, the maximum power dissipated in the heater is 0.5 mW, This is sufficient to provide an observable and repeatable level for calibrating the generated heating in 40 nm gate length NFET pair thermometers. In order to know the impact of self-heating, the measurements require the devices to be placed on the chuck of the probe station under room temperature (around 300K), and a bias above the threshold voltage applied to the heater NFET with a certain time delay to heat the silicon active region up to thermal equilibrium state. The thermometer gate is swept over the subthreshold range to measure the drain current on thermometer side. After calculating the sub-threshold slope for the thermometer drain current, the local heating of the thermometer NFET temperature is

determined by using equations (2.2) and (2.3). Finally, the relationship between the change in thermometer temperature and the power dissipated in the NFET heater be determined as Figure 3.1. [13] shows. The various gate voltages applied on heater side are: solid triangles present the thermometer temperature under Vg=0.5V condition, open squares present Vg=0.75V, and open circles present Vg=1V. A fixed gate voltage is applied to the heater, while the drain voltage is swept from 0 to 1V with a voltage step of 0.1V. As Figure 2.5. in the Chapter 2 shows the saturation drain current decreases with lower gate voltage, and higher gate voltage gives higher saturation drain current, so the power dissipated in the heater also changes. As Figure 3.1. shows the NFET thermometer temperature increase quadratically with increasing heater power level (voltage applied times current flow, P=IV). The data for different gate voltages fit together and overlap, which means the increased thermometer temperature is well controlled by increasing the heater drain current. This conclusion also confirms the thermometer temperature calibration is independent of the drain current flowing on the heater side because of the low parasitic resistance from the source or drain contacts to the 96 x 96 um^2 pad. If this were not the case there would be a large amount of voltage drop across the common source to the thermometer, as discussed in Chapter 2. Typically, the parasitic resistance for a wide and narrow device is around 350 to 600 Ohms. For the 40 nm gate length NFET pairs, the maximum current is 0.5mA, and based on the 6 Ohms series resistance, the resulting voltage drop of ~ 3mV, will not significantly affect the NFET thermometer calibration.

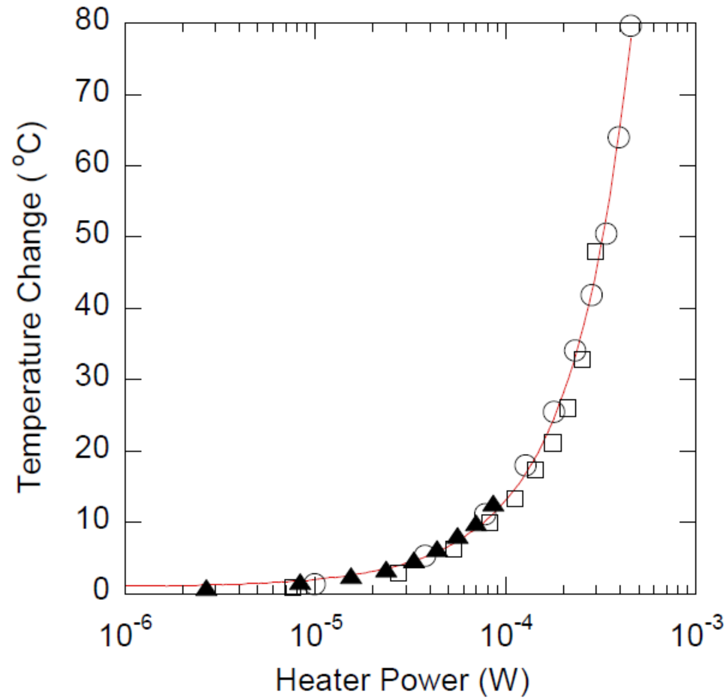

Figure 3.1. The relationship between the thermometer temperature changes and the heater power dissipated, the red line is a quadratic fit for all different gate voltages biased under 0.5V (solid triangles), 0.75V (open squares), 1V (open circles), respectively.

Overall, the measurement results indicate the sub-threshold slope (SS) can be used for calibrating the temperature of closely-placed devices, by biasing the NFET heater above threshold voltage to heat the active silicon region, and biasing the NFET thermometer in the sub-threshold regime to capture the drain current of the thermometer.

3.2. Trap-Rich, High Resistivity Substrate and Bulk Silicon Substrate SOI MOSFETs Performance Comparison.

Device on trap-rich, high resistivity SOI substrates have better performance due to lower power loss in active and passive devices and reduced cross-talk between components [9] [10]. However, because of the lower thermal conductivity, 10 $W.m^{-1}.K^{-1}$ for the trap-rich layer, compared to the thermal conductivity of crystalline silicon, 140 $W.m^{-1}.K^{-1}$, the trap-rich wafer has lower heat conducting ability than conventional bulk silicon substrates, which suggests that trap-rich SOI devices may be more seriously affectated by self-heating effects. In this section, there is a performance comparison between conventional bulk silicon SOI substrates and trap-rich, high resistivity SOI substrates. The same thermometer calibration method is used to determine how much difference in self-heating effect is caused by these two different substrates.

Firstly, to calibrate NFET heater and thermometer pairs, the sub-threshold slope values need to be measured and compares between two different SOI substrates. Figure 3.2. [5] shows the relationship between drain current and gate voltage. The open squares, and the open circles represent trap-rich, high resistivity SOI substrates and conventional bulk silicon SOI substrates, respectively. The results indicate that these two types of substrates agree well with only small variations, leading to a 10mV difference for the threshold voltage. And the sub-threshold slope values increase when the probe station chuck temperature is increased.

\

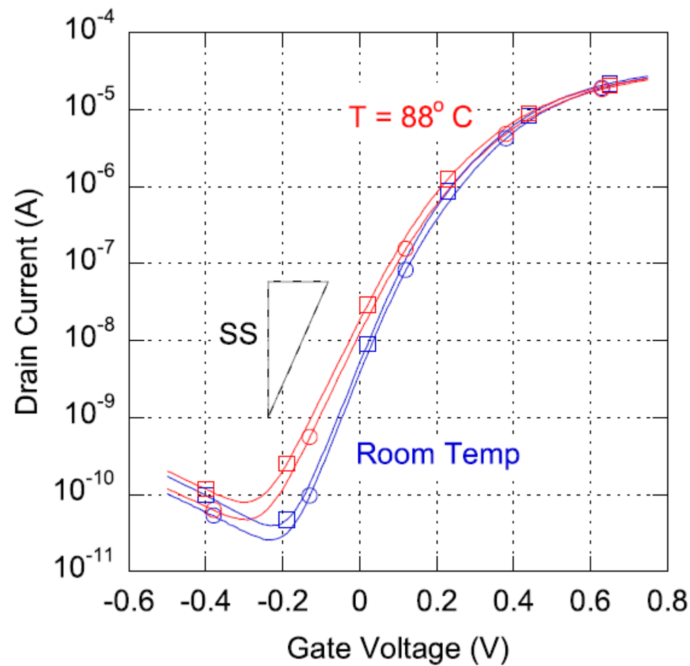

Figure 3.2. Comparison between trap-rich, high resistivity SOI substates with conventional bulk silicon SOI substrates for the relationship between gate voltage and drain current.

As demonstrated in the Chapter 2, sub-threshold slope values change, for both room temperature and 88-degree Celsius, but the drain current variations with gate voltage bias are repeatable and without a significant difference. By using the sub-threshold slope values, we can calibrate the device temperature for both types of substrates. As Figure 3.3. [5] shows, the relationship between the calibrated temperature and the SS values agree well for both the trap-rich, high resistivity SOI substrates (open red squares) and the conventional bulk silicon SOI substrates (open blue circles) devices. The solid black line shows that a quadratic fit for the SS values can be used to determine the thermometer temperature.

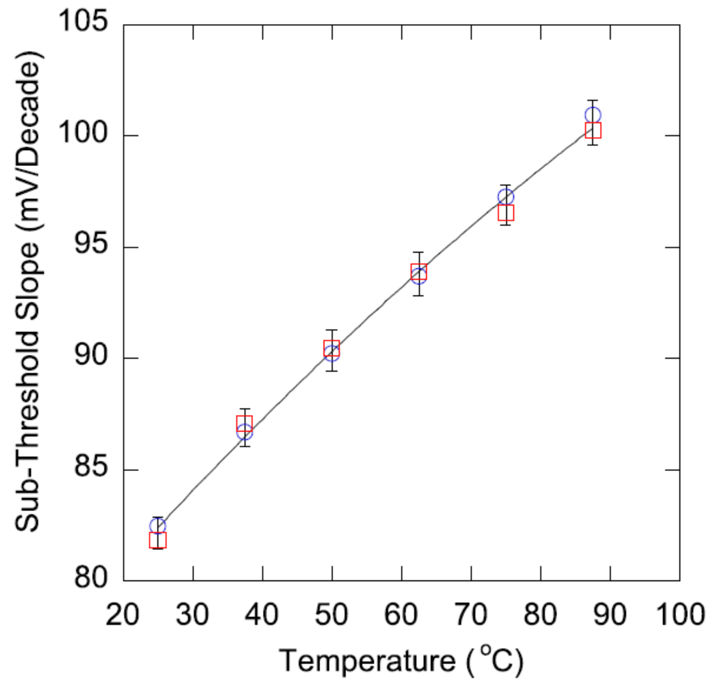

Figure 3.3. Sub-threshold slope as a function of temperature captured on the thermometer, and the device-to-device variation shown by error bars. The open red squares represent trap-rich, high resistivity SOI substrates, and the open blue circles represent conventional bulk silicon SOI substrates.

Due to the small differences in device-to-device variation and mismatch between threshold voltage (V_{th}) and transconductance (g_m), Figure 3.4. [5] shows the family-of-curves for both the trap-rich, high resistivity SOI substrates and the conventional bulk silicon substrate SOI devices. The curves come with different gate voltage conditions, from 0.2V to 0.9V with a voltage step of 0.1V. The error bars show the variation between NFETs for the two different types of substrates. Combining the total channel width of 500 nm and the parasitic resistance between the source or drain contact to the pad, which is around 5 to 6 Ohms, the maximum current flow through the common source of the NFETs is 0.5mA and the voltage drop is ~ 3mV, which can be neglected when compared with the operating voltage.

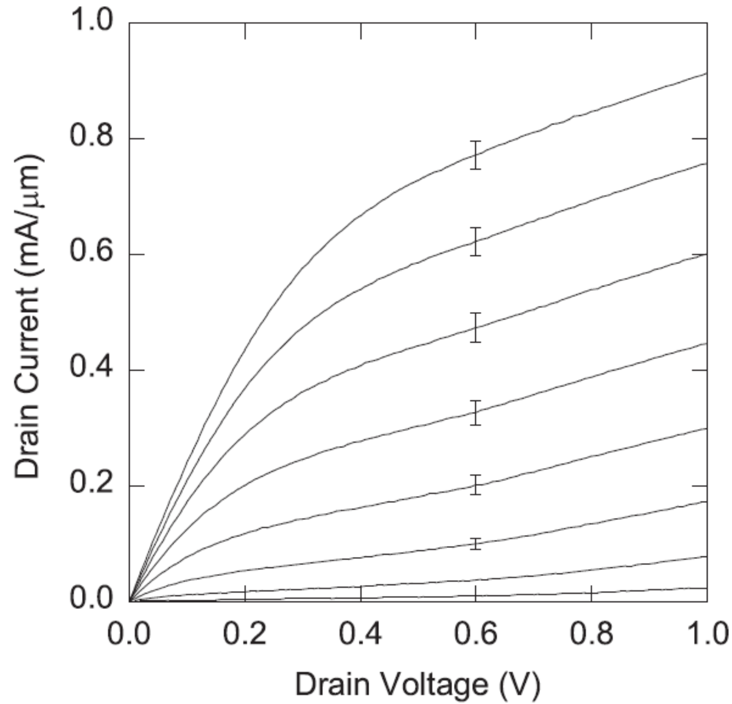

Figure 3.4. Family-of-curves for 40 nm gate length NFETs on SOI substrates, the curves present different gate voltage conditions, from 0.2V to 1V with step 0.1V, and the error bars indicate the difference between two different types of substrate devices.

Furthermore, the power dissipated can be calculated as the voltage applied times the current flow through the NFETs. As Figure 3.4. shows the maximum current through the channel is around 0.5 mA and this specific designed SOI NFET allows a maximum voltage of 1V. So the maximum power dissipated ~ 0.5mW, which the heater can supply to heat in the thermometer side of the NFET pair. Figure 3.5. [5] shows that when a maximum operating voltage of 1V is applied on the NFET heater, the increase in temperature with heater power changes for both the trap-rich, high resistivity SOI substrates (open red squares) and the conventional bulk silicon SOI substrates (open blue circles), and the error bars show the standard deviation from three measurements on different devices on the same die due to the device-to-device variations.

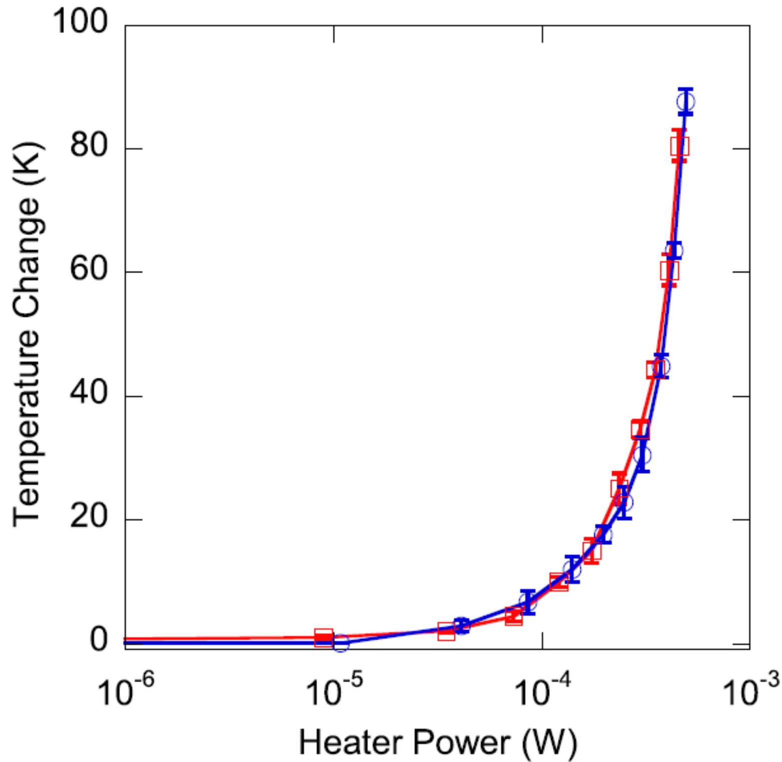

Figure 3.5. The change in temperature of the calibrated thermometer with applied heater power for both trap-rich, high resistivity SOI substrates (open red circles) and the conventional bulk silicon SOI substrates (open blue squares).

The thermal conductivity of the poly-crystalline trap-rich silicon layer is 10-15 times lower than that of conventional crystalline silicon [18], which suggests that more heating would occur in the trap-rich, high resistivity SOI substrates compared to the conventional bulk silicon SOI substrates. On the contrary, based on the experimental results, under the voltage bias conditions, NFETs on the trap-rich, high resistivity SOI substrates experience a similar increase in temperature as the conventional bulk silicon substrate SOI MOSFET devices. This is opposite to our expectation, and there are some possible explanations based on the heat conduction and temperature distribution. The extra created heating may go flow to the surface through the metal layers, or go to bottom of the substrate via the buried oxide

(BOX) layer. In order to understand the temperature distribution and how the heat flows, it is necessary to build a numerical model of the structure device and use it to simulate the heat conduction. Moreover, the previous work shows the temperature of the heater is around 2.5 to 3 times higher than the thermometer for FinFET and planar transistors [15] [17]. So if the highest thermometer temperature is around 380 K (room temperature is 300K, and the highest delta temperature is 80K as Figure 3.1. shows), it may reach the temperature limitation and overheat if the heater based on heater temperature is 2.5 to 3 times higher than that of the thermometer. Therefore, numerical simulation work is obviously needed to determine the temperature distribution among the whole device and compare the temperature on both the heater and the thermometer regions. By combining the measurements results and an accurate numerical simulation model we can calibrate the power dissipation and heat flow through the SOI MOSFETs, which also can be used to optimize for radio frequency integrated circuits (RFICs) applications.

CHAPTER 4

SILVACO SIMULATION

In order to understand the heat flow through and temperature distribution among the devices, we need to build a physical simulation model to explain the temperature distribution and to explain the reason why both low resistivity and trap-rich, high resistivity substrates experience a similar amount of heating. Combining the device size and layout, it is possible to design a similar device structure for both low resistivity substrate SOI MOSFETs and similar ones on trap-rich, high resistivity SOI substrates. Moreover, the heating distribution can show the main heating source and dissipation through to the substrate region or up through the metal layers. Therefore, we need to simulate both the substrate layer and the metal contact layer. However, there are some concerns and issues during the simulation, for example, the unknown concentration of doping levels in the SOI NFETs, it means we have to use the average level typically used for manufacturing. The thickness of both the metal and the substrate need to be carefully considered. In reality, the metal layer contains up to 10 layers of metal, and the substrate thickness is several hundreds of microns, but it is not necessary to simulate the entire substrate thickness and all of the metal layers to compare accurately with the 40 nm gate channel length device. Furthermore, self-heating can be considered at different thickness levels, for example, for the local self-heating effects, it runs at the atomistic level of around one nanometer, while the transistor-level is around 10~100 nanometers, and for the metallization layers it goes up to ten or hundreds of microns. Then for the global self-heating effect, it runs to die or chip level to one-millimeter thickness. In this study, we only focus on the local self-heating effect, which contains the transistor level and the lower metallization layers. It covers the whole

size of the device under 5 micrometers including the device layers, 2 microns thickness of the metal contact, and 2 microns for the conventional bulk silicon substrates thickness, or one-micron of the trap-rich layer plus one-micron of trap-rich, high resistivity substrate SOI MOSFETs.

4.1. Overview

For the manufacturing of semiconductors, companies and industries normally invest hundreds of millions of dollars to design, produce, and characterize different techniques or processing steps in cleanrooms. An accurate numerical model can simulate the working functions of devices and explain the phenomena that happens inside of the devices. For example, the temperature distribution for the entire device and the heating flow directions for the impact of the self-heating effect can be shown and quantified by a numerical simulation model. Based on the semiconductor fundamental physics theories, a model typically uses visual software to build devices and simulate with different external working conditions. In this chapter, Silvaco simulation software has been used, with Athena used for creating the device structure and Atlas is used for giving the additional voltage bias to operate the device. Combining the experimental results to confirm the condition of the device is similar to a real device, and the temperature distribution graph can be given by 2D simulations, and it indicates the heat flow directions and temperature distributions among the whole of the device.

Silvaco is a leading electronic design automation (EDA) provider of software tools. It was founded in 1984 and has become the largest private EDA company and continues to grow. It has both 2D and 3D simulation tool for processing and device simulation with a

framework for the development of analog/mixed-signal, power integrated circuits and memory design. Silvaco comprises Athena for a 1D/2D process simulator and Altas for 2D/3D device simulation framework. It includes interactive tools, such as DeckBuild for the running-time environment, DevEdit for structure and mesh editor, TonyPlot for 1D/2D/3D interactive visualization utility, Optimizer for optimization utility, and Maskviews for layout editor. Overall, in this chapter, the whole simulation process goes through Athena to build the device structure and uses Atlas to models and apply voltage biases etc., after confirming and comparing device performance with experimental results, it then uses temperature models to calibrate self-heating effect and the generation heat distribution among the whole device.

4.2. SOI MOSFETs Device Modeling

The 2-dimensional simulation model is built for a 45 nm partially depleted (PD) SOI device and relates to the self-heating effect. A comparison of both trap-rich, high resistivity SOI substrates and conventional crystalline silicon SOI substrates by simulation can explain the heat flow directions for the extra generated heat. As Figure 4.1. [5] shows, the 3D layout version for NFET pairs of heater and thermometer with five terminal probe contact pads and the interconnect wiring up to metal-2, there are two gates, two drains, and one common source. First of all, for SOI MOSFET device structure modeling, we follow the original device structure as a basic rule to build a numerical model, with a gate length of 40 nm, an active silicon layer thickness of 80 nm, and a buried oxide insulting layer thickness of 225 nm. Since there are two identical NFETs placed together they are not significantly affected by each other due to the small parasitic resistance from the source or

drain contact to pads with a 3mV voltage drop. Beginning with a three terminals device model is a good start for simulation.

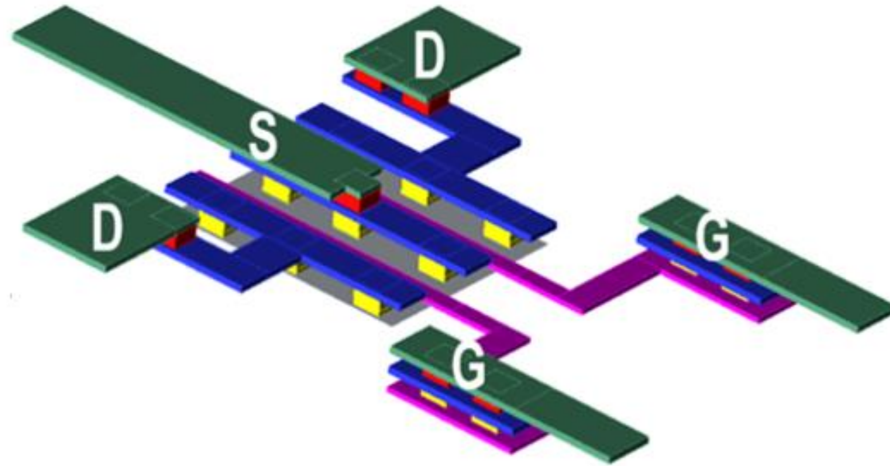

Figure 4.1. 3D version of the NFET pairs of heater and thermometer structure with interconnect wiring up to metal-2 contact.

4.2.1. Three-Terminals Modeling

Combining the device structure layout, Silvaco simulation allows us to design a regular SOI MOSFET with 40 nm gate length, 80 nm active silicon region thickness, and buried oxide (BOX) layer is 225 nm. The previous work indicates the structure of a 45 nm SOI CMOS process with 8 metal layers and all the metal layers made by copper, except for the top layer which is aluminum as shown in Figure 4.2. [11]. In this chapter, there is no need to simulate all eight metal layers because the thickness of the metal layers compares to the channel size. However, a reasonably thick metal is needed, and the thermal resistances can be calculated by the measured parasitic resistance related to an equivalent conductivity value.

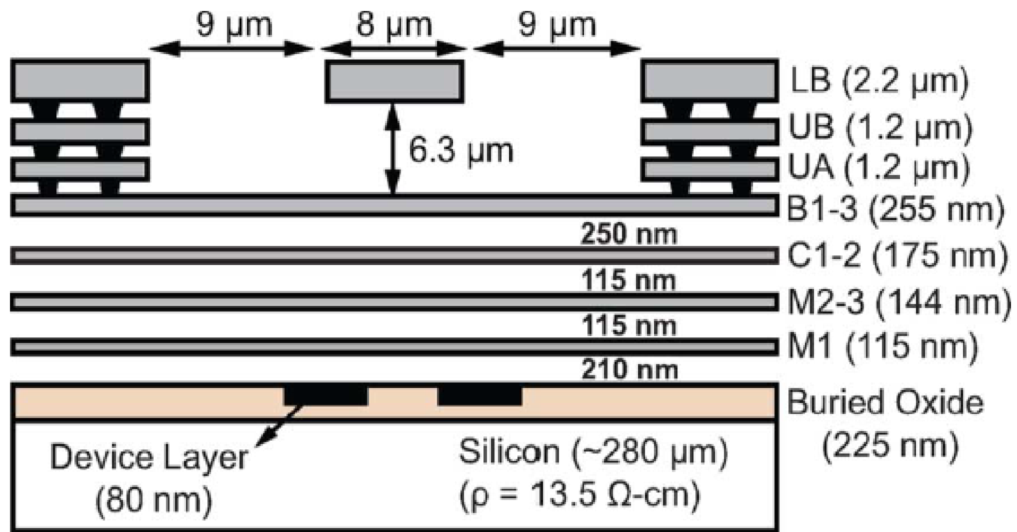

Figure 4.2. 2D Cross-section of a 45-nm SOI CMOS process metal stack-up. All metal layers are copper, except the aluminum top metal [11].

Athena tools can build a device structure with a simulated manufacturing process, which includes doping, deposition, etching, and even for the oxidation and diffusion process. Since the submitted layout is fabricated as a multi-project-wafer (MPW), the only difference between the two different types of device is the trap-rich layer, which has a high resistivity substrate and leads to different structure, by using a one-micron thick polysilicon layer inserted in between the buried oxide layer and the silicon substrate without any other changes. Therefore, by starting with the three-terminal device shown in Figure 4.3, it uses a simple structure to calibrate and compare the threshold voltage and current drive with the real devices, since the two NFETs are nominally identical and independent. Athena has a built-in mesh adaption module which is used to optimize the grid for the simulations. Obviously, the channel region needs more mesh points in both X and Y directions, and the amount of mesh points is a trade-off between accuracy and simulation timing, so the

substrate region may not need as many mesh points as the channel region. The balanced and reasonable setting for a mesh adaption module can balance the accuracy and speed of the diffusion and oxidation stages, during which the simulation time window changes with various impurity profiles [19] [20]. A triangulation scheme is used by default as an error estimator in this chapter for a 2D version of the simulation to remove boundary problems, otherwise, a rectangle shape scheme is more widely used for 3D numerical simulation models.

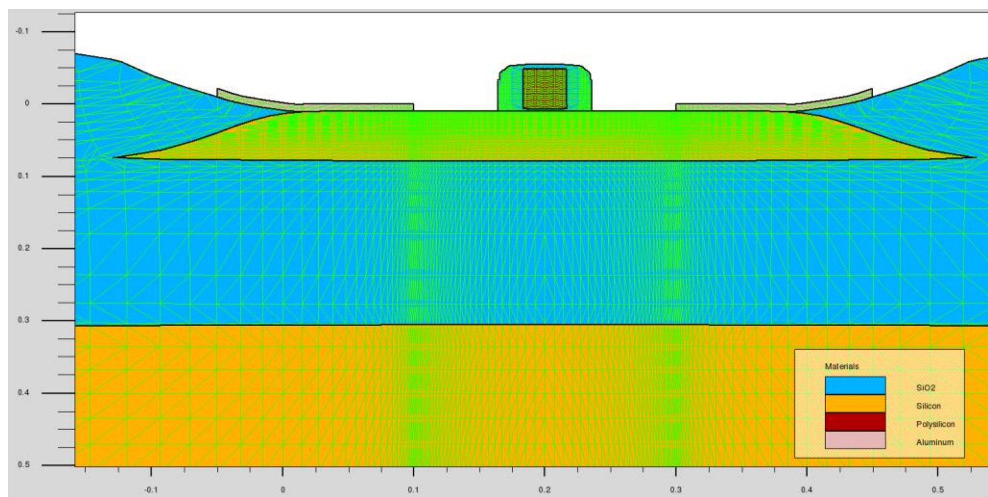

Figure 4.3. 2D cross-section for a three-terminal SOI device with 40 nm gate length, 80 nm active silicon region, and 225 nm for the insulating BOX layer, and more mesh points distributed in channel area.

During simulation, the time for oxidation or diffusion period has been divided into different small steps, and the mesh adaption module allows to optimize the ion implanted profiles based on the result of the previous step, and either generates the additional needed mesh points or deletes unnecessary mesh points to reduce the total simulation time while keeping the same precision. Moreover, the algorithm of mesh adaption module also can gradually increase/decrease the mesh density if the current mesh density needs

larger/smaller increments than the previous step until an accurate implanted profile distribution is reached. Therefore, the mesh adaption module of Athena is used as a dynamic cycle to minimize the mesh density and decrease the simulation time with more accurate meshing used to compare the initial setting at the beginning.

Instead of the exact same doping concentration as foundries use, the doping concentration level of each terminal in the simulated device is set using acceptable material and doping ranges typically used by companies and industries. As Figure 4.4. shows, a cutline through the gate to the active silicon region display the doping level in terms of the active boron and active phosphorus concentration. Since the devices used are n-type MOSFETs, which has n-channel region between the drain and the source contact, and the drain and source are doped n-type, while the substrates are doped p-type dopant. Typically, phosphorus or arsenic are used as the n-type dopant, and boron as the p-type dopant.

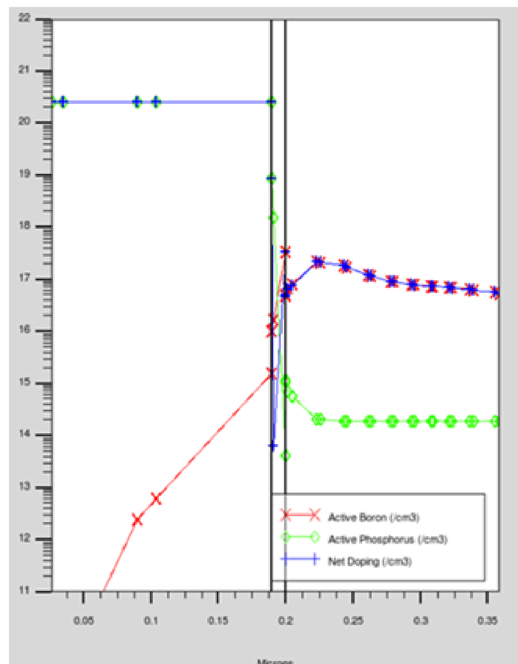

Figure 4.4. Cutline through the gate to the active silicon region. The open green squares present active phosphorus doping level, 2E14 cm^{-3}, and the red crossed solid line presents the active boron doping level, 1E17 cm^{-3} in active silicon region.

After the device structure is built-up, due to the low parasitic of the NFET pairs and the neglectable voltage drop between source or drain to contact pad, lead to the heater and the thermometer are independent. In the three-terminal simulation, to confirm the numerical model structure design and doping levels are similar as the real devices, we use the same voltage bias conditions and capture the drain currents to compare with measurement results. Figure 4.5. and Figure 4.6. show the comparison between the measurement results (open black squares) and the simulation results (open red triangles) based on the family-of-curves and turn-on characteristics curves.

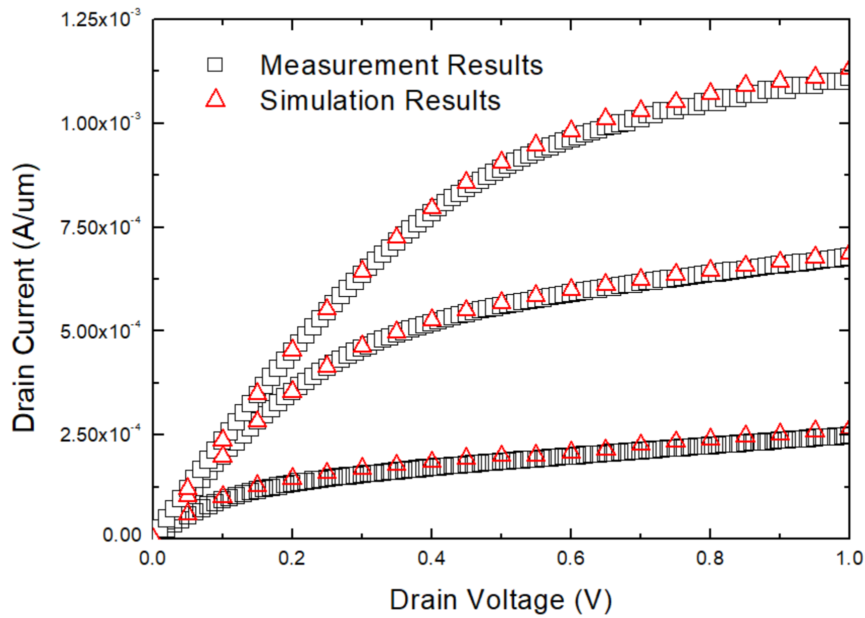

Figure 4.5. Family-of-curves comparison for measurement and simulation results by using the exact same bias voltage condition. The drain voltage is swept from 0 to1 V, and bias different gate voltages, 0.5V, 0.75V, 1V, respectively.

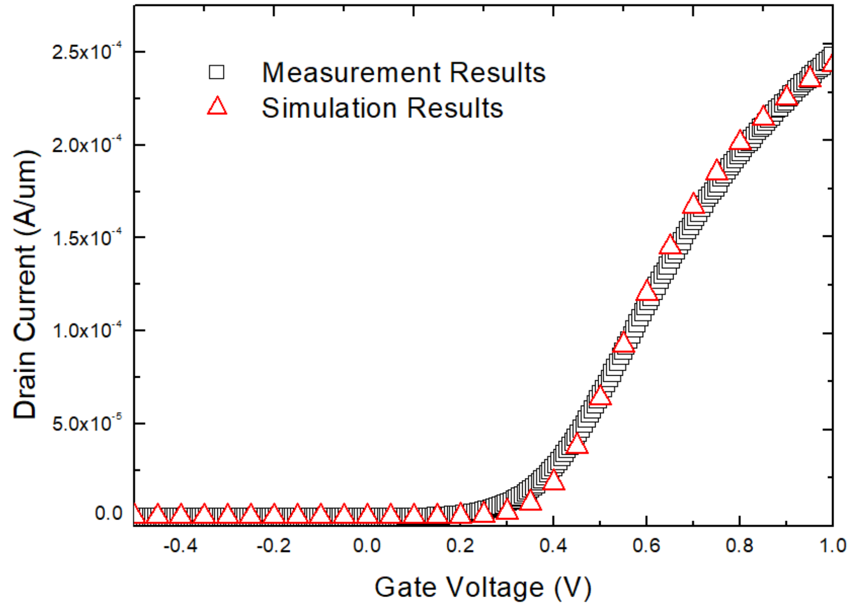

Figure 4.6. Comparison of the turn-on characteristics curves measurement and simulation results by using the exact bias voltage conditions. The gate voltage is swept from -0.5V to 1V, and the drain voltage bias is set at 0.1V.

4.2.2. Ion Implantation Model

The implantation process is one of the indispensable sections for the manufacturing and fabrication of semiconductors. And the implant method matters with materials structure and the tilt angle with or without rotation during the manufacturing process. The Silvaco Athena tool uses statistical techniques and analytical models to simulate ion implantation, which are based on the measured or calculated distribution moments. It starts with a Gaussian distribution with the symmetrical ion-implantation method, and gets improvement to the asymmetrical method, named the Pearson implant model, the most widely used model for ion-implantation profiles using the Pearson type IV distribution [21]. However, the Pearson implantation model is often used for a simple planar structures and silicon materials, while for non-planar structures or other materials simulation, Athena

provides Monte Carlo implant models, that are useful for InGaAs and SiC device simulation. The Monte Carlo model offers flexible ion implantation in non-standard conditions and is also more accurate if tilt angle with rotation is required, compared with analytical models [22]. Overall, based on binary collision approximation (BCA), the Monte Carlo ion implant model allows implantation profiles in an arbitrary structure with non-silicon material simulation.

In this chapter, the Monte Carlo ion implantation model is used for all implantation steps, and Table (4.1) shows the different implantation process details. It involves p-well, threshold-adjust, n-channel lightly-doped-drain (N-LDD), and source/drain implant parameters. The source and drain contact are doped n-type when the MOSFET has an n-type inversion layer channel. The N-LDD implantation is used to enable an initial gate doping by have doping masks [23], which create a lightly doped area near the gate region and provide many electrical advantages, but also suffers from a higher resistivity at the same time [24] [25].

Region	Ions	Dose (cm^{-2})	Energy (keV)
P-well implant	Boron	8E12	30
Threshold-adjust Implants	Boron	3E13	15
N-LDD implant	Phosphorus	1E12	10
Source/Drain implant	Arsenic	5E13	5

Table 4.1 implantation details for the device modeling in Athena.

Here, ion implants are used for the source and drain extensions, creating the halo regions, and adjust the threshold voltage. As Figure 4.7. shows, the source and drain extensions can eliminate having the bulky source and drain regions with low resistance [37]. And creating the heavily doped halo regions can reduce the short channel effects. Moreover, the threshold-adjust implant can change the threshold voltage value by implanting extra ions near the surface. Without the threshold-adjust implant, in the general case, the substrate will be highly doped which can affect the threshold voltage, and by involving the extra donors, the threshold voltage value can be adjusted by changing the effective body doping.

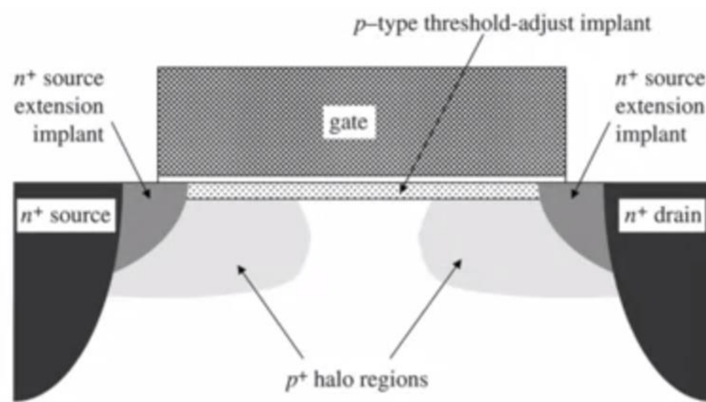

Figure 4.7. Functions of ion implantation in a n-channel MOSFET [37].

4.2.3. Five-Terminals Modeling

As described in previous chapters, the NFET pairs of heater and thermometer are made by two nominally identical 40 nm gate length SOI MOSFETs, and both two different types of substrate are fabricated in same design, the only difference indicates an inserted trap-rich layer for high resistivity substrate devices. Figure 4.8. shows the five-terminals SOI device modeling, which is similar to Figure 2.1.

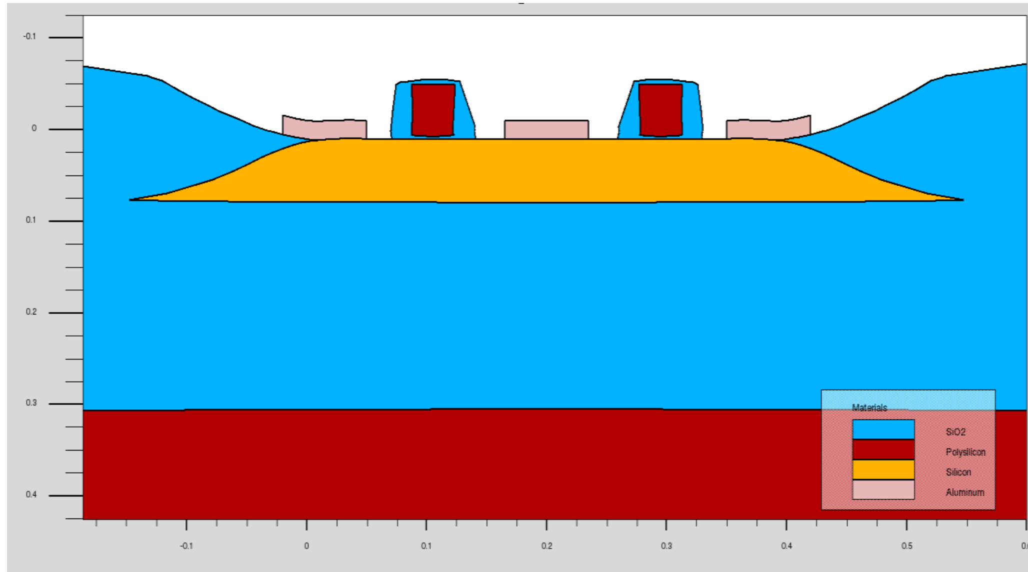

Figure 4.8. 2D Cross-section for five-terminals SOI device with 40 nm gate length, 225 nm thickness for the buried oxide layer, and both devices share an 80 nm thick active silicon region. The red bottom region indicates polysilicon formed by a chemical vapor deposition step with one-micron thickness.

Compared to the resistivity of conventional bulk silicon substrates, which is ~ 13.5 kΩ.cm, the resistivity of the trap-rich, high resistivity substrate is 1-10 kΩ.cm, around 1000 times higher than the bulk substrate. The thermal conductivity value of polysilicon (10 $W.m^{-1}.K^{-1}$) is around 14 times lower than bulk substrate (140 $W.m^{-1}.K^{-1}$), which means the trap-rich, high resistivity substrates involve more traps in the device with lower thermal conducting abilities. The simulation with five-terminals SOI device offers the temperature distribution among the whole of device. Basically, the five-terminals structure is mirrored from left to right, and the device size extends to be doubled as before, since it has been proved, the heater and thermometer will not impact each other due to the measured low parasitic resistance, 5 to 6 Ohms in total from the source or drain contact to the pads.

4.3. Theoretical Model

To have accurate modeling of self-heating effects, the heat conduction model has to be coupled self-consistently with an appropriate transport model. There are two distinct processes that comprise heat conduction: heat generation and heat dissipation. Due to the application of bias in the device and the presence of high electric fields, there are hot electrons in the system, which, interacting with the optical phonons and acoustic phonons transfer the heat to the phonon bath. Next, the heat dissipation through the device depends on the different thermal conductivities of the materials the device is made of. In the whole process, the interaction time among hot electrons, optical phonons and acoustic phonons is under the picosecond level [7]. Based on analyzing phonon dispersions, energy is transferred from hot electrons to optical phonons with high energies but low group velocities, while for acoustic phonons it is the opposite i.e. low energies but high group velocities [31]. This indicates that the heat conduction mainly depends on the high velocity acoustic phonons. Therefore, in order to promote heat conduction in nano-scaled devices, high-energy optical phonons need to be decomposed into low-energy acoustic phonons. However, due to the fact that the time to transfer energies between optical phonons and acoustic phonons is 50 to 100 times slower than the time it takes for hot electrons to transfer energy to both optical and acoustic phonons, there is a non-thermal equilibrium state between optical and acoustic phonons and hot electrons are generated near regions with high electric fields [18] [31]. This also explains why the scattering process between hot electrons and optical phonons takes the dominant role of energy transfer, with transfer of energy from optical phonons to acoustic phonons, and finally the heat dissipation from acoustic phonons to the material [32]. Overall, the rate at which heat is generated is faster

than the rate at which it is dissipated, leading to the self-heating effect, especially for devices with low thermal conductivity materials [39]. In this section, self-heating effects are simulated by solving the heat conduction equation self-consistently with the Poisson equation and appropriate transport models for the electrons. Since this is a short channel device and there is significant velocity overshoot, the energy balance transport model is most appropriate.

4.3.1. Fourier Law of Heat Conduction

Thermal conduction describes the internal energy transfer or dissipation by particle collisions and particle movement [26]. The Fourier law of heat conduction indicates that heat transfer or dissipation can be described in terms of the thermal conductivity and the temperature gradient. As equation (4.1) shows, the differential form of the Fourier law of heat conduction, through the material is proportional to the negative value of the temperature gradient.

$$\Phi = -\,k * \nabla T \tag{4.1}$$

Where

Φ, is the local heat flux density, $W \cdot m^{-2}$

k, is the material's conductivity, $W \cdot m^{-1} \cdot K^{-1}$

∇T, is the temperature gradient, $K \cdot m^{-1}$

According to equation (4.1), the heat flows in the direction opposite of the temperature gradient. Fourier’s law of thermal conduction is the fundamental rule for heat transfer, for example, Newton’s law of cooling comes from the discrete analog of Fourier’s law [27],

while Ohm's law comes from the electrical analog [28], and Fick's laws of diffusion comes from the chemical analogue [29]. It explains the heat flow from high temperature to low temperature region.

4.3.2. Drift-Diffusion (DD) Transport Model

Derived from the Boltzmann transport equation (BTE), the drift-diffusion (DD) transport model offers both a steady-state and transient description for device simulation. The DD model simulates particle movement under diffusion processes. It is widely used for approximate simulation of planar or FinFET devices [35]. Basically, it describes random walk under thermal equilibrium, drift under the applied electric field, and diffusion due to the concentration gradient as shown in Figure 4.9.

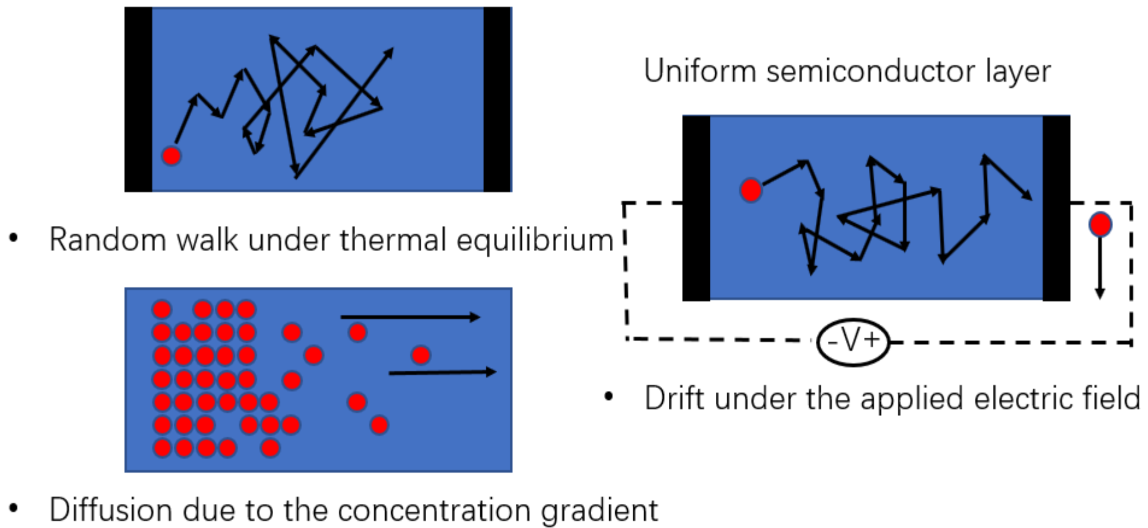

Figure 4.9. Summary of drift diffusion (DD) transport mechanisms

In the classical drift diffusion model, the drift component is driven by the electric field and the diffusion component is driven by the electron density gradient [30]. As equations (4.2), (4.3) show the DD model consists of the electron and hole continuity equations, respectively [33].

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \mathbf{J}_n + U_n \tag{4.2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \mathbf{J}_p + U_p \tag{4.3}$$

Where U_n and U_p are the net generation-recombination rates for electrons and holes, J_n and J_p are the electron and hole current densities, as equations (4.4) (4.5) show.

$$J_n = qn(x)\mu_n E(x) + qD_n \frac{dn}{dx} \tag{4.4}$$

$$J_p = qp(x)\mu_p E(x) - qD_p \frac{dn}{dx} \tag{4.5}$$

Where

q, the elementary charge

μ_n, the electron mobility, $cm^2/(V \cdot s)$.

μ_p, the hole mobility, $cm^2/(V \cdot s)$.

D_n, diffusion coefficient of electrons, m^2/s

D_p, diffusion coefficient of holes, m^2/s

J_n, the electron current density, $A\ m^{-2}$

J_p, the hole current density, $A\ m^{-2}$

4.3.3. Energy Balance Transport Model

For long channel devices, in which transport is collision-dominated, the DD model is a good approximation. For short channel devices, in which ballistic transport effects play a significant role, to overcome the limitation of the drift diffusion model, an additional balance equation term is added for the current density that is proportional to the gradient of the carrier temperature [34] [36]. In the DD model approach, the hot electron is assumed to be in thermal equilibrium, which indicates that the lattice temperature equals the carrier temperature. However, in the short channel device with high electric field, the energy and temperature of electrons has increased, and the driving force also needs to involve the additional temperature gradient plus the density gradient and the high electric field [30]. Furthermore, the average energy lags behind the fast-increasing electric field, and the rise of an average energy lag leads to an overshoot in the carrier saturation velocity. In particular, due to the ballistic transport effect, the saturation velocity has to be approximately doubled compared to long channel devices. Therefore, based on the device size continuously shrinking down, it is necessary to exchange the drift diffusion transport model to hydrodynamic or energy balance models due to the significant velocity overshoot. Altas allows use of an energy balance and a hydrodynamic transport models are both derived from the Boltzmann transport equation. Equations (4.6) and (4.7) depict the current densities for an energy balance transport model. Basically, the first two terms on the right hand side (RHS) of the equations are exactly the same as in the DD model. The difference is the third term that is a function of the electron temperature.

$$J_N = qn\mu_n E + qD_N \nabla n - qn\mu_n P_n \nabla \mathrm{T} \tag{4.6}$$

$$J_P = qp\mu_p E - qD_P \nabla p - qp\mu_p P_p \nabla \mathrm{T} \quad (4.7)$$

In general, as the device shrinks down, there is less scattering and interaction of electrons and phonons in the channel, and consequently a smaller amount of energy transferred to the lattice. Then, carrier temperature can be different from the lattice temperature for energy balance transport model as equation (4.8) shows [38]. In this study, an energy balance transport model was used for electron transport.

$$\nabla \cdot \boldsymbol{S}_n = \boldsymbol{E}\boldsymbol{J}_n - \frac{3\mathrm{k_B}}{2}\left(\frac{\partial n T_n}{\partial t} + RT_n + n\frac{T_n - T_\mathrm{L}}{\tau_{e,n}}\right) \quad (4.8)$$

In equation (4.8)

S_n, is flux of energy (or heat) from carrier to lattice. ($W \cdot m^{-2}$ or $J \cdot m^{-2} \cdot s^{-1}$)

T_n, is carrier temperature, (K)

T_L, is lattice temperature, (K)

4.4. Temperature Distribution Comparison Between Trap-Rich, High Resistivity SOI Substrates and Conventional Bulk Silicon Substrate SOI Devices.

Once a theoretical model has been chosen, we performed a number of simulations. Silvaco provides a function to display the lattice temperature distribution for the whole device and as Figure 4.10. shows, there is an increased temperature on the thermometer side, and the appearance of a hot spot on the heater side. For better visualization, Figure 4.11. shows the zoomed-in version of the channel region. In a previous analysis of bulk CMOS devices, the heat goes to the bulk substrate primarily and the temperature of the heater is 2.5 or 3 times higher than the temperature of the thermometer [15]. Due to the lower thermal conductivity of the SOI device, especially for trap-rich, high resistivity SOI

substrate devices, the heat generated in the channel cannot be dissipated through the substrate rapidly, and there is a clear evidence that the heat dissipates from the channel to the metal contact layer, and the temperature of the thermometer is only about 20 degrees Kelvin lower than the temperature of the hot spot.

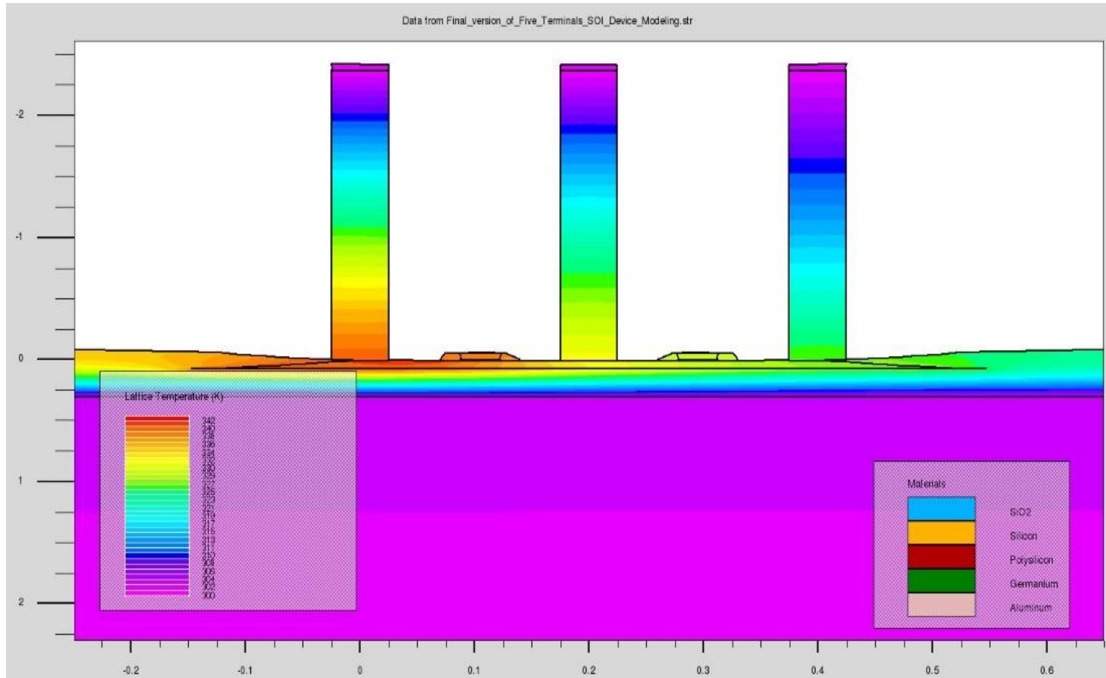

Figure 4.10. Temperature distribution for 40nm gate length SOI NFET pairs.

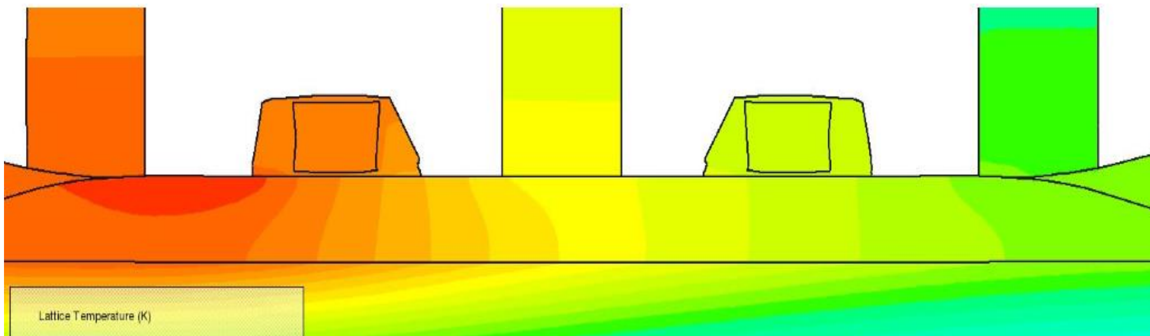

Figure 4.11. A closer look at the temperature distribution, the heat transfer from high temperature to lower temperature, and the thermometer temperature is around 20-degree Celsius lower compared to the heater temperature.

To confirm where the heat flows a comparison between devices with thick metal contacts and without thick metal contacts, is shown in Tables 4.2 and 4.3. The measurement results indicate that the two types of substrates have similar performance for the self-heating effect as Figure 3.5. shows in chapter 3, so the averaged values of calibrated temperature changes for two types of substrates are used as references to compare with the simulation results.

Based on the results presented in Tables 4.2 and 4.3, the temperature of trap-rich, high resistivity substrate devices without thick metal contacts is higher than that in conventional bulk silicon substrate SOI devices. As expected, the material with lower thermal conductivity value leads to higher temperature operation, as the thermal conductivity of the trap-rich layer, poly-crystalline silicon is around 10-15 times lower than that of the bulk substrate, single crystal silicon [18], leading to the 20 degrees Kelvin difference. However, with thick metal contacts, both types of SOI substrate devices have similar performance based on the temperature increase. The differences between simulations with or without thick metal contacts indicate that, instead of heat dissipating primarily through the bulk substrate [15], the metal layers can also dissipate heat and decrease the device temperature for low thermal conductivity SOI devices.

Note that the simulation results are only 5 degrees Kelvin higher than the measurement results. The reason for this difference may be due to the fact that not only the metal interconnects can dissipate heat, but also heat can flow away through the surrounding glassy layers or air gaps.

	Temperature calibrated by measurement results (K)	Simulation results of temperature captured on thermometer by trap-rich, high resistivity SOI substrate without thick metal (K)	Simulation results of temperature captured on thermometer by conventional bulk silicon SOI substrate without thick metal (K)
Vg=0.5V	315	326	313
Vg=0.75V	350	369	350
Vg=1V	385	413	385

Table 4.2. A comparison between the temperature captured on the thermometer NFET measurements and simulation results for two types of SOI substrate device without thick metal contact.

	Temperature calibrated by measurement results (K)	Simulation results of temperature captured on thermometer by trap-rich, high resistivity SOI substrate with 2μm thick metal (K)	Simulation results of temperature captured on thermometer by conventional bulk silicon SOI substrate with 2μm thick metal (K)
Vg=0.5V	315	317	315
Vg=0.75V	350	357	355
Vg=1V	385	391	389

Table 4.3. A comparison between the temperature captured on the thermometer NFET measurements and simulation results for two types of SOI substrate device with 2 μm thick metal contact.

CHAPTER 5

DISCUSSION AND SUMMARY

Combining the experimental and simulation results, it is clear that devices on the trap-rich, high resistivity substrate have similar performance to those on conventional bulk silicon substrate SOI devices. In this chapter, we present a discussion about how to design a numerical simulation model with high accuracy, in which the material and the thickness of metal contact are included. Then combining the measurement and simulation results, there is a conclusion and further plans about how self-heating effects impact device performance.

5.1. Mesh Convergency

For the Silivaco simulation work, the numerical problem has been affected by mesh points design and calculation methods. Especially for this specific partially depleted silicon-on-insulator (PD-SOI) device, due to the floating body effect, the device body forms a capacitor against the SOI substrate, and charges accumulate on the capacitor, which cause off-state leakage and higher current consumptions [40]. There are two possible solutions for this situation, one is increasing the mesh points to trade-off with simulation time, another is using a more complicated method to calculate the mesh points. As mentioned in the Chapter 4.2, although Athena offers a mesh adaption module to optimize the mesh calculation, it is still hard to converge all the mesh points. Figure 5.1. shows an example of this, with the drain voltage swept from 0 to 1V, voltage step is 0.04V, under different gate voltage condition of 0.5V, 0.75V, 1V for both measurement results and simulation results of conventional bulk silicon substrate SOI devices. During bias voltages

in the simulation process, typically, there is an initial voltage bias on the drain with a smaller voltage step first, then Silvaco sweeps the initial voltage to the final target voltage with a larger voltage step. For example, the initial voltage is set as 0.04V, from 0V to 0.04V, the original voltage step sweeps on the drain is 0.04V. It usually sets the voltage step as 0.004V to have a better initial meshing attempt, after those ten steps sweeping to 0.04V, then continues the bias voltage with 0.04V step to 1V. However, due to the floating body effect of SOI devices, it has been tried 0.001V for main voltage step and initial voltage step sets as small as 0.0001V. Figure 5.1. indicates the conventional bulk silicon substrate under gate voltage up to 0.75V condition, the simulations are not converged even with a small voltage step, and it leads the curve in the wrong direction.

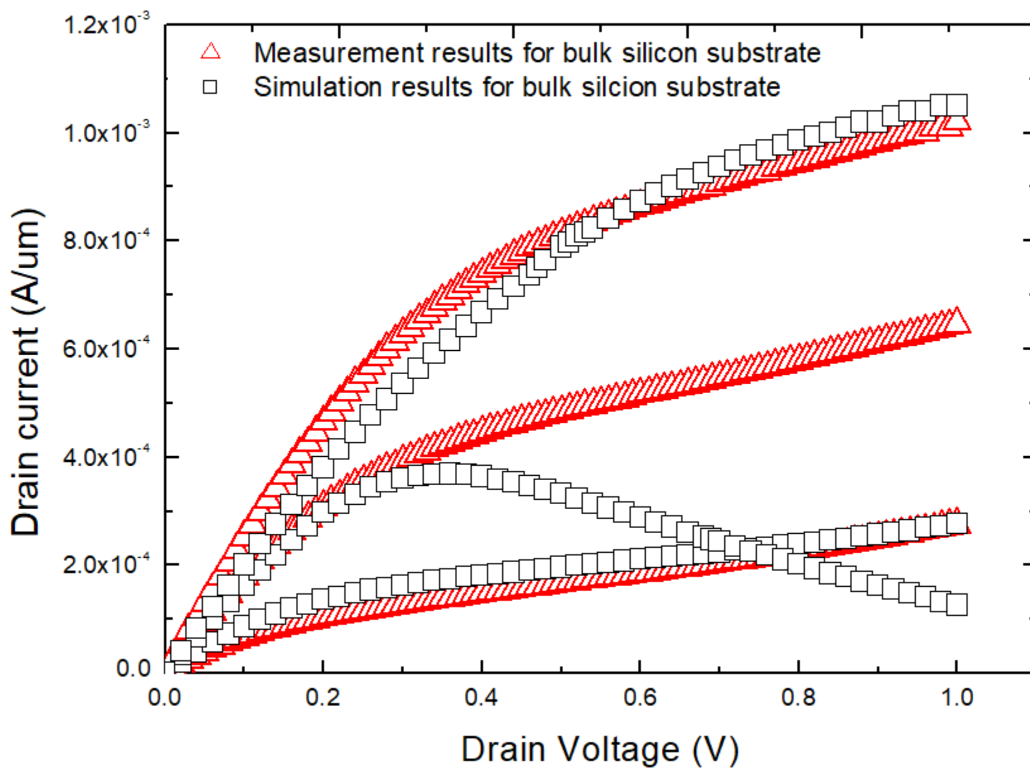

Figure 5.1. Comparison between measurement and simulation results for conventional bulk silicon substrate with mesh convergency problem for Vg=0.75V (middle open black square curve).

There is another possible way to solve the mesh convergence problem by using a more complicated method with more trap times. Obviously, it is also a trade-off and is a time-consuming method, but Figure 5.2. shows the family-of-curves of both two types substrate under various gate voltage converged successfully with the same numerical model. The Newton method is the most widely used approach for calculating mesh points, by using the 'Gummel Block Newton' method with 60 times for maxtraps, which means there are 60 chances to sweep the current voltage to the next voltage by using various voltage steps if the original voltage step does not converge. In other words, the 'Gummel Block Newton' method can increase the accuracy of the simulation and solve the convergence problem properly.

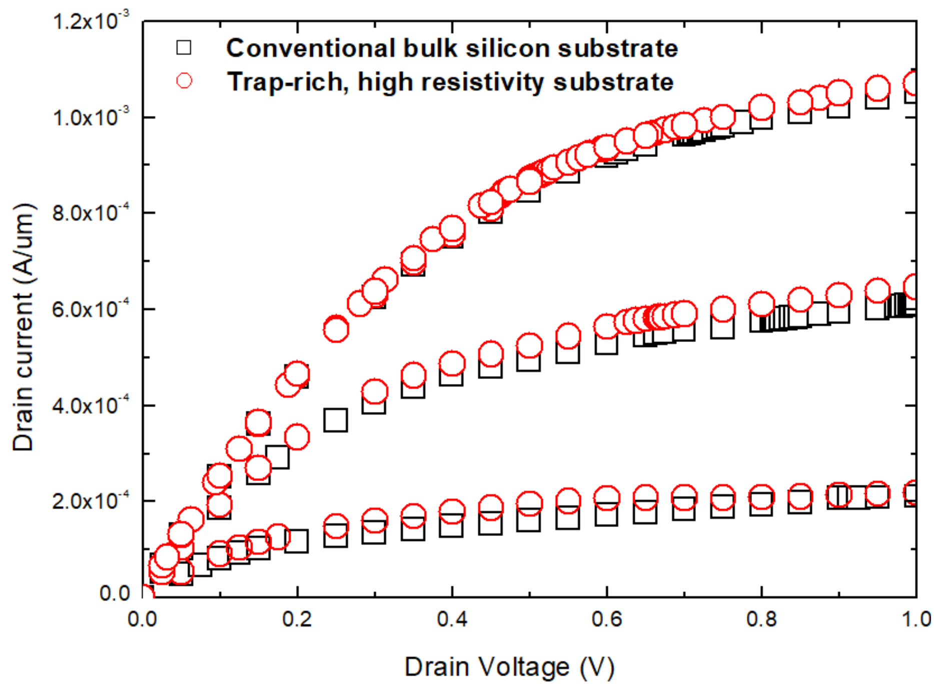

Figure 5.2. Comparison between simulated family-of-curves for both two types of substrate under various gate voltages, 0.5V, 0.75, 1V. The open black squares represent conventional bulk silicon substrate, while the open red circles present trap-rich, high resistivity substrate devices by using 'Gummel Block Newton' method.

5.2. Metal Contact Material

As an indispensable part for device modeling, metal contacts are required for the 40 nm gate length NFET pairs of heater and thermometer. In Silvaco, it is not possible to simulate temperature distribution with thick metal contacts. This is because all the metal layers are regard as a line or a point for the thermal boundary setting. In this work, a heavily doped semiconductor, germanium (Ge), instead of copper (Cu), which is used in manufacturing process, is used as the material for the metal contact. In Silvaco, it is possible to set the material properties and define a new material. For example, the band gap (eV), electron and hole density of states (cm^{-3}), dielectric permittivity, thermal conductivity ($W \cdot cm^{-1} \cdot K^{-1}$), mobility for electrons and holes ($cm^2/(V \cdot s)$) can all be specified. All the properties of the material need to be redefined before using.

As described in previous chapters, the parasitic resistance for this specific 40 nm gate length device is around 5 to 6 Ohms, and it can be embedded to the metal contact by transferring the electrical resistance to thermal resistance. Equation 5.1 shows the resistance in terms of electrical resistivity, ρ, length of contact, L, and area of contact, A.

$$R = \frac{\rho L}{A} \tag{5.1}$$

By knowing the electrical resistivity of copper and the total parasitic resistance, it is possible to determine the ratio of length and area of contact, then combining the thermal conductivity of copper with the calculated ratio, the thermal resistance based on copper can be determined. Then using the designed length and area of the contact, the equivalent thermal conductivity value for germanium is calculated.

5.3. Thermal Boundary

The thickness of the substrate and metal determine the simulation of the thermal boundaries setting, but in practice there is no need model the whole device thickness to correctly simulate the temperature distribution and heat flow dissipation. In this study, local self-heating effects are used to simulate the SOI device, which includes the transistor level, 10-100 nanometer, and the metallization level, 1-100 micron. Comparing numerical simulation for NFETs with a 40 nm gate length and 500 nm of total width. Figure 5.3. indicates that the current drive is similar. However, as shown in Figure 5.4 the simulated temperature may not be properly reproduced if the simulated substrate is too thin. For example, Figure 5.4. confirms one-micron thickness for trap-rich, high resistivity substrate is thick enough for thermal boundaries setting. Otherwise if it is less than one-micron thick, the thermal boundary setting may affect the temperature calibration and temperature distribution.

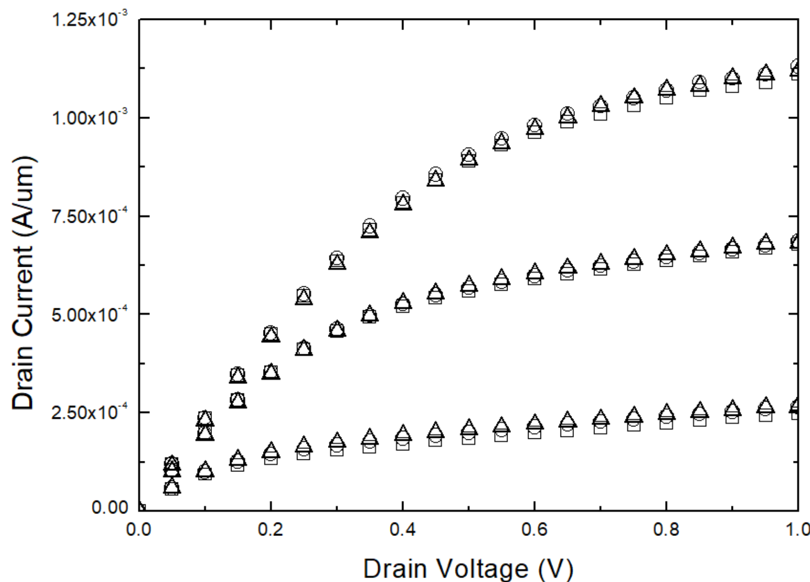

Figure 5.3. Comparison of simulated family-of-curves for various substrate thickness. The open circles are for substrate thickness=0.1um, squares for substrate thickness=1um, triangles for substrate thickness=5um, under different gate voltage, 0.5V, 0.75V, 1V.

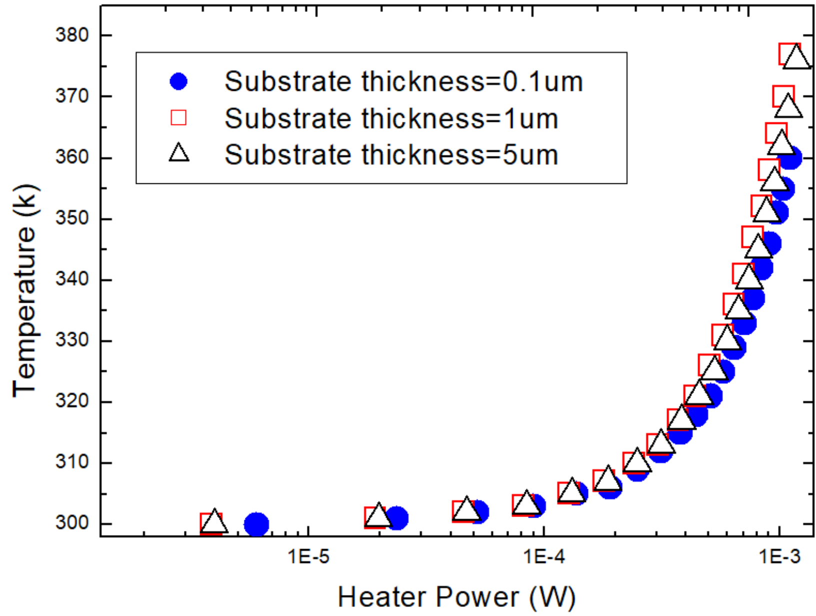

Figure 5.4. Comparison of the simulated temperature determined for different substrate thickness. The blue solid circles are for a substrate thickness=0.1um, red open squares for substrate thickness=1um, and black open triangles for substrate thickness=5um.

5.4. Summary and Further Plan

Both experimental results and simulation results fit together and show the amount of increased temperature are similar for the 40 nm n-channel MOSFETs on conventional bulk SOI substrates and trap-rich, high resistivity SOI substrates. Due to the thermal conductivity of the poly-crystalline trap-rich layer which is 10-15 times lower than the SOI channel region [18], we expect more heating to be created by the trap-rich substrate device. However, there is not much difference in the self-heating created, and the numerical device model simulation results indicate that heat is also dissipated through the metals layers instead of primarily through the bottom substrate. Unlike the numerical simulation of planar and FinFETs transistors [15] [17] that show the increased temperature of the heater is around 2 to 3.5 times higher than the temperature at the thermometer side, and explain

that the heat flow goes through the bulk substrate. However, based on this study, 40 nm n-channel MOSFETs measured on both conventional bulk SOI substrate and trap-rich, high resistivity SOI substrates shows similar performance under self-heating conditions. The previous simulation [15] [17] only modeled up to the metal-1 layer, and maybe that is the main reason that cause this difference. Also, there it is no need to calibrate the whole device including all the substrate and metal contact layers. Therefore, choosing a suitable thickness is also important for numerical simulation. Using the equivalent electrical resistance to transfer the thermal resistance and thermal resistivity for metal layers also increases the accuracy of the simulation instead of considering metal-1 only. Overall, an accurate numerical simulation can help with the understanding of temperature distribution and heat flow in SOI MOSFET devices. Although the simulation work probably underestimates the conditions to model the device, there are still some different ways to increase the accuracy of the simulation level. The most common ways are to increase the mesh points, decrease the sweep and the voltage steps, and choose a more accurate transport equation, but it results in a tradeoff for simulation timing. Furthermore, due to the floating body effect of SOI devices, the convergence issue is the most challenging problem during the whole simulation process. In this study, increasing the trap parameters and number of mesh points has been to overcome convergence problems and a poor initial guess situation.

Indeed, the buried oxide (BOX) used for the SOI substrate leads to self-heating effects, and becomes a more serious problem for developing the SOI technique, because of the 100 times lower thermal conductivity of SiO_2, 1-1.5 $W.m^{-1}.K^{-1}$ [8]. Therefore, how to reduce the self-heating effect becomes more and more important, and it also could be an interesting

topic for future research plans. There are two possible ways to decrease the impact of self-heating, use a material with a high thermal conductivity value [42], or use a dual-gate device instead of the front gate only [43].

Comparing the thermal conductivity of SiO_2, the high thermal conductivity material, for example, diamond and aluminum nitride (AlN), as Table 5.1. shows, the thermal conductivity value and dielectric constant comparison with SiO_2, high thermal conductivity materials have visible benefits for heat dissipation. Even compared to thermal conductivity of bulk silicon, 140 $W.m^{-1}.K^{-1}$, both silicon-on-diamond and silicon-on-aluminum nitride (SOAlN) also have excellent performance with heat conducting abilities. So by using high thermal conductivity materials it will be possible to reduce the impact of self-heating effects in nano-scaled devices. Moreover, dual-gate SOI devices indicate that the bottom gate is better from a thermal perspective, and based on the lattice temperature profile, dual-gate SOI devices offer 1.5-1.7 times larger amount of current than regular SOI devices with the same current degradation [41].

Insulating box material	Dielectric constant	Thermal conductivity ($W.m^{-1}.K^{-1}$)
SiO_2	3.9	1.38
Diamond	5.68	2000
AlN	9.14	272

Table 5.1. Insulator material properties comparison.

As self-heating effect can degrade the current and limit the lifetime of devices, engineers typically focus on the self-heating effect under DC conditions rather than AC

conditions. Based on the measurement and simulation results for the past few years, the temperature increase of silicon devices under DC conditions can reach 100 Celsius [15], and only 10 Celsius under AC conditions [44]. It indicates that the self-heating effect under AC conditions has less impact than operating under DC conditions [45],[46]. However, based on the difference between DC and AC operating environments, the voltage applied on the device is either a constant value all the time or a discontinuous value in certain time. Furthermore, the self-heating effect is caused by heat accumulation in the device, and the rate of heat generation (τ ~0.1 ps) is 100 times faster the rate of heat conduction between optical phonons and acoustic phonons (τ ~10 ps) [7]. So if the experimental or simulation is long enough, there may be sufficient heat accumulation caused by the difference between heat generated and heat conduction [47] [48]. Therefore, studying the impact of self-heating effects under AC conditions may also towards another research direction.

Overall, understanding the impact of self-heating effect for SOI can optimize the RFIC applications. For example, RF power amplifiers (PAs) generally operate at less than 50% efficiency because of high temperature risk, and one or multiple NFET thermometers can be placed around a CMOS power amplifier to track the local temperature for built-in self-test applications. This will lead to only a minimal increase in die area and power consumption but will protect the PAs before they are damaged by overheated.

REFERENCES

[1] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. Soong, and J. C. Zhang, "What will 5G be?" in IEEE J. Sel. Areas Commun., vol. 32, no. 6, pp. 1065–1082, Jun. 2014.

[2] Marshall, Andrew; Natarajan, Sreedhar (2002). SOI design: analog, memory and digital techniques. Boston: Kluwer. ISBN 0792376404.

[3] J. P. Colinge, Silicon-On-Insulator Technology: Materials to VLSI, 2nd Ed. Kluwer Academic Publisher, 1997.

[4] Olejarz, Piotr et al. “0.5 μW Sub-Threshold Operational Transconductance Amplifiers Using 0.15 Mm Fully Depleted Silicon-on-Insulator (FDSOI) Process.” Journal of low power electronics and applications 2.2 (2012): 155–167. Web.

[5] X. Zhang, Mehr, P., & Thornton, T. (2020). Self-Heating in 40 nm SOI MOSFETs on High Resistivity, Trap-Rich Substrates. IEEE Transactions on Nanotechnology, 19, 42–46. https://doi.org/10.1109/tnano.2019.2952759

[6] C. Li, M. Wang, T. Chi, A. Kumar, M. Boenke, N. Cahoon, A. Bandyopadhyay, A. Joseph, and H. Wang “A high-efficiency 5G K/Ka-band stacked power amplifier in 45 nm CMOS SOI process,” in Texas Symp. on Wireless and Microw. Circuits and Systems, Waco, TX, 2017, pp. 1-4.

[7] K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, “Modeling Thermal Effects in Nanodevices,” in IEEE Trans. Electron Devices, vol. 55, no. 6, pp. 1306 – 1316, June 2008.

[8] M. Asheghi, M. N. Touzelbaev, K. E. Goodson, Y. K. Leung, and S. S. Wong, “Temperature-dependent thermal conductivity of singlecrystal silicon layers in SOI substrates,” J. Heat Transfer, vol. 120, pp. 30–36, Feb. 1998.

[9] J. P. Raskin, A. Viviani, D. Flandre, and J. P. Colinge, “Substrate crosstalk reduction using SOI technology,” IEEE Trans. Electron Devices, 1997.

[10] B. K. Esfeh et al., “RF SOI CMOS technology on 1st and 2nd generation trap-rich high resistivity SOI wafers,” Solid-State Electron., vol. 128, pp. 121–128, 2017.

[11] Y. Shim, J. Raskin, C. Roda Neve, and M. Rais-Zadeh, “RF MEMS passives on high-resistivity silicon substrates,” IEEE Microw. Wireless Compon. Lett., vol. 23, no. 12, pp. 632–634, Dec. 2013.

[12] P. D. Maycock, “Thermal conductivity of silicon, germanium, III-V compounds and III-V alloys,” Solid-State Electron., vol. 10, pp. 161–167, 1967.

[13] X. Zhang, P. Mehr, D. Vasileska, and T. J. Thornton, “Self-heating in SOI MOSFETs at the 45 nm node,” Proc. 13th IEEE Nanotechnology. Mater. Devices Conf., Portland, OR, USA, Oct. 2018, pp. 1–4.

[14] P. Paliwoda et al., "Self-Heating Assessment on Bulk FinFET Devices Through Characterization and Predictive Simulation," in IEEE Transactions on Device and Materials Reliability, vol. 18, no. 2, pp. 133-138, June 2018, doi: 10.1109/TDMR.2018.2818930.

[15] E. Bury, B. Kaczer, P. Roussel, R. Ritzenthaler, K. Raleva, D. Vasileska, and G. Groeseneken “Experimental validation of self-heating simulations and projections for transistors in deeply scaled nodes” IEEE International Reliability Physics Symposium, Waikoloa, HI, 2014, pp. XT.8.1-XT.8.6. doi: 10.1109/IRPS.2014.6861186, 2014.

[16] Y. Tsividis “Operation and Modeling of the MOS Transistor” 2nd edition, published by Oxford University Press, Oxfodr, UK, 1999.

[17] E. Bury, B. Kaczer, J. Mitard, N. Collaert, N. S. Khatami, Z. Aksamija, D. Vasileska, K. Raleva, L. Witters, G. Hellings, D. Linten, G. Groeseneken, A. Thean, “Characterization of self-heating in high-mobility Ge FinFET pMOS devices”, 2015 Symposium on VLSI Devices, pp. T60 - T61, doi: 10.1109/VLSIT.2015.7223703.

[18] McConnell, A.D, S Uma, and K.E Goodson. “Thermal Conductivity of Doped Polysilicon Layers.” J.MEMS 10.3 (2001): 360–369. Web

[19] C. C. Lin and M. E. Law, “2-D Mesh Adaption and Flux Discretizations for Dopant Diffusion Modeling”, IEEE Trans. CAD, v. 15, p. 194, 1995.

[20] C. C. Lin and M. E. Law, “Mesh Adaptation and Flux Discretizations for Dopant Diffusion Modeling”, NUPAD-V, p. 151, 1994.

[21] Pearson, Karl (1916). "Mathematical contributions to the theory of evolution, XIX: Second supplement to a memoir on skew variation". Philosophical Transactions of the Royal Society A. 216 (538–548): 429457. Bibcode:1916RSPTA.216..429P. doi:10.1098/rsta.1916.0009. JSTOR 91092.

[22] A.F. Burenkov, F.F.Komarov, M.A.Kumakhov, and M.M.Temkin. Tables of Ion Implantation Spatial Distributions. Gordon & Breach Science Publishers, 1986.

[23] Juang, Miin-Horng, and Yi-Ming Chiu. “Effects of a Lightly-Doped-Drain (LDD) Implantation Condition on the Device Characteristics of Polycrystalline-Si Thin-Film Transistors.” Semiconductor Science and Technology 21.3 (2006): 291–294. Web.

[24] Akinwande, A.I, P.J Vold, and D.E Grider. “An Asymmetrical Lightly Doped Drain (LDD) Self-Aligned Gate Heterostructure Field Effect Transistor.” IEEE Transactions on Electron Devices 35.12 (1988): 2450–2451. Web.

[25] Liu, Xiangyu et al. “Study of Novel Junctionless Ge n-Tunneling Field-Effect Transistors with Lightly Doped Drain (LDD) Region.” Superlattices and microstructures 102 (2017): 7–16. Web.

[26] Bergman, Theodore L.; Lavine, Adrienne S.; Incropera, Frank P.; Dewitt, David P. (2011). Fundamentals of heat and mass transfer (7th ed.). Hoboken, NJ: Wiley. ISBN 9780470501979. OCLC 713621645.

[27] Yan, H, and Hao Guo. “Efficiency and Its Bounds for Thermal Engines at Maximum Power Using Newton’s Law of Cooling.” Physical review. E, Statistical, nonlinear, and soft matter physics 85.1 Pt 1 (2012): 011146–. Web.

[28] Fuller, Robert G. Study Modules for Calculus-Based General Physics. [Includes Modules 24-26 Electric Potential; Ohm’s Law; and Capacitors] . S.l: Distributed by ERIC Clearinghouse, 1975. Print.

[29] Margetis, Dionisios. “Homogenization of Reconstructed Crystal Surfaces: Fick’s Law of Diffusion.” Physical review. E, Statistical, nonlinear, and soft matter physics 79.5 Pt 1 (2009): 052601–. Web.

[30] Grasser, Tang. “A Review of Hydrodynamic and Energy-Transport Models for Semiconductor Device Simulation.” Proceedings of the IEEE 91.2 (2003): 251–274. Web

[31] Gada, Manan Laxmichand. “Modeling of Self-Heating Effects in 25nm SOI Devices.” Arizona State University, 2013. Print.

[32] J. Lai and A. Majumder, “Concurrent Thermal and Electrical Modeling of Sub-Micrometer Silicon Devices”, *J. Appl. Phys*. Vol. 79, pp. 7353-7361 (1996).

[33] D.Vasileska, “Drift-Diffusion model: introduction”, online materials to nanohub.org. resource link:https://nanohub.org/resources/1545/download/ddmodel_introductory_part_word.pdf

[34] R. Stratton, “Diffusion of hot and cold electrons in semiconductor barriers,” Phys. Rev., vol. 126, no. 6, pp. 2002–2014, 1962.

[35] J. Y. Sun, R. H. Liu, X. J. Li, Y. B. Sun, Y. L. Shi, S. M. Chen, S. J. Hu, & A. Guo, Self-Heating Effects Investigation on Nanoscale FinFET and Its Thermal Resistance Modeling, Proceedings of IEEE International Conference on Solid-State

and Integrated Circuit Technology, 2018: 1–3

[36] K. Bløtekjær, “Transport equations for electrons in two-valley semiconductors,” IEEE Trans. Electron Devices, vol. ED-17, pp. 38–47, Jan. 1970.

[37] Yannis Tsividis, “MOS transistor”, Columbia university, online resource link: https://www.coursera.org/lecture/mosfet/ion-implantation-threshold-adjust-implant-SPxV7

[38] A. Shen, A. Q. Chen, D. Z. Ding and R. S. Chen, "Electron analysis of a deep sub-micrometer MOSFET device based on spectral element method," 2017 International Applied Computational Electromagnetics Society Symposium (ACES), Suzhou, 2017, pp. 1-2.

[39] E. R. Hsieh, M. R. Jiang, J. L. Lin, S. S. Chung, T. P. Chen, S. A. Huang, T. J. Chen, & O. Cheng, An Experimental Approach to Characterizing the Channel Local Temperature Induced by Self-Heating Effect in FinFET, IEEE Journal of the Electron Devices Society, 2018: 866–874.

[40] J. Chen et al., "A Tunnel Diode Body Contact Structure to Suppress the Floating-Body Effect in Partially Depleted SOI MOSFETs," in IEEE Electron Device Letters, vol. 32, no. 10, pp. 1346-1348, Oct. 2011, doi: 10.1109/LED.2011.2162813.

[41] Z. Chen, L. Sun, J. Liu, G. Su, & W. Zhou, Investigation of Geometry Dependence of Thermal Resistance and Capacitance in RF SOI MOSFETs, IEEE Transactions on Electron Devices, 2018, 65(10): 4232–4237.

[42] K. Raleva, D. Vasileska, S. M. Goodnick, Is SOD Technology the Solution to Heating Problems in SOI Devices? Electron Device Letters, IEEE, Volume 29, Issue 6, June 2008 Page(s):621 - 624.

[43] S.M. Goodnick, D. Vasileska, K. Raleva, “Is Dual Gate Device Better From a Thermal Perspective?”, Proceedings of 2008 SISPAD Conference, pp. 125 - 128.

[44] Myeong, Ilho et al. “Analysis of Self Heating Effect in DC/AC Mode in Multi-Channel GAA-Field Effect Transistor.” IEEE transactions on electron devices 66.11 (2019): 4631–4637. Web.

[45] M. A. Wahab, S. Shin and M. A. Alam, "3D Modeling of Spatio-temporal Heat-transport in III-V Gate-all-around Transistors Allows Accurate Estimation and Optimization of Nanowire Temperature," in IEEE Transactions on Electron Devices, vol. 62, no. 11, pp. 3595-3604, Nov. 2015, doi: 10.1109/TED.2015.2478844.

[46] H. Jiang, S. Shin, X. Liu, X. Zhang and M. A. Alam, "The Impact of Self-Heating

on HCI Reliability in High-Performance Digital Circuits," in IEEE Electron Device Letters, vol. 38, no. 4, pp. 430-433, April 2017, doi: 10.1109/LED.2017.2674658.

[47] D. Son, I. Myeong, H. Kim, M. Kang, J. Jeon and H. Shin, "Analysis of Electrothermal Characteristics of GAA Vertical Nanoplate-Shaped FETs," in IEEE Transactions on Electron Devices, vol. 65, no. 7, pp. 3061-3064, July 2018, doi: 10.1109/TED.2018.2832239.

[48] Myeong, D. Son, H. Kim and H. Shin, "Analysis of Self Heating Effect in DC/AC Mode in Multi-Channel GAA-Field Effect Transistor," in IEEE Transactions on Electron Devices, vol. 66, no. 11, pp. 4631-4637, Nov. 2019, doi: 10.1109/TED.2019.2942074.

APPENDIX A

SILVACO SIMULATION CODE

```
# (c) Silvaco Inc., 2017
#TITLE: SOI Process and Device Simulation

go athena

# Substrate mesh definition
line y loc=0       spac=0.0004   tag=top
line y loc=0.04     spac=0.002
line y loc=0.08     spac=0.005   tag=oxtop
line y loc=0.18     spac=0.1
line y loc=0.305    spac=0.02    tag=oxbot
#line y loc=1.305   spac=0.1    tag=surf
#for trap-rich, high resistivity substrate SOI device modeling
line y loc=2.305    spac=0.1    tag=botton

line x loc=-0.25   spac=0.025    tag=left
line x loc=0      spac=0.005
line x loc=0.1    spac=0.001
line x loc=0.2    spac=0.005    tag=right
#
region silicon xlo=left xhi=right ylo=top yhi=oxtop
region oxide xlo=left xhi=right ylo=oxtop yhi=oxbot
#region polysilicon xlo=left xhi=right ylo=oxbot yhi=surf
#for trap-rich, high resistivity substrate SOI device modeling
region silicon xlo=left xhi=right ylo=oxbot yhi=botton

init orient=100 c.phos=1e14 space.mult=1.5
structure outfile=Five_Terminals_SOI_Device_Modeling_1.str
#tonyplot Five_Terminals_SOI_Device_Modeling_1.str

# pad oxide and nitride mask
deposit oxide thick=0.004 div=1
deposit nitride thick=0.02 div=1

# from now on the situation is 2-D
etch    nitride left p1.x=-0.15
etch    oxide   left p1.x=-0.15
structure outfile=Five_Terminals_SOI_Device_Modeling_2.str
#tonyplot Five_Terminals_SOI_Device_Modeling_2.str

# field oxidation
method compress fermi grid.oxide=0.01 gridinit.ox=0.01
#method compress fermi adapt diff.smooth
diffus time=2 temp=1200 weto2 press=2.0 hcl.pc=0
structure outfile=Five_Terminals_SOI_Device_Modeling_3.str
```

```
#tonyplot Five_Terminals_SOI_Device_Modeling_3.str

etch nitride all
structure outfile=Five_Terminals_SOI_Device_Modeling_4.str
#tonyplot Five_Terminals_SOI_Device_Modeling_4.str

etch oxide start x=0.05 y=-0.9
etch continue x=0.35 y=-0.9
etch continue x=0.35 y=0.01
etch done x=0.05 y=0.01
structure outfile=Five_Terminals_SOI_Device_Modeling_5.str
#tonyplot Five_Terminals_SOI_Device_Modeling_5.str

# pwell formation including masking of the nwell
diffus time=15 temp=1000 dryo2 press=1.00 hcl=3
structure outfile=Five_Terminals_SOI_Device_Modeling_6.str
#tonyplot Five_Terminals_SOI_Device_Modeling_6.str

etch oxide thick=0.022

structure outfile=Five_Terminals_SOI_Device_Modeling_7.str
#tonyplot Five_Terminals_SOI_Device_Modeling_7.str

##############################################
# P-well Implant
implant boron dose=8e12 energy=30 BCA
structure outfile=Five_Terminals_SOI_Device_Modeling_8.str
#tonyplot Five_Terminals_SOI_Device_Modeling_8.str
##############################################

# welldrive starts here
diffus time=10 temp=1200 nitro press=11
diffus time=5 temp=1000 t.rate=-4.444 nitro press=12
structure outfile=Five_Terminals_SOI_Device_Modeling_9.str
#tonyplot Five_Terminals_SOI_Device_Modeling_9.str

etch oxide thickness=0.004
structure outfile=Five_Terminals_SOI_Device_Modeling_10.str
#tonyplot Five_Terminals_SOI_Device_Modeling_10.str
# gate oxide grown here:
diffus time=0.2 temp=700 dryo2 press=1.00 hcl=3
structure outfile=Five_Terminals_SOI_Device_Modeling_11.str
#tonyplot Five_Terminals_SOI_Device_Modeling_11.str

# extract a design parameter
```

```
extract name="gateox" thickness oxide mat.occno=1 x.val=0.2

##############################################
# vt adjust implant
implant boron dose=1.5e13 energy=15 BCA
structure outfile=Five_Terminals_SOI_Device_Modeling_12.str
#tonyplot Five_Terminals_SOI_Device_Modeling_12.str
##############################################

# polysilicon gate formation
depo poly thick=0.06 divi=2 c.phosphor=2e20
structure outfile=Five_Terminals_SOI_Device_Modeling_13.str
#tonyplot Five_Terminals_SOI_Device_Modeling_13.str

etch poly left p1.x=0.085
etch poly start x=0.125 y=0.008
etch cont x=0.2 y=0.008
etch cont x=0.2 y=-0.074
etch done x=0.125 y=-0.074
structure outfile=Five_Terminals_SOI_Device_Modeling_14.str
#tonyplot Five_Terminals_SOI_Device_Modeling_14.str

# oxidise polysilicon
method fermi compress  grid.oxide=0.01 gridinit.ox=0.01
#method fermi compress adapt diff.smooth
diffuse time=0.5 temp=800 weto2 press=1.0
structure outfile=Five_Terminals_SOI_Device_Modeling_15.str
#tonyplot Five_Terminals_SOI_Device_Modeling_15.str

##############################################
# N- LDD (n channel light doped source/drain)implant to minimize the hot carrier effect
#and short channel effect, the drain near the channel is doped less compared to the main
#drain area, to minimize the process complications, both source and drain are doped
#lightly near the channel region
implant phosphor dose=1.0e12 energy=10 tilt=0 rotation=0 BCA
structure outfile=Five_Terminals_SOI_Device_Modeling_16.str
#tonyplot Five_Terminals_SOI_Device_Modeling_16.str
##############################################
# create sidewalls
depo oxide thick=0.01 divisions=8
structure outfile=Five_Terminals_SOI_Device_Modeling_17.str
#tonyplot Five_Terminals_SOI_Device_Modeling_17.str

etch oxide dry thick=0.01
structure outfile=Five_Terminals_SOI_Device_Modeling_18.str
```

```
#tonyplot Five_Terminals_SOI_Device_Modeling_18.str

################################################
# S/D implant
implant arsenic dose=5.0e14 energy=5 BCA
structure outfile=Five_Terminals_SOI_Device_Modeling_19.str
#tonyplot Five_Terminals_SOI_Device_Modeling_19.str
################################################

method fermi compress  grid.oxide=0.01 gridinit.ox=0.01
diffuse time=1 temp=800 nitro press=1.0
structure outfile=Five_Terminals_SOI_Device_Modeling_20.str
#tonyplot Five_Terminals_SOI_Device_Modeling_20.str

etch oxide thickness=0.003
structure outfile=Five_Terminals_SOI_Device_Modeling_21.str
#tonyplot Five_Terminals_SOI_Device_Modeling_21.str

##################################################
deposit material="germanium" thick=2.315 divi=150 c.phosphor=1e21
structure outfile=Five_Terminals_SOI_Device_Modeling_22.str
#tonyplot Five_Terminals_SOI_Device_Modeling_22.str

etch material="germanium" left p1.x=-0.025
etch material="germanium" start x=0.025 y=0.03
etch continue x=0.175 y=0.03
etch continue x=0.175 y=-3
etch done x=0.025 y=-3
structure outfile=Five_Terminals_SOI_Device_Modeling_23.str
#tonyplot Five_Terminals_SOI_Device_Modeling_23.str
######################################################

# metal deposition and patterning for S/G/D
deposit material="Aluminum" thick=0.05 divi=50
structure outfile=Five_Terminals_SOI_Device_Modeling_24.str
#tonyplot Five_Terminals_SOI_Device_Modeling_24.str

etch material="Aluminum" left p1.x=-0.025
etch material="Aluminum" start x=0.025 y=0.02
etch continue x=0.175 y=0.02
etch continue x=0.175 y=-3
etch done x=0.025 y=-3
structure outfile=Five_Terminals_SOI_Device_Modeling_25.str
#tonyplot Five_Terminals_SOI_Device_Modeling_25.str
```

```
struct mirror right
structure outfile=Five_Terminals_SOI_Device_Modeling_26.str
#tonyplot Five_Terminals_SOI_Device_Modeling_26.str

# electrode definition
electrode name=gate x=0.1 y=-0.02
electrode name=g1 x=0.3 y=-0.02
electrode name=source x=0.2 y=-2.4
electrode name=drain x=0 y=-2.4
electrode name=d1 x=0.4 y=-2.4
electrode name=substrate backside
structure outfile=Five_Terminals_SOI_Device_Modeling_27.str
#tonyplot Five_Terminals_SOI_Device_Modeling_27.str


##########################################################################

go atlas

# set workfunction of gate
contact name=gate n.poly
#contact name=source resistance=135
#thermcontact name=substrate
#temperature=300

THERMCONTACT NUM=1 elec.num=4 X.MIN=-0.02 X.MAX=0.05 Y.MIN=-2.4 Y.MAX=-2.4 ext.temp=300
THERMCONTACT NUM=2 elec.num=3 X.MIN=0.165 X.MAX=0.235 Y.MIN=-2.4 Y.MAX=-2.4 ext.temp=300
THERMCONTACT NUM=3 elec.num=5 X.MIN=0.35 X.MAX=0.42 Y.MIN=-2.4 Y.MAX=-2.4 ext.temp=300
THERMCONTACT NUM=4 elec.num=6 X.MIN=-0.25 X.MAX=0.65 Y.MIN=2.305 Y.MAX=2.305 EXT.TEMP=300

# (a) Hydrodynamic simulation
material silicon taurel.el=2.5e-13 taumob.el=2.5e-13

#material="copper" TC.CONST=4
material mat="germanium" TCON.CONST TC.CONST=4
#material mat="germanium" TCON.CONST TC.CONST=0.482
material material="germanium" EG300=0.1
material material="germanium" NC300=2.8E19 NV300=1.04e19
material material="germanium" mun=21.27 mup=0
#material material="germanium" AFFINITY=3
material material="germanium" permittivity=1 permeability=1
```

```
##########################################################################
TAUMOB.EL specifies the relaxation time for electrons in the temperature dependent mobility model
#TAUMOB.HO specifies the relaxation time for holes in the temperature dependent mobility model
#TAUREL.EL specifies the relaxation time for electrons in the energy balance model
#TAUREL.HO specifies the relaxation time for holes in the energy balance model
##########################################################################

#active the self-heating effect
models hcte.el lat.temp print

##########################
#cvt---lombardi moility model
#srh---shockley-read-hall
#fermi---fermi statistics
#shi--shirahata
#############################

# do IDVD characteristics
output e.velocity ex.velocity
#E.VELOCITY specifies that the total electron velocity will be included in the standard structure file
#EX.VELOCITY specifies that the x-component of electron velocity will be included in the standard structure file.

solve init
method     Gummel Block Newton trap maxtraps=60
solve      prev

# save structure parameters
output con.band val.band
save  outfile=Five_Terminals_SOI_Device_Modeling_28.str
#tonyplot Five_Terminals_SOI_Device_Modeling_28.str

#######################################################################
######                   Family-of-curves characteristic                   ######
#######################################################################

#solve      vgate = 0. vstep=0.01 name=gate vfinal=0.05
#solve      vgate=0.05 vstep=0.05 vfinal=1 name=gate
#log        outf= Family_of_curves_characteristic.log
#solve      vdrain=0 vstep=0.02 name=drain vfinal=1
```

```
########################################################################
######                    Turn-on characteristic                  ######
########################################################################

solve      vdrain = 0. vstep=0.01 name=drain vfinal=0.05
solve      vdrain=0.05 vstep=0.05 vfinal=0.1 name=drain
log        outf= Turn_on_characteristic.log
solve      vgate=0 vstep=0.02 name=gate vfinal=1

log off

#tonyplot Family_of_curves_characteristic.log
tonyplot Turn_on_characteristic.log

save outf=Final_version_of_Five_Terminals_SOI_Device_Modeling.str
tonyplot Final_version_of_Five_Terminals_SOI_Device_Modeling.str

quit
```