Analytical Modeling and Development of GaN-Based Point of Load Buck Converter with

Optimized Reverse Conduction Loss

by

Gauri Koli

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Graduate Supervisory Committee:

Jennifer Kitchen, Chair
Bertan Bakkaloglu
Sule Ozev

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ABSTRACT

This work analyzes and develops a point-of-load (PoL) synchronous buck converter using enhancement-mode Gallium Nitride (e-GaN), with emphasis on optimizing reverse conduction loss by using a well-known technique of placing an anti-parallel Schottky diode across the synchronous power device. This work develops an improved analytical switching model for the GaN-based converter with the Schottky diode using piecewise linear approximations.

To avoid a shoot-through between the power switches of the buck converter, a small dead-time is inserted between gate drive switching transitions. Despite optimum dead-time management for a power converter, optimum dead-times vary for different load conditions. These variations become considerably large for PoL applications, which demand high output current with low output voltages. At high switching frequencies, these variations translate into losses that contribute significantly to the total loss of the converter. To understand and quantify power loss in a hard-switching buck converter that uses a GaN power device in parallel with a Schottky diode, piecewise transitions are used to develop an analytical switching model that quantifies the contribution of reverse conduction loss of GaN during dead-time.

The effects of parasitic elements on the dynamics of the switching converter are investigated during one switching cycle of the converter. A designed prototype of a buck converter is correlated to the predicted model to determine the accuracy of the model. This comparison is presented using simulations and measurements at 400 kHz and 2 MHz converter switching speeds for load (1A) condition and fixed dead-time values. Furthermore, performance of the buck converter with and without the Schottky diode is also measured and compared to demonstrate and quantify the

enhanced performance when using an anti-parallel diode. The developed power converter achieves peak efficiencies of 91.7% and 93.86% for 2 MHz and 400 KHz switching frequencies, respectively, and drives load currents up to 6A for a voltage conversion from 12V input to 3.3V output.

In addition, various industry Schottky diodes have been categorized based on their packaging and electrical characteristics and the developed analytical model provides analytical expressions relating the diode characteristics to power stage performance parameters. The performance of these diodes has been characterized for different buck converter voltage step-down ratios that are typically used in industry applications and different switching frequencies ranging from 400 KHz to 2 MHz.

DEDICATION

Dedicated to my parents, my brother and my friends for their constant support and understanding!

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1. INTRODUCTION

1.1 Motivation

Power converters find many applications in consumer electronics, low-power mobile devices, as well as systems requiring point of load power conversion in space, nuclear, automobile, and aero-space electronics. The fundamental requirements of any power system are its efficiency and reliability. For space and automobile applications, efforts are underway to minimize the size of power converters while maintaining their efficiency and reliability.

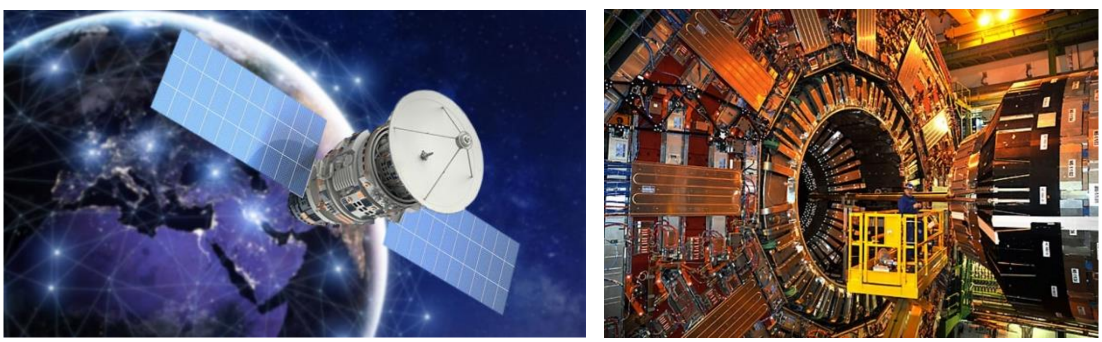

Figure 1. Power Converter Applications In Space Electronics And Particle Accelerator At CERN

The use of power converters in Point of Load (PoL) applications demands high load current capability (up to 5A peak) for high conversion ratios and smaller component size. Reduction in the component size can be achieved by integrating the power electronics system within a chip. This small form factor can be achieved by operating the converter at high switching frequencies. To avoid compromising efficiency and reliability, the power devices and the off-chip components must be rated higher than the maximum power required by the load. The most important component selection during the design of a power converter is the power switch. For decades, IGBT (insulated gate bipolar transistor), MCT (MOS controlled thyristor), MOSFET, and GTO (gate-turn off thyristor) devices have been the most popular selections for power switches in space electronic converters [1]. Silicon based power MOSFETs have been a popular choice for PoL converters in automotive, space, and other applications. The higher gate capacitance of silicon-based power FETs limits the operation of high efficiency medium power switching converters up to frequencies in the lower 100 KHz range , thus motivating the need for power devices that achieve the same performance parameters with higher switching frequencies.

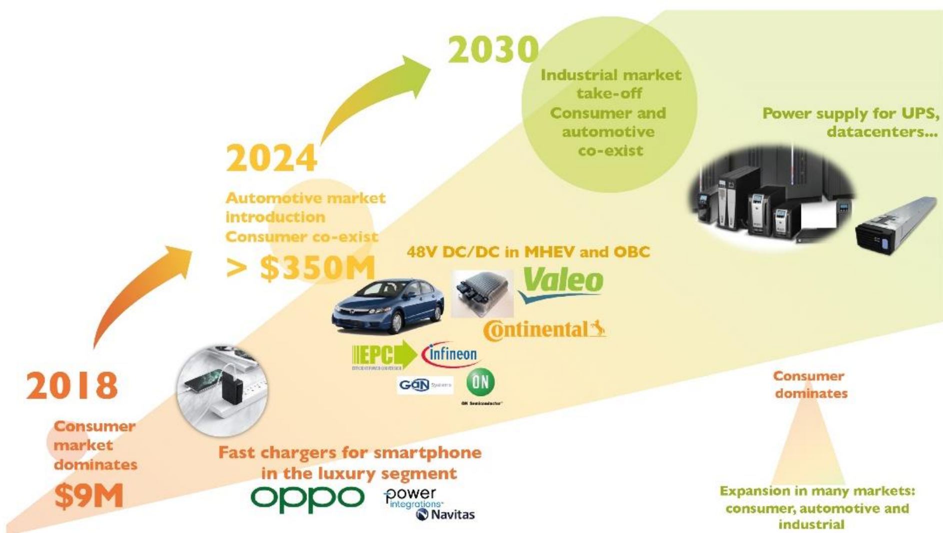

Figure 2. GaN Market Evolution And Trends

Being a wide-bandgap material, gallium nitride (GaN) has gained recent traction in power electronics, as it promises high power density with efficient thermal management, low gate charge leading to switching speeds higher than the silicon counterparts, higher allowable operating temperatures than silicon, and a much lower on state resistance [2]. GaN operates on a different principle than silicon. In GaN, the conduction layer beneath the gate is formed due to the two-dimensional electron gas (2DEG), unlike the inversion layer for a MOSFET. It has a higher electron mobility than the conducting channel in MOSFET, which translates to lower on-state-resistance. This gives the GaN-based PoL converters an advantage of achieving similar ranges of load current with higher efficiency compared to MOSFET-based PoL converters, while also being physically smaller.

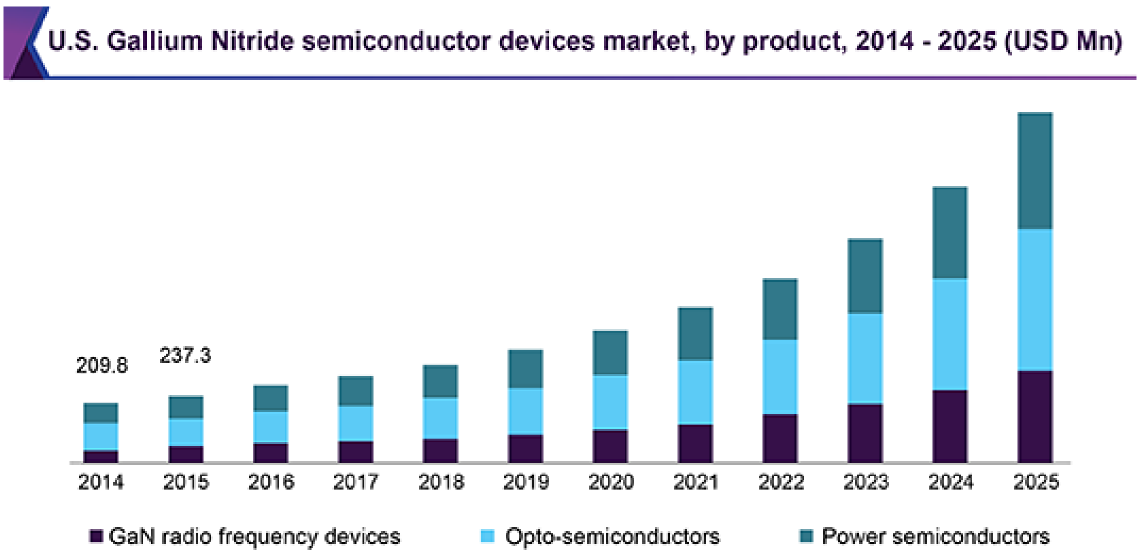

Figure 3. Application Of GaN In Various Semiconductor Sectors

GaN has seen a myriad of applications over the past decade ranging from robust light-emitting diodes to power conversion in analog and RF. According to a Bloomberg press-release report published in August 2019, the global market for GaN devices is anticipated to reach $54,881.2 million by 2025 [3]. The PoL buck converter developed in this work uses enhancement-mode GaN devices from EPC (Efficient Power Corporation) to implement a high efficiency power stage.

A major challenge in designing a switching converter with GaN is understanding and quantifying design trade-offs. The form factor and power density requirements of a power converter drive the switching speed requirements, through which the designer can set the system parameters such as the converter topology, filter design, and control architecture. For high frequency (MHz) operation with GaN, switching losses dominate the converter's loss. A key contributor to switching losses is reverse conduction loss, which occurs in the converter's dead-time. Most industrial controllers offer a dead-time higher than 10ns and up to 40ns for PoL applications. In such cases, a well-known technique is used that introduces an anti-parallel Schottky diode across the synchronous FET for shared commutation and reduced dead-time losses.

This work presents and evaluates the performance of a PoL buck converter with and without a Schottky diode in parallel with the synchronous GaN FET. The converter operates in continuous conduction mode for load currents up to 6A. Furthermore, to evaluate the overall efficiency of the power converter before fabrication, the sources of power loss in the power converter are realized. To estimate the contribution of these sources of power loss, an analytical switching loss model is presented. In addition to the equivalent models of the major components like power FETs and filters, loss contributors such as parasitic passive elements and aiding active elements are also added to the proposed model. A buck converter is implemented to drive GaN at high switching frequencies (up to 2MHz) using components-off-the-shelf (COTS). The measured performance of this developed converter is used to verify the proposed model.

1.2 Thesis Objectives

The presented buck converter evaluates enhancement-mode GaN power devices for PoL applications, at switching frequencies of 400KHz and 2MHz. As the switching frequency rises, the parasitic impedances of the traces connecting GaN to other components on the printed circuit board (PCB) become comparable to the input and output capacitance of GaN, interfering with the switching transitions. A detailed analysis of the converter that includes the parasitic elements from PCB traces and equivalent models of the active elements is required to understand the switching performance of a buck converter using GaN power devices. The objectives of this work are as follows:

1. Detailed study of the switching operation of a DC-DC buck converter to understand the effect of the antiparallel Schottky diode on the power converter's performance.
2. Develop an analytical switching model that quantifies dead-time power loss to further predict performance during the converter's design phase. For this study, parasitic elements in the power stage of the designed board have been characterized and quantified for estimation of total power loss.
3. Characterization of industry diodes for performance evaluation of dead-time loss with high load currents (up to 6A). For this study, different Schottky diodes have been categorized by datasheet parameters and the converter performance is analyzed under a set of dead-time values for various output voltage ranges of the power converter.

1.3 Thesis Organization

Chapter 1 of this thesis motivates the need for the presented analytical model and analysis of GaN-based buck converters. Chapter 2 describes the background of a hard-switched buck converter with GaN and the prior work in GaN-based buck converters and GaN power device modeling. An analytical model is proposed in Chapter 3, along with the details of the equivalent circuit used to study piecewise operation of a buck converter. The various phases of converter operation, including switching transitions for the high side transistor and the low side transistor, are discussed with timing analysis in Chapter 3. In Chapter 4, the simulated and measured power loss of the converter are correlated with the calculated values for model verification. The details of the designed, fabricated, and measured COTS buck converter are given in Chapter 4. Additionally, categorization of high current Schottky diodes for shared commutation in a buck converter is presented for discrete converter applications. Finally, a performance summary is presented in Chapter 5, along with ideas for future improvements.

2. BACKGROUND AND PRIOR WORK

2.1 Buck Converter Operation

A DC-DC buck converter is a switching converter capable of reducing the DC voltage magnitude using non-dissipative switches, inductors and capacitors. The switch network comprises of the SPDT switch which changes its position periodically with a duty cycle, D, where 0≤D≤1. The SPDT switch will be later realized by active semiconductor devices. Due to the harmonics derived from the switching, there is a need for an output low pass filter with corner frequency (f_c) that is relatively smaller than the switching frequency (f_{sw}). The value of f_c can be calculated from equation (2.1).

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

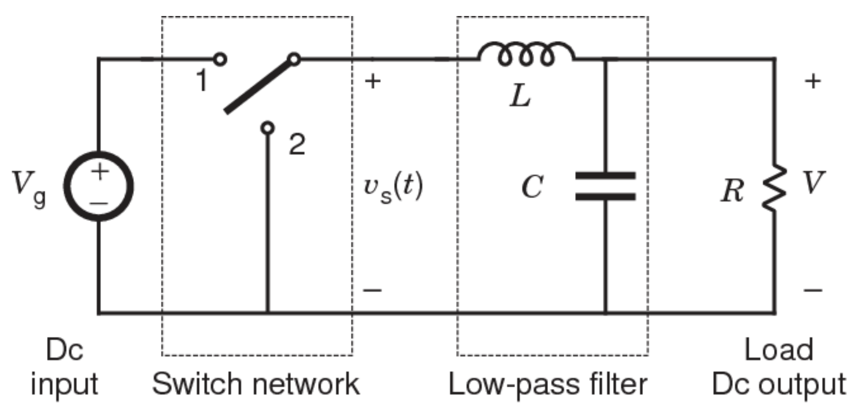

Figure 4. Ideal Circuit Of A Buck Converter [4]

As the switching and filter elements are not ideal, there will always be some power loss, which will degrade the efficiency (η) that is defined by equation (2.2). Total Power loss is defined by equation (2.3) and generalized by equation (2.4) where the first and second term denote conduction loss in FET channel and filter elements, respectively. The third and fourth term denote switching losses and dead-time losses respectively.

$$\eta = \frac{Input\ Power - Total\ Power\ loss}{Input\ Power} \tag{2.2}$$

$$Total\ Power\ Loss = Conduction\ loss + Switching\ Loss + Deadtime\ Loss \tag{2.3}$$

$$\begin{aligned} Total\ Power\ Loss &= \left\{ R_{DS(on)}.I_L^2 \right\} + \left\{ \left(R_{DS(on)} + R_{ESRL} + R_{ESRC} \right). \frac{\Delta I^2}{2} \right\} \\ &+ \left\{ \left(t_{RISE} + t_{FALL} \right). \frac{V_{IN}.I_L}{2}.f_{sw} \right\} \\ &+ \left\{ 2.V_{deadtime}.I_L.T_{deadtime}.f_{sw} \right\} \end{aligned} \tag{2.4}$$

2.2 Prior Work in GaN PoL Converters

In recent years, point of load (PoL) converters have been popular in computer processors, data centers, mobile phones and automobile power distribution. All applications employing PoL converters demand very high load current with accurate low-voltage requirements. These converters must achieve stringent voltage/current requirements without increasing the footprint of the additional filters. One such example is the FPGA I/O and Digital Signal Processor (DSP) core that operates at 3.3V with up to 1A load current, deriving power from a 48V bus. A popular approach of reducing power loss while distributing power to different circuits in a multiprocessor system is to improve efficiency by cascading multiple step-down stages with low voltage conversion ratios. This means stepping down from 48V range to 12V range and finally down to regulated 1V to 5V voltage range. Voltage conversion from 48V to 1V has been achieved using GaN switches in cascaded power conversion stages, from 48V to 12V and 12V to 1V with a fast loop response and to attain a small converter size [5].

Efforts have been taken to design fast switching PoL converters for devices that demand high load current without compromising on efficiency by using GaN in multi-phase control architectures [6, 7]. With this architecture, higher current requirements are fulfilled with more than one buck converter using interleaved phases to reduce the load current ripple. This architecture is represented in Figure 5 for a converter employing two phases that had specific requirements for high particle instrumentation.

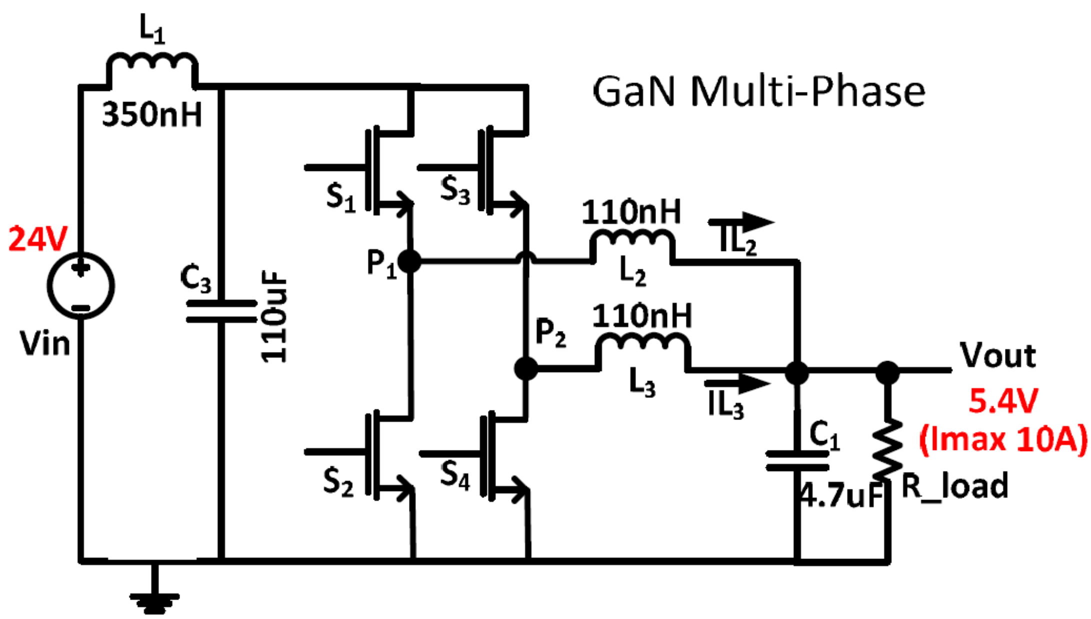

Figure 5. Schematic Diagram Of A Two-Phase GaN Based Buck Converter [6]

Another approach has been used to improve efficiency by integrating GaN power devices with the driver [8] and minimizing losses due to packaging parasitics in the gate loop. The block diagram for this integrated circuit is shown in Figure 6.

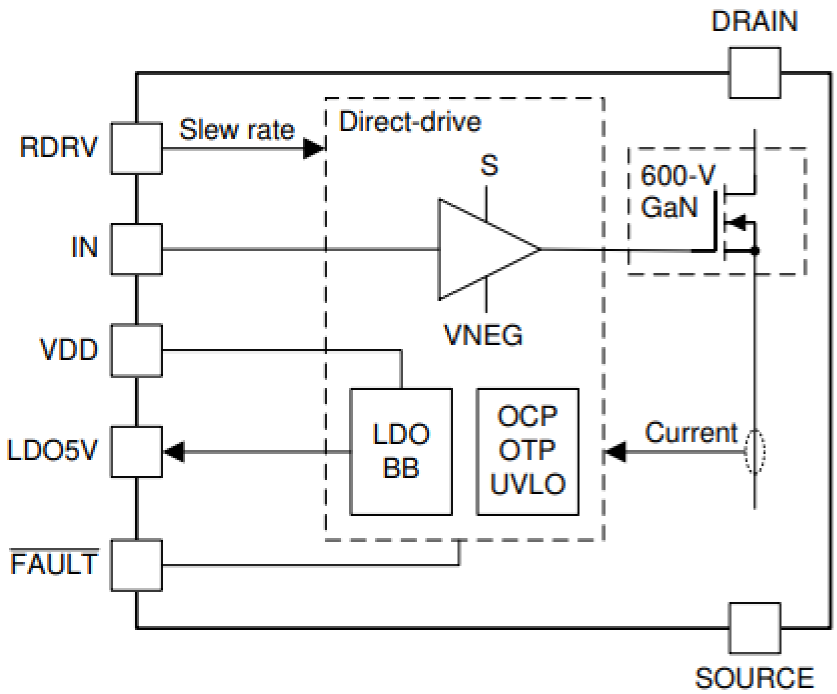

Figure 6. Block Diagram Of The Integrated Driver With GaN FET In LMG3411 [8]

Recent work in power conversion is progressing towards a voltage conversion from 12V to less than 1V using GaN devices for PoL converters. In such cases, it becomes mandatory to optimize performance and enhance power handling capability. Regardless of the converter control architecture used, a detailed analysis of the power converter is required, which can help to understand the operation of the converter to trade-off design parameters and optimize the converter's performance.

2.3 Reverse Conduction Loss in GaN Power Switches

Unlike MOSFETs, GaN HEMTs do not suffer from reverse recovery loss. A phenomenon termed "reverse conduction loss" occurs during the dead-time period, when the Low side FET conducts current through its conducting channel, but in the reverse direction. This happens mainly due to the symmetrical structure of GaN FETs. Unlike MOSFETs, GaN HEMTs do not have a body diode. In MOSFETs, the body diode will create a voltage drop of around 700mV across the low side FET. For GaN, this voltage drop can be as high as 1.8V-2.5V. This reverse conduction loss contributes to the GaN devices' switching losses.

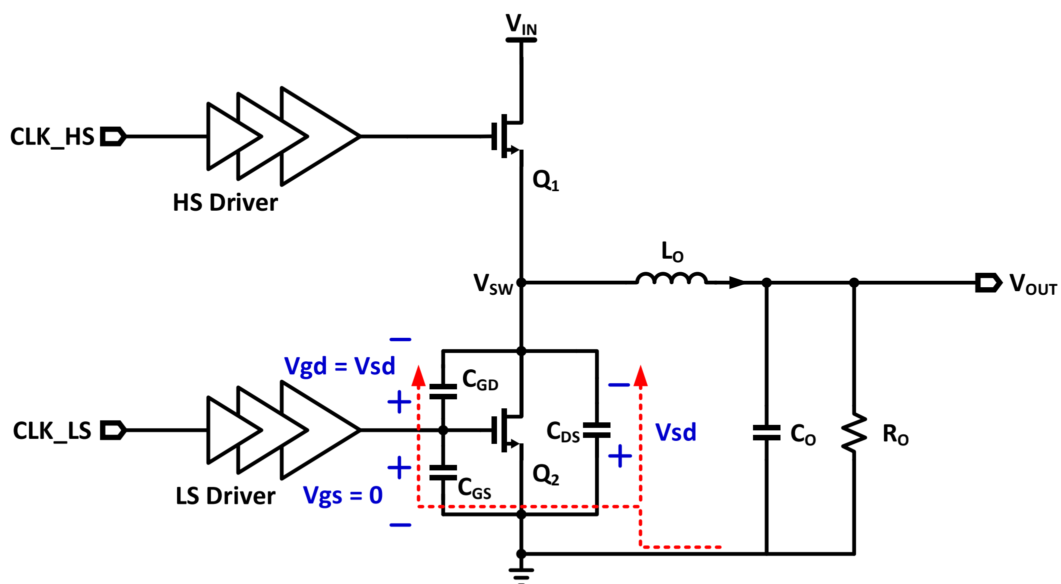

Figure 7. Buck Converter: Reverse Conduction Loss Explained

A buck converter is shown in Figure 7 that illustrates the reverse conduction process with GaN. To avoid shoot through current between the two power switches, a small blanking period is applied between the conducting phases of each power device. This period is called dead-time. During the dead-time, after the high side (HS) GaN is turned off, the gate and source terminals of the low side (LS) GaN are practically shorted to ground and drain to source voltage can be given by equation ((2.5). The inductor current freewheels through the LS FET, charging the parasitic source-to-drain and gate-to-drain capacitances, C_{SD} and C_{GD}. With V_{gs} practically shorted, GaN can conduct current in the reverse direction, if the gate-to-drain voltage is high enough to turn the device on in the reverse direction, as described in equation ((2.6) .When V_{gd} approaches the threshold voltage for conducting reverse current (Vgdth), this charging of parasitic capacitors can cause a false turn on of the LS FET and a voltage drop of about V_{gdth} is observed across the source and drain terminals, as described by equation ((2.7).

$$V_{sd} = V_{sg} + V_{gs} \tag{2.5}$$

When the low side FET is off, $V_{sd} = V_{gs}$ (2.6)

$$V_{sd} = V_{gdth} \ \ (\sim 1.8\text{V}) \tag{2.7}$$

Since, this operation does not involve minority charge carrier transport, there is no reverse recovery loss associated with this phenomenon. This phenomenon can be related to the body diode of a MOSFET without reverse recovery loss, and with a forward voltage drop over three times larger than MOSFET.

Different gate drive techniques have been proposed in the past to minimize loss due to reverse conduction, including dead-time optimization and power stage architectures using an anti-parallel diode configuration. A new driving technique was proposed in [9] to optimize dead-time while limiting the frequency range by introducing an intermediate drive level within the gate drive transition period. Furthermore, techniques like adaptive dead-time control for buck converters and zero-voltage switching (ZVS) have been used to optimize dead-time [10], but these techniques cannot be applied to high frequency discrete PoL power converters due to limitations from package and PCB trace parasitic elements.

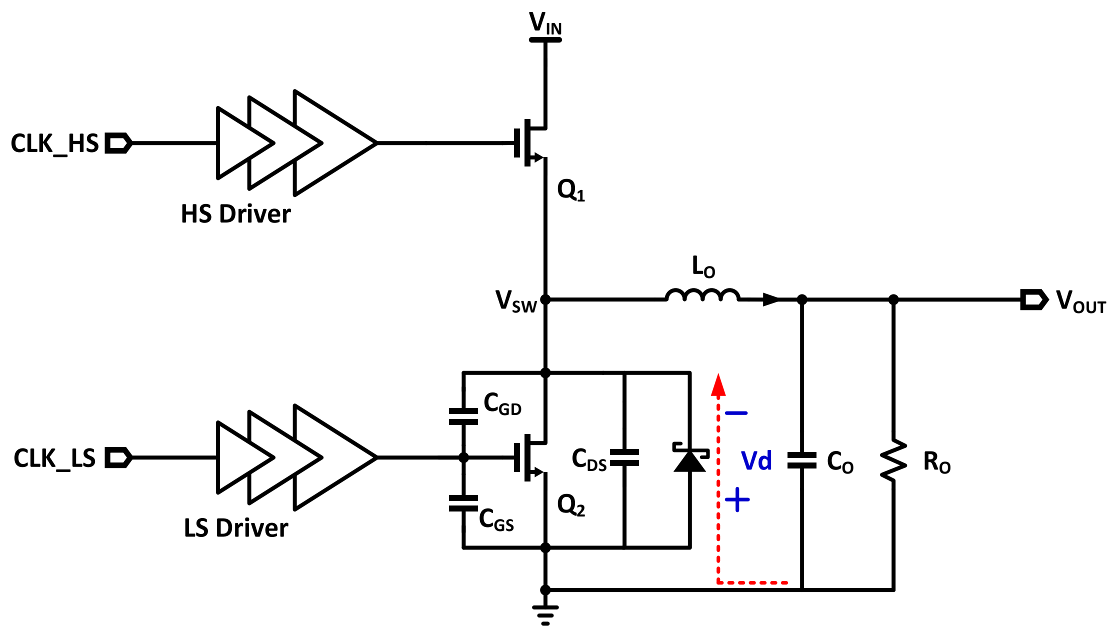

Figure 8. Addition Of Anti-Parallel Schottky Diode

A well-known and reliable method to reduce reverse conduction losses without adding complicated drive techniques is to add an anti-parallel Schottky diode with the synchronous FET [11]. As shown in Figure 8, the inductor current is commutated through the diode during dead-time. This sets the source to drain voltage of the LS FET to approximately the forward drop of the Schottky diode, as given in equation ((2.8), which ranges from 100mV to 600mV based on the instantaneous forward current through the diode. This forward drop is much smaller than the reverse conduction voltage of the GaN device, which can range anywhere from 1.7V to 2.5V [12].

$$V_{sd} = V_d < V_{gdth} \tag{2.8}$$

Most discrete power converters with GaN use industry controllers that provide dead-time from 10ns up to 40ns based on the controller's switching frequency range. In such cases of non-optimized dead-times, it becomes important to study the effect on functionality of the converter with the Schottky diode, in addition to analyzing sources of power loss during the dead-time and their contribution to the total power loss of the converter. This performance can be evaluated using the developed and presented analytical power loss models.

2.4 Prior Work in Modeling of GaN-Based Power Converters

Analytical models are very crucial in determining the performance and loss of any power converter circuit. As power converter operation moves towards higher switching frequencies, the parasitic elements of the traces connecting the devices together start interfering in the regular operation. Different switching models have been presented in the past to analyze losses in a buck converter. These papers use piecewise linear models to predict switching losses. Different techniques have been applied to predict switching power losses. One technique is to obtain equations with loop parameters (like voltages and currents in each loop) as variables in one clock cycle and calculate using iterative methods such as FEMs, to replicate the waveform for easy calculation of conduction and switching losses. Another technique used to calculate power loss is to estimate the time taken for switching transitions using piecewise linear approximations and evaluating power loss based on time taken during different current and voltage transitions during one switching cycle.

A practical switching loss model is presented for buck converters using power MOSFETs [13] by means of detailed analytical analysis. These models cannot be used to analyze the switching losses in GaN because GaN devices have a different third quadrant current voltage operation than MOSFETs, in which GaN FETs conduct similar to a MOSFET’s body diode, but with a much higher forward drop in the range of 1.7V to 2.5V compared to MOSFETs that have 700-800mV forward drop. More importantly, unlike MOSFETs, GaN devices do not have reverse recovery loss because of the absence of minority carriers. Therefore, there is a need for a device model that addresses GaN performance for GaN based buck converters.

A simple analytical model for low voltage eGaN HEMTs was first developed in [14], as shown in Figure 9. The analysis includes switching transitions of the HS FET only.

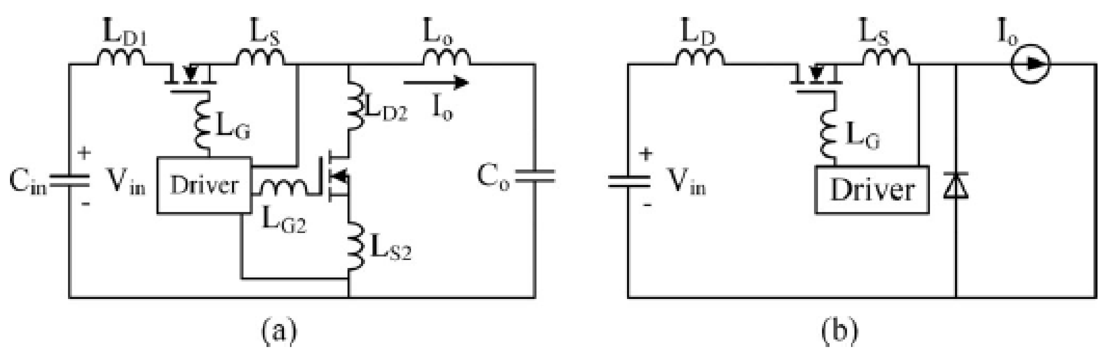

Figure 9. (a) Synchronous Buck Converter (b) Simplified Equivalent Circuit With High Side Performance Evaluation Only [14]

Later, a modified analytical switching model was developed [15], which cannot be used for this study because it excludes dead-time analysis. The equivalent circuit for this model is shown in Figure 11, and the switching waveforms for the turn off transition of HS FET are shown in Figure 10. The dead-time is not clearly defined in this model. This analysis is done by estimating the transition time when switching the power FETs on/off.

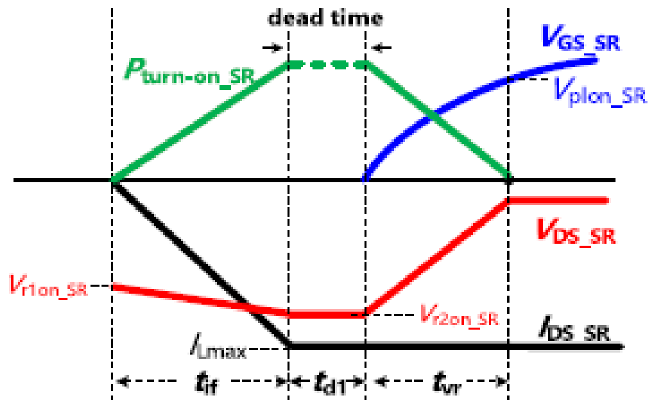

Figure 10. Turn Off Transition Of HS FET In 3 Phases [15]

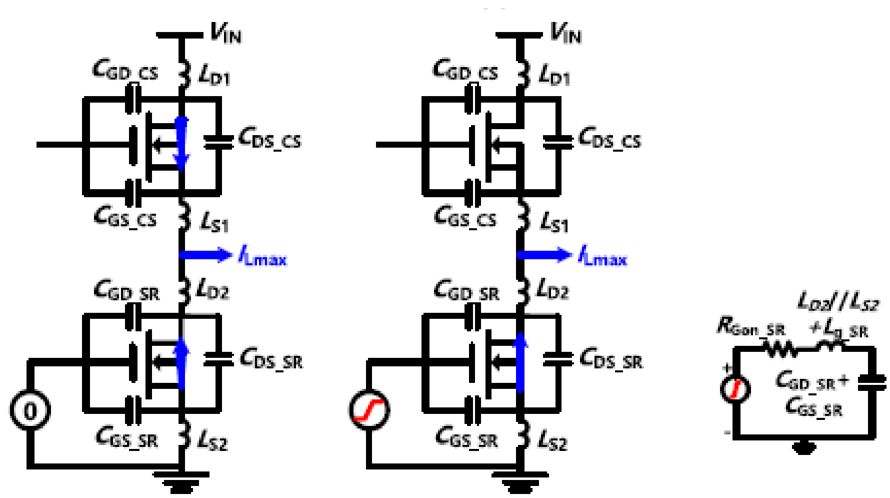

Figure 11. Equivalent Circuit Diagram For HS FET Turn-Off Phase [15]

A complete switching model for low voltage eGaN is developed in [16], which quantifies the switching performance of the synchronous GaN FET along with a very simplified power loss analysis for the reverse conduction loss. The equivalent circuit for this model is shown in Figure 12, and the switching waveforms for the turn off transition of HS FET are shown in Figure 13. In this model, loss analysis is done using iterative methods. But this model does not detail dead-time loss and does not include an expression to calculate the effective dead-time. The effective dead-time seen at the switch node is set by the power loop parasitics and load current, which is explained in later sections.

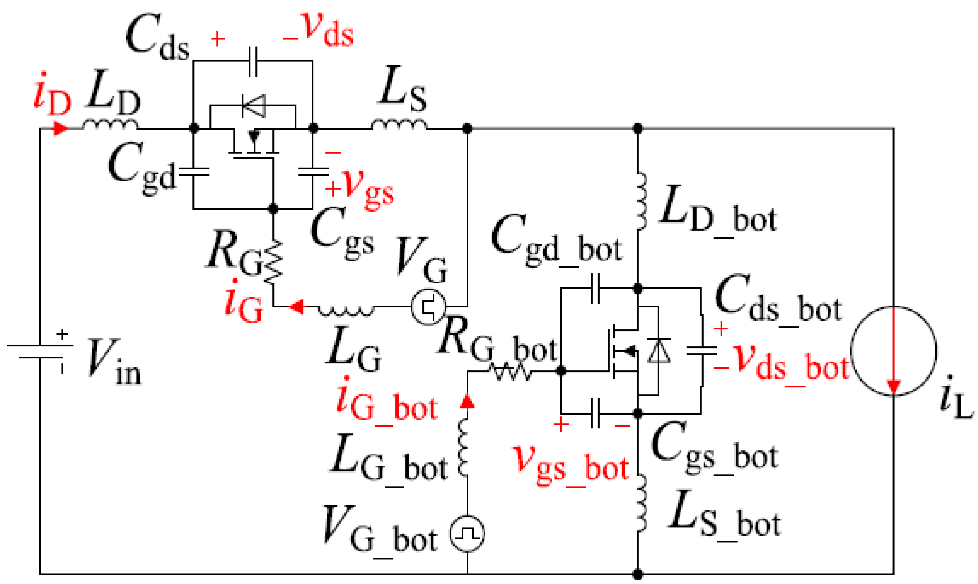

Figure 12. Equivalent Circuit Diagram [16]

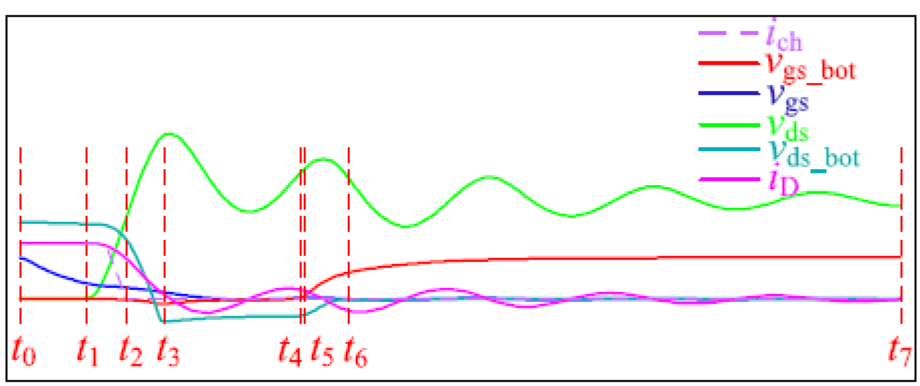

Figure 13. Transition Diagram For Turn-Off Of HS FET [16]

For higher switching frequencies and varying load currents, it is important to analyze the parasitic elements in the traces and packaging of components because they are comparable to the parasitic elements introduced by the board layout and packaging and the diode of the power converter. Their presence modifies the dynamics of the power converter operation and the power loss. The presented model expands upon the previously derived analytical models, but with the addition of an anti-parallel Schottky diode for the synchronous GaN FET added to achieve lower reverse conduction loss. Additionally, the presented model includes parasitic elements and accounts for loss during dead-time.

3. ANALYTICAL MODEL OVERVIEW

In this work, we build upon the previous piecewise linear analytical models [14-16] to understand the effect of the antiparallel Schottky diode on the whole power converter. In the proposed model, we calculate the transition time by using a piecewise approach for every transition in the gate and power loop. These calculated transition periods are later compared to simulations and measured results.

3.1 Analytical Model's Equivalent Circuit

The equivalent circuit modelled to derive power loss equations includes the equivalent parasitic model of e-GaN FET and the anti-parallel Schottky diode (marked in red) in Figure 14.

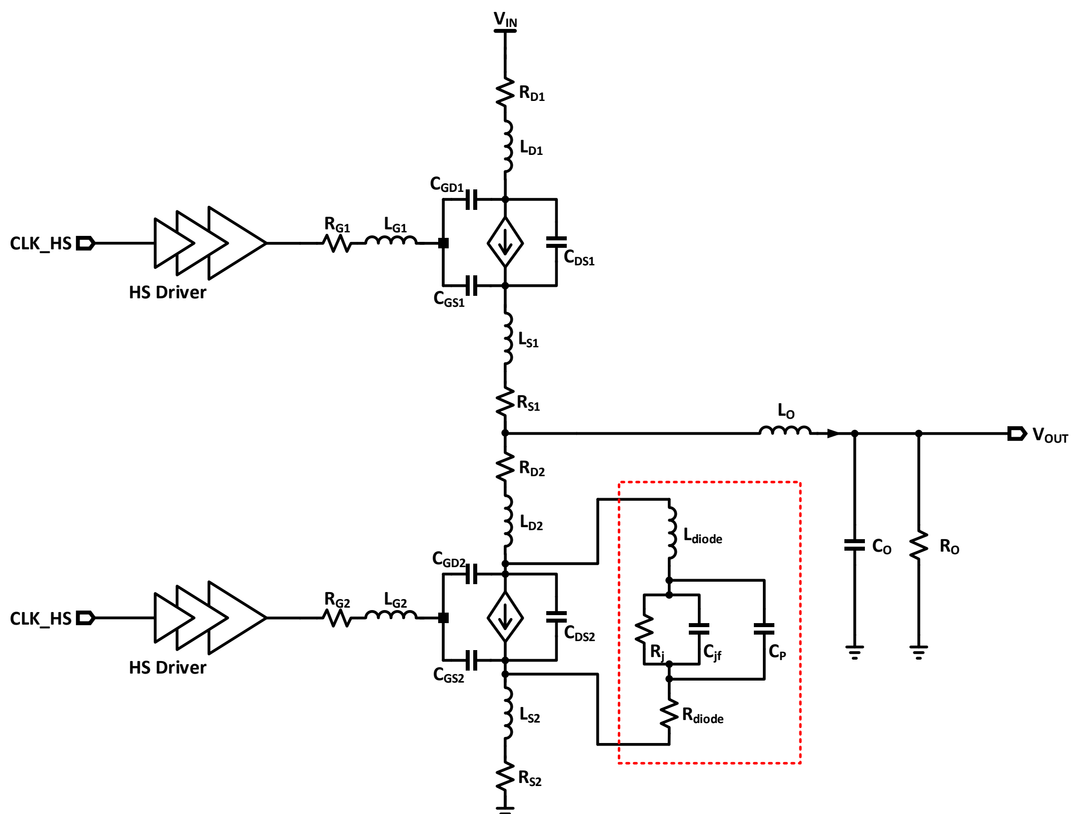

Figure 14. Equivalent Circuit Diagram Of The Proposed Model

E-GaN model for medium voltage devices

The equivalent model in Figure 14 includes all parasitic components associated with an enhancement mode GaN FET EPC2014C.

Parasitic Parameter	Abbreviation	Datasheet Value
Input Capacitance @ VDS=20V	C_{iss}	300pF
Output Capacitance @ VDS=20V	C_{oss}	210pF
Reverse Transfer Capacitance @ VDS=20V	C_{rss}	9.5pF
Gate Resistance	R_{gate}	400mΩ
Gate threshold voltage	$V_{GS(th)}$	1.4V (typ)
Source-drain voltage @500mA and VGS=0	V_{gdth}	1.8V

Table 1. GaN Device Parameters

The resistance in the gate loop, R_G, which includes PCB trace and driver output resistance, is included in the model because this contributes to the time taken to charge/discharge the gate capacitance. Series resistances in the source and drain path of GaN are defined as R_S and R_D, respectively. For a power stage designed using optimum layout techniques [17], R_S and R_D are much smaller than R_G. The gate-to-source capacitance, drain-to-source capacitance and gate-to-drain capacitance of the GaN FET are given by C_{GS}, C_{DS} and C_{GD}, respectively. In addition to determining charging/discharging time, they significantly contribute to switching losses. Stray inductance in the gate loop, drain path and source path are given by L_G, L_D, and L_S, respectively. Inductance in gate loop due to L_G and L_S limits the slew rate of the gate drive current, and L_D contributes to the ringing at switch node during switching transitions. Input capacitance is given by C_{iss}, which is the sum of C_{GS} and C_{GD}, and Output capacitance is given by C_{oss}, which is the sum of C_{DS} and C_{GD} [12]. Current through channel is shown modeled by a voltage controlled current source and is denoted by i_{ch}. Parameters with subscripts 1 and 2 represent the HS and LS FET, respectively.

Schottky diode model

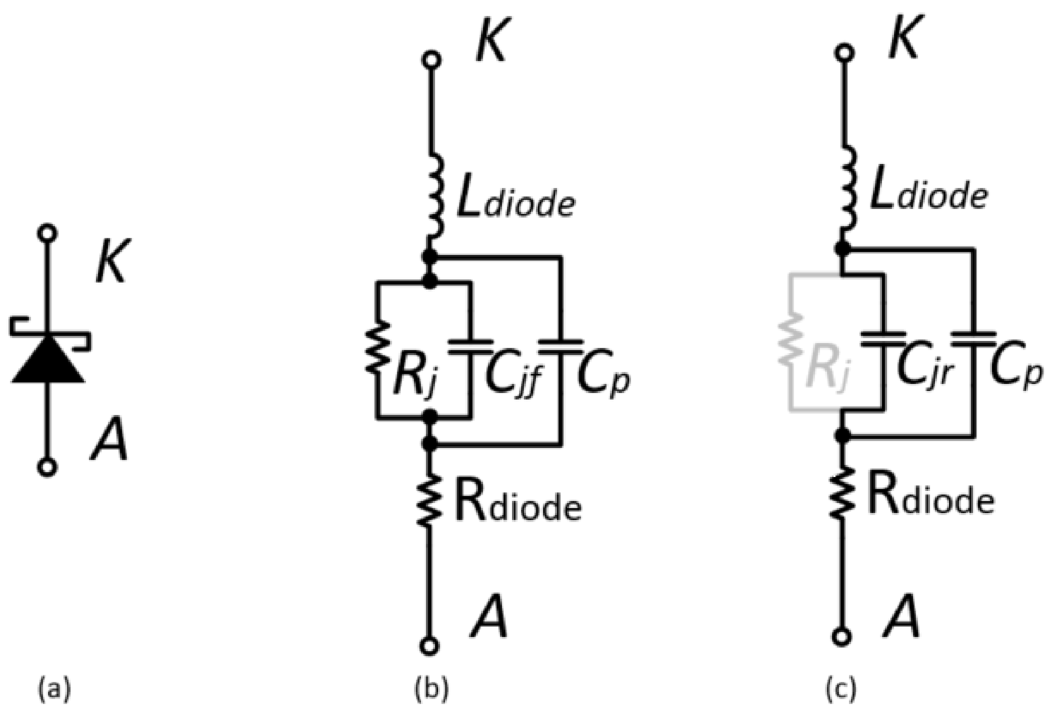

Figure 15 . Schottky Diode (a) Symbol (b) Equivalent Circuit In Forward Bias (c) Equivalent Circuit In Reverse Bias

The equivalent circuit for the Schottky diode is shown in Figure 15. For a forward biased diode, this model can be represented by a junction capacitance, C_{jf}, in parallel with junction resistance, R_j, and both in series with package and PCB trace inductance, L_{diode}. Any resistance in trace path from diode to GaN is denoted by R_{diode}. R_j can be calculated from the datasheet based on the instantaneous forward voltage and load current. Most manufacturers use n-type Si for Schottky diodes where the

C_{jf} is dependent on the voltage applied across the diode [18]. This capacitance is negligible for a Schottky diode in forward bias in comparison with C_{oss} of GaN. In addition, reverse recovery time for Schottky diodes is very close to zero due to the absence of minority carriers. Furthermore, the oxide passivation creates a capacitance defined as (C_o) overlay capacitance and the package capacitance ($C_{package}$). These values are set by the material and packaging used by the manufacturer and can be found in datasheets. For simplicity of the analysis, this model refers to total capacitance from the datasheet [19] and includes it in C_p.

For a reverse biased diode, R_j is very high and is not included in the model. The junction capacitance during reverse bias is denoted by C_{jr}. The sum of C_{jr} and C_p is defined in datasheets as C_{diode}, C_{total}, or $C_{junction}$, and can be derived from the total capacitance versus reverse voltage characteristic curve in the datasheet.

Parasitic Parameter	**Abbreviation**	**Datasheet Value**
Forward Voltage	V_F	0.42V typical @ 1A
Forward current	I_A	1A
Reverse blocking voltage	V_R	30V
Reverse Capacitance	C_P	1000pF at 0V

Table 2. Schottky Diode Parameters [19]

The buck converter's switching analysis is separated into 7 phases by time for the HS turn on and LS turn on that will be elaborated in this section.

3.2 Switching Analysis for High Side Turn On

Seven phases of transition are investigated from LS GaN turn off to a complete HS GaN turn-on. We observe the behavior of V_{DS} (drain to source voltage), I_{DS} (drain to source current), V_{GS} (gate to source voltage) and i_{ch} (channel current) of both HS and LS FET along with the diode commutation current shown as i_{diode}. The piecewise approximated waveforms for this transition are given in Figure 16. Any assumptions made are specified in the respective transitions.

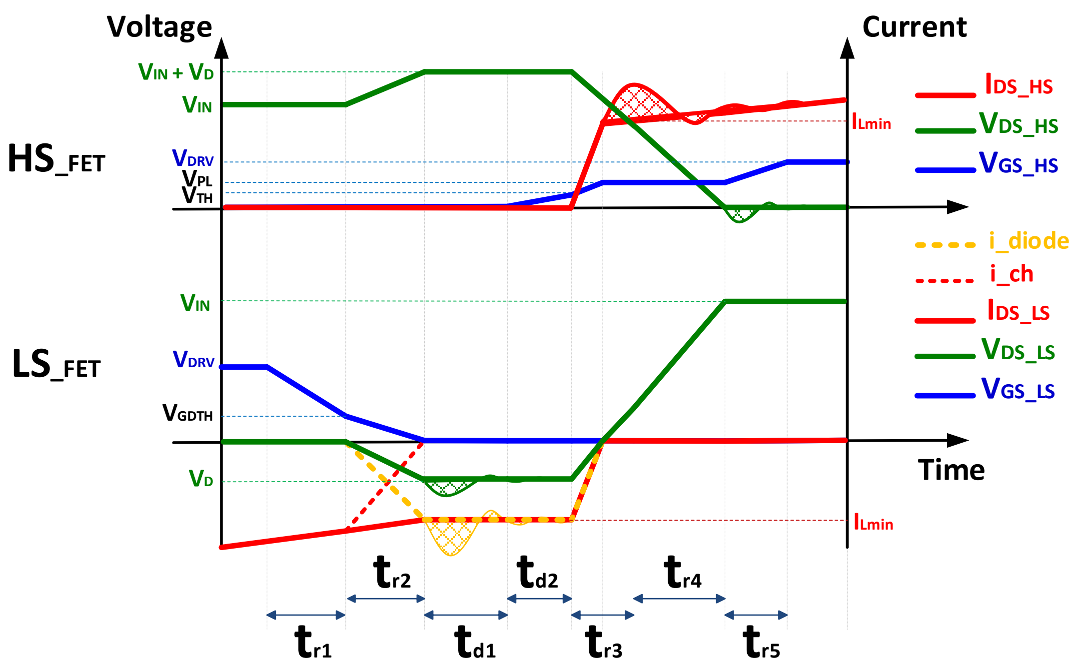

Figure 16. Transition Diagrams For Switching Analysis For High Side Turn On

A. Stage 1(tr1: LS driver turn-off initiated)

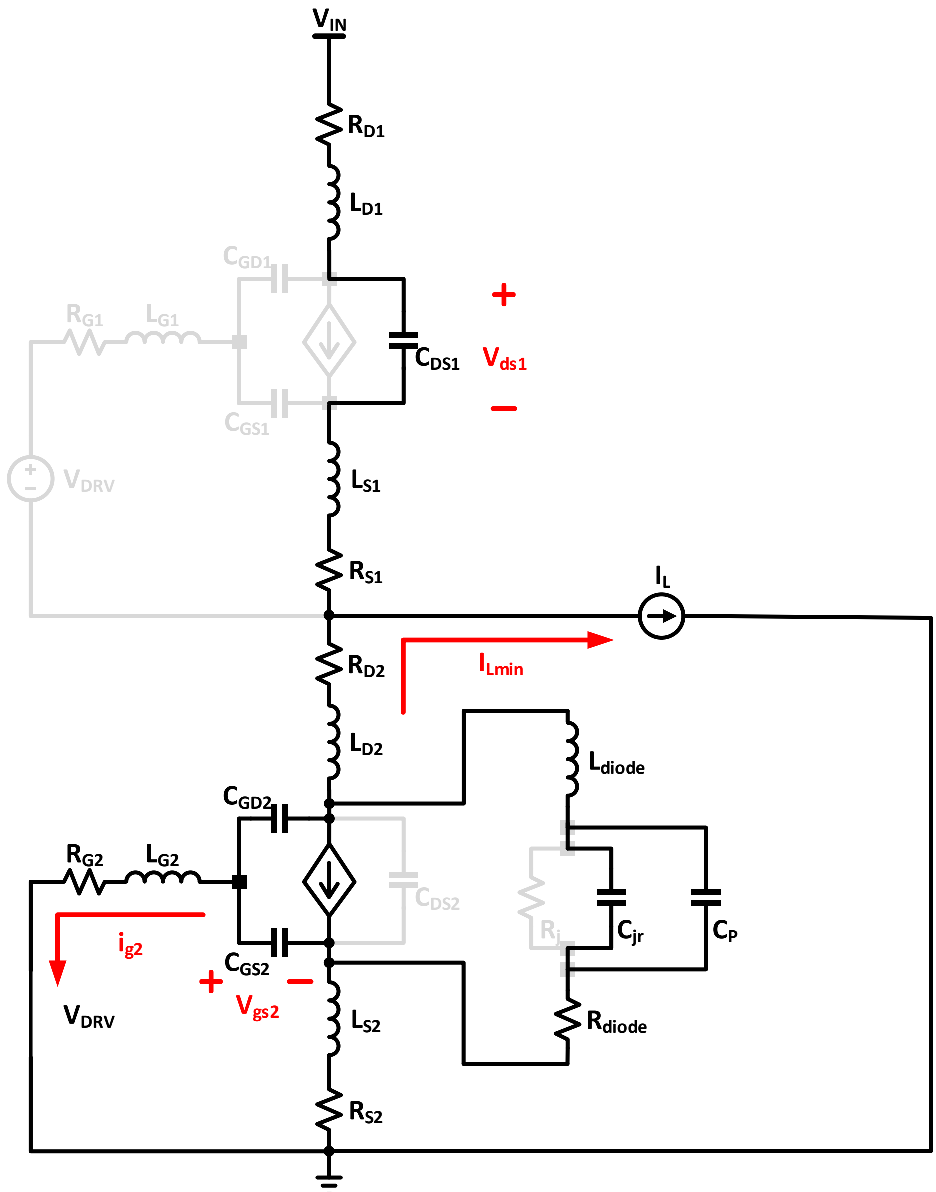

Figure 17. tr1: LS Driver Turn-Off Initiated

The equivalent circuit during this phase is shown in Figure 17. At the beginning of this period, the LS driver pulls down the gate of the LS FET and input capacitor of LS FET starts discharging with V_{DS2} being very close to zero. For simplicity of the calculations, we assume that this period does not contribute to switching loss. The period t_{r1} is dominated by the input capacitance C_{iss} and discharge current of the driver, i_{g2}, which can be extracted from datasheet. If discharge current is not mentioned, this can be approximated from the fall transition characteristics of LS driver in the datasheet.

The gate drive current can be approximated for initial and final conditions during this period by I_{g1} and I_{g2} respectively, as given in equation (3.1) and equation (3.2).

$$I_{g1} = \frac{V_{DRV}}{R_{G2} + R_{S2}} \tag{3.1}$$

$$I_{g2} = \frac{V_{gdth}}{R_{G2} + R_{S2}} \tag{3.2}$$

Thus, the average gate current, $I_{g(avg)1}$ during this period is calculated from equation(3.1) and equation(3.2), and given by equation(3.3), where V_{DRV} is the driver supply voltage and V_{gdth} is the drain-source threshold voltage as given in Table 1.

$$I_{g(avg)1} = \frac{V_{DRV} + V_{gdth}}{2(R_{G2} + R_{S2})} \tag{3.3}$$

A first order approximation can be made for the input capacitor charging as given in equation (3.4).

$$t_{r1(apprx)} = \frac{(C_{GS2}+C_{GD2}).(V_{DRV} - V_{gdth})}{I_{g(avg)1}} = \frac{2(R_{G2} + R_{S2}).(C_{GS2}+C_{GD2}).(V_{DRV} - V_{gdth})}{(V_{DRV} + V_{gdth})} \tag{3.4}$$

A correction factor is made in equation (3.5) by adding the effect of the inductor on the gate current. The final value of this period is calculated in equation (3.6).

$$\Delta t_{r1} = \frac{(C_{GS2}+C_{GD2})}{I_{g(avg)1}} \cdot \frac{(L_{G2}+L_{S2}).(V_{DRV}-V_{gdth})}{(R_{G2}+R_{S2}).t_{r1(approx)}} \tag{3.5}$$

$$t_{r1} = t_{r1(approx)} + \Delta t_{r1} \tag{3.6}$$

This period ends when V_{GS2} reaches V_{gdth}.

B. Stage 2(tr2: LS turn off delay, VDS2: 0 to -V_D)

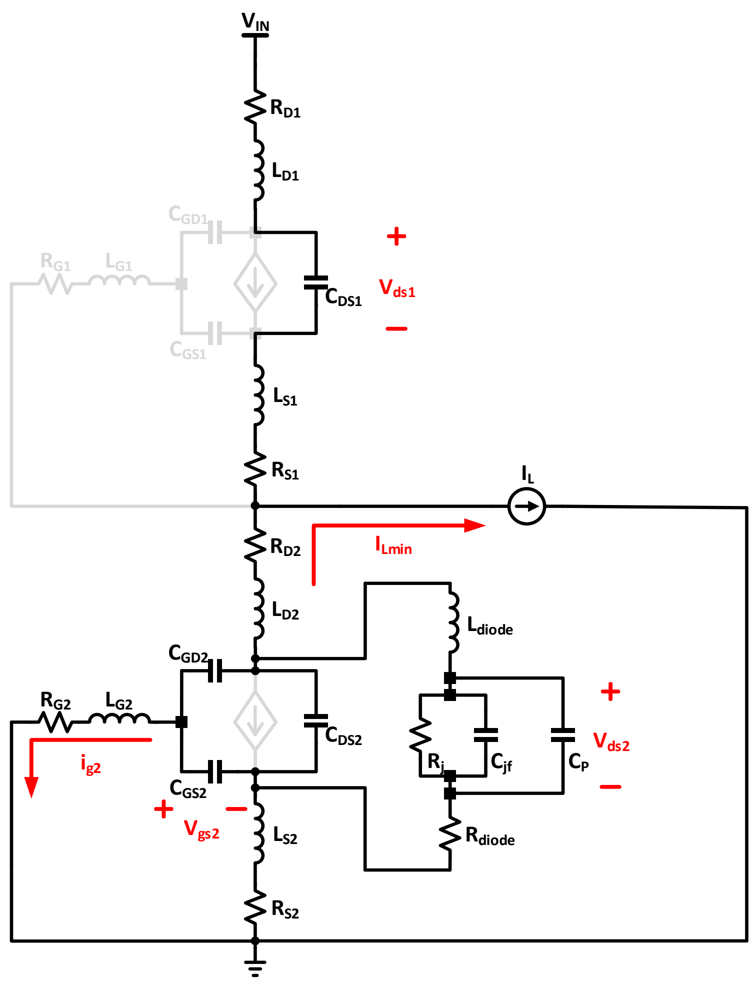

Figure 18. tr2: LS Turn Off Delay, VDS2: 0 To -V_d

The equivalent circuit during this phase is shown in Figure 18. Holding the assumption made in the previous stage that V_{DS2}=0, we begin analysis of the transition of V_{DS2} from 0 to -V_D, where V_D is the forward drop voltage of the Schottky diode as given in Table 2. At the beginning of this transition, V_{GS} starts dropping below V_{gdth} and a part of the inductor current starts charging the output capacitor of LS, i.e. C_{SD2}, C_P and C_{jf}. This period ends when V_{DS2} reaches -V_D and current starts commuting through the diode. This period can be approximated from [15] and is given by equation (3.7).

$$t_{r2} = 2.\pi.\sqrt{(L_{D2} + L_{S2} + L_{diode}).(C_{DS2} + C_P + C_{jf})} \tag{3.7}$$

Ideally, a saturation current rating matching the maximum value of inductor current is chosen for a Schottky diode. The trace between Schottky diode and LS FET impacts the performance during this transition.

C. Stage 3(td1: dead-time after LS turn off)

The equivalent circuit during this phase is shown in Figure 19. In the absence of a Schottky diode, when LS turns off, all the load current would commutate through reverse conduction of the LS switch and the voltage drop across LS would reach about the threshold voltage from gate to drain, which is found in the datasheets and usually ranging from 1.7V to 2.5V. This could increase the dead-time loss with improper management of the dead-time period. In the presence of a Schottky diode, the inductor current is commutated entirely through the diode. The value of t_{d1} set in this case can be calculated by equation (3.8) as a byproduct of phases t_{r1} and t_{r2} and dead-time ($t_{dead\text{-}time}$) externally set by the controller.

$$t_{d1} = t_{dead-time} - (\, t_{r1} + t_{r2}) \tag{3.8}$$

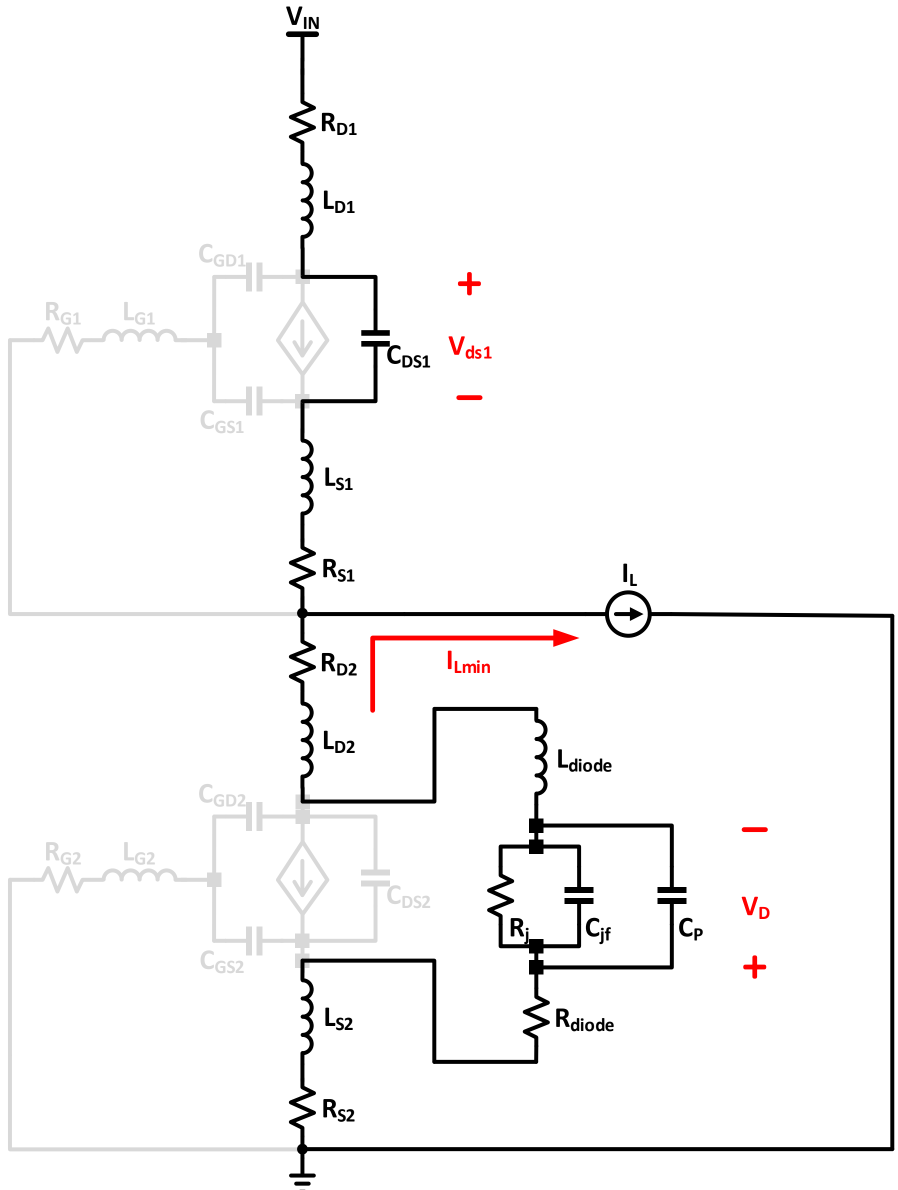

Figure 19. td1: Dead-time After LS Turn Off

D. Stage 4(td2: HS turn on delay, V_{GS1}: 0 to V_{th})

At the beginning of this period, HS gate is pulled up and input capacitor of HS FET starts charging. V_{GS1} is at zero initially and reaches V_{th} at the end of this period. The inductor current is still commuting through the Schottky diode.

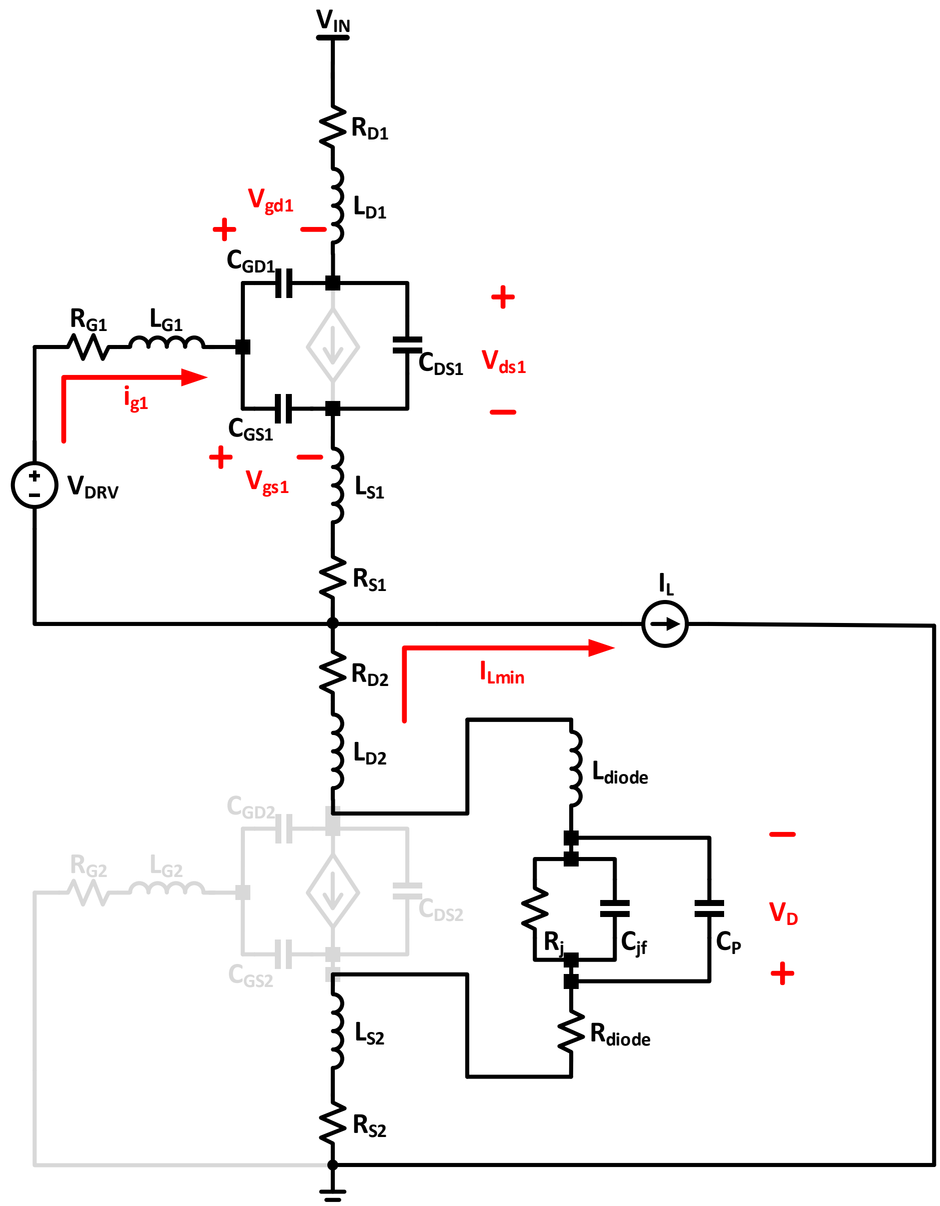

Figure 20. td2: HS Turn On Delay, V_{GS1}: 0 To V_{th}

The time taken t_{d2} can be calculated from equation (3.9), where i_{gdr1} is the sink current of the gate driver which can be modeled by equation (3.10). The equivalent circuit during this phase is shown in Figure 20 .

$$t_{d2} = \frac{(C_{GS1} + C_{GS2}).V_{th}}{i_{gdr1}} \tag{3.9}$$

$$i_{gdr}1 = \frac{Rated\ gate\ capacitance\ .\Delta V_{GS}}{\Delta t(condition)} \tag{3.10}$$

E. Stage 5(tr3: HS turn on state, V_{GS1}: V_{th} to V_{pl})

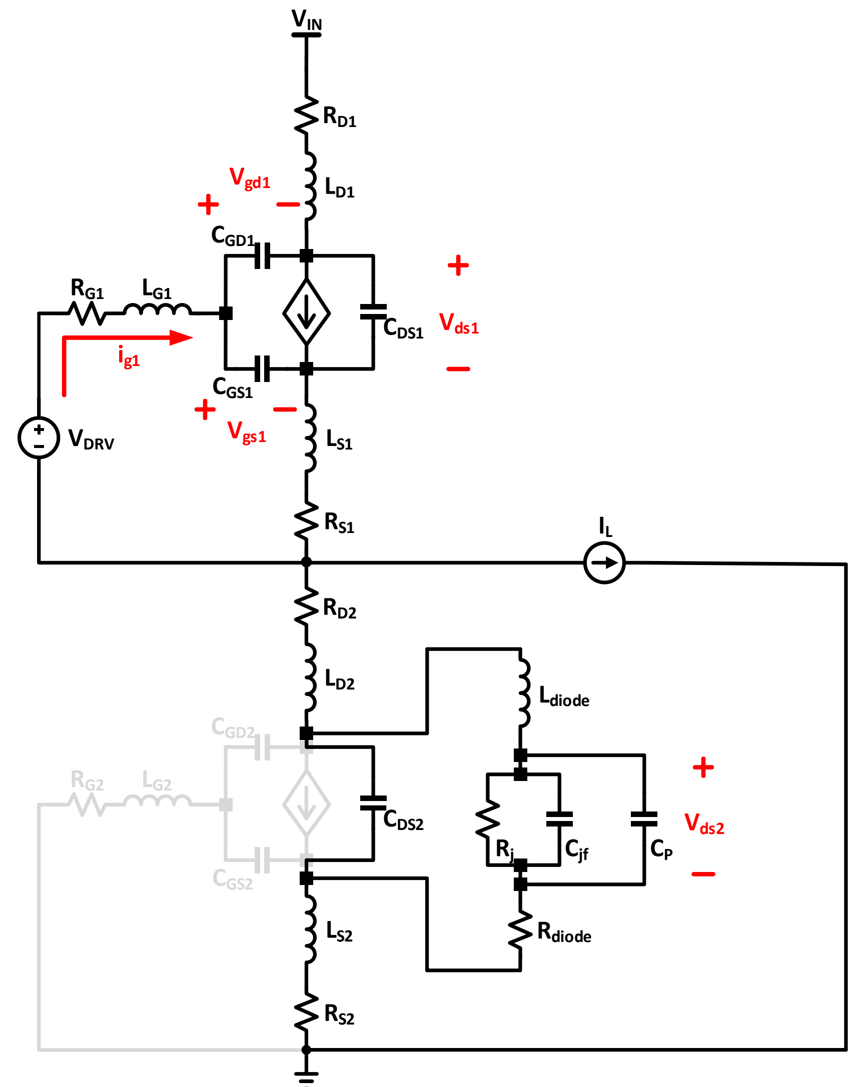

Figure 21.tr3: HS Turn On State, V_{GS1}: V_{th} To V_{pl}

The equivalent circuit during this phase is shown in Figure 21. During this period, the HS channel current begins to rise and input capacitor of HS charges from V_{th} to V_{pl}. For the simplicity of calculation, all transitions are assumed linear. This transition period can be calculated from equation (3.11),

$$t_{r3} = \frac{(C_{GS1} + C_{GD1}).(V_{PL} - V_{th})}{i_{gdr1}} \tag{3.11}$$

where the plateau voltage V_{PL} is derived and expressed in equation (3.12). The forward trans-conductance of the GaN FET is given by g_{fs} and the inductor current during this transition is $I_{Lmin,}$ which is calculated from the inductor ripple.

$$V_{PL} = V_{th} + \frac{I_{Lmin}}{g_{fs}} \tag{3.12}$$

F. Stage 6(tr4: Plateau period of HS gate)

As i_{g1} increases, V_{GS1} remains constant due to drop across the common source inductance. This is the 'Plateau period'. It ends with V_{DS1}=0. The equivalent circuit during this phase is shown in Figure 22.

Unlike MOSFETs, eGaN FETs do not have a p-n junction body diode and the HS FET is not effected by lagging reverse recovery current from the LS FET during high side turn-on. This effect is rooted from the minority carrier movement into the depletion region of the p-n junction body diode of the LS FET. The period can be approximated from [15] and given by equation (3.13).

$$t_{r4} = \frac{1}{2f_{loop}} = \pi.\sqrt{(L_{D1} + L_{S1} + L_{D2} + L_{S2}).(C_{DS2} + C_P)} \tag{3.13}$$

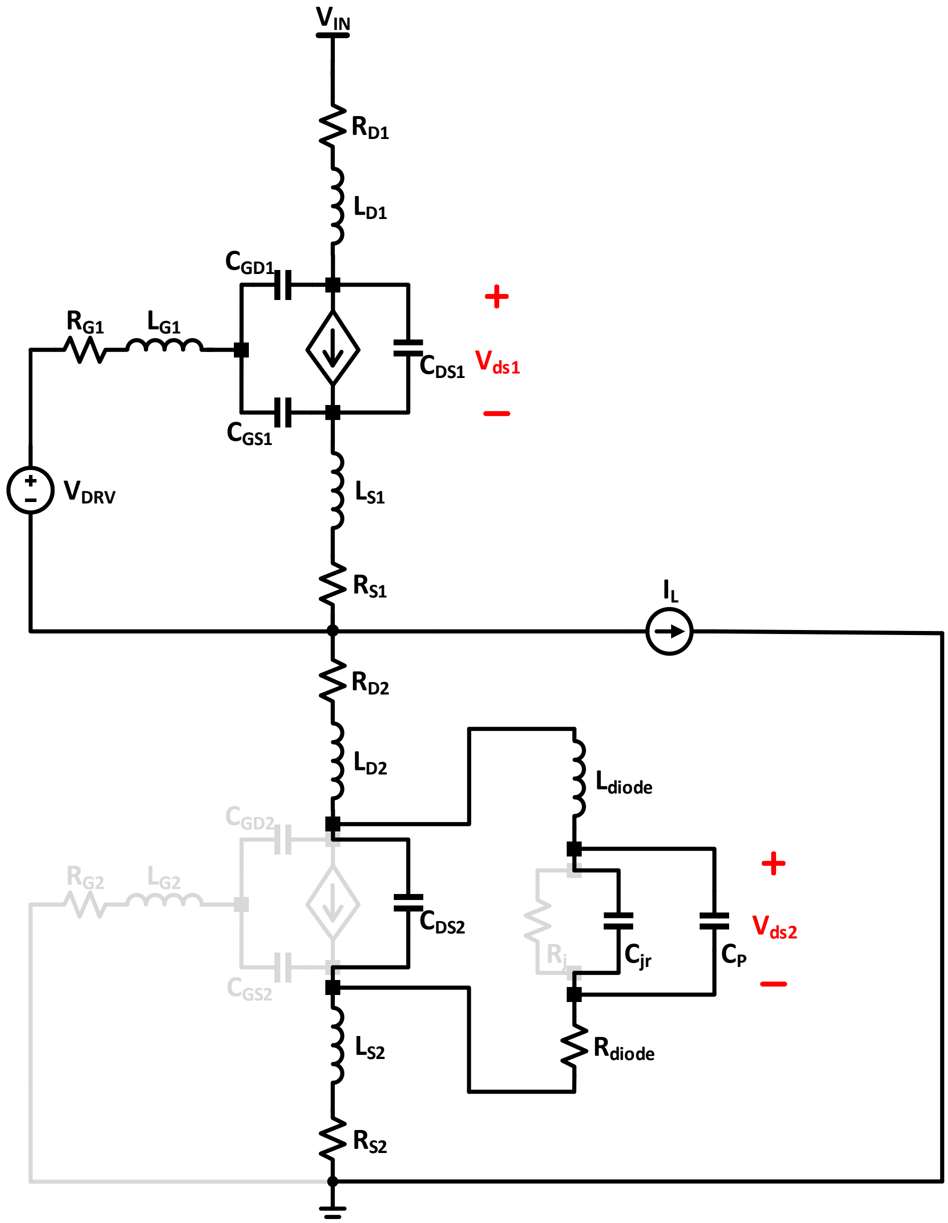

Figure 22. tr4: Plateau Period Of HS Gate

In a Schottky diode, the presence of an ohmic contact eliminates the flow of minority carriers by tunneling majority carriers and there is no stored charge, unlike pn junction diodes. It is important to understand the loss due to the Schottky diode and plateau effect and be able to estimate their contribution to the main model. There is additional reverse recovery loss due to the Schottky diode. C_{oss2} and C_P are the main contributors to peaking of the current. From this power lost in the channel, I_{peak} can be estimated, where Z_o is the characteristic impedance.

$$I_{peak} = \frac{\Delta V_{DS1}}{Z_o} = \frac{\dfrac{tr4.(V_{in} + Vd)}{(tr_3 + tr_4)}}{\sqrt{\dfrac{L_{D1} + L_{S1} + L_{D2} + L_{S2}}{C_{DS2} + C_P}}} \tag{3.14}$$

G. Stage 7(tr5: remaining transition after plateau ends)

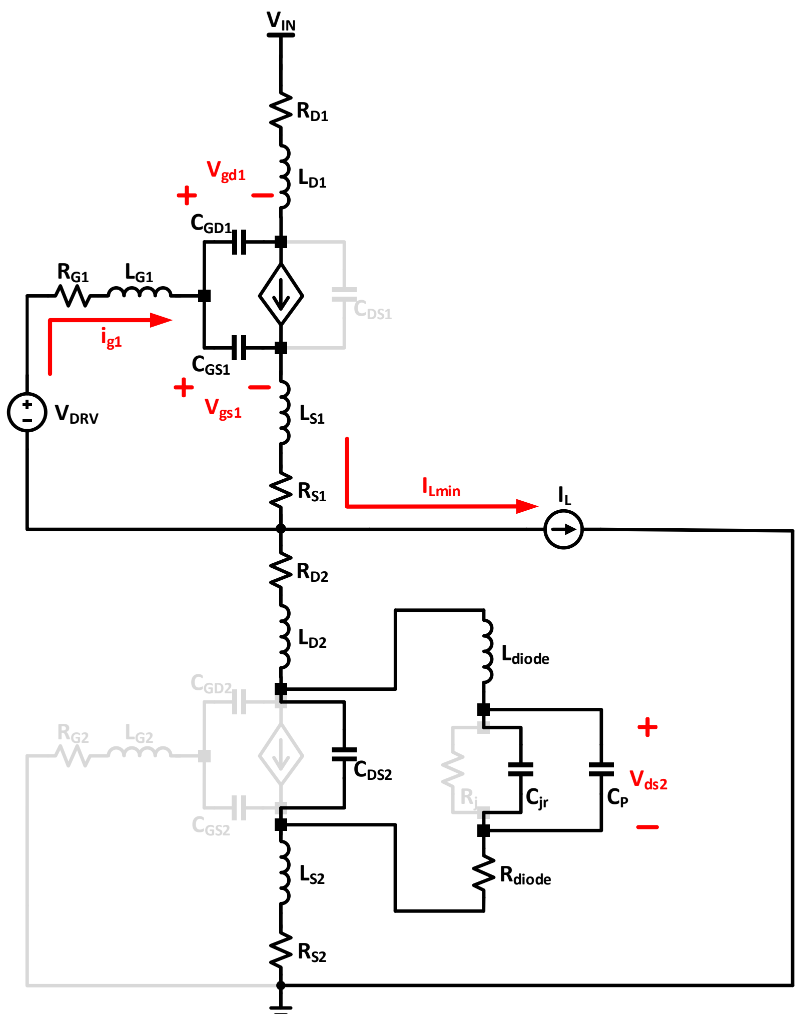

Figure 23. tr5: Remaining Transition After Plateau Ends

This period signifies the time taken for a complete turn on of the HS FET. The equivalent circuit during this phase is shown in Figure 23. We do not calculate this period for the loss analysis because it does not contribute to the switching losses.

3.3 Switching Analysis for Low side Turn On

Seven phases of transitions are analyzed, starting from when HS switch is turned off to the end of the LS switch turn-on. All waveform transitions are labelled in Figure 24. The behavior of V_{DS}, I_{DS}, V_{GS}, i_{diode} and i_{ch} of both LS and HS FETs is observed. Any assumptions made are specified in the respective transitions.

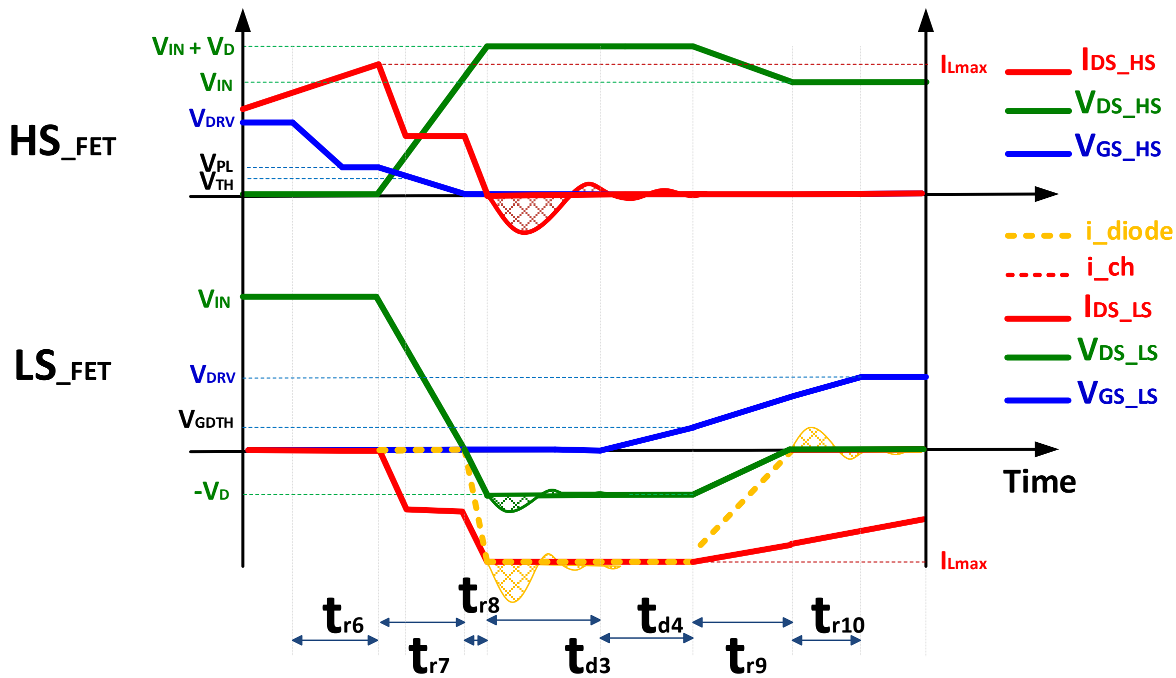

Figure 24. Transition Diagrams For Switching Analysis For Low Side Turn On

A. Stage 1(tr6: Hs driver is pulled down to initiate HS turn off)

During this stage, the HS driver is pulled down to initiate HS turn off. The input capacitor of the HS FET starts discharging from V_{DRV} to V_{PL}. The equivalent circuit is shown in Figure 25. The analysis of this stage can be done by using the gate sink current i_{gdr1}.

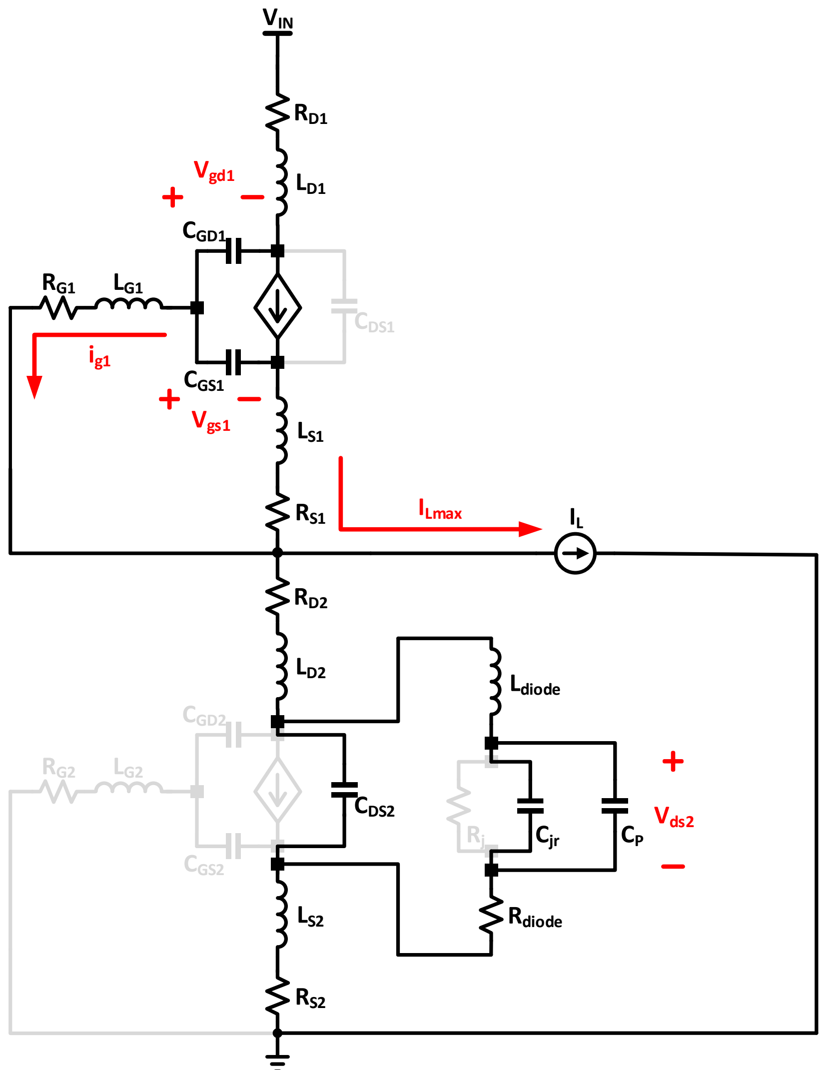

Figure 25. tr6: HS Driver Is Pulled Down To Initiate HS Turn Off

This stage is not considered for power loss analysis because V_{DS1} is assumed zero during this period. But this period is calculated to study the effective dead-time. The transition time during this phase is given by equation (3.15), where plateau voltage is calculated in equation (3.16).

$$t_{r6} = \frac{(C_{GS1} + C_{GD1}).(V_{DRV} - V_{PL})}{i_{gdr1}} \tag{3.15}$$

$$V_{PL} = V_{th} + \frac{I_{Lmax}}{g_{fs}} \tag{3.16}$$

B. Stage 2(tr7: HS turn off period)

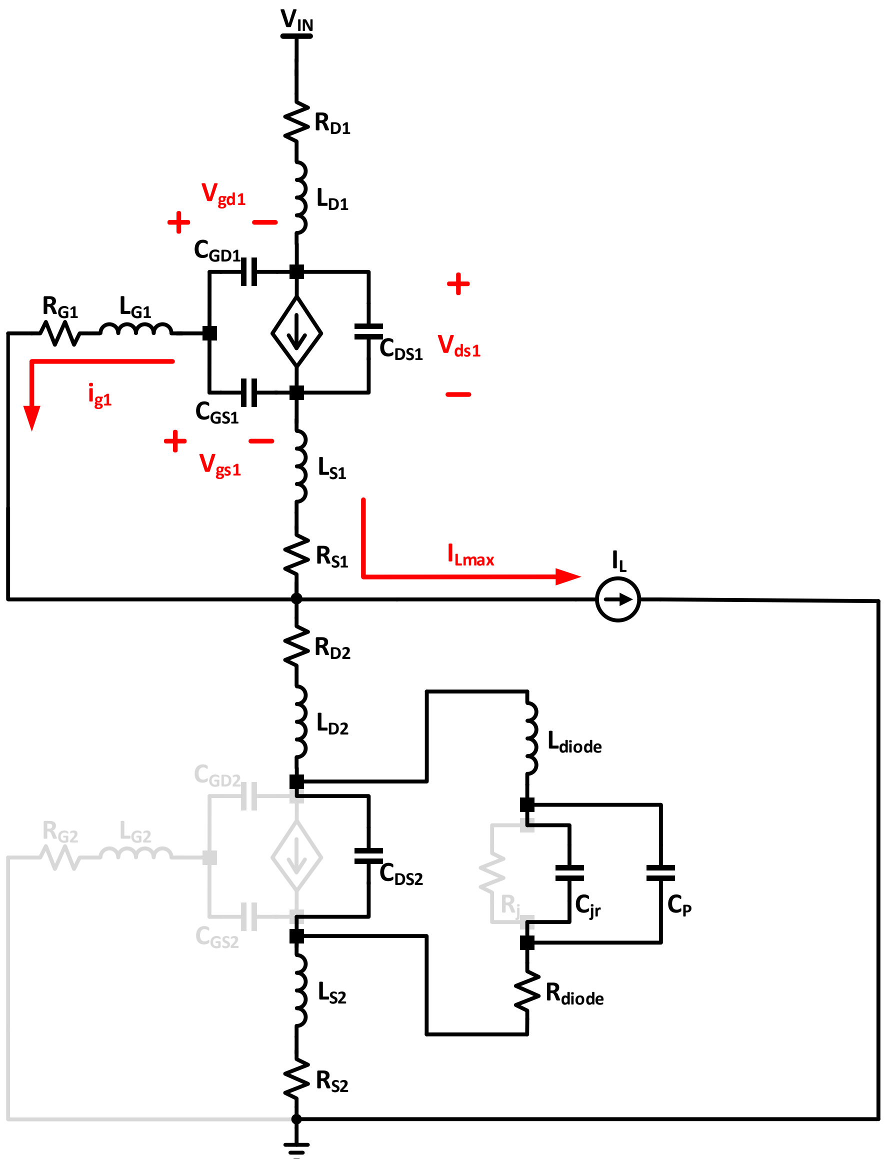

Figure 26. tr7: HS Turn Off Period

During this period, as V_{GS2} drops below V_{PL}, the channel current of HS starts to decrease. The equivalent circuit during this phase is shown in Figure 26. The rate of change of drain current of HS and LF FET is limited by the parasitic inductances in the loop. A faster gate loop will cause i_{ch1} to drop to zero before the Schottky diode is at maximum forward bias potential. The equivalent output capacitor of HS C_{DS1} starts charging and I_{DS1} drops from I_{Lmax} to zero. The presence of a higher reverse capacitance from the Schottky diode decreases the rate at which the switch node voltage drops. This period ends when V_{DS2} = 0. This period can be calculated from [15], and is given by equation (3.17).

$$t_{r7} = \frac{(C_{GS1} + C_{GD1}).I_{Lmax}.R_{G1(off)} - I_{Lmax}.L_S.g_{fs}}{\frac{I_{Lmax}}{2} - \frac{C_{GD1}.I_{Lmax}.R_{G1(off)}.g_{fs}}{2.C_{DS1}}} \tag{3.17}$$

C. Stage 3(tr8: turning on delay for Schottky diode)

This period signifies the time taken to completely turn on the Schottky diode. The equivalent circuit during this phase is shown in Figure 27. The transition time is derived and given in equation (3.18).

$$t_{r8} = \frac{2.C_P.(V_d)}{I_{Lmax}} \tag{3.18}$$

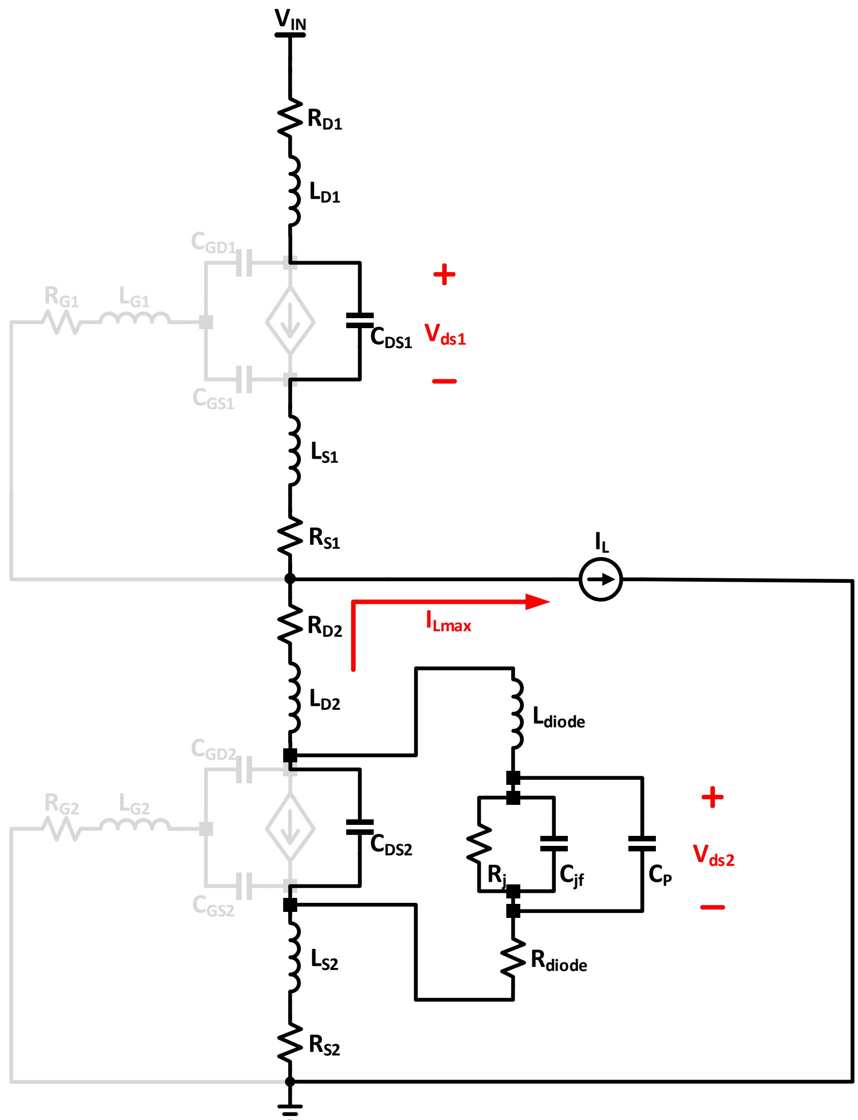

Figure 27. tr8: Turning On Delay For Schottky Diode

D. Stage 4(td3: dead-time after HS turn off)

As discussed before, if the dead-time is not optimized for a regular buck converter without an anti-parallel Schottky diode, the conduction losses in the dead-time will be very high. The Schottky diode limits this to around -0.3V without having the need to design a complex circuit to optimize dead-time. The conduction time is set by the controller is $t_{dead\text{-}time2}$. The equivalent circuit during this phase is shown in Figure 28.

This stage ends when the LS FET gate is pulled high. This transition period is given by equation (3.19), which is a byproduct of t_{r6}, t_{r7}, t_{r8} and $t_{dead\text{-}time2}$.

$$t_{d3} = t_{dead-time2} - (t_{r6} + t_{r7} + t_{r8}) \tag{3.19}$$

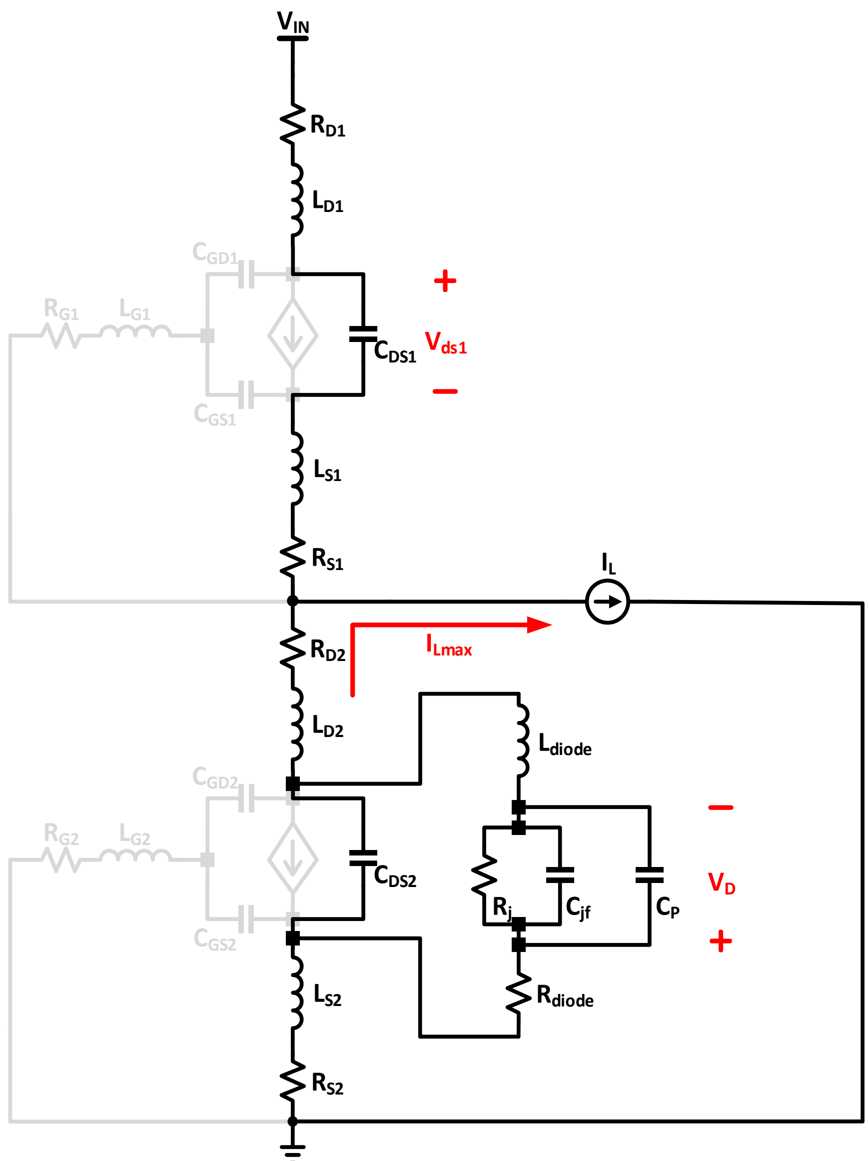

Figure 28. td3: Dead-Time Period After HS Turn Off

E. Stage 5(td4: dead-time after LS turn on)

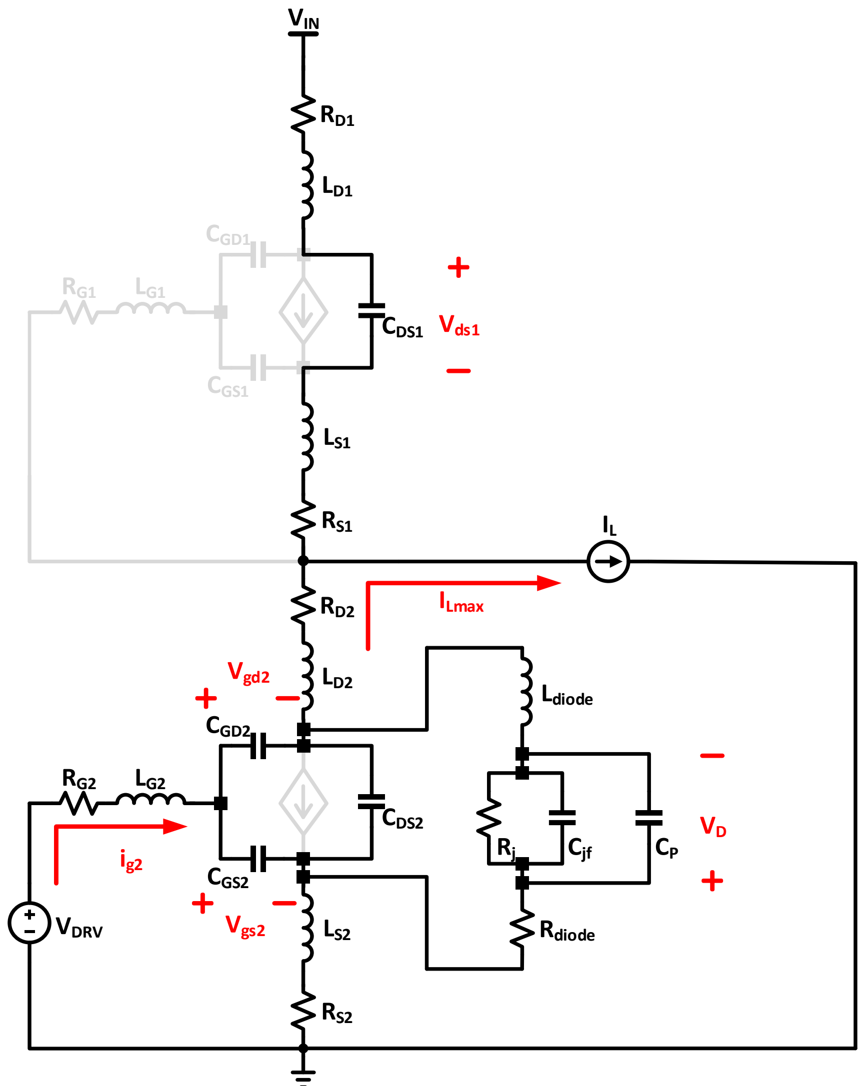

Figure 29. td4: Dead-time After LS Turn On

The equivalent circuit for this phase is shown in Figure 29. At the beginning of this transition, the LS gate driver is pulled high and the LS gate capacitor starts charging. The conduction through the Schottky diode continues until $V_{GS2} = V_{gdth}$. The time period for this stage is given in equation (3.20). This stage ends when V_{GD2} reaches V_{gdth}.

$$t_{d4} = \frac{(C_{GS2} + C_{GD2}).(V_{gdth} - V_d)}{I_{gdr1}} \tag{3.20}$$

F. Stage 6(tr9: turning off delay for the Schottky diode and LS turn on)

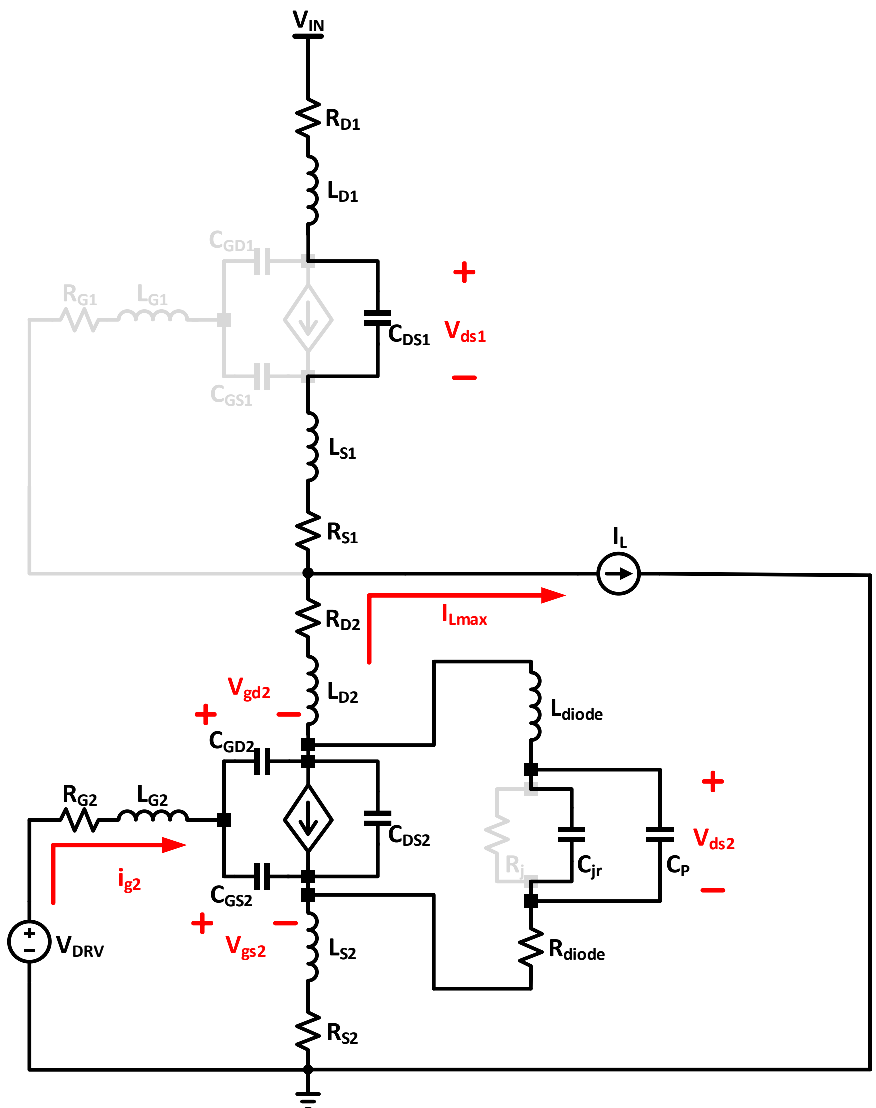

Figure 30. tr9: Turning Off Delay For Schottky Diode And LS Turn On

The equivalent circuit for this stage is given in Figure 30. This time can be calculated the same as t_{r9} from Stage 3, given by equation (3.21).

$$t_{r9} = \frac{2.C_P.(V_d)}{I_{Lmax}} \tag{3.21}$$

G. Stage 7(tr10: remaining rise period of LS)

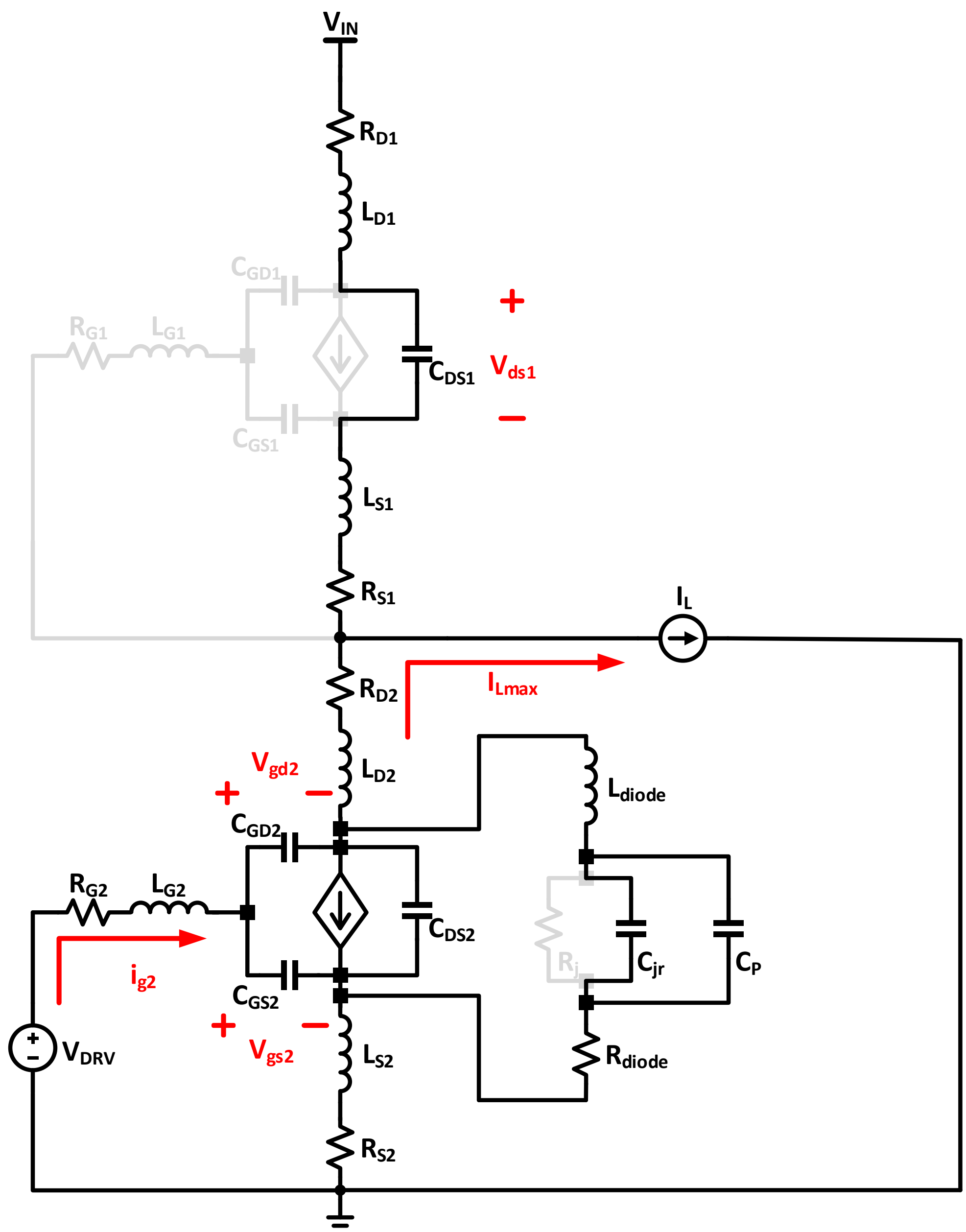

Figure 31. tr10: Remaining Rise Period Of LS

The input capacitor charges above V_{gdth} and the LS FET conducts dissipating current in the channel. The equivalent circuit for this stage is given in Figure 31. This transition period is not calculated here because this phase does not contribute to the switching loss.

3.4 Process Flow Diagram

The transition times for every phase are calculated in section 3.2 and section 3.3 using piecewise analysis. These timing values are used to derive the switching power losses during one clock cycle of the converter and the effective dead-time expression, which will be detailed in chapter 4. The transition times calculated will be verified to the simulated and the measured values from the transition waveforms in Chapter 4. The process flow diagram for the modeling sequence is shown in Figure 32.

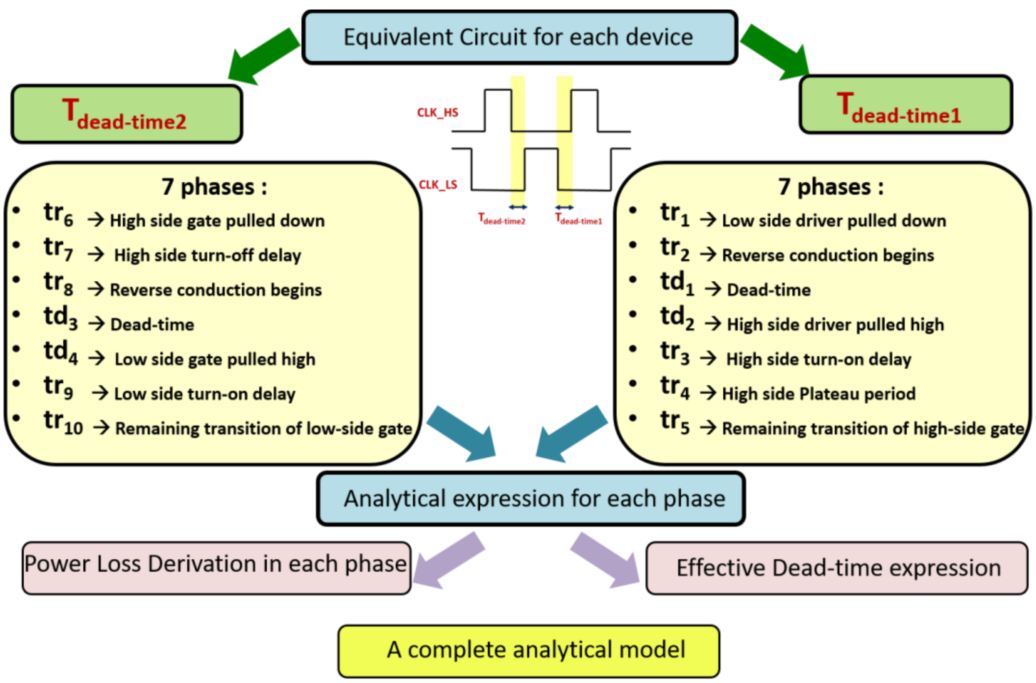

Figure 32. Process Flow Diagram For The Analytical Modeling

4. MODEL VERIFICATION AND DIODE CHARACTERIZATION

An industrial controller and driver have been used to design a buck converter in Figure 33 using GaN FETs for switching frequencies, 400 KHz and 2 MHz. The key parameter ranges for converter design are specified in Table 3.

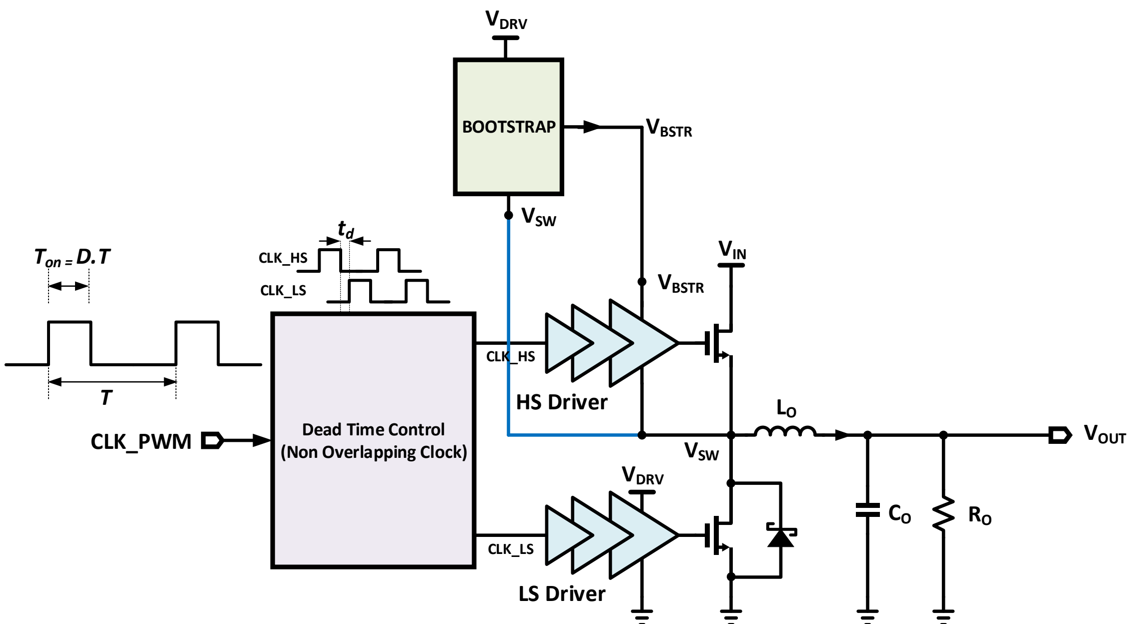

Figure 33. System Overview Of The Designed Buck Converter Power Stage

Parameter	**Design Range**	**Unit**
Input Voltages	8 - 20	V
Output Voltages	1.5 - 5	V
Switching Frequency	0.4 and 2	MHz
Load Current	0.5 - 6	A
Dead-time	10 - 110	ns

Table 3. Design Specifications

For calculation of effective dead-time from the analytical model, different transition phases were analyzed. The dead-time period for LS off to HS on transition (effective dead-time 1) that is set by the dead-time generating block can be calculated from the difference in the moments when the LS driver is pulled low to when the HS driver is pulled high. But, the effective dead-time is the one seen at the switch node, which varies according to the inductor current. The dead-time period for HS off to LS on transition (effective dead-time 2) follows the same principle. Effective dead-times are derived in equations ((4.1) and ((4.2).

$$effective\ deadtime\ 1 = t_{r2} + t_{d1} + t_{d2} + t_{r3} \tag{4.1}$$

$$effective\ deadtime\ 2 = t_{r8} + t_{d3} + t_{d4} + t_{r9} \tag{4.2}$$

The total power loss can be estimated from the analytical models as a sum of conduction loss, switching loss, reverse conduction loss, and gate drive loss, which are given in expressions ((4.3) to ((4.6).

$$\begin{aligned} Switching\ Loss = f_{sw}.\Bigg[& \int_0^{t_{r2}} i_{DS2}.v_{DS2}.dt + \int_0^{t_{r3}} i_{DS2}.v_{DS2}.dt + \int_0^{t_{r3}} i_{DS1}.v_{DS1}.dt \\ & + \int_0^{t_{r4}} i_{DS1}.v_{DS1}.dt + \int_0^{t_{r7}} i_{DS2}.v_{DS2}.dt + \int_0^{t_{r8}} i_{DS2}.v_{DS2}.dt \\ & + \int_0^{t_{r7}} i_{DS1}.v_{DS1}.dt + \int_0^{t_{r8}} i_{DS1}.v_{DS1}.dt + \int_0^{t_{r9}} i_{DS2}.v_{DS2}.dt \Bigg] \end{aligned} \tag{4.3}$$

$$Deadtime\ Loss = f_{sw}.\left[\int_0^{t_{d1}+t_{d2}} i_{DS2}.v_{DS2}.dt + \int_0^{t_{d3}+t_{d4}} i_{DS1}.v_{DS1}.dt \right] \tag{4.4}$$

$$Gate\ Drive\ Loss = 2.f_{sw}.[C_{GS1} + C_{GD1} + C_{GS2} + C_{GD2}].V_{DRV}^2 \tag{4.5}$$

$$Conduction\ Loss = 2.f_{sw}.\left[R_{DS(on)} + R_{ESL} \right].I_L^2 \tag{4.6}$$

4.1Measurement Setup

A single phase hard switching buck converter (shown in Figure 34) was measured for different cases to verify switching operation under different dead-time values. A

TI driver, LM5113, was used to drive low voltage enhancement mode GaN part number: 2014C from EPC. Dead-time was adjusted within a range of 10ns to 90ns. An external waveform generator was used to set the switching frequency in the range from 400 KHz to 2 MHz. The measurement setup is shown in Figure 35.

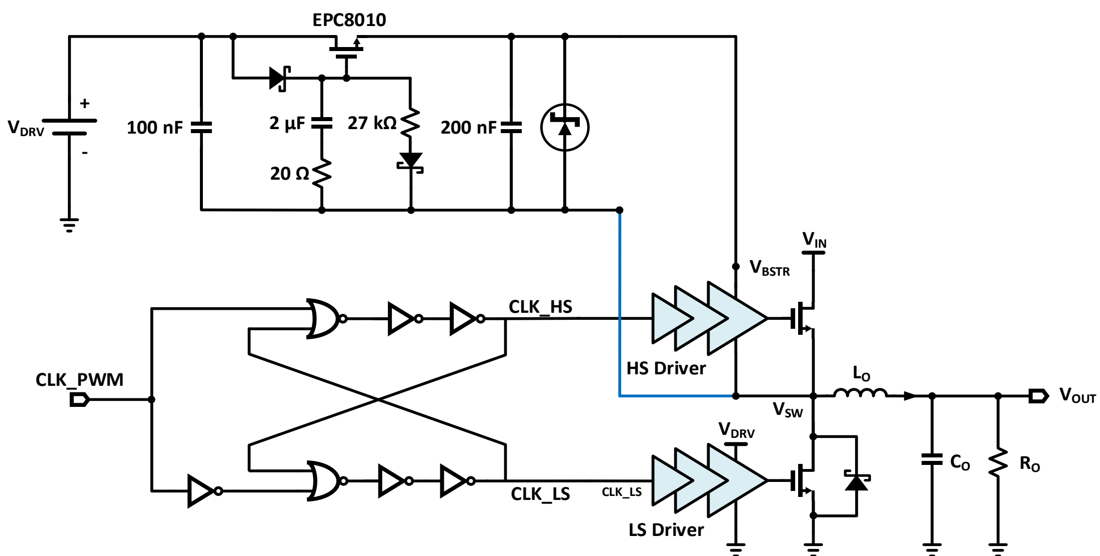

Figure 34. Buck Converter Design

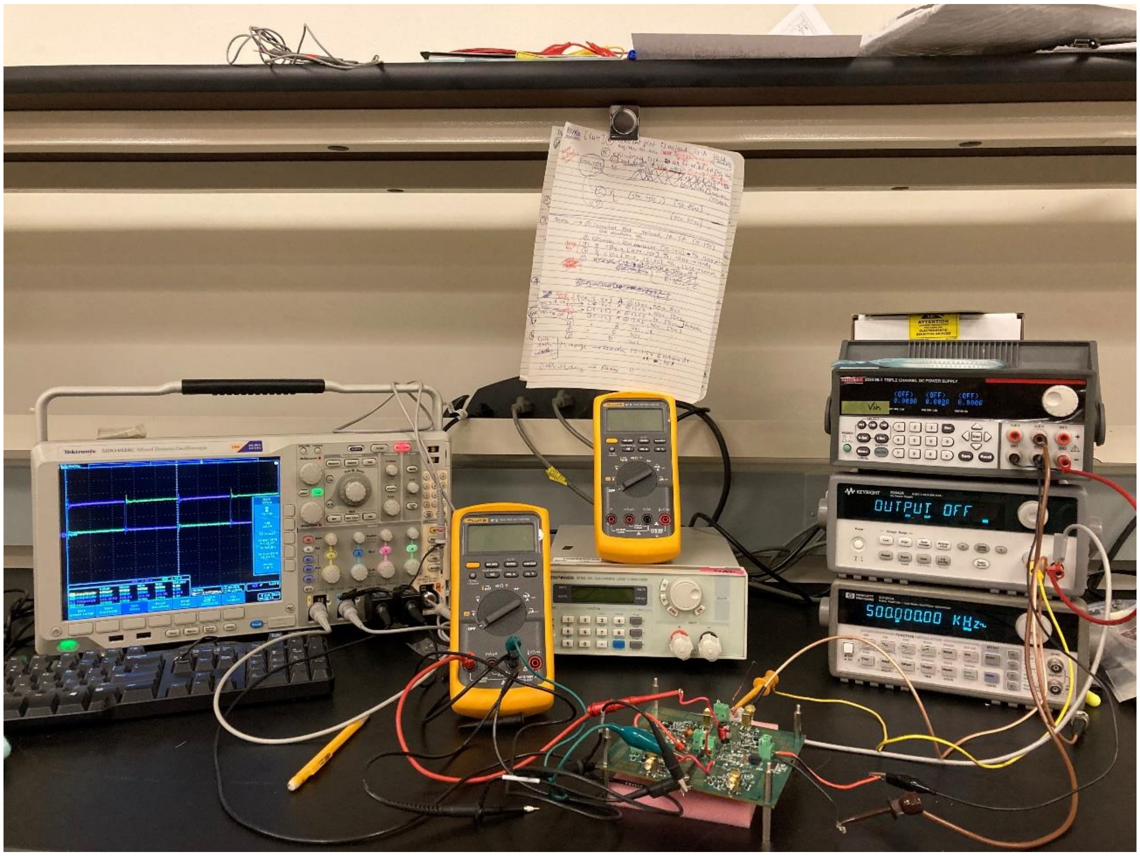

Figure 35. Hardware Measurement Set-Up

4.2 Model Verification

The total loss can be derived from conduction loss and switching loss. The main sources of conduction loss are channel resistances from the HS and LS FETs and the effective series resistance loss of the output inductor. The main sources of switching loss are the loop resistances set by the PCB tracks, voltage controlled current sources of the HS and LS FETs, and the conduction loss from the Schottky diode. High frequency turn-on and turn-off ringing loss is also added to the analysis.

For a broader understanding of the buck converter with GaN power FETs, a buck converter with synchronous rectifier was designed and simulated using EPC2014C for the high side and low side FETs. The simulation model was provided by EPC in LTSpice software.

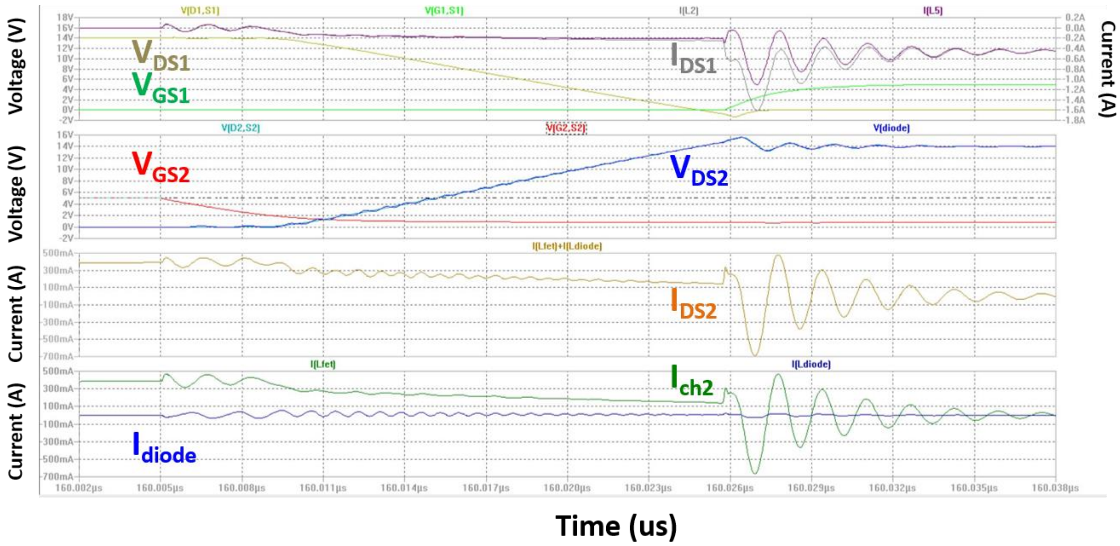

Figure 36. LS Off And HS On Transition Simulation

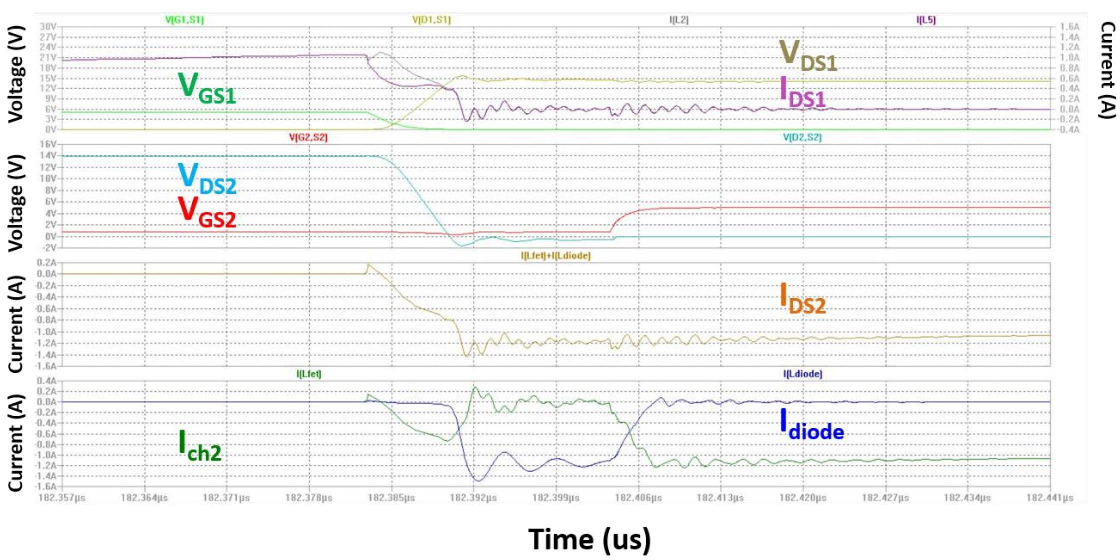

Figure 37. HS Off And LS On Transition Simulation

Figure 36 shows simulations for time period calculation for each phase in switching transitions from LS turn-off to HS turn-on and

Figure 37 shows simulations for time period calculation for each phase switching transitions from HS turn-off to LS turn-on at 2MHz and 1A load current. The values obtained from model are compared to simulated and measured results.

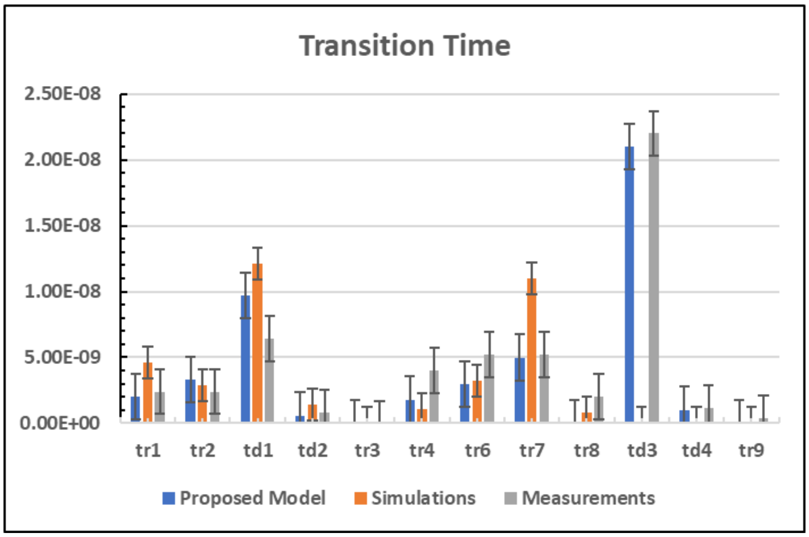

Figure 38. Transition Time Correlation at 400 KHz For 12V To 3.3V Conversion

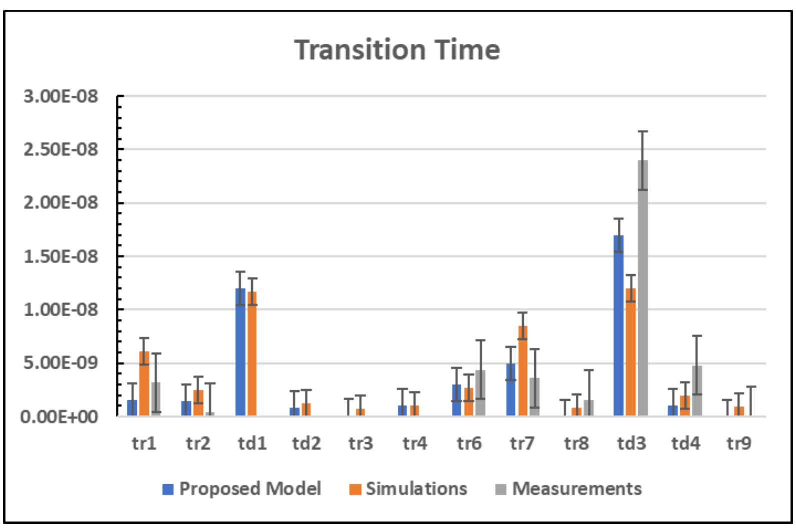

Figure 39. Transition Time Correlation at 2 MHz For 12V To 3.3V Conversion

Figure 38 and Figure 39 show correlation of the calculated values of transition time phases to simulated and measured results. To observe the contribution of reverse conduction loss to total power loss of the buck converter, simulations were done at varying dead-time and load currents for two cases: with and without a Schottky diode in parallel with the synchronous LS FET. The switching frequencies at which all calculations were done range from 400 KHz and 2 MHz with an input voltage range of 8-20V to an output voltage range of 1.5-5V. A time domain snapshot of the switch node voltage and diode current is shown in Figure 40 to show relation of diode current with switch node voltage.

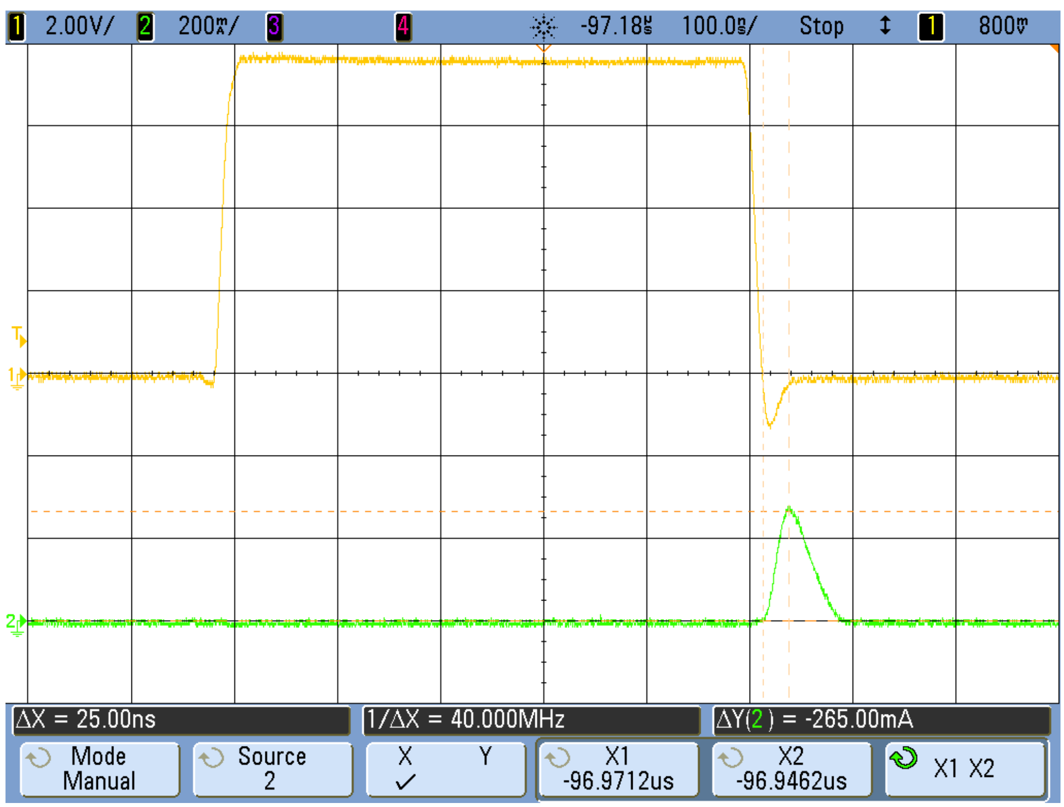

Figure 40. Switch Node Voltage And Diode Current At 400khz

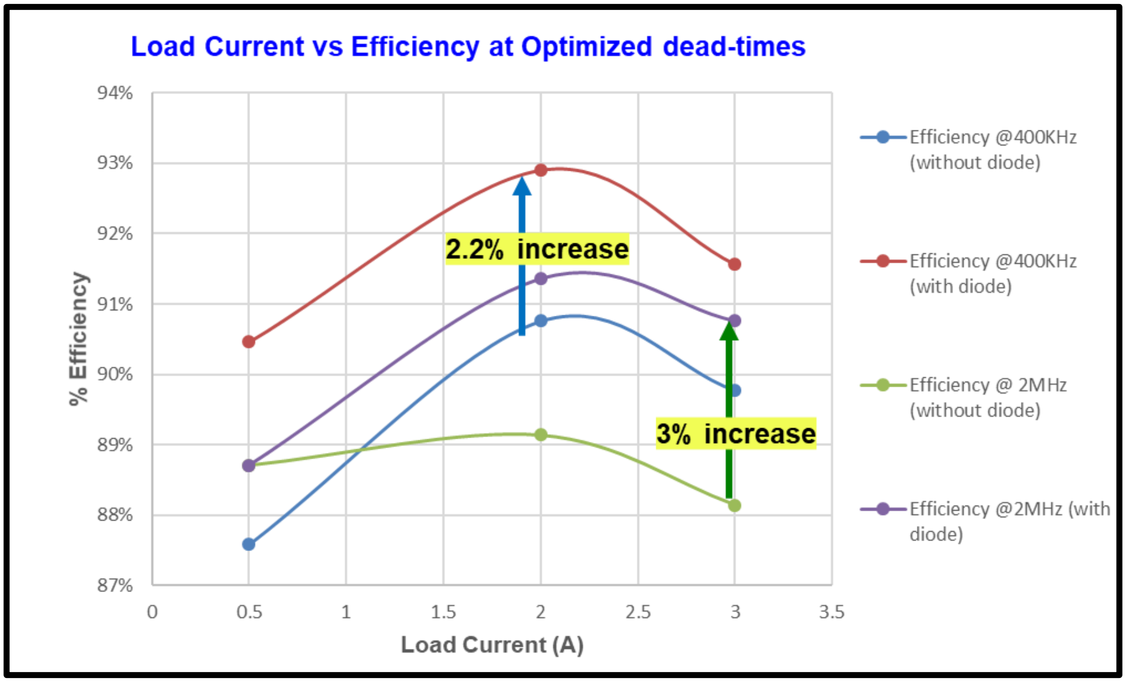

Figure 41. Load Current Vs Efficiency At Optimized Dead-Times

Figure 41 shows an added advantage of the Schottky diode on the efficiency of the converter for 400 KHz and 2 MHz at varying load currents from 500mA to 3A. The converter's efficiency improves by 2 to 3% when including an anti-parallel diode. Figure 42 shows error between calculated and measured effective dead-times for 12V to 3.3V at 1A load current. Figure 43 shows percentage error between calculated and measured effective dead-times for 400 KHz switching frequency at different dead-time values. A 25% error at lower dead-time values is observed due to the non-optimized dead-time values set by the controller for a converter operating at 400 KHz. As per the measurements, around 90ns of optimum dead-time was observed for this condition where the error is around 7%. Finally, Figure 44 shows the trend for less variation in dead-times at higher load currents.

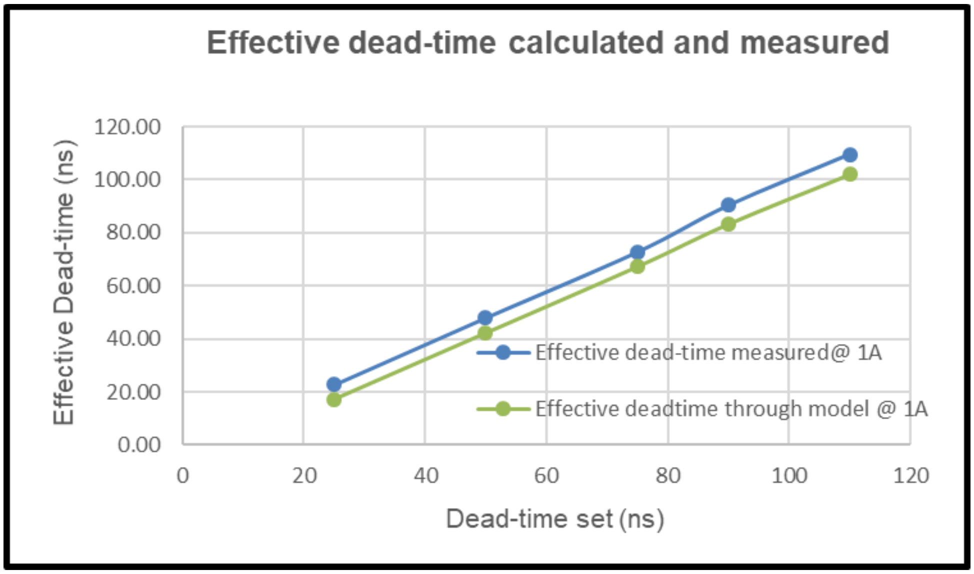

Figure 42. Effective Dead-Time Calculated And Measured

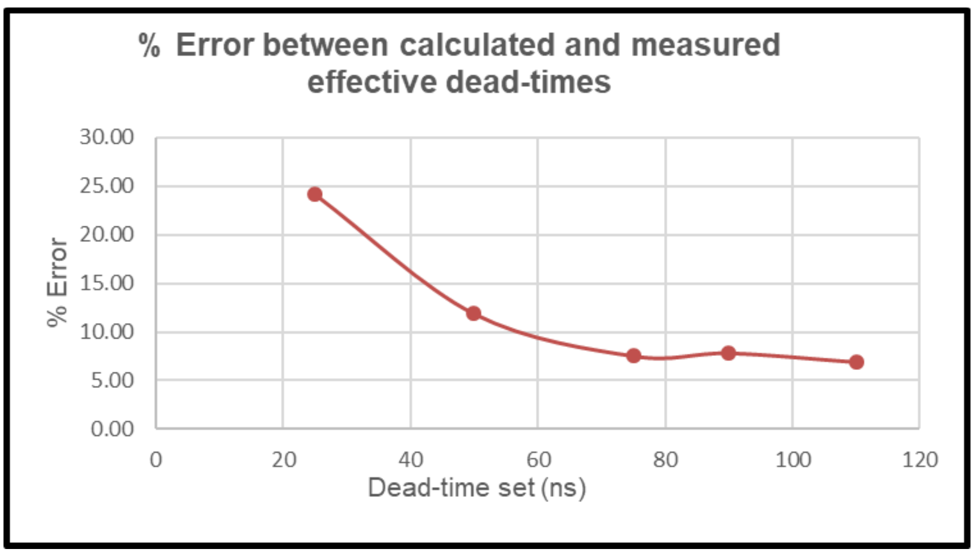

Figure 43. Percentage Error Between Calculated And Measured Effective Dead-Times

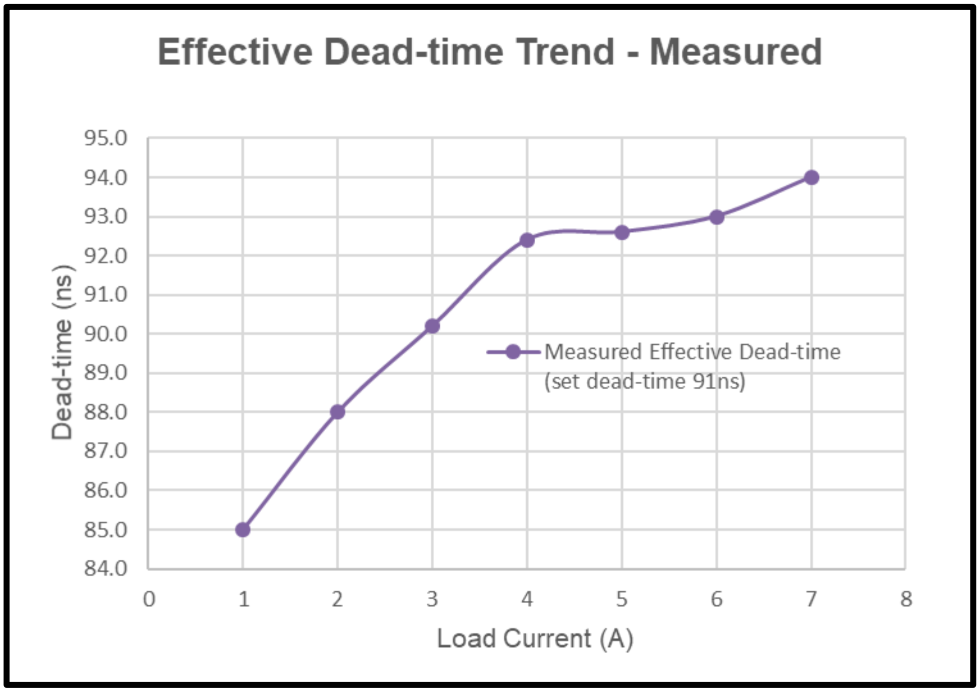

Figure 44. Effective Dead-Time With Increasing Load Current

4.3 Diode Characterization

Different industry diodes are characterized based on the packaging and electrical characteristics to categorize them by application and performance. For selection of a Schottky diode, a selection criteria can be set by introducing a new parameter, D_{limit} that can be calculated from datasheet parameters, which is defined in equation ((4.7).

$$D_{limit} = \frac{I_{F(avg)}}{I_{F(rms)}} \tag{4.7}$$

$I_{F(avg)}$ is the rated average forward current of the Schottky diode and $I_{F(rms)}$ is the repetitive forward current (peak forward current) of the Schottky diode.

If $\frac{t_{deadtime(effective)} \times f_{sw}}{I_{Lmax}} < D_{limit}$, then the choice of the Schottky diode is limited by $I_{F(rms)}$.

If $\frac{t_{deadtime(effective)} \times f_{sw}}{I_{Lmax}} \geq D_{limit}$, then the choice of the Schottky diode is limited by $I_{F(avg)}$.

4.4 Conclusions from Measurements

The effective dead-time observed from the switching analysis through calculations, simulations, and measurements is different than the values set by the controller, which happens due to the interaction between parasitic elements of the power converter. Additional losses due to parasitic components of the Schottky diode add to total power loss. The diode must be rated for the maximum inductor current with lowest parasitic inductances otherwise high amplitude ringing is observed during both the dead-times which increases power loss by 1-2%. Analytical model transition time values are correlated to simulations and measured results, and the developed model shows good correlation with simulations and measured results at 400 KHz and 2 MHz with 1A load current. It has been concluded that the developed model effectively predicts power stage performance for a low side FET using anti-parallel diode in GaN-based PoL buck converters.

5. MODEL COMPARISON TABLE AND CONCLUSION

5.1 Analytical Model Summary

Parameter	TPE 2016	JESTPE 2019	TIE 2020	This work
Synchronous FET analysis	Not present	Present	Present	Present
Dead-time Analysis	Not present	Not present	Present*	Present (analysis)
Switching frequency	2MHz	400KHz, 700KHz and 1MHz	2MHz	400KHz, 1MHz, 4MHz
Converter ratio	12V - 3.6V	12V – 1.2V	12V – 3.3V	20V - 5V, 12V -3.3V,and 8V – 1.5V
Max. Output Power	26W	18W	26W	30W
Max. Load Current	7.9A	15A	8A	6A
GaN device	EPC 2015	EPC 2015C	EPC 2015	EPC 2014C
Driver	LM5113	LM5113	LM5113	LM5113
Max. Efficiency	89.5%	93%	89.9%	93%
Model Novelty	First analytical switching model for eGaN main FET only	Comparison of analysis with and without Synchronous FET	Addition of parasitic elements for high switching frequency	Analysis with anti-parallel Schottky diode with SR FET
Analysis technique	Average power calculation using circuit parameter values obtained from FEA method	On/Off Transition time analysis	Average power calculation using circuit parameters from FEA method (excludes dead-time loss)	On/Off transition time and dead-time loss analysis

Parameter	TPE 2016	JESTPE 2019	TIE 2020	This work
Additional Information	Novel current measuring method based on magnetic coupling			Categorization of Schottky diodes to improve performance of converter

Table 4. Comparison With Prior Work

5.2 Future Work/Improvements

This model can be further developed for extremely low load currents that modify the operation of the buck converter. The proposed model can be updated and expanded to analyze the power loss in other power converter topologies. This model can also be used to analyze losses before the development of adaptive dead-time control strategies.

With an integrated GaN and Schottky as a system-in-chip, the switching performance of a buck converter using GaN can be significantly improved for PoL applications. Control architectures for optimized dead-time using adaptive dead-time techniques can be implemented to improve converter efficiency.

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