Improved Accuracy Area Efficient Hybrid CMOS/GaN DC-DC Buck Converter for High Step-Down Ratio Applications

by

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ABSTRACT

Point of Load (POL) DC-DC converters are increasingly used in space applications, data centres, electric vehicles, portable computers and devices and medical electronics. Heavy computing and processing capabilities of the modern devices have ushered the use of higher battery supply voltage to increase power storage. The need to address this consumer experience driven requirement has propelled the evolution of next generation of small form-factor power converters which can operate with higher step down ratios while supplying heavy continuous load currents without sacrificing efficiency. Constant On Time (COT) converter topology is capable of achieving stable operation at high conversion ratio with a minimum off-chip components and small silicon area.

This work proposes a Constant On Time buck dc-dc converter for a wide dynamic input range and load currents from 100mA to 10A. Accuracy of this ripple based converter is improved by a unique voltage positioning technique which modulates the reference voltage to lower the average ripple profile close to nominal output. Adaptive On time block features a transient enhancement scheme to assist in faster voltage droop recovery when the output voltage dips below a defined threshold. Utilizing Gallium Nitride (GaN) power switches enables the proposed converter to achieve very high efficiency while using smaller size inductor capacitor (LC) power-stage. Use of novel Superjunction devices with higher drain-source blocking voltage, simplifies the complex driver design and enables faster frequency of operation. It allows 1.8V Complementary Metal-Oxide Semiconductor (CMOS) devices to effectively drive GaN power FETs which require 5V gate signal swing.

The presented controller circuit uses internal ripple generation which reduces reliance on output cap equivalent series resistance (ESR) for loop stability and facilitates ripple reduction at the output. The ripple generation network is designed provide a

optimally stable performance while maintaining load regulation and line regulation accuracy withing specified margin. The chip with ts external Power FET package is proposed to be integrated on a printed circuit board for testing. The designed power converter is expected to operate under 200 MRad of total ionising dose of radiation enabling it to function within large hadron collider at CERN and space satellite and probe missions.

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INTRODUCTION

1.1. Motivation

Power Management systems are employed as effective means of delivering, regulating and utilizing power from a supply source to the circuits which achieve functional objectives of the electronic product. Power management ICs (PMICs) mainly consist of switching and linear regulators supported by other peripheral circuits. Switching regulators are highly efficient for high step up-down ratios. Buck dc-dc converters have a power switch which is switched between supply and ground. The switches offer zero to very low impedance when closed and infinite impedance when open. Power dissipation occurs due to switching losses, conduction losses and other fixed losses. The circuit must be designed to have minimal overhead power consumption through peripheral circuits and losses for high efficiency. GaN power FETs help the alleviate the switching losses because of low RDS_{ON}. A L-C filter is a a part of this power stage which averages out the switching waveform and provides a continuous output. Figure 1.1 represents a simple and widely used buck converter topology.

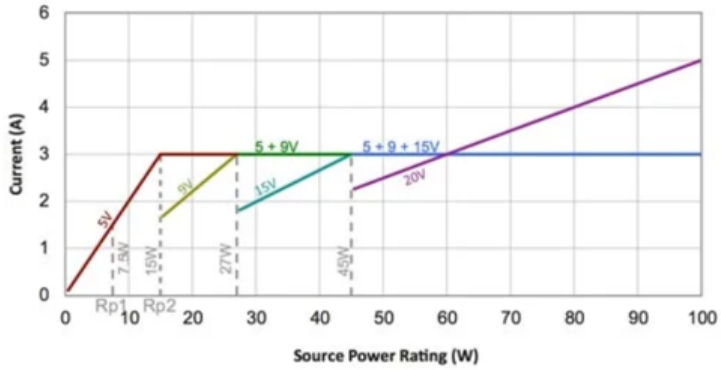

Figure 1.1: Four Voltage Levels (5, 9, 15, 20 V) and Currents up to 5 A in USB PD 3.0,Enabling Power Delivery up to 100 Watts

A closed loop system includes a controller which maintains the stability of the circuit during various operating conditions. The controller must also be able to mitigate the variations in output due to load and line fluctuations. As shown in Fig 1.1, current trends in PMIC focus on building regulators for high levels of power often exceeding 10W for power delivery and POL applications[4]. Integrated chip solutions are unable to support high current operation due to limited current handling capacity with tolerable losses within margin. Also, the frequency of operation is limited by switching losses due to on resistance of Silicon MOSFET. A small form factor is also desirable in this high level power segment.

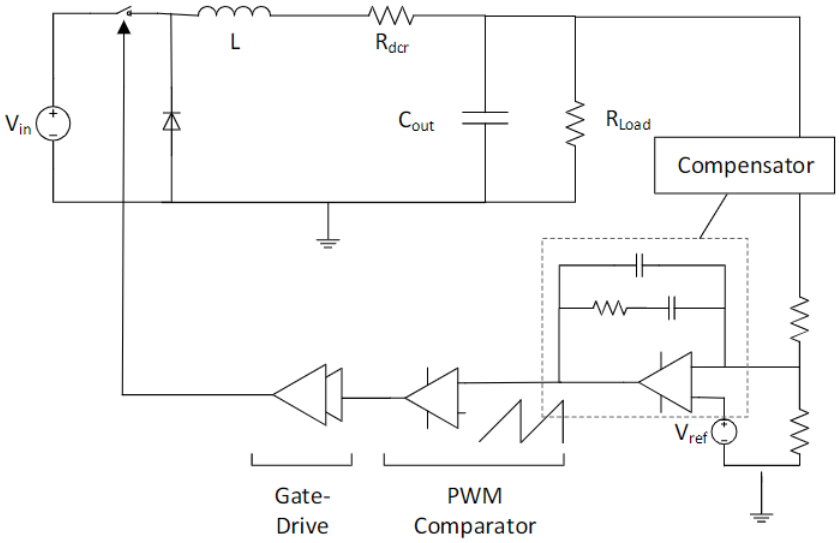

Figure 1.2: Buck Converter With Voltage-mode Control

Gan switch based converters have a huge potential in the industry with the demand expected to cross 1 billion USD by 2022.[13]. Figure 1.3 indicates the major metrics in consideration like efficiency, cost, size and weight, volume, reliability for a optimised design of a power converter product.

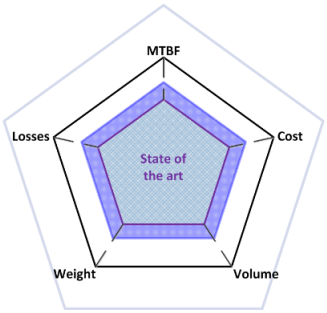

Figure 1.3: Consideration for design of POL converters

GaN is the enabling technology for high power density converters.[19]. The proposed work utilizes this feature of GaN to produce a high accuracy, fast converter.Enhancement mode GaN from EPC are used for this work. One advantage of GaN is that it is very tolerant to high total ionising dose of radiation. The numbers published by EPC indicate a very high tolerance to radiation. This allows this work to be used in military, space and scientific applications in nuclear environment.GaN has a high breakdown voltage and upto tens of GHz of operation.Compared to Silicon FETs, it has almost 2x lower ON resistance and almost 100 times power density[19]. Combined with inherent radiation hardness, GaN is the suitable candidate for our application. The low Ciss and Coss of GaN means that the loop frequency of converter can be much higher than its Si counterpart resulting in greater speed and accuracy[20].

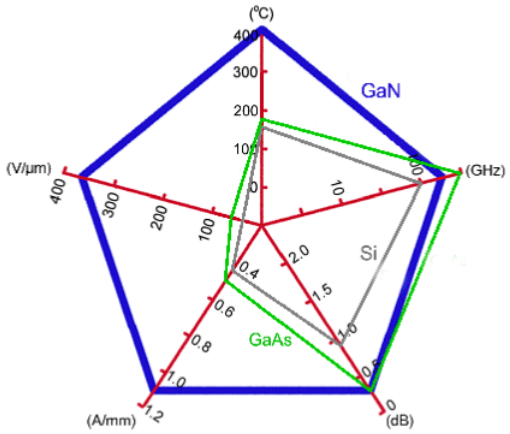

Figure 1.4: Benefits of GaN over Si and GaAs [7]

To harness all the features of GaN as switch[20], a high speed CMOS driver and controller is designed which can function continuously in normal and radioactive environment. The traditional voltage mode type-III buck dc-dc controllers provide the highest accuracy dues to high gain. However, they are not suitable for very

high step-down ratios as they produce very low duty cycle which is highly unreliable. Also they are bulky due to presence of external compensating network components. Stabilizing them for entire dynamic input and output range is also complex and challenging. Their fixed frequency operation also makes this architecture an overkill for applications where need for speed precedes accuracy. Alternatively, hysteritic aka 'bang bang' converters are highly preferred for high speed operation. They have simple loop with very less propagation delay and don't require compensation.[8]. However they tend to overshoot for very low duty cycles as the propagation delay becomes comparable to the duty cycle time. This requires a comparator to be designed with very low offset, propagation delay and high bandwidth. This makes the design colossal.

Constant ON Time converters address this shortcomings by having a minimum dead time larger than the comparator delay[1]. This prevents overshoot during High Side turn-on time. Most of the state of art high step-down ration converters in industry are based on COT topology. However, they have poor load output accuracy due to presence of significant ripple at the output. Also, the noise content is spread across wide frequency band as the converter operates at pseudo-fixed frequency[8, 11]. This makes it necessary to use a Low Drop regulator(LDO) at output to achieve smooth ripple free output. This increases the silicon area and cost of the power management system. This work mitigates the above problems by using a Constant On Time buck dc-dc converter for a wide dynamic input range and load currents from 100mA to 10A. The accuracy of this ripple based converter is improved by a unique voltage positioning technique which modulates the reference voltage to lower the average ripple profile close to nominal output. Adaptive On time block features a transient enhancement scheme to assist in faster voltage droop recovery when the output voltage dips below a defined threshold. Utilizing GaN power switches enables

the proposed converter to achieve very high efficiency while using smaller size LC power-stage. Use of novel Superjunction devices with higher drain-source blocking voltage, simplifies the complex driver design and enables faster frequency of operation. It allows 1.8V CMOS devices to effectively drive GaN power FETs which require 5V gate signal swing.

The presented controller circuit uses internal ripple generation which reduces reliance on output cap ESR for loop stability and facilitates ripple reduction at the output[21]. The designed power converter is expected to operate under 200 MRad of total ionising dose of radiation enabling it to function within large hadron collider at CERN and space satellite and probe missions.

1.2. Objective and Challenges

This research aims to design a integrated CMOS driver and controller to drive GaN Power FETs up to 1MHz frequency. This reduces form factor by reducing size of inductor and capacitor. The inductor used is air core as the converter is proposed to work in radiation prone environment.Higher conversion ratio is achieved by a small ON time of the converter and by use of GaN power devices that exhibit low parasitic gate capacitance. This work tries to address major design challenges in rad-hardened, minimized form-factor power converters with high efficiency, minimum ringing at critical nodes for stability. Use of SuperJunction device to enable low voltage-rated devices to drive the high voltage GaN FETs, high gate drive current capability design,

Major challenges involved in this design are:

- Reducing the ripple at output while maintaining sufficient ripple profile at the feedback node for stability.
- Validating use of high voltage SuperJunction devices to simplify design.
- Implementing Voltage Positioning scheme and Transient Enhancement circuit for better Load and Line regulation.

1.3. Prior Work

Some of the major avenues where prior research is carried out is multi-phase integrated converters for high load current, low conversion ration converters with closer input and output voltages and low load capability converters. Transformer based solution is also used for high switching frequency but its not suitable for small form factor applications. Many commercially available COT converters are offer high conversion ratio but do not meet the high load current capabilities due to monolithic integrated approach[14].Also they have lower output accuracy due to significant ripple at the output. Table 1.1 compares one state of the art power converter that is most closely related to the proposed design solution. The proposed power converter has significant advantages when compared with current state-of-the-art DC-DC converters. Higher switching frequency reduces the filter component size giving a small form-factor.
General trend for the fully-integrated buck converters shows that for high switching frequency applications, the load current is limited as heat dissipation losses due to switching and FET resistance. This is the limiting factor for the load current (<1A). Discrete Power FETs can achieve 100's MHz of frequency. This work employs a hybrid CMOS/GaN architecture to increase the load current to 10A at 1 MHz switching frequency. Most of the prior work have very low efficiency at high step-down ratios[9]. Moreover, fully-integrated silicon solutions have conversion ratios higher than 30 % and typically operate for sub-5V input and output voltages[24]. A goal of this work is to maintain high efficiency at low duty cycle operation (20%) and allow for high conversion ratios.

The project expects following functional specifications from the design:

Parameters	Feast [17]	DOE 7027	This Work
Process	Onsemi i3t25 350nm	Onsemi i3t25 350nm	XFAB 180nm SOI
Input Voltage (V)	5.0 - 12.0	8.0 - 18.0	8.0 -18.0
Output voltage (V)	-	1.0 - 3.3	1.5/2/12
Load Current (A)	$<$ 4A	7	10
Fsw (MHz)	2.0-4.0	1.0-5.0	1
Efficiency η	70%	80%	80% -90%

Table 1.1: Comparison of the Proposed Work with the State-of-art Power Converter

1.4. Proposed Solution

The proposed solution features a Constant On Time buck dc-dc converter for a wide dynamic input range and load currents from 100mA to 10A. The accuracy of this ripple based converter is improved by a unique voltage positioning technique which modulates the reference voltage to lower the average ripple profile close to nominal output. Adaptive On time block features a transient enhancement scheme to assist in faster voltage droop recovery when the output voltage dips below a defined threshold. Utilizing GaN power switches enables the proposed converter to achieve very high efficiency while using smaller size LC power-stage. Use of novel Superjunction devices with higher drain-source blocking voltage, simplifies the complex driver design and enables faster frequency of operation. It allows 1.8V CMOS devices to effectively drive GaN power FETs which require 5V gate signal swing.

The presented controller operates for a input range of 8V-18V with output as low as 1-1.5V. It has a pseudo-fixed frequency of operation around 600KHz. The circuit uses internal ripple generation which reduces reliance on output cap ESR for loop stability and facilitates ripple reduction at the output The designed power converter

with a enclosed gate layout is expected to operate under 200 MRad of total ionising dose of radiation enabling it to function within large hadron collider at CERN and space satellite and probe missions.

1.5. Thesis Organisation

Chapter 1 introduces the research topic, motivation behind this work. Prior work and and the proposed solution is also discussed in the chapter. Chapter 2 provides a detailed COT system overview, MATLAB modelling approach using linearized transfer-function. Chapter 3 discusses the SuperJunction Device Driver and CMOS controller design. Chapter 4 discusses the model and circuit simulation results. The conclusions and future improvements are discussed in Chapter 5.

Chapter 2

CONSTANT ON TIME BUCK CONVERTER ARCHITECTURE

2.1. Buck Converter System

A general buck dc-dc converter is switching based regulator circuit which steps down the input voltage and lowers it to required output. The buck converter obeys the transformer principle:

$$V_{in} * I_{in} = V_{out} * I_{out}$$

The main blocks of the buck dc-dc converter is the Power Stage, the controller stage and the Gate driver stage as shown in the figure. The power FETs produce switching waveform between input supply voltage and ground. The switching waveform is averaged by the L-C filter stage and fed to the output. The controller part regulates the output voltage and minimizes variations in output voltage against load transient, line transient etc. The controller is also designed to imparts stability to the plant (L-C filter) in all conditions. The controller operates at low voltage of 1.8V whereas the power FETs operate with gate swing of 5V and toggle between 0-18V domain. A series of level shifter's are used to translate the gate control signal from low level to high level. The gate of FET represent a large gate capacitance which needs to be driven without any delay. The gate drive strength of the driver stage must be designed carefully to drive the FET gate. The driver design presents a considerable challenge to prevent instability due to ringing and loss in efficiency due to gate leakage.

2.2. Constant ON Time Converter

Unlike traditional voltage or voltage mode control, Constant ON Time control is a unique way to eliminate loop compensation. It does not require a error amplifier and produces a fixed ON time when the feedback voltage falls below a fixed known reference. When during the time where

$$V_{feedback} < V_{reference}$$

is monotonic i.e. in phase with the inductor ripple, then the system operates at a fix frequency based on the ON time set by the one-shot timer. An easy and popular way is to sense inductor current is to use the output cap esr. If the cap ESR is sufficient,

$$ESR * \Delta I_L$$

. ripple dominates the cap ripple and this ripple ensures COT operation through the feedback node. A COT controller like hysteritic controller is fast and simple without any external compensation. Figure 2.1 and 2.2 shows a block diagram of a

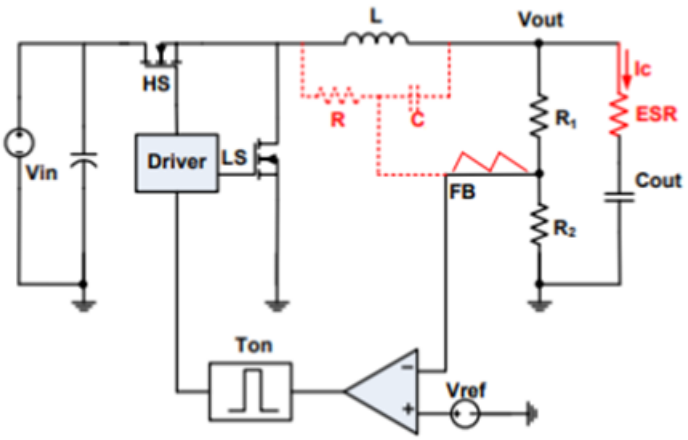

Figure 2.1: Cot Converter Topology [source: TI]

COT controlled buck converter and its operating waveform. It works simply using a comparator , a set-reset (RS) trigger and a ON timer. The COT converter overcomes the problem of overshooting in Hysteritic converter in High step-down ratio operation. Since the on time is pre-determined by an on-time generator corresponding to the requirement of pseudo-fixed frequency operation, and the off time is modulated in the traditional hysteric way,the converter operates in pulse frequency modulation (PFM) mode at light load, which improves the light load efficiency compared with traditional PWM control.

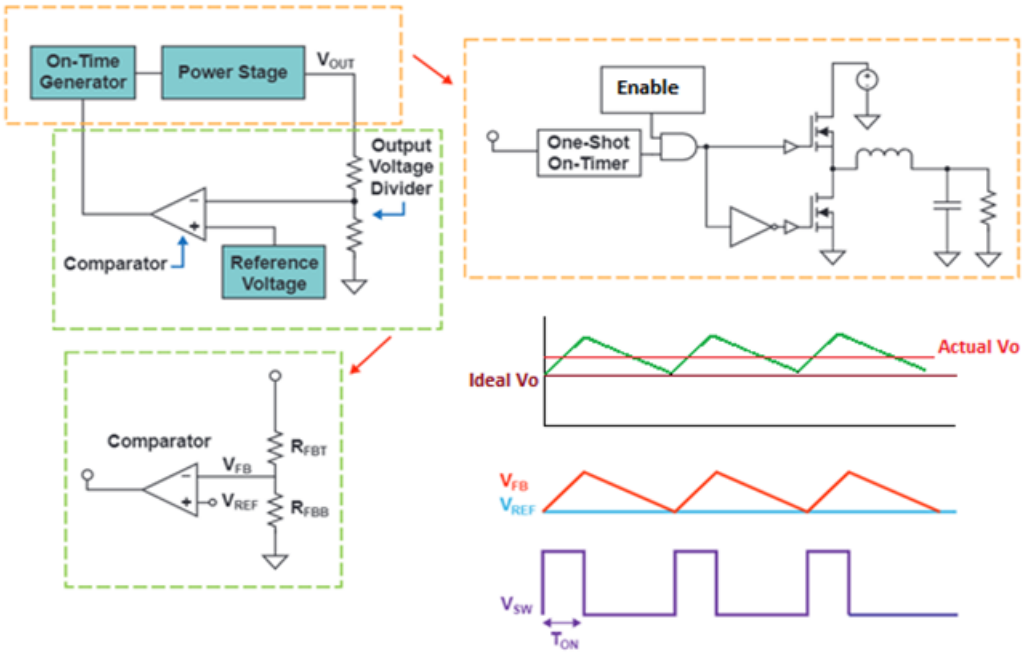

Figure 2.2: Cot Converter Operational Diagram

2.2.1. Stability in COT Converters

2.2.1.1. Pulse Bursting in COT Converter

The operating principle of the COT-controlled buck converter shown in Fig.2.2, is that, at the end of the COT ON time interval, i.e., when one shot timer is turned off after S goes low, V_o must be held higher than V_{ref} to ensure normal operation. Otherwise,in the another COT interval, after a very small off-time caused by the reset signal of the RS trigger, Set signal will trigger till the output is again above the V_{ref}. This multiple ON time intervals withing a short time is called Pulse Bursting Phenomenon, which causes a large inductor current and output voltage ripple. Output voltage of the COT converter is made of ripple around a dc value. This ripple is due to the cap ripple and ESR ripple. This is because the switching frequency is higher than loop frequency which causes inductor current to flow through the capacitor and not the output node.Therefore, it increases with inductor tipple current and ESR and Cap value. The voltage across the capacitor varies depending the inductor and load current. If inductor current is less than load, the the capacitor will discharge in all conditions and thus the output will fall below V_{ref}. This results in Pulse Bursting. Thus, whenever,

$$\Delta Cap_{ripple} > \Delta ESR_{ripple}$$

, Pulse Bursting is observed as shown in Figure.

2.2.1.2. Criteria to Mitigate Pulse Bursting

Figure. 2.3(a) and 2.3(b)[23] depicts steady-state waveform of the inductor current iL and capacitor voltage ripple vc_{ripple} at the output, the negative voltage -v_{ESR} across the ESR resistor, the output voltage V_o, and the RS F/F output under condition of large and small ESR resistors R_{ESR}.As shown in Figure 2.3(a), when the voltage v_{ESR} across the -v_{ESR} resistor is large enough to dominate the output voltage

variation, the COT-controlled buck converter operates normally without pulse bursting phenomenon. When v_{ESR} is not large enough to dominate the output voltage variation, as shown in Fig. 2.3(b), the pulse bursting phenomenon occurs.

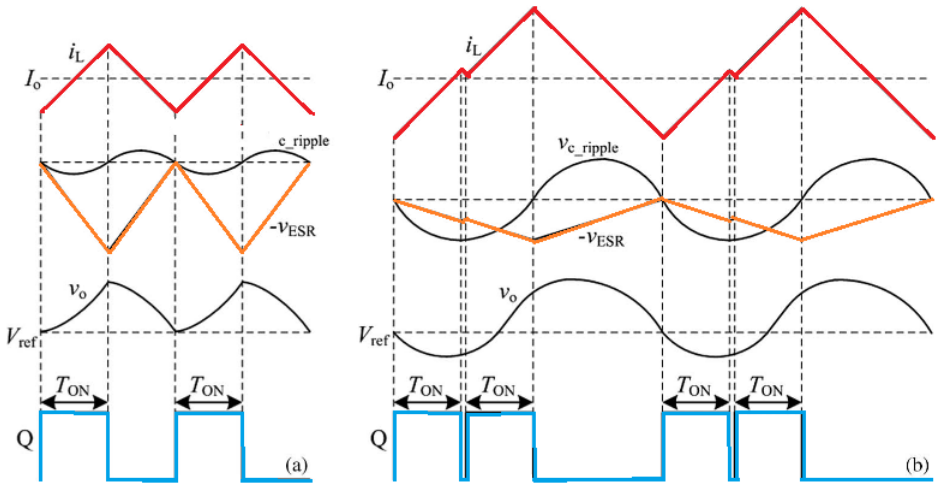

Figure 2.3: Waveforms of the COT-controlled Buck Converter Under Two Different Cases: (a) With Large R_{ESR} and (b) With Small R_{ESR}

As shown in Fig.2.3(b), after some COT intervals, S is turned off for a relatively long time, resulting in large inductor current and output voltage variations. Between the adjacent COT intervals, there is a very short off-time caused by the reset signal of the RS trigger.By observing Fig. 2.3, it can be found that, if the slope of -v_{ESR} is less than or equal to that of Vc_{ripple} at the time instant when S is just turned on, v_o will always be higher than V_{ref} at the time instant when S is just turned off; normal operation can thus be ensured, and no pulse bursting phenomenon occurs. Otherwise, the buck converter will operate abnormally, and pulse bursting phenomenon will occur. Thus, the slope of -v_{ESR} equal to the slope of vc_{ripple} is the critical condition for the normal operation of the COT-controlled buck converter[23].The slopes of -v_{ESR}

and vc_{ripple} at the time instant when S is just turned on can be obtained as:

$$\frac{d(-v_{ESR})}{dt}|_{t=nT_s} = -\frac{d(R_{ESR} * (i_L - I_o))}{dt}|_{t=nT_s} \tag{2.1}$$

$$= -R_{ESR} * \frac{d(-v_{ESR})}{dt}|_{t=nT_s} \tag{2.2}$$

$$= -R_{ESR} * \frac{(v_{in}) - v_o}{L} \tag{2.3}$$

$$\frac{d(v_{c_ripple})}{dt}|_{t=nT_s} = \frac{(i_L) - I_o}{C} = -\frac{\Delta I_L}{2C} \tag{2.4}$$

$$= -\frac{(v_{in} - v_o) * T_{ON}}{2LC} \tag{2.5}$$

respectively, where ILis the peak-to-peak value of the inductor current in steady state.Letting (2.3) equal to (2.5), the critical ESR is:

$$R_{ESR_{critical}} = \frac{T_{ON}}{2C} \tag{2.6}$$

$$R_{ESR_{critical}} * C \geqslant \frac{T_{ON}}{2C} \tag{2.7}$$

To ensure normal operation, R_{ESR} must be greater than $R_{ESR_{critical}}$. Else, the COT-controlled buck converter will work abnormally, and pulse bursting phenomenon will occur.

A very small feedback ramp can cause trouble other than jitter: a 90 phase delay in ESR ripple and cap ripple may make combined FB ripple non-monotonic if the capacitor ripple dominates the ramp ripple. Also, if the ESR ripple is too small, then the capacitor ripple dominates the FB ripple, the sub-harmonics become noticeable for non-monotonic FB ripple.

2.3. COT Control Design for Jitter

2.3.1. Non-Architectural Causes of Jitter[10]

Jitter has origin in power supply implementation issues like as loop stability and PCB layout design. Common non-architectural causes of jitter include:

- Sub-harmonic oscillation due to marginal stability – If the COT control loop has instability, the output voltage and the control signal can crop up either as random jitter, or bi-modal jitter (long-pulse-short-pulse operation).
- High gain compensation design – Error amplifier gain in control loop must not have high gain for noise frequency.
- PCB layout – The magnetic and capacitive coupling of switching signals on PCB must be well isolated to reduce interference induced noise jitter.

Effect of Jitter on Output Voltage Ripple: Usually, it is presumed that increased amount of jitter will cause more ripple at out put. However, COT converters has be proven to have low ripple at output compared to voltage mode control for same amount of jitter at feedback node.

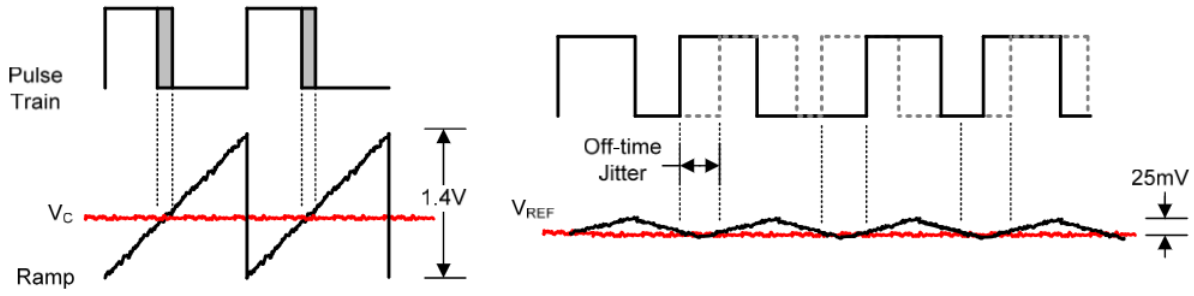

Figure 2.4: Noise Margin Comparison in VMC and COT [10]

Reason for COT having more ripple compared to Voltage Mode Control:

- Higher SNR- In VMC control, the output of error amplifier is around 1V for most modern processes. This results in the amplitude of noise which is usually in 10s of mV being much lesser than the signal i.e. error amplifier output. Thus the SNR is usually quite high. For example, a 1mV noise amplitude accounts for 0.07% of the ramp signal in Voltage mode control for a 1.4V ramp amplitude as shown in Fig 2.4.

- Whereas in COT, the ripple at the feedback is usually not more than 25mV which is quite comparable to noise magnitude. So due to lower SNR, it undergoes more jitter magnitude at output.For example, a 1mV noise amplitude accounts for 0.07% of the ramp signal in Voltage mode control. For example, a 1mV noise amplitude accounts for significantly 4% of the ramp signal in COT control for 25mV ramp.

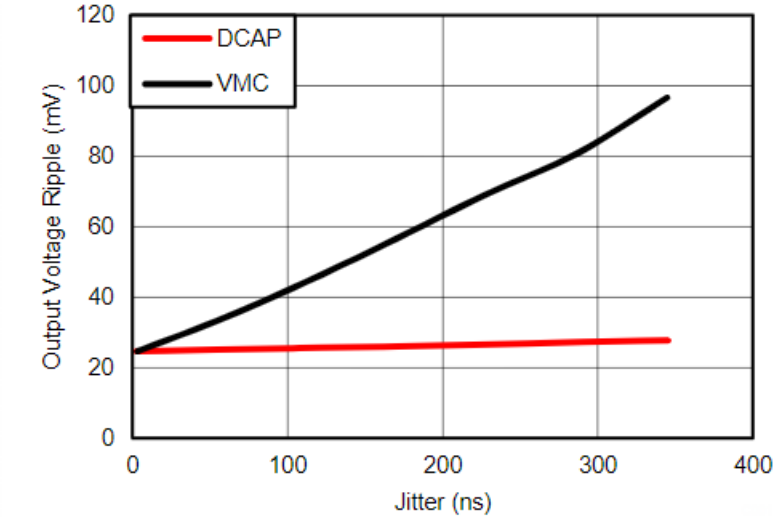

Figure 2.5: Output Ripple Voltage vs Jitter [10]

Figure 2.5 shows that for same jitter the COT has much less ripple over voltage mode control. This is due to two reasons, 1) the nature of fixed frequency control and 2) Speed of control loop.

In voltage mode control, since the frequency is fixed, there is crowding of pulses when jitter occurs. Thus even if previous pulse delivered extra power to output, the next pulse will also contribute to some extra energy which is over the load requirement and cause output to overshoot. In COT, since there is no fixed frequency, the energy delivered decreases as pulse density decreases. Hence, jitter in COT gets corrected in each cycle whereas in fixed frequency operation it doesn't get corrected. Secondly, in voltage mode fixed frequency operation, the feedback coming from error amplifier must slew out of ramp signal range to skip the pulse when energy crowding occurs due to pulse crowding. However, it is possible only if loop response is fast. that calls for a much higher i.e. approx 10 to 50 times more faster switching frequency. In COT control, output itself is the feedback. So any overshoot in the output is easily mitigated through feedback without requirement of slew compensation even for a small signal transient. This is not possible in fixed frequency unless the transient is large enough.

So in conclusion, little jitter in unavoidable in switching power converters/ It is mainly due to noise at the input node to modulator which controls power switched by creating error signal by comparing the output to desired output using a known reference. Different control architectures such as voltage mode control, current mode control and constant on-time ,have different methods to control switching so these schemes have different jitter signatures. Fixed frequency converter are affected by both ON time and OFF time jitter. This includes voltage mode control and fast current mode control. COT control is susceptible to only OFF time jitters the ON time is controlled by ONE shot timer. It is not uncommon to see voltage mode

converters with on-time jitter with only 20 ns, where a typical constant on-time COT converter might have 100 ns of off-time jitter.

2.3.2. Feedback Ramp and Load Regulation

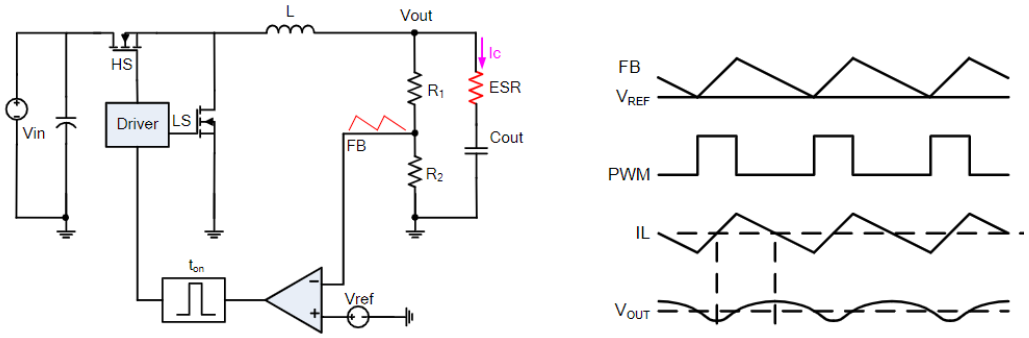

Figure 2.6: COT Buck Circuit Diagram and Operational Signal Diagram [5]

COT control turns on the HS signal every time the V_{FB} falls slightly below V_{ref}. This results in the V_{ref} is almost equal to minimum value of V_{FB} but the average V_{FB} is $V_{ref} + \frac{V_{ramp}}{2}$. COT control switches from CCM to PFM at light loads seamlessly. In PFM mode, the V_{FB} decreases ad the switching frequency reduces and ramp density decreases and shape becomes flatter. This brings V_{FB} closer to V_{ref}. Figure shows the variation on the FB ramp with different loads.

The V_{FB} ramp alters as the load changes from critical CCM mode to no-load; as the load decreases, $V_{FB_{avg}}$ decreases.So as it changes from CCM load to no load to , the load regulation increases in the PFM mode when the load decreases. The relationship between the $V_{FB_{avg}}$ and the VOUT could be simplified as:

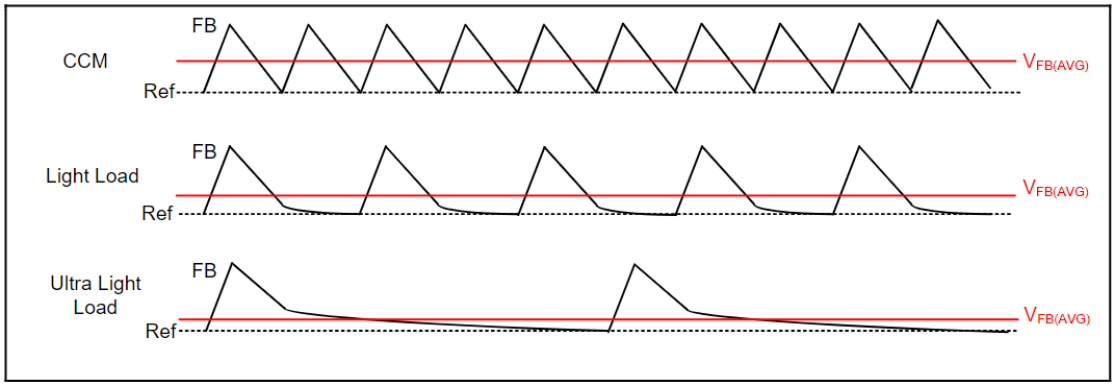

Figure 2.7: Feedback Ramp Under Different Load Conditions [5]

$$V_{out} = \frac{R_1 + R_2}{R_2} * V_{FB_{avg}} \tag{2.8}$$

So the ΔV_{out} when the load changes from CCM to no-load condition could be estimated as:

$$\Delta V_{out} = \frac{R_1 + R_2}{R_2} * V_{FB_{avg}} \approx k * \frac{R_1 + R_2}{R_2} * V_{ramp} \tag{2.9}$$

here k is difference between $V_{FB_{avg}}$ during CCM versus PFM — usually around 0.25. Reducing R1 and R2 reduces k. VRAMP is the amplitude of the FB ramp.

When ESR is dominant in the feedback:

$$V_{ramp} = \frac{R_2}{R_1 + R_2} * \frac{1 - D}{\frac{L}{R_{ESR}}} * T_{sw} * V_{out} \tag{2.10}$$

If the external ramp from R_{fb} and C_{fb} dominates the FB ramp:

$$V_{ramp} = \frac{1-D}{R_{fb} * C_{FB}} * T_{sw} * V_{out} \tag{2.11}$$

Where t_{sw} is the switching period, D is the duty cycle period, and L, RESR are power stage inductor an dcap esr and $R_{FB} and C_{FB}$ are feedback ripple network generator refer to components.

2.3.3. Feedback Ramp and Line Regulation

COT due to its pseudo-fixed frequency operation in CCM mode provides relatively fix frequency. The V_{FB} changes as inductor current changes. $V_{FB_{avg}}$ is worst in CCM and improves with light load conditrions as $V_{FB_{avg}}$ is closer to V_{ref}.

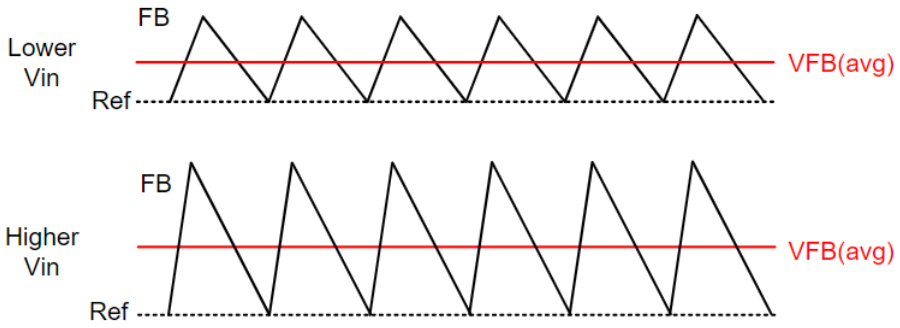

Figure 2.8: Feedback Ramp Under Different Input Conditions [5]

We know:

$$V_{FBavg} - V_{ref} \approx \frac{1}{2} V_{ramp} \tag{2.12}$$

As V_{IN} increases, V_{FBavg} increases as the duty decreases for a V_{out} to increase as shown in figure:

V_{OUT} vs.V_{IN} in CCM mode is expressed as:

$$\Delta V_{out_{ESR}} = \frac{1}{2} * \frac{\Delta D}{\frac{L}{R_{ESR}}} * T_{sw} * V_{out} \tag{2.13}$$

$$\Delta V_{out_{RC}} = \frac{1}{2} * \frac{R_1 + R_2}{R_2} * \frac{\Delta D}{C_4 * R_4} * V_{OUT} * T_{SW} \tag{2.14}$$

Where $\Delta V_{out_{ESR}}$ represents changes in V_{OUT} with different ESR capacitors at the output, and $\Delta V_{out_{RC}}$ represents changes in V_{OUT} based on external RC compensation with ceramic capacitors due to the VIN change.Generally, a smaller FB ramp results in better line regulation.

2.4. MATLAB Modelling of Constant ON Time with Bottom Detection Control for Buck Converter

Constant ON time converter which is a fixed on-time with bottom detection control having ripple injection has become very attractive due to practical usage and realization of ceramic capacitor solution for output while keeping ultra fast transient response.

Figure 2.9[22] depicts a block diagram of COT with ripple generation network across L. Generated ripple is injected to feedback node. This is then compared at the comparator by passing ramp through a dc blocking capacitor.The feedback voltage is compared to a known reference and a fixed ON time generator generates a pulse which switches ON the High side. The output voltage rises and is replicated as the rising ramp at feedback node. The voltage ripple ΔV_{FB} is given by:

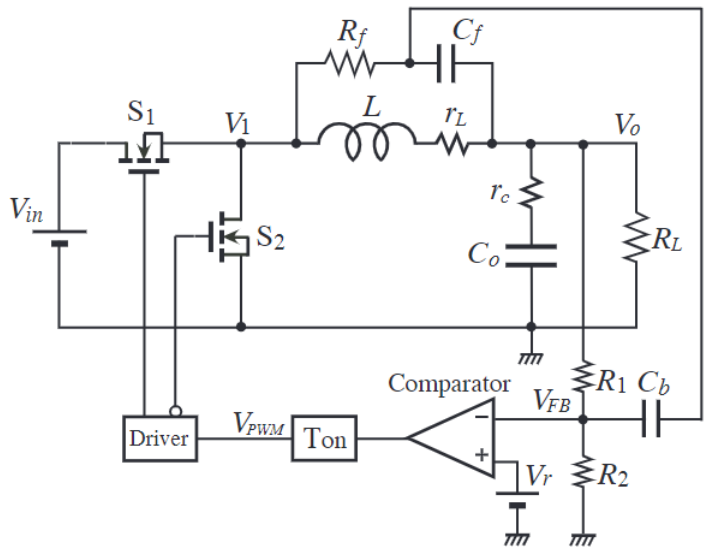

Figure 2.9: COT diagram for MATLAB modelling

$$\Delta V_{out_{ESR}} = \frac{V_{IN} - V_o}{C_f * R_f} * T_{ON} \tag{2.15}$$

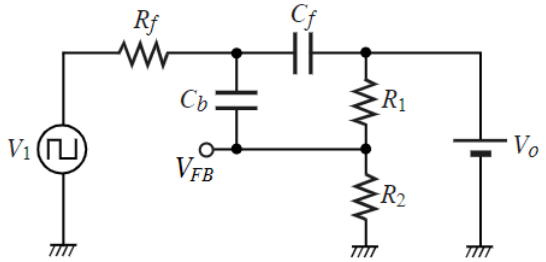

Figure 2.10: Equivalent Circuit of Feedback Circuit

Figure 2.10 [22] shows a small signal equivalent under steady state of operation. In Figure 2.10, V1 is node voltage of switches. Applying averaging method on node

voltage an d branch current on one switch period, a conventional linear circuit is able for lower frequency range. Average value of V1 can be expressed as V_1 - D* V_{in} with D being the duty cycle. Assuming a ideal comparator and small injected ripple, V_{FB} V_{ref} are considered equal. The transfer function from Vo to Vr is derived using principle of superposition by assuming $V_1 = 0$ and $V_o = 0$ respectively.

When $V_o = 0, V'_{FB}$ is given as:

$$V'_{FB} = H_1(s) * D * V_{in} \tag{2.16}$$

where $H_1(s)$,

$$H_1(s) = (\frac{C_b * R_{12}}{C_f R_f C_b R_{12} s^2 + (C_f R_f + R_{12} C_b + C_b R_f)s + 1}) * DV_{in} \tag{2.17}$$

When $V_1 = 0, V"_{FB}$ is given as:

$$V"_{FB} = H_2(s) * V_o \tag{2.18}$$

here R_{12}:

$$R_{12} = \frac{R_1 R_2}{R_1 + R_2} \tag{2.19}$$

where $H_2(s)$,

$$H_2(s) = (\frac{C_f R_f C_b R_1 s^2 + (C_f R_f + C_b R_f)s + 1}{C_f R_f C_b R_1 s^2 + [C_b R_1 + \frac{R_1}{R_{12}}(R_f C_f + C_b R_f)]s + \frac{R_1}{R_{12}}}) * V_o \tag{2.20}$$

$V_r = V_{FB} = V'_{FB} + V"_{FB} = H_1(s) * D * V_{in} + H_2(s) * V_o$

The transfer function from ΔV_o to ΔD is expressed as:

$$\frac{\Delta D}{\Delta V_o} = \frac{H_2(s)}{H_1(s) * V_{in} s} \tag{2.21}$$

The transfer function has infinite dc gain since the comparator is considered to be ideal. Thus, there is no steady-state error. Assuming that the dc blocking capacitor Cb=∞, the equation is expressed as below:

$$\frac{\Delta D}{\Delta V_o}|_{C_b=\infty} = \frac{-R_f}{R_1 V_{in}}(1 + sC_f R_1) \tag{2.22}$$

Due to fixed ON time, the ON time pulse cannot change even when output changes. there is a delay given as:

$$H_d(s) = e^{-sDT_{ON}} \tag{2.23}$$

The transger function of the power stage is given as $G_{dv}(s)$ and is derived using state space-averaging method:

$$G_{dv}(s) = \frac{V_{in}(1 + \frac{s}{ESR})}{1 + 2\delta\frac{s}{\omega_o} + (\frac{s}{\omega_o})^2} \tag{2.24}$$

where δ:

$$\delta = \frac{\sqrt{\frac{L_o}{C_o}} + R_L(r_{DCR} + r_{ESR})\sqrt{\frac{C_o}{L_o}}}{2R_L\sqrt{1 + \frac{r_{DCR}}{R_L}}} \tag{2.25}$$

$$\omega_o = \sqrt{\frac{1 + \frac{r_{DCR}}{R_L}}{L_o C_o}} \tag{2.26}$$

$$\omega_{ESR} = \frac{1}{C_o r_{ESR}} \tag{2.27}$$

The open loop transfer function of the the controller is given as:

$$G_{Eopen}(s) = \frac{\Delta D}{\Delta V_o} H_d(s) G_{dv}(s) \tag{2.28}$$

$$G_{Eopen}(s) = (\frac{C_b * R_{12}}{C_f R_f C_b R_{12} s^2 + (C_f R_f + R_{12} C_b + C_b R_f)s + 1}) G_{dv}(s) e^{-sDT_{ON}} \tag{2.29}$$

$$= \frac{C_b * R_{12}}{C_f R_f C_b R_{12} s^2 + (C_f R_f + R_{12} C_b + C_b R_f)s + 1} \frac{V_{in}(1 + \frac{s}{ESR})}{1 + 2\delta\frac{s}{\omega_o} + (\frac{s}{\omega_o})^2} e^{-sDT_{ON}} \tag{2.30}$$

The loop transfer function is written in MATLAB with the following component values:

Parameter	**Value**	**Parameter**	**Value**
V_{in}	18V	R_{ESR}	$\leq$ 10mΩ
V_{out}	1V	C_b	250pFΩ
T_{ON}	$\approx$ 100ns	R_1, R_2	100K Ω
L	500nH Ω	R_f	25K Ω
R_{DCR}	17mΩ	C_f	1.5nFΩ
C_{out}	66uFΩ	C_b	250pFΩ

Table 2.1: COT Converter Parameters Used in MATLAB Model Simulation and Transistor Level Schematics For Stable Operation

The MATLAB code for this model is given in Appendix A.

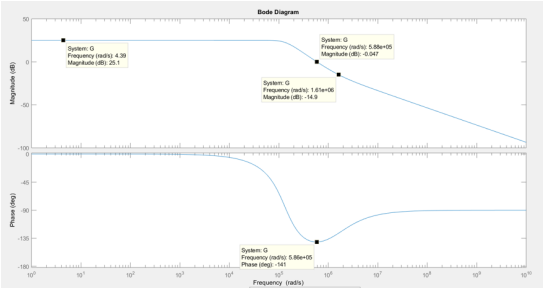

Figure 2.11: Plant Transfer Function - Mag: 25dB, BW: 93.5KHz; PM: 40°

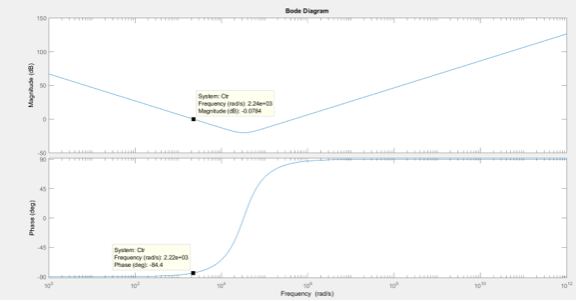

Figure 2.12: Controller Transfer Function - Mag: 60dB, PM: 116°

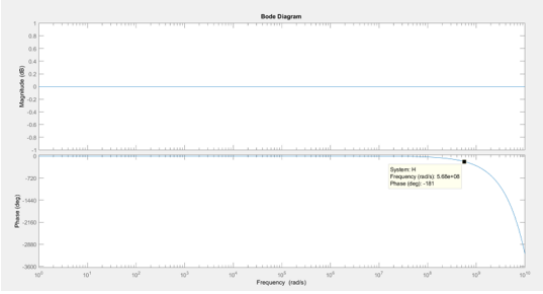

Figure 2.13: ON Timer Transfer Function

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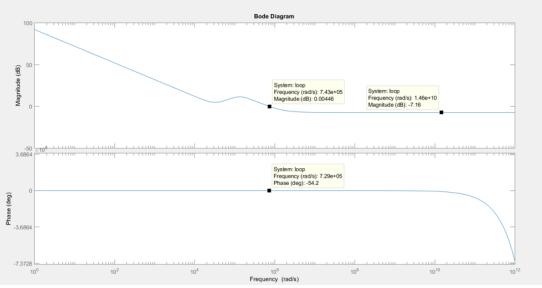


Figure 2.14: Complete Loop Transfer Function - Crossover Frequency: 118KHz; PM: 126°

Chapter 3

DESIGN IMPLEMENTATION OF INTEGRATED CIRCUIT SYSTEM

3.1. Top Level Architecture

The main challenge for the proposed converter is to develop a solution which can respond fast and stably to input and output voltage an current transients while maintaining high efficiency at over entire dynamic range without being affected by radiation effects which induce parameter shifts in device characteristics. The switch node buck regulator is designed provide a current in range of 100mA to 10A at 1V output with state of art efficiency. The input dynamic range is from 8V to 18V which results in a very high conversion ratio of 12.5% and 5.56% of output to the input. The effort is to try to switch the converter at as high frequency as possible in order to reduce the passive component device sizing and reduce area of integration. However, the limit on size of inductor due to concern about radiation in ferrite core and the minimum ON time, switching frequency is not an independently controlled variable. Hence, its difficult to design COT converter for very high frequency at low output voltages. GaN power stage is used with CMOS based driver, feedback loop and other peripherals.

The CMOS IC is divided into two domains; 18V driver and level shifter domain, 1.8V controller domain. An intermediate 5V is used for the low side driver and external bootstrap circuit. The logic and control circuitry operates at 1.8V. The on-chip 1.8V and 5V LDOs generate the supply rail voltages. A proper start-up sequence is designed for soft start of the chip. This enables all the biases and reference voltages to be generated internally. Thus the entire chip runs only on a single V_{in} input. The

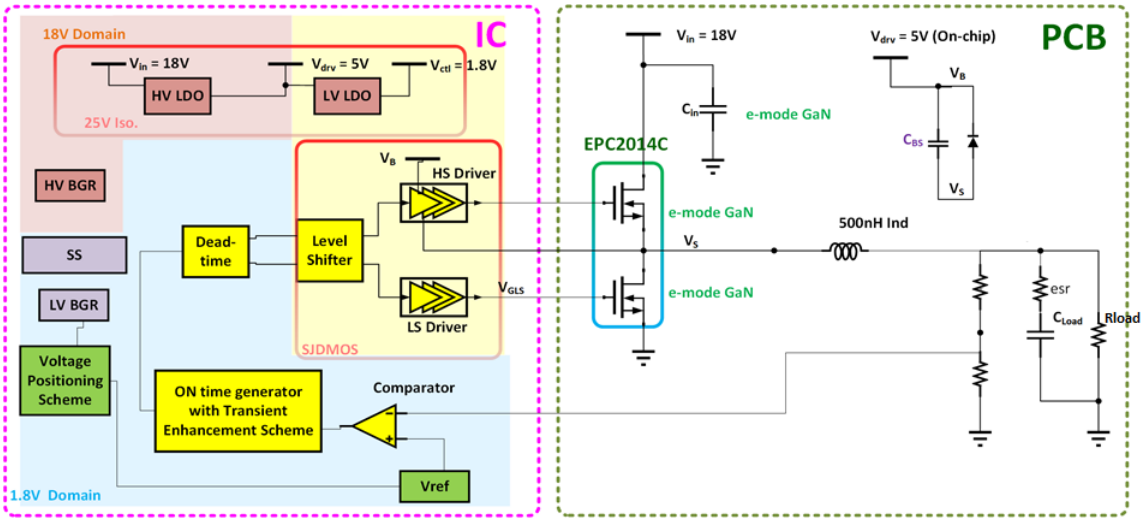


Figure 3.1: Complete Constant ON Time Top-Level System Architecture

low-side gate driver is implemented at 5V. The high-side devices operate on a 5V supply rail over the 18V supply. The accuracy of this ripple based circuit is improved by adding a V_{REF} positioning circuit and using a transient enhancing adaptive ON time circuit for faster droop recovery.

Design challenges, innovation and the solution targeted in this work are shown in the Table. There is an optimal division of functionality present between GaN and silicon CMOS. The system is designed to improve the efficiency at large conversion ratio with the CMOS gate driver architectures to control the GaN power devices.

Design Challenge	**Innovation and Solution**
V_{gs} swing of 5V for GaN	Super Junction Device based Driver
Transient response	Adaptive ON time circuit
High conversion, Low duty cycle operation	Constant ON Time architecture
Single 18V Supply solution	Two integrated linear regulators
Reducing steady state ripple error	Voltage Positioning scheme
Shoot through protection for Power FETs	Driver integrated V_{gs} sensing based shoot through protection

Table 3.1: Overview of Design Challenges and Solution

Based upon the selection of EPC power devices as well as the CMOS process technology of XFAB 180nm SOI process, Figure 3.1 depicts the complete DC-DC power converter. CMOS based circuitry is used in controller and driver. The feedback compensation doesn't have any external components. However there are some capacitor and resistors used for feedback voltage ripple from induct to comparator. The out put filter is implemented off-chip. Since the requirements of the POL circuit is to operate in radioactive environment, the inductor cannot have a ferrite core as it induces polarisation under radiation. So a air core inductor has to be used. This reduces the value of inductor that can be used in the design. This doesn't help in use of high frequency operation.The power stage architecture is chosen based upon the design equation discussed in this chapter. The single-stage power architecture has smallest area as it ha one capacitor an inductor and just two power FETs. The sub-blocks of the Constant ON time controller stage are discussed in this chapter. The COT has advantages of simple single loop control, less off-chip components, fast transient response as frequency is variable, very robust to jitter induced variations in output, good noise margin due to digital logic control, better line and load transients, simple stability constraint based on ESR and feedback ripple, loop gain variation due to input voltage is low. Since switching frequency is not very high, the loop bandwidth cannot is very high which might slow down the system. The chip utilizes internal supplies to scale down input 18V to 5V and 1.8V. The chip includes a band-gap reference circuit, tunable deadtime control, comparator for feedback and reference comparison, adaptive on time one shot generator, High-side and low-side driver circuit, digital logic gates and flip-flop for logical operation based of comparator decision. The 180nm process is proven to be inherently rad hard to upto 700 Mrads of radioactive total ionizing dose[18]. This is because of thin gate oxide with thickness less than 5nm which enables active tunneling of electrons from channel to

gate.

3.2. CMOS Driver and Controller design

The CMOS driver and controller are integrated in a single IC capable which drives a GaN with cap load (C_{iss}) of 200pF-300pF for 200KHz to 1MHz of switching frequency. The Cap load is almost $\frac{1}{10^{th}}$ of that compared to a Si load due to use of direct band-gap semiconductor. The PVT corner simulation is undertaken to ensure individual and system level operation of the converter. The BGR generates reference voltage which is used for ONE shot trigger refernce, as input for voltage positioning scheme and for biasing the LDOs. The comparator used is high speed comparator with very less steady state offset. The design innovations and challenges used in this work are summarized as follows:

- Integrated buck converter topology with minimum off chip components for small form factor.
- Utilizing high current handling capacity of GaN devices for power stage and easy implementation of control circuitry on CMOS.
- Selection of thin gate-oxide SOI transistors for immunity to radiation induced gate threshold voltage shift.
- Use of Super Junction FETs fro driver design which simplifies the design and enables high voltage tolerance across the drain-source terminal.
- Voltage positioning scheme for for accurate reference modulation to reduce the steady state error between nominal output voltage due to ripple and the expected output voltage.
- Adaptive ON time for faster output voltage droop recovery due to load transient.

- A Shoot through protection circuit for preventing Power FET burn out while implementing minimum deadtime for max efficiency in GaN switching.

3.3. Super Junction Based CMOS Driver

Gallium Nitride (GaN) based high electron mobility transistors with low temperature coefficient and lateral structure offer very low RDS(on), lower total gate charge etc. This makes them very attractive for use in high power, high frequency switching applications[6]. GaN has also successfully demonstrated low susceptibility and inherent robustness to radiation induced material and performance degradation and is emerging as a workhorse in space electronics industry. However, GaN poses challenges in gate driver circuit design as they are very sensitive to gate drive pulse voltage and shape. A low gate drive drastically increases the on resistance and degrades the overall efficiency whereas a high gate drive might rupture the gate[6]. The gate driver is the block on chip having direct interaction with the GaN switches on board. Hence it becomes imperative to design a robust driver which generates gate pulses tightly controlled within the operating specifications across all PVT and radiation induced variations.

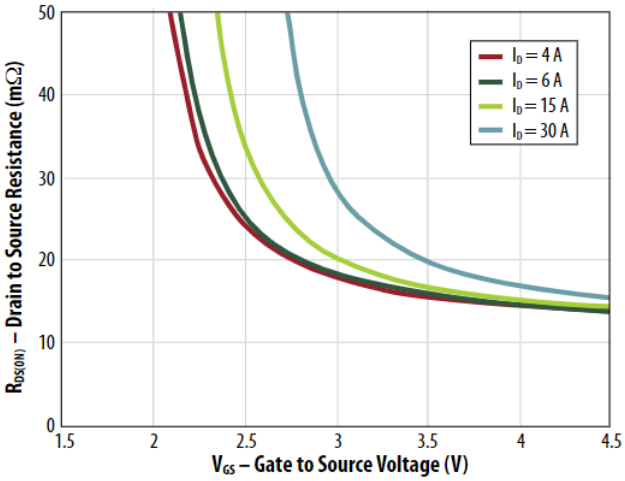


Figure 3.2: Gate-Source Voltage of GaN vs $R_{DS_{ON}}$

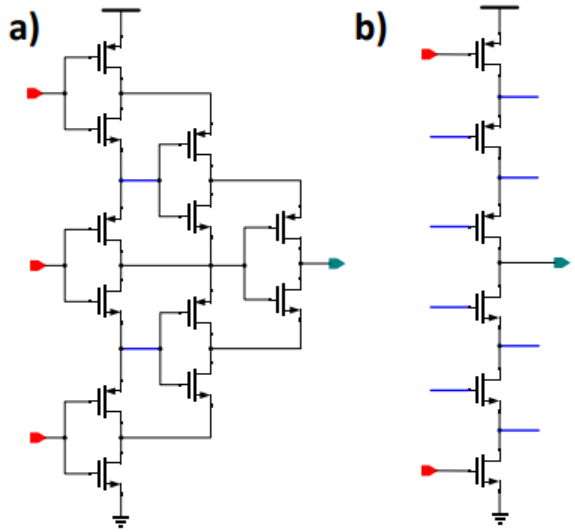


Figure 3.3: Stacked GaN Driver Design a) House of Cards Driver, b) Simple Stack Driver

Current technology from EPC requires 4.5V to 5V for gate drive for GaN device to achieve the low enough conduction loss. Since for current low-voltage sub-micron silicon technologies, 5V is beyond the power supply limit for core transistors, a high-voltage output gate driver is needed. Fig. 3.3 shows the commonly used high-voltage

gate driver with low V_{gs} thin gate oxide devices called as House-of-Card cascoded structure. In this structure high voltage swing is propagated along inverter stages. The power supply is divided into multiple voltage domains as shown by the capacitive divider and inverter at each voltage domain is driven by shifted gate signals. However, complex biasing network is needed for all blue lines in (b).

Alternatively,Super-Junction based driver provides a much simpler design and does not need scaling with changes in gate drive voltages for different GaN. The novel Super Junction (SJ) DMOS devices from XFAB 180nm process, as shown in Figure 3.4[3], can eliminate the need for a relatively complex stacked driver, while having immunity to SEBs, and high enough TID tolerance.

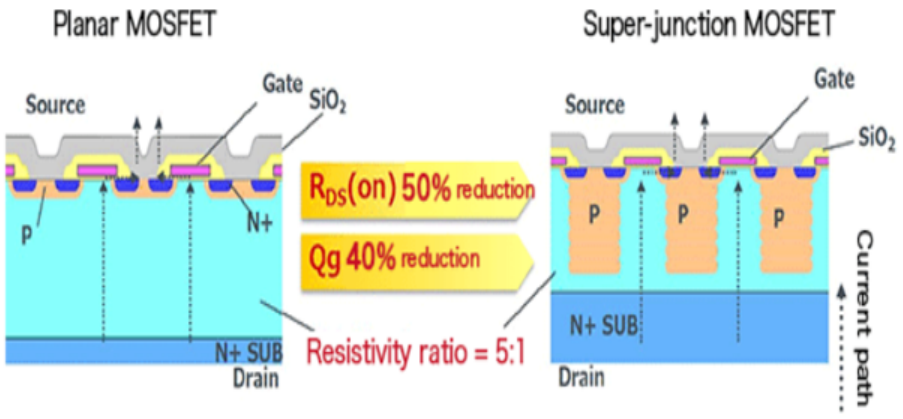


Figure 3.4: Cross Section of Conventional MOSFET and SJDMOS

The lateral device construction of SJDMOS with the quasi-charge neutral diffusion region of this devices enables high Drain-Source voltage handling capabilities up to 200V unlike conventional LDMOS. These devices are similar to "low-voltage" CMOS devices that do not have PN junction type of isolation for high voltage applications, do not exhibit SEB or SEL by their nature. The isolation is achieved by the epitaxial depletion region. The Planar MOS has a low doped thick epi region for high voltage

blocking capabilities[3]. The thick epi region results in higher drain to source voltage. The ON resistance remains high due to low doping profile. At higher drain-source resistance, resistance of epitaxial layer dominates the channel and substrate resistance. By adding pillars of p region in the SJDMOS, the length of diffusion region for the carrier is effectively decreased. Also a thicker reverse biased region allows higher blocking voltage with thinner epi layer. This facilitates use of higher doping profile for the same blocking voltage. In SJDMOS, blocking voltage is solely a function of epi thickness.The electric field is much uniformly distributed in the epi region[3]. The larger PN junction reverse bias junction allows higher reverse recovery current while transistor is switched off. So the charge from the channel is removed at a much faster pace. Thus lesser reverse recovery time allows high frequency operation. High gate charge also increases switching loss at higher frequency in Planar MOS which is lowered in SJMOS due to almost 50% reduction in gate charge[3].

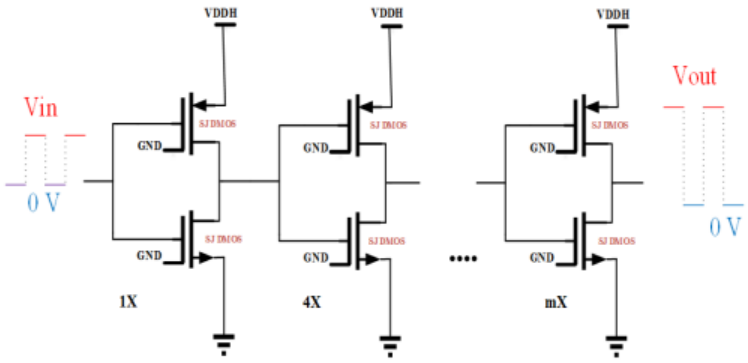


Figure 3.5: Schematic Diagram of SJ DMOS GaN Driver

Although SJ DMOS driver is fairly simple in construction and highly reliable for high voltage applications, it consumes more area and power in comparison to stacked gate drivers for the same drive capability due to the large $R_{ds_{on}}$ and capacitance of the MOS structure.

3.3.1. Driver Circuit - Sizing

The driver circuit using SJDMOS is a simple series chain of inverters of increasing size. The PMOS/NMOS (P/N) sizing is based on rise time, falltime, propagation delay, Fan-out parameters.

Optimal Fan-out for a driver is achieved in the following calculation:

Consider the chain of inverters as shown below.

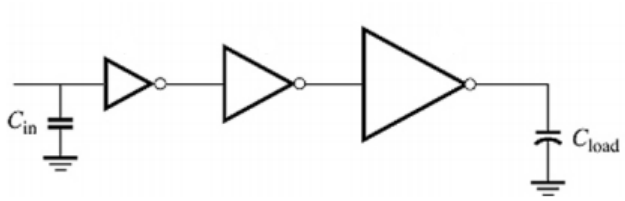


Figure 3.6: Driver Inverter Chain

The inverter delay:

$$t_{pi} = t_{po} * (1 + f_i)$$

$$t_{pi} = t_{po} * (1 + \frac{C_{Li}}{C_{gi}})$$

where; f_i = fanout of ith inverter.

C_{Li} = Final load capacitor of i^{th} inverter.

C_{gi} = gate capacitance of i^{th} inverter.

For series of N inverters, overall delay:

$$t_p = \sum_{i=1}^{N} t_{pi}$$

$$t_p = N * t_{po} + \sum_{i=1}^{N} \frac{C_{Li}}{C_{gi}}$$

t_p is equal when all f_i are equal.

$$f^N = \frac{C_L}{C_{in}}$$

$$t_p = N * t_{po} * (1 + f)$$

$$f = (\sqrt{\frac{C_L}{C_{in}}})^{\frac{1}{N}}$$

Optimum number of inverters stages:

$$N = \frac{ln(\frac{C_L}{C_{in}})}{ln(f)}$$

Therefore,

$$t_p = N * t_{po} * (1 + f) = \frac{ln(\frac{C_L}{C_{in}})}{ln(f)} * t_{po} * (1 + f)$$

Differentiating w.r.t 0, we get:

$$f = 3.6 \approx 4$$

Number of stages:

$$N = \frac{ln(\frac{C_L}{C_{in}})}{ln(f)} = \frac{ln(\frac{220pF}{1pF})}{ln(4)} = 3.891 \approx 4$$

where, $C_{in} \approx 1pF, C_{load} = 220pFGaN$

Optimal Sizing is based on rise time an fall time requirements and process constants $K_{n,p}^{`} = \frac{W*\mu_o*C_{ox}}{L}$:, ratio of mobility

P/N ratio of $\approx 1.4 - 1.5$ is found to give minimum propagation delay and sufficient rise, fall time to charge the load cap.

3.3.2. Validating Driver Size Through Frequency Simulation.

The Driver shown below is tested for its ability to drive the required load.The on resistance of the PMOS and NMOS which play a crucial role in driver functionality are simulated and tested for all the corner and temperature sweep.

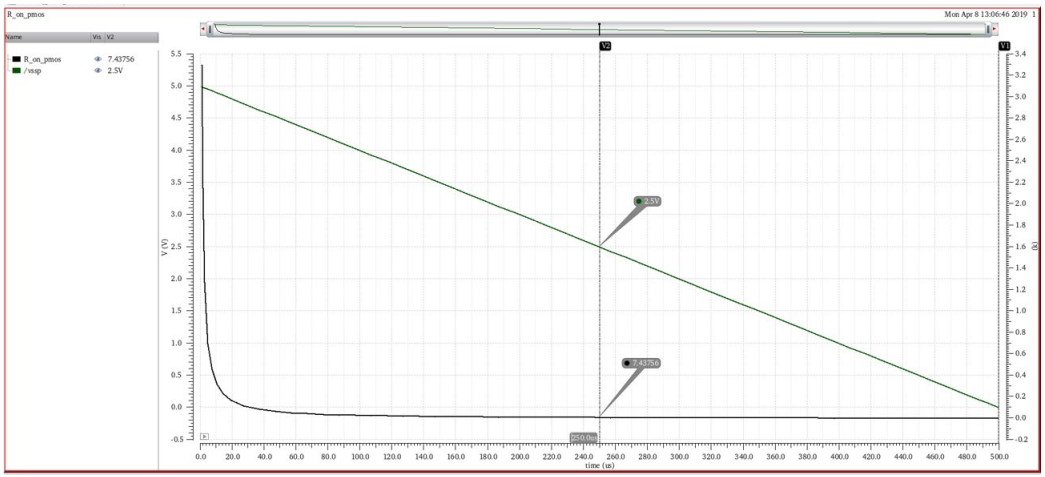


Figure 3.7: Average ON Resistance of PMOS for Gate Voltage Varying from 0-5V.

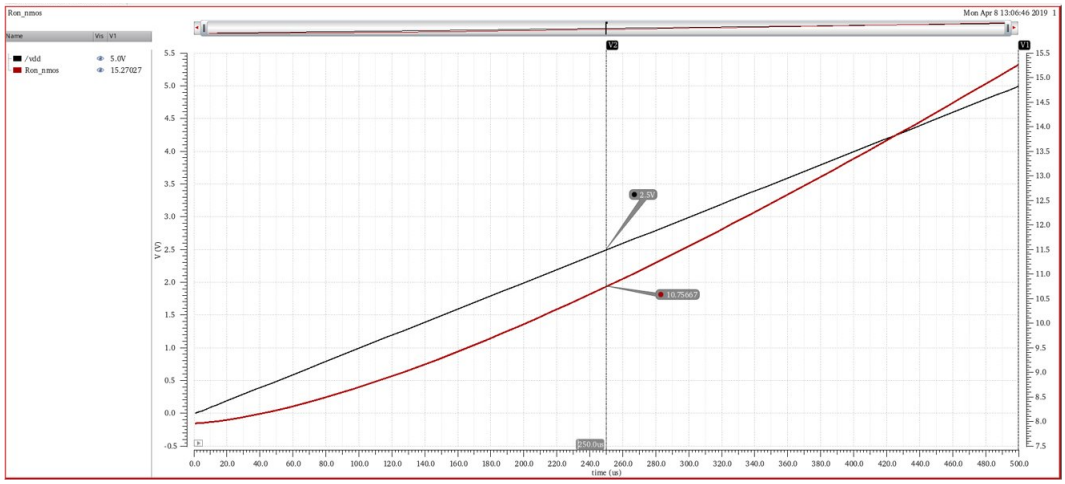


Figure 3.8: Average ON Resistance of NMOS for Gate Voltage Varying from 0-5V.

The result values obtained from the simulation confirm with datasheet values.

This result is used to find the max operating frequency for the SJ-MOS driver.

Rise time: @1MHz= 8.78nS ; Required $R_{ON} = \frac{8.78n}{220pF} = \mathbf{39.9}\ \Omega$

Average R_{ON} **from Figure 3.7 =** $\mathbf{36}\Omega$

Thus, last stage PMOS can successfully drive the GaN at 1MHz.

Fall time: @1MHz= 5.74nS ; Required $R_{ON} = \frac{5.74n}{220pF} = \mathbf{10.75}\ \Omega$

Average R_{ON} **from Figure 3.8 =** $\mathbf{11.03}\Omega$

Thus, last stage NMOS can successfully drive the GaN at 1MHz.

Based on above results, it is concluded that:

- The Driver is sized according to Table 3.2 values and validated to function up to 1MHz and 120° Celsius temperature across all corners.
- The driver is also tested for 2 and 5 MHz in typical corners and performs adequately.

Stage	PMOS	NMOS	Multiplier
1	28μ	20μ	4
2	112μ	80μ	4
3	448μ	320μ	4
4	1792μ	1280μ	4

Table 3.2: Device Sizes

Fig 3.9 shows the driver schematic with shoot through protection circuit implementation. Gate voltage of SJ MOS is monitored continuously. If LS FET's gate voltage increases, HS control switch is pulled down. HS can then only have a com-

plementary signal to LS. Vgs variation of SJ NMOS is in range of 200mV for current pulse from 1A $\rightarrow$ 10A

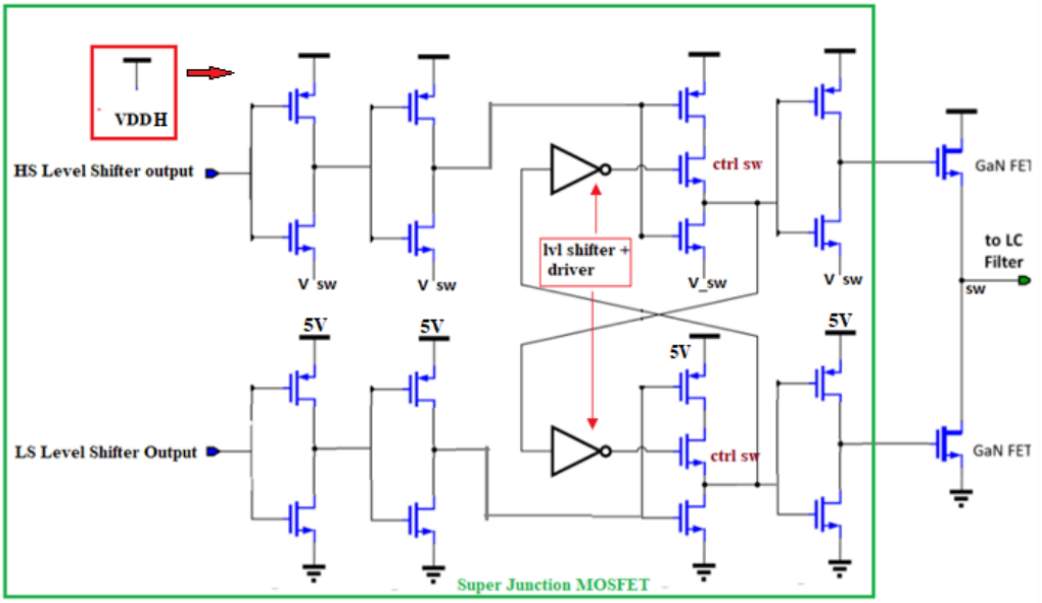


Figure 3.9: SJMOS Driver With Shoot Through Protection Circuit

Fig 3.10 shows that at zero deadtime, shoot through occurs with 22A current through GaN Reduces GaN lifetime increases loss. Fig 3.11 shows that at with shoot through protection, a small non overlap introduced within driver output waveform. Minimum deadtime (<2ns) can be used to improve GaN efficiency.

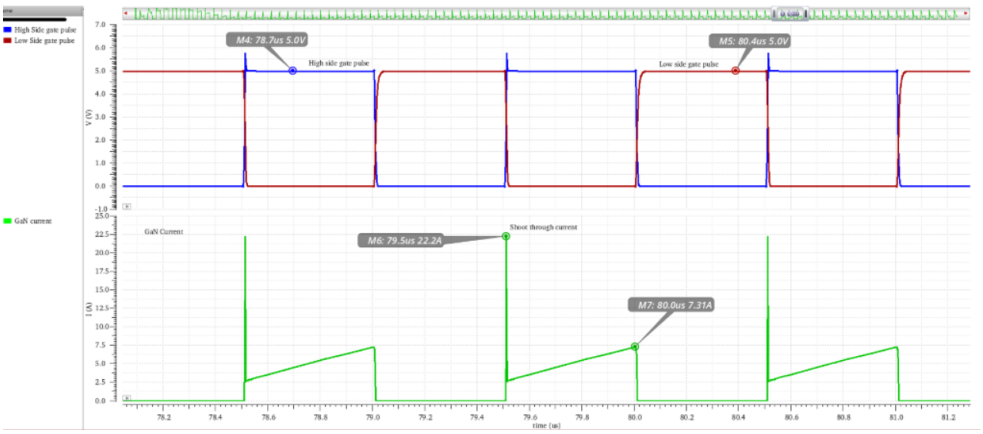


Figure 3.10: Driver Shoot Through Current at 0 Deadtime Without Protection

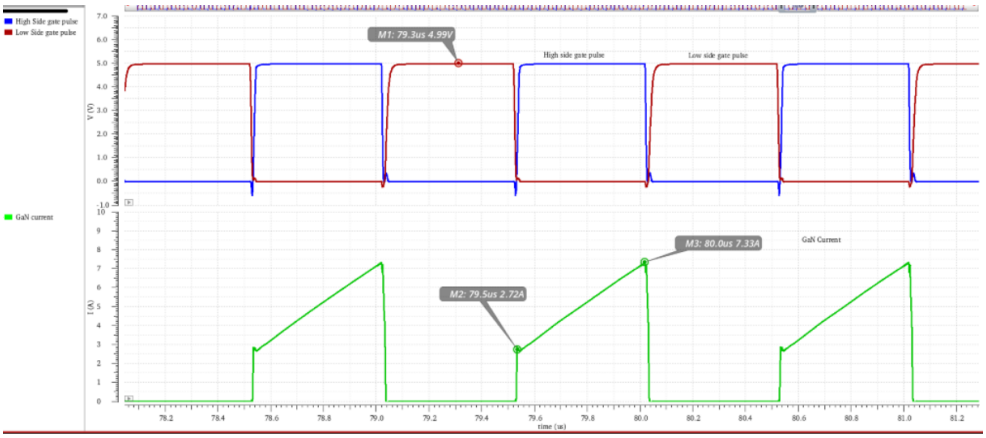


Figure 3.11: Driver Shoot through Current at 0 Deadtime With Protection

LS driver switches between 0-5V. High Side driver switches between 18-23V. HS driver is supplied by bootstrap ckt. Bootstrap cap is 80nF to be able to supply Driver, level shifter with big gate cap load. Droop at bootstrap is ensured to be less than 5%. Deadtime achieved is 6-7ns. Reverse body conduction during deadtime results in power loss and driver falls below 0V[25].

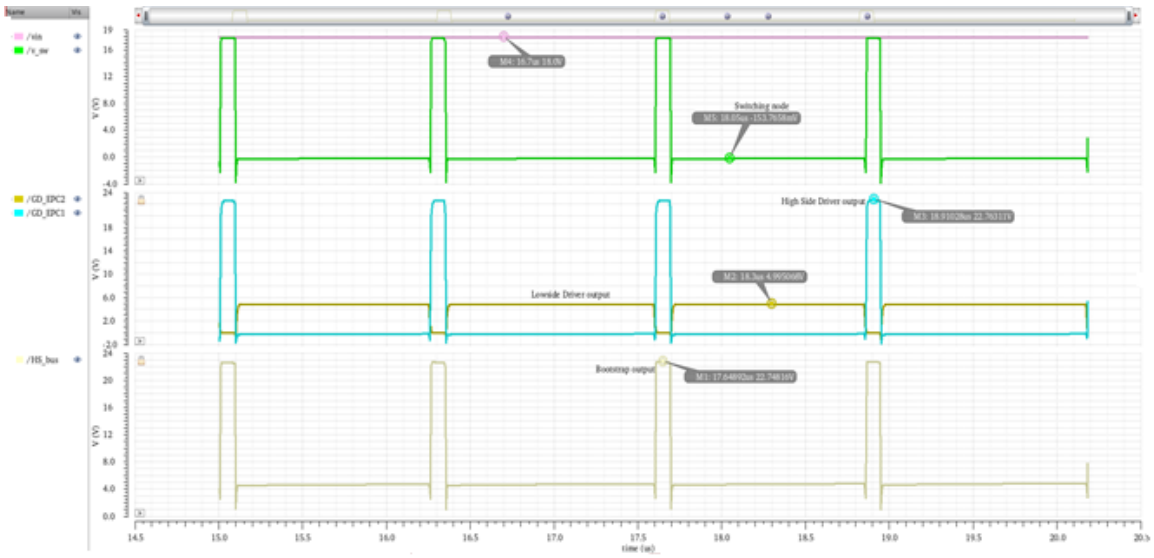


Figure 3.12: Driver and Bootstrap Waveforms

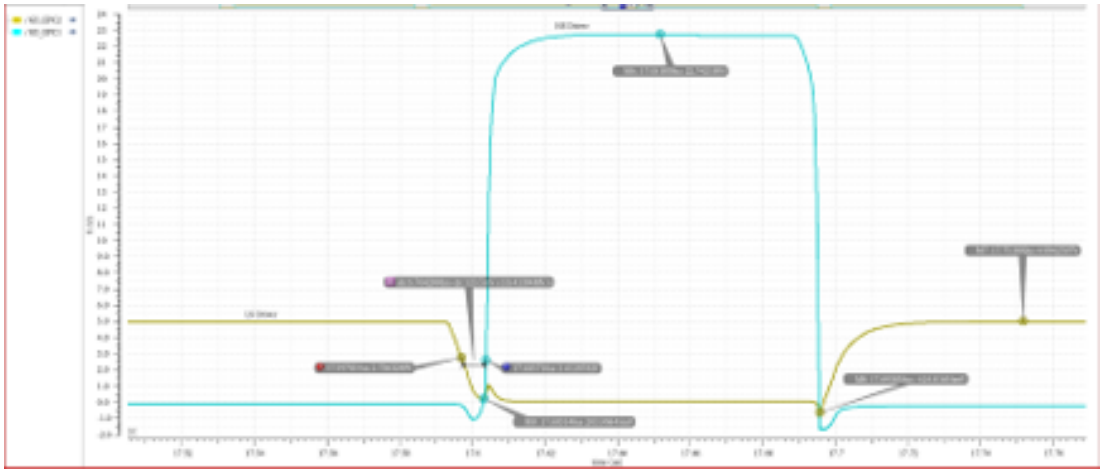


Figure 3.13: Deadtime at Driver Output

In Fig 3.12, bootstrap, HS Driver and LS Driver wave forms are shown. The negative going peak reduces efficiency of Gan and results in loss of efficiency. An external diode must be connected anti-parallel to GaN if the reverse voltage at Gan output is comparable to the converter output voltage.

3.3.3. Selecting Gate Resistance

EPC recommends to begin with ideal resistor of values less than 5Ω and simulate for optimum results iterative [6].Following factors are considered for selecting gate resistance. The final sims were carried out with 0.5Ω resistor for both pull-up and pull-down branch of the output stage.

- Gate resistor influence the switching frequency. The RG value must be added to the R_ON value of the Output stage PMOS/NMOS for validating frequency operation.
- RG is also crucial to preventing gate ringing and instability due to $\frac{dv}{dt}$ and common source inductance.
- A smaller RG will result in high $\frac{dv}{dt}$ induced ringing at gate causing high switching loss and risk of Miller turn-on.
- A smaller pull down RG (NMOS side) is recommended to provide stronger pull down for a stronger gate drive.

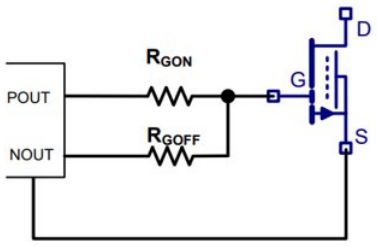


Figure 3.14: Preferred Approach for Gate Resistor Implementation.

- RG less 0.3Ω displayed VGS undershoot and deadtime conduction loss due to increased deadtime.

- RG shoud also have very less inductance if using off-chip resistor to reduce gate inductance.

Note: Clamp circuit is avoided for GaN as to keep intact the advantages of GaN related to low input capacitance. If Clamp is used, RG should be altered taking the new total capacitance into account.

3.4. Methods to Improve Accuracy of Ripple Based Converter

3.4.1. Adaptive ON Time Generator

To minimize the steady state switching frequency variation when the input voltage and output voltage are varied, the turn-on time Ton of power transistor in each switching period is designed to be a function of input voltage Vin and output voltage Vout [15].

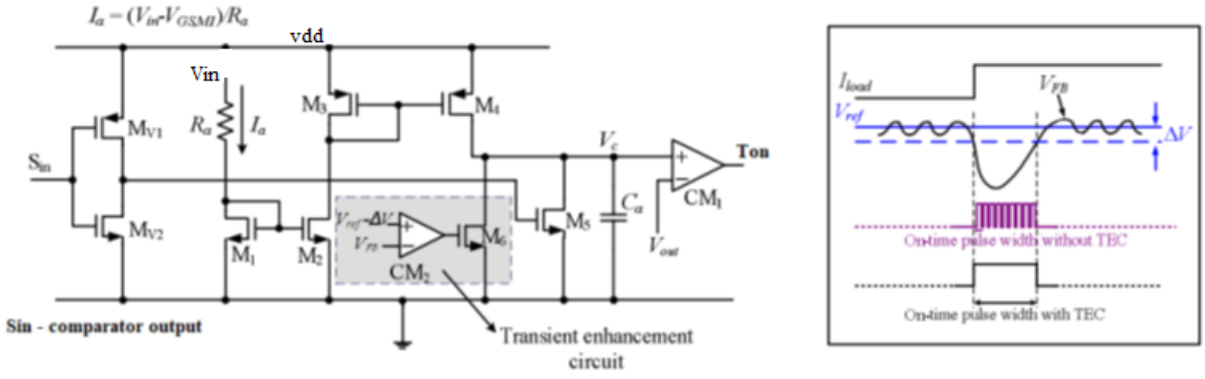


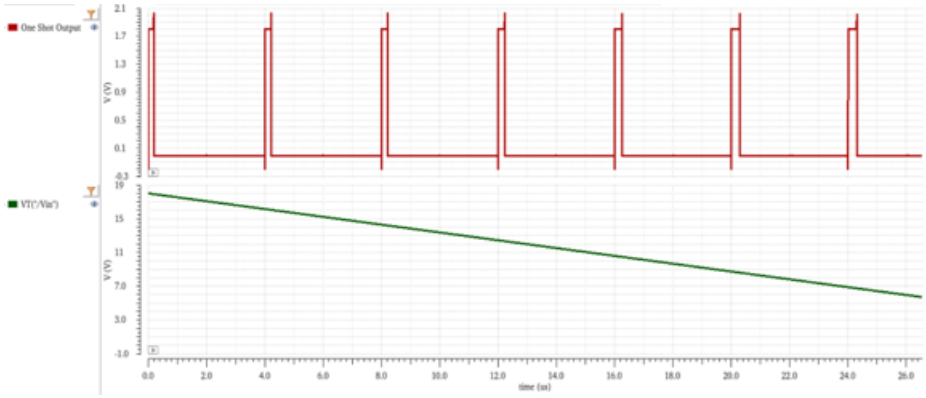
Figure 3.15: Adaptive ON Time With Transient Enhancement Circuit

As shown in figure, variable current source Ia that is dependent on Vin is used to charge the capacitor Ca. The charging time Tc required for charging capacitor Ca from zero state to output voltage Vout is therefore linearly proportional to Vout/Vin. To achieve the required turn-on time, an adaptive on-time signal generator circuit is

shown. The basic operation of this circuit is to generate the delay-time, and consequently the on-time pulse of HS FET is produced. The variable current source Ia is realized by impressing Vin-VGS,M1 across Ra and is mirrored through M1, M2, M3, and M4 to charge the capacitor Ca. Hence, the turn-on time Ton of MP can be expressed as

$$T_{ON} = \frac{V_{out} * R_a * C_a}{V_{in} - V_{GS,M1}}$$

where VGS,M1 is the gate-source voltage of M1. Although the above switching frequency varies when Vin changes, the frequency variation is less than 10switching frequency for Vin varied around 1.8V.



V_{IN}	T_{ON}
18V	197ns
16.1V	210ns
14.4V	224ns
12.5V	241ns
10.6	261ns
8.5V	285ns
7.0V	314ns

Figure 3.16: ON Time Variation

Hence, the proposed adaptive on-time signal generator is sufficient to solve the significant switching frequency variation problem. Moreover, to further enhance the transient response in a large step-up load change, a transient enhancement circuit

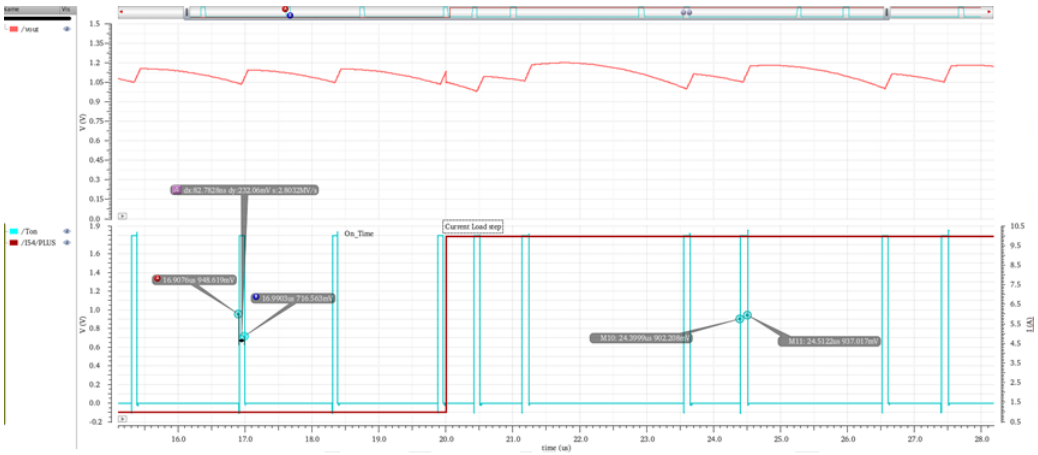


Figure 3.17: Transient Enhancement Circuit Operation

	1A Load	**10A load**
T_{ON}	80ns	115ns

Table 3.4: ON Time Variation With Transient Enhancement Circuit

(TEC) is added to the proposed adaptive on-time generator as shown in Fig. 3.15 A comparator CM2 is used to determine the operation mode of the adaptive on-time generator. For VFB > Vref – Δ V (Δ V is a small bias voltage and VFB is feedback signal), the output state of CM2 is low, and consequently M6 is turned off. The proposed adaptive on-time generator works normally; For VFB ≤ Vref – ΔV (VFB drops during a large step-up load change), the output state of CM2 is in a transition from low to high, M6 is therefore turned on, and the capacitor voltage VC is pulled down to low state. Thus, the adaptive on-time generator continues to output a wide on-time pulse, and the power transistor MP is turned on to provide the required current for output load until Vout is pulled back to the desired value as shown in Fig. 3.17. As seen in Fig 3.17,when the Vout droops by 50mV, recovery is in less than <500ns due to TEC as ON time increases to 115ns from 80ns. Therefore, the

transient response of proposed constant on-time controller can be further improved in a step-up load change.

3.4.2. Voltage Positioning Scheme

The control method of COT converter greatly affects the accuracy performance of the converter. COT has a fast transient response and excellent light load regulation and condition. The output of the COT converter is the reference voltage and a average of the ripple voltage at the feedback node. This reduces the steady state accuracy and and in conditions when load varies. A novel method of updating the reference voltage with the real time ripple voltage information is used in this work to improve the performance of the the converter[16]. It is known that the valley of the output voltage is the reference voltage at one of the inputs of the comparator. We define the ΔV_o is the voltage ripple at the output. Thus average output voltage:

$$\bar{v_o} = V_{REF} + \frac{\Delta V_o}{2} \tag{3.1}$$

where,

$\bar{v_o}$ is average output voltage,

V_{REF} is the reference voltage,

$\frac{\Delta V_o}{2}$ is the average of ripple magnitude.

The new v_{ref} can be calculated by subtracting the peak and valley magnitude of ripple from a sample and hold circuit:

$$\frac{\Delta V_o}{2} = v_H - v_L \tag{3.2}$$

$$v_{ref} = V_{REF} - \frac{\Delta V_o}{2} = V_{REF} - v_H + v_L \tag{3.3}$$

where,

v_H peak ripple magnitude value,

v_L valley ripple magnitude value,

$_{ref}$ is the new reference voltage

If the half of the ripple component is removed from the reference voltage, the output voltage is given by:

$$\bar{v_o} = v_{ref} + \frac{\Delta V_o}{2} = V_{REF} \tag{3.4}$$

The resulting output voltage has a ripple whose average is equal to the reference voltage. Thus Voltage positioning scheme improves the load, line and steady state accuracy by modulating the reference voltage based on output ripple information. The Fig 3.18 depicts the algorithm to extract the half ripple magnitude using a sample and hold circuit and modulate the voltage reference.

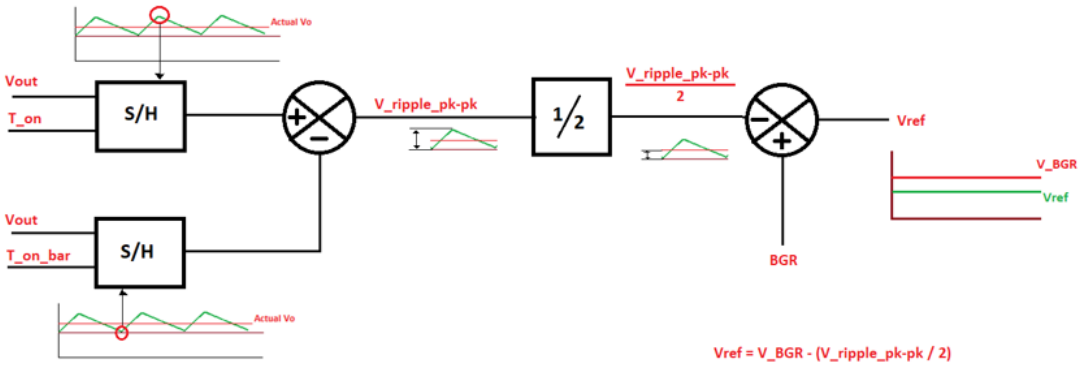
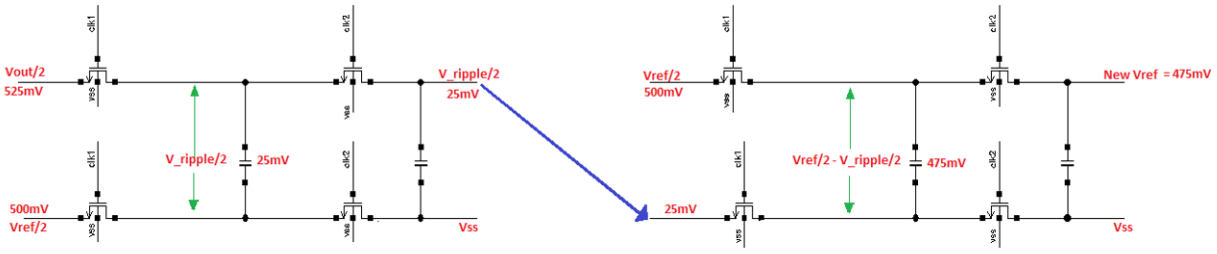


Figure 3.18: Voltage Positioning Scheme Block Diagram

The Fig 3.19 represents the schematic implementation of the voltage positioning system implemented in cadence spectre. The sample and hold function is carried out by the metal-insulator-metal (mim) capacitor based S/H circuit which operates on clock at which converter operates. This enables one correction per cycle without affecting the stability of converter by introducing excess jitter noise on reference voltage. The entire operation take four clock cycles to sample and hold and appear at the output. Thus there is one cycle delay in correction which is the min resolution

of this system. the deadtime generator can be buffered and used as clock generator for sampling. This will allow to precise capture the ripple value during its On time or OFF time depending on the logical implementation of the circuit. The sampled error voltage is then subtracted from the steady reference using switch cap subtractor. The resultant voltage is fed to comparator for comparison with the output voltage. MIM capacitors are used to reduce the leakage loss when compare to the MOS capacitor.



Sweep	Nominal vout @ load 5A , Vin 18V	COT average vout (V)	% variation	ICOT average vout (V)	% variation
Supply (8V – 18V)	1.029	1.069	4	1.025	-0.4
Load (10A – 100mA)		1.099	7	1.015	-1.4

Figure 3.19: Voltage Positioning Scheme Switch Capacitor Based Implementation and Accuracy Improvement

3.5. Dead Time Circuit

Energy lost in deadtime is proportional to the deadtime interval for a GaN FET. Accordingly, GaN achieves higher efficiency with a smaller deadtime. The lower threshold value of deadtime is determined by the minimum separation required between High side (HS) and Low side (LS) switched to avoid shoot through. Shoot through between supply and reference ground results in a high current spike resulting in reduced GaN lifetime or permanent damage due to burnout.

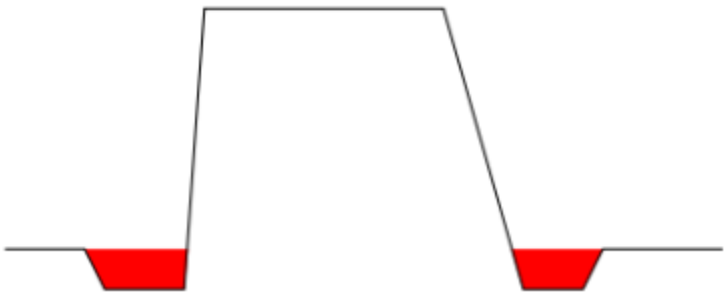


Figure 3.20: Ideal Switch Node Waveform of Buck converter. The Red Area is the Dead Time Loss.

Optimum Dead time= Worst case driver propagation delay skewing + turn-off delay time + fall time

In our work,the worst case propagation delay was about **13ns** as obtained from below Fig 3.11. Selecting our deadtime simply based on this information results in a huge deadtime conduction loss for a deadtime of about 20ns. EPC's evaluation results suggest using **5ns-20ns** of deadtime based on converter conversion ratio.

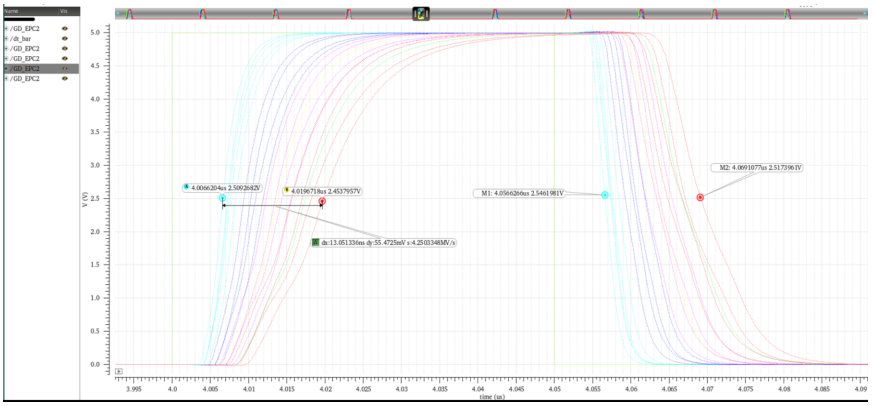


Figure 3.21: Worst Case Propagation Delay Skew

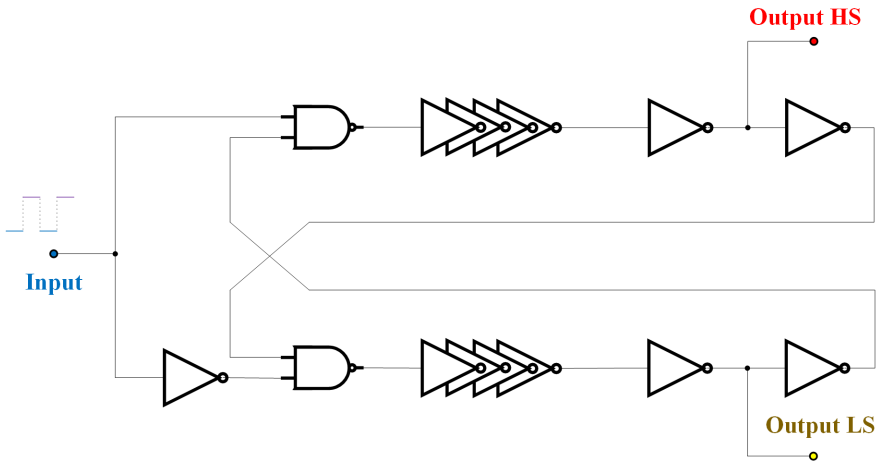


Figure 3.22: Dead Time Generator Block

The dead time control circuit (non-overlapping clock generator) is design and implemented using the standard cross coupled chain of inverters. It is designed to provide a deadtime of less than 2ns.

3.6. High-Speed Comparator

The 3 stage fast comparator is based on the design adopted from CMOS Circuit Design, Layout, and Simulation by Dr Jacob Baker. It consist of the following stages:Pre-amplification, Decision feedback, and Post amplification (output buffer). The pre-amplification stage enables the ability to resolve even the smallest signal. The positive feedback cross coupled latch is the decision making block in this topology. The positive feedback allows high speed operation. The resolved signal is then provided full rail to rail swing through buffered output stage.

The diode connected connection in the second stage level shifts for high speed operation. There are high impedance nodes only at the input and output which allows high speed operation tested up to 5MHz. The systematic offset of the comparator is as low as 3-5mV for slow DC signal. The comparator is PMOS input as the reference

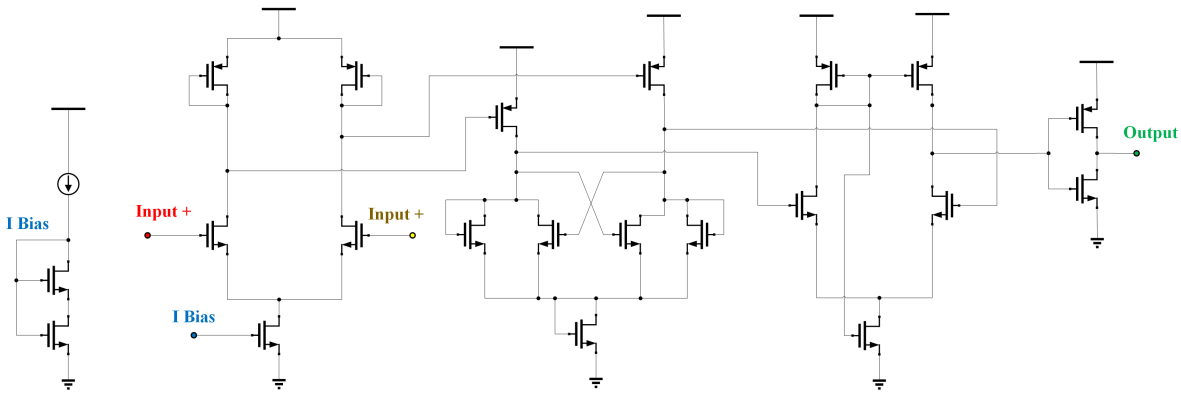


Figure 3.23: High Speed Comparator

and feedback voltage is on less than 700mV. Th comparator must be able to perform flawlessly in radioactive environment too.

3.7. Level Shifter

The level shifter are designed using the cross coupled inverter stage.The block shifts the control signal from 1.8V domain to high voltage 18V domain. The presence of High Voltage–bootstrap circuit requires the use of high voltage devices. Here Super unction devices are used to in Level shifting operation and driver design. This adds additional challenges for the high side level shifter stage with its low level being the switching node of the power converter. For driving the cascaded driver, a complementary signal is required for HS and LS. The level shifter adds some more dead-time to the driven signals in order of 2-3nS for 1MHz.

3.8. Amplifier Topology

A two stage class AB folded cascode amplifier is used inside LDOs and as a unity gain buffer.The frequency response of the amplifier is shown in the figure. The open loop gain is around 82dB with 15.13MHz of UGB. With a switching frequency of 600KHz - 1MHz, the loop bandwidth is 200KHz. Thus amplifier can respond to fast transients and reduce error in output.

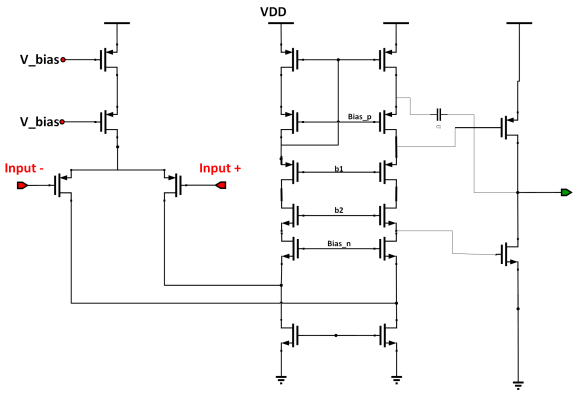


Figure 3.24: Folded Cascode Amplifier

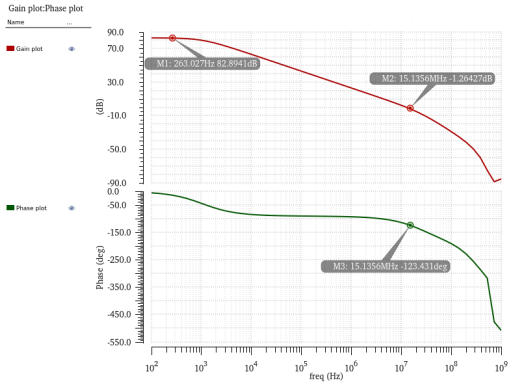


Figure 3.25: Gain and Phase Plot Of Amplifier

The indirect compensation allows high UGB without sacrificing gain. Also the separate gain and rout stage enables higher gain possible. The class AB output stage conserves power by alternate on-off cycles. The Phase margin is set to approx 60°

3.8.1. Low Dropout Regulator (Linear Regulator)

The PMOS based LDO provides power to 5V domain and 1.8V circuit blocks from 18V. The 18V-5V LDO powers the 5-1.8V LDO. This enables the slow ramping of power signals in the soft start sequence.

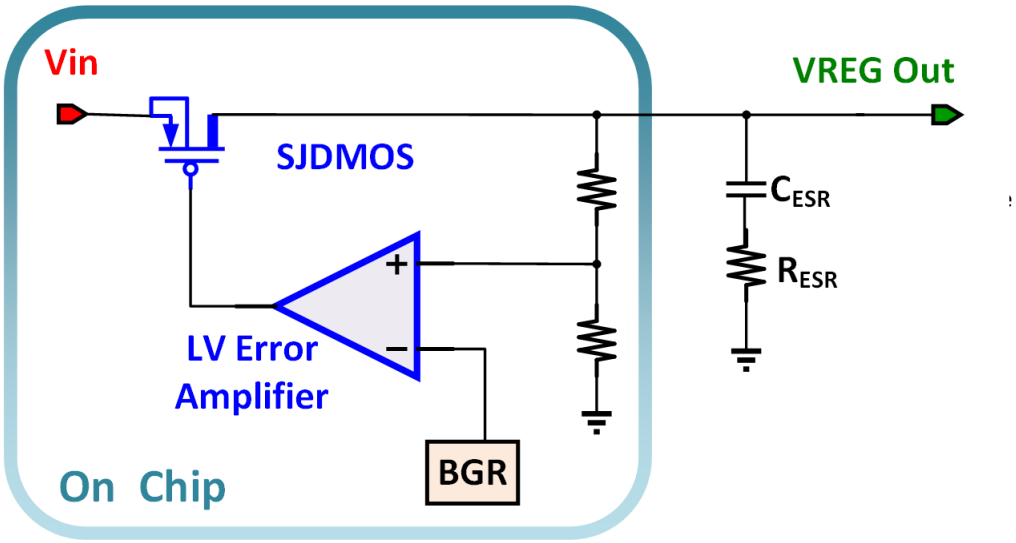


Figure 3.26: Low Dropout Regulator Topology

The amplifier used in LDO is the two stage PMOS input class AB folded cascode amplifier.Up to 1pF of compensation capacitor is used for indirect compensation. The output pole is the dominant pole provided by 44uF output cap. The second stage gain is almost 82 dB with unity gain frequency of few MHz customized for each LDO. The LDO is designed to provide average current of 100mA to 200mA.

3.9. Power Stage Design

3.9.1. GaN Package Selection

The EPC GaN package EPC 2014C was selected for the driver design purpose[6]. Following are the ratings of the EPC2014C FET:

Dynamic Characteristics important for design considerations are listed below:

- The Gate Voltage must be held at 4.5V-5.5V to maintain minimal $R_{DSon} = 15m\Omega$.
- HS Gate voltage must be prevented from dropping below -4V. This becomes important parameter in optimal deadtime design as the reverse dode voltage drop can go to -2.5V and beyond easily if deadtime is not carefully counted.[2]
- Max load current should not exceed 40A.
- Input capacitor (Ciss) is 220pF. The drive strength must be adequate to charge/discharge this big cap withing rise/fall time constraints.
- Miller turn-on ratio $\frac{Q_{GD}}{Q_{GS}} = \frac{0.3}{0.7} < 0.5$.
- Bootstrap package will be required for HV design on HS as both are NMOS switches.
- Source-Drain recovery charge (Q_{RR}) being 0 enables high frequency operation.

3.9.2. Necessary Parameters of the PowerStage

3.9.2.1. Maximum Switch Current

Maximum duty cycle which causes maximum switch node current is calculated as:

$$D_{max} = \frac{V_out}{V_{in_{MAX}} * \eta} \tag{3.5}$$

where: V_{inMAX} = maximum input voltage

V_out = nominal output voltage

η = efficiency of the converter

Since the converter also has to account for the energy used dissipated in the internal operation of the converter and other losses, the efficiency must be added to the duty cycle calculation.

Using the air-core 500nH Coilcraft inductor with 17mOhm of max esr, Δ Inductor current ripple is calculated as:

$$\Delta I_{L_{ripple}} = \frac{(V_{in_{Max}} - V_{out}) * D}{f_{sw} * L} \tag{3.6}$$

where: V_{inMAX} = maximum input voltage

V_out = nominal output voltage

η = efficiency of the converter

f_{sw} = switching frequency

L = off-chip inductor

D = Duty cycle

Maximum switch current = $\frac{\Delta I_L}{2} + I_{OUT_{Max}}$

where: ΔI_L = Inductor current ripple

$I_{OUT_{Max}}$ = Required load current

3.9.2.2. Inductor Selection

A lower value of inductor is preferred to save on space and form factor. The inductor must have higher current rating then the max current requirements. Larger inductors can help reduce ripple. Air-core inductor is selected in the application as the solution is used in radioactive environment where the radiation polarizes the ferrite and other composite cores.

A good estimation of inductor range can be obtained as:

$$L = \frac{V_{out} * (V_{in} - V_{out}) * D}{f_{sw} * V_{in} * \Delta I_{L_{ripple}}} \tag{3.7}$$

where: V_{in} = input voltage

V_out = nominal output voltage

$\Delta I_{L_{ripple}}$ = inductor ripple current

f_{sw} = switching frequency

L = off-chip inductor

D = Duty cycle

A good estimation of ripple current is 20% to 40% of Inductor current.

$$\Delta I_L = (0.2 \text{ to } 0.4) * I_{outMax} \tag{3.8}$$

3.9.2.3. Resistor divider for Setting Output Voltage

Most converters have resistor divider network for setting the output voltage. The resistor divider network can be designed using the V_{FB} & I_{FB} To improve accuracy, current through the divider network must be 100 times the feedback current:

$$I_{R\frac{1}{2}} > 100 * I_{FB}$$

$I_{R\frac{1}{2}}$= current through the resistive divider

I_{FB}= feedback bias current

This reduces the inaccuracy to less than 1%. Using more current is beneficial but it leads to more power loss within the converter. The resistors are calculated as:

$$R_2 = \frac{V_{FB}}{I_{R_{\frac{1}{2}}}} \tag{3.9}$$

$$R_1 = R_2 * \frac{V_{OUT}}{V_{FB}} - 1 \tag{3.10}$$

V_{FB} = feedback voltage

V_{OUT} = nominal output voltage

$\Delta I_{R_{1/2}}$ = inductor ripple current

R_2, R_1 = Resistor Divider

3.9.2.4. Output Capacitor Selection

Ideally low ESR off-chip capacitor should be used on the converter to minimize the ripple on the output.Ceramic capacitor are good choice owing to their low esr if dielectric is better than or equivalent to X5R. The value of output capacitor is calculated based on desired output ripple:

$$C_{OUT_{(min)}} = \frac{\Delta I_L}{8 * f_{sw} * \Delta V_{OUT}} \tag{3.11}$$

C_{OUT} = minimum allowed capacitor

ΔI_L =estimated ripple inductor current

$f - sw$ = switching frequency

ΔV_{OUT} = desired output voltage ripple

The ESR of output capacitor adds ripple to the output with the magnitude:

$$\Delta V_{OUT_{ESR}} = ESR * \Delta I_L \tag{3.12}$$

The minimum output capacitor based on minimum overshoot required is calculated as:

$$C_{OUT_{(min)}} = \frac{\Delta I_{OUT}^2 * L}{2 * V_{OS} * V_{OUT}} \tag{3.13}$$

3.9.2.5. Input Capacitor Selection

The input capacitor is normally mentioned for commercial solutions. The cap is seletced based on minimum value reuired to stabilize the input voltage when peak current requirement by switching converter occurs. Usually low ESR caps are preferred. Higher value caps can be used for lowering noise.

3.10. Ripple Generation Network

While the ON time in COT converter is determined by the ONE shot generator whose ON time is decided based on frequency of operation required, the conversion ration and the ripple magnitude. The OFF time of the converter is calculated as:

$$t_{OFF} = \frac{L * \Delta I_L}{V_{OUT} + (R_{DCR} + R_{DS_{ON}}) * I_{OUT}} \tag{3.14}$$

For accurate off time and output regulation, feedback voltage must decrease monotonically with in phase with the inductor current. Ideally the feedback voltage can be 90° out of phase with the inductor current. So cap ESR ripple is preferred to dominate cap ripple as it is in-phase with the inductor current and can ensure stability of the system. Further, more the feedback ripple must be larger to accommodate any changes due to the noise present in the system. Ideally, to reduce the output ripple, big capacitor with lower ESR are preferred. In this case it becomes critical to generate sufficient ripple at the feedback node. This is achieved using passive networks designed to generate ripple using inductor current at the feedback node. This work uses the type III ripple generation network which gives lowest output ripple while ensuring sufficient feedback node ripple for stability[12].

The type III network consist of filter components R_A, C_A and the coupling capacitor C_B. The HPF network ensures that the required amplitude ripple is generated at the feedback node.

$$C_A = \frac{10}{F_{SW} * R_{FB1} * R_{FB2}} \tag{3.15}$$

where, F_{SW} is the switching frequency and R_{FB1} & R_{FB2} are the feedback resistors.

$$R_A C_A = \frac{(V_{IN-nom} - V_{out}) T_{ON}}{20mV} \tag{3.16}$$

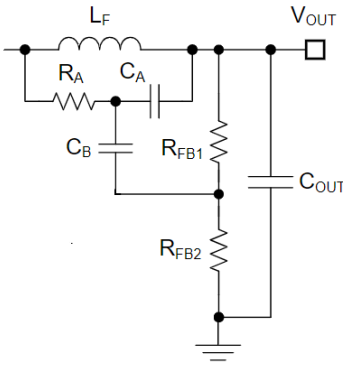


Figure 3.27: Type II Ripple Network

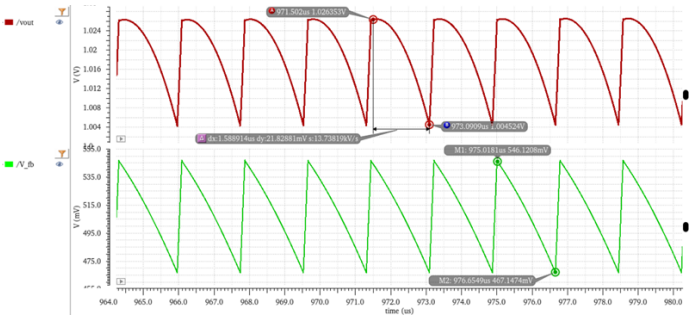


Figure 3.28: Ripple at Output & Feedback Node with Ripple Ratio = 4

where, T_{ON} is the ON time of COT and V_{IN-nom} & V_{OUT} are input and output voltages respectively. The coupling capacitor value is based on load transient settling time C_B and is calculated as:

$$C_B = \frac{T_{TR-settling}}{3.R_{FB1}} \tag{3.17}$$

where, $T_{TR-settling}$ is the switching frequency and R_{FB1} is the feedback resistor. With a ripple ratio of 4, the feedback ripple is approx 80mV while the output ripple remains to conservative 20mV. This helps to achieve stability even when output in-phase ripple diminishes due dominating capacitor ripple.

Chapter 4

SIMULATION RESULTS

4.1. Load Transient Response

4.1.1. V_{OUT}

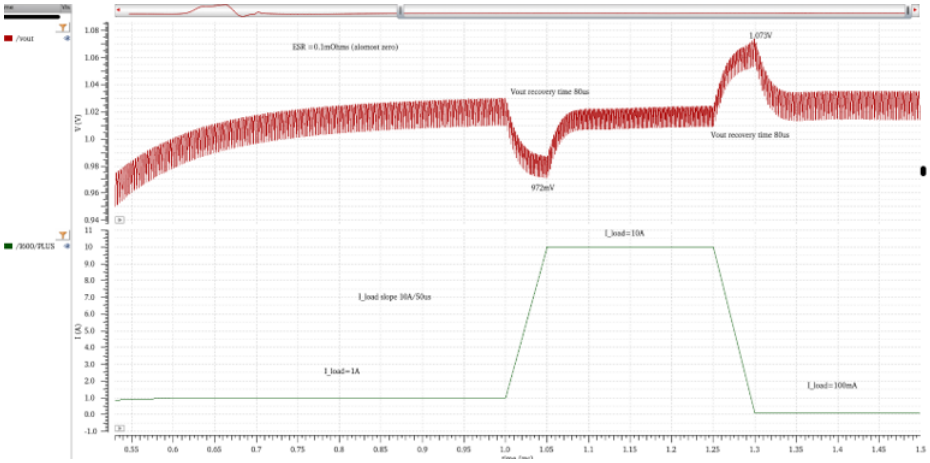


Figure 4.1: Output Load Transient Voltage Simulated in Spectre

I_{OUT} **transient**	V_{OUT} **change**	**Percent Change**
10A $\rightarrow$ 100mA	48mV	4.7%
1A $\rightarrow$ 10A	28mV	2.75%

Table 4.1: COT Converter Parameters Used in MATLAB Model Simulation and Transistor Level Schematics for Stable Operation

4.1.2. Load Transient with Voltage Positioning Scheme Deployed

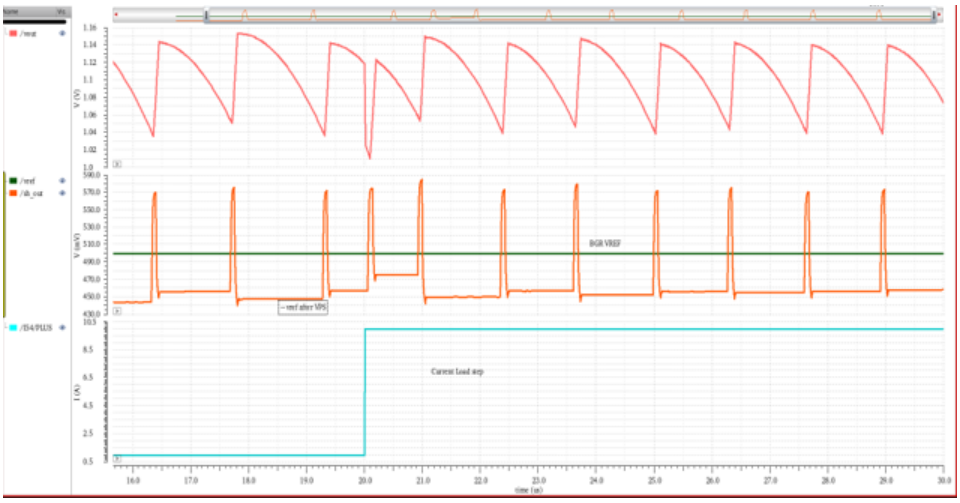


Figure 4.2: Reference Voltage Modulation With Step Load Transient

I_{OUT} **transient**	**VPS** v_{ref}
1A	445mV
10A	457mV
During Load Step	476mV

Table 4.2: VPS Response to Load Transient From 1A $\rightarrow$ 10A

Output recovers in less than 300ns (within 1 cycle – 1us)

4.1.3. Load Regulation

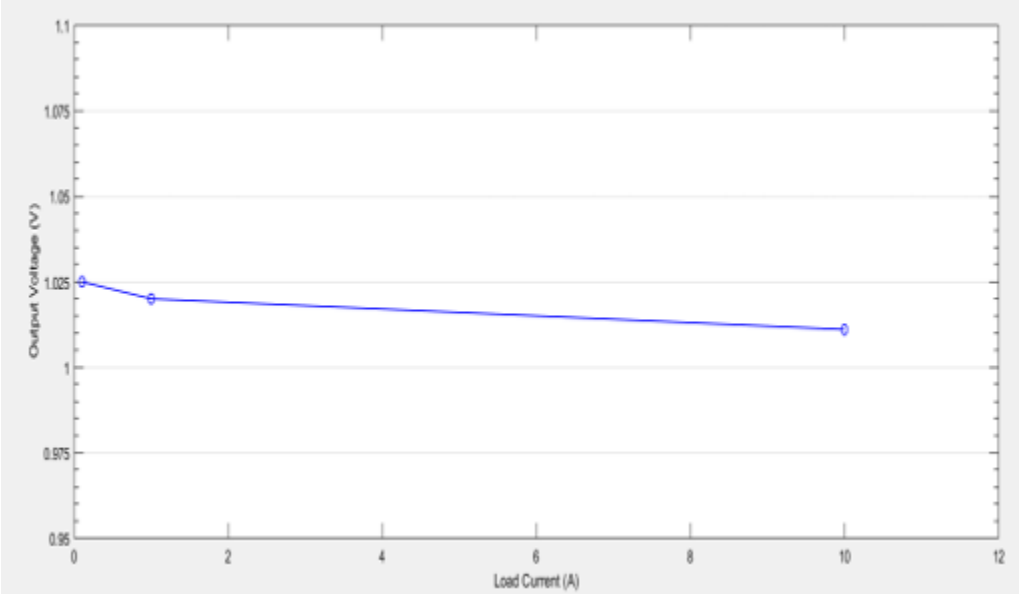


Figure 4.3: Output Load Regulation

Load Current	**Average V_{OUT}**	**Ripple pk-pk**
100mA	1.025V	21mV
1A	1.020V	19mV
10A	1.011V	15mV

Table 4.3: Load Regulation Table

As load decreases, switching frequency decreases, average feedback voltage reduces due to lower frequency. Regulation improves at lower loads as the feedback voltage is closer to the reference.

4.1.4. Inductor Current

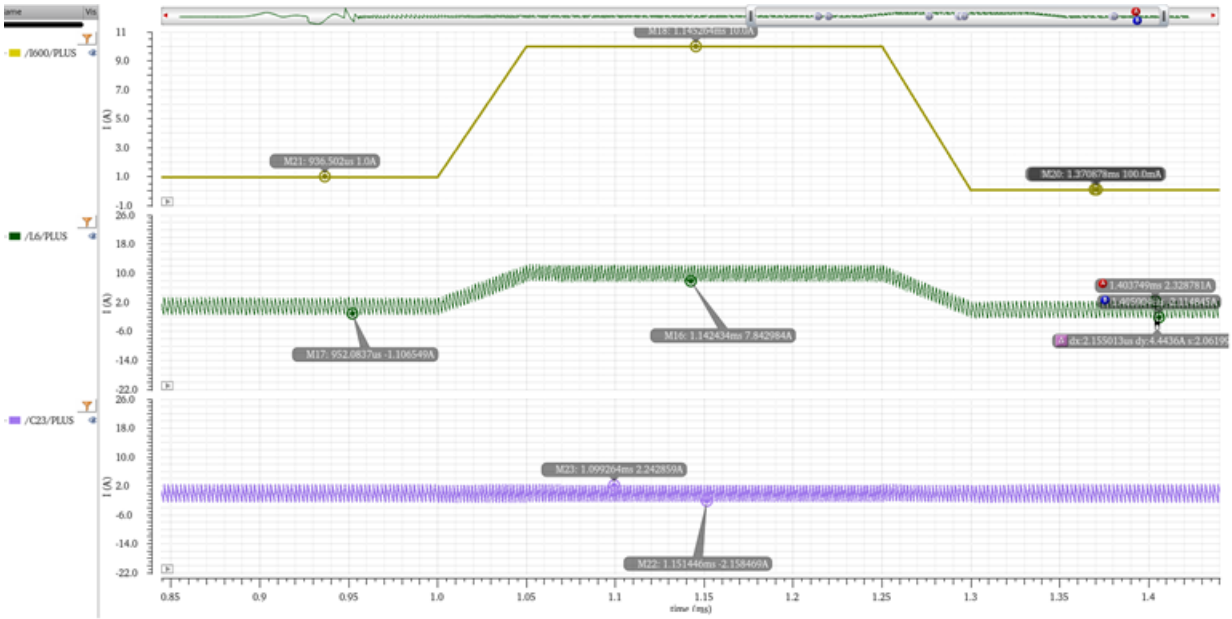


Figure 4.4: Output Load Regulation

Load	Inductor Current Ripple
100mA	4.44A
1A	4.47A
10A	4.51A

Table 4.4: Load Regulation Table

4.2. Line Transient

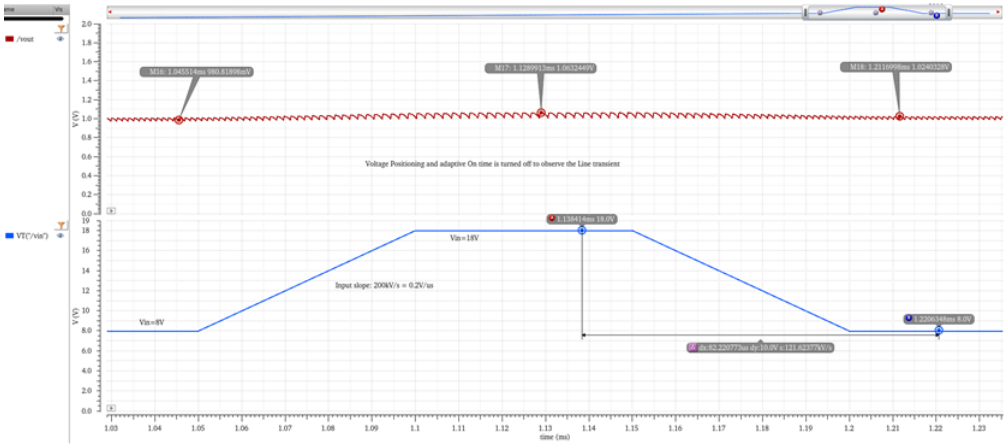


Figure 4.5: Line Transient: $8V \rightarrow 18V$

Load	V_{OUT}	**Percent Change**
8V $\rightarrow$ 18V	40mV	4.04%
18V $\rightarrow$ 8V	18mV	1.75%

Table 4.5: Line Transient Accuracy

Line accuracy reduces with as V_{in} increases. At lower input supply, the feedback is closer to refernce voltage which provides better line regulation.

4.2.1. Line Transient With Voltage Positioning Scheme Deployed

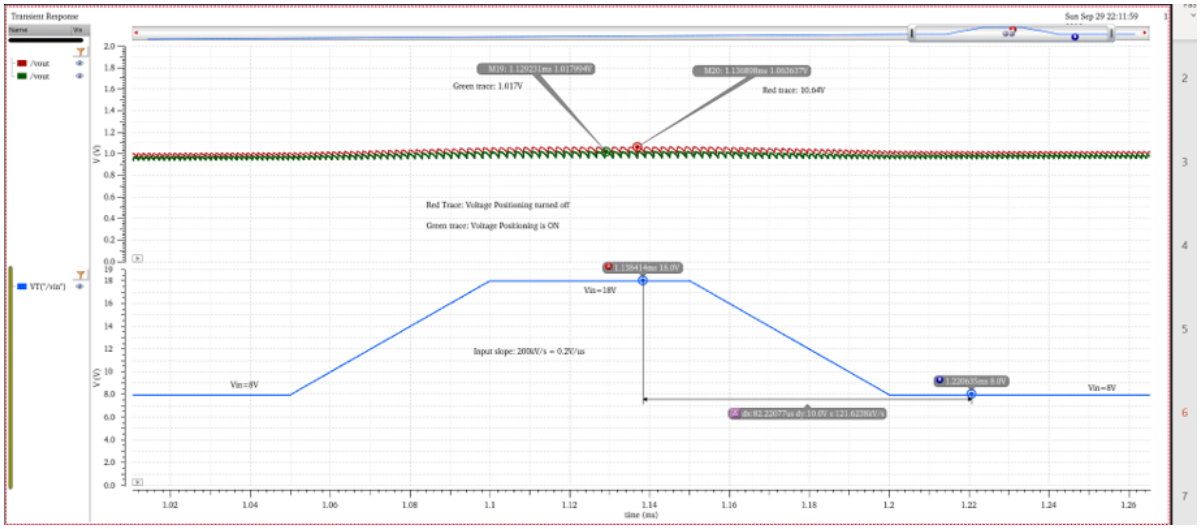


Figure 4.6: Reference Voltage Modulation With Line transient

I_{OUT} **transient**	**VPS OFF**	**VPS ON**
$V_{out_{peak}}$	1.064V	1.017V

Table 4.6: VPS Response to Line Transient From 8V → 18V

Vout peak is 47mV higher. 4.7

4.3. Reference Voltage Modulation

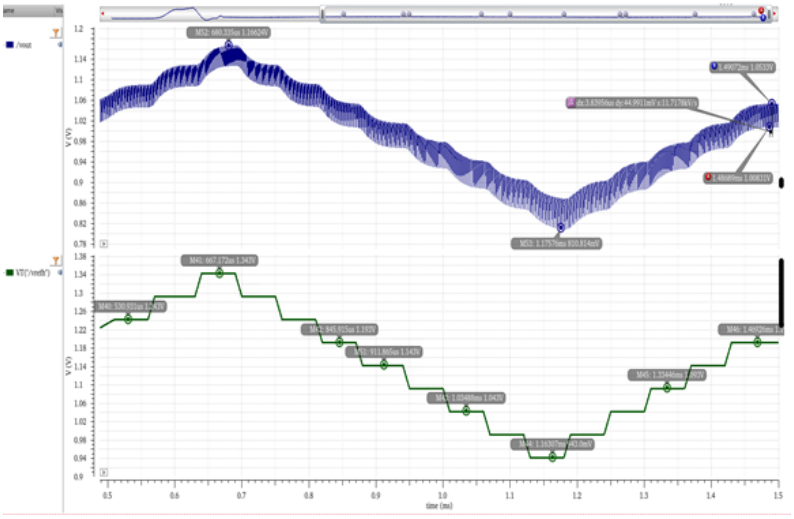


Figure 4.7: Reference Voltage Modulation $943mV \rightarrow 1.343V$

Vref (V)	$Ripple_{pk-pk}$	**Average** V_{OUT}	**% Change**
0.943V	59.63mV	0.839 V	-18.54%
1.043mV	50.17mV	0.922 V	-10.4%
1.093V	54.52mV	0.957 V	-7.09%
1.143V	46.97mV	0.993 V	-3.59%
1.193V	44.99mV	1.030 V	0%
1.243V	1.0686 V	42.80mV	+3.79%
1.343V	39.31mV	1.166 V	+13.2%

Table 4.7: Output Variation With Reference Voltage

The peak side ripple is regulated by the fix ON time which doesn't allow it to increase. Since, the valley is compared the reference, as the Vref decreases, the ripple magnitude increases.

4.4. Output Waveform & Efficiency

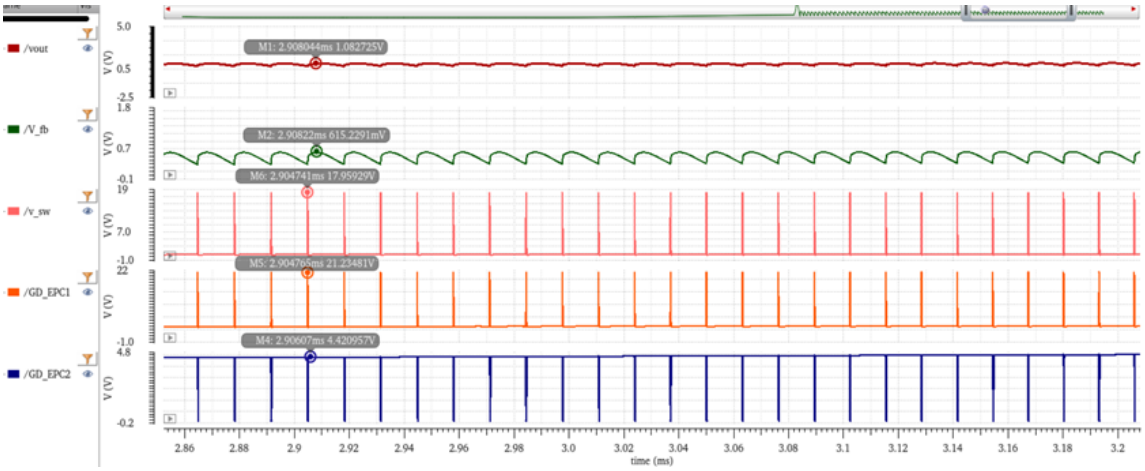


Figure 4.8: Output Waveform of Complete COT Converter

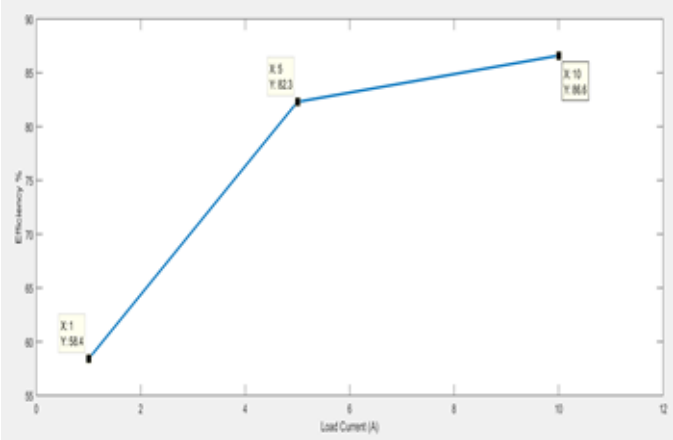


Figure 4.9: Efficiency vs Load

The efficiency is above 85% for 10A of load and above 80% for 5A PFM starts at very light loads but since the inductor current goes negative, reverse conduction occurs and efficiency falls below 60% at light loads ZCD implementation can increase the efficiency at light loads.

Chapter 5

CONCLUSION

Constant ON Time converter with GaN power FET as a potential solution for small size, high step-down ratio applications in radiation environment is presented and the performance is validated for high efficiency through simulation. Owing to the topology selection and use of GaN FETs, the driver and controller size is significantly reduced which saves the physical form factor and provides a small PCB solution. The benefits of the GaN Power FETs, SJMOS device for driver and process robustness in radiation environment are evaluated. It can be concluded from this study that GaN exhibits high efficiency in high power, fast switching application. The High step down ratio from 18V to 1V at 10A load current is demonstrated which establishes the sleek performance of the converter for applications in >10W power delivery systems. Method to improve accuracy by lowering ripple is implemented. Switch capacitor-based voltage positioning scheme is unique to this work in terms of transistor level implementation. It successfully demonstrated improved line, load and steady state accuracy by reducing the ripple induce steady offset in output voltage. MATLAB model of converter loop is simulated for stability and close equivalence is found from transistor level implementation. 86% efficiency is achieved for full load operation.

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APPENDIX A

MATLAB CODE FOR LINEARIZED COT SYSTEM

```
s=tf('s');


Vin=18;Vo=1;

%Controllerdel_D/del_VoutRa=25e3;
Rfb1 = 100e3;Ca = 1.5e-9;Cb = 250e-12;


a=Ra*Rfb1*Ca*Cb;b=Ra*(Ca+Cb);c=Vin*Rfb1*Cb;

Ctr=((a*s^2+b*s+1)/(c*s));%Power stage

L=1000e-9;
Co=66e-6;dcr=17e-3;esr=10e-3;R_load=0.1;

Wo=sqrt((1+(dcr/R_load))/(L*Co));Wesr=1/(Co*esr);

Q=((sqrt(L/Co)+R_load*(dcr+esr)*sqrt(Co/L))/(2*R_load*sqrt(1+(dcr/R_

load))));G=((Vin*(1+(s/Wesr)))/(1+((2*Q*s)/Wo)+(s/Wo)^2));

%ON-Time stage

Ton=100e-9;

D=(Vo/Vin);

H=exp(-s*D*Ton);
```

```
%Total_loop

loop= H*Ctr*G;

%H=tf([-a -b -1],[0 c 0]);
%opts.FreqUnits = 'Hz';
%h = bodeplot(tf([-a -b -1],[0 c 0]),opts)

opts.FreqUnits = 'Hz';%h =
bodeplot(loop,opts)

%bodeplot(H)
hold on;
figure(1);bodeplot(G,{1,10000000000});

figure(2);bode(Ctr,{1,1000000000000});

figure(3);bode(H,{1,1000000000000});

figure(4);bode(loop,{1,1000000000000});

figure(5);
P = pzplot(loop)hold off;

V_feedback_ripple= ((Vin-Vo)*Ton*1000)/(Ra*Ca)
```