Reconfigurable Solar Array Interface for Maximum Power Extraction in Spacecrafts

by

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ABSTRACT

The efficiency of spacecraft's solar cells reduces over the course of their operation. Traditionally, they are configured to extract maximum power at the end of their life and not have a system which dynamically extracts the maximum power over their entire life. This work demonstrates the benefit of dynamic re-configuration of spacecraft's solar arrays to access the full power available from the solar panels throughout their lifetime. This dynamic re-configuration is achieved using enhancement mode GaN devices as the switches due to their low R_{on} and small footprint.

This work discusses hardware Implementation challenges and a prototype board is designed using components-off-the-shelf (COTS) to study the behavior of photovoltaic (PV) panels with different configurations of switches between 5 PV cells. The measurement results from the board proves the feasibility of the idea, showing the power improvements of having the switch structure. The measurement results are used to simulate a 1kW satellite system and understand practical trade-offs of this idea in actual satellite power systems.

Additionally, this work also presents the implementation of CMOS controller integrated circuit (IC) in 0.18um technology. The CMOS controller IC includes switched-capacitor converters in open loop to provide the floating voltages required to drive the GaN switches. Each CMOS controller IC can drive 10 switches in series and parallel combination. Furthermore, the designed controller IC is expected to operate under high total doses of radiation, thus enabling the controller modules to be placed on the solar cell wings of the satellites.

DEDICATION

Dedicated to my beloved parents and my wonderful sister

ACKNOWLEDGMENTS

Firstly, my heartfelt and sincere thanks to my advisor Dr. Jennifer Kitchen for providing me an opportunity to work on this valuable research project. Her guidance and support during my Master's and this project has been amazing and I am deeply grateful to her.

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1 INTRODUCTION

1.1 Motivation

With a great economic potential of the solar arrays as a power source, there is tremendous emphasis on improving the energy conversion efficiency of PV cells. However, these efficiency gains presently come at an unreasonable cost. A mono-crystalline silicon solar panel at 25.6% efficiency costs 50% more than a poly-crystalline silicon solar panel at 20.8% efficiency [1]. The ability of a single cell to capture the available energy at high efficiency is only half the story. A large percentage of the efficiency is subsequently lost, since solar cells are rarely used in isolation and when they are connected in an array, the array performance is reduced to the lowest common denominator [2]. There is an urgent need to close the gap between cell-level energy improvement and system-level energy extraction, which can be closed with efficient power management schemes at the panel and sub-panel level.

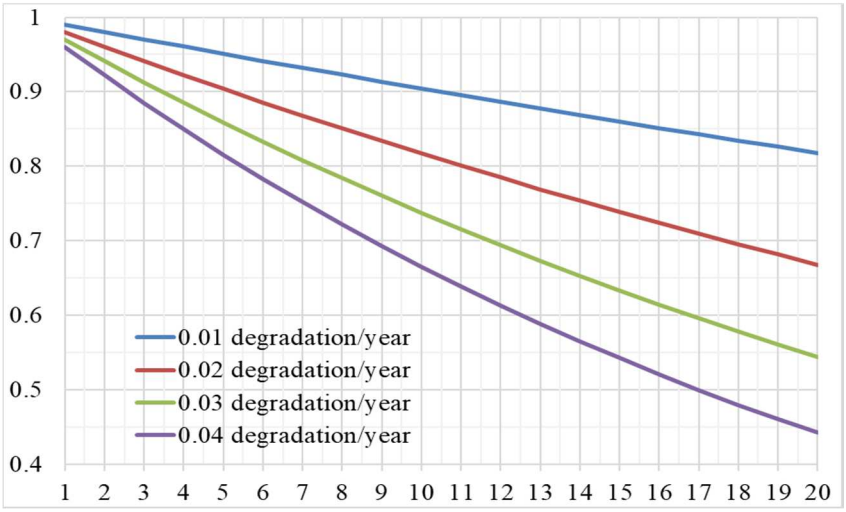


Figure 1: Solar Cell Power Performance Degradation over Their Lifetime. The Power Is Normalized to 1

Additionally, in space, the spacecraft solar arrays can degrade from 20% to 50% in power producing capability over a 15-year mission [3] as shown in Figure 1, making it unfeasible for current state-of-the art designs to access the full power available from the solar array because the solar array interface (SAI) is not optimized to extract peak power over the entire spacecraft lifetime. This prompts the need to develop a solar array that delivers full power from the spacecraft's beginning to end of life. Furthermore, these array configurations are traditionally fixed solar PV arrays that have hard wired interconnections between their solar cells. These connections are not changed after installation and must therefore be designed for the spacecraft's end-of-life (EOL) performance, hence wasting 10-50% of the spacecraft power during the beginning of life (BOL). This is illustrated by observing the BOL versus EOL power capability for various example spacecrafts in Figure 2 [4]. Currently, the extra BOL power is not used, as current spacecraft power systems do not have the capability to re-allocate power to different loads outside of the spacecraft bus or convert the additional power to an effective power source for the bus.

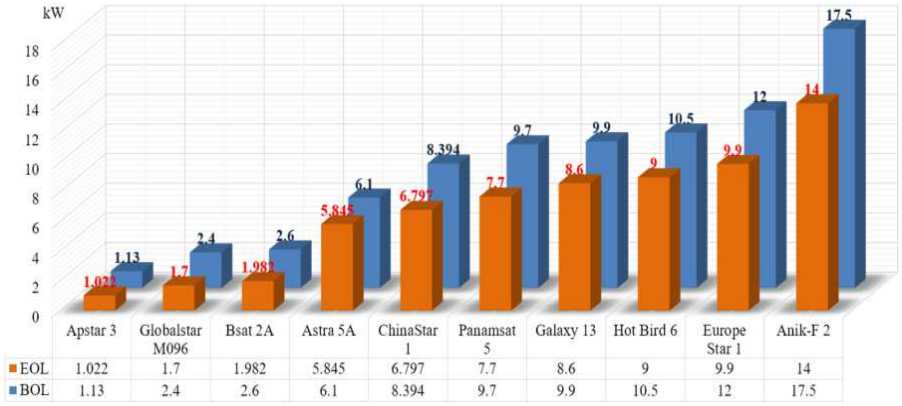


Figure 2: BOL and EOL Solar Power Capability for Various Spacecrafts Still Within Their Operational Lifetime

1.2 Objectives and Challenges

This work presents the advantages of dynamic re-configuration of solar cells in solar arrays. With the dynamic re-configuration, it is possible to increase the efficiency of the solar array by continuously rearrange solar cells in series and parallel connections to facilitate the photovoltaic system to work more as a constant power source in different operating conditions (i.e. temperature, irradiation, loads) [5]. The objectives of this research are to: 1) develop a dynamically reconfigurable solar cell array for spacecraft applications, 2) investigate and choose and optimal power device for realizing the power switches in the presented reconfigurable architecture, and 3) solve the challenge associated with floating gate control of power switches by innovating circuits and implementing a silicon CMOS controller chip.

In order to extract maximum power out of the solar array even after a number of the solar cells have failed or degraded in terms of performance, the solar array must be dynamically reconfigured. Following are the three major components to enable dynamic reconfiguration: (a) a radhard, high voltage, low-leakage electronic switch module consisting of GaN power switches for physically reconnecting/reconfiguring the solar cells, (b) design of a radhard CMOS controller chip for turning the power switches on/off according to a digital command signal, and (c) a solar cell array architecture and assembly that allows for reconfiguration and insertion of the switch module electronics.

The developed electronics should have the following specifications to be integrated:

- Consume less than 1% of the solar array's power.

- Extreme radiation hardness (+300Mrad TID, +1E15 proton fluence).
- Integrated, compact, low-mass, switch module solution that includes GaN power switches for reconfiguration and silicon-based CMOS-integrated controller and power switch drivers. These components should be integrated within a module to provide a small form factor solution that can be embedded in the solar cells on the spacecraft wings.

1.3 Existing Solution and its Challenges

In large terrestrial systems, each of the solar submodules are connected to its own maximum power point (MPP) tracking DC-DC boost converter and can individually operate near its own MPP to provide distributed maximum power point tracking (DMPPT). Thus, the efficiency of the whole system is increased [6] [7] [8]. However, this method requires a large number of high-performance, small form-factor DC-DC boost converters. The implementation in Figure 3 show boost converters designed to regulate an input voltage of 8-12V (common in terrestrial applications) up to 36V, to maintain the bus voltage of 100V. This would allow the bus voltage to be maintained even with the degrading PV cells. Although this solution seems to be feasible, following are the challenges to implement:

- Mounting complex electronics within the spacecraft's solar cell array would require extensive measurement characterization and qualification testing
- Excessive routing to/from the converters and central power system
- Additional mass of the converters

- Physical ability to embed the converters within the solar array.

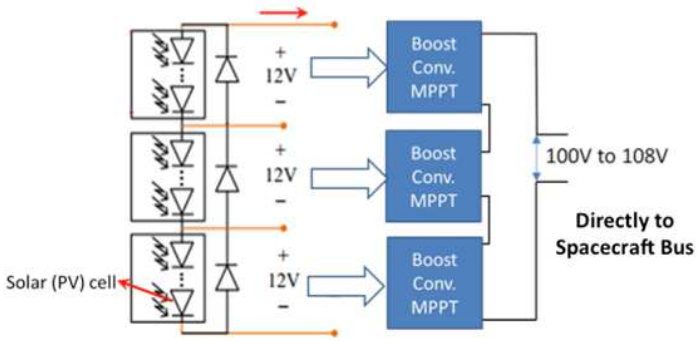


Figure 3: Power Converter Architecture for Solar Array Interface to 100V Spacecraft Power Bus

Due to the above challenges, a strategy for reconfiguring a solar array using switches to physically reconnect the solar array is proposed in this work.

1.4 Proposed Solution

In the proposed solar array structure, individual solar (PV) cells, strings of cells, and even sub-arrays can be reconfigured to deliver the maximum attainable power from the overall solar array, where maximum attainable power is defined as the sum of maximum power of all functioning solar cells. The number and location of such cells can be time varying due to aging and radiation effects and will be steadily decreasing over the lifetime of the mission. Based on the reliability studies, one can determine the minimum number of solar cells necessary to complete the mission. However, having this minimum number of functioning cells does not guarantee the desired power delivery because the overall performance is determined by the lowest performing (weakest link) solar cells in a solar cell array. One solution to this problem is dynamically reconfiguring the rows and columns of the solar array based on functioning cells.

As an emerging research field, the focus of this research is to adaptively reconfigure solar array connections in real time to track maximum output power [9]. Recent studies have started to develop methods to reconfigure solar cells to improve power output in shaded conditions. In addition to improving overall power extraction efficiency of the array over environmental changes and aging, this method may also be used to reconfigure solar arrays into sub-arrays that may power various spacecraft loads outside of the bus (e.g. electric propulsion system).

Additionally, the reconfiguration may be used to maintain a constant spacecraft bus voltage in solar array systems that cannot have output voltage flexibility. An example demonstrating reconfiguration to maintain a spacecraft bus voltage of approximately 100V +/- 10% is given in Figure 5. This case study uses a model that reflects PV characteristics and degradation patterns of solar cell for spacecraft power systems [10]. The sample array contains 495 cells, where each active device symbol in the figure represents 5 XJT Prime solar cells. The array's string (column) length is initially sized to ensure that EOL output voltage is within 10% of 100V. When doing this, there are 55 cells stacked in a column. At the BOL, this 55-cell stack gives significantly higher output voltage that necessary. Since the spacecraft cannot use this excess voltage, this power capability is lost in a fixed-configuration array. With a flexible array, the extra solar cells that are not required for voltage at BOL may be reconfigured and used to provide more power to the bus. An example of this reconfiguration is given in Figure 5(b), where the original 55 x 45 array is reconfigured to a 45 x 55 array to provide more current and less stacked voltage. When more cells are required in each column to meet the 100V spacecraft bus at EOL, the array

can be configured back to Figure 5(a). Another way to see the benefit of reconfiguration is to compare a fixed array with a reconfigurable one and observe that the reconfigurable array may switch the architecture to recover voltage with aging.

The Figure 4 shows the maximum array voltage before and after the switching. As discussed before, the array voltage reduces over time due to radiation and the re-configuration helps to maintain the maximum array voltage within 10% of 100V throughout the spacecraft lifetime.

The efficiency to the device used as a switch used for re-configuration is very important to reduce the switch losses. Also, the switch must be characterized for high doses of radiation as they are integrated with the solar (PV) cells on the spacecraft's wings. This makes choosing the right switch device very important. A quick comparison between the GaN HEMT, in particular eGaN from EPC and some rad-hard power MOSFET from international rectifier illustrates the benefits of eGaN in the context of satellite missions. Efficiencies obtained using eGaN transistors in DC-DC converter are shown to be in the 90% range and higher for several operating conditions when they hardly reach the 80% percent when using IR rad-hard power MOSFETs (see Figure 6(a)) [11]. Such increase of performance is obtained with devices that also are much smaller in size as shown in Figure 6(b) where the dimension of a radiation-hardened power MOSFET is compared to the dimension of an EPC eGaN device.

The difference in dimension between power MOSFET and eGaN devices is worth mentioning as it presents a reduction of the effective volume to be considered for the volume/area presented to particles in Single Event Effects (SEE) and Total Ionization

Dosage (TID), and it is also important for reducing the space occupied by the circuitry placed on top of the solar arrays.

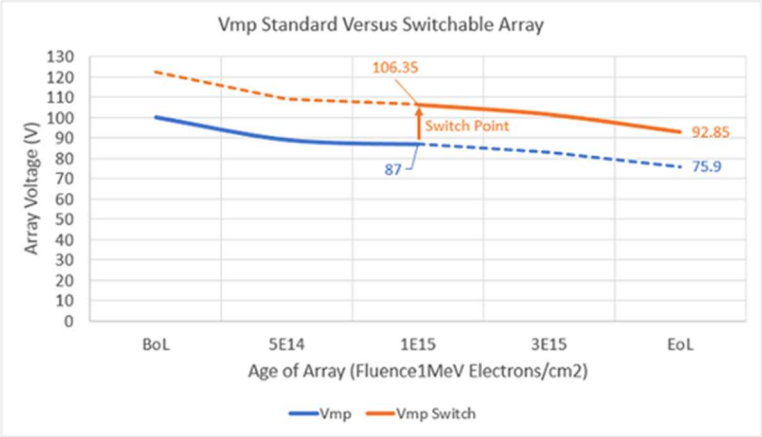


Figure 4: Array Output Voltage with Aging (Irradiation). The Output Voltage Degrades with Time, and Switching the Array Configuration Can Recover Output Voltage

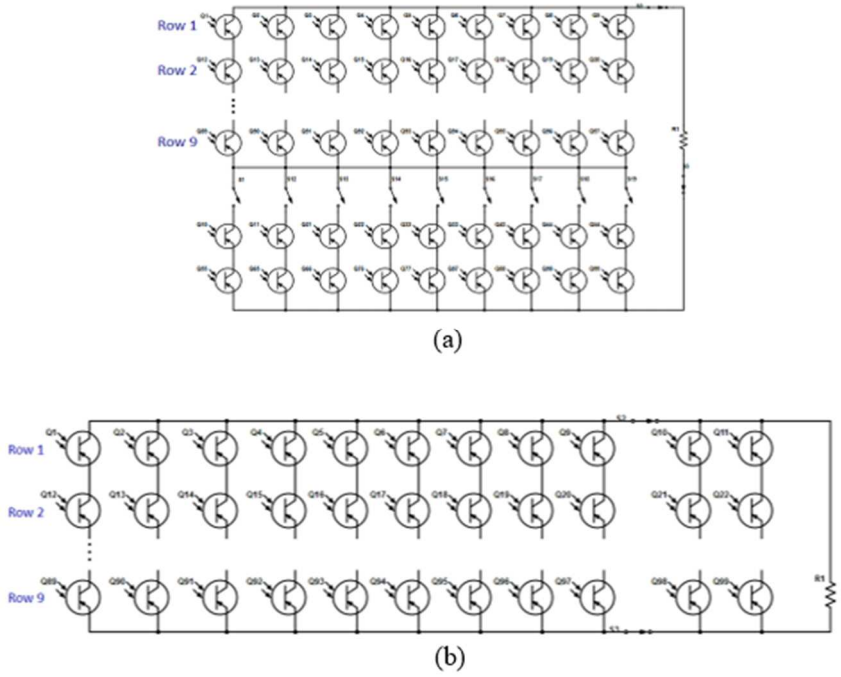
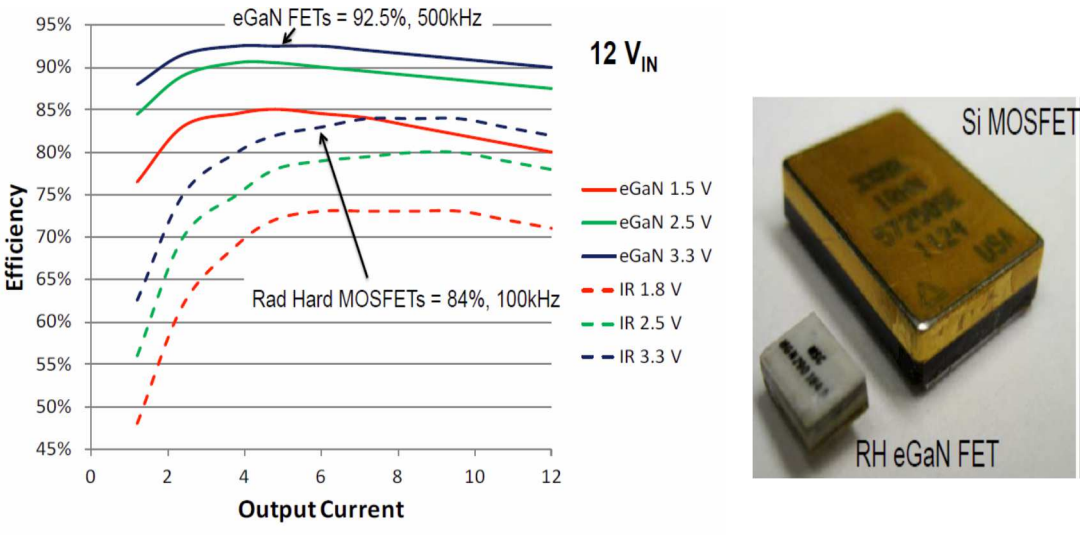


Figure 5: Diagram Illustrating Solar Cell Reconfiguration from an (a) 55 x 45 Configuration of Solar Cells to (b) 45 x 55 Configuration



(a) (b)

Figure 6: (a) Typical Efficiencies Obtained on a DC-DC Using eGaN Devices and Rad-hard Power Mosfet Devices, (b) Package Dimensions of eGaN and Rad-hard Power Mosfet, from [11]

1.5 Thesis Organization

This thesis details the design and implementation of both discrete and integrated solutions for dynamic solar array reconfigurations. The thesis is organized in 5 chapters. Chapter 1 gives a brief introduction of the motivation and the proposed solution. Chapter 2 details the overview of architectures of the switch re-configurations. Chapter 3 discusses the implementation of the board-level reconfiguration architecture and simulation results. Chapter 4 details the design of CMOS controller integrated solution (IC) for dynamic reconfigurations. Finally, the conclusion of this work is presented in Chapter 5.

2 SOLAR ARRAY RECONFIGURATION AND SWITCH DRIVER ARCHITECTURES

This chapter gives detailed overview of solar array reconfiguration and switch driver architectures. Section 2.1 introduces the photovoltaic cell model, Section 2.2 defines cell resolution terminologies, Section 2.3 details solar array reconfiguration architectures, Section 2.4 explains the need for different switch topologies and Section 2.5 presents high voltage floating switch drive architectures.

2.1 Photovoltaic Cell

To design a switch reconfiguration structure for PV cells, it is important to understand the model and the electrical characteristics of PV cells. Solar (PV) cells convert light directly into electrical energy [12]. When sunlight falls on the PV cells, voltage is developed across the terminals of PV cells and when a load is connected across these terminals, current flows from the PV cells. The simplest PV cell model is called a single diode model and it is shown in Figure 7.

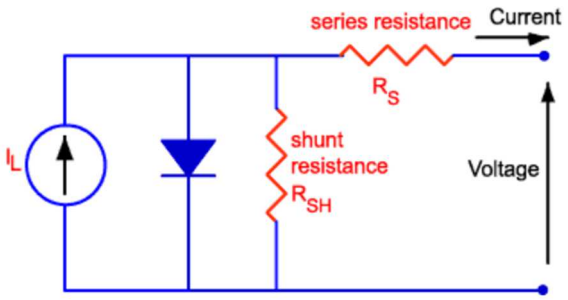


Figure 7: Single Diode Model of PV Cell

The current (I) and the voltage (V) seen in Figure **7** are given by the following equation,

$$I = I_L - I_O * e^{\frac{q(V+IRS)}{nkT}} - \frac{V + I * R_S}{R_{SH}}$$

Here I_L is light generated current, I_0 is dark saturation current (the diode leakage current density in the absence of light), T is the absolute temperature (K), R_S is series resistance, R_{SH} is shunt resistance, and

q = 1.602×10^{-19}C (absolute value of electron charge).

k = $1.38\times10^{-23}m^2kgs^{-2}K^{-1}$ (Boltzmann Constant).

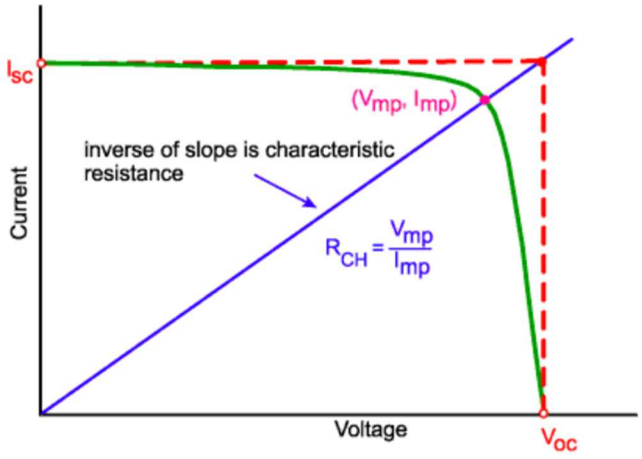


Figure 8: IV Curve of a PV Cell

Following are some of the common terms associated with a PV cell, I_{SC} is the Short circuit current, V_{OC} is the Open circuit voltage, I_{MP} is the PV output current at maximum power point, V_{MP} is the PV output voltage at maximum power point, and P_{MP} is the PV output power at maximum power point.

Figure 8 shows the IV curve of a PV cell. The load should be configured to operate the PV cell at the intersecting point of V_{MP} and I_{MP}. This point is called a maximum power point. It is the operating condition of the PV cell where the most power can be extracted

(P_{MP}). There are various algorithms available to achieve the maximum power point [13]. They are called maximum power point tracking (MPPT) algorithms.

2.2 Cell Resolution

The cell resolution is the group of cells which are always connected in series with no switching reconfiguration possible between them. These sets of cells behave as a single cell unit in different reconfiguration types. Depending on the number of cells, they define the resolution of voltage in the system. For example, if a single cell output voltage is 2.71V, a 3-cell resolution system can add or control the output voltages only in multiples of 8.13V. The 5-cell resolution can control the voltages in multiples of 13.55V.

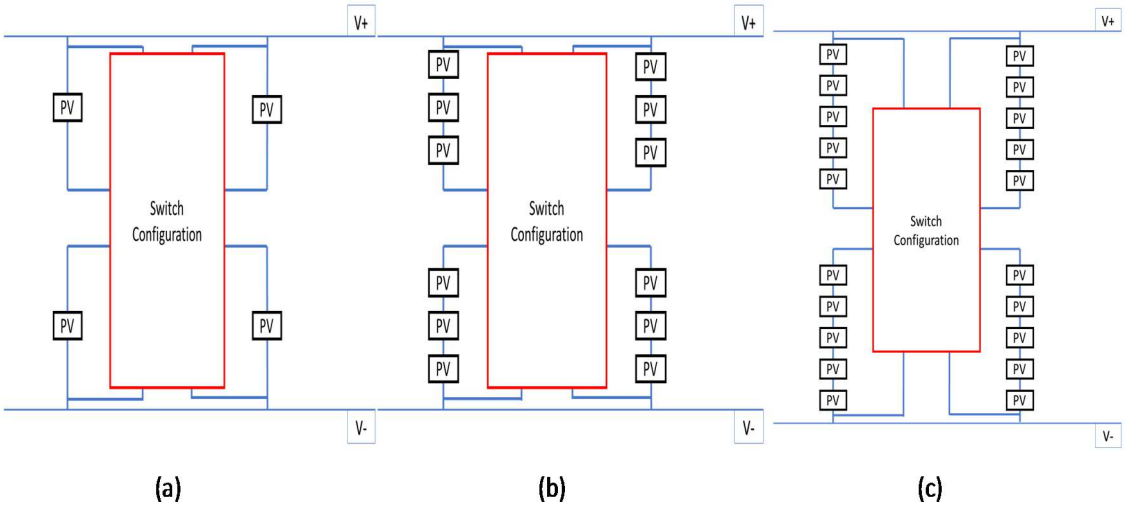


Figure 9: (a) 1-Cell Resolution, (b) 3-Cell Resolution and (c) 5-Cell Resolution

Figure 9 (a), (b) and (c) show 1-cell, 3-cell and 5-cell resolution respectively. The cell resolution can be selected based on the resolution of the voltage required. With

decrease in resolution, the system becomes more complex as more switches are needed to control the same number of PV cells.

2.3 Solar Array Reconfiguration Architectures

Two types of reconfiguration architectures are presented in this section. These reconfiguration architectures are designed to be integrated with four PV cells. It should be noted that the label 'cell(s)' in Figure 10 and Figure 11 may refer to a single cell or group of cells connected in series depending on the cell resolution.

2.3.1 Reconfiguration Type – I

Figure 10 shows the type – I reconfiguration architecture. It is a structure with simple series and bypass switches. Due to the nature of its structure, this architecture has higher losses as the PV cells are not completely isolated in their bypass state. However, since only 8 switches are needed to implement this structure, the hardware complexity is significantly reduced. A prototype board is designed with this reconfiguration type, and the feasibility of this topology is confirmed. The total number of cells required to implement this reconfiguration type is 2*n. Here, n is the number of PV cells.

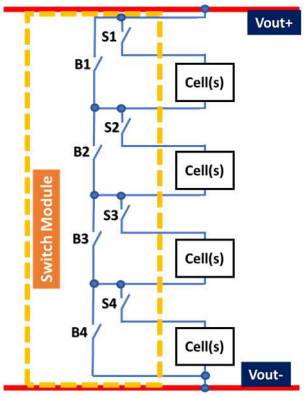
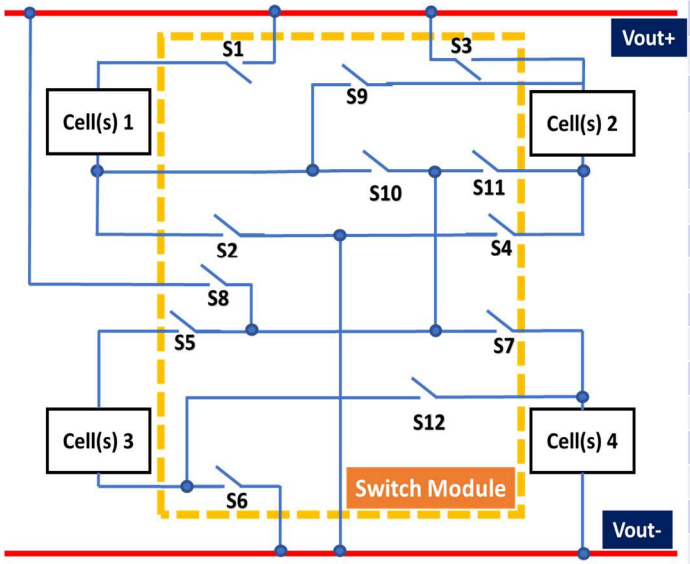


Figure 10: Reconfiguration Type - I Architecture

2.3.2 Reconfiguration Type – II

Type – II reconfiguration architecture is a 12-switch configuration to achieve the reconfiguration of PV cells (or set of cells). The 12-switch configuration architecture is placed between four cells or sets of cells (depending on the cell resolution). In all the possible combinations, it connects the PV cells in series as a single string. Figure 11 shows the switch network between the cell(s), and the table on the right shows the panel combinations to be switched on to get the respective switch combination of the cell(s) in series. The total number of cells required to implement this reconfiguration type is 3*n. Here, n is the number of PV cells and is always in multiples of 4.



Cell Combination (to be turned on)	On switch
Cell 1	S1,S2
Cell 2	S3,S4
Cell 3	S8,S5,S6
Cell 4	S8,S7
Cell 1, Cell 2	S1,S9,S4
Cell 1, Cell 3	S1,S10,S5,S6
Cell 1, Cell 4	S1,S10,S7
Cell 2, Cell 3	S3,S11,S5,S6
Cell 2, Cell 4	S3,S11,S7
Cell 3, Cell 4	S8,S5,S12
Cell 1, Cell 2, Cell 3	S1,S9,S11,S5,S6
Cell 1, Cell 2, Cell 4	S1,S9,S11,S7
Cell 1, Cell 3, Cell 4	S1,S10,S5,S12
Cell 2, Cell 3, Cell 4	S3,S11,S5,S12
Cell 1, Cell 2, Cell 3, Cell 4	S1,S9,S11,S5,S12
NONE	S8,S11,S4

Figure 11: Reconfiguration Type - II Architecture

2.4 Switch Topologies

This section presents the switch topologies used to for the dynamic reconfiguration of PV cells. GaN devices are used as power switches because of their low R_{on} and high R_{off} [14]. Since GaN devices have freewheeling diodes, it is important to discuss the topologies to overcome the leakage problem through these diodes. If the source voltage of a GaN is less than the drain voltage, a single GaN device can be used as a switch. This switch topology between 2 solar (PV) cells is shown in Figure 13.

However, when a switch sees the source voltage greater than the drain voltage, 2-GaN topology is used. The bypass switches discussed in type – I reconfiguration are designed with 2 GaN devices connected in series with sources terminals shorted together. It is designed this way because of the presence of the inherent body diode which leaks current even when the bypass switch is off (diode is forward biased). Figure 12 shows the topology of the bypass switch. 'Drain 1' and 'Drain 2' are two terminals of the switch. The gate node is where the control signal is sent.

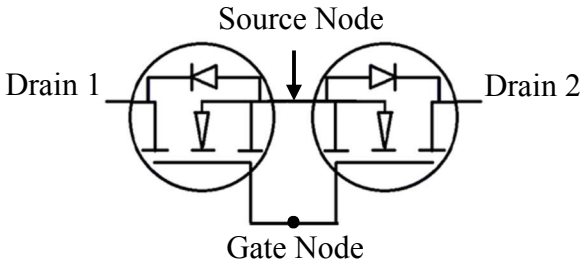


Figure 12: 2-GaN Switch Topology

Various methods were studied to overcome this leakage problem. The freewheeling diode, even though helpful in other power applications, is a problem here. The literature survey shows that a possible solution is to have another diode in the opposite direction to

the body diode so that the leakage current could be stopped [15]. But the R_{on} of the external diode is much higher than that of GaN. So, it is suitable to have to GaN with the source shorted together because single signal at the gate can control the switch. The body diodes of both GaN devices are in the opposite direction and there is no leakage current when the switch is off.

2.5 Switch Driver Architectures

This section presents the architecture of the single switch driver structure. Although power switches needed for reconfigurations are not high-speed switches, a switch driver topology need to read the varying PV cell voltages (where sources of GaN devices are connected) and provide the corresponding floating drive voltages.

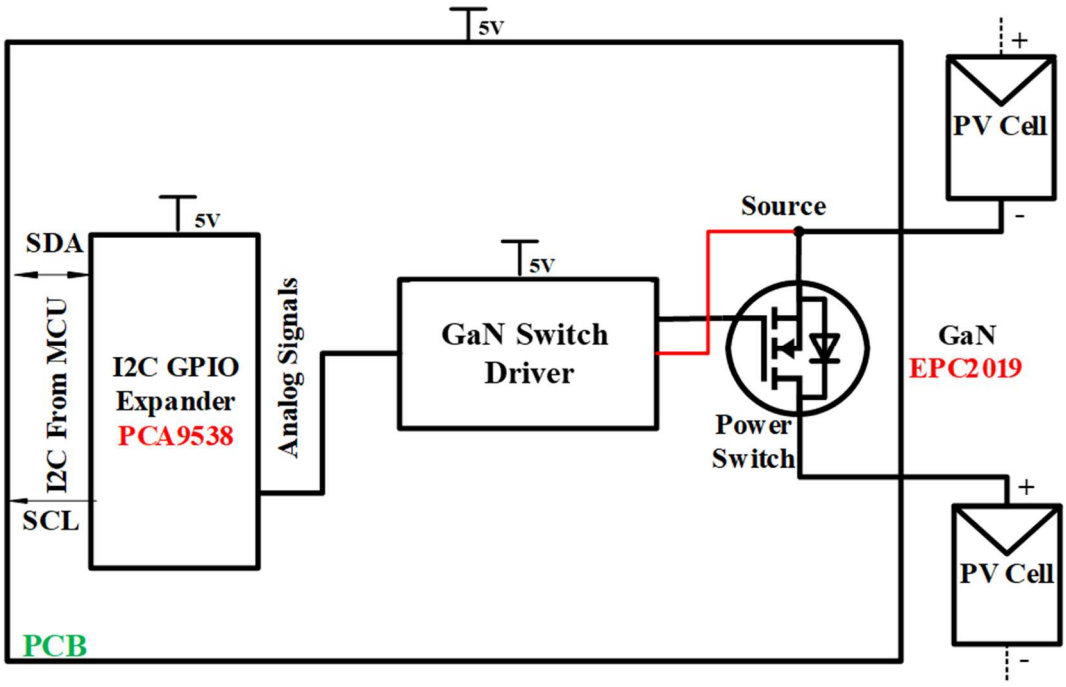


Figure 13: Transformer / Capacitive Based Single GaN Switch Driver

Figure 13 shows the block diagram of a single switch structure. Algorithm used to control the switches is stored in the micro controller unit (MCU). MCU uses serial communication protocol to send the switching information to the GPIO expander. The GPIO expander then decodes this signal into parallel analog signals. These analog signals must be level shifted to appropriate floating drive voltages of the GaN switches. The floating voltages can be generated with either a transformer-based architecture or a capacitive based architecture. Each architecture has their own advantages and disadvantages. Prototype board with the components-off-the-shelf (COTS) are designed with transformer-based topology to generate the floating voltages. The integrated circuit (IC) solution uses capacitor based floating voltage generator topology due to ease of its on-chip integration.

3 PROTOTYPE BOARD DEVELOPMENT

3.1 Overview

This section presents hardware Implementation challenges and a prototype board is designed using components-off-the-shelf (COTS) to study the behavior of photovoltaic (PV) panels with reconfiguration electronics (GaN switches). The measurement results from the board proves the feasibility of the idea, showing the power losses of having switch structure. The measurement results are used to simulate a 1kW satellite system in MATLAB and understand practical trade-offs of this idea in actual satellite power systems.

The prototype board describes two types of measurement setups and results. They are for standalone test structure and for multi-switch prototype module. The standalone structure is used to characterize a single GaN switch and multi-switch prototype module is used to verify the number of switches and their reconfiguration (arrangement of switches).

Type – I reconfiguration architecture is implemented on the prototype board. There are three series switches and two bypass switches on the board. The architecture of these 5 switches is shown in Figure 14. When all the cells in the prototype are connected in series, the switches S1, S2 and S3 are turned on and the both the bypass switches (B1 and B2) are turned off. In Figure 14, PV Set – I cells are the three cells connected in series between switches S1 and S2 and PV Set – II cells are the two cells connected in series between S3 and the negative terminal of the measurement unit. Although Figure 14 has cells arranged in a 3-2 combination, the number of cells in PV Set – I and PV Set – II can be different.

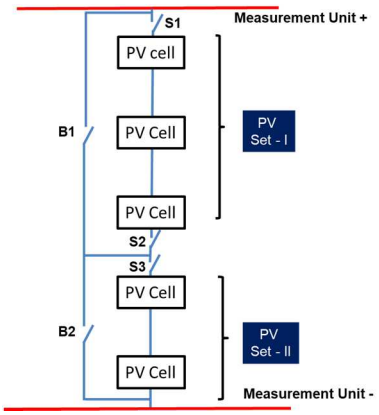


Figure 14: 5 Cells in 3-2 Cell Configuration

3.2 Switch Architecture Implementation on Board

The topology of a switch between the PV cells on the prototype board is shown in Figure 15.

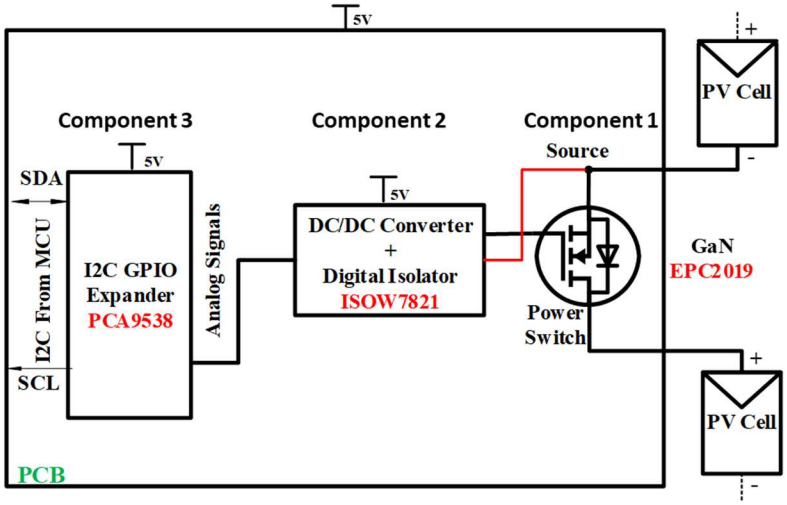


Figure 15: Implementation of the Single Switch and Driver

The switching signal is generated from the MCU of a satellite which already has the algorithm stored. The MCU sends the data to a GPIO expander with I2C protocol. NXP

part [16] (shown as component 3) is used as an expander on the board. The analog signals from the expander are converted into isolated signals with respect to the source of GaN with a TI component ISOW7821 [17] (shown as component 2). This component is used to drive GaN switches. An Efficient Power Conversion (EPC) device EPC2019 [14] (shown as component 1) is used as a GaN switch between the PV cells. This device has breakdown voltage of 200V and drain current breakdown of 8.5A, which is sufficient for power switch for PV cell reconfigurations. The board picture, shown in Figure 16, annotates the placement of the primary components. The board also has a test structure to completely characterize a GaN switch. This is present in the bottom left corner of the board shown in Figure 16.

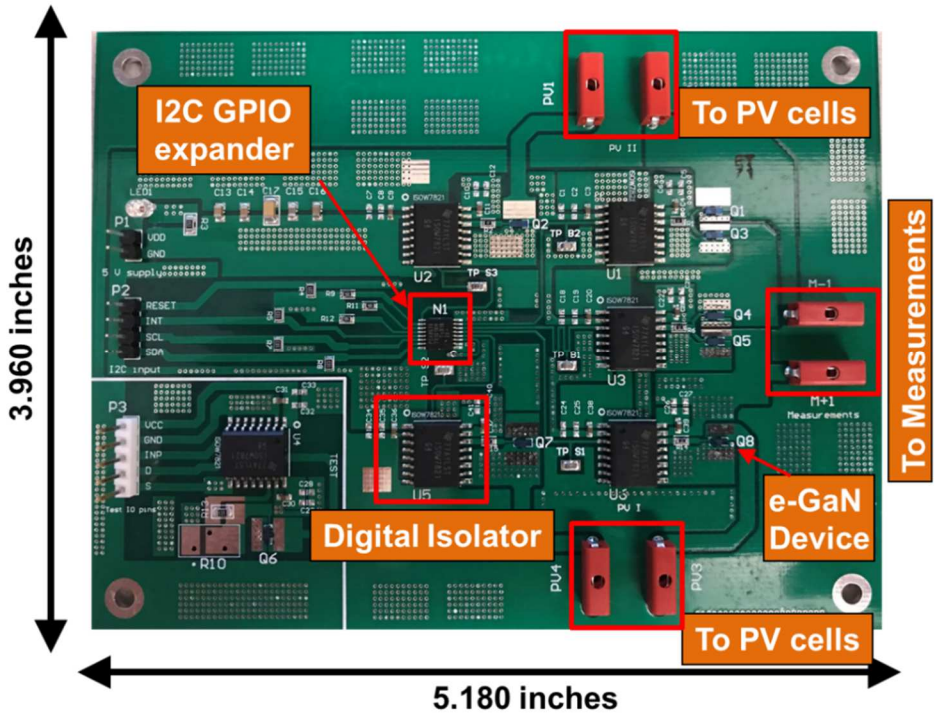


Figure 16: Prototype Switch Module

3.3 Board Layout

The prototype board is implemented as a 2-layer FR4 integrated printed circuit board (PCB) design. The switch design uses the top layer for mounting components and providing critical signal routing, including switching signals. The second layer is used as a continuous ground (GND) plane, with small routing sections. The board has 5 switch structures, with 3 series and 2 bypass switches. The bypass switches have 2 GaN devices with sources shorted to avoid their body diode in the off condition.

The active area of the prototype board is 3.960” x 5.180”. All the pin and component placements are optimized for minimum trace lengths. A wide-trace layout and low resistance I/O plugs are used to minimize losses. Test points are provided at all nodes to help with the debugging. Standoffs are placed at each of the four corners for board mounting. A standalone test structure is also included to characterize a single switch independently.

3.4 Measurement Setup and Results

There are two measurement setups and results described in this section: the test setup for characterizing a standalone test structure and the test setup for complete prototype board. The standalone structure is used to understand the characteristics of a single GaN switch and the complete board setup is used to verify the number of switches and their arrangements.

3.4.1 Test setup for the standalone structure

The measurement setup to study a single GaN is shown in Figure 17. A single PV cell is connected in series with a switch to reduce the variability induced by unequal irradiances and temperatures of multiple PV cells. The GaN switch, shown as EPC 2019 in Figure 17, has an independent gate voltage supply. This will help to provide different V_{GS} voltage values while tracing the I-V curves of the PV cell. There is also an I-V curve without the switch present. That will help to show the power loss due to the switch.

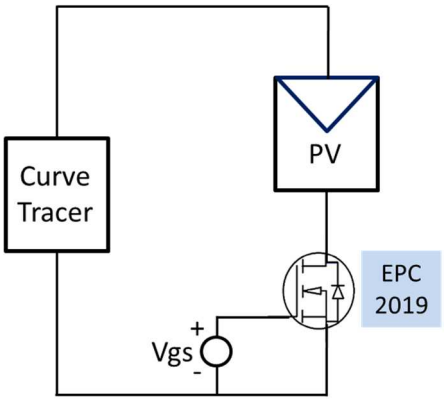


Figure 17: Measurement Setup of Test Structure

3.4.1.1 Measurement results

The I-V curves are shown in Figure 18. The V_{OC} of the individual PV cell at the measurement irradiance is around 4.5 V and I_{SC} of around 0.45 A. A 300W lamp is used for irradiance and it is switched on 15 minutes prior to taking the measurement results. The measurements are for the PV cell without switch and PV cells with GaN switch bias at different bias voltages. All the measurements are taking in the quick succession. The plots with switch biased at V_{GS} = 5V and the one without a switch are considered to study switch

loss. The drop-in voltage was found to be ~30mV. The plots with V_{GS} = 4V and V_{GS} = 5V overlap, confirming that eGaN has small R_{on} with V_{GS} > 4V [14]. This allows us to operate eGaN at V_{GS} = 4V-4.5V. The voltage drop with V_{GS} = 3V from V_{GS} = 5V is 50mV. Beyond V_{GS} = 2V, the transistor shows very high voltage drops.

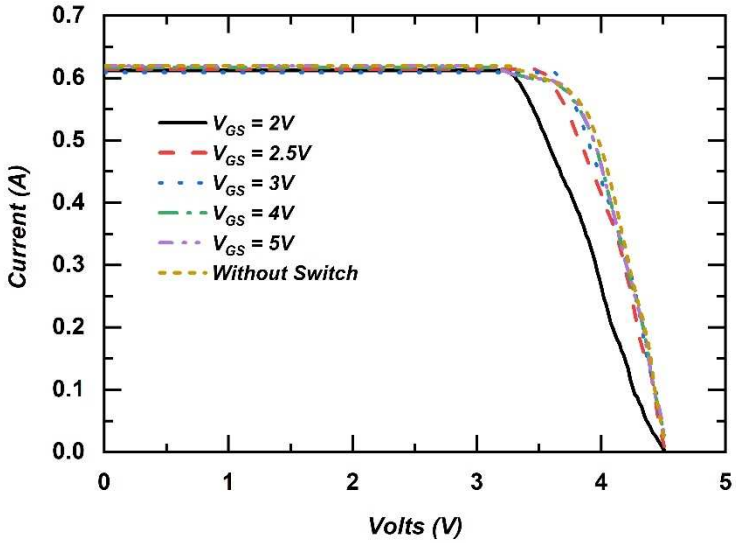


Figure 18: I-V Curves of the Standalone Test Structure

The Table 1 presents with the values of important parameters of the PV cell I-V curves without a switch and with GaN switch biased at different voltages.

Table 1: Parameter Values of IV Curves of the Test Structure

Name	Power	Isc	Voc	Ipeak	Vpeak	Fill Factor
Vgs=2V	2.0	0.635	4.525	0.614	3.251	69.4
Vgs=2.5V	2.2	0.617	4.520	0.617	3.498	77.4
Vgs=3V	2.2	0.623	4.524	0.611	3.629	78.6
Vgs=4V	2.2	0.642	4.524	0.587	3.681	74.4
Vgs=5V	2.2	0.645	4.525	0.590	3.683	74.4
Without_switches	2.2	0.651	4.526	0.587	3.719	74.1

3.4.2 Test setup for switch module

The prototype board measurements are helpful to understand the switch configuration needed to completely control the PV cells. In this section, all the combination of switching is performed, and the results are analyzed to determine the significance of each switch and its arrangement.

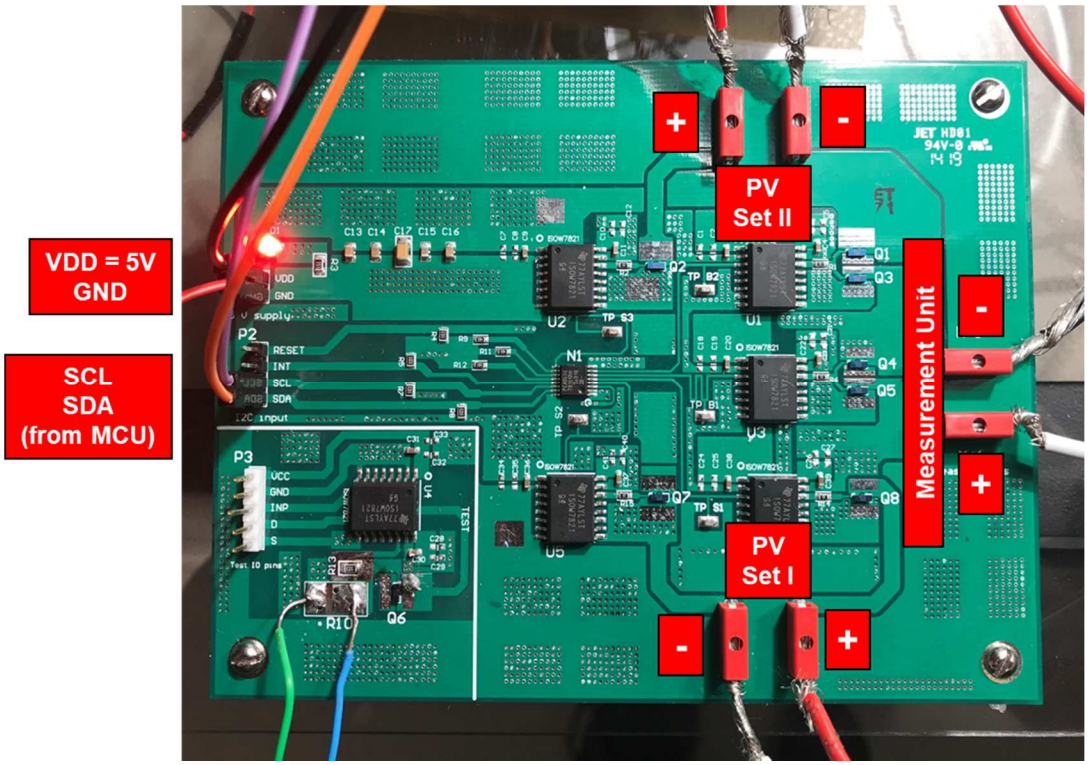


Figure 19: Prototype Board Test Setup

Figure 19 shows the pin connections to the prototype board, and the corresponding labels are shown in Figure 20. The board is powered by a 5V DC power supply. The GPIO expander accepts I2C input, so the serial clock (SCL) and serial data (SDA) input should be generated from a microcontroller. In this test bench, an Arduino Uno board is used to program the expander. The interrupt and the reset pins need not be connected and can be

left open, as I2C has open drain configuration, making them high impedance connections. The PV Set I and PV Set II are the input from the solar panels into the switch configuration. The PV Set I is connected from the top three PV cells in series (in Figure 20) and PV Set II is connected from the bottom two PV cells in series (in Figure 20). The positive and the negative terminals of the PV cells are respectively annotated on Figure 19. The wires from the measurement unit are connected to the curve tracing unit.

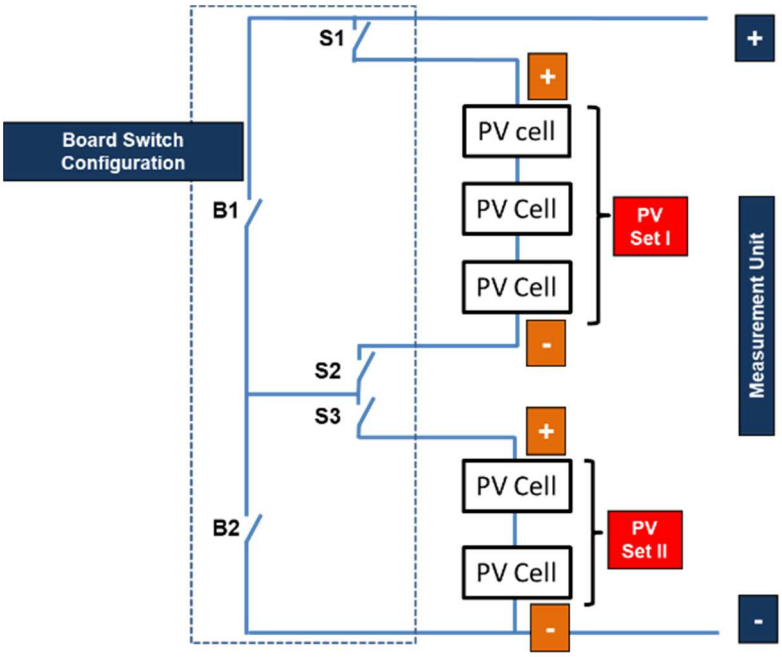


Figure 20: Block Diagram of Test Bench Setup

3.4.2.1 Generating I2C

The I2C serial data for the switch control is generated from the Arduino UNO board. Figure 21 shows the connection between the Arduino and the prototype board.

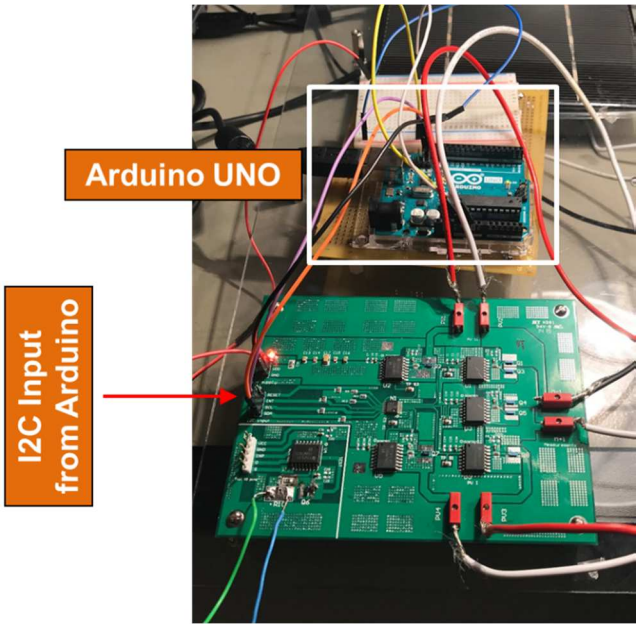


Figure 21: Measurement Setup for I2C Generation

Programming Arduino UNO

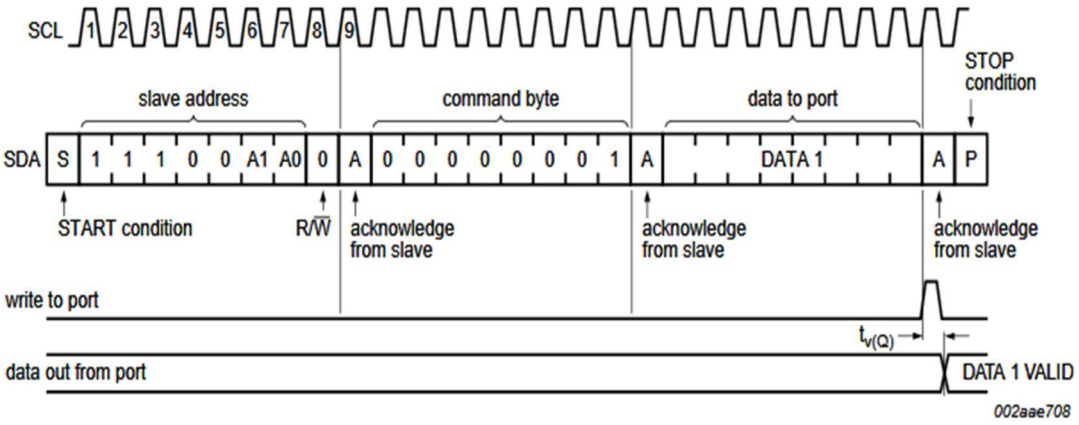


Figure 22: Write Protocol to be Followed for Communication with GPIO Expander

Figure 22 shows the communication protocol to write data onto GPIO expander. First set of 7 bits are address bits. Once the device with the matching address

acknowledges, the command byte is sent which configures the ports as the output ports. After receiving acknowledgment of command byte, the GPIO expander is ready to receive the data. The output ports hold the data sent till the Arduino re-writes the data.

Device address

Since there is only one slave connected to Arduino, there is no need to use the hardware selectable pins shown in Figure 23. They are grounded in our prototype board. That makes the address in binary as '1110000' or '0x70' in hexadecimal numbers. The Wire library of Arduino has very strong functions that makes communication with Arduino very easy.

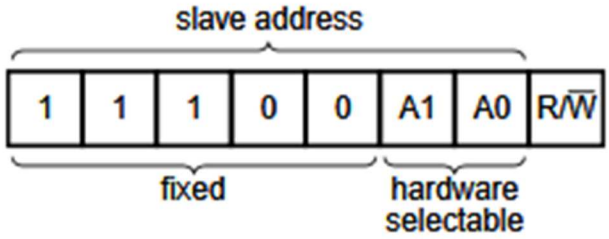


Figure 23: Device Address Bits

Command byte

The command byte is the first byte to follow the address byte during a write transmission. Table 2 has byte value for different register access. After the address, '0x3' should be transmitted to access the configuration register. To transmit data, byte '0x1' should be sent to configure ports as the output ports. When this acknowledge is received, the data is ready to be sent. The bits that control the switches are in the order, S3-B2-B1-S2-S1. For example, if the S3 needs to be switched on, "1" bit must be transmitted.

Similarly, “0” bit for off condition. It is also explained with different combinations in the measured results.

Table 2: Command Byte Register Values

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

Figure 24: DS-100C Curve Tracer

3.4.2.2 Curve tracer

The curve tracer used for the measurement is called DS-100C, manufactured by Daystar Inc. The instrument is shown in Figure 24. The tracer is connected to the computer with RS-232 connector. IVPC is the interfacing software supported by Windows.

Figure 25 shows complete work bench setup. A total of 5 PV cells in the combination of 3-2 are connected to prototype board. The I2C input for the prototype board is generated with Arduino board. I-V curve tracing is done by DS-100C and computer is used to program Arduino and get the data from the curve tracer.

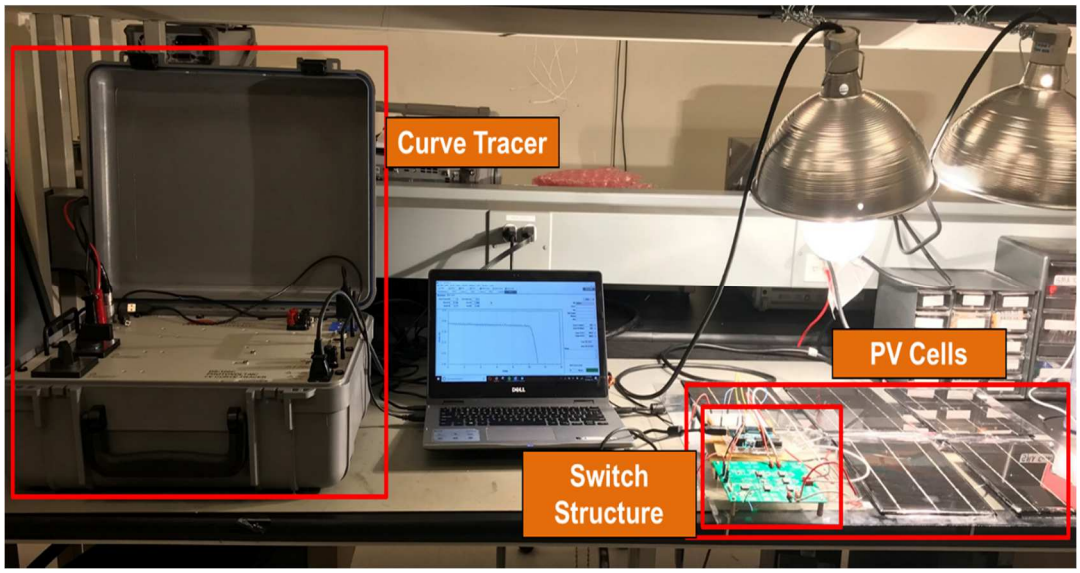


Figure 25: Complete Measurement Setup

3.4.2.3 Measurement results

The I-V curves with all the 5 cells present in series is shown in Figure 26, with switch configuration shown to the left. One of the plot is with the switches included. The other one is I-V curve without the switches present. The difference in the two plots give the switch loss value. Each of the cells have V_{OC} of around 5.5V that verifies that all the 5 cells are in series in the I-V plot. The drop of ~90mV is observed close to the maximum power point. This is due to 3 switch switches present in the current path. The parameters of the I-V curves are also shown in the included table.

Figure 27 shows 3 cells in series, hence the V_{OC} is ~14V. In this configuration, 3 cells of PV Set I are in series. The same PV Set I cells are connected independently to measure to loss, drop of ~89mV was observed with the switches connected.

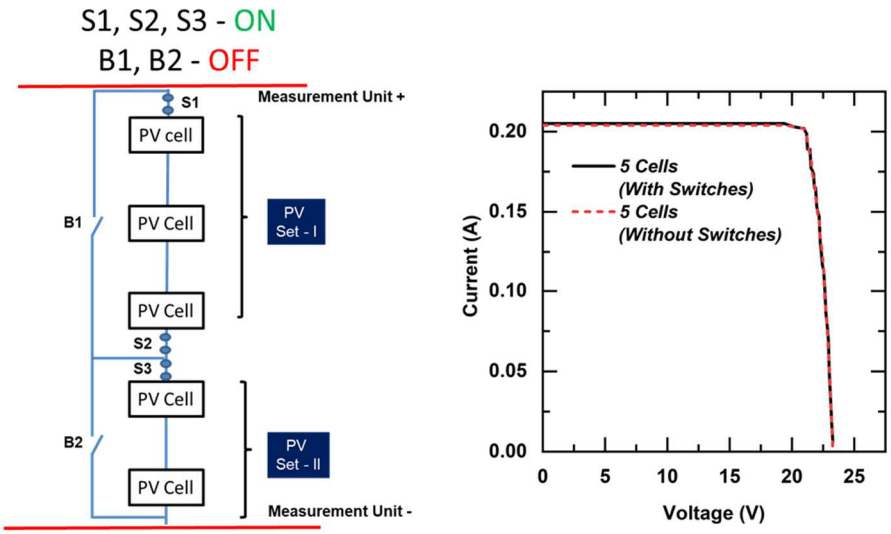


Figure 26: I-V Curve Plot-1 with 5 Cells in Series

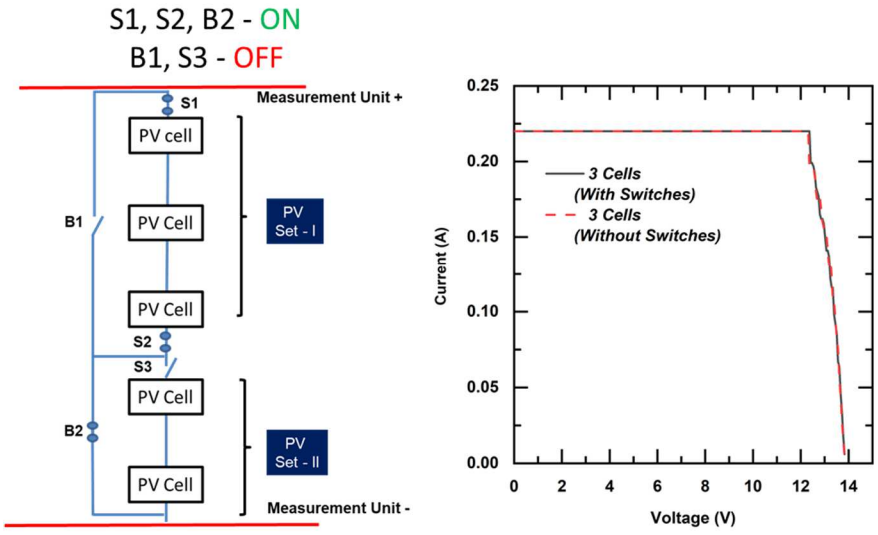


Figure 27: I-V Curve Plot-2 with 3 Cells in Series

In the configuration shown in Figure 28, 2 cells of PV Set II are in series and the V_{OC} of plots verifies the same. The same PV Set II cells are connected independently without the switches to measure to loss, drop of ~76mV was observed with the switches connected.

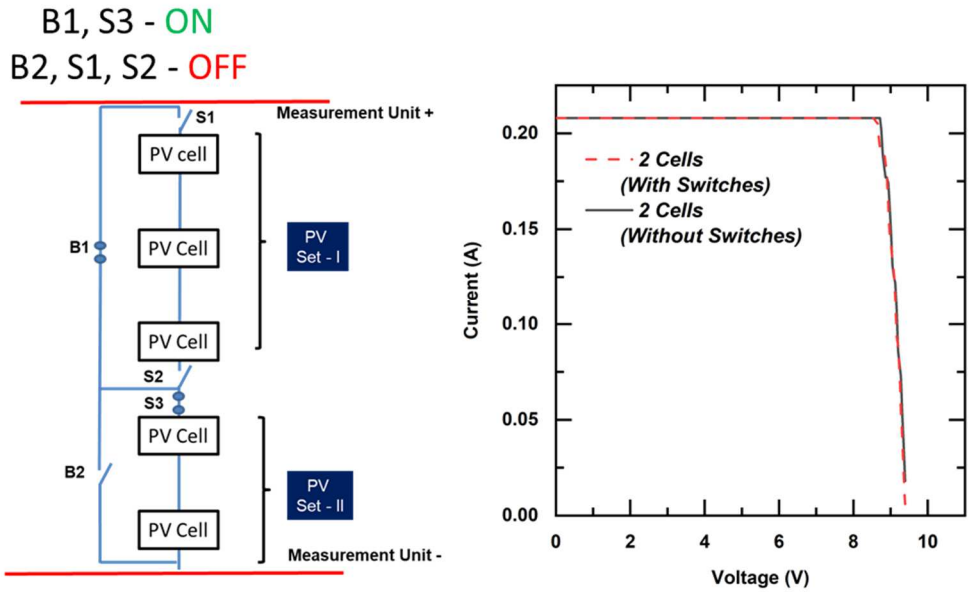


Figure 28: I-V Curve Plot-3 with 2 Cells in Series

3.4.2.5 Bi-directional operation of GaN switches

Connections of PV cells and measurement unit for both the direction of current is shown in Figure 29. All the connections are interchanged which reverses the direction of current through the PV cells. The operation of all the 3 switch configurations were verified, confirming eGaN as bi-directional switch and the results are shown in Figure 30.

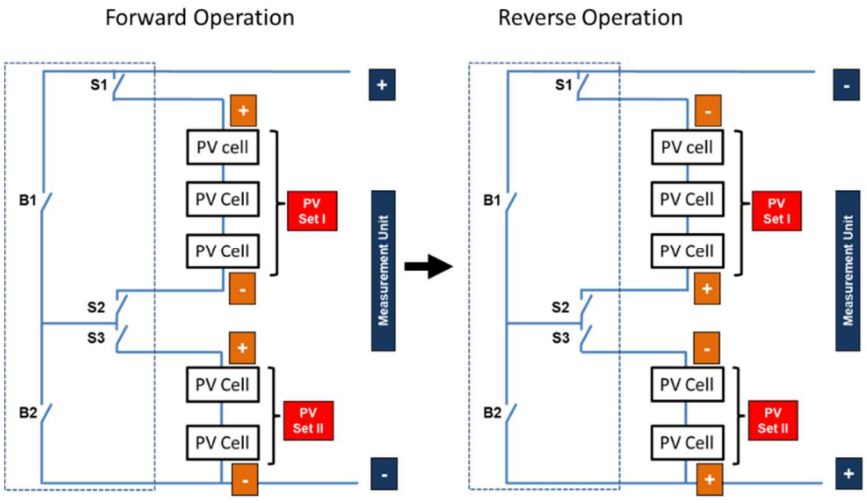


Figure 29: Connections for Bi-directional Current Flow

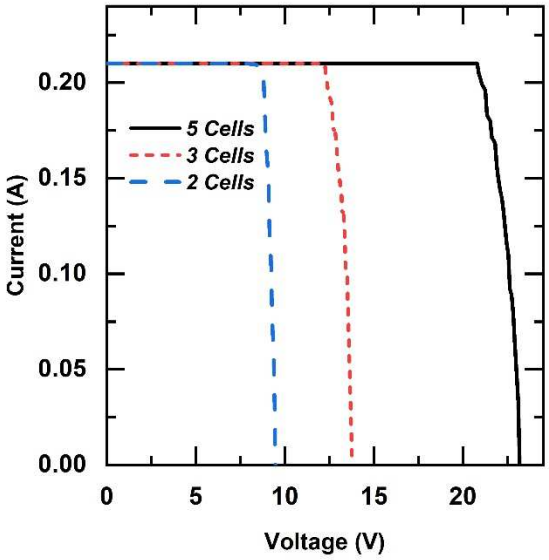


Figure 30: Measurement Results of Different Configurations for Reverse Current Direction

3.4.2.6 By-pass switch configuration

The bypass switches are designed with 2 GaN devices with their sources tied together to stop the leakage of current through its body diode. Figure 31 shows the two

GaN topologies and their placement on the prototype board. As the body diode of both the source connected GaN are in opposite direction, the voltage across the bypass GaN switch does not matter as there will not be any leakage through body diodes. Prototype board was tested by removing one GaN at-a-time to see if this problem could be fixed with a single GaN as a bypass switch. Measurement plots show that one of the GaN does not see leakage through it and can be used independently.

Figure 32 shows that with the bottom GaN shorted, the source voltage (negative terminal) of the top GaN is less than drain (positive terminal) and there should not be any leakage through the body diode. This is confirmed by the plots shown. This switch topology works for all 3 configurations.

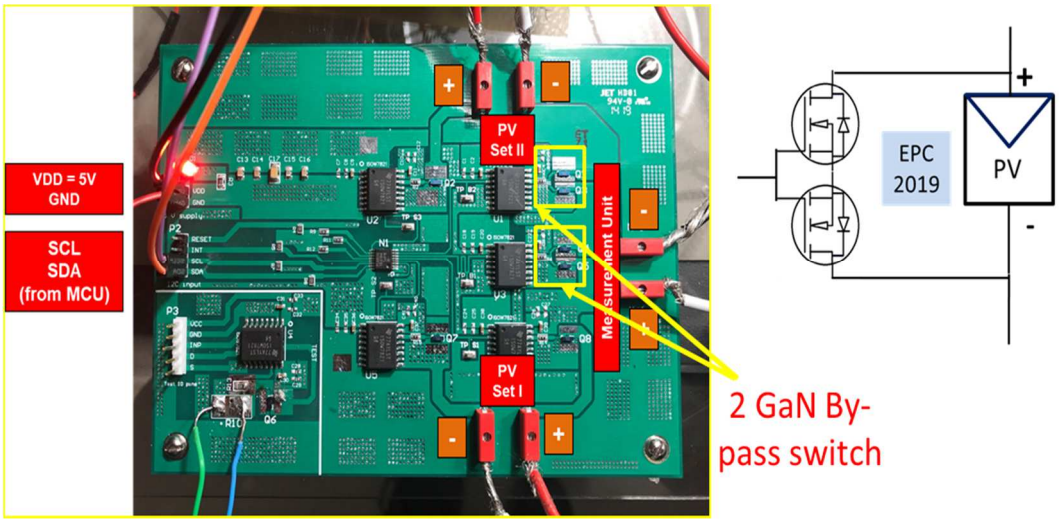


Figure 31: Bypass Switch 2 GaN Topology

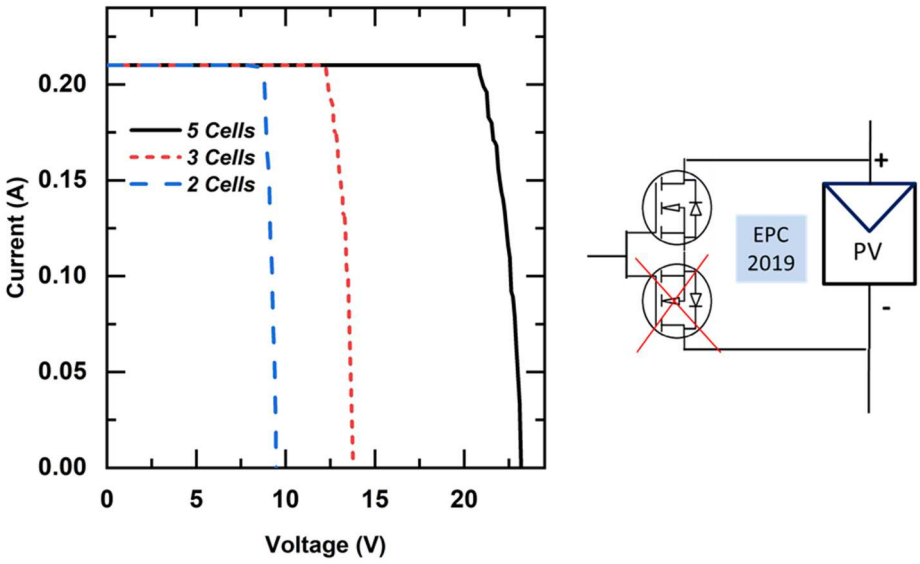


Figure 32: Single GaN Bypass Topology Working Correctly

Figure 33 shows that with the top GaN shorted, source voltage (pos terminal) is more than drain (neg terminal). This topology does not work when bypass is off. The plots show the leakage when this switch is off (5-cells and 2-cells).

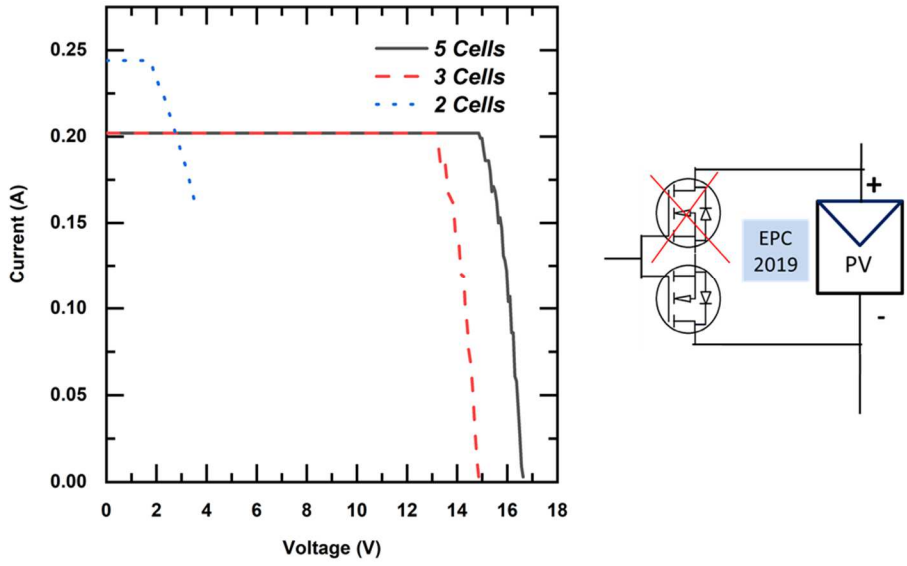


Figure 33: Single GaN Bypass Topology with Current Leakage

3.5 MATLAB Simulation of a 1kW Satellite System

This section has simulated results of MATLAB code for a 1kW satellite system. The measured switch loss values are considered to extrapolate switch losses in a 1kW satellite power system. Measurement results show reduction of about 30mV for a single GaN switch. A 1kW satellite system is considered with a 100V bus voltage, with V_{OC} and I_{SC} of individual cells as 4.67V and 0.22A respectively.

Figure 34 shows the IV curve a single PV cell with and without the switch losses. R_{ON} of 0.14Ω was introduced as on resistance for switch loss simulation. This gives 30mV drop in voltage near the maximum power point. Maximum power generated by single PV cell shown in Figure 34 with and without switch losses are 0.799W and 0.8049W respectively. This gives the percentage loss of 0.73% for a single cell.

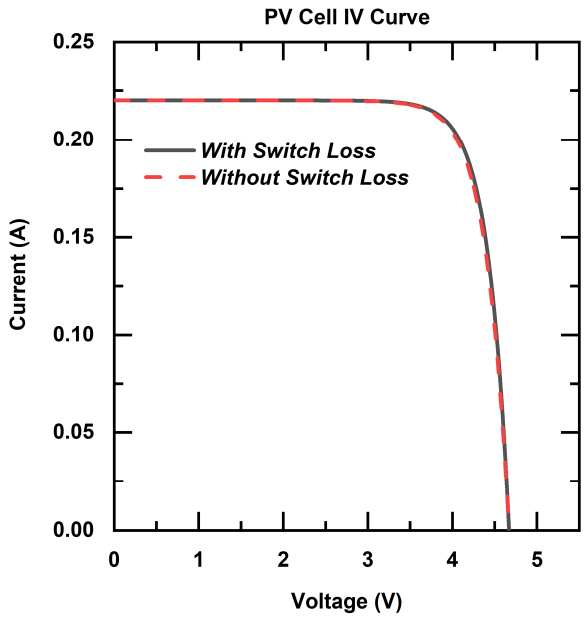


Figure 34: IV Curves of a Single PV Cell with and Without Switch Loss

To generate and maintain a bus voltage of 100V (which is the requirement in satellite power systems), 28 PV cells are simulated in series (in multiple of 4, as the switch module is designed for set of 4 cells). To get 1kW output power from the system, 45 strings of PV cells are simulated in parallel connection.

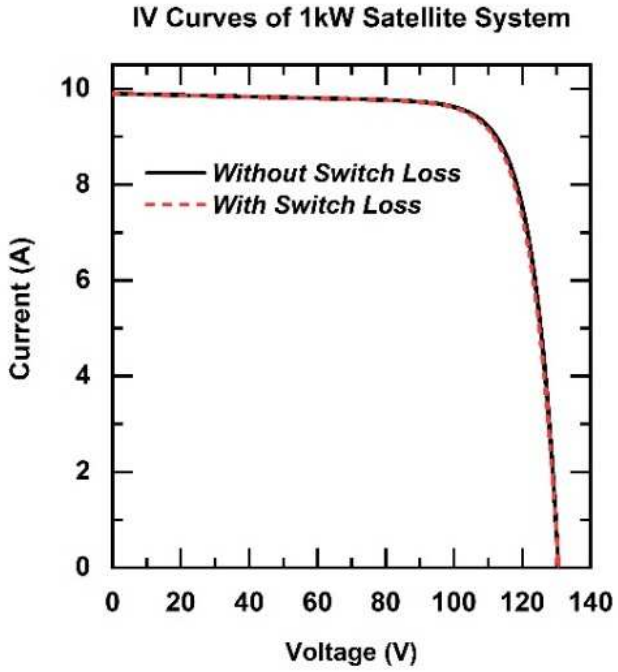


Figure 35: IV Curves of a 1kW Satellite Power System with and without Switch Loss

Figure 35 shows the IV curve of a 1kW satellite power system with and without switch losses. Maximum power generated by this system with and without switch losses are 1.013KW and 1.006W respectively. This gives the percentage loss of 0.72% for the complete system, which is acceptable. Furthermore, the system simulated above has 1-cell resolution. The losses can be significantly reduced by increasing the resolution, thereby reducing the number of switches.

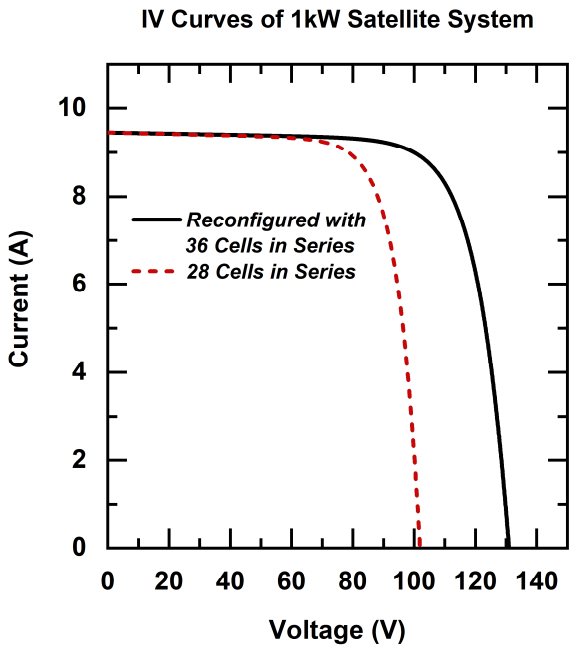


Figure 36: IV Curves of a 1kW Satellite Power System with and without Reconfiguration at the End-of-life (EOL)

Figure 36 shows the advantage of dynamic reconfiguration in a satellite power system at the end of life (EOL). The PV cells show 22% reduction in V_{OC} and 7% reduction in I_{SC} throughout their lifetime [10]. Reconfiguration allows 8 cells to be added in series. This helps to maintain the bus voltage of 100V. These extra 8 cells could be used as an auxiliary power source in the beginning, when only 28 cells are sufficient to maintain 100V bus voltage. However, without reconfiguration, these 8 cells would have to be hardwired in series wasting the extra power since the bus voltage would well exceed 100V requirement.

4 INTEGRATED CIRCUIT DEVELOPMENT

The prototype board designed shows the feasibility of having a solar array reconfiguration structure. However, to make the switch controller compact and low-mass, silicon-based CMOS-integrated controller and power switch driver is necessary.

4.1 SWITCH ARRANGEMENT

The main challenge for the proposed controller integrated circuit (IC) is providing the correct floating gate drive voltages for the power switches (GaN devices). These floating voltage generators must read the PV cell voltages (where the GaN sources are connected) and provide appropriate gate drive voltages for GaN devices to control them. It is shown in Figure 37. Since the source voltage varies with the PV cell voltage, the floating gate voltage also must be generated correspondingly.

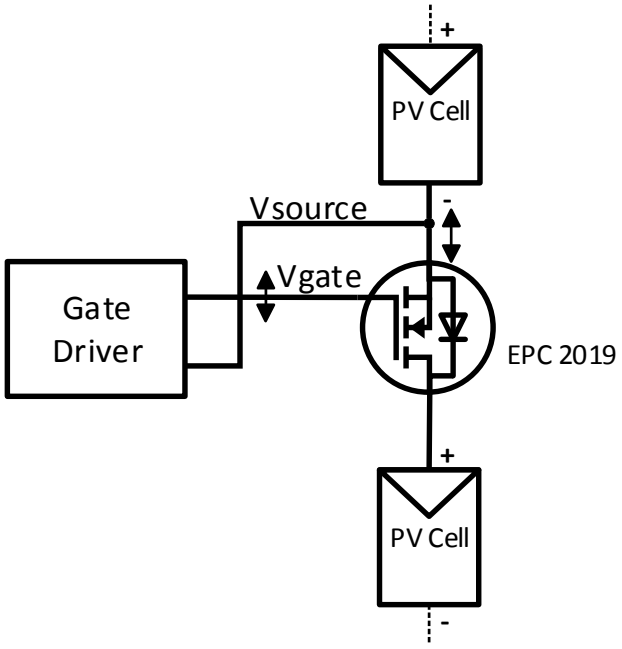


Figure 37: Floating Gate Drive Voltage Generation

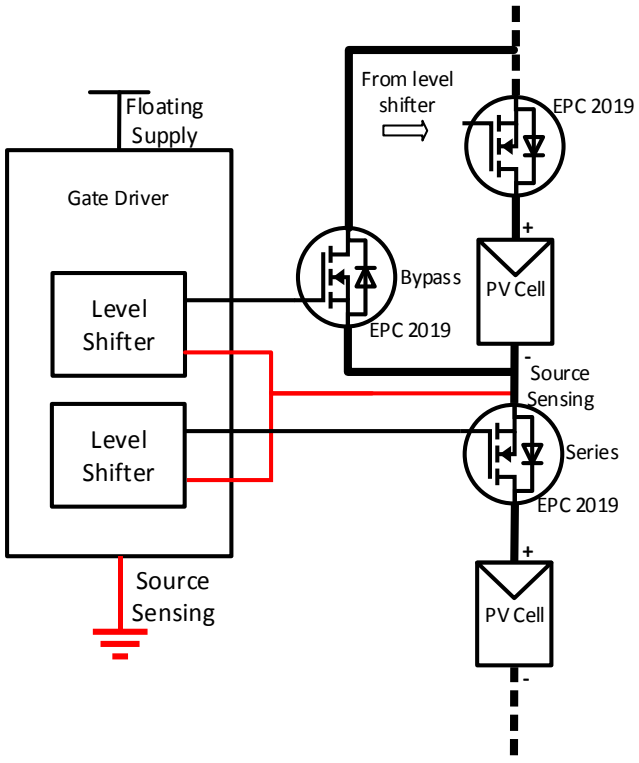


Figure 38: Series and Bypass Switch Topology

Figure 38 shows the series and bypass switch topology. The prototype measurement result confirmed the working of this topology. The series and the bypass switch share a source node with each other. Hence, a single floating voltage can supply the correct gate drive voltage and area on chip is saved. This adds load to the supply, but simulations show small decrease in supply voltage.

4.1 Top Level Architecture

The integrated circuit (IC) solution adopts switched capacitor converter topology to generate these floating voltages. This is due to the ease of integration on chip. The proposed design employs high switching (clocking) speeds of 5MHz to reduce the passive device sizes. The switched capacitor circuit has capacitive coupled level shifter driver

circuits to generate appropriate control voltages. This integrated circuit (IC) has clock generation in two voltage domains. The non-overlapping clock phases are generated in 1.8V domain and then the signals are converted to 5V domain with the level shifters to drive the switched capacitor circuits. The use of 1.8V devices is to reduce the power consumption and to make the design radiation robust as the low voltage devices have shown to be immune to total dose radiation effects.

Figure 39 shows the architecture diagram of the proposed IC implementation. The IC is powered by a 5V DC supply. GaN device EPC 2019 is selected as the power switches and it is controlled by the IC designed in CMOS process technology of XFAB's XT018 (180nm) process. The serial data and the clock are generated by a microcontroller and are sent through an I2C protocol. This I2C serial data is then fed to a GPIO expander that converters it into analog signals. The switched capacitor converter reads the source voltage and provides 5V higher than that voltage. The clock phases generator provides non-overlapping clock phases to switched capacitor circuit. The GaN level shifter driver circuit helps to convert the ground referenced logic to the floating ground. The output from the level shifter is responsible to control the GaN switches.

4.2 PV Cell Verilog Model

The modelling of the PV cells to simulate the load connected in between the GaN switches is very important to verify the voltage condition throughout the circuit. The PV cell is modelled in Verilog-A based on the single diode model [18]. Figure 40 shows the PV cell symbol and I-V curve plot of a single cell. For a single PV cell, the open circuit voltage is 4.67V and the short circuit current is 0.22A.

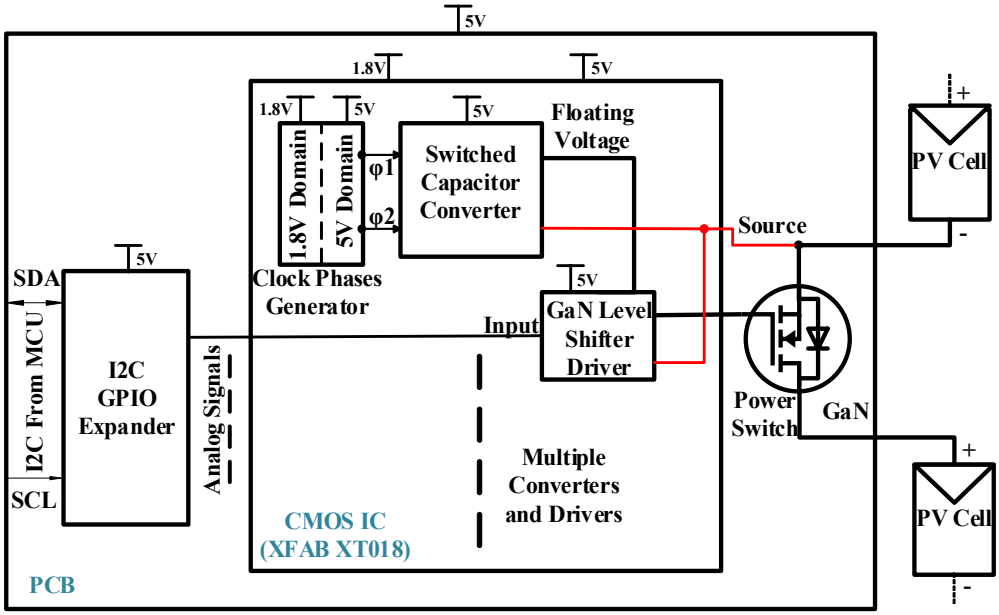


Figure 39: Top Level Architecture of the IC Development

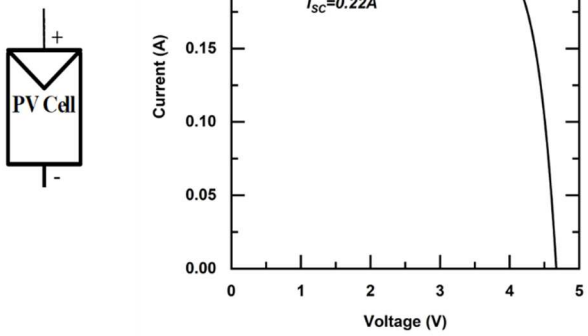


Figure 40: PV Cell Symbol and I-V Curve

4.3 Clock Phases Generator

The clock circuit block is used to provide the non-overlapping clock phases to switched capacitor converter circuit. This section provides a detailed implementation of

the clock circuit blocks. All the circuits used in this block are discussed along with their simulation results.

Figure 41 shows all the circuits involved in the generation of non-overlapping clock signals. Beta-multiplier circuit is used to provide biases for current starved oscillator [19]. The current starved oscillator generates the clock signal. Non-overlapping clock generator circuit provides non-overlapping clock phases in 1.8V domain. The level shifter circuit coverts the voltage levels of both the clock phases from 1.8V to 5V. Buffers are used to maintain signal swing and equal rise and fall times.

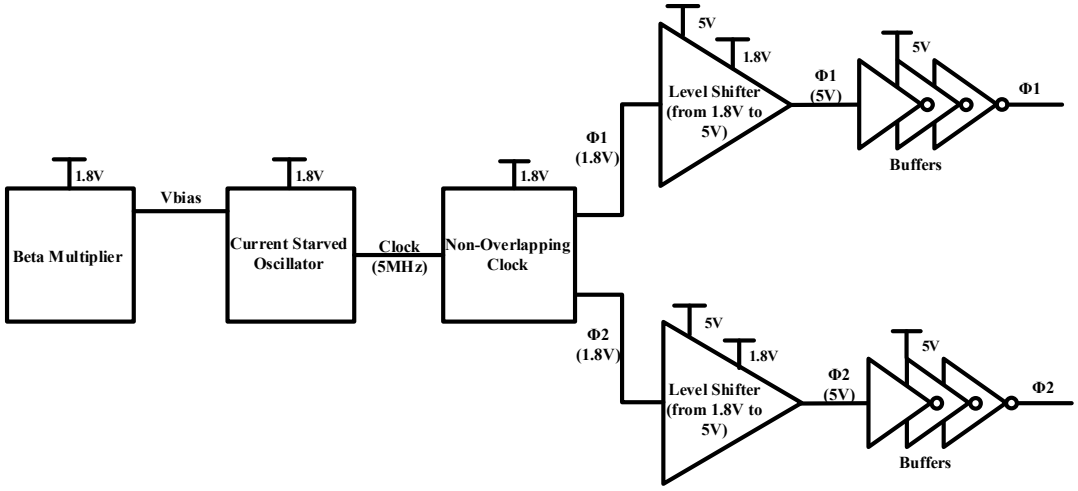


Figure 41: Signal Flow Diagram

In the following sub-sections, all the circuits are individually discussed with the simulation results.

4.3.1 Current starved oscillator

Ring oscillator is designed with voltage-controlled topology. The frequency of this oscillator depends on the number of stages and the bias voltages, which control the delay

of each stage [20]. Figure 42 shows the ring oscillator used to generate the clock signal. A 7-stage ring oscillator is designed in open loop with the frequency generation of around 5MHz. Beta multiplier and current mirror circuits are used to generate the bias voltages, as the bias voltages need not be very precise. Inverter buffers are used at the output to maintain the equal rise and fall time. Figure 43 shows transient plot of the generated output. The generated output is 1.8V signal.

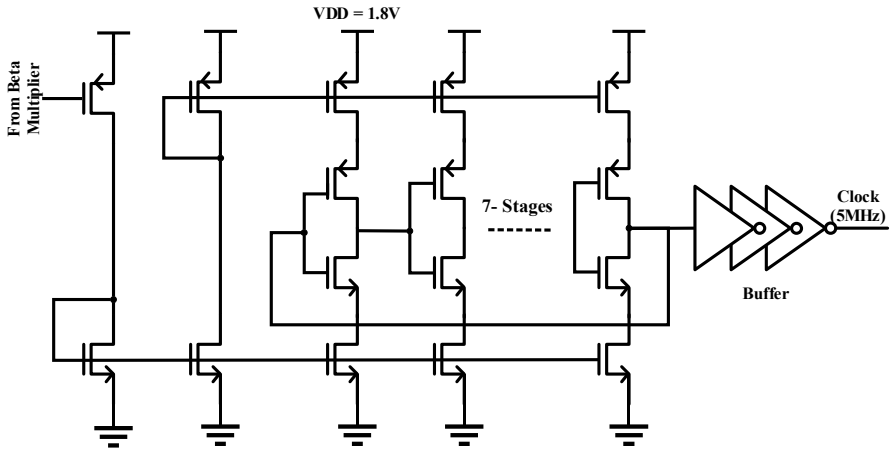


Figure 42: 7-stage Current Starved Ring Oscillator

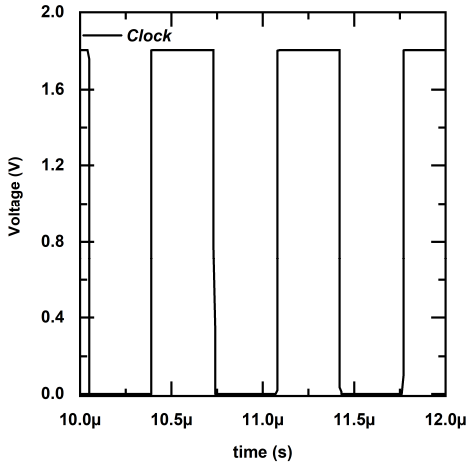


Figure 43: Transient Plots of Clock Output

4.3.2 Non-Overlapping Clock

Figure 44 shows the standard cross coupled non-overlapping clock generator circuit [21]. The clock voltage generated from the oscillator is the input of this circuit and the outputs are the two phases which are completely isolated with around 20ns of dead time. Small delay capacitor of 200fF is used on the delay line to reduce the number of stages and obtain enough delay in the operation. Figure 45 show the transient plot of both the phases.

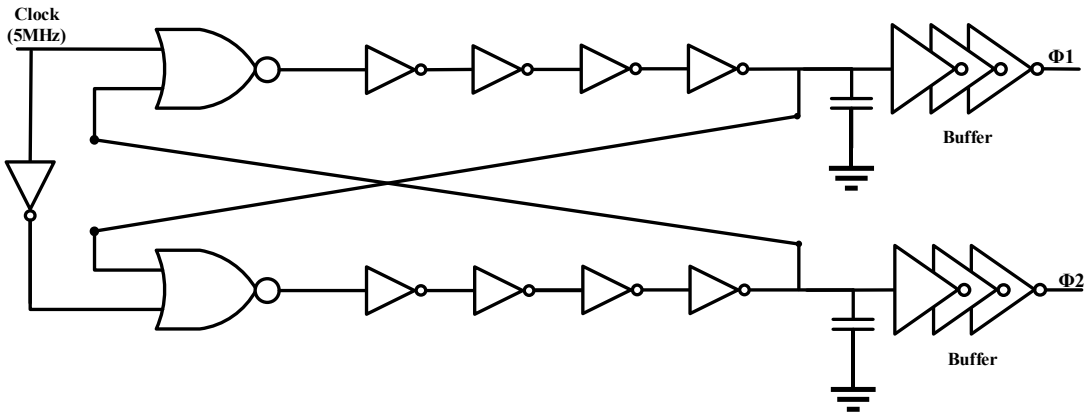


Figure 44: Schematic Diagram of Non-overlapping Clock Generator

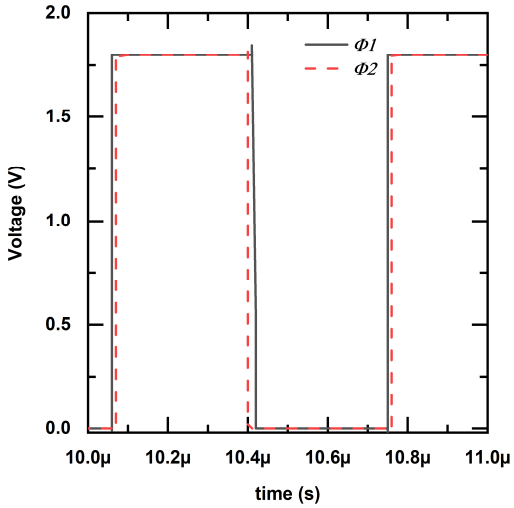


Figure 45: Transient Plots of Non-overlapping Clock Phases

4.3.3 Level shifter (from 1.8V to 5V)

The circuit of a conventional level shifter is shown in Figure 46 [22]. This circuit is used to convert 1.8V domain clock phases into 5V domain clock phases. This level shifter has latch topology to maintain the appropriate output values. Large buffers are added at the output to drive the switched capacitor switches. Figure 47 shows the output plots of the level shifted clock phase.

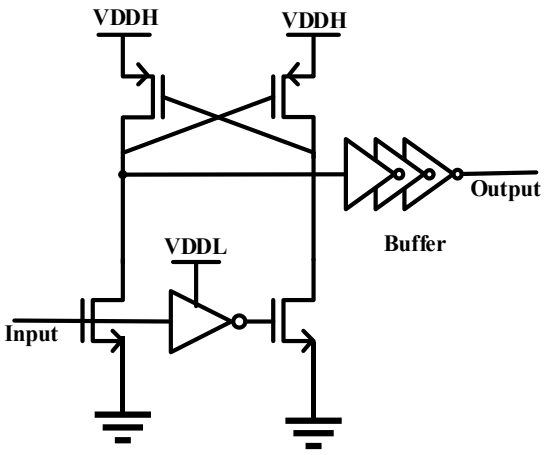


Figure 46: Schematic of Level Shifter Circuit from VDDL = 1.8V Domain to VDDH = 5V Domain

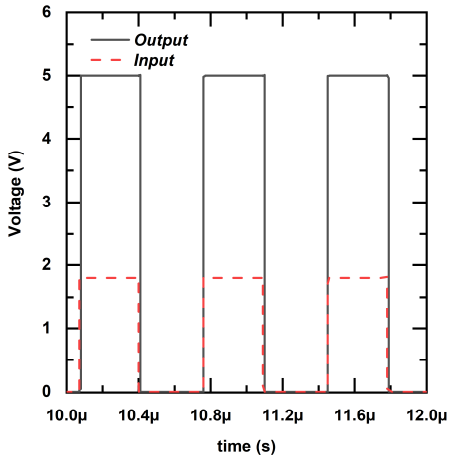


Figure 47: Transient Plots of Level Shifted Clock Phase

4.4 Switched Capacitor Converter Circuit

4.4.1 Overview

Figure 48 shows the behavior diagram of the switched capacitor converter circuit in open loop. When clock Ø1 is high, the Cfly capacitor is charged to 5V and when clock Ø2 is high, the bottom plate of the Cfly capacitor is connected to the floating node (source node of the GaN switch) and the top plate provides the Δ5V with respect to the floating node voltage. However, in the Ø2 cycle, due to the charge sharing of Cload with C_{GS} of GaN, the output voltage will always be less than Δ5V corresponding to the floating node voltages [23]. Since the intermediate node voltages see high voltages, the capacitor switches need to have high V_{DS} breakdown voltages. The super-junction transistors available in XFAB's XT018 process are used as they have very high breakdown voltages [24]. However, as these devices have very high R_{ON} and there is significant switching losses.

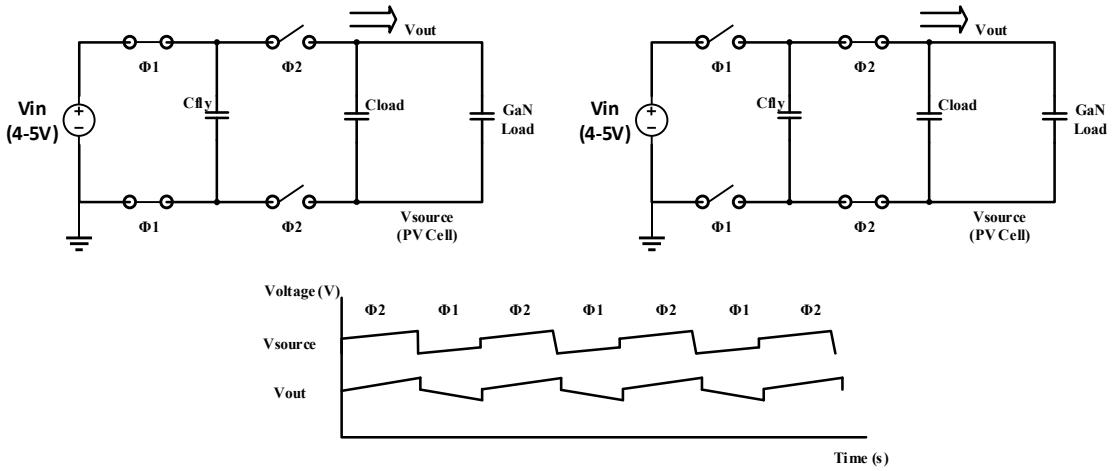


Figure 48: Schematic Diagram of SC Converter

4.4.2 Capacitively Coupled Level Shifter - N

The schematic of capacitively coupled Level shifter that has the N-type DMOS transistors cross coupled is shown in Figure 49 [25]. It is a modified version of the voltage doubler circuit. The output of this capacitive coupled level shifter can drive the transistor by reading the SRC node and providing 5V drive above that node. This is due to bias set by the cross coupled transistors at the output. Figure 50 shows the transient plots of input, output and SRC voltages. SRC voltage is 5V and the output swing is from 5V to 10V. The output of this level shifter is used to drive N-type load because it provides the gate drive voltage above the SRC voltage of NMOS.

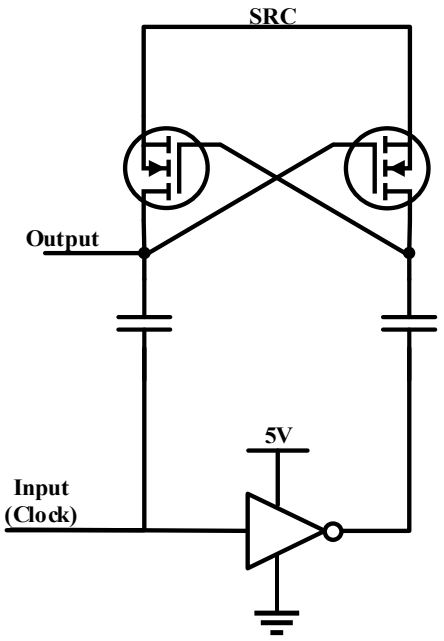


Figure 49: Schematic Diagram of N-Level Circuit

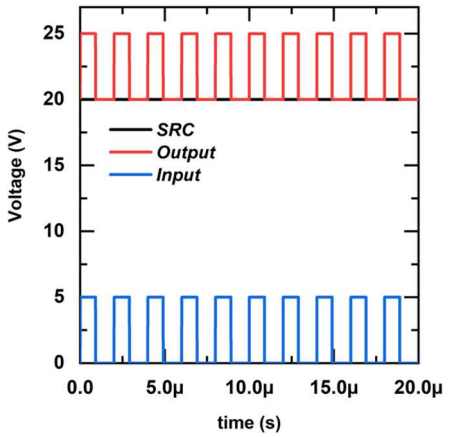


Figure 50: Transient Plots of Output of N-Level Shifter Circuit

4.4.3 Capacitively Coupled Level Shifter - P

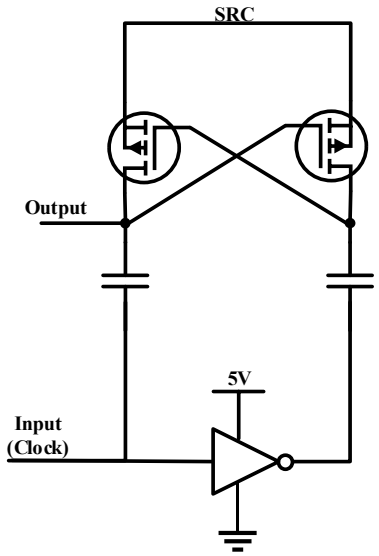


Figure 51: Schematic Diagram of P-Level Circuit

The schematic of capacitively coupled Level shifter that has the P-type DMOS transistors cross coupled is shown in Figure 51 [26]. The output of this capacitive coupled level shifter can drive the transistor by reading the SRC node and providing 5V drive below that node. This is due to bias set by the cross coupled transistors at the output. Figure 52

shows the transient plots of input, output and SRC voltages. The output of this level shifter is used to drive P-type load because it provides the gate drive voltage below the SRC voltage of PMOS.

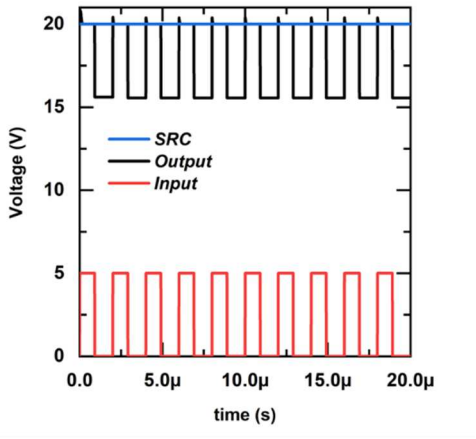


Figure 52: Transient Plots of Output of P-Level Shifter Circuit

4.4.4 Switch Capacitor Converter

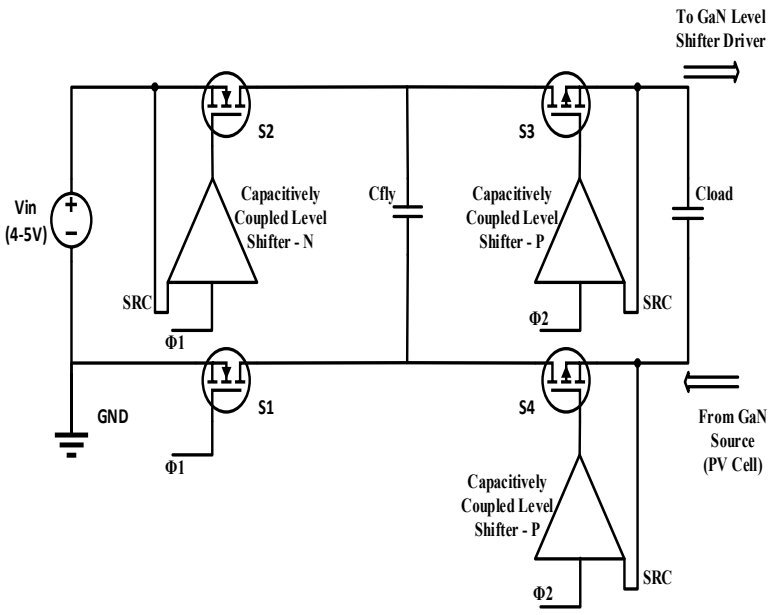


Figure 53: Switched Capacitor Converter Circuit

The complete switched capacitor converter circuit is shown in Figure 53. Switches S1 and S2 are N-type transistors and switched S3 and S4 are P-type transistors. This is decided after considering the node V_{DS} voltages seen by these transistors. Switch S2 is driven by capacitively a coupled level shifter-N and switches S3 and S4 are driven by capacitively coupled level shifter-P. The floating output of the switched capacitor converter circuit is shown in Figure 54.

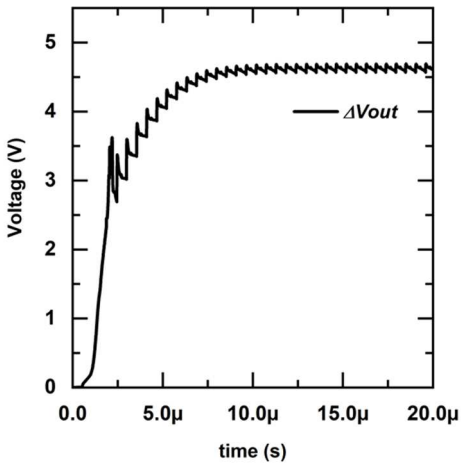


Figure 54: Transient Plot of Switched Capacitor Converter Circuit Output

4.5 GaN Level Shifter Driver

The output of the switched capacitor circuit provides the voltage supply to level shifter and inverter buffers circuits. The level shifter employed here is a traditional clamped level shifter with diode connected transistor to maintain the output voltage [27]. This architecture needs high breakdown voltage transistors. The input to the level shifter is a DC ground referenced voltage, determining the switch condition as on or off. Figure 55 shows the schematic of the level shifter circuit to drive the GaN load. Figure 56 shows the

output of the Level shifter with respect to the floating voltage. This voltage is always less than 5V that ensures the voltage less than V_{GS} breakdown of GaN.

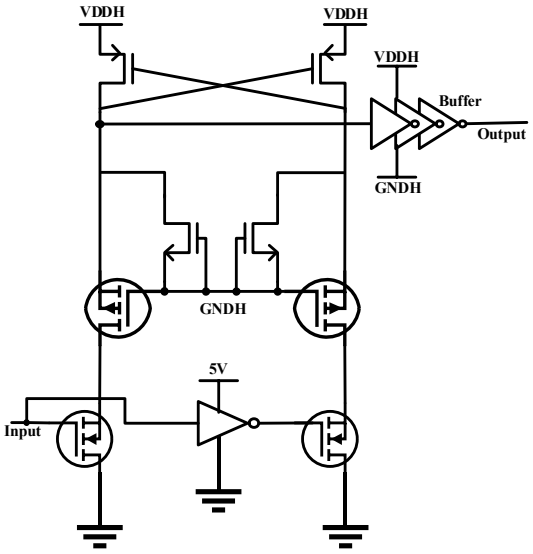


Figure 55: GaN Level Shifter Driver Circuit

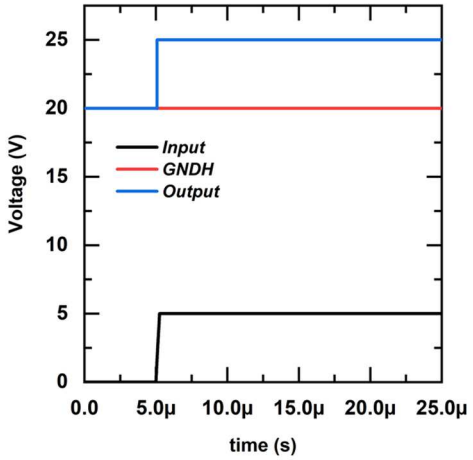


Figure 56: Transient Output Plot of GaN Level Shifter Driver

4.6 System Level Simulation

The system level setup shown in Figure 57 is type – I reconfiguration topology. This topology is verified from the measured prototype board. A single CMOS controller

integrated circuit (IC) can control 8 switches in total (4 series and 4 bypass switches). As a series and a bypass switch (GaN) shares a source node, same switched capacitor converter can be used to provide the floating voltages.

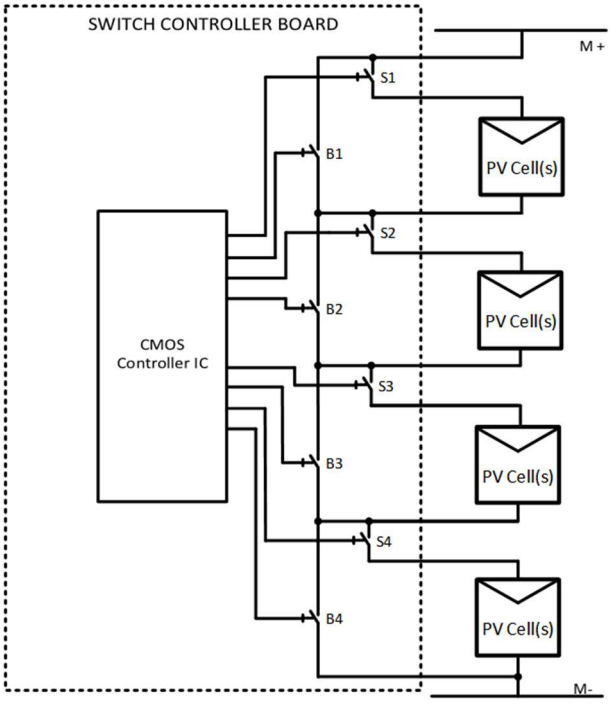


Figure 57: CMOS Controller IC Setup

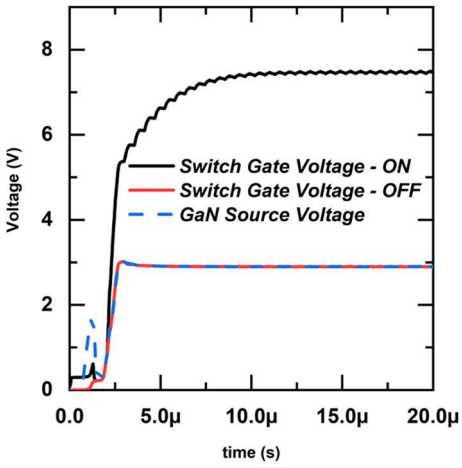


Figure 58: Floating Switch Control Voltages

Figure 58 shows the GaN gate drive voltages. The input is ground referenced 5V signal and the output voltage is floating corresponding to the source node voltage of the GaN. The source node here is 3V and the on-gate voltage is 7.6V and the off-gate drive voltage is 3V.

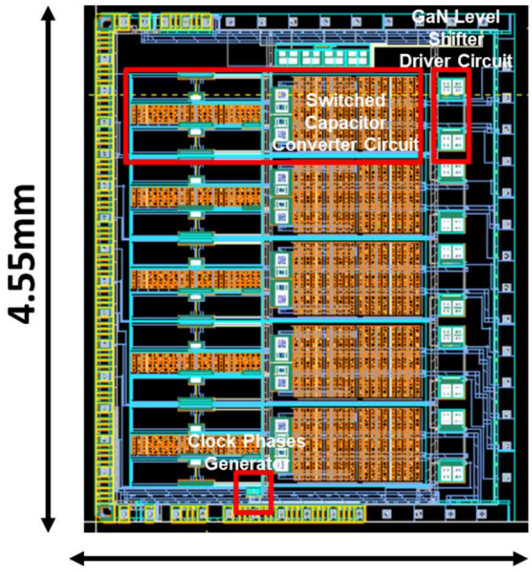


Figure 59: Complete Layout with 5 Converters

Figure 59 shows the complete layout in the allowed die area. This is the extent of work that could be submitted in this thesis report due to deadline.

5 CONCLUSION

The need for solar array reconfiguration was defined and a prototype board was fabricated to verify the topology of solar array reconfiguration. The measurement results from this board helped to design a compact and low-mass silicon-based CMOS-integrated controller. Due to timing constraints, the measured integrated circuit (IC) results could not be shared. However, all the post layout simulation results are shown. The measurement results of the prototype board with commercial-off-the-shelf components (COTS) show the switch on resistance as R_{ON} = 0.14Ω. MATLAB simulations for 1kW satellite power system was done with V_{OC} and I_{SC} of individual solar cells as 4.67V and 0.22A respectively. Simulations show the total power loss due to switches as 0.72%. This loss is very small compared to the power saved by reconfiguration.

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