Time-Domain/Digital Frequency Synchronized Hysteresis Based Fully Integrated Voltage Regulator

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved June 2019 by the
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ARIZONA STATE UNIVERSITY

December 2019

ABSTRACT

Power management integrated circuit (PMIC) design is a key module in almost all electronics around us such as Phones, Tablets, Computers, Laptop, Electric vehicles, etc. The on-chip loads such as microprocessors cores, memories, Analog/RF, etc. requires multiple supply voltage domains. Providing these supply voltages from off-chip voltage regulators will increase the overall system cost and limits the performance due to the board and package parasitics. Therefore, an on-chip fully integrated voltage regulator (FIVR) is required. The dissertation presents a topology for a fully integrated power stage in a DC-DC buck converter achieving a high-power density and a time-domain hysteresis based highly integrated buck converter. A multi-phase time-domain comparator is proposed in this work for implementing the hysteresis control, thereby achieving a process scaling friendly highly digital design. A higher-order LC notch filter along with a flying capacitor which couples the input and output voltage ripple is implemented. The power stage operates at 500 MHz and can deliver a maximum power of 1.0 W and load current of 1.67 A, while occupying 1.21 mm^2 active die area. Thus achieving a power density of 0.867 W/mm^2 and current density of 1.377 A/mm^2. The peak efficiency obtained is 71% at 780 mA of load current. The power stage with the additional off-chip LC is utilized to design a highly integrated current mode hysteretic buck converter operating at 180 MHz. It achieves 20 ns of settling and 2-5 ns of rise/fall time for reference tracking. The second part of the dissertation discuss an integrated low voltage switched-capacitor based power sensor, to measure the output power of a DC-DC boost converter. This approach results in a lower complexity, area, power consumption, and a lower component count for the overall PV MPPT system. Designed in a 180 nm CMOS process, the circuit can operate with a supply voltage of 1.8 V. It achieves a power sense accuracy of 7.6% , occupies a die area of 0.0519 mm^2, and consumes 0.748 mW of power.

To my spiritual guru

H.H Sant Shri Asharam Ji Bapu

for his teachings of Sanatan Dharm

& to my parents

for their sacrifices, care, and love

ACKNOWLEDGMENTS

I am extremely grateful to Prof. Sayfe Kiaei for giving me the opportunity to work on the challenging projects. His teachings are not only limited to circuits but extend much further. He gave me all the resources and freedom to execute my ideas and believed in me. I am also very thankful to Prof. Bertan Bakkaloglu whose technical expertise, continuous guidance, and support were of invaluable help to my research. And to both the professors for giving me the opportunity to teach in EEE433/591 and EEE523 courses, which gave me another dimension to my career and platform to demonstrate my teaching capability. Also, their constant motivation helped me to deliver better throughout my graduate studies. Thanks to Prof. Jennifer Kitchen for taking the time to serve as a committee member. Thanks to Prof. Hongjiang Song for serving as a committee member and to teach some of the best courses at ASU, the learning from these courses goes beyond circuit design. Thank you to all the professors at ASU for teaching me the advance courses in Analog and Mixed Signal/RF IC design and making me a better engineer.

This research would not have been possible without the financial support of NXP Semiconductors, Chandler, AZ, USA. My special thanks to Bin Shao, Jim Spehar, John Pigott, and the entire team at NXP for providing the valuable feedback during the technical reviews and support throughout the project. Also, thanks for allowing me to use the lab at NXP for the measurements.

I want to thank my seniors and alumni of our lab, Dr. Navankur Beohar and Vivek Parasuram for being my mentor in both personal and professional life, for guiding me and extending their help at every occasion. Dr. Debashis Mandal, Dr. Raveesh Magod, Amit Kumar, Sidhanto Roy, Dr. Amir Ayati, and Dr. Chai Yong Lim for always being there to help me in every step during the graduate studies. Even after graduating from ASU, they were available whenever I needed them.

Kishan Joshi and Bhushan Talele were not only great friends but for me, they were mentors too, their technical expertise was a great help in my project on several occasions. Also, thanks to my colleagues Rakshit Nayak, Shashank Alevoor, Sams Farhana, Abhishek Ray, Prassana Kalyan, Prajakta Zol, Fan Guo, Soroush Moallemi, Mahdi Javid, Kevin Grout, Pouria Pazhouhesh, Parisa Mahmoudidaryan, Dr. Amirreza Alizadeh who were always there when I needed them and for making the research lab a better place to work. Also, thanks to several brainstorming and interesting discussions. Many thanks to Sankalp Jain for spending several hours after his full-time job to help me in the APR of the digital circuits, his effort was very valuable in the tape-out. His hard work and dedication are one of the factors for meeting the project deadline.

I want to thank my friends Sumit Bhardwaj, Gauri Koli, Pragya Malakar, and Yugandhra Chandratre for all the analog circuit discussions and extending their help in the layout and testing of FIVR. In addition to these folks, the group of twenty more friends at Oak-Creek/2009 for making the last two years full of entertainment and giving some of the best memories at ASU, to be cherished for the lifetime. Also, I can not forget the contribution of many students to whom I served as TA, for their constant love, support, and for motivation. I learned so much from everyone. I honored to get such love and respect from all of you throughout the last few years.

Thanks also goes to Timothy Ness, Delilah Alirez, and other staff members for taking care of all purchase requests and other business operation and support. Special thanks to James Laux for always helping in CAD tools and IT infrastructure, his help is invaluable and was very crucial in this work. He has responded keenly to all the issues I faced in this regards. Finally, I am thankful to my dear parents, brother, sister and all my dear friends for their unconditional love, support, motivation, and encouragement. I am very much thankful to all of you.

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CHAPTER 1

INTRODUCTION

The computing power requirements are continuing to increase in battery operated mobile systems as well as in telecommunication server systems such as data centers. The modern multicore microprocessor is utilized for real-time computing, coding, modulation, and multimedia processing. Intel 4^{th} generation quad-core processor [6] is one such modern processor, utilizing four cores. Moreover, the power consumption demand from on-chip load such as hardware accelerators, and GPU, etc. is also continuing to increase. By adaptively varying both the voltage and frequency with respect to the changing load conditions, the overall power consumption can be greatly reduced. Also, the voltage needs to adjust at a faster rate to achieve the full advantage of dynamic voltage and frequency scaling (DVFS). These multi-core processors require multiple voltage domains to operate with dynamic voltage scaling [7].

The need for voltage regulation for each core and fast point of load regulation lead to a surge in on-chip DC-DC converters or fully integrated voltage regulators (FIVRs) [8–16] . By using multiple on-chip DC-DC converters, multiple voltage domains with the fast transient time can be achieved, thus improving the overall system efficiency and performance. Intel 4^{th} generation core microprocessors are powered by FIVR, which helps enable 50% or more battery life improvements for mobile products [15].

The on-chip voltage regulators are required to deliver higher power with small die area to minimize the overall cost and size of the power delivery system. This leads to a high-power density requirement from the on-chip voltage regulators. Thus, making high efficiency and high-power density as one of the important specifications for these on-chip converters [17]. The on-chip voltage regulator must operate at very high frequency to reduce the size of passives, at these high frequencies switching regulator

incurs a high switching loss. Often the switching frequency is in order of 100's of MHz, at these frequencies for acceptable ripple, the minimum required value of the inductor is still in few nH [8–16].

The on-chip air core inductors have a very poor-quality factor which limits the overall power efficiency. Also, due to high DC resistance (DCR) of the inductor, the conduction loss becomes significant at higher load currents, limiting its high current use [12]. Therefore, an efficient power stage which can deliver high current using the low values of inductor and capacitors needs to be developed.

1.1 Research Background

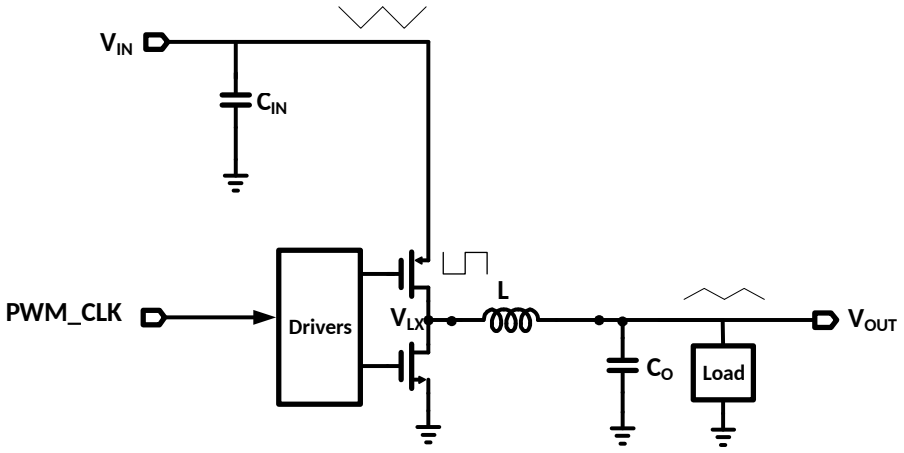

Figure 1.1: Second Order LC Filter in a Conventional Buck DC-DC Converter.

In a conventional buck converter, typically a second-order LC filter is typically used, as shown in figure 1.1. The switching waveform at V_{LX} is filtered by the second order LC low pass filter. The magnitude of the ripple is a function of switching frequency and the value of L and C. For a given output voltage ripple, the switching frequency needs to be increased or the value of inductor and capacitor needs to be very high. High switching frequency increases the switching losses and higher value of inductor and capacitor consumes larger area and thus decreases the power density and increases the cost of the overall solution. Additionally, for the high value of an inductor, the current slew rate is lower.

To reduce the output ripple further, a fourth order filter is proposed in [1] as shown in figure 1.2. However, the power density of 0.194 W/mm^2 still is very low, and the maximum load current delivered by this power stage is 180 mA.

To achieve the higher power density required by FIVRs, this paper proposes an architecture that utilizes a low value of inductor and capacitor to deliver high power demand. A higher-order notch filter, in addition to the flying capacitor between

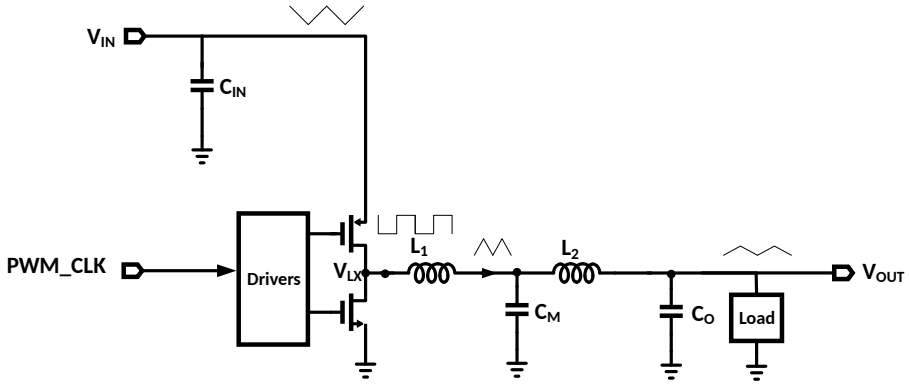

Figure 1.2: Fourth Order LC Filter Utilized in Buck DC-DC [1].

input and output [13] reduces the output ripple further while achieving low value of passives used. A prototype buck converter IC is fabricated in 65nm CMOS. The fully integrated power stage demonstrates a power density of 0.867 W/mm^2 and a current density of 1.377 A/mm^2. The power stage is controlled by a closed loop voltage regulation. In this paper, the fully integrated power stage along with bond wire and off-chip 1 nF capacitor is utilized to make a highly integrated buck converter. The buck converter is controlled using a current mode hysteretic controller, which is inherently stable. Moreover, a very fast reference tracking (20 ns) is also achieved.

Time domain circuits operate on CMOS-level rail-to-rail signals and compose of mostly digital circuits. Therefore, time-domain circuits have the advantage of CMOS scaling and better robustness and noise immunity compared to their analog counterparts. The supply voltage also scales down with the process scaling, thereby decreasing the voltage swing. As noise does not scale with the process, the signal to noise ratio degrades for analog circuits. Moreover, the threshold voltage does not scale in the same proportion as the supply voltage making cascoding technique difficult to implement [18–20]. Therefore, there is a surge of interest in building time domain circuits especially in the deep sub-micron (DSM) technology [18, 21–28]. Time domain voltage mode DC-DC buck converter is reported in [29, 30], and time domain current

mode buck converter is presented in [31]. The hysteretic controlled buck converter can achieve better transient response than voltage mode and current mode controlled buck converter [32]. Therefore, a time domain hysteretic controlled buck converter can achieve the advantage of fast transient and digital implementation. To implement a time domain hysteresis controller a time domain comparator is required. The speed of time-domain comparator (TDC) presented in [18, 21–23, 25–28] is limited by the clock frequency and thus limiting the frequency of the input voltage. The proposed time-domain comparator works on a multi-phase approach and achieves the sampling clock frequency limited to the one buffer delay, which is limited by the process and gets better with the scaling.

Chapter 2 describes the proposed architecture for the fully integrated power stage. A highly integrated buck converter using the proposed power stage and the time-domain hysteresis controller is then described in Chapter 3. The measurement results are presented in Chapter 4.

CHAPTER 2

FULLY INTEGRATED POWER STAGE

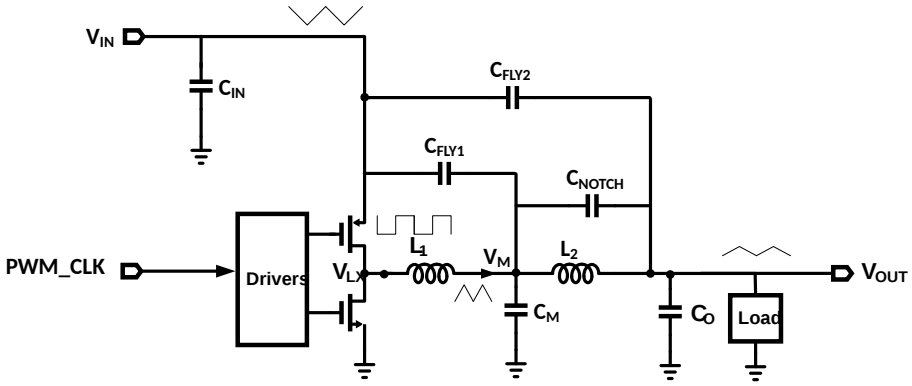

Figure 2.1: Proposed Power Stage with Higher Order Notch Filter with C_{FLY}.

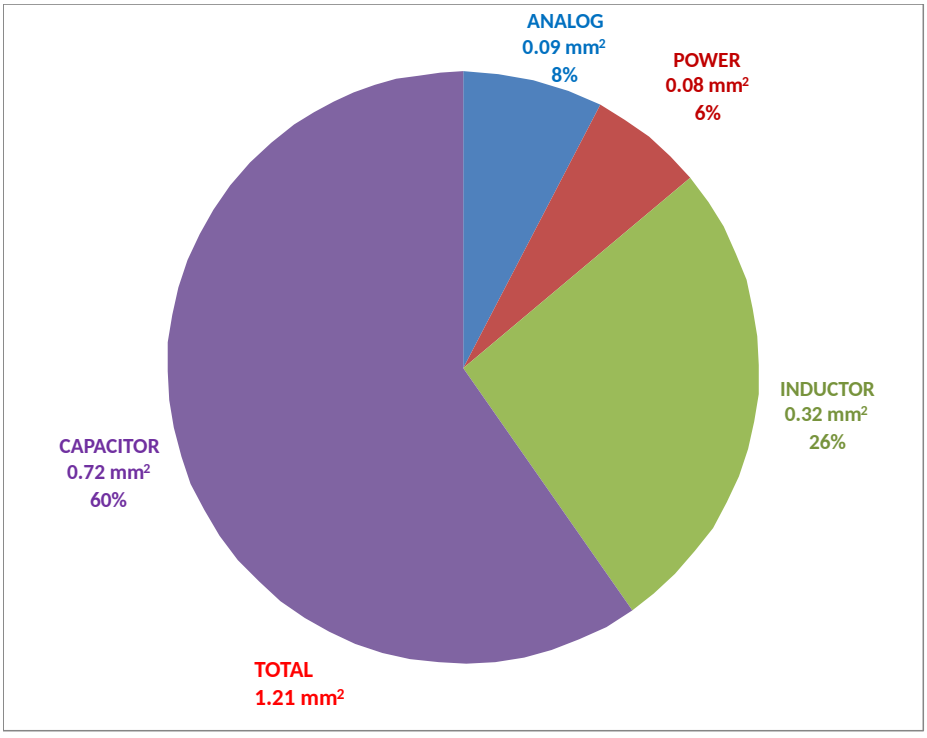

Figure 2.2: Die Area Breakdown of the Power Stage.

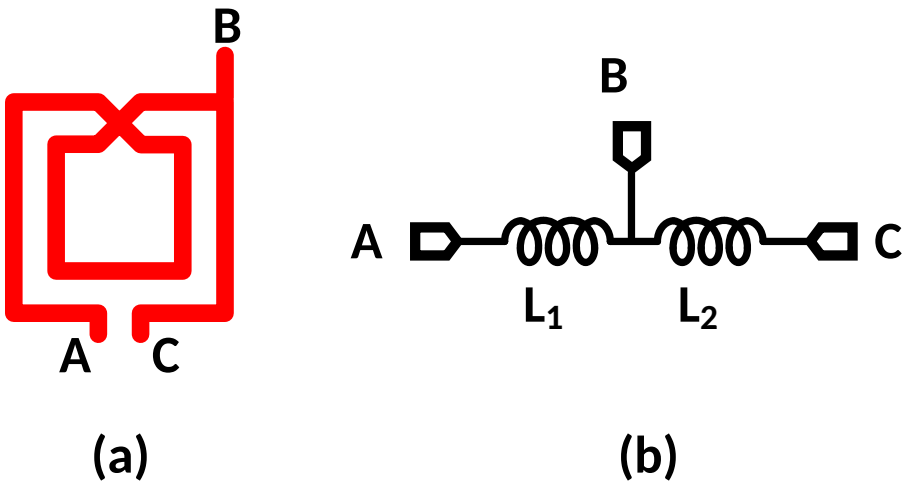

Figure 2.3: (a) Structure of the Designed Inductor (b) Symbol Showing the Intermediate Tapping.

The proposed power stage is shown in figure 2.1, where L_1 and L_2 are part of the same on-chip planar spiral inductor. C_{IN} and C_O are the input and output decoupling capacitors. CC_{NOTCH} is a capacitor connected in parallel with L_2 to form a notch filter. C_{FLY1} and C_{FLY2} are the flying capacitor to couple the out of phase ripple to the output.

The passive on-chip LC consumes a significant die area. To decrease the cost while increasing the power density of the converter, the total area occupied by the inductor and capacitor needs to be minimized while still achieving low output voltage ripple. A fourth-order filter as shown in figure 1.2 from [1] can achieve 2.2 times smaller value of inductor as compared to the inductor required in first-order filter, for a given attenuation and the total capacitance. The DCR of the on-chip inductor is in the range of 200-300 mΩ /nH [12], the lower inductor will have lower DCR and thus decrease the conduction loss due the DCR at high current load. In the proposed power stage, the fourth-order filter is formed by L_1, C_M, L_2, and C_O. A notch filter with the notch frequency around the switching frequency can attenuate the voltage

Table 2.1: VALUE OF PASSIVE COMPONENTS IN PROPOSED POWER STAGE

Component	**Values**
L_1	0.862 nH
L_2	0.272 nH
C_{IN}	0.5 nF
C_O	1.55 nF
C_M	0.7 nF
C_{NOTCH}	1.0 nF
C_{FLY1}	0.6 nF
C_{FLY2}	0.2 nF

ripple further. Although, with the process variation the notch frequency will vary, but still it will achieve a better attenuation than the fourth order filter without the notch. The notch filter is formed by L_2 and C_{NOTCH}.

Flying capacitor topology can further reduce the area of the decoupling capacitor required at input voltage (V_{IN}) and output voltage (V_O) [13]. The flying capacitor C_{FLY1} is connected across the V_{IN} and V_M, and the flying capacitor C_{FLY2} is connected across V_{IN} and V_O, to take advantage of out-of-phase input voltage ripple for effective

Table 2.2: AREA OF DIFFERENT SUB-CIRCUIT BLOCKS IN THE PROPOSED POWER STAGE

	Area (mm^2)	**% of Total Area**
Analog	0.09	8
Power	0.08	6
Inductor	0.32	26
Capacitor	0.72	60
Total	1.21	100

ripple cancellation. Due to the combined advantage from the fourth-order filter, notch filter, and flying capacitor topology, the power stage can achieve a low voltage ripple, even with the total on-chip capacitance of 4.55 nF and on-chip inductor L_1 and L_2 of 0.86 nH and 0.27 nH respectively. The on-chip capacitors are implemented by combining the MOS and MIM capacitors to increase the capacitor density. The inductor and capacitor values are summarized in TABLE 2.1. The die area of an inductor, capacitor, and power stage are summarized in TABLE 2.2 and the area

breakdown is depicted in a pie chart in figure 2.2.

2.1 Inductor Design

The performance of the power stage is mostly dependent on the output filter inductor and capacitor. The top two thick metal layers available in 65nm CMOS are used for designing the on-chip inductor. The on-chip planar spiral inductor in terms of dimension of the inductor can be expressed as,

$$L = K_1 \mu_0 . \frac{n^2 \left(d_0 + d_i\right)^2}{2 \left(d_0 + d_i + K_2 d_0 - K_2 d_i\right)} \tag{2.1}$$

$$d_i = d_0 - 2n \left(w + s\right) \tag{2.2}$$

Where K_1 and K_2 are layout-dependent coefficients, μ_0 is the free space permeability, n is the number of turns, d_0 is the outer diameter, d_i is the inner diameter, w is the width of the trace, s is the spacing between the adjacent turns [1]. From (1) it is evident that for a larger inductor value, a larger d_0 is required, which in means a larger area. Moreover, the DCR is proportional to the length of the inductor spiral metal. The main challenge for the plannar inductor design is to design an inductor with high inductance and lower DCR occupying less on-chip area. The designed inductor topology [12], [1] is shown in 2.3. The inductor trace is formed by stacking the top two metals (M_9-M_8), the width w is 85 μ m, the spacing s is 10 μ m, and the dimension of the inductor is 568 μ m X 572 μ m, occupying 0.32 mm^2 of the die area. The inductor spiral metal width is kept at 85 μ m, for reducing the DCR, which is a dominant source of the conduction loss in a high load condition.

The inductor is placed on a patterned ground shield (PGS) formed by the metal, M_1 to suppress the electric coupling. The proposed design is simulated by a 3D field solver, Advance Design System (ADS). The obtained inductor values for L_1 is 0.862 nH and L_2 is 0.272 nH, and the combined DCR of L_1 and L_2 is 320 mΩ .

CHAPTER 3

HIGHLY INTEGRATED BUCK CONVERTER

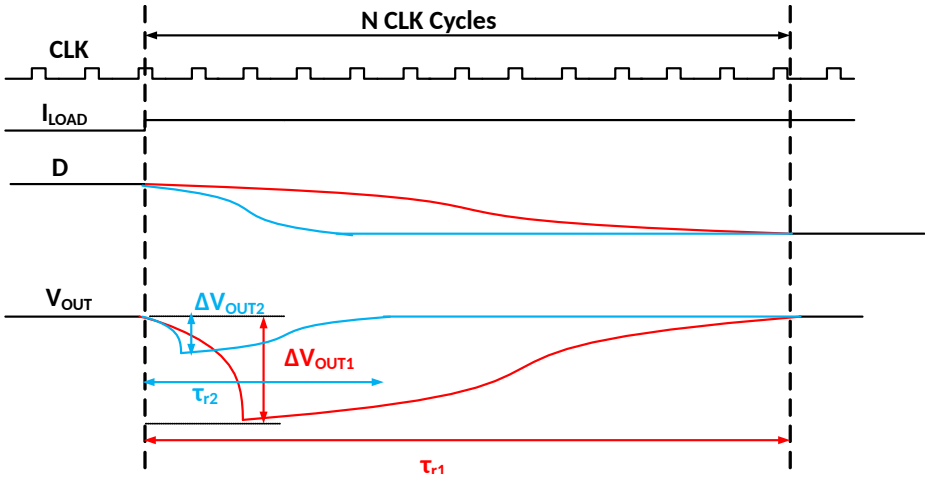

Figure 3.1: Timing Diagram of the Output Voltage and the Duty Cycle of a Linear and Hysteretic Control, when a Load Transient is Applied.

A control loop around the power stage is required to get a regulated output voltage. Linear control techniques such as voltage mode or a current mode control [33–37], are the most commonly used methods in DC-DC converters. In linear control schemes, the eror voltage is integrated and amplified, whereas in non-linear control schemes such as hysteretic control, an error integrator is not required. The output voltage is regulated at every switching clock cycle [38]. A typical response of the buck converter to a load transient for linear and nonlinear control is depicted in figure 3.1. Hysteretic control techniques can achieve a fast response in the order of the few switching time periods [32]. However, the switching frequency of the hysteretic buck converter is not constant and it varies with V_{IN}, V_{OUT}, driver delay, comparator delay, and the load current (I_{LOAD}). In this work, the switching frequency is regulated by utilizing a digital phase locked loop (DPLL) [39].

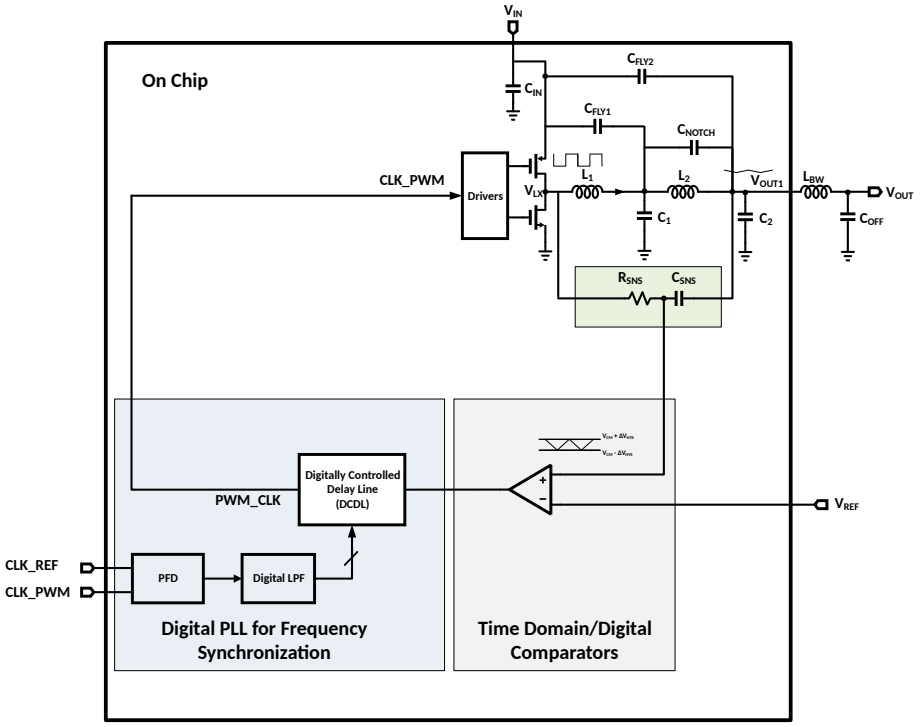

Figure 3.2: Hysteretic Buck Converter Utilizing the Proposed Power Stage and the Proposed Time-Domain Comparator (TDC).

The block diagram of the proposed hysteretic buck converter utilizing the proposed power stage and time-domain comparator is shown in figure 3.2. The buck converter consist of the proposed power stage, which is controlled by a time-domain hysteresis controller. Inductor current is sensed [40] by utilizing the quasi current sensor formed by R_{SNS} and C_{SNS}. V_{SNS} has an average voltage equal to VOUT and the ripple proportional to the inductor current. V_{SNS} is compared with the reference voltage VREF, to regulate the output voltage. The comparator output then drives the driver of the power stage with an additional delay introduced by the digitally controlled delay line (DCDL) [41] in the DPLL. A DPLL based frequency synchronization architecture such as [39], is used in this design.

The inherent delay of the comparator and power stage for the proposed design in

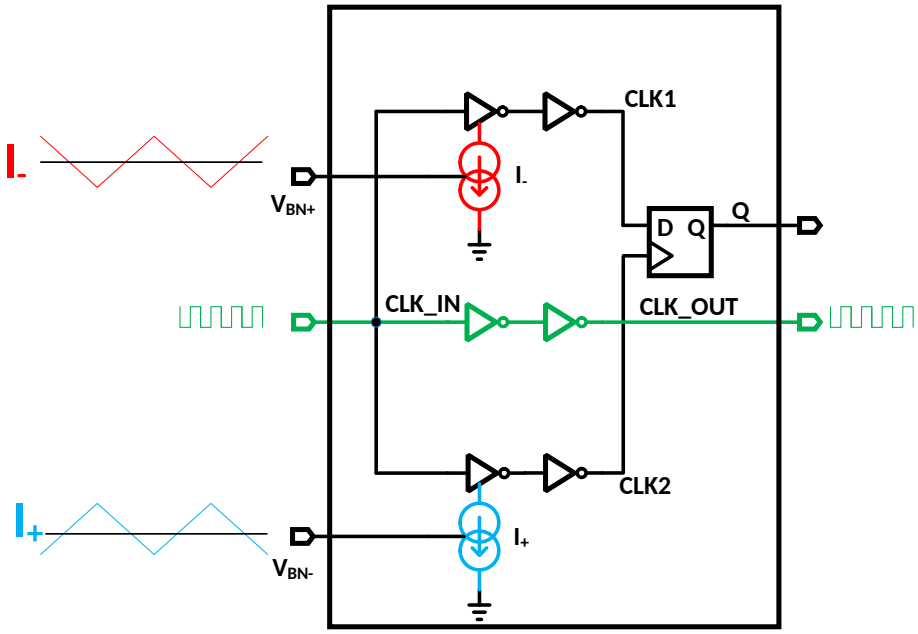

Figure 3.3: Conventional Single Phase Time-Domain Comparator.

65nm CMOS is high, such that the buck converter's switching frequency is limited to less than 240 MHz. The designed buck converter's switching frequency is kept at 180 MHz. Since the power stage is designed for the switching frequencies greater than ¿ 300 MHz, an off-chip 1 nF capacitor is connected to the die via a bond wire, to further filter the voltage ripple at 180 MHz. The capacitor can be placed in the package as well. If the power stage is optimized at 180 MHz, the extra off-chip capacitor will not be required. This design is to show the proof of concept, but the better performance will be achieved at the scaled processes. Building blocks of the proposed hysteretic buck converter is discussed next.

3.1 Current Sensor

A current sensor is required in order to sense the inductor current for implementing the current mode hysteresis. The quasi current sensor formed by R_{SNS} and C_{SNS} senses the inductor current. Due to the significant DCR, the average voltage of V_{SNS} is equal

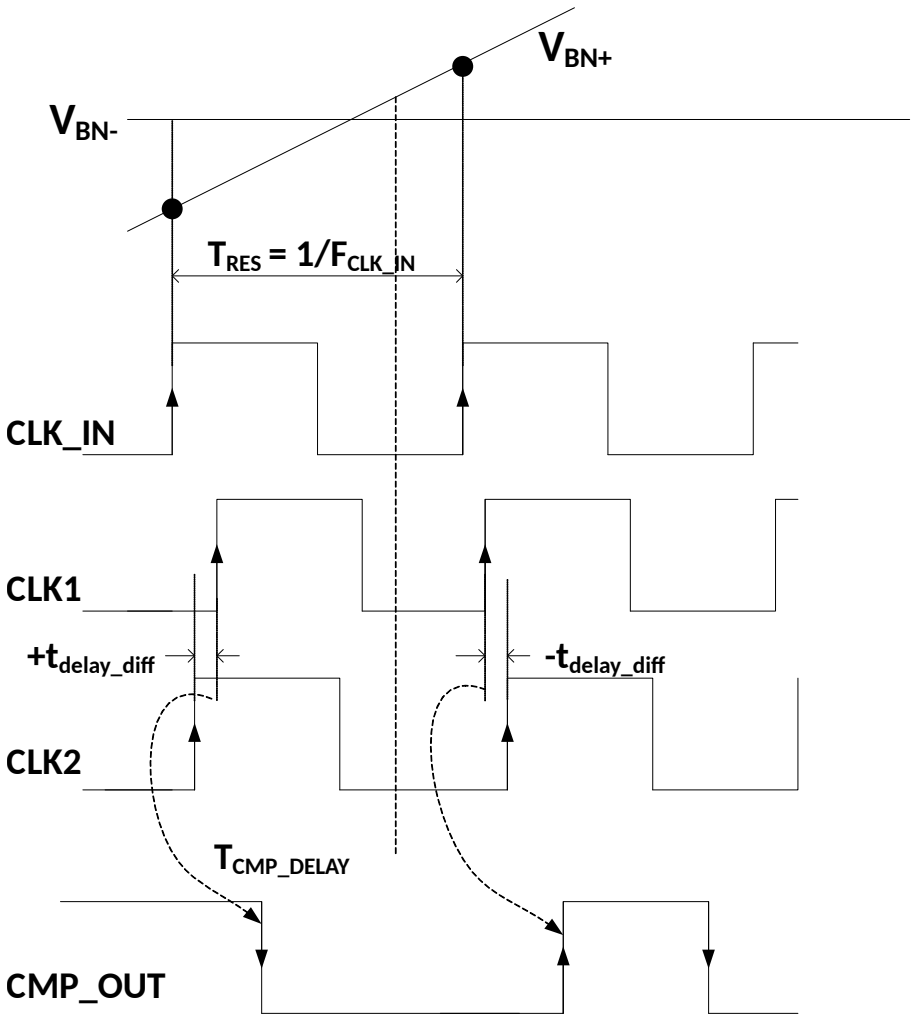

Figure 3.4: Timing Waveforms of the Conventional TDC.

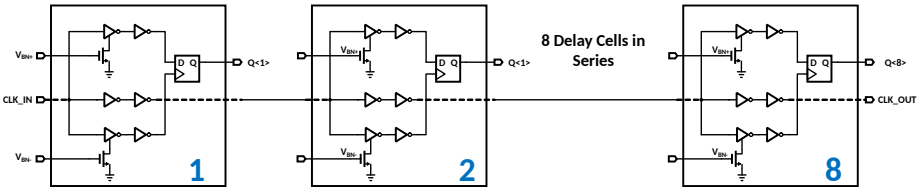

Figure 3.5: Eight Single Phase Cascaded Comparator Operating on the Clock Separated by the Two Inverter Delay.

to V_{OUT} -$I_{LOAD}R_{DCR}$. So, the regulation at higher load current is poor due to the finite DCR. The regulation can be improved by utilizing an integrator in the loop,

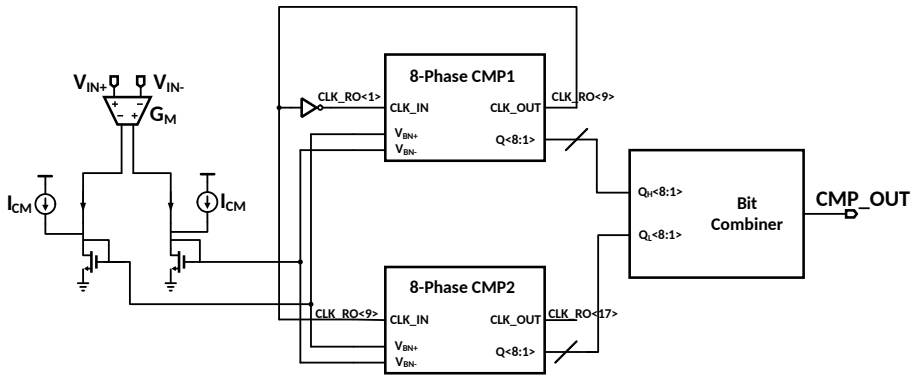

Figure 3.6: The Proposed 16-Phase TDC, Which Achieves 1/16 of the Time-Resolution than the Conventional TDC.

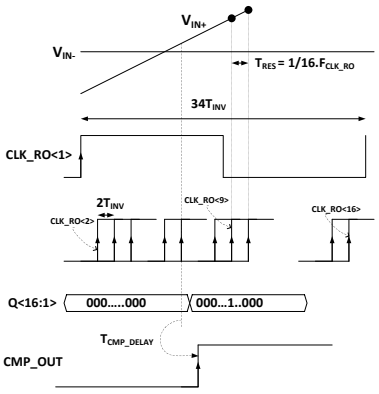

Figure 3.7: Timing Waveforms of the Proposed Multi-phas TDC.

such as V^2 control in [42]. The values of sensor R_{SNS} and C_{SNS} also sets the switching frequency [40].

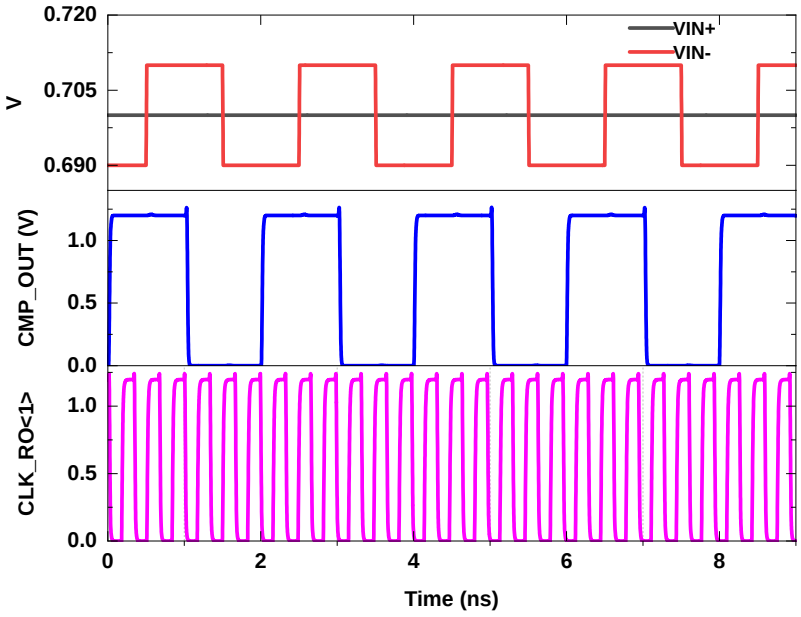

Figure 3.8: Simulated Behavior of the Proposed Multi-phase TDC.

3.2 Frequency Synchronization

Switching frequency can be regulated by controlling the delay inside the loop. A digitally controlled delay line (DCDL) is inserted between the comparator output and the drivers. A NAND based DCDL [41] is implemented, which achieves a minimum zero code delay. The digital code for the DCDL is generated from the digital PLL loop. Switching clock, CLK_PWM is compared with the reference clock CLK_REF, using a 1-bit bang-bang PFD. The bang-bang PFD output is passed through a digital LPF, which generates a digital code to control the DCDL, such that the switching frequency is regulated to the desired value [39].

3.3 Time Domain Hysteresis Controller

Time domain implementation of the comparator is introduced in [18, 21–23, 25–28]. Time domain control offers several advantages over the voltage domain comparator. However, the comparator's maximum speed is limited by the process technology. To achieve a higher frequency operation a multi-phase comparator architecture is developed. Figure 3.3 shows the architecture of the conventional single-phase time-domain comparator [27] and the timing waveforms are shown in figure 3.4. A differential current signal is applied to the current starved inverter. The current starved inverters implement a current controlled delay. The output of the inverters will have a time delay difference (t_{delay_diff}) proportional to the applied input differential signal (V_{BN+} - V_{BN-} or I_+ - I.). The difference of the delay can be sensed by a D flip-flop, and its output is a logic high if the t_{delay_diff} is negative or a logic low if the t_{delay_diff} is positive, thus implementing a time domain comparator. The time resolution of this TDC is limited by the sampling clock frequency. The input clock frequency should be very high in order to achieve lower time resolution.

The proposed TDC achieves a lower time resolution without using a very high frequency for the input clock. Operating each of the conventional TDC at the multi-phase of the clock, the effective sampling frequency can be increased by the factor of a number of phases. Eight single phase TDCs are connected in cascade as shown in figure 3.5, each of the TDC gets the input clock after a two inverter delay. Therefore, the minimum time resolution is limited by the inverter delay in the process. The overall schematic of the proposed multi-phase time domain comparator is shown in figure 3.6. Two blocks of the 8-phase TDCs 8-phase comparators CMP1 and 8-phase CMP2 are utilized, to cover both high and low cycle of $CLK\_RO < 1 >$.

In the process used, the delay associated with two inverter delays is approximately

20 ps, hence a sampling rate of approximately 50 GHz is achieved without the need for a clock signal of 50 GHz. The clock signal required for the TDC can be generated by forming a ring oscillator. An additional inverter along with the even number of inverters in the TDCs form a ring oscillator, which oscillate at approximately 3 GHz at the typical condition. Eight phases of the ring oscillator clock, $CLK\_RO < 8:1 >$ is generated in an 8-phase CMP1 and other eight phase $CLK\_RO < 16:9 >$ is generated in 8-phase CMP2. The single phase TDC operates on each of the 16 phases and achieves the effective resolution, T_{RES} of $1/16F_{CLK\_RO}$. The sixteen outputs of TDCs are logically operated by the digital logic combiner block to get a single bit comparator output. The current controlling the TDCs is generated by using an OTA and current mirrors. The typical waveforms of the proposed TDC, for the case when negative input $V_{IN-}$is kept constant and the positive input $V_{IN+}$is ramped, is shown in figure 3.7. The simulation results of the proposed TDC are shown in figure 3.8.

CHAPTER 4

FIVR MEASUREMENT RESULT

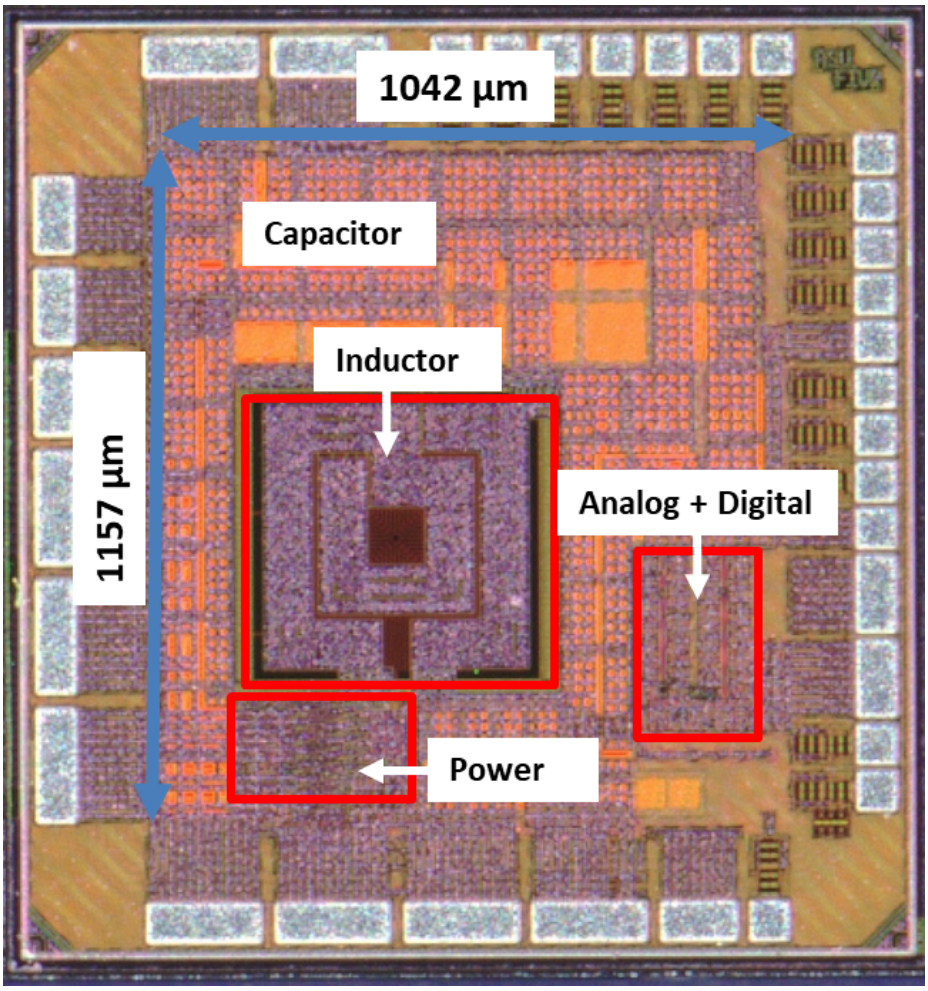

Figure 4.1: Die Micrograph of the Proposed Power Stage and Time-domain Comparator.

In this chapter, the measurement results of FIVR are discussed. The FIVR is measured for various input and output voltages. The proposed power stage is implemented in a 65nm CMOS process and packaged in 32-pin QFN package. The die micrograph of the power stage with on-chip inductor and on-chip capacitor is shown

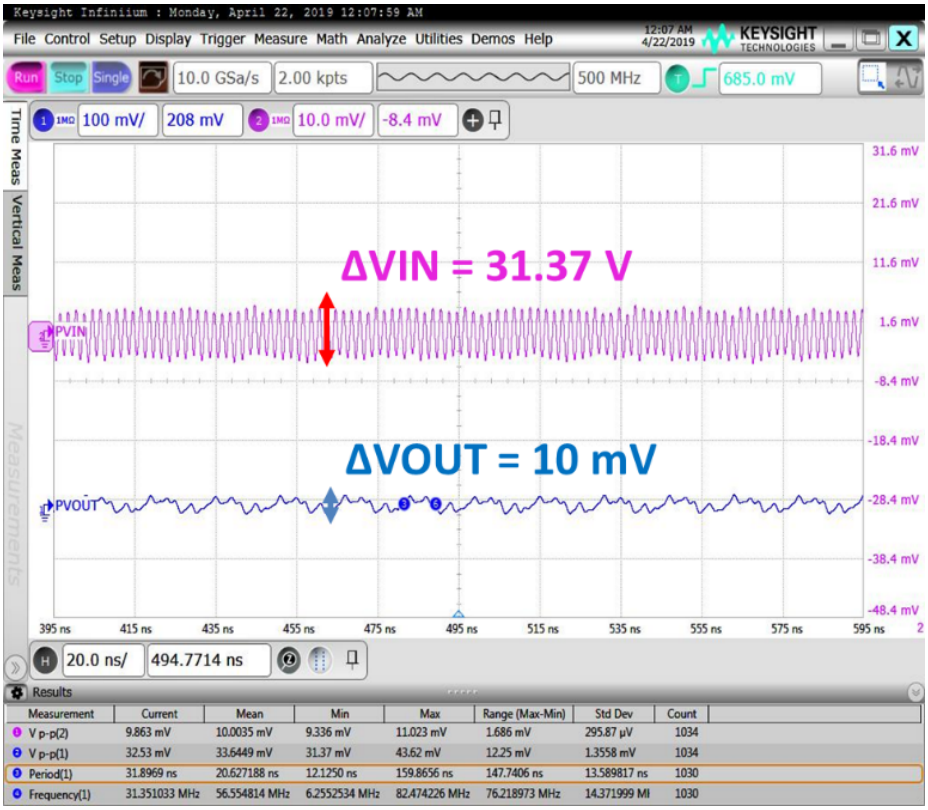

Figure 4.2: Measured Input and Output Voltage Ripple, at V_{IN} = 1.2 V, V_{OUT} = 0.625 V, I_{LOAD} = 0.780 A.

in figure 4.1. The active area of the die, including the on-chip inductor and capacitor for the higher order LC filter, is 1.21 mm^2. The inductors consume 0.32 mm^2 and the capacitors consume 0.72 mm^2 of the die area. While operating at 500 MHz, the proposed power stage achieves a peak power efficiency of 71.02 % and a maximum power density of 0.861 W/mm^2.

figure 4.2 shows the output voltage ripple at the load current of 0.780 A. Even with a low value of on-chip inductor and capacitor a very low output voltage ripple of 10 mV is achieved. Although at different operating conditions the output voltage ripple increases, figure 4.3 shows the output voltage ripple of 55.49 mV at a load current of 1.6 A. The output voltage ripple at 1 A load current as a function of

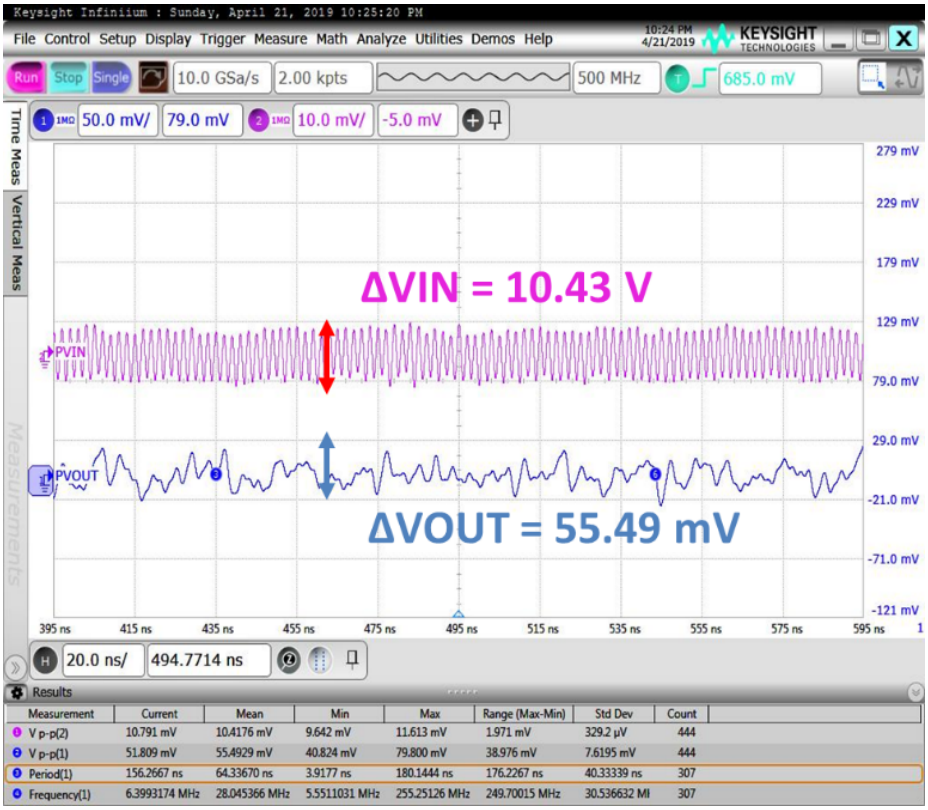

Figure 4.3: Input and Output Voltage Ripple, at $V_{IN} = 1.2$ V, $V_{OUT} = 0.625$ V, $I_{LOAD} = 1.6$ A.

switching frequency is plotted in figure 4.4. Although the notch in the LC filter is tuned around 300 MHz, figure 4.4 shows that the output voltage ripple is low throughout the frequency range of 480 MHz to 720 MHz, because of the higher order filter and the capacitor C_{FLY1} and C_{FLY2}.

The on-chip load is implemented by an NMOS transistor in a linear region, which serves as a resistor load. Multiple of such resistors are connected in parallel and can be selectively turned on or off to get the range of load resistance from 400 mΩ to 10 Ω . By varying the on-chip load resistance, the efficiency versus output power is measured and plotted in figure 4.5. The efficiency at the low current level is low as the power stage is going to discontinue conduction mode (DCM). At high current

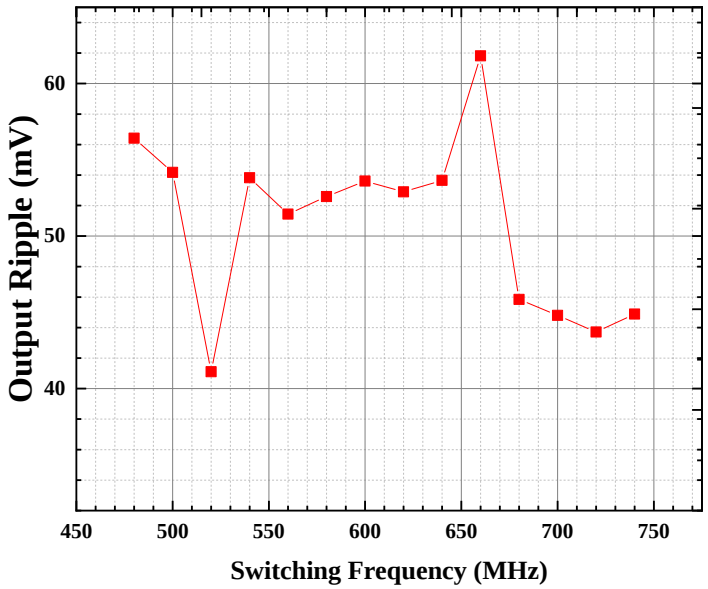

Figure 4.4: Output Voltage Ripple at Different Switching Frequencies, at Load Current of 1A at $V_{IN} = 1.4$ V, and $V_{OUT} = 0.35$ V.

levels, the efficiency is degraded by the higher conduction loss due to power MOS and inductor DCR. At moderate current levels, the switching loss becomes one of the significant contributors to the overall loss. The maximum power delivered is 1.04 W at voltage conversion ratio (VCR) of 0.66 and achieves 61.03 % efficiency. Efficiency at different VCR while delivering 1.04 W of power is plotted in figure 4.6. Therefore, the maximum power density is 0.861W/mm^2, which is the highest among the state-of-the-art FIVRs.

The closed-loop characteristic of the hysteretic buck converter is also measured. The LC filter is designed for more than 300 MHz switching frequency. But due to the significant delay from the comparator, driver, and the logic circuit of DCDL in 65nm CMOS, the closed loop switching frequency is limited to less than 240 MHz. An

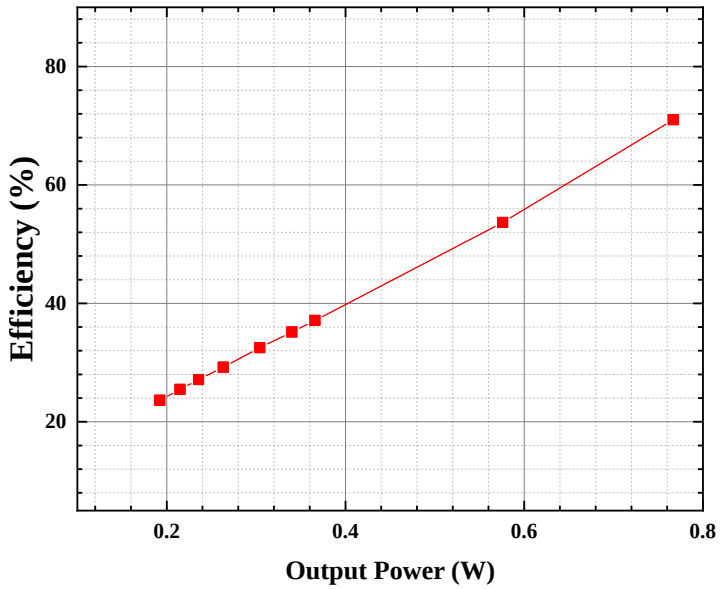

Figure 4.5: Efficiency Versus Output Power.

off-chip capacitor of 1 nF is therefore added through the bond wire of approximately 0.3 nH, to achieve the required ripple at this reduced switching frequency.

Moreover, for most of the load range, the converter is operating in DCM and thus achieves a poor efficiency. The presented design is proof of concept for fast transient buck converter in 65nm CMOS. The design will achieve a better performance if implemented in the lower node process, as the delay of the drivers and comparator will be less and will not limit the buck converter switching frequency. In addition, unlike this design, the off-chip capacitor will also be not required if implemented in the lower node processes. The efficiency of the buck converter operating at 180 MHz, as a function of VCR at different load currents are plotted in figure 4.7. The efficiency is also compared with an ideal LDO and plotted in figure 4.8, the buck converter achieves higher efficiency than the ideal LDO.

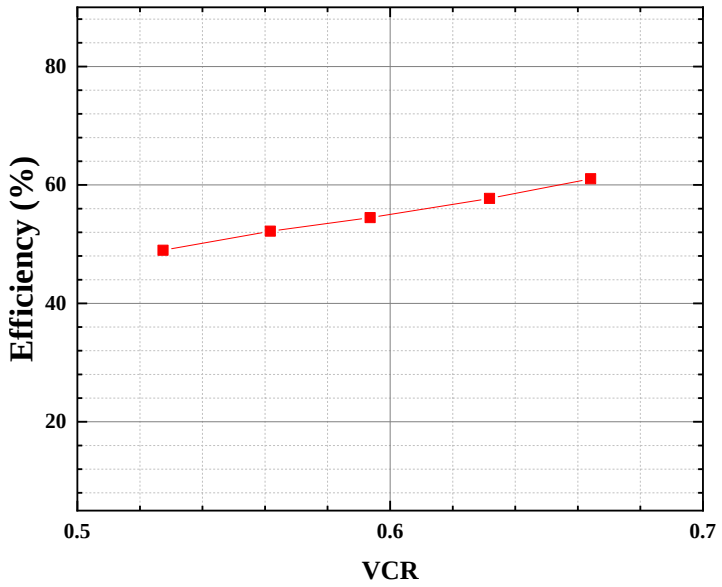

Figure 4.6: Efficiency Versus VCR.

The load transient response is plotted in figure 4.9. An on-chip load transient from 600 mA to 900 mA and vice versa in 200 ps rise/fall time is applied at the output of the buck converter. Settling time of 15 ns and 10 ns is observed for load rise and fall respectively. A high slew rate of 40 V/μ s is also observed. In figure 4.10 the output voltage response to a reference step of 200 mV is plotted. Settling time of 20 ns is observed in this case, which makes it the best fit for DVFS application, where a fast reference tracking is desirable. A comparison table with the state-of-the-art for power stage speciation is shown in TABLE 4.1, the proposed power stage achieves the highest power and current density among state of the art published papers. The highly integrated hysteretic buck converter comparison with state of the art is provided in TABLE 4.2, it achieves the fast response in order of 10's of ns which is better than the state of the art published works.

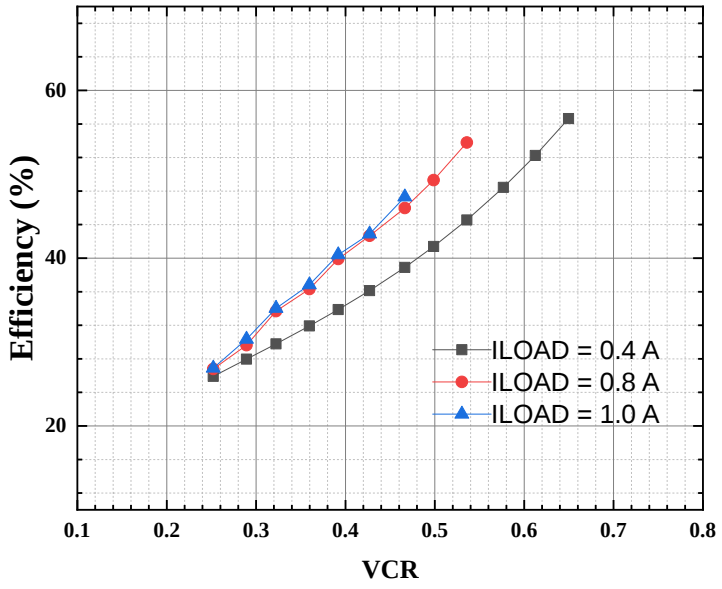

Figure 4.7: Efficiency of Hysteretic Buck Converter at Different VCR, at V_{IN} = 1.4 V and at I_{LOAD} = 0.4 A, 0.8 A, and 1A.

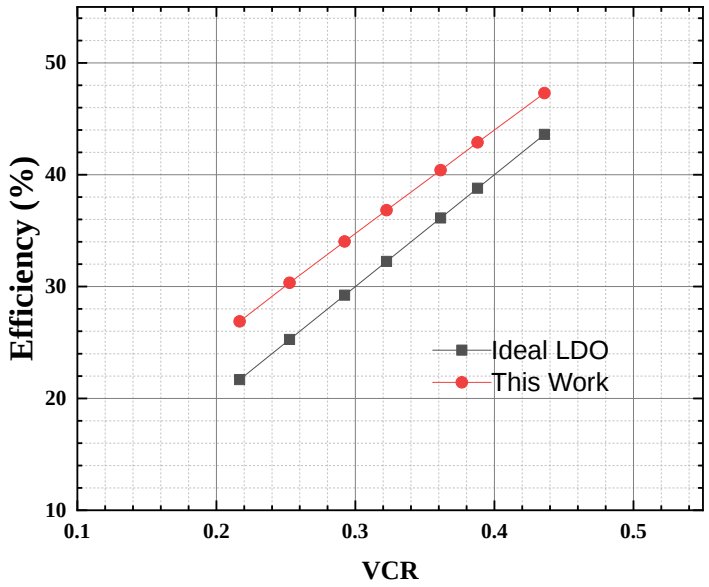

Figure 4.8: Efficiency of Hysteretic Buck Converter and an Ideal LDO versus VCR for $I_{LOAD} = 1$ A.

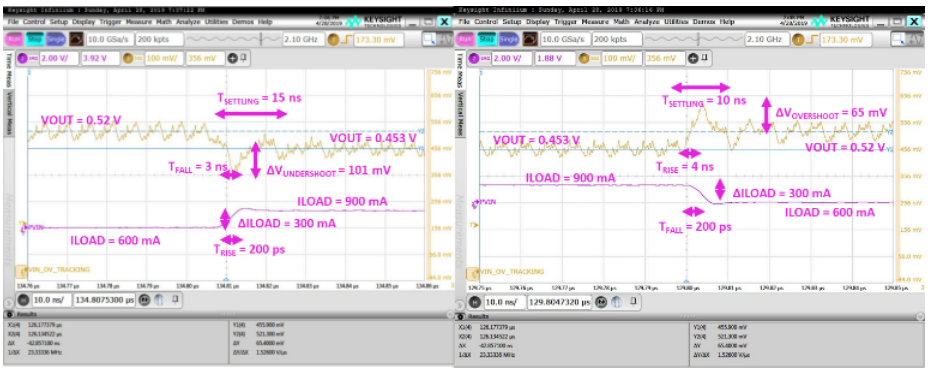

Figure 4.9: Output Voltage Response for a Load Transient from 600 mA to 900 mA.

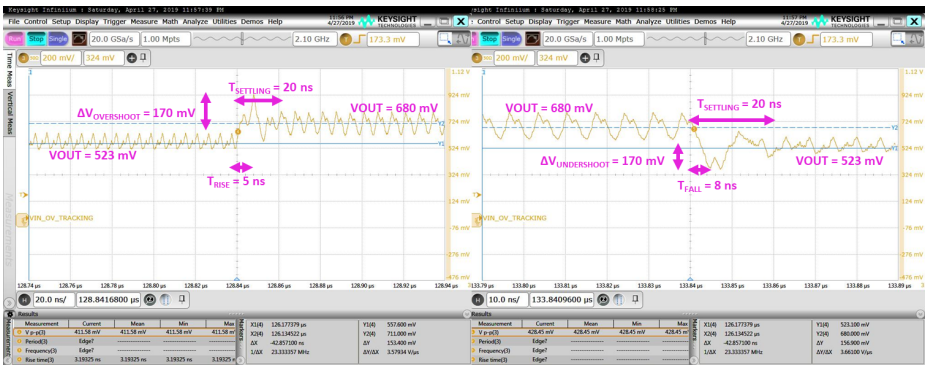

Figure 4.10: Reference Tracking From 523 mV to 680 mV, at I_{LOAD} = 0.5 A.

Table 4.1: PERFORMANCE OF THE PROPOSED POWER STAGE AND ITS COMPARISON WITH THE STATE-OF-THE-ART

Publication	**VLSI 2007 [42]**	**JSSC 2012 [42]**	**VLSI 2014 [6]**	**TOIA 2016 [7]**	**TPE 2016[13]**	**ISSCC 2019 [39]**	**ISSCC 2019 [40]**	**This Work**
Technology	130 nm CMOS	130 nm CMOS	22 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm CMOS	65 nm CMOS
Buck power stage topology	2-phase stacked interleaved	3-level	Second order LC	2-phase negatively coupled inductor	Fourth	Switched inductor capacitor	Hybrid Resonant	Higher order LC+ Notch + Fly Cap
Order LC								
Integration (L/C)	Full (ON-chip)	Full (ON-chip)	Full (ON-chip)	Full (ON-chip)	Full (ON-chip)	Full (ON-chip)	Full (ON-chip)	Full (ON-chip)
VIN [V]	1.2	2.4	1.5	2.0-2.2	1	1.2	3.0-4.5	1.2
VOUT [V]	0.9	0.4-1.4	0.6-1.0	0.7-1.2	0.5-0.8	0.6-0.9	1.5-1.8	0.5-1.0
Frequency [MHz]	170	50-250	500	500	450	450	35-50	500
L [nH] (No. of Phase)	2(2)	1(4)	1.5(1)	1.54(2)	1.8(1)	0.85 (1)	9 (1)	0.9(1)
CIN [nF]	4.3	1	2	0.83	-		0.18	0.5
CFLY [nF]	-	18	-	-	-		2	0.8
COUT [nF]	5.2	10	10	1.83	4		10	1.55
CTOTAL [nF]	9.5	29	12	2.63	-	4.82	12.18	4.55
Bandwidth [MHz]	-	-	43	-	16.2			-
Output voltage ripple [mV]	40	25-200	10	80**	15	20-56	35	Oct-55
Load Current [A]	0.19-0.35	<0.8	<0.25	0.2-0.7	0.18	0.533	0.12	1.66
Max Power [W]	0.315	1	0.25	0.84	0.126	0.365	0.216	1.038
Area [mm2]	1.5	5	1.5	1.1	0.65	0.65	7.83	1.21
Current density [A/mm2]	0.233	0.16	0.17	0.64	0.276	0.82	0.015**	1.377
Power density [W/mm2]	0.21	0.2	0.17	0.76	0.19	0.73	0.028	0.861
Efficiency (at maximum power density)	76	63	-	71	74.5	-	-	48.96
Peak efficiency [%]	77.9	77	68	76.2	76.1	78	85	71.02

** Extracted from the paper

- Not applicable or not available

Table 4.2: PERFORMANCE OF THE PROPOSED BUCK CONVERTER AND ITS COMPARISON WITH THE STATE-OF-THE-ART

Publication	**TOIA 2016**	**JSSC 2015**	**JSSC 2015**	**JSSC 2019**	**This Work**
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Controller	Digital PWM based Voltage Mode	Time domain Voltage mode	Time domain Voltage mode	Time domain Current mode	Time domain Current mode hysteretic
Buck power stage topology	2-phase negatively coupled inductor	Second order	4-phase second order	Second order	Higher order + Notch + Fly capacitor
Integration (L/C)	Full (On-chip)	Off-chip	Off-chip	Off-chip	On-chip + Off-chip
VIN [V]	2.0-2.2	1.8	1.8	1.8	1.2
VOUT [V]	0.7-1.2	0.6-1.5	0.6-1.5	0.15-1.69	0.5-1.0
Frequency [MHz]	500	11-25	30-70	10	180
L [nH] (No. of Phase)	1.54(2)	220	90(4)	2200(1)	0.9+0.4#
CIN [nF]	0.83	-	-	-	0.5
CFLY [nF]	-	-	-	-	0.8
COUT [nF]	1.83	4700	470	4700	1.55+1
CTOTAL [nF]	2.63	4700	470	4700	5.55
Bandwidth [MHz]	-	1	9.85	1	-
Load transient settling time [ns](step up/down)	-	3500	600/600*	3500/3500	15/10
Reference tracking time [ns] (step up/down)	8300/11200	17500	-	3000/3500	2-Feb
Voltage slew [V/µs]	-	0.14*	-	-	45
Overshoot voltage [mV]	100	60	65	100*	65
Undershoot voltage [mV]	83	60	65	100*	101
Nominal output voltage ripple [mV]	80*		3.5	-	100
Load current [A]	0.2-0.7	0.6	0.8	0.6	1
Max power [W]	0.84		1.2*		0.607
Area [mm2]	1.1	0.24**	0.48**	0.19**	1.21**
Peak efficiency	76.2	94	87	94.9	57.55

* Extracted from the paper
** Without including off chip L/C
# Estimated bondwire inductance
- Not applicable or not available

CHAPTER 5

INTEGRATED SWITCHED CAPACITOR POWER SENSOR

This chapter presents the power sensor to measure the output power of a DC-DC boost converter, which is used for photo voltaic (PV) application. The proposed approach obviates the need for a series current sense resistor and a complex current/voltage digitization and multiplication circuitry required for calculating power. Thereby, this technique does not require Analog Multipliers, ADCs, DSP, and FPGA, thus reducing the bill of material, silicon area, and power consumption of the overall system. Additionally, it provides the DC electrical isolation between the high output voltage of the boost converter and low voltage integrated CMOS power sensor circuit. The proposed power sensor circuit is implemented using a switched capacitor differentiator (SCD) and a voltage to time converter (VTC). This approach results in lower complexity, lower silicon area, lower power consumption, and lower component count for the overall PV MPPT system. Designed in a 180 nm CMOS process, the circuit can operate with a supply voltage of 1.8 V. It achieves a power sense accuracy of 7.6%, occupies a die area of 0.0519 mm^2, and consumes 0.748 mW of power.

5.1 Introduction

Photovoltaic (PV) technology has started to play an important role in fulfilling the present energy needs, as the solar resource is abundant, free of cost, and cannot be monopolized by one country [43]. PV, still in its nascent stages of large scale utilization, is one of the rapidly growing industry with an annual growth rate of 40% in the last two decades [43]. PV energy is being utilized in an every possible sector and the power required in those sectors can differ by a several order of the magnitude. The low power required for Internet of Things (IoT) devices [44, 45] or very high power required by the residential units can be firmly supplied using the PV

technology. Additionally, PV energy is being used in the electric vehicles (EV) [46], EV charging stations [47], and to power space aircrafts [48]. The power delivered by the PV systems depend on the light intensity and the load conditions. Due to this dependence, the power derived from a PV cell is not always the maximum power it can supply. To extract the maximum power, a Maximum Power Point Tracking (MPPT) circuit is used [49]. This circuit ensures that for any load and solar insolation, the PV cell is delivering its maximum power. Often a DC-DC converter is inserted between the PV cell and the load or a battery, this DC-DC converter is then controlled by an MPPT circuit to harness the maximum power from the PV cell.

Several different algorithms exist for performing the MPPT [49]. Perturb & Observe (P&O) algorithm [50–52] is one of the most used algorithm because of its simplicity. In this algorithm, output power of the DC-DC converter is sensed by the MPPT circuitry. Based on the present and past value of the sensed power the duty cycle of the DC-DC converter is controlled such that the power delivered to the load is maximum. The computation required to calculate the power for MPPT utilizes discrete level high precision Digital Signal Processor (DSP) core or FPGA, Analog to Digital Converter (ADC), DACs as shown in Figure 5.1 [2, 53–58]. Sensing current [59] and obtaining the product of sensed current with the sensed voltage is expensive in terms of the bill of material of off-chip components, die area, and power consumption.

A series resistor based approach is conventionally used for sensing the current, in which a sense resistor is inserted in series of the current path [60, 61] as shown in Figure 5.2. The voltage across the resistor is proportional to the current flowing through it, which is sensed by an amplifier. Although the biggest advantage of this scheme is its simplicity, it possesses many limitations as it introduces significant power loss and large voltage drop for high current, resulting in low power efficiency.

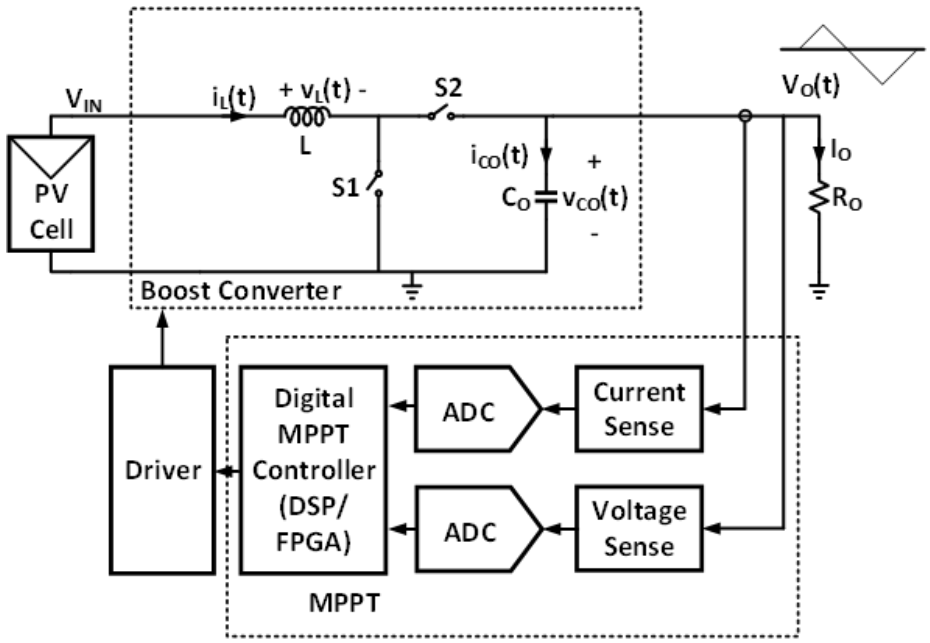

Figure 5.1: The Conventional MPPT System Utilizing Voltage and Current Sensing Followed by the Digitization and Digital Computation Using ADCs and DSP/FPGA Respectively [2]

Additionally, in case of high side current sensing, the amplifier required to sense the voltage across the series resistor needs to be high voltage compliant, which may not be a realistic solution for an IC implementation.

A scaled version of the high current can also be sensed, and by terminating this scaled current across a sensing resistor the voltage proportional to the high current can be measured [62, 63], but it also require ADCs and DSPs or analog multiplier to calculate the power. Other existing methods for current sensing are to utilize the DC resistance of the inductor [64, 65], use inductor coupling to sense the current flowing in the main inductor, employ a transformer, or a Hall Effect current sensor [3, 4, 59, 66–68]. These circuits are often bulky consuming a large printed circuit board real estate, cannot be integrated in an IC based solution, inefficient, and have low reliability.

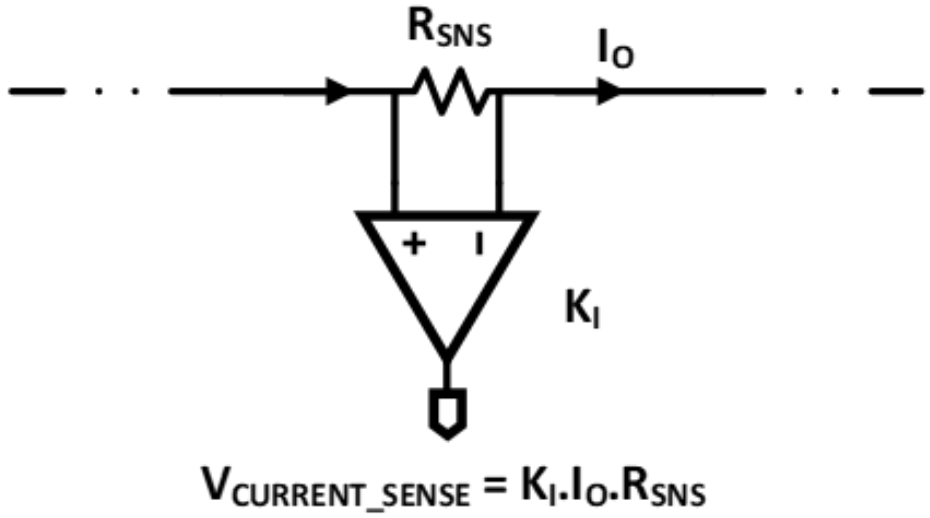

Figure 5.2: Conventional Series Resistor Based Current Sensor [3]

Irrespective of any approach used for current sensing, in commonly used P&O MPPT circuit, the power is evaluated by first digitizing each of the sensed voltage and current sample using an ADC, followed by a DSP or a FPGA to calculate the power [53–57].

MPPT can get rid of the two ADCs and DSP/FPGA if it is implemented in analog domain, resulting in a smaller form factor [5, 68] as shown in Figure 5.3. In such an approach, sensed voltage and current are multiplied in the analog domain. To ensure high efficiency from such a system the design of efficient power sensor is important. The high power consumption of the conventional analog multiplier can reduce the overall efficiency and occupy a large die area. One efficient way to sense the power in analog domain is proposed in [61]. Current and voltage are converted into pulse width and amplitude of a current pulse. Averaging of this pulse will result in the product of sensed voltage and current. However, this current sensing method uses a lossy MOS resistor, which occupies significant area and have similar drawbacks as series resistor based current sensing. A loss-less current-to-digital (IDC) based

current sensing method is presented in [69]. This method provides the DC electrical isolation between the high voltage at the boost converter output and the low voltage current sensor used for the MPPT. However, this method requires an ADC to digitize the sensed voltage and a computational DSP for calculating the product to obtain the power.

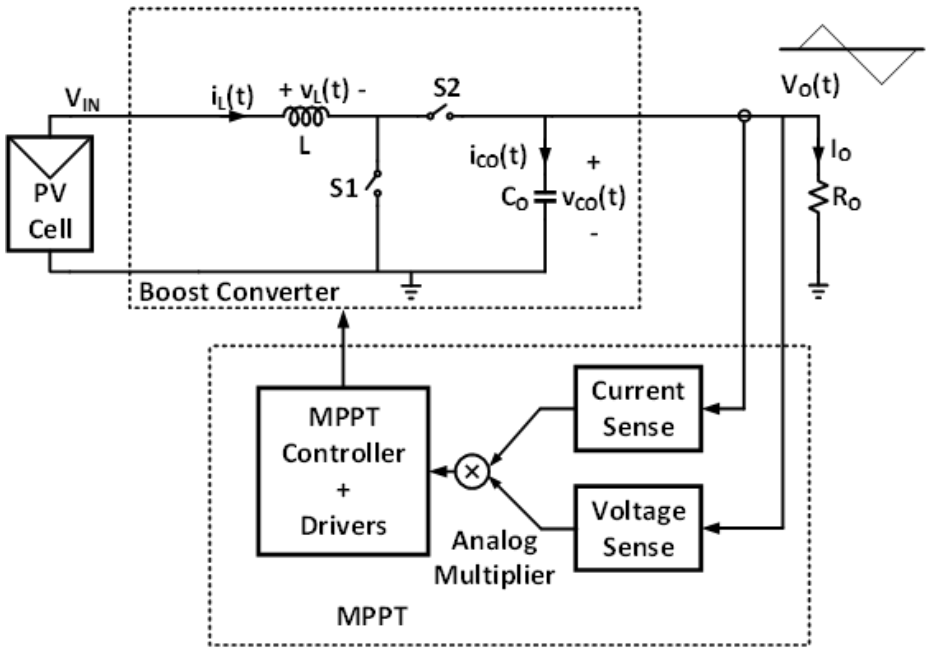

Figure 5.3: Simplified Diagram of a Conventional MPPT System Utilizing Voltage Sensing, Current Sensing, and Analog Multiplier [4, 5]

This paper presents an efficient, CMOS compatible fully integrated analog power/current sensor architecture to sense the power/current at the DC-DC converter output. The proposed architecture [70, 71] addresses the limitation of the conventional analog or digital power sensors. It does not require any series resistance in the current path, thereby eliminating power loss and voltage drop. Additionally, the power is calculated without digitizing the sensed voltage and current using ADCs, or multiplying the digitized values in DSPs/FPGAs. Moreover, this architecture also achieves the

advantage of isolating the high voltage power circuit and low voltage CMOS compatible sensor circuits. In addition to being useful in MPPT, the proposed sensor can also be used for monitoring average current in current sensing applications.

CHAPTER 6

POWER SENSOR SYSTEM DESIGN

The block diagram of a boost converter with a MPPT controller and the proposed power sensor is shown in Figure 6.1(a). T_S and D are the time period and duty cycle of the boost converter switching clock, respectively. In steady state condition, the output voltage ($V_O(t)$) of the converter has a periodic ripple voltage ($V_{O\_RIPPLE}(t)$) around the DC voltage (V_{O_AVG}) as shown in Figure 6.1(b). During the inductor charging phase (S1: close, S2: open), the output capacitor (C_O) supplies the load current (I_O). Hence, the slope of $V_{O\_RIPPLE}(t)$ can be expressed as,

$$\frac{dV_{O\_RIPPLE}(t)}{dt} = \frac{I_{CO}(t)}{C_O} \approx -\frac{I_O}{C_O} \tag{6.1}$$

Where, $I_{CO}(t)$ is the current through C_O, and I_O is the average load current. Therefore, a differentiator can be used to extract I_O from the slope of $V_{O\_RIPPLE}(t)$. If a RC differentiator as shown in Figure 6.2 is employed for differentiating the ripple, its output V_{O_DIFF} can be expressed as

$$V_{O\_DIFF} = -C_{DIFF}R_{DIFF}\frac{dV_{O_{RIPPLE}}(t)}{dt} \tag{6.2}$$

Using 6.1, 6.2 can be rewritten as

$$V_{O\_DIFF} = C_{DIFF}R_{DIFF}\frac{I_O}{C_O} \tag{6.3}$$

Equation 6.3 shows that the output of the differentiator (V_{O_DIFF}) is proportional to the load current (I_O), where C_{DIFF} and R_{DIFF} are the value of capacitor and

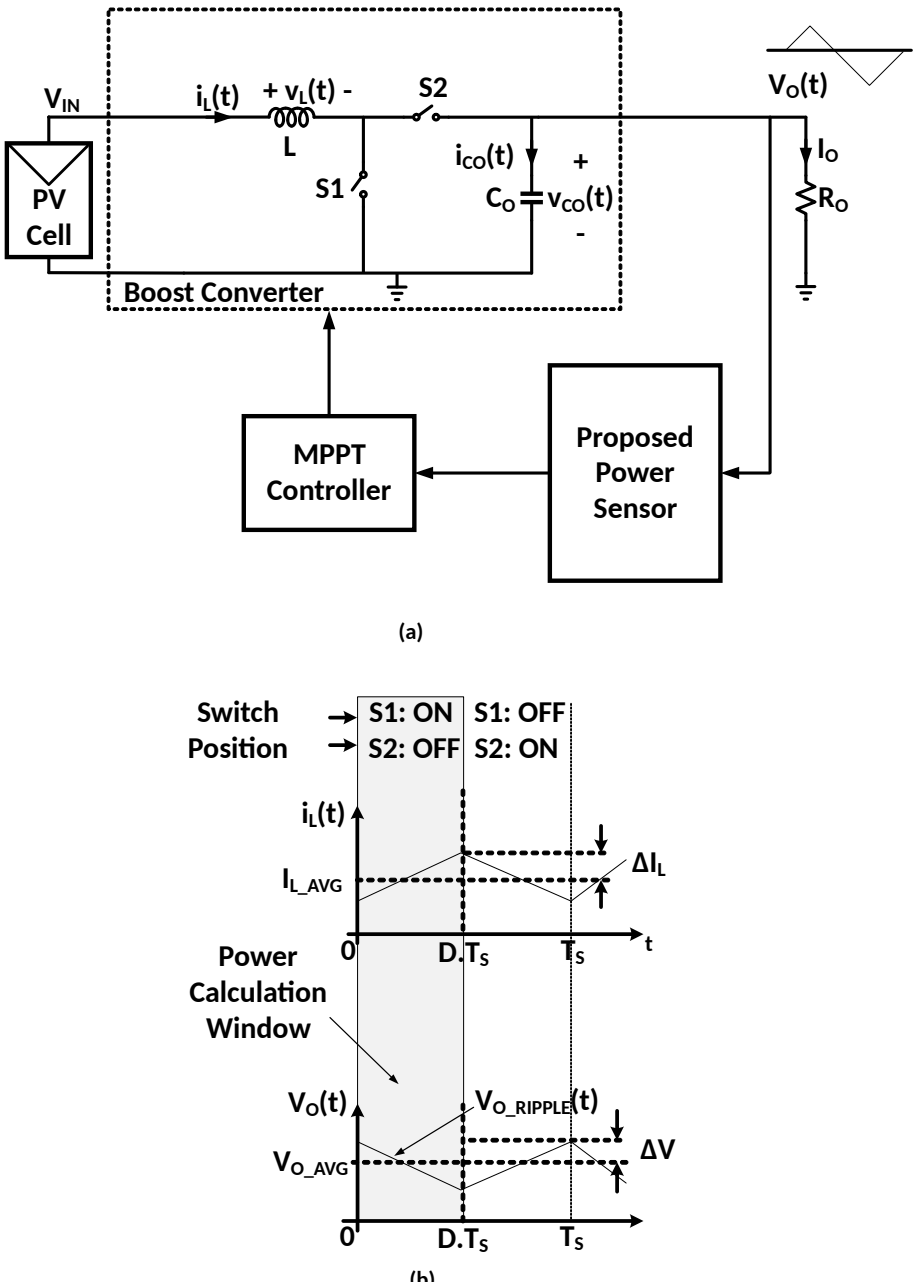

Figure 6.1: (a) Simplified Block Diagram of the Proposed Power Sensor in a MPPT System, and (b) Inductor Current and Output Voltage Waveforms of the Boost Converter.

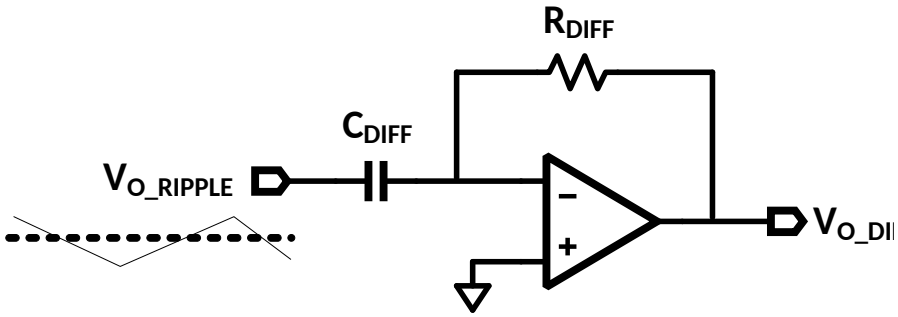

Figure 6.2: An Opamp-RC Differentiator.

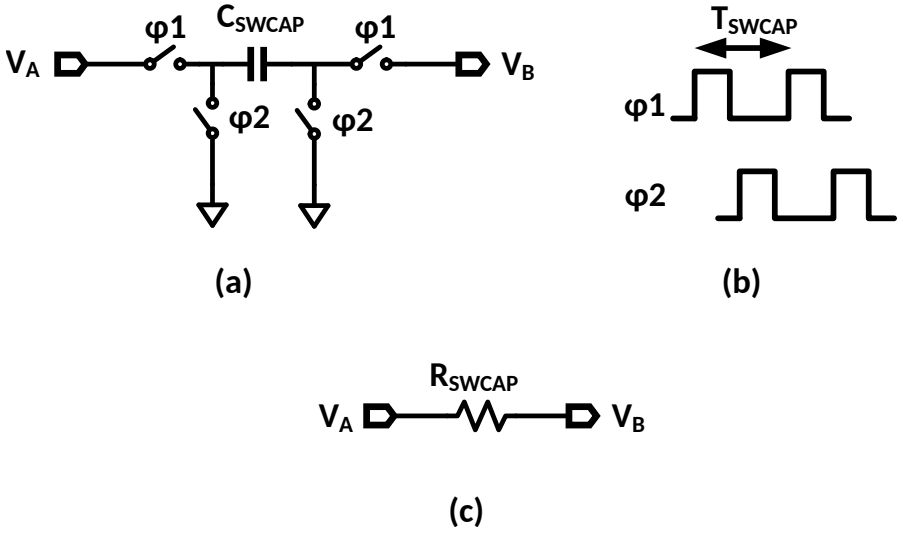

Figure 6.3: Switched Capacitor Based Resistor. (a) Circuit Diagram. (b) Timing Diagram. (c) Equivalent Resistor.

resistor, respectively, providing the differentiator time constant $C_{DIFF}R_{DIFF}$.

6.1 Power Sensor

The proportionality constant term in Equation 6.3 is the differentiator time constant $C_{DIFF}R_{DIFF}$. If the term $C_{DIFF}R_{DIFF}$ can be made proportional to V_{O_AVG}, then V_{O_DIFF} can be expressed as.

$$V_{O\_DIFF} \propto V_{O\_AVG} I_O \tag{6.4}$$

Equation 6.4 shows that the differentiator output is proportional to the output power delivered to the load. One way to achieve this is by making R_{DIFF} proportional to the V_{O_DIFF}. A variable resistor can be implemented by using switched capacitor technique. Resistor implemented by a switch capacitor network [72] depicted in Figure 6.3(a) can be expressed as

$$R_{SWCAP} \propto \frac{T_{SWCAP}}{C_{SWCAP}} \tag{6.5}$$

where, R_{SWCAP} is the equivalent resistance of the switched capacitor network, C_{SWCAP} is the value of capacitor, and T_{SWCAP} is the time-period of the clock signal in the switch capacitor network. T_{SWCAP} can be made proportional to the V_{O_AVG} using a Voltage to Time Converter (VTC), to get a R_{SWCAP} proportional to V_{O_AVG}. Thus, achieving a value proportional to the average output power of boost DC-DC converter at the differentiator output.

6.2 Power Sensor Architecture

A differentiator with a switch capacitor resistor is used in this work as a power sensor. The clock signal for this Switched Capacitor Differentiator (SCD) [73] is generated from a VTC. The simplified block diagram of the proposed power sensor consisting of a SCD and a VTC is depicted in Figure 6.4.

6.2.1 Switched Capacitor Differentiator

SCD is shown in the Figure 6.5(a). The timing control of phase φ 1 and φ 2 are shown in Figure 6.5(b). The net change of charges C_1 during the clock period T is

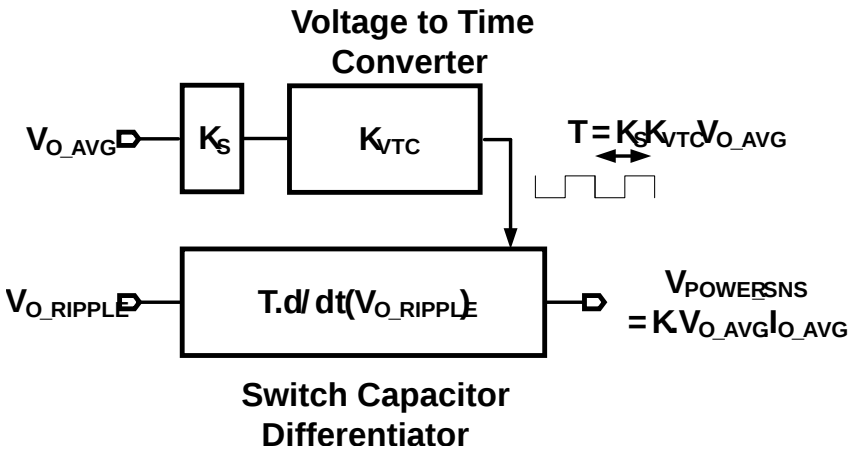

Figure 6.4: Simplified Block Diagram of the Proposed Power Sensor.

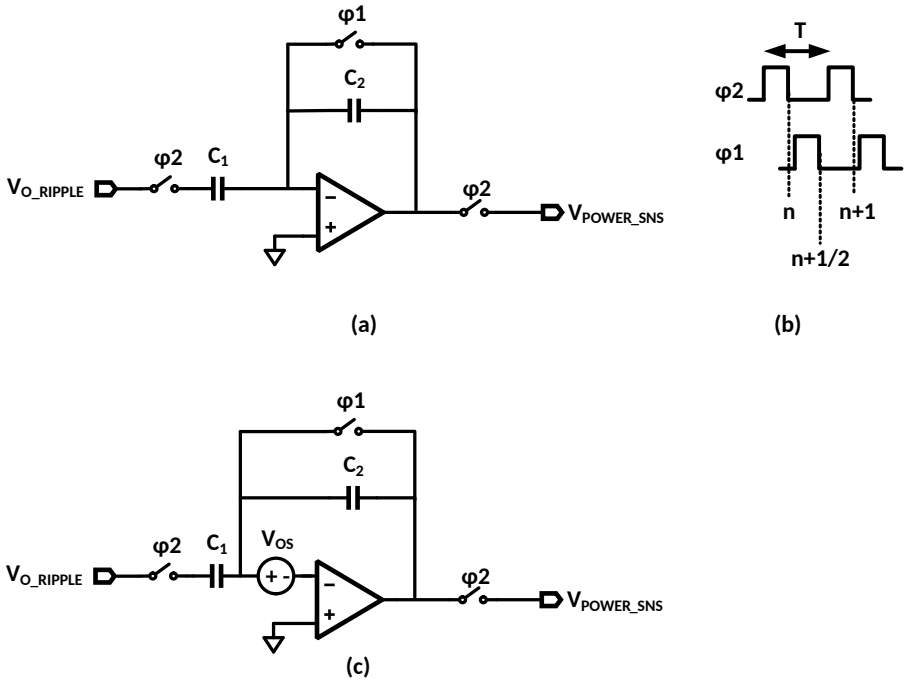

Figure 6.5: Switch Capacitor Differentiator. (a) Circuit Diagram. (b) Timing Diagram. (c) Circuit Diagram with Opamp Input Offset.

$C_1(V_{O\_RIPPLE}[(n+1)T]–V_{O\_RIPPLE}[nT])$, this charge will be transferred to C_2 during the phase φ 2. Thus, the output voltage V_{POWER_SNS} can be written as

$$V_{POWER\_SNS}\left[(n+1)\,T\right] = -C_1\frac{\left(V_{O\_RIPPLE}\left[(n+1)\,T\right] - V_{O\_RIPPLE}\left[nT\right]\right)}{C_2} \tag{6.6}$$

Applying the z transformation on equation 6.6

$$V_{POWER\_SNS}\left[z\right] = -C_1\frac{\left(1-z^{-1}\right)V_{O\_RIPPLE}\left[z\right]}{C_2} \tag{6.7}$$

Applying the Euler mapping [74] with $s = (1 - z^{-}1)/T$, equation 6.7 in s-domain can be written as

$$V_{POWER\_SNS}\left(s\right) = -sT.\frac{C_1}{C_2}.V_{O\_RIPPLE}\left(s\right) \tag{6.8}$$

The s domain expression in equation 6.8 realizes a differentiation function. Applying the inverse s transformation, the time domain expression can be given as

$$V_{POWER\_SNS}\left(t\right) = -T.\frac{C_1}{C_2}.\frac{dV_{O\_RIPPLE}\left(t\right)}{dt} \tag{6.9}$$

By comparing equation 6.8 with equation 6.2, it can be observed that the SCD of Figure 6.5(a) has an equivalent resistor of T/C2. Using equation 6.1 the output of differentiator operating on the boost converter output ripple is

$$V_{POWER\_SNS}\left(t\right) = T.\frac{C_1}{C_2}.\frac{I_O}{C_0} \tag{6.10}$$

Opamp input offset can introduce additional term in equation 6.10. A SCD including the offset is shown in Figure 6.5(c), where VOS is the equivalent DC offset at the opamp inverting input terminal. The similar analysis will yield the expression,

$$V_{POWER\_SNS}\left(t\right) = T.\frac{C_1}{C_2}.\frac{I_O}{C_0} + V_{OS} \tag{6.11}$$

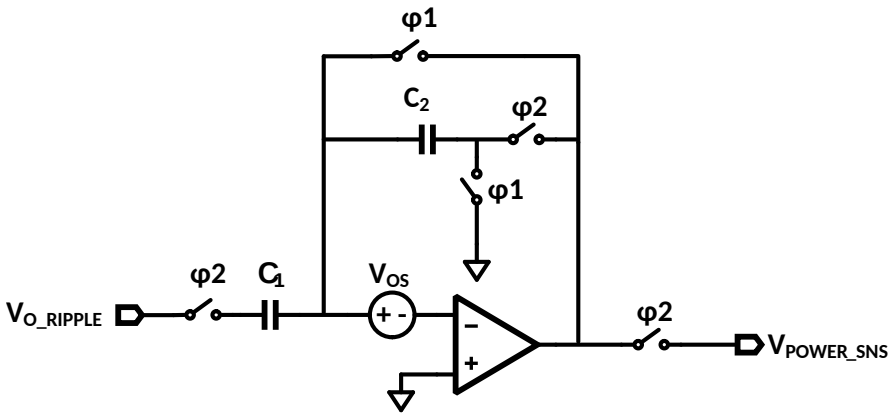

Figure 6.6: SCD with Offset Cancellation.

6.2.2 Opamp Offset Cancellation

To mitigate the effect of non-zero offset of the opamp, offset cancellation technique proposed in [75], is used. The modified SCD is shown in the Figure 6.6. During the phase $\varphi 1((n+1/2)T)$, the capacitor C_2 will store the offset voltage $(-V_O S)$, and $(V_{POWER\_SNS}[(n+1)T] - V_{OS})$ during $\varphi 2((n+1)T)$. The net change of charge on C_2 during clock period T, is

$$\Delta Q_2 = C_2(V_{POWER\_SNS}[(n+1)T] - V_{OS}) - (-V_{OS}) = C_2.V_{O\_RIPPLE}[(n+1)T]) \tag{6.12}$$

The capacitor C_1 will sample $(V_{O\_RIPPLE}[nT] - V_{OS})$ during phase $\varphi 2(nT)$, and $(V_{O\_RIPPLE}[(n+1)T] - V_{OS})$ in the next phase $\varphi 2((n+1)T)$. The net change of charge on C_1 during the clock period T, is

$$\begin{aligned}\Delta Q_1 = C_1((V_{O\_RIPPLE}[(n+1)T] - V_{OS}) - (V_{O\_RIPPLE}[nT] - V_{OS})) \\ = C_2.V_{O\_RIPPLE}[(n+1)T])\end{aligned} \tag{6.13}$$

The total change of charge, $\Delta Q_1 + \Delta Q_2$ should be equal to zero, this will yield the same expression as equation 6.6, and following the further similar analysis, equation 6.10 will be obtained. Thus, the effect of opamp input offset is mitigated. Moreover, the effect of low frequency 1/f noise is also mitigated by this technique [75].

6.2.3 Alternate Architecture for SCD

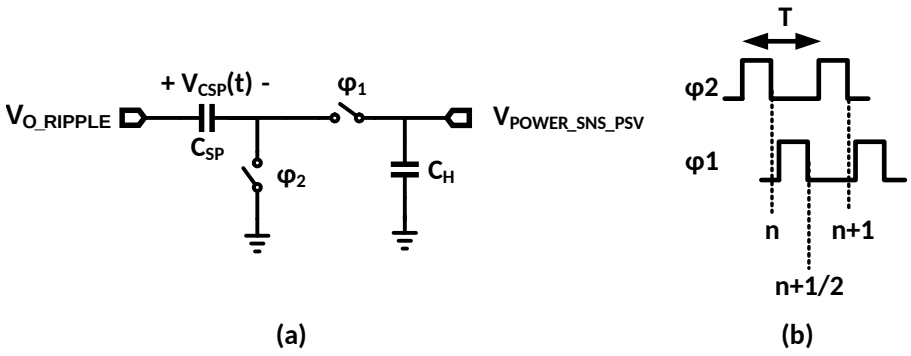

Figure 6.7: Passive implementation of SCD. (a) Circuit Diagram. (b) Timing Diagram.

A passive implementation of SCD as shown in Figure 6.7(a) can also be used in the power sensor. During the phase $\varphi 2(nT)$, the capacitor CSP will charge to the input voltage $V_{O\_RIPPLE}[nT]$, this voltage will be stored in the capacitor. During $\varphi 1((n+0.5)T)$, the stored capacitor voltage will be subtracted from $V_{O\_RIPPLE}[(n+0.5)T]$ and the resultant voltage will be sampled on the output cap C_H. Thus, the passive SCD output voltage $V_{POWER\_SNS\_PSV}$ can be written as

$$V_{POWER\_SNS\_PSV}\left[(n+0.5)\,T\right] = V_{O\_RIPPLE}\left[(n+0.5)\,T\right] - V_{O\_RIPPLE}\left[nT\right] \qquad (6.14)$$

Applying the z transformation on equation 6.14

$$V_{POWER\_SNS\_PSV}[z] = \left(1 - z^{-1/2}\right) V_{O\_RIPPLE}[z] \tag{6.15}$$

Applying the s-to-z transformation [74] with z = exp(sT), and assuming $sT << 1$, equation 6.15 in s-domain can be written as

$$V_{POWER\_SNS\_PSV}(s) = \frac{sT}{2}.V_{O\_RIPPLE}(s) \tag{6.16}$$

The s domain expression in equation 6.16 realizes a differentiation function similar to equation 6.8. Applying the inverse s transformation, the time domain expression can be given as

$$V_{POWER\_SNS\_PSV}(t) = \frac{T}{2}.\frac{dV_{O\_RIPPLE}(t)}{dt} \tag{6.17}$$

Using equation 6.1, equation 6.17 can be rewritten as

$$V_{POWER\_SNS\_PSV}(t) = -\frac{T}{2}.\frac{I_O}{C_0} \tag{6.18}$$

The advantage of the passive SCD is less power consumption, less area, and less added offset/noise due to the opamp-less design. The only drawback of the passive SCD is that it cannot provide any gain like an active SCD implementation. Hence, the power sensor resolution is limited by the noise and offset of the following comparator or amplifier stage.

6.2.4 Voltage to Time Converter

A Voltage to Time Converter (VTC) is shown in Figure 6.8(a), this circuit is derived from the simplified version of an RC relaxation oscillator [76]. The capacitor, C is charged by a constant current I, as a result the voltage across capacitor VC increases linearly with the time. When V_C crosses V_{CTRL_VTC}, the comparator output

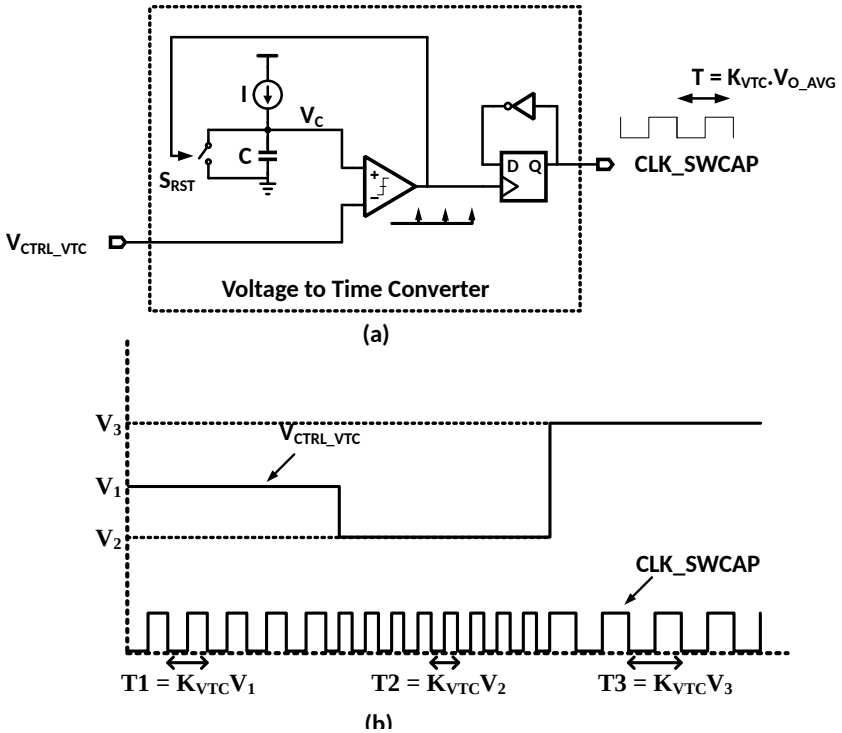

Figure 6.8: Voltage to Time Converter. (a) Schematic Diagram. (b) Timing Diagram.

becomes logic high, which turns on the switch S_{RST}. This leads to the discharging of the capacitor, and the comparator output becomes logic zero, which in turn starts charging the capacitor again and this cycle repeats periodically. A D-flip-flop (DFF) based divide-by-2 circuit is used to generate a 50% duty cycle clock signal. A typical waveform of VTC is shown in Figure 6.8(b). The time-period T of the VTC output clock CLK_SWCAP is proportional to $VCTRL\_VTC$ as shown in equation 6.19.

$$T = K_{VTC}V_{CTRL\_VTC} \tag{6.19}$$

where, K_{VTC} is

$$K_{VTC} = \frac{2C}{I} \tag{6.20}$$

CHAPTER 7

POWER SENSOR INTERFACE WITH BOOST CONVERTER

The detailed schematic of the proposed power sensor utilizing the SCD and VTC is depicted in Figure 7.1(a) and the waveforms in Figure 7.1(b). This CMOS compatible low voltage domain power sensor can be interfaced to the high output voltage of the boost converter as shown in Figure 7.2. The DC electrical isolation between high output voltage of boost V_O and the SCD input of the power sensor is achieved by the coupling capacitor C_C, which forms a high pass filter with resistor R_C. The low voltage compatibility for V_{CTRL_VTC} input of the power sensor is achieved by scaling V_O down by a factor K_S. Where the scaling factor $\mathrm{K_S = R_2/(R_1 + R_2)}$, and is less than unity. A capacitor $\mathrm{C_{LPF}}$ is added in parallel with resistor $\mathrm{R_2}$ to form a low pass filter (LPF), to extract only the average DC component $\mathrm{V_{O\_AVG}}$ of $\mathrm{V_O}$. These high pass and low pass filters do not affect the boost converter performance, as these filters are not part of the voltage regulation loop of the boost. The relation between $\mathrm{V_{CTRL\_VTC}}$ and $\mathrm{V_{O\_AVG}}$ can be expressed as

$$V_{CTRL\_VTC} = K_S V_{O\_AVG} \tag{7.1}$$

Using equation 6.10, 6.19, and 7.1 the power sensor output in terms of the average output voltage V_{O_AVG} and the average output current I_O can be expressed as,

$$V_{CTRL\_VTC} = K_S V_{O\_AVG} \tag{7.2}$$

Where K is

$$K = K_S K_{VTC} \frac{C_1}{C_2} \frac{1}{C_0} \tag{7.3}$$

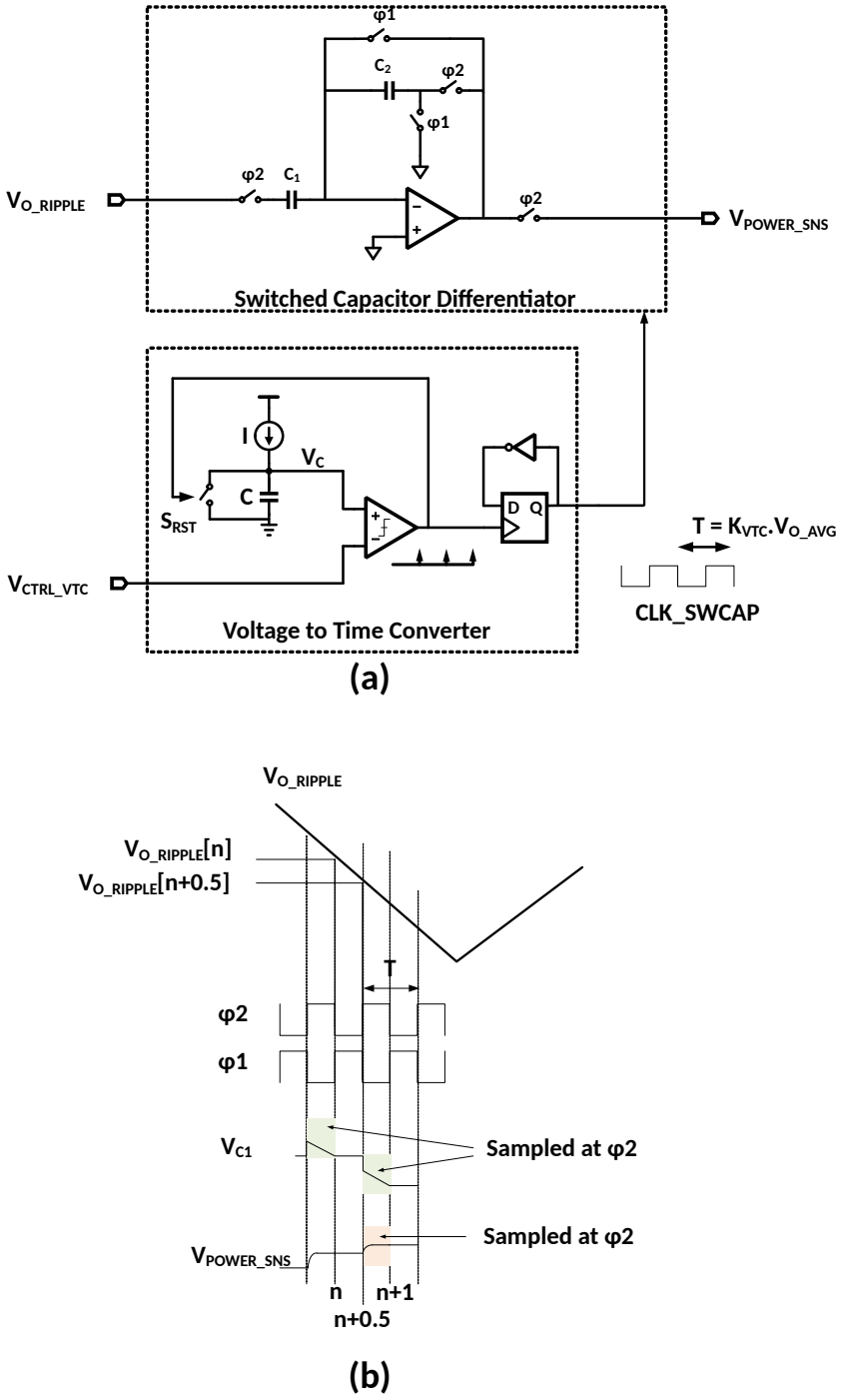

Figure 7.1: Proposed Power Sensor. (a) Detailed Diagram. (b) Timing Diagram of the SCD Signals.

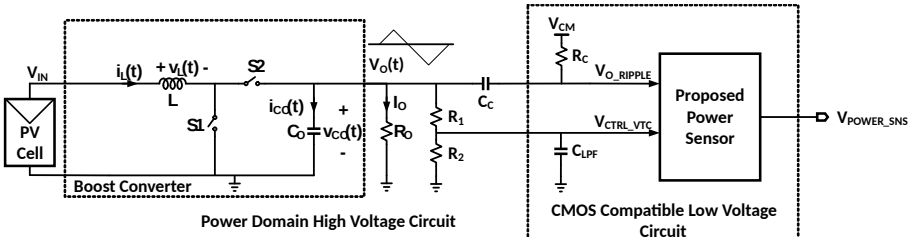

Figure 7.2: Interface of the Proposed Power Sensor with the Boost Converter Emphasizing the Electrical DC Isolation Between High Voltage and Low Voltage Domain.

From equation 7.3, it can be observed that the proposed power sensor output is proportional to the average power delivered by the boost converter.

The relation between the time-period of VTC output clock CLK_SWCAP and the switching time-period of the boost converter should be chosen with the consideration that the SCD operates on the V_{O_RIPPLE} in inductor charging phase and needs at least a clock cycles of CLK_SWCAP in this power sensing window. The condition can be expressed as,

$$max\{T\} < D.T_S \tag{7.4}$$

Therefore, the sampling clock frequency should be at least 1/D times faster than the boost converter switching frequency.

The power sensor can be configured to sense the current only. This can be achieved by using a clock signal of a fixed time-period for SCD, instead of providing it from the VTC. In this case, the power sensor will provide only the sensed current information.

7.1 Effect of Boost Output Capacitor ESR

If output capacitor has an equivalent series resistance (ESR), its effect on the proposed power sensor can be analyzed as has been done for IDC in [69]. Figure 7.3(a)

Table 7.1: AREA OF DIFFERENT SUB-CIRCUIT BLOCKS IN PROPOSED POWER SENSOR

	Area (µm2)	**% of Total Area**
SCD	41766	80.55
VTC	4984	9.61
Logic	5100	9.84
Total	51850	100

shows the output stage of the boost converter depicted in Figure 7.2 with capacitor C_O with an ESR of R_{ESR}. Figure 7.3(b) shows the output voltage $V_O(t)$ during the boost inductor charging phase (S1: close, S2: open),

$$V_O(t) = V_{CO}(t) + R_{ESR} i_{CO}(t) \tag{7.5}$$

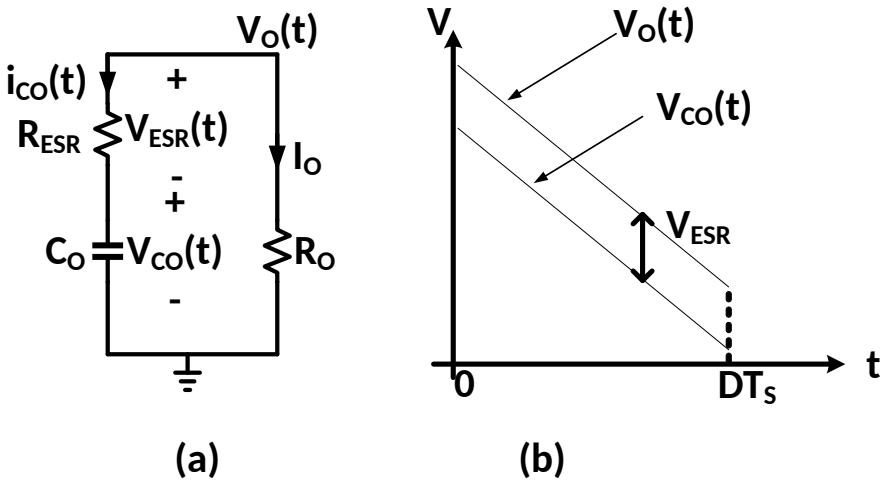

Figure 7.3: Load Capacitor with Effective Series Resistance (ESR). (a) Circuit Diagram. (b) Voltage Ripple During the Boost Inductor-Charging Phase.

Where $V_{CO}(t)$ is the voltage across C_O. Since $i_{CO}(t)$ is almost constant and equal (with opposite sign) to the average load current I_O during the small time period of sensing, equation 7.5 can be rewritten as

$$V_O(t) = V_{CO}(t) - I_O R_{ESR} \tag{7.6}$$

From equation 7.6 it can be seen that the $V_O(t)$ and $V_{CO}(t)$ differ by a constant DC voltage $I_O R_{ESR}$. As the SCD only operates on the AC ripple present in $V_O(t)$, the derivative of $V_O(t)$ can be written as,

$$\frac{dV_O(t)}{dt} = \frac{dV_{CO}(t)}{dt} \tag{7.7}$$

It can be seen that derivative of the $V_O(t)$ and $V_{CO}(t)$ are equal, and so the sensed current/power. Therefore, the effect of ESR resistance R_{ESR} can be neglected for the proposed power sensor.

CHAPTER 8

POWER SENSOR SIMULATION RESULTS

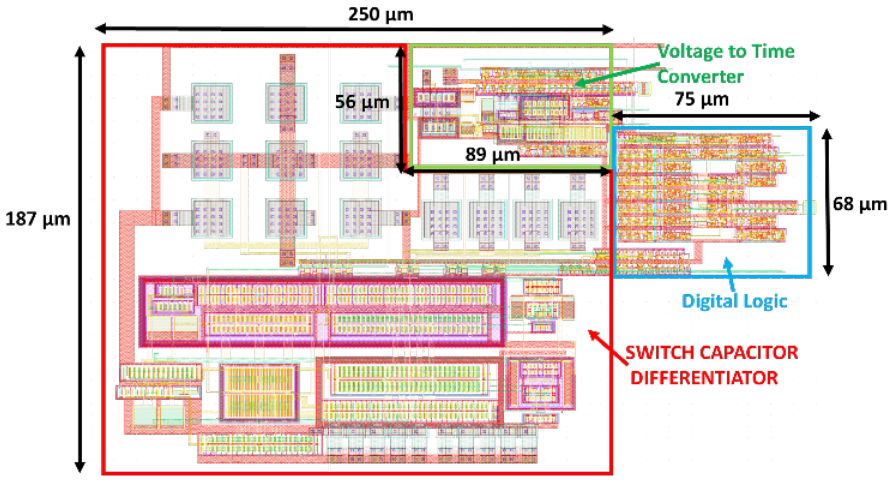

Figure 8.1: Layout of the Proposed Power Sensor.

The proposed power sensor is designed in a 0.18 μm CMOS process, and operates at the nominal supply voltage of 1.8 V. The power sensor occupies 0.0519 mm^2 of silicon area, and consumes nominal current of 424 μA from the 1.8 V supply. The layout of the proposed power sensor circuit is shown in Figure 8.1. The area breakdown of various sub-circuits of the designed power sensor is listed in table I. The proposed power sensor is interfaced with the boost converter as shown in Figure 7.2. Input voltage, V_IN of the boost converter is 0.5 V, and switches S_1 and S_2 are operated from a non-overlapping clock generated from a switching clock $SWCLK\_BOOST$ of 500 kHz frequency. Value of K_S is set to 0.2 by choosing $R_1 = 40k\Omega$ and $R_2 = 10k\Omega$. The low pass filter cap C_LPF is 2 nF, setting the cutoff frequency of the low pass filter formed by R_1, R_2, and C_LPF to 9.95 kHz. The VO_RIPPLE coupling capacitor $C_C = 1F$, and value of RC is 10 Ωwhich sets the cutoff frequency of the high pass filter to 7.96 kHz. The VTC has a current I = 1 µA, MIM capacitor C = 0.5 pF.

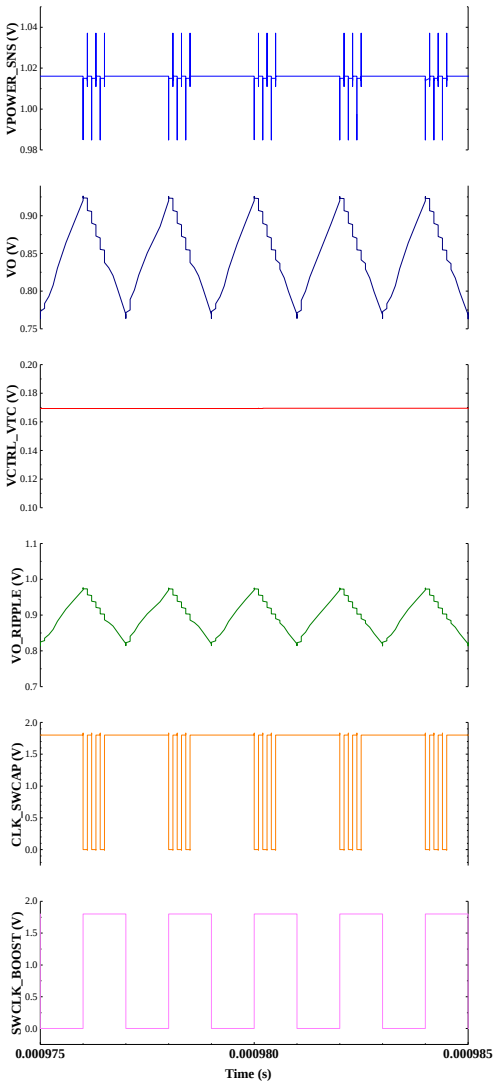

Figure 8.2: Simulated Waveform of V_{POWER_SNS}, V_O, V_{CTRL_VTC}, V_{O_RIPPLE}, CLK_SWCAP, and SWCLK_BOOST in the Proposed Power Sensor and DC-DC Boost Converter.

The SCD also uses MIM capacitors for C_1 and C_2, of the value $C_1 = 2$ pF and $C_2 = 0.5$ pF, to provide the active gain of $C_1/C_2 = 4$. The design component and parameter values are summarized in TABLE 8.1. The simulated waveforms for the key signals of the boost converter and the proposed power sensor are shown in Figure 8.2. It is

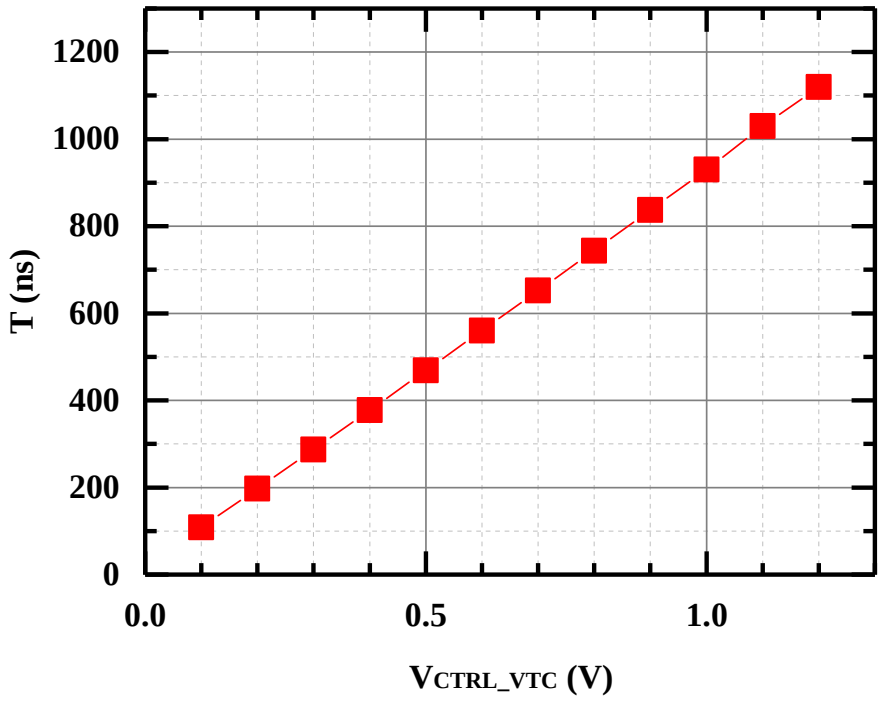

Figure 8.3: Simulated Performance of the VTC. The Time Period T of the VTC Output Clock is Plotted Versus the Control Voltage V_{CTRL_VTC}.

important to note that the CLK_SWCAP is only activated in power sensing window and remains logic high for rest of the time to save the switching power in SCD. The VTC output clock time-period T versus the control voltage VCTRL_VTC is plotted in the Figure 8.3.

The proposed power sensor performance is summarized in the TABLE 8.2. The power sensor is characterized for the I_O up to 1 A. The plot of the proposed power sensor output and the expected ideal power sensor values versus IO are plotted in Figure 8.4 and Figure 8.5 for 60% and 40% duty cycle, respectively. The ideal power sensor value will be K times the actual average output power delivered by the boost as per equation 7.2.

The current consumption of the proposed power sensor versus the load current IO

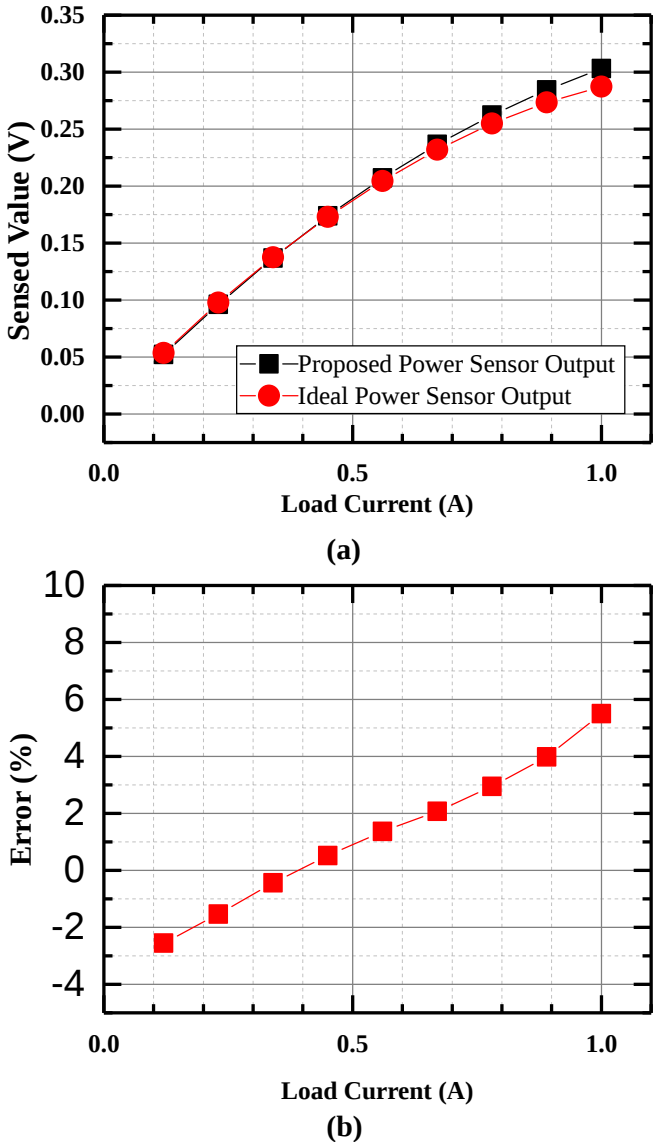

Figure 8.4: Simulated Performance of the Proposed Power Sensor and Ideal Power Sensor (Boost Converter Operating at 60% Duty Cycle). (a) Sensed Value Versus Load Current. (b) Error Versus Load Current.

is plotted in Figure 8.6(a), which illustrates that the power consumption is relatively constant with increasing I_O. Power consumed by a series resistor of 20 mΩconducting the same I_O is plotted on the same graph in Figure 8.6(b). It can be observed

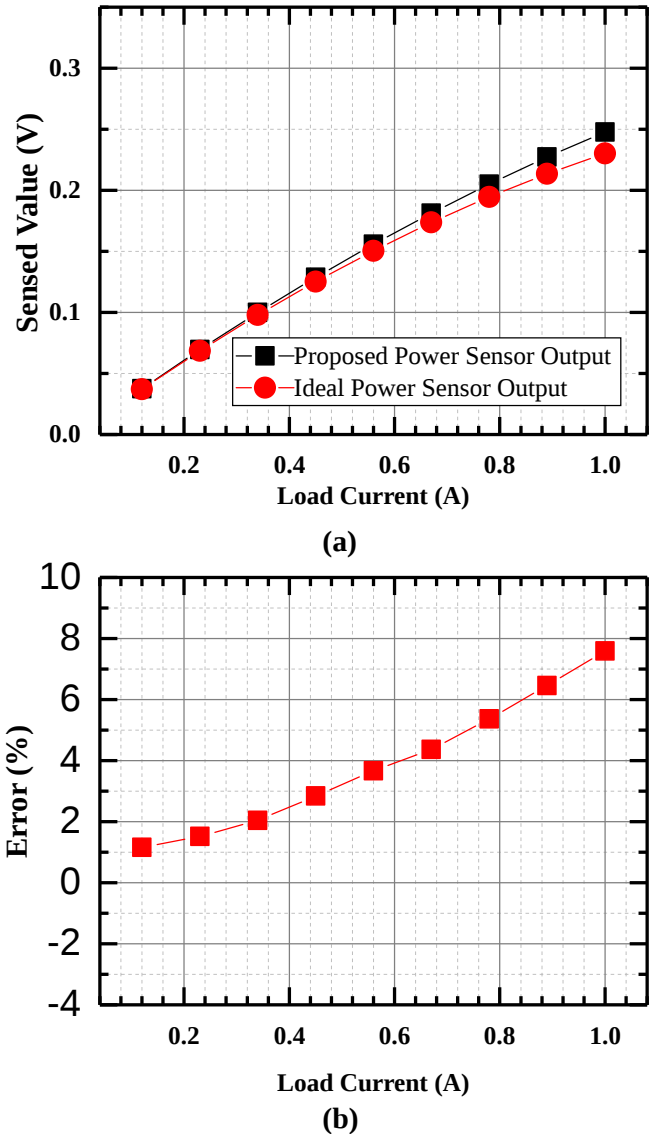

Figure 8.5: Simulated Performance of the Proposed Power Sensor and Ideal Power Sensor (Boost Converter Operating at 40% Duty Cycle). (a) Sensed Value Versus Load Current. (b) Error Versus Load Current.

that the power loss in series resistor based approach increases with increasing the I_O quadratically (I2R loss). Also, note that this is the power dissipated across the sense resistor only. The power required by additional circuitry such as sense amplifier,

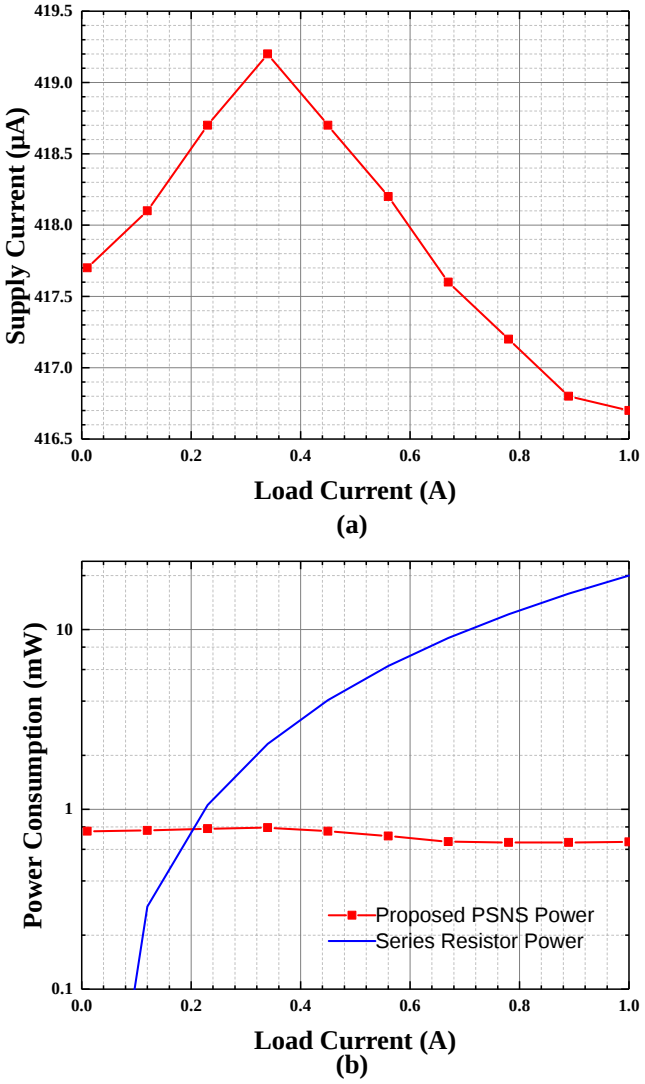

Figure 8.6: Simulation characteristics of (a) Supply Current Drawn by the Proposed Power Sensor. (b) Power Consumed by Proposed Power Sensor and Power Dissipated Across a Series Sense Resistor of $20m\Omega$.

ADCs, DSP is not included. To observe the effect of opamp input offset and to compare the topology of Figure 6.5(c) and Figure 6.6, the power sensor is simulated with the opamp input offset voltage V_{OS} of 5 mV, for this simulation, I_O is set to 340 mA and boost is operating at 50% duty cycle. The error in power sensor due to the

Table 8.1: COMPONENT VALUES FOR BOOST CONVERTER AND PROPOSED POWER SENSOR

Boost Converter's and External Components	
L	30 µH
C_O	2 µF
R_1	40 kΩ
R_2	10 kΩ
C_{LPF}	2 nF
C_C	1 µF
R_C	10 Ω
Power Sensor's Component Values	
C_1	2 pF
C_2	0.5 pF
I	1 µA
C	0.5 pF
Power Sensor Parameters	
K_S	0.2
K_{VTC}	1 µs/V

offset for both the cases of with and without offset cancellation is given in TABLE 8.3. Clearly, it can be seen that the SCD of Figure 6.6 with the offset cancellation has the better accuracy.

A performance comparison with the state-of-the-art power/current sensing tech-

Table 8.2: PERFORMANCE SUMMARY

Technology	**180 nm CMOS**
Core Area	0.0519 mm2
Supply Voltage	1.8 V
Switching Frequency of Boost Converter	500 KHz
Current Consumption from Supply	424 µA
Power Consumption	0.763 mW
Accuracy	±7.6 %

Table 8.3: ACCURACY WITH AND WITHOUT OFFSET CANCELLATION

SCD	**Error in Sensed Power (%)**
Without Offset Cancellation	4.71
With Offset Cancellation	0.87

nique is summarized in the TABLE 8.4.

Table 8.4: PERFORMANCE COMPARISON WITH STATE-OF-THE-ART

Type	**Resistor (1)(2)(5)**	**Current Transformer (1)(3)**	**Hall Effect (1)**	**IDC [69]**	**Pulse Integration (5) [61]**	**This Work (SCD + VTC)**
Process	N.A	N.A	N.A	0.7 µm CMOS	0.35 µm 50 V CMOS	0.18 µm CMOS
CMOS Process Voltage [V]	>20 V	5 V	5 V	5 V	3.3 V	1.8 V
Size/Area [mm2]	78	140	420	4	1.19 (6)	0.0268
Power Consumption [mW]	∼60.3-107.4	∼41.3-82.8	∼187-379	∼27	$0.409 + I_{SNS}^2 R_{SNS}$ (4)	0.748
Lossless current sensing	NO	YES	YES	YES	NO	YES
Can be Integrated in CMOS IC	YES	NO	NO	YES	YES	YES
Number of ADCs Required	2	2	2	1	0	0
DSP/FPGA Required	YES	YES	YES	YES	NO	NO
Provides DC voltage Isolation	NO	YES	YES	YES	YES (6)	YES

(1) Numbers are taken from the comparison table in [69]. The values are for sensing maximum current of 830 mA at 12 V output setting

(2) 20 mΩ sense resistor

(3) 1:20 turn ratio

(4) Power dissipated in RSNS (which is an NMOS) is not explicitly known

(5) Provides DC isolation only if it is low side sensing

(6) Includes the area of the on-chip sensing NMOS. The area is estimated from the die monograph provided in the paper

CHAPTER 9

CONCLUSION AND FUTURE WORK

9.1 Conclusion

A power stage with high power and current density is demonstrated in 65nm CMOS. By combining a higher order notch LC filter and flying capacitor topology the low output voltage ripple and high load current capability are achieved. Measurement results obtained from the prototype power stage operating at 500 MHz indicate the peak efficiency of 71.02% at 780 mA of load current. Moreover, it achieves a current density of 1.377 A/mm^2 and a power density of 0.861 W/mm^2, which is significantly higher than the conventional FIVRs. A multi-phase time-domain comparator is proposed, which offers better time resolution than the conventional time-domain comparators. A highly integrated hysteretic controlled buck converter utilizing the proposed power stage and the proposed time-domain comparator is also demonstrated. The buck converter operates at 180 MHz and achieves a very fast transient response for load transition and reference tracking, due to the hysteretic control, the measured settling time is better than the existing state of the art. A comparison between the existing state of the art is also provided for both proposed power stage and for the time-domain hysteretic controlled buck converter.

Also a novel architecture of a lossless power sensor designed in 0.18 µm CMOS process is presented. The proposed design is based on the switch capacitor differentiator and voltage-to-time converter. The proposed approach senses the output power/current of a boost converter without using any series resistor. Moreover, digitizing ADCs and computation DSPs/FPGAs are not required for calculating the power. The proposed power sensor can provide DC electrical isolation between the high output voltage of the DC-DC boost converter and the low voltage CMOS com-

patible power sensor circuit. The effect of load capacitor ESR and opamp input offset on the power sensor are discussed. The power sensor occupies 0.0519 mm2 of silicon area and draw 424 µA current from a supply of 1.8 V. The power sensor achieves the accuracy of ±7.6 %.

9.2 Future Work

FIVR in this thesis is demonstrated with 65nm process. In the future design a modern process such as 14nm or lower can be used to demonstrate that the digital/time domain technique is indeed beneficial for FIVR.

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