Hybrid Envelope Tracking Supply Modulator Analysis and Design for Wideband Applications

by

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ABSTRACT

A wideband hybrid envelope tracking modulator utilizing a hysteretic-controlled three-level switching converter and a slew-rate enhanced linear amplifier is presented. In addition to smaller ripple and lower losses of three-level switching converters, employing the proposed hysteresis control loop results in a higher speed loop and wider bandwidth converter, enabling over 80MHz of switching frequency. A concurrent sensor circuit monitors and regulates the flying capacitor voltage V_{CF} and eliminates conventional required calibration loop to control it. The hysteretic-controlled three-level switching converter provides a high percentage of power amplifier supply load current with lower ripple, reducing the linear amplifier high-frequency current and ripple cancellation current, improving the overall system efficiency. A slew-rate enhancement (SRE) circuit is employed in the linear amplifier resulting in slew-rate of over 307V/μs and bandwidth of over 275MHz for the linear amplifier. The slew-rate enhancement circuit provides a parallel auxiliary current path directly to the gate of the class-AB output stage transistors, speeding-up the charging or discharging of output without modifying the operating point of the remaining linear amplifier, while maintaining the quiescent current of the class-AB stage. The supply modulator is fabricated in 65nm CMOS process. The measurement results show the tracking of LTE-40MHz envelope with 93% peak efficiency at 1W output power, while the SRE is disabled. Enabling the SRE it can track LTE-80MHz envelope with peak efficiency of 91%.

DEDICATION

To my parents.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my advisor Prof. Sayfe Kiaei and Prof. Bertan Bakkaloglu for their continuous support of my Ph.D study and related research, for their patience, motivation, and immense knowledge. Besides, I would like to thank the rest of my dissertation committee members, Dr. Shahin Mehdizad Taleie and Dr. Jennifer Kitchen for their great support and invaluable advice.

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Chapter 1

INTRODUCTION

As the application of handheld devices grows, expectations of them increases, as well. High-speed communication systems connect people around the world and demand for higher speed network increases which requires wideband communication systems. Increasing the frequency spectrum to increase bandwidth is not practical. Thus, to increase bandwidth efficiency of communication systems, complex digital-domain modulation schemes such as QPSK, 64-QAM and OFDM are used, that employs both amplitude-modulation and phase-modulation [1]. This means that radio frequency (RF) signal envelope is not constant and peak to average power ratio (PAPR) of the signals increases dramatically. Thus, high efficiency switching power amplifier (PA) is not suitable to transmit these signals and highly linear PA is required to attain the applied in-band modulation and avoid non-linearity and out-of-band spectral growth. In the other hand the efficiency of linear PAs such as class A, B or AB are very low at back-off region. This arises another criterion for handheld devices: battery charge life-time. PA is one of the most power-hungry components in a transceiver. Thus, circuit designers need to propose wideband, linear and high-efficiency PAs to satisfy high-speed communication with long-lasting batteries demand.

The probability density function (PDF) of an OFDM signal and efficiency of a class-B PAs versus output power are shown in Figure. 1.1. It shows that the PA with the maximum power of 30dBm, most of the time is operating at 10dB back-off power. While the peak efficiency of a class-B is about 78.5%, at 10dB back-off its efficiency drops below 20% and the PA contributes to a large amount of power loss.

Different techniques have been proposed to increase the efficiency of linear PAs

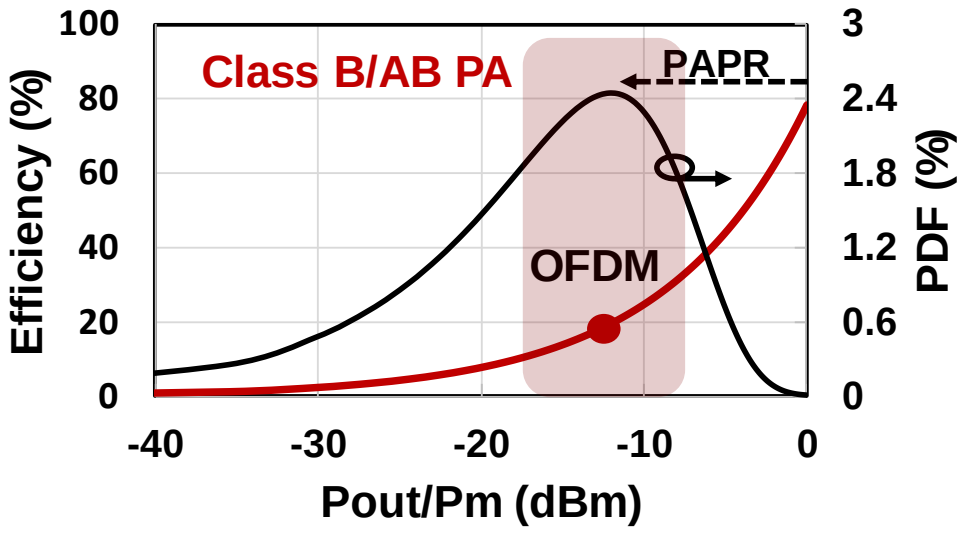

Figure 1.1: PDF of OFDM Signal, and Efficiency of Class-B PA.

[2]. Doherty technique increases the efficiency by active loadline modulation of the PA and providing optimum load for the PA for different input signal level [3]. Since matching network and load-modulation circuit design of Doherty PA depends on the RF frequency, it is usually proper for single-band applications with constant bandwidth and constant center frequency. So, applying Doherty architecture for multiband applications is challenging.

Outphasing technique is also used where the input signal is decomposed into two constant-amplitude, phase only modulated signals. These signals can be summed to provide the desired output using their relative phase. Thus the PA is always operating with a constant envelope input signal at its maximum efficiency. Thus, nonlinear or switch mode PAs can be used to provide the output signal. At the output combiners are employed to to combine constant amplitude, phase modulated signals to a phase and amplitude modulated signal [4, 5].

Supply modulation is a promising technique for multiband application, as the supply modulator operates based on envelope bandwidth and do not depend on the RF center frequency.

Envelope elimination and restoration (EER) is an effective supply modulation method which separates RF phase and RF envelope. High-efficiency and usually non-linear PA amplifies the input signal and maintains RF phase information, and a PA supply modulator, modulation the supply voltage of the PA, provides RF envelope information [6, 7]. In this method, the envelope and phase information of the signal are separated; the phase information is fed to the RF PA with constant signal level to drive the PA at its highest efficiency; the envelope signal is supplied to the PA using supply modulator to combine the phase and envelope information at the output of the PA and retain the amplitude modulation. The PA usually operates as a switching PA with high efficiency. This method is very effective for low bandwidth applications. Since phase and envelope signals face different delays, to avoid non-linearity and spectral regrowth, very fine timing alignment is required between these two paths. As the bandwidth increases, timing mismatch becomes more critical, so applying EER for wideband applications is challenging.

Envelope tracking (ET) supply modulator has gained attention for wideband applications as it utilizes linear PA and both phase and amplitude information is used in the RF path, so time mismatch requirements between envelope and RF path are more relaxed, which makes it applicable for wideband applications [8–12]. In this technique the supply modulator, modulates the supply voltage of the linear PA according to the envelope level, so ideally, it drives the PA at its highest efficiency for the dynamic range. Figure. 1.2 shows the diagram of an envelope tracking PA in the transmitter. In this technique, the overall efficiency is the efficiency of PA multiplied by efficiency of the ET modulator and the modulator efficiency is as important as

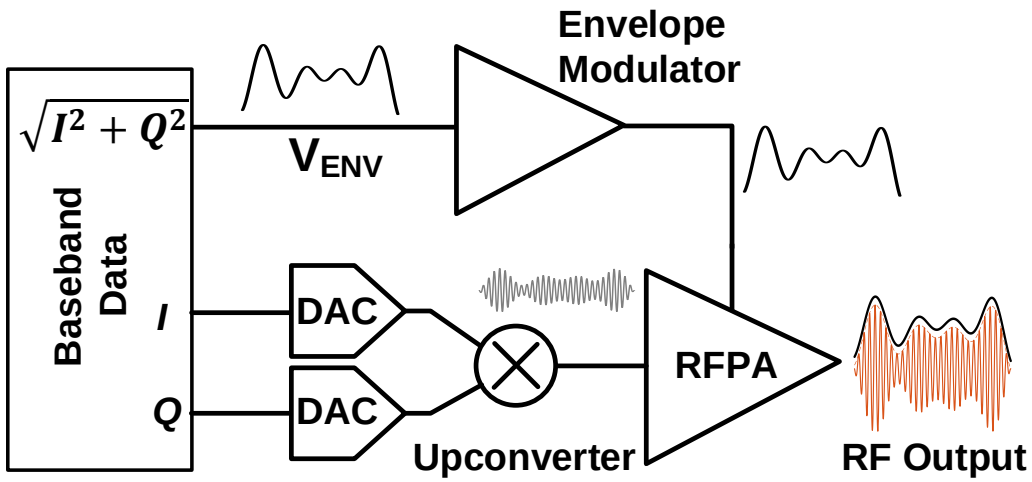

Figure 1.2: Envelope Tracking Technique Diagram.

the PA efficiency. Also, any noise or non-linearity of the modulator will appear at the output of the PA with the PAs power supply rejection ratio (PSRR). Thus, a wideband, low noise ET supply modulator is needed as well as high efficiency.

The rest of this work is organized as follows. Chapter 2 provides literature review and introduces previous methods on envelope tracking with more focus on hybrid envelope tracking modulator design. The advantages and challenges of each method are discussed. In Chapter 3, the proposed hybrid envelope tracking modulator design, system level and circuit level details are explained. The proposed structure is designed and fabricated in 65nm CMOS technology. Measurement results are given in Chapter 4 for proof of concept. Chapter 5 gives the conclusion and future work.

Chapter 2

SUPPLY MODULATOR LITERATURE REVIEW

High data-rate wireless communication systems including LTE, LTE-advanced inter- or intra-band carrier aggregation, with spectral efficient modulation schemes and orthogonal frequency division multiplexing (OFDM) result in high peak-to-average power ratio (PAPR) transmit signals. This requires a wideband, high-efficiency and linear power amplifier (PA) to transmit the signal with low distortion and power loss. Envelope tracking (ET) is widely used to increase the efficiency by modulating the supply voltage of linear PAs according to the envelope level [1, 13–15].

Different ET techniques have been developed ranging from a very simple one such as an LDO, to very advanced techniques with complex control loops and multiple switching and linear amplifiers. Depending on the application and specification different techniques can be used. The manuscript discusses different techniques have been used in hybrid supply modulator design and compares different methods based on their implementation, and applications they suit.

1) Linear regulators: Linear regulators such as low drop out regulator (LDO) provide a wideband low-noise supply modulator, while they are extremely inefficient, as there is large voltage drop across the LDO at lower envelope levels.

2) Switching regulators: Switching regulators form high efficiency modulators. But, they generate large ripple and noise at the output [16]s. To eliminate the ripple, low pass filter (LPF) with large on-chip or off-chip passive components is required. This contributes to extra loss and limits the bandwidth. To increase the bandwidth of the switching regulator, smaller inductor can be used to increase the switching frequency. This approach leads to higher switching losses of the regulator.

3) Hybrid modulators: Hybrid ET modulators, combining high efficiency switching converter (SWC) in parallel with a wideband linear amplifier (LA) has been proposed to provide higher-bandwidth, improved efficiency and linearity. The block diagram of a hybrid modulator is shown in Figure. 2.1(a), along with frequency-domain and time-domain current share of switching converter and linear amplifier in Figure. 2.1(b). In hybrid modulators, the switching converter provides lower frequency content of output current with higher efficiency. The linear amplifier operates at the higher frequency and compensates for the current ripple and slow response of the switching converter. The linear amplifier, however, degrades the efficiency of the modulator in wideband applications. In hybrid modulators, the switching converter provides lower frequency content of output current with higher efficiency. The linear amplifier operates at the higher frequency and compensates for the current ripple and slow response of the switching converter. The linear amplifier, however, degrades the efficiency of the modulator in wideband applications.

2.1 Hybrid Supply Modulator

2.1.1 Efficiency

The efficiency of a switching linear hybrid modulator depends on the efficiency of both switching and linear amplifiers as expressed in:

$$\frac{1}{\eta} = \frac{\alpha}{\eta_{SW}} + \frac{1-\alpha}{\eta_{LA}}. \tag{2.1}$$

Where α is the current ratio of the switching regulator to the output current.

In order to optimize the efficiency of the hybrid modulator the loss mechanisms involved in the modulator are discussed here.

1) The switching regulator:[17]

A conventional switching regulator is shown in Figure. 2.2, which consists of a

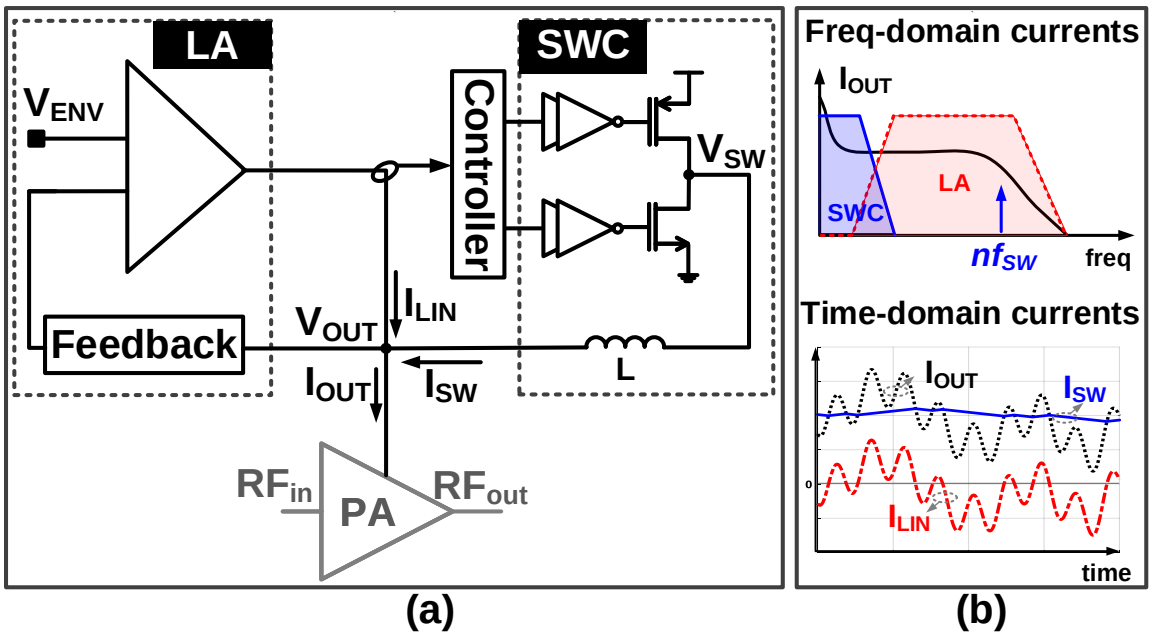

Figure 2.1: (a) Conventional Hybrid Envelope Tracking Modulator Structure, with (b) Time-Domain and Frequency-Domain Current Shares of the LA and SWC.

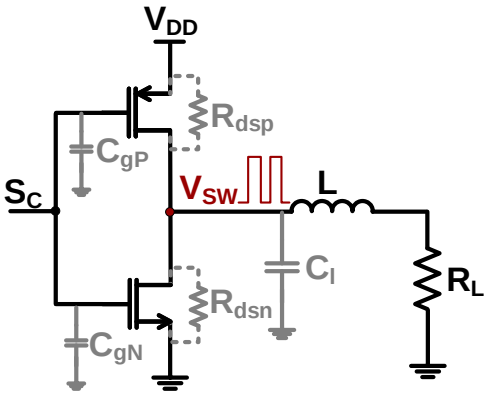

Figure 2.2: Switching Regulator with Parasitics Model.

PMOS switch, a NMOS switch and an inductor. Main power loss sources involved in this architecture are:

a) Switching loss

Parasitic capacitors of the switches in the gate and drain cause a switching loss in the regulator, which is given as PSW.

$$P_{SW} = {V_{DD}}^2 C_p f_{SW}. \tag{2.2}$$

It is clear from the equation that increasing f_{SW} to achieve wider bandwidth, increases the loss. For a given supply voltage (V_{DD}) and f_{SW}, choosing small transistors for power switches, reduces the parasitic capacitor and reduces switching loss.

b) Conduction loss When the either of the switches is on, its equivalent on-resistance inserts a voltage drop in the signal path which contributes to the conduction loss of the regulator, which can be calculated as:

$$P_{COND} = {I_{avg}}^2 R_{ONp} D + {I_{avg}}^2 R_{ONp}(1 - D). \tag{2.3}$$

Where, R_{ONp} and R_{ONn} are equivalent on-resistance of PMOS and NMOS switches, respectively. The duty cycle of the on-time of the PMOS switch is shown with D.

By choosing larger switches, the on-resistance of switches and consequently the regulators conduction loss decreases. Thus, the overall loss of switching regulator can be stated as:

$$P_{SWR} = P_{SW} + P_{COND}. \tag{2.4}$$

Comparing switching loss and conduction loss, there is a trade-off on the switches size selection. Reducing switch size improves switching loss and degrades conduction loss.

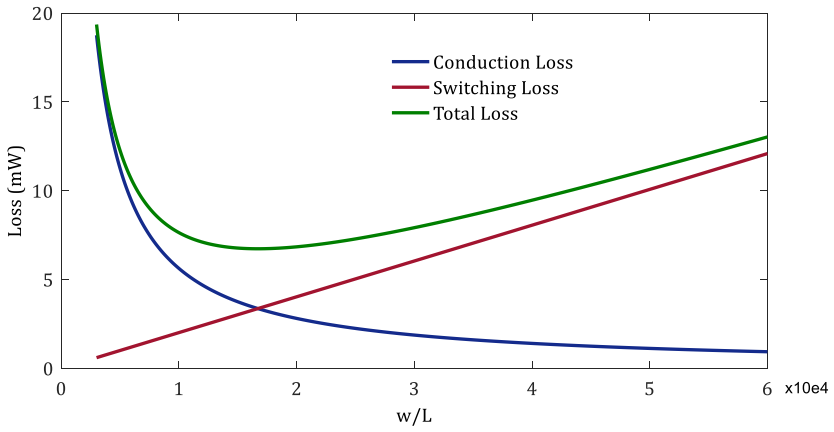

Figure 2.3: Switch Size Design to Achieve Minimum Losses

Thus, for a given switch size, if we increase the switch size by k times, the P_{SW} increases by k times while P_{COND} decreases by k times. Figure. 2.3 shows the P_{SW}, P_{COND} and P_{SWR} for a given switch versus switch size. The switch size should be chosen to have equal P_{COND} and P_{SW}, to minimize the P_{SWR}. This value for D=1/2 is given as:

$$P_{SWRmin} = 2I_{avg}V_{DD}\sqrt{R_{ON}C_P f_{SW}}. \tag{2.5}$$

$$R_{ON} = R_{ONp} + R_{ONn}. \tag{2.6}$$

2) The linear amplifier:

The linear amplifier loss can be divided into two main sources. First constant loss which is because of quiescent bias current of the linear amplifier. Second, dynamic loss, due to class-AB operation of last stage. The class-AB stage loss is divided to PMOS transistor loss and NMOS transistor loss. So, the total loss of the linear amplifier is approximately expressed as:

$$P_{LIN} = P_Q + P_P + P_N. \tag{2.7}$$

$$P_Q = V_{DD} I_Q. \tag{2.8}$$

$$P_N = V_{ENV} I_{LIN}. \tag{2.9}$$

$$P_N = (V_{DD} - V_{ENV}) I_{LIN}. \tag{2.10}$$

The power loss of the linear amplifier increases as its current increases. Thus, different techniques to reduce linear amplifier current is used in literature to reduce power loss and improve the overall efficiency.

2.1.2 Control Methods

There are two main control methods to distribute current between linear and switching regulators: pulse-width modulation (PWM) control method and hysteresis control. The basic operation principle of these control methods, their advantages and challenges, along with new techniques derived from the conventional hysteresis and PWM control are discussed.

PWM Control

In PWM control, the linear amplifier current is converted to a control voltage and after passing through the compensation circuit, it is compared with a synchronization signal and modulated the duty cycle of the PWM signal to generate proper signals to control the switching converter. In PWM control the frequency of switching is precisely controlled. Determined fixed switching frequency in PWM control offers

some advantages. Switching noise of the switching converter can be canceled or attenuated using a notch filter at the harmonics of switching frequency, and EMI be controlled. In addition, multiphase switching converters use PWM control with proper phase alignment between phases to increase effective frequency at the output and reduce ripple current.

As mentioned, to stabilize a PWM controlled loop, compensation circuit is required, where the loop bandwidth is chosen to ensure the loop is stable. For wide-band applications, the compensation circuit design is more challenging as it might cause instability in the loop. Also, it requires synchronization signals generator. In multiphase converters, synchronization signals with precise phase/time alignment is required that in higher frequencies can be challenging.

The PWM control is more of an average voltage/current and its bandwidth is a fraction of switching frequency. Feedforward path in PWM control loop has been used to increase the bandwidth by adding a parallel path to the loop.

2) Hysteresis control:

In a hysteresis-controlled modulator, the linear amplifier is sensed and introduces to a hysteresis comparator to control the switching amplifier current such that the sense signal is bounded to the hysteresis window of the comparator. This type of controller is widely used because of its simple structure and high-speed. Hysteresis controlled loop is stable and does not require compensation circuits. Thus, the loop speed can be as high as switching frequency.

a. Ripple based control: Hysteresis-controlled modulators usually employ a comparator to regulate output voltage or current in a hysteresis window to desired voltage or current value. The comparator continuously compares its two inputs and generates proper signal to control the loop. Thus, the hysteresis loop can operate at very high frequency with a high-speed, depending on the speed of the comparator and other

components in the design. Due to its simplicity and high-speed this technique is utilized in many of the reported ET modulators.

The switching frequency of a hysteresis-controlled loop is:

$$f_{SW} = \frac{R_{sense} V_{OUT}(V_{DD} - V_{OUT})}{2 V_{DD} N L V_{hys}} \tag{2.11}$$

where $V_{DD}, V_{OUT}, V_{hys}, R_{sense}, L$, and N are the supply voltage, the output voltage of the supply modulator, the hysteresis voltage of comparator, the current sensing resistance, the inductance, and the current sensing gain, respectively. By selecting different design parameters V_{hys}, R_{sense}, L, and N , the switching frequency can be optimized between efficiency and linearity [18]. Since the V_{OUT} in envelope tracking applications is variable, the switching frequency of this control method is variable, as well. Due to variable switching frequency, the hysteresis loop does not support multiple switching phases [8].

b. Sensing current using a mirroring stage, removes the loss of the series resistance from the signal path.

c. Average ripple current control with integrating current in the capacitor instead of absolute ripple current control. The basic idea of the proposed single-capacitor current integration (SCCI) control is to use the charge from the LA for control, which is obtained by integrating a scaled version of the output current from the LA. By controlling the maximum amount of charge from the LA, the ripple current of the LA is controlled indirectly [19].

2.1.3 Advanced Techniques in Hybrid Supply Modulators

1) AC-coupling is utilized to improve mid-range power efficiency [20]. As shown in Figure. 2.4(a), the capacitor isolate output envelope level from supply voltage of the linear amplifier and provides level-shift between them. It also ensures no dc

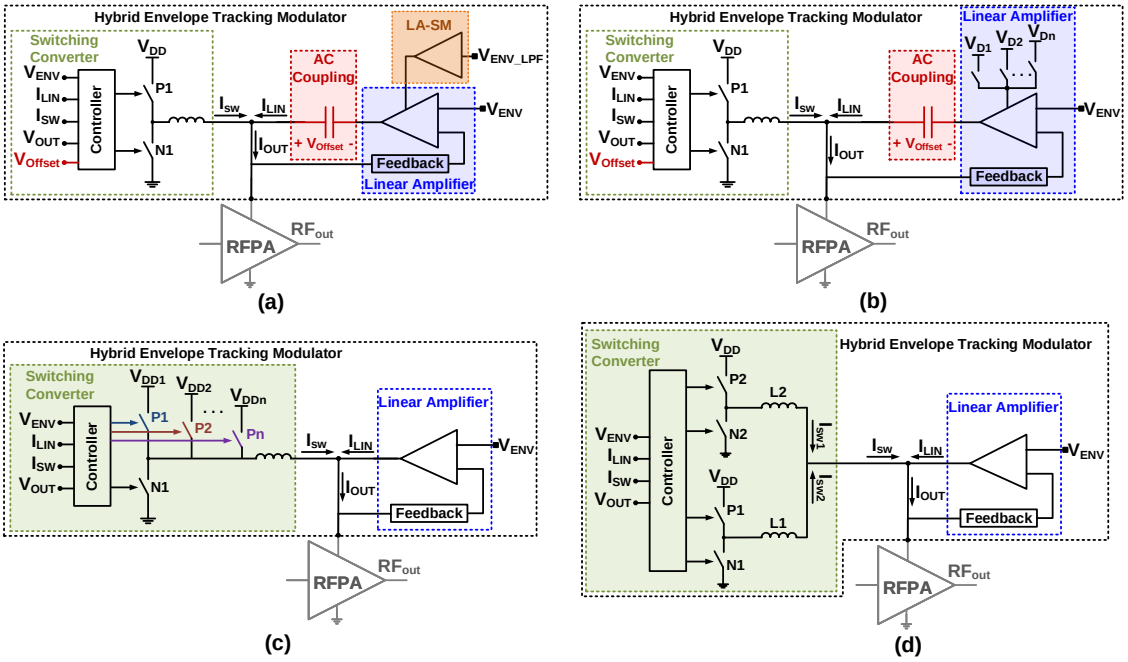

Figure 2.4: Advanced Techniques in Hybrid Supply Modulator. (a) AC-Coupled LA with Different Supply Voltages, (b) Supply Modulated LA in Hybrid Structure, (c) Multilevel Switching Regulator, (d) Dual-Phase Switching Regulator.

current is provided from linear amplifier. In this technique a large capacitor, usually off-chip, isolates linear amplifier output from output node. The voltage across the capacitor need to be carefully regulated to generate proper envelope voltage at the output. Thus, the Class-AB supply voltage should be equal to the ac signal swing, not the peak envelope level, and peak voltage can go above the Class-AB supply voltage. Since, the capacitor isolates the output node voltage form linear amplifiers output, the supply voltage and voltage level of linear amplifier can be designed to optimize the efficiency. To take advantage of that, additional buck/boost converter can be employed to adjust the supply voltage of the linear amplifier according to the envelope level, reducing power loss in the class-AB stage at low power and improving linear amplifier and overall efficiency.

2) One of the advantages of AC-coupling LAs is that the AC-coupling capacitor isolates the supply voltage level of the class-AB from the modulator output voltage.

Thus, the supply voltage of the class-AB does not need to be as high as the peak voltage of the output signals, and it is just needed to be equal to AC swing plus headroom. By using smaller supply voltage for the class-AB linear amplifier, the mid-range efficiency is improved [20]. In addition, the supply voltage of the linear amplifier is controlled with another regulator and the supply is reduced as the average envelope level reduces, resulting in improved efficiency in the back-off region. However, the disadvantages of the AC-coupling capacitor method include: a) extra off-chip capacitor which is usually large and in the F ranges; b) the offset voltage across the AC-coupling capacitor needs to be carefully controlled to attain output envelope signal; c) multi-loop control with increased complexity is required.

Figure. 2.4(a) and (b) show two different techniques of supply modulation of the LA. In Figure. 2.4(a) an individual modulator is used to modulate the supply voltage of the LA according to envelope level. For this purpose usually low pass filtered envelope signal can be used. In Figure. 2.4(b) a number of discrete supply voltages are used to be supply the LA according to envelope level.

3) Multilevel switching is another technique to further improve the ripple and efficiency of the switching regulators [21–24]. In this technique, according to envelope level, the proper supply voltage level is chosen for the switching regulator to reduce the ripple and adjust the slew-rate of the switching current. So, the current provided from the linear amplifier also decreases and overall efficiency improves. Multiple switching regulators with different supply voltages is required to implement the regulator. This technique is shown in Figure. 2.4(c). However, the board and chip area increase.

Three level switching regulators provide three level of switching voltage instead of two, which reduces inductor current ripple with two times. This can facilitate wider band switching regulators with higher efficiency.

4) Multiphase Switching (multiple switching stages): As mentioned earlier, the low

efficiency of the linear amplifier leads to low overall efficiency. However, as the signal bandwidth increases, the burden on the linear amplifier increases correspondingly. In order to relax linear amplifier burden, multiple switching stages have been reported that utilizes two [25] or more switching stages. Figure. 2.4(d) shows a dual-phase switching stage in hybrid structure.

Usually the switching stages classify as: 1) slow switching stages, which is the same as switching stage in conventional hybrid structure; 2) fast switching stages which is switching at higher frequency with wider bandwidth to help the linear amplifier in providing high frequency current.

5) Efficiency Improved Linear amplifiers: By increasing wideband signal application with high PAPR, the slew-rate of the signal also increases. Thus, the linear amplifier not only should have sufficient low-frequency gain and wide bandwidth, but also high slew rate and large drive capability to effectively track the large PAPR envelope signal, maintain a good linearity, and drive the low equivalent PA resistance. In order to have high slew-rate linear amplifiers, the efficiency degrades even more because high DC bias current is required. However, checking the slew-rate histogram of the signals with different modulation, Figure. 2.5, shows that the high slew-rate is only required in a very low-percentage of the signal time. Thus, design of the linear amplifier for high slew-rate is overdesign that kills the efficiency. Thus, slew-rate enhanced linear amplifiers have been reported that increases the slew rate only when then signal slew-rate is high and other times it is operating with lower bias current.

[18] employs signal level tracking adaptive biasing and gain enhanced current mirror operational transconductance amplifier (OTA), in parallel with a buck switching amplifier. [26] uses current reuse technique in the linear amplifier design to improve gain-bandwidth of the linear amplifier without increasing current consumption.

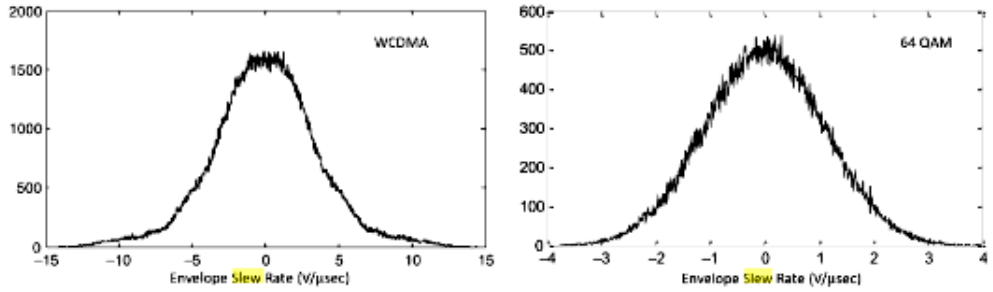

Figure 9-36 Slew rate histograms for WCDMA and 64 QAM signals of similar bandwidth and with identical Nyquist bandlimiting filters. The uniform constellation point spacing of the QAM signal keeps the slew rate span down compared to the nonuniform constellation used in this WCDMA signal.

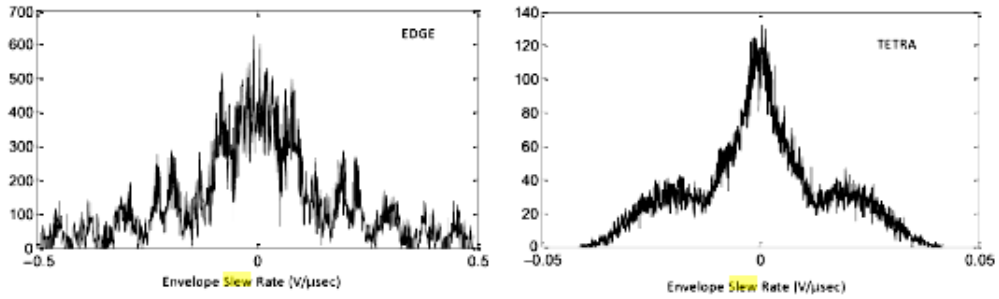

Figure 9-37 Slew rate histograms for EDGE and TETRA signals. Both of these have slow slew rates due to both their narrow occupied bandwidths and from their non zero-crossing envelopes.

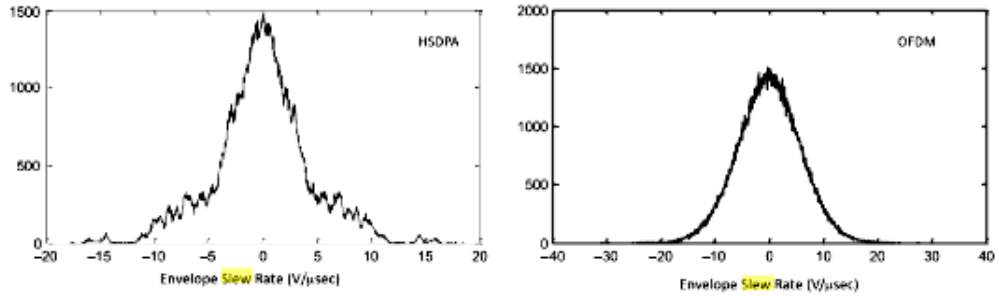

Figure 9-38 Slew rate histograms for HSDPA (uplink) and OFDM signals with similar occupied bandwidth. These signals have the widest range of slew rates, primarily due to a very nonuniform constellation for the HSDPA signal and to the large number of zero crossings in the OFDM signal.

Figure 2.5: Slew-Rate Histogram of Different Signals with Different Digital Modulations.

2.2 Summary

To Summarize what is discussed in this chapter we have:

AC-coupled LAs can improve the efficiency by eliminating DC current share from the LA, and decoupling output envelope level from the LA supply voltage [20, 22, 27–30]. However, at higher frequencies, majority of the output AC-current is drawn from the LA which degrades the efficiency. Furthermore, this approach requires large off-chip AC-coupling capacitor. Another approach uses a dedicated buck/buck-boost converter to modulate the LA supply [20, 22, 27], [17, 29–33] and switching regulator supply [22, 29, 32] to improve the system efficiency. However, additional off-chip large inductors for the supply regulators are required.

Dual switching has been proposed to reduce the inductor current ripple and the LA current [25, 34, 35]. Multilevel buck regulator can be used to replace the LA [36, 37] however this topology has a limited modulator bandwidth. Multilevel switching converters are also used to track the slew-rate of the switching stage current with the load current and reduce the LA current. However, the proposed methods are complex as they require multiple supply voltages, multiple feedback loops within the regulator with synchronization among the loops, and increased area [24].

Another approach tracks and controls the LA average current instead of the ripple current for efficiency optimization, but the tracking bandwidth is limited to 10MHz [19].

Three-level switching converter (3L-SWC) with single supply voltage has been used, reducing the switching current ripple amplitude by at least 50% compared to conventional two-level (2L) converters. To achieve a fast response and small inductance value, three-level converters are used in [38–40].

Typical control method used in 3L-SWCs is pulse width modulation (PWM) [28,

36, 39–42]. However the PWM control for ET modulators faces several challenges. Firstly, the loop-bandwidth is only a fraction of switching frequency [8], therefore the converter suffers from high switching losses to achieve wideband output current. Feed-forward paths are used to compensate the low speed switching loop [34, 43], at the cost of increased complexity in the control loop. Second, for loop stabilization, a compensation circuit is required, which reduces the overall bandwidth. The challenges of PWM control loop has extra limitations associated with 3L-SWCs. In PWM-controlled 3L-SWCs, accurate 180-degree phase shifted synchronization signals are required to control two pairs of power switches, which require accurate timing signal generators. Moreover, in 3L-SWCs, the flying capacitor voltage (V_{CF}) should be regulated to a certain value to prevent loop instability and damages to the thin gate-oxide transistors. However, process, voltage, temperature (PVT) variations, device mismatch, control signal duty-cycle error, and device parasitics can cause deviation of the V_{CF} from its desired value [44, 45]. Therefore, an additional calibration loop is required in PWM controlled 3L-SWCs [39]. This further increases the complexity of the control loop design.

In hybrid ET modulators, the system bandwidth and output ripple magnitude strongly depend on the LA bandwidth and DC-gain. Increasing unity-gain bandwidth of the LA requires large current consumption. Using dual-path crossover current-reuse mechanism enhances the gain of the LA [26]. Also, a wide-bandwidth buffered-switching class-AB linear amplifier is presented in [46]. However, LA with high unity-gain bandwidth is not enough to track the high-power and wideband signal accurately, since high slew-rate modulator is also required to drive large load of the PA supply. High slew-rate LAs consume even more biasing current, which degrades the overall efficiency. Adaptive biasing is utilized to improve DC-gain and slew-rate without increasing quiescent bias current in [18]. Also, source cross-coupled class-AB amplifier

at the first stage of the LA lowers DC biasing and improves the slew-rate [17]. These techniques enhance slew-rate by increasing input stage current during slewing, thus the current needs to be transferred to the last stage to charge or discharge parasitic capacitors and reduce tracking error.

In this work, a three-level switching converter with a hysteresis control loop is proposed, benefiting low-ripple and low-loss properties of three-level converters while resolving challenges associated with PWM-controlled loops. The architecture proposes a concurrent flying capacitor voltage V_{CF} regulation. Employing the proposed hysteresis-controlled 3L-SWC results in a high-speed control loop; eliminates flying capacitor C_F calibration loop; reduces high-frequency current percentage provided by the LA; and achieves a high efficiency modulator. In addition, the LA operating in parallel with the SWC uses slew rate enhancement (SRE) to improve the slew-rate of the LA and the modulator. The SRE circuit directly injects current to the last stage capacitors, without increasing input tail current, to bypass previous stages delay; avoid disturbing their operating point and degrading the LA DC-gain and gain-bandwidth (GBW).

Chapter 3

PROPOSED SUPPLY MODULATOR DESIGN

Three-level switching converter (3L-SWC) with single supply voltage has been used, reducing the switching current ripple amplitude by at least 50% compared to conventional two-level (2L) converters. To achieve a fast response and small inductance value, three-level converters are used in [38–40].

Typical control method used in 3L-SWCs is pulse width modulation (PWM) [28, 36, 39–42]. However the PWM control for ET modulators faces several challenges. Firstly, the loop-bandwidth is only a fraction of switching frequency [8], therefore the converter suffers from high switching losses to achieve wideband output current. Feed-forward paths are used to compensate the low speed switching loop [34, 43], at the cost of increased complexity in the control loop. Second, for loop stabilization, a compensation circuit is required, which reduces the overall bandwidth. The challenges of PWM control loop has extra limitations associated with 3L-SWCs. In PWM-controlled 3L-SWCs, accurate 180-degree phase shifted synchronization signals are required to control two pairs of power switches, which require accurate timing signal generators. Moreover, in 3L-SWCs, the flying capacitor voltage (V_{CF}) should be regulated to a certain value to prevent loop instability and damages to the thin gate-oxide transistors. However, process, voltage, temperature (PVT) variations, device mismatch, control signal duty-cycle error, and device parasitics can cause deviation of the V_{CF} from its desired value [44, 45]. Therefore, an additional calibration loop is required in PWM controlled 3L-SWCs [39]. This further increases the complexity of the control loop design.

In hybrid ET modulators, the system bandwidth and output ripple magnitude

strongly depend on the LA bandwidth and DC-gain. Increasing unity-gain bandwidth of the LA requires large current consumption. Using dual-path crossover current-reuse mechanism enhances the gain of the LA [26]. Also, a wide-bandwidth buffered-switching class-AB linear amplifier is presented in [46]. However, LA with high unity-gain bandwidth is not enough to track the high-power and wideband signal accurately, since high slew-rate modulator is also required to drive large load of the PA supply. High slew-rate LAs consume even more biasing current, which degrades the overall efficiency. Adaptive biasing is utilized to improve DC-gain and slew-rate without increasing quiescent bias current in [18]. Also, source cross-coupled class-AB amplifier at the first stage of the LA lowers DC biasing and improves the slew-rate [17]. These techniques enhance slew-rate by increasing input stage current during slewing, thus the current needs to be transferred to the last stage to charge or discharge parasitic capacitors and reduce tracking error.

In this work, a three-level switching converter with a hysteresis control loop is proposed, benefiting low-ripple and low-loss properties of three-level converters while resolving challenges associated with PWM-controlled loops. The architecture proposes a concurrent flying capacitor voltage V_{CF} regulation. Employing the proposed hysteresis-controlled 3L-SWC results in a high-speed control loop; eliminates flying capacitor C_F calibration loop; reduces high-frequency current percentage provided by the LA; and achieves a high efficiency modulator. In addition, the LA operating in parallel with the SWC uses slew rate enhancement (SRE) to improve the slew-rate of the LA and the modulator. The SRE circuit directly injects current to the last stage capacitors, without increasing input tail current, to bypass previous stages delay; avoid disturbing their operating point and degrading the LA DC-gain and gain-bandwidth (GBW).

The proposed envelope tracking modulator is shown in Figure. 3.1, and consists

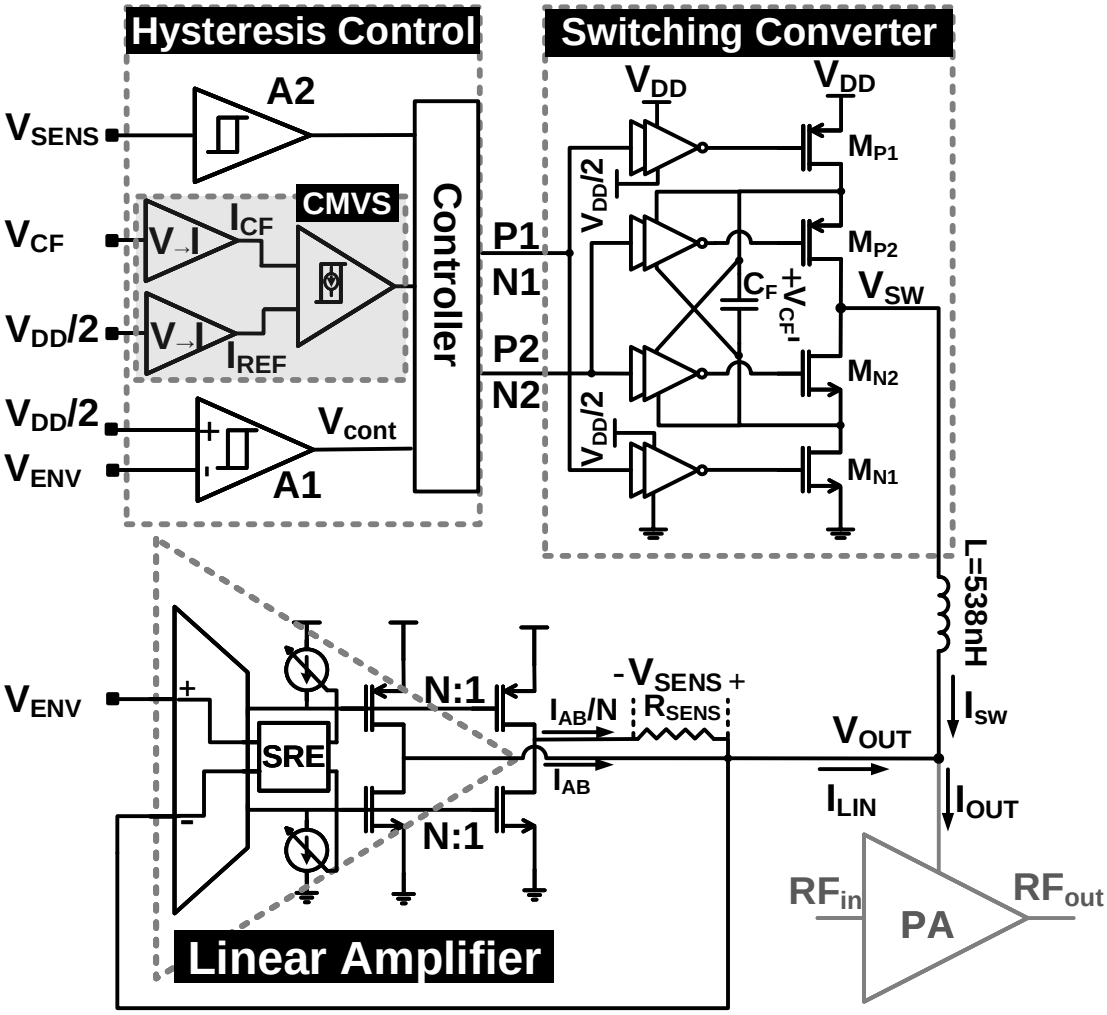

Figure 3.1: Block Diagram of the Proposed Envelope Tracking Modulator.

of three main building blocks: 1) three-level switching converter, 2) hysteresis control loop and 3) slew-rate enhanced linear amplifier [47]. Design challenges and considerations of major blocks are discussed in this section. In this work the fundamental design goal is to minimize losses and ripple, while meeting the wideband requirement

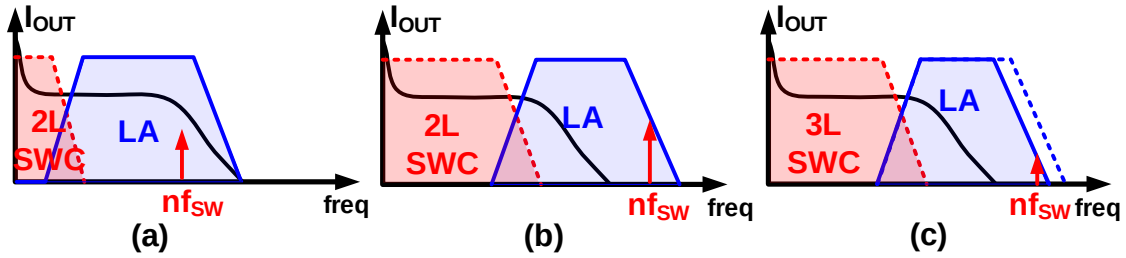

Figure 3.2: Current Share of the SWC and LA for (a) Low Switching Frequency 2L-SWC, (b) High Switching Frequency 2L-SWC, (c) High Switching Frequency 3L-SWC.

such as LTE-80MHz envelope.

3.1 System Level Design

3.1.1 Switching Regulator

In the hybrid ET modulators, the LA provides a greater share of the high-frequency content of the output current as shown in Figure. 3.2(a), and is a limiting factor in overall system efficiency. To compensate for this, an efficient wideband switching converter is required to lower the LA high-frequency current share. Wideband, high-frequency SWCs faces two challenges: high switching frequency increases the switching losses, and the high frequency ripple content of output current generated by the switching converter needs a wideband LA for ripple cancellation. This feature is shown in Figure. 3.2(b), where the SWC operates at wider frequency range, and the LA compensates for the high frequency operation and also the switching current ripple harmonics, indicated as nf_{SW} in the figure. Technique such as resonance frequency tuning scheme [27], is used to reduce the ripple by canceling parasitic capacitor of the inductor in the SWC, where a capacitor bank with fine tuning option is needed.

One method to increase the switching converter bandwidth while maintaining lower losses and lower ripple is using three-level switching converter. In 3L-SWCs,

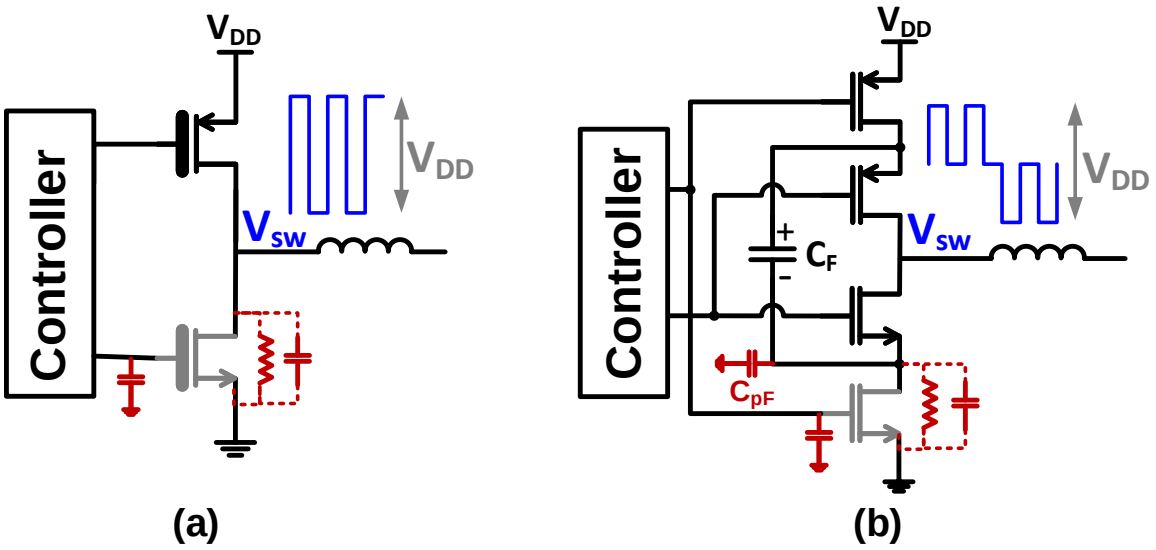

Figure 3.3: (a) 2L-SWC and, (b) 3L-SWC, with a Model of Parasitics of a Single Switch and C_F.

the voltage across each device is half of a typical two-level switching converter (2L-SWC) with the same supply voltage, enabling use of thin gate-oxide transistors with lower parasitics and reduced losses. Figure. 3.3 shows a 2L-SWC with thick gate-oxide devices and a 3L-SWC made of thin gate-oxide devices, where parasitics model of one device is also shown. As the switching node voltage V_{SW} is reduced by half, the ripple of output current reduces by at least 50%. Figure. 3.2(c) shows that due to smaller ripple, LA gain-bandwidth requirements are relaxed compared to 2L-SWC.

Switching loss of a three-level switching converter P_{SW3L} relative to switching loss of a two-level switching converter P_{SW2L}, with the same supply voltage is expressed as,

$$\frac{P_{SW3L}}{P_{SW2L}} = \frac{4 \times \frac{1}{2} C_{P3L} {V_{SW3L}}^2 f_{SW3L} + C_{pF} {V_{SW3L}}^2 f_{SW3L}}{2 \times \frac{1}{2} C_{P2L} {V_{SW2L}}^2 f_{SW2L}} \tag{3.1}$$

where, C_{P3L} and C_{P2L} are the parasitic capacitors of thin gate-oxide transistors in 3L-SWC and thick gate-oxide transistors in 2L-SWC, respectively, while the assumption is that, in each topology, all the devices have identical parasitics values. V_{SW3L} is

switching voltage and f_{SW3L} is switching frequency of parasitic capacitor in 3L-SWC, while V_{SW2L} and f_{SW2L} are corresponding parameters in 2L-SWC. The factors 4 in the numerator and 2 in the denominator represents the number of devices in each topology. The contribution of bottom-plate parasitic capacitor of the flying capacitor C_{pF} to the switching loss is also included in (3.1) as given in [44]. Compared to 2L-SWC with the same switching frequency, 3L-SWC with thin gate-oxide transistors has smaller parasitics and V_{SW3L} is half of V_{SW2L}. Given that C_{pF} is related to C_F by the factor of ρ, (3.1) can be rewritten as:

$$\frac{P_{SW3L}}{P_{SW2L}} = \frac{2C_{P3L} + \rho C_F}{4C_{P2L}}. \tag{3.2}$$

Therefore, flying capacitor C_F can be appropriately sized to minimize the switching loss of a 3L-SWC compared to 2L-SWC.

In addition to switching loss, the conduction and ripple losses of the converter due to on-resistance R_{ON} of the power devices should be considered [38]. The ratio of the total conduction and ripple losses of the 3L-SWC to 2L-SWC can be calculated as,

$$\frac{P_{Cond3L}}{P_{Cond2L}} = \frac{2 \times R_{ON3L} \times {I_{L3L}}^2 (1 + \frac{{\Delta I_{3L}}^2}{12 {I_{L3L}}^2})}{R_{ON2L} \times {I_{L2L}}^2 (1 + \frac{{\Delta I_{2L}}^2}{12 {I_{L2L}}^2})} \tag{3.3}$$

where, R_{ON3L} is on-resistance of the each device in the 3L-SWC, assuming that switches are identical; and R_{ON2L} is corresponding parameters in 2L-SWC. I_{L3L} and I_{L2L} are the average inductor currents in 3L and 2L SWCs. ΔI_{3L} and ΔI_{2L} are the ripple currents of the inductors in 3L and 2L SWCs, respectively. Since, the inductor current ripple in 3L-SWC is at least two times smaller than in 2L-SWC, (3.3) and assuming that average inductor current is the same in two cases and equal to I_L, the expression in (3.3) reduces to,

$$\frac{P_{Cond3L}}{P_{Cond2L}} = \frac{2 \times R_{ON3L}}{R_{ON2L}} \frac{1 + \frac{{\Delta I_{3L}}^2}{12 {I_L}^2}}{1 + 4 \times \frac{{\Delta I_{3L}}^2}{12 {I_L}^2}}. \tag{3.4}$$

According to (3.4), depending on the on-resistances and the ripple current magnitudes, P_{Cond3L}/P_{Cond2L} can be less than one, while in the worst case when inductor current ripple is small, this ratio will be $2R_{ON3L}/R_{ON2L}$. Therefore, in order to have equal conduction loss in 3L and 2L SWCs, the on-resistance of each device in 3L-SWC should be half of the 2L-SWC devices.

Thus, 3L-SWCs with small current ripple and less switching losses are a good choice for wideband applications. For this purpose, a high-speed and wideband control loop is required to dynamically control and adjust the switching converter current according to input envelope level, output current and the LA current.

3.1.2 Control Loop

As discussed in previous section, 3L-SWCs show promising properties for low-loss and wideband applications. However they require a synchronized PWM control method for their switch timing and a separate V_{CF} calibration method. PWM control requires a compensation circuit, which reduces the bandwidth of the converter, making 3L-SWC less suitable for wideband ET applications.

A hysteresis control loop can address the PWM control challenges and yield better results. In this work, a hysteresis control loop is proposed for the 3L-SWC. The advantages of this method are: 1) The hysteresis loop is inherently stable across a wide load range and does not require compensation circuit. Thus, by simplifying loop design, higher speed loop and wider bandwidth converter can be achieved. 2) The loop bandwidth in hysteresis control is as high as switching frequency, therefore the converter does not contribute to higher switching losses. 3) No synchronization signal is required, despite PWM control loop where the timing accuracy of the synchronization signals is a limiting factor in increasing the switching frequency. 4) The flying capacitor voltage V_{CF} is sensed and regulated in the main control loop on every

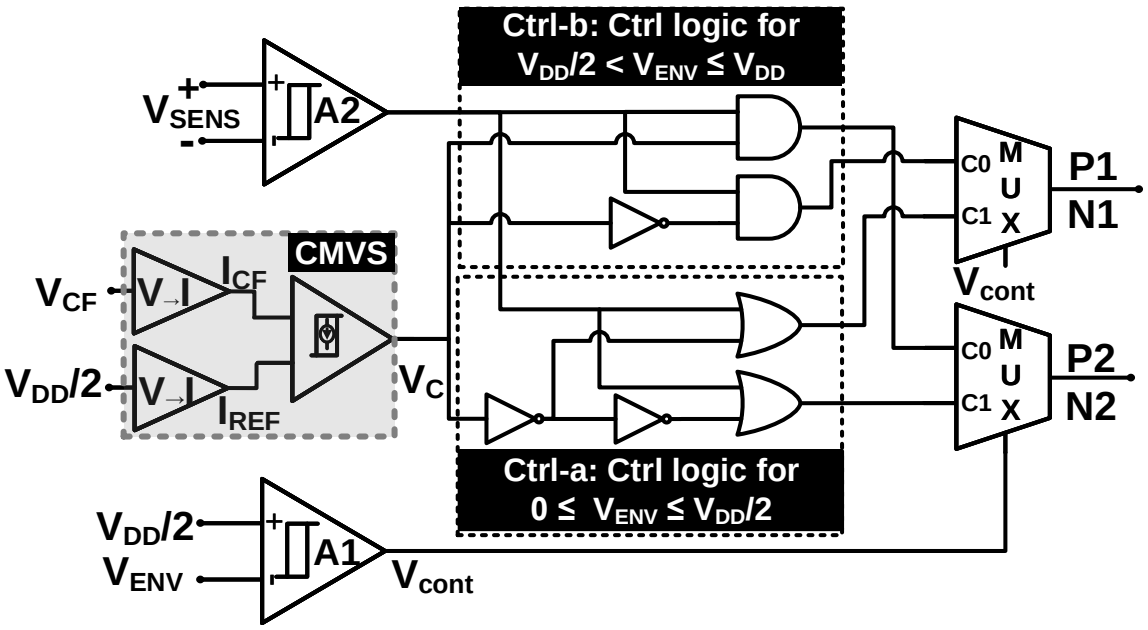

Figure 3.4: Proposed Hysteresis Controller.

cycle. Therefore, the requirement for an extra calibration loop is eliminated in this proposed technique, and the controller ensures $V_{DD}/2$ voltage across the switches to prevent over-stressing thin-gate transistors. With the above mentioned properties, over 80MHz switching frequency and loop bandwidth is achievable.

The proposed hysteresis control architecture is shown in Figure. 3.4. The inputs of the controller are V_{CF}, input envelope voltage $\mathrm{V_{ENV}}$ and $\mathrm{V_{SENS}}$. A sense resistor $\mathrm{R_{SENS}}$ (Fig. 3.1) connected between output node V_{OUT} and the sensing stage, with current scaled down to $1/N^{th}$ of class-AB output stage, generates $\mathrm{V_{SENS}}$, thus the $\mathrm{R_{SENS}}$ loss is removed from the main path of LA current $\mathrm{I_{LIN}}$ [18].

In a 3LSWC, the switching node voltage V_{SW} switches between three levels: 0, $V_{DD}/2$, and V_{DD}. Therefore, the control method is divided down into two regions based on input envelope signal level $\mathrm{V_{ENV}}$. If $\mathrm{V_{ENV}}$ is less than $V_{DD}/2$, by selecting the Ctrl-a path in the Figure. 3.4, the switching node voltage V_{SW} switches between 0 and $V_{DD}/2$. For $\mathrm{V_{ENV}}$ larger than $V_{DD}/2$, the Ctrl-b path is selected and the V_{SW} switches between $V_{DD}/2$ and V_{DD}. In addition, the controller monitors the flying

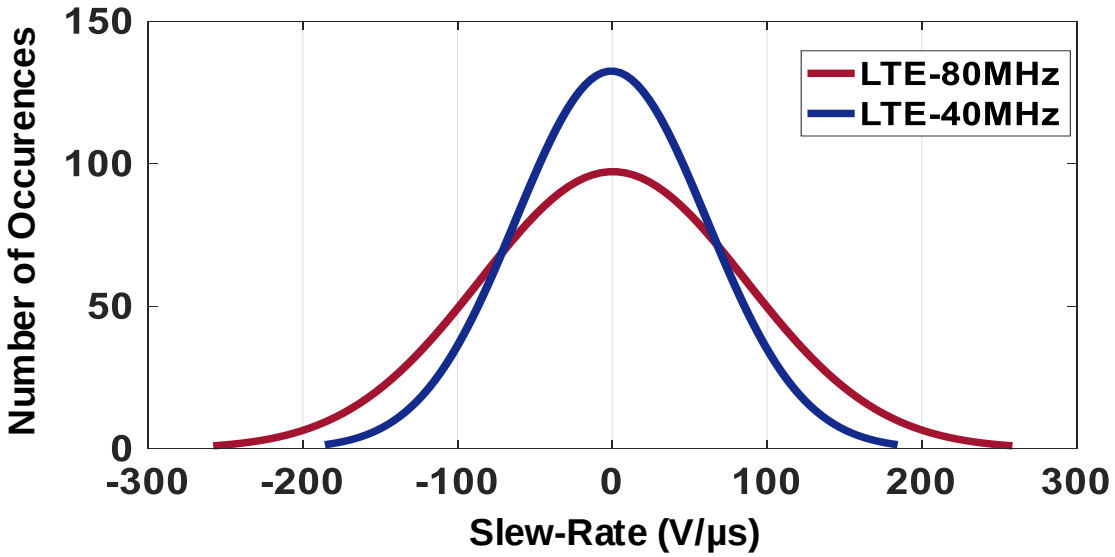

Figure 3.5: Histogram of QPSK LTE-80MHz and LTE-40MHz Envelope Signal.

capacitor voltage V_{CF} using a current-mode voltage sensor (CMVS) and regulates to the desired value of $V_{DD}/2$ in every cycle. For this purpose, in any of the control paths, in order to set the V_{SW} to $V_{DD}/2$, the controller can choose a charging path or discharging path for the C_F. Thus, based on the sensed V_{CF}, if $V_{CF}<V_{DD}/2$ the charging path will be chosen to enhance the V_{CF} to desired value. For $V_{CF}>V_{DD}/2$ by choosing the discharging path, $V_{DD}/2$ can be maintained across the C_F.

3.1.3 Linear Amplifier

In hybrid ET modulators, DC-gain and bandwidth of the LA affects the system bandwidth and ripple. Also, high slew-rate modulator is required to provide current to the large load of the PA supply. The slew-rate histogram of a quadrature phase shift keying (QPSK) LTE-80MHz and LTE-40MHz envelope signals with 2.4V peak-to-peak voltage, and respectively 7.84dB and 8.06dB PAPR are shown in Figure. 3.5. As it is shown, the slew-rate can be as high as $\pm 300V/\mu s$, thus a LA with high DC current is required. However, due to high density of slew-rate histogram below

$\pm 100V/\mu$s range, biasing the amplifier for maximum slew-rate is unnecessary and will degrade efficiency dramatically. Instead, utilizing SRE technique to improve only at high-slew-rate inputs can save DC quiescent bias current [48, 49].

In the proposed technique, the SRE circuit is in parallel with the main amplifier and only contributes required current when there is an error signal between input and output signals. By directly sourcing or sinking current to the large parasitic capacitors of the final class-AB stage, the SRE circuit does not affect the operation point of the rest of the LA, and the phase delay associated with the middle stage does not contribute to the phase margin of the SRE. Figure. 3.6 shows the conceptual architecture of the typical technique, where SRE enhances by increasing input stage current during slewing, and the proposed technique. The transfer function of the slewing error can be given as,

$$TF_{SRE} = k_{SRE} \frac{1}{1 + \frac{s}{P_1}} \frac{1}{1 + \frac{s}{P_2}} \tag{3.5}$$

where, k_{SRE} is the large signal gain from input to the output and P_1 is the first stage equivalent pole for both conventional and proposed SRE architectures. P_2 stands for the middle gain stage equivalent pole and the SRE parallel path equivalent pole, in the conventional structure and the proposed architecture, respectively. The middle stage transistors need to have large aspect ratios to provide headroom in the signal path. However, the SRE circuit is not in the main signal path and can be designed with small size devices to minimize phase delay.

The designed LA operates in unity-gain feedback mode with both PMOS and NMOS input pairs. Unity-gain feedback removes the extra pole in the feedback-path of a non-unity-gain configuration as used in [18, 28] resulting in a wider loop bandwidth and better transient response.

In rail-to-rail input range amplifiers with both PMOS and NMOS input pairs,

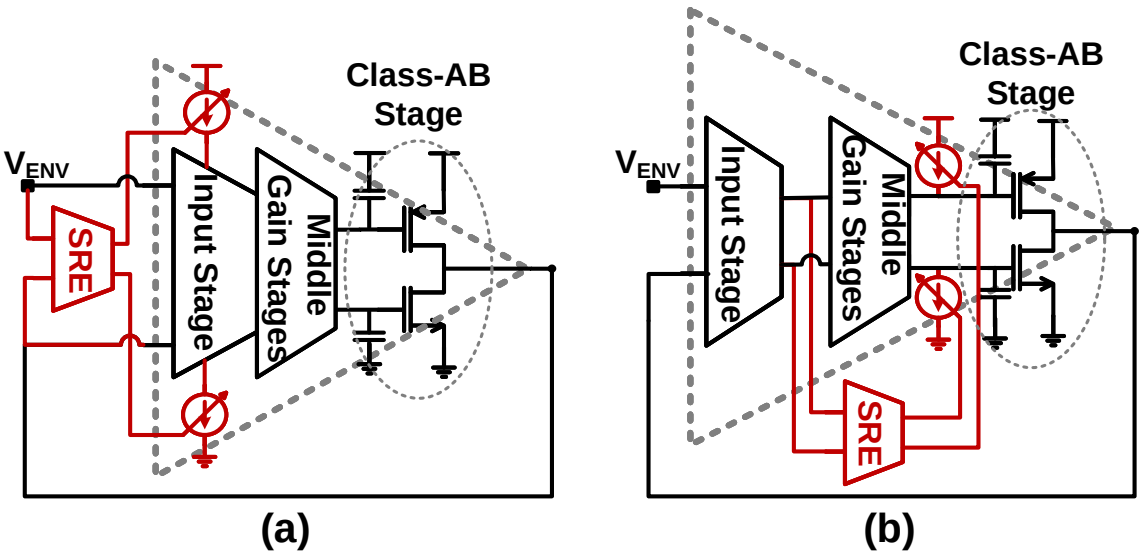

Figure 3.6: (a) Conventional SRE Technique, (b)Proposed SRE Technique.

depending on the input common mode (CM) level, the input transconductance (gm) changes and the gain and stability of the LA are input CM dependent. In the proposed structure this problem is resolved by using maximum current selection (MCS) circuit. The MCS circuit selects the larger current of the input pairs and transfers to the next stage, independent of the input common mode level. Thus, it makes input stage transconductance constant over the input CM variation, and stabilizes the quiescent current of output class-AB stage. This approach removes input common-mode dependent stability problems, and ensures push-pull operation at the class-AB output stage with a rail-to-rail input operation.

A LA with rail-to-rail input stage, rail-to-rail push-pull class-AB output stage and slew-rate enhancement circuit with block diagram as shown in Figure. 3.7 is designed. The details of the design are given in the next sections.

3.2 Circuit Level Design

This section describes the circuit level implementation of main building blocks of the modulator.

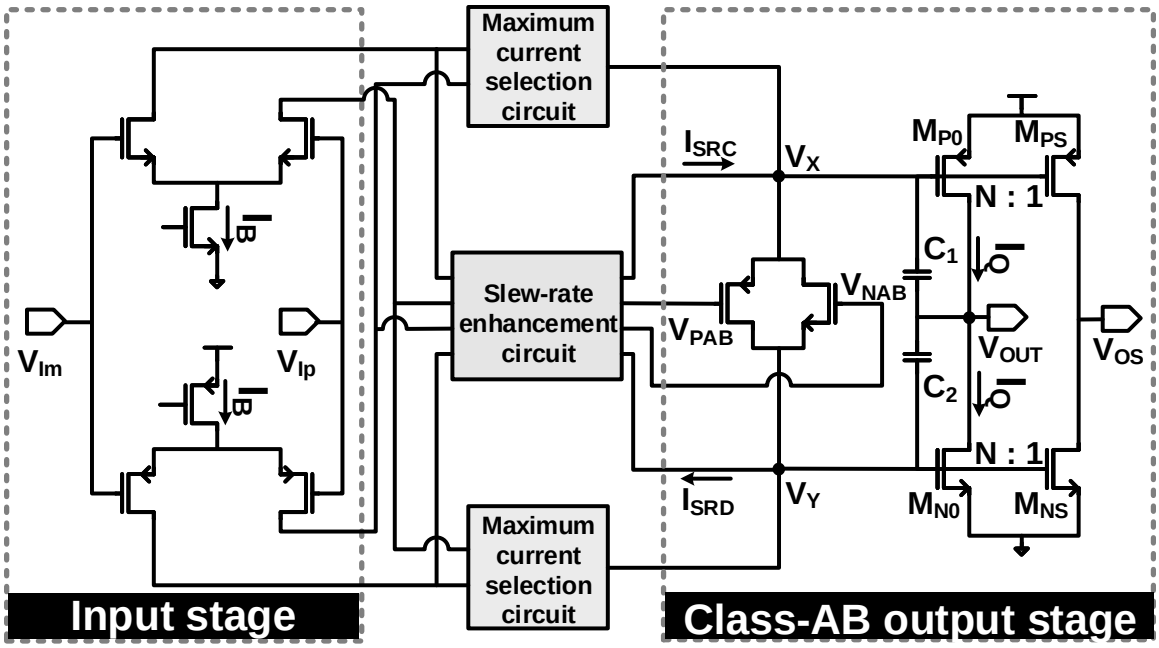

Figure 3.7: Linear Amplifier Conceptual Block Diagram.

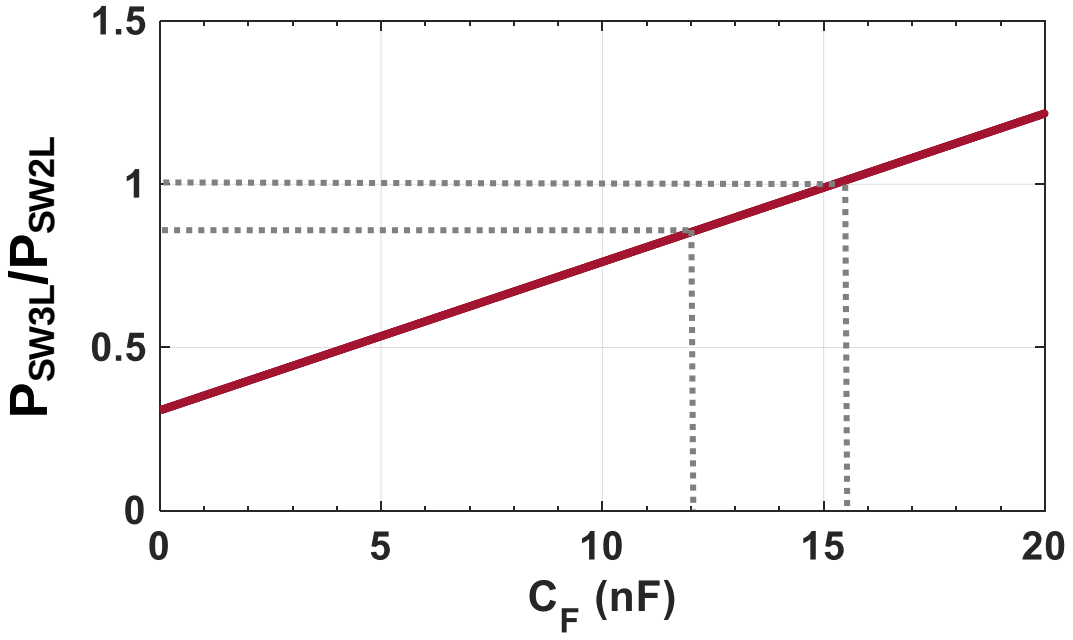

Figure 3.8: Switching Loss of the 3L-SWC Compared to 2L-SWC Versus C_F Value.

3.2.1 Three-level Switching Converter

As mentioned in Section II. A, 3L-SWCs require optimum sizing of the power transistors and flying capacitor in order to achieve low switching losses. In the 65nm

CMOS technology used in this work, with the same total R_{ON} in the switching current path, the parasitic capacitor of a thin-gate transistor is two times smaller than a thick-gate transistor. However, according to (3.2) the bottom plate capacitor of the flying capacitor contributes to the losses as well. In order to optimize the design for this purpose, the P_{SW3L}/P_{SW2L} versus C_F is plotted in Figure. 3.8. In this work, an NMOS-capacitor in deep-nwell is chosen for flying capacitor, due to its higher capacitor density, where parasitic deep-nwell-to-substrate bottom plate capacitor C_{pF} is 0.8% of the C_F. Therefore, this plot sets the maximum size of the C_F to ensure that the P_{SW3L} is smaller than the P_{SW2L} for C_F less than 15.2nF. On the other hand, a smaller capacitor has smaller time constant and voltage across it will have larger variation in every switching cycle. Thus, the minimum size of the C_F, C_{Fmin} is limited by the maximum allowed switching frequency. In this work, in order to achieve flying capacitor voltage variation ΔV_{CF} of 250mV ($\pm$125mV), set by the thin-gate transistors tolerance voltage, with maximum switching frequency f_{SW} of 100MHz, where charging or discharging duration of the C_F is $1/2f_{SW}$, and the maximum current is passing through the C_F (I_{CFmax}), C_{Fmin} can be calculated as,

$$C_{Fmin} = \frac{I_{CFmax}\Delta t}{\Delta V_{CF}} = \frac{V_{DD}}{R_L}\frac{1}{2f_{SW}}\frac{1}{\Delta V_{CF}} \tag{3.6}$$

where, V_{DD} is the supply voltage at 2.4V, and R_L is the equivalent load resistor of the modulator which is 4.7Ω in this design. C_{Fmin} of 10.6nH is calculated, and C_F of 12nF is chosen to achieve small V_{CF} variation during each cycle, and losses are 0.85 of the P_{SW2L}.

3.2.2 Hysteresis Controller

The proposed hysteresis control system is shown in Figure. 3.4. Here, the operation and timing diagram of the hysteresis controller and three-level switching converter for

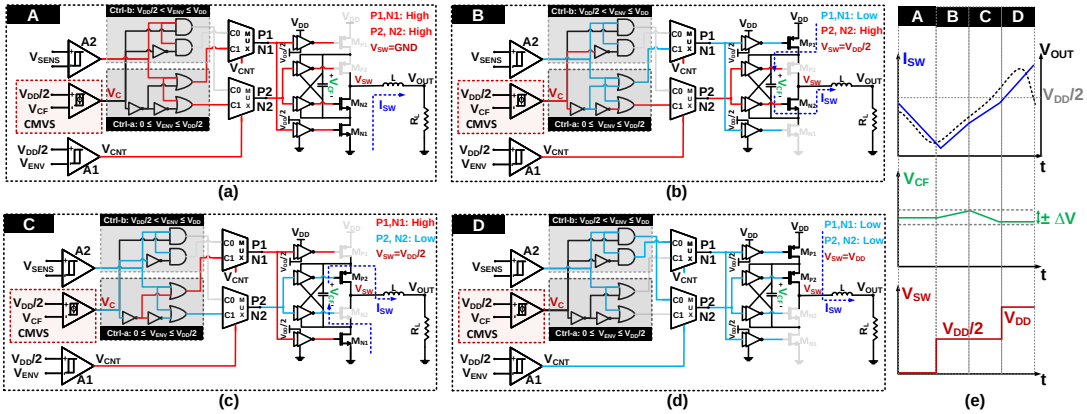

Figure 3.9: Operation of the Hysteresis-Controlled 3L-SWC for: (a) $V_{ENV} < V_{DD}/2$ and $V_{SENS} > +V_{HYS}$, (b) $V_{ENV} < V_{DD}/2$, $V_{SENS} < -V_{HYS}$ and $V_{CF} < V_{DD}/2$, (c) $V_{ENV} < V_{DD}/2$, $V_{SENS} < -V_{HYS}$ and $V_{CF} > V_{DD}/2$, (d) $V_{ENV} > V_{DD}/2$ and $V_{SENS} < -V_{HYS}$ (e)Transient Response of the Hysteresis-Controlled 3L-SWC. (Blue Lines: Logic-Low, Red Lines: Logic-High)

an example input signal is shown in Figure. 3.9. Its operation is explained as follows.

$0 < V_{ENV} < V_{DD}/2$: Ctrl-a

When the sinking linear amplifier current I_{LIN} increases, the voltage V_{SENS} across the sense resistor R_{SENS} in Figure. 3.1, passes the hysteresis window $+V_{HYS}$ of the comparator A2, it sets signals N1, P1 and N2, P2 to logic-high, turning M_{N1}, M_{N2} on and M_{P1}, M_{P2} off, and decreasing I_{SW} and I_{LIN}, as indicated in Figure. 3.9(a). The V_{CF} remains unchanged. When the sourcing current I_{LIN} makes V_{SENS} to cross $-V_{HYS}$, A2 output is logic-low and V_C, which is the comparison result of V_{CF} with $V_{DD}/2$, becomes the dominant control signal. If V_{CF} drops from $V_{DD}/2$, the N1, P1 is logic-low and N2, P2 is logic-high, turning M_{N2}, M_{P1} on to charge the C_F (Fig. 3.9(b)). Conversely, for V_{CF} more than $V_{DD}/2$, M_{N1} and M_{P2} are turned on as indicated in Figure. 3.9(c), to discharge the C_F and maintain desired voltage value for V_{CF}. Choosing either of these options, switching node voltage V_{SW} is set to $V_{DD}/2$ to increase I_{SW}. Thus, the V_{SW} switches between 0V (ground voltage) and $V_{DD}/2$.

$V_{DD}/2 < \mathbf{V_{ENV}} < V_{DD}$: Ctrl-b

When sourcing current I_{LIN} increases, the A2 output will turn logic-low, turning on M_{P1} and M_{P2}, setting V_{SW} to V_{DD} as indicated in Figure. 3.9(d). This ensures that more load current is supplied by SWC, which results in decreased current from LA. In the sinking mode of the linear amplifier, to decrease output current of the SWC and limit sinking current of the LA, V_{SW} should be set to $V_{DD}/2$. Similar to Ctrl-a path, according to V_{CF}, either charging or discharging path for C_F will be chosen. The implementation of the control circuit is highlighted as Ctrl-b in Figure. 3.4.

Implemented with simple logic circuits and comparators, the control loop can handle high switching frequency with a small delay. Utilizing this control method, it is ensured that desired range of V_{CF} is attained in each cycle.

As mentioned, in the proposed hysteresis loop, the flying capacitor voltage V_{CF} is being sensed and regulated on every switching cycle. In order to have a high-speed V_{CF} regulation loop, a high-speed voltage sensor is also required. Therefore, a fast current-mode voltage sensor is developed. Given the voltage variance ΔV set by the thin-gate transistors tolerance voltage, the objective is to ensure that V_{CF} is in the desired range of $V_{DD}/2 \pm \Delta V$. The proposed current-mode voltage sensor circuit shown in Figure. 3.10, converts V_{CF} to a proportional current I_{CF} using a diode connected transistor and a resistor R. Similarly, two reference currents $I_{REF}/2 \pm \Delta I$ proportional to $V_{DD}/2 \pm \Delta V$ are generated from $V_{DD}/2$ and mirrored into a comparison stage with I_{CF}. In the current mode, comparing I_{CF} with $I_{REF}/2 \pm \Delta I$ triggers proper set or reset signal for an RS latch to produce the control signal V_C for the hysteresis controller to regulate V_{CF}. To assess a high-speed loop as well as low power to prevent discharging of V_{CF}, I_{CF} of $20\mu A$ is chosen.

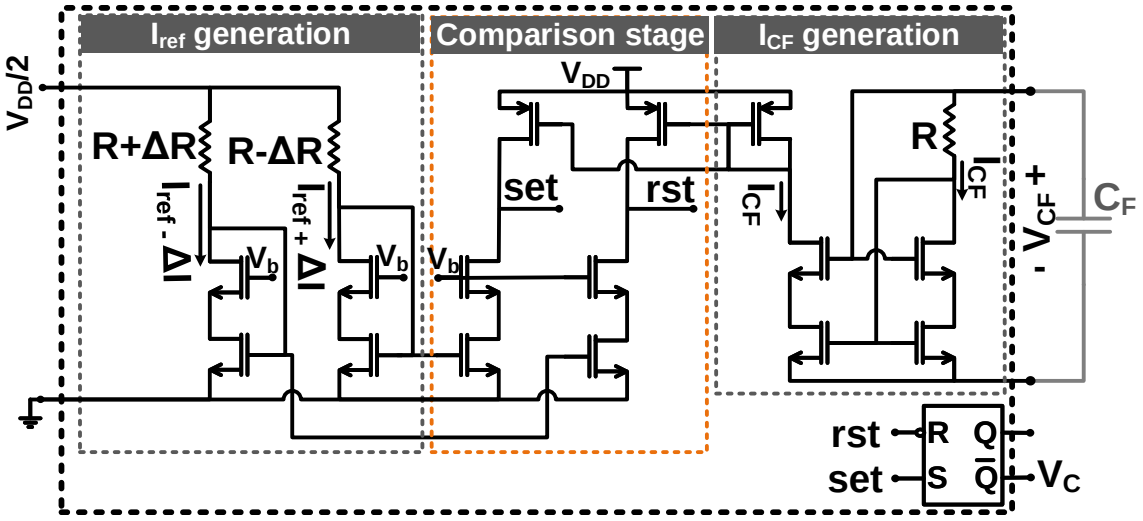

Figure 3.10: Current-Mode Voltage Sensor (CMVS) Circuit of the C_F.

3.2.3 Linear Amplifier Design

The LA design with rail-to-rail input and output operation range, input maximum current selection for stabilized GBW over input CM range, and SRE to obtain high slew-rate and bandwidth without extra power consumption is explained in this section.

Maximum Current Selection Circuit

The MCS circuit shown in Figure. 3.11 compares the NMOS and PMOS input pairs currents, selects the maximum of them and transfers to the output, independent of the input common mode range. This stabilizes the gain-bandwidth and class-AB bias current; and ensures push-pull operation over the CM range.

For high input common-mode level when only NMOS differential pair is on, and PMOS differential pair turns off, M_{N3-6} and M_{N9} are off. So, IN_{MCS} which is $1/K1 \times I_B/2$ flows through diode connected M_{N7} and mirrors to M_{N8}. Hence, last stage current will be $K2/K1 \times I_B/2$. On the other hand, IP_{MCS}, which is mirrored from PMOS differential pair input stage is negligible and there is no current flow

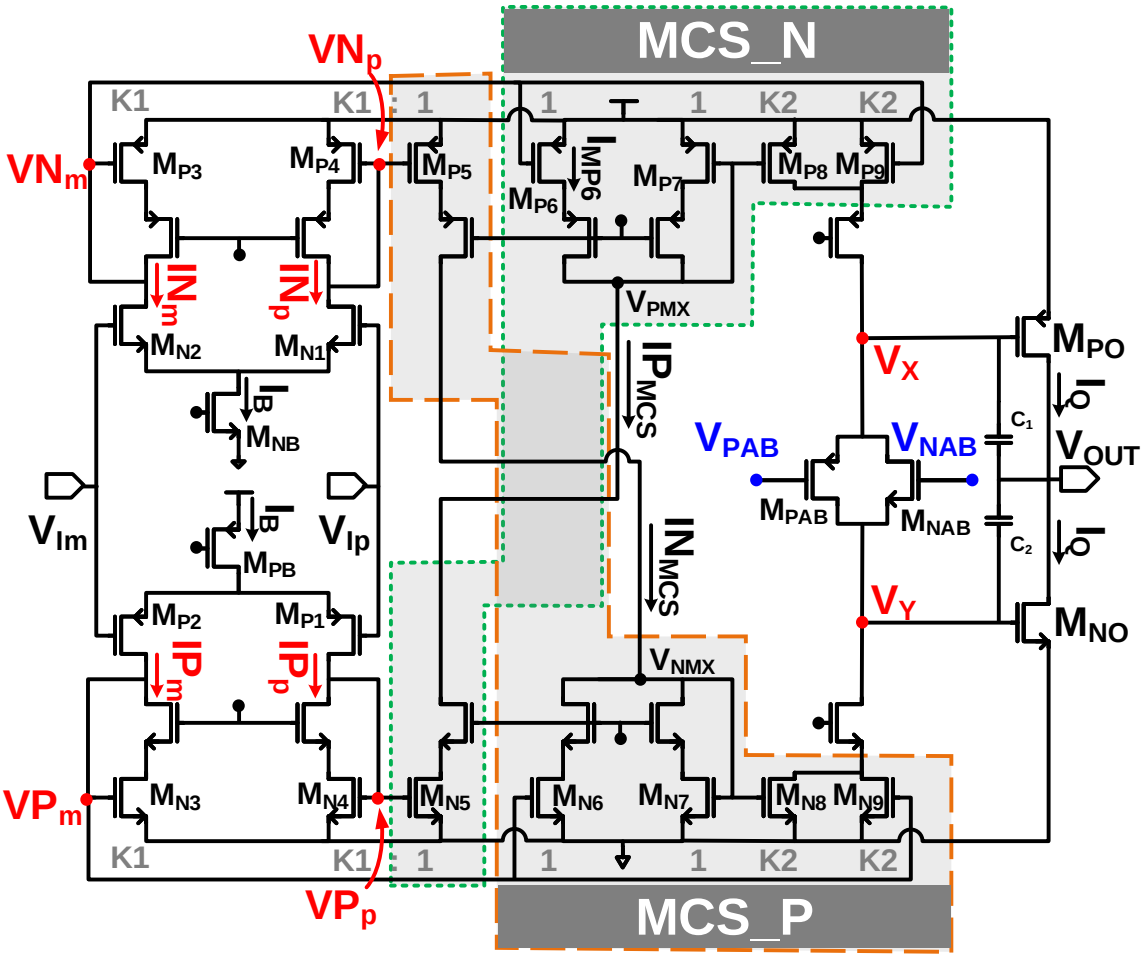

Figure 3.11: Proposed Linear Amplifier with the Input Maximum Current Selection Circuits.

through M_{P6-8} and current directly mirrors from M_{P3} to M_{P9} and defines output bias stages current with the value of $K2/K1 \times I_B/2$. A similar, but complementary operation is expected when the input signal level is low and only PMOS pair is on.

Around common-mode voltage when both NMOS and PMOS input pairs are on, current flowing through M_{P6} (I_{MP6}) is compared with the IP_{MCS}. For $I_{MP6} > IP_{MCS}$, V_{PMX} node is pulled-up to V_{DD}, and M_{P6} is in linear region, and M_{P7-8} are in cut-off region. Current flowing through M_{P9} sets the pull-up current. When $I_{MP6} < IP_{MCS}$, current $(IP_{MCS} - I_{MP6})$ flows through M_{P7} which is mirrored to M_{P8}, and the sum of the currents flowing through M_{P8} and M_{P9} set the pull-up current. Hence, the

maximum current of I_{MP6} and IP_{MCS} is selected in both the cases. Similarly, in the maximum current selection circuit on the pull-down path, the current flowing through M_{N6} is compared with the IN_{MCS}. The maximum current among then is selected, setting the pull-down current of the class-AB stage.

The GBW of the proposed amplifier with the maximum current selection is constant for the input common mode range which is expressed as GBW_{main},

$$GBW_{main} = \frac{K2}{K1}\frac{g_m}{C_M} \tag{3.7}$$

where, g_m is the transconductance of input transistor M_{N1}, M_{N2}, M_{P1} or M_{P2} (assuming all of them are identical), C_M is the equivalent capacitance at the output stage $\mathrm{V_X}$ and $\mathrm{V_Y}$ nodes, and $K2/K1$ is the current mirroring ratio between the last stage and input stage currents.

Slew Rate Enhancement Circuit with Bias Adjustment

The LA with parallel SRE paths is shown in Figure. 3.12. The parallel SRE path mirrors input stage branch currents IN_m, IN_p, IP_m, IP_p (shown in Figure. 3.11), with the ratio of γ, where γ is chosen $1/16^{th}$ to limit current consumption of the SRE circuit. Then, the SRE circuit subtracts the copied currents, and since after subtraction the currents are small, it scales up to the factor of α to generate the auxiliary currents $I_{SRDn} = \alpha IN_p - \alpha IN_m$, $I_{SRDp} = \alpha IP_m - \alpha IP_p$, $I_{SRCn} = \alpha IN_m - \alpha IN_p$, $I_{SRCp} = \alpha IP_p - \alpha IP_m$. These auxiliary currents are directly injected to the dominant pole capacitors at the gate of the class-AB stage devices $\mathrm{V_X}$ and $\mathrm{V_Y}$ to speed up the discharging or charging of these capacitors.

This circuit also adjusts the floating voltage sources V_{PAB} and V_{NAB} to maintain a minimum output stage quiescent current I_Q during the SRE. Minimum I_Q is required to ensure that the push-pull stage is operating in class-AB mode, and eliminate cross-

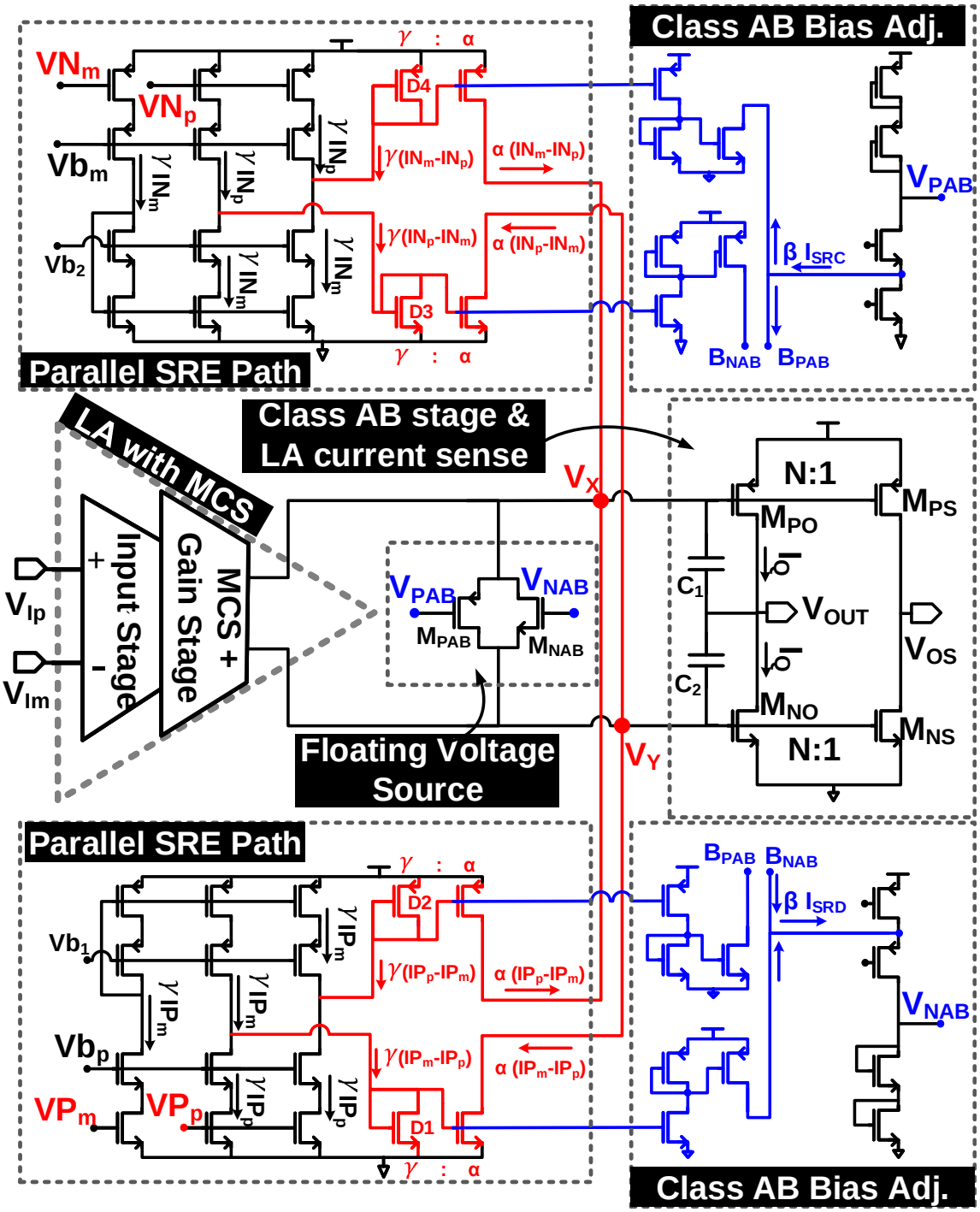

Figure 3.12: Overall Linear Amplifier with Parallel SRE and class-AB Bias Adjustment.

over distortion. When $V_{ENV} - V_{OUT}$ $(V_{Ip} - V_{Im})$ is positive, the currents I_{SRDn} and I_{SRDp} will sum up to generate $I_{SRD} = I_{SRDn} + I_{SRDp}$, to pull down V_X and supply

current to the V_{OUT} by M_{PO}. This operation also pulls down the V_Y node and forces M_{NO} into cut-off region. This will cause a dead-band in the transition point from M_{PO} to M_{NO} and degrade transient response. Thus, a minimum quiescent current should be maintained in M_{NO} to avoid this problem. For this purpose, the floating voltage source adjusts during SRE, as the mirrored current of βI_{SRD} increases the V_{NAB} and consequently the V_Y voltage. The similar operation is expected for the negative slewing of $V_{ENV} - V_{OUT}$ by increasing $I_{SRC} = I_{SRCn} + I_{SRCp}$, to charge V_Y node, and decreasing V_{PAB} to attain I_Q at M_{PO}. When the circuit is not slewing, currents flow through input branches are equal and the current difference, I_{SRD}, and I_{SRC} are ideally zero and do not affect the LA operation.

Simulated transient response of the LA for input signal of $1.6V_{pp}$, 60MHz signal is shown in the Figure. 3.13. When the SRE circuit is disabled, the output is clearly slewing and cannot follow the input signal. While turning on the SRE, although the output is not slewing anymore, there is a risk of distortion due to transition dead-band between M_{PO} and M_{NO}. Using class-AB bias adjustment circuit, more smooth transition is achieved.

According to SRE circuit operation, improvement in slew-rate can be achieved not only at middle CM level, but also at high or low input CM level when only one input pair is active. In the absence of the slew-rate enhancement circuit for the large signal operation when LA enters slewing mode of operation, the charging or discharging of V_X and V_Y nodes is limited by the bias tail current through M_{NB} or M_{PB}, I_B shown in Figure. 3.11. Therefore, the slew-rate at V_X and V_Y nodes, due to one of input pairs, is represented as,

$$SR_{X,Y,SRE-OFF} = \frac{K2.I_B}{K1.C_M} \tag{3.8}$$

where, C_M is the equivalent capacitance at nodes V_X and V_Y. The slew-rate enhance-

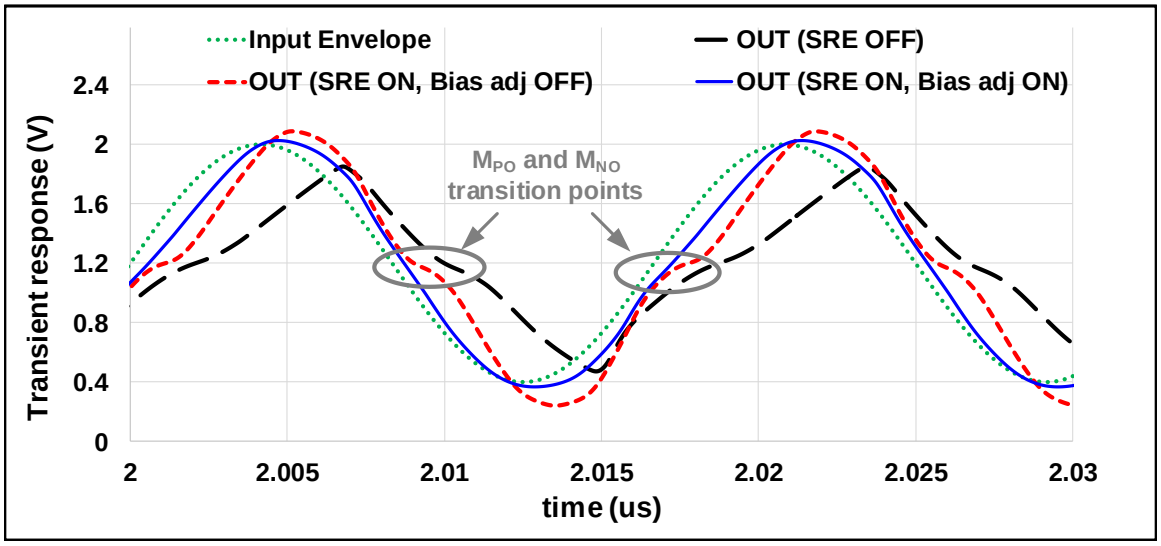

Figure 3.13: Simulated Transient Response of the Linear Amplifier for 60MHz Sine Wave, While SRE Is Disabled, SRE Is Enabled and Bias Adj. Is Off, and SRE and Bias Adj. Are Both Enabled.

ment circuit generates the additional charging or discharging current I_{SRC} or I_{SRD} which improves the slew-rate of the LA. Hence, for the proposed LA, the slew-rate is written as,

$$SR_{X,Y,SRE-ON} = (\frac{K2}{K1} + \alpha)\frac{I_B}{C_M} \tag{3.9}$$

As mentioned earlier and $K2/K1$ is the current mirroring ratio between last stage and input stage, and α is current mirroring ratio between SRE stage and input stage. The slew-rate increases by,

$$\frac{SR_{SRE-ON}}{SR_{SRE-OFF}} = 1 + \alpha\frac{K1}{K2} \tag{3.10}$$

where in the design, $K2/K1$ ratio is 3 and α can be adjusted from 1×3/16 to 15×3/16. It is critical to note that in the small signal operation, input stage branches carry the same amount of current and current consumption of SRE circuit is negligible.

The post-layout simulation results show that using this method and α =4×3/16, the slew-rate improves from 178V/μs to 325V/μs and -169V/μs to -307V/μs, which

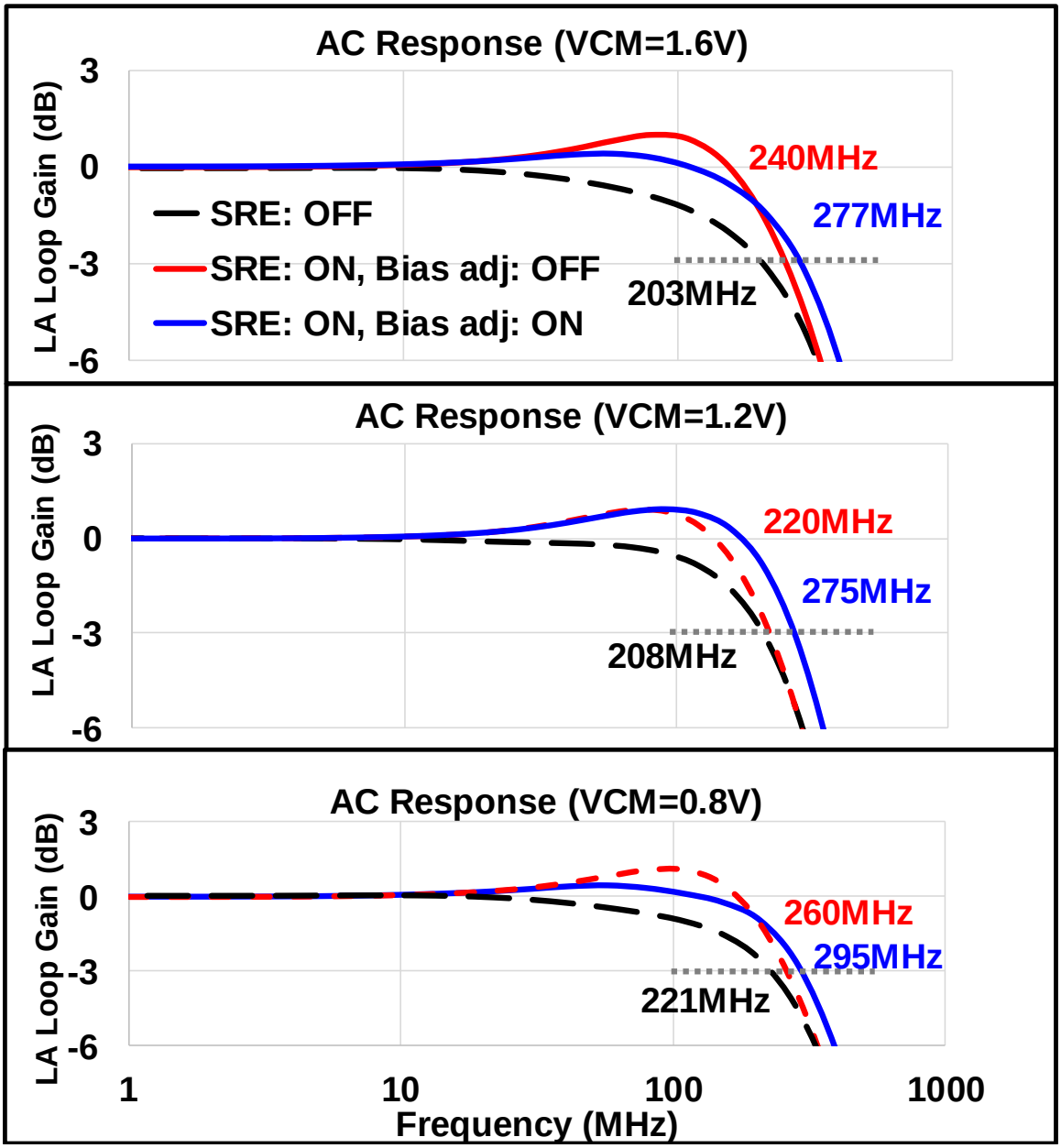

Figure 3.14: Simulated AC Response of the LA with SRE Is Disabled, SRE Is Enabled and Bias adj. Is Off, and SRE and Bias Adj. Are Both Enabled.

is adequate for tracking LTE-80MHz envelope signal. Figure. 3.14 shows the AC response of the LA for input CM level of 0.8V, 1.2V and 1.6V. Due to the MCS circuit, GBW of the LA for the CM range has only 8% variation (from 203MHz to 221MHz), while without MCS, this value can be up to 50%. Using SRE and class

AB bias adjustment, GBW improves up to 275MHz. Although in the small-signal mode the DC currents at subtractors output in the SRE circuit are ideally zero, the diode connected transistors (D1–D4) are in sub-threshold region and contribute to the simall-signal gain. Therefore, there is a small-signal path through SRE circuit that causes the improvement in the GBW when it is enabled.

Chapter 4

MEASUREMENT RESULTS

The modulator is fabricated on a 65nm CMOS technology and occupies core area of 1.7mm×1.6mm including 12nF on-chip flying capacitor, as shown in the die micrograph in Figure. 4.1. The modulator operates with a maximum supply voltage option of 2.4V, while 1.2V thin gate-oxide devices are used for the switching converter. An off-chip inductor of 538nH is used for testing, and the modulator is characterized with 4.7Ω constant resistor load resembling the supply node impedance of a PA.

Fig. 4.2 shows the measured waveforms for LTE-80MHz signal with quadrature phase shift keying modulation and 7.84dB PAPR. Input envelope signal, output signal, switching node voltage and flying capacitor voltage are shown in the figure. The

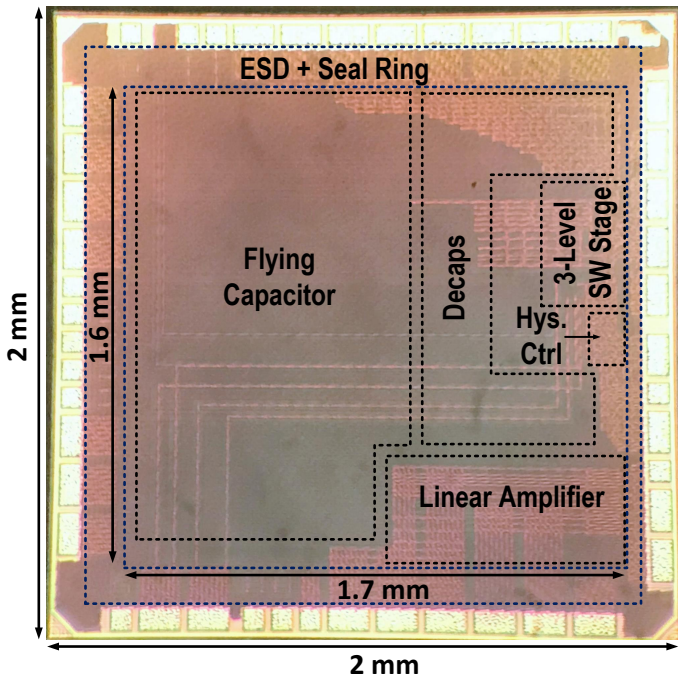

Figure 4.1: Die Micrograph.

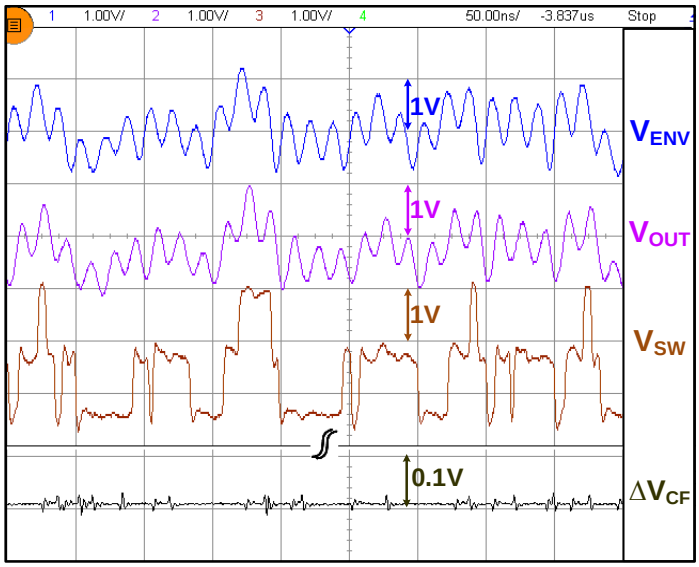

Figure 4.2: Measured Transient Response of the ET Modulator to LTE-80MHz Envelope Signal.

output is following the input envelope signal with about 6ns delay. The 3-level V_{SW} node, as expected, switches between 0V, 1.2V and 2.4V. As it can be seen, the V_{SW} only switches to 2.4V when the input envelope level is more than 1.2V. V_{CF} is regulated to 1.2V within 40mV accuracy.

Fig. 18 shows the measured tracking error between output and input voltages versus output power. When the SRE circuit is off, the modulator tracks LTE-40MHz with 8.06dB PAPR and less than 2.3% output-input tracking error. In this case, turning the SRE circuit on, has negligible impact on the tracking error. However, for wide bandwidth LTE-80MHz signal, the SRE circuit impact is more significant. When the SRE circuit is off, the modulator output slews and the tracking error increases dramatically. By turning the SRE on, the modulator bandwidth meets the LTE-80MHz standard with 7.84dB PAPR, and it tracks the signal envelope with less than 3.2% error.

The measured ET modulator efficiency with constant load resistor of 4.7Ω is shown in Figure. 4.4, where the modulator achieves 91% of peak efficiency for LTE-80MHz

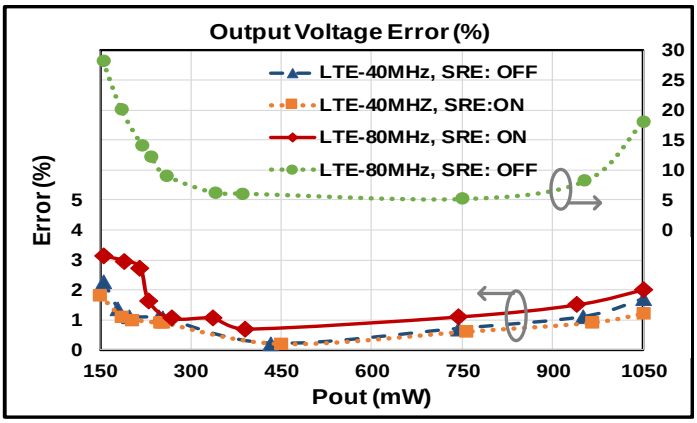

Figure 4.3: Measured Error Between Output and Input Voltage versus Output Power for SRE ON and OFF Conditions

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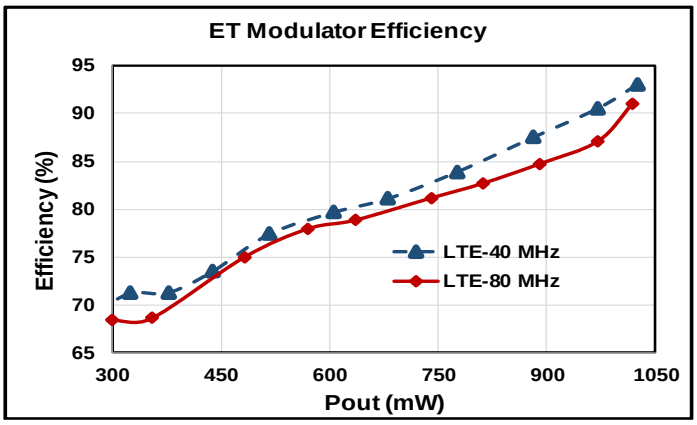

Figure 4.4: Measured Efficiency of Envelope Tracking Modulator with 4.7Ω Resistor Load.

signal, while this value for LTE-40MHz is 93%. At 500mW output power (3dB back-off), modulator efficiency is more than 76% and at 300mW (5.2dB back-off) efficiency is more than 68%.

The modulator is tested with a commercial PA and the output spectrum for LTE-80MHz is shown in Fig. 4.5. The challenges of 65nm CMOS technology with lower supply voltage lead to lower RF output power level at 24dBm, and lower linearity of the PA resulting in adjacent channel leakage ratio (ACLR) of 32.5dBc.

We measured the modulator with 5G NR 100 MHz signal. With10-ohms resistor

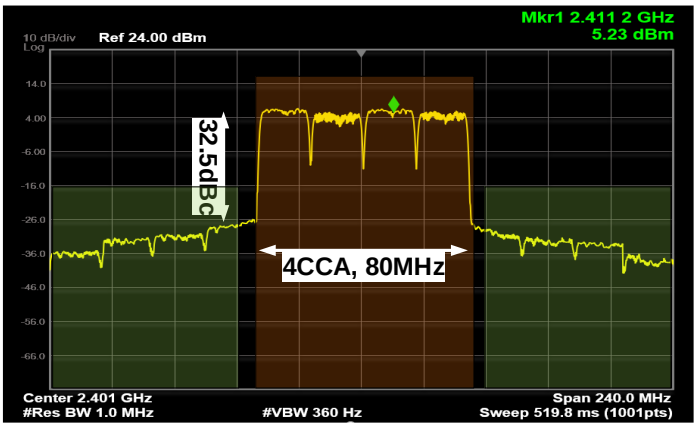

Figure 4.5: Output Spectrum of Supply Modulated PA for 4 Intra-Band Carrier Aggregation (4CA) LTE-80MHz Signal.

Figure 4.6: Measured Efficiency of Envelope Tracking Modulator with 4.7Ω Resistor Load.

load at the output and 1.5V swing, the modulator can operate for 5G NR 100MHz signal and track its envelope. Figure. 4.6 shows the input and output envelope signals. However, the key goal of this paper is to support bandwidth up to LTE-80MHz, and the modulator shows limited performance for 100MHz bandwidth.

The comparison of the proposed ET modulator with prior state-of-the-art is given in Table I. The modulator demonstrates wideband tracking for LTE-80MHz envelope signal. It also achieves high peak efficiency of 93%. The proposed modulator has

minimal off-chip components with only one off-chip inductor and no AC -coupling capacitors. On the other hand, in the AC-coupled LA in hybrid structures, the supply voltage of the class-AB amplifier does not need to be as high as the peak voltage of the output signal, and it is just needed to be equal to the AC swing plus headroom. Thus, by using smaller supply voltage for the class-AB linear amplifier, mid-range efficiency can improve as in [27–29, 50]. Thanks to the proposed hysteresis control, the switching converter achieves over 80MHz of switching frequency.

Table 4.1: Comparison of the Proposed Approach with Prior State-of-the-arts

Ref.	**This work**	[28]	[32]	[12]	[50]	[29]	[46]	[26]	[8]	[27]
CMOS Tech.	**65nm**	65nm	130nm	180nm	90nm	153nm	65nm	180nm	130nm	130nm
Supply (V)	**2.4**	2.4	3.2–4.6	3.6	5	3.8	1.2	NA	1.2	4
Protocol	**LTE-A 80MHz**	LTE 20MHz	LTE 20MHz	LTE-A 40MHz	5G NR 100MHz	LTE-A 80MHz	Sine-wave 9MHz	LTE-A 80MHz	Sine-wave 13MHz	LTE 10MHz
Out Power (W)	**1**	0.8	0.8	2.5	0.8	4	0.23	1.1	0.2	0.8
Peak Eff. (%)	**91 @80MHz 93 @40MHz**	88.7	88.2	91	88	81.2 @80MHz 85.5 @40MHz	87.7	72.8 @80MHz 76.4 @40MHz	88.2	82
PAPR (dB)	**7.84 @80MHz 8.06 @40MHz**	7–9	5.8	NA	6	8.3 @80MHz 7.54 @40MHz	NA	12.5 @80MHz 9.6 @40MHz	NA	5.8
Off-Chip Ind.	**538nH**	206nH	4.7μH + 1 ind*	1μH	4 ind*	1μH +0.68μH	4.5μH	1 ind*	100nH	2 ind*
Off-Chip Cap.	**none**	1μF	none	none	1 cap*	4.7μF	none	none	none	1 cap*
RF Power (dBm)	**24**	23.9	27	28.5	23	26	NA	21.7	NA	27
ACLR (dBc)	**-32.5**	-32	-40	NA	-38.1	-38.1	NA	-30	NA	-41.1

*Component value is not available.

Chapter 5

CONCLUSION AND FUTURE WORK

Different blocks in the transceiver and communications circuits gets affected to meet the bandwidth and power requirements of the new communication standards. Blocks such as low noise amplifiers, voltage controlled oscillators, data converters, power amplifiers and many other blocks require novel techniques to optimize the performance [51–58]. In this work, the emphasis is on the efficiency improvement of the power amplifier using hybrid envelope tracking technique.

5.1 Conclusion

A hybrid switching-linear envelope tracking (ET) modulator for wideband applications is proposed. A hysteresis control method for three-level switching converters is developed, achieving a high-speed controller with a high switching frequency, utilizing the hybrid ET modulator structure. Combined operation provides a high bandwidth switching converter with small current ripple. A slew-rate enhanced linear amplifier (LA) is designed to track wideband signal with low quiescent current consumption. The slew-rate enhancement (SRE) technique injects current directly to the dominant pole capacitor node to speed-up charging and discharging process and avoid changing the operating point of the previous stages. Also, the minimum quiescent current for class-AB push-pull stage is maintained by adjusting their bias voltages during SRE circuit operation. Maximum current selection is employed to attain constant input stage transconductance and constant bias current for last stage over the input common mode range. The measurement results show the tracking of LTE-40MHz envelope with 93% peak efficiency while the SRE is disabled. Enabling the SRE, it

can track LTE-80MHz envelope with peak efficiency of 91%. With the supply voltage of 2.4V, the modulator can provide up to 1W output power.

5.2 Future Work

To further improve this design, different approaches can be taken. This improvement can be attained in bandwidth improvement, efficiency improvement, or both. One way to improve the back-off efficiency is AC-coupling the linear amplifier the output. Thus, the supply voltage of the LA can be controlled to reduce power loss at lower power level and improve overall efficiency. Also, the envelope signal can be shaped to reduce the peak-to-average power ratio.

To further reduce the current provided by the LA, wider bandwidth switching stage can be used with smaller inductor.

Average power tracking is another option to improve efficiency at low power level. In this case, the low pass filtered envelope can be used, so the bandwidth of the signal decreases, thus the LA can be disabled and the whole power can be provided by the switching regulator to improve efficiency.

Another design, could use larger technology point to be able to support higher supply voltage and deliver higher power to the PA.

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