A Study of Dendritic Filament Growth in Tungsten Tri-oxide and Copper Electrolytes

by

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ABSTRACT

Programmable metallization cell (PMC) technology uses the mechanism of metal ion transport in solid electrolytes and electrochemical redox reactions to form metallic electrodeposits. When a positive bias is applied from anode to cathode, atoms at the anode are oxidized to ions and dissolve in the solid electrolyte. They travel to the cathode under the influence of an electric field, where they are reduced to form electrodeposits. These electrodeposits are filamentary in nature and grow in different patterns. Devices that make use of the principle of filament growth have applications in memory, RF switching, and hardware security.

The solid electrolyte under investigation is tungsten trioxide with copper deposited on top. For a standard PMC, these layers are heated in a convection oven to dope the electrolyte. Once the heating process is completed, electrodes are deposited on top of the electrolyte and biased to grow the filaments. What is investigated is the rate of dendritic growth to applied field on the PMC and the composition of the electrolyte. Also investigated are modified three-terminal PMC capacitance change devices. These devices have a buried sensing electrode that senses the increasing capacitance as the filaments grow and increase the upper electrode area.

The rate of dendritic growth in the tungsten trioxide and copper electrolyte of different chemistries and applied field to the PMC devices is the important parameter. The rate of dendritic growth is related to the change of capacitance. Through sensing the change in capacitance over time the modified PMC device will function as an odometer device that can be attached to chips. The attachment of these devices to chips, help in preventing

illegal recycling of old chips by marking those chips as old. This will prevent would-be attackers from inserting modified chips in systems that will enable them to by-pass any software security precautions.

This thesis is dedicated to my family and colleagues who helped me through all the work required for this thesis.

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TABLE OF CONTENTS

CHAPTER Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

Chapter 1

INTRODUCTION

MOTIVATION

Electronic devices are ubiquitous in modern civilization. They are used in defense, finance, transportation, and communications thereby forming the very basis of our infrastructure. In order for our infrastructure to function smoothly, these systems need to function effectively by operating as intended. The loss of one or more devices in the system can increase the probability of breakdown in one or more parts of the infrastructure.

The advent of the Internet of Things (IoT) has turned everyday appliances into communication devices and in a few cases computing devices. Cars, for instance, have become computers on wheels [1]. Medical devices can be accessed wirelessly. Voting machines, watches, and of course computers and cell phones have a lot of hardware that can be exploited [1]. We rely on integrated circuits for everything from the internet, the power grid, financial markets, computer, phones, and many other devices and networks. Defense systems are also reliant on chips to gather, analyze, and move information as it relates to military strategy and combat. Essentially, it is impossible to overestimate the importance of integrated circuits in our civilization.

In addition to ubiquity, there is the problem of complexity. Thanks to advances in accordance with Moore's Law [2], chips have become staggeringly complex. Why is this concept important? The concept correlates with the increasing design and function complexity of the various integrated circuits used in the aforementioned systems.

Increasing design, manufacturing, and functional complexity means more steps in processing a finished device [3]. The upshot of this is more money, more fabrication facilities, more design and manufacturing teams, and so on. Ultimately, this means more steps in which security breaches can happen.

Breaches can lead to intellectual property theft, hacking into systems to obtain data, denial of service, political subterfuge in the case of voting machines [1], death in the case of medical devices or car hacking [1], and other consequences. Due to these potentially disastrous consequences, trust must be ensured in the microelectronic supply chain process.

So, while the increasing complexity has improved our capabilities, there is the issue of trust in the whole process of manufacturing and testing chips [4]. In the past, it was simpler to test nearly all the functionality of a chip [4]. With the increase in devices within a chip, both design complexity and the number of functions have increased. The upshot is that no one person can understand every detail of a chip's design and even the fastest testing systems can take years to exhaustively test all the functionality of a modern chip. To perform that exhaustive testing means that the delivery dates of devices will be pushed back. Therefore, only some functionality is tested of all the possible outputs and those results are used to infer the functionality that was not specifically tested [4]. While this worked quite well historically, hidden functionality can now be inserted that will not be detected by this method of testing which assumes that all the functionality can be sorted out during the verification process.

The insertion of hidden malicious functions into a chip and the insertion of that chip into a system, means that cybersecurity needs to account for hardware as well as software. While hardware hacking requires skills that fewer people have, it is harder to defend against since replacing corrupted hardware is expensive and difficult [3]. Since hardware attacks can circumvent software defenses, it is an exploitable hole that can be used by attackers to exploit a system. One example of one such exploitation is the stealing and decryption of data from a chip [4].

Some attacks cause minor damage that can be contained by security measures already in place. However, others can cause more extensive damage. For instance, attacks aimed at spying and extracting information can hurt national security. In the battlefield, an attack on weapons systems can lead to extensive damage and more important, loss of lives. Other forms of attack can involve denial of service. For instance, attacking a nuclear power plant and disabling its safety systems can cause economic damage and loss of life as well [1].

Cybersecurity largely remains software focused these days. While hardware based cyberattacks are harder to undertake, due to cost and number of people who can get access, it is harder to defend against. Replacing corrupted hardware is very difficult and expensive. While software security is critical, a complete solution will include hardware security as well. There are a variety of counterfeiting techniques that are used by adversaries [4]. Figure 1 below [3], shows the areas in which these attacks can take place.

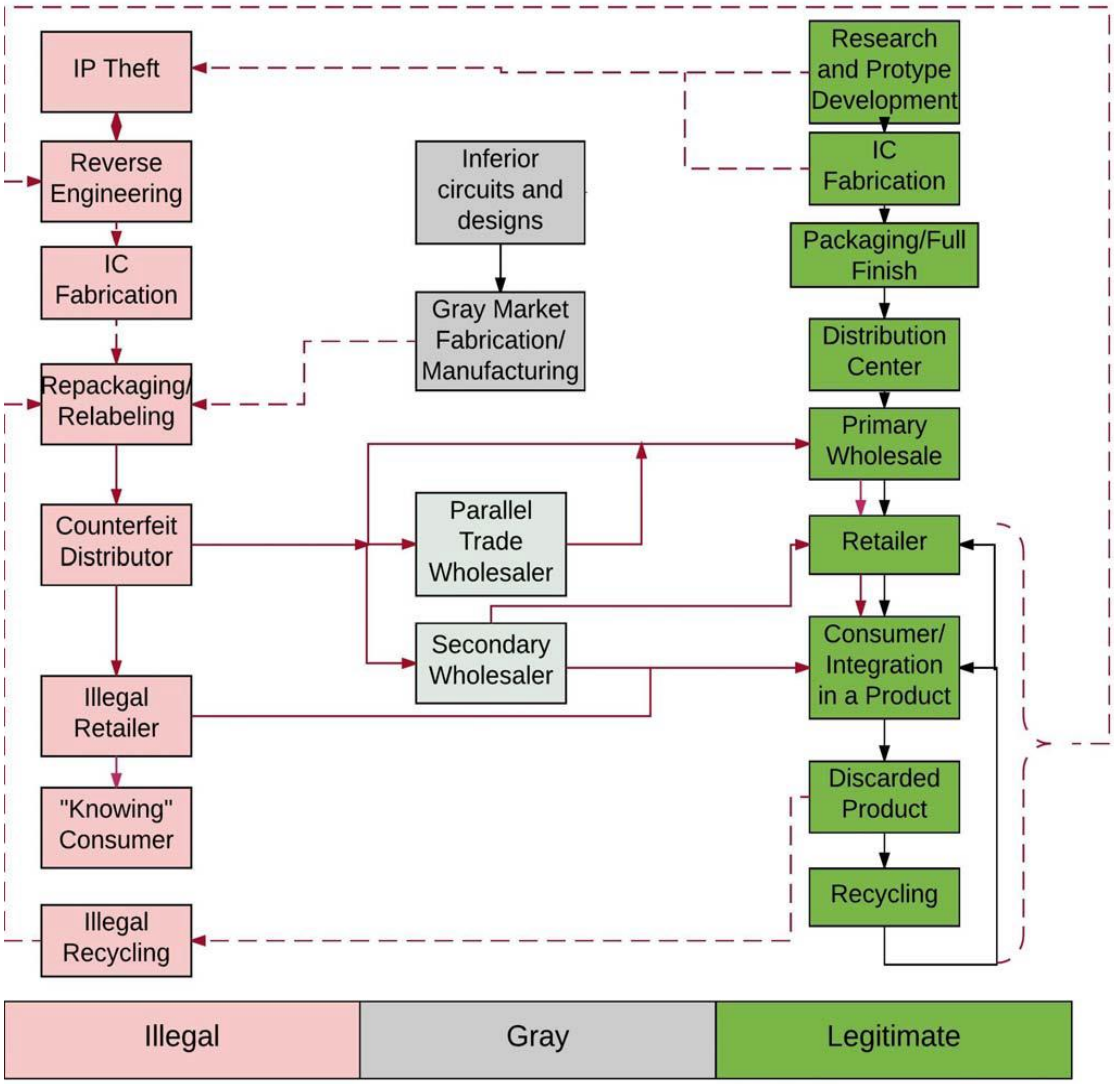


Figure 1: Paths for counterfeit ICs to enter into the IC supply chain

Since quite a few of the supply chain steps are executed by overseas manufacturers and many subcontractors, it makes it especially difficult to protect integrated circuits. It is therefore, important to safeguard the supply chain integrity in order to not only prevent IP theft and money loss, but also attacks on important systems such as those used in medicine and defense. As described before, counterfeiting of hardware is a growing enterprise. Cost of manufacturing and reverse engineering has gone down tremendously.

Additionally, human factors and error can weaken the integrity of the supply chain [3]. Legal action and law enforcement can help with this, but they are largely after the fact solutions [3]. As a preventative measure, physical inspection can help but with cheaper printing and increasing sophistication of attacks, it is becoming less reliable [3]. Good hardware security can provide dynamic detection of counterfeit ICs and help to the legal authorities in the event of finding the chain of illegal products and IP infringement lawsuits.

In order to help with maintaining the integrity of the supply chain, authentication technologies are needed. Below are a few examples of such technologies.

1) *Tagging and Certification of Authenticity*: Label the device with a serial number and keep in database. It does not protect against theft and reuse. It can also be duplicated easily.
2) *Watermarking*: Watermarking adds signatures in the circuit design without changing the functionality of a chip [5]. Watermarking is done for a batch of devices during manufacturing and it tells one which company manufactured the device. It is limited in its protective capabilities because employees can either choose not to add the watermark or add the watermark to a harmful device.
3) *Fingerprinting*: While watermarking creates a unique signature for each batch of fabricated devices, hardware fingerprints are unique for each device. It is relatively expensive to implement because of the unique nature of fingerprint as compared to watermarking[4]. Again, the limitation is that fingerprints can be added to harmful devices or not added at all.

4) *Circuit Obfuscation*: Circuit obfuscation and IC camouflaging techniques try to obfuscate the functional properties of a given IC by adding additional logical blocks in the design[6][7][8]. It usually requires a key and the security of the obfuscation depends on the security of the key. The key could be obtained through social engineering methods.

5) *Parametric and Functional Tests*: This is essentially testing the functions and performance of the chip. Parametric measures factors like power consumption, propagation delay, etc. in order to check if the circuit is the right one [9], [10]. As stated before the functionality tests measure how the chip functions. Parametric tests suffer from process variation and aging. A tester could get values within a certain range for the counterfeit chip. Functional tests are limited, because there are too many functions to test and a counterfeit chip can function the same as the original.

6) *Hardware Metering*: Essentially this is an odometer for chip usage. It can be expensive to implement as a solution [4].

7) *Physically Unclonable Functions (PUFs)*: Essentially, PUFs can provide strong challenge-response-based authentication mechanisms for authentic ICs. Since the challenge-response pairs are derived from the unique physical fingerprint of a given device, it is physically impossible to replicate the same responses [11]. It has great security due to the uniqueness of the challenge-response system, but can be expensive to implement [4].

8) *Aging Models and Sensors*: Finally, aging models and sensor can be used for detecting recycled counterfeit ICs [12]. Essentially, it measures the breakdown of

the device by checking the threshold voltage of a new device versus an aged one. However, one can insert a properly functioning device into the supply chain negating the security measures provided by this solution.

Although there are several anti-counterfeiting techniques, the implementations of such techniques are not widely practiced yet. The key reasons for this scenario can be associated with inertia in design and development, cost of maintaining an anti-counterfeit program, lack of technological advancement for testing design and system integrity during runtime, cost of recycling and regulated disposal, cost of maintaining the database of failed and replaced parts, compliance with regulations, and an overall apathy towards counterfeiting.

DENDRITIC FILAMENT GROWTH DEVICES

The idea behind this research is to find an application that will use one or more of the above solutions to hardware hacking and still be relatively cheap and easy to install and implement. The installation of such a device would have to be checked in every step of the supply chain process. Its integration into the supply chain process would aid in counterfeit detection because the absence of such a device or the presence of a different device would cause the counterfeit chip to be immediately discarded. Indeed, this would make it a lot harder to insert malicious hardware into a system.

The device in question is called a dendritic growth device. These devices can fall under a few solution categories. Since they grow in different patterns, they can be watermarks, tags, or fingerprints. Since they grow from one area to another (e.g. cathode to anode under a bias), they can function as an odometer using distance grown over a certain time period. In conjunction with other aging detection methods, dendritic growth devices can form part of a complete solution to hardware hacking.

Dendritic growth devices fall under the category of devices known as programmable metallization cells (PMCs). PMCs employ the mechanisms of metal ion transport in solid electrolytes [13]. A cathode and anode are used for these devices. A positive bias is applied to the anode and atoms at the anode are oxidized into ions. These ions travel under the influence of the electric field that comes from the applied bias. The ions reduce at the cathode to form electrodeposits. These electrodeposits are filamentary in nature and persistent. They can alter the physical characteristics of the material on which they are formed [13]. PMCs can be vertical, where the anode and cathode are vertical relative to each other, or lateral, where they are side to side. Whether they are lateral or vertical,

there are a variety of memory and switch applications (usually vertical devices) for these devices as well as security applications (usually lateral devices). No one device grows the same pattern and so they are as unique as fingerprints.

As mentioned before, PMCs use solid electrolytes as the medium of filament growth and deposition. Past electrolytes used for these PMCs (both vertical and lateral) are chalcogenides [13] and oxides [14]. Electrolytes are created by depositing a glass or an oxide layer and a small amount of metal. The layers are then doped (either through UV light or thermally by heating the layers in an oven) for a certain period of time (usually 30 minutes). The doping of these layers will cause the metal to mix with the glass and provide a supply of metal ions for filament growth (in addition of course to the metal ion supply provided by the anode metal). Once the electrolyte doping is complete, the electrodes can then be deposited and the device is ready for testing.

In the past, various glasses and oxides have been employed as part of the solid electrolyte matrix. Examples are chalcogenide glasses (such as germanium selenides and sulfides of various chemistries [13]) and oxides (SiO_2 [14] and WO_3 [15]). Generally, in the case of chalcogenides, silver has been used as the metal of choice for the electrolytic matrix. A small amount of silver (20-30nm) are deposited on the glass and then hit with UV light for half hour to spread the silver into the chalcogenide matrix. This ensures a supply of silver ions, in addition to the anodic silver, that will be reduced at the cathode to form the filaments. With oxides like WO_3, a small amount of copper (again 20-30nm) is deposited and heated at or above 135C for 30 minutes in the convection oven. Some of the copper oxidizes and some diffuses into the oxide and again this ensures a supply of copper ions, in addition to the anodic copper, for facilitating filament growth.

While chalcogenides are a very good switching solid electrolyte for both vertical and lateral devices, they are not industry friendly. Oxides like WO_3 and SiO_2 are more fabrication facility friendly. As part of this research, tungsten trioxide is investigated. Filament growth in tungsten tri-oxide and copper has been proven in previous research by Dr. Kozicki and Dr. Gopalan [15] [16].

A normal PMC is just an anode and a cathode on an electrolyte as described above. Following is a figure to show the operation of a modified lateral PMC device, of the type studied in this research.

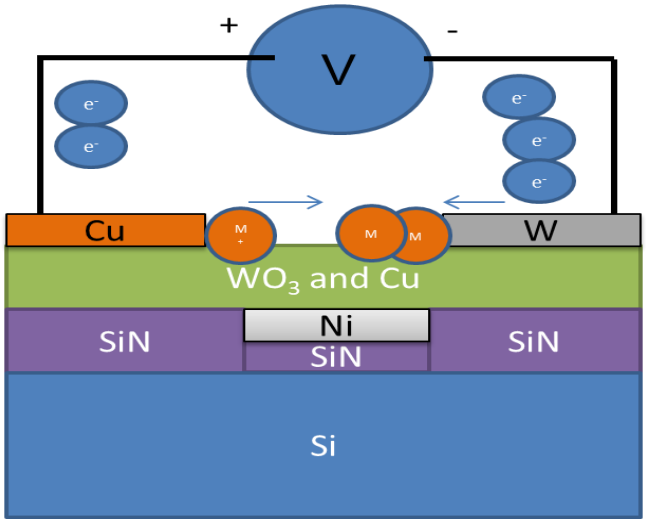


Figure 2: Three-terminal Lateral Device operation

Figure 2 shows how a typical device would operate in the context of capacitance change devices. As the positive bias is applied from cathode to anode, the anode metal is oxidized. The oxidized metal ions travel across the electrolyte toward the cathode under the influence of the electric field. The metal ions go to the cathode and are reduced by the electrons coming out of the cathode. The reduced anode metal accumulates, in different patterns, at the cathode and start to grow toward the anode forming the filament

that will eventually short the device if the bias is applied long enough. The rate of the filament growth is limited by the ability of the metal ions to diffuse through the electrolyte.

As the filament grows from cathode to anode the capacitance increases. The equation for capacitance germane to this device is $C= e_0 e_r A/d$, where e_0 is the permittivity in free space and e_r is the dielectric constant of the electrolyte. As the filament grows, the area A above the electrode increases and the distance d decreases which results in the capacitance increasing.

The tungsten tri-oxide and copper electrolyte is different from the chalcogenide electrolyte in that it is a lot slower in diffusing copper and hence growing dendrites is a lot slower as well. While selenide devices grow dendrites within minutes and sulfide devices grow dendrites within 10 minutes or higher, WO_3/Cu devices can take hours to days depending on the bias voltage. Since it is a new electrolyte compared to the chalcogenides, it had to be tested, even though as stated before, it has been proven to work. The two-terminal devices mentioned below were a way to test the growth of dendrites in the WO_3/Cu system.

Chapter 2

TWO TERMINAL DEVICES

DESCRIPTION

Two-terminal devices just have two terminals: a cathode and an anode. The buried electrode as shown in Figure 2 is not in this device. Hence, it is more like the typical PMC. Figure 3 shows a complete two-terminal device with a tungsten trioxide blanket film and copper blanket film deposited in sequence. The layers are annealed at 135C for half hour. The cathode and anode which are deposited after the annealing process are both copper. These devices were created and tested as a proof of concept to confirm that tungsten tri-oxide will work as a good lateral filament growth electrolyte. Dr. Gopalan has shown that WO_3/Cu does work as a good lateral electrolyte [16].

Two terminal devices were created using a silicon substrate with an isolation nitride. Tungsten tri-oxide was deposited using e-beam evaporation at the rate of 1.2 A/s for a total thickness of 100 nm. Copper (except for the control sample) was deposited at different thicknesses (20, 25, and 30 nm) and then thermally dissolved at 135-140C for half an hour in the convection oven. Copper anodes and cathodes were patterned and

deposited on top of the electrolytic matrix

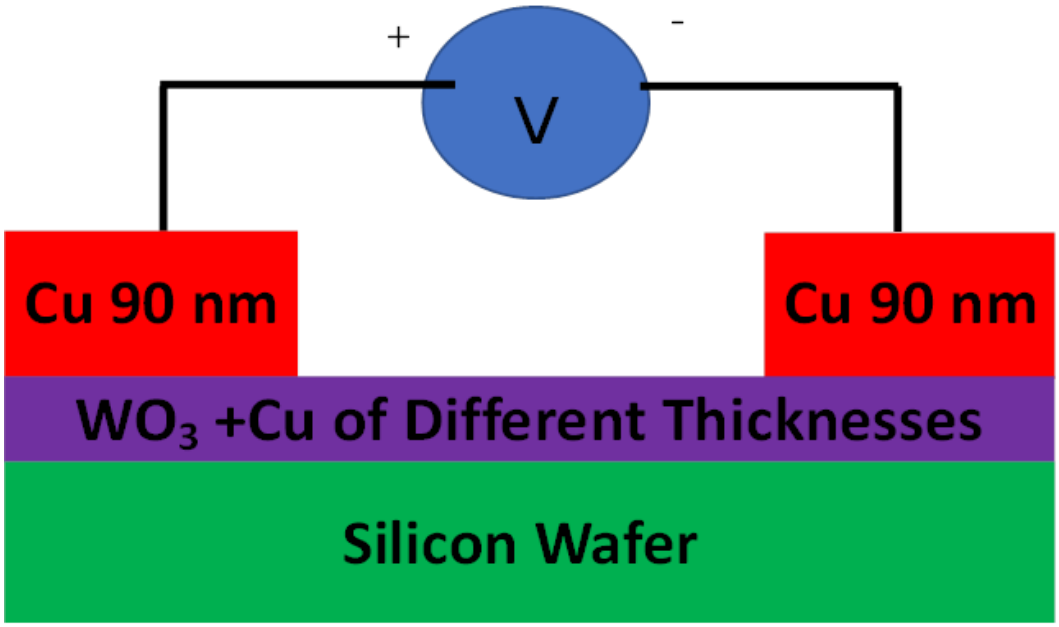


Figure 3: Schematic for a two terminal device structure

PROCESSING

These two terminal devices were relatively simple to process as shown in the figure above. A silicon wafer was used as the base. This wafer was split into quarter wafers. On each wafer piece, 100 nm of tungsten tri-oxide was deposited as a blanket film using electron beam evaporation. Then after one piece was saved as a witness piece, the other three pieces had 20, 25, and 30 nm of copper deposited as blanket films as well. All three wafer pieces were annealed at 135C for half hour.

An initial test was done with 75nm of WO_3 and 15nm of copper. A four point probe measurement of the surface resistance yielded a result of 0.6 ohms/square. Then 2 hours of UV doping was done on the sample and measured again using the four point probe. It was still 0.6 ohms/square. So up to 15 hours of UV doping was done to the sample.

After leaving the sample for a day, the surface resistance was open circuit. The copper may have diffused and oxidized. Testing this sample after depositing electrodes, did not yield filament growth. When depositing thicker amounts of copper as described above, it was decided to use the convection oven to anneal the sample since UV doping did not affect the surface resistance in the thicker witness samples. Annealing in the convection oven did cause the sample to yield an open circuit resistance.

After the annealing process, the electrodes were deposited. To deposit the electrodes, the following process was used:

1) HMDS spun at 4000 rpm for 30 seconds and baked at 120C for 1 minute
2) OCG825 resist spun at 4000 rpm for 30 seconds and baked at 105C for 1 minute
3) AZ 3312 resist spun at 4000 rpm for 30 seconds and baked at 100C for 1 minute
4) Expose using cathode mask for 4.5 seconds
5) Post exposure bake at 100C for 1 minute
6) Develop using MIF300 for two minutes, wash and inspect

After the above steps are complete, 90 nm copper electrodes were deposited on the electrolytic mixture. After this step, acetone is used to lift off the excess metal leaving the electrodes intact. The same procedure described above is then done for the anode side. As shown in the figure, both the cathode and the anode are copper.

There are two types of devices (based on the shape of the electrode) that were tested in these series of experiments, triangular devices and rectangular devices. For the purpose of the tests run for these devices, the naming convention for the devices will be type

(triangular (P for pointed) or rectangular (E for edged)), column (letter) and row (number). So device PF3 will be the triangular (pointed) device in column F row 3.

Figures 4, 5, and 6 are the images made after the processing was completed, but prior to testing.

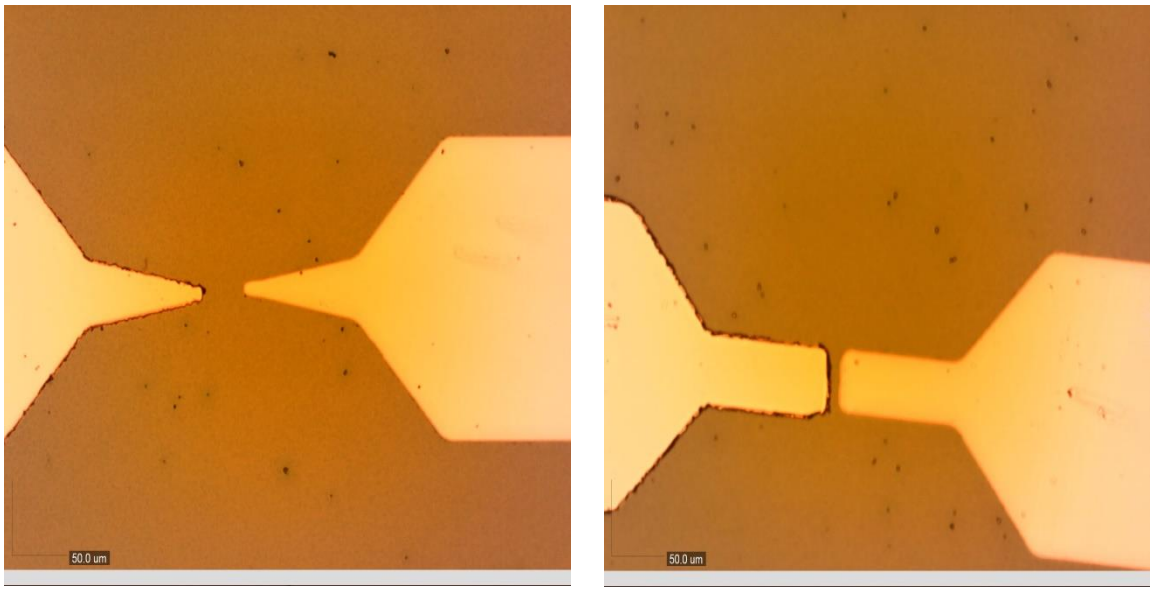


Figure 4: Images of triangular device and rectangular device on 25nm sample at 100X magnification. The anode is on the right for both (reverse microscope). Average distance in pointed device is 38 um and average distance in edged device is 11 um

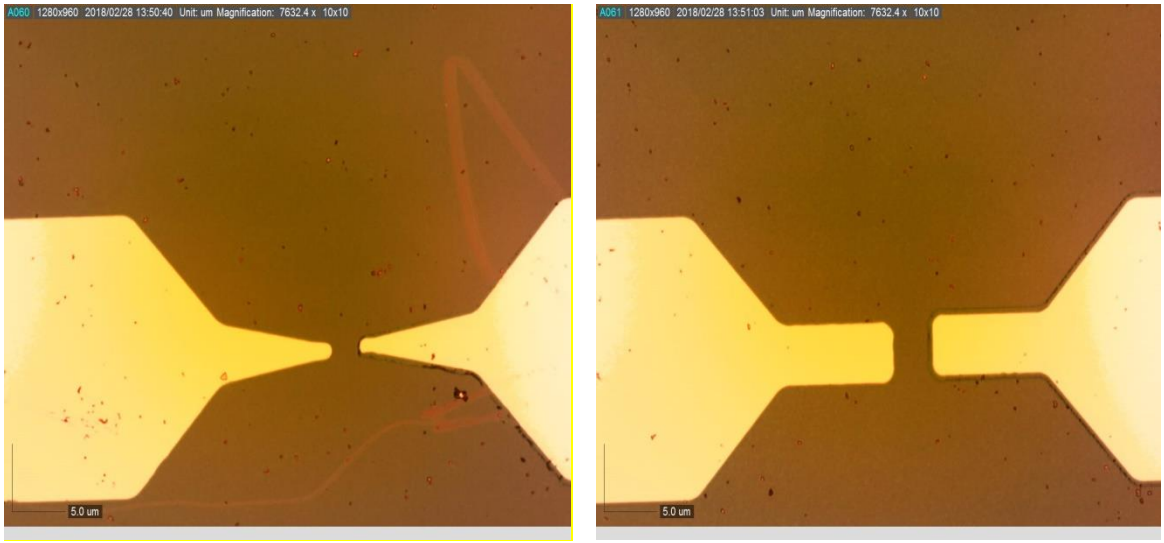


Figure 5: Images of triangular device and rectangular device on 20nm sample at 100X magnification.The anode is on the right for both. Average distance in pointed device is 35 um and average distance in edged device is 11 um

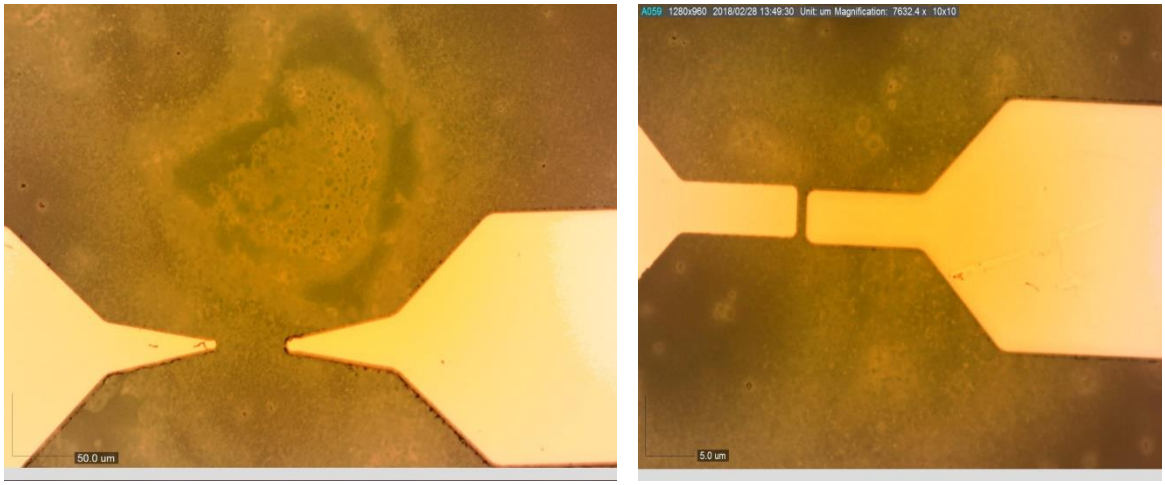


Figure 6: Images of triangular device and rectangular device on 30nm sample at 100X magnification. The anode is on the right for both images. Average distance in pointed device is 35 um and average distance in edged device is 11 um

As can be observed from these images, the 20 nm and 25 nm Cu samples look cleaner than the 30 nm sample. This is due to more surface copper with the thicker sample. This relatively dirty surface becomes more important when discussing the results after doing the DC biasing tests. The next couple of tests were performed to check for proper functionality.

PRELIMINARY TESTS:

Testing the two-terminal devices was a simple process that involving biasing the terminals from anode to cathode at high DC voltages. The reason for this high field application was to accelerate filament growth in the oxide copper matrix. As stated before, unlike the chalcogenide electrolytes, WO_3 and copper are very slow in growing filaments. Like the chalcogenide devices, the filaments in the following images did grow from cathode to anode. The following devices EA1 and PB1 were tested in the 25nm

copper sample, for the purpose of determining whether the devices were functional. The following figures show EA1 which was tested at 20V for 68 hours.

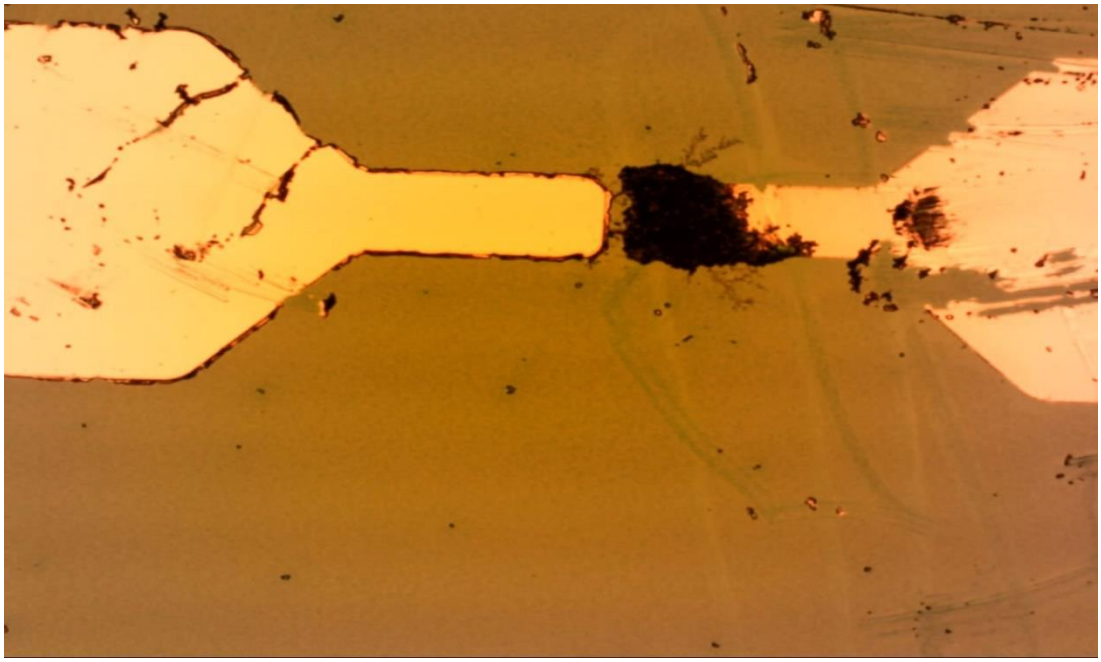


Figure 7: Image of tested rectangular device EA1 in the 25nm Cu sample at 100X magnification. Anode is on the right side (reverse microscope)

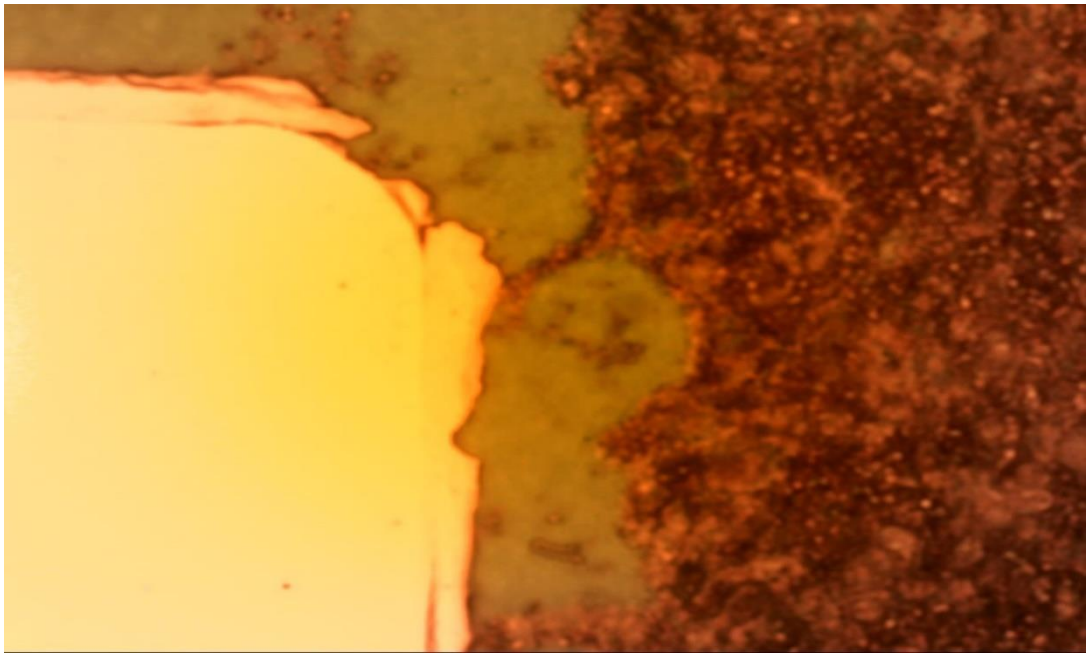


Figure 8: Image of rectangular device EA1 at 1000X magnification. Anode is on the right side (reverse microscope)

These filaments from Figures 7 and 8 grew after testing the device at 20V for 68 hours. The actual shorting of the device occurred at 10.6 hours after voltage application. This is shown by the rise in current in the graph below:

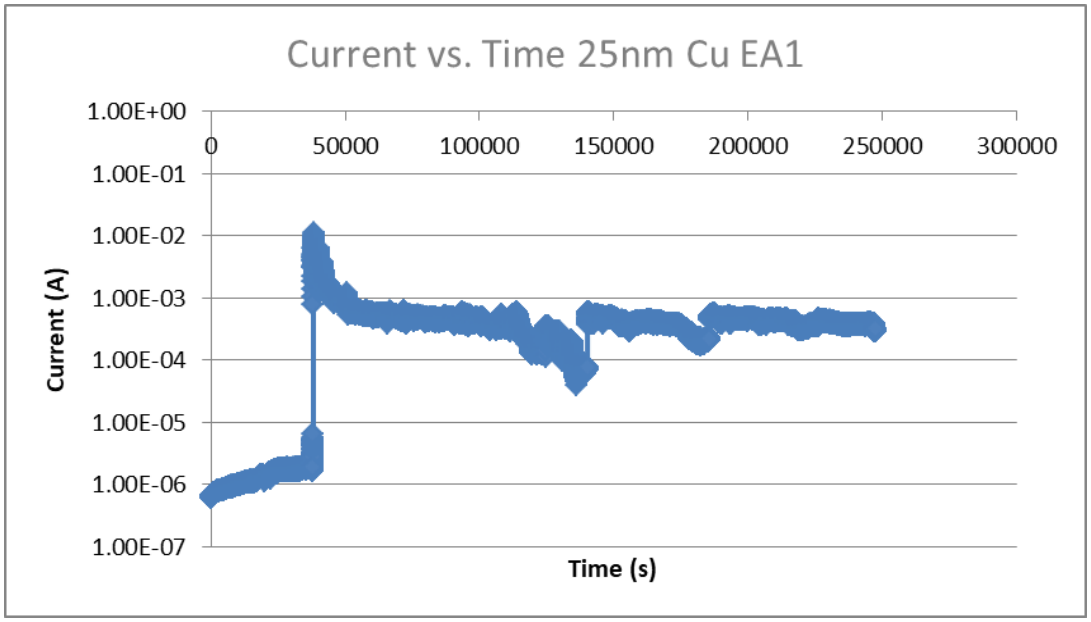


Figure 9: Current vs. Time for the Rectangular Device EA1 for 25nm Cu sample tested in Figures 7 and 8 Images

This graph shows a rise from about 600 nA to about 10 mA at 10.6 hours. This indicates the point at which the filament grew and shorted out the device. Due to the destruction of the device and the electrolyte, the resistance builds back up again slightly, thereby reducing the current after the device is shorted.

A triangular device PB1 was also tested in the same 25nm copper sample. Since the distance was larger between cathode and anode, the testing voltages (in order to get bigger fields across the device) need to be larger as well. The testing started at 50V and then moved to 76V when the filaments were not growing fast enough.

Here is the triangular device, PB1 after testing at 50 and 76 volts at 100X magnification:

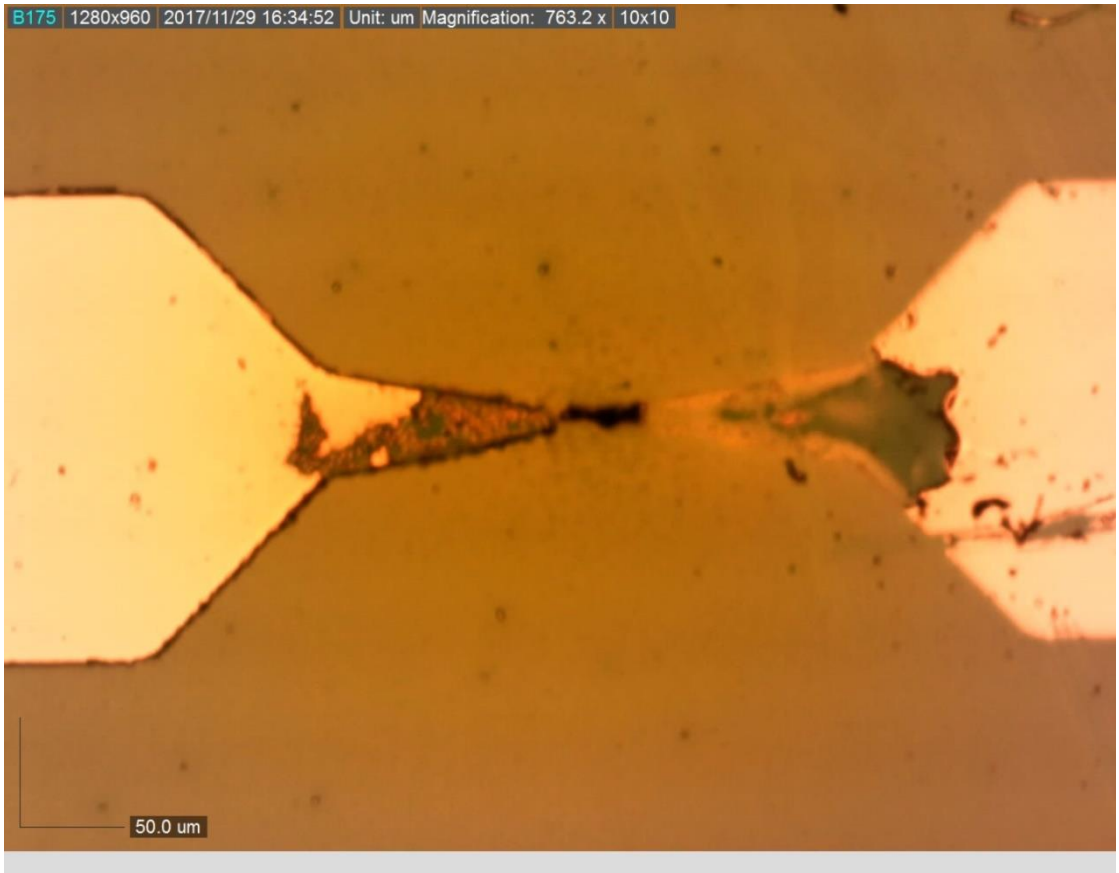


Figure 10: 100X image of triangular device PB1 after testing: anode is on the right side (reverse microscope)

Following is a picture of the same device PB1 taken at 1000X magnification. As can be seen in Figures 10 and 11 as well as Figures 7 and 8, it can be observed that the electrolyte and devices are destroyed. In Figures 10 and 11, it can be seen that there is a "splatter" pattern of dendritic growth, wherein the dendrites are not solid. Rather they are formed in little island shapes. As will be seen later, this seems to be an artifact of high fields in the triangular devices. The rectangular devices do not seem to have this "splatter" pattern like the triangular devices.

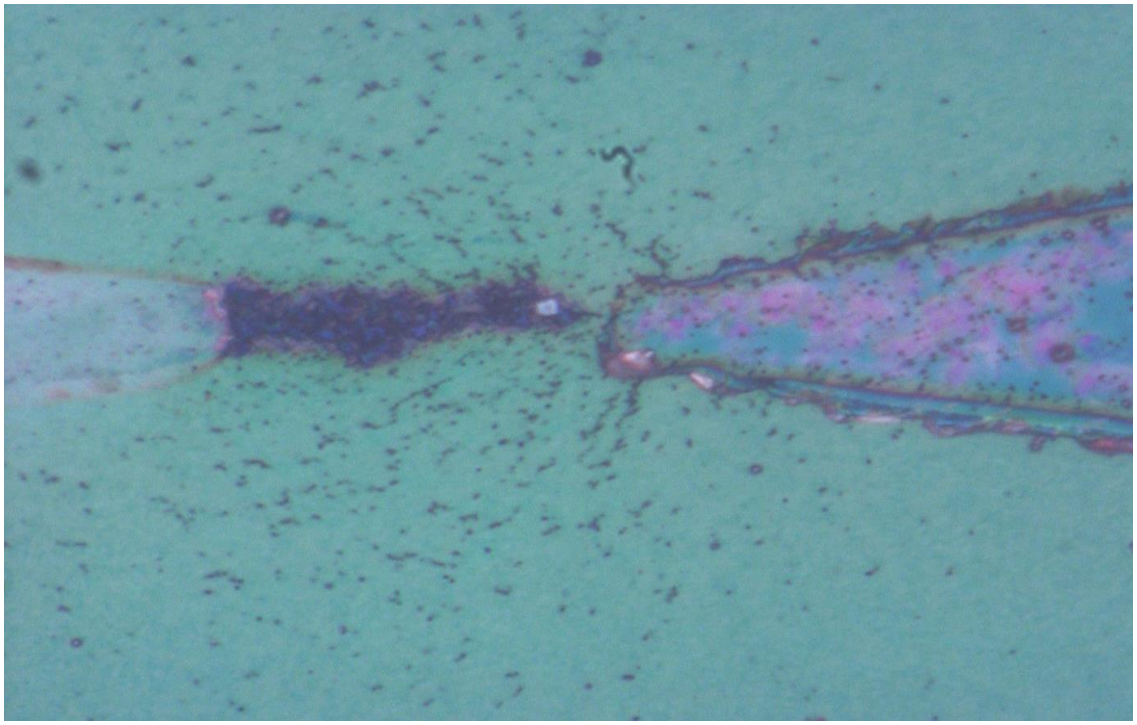


Figure 11: 1000X image of triangular device PB1 after testing. Anode is on the left side (regular microscope)

Following is a graph that shows the rise in current after 2.6 hours of testing at 76 volts.

Not included in the graph is the 1.5 hours of the same device tested at 50V.

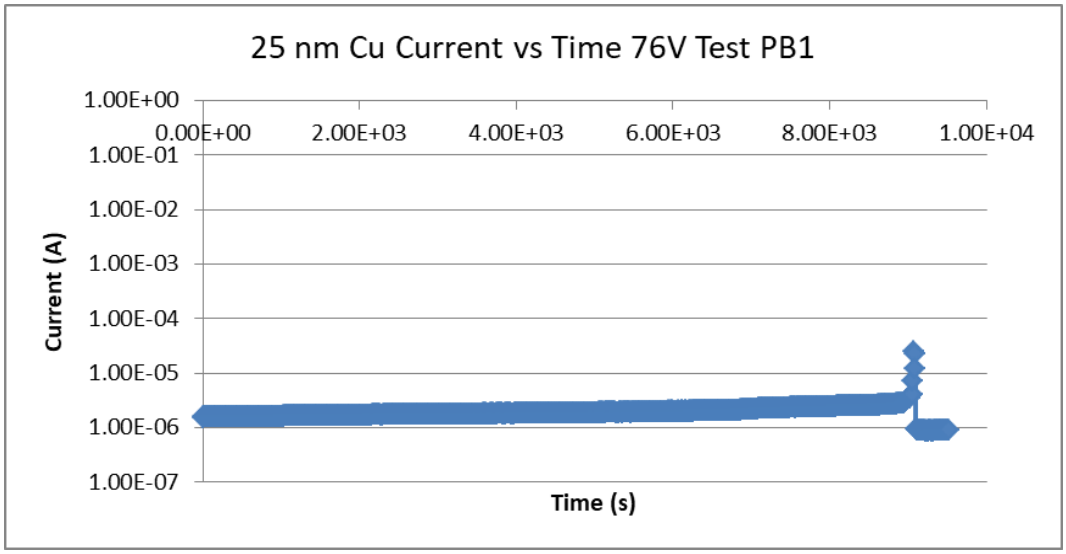


Figure 12: Current versus time graph for triangular device PB1 25nm Cu

The current rises from 7.5e-6 amps to 2.5e-5 amps at 2.5 hours, indicating the time when the filaments grew and shorted out the device. The current goes back down, again, due to the destruction of the device.

As stated before, these tests on devices EA1 and PB1 were performed as proof of concept tests to check whether the devices were functional. Once, they were shown to be functional, the important metric to obtain was the filament growth rate. That was the purpose of the next few tests. Data for the growth rates as a function of field (in V/m) will be given for the samples. Since these are two terminal devices, capacitance is not tested. Additionally, the variables being watched in this initial test is the rate of dendritic growth versus voltage, and eventually copper thickness, anneal temperature, and anneal time.

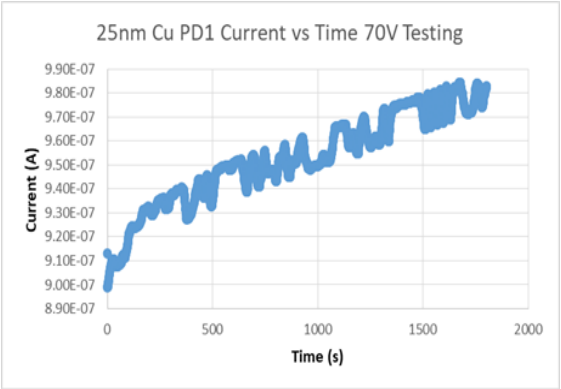
25 NM TRIANGULAR DEVICES

Now that it is established that filaments grow in the WO_3/Cu electrolyte, the relationship between the rate of filament growth, the applied field, and the electrolyte chemistry must be established. To that end, biasing tests are conducted on several devices. It is expected that the ion transport across the electrolyte is the rate limiting step when it comes to filament growth. It is also expected that with electrolyte composition remaining the same, increasing the applied field increases the rate of oxidation. It is also expected that the rate of ion transport will be increase as well. According to the Butler-Volmer equation, there is an exponential relationship between the current and the potential [17].

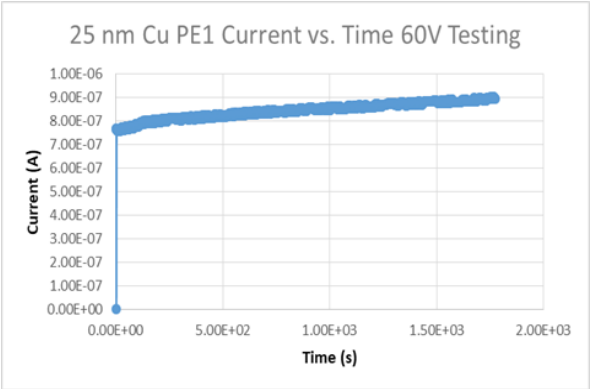
$$i = \vec{i} - \overleftarrow{i} = \vec{k}C_{red}\exp\left(\frac{\alpha_a F}{RT}E\right) - \overleftarrow{k}C_{ox}\exp\left(\frac{\alpha_c F}{RT}E\right)$$

where F is Faraday's constant, R is the universal gas constant, T is temperature in kelvin, α_c and α_a are the cathodic and anodic charge transfer coefficients respectively, E is the electrode potential, and kC_{red} and kC_{ox} are the exchange currents. If the movement of charge is related exponentially to the applied voltage, it is expected that the filament growth rates will be exponential as well.

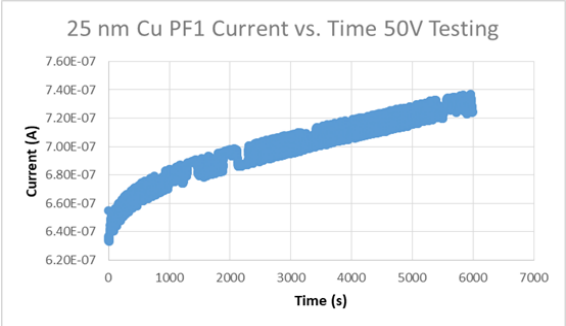
To the end of discovering whether dendritic growth rates are exponentially related to applied voltage, the next series of biasing tests described here were performed on the 25 nm copper sample. The first tests were performed on the triangular devices in the first row. These had an average distance of 38 um between cathode and anode. Following are the data and images for the triangular devices in this sample. These devices were not tested long enough to short them out. Following are the current versus time graphs for devices PD1, PE1, and PF1 which are located in the first row of the triangular devices.



(a)



(b)



(c)

Figure 13: Current versus time graphs for 25 nm first row triangular devices (a) PD1, (b) PE1, and (c) PF1 in 25nm Cu sample

The first device tested was the triangular PD1. It was tested at 70V for 12000 seconds. Figure 13(a) is for the last 1800 seconds of the PD1 device test. PE1 was tested at 60V for 17320 seconds. Figure 13(b) is the data for the last 5320 seconds of that test. PF1 was tested at 50V for 18000 seconds. Figure 13(c) is the data for the last 6000 seconds of the test.

Note that the current rises over time in all the data in Figure 13. A rise in current is generally expected to indicate filament growth. The reduction of the distance between cathode and anode as the filaments grow, reduces the amount of electrolyte available between the electrodes and hence reduces resistance and increases current.

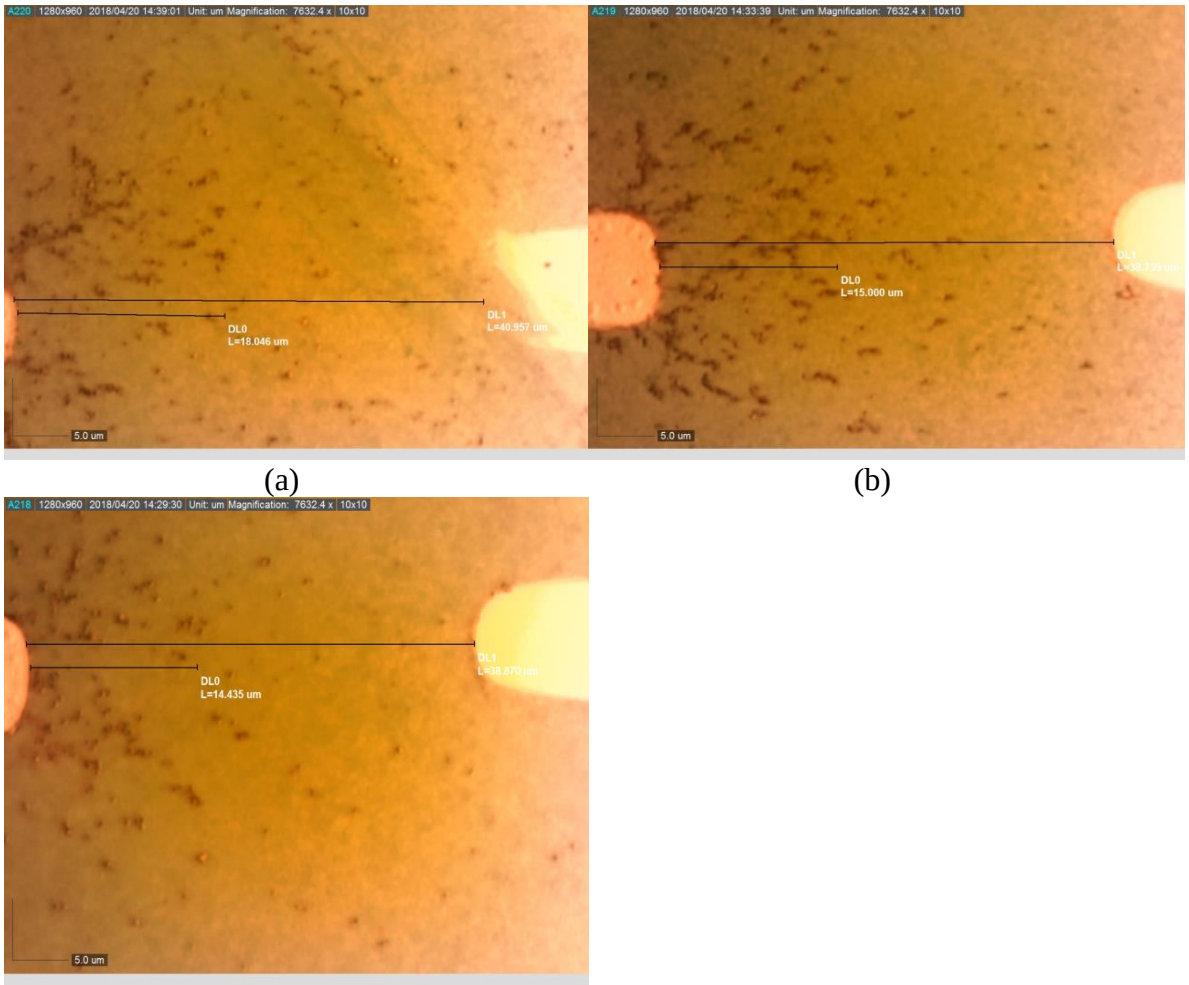
In the case of device PD1, the filaments grew to about 18.046 um in 12000 seconds giving a calculated rate of 0.0015 um/sec for an applied field of 1709109.55 V/m

(70V/40.957um). Figure 13(a) shows a rise in current from 900 nA to 980 nA for the last 1800 seconds and the filament growth is confirmed in Figure 14(a).

PE1 was tested at 60V for 17320 seconds. Figure 13(b) is the graph for the last 5320 seconds of the test. As confirmed in Figure 14(b), the filaments grew to about 15.000 um in the testing time. This gives a rate of 0.000866 um/sec. The applied field at 60V for a distance of 38.739 um was 1548826.76 V/m.

PF1 was tested at 50V for 18000 seconds. Figure 13(c) is the graph for the last 6000 seconds of the test. As confirmed in Figure 14(c), the filaments grew to about 14.435 um in the testing time giving a rate of 0.0008 um/sec. The applied field at 50V at a distance of 38.87 um is 1386339.08 V/m. Please see Table 1 for the data.

Figure 14 shows the 1000X images for the tested devices. The dendrites grew very discontinuously. As the images show, they look like copper islands spreading through the electrolyte. It is expected that at low fields, the filament growth would be continuous and more solid than what was observed. At high fields, it is expected that the growth rate will be faster, but the pattern will still be continuous. However, Figure 14 shows that the patterns are discontinuous.



(a) (b)

(c)

Figure 14: 1000X images for 25 nm first row triangular devices (a) PD1, (b) PE1, and (c) PF1. The anode is on the right side (reverse microscope)

Finally, the fields applied and the growth rates are as follows:

Device	Electrode Distance (um)	DC Bias Voltage (V)	Applied Field (V/m)	Growth Rate (um/sec)
PF1	38.87	50	1286339.08	0.000800
PE1	38.74	60	1548828.76	0.000866
PD1	40.96	70	1709109.55	0.00150

Table 1: Data for 25um Triangular Device Tests (PD1, PE1, and PF1)

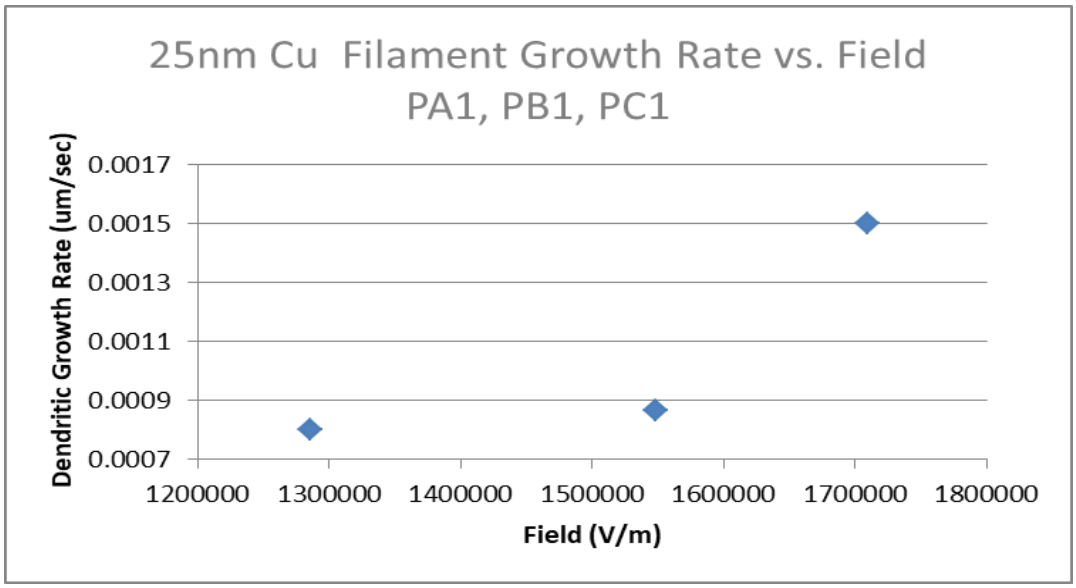


Figure 15: Dendritic rate of growth vs. electric field for PD1, PE1, and PF1

What can be garnered from Figure 15 is that as the field is increased on the devices, the dendritic growth rates increase. However, it is not an exponential increase as expected. Further study is required to discern what is occurring in the electrolyte. There is a possibility that there is a series resistance in the electrolyte that slows down the ion transport, even at high fields. This resistance causes the relationship between filament growth rates and applied field not to be exponential.

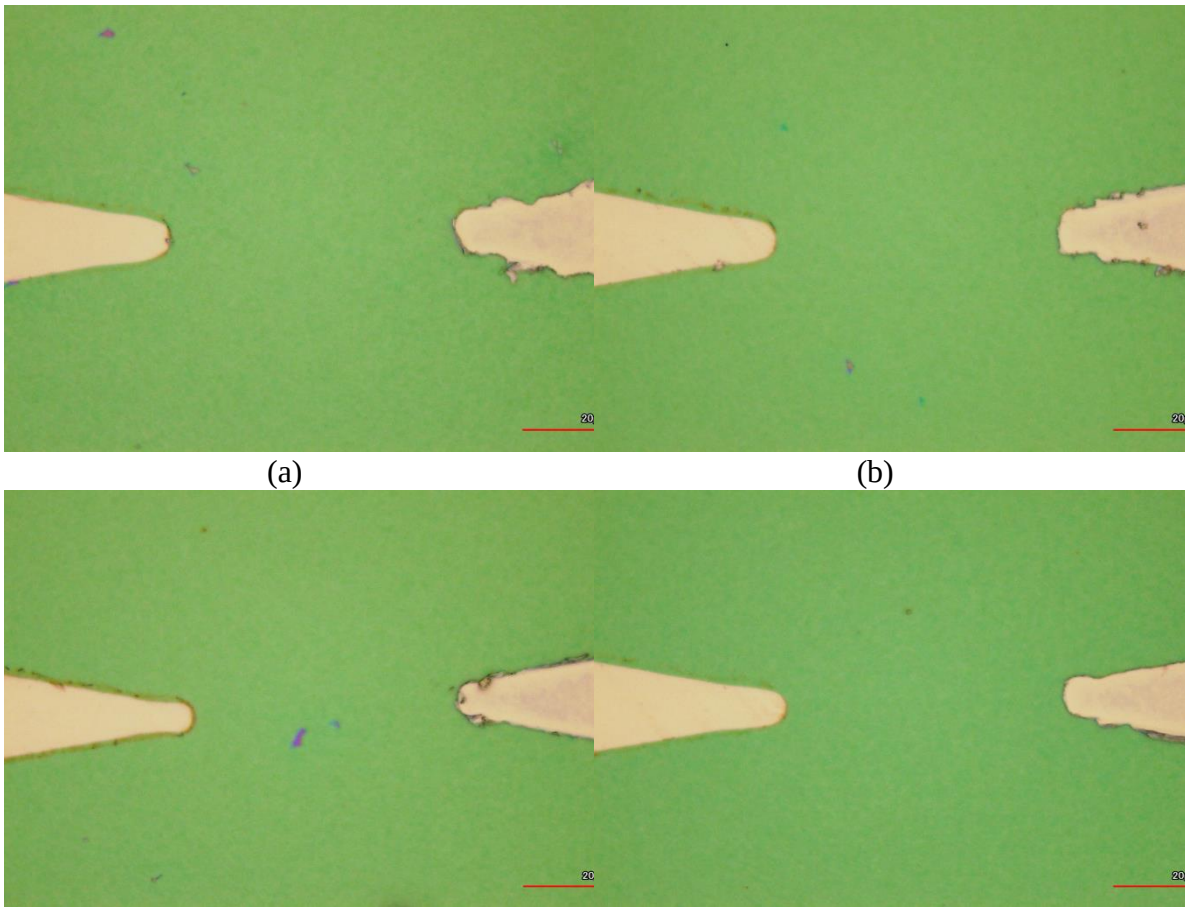
In order to further establish a relationship between the field and dendritic growth rate in the 25 nm sample, more tests were performed on triangular and rectangular devices. For the triangular devices the next higher row above the formerly tested was used. The distance between the electrodes for this second row was 63 um, as opposed to the 38 um in the first row. The reason for these tests is to check on the expected hypothesis that the rates and field have an exponential relationship. They were also used to apply lower fields to test the hypothesis that lower fields means continuous dendritic growth. The

greater distances would provide for lower fields and hence, could lead to more continuous dendrites. Following were the tested devices:

Triangular Devices

- PB2 (at 40V for 50000 seconds)
- PC2 (at 50V for 50000 seconds)
- PI2 (at 60V for 30210 seconds)
- PD2 (at 70V for 50000 seconds)

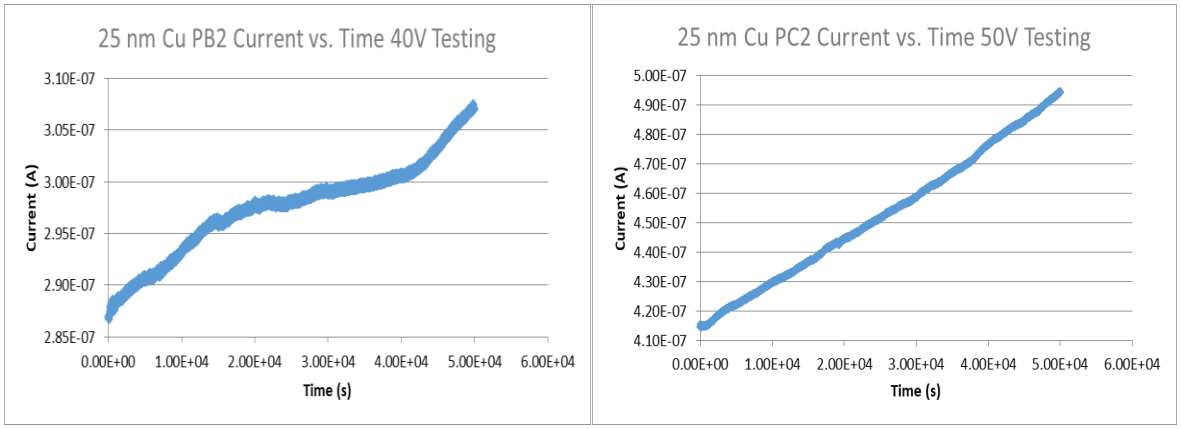
Following are the results for the second row triangular devices, starting with the images before the biasing. Once biased, Figure 17 shows the current versus time data for each device.



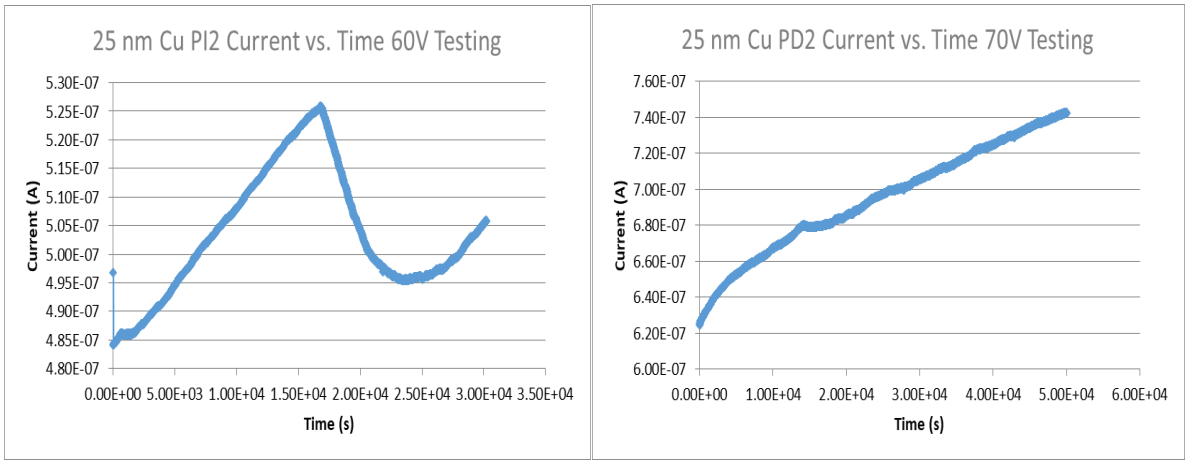
(a) (b)

(c) (d)

Figure 16: Second row triangular device 1000X images prior to testing: (a) PB2, (b) PC2, (c) PI2, and (d) PD2, anode is on the left (regular microscope)



(a) (b)

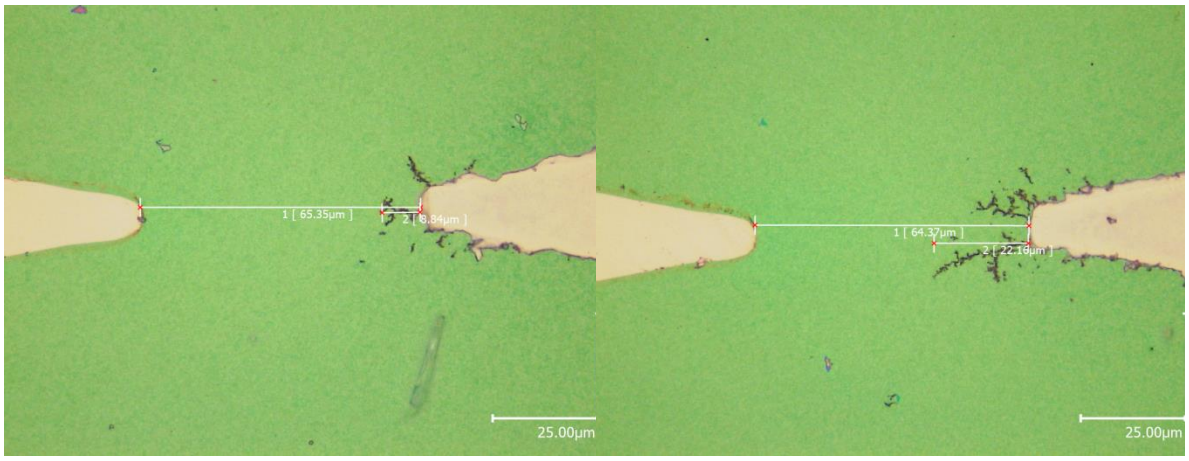


(c) (d)

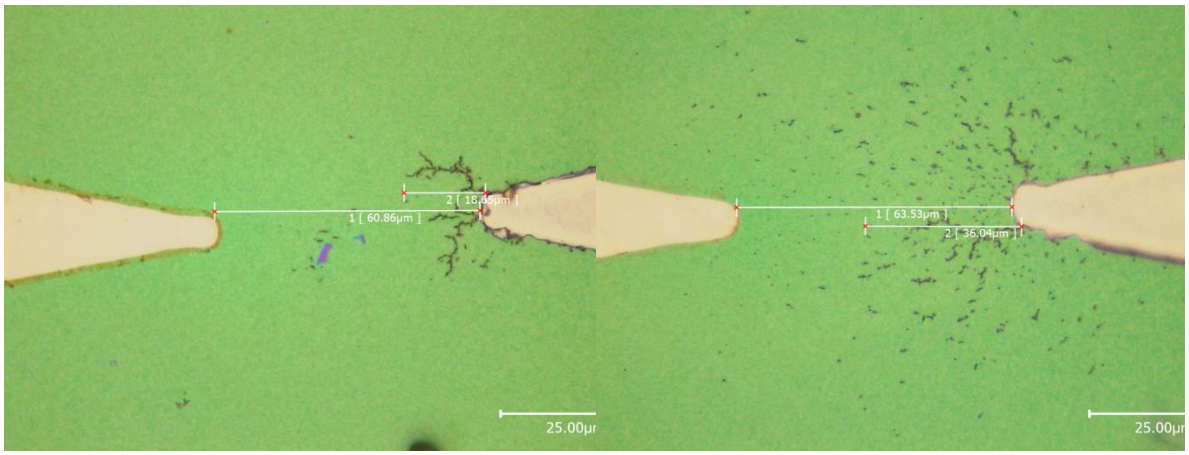
Figure 17: Current versus time graphs for 25 nm second row triangular devices (a) PB2, (b) PC2, and (c) PI2, and (d) PD2

Note, once again, that the current rises over time in all the data in Figure 17. This rise, as stated before, indicates filament growth across the electrolyte. Although PI2 shows an anomalous pattern in current versus time, the current was still rising.

Please see Table 2 for the dendritic growth rates and applied fields. Figure 18 shows the filament growth after the biasing tests were completed on the aforementioned triangular devices.



(a) (b)



(c) (d)

Figure 18: Second row triangular 1000X device images after testing: (a) PB2, (b) PC2, (c) PI2, and (d) PD2, anode is on the left side (regular microscope)

As can be seen in Figure 18, the aforementioned discontinuous growth pattern is seen in device PD2 which has more than 1,000,000 V/m applied to it. Devices PB2, PC2, and PI2 which have lower than 1,000,000 V/m fields applied to them, show more continuous dendritic growth. Table 2 shows the applied fields and the rates.

Device	Electrode Distance (um)	DC Bias Voltage (V)	Applied Field (V/m)	Growth Rate (um/sec)
PB2	66.35	40	602863.6	0.0001768
PC2	64.37	50	7767759.4	0.0004432
PI2	60.86	60	985869.2	0.0006174
PD2	63.53	70	1101842	0.0007208

Table 2: Data for 25um sample second row triangular devices (PB2, PC2, PI2, and PD2)

The discontinuous pattern for PD2, is shown in Figure 18(d). Having observed the patterns in the triangular devices in the first row (PD1-PF1), it is now expected that the discontinuous growth pattern of filaments will be seen in fields above 1e6 V/m, in triangular devices. Further testing will be needed to establish this hypothesis.

Figure 19 shows the graph of the dendritic growth rates versus the applied field. The data is from Table 2.

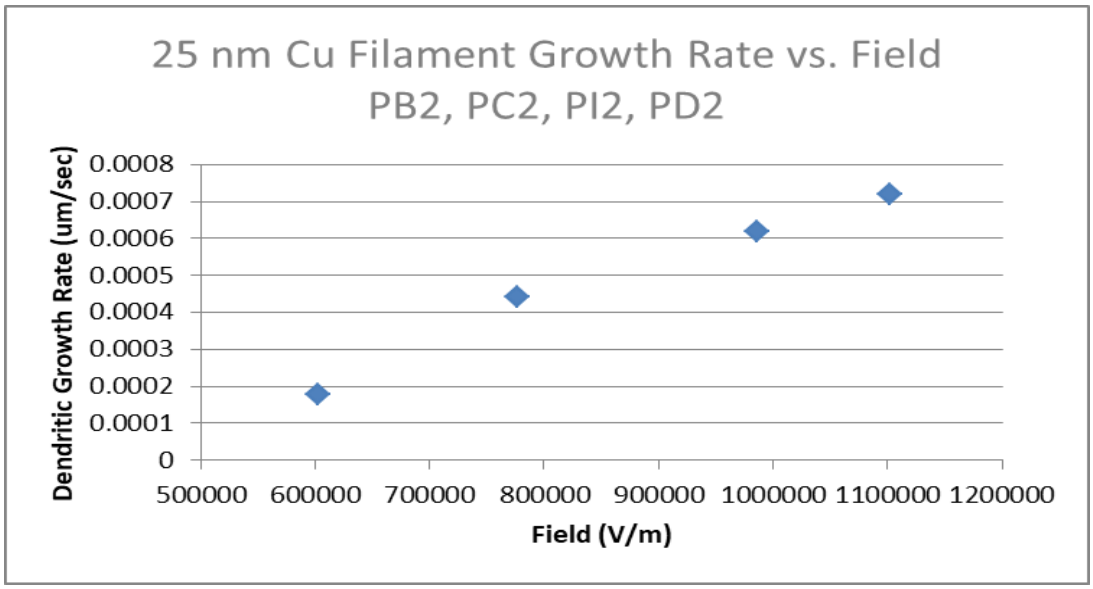


Figure 19: Dendritic rate of growth vs. electric field for PB2, PC2, PI2, and PD2

Again, it can be observed that as the applied field is increased, the filament growth rates increase as well. Once again, the relationship between rates and field is not exponential. There may be a series resistance in the electrolyte that limits ion transport. Further study is required to discern a more precise relationship.

The discontinuous pattern observed in PD1-PF1 as well as PD2, spreads to greater distances than the measured distance. The measurements were taken up to where the majority of the filaments stop according to the microscope. There is a possibility that the filaments traveled the distance between the electrodes. Further testing will be needed to see how far the filaments actually traveled.

The upshot of all of this testing is that increasing filament growth rate is a function of electrode distance and increasing applied field. As will be seen in the 20nm and 30 nm copper sample tests, electrolyte composition also plays a big role in the dendritic growth rate. However, more tests will need to be conducted on more samples to establish a precise correlation.

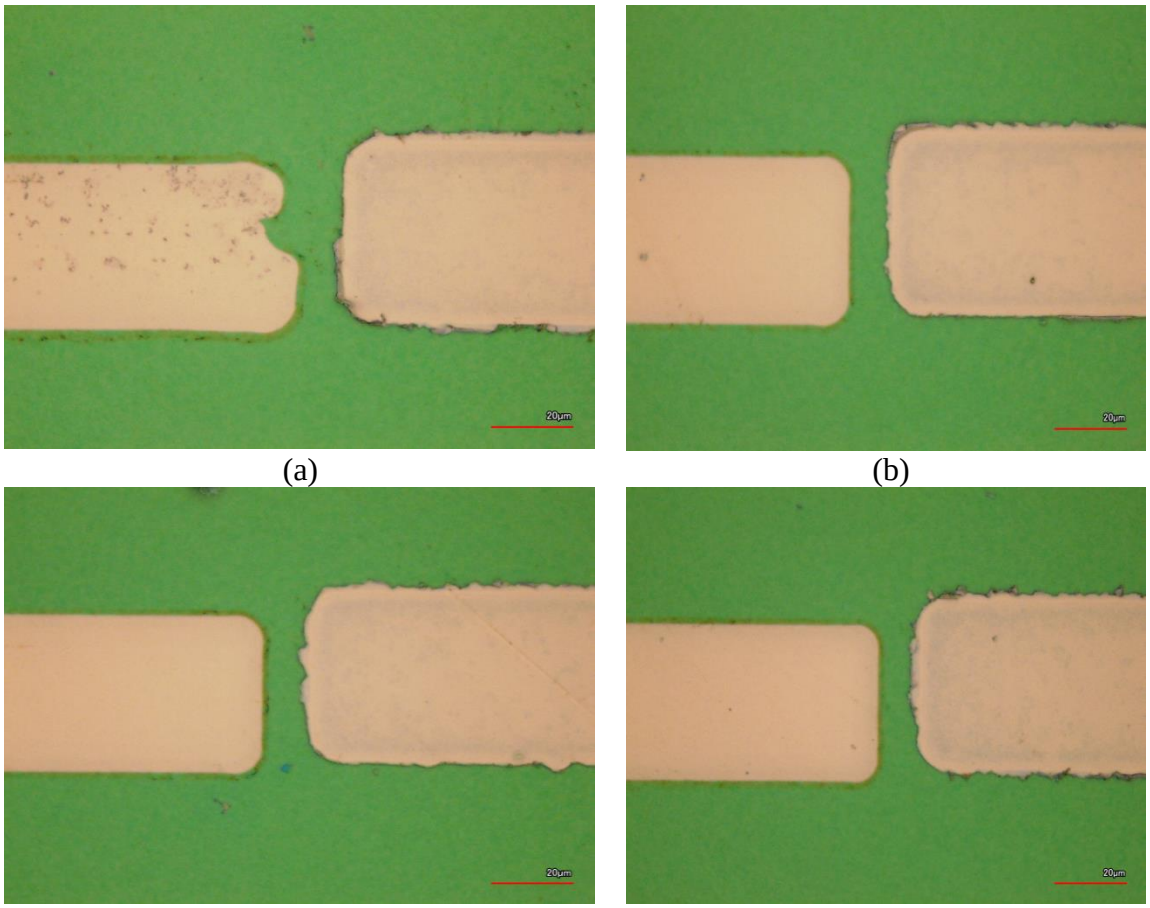
25 NM RECTANGULAR DEVICES

The following rectangular devices were in the first row as usual with an average electrode distance of 10 um. The reason for testing the rectangular devices was to compare the filament growth patterns between the triangular and the rectangular devices. In addition, it was desired to check the growth rate in these devices as well. These devices were tested for the aforementioned purposes:

Rectangular Devices

- EG1 (at 40V for 4250 seconds)
- EH1 (at 30V for 4870 seconds)
- EI1 (at 20V for 4860 seconds)
- EJ1 (at 10V for 16000 seconds)

The rectangular devices averaged a distance of approximately 10 um from cathode to anode. Considering these small distances and greater electrode cross section (relative to the triangular devices), lower voltages (hence fields) were used to test these rectangular devices. It is also worthy of noting that for device EA1 20V was all that was required for shorting.



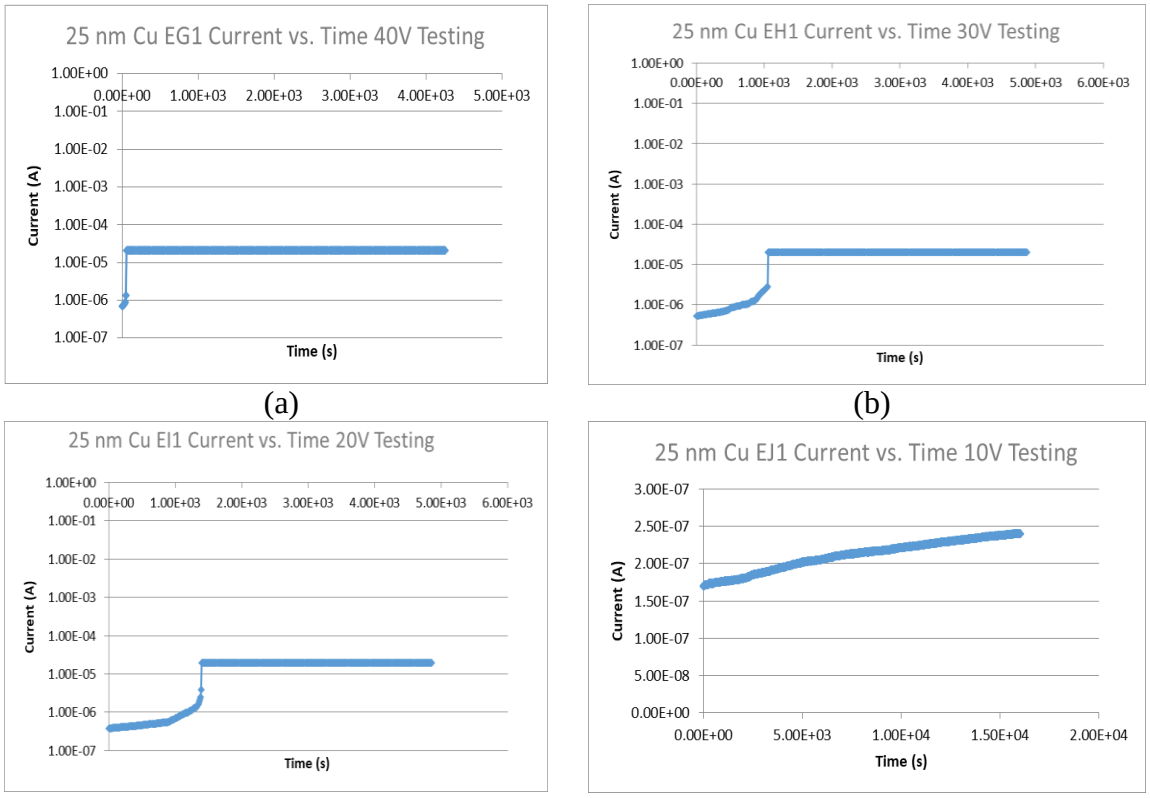
(a) (b)

(c) (d)

Figure 20: Rectangular device 1000X images prior to testing: (a) EG1, (b) EH1, (c) EI1, and (d) EJ1, anode is on the left side (regular microscope)

Following is the current versus time data for the tested rectangular devices. Please see

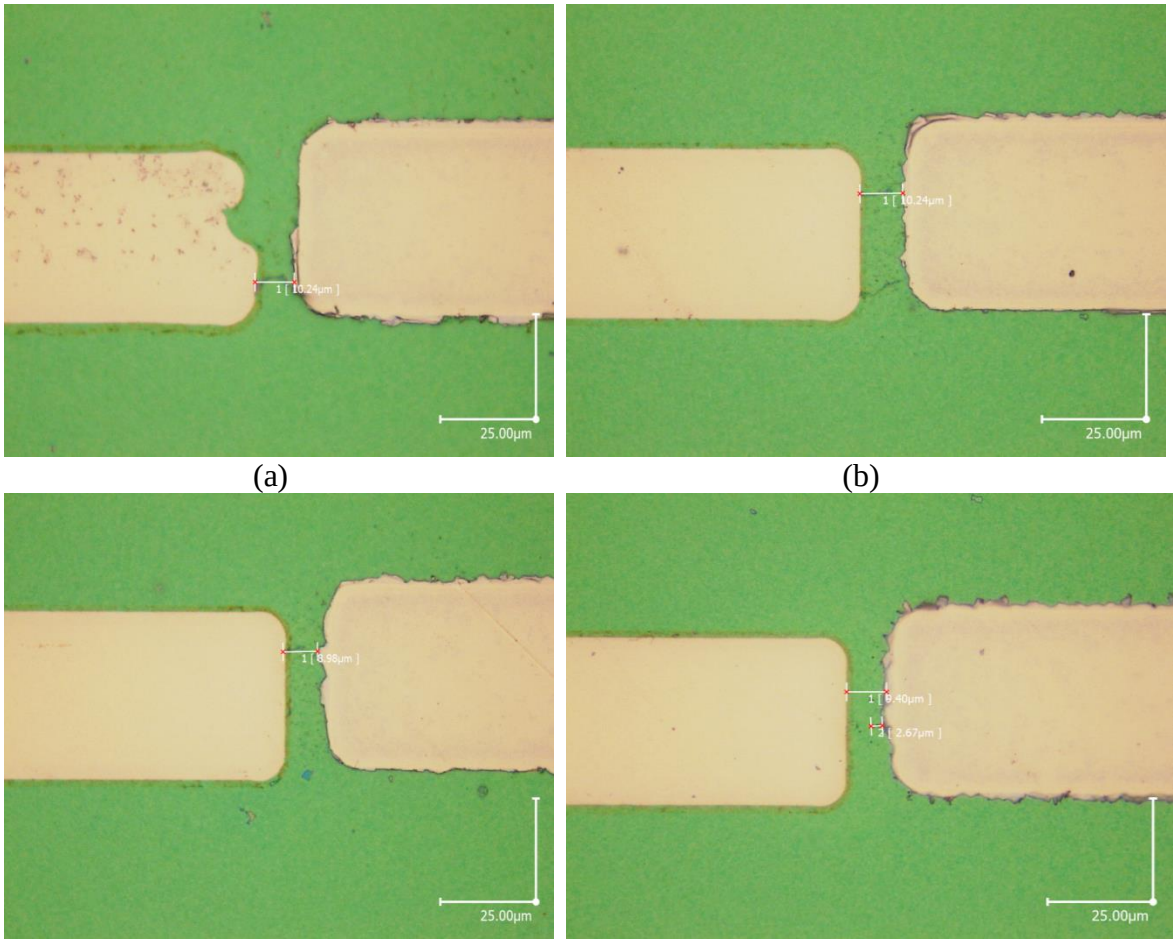
Table 3 for the applied fields and rates.



(a) (b) (c) (d)

Figure 21: Current versus time graphs for 25 nm first row rectangular devices (a) EG1, (b) EH1, and (c) EI1, and (d) EJ1

As shown in Figure 21, EG1, EH1, and EI1 completely shorted out. The current rose and then spiked to the compliance current of 2e-5 A. The rising current, once again, indicates filament growth and the spike in current (as in the proof of concept tests) indicates shorting of the devices. EG1 (Figure 25(a)) was tested for 4250 seconds, but shorted out at 50 seconds. This means that the filament traveled 10.24 um in 50 seconds. EH1 (Figure 25(b)) was tested for 4270 seconds and shorted at 1060 seconds. EI1 (Figure 25(c)) was tested for 4260 seconds and shorted at 1400 seconds. EJ1 was tested for 16000 seconds and never shorted out. The filament grew 2.67 um in that time. Figure 22 shows the rectangular devices after testing.



(a) (b)

(c) (d)

Figure 22: Rectangular device 1000X images after testing: (a) EG1, (b) EH1, (c) EI1, and (d) EJ1, anode is on the left side (regular microscope)

As can be seen from Figure 22, the devices were, indeed shorted out. However, the discontinuous growth pattern seen in the triangular devices is not observed here. In fact, a straight continuous filament is seen. In the rectangular devices, only one filament wins the dendritic growth "race". Filaments that may grow on other areas will stop their growth once the winning filament grows long.

The following figure shows the graph of the dendritic growth rates versus the applied field. The applied fields and rates are shown in Table 3 and the graph of the rates versus the fields is shown in Figure 23.

Device	Electrode Distance (um)	DC Bias Voltage (V)	Applied Field (V/m)	Growth Rate (um/sec)
EJ1	9.4	10	1063830	0.000167
EI1	8.9	20	2247191	0.00636
EH1	10.24	30	2929688	0.00966
EG1	10.24	40	3906250	0.205

Table 3: Data for 25um sample first row rectangular devices (EJ1, EI1, EJ1, and EG1)

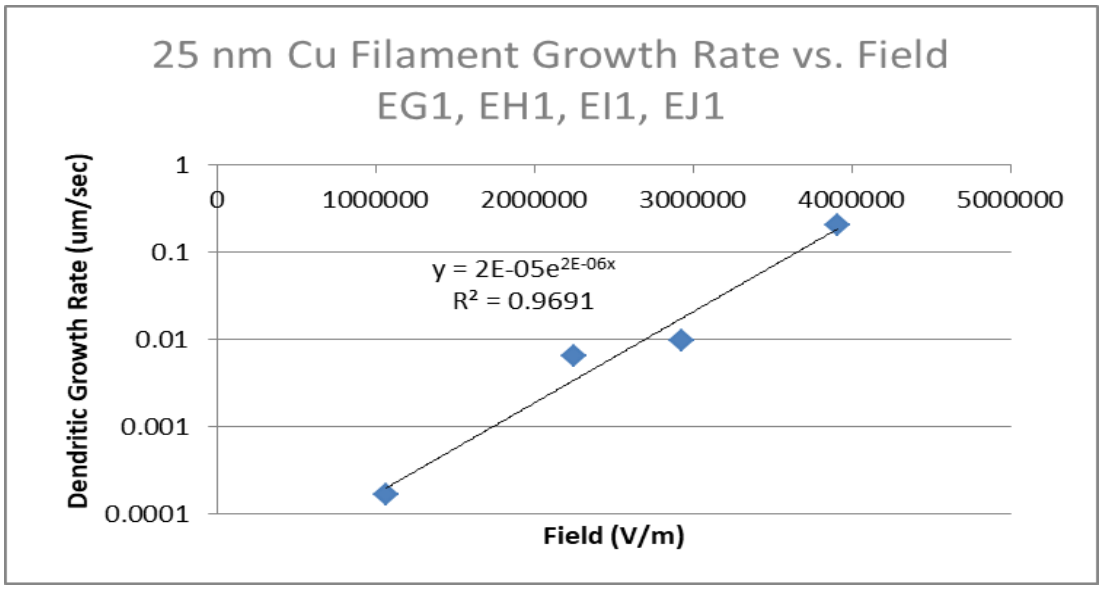


Figure 23: Dendritic rate of growth vs. electric field for EG1, EH1, EI1, and EJ1

Figure 23 shows the expected exponential relationship between growth rate and field. Note that the growth rate axis is now in the logarithmic scale as opposed to the linear scale of Figures 15 and 19. As stated before, it can be said in the case of the 25nm copper sample tests, without loss of generality, that the closer the electrode distance and the higher the applied field, the faster the filament growth rate will be. More tests will be required to improve on the precision of that relationship.

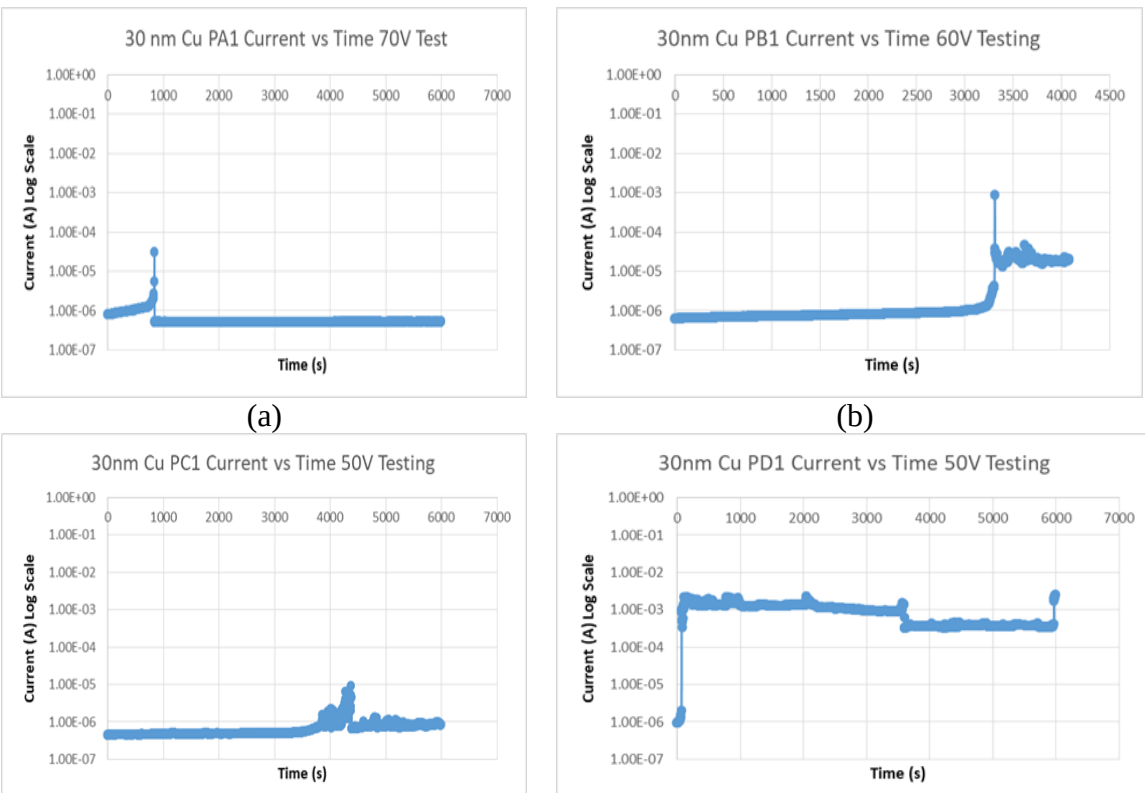
30 NM TRIANGULAR DEVICES

After the 25 nm copper sample tests were completed, the 30nm copper sample tests were performed. The following set of results is for the 30 nm copper sample. The devices tested are the following for checking filament growth rates:

Triangular Devices

- PA1 tested at 70V for 6000 seconds
- PB1 tested at 60V for 4090 seconds
- PC1 tested at 50V for 6000 seconds
- PD1 tested at 50V for 6000 seconds

Following are the current versus time graphs for the triangular devices. Please see Table 4 for the rates and the applied fields.



(a) (b) (c) (d)

Figure 24: Current versus time graphs for 30 nm first row triangular devices (a) PA1, (b) PB1, and (c) PC1, and (d) PD1

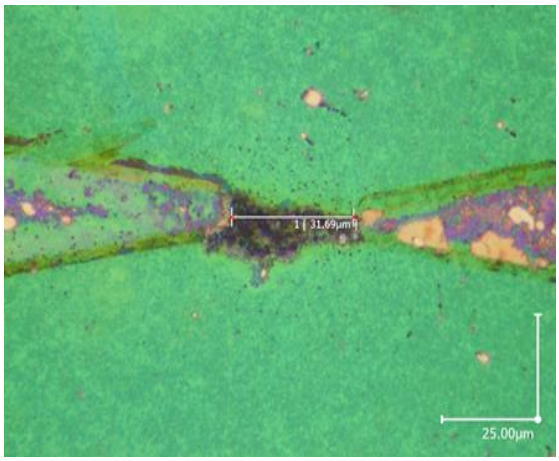
PA1 was biased at 70 for 6000 seconds. As shown in Figure 24(a), the device shorted out at 840 seconds. This means that the filaments traveled 31.69 um in 840 seconds.

The second triangular device tested on this 30 nm sample was triangular device PB1. This device was tested at 60V for 4090 seconds as shown in Figure 24(b). Device shorted out at 3310 seconds, which means the filaments traveled 34.08 um in that time.

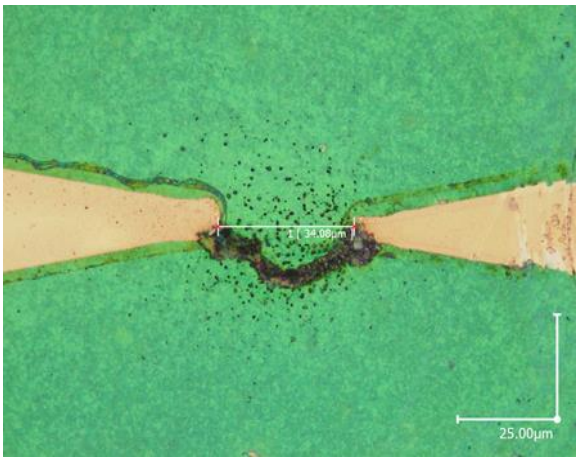
PC1 was tested at 50V for 6000 seconds. Although the dendrites appear to have traveled only 15.15 um as shown in Figure 25(c), the device shorted out to 33.66 um at 4380 seconds as shown in Figure 24(c).

PD1 was tested at 50V for 6000 seconds. Device shorted out at 72 seconds as shown in Figure 24(d). Device PD1 shorted out quickly compared to the other triangular devices in this group.

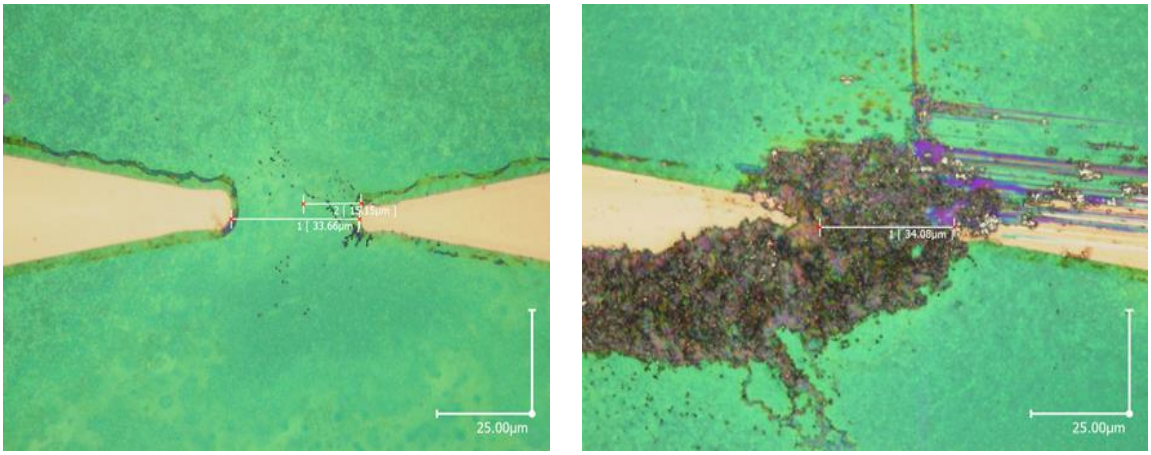
Figure 25 shows the filament growths after the tests.



(a)



(b)



(c) (d)

Figure 25: First row triangular device 1000X images after testing: (a) PA1, (b) PB1, (c) PC1, and (d) PD1, anode is on the left side (regular microscope)

Figure 25(a) and 25(b) clearly shows the filaments shorting the devices (PA1 and PB1) as confirmed by the corresponding current versus time graphs. Around the shorting filament the discontinuous island pattern that is expected of fields higher than 1,000,000 V/m can be seen. Figure 25(c) for PC1, does not show the shorting that one would expect from observing the current spike shown in Figure 24(c). The dendrites do grow discontinuously and the visible dendrites go to 15.15 um but the device is shorted. A possible reason for this is the high field as shown in Table 4 and the higher amount of copper in the electrolyte.

Since PD1 shorted out very quickly, it is not included in the graph in Figure 26 and the data in Table 4. The higher amount of copper and the non-uniformity of copper distribution is the reason for this as will be confirmed in later tests. As shown in Figure 25(d), though the device shorted quickly, there are a lot of copper islands around the shorting filament. For devices PA1-PC1, the relationship between filament growth rate and field is exponential. Following are the fields and growth rates for PA1, PB1, and PC1.

Device	Electrode Distance (um)	DC Bias Voltage (V)	Applied Field (V/m)	Growth Rate (um/sec)
PC1	33.66	50	1485442.66	0.007685
PB1	34.08	60	1760563.38	0.0103
PA1	31.69	70	2208898.71	0.0377

Table 4: Data for 25um sample first row triangular devices (PA1, PB1, PC1)

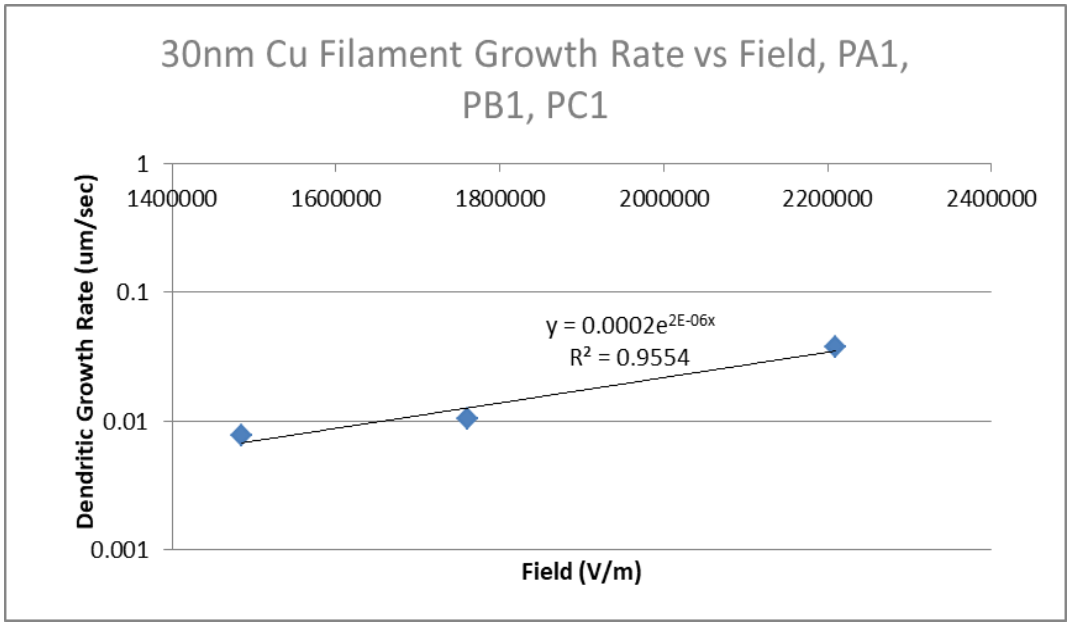


Figure 26: Dendritic rate of growth vs. Electric Field for first row triangular devices PA1, PB1, and PC1

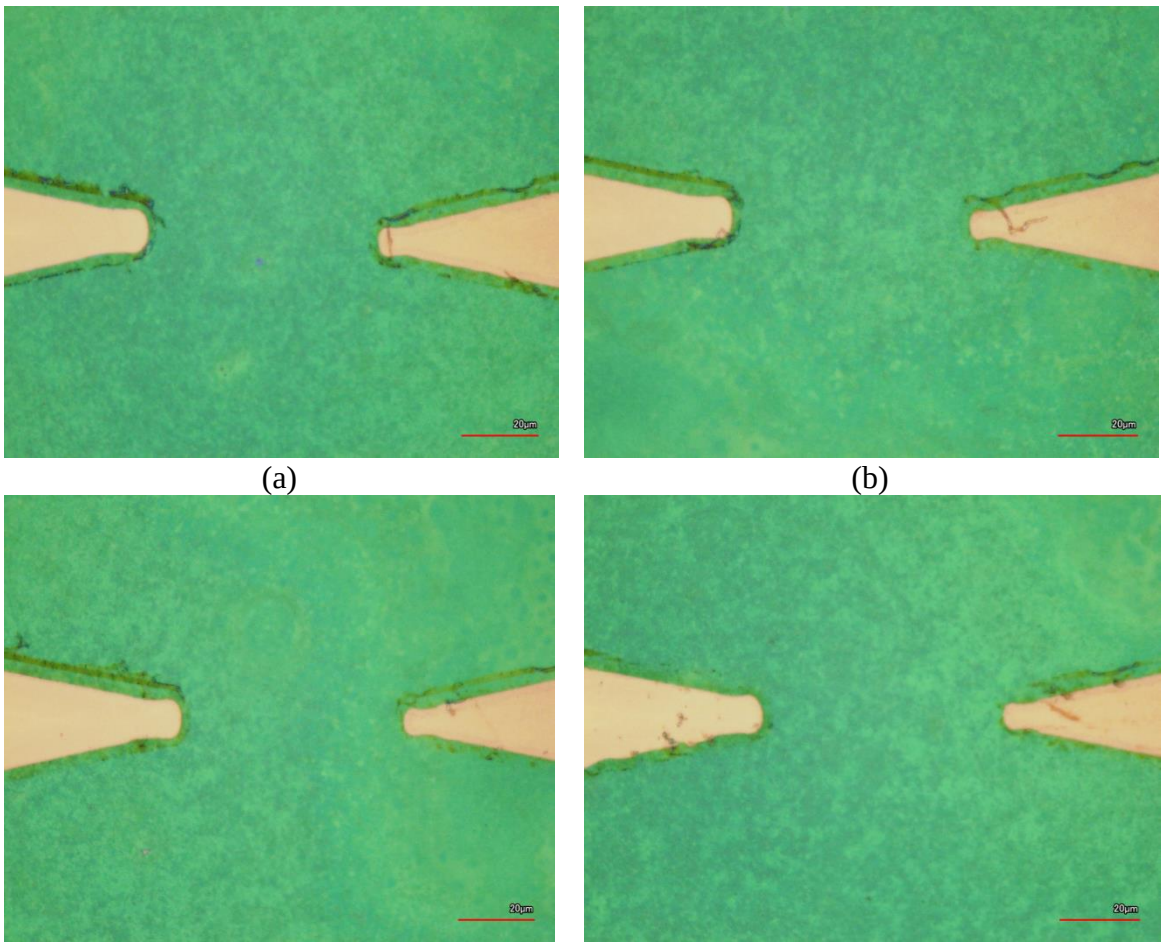
Figure 26 also shows the expected exponential relationship between growth rate and field. Once again, note that the growth rate axis is now in the logarithmic scale as opposed to the linear scale. More tests are required to confirm this relationship. Additionally comparing the rates from Table 4 to the equivalent 25nm samples in Table 1, the expected result of the rates being faster in the 30 nm devices can be observed. With more copper in the 30 nm sample, the dendritic growth rates should be faster and in this case, they are.

In order to confirm the exponential relationship in the 30 nm sample, more tests were performed on triangular devices. The second row triangular devices were chosen for lower applied fields. The following devices were tested in the 30 nm sample:

Triangular Devices Tested

- PA2 (at 40V for 50000 seconds)
- PC2 (at 50V for 50000 seconds)
- PE2 (at 60V for 50000 seconds)
- PF2 (at 70V for 50000 seconds)

These triangular devices averaged a 59 um distance from cathode to anode. They did not have the same problem as the later tested rectangular devices in terms of shorting very quickly. This may be due to the greater distance from cathode to anode. Figure 27 shows the images of the triangular devices mentioned above.



(a) (b)

(c) (d)

Figure 27: Second row Triangular device 1000X images prior to testing: (a) PA2, (b) PC2, (c) PE2, and (d) PF2, anode is on the left side (regular microscope)

Following is the test data for the pointed devices in the 30nm sample. All these devices were tested for 50000 seconds. As always, the rising current indicates that the filaments are growing. Again, these devices were not shorted. Please see Table 5 for the applied fields and growth rates.

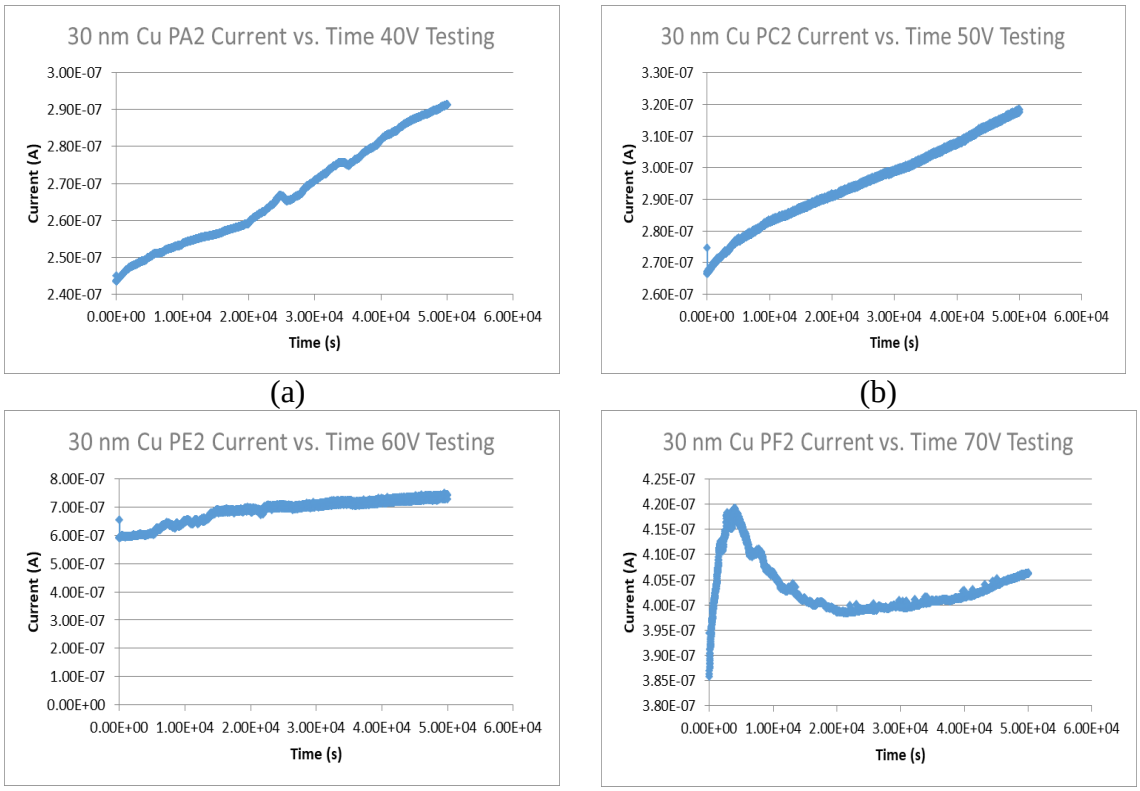
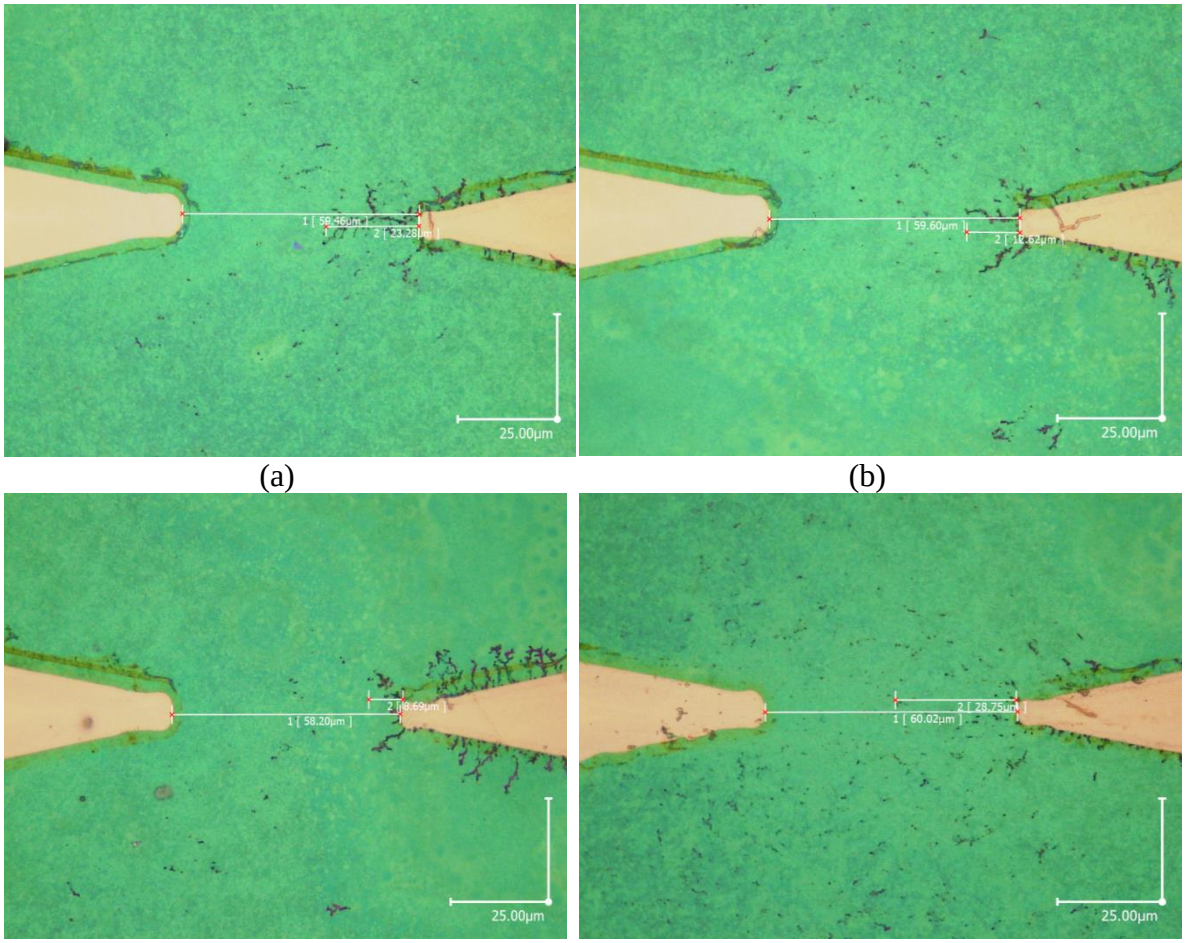


Figure 28: Current versus time graphs for 30 nm second row triangular devices: (a) PA2, (b) PC2, (c) PE2, and (d) PF2

Here are images of the 30nm triangular devices after the tests were performed:



(a) (b)

(c) (d)

Figure 29: Second row triangular device 1000X images after testing: (a) PA2, (b) PC2, (c) PE2, and (d) PF2, anode is on the left side (regular microscope)

In this case, as shown in Figure 29, the discontinuous growth pattern is seen on all the tested devices in the 30 nm sample. In the lower fields, the dendrites start off growing solidly, but then they start to split off as they continue growing. PF2, which has the highest applied field, starts off growing in a discontinuous manner. The applied fields and filament growth rates for this set of triangular devices are shown in Table 5.

Device	Electrode Distance (um)	DC Bias Voltage (V)	Applied Field (V/m)	Growth Rate (um/sec)
PA2	59.46	40	672721.16	0.000466
PC2	59.60	50	838926.17	0.000252
PE2	58.20	60	1030927.84	0.000174
PF2	60.02	70	1166277.91	0.000575

Table 5: Data for 25um sample second row triangular devices (PA2, PC2, PE2, PF2)

The discontinuous growth island pattern in the 25 nm sample occurs in fields above a million V/m. In the 30 nm sample, however, the same pattern occurs in all the tested devices. This morphology of dendritic growth may be due to the extra copper in the electrolyte relative to the 25 nm sample. As mentioned in the section describing the tests of the corresponding triangular devices in the 25 nm sample, the dendrites have grown more than what appears in the microscope images. Further testing will be required.

When comparing the correpsonding devices from Table 2, the rates of filament growth are comparable and sometimes less in the 30 nm sample. Generally, the rates for higher copper in the electrolyte are faster, however, in this case they are not. This may be due to the non-uniformity of copper distribution in the electrolyte. Further processing and testing will be required.

Figure 30 shows the graph of the dendritic growth rates versus the applied field.

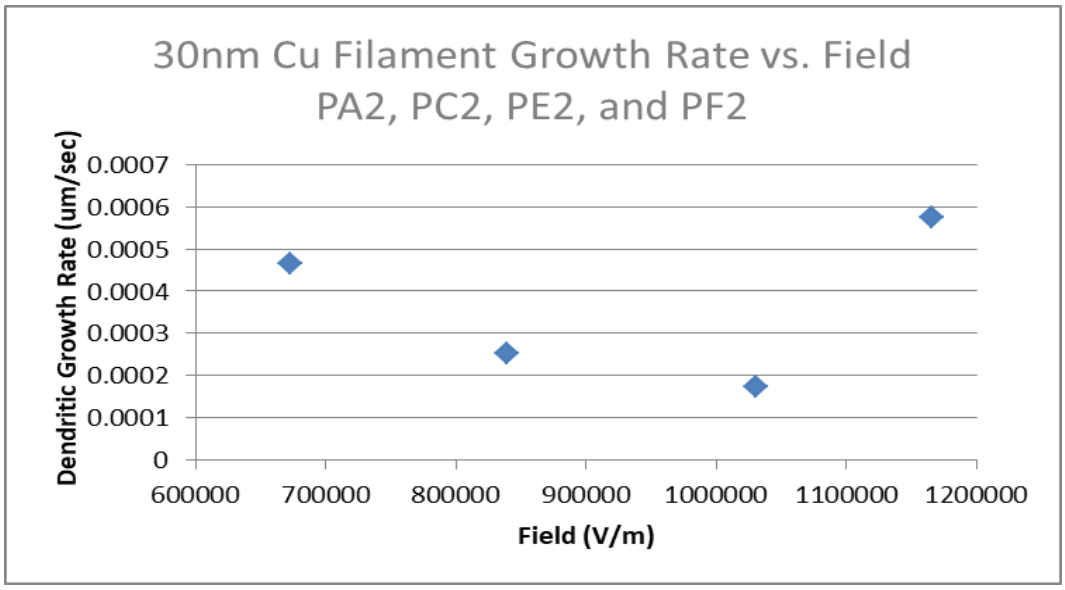


Figure 30: Dendritic rate of growth vs. Electric Field for triangular devices PA2, PC2, PE2, and PF2

Figure 30 shows no distinct pattern in the relationship between growth rate and field. Once again, an exponential relationship is expected between the rates and the fields with electrolyte composition being held constant. However, that was not the case here. The rates were comparable to the 25 nm corresponding triangular devices and the relationship was not exponential. Why would the rates, in some cases, go down with increasing field? This can only be attributed to the non-uniformity of copper in the electrolyte. Further study is warranted here.

A future course of action would be to deposit 30 nm of copper on 100 nm of WO_3 and heat it at different times and different temperatures (using a design of experiments). Inspect these samples under the microscope after heating and take 4-point probe measurements. Then deposit the electrodes and test for the dendritic growth rate. The idea for this experiment is to find out what it takes for expected dendritic growth behavior to occur in the 30 nm sample.

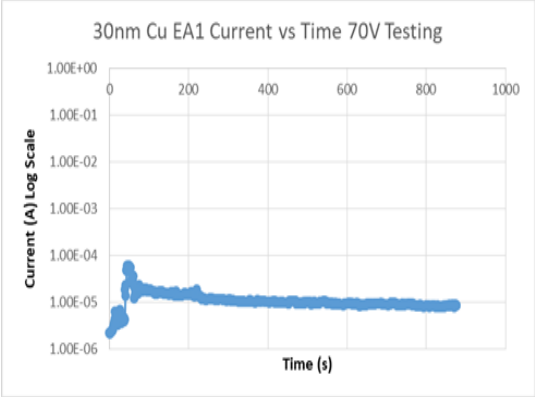
30 NM RECTANGULAR DEVICES

Following are the rectangular devices tested in the 30 nm sample:

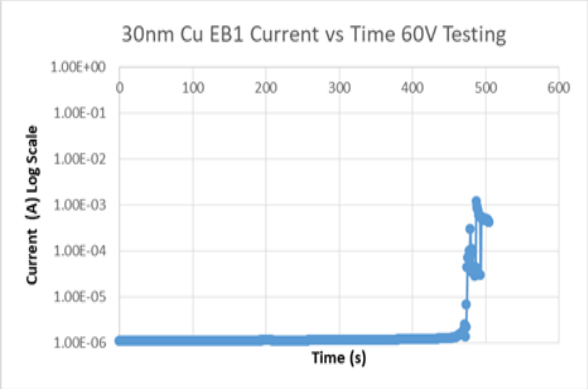
- EA1 tested at 70V for 877 seconds
- EB1 tested at 60V for 505 seconds
- EC1 tested at 60V for 138 seconds
- EG1 tested at 50V for 1200 seconds
- EJ1 tested at 50V for 1200 seconds
- EF1 tested at 10V for 50000 seconds

The distance from cathode to anode on these devices, is on average 10 um. The devices were shorted very quickly relative to the triangular devices and relative to the corresponding rectangular devices for the 25 nm copper sample. The growth rates showed no particular pattern when related to the electric field. The quick shorting of the devices is due to the higher amount of copper in the electrolyte for that location, in combination with the short distance between the electrodes.

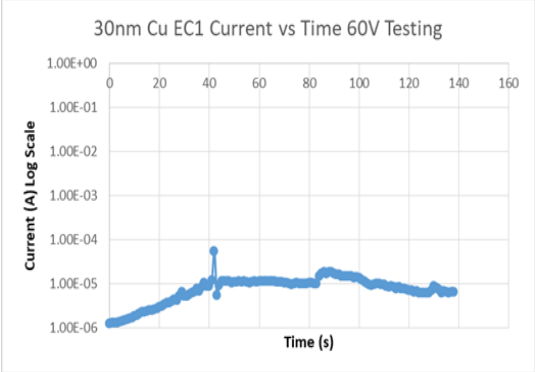
Figure 31 shows the current versus time graphs for EA1, EB1, and EC1.



(a)



(b)



(c)

Figure 31: Current versus time graphs for 30 nm first row rectangular devices: (a) EA1, (b) EB1, (c) EC1

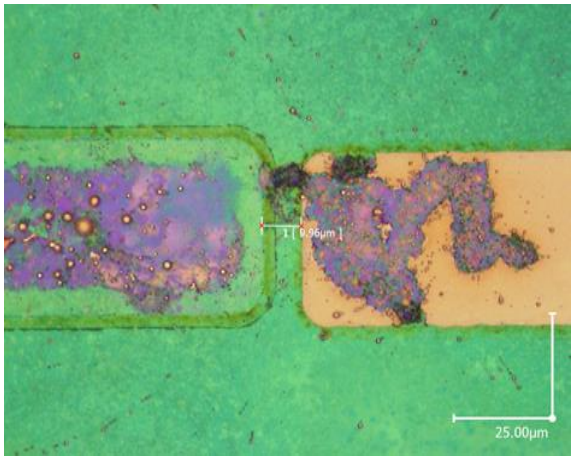
Please refer to Table 6 for the rates and applied fields for the rectangular devices. EA1 was biased at 70V. Device shorted out at 44 seconds, which means the filaments traveled

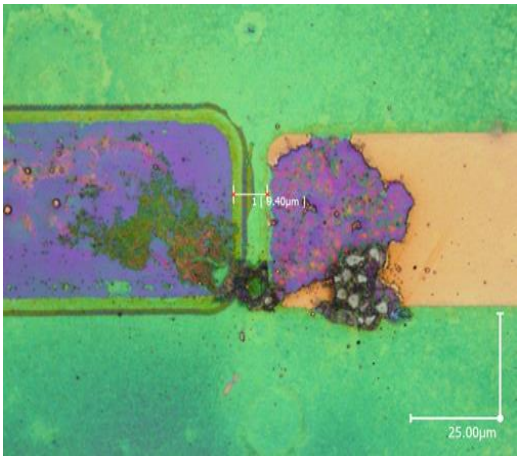
9.96 um in that time. This quick shorting out of the device is likely due to a higher supply of copper in this area and the cathode to anode distance is a lot smaller at the 9.96 um shown in Figure 32(a).

The second rectangular device tested was EB1. It was biased at 60 V for 505 seconds and shorted at 474 seconds as shown in Figure 31(b). This means that the filaments traveled 9.4 um in the time it took to short the device.

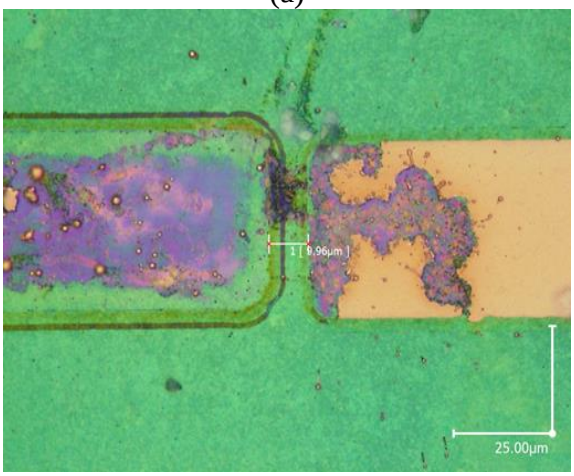
Due to the short time it took for the filaments to travel from cathode to anode, a second rectangular device EC1 was biased at 60V for 138 seconds. The device shorted at 42 seconds which means the filaments traveled 9.96 um in that time. The non-uniform distribution of copper in this sample is the likely cause of this quick growth.

Figure 32 shows the images for EA1, EB1, and EC1 after the devices were tested.





(a) (b)

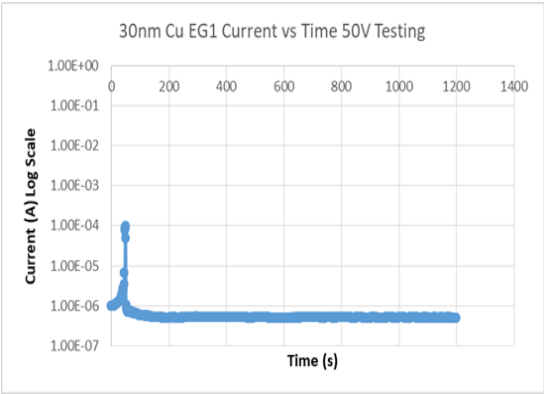


(c)

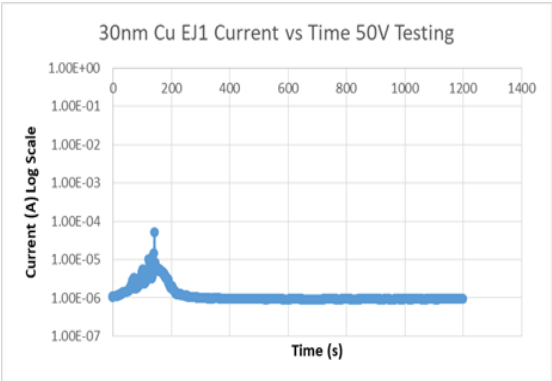
Figure 32: First row rectangular device images after testing: (a) EA1, (b) EB1, and (c) EC1, anode is on the left side (regular microscope)

As can be seen in these tested devices there are one or two filaments grow from cathode to anode. EA1 which is shown in Figure 32(a) shows the filament shorting the device. Between and around the device there are a lot of copper islands. The non-uniform distribution of copper was especially prevalent in the location of these rectangular devices. EB1 and EC1, show a similar pattern likely due to the high field and excess copper at this location.

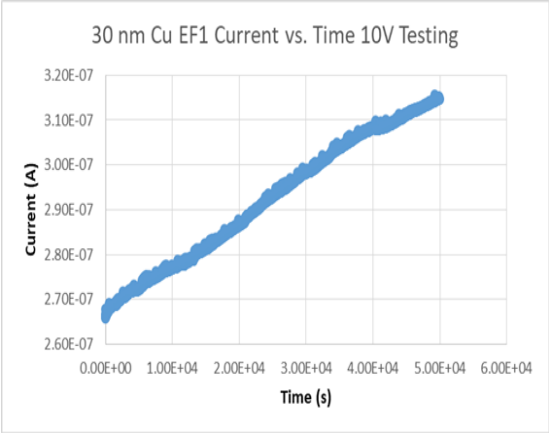
Figure 33 shows current versus time data for the rest of the tested devices in this row, EG1, EJ1, and EF1.



(a)



(b)



(c)

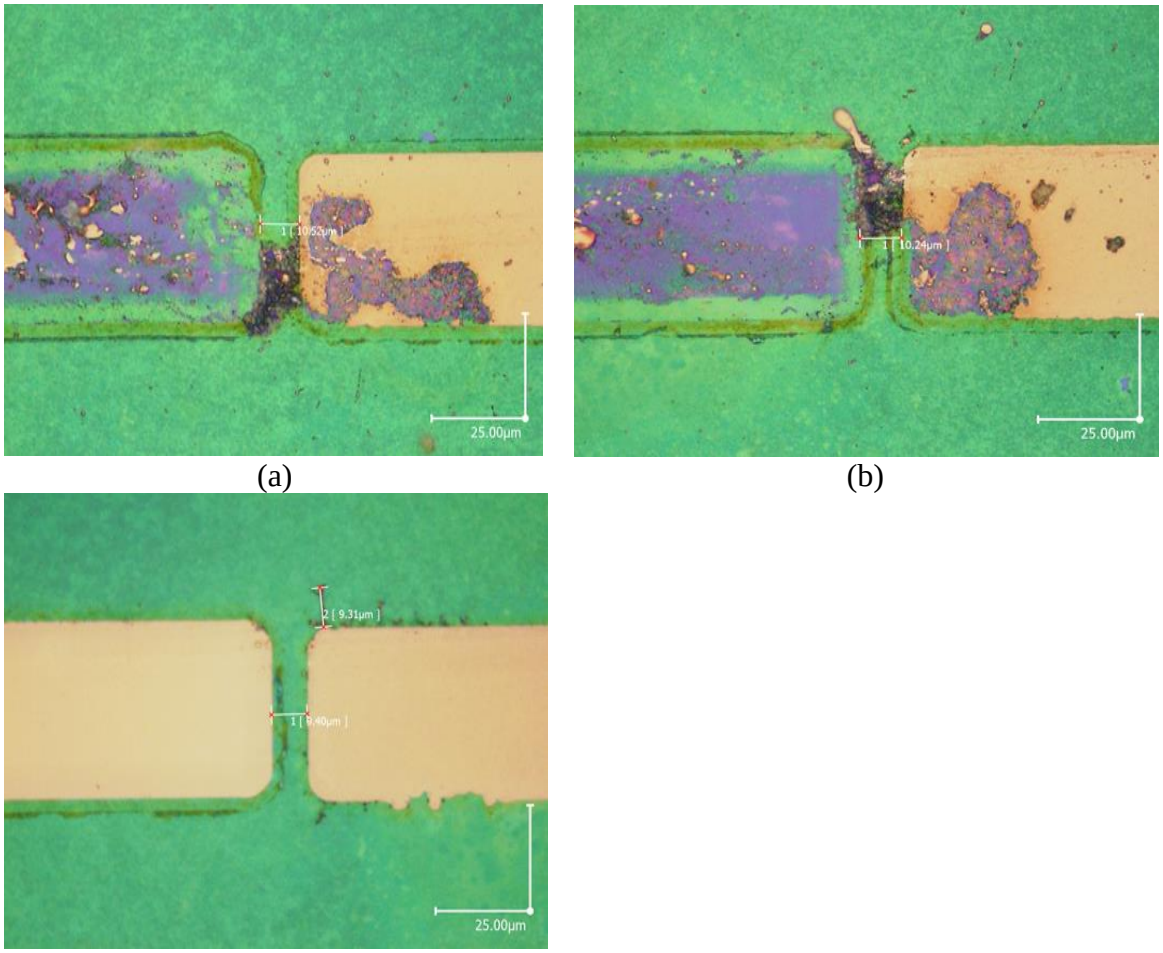
Figure 33: Current versus time graphs for 30 nm first row rectangular devices: (a) EG1, (b) EJ1, (c) EF1

EG1 was biased at 50 V for 1200 seconds and shorted at 51 seconds as shown in Figure 33(a). This device was another that shorted out very quickly even with a lower bias compared to device EA1-EC1. Once again, the non-uniform distribution of copper and the excess copper at this location likely caused the rate of growth to be very fast.

EJ1 was biased at 50 V for 1200 seconds and shorted at 142 seconds as shown in Figure 33(b). This was a repeat test to see if a slower dendritic growth rate could be obtained under the same DC bias conditions. However, the rate of growth was still very fast relative to the equivalent 25 nm sample rectangular device.

EF1 was biased at 10Vfor 50000 seconds. This lower field was applied because of the smaller distances between electrodes and so that shorting does not occur too quickly as it did in the aforementioned devices. The device never shorted out as seen in Figure 33(c).

Figure 34 shows the filament growth images for EG1, EJ1, and EF1.



(a) (b)

(c)

Figure 34: First row rectangular device 1000X images after testing: (a) EG1, (b) EJ1, (c) EF1, anode is on the left side (regular microscope)

EG1 and EJ1 shown in Figure 34(a) and 34(b) show the standard filament growth shorting the devices. There are some islands of copper between and around the device. Again, this is likely due to the distribution of copper in this area. EF1, which is shown in Figure 34(c), did not short out as confirmed in Figure 33(c). The image shows that the dendrite did not grow between the electrodes as expected. Further study and processing is required, however, it is likely that in this area, copper distribution is non-uniform and excessive in certain places.

It is worthy of note that the rest of the rectangular devices in this row went to compliance current almost immediately after biasing. This means that the devices were already shorted by a path of metallic copper. Once again, this shows the non-uniformity of the copper distribution for this sample. Making another sample and testing it along with further study is required.

The relationship between the dendritic growth rates versus the field is shown in Figure 35. Table 6 shows the fields and rates of filament growth for each of the rectangular devices:

Device	Electrode Distance (um)	DC Bias Voltage (V)	Applied Field (V/m)	Growth Rate (um/sec)
EF1	9.40	10	1063829.79	0.000186
EJ1	10.24	50	4882812.50	0.0721
EG1	10.52	50	4752851.71	0.206
EC1	9.96	60	6024096.39	0.237
EB1	9.4	60	6381978.72	0.019
EA1	9.96	70	7028112.45	0.226

Table 6: Data for 30 um sample first row rectangular devices (EF1, EJ1, EG1, EC1, EB1, EA1)

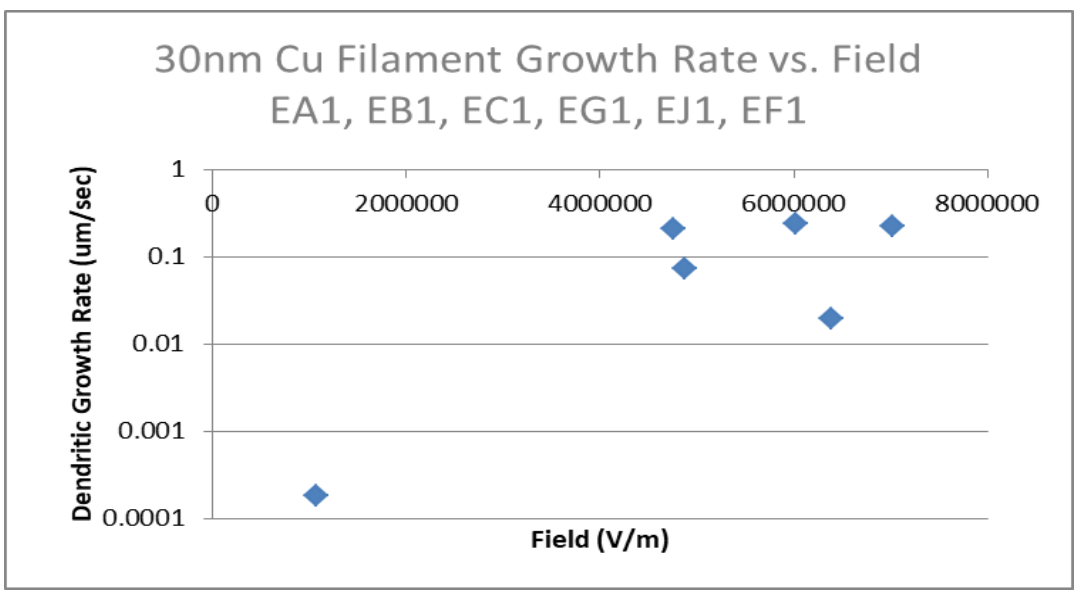


Figure 35: Dendritic rate of growth vs. Electric Field for rectangular devices EA1, EB1, EC1, EG1, EJ1, and EF1

As shown in Figure 35, there is no set pattern in the relationship between dendritic growth rate and applied field. EB1, EC1, and EG1 skew the results for the pattern. Why would this be the case? This is likely due to the amount of metallic copper in the electrolyte in the vicinity of those devices. The 30 nm copper sample is shown to be dirtier than the 20 nm and 25 nm samples when comparing Figure 4 to 6. The deposition and annealing of this sample likely lead to a non-uniform distribution of copper in the electrolyte matrix. Hence, the rates are varied. As stated before, some of the rectangular devices in the same row reached compliance current immediately, indicating enough metallic copper to short the device. In these cases, the bias amount did not matter. Even at 5V the devices reached compliance.

Generally comparing Table 6 (30 nm rectangular devices) to Table 3 (25 nm rectangular devices), the rates at 50 to 70V bias were much faster as expected. More uniform copper distribution and further study of those samples is needed to establish a more precise relationship between amount of copper in the electrolyte and the dendritic growth.

20 NM SAMPLE TRIANGULAR DEVICES

The 20 nm copper sample had only two triangular devices tested. PF1 was biased at 70V for 861,540 seconds and PG1 was biased at 80V for 100,000 seconds.

Figure 36 shows the graph for the final 262,644 seconds

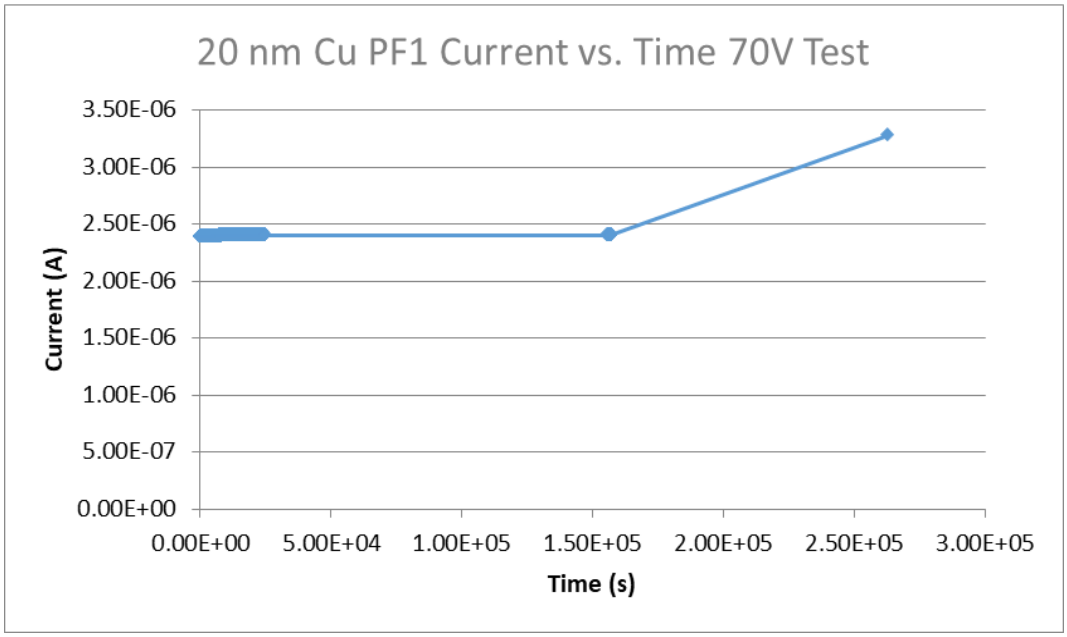


Figure 36: Final 262,644 seconds of PF1 70V test

As seen in Figure 36, the current is rising, indicating filament growth. This growth is shown in Figure 37.

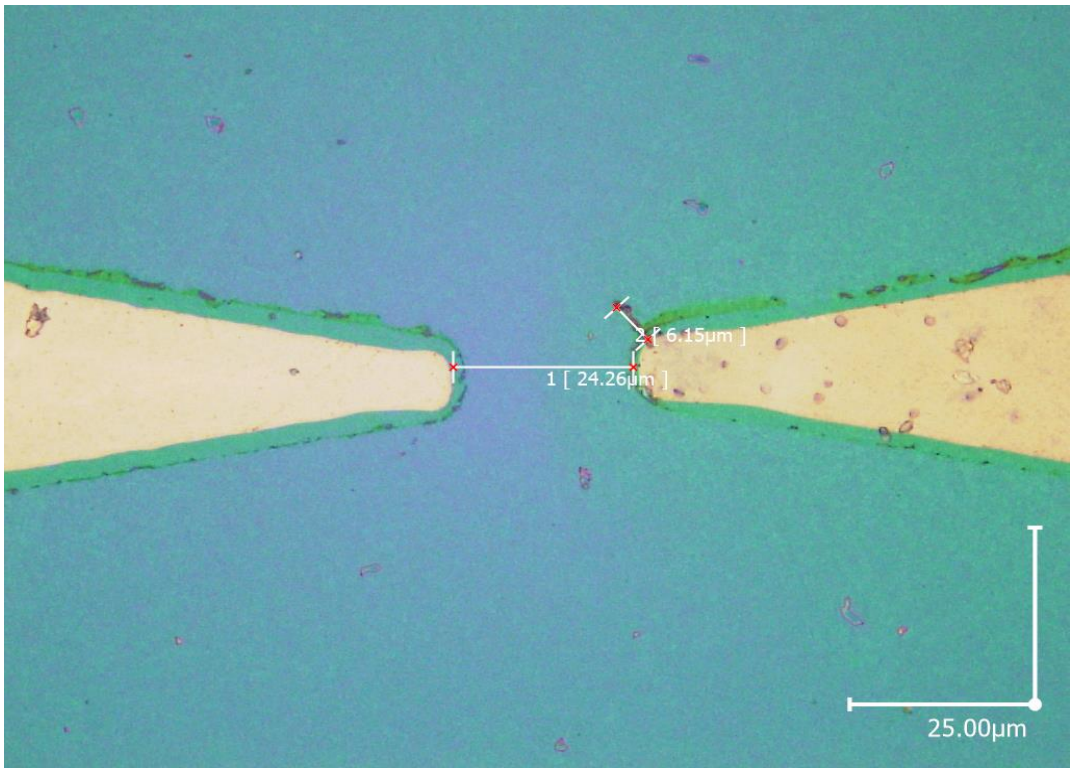


Figure 37: 1000X image for device PF1 in the 20 nm Cu sample taken after the 70V 861,540 second test, anode on the left side

As shown in Figure 37, it took the dendrite 861,540 seconds to grow 6.15 um, which gives a rate of 7.134e-6 um/sec. This is an extremely slow rate for a 70V bias, which is a field of 2885408.08 V/m. This slowness in the filament growth is the reason only two devices were tested for this sample.

The second device tested was PG1 at 80V which is a field of 3223207.1 V/m. The bias time was 100,000 seconds. Figure 38 shows the last 50000 seconds of the test. The current shows a slight rise over time, again, indicating filament growth which is shown in Figure 39.

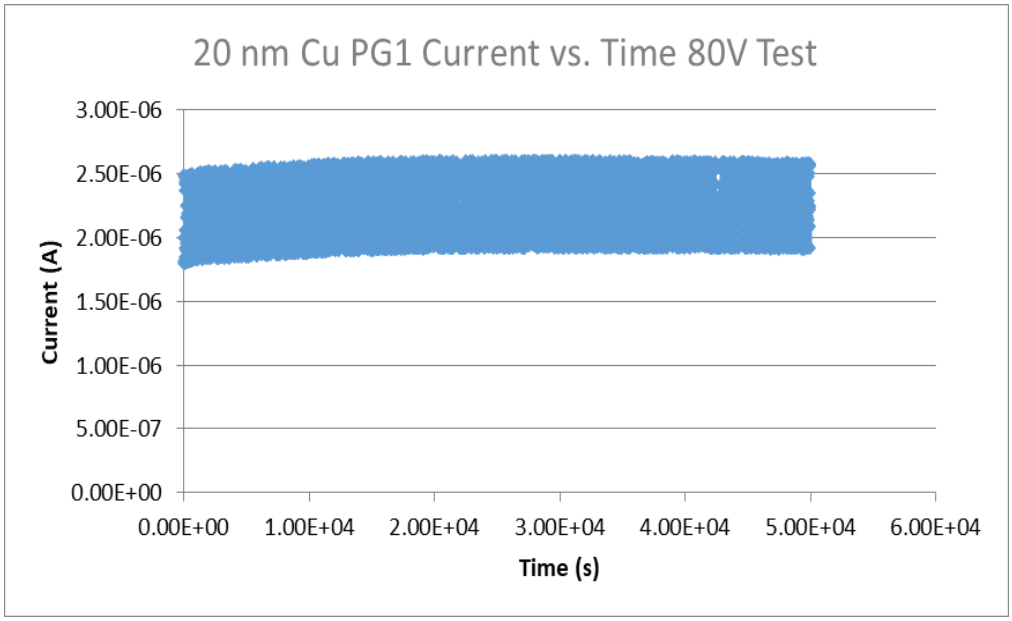


Figure 38: Final 50000 seconds of PG1 80V test

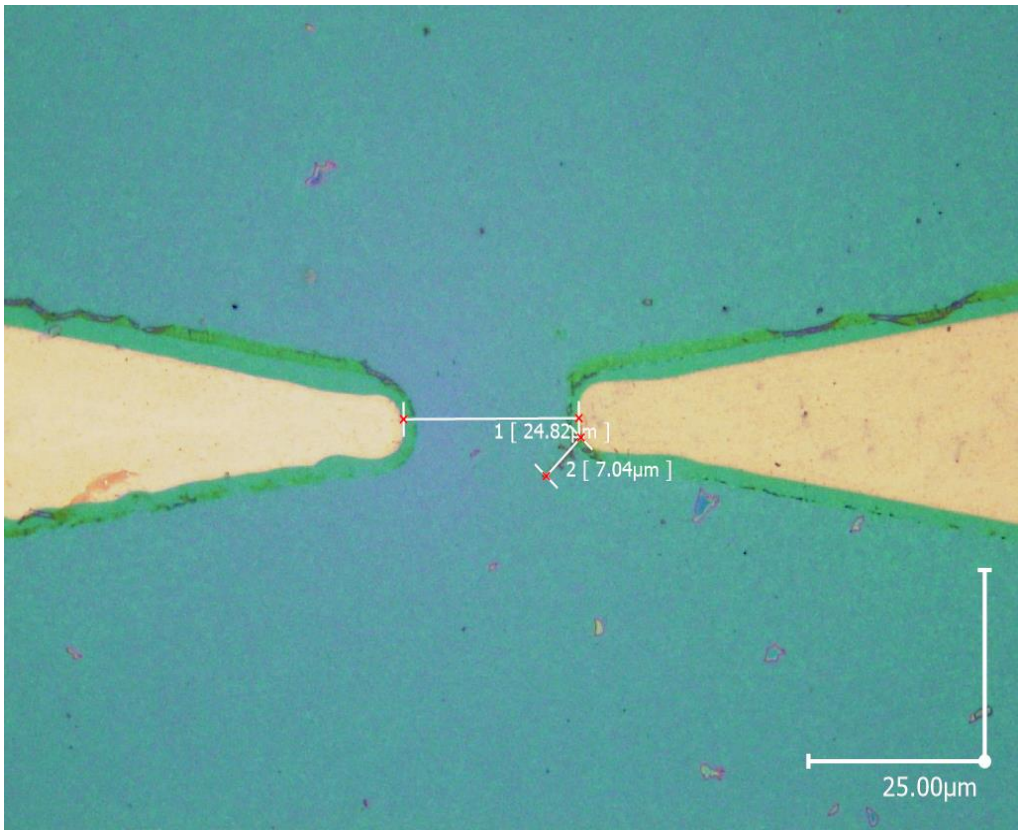


Figure 39: 1000X image for device PG1 in the 20 nm Cu sample taken after the 80V 100,000 second test, anode on the left side

The dendrite only grew 7.04 um in 100,000 seconds giving a rate of 7.04e-5 um/sec. This is 10 times the rate of the PF1 dendrite. However, it is still very slow compared to the devices in the 25 and 30 nm samples. More, long term (days of testing), high DC bias (70 to 90V or higher), in both rectangular and triangular devices will be required to establish a rate to field relationship. The rates can be compared to the 25 nm and 30 nm samples to establish a more precise relationship between copper concentration in the electrolyte and the rates.

Please note that the dendrites grew continuously in this sample. This confirms, at least as far as the previous tests are concerned, that both the applied field and the amount of copper in the electrolyte both factor into the dendritic growth rate and the dendritic

pattern continuity. Once again, further processing and testing are needed to establish a more precise relationship between growth rates and fields and deposited copper.

PROFILE OF DENDRITIC GROWTH

When the filaments grow from cathode to anode, are they growing on the copper oxide surface or cutting through the electrolyte? Is it a combination of both? Atomic Force Microscopy was performed on the 25 nm copper sample triangular device PE2. This device was tested at 60V for 100000 seconds. The field applied for the bias and the 62.83 um distance as shown in Figure 40 is 954957.82 V/m.

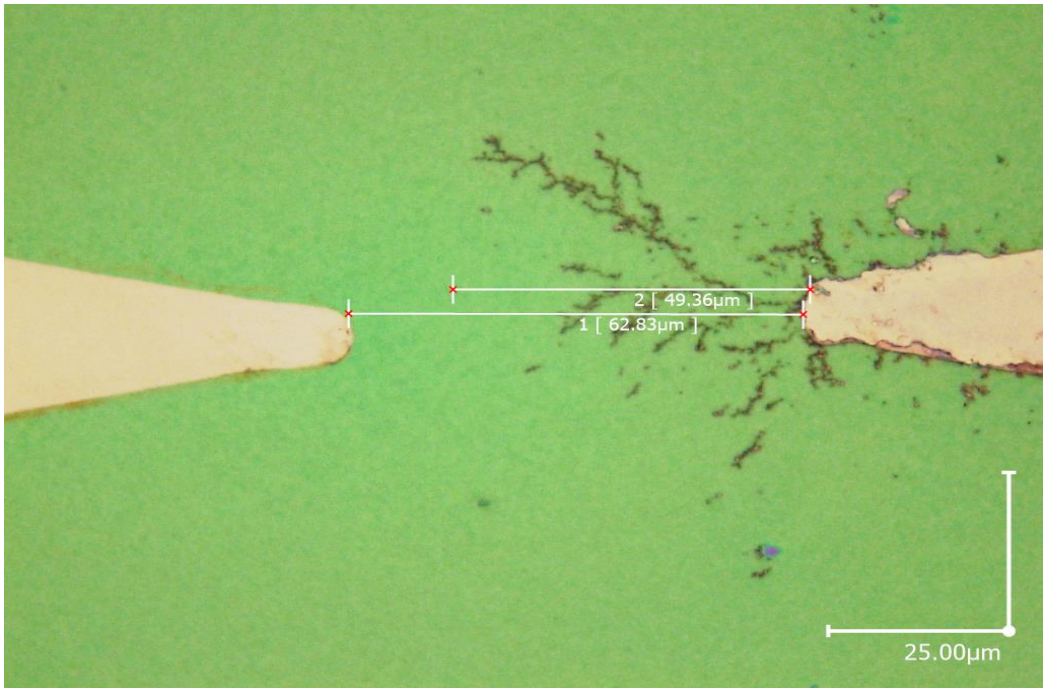


Figure 40: 1000X image for device PE2 in the 25 nm Cu sample taken after the 60V 100,000 second test, anode on the left side

The dendrites here are pretty continuous as expected for the low field applied in the 25 nm sample device. A careful scrutiny of Figure 40 shows some faintness in the dendrites

initially growing out of the cathode. A possible explanation is that they are cutting through the electrolyte under the surface before growing on the surface. Figure 41 shows the 3D image taken from a confocal microscope.

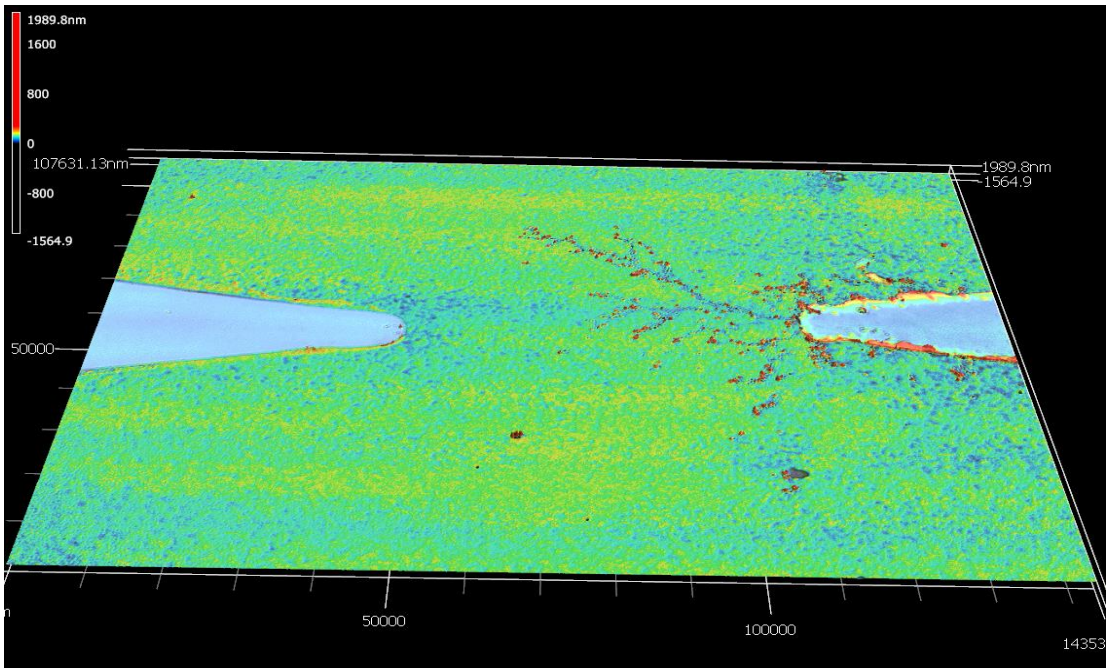
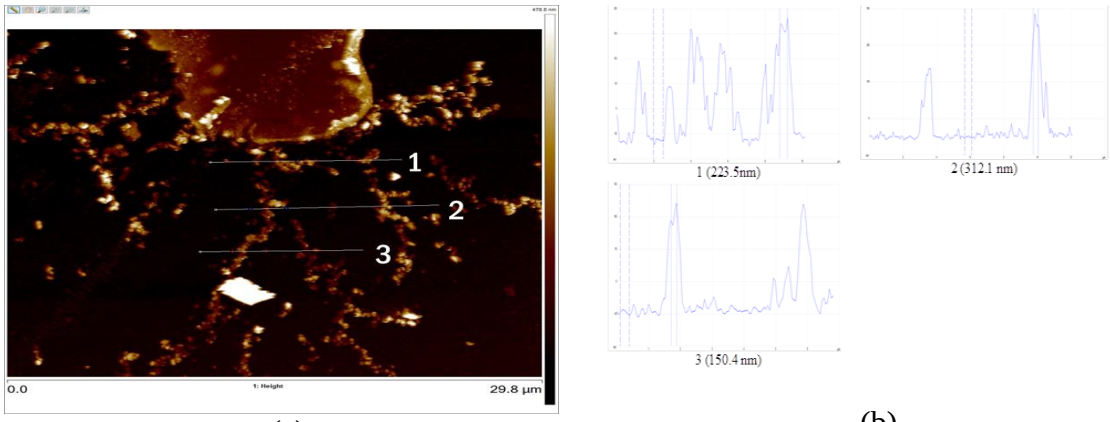


Figure 41: 3D image for device PE2 in the 25 nm Cu sample taken after the 60V 100,000 second test, anode on the left side

The 3D image of Figure 41 serves as a height image as well. The scale shows that the blue color is the lowest, green is the third highest, yellow is second highest, and red is the highest. Going by the image in Figure 41, it appears that most of the dendrites are growing underneath the surface.

Atomic Force Microscopy (AFM) was performed on this device by Smitha Swain. Figure 42 shows the AFM image and the linear profiles taken at three different locations:



(a) (b)

Figure 42: (a) 2D AFM Image of device PE2, (b) Linear profiles taken at three different locations in the dendritic growth

First of all, the linear profiles clearly show that there is activity on the electrolyte surface.

There are three hypotheses on what could be occurring:

- Filament growth is occurring on the surface
- Filaments are growing under the surface and pushing up the electrolyte and surface copper oxide (see chapter 4 and references [19], [20], [21], and [22])
- Filament cuts under the surface and then breaks through the surface

The linear profile in Figure 42(b) for location 1, which is closest to the cathode is shorter than the profile taken at location 2. The expected result is for the location closest to the electrode to be the tallest and shorter at locations further away. While location 3 is the shortest as expected, locations 1 and 2 do not show the expected result. This harkens back to the possible explanation that the filaments cut through the electrolyte as it grows from the cathode and then grows above the surface. This image and profiles taken seem more consistent with the third hypothesis. However, further testing is required to confirm or reject this explanation.

Figure 43 shows the 3D image of the AFM taken for device PE2.

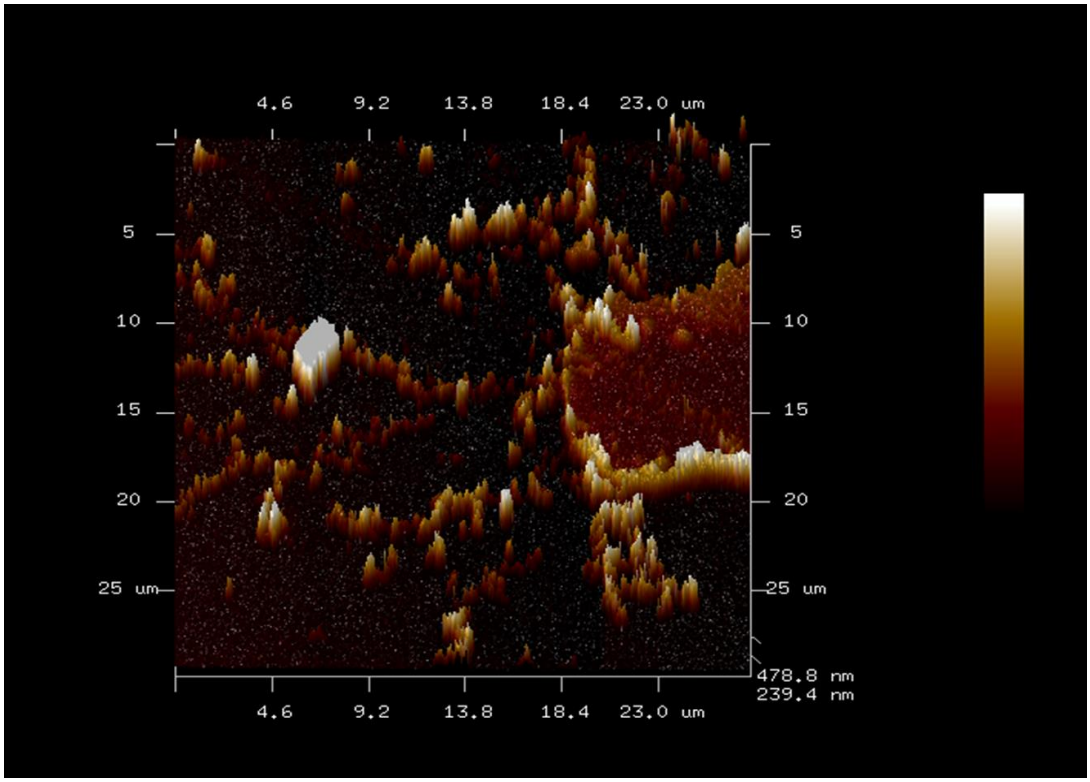


Figure 43: 3D image for the AFM taken of device PE2 in the 25 nm Cu sample taken after the 60V 100,000 second test

The 3D AFM image from Figure 43 shows clear activity occurring on the surface. Further testing will be needed to confirm which of the three aforementioned hypotheses fit with what is shown in this 3D AFM image. Conductive AFM, scanning electron microscopy, and tunneling electron microscopy is suggested for select devices to discern what is occurring on the surface and below.

Chapter 3

THREE TERMINAL DEVICES

DESCRIPTION

Unlike the two-terminal devices, three terminal devices include a buried electrode element in the device. As can be seen in Figure 2, the buried electrode is used to measure capacitance change over the time of dendritic growth. As the filaments grow, the area increases and the capacitance also increases with area.

The processing of the three terminal devices is more complex than the two terminal devices due mainly to the inclusion of the buried electrode and isolation layer (to isolate the buried electrode from the rest of the device. The section on optimization details how the isolation layer is not needed since the metallic copper in the electrolytic matrix does not actually short the device. However, for this section, the isolation layer was added and will be described.

PROCESSING

There are 4 main sections for processing:

1) Buried electrode and isolation layer
2) Electrolyte deposition and doping
3) Electrode depositions
4) Etching to expose the buried electrode

The first series of steps are to create the buried nickel electrode. A silicon wafer with 200 nm of nitride deposited on top is used as a base for these devices. Photolithography is performed as described above for the two-terminal devices using OCG825 and AZ3312. In the next section on optimizing the WO_3 electrolyte, a different photolithography recipe is used to solve the problem of jutting sidewalls that spring up after the buried electrode is deposited and excess metal is lifted off. These jutting sidewalls skew the capacitance results since they reduce the distance to the buried electrode as the filaments grow.

The following image shows the completion of the photolithography step using the buried electrode mask (Mask 1). The procedure described for the two terminal device was used:

1) HMDS spun at 4000 rpm for 30 seconds and baked at 120C for 1 minute
2) OCG825 resist spun at 4000 rpm for 30 seconds and baked at 105C for 1 minute
3) AZ 3312 resist spun at 4000 rpm for 30 seconds and baked at 100C for 1 minute
4) Expose using cathode mask for 4.5 seconds
5) Post exposure bake at 100C for 1 minute
6) Develop using MIF300 for two minutes, wash and inspect

Figure 44 shows the image after the above steps are completed.

Figure 44: Three-terminal device buried electrode photolithography 100X image after exposure using Mask 1 and 2 minute development

As can be observed in Figure 44, there is no remaining resist in the deposition area. After the photolithography step was completed, a dektak profile was taken. This was done to make sure that at least 1.6 um of photoresist was deposited based on the spinning described in the process above. As shown in the profile taken, 1.6 um of photoresist was indeed deposited.

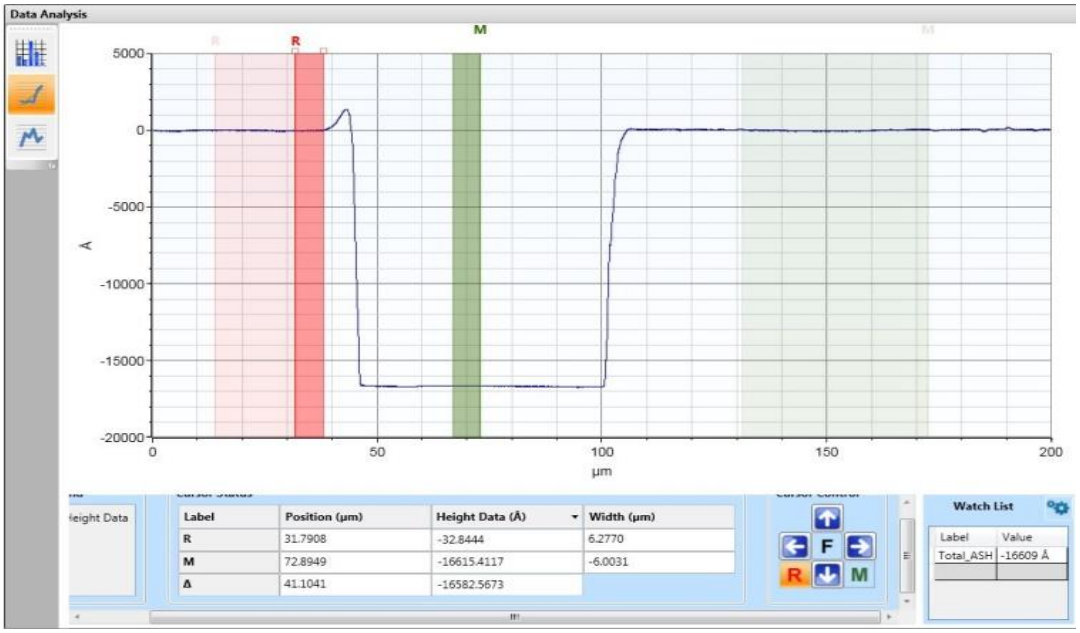


Figure 45: Dektak profilometry for the buried electrode photolithography

Once the photolithography step was completed, etching was needed. Using the PlasmaTherm790 fluorine etch machine, a 1 minute etch was done. This removed 45 nm of silicon nitride out of the patterned areas (this was found to be a bit deep for the buried electrode and 30 nm of etching was done in future processing). The following image shows the result after the etching was completed

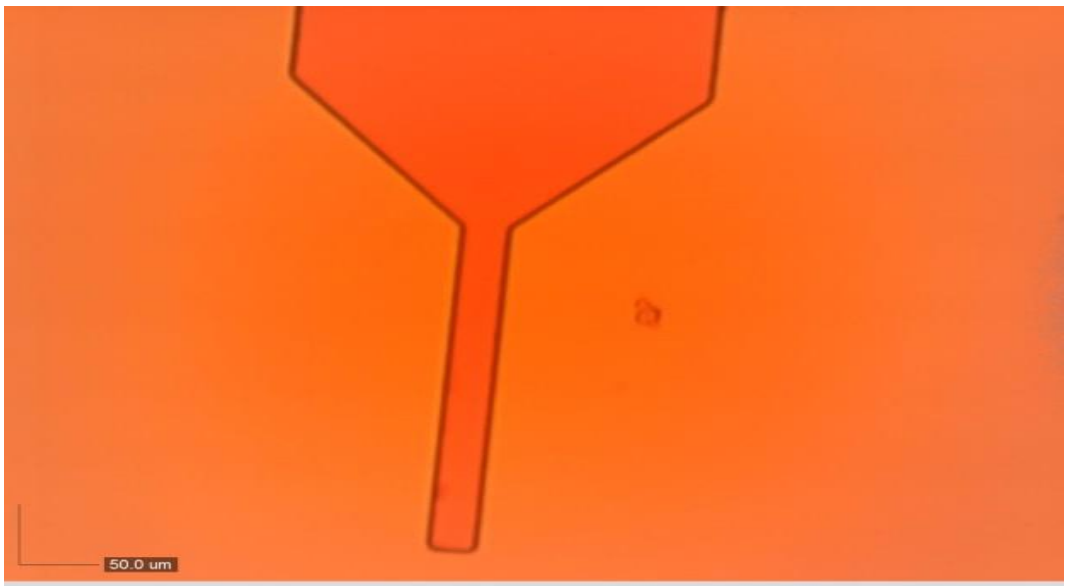


Figure 46: 100X image of three-terminal device buried electrode photolithography image after fluorine etch of silicon nitride

To ensure that the etching process did not remove too much photoresist, another dektak profile was taken. As shown in Figure 47, there was no photoresist removed.

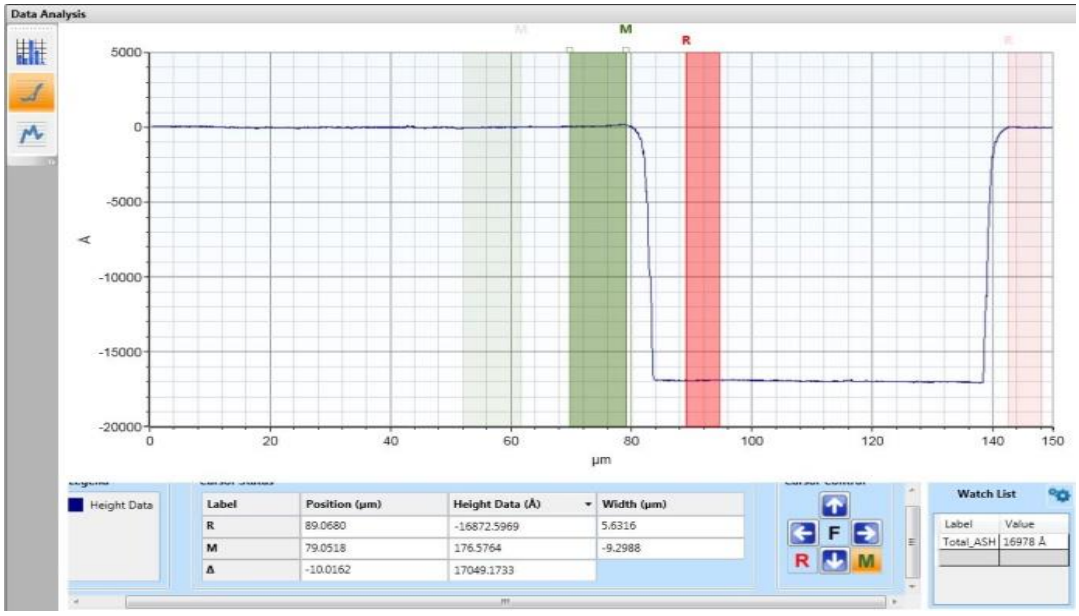


Figure 47: Dektak profilometry for the buried electrode photolithography after the etching before depositing the buried electrode

Once the etching was complete, the next step was to deposit nickel in the etched pattern using electron beam evaporation at a rate of 1 angstrom/second. This rate was found to be too fast and in combination with the 40 nm depth was found to lead to the sidewalls shown below. The deposition rate in future processings was 0.5 angstroms/second. Figure 48 is an image taken after approximately 45 nm of nickel was deposited and the excess lifted off using acetone.

Figure 48: 100X Image of buried electrode after nickel deposition

The dektak profile in Figure 49, taken after the completion of the step shows the sidewalls around the electrode. As can be observed in Figure , the sidewalls are approximatele 25 to 55 nm in height. The relatively large height and small area can skew capacitance measurements as they are taken. Ideally the profile must be flat and there should be no sidewalls. Later processes would take care of this problem as described in chapter 4.

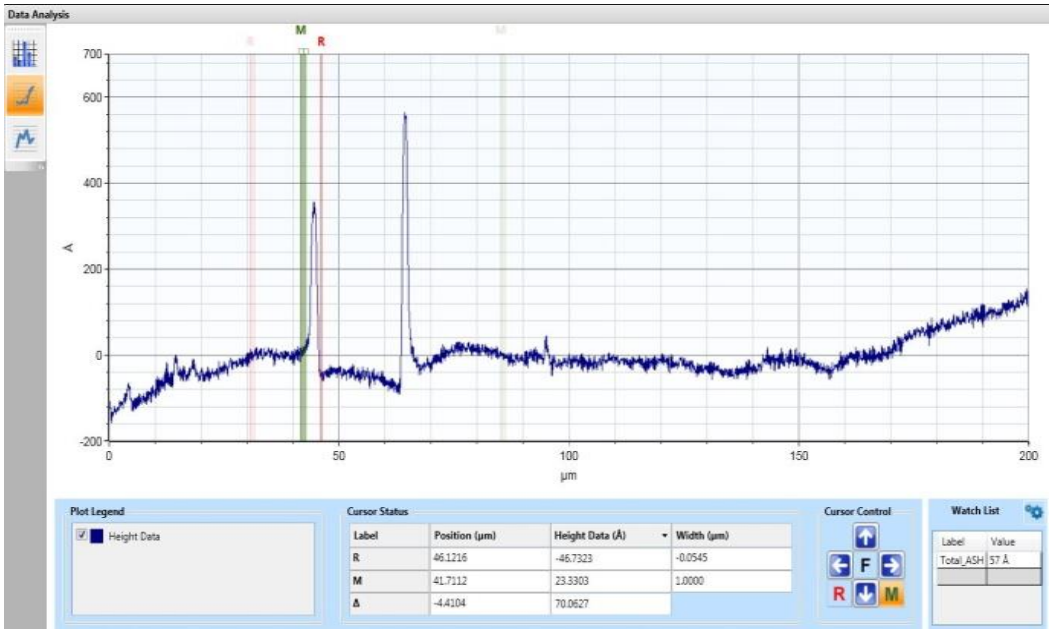


Figure 49: Dektak profilometry for the buried electrode step after the deposition and liftoff of nickel

After depositing the buried nickel electrode, a 50 nm isolation silicon oxide was deposited using RPCVD. After RPCVD, the electrolytic layer was processed. Figure 50 shows the electrolyte layer image after photolithography was completed. Figure 51 shows the dektak profile after the photolithography. Again, the profile and image show that the process was accomplished cleanly in that there is no resist or defects in the deposition area.

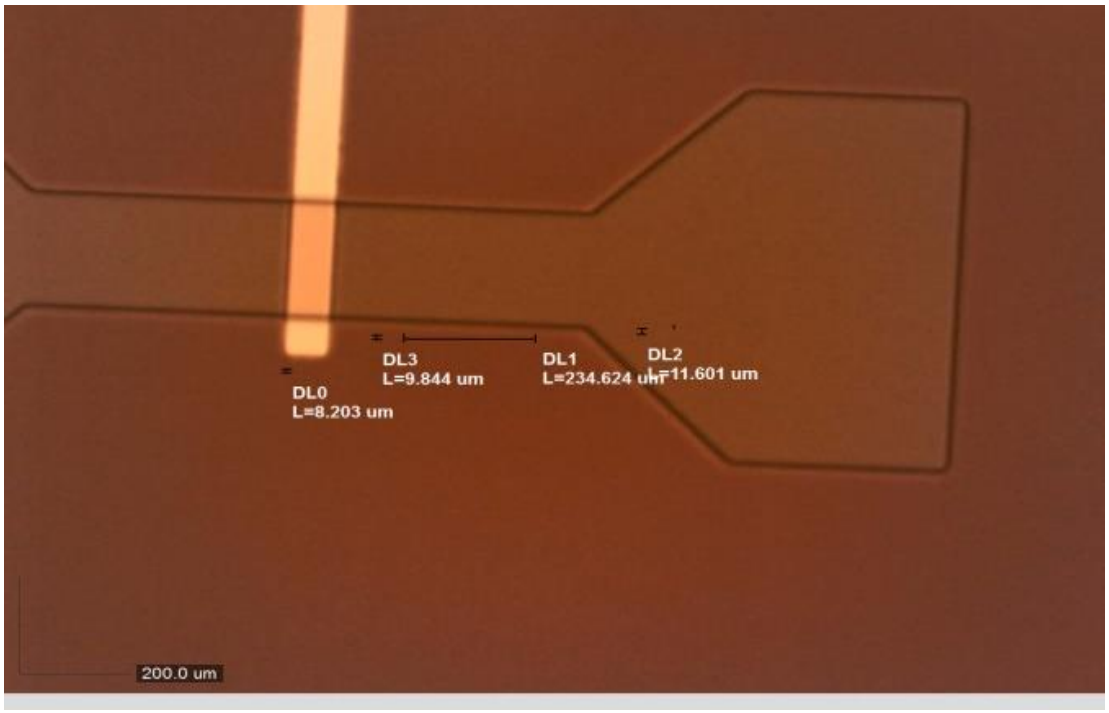


Figure 50: Three-terminal device WO3/Cu electrolyte layer photolithography 100X image after exposure using Mask 2 and 2 minute development

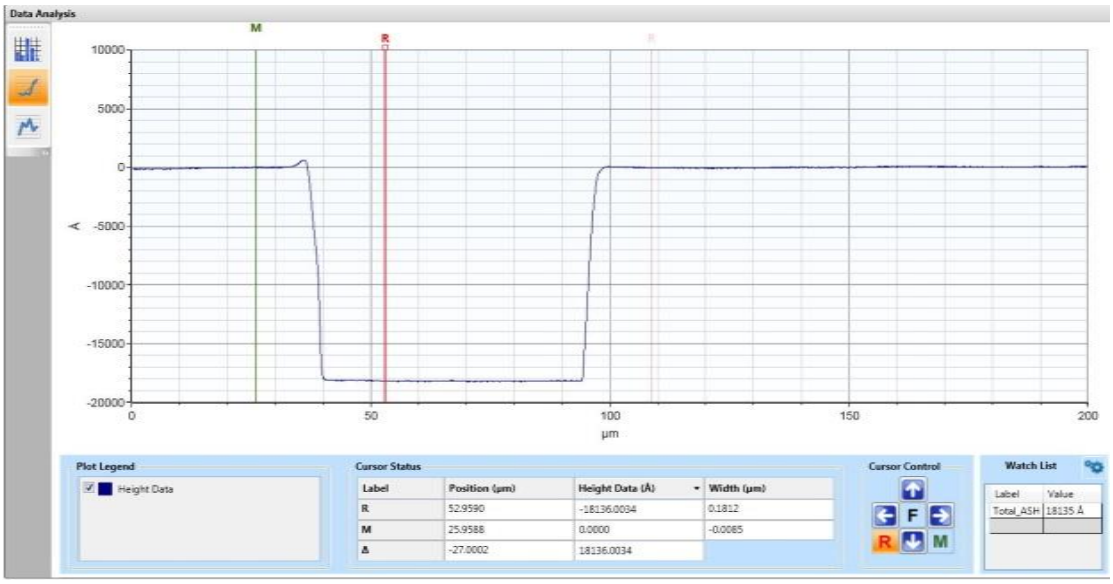


Figure 51: Dektak profilometry for WO3/Cu electrolyte step after photolithography

Once the lithography is complete, e-beam evaporation is used to deposit 100nm of WO_3 and 25nm of Cu. Both were deposited at a rate of 1 angstrom/sec. The excess electrolyte layer is lifted off using acetone. Figure 52 shows the image of the electrolyte step after deposition and liftoff were completed.

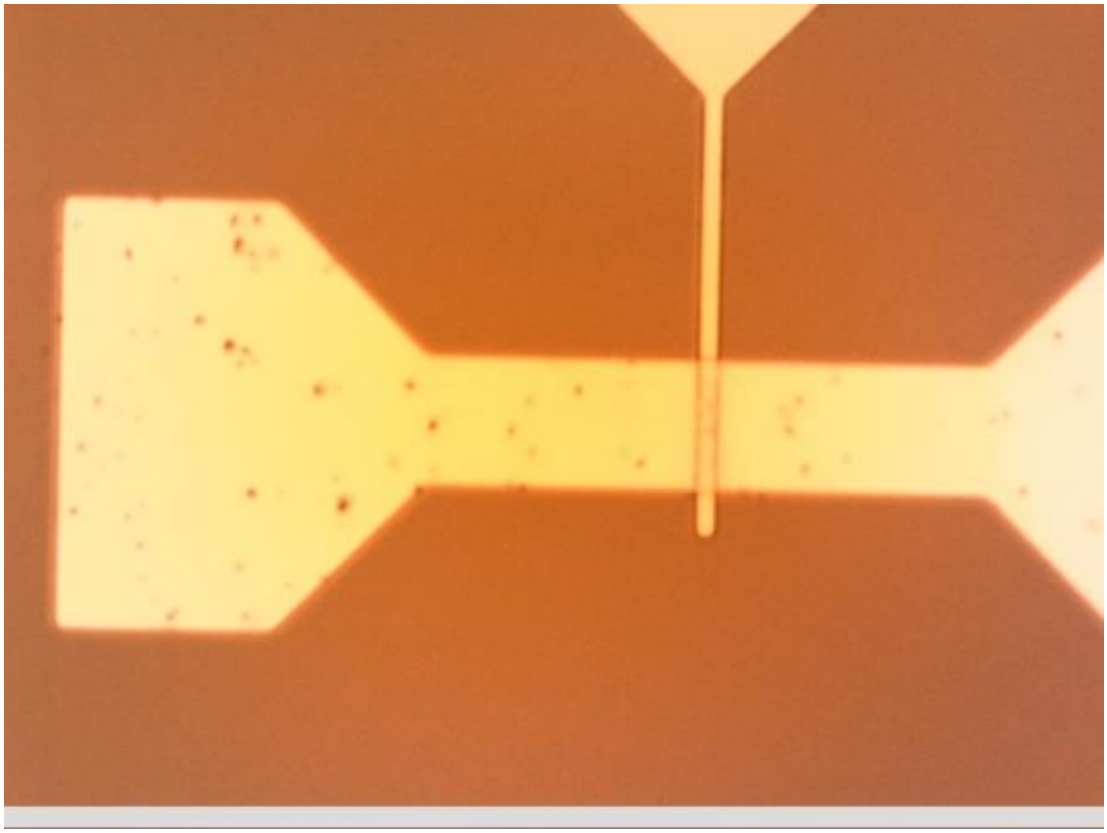


Figure 52: Three-terminal device buried electrode after WO3/Cu deposition and liftoff, 100X image

After the liftoff step is completed, the wafer is heated at 135C in a convection oven for 30 minutes. Figure 53 shows an image of the result after annealing has occurred.

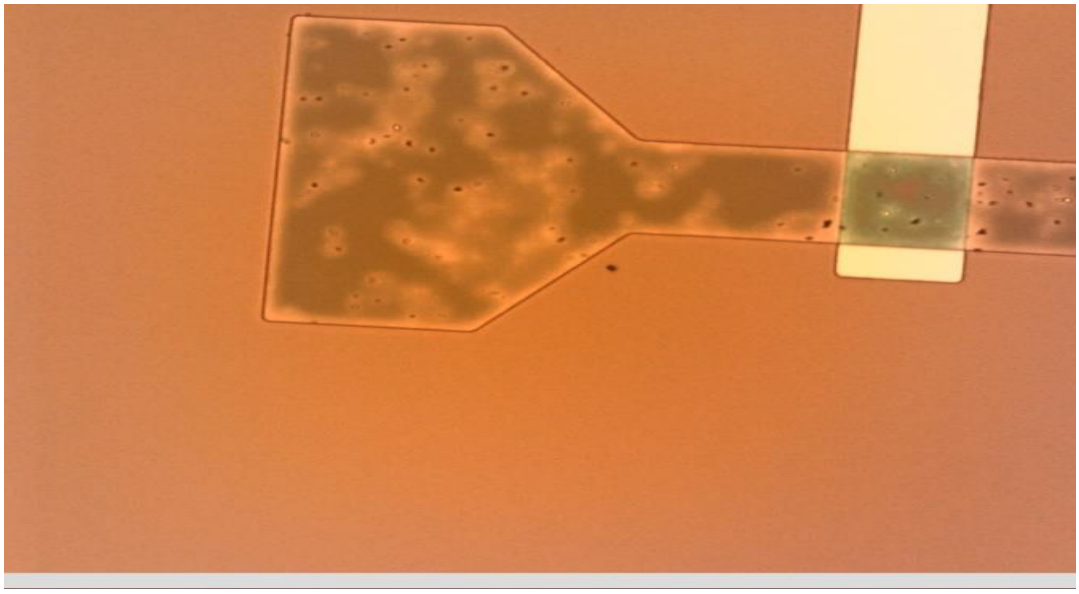


Figure 53: Three-terminal device buried electrode after WO3/Cu after baking in convection oven at 135C for 30 minutes, 100X image

After the annealing, another dektak profile is taken of the electrolyte layer. Figure 54 shows the resulting profile. The height is at about 1442 angstroms or 144 nm. This is due to the slight expansion of copper when it oxidizes.

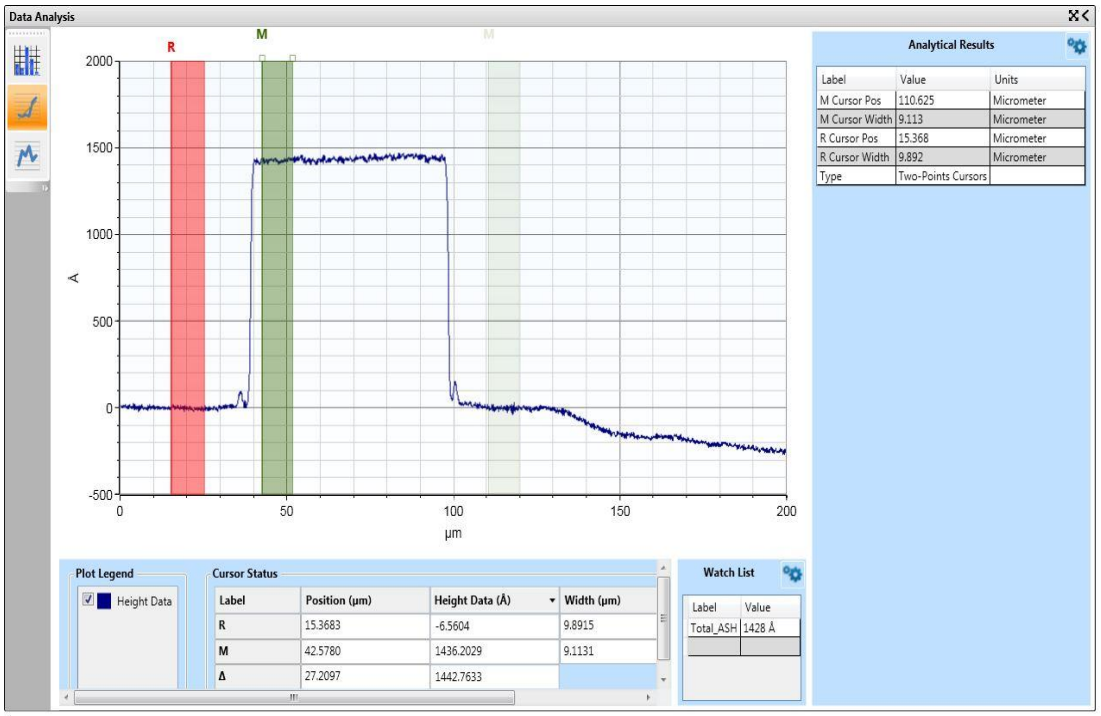


Figure 54: Dektak profilometry for WO3/Cu electrolyte step after 135C anneal step

Once the electrolyte was annealed, the electrodes were deposited using Mask 4 for the tungsten cathode and Mask 3 for the copper anode. After photolithography, 90 nm of tungsten for the cathode was deposited using sputtering, at a rate of 1 angstrom/second and lifted off using acetone. This process was repeated for the copper anode with the same 90 nm of copper deposited using e-beam. Figure 55 shows the final resulting image of a device after the electrodes are deposited.

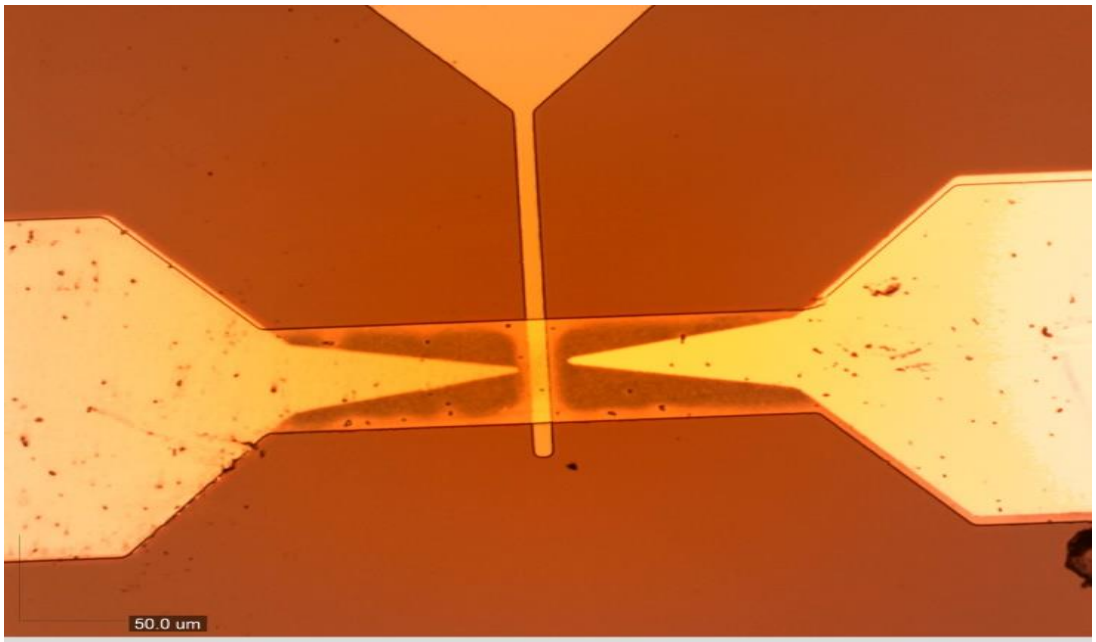


Figure 55: Three-terminal device electrode deposition, anode is on the right (reverse microscope)

Dektak profiles were take for both the tungsten cathode and copper anode. Figures 56 and 57 show the profiles. As can be seen in Figure 56, the tungsten cathode has a height of about 70 nm. This amount is enough for probing. The same is true for the copper anode.

Figure 56: Dektak profilometry for tungsten cathode deposition

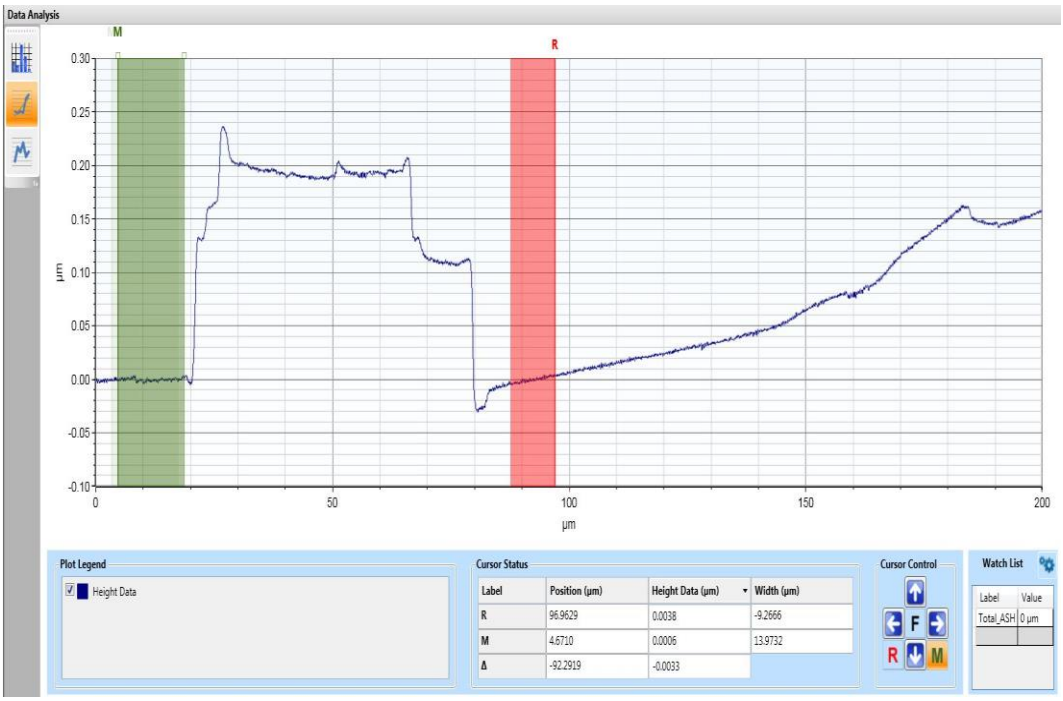


Figure 57: Dektak profilometry for copper anode deposition

After the electrodes are deposited, the buried electrode needs to be exposed for probing. This is accomplished using the PlasmaTherm790 fluorine etch. First Mask 7 was used for photolithography to protect the parts of the wafer that did not need etching. Figure 58 shows the photolithography image.

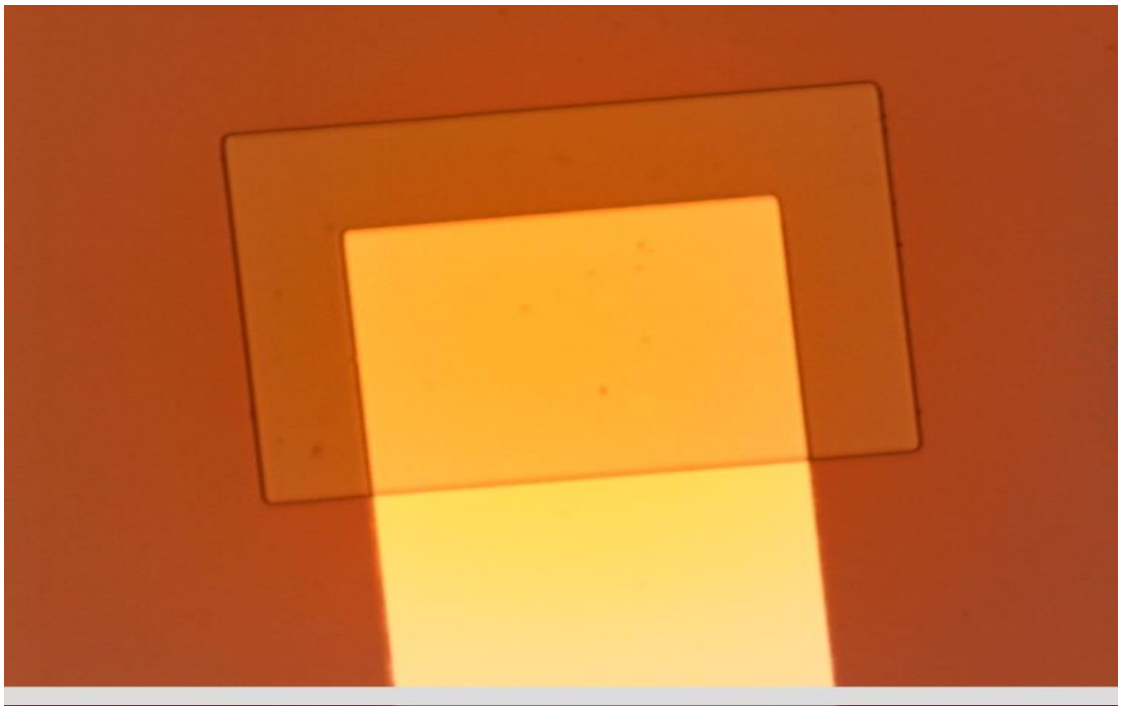
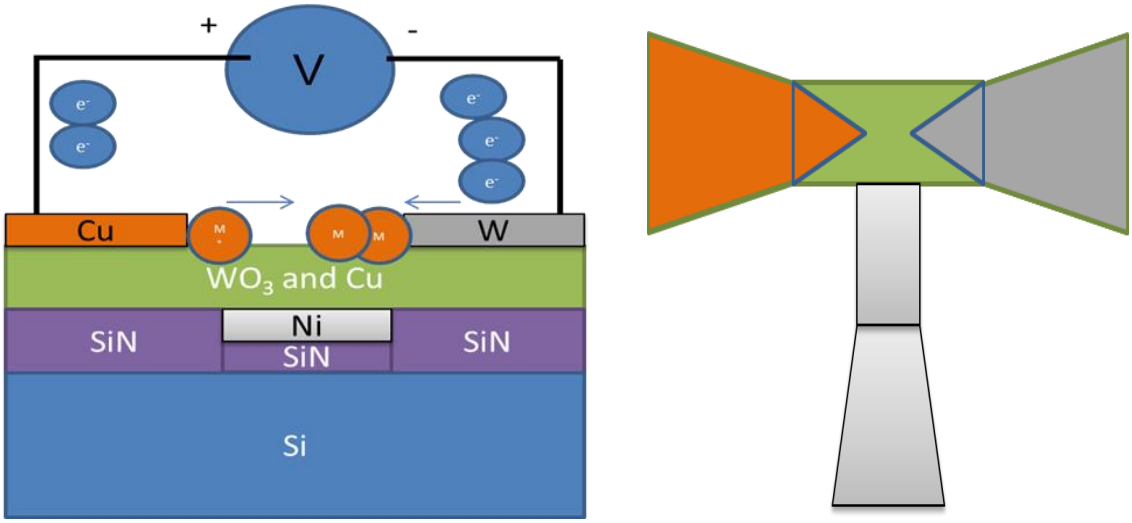


Figure 58: Three-terminal device buried electrode exposure photolithography

Once the photolithography is complete, the oxide was etched using an oxide etch recipe for 1 minute to remove the 50 nm of isolation oxide. After this, the photoresist was removed using acetone and the device is complete.

Figure 59 shows a schematic of how the final device looks like after processing is complete. An image of a completed device is shown in the testing section.



(a) (b)

Figure 59: Completed three-terminal device schematic, Sideview (a) and top view (b)

The differences in processing between the tungsten trioxide electrolyte processing and the chalcogenides is that silver is used instead of copper, UV doping was done to mix in the silver in the chalcogenide instead of thermal doping, and nickel is used as the cathode instead of tungsten. The device looks essentially the same as the schematics above.

THREE TERMINAL DEVICE TESTING

The testing and write-up of this report was performed by Dr. Yago Gonzalez-Velo. In order to compare to the tungsten trioxide electrolyte, the chalcogenide based three terminal devices were tested. That testing has been conducted on different manufacturing batches using similar stress conditions in order to be able to have a sense of how much faster or slower given electrolytes are with respect to others similarly to what has been done in previous quarters in a continuing effort to characterize the manufactured devices. Figure 60 shows a chalcogenide based three-terminal device under bias.

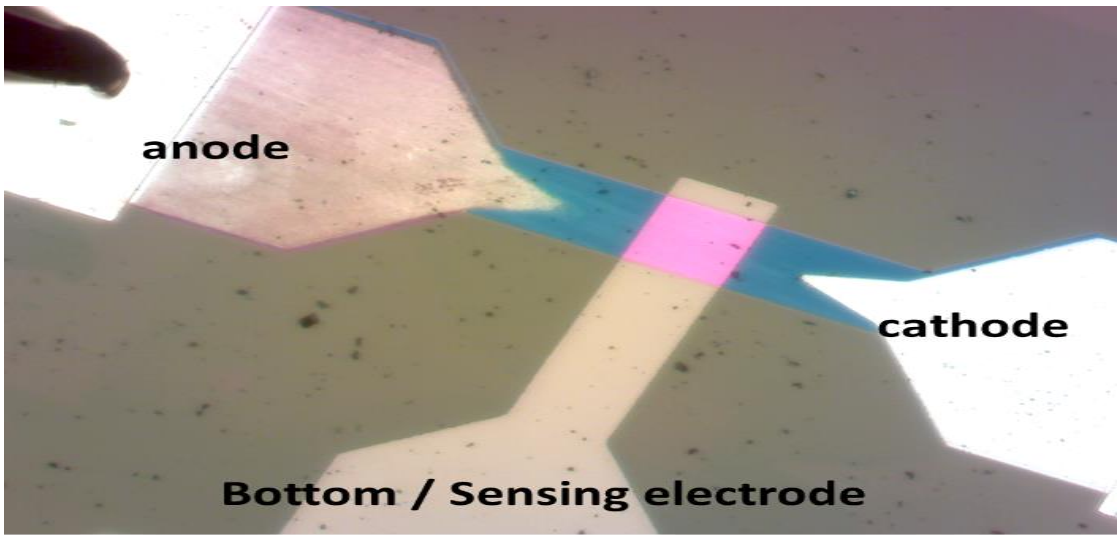


Figure 60: Top view microphotograph of a 3-terminal device with names of the electrodes shown: bottom sensing electrode, the anode (silver) and cathode (Nickel). The dendrite growth occurs on the cathode. The varying capacitance is measured between the cathode and the sensing electrode

Devices with varying distances and geometries were tested using the 4284 LCR meter, an 81160 pulse pattern generator, and a 4156C analyzer. The results described here are only for the triangular devices that are 12 um apart with a buried electrode width of 8 um for both the chalcogenide and tungsten tri-oxide devices. The same geometries were used in both samples for easier comparison. The LCR meter was used to measure the capacitance at various sensing frequencies (1kHz, 10kHz, 100kHz and 1MHz). The pulse generator sent the pulses across the device at a set frequency and duty cycle to grow the dendrites. The analyzer measured the current and voltage across the device through the duration of the test. Figure 61 shows the testing protocol used for these devices.

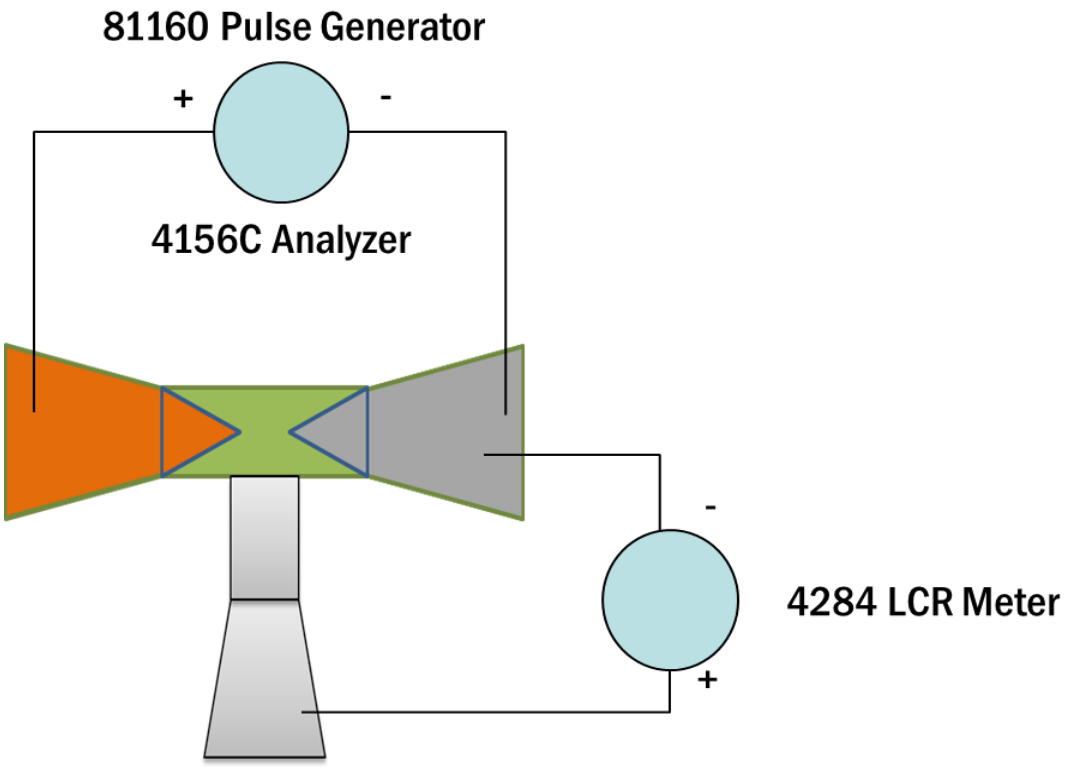


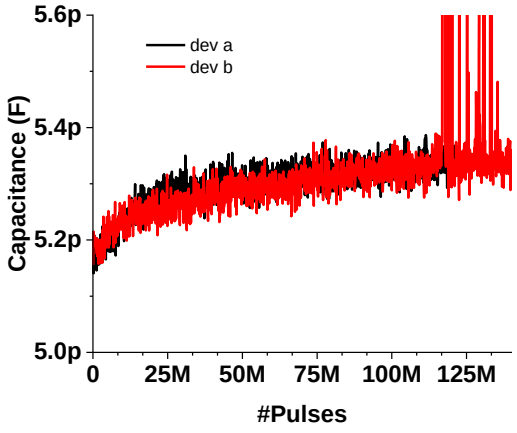
Figure 61: Testing setup for the three-terminal device

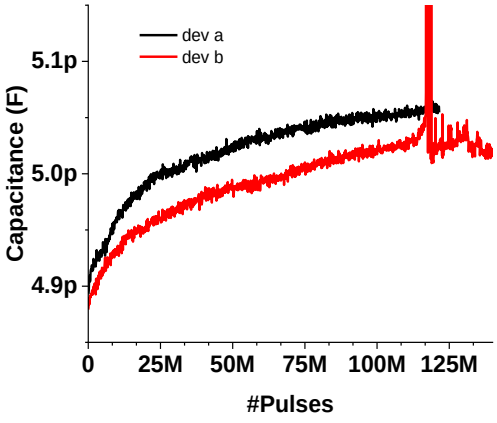
For the chalcogenide-based devices, the test parameters were a pulse amplitude of 2.5 volts, a 1kHz stress frequency, and duty cycle of 50%. To accelerate the testing for the

tungsten tri-oxide electrolyte, the parameters used were 10 volts, 1kHz stress frequency, and a duty cycle of 50%. The comparison between the devices is described in the next section.

TUNGSTEN TRI-OXIDE DEVICE TESTING

Following are the test results for the WO_3/Cu electrolyte that was described in the processing section above. Testing results are reported in Figure 62, whereas illustration of the dendrite growth occurring on one of those devices is shown in Figure 63, Figure 64, and Figure 65. The testing was conducted using a pulse amplitude set to 10 volts in order to accelerate the testing of the device. In addition, a device with minimal distance of 12 micrometers between the anode and the cathode electrodes has been used also to accelerate the testing of the devices. This proves that a 3 terminal structure based on WO_3 would, for identical stressing conditions than chalcogenide electrolyte enable to account for much longer periods of time.





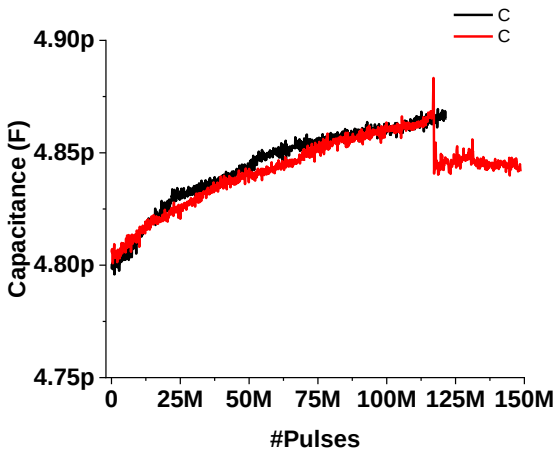


Figure 62: Capacitance variation observed on WO3 based timing devices as a function of the number of 10Volt amplitude pulses at a sensing frequency of (a) 1kHz; (b) 10kHz; (c) 1MHz

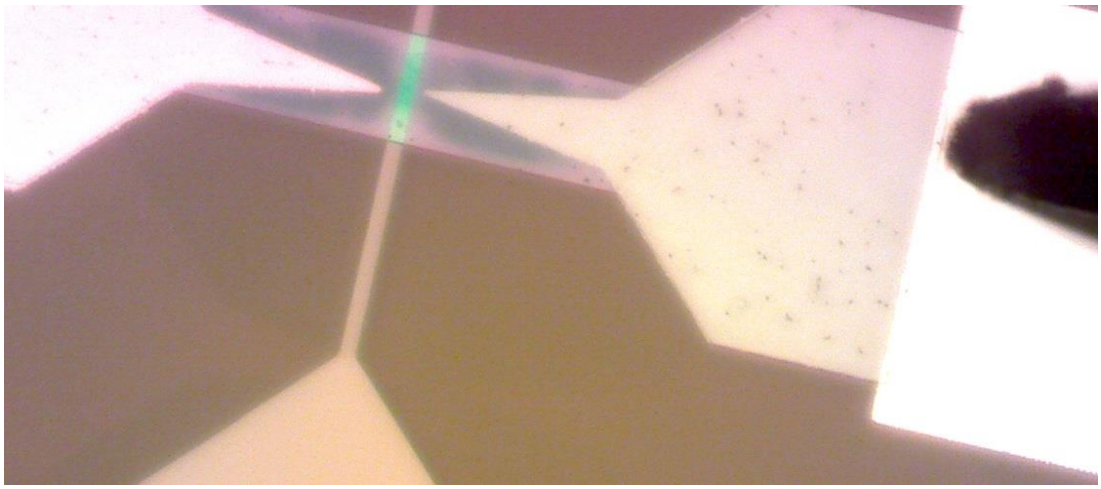


Figure 63: Top view photomicrograph of a WO3 based devices before testing. Distance between anode and cathode is 12 micrometers and width of the bottom electrode is 8 micrometers.

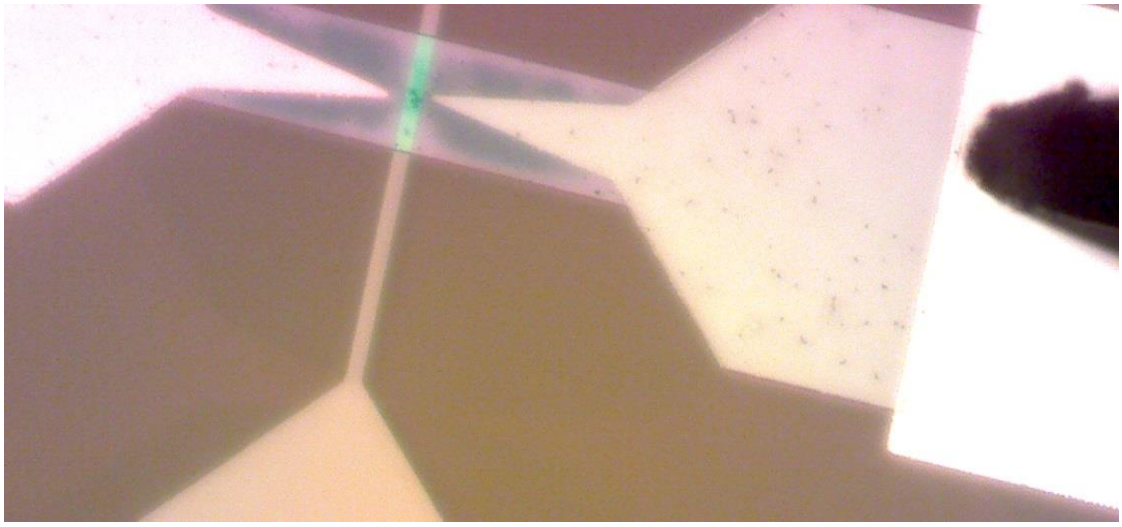


Figure 64: Top view photomicrograph of a WO3 based devices after 78.6 106 pulses applied. Distance between anode and cathode is 12 micrometers and width of the bottom electrode is 8 micrometers.

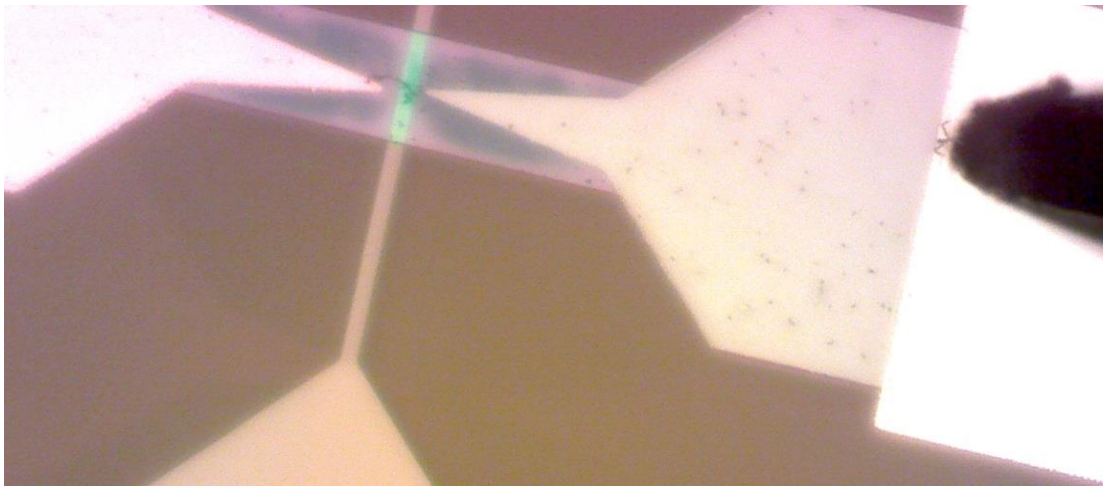


Figure 65: Top view photomicrograph of a WO3 based devices after 148 106 pulses applied. Distance between anode and cathode is 12 micrometers and width of the bottom electrode is 8 micrometers.

A comparison with chalcogenide-based device of the same dimension (8um bottom width, 12um spacing) shows that tungsten WO_3 based devices have the potential for dramatically expending the time counting capability of such devices.

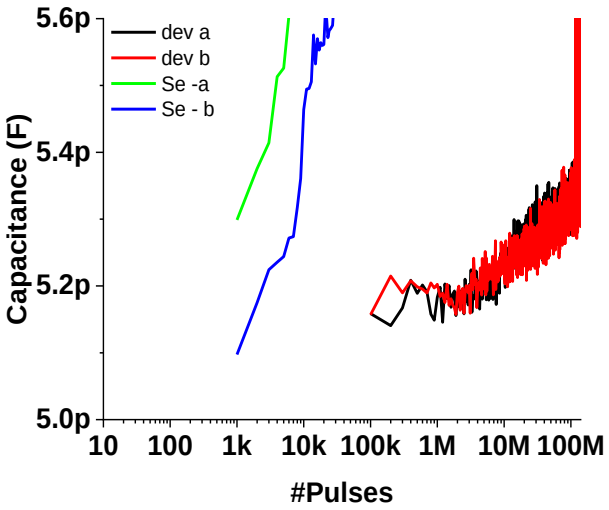


Figure 66: Comparison of the variation of capacitance observed during dendrite growth on small geometry devices made of chalcogenide and tungsten trioxide electrolytes

For chalcogenide-based devices stressed with 2.5 V pulses, capacitance variation and dendrite growth occur over 10kpulses whereas for 10V stressed tungsten trioxide based devices the transition occurs over 100Mpulses. This is a factor of 10^4, and this is for different stress voltage, so the factor for equivalent stressing voltage would be even longer.

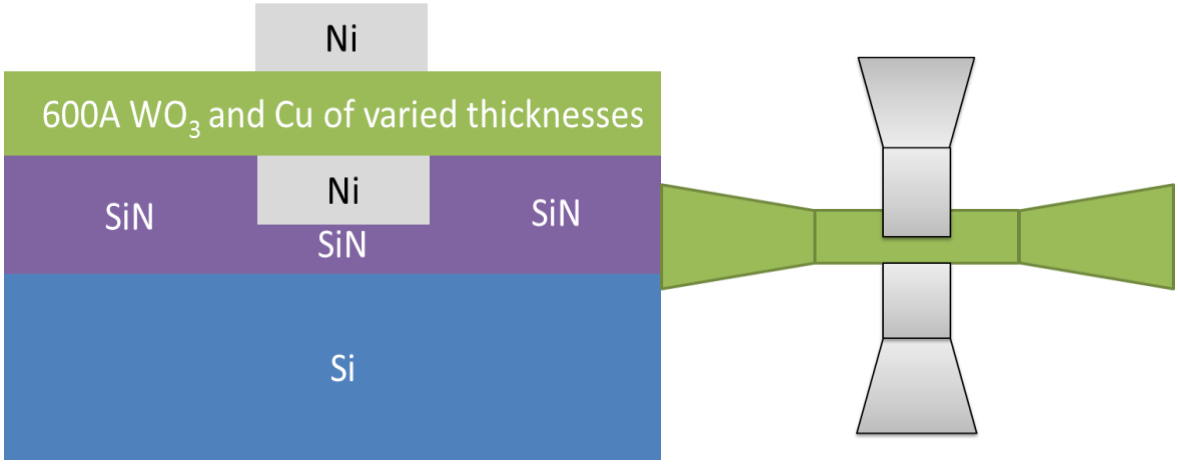
Chapter 4

INVESTIGATION INTO THE TUNGSTEN TRI-OXIDE AND COPPER ELECTROLYTE

DESCRIPTION

In order to investigate and optimize the tungsten trioxide and copper electrolyte, the following questions need to be answered. What is occurring in the electrolyte matrix during and after the annealing process? Does the copper dissolve? Does it oxidize? Is there a combination of dissolution and oxidation occurring? Will it short the device? The purpose of this investigation is to find out what is happening in the electrolyte.

The following structure was created to investigate the electrolyte. As can be seen in the figure below, it is a capacitive structure with nickel electrodes enclosing a dielectric of different compositions and anneal times and temperatures as described in the design of experiments table below. This structure was tested for capacitance, resistance through the device from the top electrode to the bottom. Blanket films were also prepared with the same composition and anneal temperatures and times as the DOE table for the purposes of materials analysis.



(a) (b)

Figure 67: (a) Cross section, (b) top view of the test structure used to test the capacitance, resistance and resistivity of various WO3 and Cu thicknesses

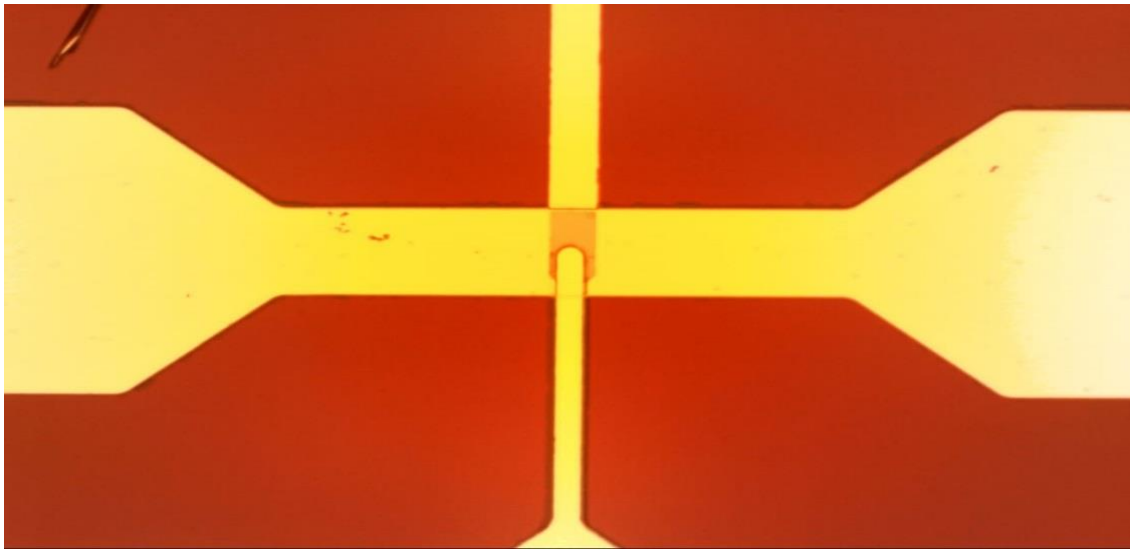


Figure 68: top view microphotographs of one of the devices manufactured as a processing test structure for copper dissolution

PROCESSING

The first step is to deposit nickel after etching into the isolation silicon nitride deposited on a silicon wafer as shown in Figure 2. This step is the most complex step. Past samples, when processed had sidewall nickel ears as shown in the profile taken in Figure 69. The problem with having these sidewall ears is that they skew the capacitance

change results as described in the three-terminal section. Following is the method used to get rid of the sidewall ears.

The photolithography process starts with a dehydration bake at 150C for 5 minutes of the wafer with the passivation silicon nitride. A 180C, 2 minute dehydration bake is also acceptable. HMDS is spun at 4000 rpm for 40 seconds and baked at 120C for a minute. Subsequently, LOR10A resist is spun at 4000 rpm for 40 seconds and baked at 180C for five minutes. After that, AZ3312 is added at 4000 rpm for 40 seconds and baked at 100C. The buried electrode mask is used to expose the sample to UV light for 5 seconds. Three minutes of development time using 300 MIF is required for these samples.

After photolithography, etching was done in the PlasmaTherm 790 flourine etch machine for 30 seconds to etch 230 angstroms off the silicon nitride passivation layer. After this 50 angstroms of titanium and 180 angstroms of nickel were deposited using the Lesker 3 electron beam evaporation (e-beam). The deposition rate of titanium was 0.8 A/s and the rate of nickel deposition was 0.5 A/s. Resist and excess metal liftoff was done using the strong base 400T since acetone is not strong enough to remove LOR10A in a timely manner. The reason for the titanium is to help the nickel adhere well to the etched trenches. Also a smaller amount of nickel at a lower rate of deposition helped ensure that the sidewall ears either did not manifest or were very small. The dektak image shown in Figure 70 has a relatively flat profile.

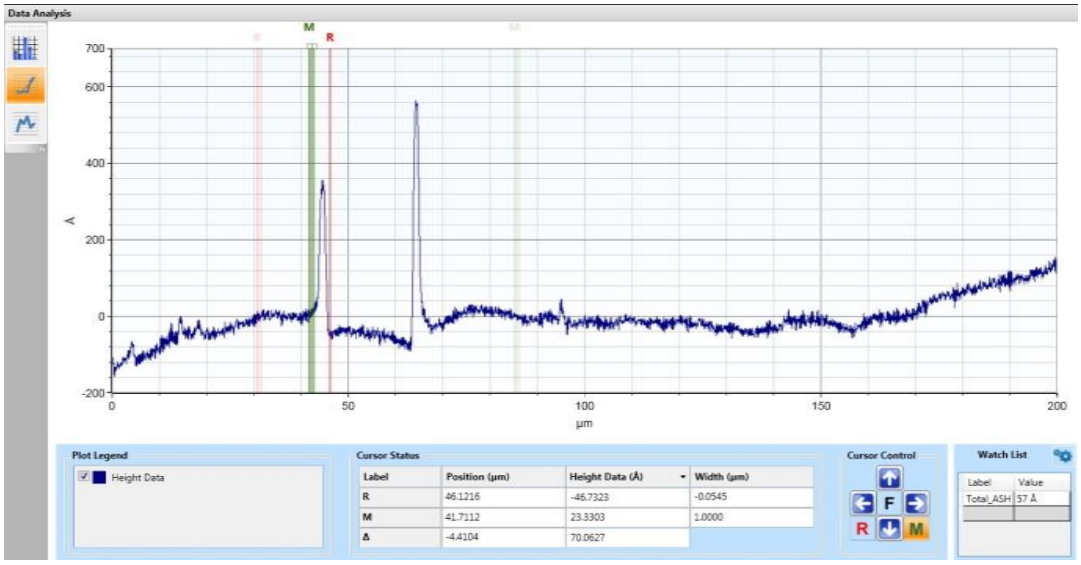


Figure 69: Example of a profile of a buried electrode deposition with sidewall nickel ears in the buried electrode step

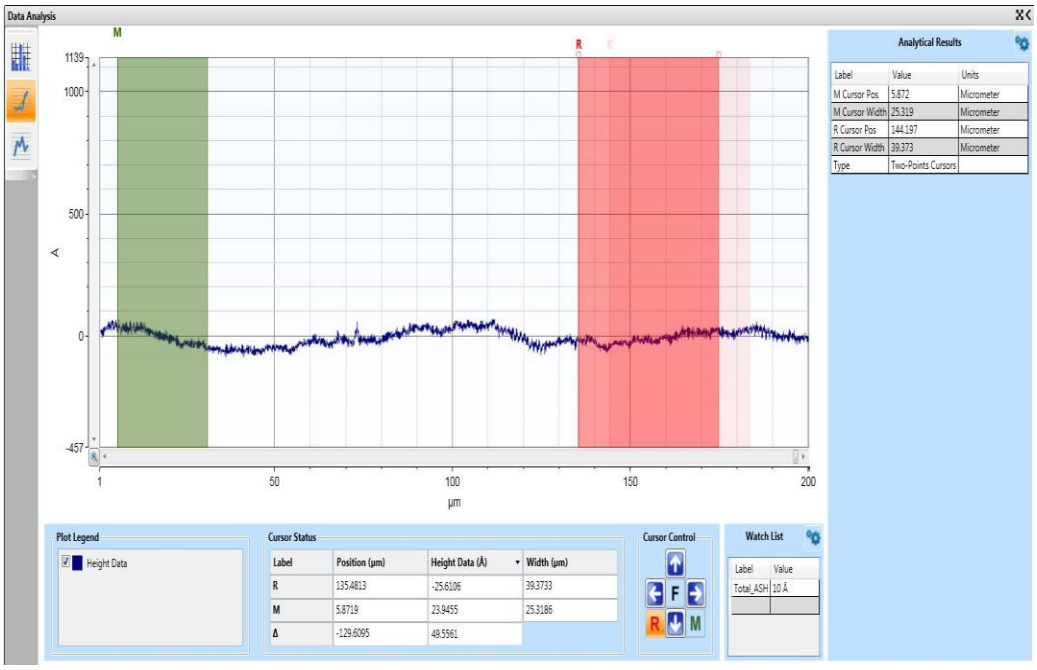


Figure 70: Buried electrode profile with LOR10A process

After the buried electrode is deposited, the next step is the deposition of the WO_3/Cu electrolyte. For this process LOR10A is not necessary since the device is not buried and the sidewall ears do not pose trouble. Therefore, in this case, the photolithography was

done using HMDS spun at 4000 rpm for 30 seconds (baked at 120C for a minute). After that OCG825 was spun at the same rate for 30 seconds and baked at 105C for a minute. Lastly, AZ3312 was spun, again at 4000 rpm for 30 seconds and baked at 100C for a minute. Using the buried electrolyte deposition mask the sample was exposed for 4.5 seconds to UV light, baked at 100C again, and developed using MIF 300 for 2 minutes. 800 angstroms (desired thickness was 600 angstroms, but machine deposited more than needed, statistical run will be needed to optimize the deposition) of WO_3 and 267 angstroms of copper were deposited using the Lesker 3 e-beam evaporation. Both were deposited at rates of 1 A/s. Figure 68 shows the completed device.

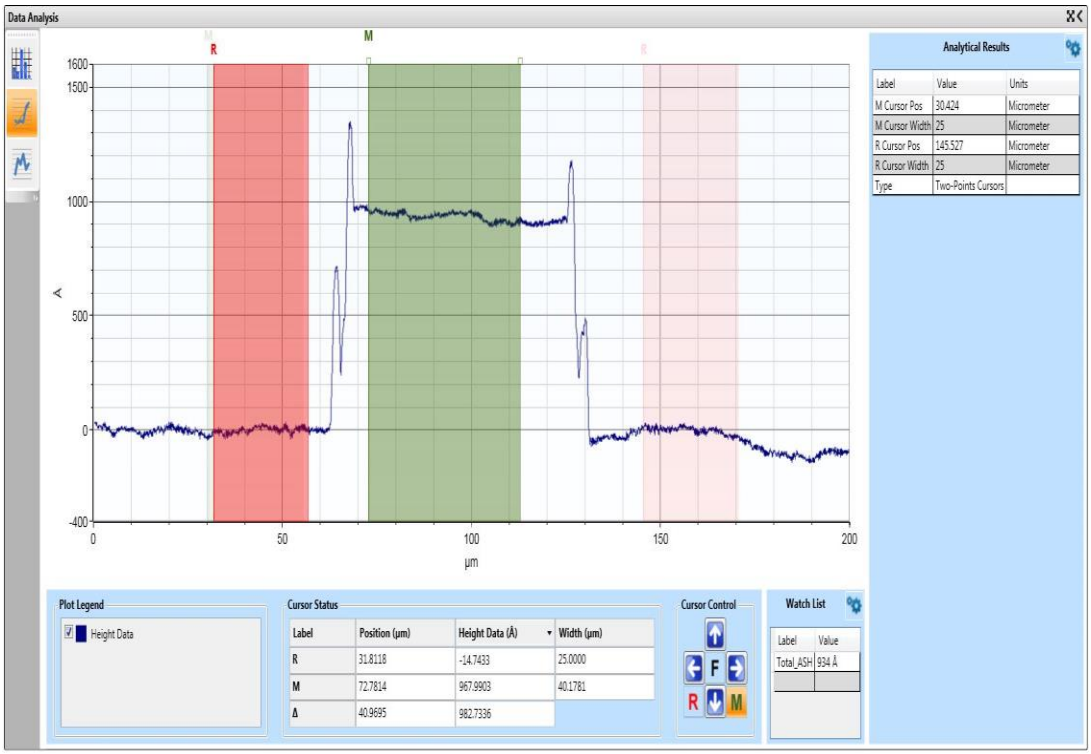


Figure 71: Dektak profilometry for the WO3/Cu electrolyte deposition step.

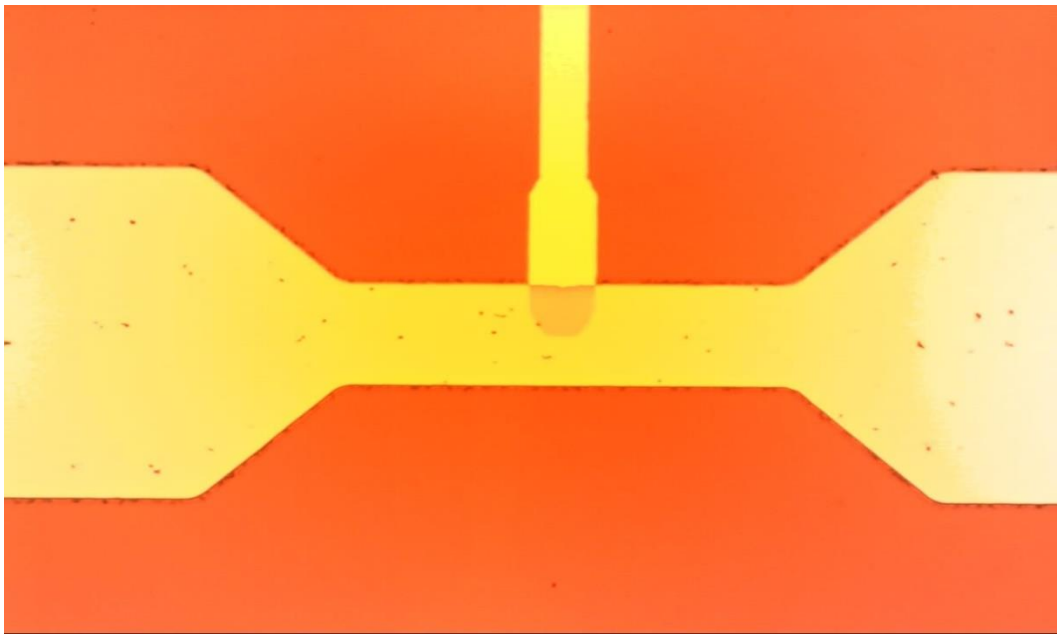


Figure 72: Image for WO3/Cu electrolyte deposition

The last step is the deposition of the top nickel electrode to complete the capacitive device. The alignment must be done such that the nickel electrodes do not short each other out. The OCG photolithography process described above is used with the top nickel electrode mask for UV exposure. 500 angstroms of nickel was deposited using e-beam evaporation. Figure 68 shows the completed device.

DESIGN OF EXPERIMENTS

Table 7 shows the design of experiments for testing the electrolyte.

Run	WO3 Thickness	Cu Thickness	Anneal Temp	Anneal Time
1	800A	267A	None (Control)	None (Control)
2	800A	267A	125C	10 min
3	800A	267A	125C	15 min
4	800A	200A	140C	60 min
5	800A	267A	125C	40 min
6	800A	200A	155C	40 min
7	800A	230A	125C	60 min

8	800A	230A	140C	40 min
9	800A	230A	155C	20 min
10	800A	200A	125C	20 min
11	800A	267A	140C	20 min
12	800A	267A	155C	60 min

Table 7: Design of experiments for testing WO3/Cu electrolyte

The idea is to experiment with 800 angstroms (A, i.e. 80 nm) of tungsten trioxide and various copper thicknesses deposited on top as given in the table below. The goal is to obtain out of the WO_3 and copper two layers, one layer with good electrolytic properties and no top copper remaining on top enabling a short circuit. The dissolution/doping of WO3 by copper will be forced by high temperature annealing. The mixtures will be annealed at different temperatures and times. The characterization looks for device thickness (thickness of the WO_3/Cu matrix), capacitance of the device at 100 kHz with an AC amplitude of 25 mV, impedance from 20 Hz to 1 Mhz, resistance of the WO_3/Cu matrix at 25 mV (measured through the horizontal green layer on the top view), the resistance through the device between the top and bottom nickel electrode, the dielectric constants of the different WO_3/Cu matrices. The characterization is conducted with an agilent 4156C semiconductor parameter analyzer for the resistance extraction and with an agilent 4284 for the capacitance/impedance characterization. Runs 1, 2, and 3 were to check the minimum required anneal time for there to be no metallic copper in the electrolyte.

The reason for these tests is to check if the copper will dissolve and will short out the device once the annealing is complete.

For the purpose of the tests run for these capacitive devices, the naming convention for the devices will be column (letter) and row (number). So device F3 will be the device in column F row 3.

IMPEDANCE SPECTROSCOPY TESTS

These tests are performed on the devices to show what is happening before annealing takes place and after. Dr. Wenhao Chen did similar tests on SiO_2 vertical devices [14] and Will West did it on chalcogenide devices [18]. It will show the change in capacitance as the copper dissolves into the tungsten trioxide and also oxidizes in the oven. These tests will also show us if the dissolving copper will short the device through the electrolyte and into the buried electrode. This last part is important for processing since an isolation layer will not be necessary to prevent the copper shorting the device. Following is the structure and testing protocol for the impedance spectroscopy (IS) tests.

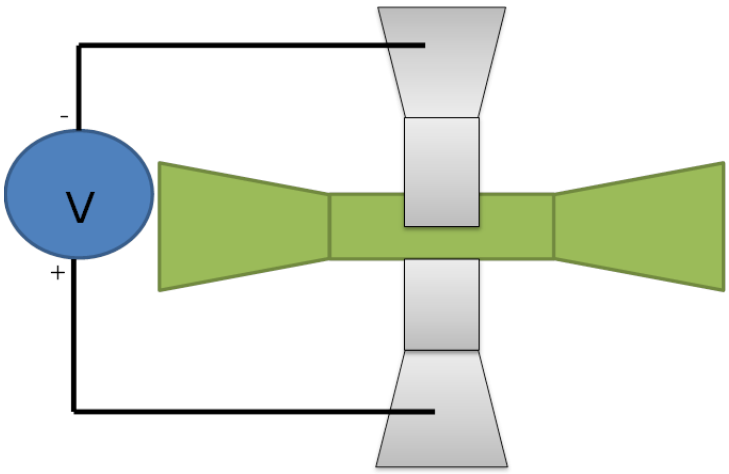


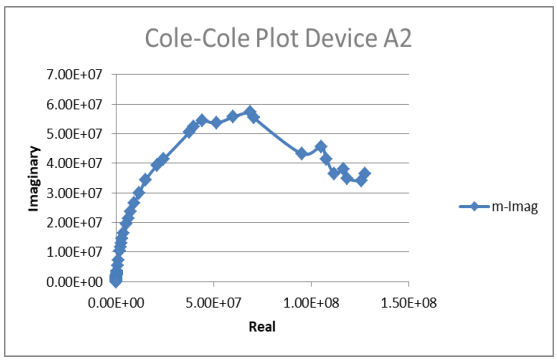
Figure 73: Impedance Spectroscopy Test Method using voltage applied from 4284 LCR Meter

The power supply in Figure 9 is a 4284A LCR meter. The IS tests were conducted in the following manner:

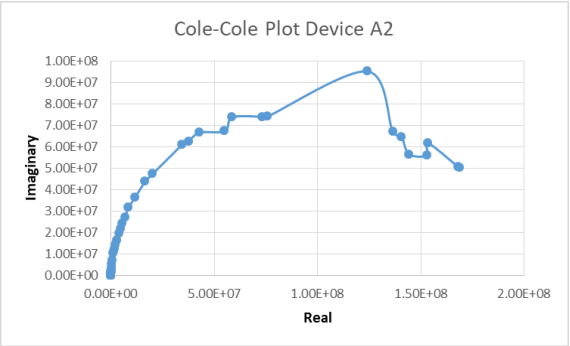
- AC frequencies from 20 Hz to 1 MHz
- Voltage signal is 25 mV or 0.025V
- From this test the imaginary vs. real Cole-Cole plot will be obtained which will indicate whether the device is capacitive (not shorted out) or inductive (shorted out)

The purpose of the Cole-cole plots is to make sure that the devices remain capacitive even after annealing. If the Cole-cole plot was in the negative, imaginary axis, it means that the device has been shorted.

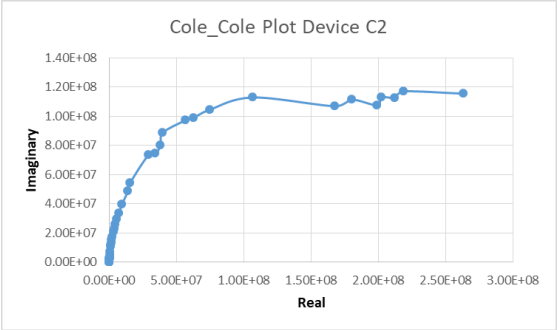
The first series of tests were run on the control sample (no anneal), the 125C 10 minute sample, and the 125C 15 minute sample. Figure 74 shows the Cole-Cole graphs for these three samples (Runs 1-3).



(a)



(b)

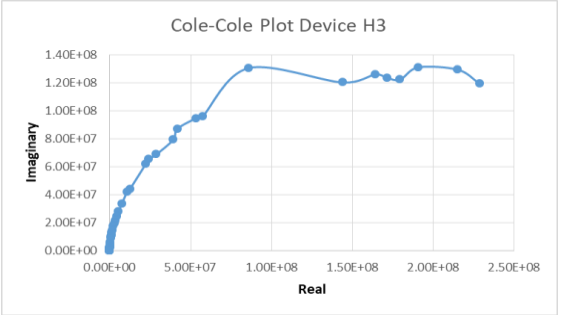


(c)

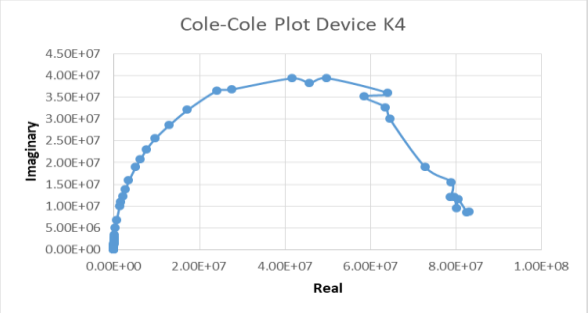
Figure 74: Impedance Spectroscopy Characteristics for runs 1-3. (a) is the control sample (no anneal), (b) is 125C for 10 minutes, and (c) is 125C for 15 minutes

The control and 125C samples described above in Figure 74 have not had a lot of copper dissolved in the electrolyte and hence it is obvious that they would not be shorted out and remain capacitive when measured from the top electrode to the buried electrode. These plots become more important at the higher temperatures since they constitute a good pass/fail test after the copper has oxidized and is dissolved. If after heating, the devices show similar Cole-cole plots like the ones in Figure 74, it means that there is no metallic copper shorting the electrolyte. This means that the electrolyte, when processed the same way in a three-terminal capacitance sensing device, will continue to function as such. Further testing is required to see what happens to the capacitance at the higher frequencies as the heating temperature and times increase. The dielectric constant for the WO_3/Cu mixture can also be obtained from this test.

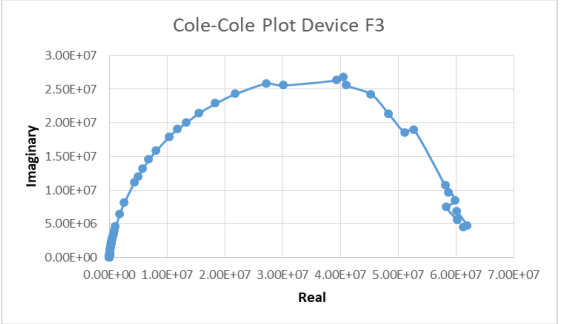
Figure 75 shows the IS results for the 26.7nm copper samples (Runs 5, 11, and 12).



(a)



(b)

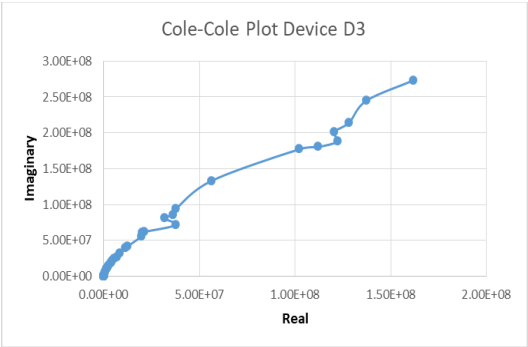


(c)

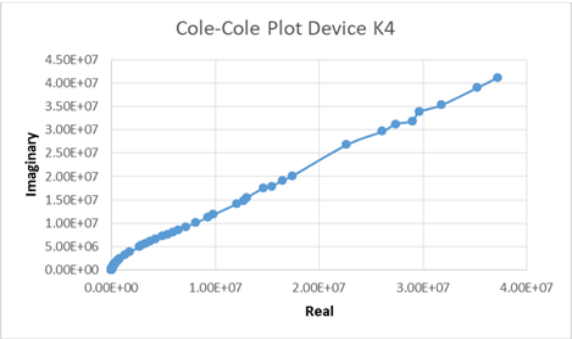
Figure 75: Impedance Spectroscopy Characteristics for the 26.7 nm Samples. (a) is 125C for 40 minutes, (b) is 140C for 20 minutes, and (c) is 155C for 60 minutes

Figure 75 shows the Cole-Cole plots for representative devices in the samples with 267A of Cu. Figure 75(a) is for the sample annealed at 125C for 40 minutes with a capacitance (100KHz) of 16.1 pF. Figure 75(b) is for the sample annealed at 140C for 20 minutes with a capacitance of 15.6 pF. Figure 75(c) is for the sample annealed at 155C for 60 minutes with a capacitance of 9.5pF. The Cole-Cole plots show that even at the highest temperature, the tested device in Figure 75(c) still passes as a capacitive device and was not shorted out.

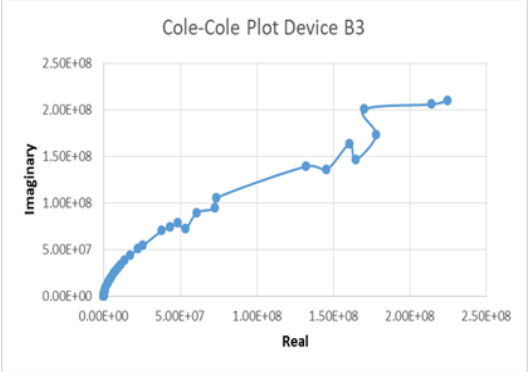
Figure 76 shows the IS results for the 23 nm copper samples (Runs 7,8, and 9).



(a)



(b)

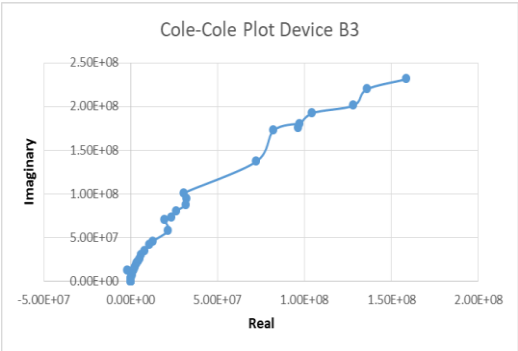


(c)

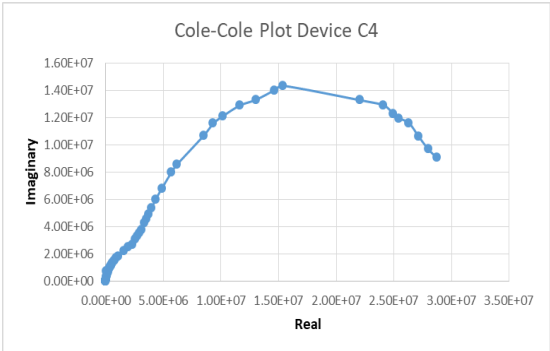
Figure 76: Impedance Spectroscopy Characteristics for the 23 nm Samples. (a) is 125C for 60 minutes, (b) is 140C for 40 minutes, and (c) is 155C for 20 minutes

Figure 76(a) is for the sample annealed at 125C for 60 minutes. Figure 76(b) is for the sample annealed at 140C for 40 minutes. Figure 76(c) is for the sample annealed at 155C for 20 minutes. These samples also pass the test as far as remaining capacitive after heating. Further tests will be required to see the change in capacitance with heating and obtain the dielectric constant at high frequencies.

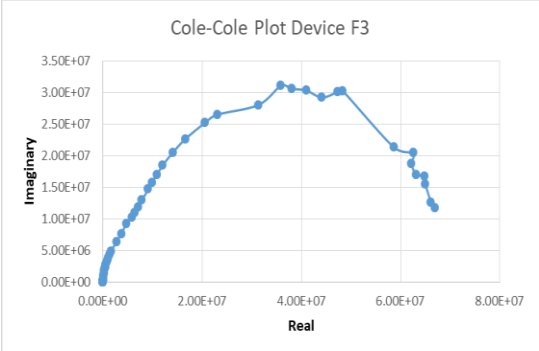
Figure 77 shows the IS results for the 20 nm copper samples (Runs 4, 6, and 10).



(a)



(b)



(c)

Figure 77: Impedance Spectroscopy Characteristics for the 20 nm Samples. (a) is 125C for 20 minutes, (b) is 140C for 60 minutes, and (c) is 155C for 40 minutes

Figure 77 shows the Cole-Cole plots for representative devices in the samples with 20 nm of Cu. Figure 77(a) is for the sample annealed at 125C for 20 minutes. Figure 77(b) is for the sample annealed at 140C for 60. Figure 77(c) is for the sample annealed at 155C for 40 minutes. Once again, all the samples remain capacitive. Further tests are required for the change in capacitance with heating and the dielectric constant.

Initial tests on devices with similar areas on samples heated at 125C and 155C show a significant reduction (about 45%) in capacitance at 100kHz (selected for low noise as shown in the Cole-Cole plots). This is likely due to the surface copper oxidizing and therefore reducing the top electrode area and the oxidized copper adding a series

capacitance to the WO_3/Cu dielectric. As stated before, further testing will be needed to determine how the capacitance changes. The study of the capacitance change can show the removal of shorting metallic copper with increasing temperature and time.

HORIZONTAL RESISTANCE TESTS

Figure 78 shows the method of testing the lateral resistance. The reason for this test was to test for the presence of metallic copper on the surface of the electrolytes where the filaments will grow. Enough metallic copper in the electrolyte can cause a shorting path for the three-terminal devices and the filaments will not grow.

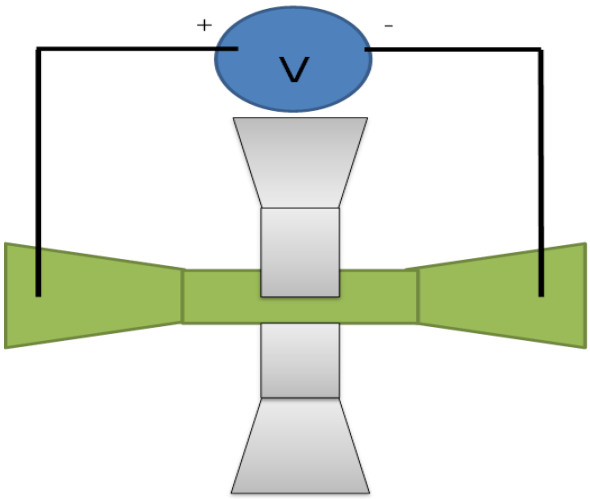
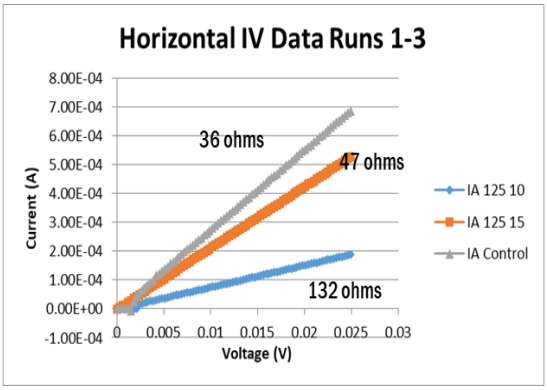
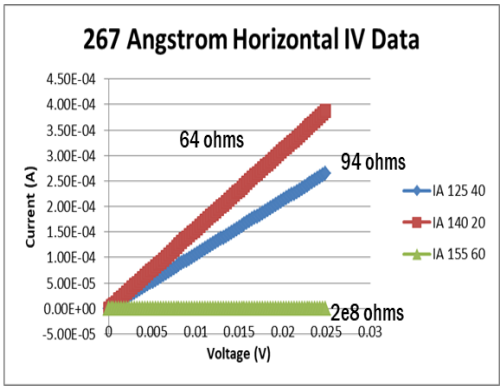


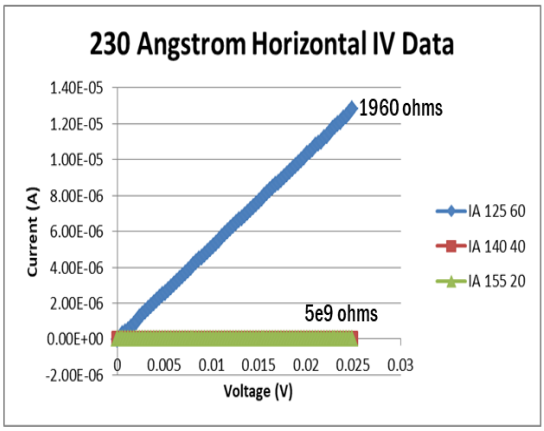
Figure 78: Horizontal Resistance Test Method using the 4156 Analyzer



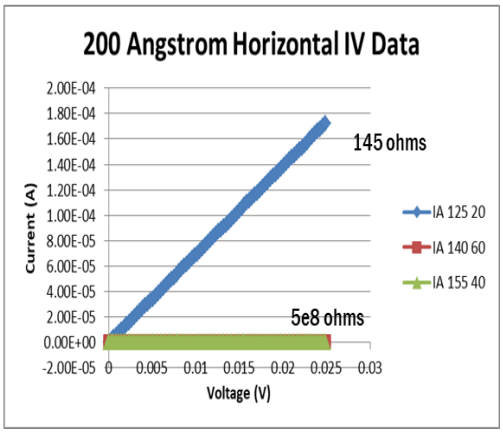
(a)



(b)



(c)



(d)

Figure 79: Horizontal resistance data for all samples

The control and minimally heated sample are shown in Figure 79(a). From the IS tests in the previous section, the devices were capacitive. As shown above, it is not because the WO_3 layer. The copper still remains on the surface and will be a shorting path.

As the data from Figure 79(b) shows, the 125C and 140C annealed sample devices show that there is enough metallic copper to cause a short on the devices. Again, the devices are capacitive because of the WO_3 layer. The resistance for the 125C sample is 94 ohms and the 140C sample is 64 ohms. The sample annealed at 155C has a resistance of 2E8 ohms. This means that it completely removed all metallic copper from the surface

through both oxidation and diffusion. Per the IS test, the 155C sample is still capacitive, indicating no shorting of the device.

For the data shown in Figure 79(c), only the 125C annealed sample at a resistance of 2000 ohms shows that there is still some metallic copper on the surface. The 140C sample at 5E9 ohms and the 155C also at 5E9 ohms show total removal of metallic copper. Again, these devices are all capacitive per the IS tests.

For the data shown in Figure 79(d), only the 125C annealed sample at a resistance of 145 ohms shows that there is still a lot of metallic copper on the surface. The 140C sample at 5e8 ohms and the 155C also at 5E8 ohms show total removal of metallic copper on still capacitive devices.

As shown in the data above, 125C annealing temperatures do not totally eliminate shorting metallic copper for any anneal time period. 140C samples require at least 40 minutes and 155C samples can even eliminate the metallic copper on the surface with 20 minutes of anneal time. Per the IS tests, even the devices that are heated at 155C do not short from the top electrode to the bottom. This means that the devices will function as capacitance sensors even at the highest temperatures.

VERTICAL RESISTANCE TESTS

Figure 80 shows the testing method for vertically measuring the resistance through the device. The IV data is obtained sweeping from 0-25mV and measures the current from bottom electrode to the top electrode.

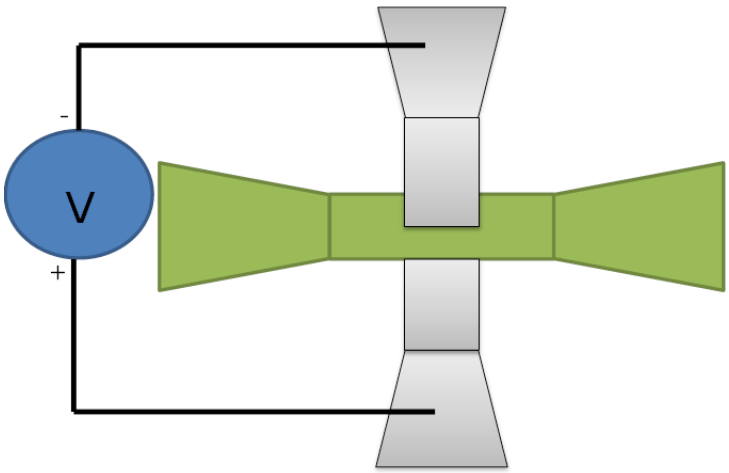


Figure 80: Vertical Resistance Test Method using the 4156 Analyzer

The reason for this test was to check whether driving the copper through the WO_3 can cause the device to short from the top to the bottom electrode. It can be used to confirm the results of the IS tests. Figure 81 shows the results for the vertical resistance for all samples:

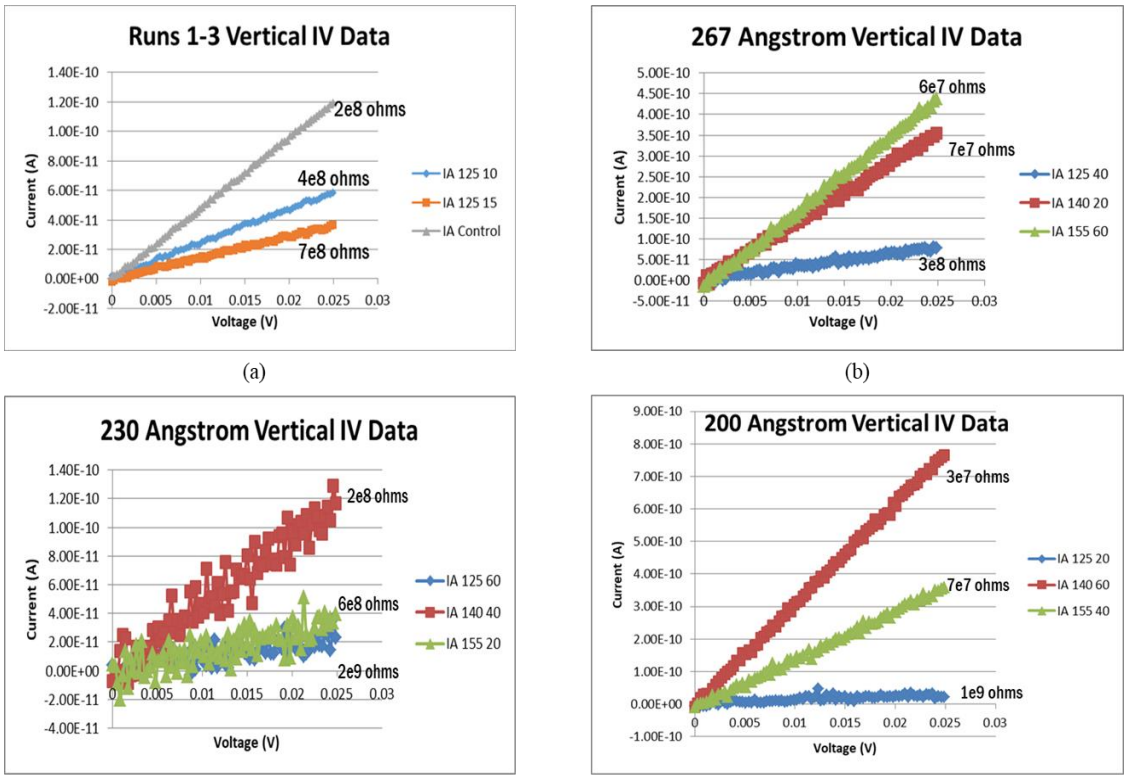


Figure 81: Vertical Resistance Data for all samples

The control samples in figure 81(a) have high vertical resistance but low horizontal resistance. This means that the resistance is mainly due to the WO_3 since the copper has not really dissolved or oxidized.

The data in Figure 81(b) shows that the annealing the Cu/WO_3 layer does not short the device at even the highest time and temperature. The 125C sample had copper on the surface and so the resistance is of mostly WO_3 and it is 3E8 ohms. The 140C and 155C samples are at 7E7 ohms and 6E7 ohms respectively. The 140C 20 minute sample also had low horizontal resistance and so the vertical resistance is due mainly to WO_3. However, the 155C 60 min had very high horizontal resistance. The vertical resistance for the 155C sample is still relatively high even with the copper oxidizing and being

driven through. This signifies that the copper being driven through does not, in fact, short the device.

The data in Figure 81(c) shows that once again that annealing at the highest temperature did not short the device. The 125C sample which still had a lot of surface metallic copper had a vertically measured resistance of 1E9 ohms due to the WO_3. The 140C and 155C samples had resistances of 2E8 ohms and 6.5E8 ohms respectively even with copper driven through the WO_3. Once again, this means no shorting through the device.

The data from Figure 81(d) also shows that the devices did not short out. The 125C sample which still had a lot of surface metallic copper had a vertically measured resistance of 1E9 ohms mainly due to WO_3. The 140C and 155C samples had resistances of 2E7 ohms and 7E7 ohms respectively. Again, this means no shorting through the device.

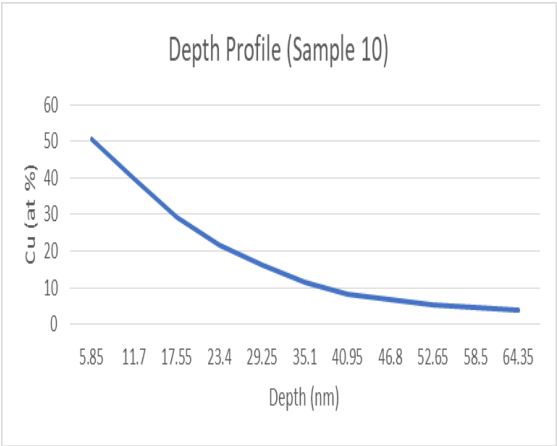
These tests show that the copper does not short the devices even at the highest temperature and time in the DOE. This means that a nitride or oxide layer isolating the buried electrode from the device is not required. This saves 2-4 hours of processing time in the cleanroom per wafer or sample made.

Horizontal and vertical tests and if possible, capacitance tests, should be initially performed on three-terminal devices when the electrolyte step is being processed to make sure that the copper is being driven through and not shorting the device. After annealing and depositing the electrodes, dendritic growth rate tests should be performed to check how the annealing process and amount of copper affect the growth rates.

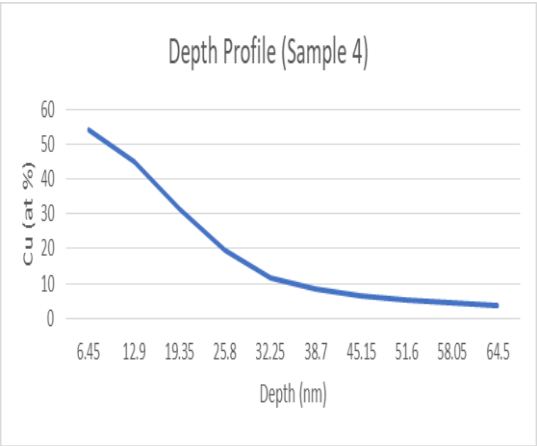
MATERIALS ANALYSIS

The materials analysis was performed by Mehmet “Bugra” Balaban. These results confirm that the copper, when diffused into the electrolyte does not short the device. Keep in mind that the copper deposited on the electrolyte does oxidize due to the oven heat and the air in the oven [19][20][21][22].

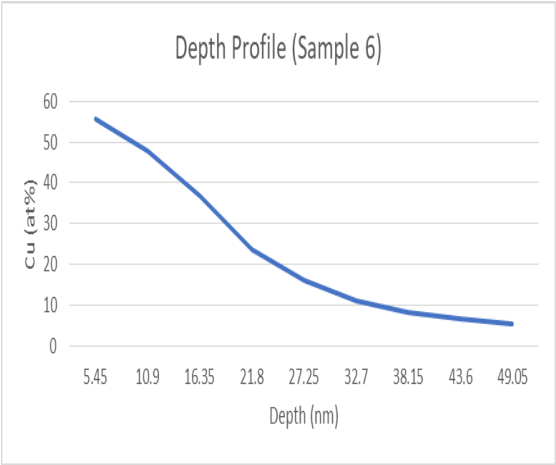
The copper depth profile was obtained using X-ray photoelectron spectroscopy (XPS) performed on witness samples with. Figure 82 shows the depth profile for the 20 nm samples which come from runs.



(a)



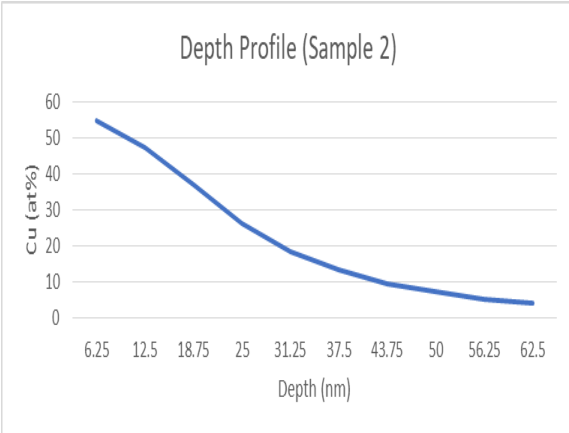
(b)



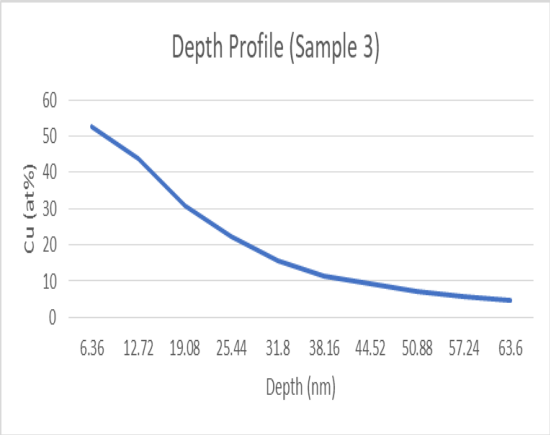
(c)

Figure 82: Copper depth profile from XPS for 20 nm samples, (a) is 125C for 20 minutes, (b) is 140C for 60 minutes, and (c) is 155C for 40 minutes

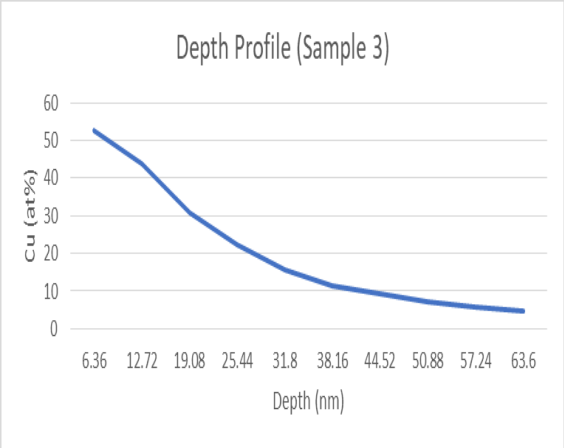
As shown above, the copper atomic percent reduces all the way down to 5% at the lowest depth taken. This is for all the temperatures and times. This indicates that the diffused copper does not form a path that will short the device to the buried electrode, thereby confirming the electrical results. Figure 83 shows the depth profile for the 23 nm samples



(a)



(b)

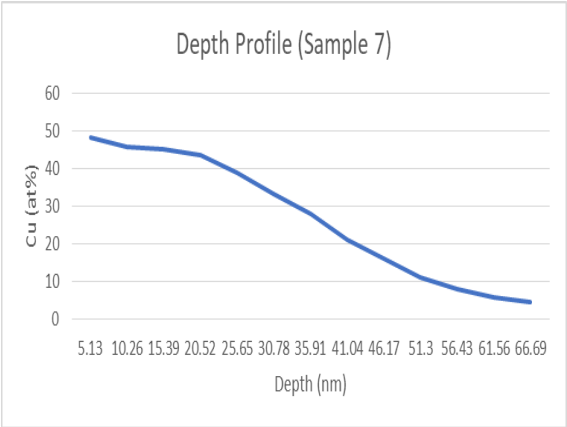


(c)

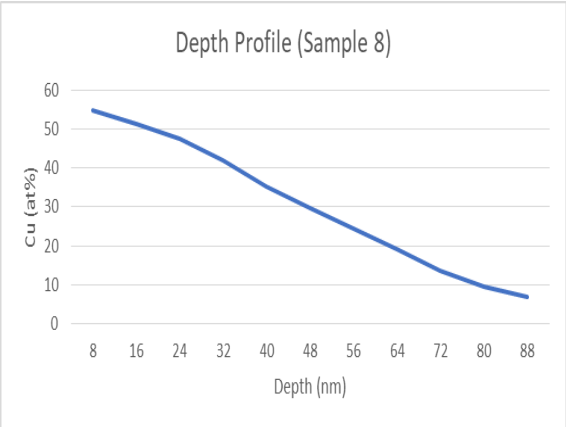
Figure 83: Copper depth profile from XPS for 23 nm samples, (a) is 125C for 60 minutes, (b) is 140C for 40 minutes, and (c) is 155C for 20 minutes

Again it is shown that at the copper atomic percentage drops quickly from the surface.

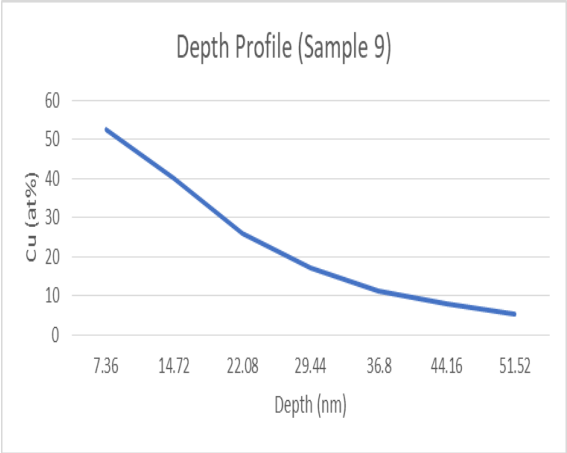
That leaves it no scope to form a shorting path to the buried electrode. Figure 84 shows the 26.7 nm samples.



(a)



(b)



(c)

Figure 84: Copper depth profile from XPS for 26.7 nm samples, (a) is 125C for 40 minutes, (b) is 140C for 20 minutes, and (c) is 155C for 60 minutes

Once again the depth profile in Figure 84 shows no scope for shorting the device to the buried electrode. This shows that for the WO_3/Cu devices have no need for an isolation layer to the buried electrode as confirmed by the electrical characterization. This removes the RPCVD step and the etching to the buried electrode step described in the three-terminal device section. Essentially, the materials analysis confirms what the electrical characterization also showed.

CONCLUSION

Tungsten trioxide and copper PMC devices have great applications as dendritic identifiers and odometer devices. The rate of filament growth is sensed through changes in capacitance and tells an end-user how long the device that the PMC is attached to has been running. The dendrites grow, in similar fractal patterns as chalcogenide devices, making it a good fingerprint for any hardware it is attached in addition to being an odometer for the hardware. This quality of the PMC will enable manufacturers and end-users to identify their devices and discard any device that is being used to circumvent any security measures put in place by the end-user of that device.

There are two main advantages to using the oxide/copper combination as a solid electrolyte for these capacitance change PMCs. Relative to chalcogenides, they are very slow in growing filaments and hence can be used as an odometer for a very long time. The other advantage is that the oxide/copper combination also very industry friendly and will not require a lot of adjustment on the part of fabrication and manufacturing facilities. It is also worthy of note that while some of the surface copper on the WO_3 oxidizes during the process, it does not stop the dendrites from growing. The exact nature of dendritic growth on/in this electrolyte requires further study. The oxidation of copper may be a possible passivation layer to protect the electrolyte from environmental effects.

As an odometer device that functions as a capacitance sensing device, the important parameter for these devices is the dendritic growth rate. Two-terminal PMC devices were tested in samples containing varying amounts of copper in WO_3. In some test cases, there was no discernible pattern between rates of growth, applied field to the PMC, and the electrolyte chemistry. However, it can be generally stated that the higher the amount

of copper in the electrolyte and the higher the applied field to a PMC in a given sample, the faster the filaments grow from cathode to anode. The reason for the lack of pattern in some cases is the uniformity of copper distribution in the solid electrolyte. Further processing and testing is required to garner a more insight into the relationship between electrolyte composition, applied fields, and dendritic growth rates.

Tests on the chalcogenide based three-terminal devices and the WO_3/Cu based devices showed that the latter electrolyte is a lot slower than the former. The difference in the number of pulses required to short the device in the WO_3/Cu matrix versus the chalcogenide devices is orders of magnitude. This is true even with 4 times the input voltage signal applied to the chalcogenide devices. These tests show that the WO_3/Cu devices can be used for a significantly longer time period than the chalcogenides as odometer devices when operated at similar biases.

Copper diffusion into tungsten trioxide was achieved thermally by heating the mixture in a convection oven. It was desirable to study the nature of that diffusion after heating the electrolyte. Specifically it was important to check whether the diffusion of copper would cut through the electrolyte. This study would help determine whether an isolation layer to protect the sensing electrode was required. Materials analysis and electrical characterization show that the diffusing copper did not provide a shorting path through the device, even when the mixture was heated at high temperatures. This means that, as long as the distribution of copper in WO_3 is uniform, there is no concern about a shorting path in the device even when annealed for high temperature and long time periods (1 hour). What this means is that a few hours of processing time is saved by not requiring

the isolation layer and by testing the electrolyte using the methods discussed above, one can determine whether a device will succeed or fail.

While, dendritic growth has been successfully demonstrated in tungsten trioxide and copper PMC devices and a general relationship has been established between field, chemistry, and filament growth rates, more study is required to determine the exact nature of WO_3/Cu chemistry. Future work will require more two-terminal testing to optimize the electrolyte chemistry and more three-terminal testing of the optimized electrolyte.

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