Single-Chip Isolated DC-DC Converter with Self-Tuned Maximum Power Transfer Frequency

by

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ABSTRACT

There is an increasing demand for fully integrated point-of-load (POL) isolated DC-DC converters that can provide an isolation barrier between the primary and the secondary side, while delivering a low ripple, low noise regulated voltage at their isolated sides to a high dynamic range, sensitive mixed signal devices, such as sensors, current-shunt-monitors and ADCs. For these applications, smaller system size and integration level is important because the whole system may need to fit to limited space. Traditional methods for providing isolated power are discrete solutions using bulky transformers. Miniaturization of isolated POL regulators is becoming highly desirable for low power applications.

A fully integrated, low noise isolated point-of-load DC-DC converter for supply regulation of high dynamic range analog and mixed signal sensor signal-chains is presented. The isolated DC-DC converter utilizes an integrated planar air-core micro-transformer as a coupled resonator and isolation barrier and enables direct connection of low-voltage mixed signal circuits to higher supply rails. The air core transformer is driven at its primary resonant frequency of 100 MHz to achieve maximum power transfer. A mixed-signal perturb-and-observe based frequency search algorithm is developed to improve maximum power transfer efficiency by 60% across the isolation barrier compared to fixed driving frequency method. The isolated converter's output ripple is reduced by utilizing spread spectrum clocking in the driver. An isolated PMOS LDO in the secondary side is used to suppress switching noise and ripple by 21dB. Conducted and radiated EMI distribution on the IC is measured by a set of integrated ring oscillator

based noise sensors with -68dBm noise sensitivity. The proposed isolated converter achieves highest level of integration with respect to earlier reported integrated isolated converters, while providing 50V on-chip junction isolation without the need for extra silicon post-processing steps.

ACKNOWLEDGMENTS

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CHAPTER 1 INTRODUCTION

1.1 Background

Fully integrated isolated DC-DC converters are an essential component in power monitoring, biomedical, and motor control applications where ground isolation is required. There are several applications that require traditional low-voltage CMOS data acquisition circuits to interface with very high common mode voltages. These include current sensors that have to operate at the high side of a voltage source, solar converters and inverters, DC motor controllers, FET drivers that have to switch high voltages and eMeter data products for smart grid management. These popular applications of isolated DC/DC converter are shown in Figure 1.

Figure 1: Sample Applications of Isolated DC-DC Converter

1.2 Motivation for Integration

There is an increasing demand for fully integrated isolated DCDC converters that can provide an isolation barrier between the primary and the secondary side, while delivering a low ripple, low noise floating voltage source in their isolated sides. A typical system block diagram of high-side current sensor signal chain application along with an isolated DC-DC converter is depicted in Fig. 1. The isolated DC-DC converter consists of a driver, a transformer, a rectifier and a regulator. The transformer provides the required electrical isolation, whereas the driver and the rectifier perform DC-AC and AC-DC conversions, respectively.

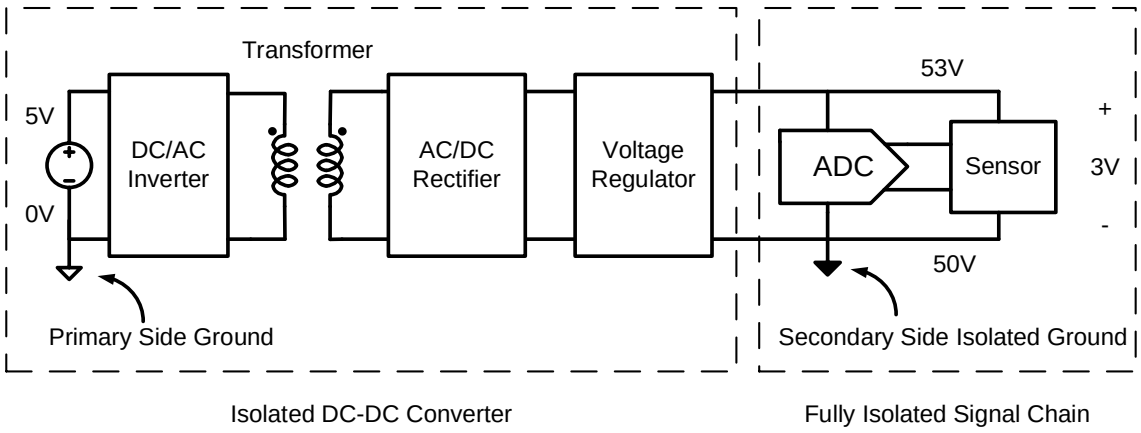


Figure 2: Typical System Level Application of An Integrated Isolated DC-DC Converter for Sensor Applications

Traditional methods for providing isolated power are discrete solutions using bulky components [1]. Miniaturization of isolated POL regulators is becoming highly desirable

for low power applications. Several levels of integration for isolated converters have been developed. In [2], a micro-transformer on silicon with magnetic core fabricated by silicon post-processing for isolation is presented. However, the converter, the transformer, and other components are implemented on separate IC's. In [3], a multi-chip module with several ICs packaged together is presented, where the micro-transformer with Aluminum (Au) thick metal and polyimide isolation layer is developed in a separate IC. These approaches minimize the converter size significantly. However, the complexity of these solutions is not compatible with large-scale and low-cost fabrication. In [4], integrated transformer is fabricated by standard BCD process to minimize the chip area, but multi-chip module is used and its power delivery ability is limited to 30mW. Furthermore, since all of these approach use fixed driving frequency, both power supply and EMI noise are concentrate at this frequency and may not suitable for low noise applications.

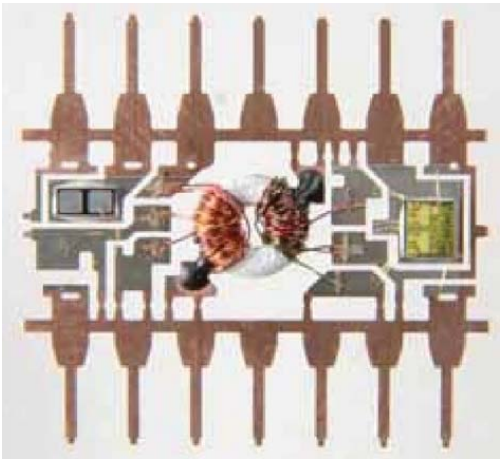


Figure 3: Discrete Type Isolated Dc/Dc Converter

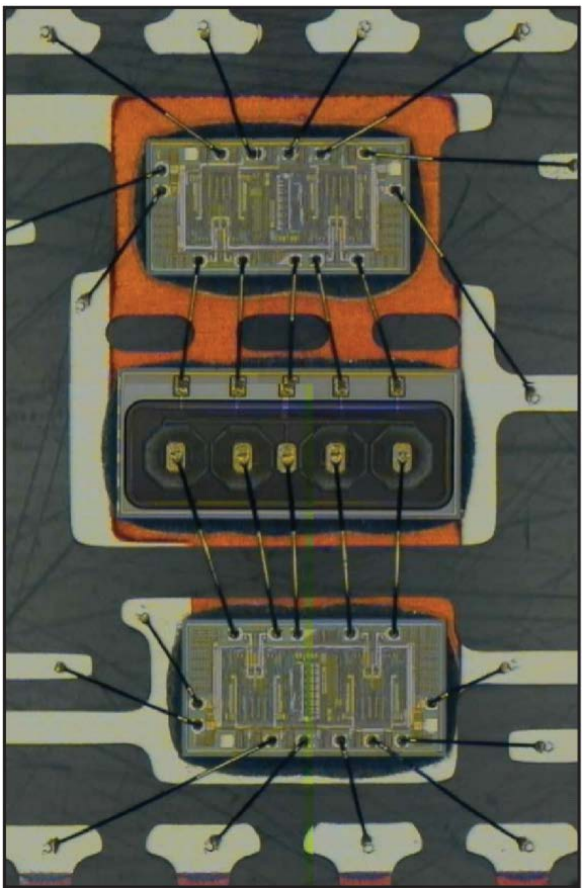


Figure 4: Partially Integrated Type Isolated Dc/Dc Converter [3]

In this paper, a single-chip fully integrated low-noise isolated point-of-load DC-DC converter design in a 6 level-metal 180nm CMOS technology is presented. To achieve high level of isolation without the need for additional process steps, a planar metal-metal transformer coupled resonator is utilized. To realize on-chip isolation, deep-nwell is utilized to provide 50V electrical isolation between the primary and secondary sides. The primary side use standard 5V devices without isolation well and secondary side uses 5V device and all secondary side devices are inside 50V isolation wells. Isolation rating

depends on process capability, and 50V isolation is used for mixed signal system integration possibility, much higher isolation can be achieved by using SOI process. Due to process variations, as well as load dependent variations in the peak power transfer frequency in the isolation transformer, a peak power transfer frequency detection circuit at the primary side sweeps the switching frequency of the driver to detect the maximum power transfer while the spread spectrum function is used to reduce output peak voltage ripple and on-chip EMI.

The proposed isolated converter is used for power, high dynamic range, low noise mixed signal sensor signal applications. To characterize the impact of on-chip driver, inductor and rectifiers, the isolated converter also has integrated radiated and conducted EMI noise sensors to measure the on-chip EMI distribution. One of the previous radiated EMI sensing methods used an off-chip coil array to measure the EMI noise [5]. Another method uses a sample and hold circuit to detect the on-chip EMI noise [6]. However, the sampled EMI noise signals routed within and outside the IC pick up additional noise, resulting in an inaccurate EMI measurement. The proposed integrated ring oscillator based EMI sensor acts as a frequency modulator to the EMI noise and provides an accurate sensed EMI noise distribution.

1.3 Organization

The remainder of this paper is organized as follows. Chapter 2 begins with an overview of architecture selection criteria of fully integrated isolated DC-DC converter. Three type of isolation method is discussed. Then proposed converter architecture is

introduced. Also LC coupled resonator model is analyzed. Chapter 3 first introduce air core transformer. Then HFSS modeling and simulation results of the transformer is presented. Finally, the testing results and the comparison to the previous simulation results are discussed. Chapter 4 introduces details of converter circuit implementation including maximum power delivery frequency control and EMI noise control. Finally, the test setup and test results of the DC-DC converter along with the measured EMI noise distribution are presented in Chapter 5.

CHAPTER 2 ARCHITECTURE OF ISOLATED DC-DC CONVERTER

When designing this isolated dc-dc power converter, the first and most critical choice is selection of the topology. This fully integrated DC-DC converter architecture is selected based on two considerations. Firstly the architecture should be able to integrate on the silicon wafer as this is the key to achieve highest power density and reliability. Secondly, the converter should have the sufficient power delivery ability in order to realize maximum power delivery in limited chip area. Typical signal chain application like ADC consumes about 50mW, this is the target power level for the converter.

2.1 Integrated Isolation Type Comparison

Traditionally, several integrated isolation approaches including transformer isolation, capacitive coupling, switched capacitor power transfer and optical coupling are introduced to provide isolation for different applications.

The Basic Theory Optical isolation has two basic elements: a light source (usually a light emitting diode) and a photo-sensitive detector. As shown in Fig. 5, these two elements are positioned facing one another and inserted in an electrical circuit to form an opto-coupler. The key property of an opto-coupler is that there is an insulating gap between the light source and the detector. No current passes through this gap, only the desired light waves representing data. Thus the two sides of the circuit are effectively "isolated" from one another. Primary Application In data communications, the primary application for optical isolation is in a point-to-point data circuit that covers a distance of several hundred feet or more. Because the connected devices are presumably on different power circuits, a ground potential difference likely exists between them. When such a

condition exists, the voltage of "ground" can be different, sometimes by several hundred volts. [7]

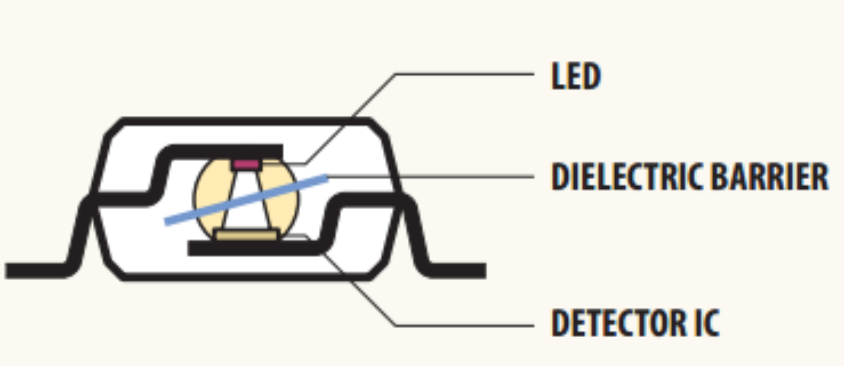


Figure 5: Isolated Capacitive Coupling DC-DC Converter

In capacitive coupling, an LC resonant tank is used for power transfer. Simplified architecture for a capacitive coupling power converter is shown in Fig. 6. Two identical capacitors C_{R1} and C_{R2} together with two identical inductors L_{R1} and L_{R2} are used to form a series resonator. This approach is used in LED driver applications [8] and data transfer applications [9]. However, since it depends on capacitors for isolation, a high voltage compliant process is needed for the capacitor integration. Other than process compatibility, all capacitors and inductors occupy large chip area.

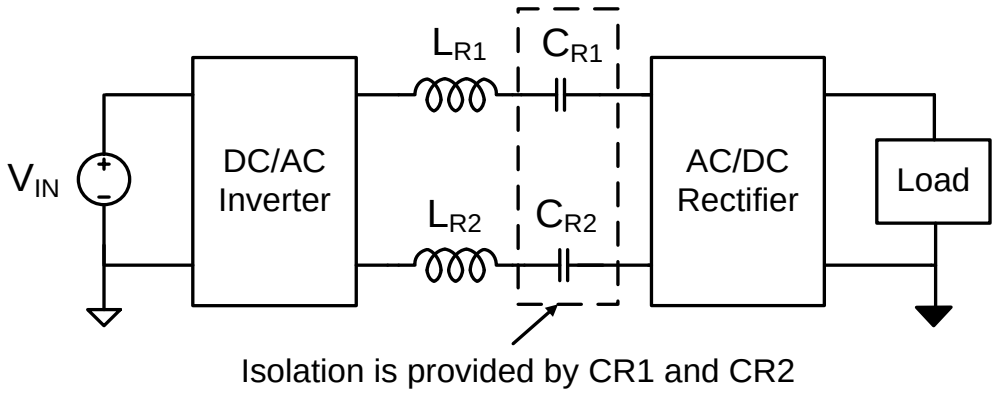
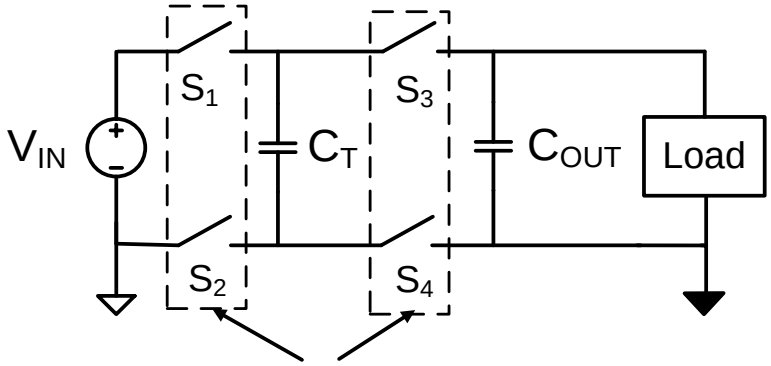
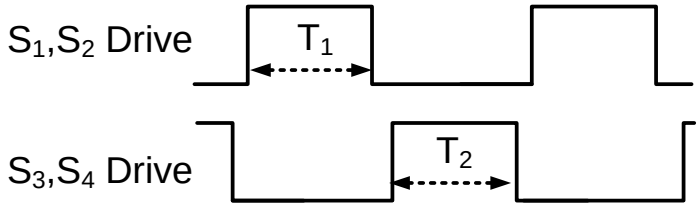


Figure 6: Isolated Capacitive Coupling DC-DC Converter



(a)



(b)

Figure 7: Isolated Switched Capacitor DC-DC Converter

An isolated switched capacitor DC-DC converter was introduced in [10] and [11]. This approach utilizes semiconductor switches to provide isolation. Its structure and control signal is shown in Fig. 7. C_T is used for transfer power from the V_{IN} to the load. During φ_1 phase, S_1 and S_2 are turned on and C_T is connected to the input voltage V_{IN}. During φ_2 phase, S_3 and S_4 are turned on and C_T is connected to the output capacitor C_{OUT} and load. This solution eliminates magnetic components, however, it requires high voltage rating, low on-resistance switches. To realize isolation by using high voltage device is much harder than using isolation barrier between primary and secondary side circuits. Also, in order to drive the switches, isolated gate drivers are needed which creates even more isolation issues.

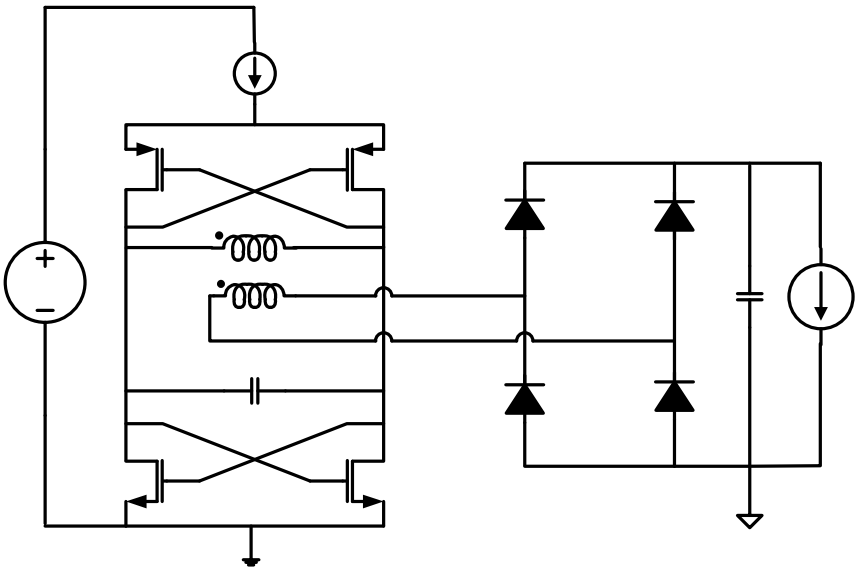


Figure 8: Cross-Coupled LC Tank Type Converter Schematic

A design example of DC-DC converter with cross coupled LC tank oscillator is presented in [3]. The block diagram is shown in Figure 8. The converter consists of LC

self-resonant tank (including the primary side of the transformer), power transformer, rectifier with smoothing capacitor, voltage regulator and an optional feedback path for optimal power transfer.

As shown in Fig. 8, one pair of PMOS switches and one pair of NMOS switches are cross-coupled to cancel the resistive loss and sustain the oscillation of the LC tank [3] [12]. The CMOS pair is used to achieve more positive gain because both the NMOS and PMOS are used to sustain the oscillation. Since the tank's inductor is the primary side coil of the power transformer which is coupled with the secondary side coil, the oscillation frequency is not only depend on the self-inductance of the primary coil and the primary capacitance, but also the mutual inductance and load capacitance.

The rectifier consists of four Schottky diodes forming a full-wave bridge rectifier. The Schottky diode has a lower forward voltage comparing to the general purpose diode, thus it can provide lower forward voltage drop in the rectification which can provide higher system efficiency. Besides, the Schottky diode can turn on and recover very fast[6], thus it can operate at high frequencies which is important for this application since the operating frequency of the transformer is high due to the limitation of the size.

In order to obtain the optimal power transfer efficiency, an optional feedback path can be used. The feedback path consists of a PI controller, PWM controller, encoder, data transformer and decoder. The PWM signal controls the switching action of the CMOS switches and will not change the operation frequency of the LC tank.

2.3 Proposed Architecture

The system level architecture of the proposed isolated DC-DC converter is shown in Fig. 9. An on-chip air-core transformer is designed for the isolation between input and output voltage domains. Primary side includes an H-bridge resonant driver, a peak power detector to detect the maximum power transfer frequency, and a spread-spectrum clock generator to reduce output peak ripple and EMI. The system operating frequency is limited by the driver conduction and switching losses, and the rectifier speed. In this design, the resonance frequency is designed to be around 100MHz as the optimum loss point between switching losses and transformer losses. Capacitor C_P, transformer inductance and rectifier capacitance form a resonator and set the resonant frequency. In order to transfer maximum power to the load, the switching frequency of the resonator driver is kept at the resonant frequency. Standard 5V Power switches M_{P1}, M_{P2}, M_{N1} and M_{N2} form the H-bridge. A ring oscillator and a non-overlapping clock generator create non-overlapped gate signals for the H-bridge driver as shown in Fig. 10. Compared to a half-bridge driver, the H-bridge structure doubles the voltage swing across both transformer input and output.

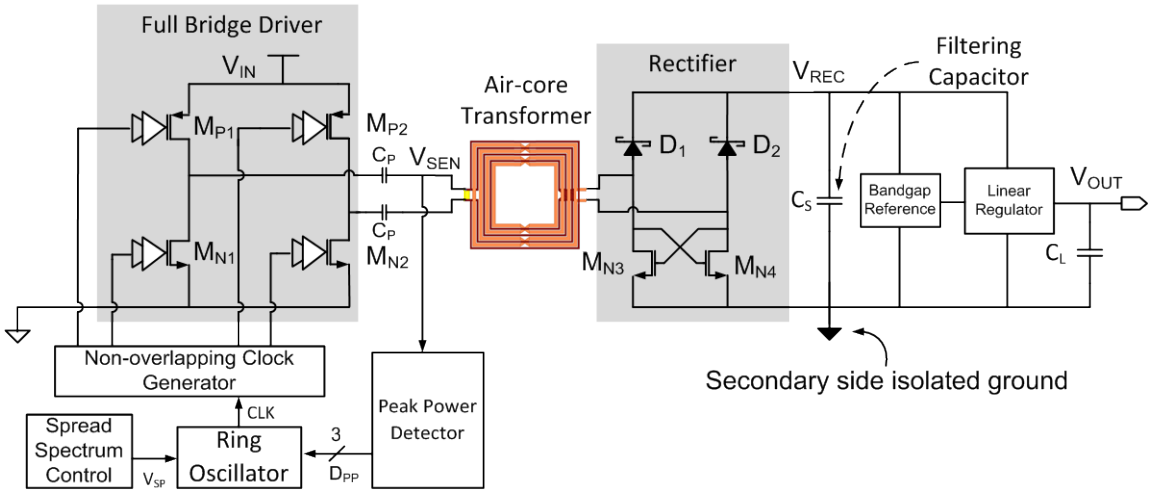


Figure 9: Proposed Isolated DC-DC Converter

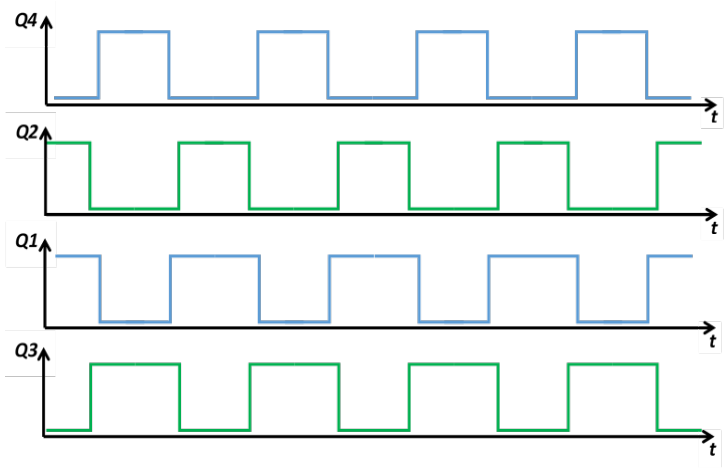


Figure 10: Non-Overlapping Clock Waveform

The secondary side consists of a full-bridge rectifier and a linear low drop-out (LDO) regulator. Usually active rectifier has better performance than passive type rectifier, however at the proposed switching frequency, active rectifiers have lower efficiency. Two Schottky diodes D_1 and D_2, and two cross-coupled NMOS transistors M_{N3} and M_{N4} are used in the rectifier. The MOS transistor gives lower forward voltage drop than a

diode, resulting in reduced loss compared to the conventional four diode bridge configuration. Since the proposed converter's design target is low power, low noise applications, efficiency is not a critical requirement and no feedback channel is used across the isolation barrier. Although its efficiency at low load condition suffers due to this, design complexity and die size is optimized. Since the isolated DC-DC converter is designed to provide regulated power to noise-sensitive circuits, an LDO is used to obtain both the output voltage regulation and the output ripple reduction.

The proposed converter works in two modes: peak power transfer frequency search mode at start-up and steady-state power transfer and regulation mode. At the beginning of the operation, the peak power detector circuit sweeps the ring oscillator frequency until the peak power transfer frequency is achieved. After the optimum switching frequency (f_{RES}) is obtained, the converter shifts to steady-state power transfer mode. At steady-state, to reduce the conducted and radiated EMI, spread-spectrum technique is enabled.

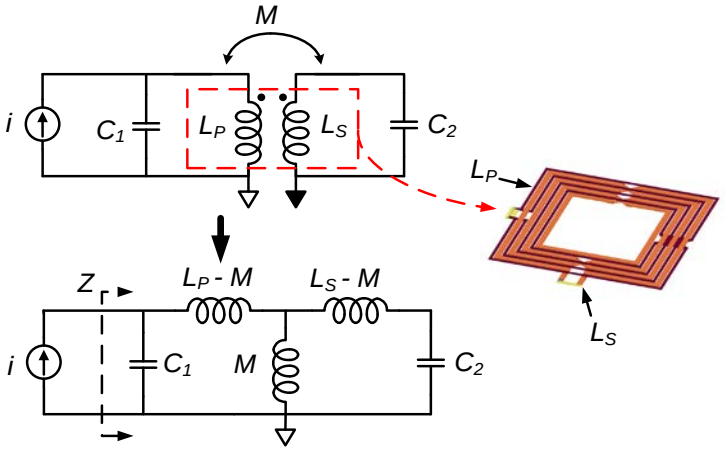


Figure 11: Equivalent Circuits of Transformer Coupled Resonator by Using T-Model

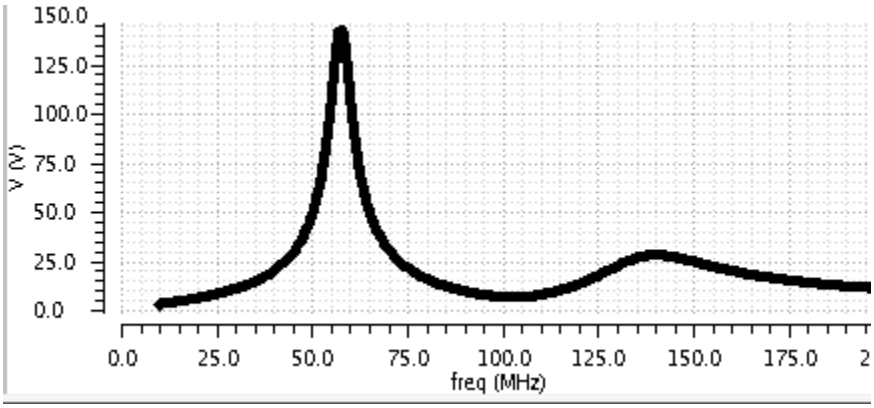


Figure 12: Example of Voltage Across Parallel LC Resonant Tank With Current Injection Across Frequency

The resonant frequency of the transformer coupled *LC* resonator can be analyzed by using the coupled resonator model shown in Fig. 11. The input equivalent capacitance C_1 is dominated by C_P while the output equivalent capacitance C_2 mainly comes from rectifier diodes and transistors. Both primary and secondary side resonant together at certain frequencies. The equivalent input impedance Z seen by the driver reaches its maximum at resonant frequency. If the L_P=L_S=L and C_1=C_2=C, the resonant frequency can be simplified as [13]

$$\omega_1^2|^{Transf} = \frac{1}{(L-M)C} \tag{1}$$

$$\omega_2^2|^{Transf} = \frac{1}{(L+M)C} \tag{2}$$

where M is the mutual inductance between the primary and secondary coils. If the serial resistance r is considered, the impedance for both resonant frequencies can be calculated as:

$$Z_{in}(\omega_1)|^{Transf} = \frac{L+M}{2rC} \tag{3}$$

$$Z_{in}(\omega_2)|^{Transf} = \frac{L-M}{2rC} \tag{4}$$

Clearly the resonating mode at low frequency $\boldsymbol{\omega_1}$ has higher input impedance and higher power transfer ability. Example of voltage across parallel LC resonant tank at different frequency is shown in Fig. 12. The peak power transfer frequency detection method is presented in the next section.

CHAPTER 3 AIR CORE TRANSFORMER DESIGN AND TEST

3.1 Transformer Basics

Fig. 13 shows an ideal transformer circuit model. The transformer can be treated as an electromagnetic energy converter [14] which consists of two or more magnetically coupled coils. A time-varying voltage applied at the primary side causes a time-varying current to flow, thus causing a changing magnetic flux in the core. The changing magnetic flux will induce a voltage at the secondary side. The core is made of ferromagnetic metals which have high permeability that increase the magnetic field. However, the ferromagnetic core is not compatible with the process and will have magnetic saturation and core losses which degrade the Q factor of the transformer.

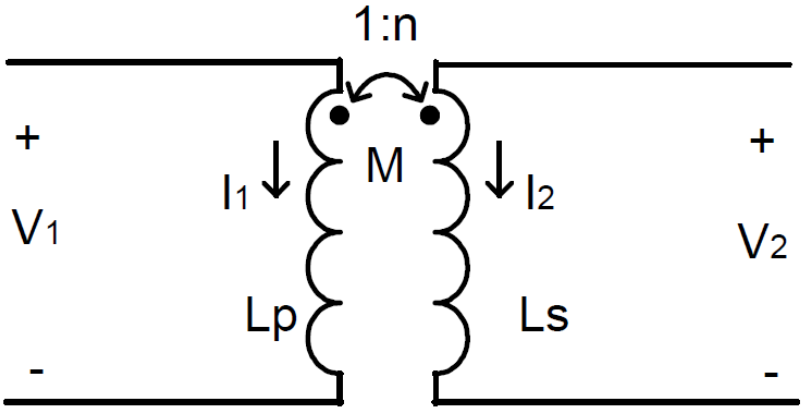


Figure 13: Ideal Transformer Circuit Model

The magnetic coupling coefficient *k* is given by

$$k = \frac{M}{\sqrt{L_P L_S}} \tag{5}$$

For an ideal transformer, k = 1. For most on-chip transformers, k is between 0.3 and 0.9 because of the leakage of magnetic flux. Other non-idealities of practical on-chip transformers include parasitic capacitance, resistances due to ohmic loss, skin effect, proximity effect and substrate eddy current. [18]

The ideal transformer model can be treated as a two port network with the following terminal voltages and currents relationship:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} j\omega L_P & j\omega M \\ j\omega M & j\omega L_S \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (6)$$

where L_P and L_S are the self-inductance of the primary and secondary side coil. M is the mutual inductance between the two coils. For ideal transformer, the power transfer will be lossless and magnetic flux is confined in the magnetic core, thus the following identity holds:

$$\frac{V_P}{V_S} = \frac{I_S}{I_P} = \frac{N_P}{N_S} = \sqrt{\frac{L_P}{L_S}} = n \quad (7)$$

where V_P and V_s are the primary and secondary voltage, I_P and I_S are the current flowing through the primary and secondary coil, N_P and N_S are the primary and secondary number of turns, n is for the turns ratio of transformer. If the two coils are perfectly coupled, k=1. Due to the leakage of magnetic flux caused by a lack of high permeability magnetic core in practical, the k for most on chip transformers is in the range of 0.3~0.9 [15] [16].

3.2 Transformer Design by HFSS

3-D EM simulation software is needed to get an accurate transformer model. HFSS is 3-D modeling and simulation software used for transformer design. For this project, 3-D structure of the transformer together with specification of material characteristics for the entire on chip structure and identify the excitation ports are required for simulation. HFSS then solves the model using finite-element-method and generates S-parameter matrix. The results are obtain by either choose to solve the model at a specific frequency or at different frequencies within certain range.

The specifications of the transformer can be calculated by the S-parameters. In the simulation, Primary side port is set to be port 1 and the secondary side port to be port 2. Thus the specifications can be calculated by:

$$L_P = \frac{im(Z_{11})}{2\pi f} \tag{8}$$

$$L_S = \frac{im(Z_{22})}{2\pi f} \tag{9}$$

$$Q_P = \frac{im(Z_{11})}{re(Z_{11})} \tag{10}$$

$$Q_S = \frac{im(Z_{22})}{re(Z_{22})} \tag{11}$$

$$k = \sqrt{\frac{im(Z_{12})im(Z_{21})}{im(Z_{11})im(Z_{22})}} \tag{12}$$

where L_P, L_S, Q_P, Q_S and k are respectively for the primary side inductance, secondary side inductance, primary side quality factor, secondary side quality factor and coupling coefficient between the two coils.

For the on-chip transformer of the isolated DC/DC converter, high coil inductance is the design target. The resonant frequency ω_0 and inductance value L have a relationship:

$$\omega_0 \propto \frac{1}{\sqrt{L}} \tag{13}$$

Thus, higher inductance value will give lower resonant frequency and hence the H-bridge driver can drive the LC tank at a lower frequency. This will reduce the switching loss happening at higher frequencies and also avoid transformer's non-idealities such as skin effect, proximity effect and substrate eddy current that come with high frequencies.

Since the transformer operates at the oscillation frequency of the coupled resonant tan. High quality factor is another design target such that the energy loss is small in the oscillation.

For the on-chip transformer, we need high coupling coefficient k between the two coils. In [17], one approach to calculate the power transfer efficiency η is given:

$$\eta = \frac{(k \cdot Q)^2}{\left[1 + \sqrt{1 + (k \cdot Q)^2}\right]^2} \tag{14}$$

where k is the coupling coefficient and Q is the quality factor. Fig. 14 shows the power transfer efficiency versus coupling coefficient for different Q values. It shows efficiency increases with increasing coupling coefficient.

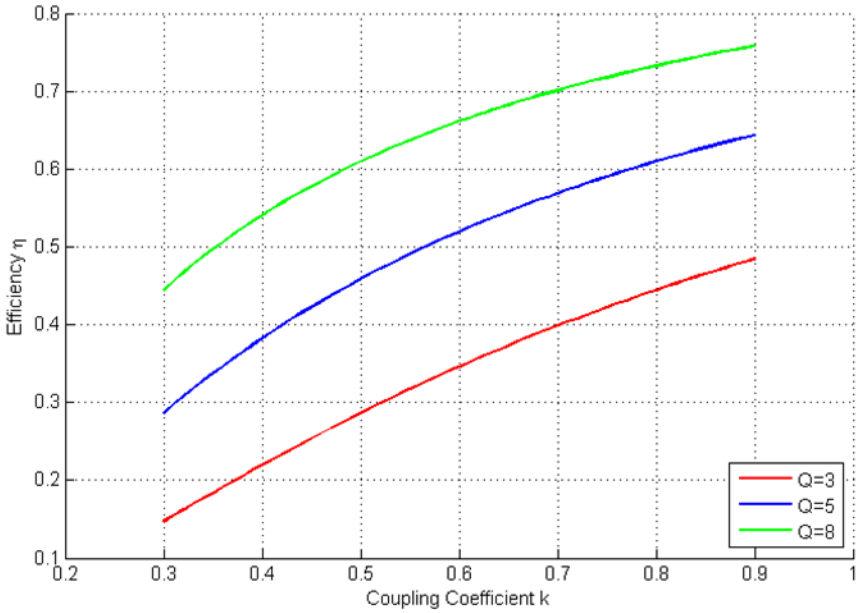


Figure 14: Efficiency vs. Coupling Coefficient for Different Q [18]

The HFSS-based transformer design flow is shown in Fig. 15. The design target is to let the transformer operate at around 100MHz with high efficiency. For different transformer designs, Quality Factor, Inductance and coupling coefficient are used to find the optimal design.

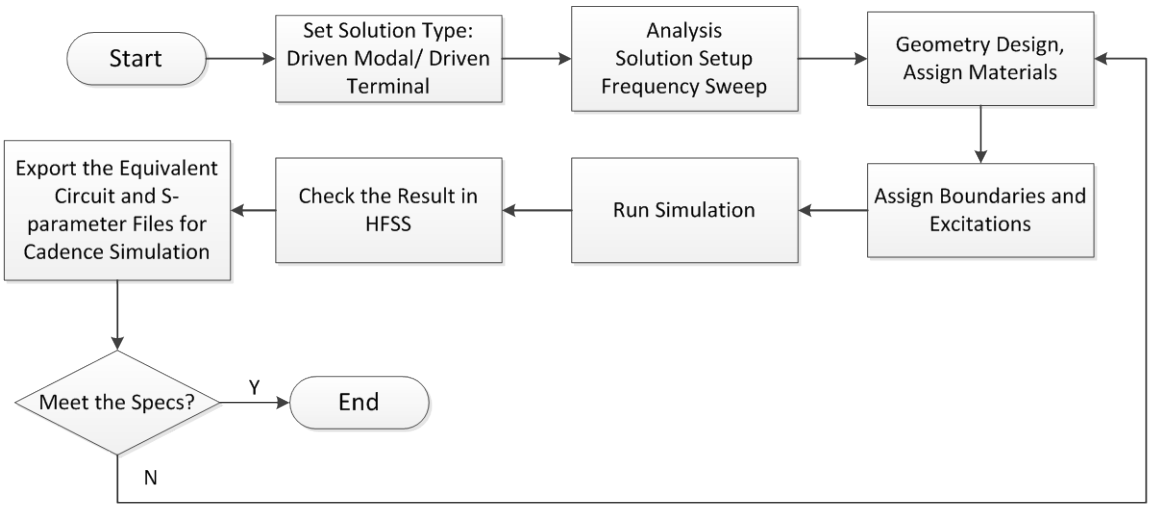


Figure 15: HFSS-Based Transformer Design Flow

AMS H18 process is used for the design. The process has 6 layers of metal with the thickest metal layer at the top. And also, the thickest metal layer sits on the thickest oxide layer, making it far away from the lower level metals. The five lower level metals have much thinner thickness than the top level metal and have certain metal density rules. The process has a poly-silicon layer that sits just on top of the substrate and the conductivity is lower than metal. In HFSS model design, the thickness of each metal and insulate layer is set to be the nominal value shown in the PDK manual. However, in the practical case, the thickness has a range to vary and this may cause some discrepancies between the simulation and measurement results. In the PDK manual, the conductivity of the metal layer is given in the form of sheet resistance. It is converted to bulk conductivity by equation (15) since HFSS material library can only accept this parameter. [18]

$$\sigma = \frac{1}{R_S \cdot t} \tag{15}$$

where σ is the bulk conductivity, R_S is the sheet resistance and t is the thickness of the layer.

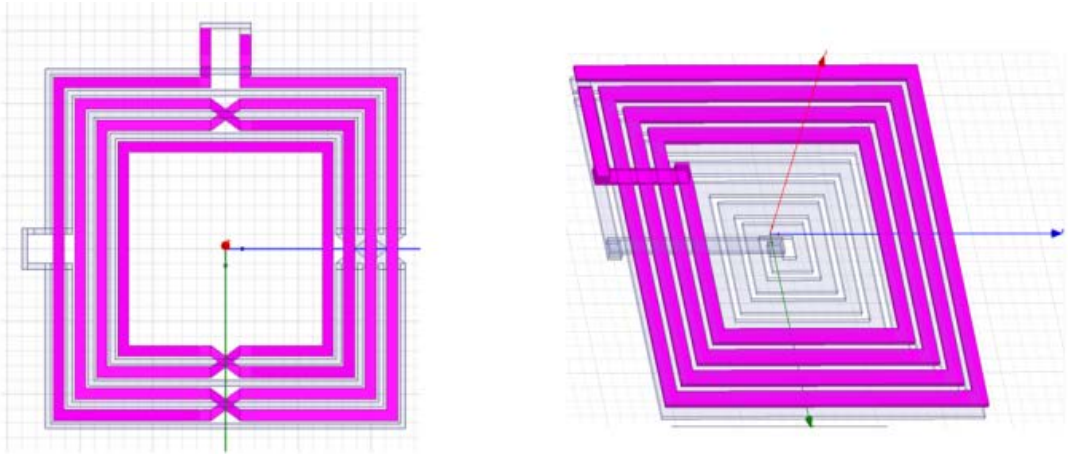


Figure 16: Transformers Structure: Planar And Stacked

For the transformer vertical structure, there are usually two types. One is the planar transformer with two coils fabricated in the same layer; the other is the stacked transformer with two coils fabricated in different layers. The two structures are shown in Fig. 16.

Both of the two structures have advantages and disadvantages. The process has 6 layers of metal. The top layer's thickness is 4um but the other layers are only 0.48um or 0.31um thick which have a higher sheet resistance. The thinner layer has high resistance than the top layer. The stacked structure uses multilayer metals to fabricate the coils. The resistive loss in the coils is high which cause low quality factor of the transformer. Thus,

planar structure is chosen to fabricate the coils at the top layer with underpasses in other layers. [18]

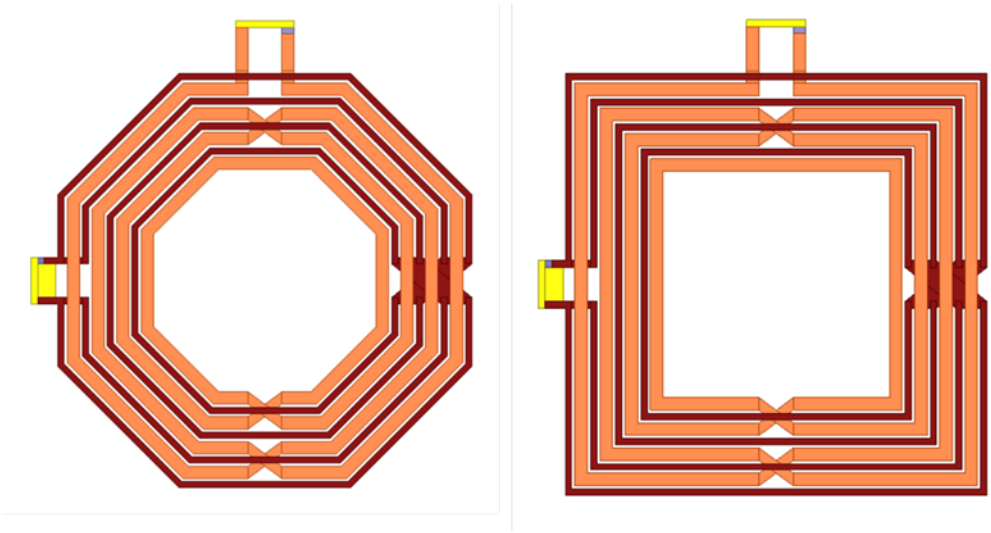


Figure 17: The Top-Down View of The Transformers: Octagonal Type And Square Type [18]

For the horizontal geometry of the transformer, not only the square shape but also the octagonal shape according is available according to the IC process design rule. Fig. 17 shows the top-down view of the two transformers. For both of the transformers, N_P:N_S=2:4, d_{out}=1.782µm, d_{in}=958µm, w=53.2µm, s_{Pri}=79.8µm, s_{Sec}=53.2µm. The simulation results at 100 MHz are shown in Table 1 below. The simulation results show that the coupling coefficients of the two transformers are close to each other. The square transformer has a primary inductance 1nH and secondary 5.2nH higher than the square shape. The contribution of the mutual inductance between the segments in the octagonal shape is not so significant comparing to the longer trace length and larger covering area

of the square shape transformer. For Q-factors comparison, square shape is slightly better than the octagonal one at 100MHz and it becomes much higher at higher frequencies. Thus, the square shape is chosen to obtain higher inductance and lower losses. [18]

Table 1: Simulation Results: Octagonal And Square Shape Transformers

	k	L_P	Ls	Q_P	Q_S
Octagonal	0.87	13.4nH	47.8nH	3.7	5.5
Square	0.86	14.4nH	53.0nH	3.81	5.74

At higher frequencies, the magnetic field generated by the transformer induces eddy current on the substrate. To reduce the loss, a ground shield is needed to reduce the eddy current and provide a ground connection. Thus, a PGS is often built underneath inductors and transformers for high frequency applications. To block the eddy current loop on the shield, it is shown in Fig. 18. The X pattern provides connection of each segment to ground.

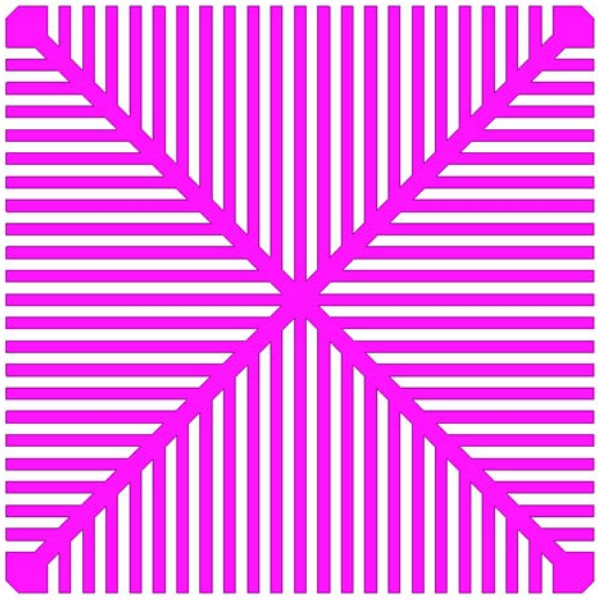


Figure 18: Patterned Ground Shield Structure of The Transformer [18]

The simulation results at 100MHz are shown in Table 2. Simulation results shows that the transformers with PGS have a higher inductance value comparing to the ones without a PGS; for transformers with metal PGS, the quality factor is degraded comparing to the ones with poly-silicon PGS and the ones without a PGS. The reason for this degradation is that the metal layer sits closer to the coil layer than the poly-silicon, creating a higher capacitance with the coil. The parasitic capacitance degrades Q. In addition, the PGS can reduce the effect of eddy current.

Table 2: Simulation Results: Without PGS, With Poly-Silicon PGS and With Metal PGS

	k	L_P	L_S	Q_P	Q_S
No PGS	0.84	9.8nH	33.3nH	3.34	5.87
Poly-silicon PGS	0.86	14.4nH	53.0nH	3.81	5.74
Metal PGS	0.83	11.2nH	37.8nH	2.31	2.8

Many standard IC processes require uniform metal density in the chemical-mechanical polishing (CMP) process [20]. Thus, the metal fills are put in the metal layers being used (except for the top layer where the transformer coils are built). The metal fill consists of an array of small dummy floating metal squares. HFSS model can provide information of the metal fill effect and save the simulation time. Fig. 19 shows the areas where to put the metal fills. The PGS is not shown for simplicity. The green square shows the metal fills consisting of M2~MT layers and the blue square area show the metal fills of M1 layer. Where M2~MT are the 2^{nd} to 5^{th} layers of metal from substrate and M1 is the first layer of metal.

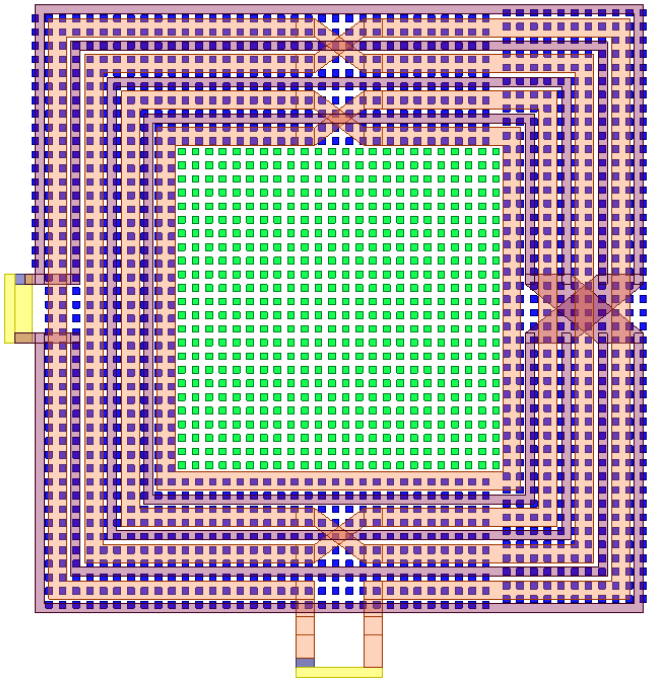


Figure 19: The Metal Fills Position of The Transformer Chip [18]

Final transformer design with dimension information is shown in Fig. 20. The results of the simulation are shown in Table 3. It is shown that the metal fills have very small effect to the performance of the transformer in the sense of inductance value, Q-factor and coupling coefficient. This is mainly because the size of the metal fill is too small to generate significant eddy current. Thus the loss caused by eddy current is small. The M1 layer fills area is overlapped with the transformer coil area, which decreases the distance from the coil to the PGS and substrate since M1 layer has physical thickness. Thus, the parasitic capacitance increases with decreased distance due to the sandwiched metal layer. However, this effect is also not so significant since the M1 layer is thinner than the other metal layers.

Table 3: Simulation Results: With Metal Fills and Without Metal Fills

	k	L_P	Ls	Q_P	Q_S
With Metal Fills	0.86	14.6nH	53.5nH	3.9	5.9
Without Metal Fills	0.86	14.4nH	53.0nH	3.8	5.7

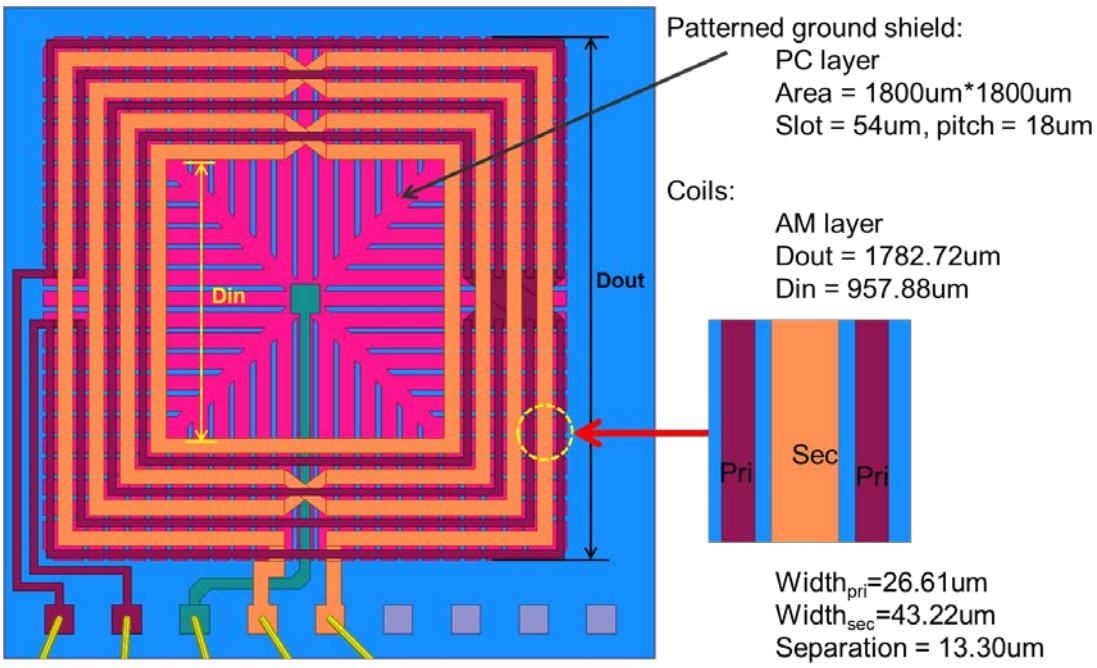


Figure 20: Final Transformer Design

3.4 Simulation and Test Results Comparison

The proposed on-chip transformer together with the Schottky diode based rectifier is implemented in high voltage AMS H18A6 0.18μm CMOS process. The die micrograph is shown in Fig. 21. The chip size is 2.236mm by 2.236mm. The transformer block size is 1.783mm by 1.783mm.

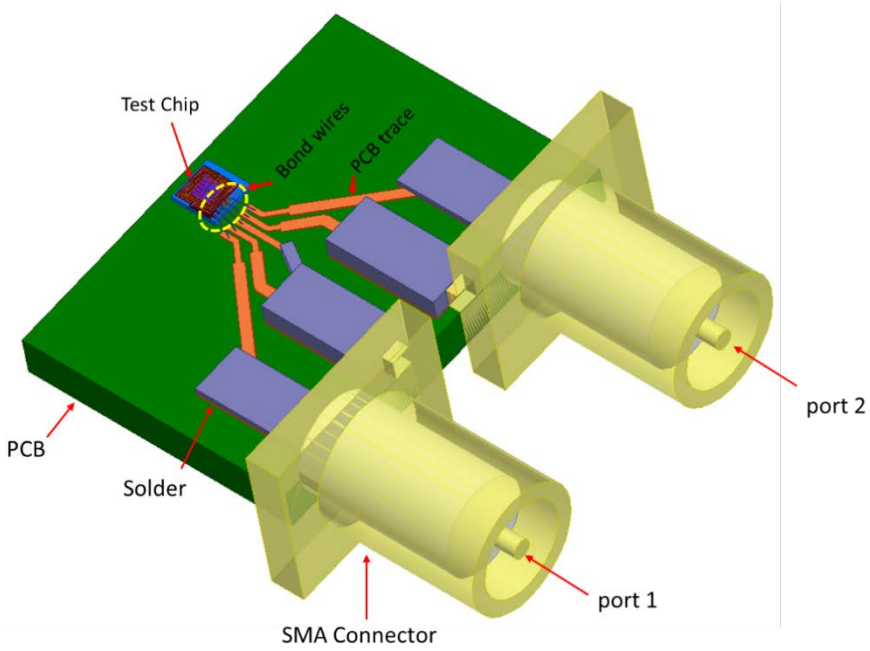


Figure 21: Transformer Model With Test Routing

To better correlate simulation and test results, more complex model is used for the simulation. It includes test chip, bond wires, PCB traces and SMA connectors. The SMA connectors' pins are coated with solder and the ground pin of the test chip is connected to the SMA ground pin using solder. This emulates the test board and gives more accurate results. The simulation sweeping frequency range is from 10MHz to 500MH.

The fabricated test board is shown in Fig. 22. These boards can be configured using zero-ohm resistors for different purposes of testing including comprehensive testing for the whole DC/DC converter, transformer testing and rectifier testing.

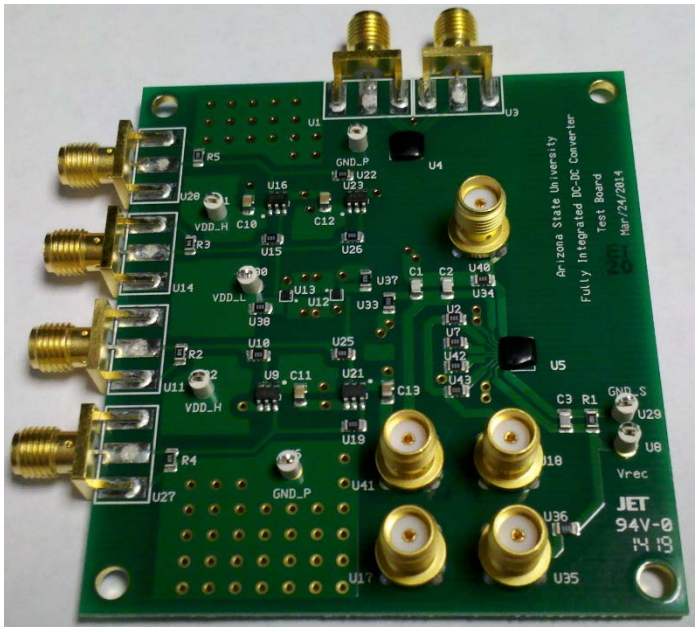
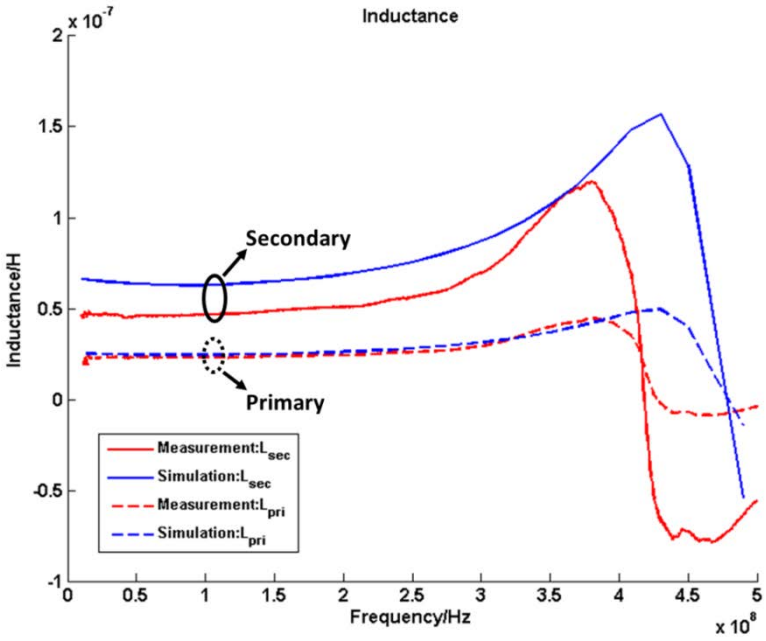


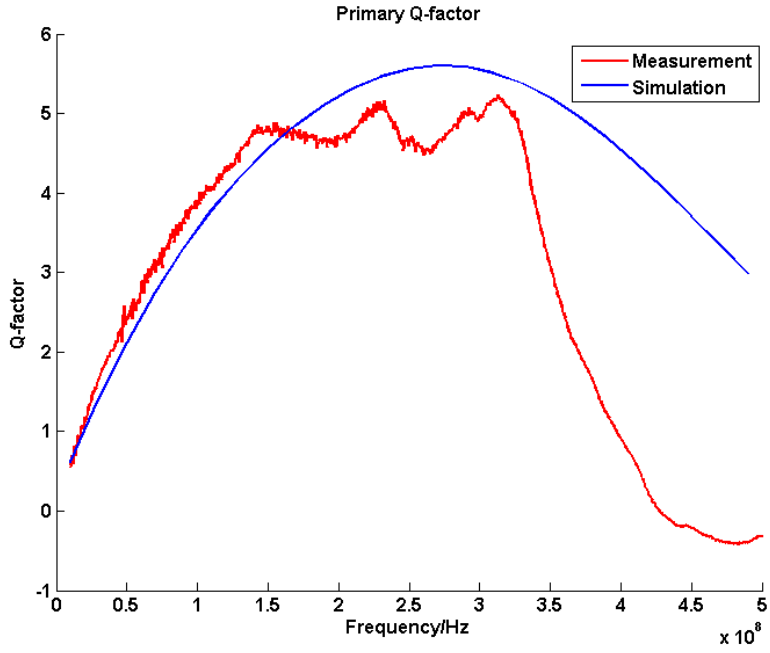
Figure 22: Transformer Test Board

The Network analyzer sweeps the frequency from 10MHz to 500MHz to measure the S-parameters. It generates a *.s2p file containing the s-parameter matrix which is exported to the Matlab script for calculations. The script converts the S-parameters to Z-parameters and calculates the k, Q and coil inductance.

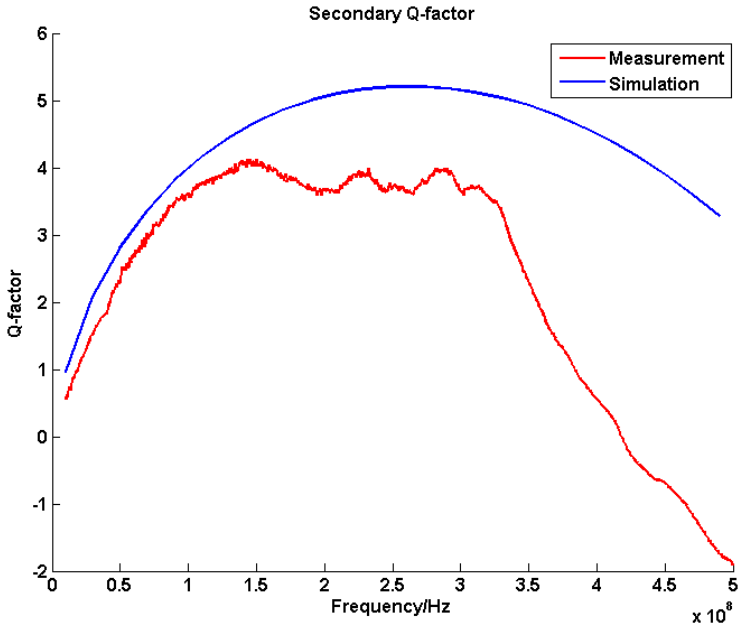
Five PCBs are manufactured, assembled and tested. The following measurement results show the typical data collected. The measurement results from Network analyzer is shown in Fig. 23. At 100MHz, k=0.46, LP=23.0nH, LS=46.7nH, QP=3.9 and QS=3.65.


Inductance
x 10^-7
Inductance/H
Frequency/Hz
x 10^8
Secondary
Primary
Measurement:L_sec
Simulation:L_sec
Measurement:L_pri
Simulation:L_pri

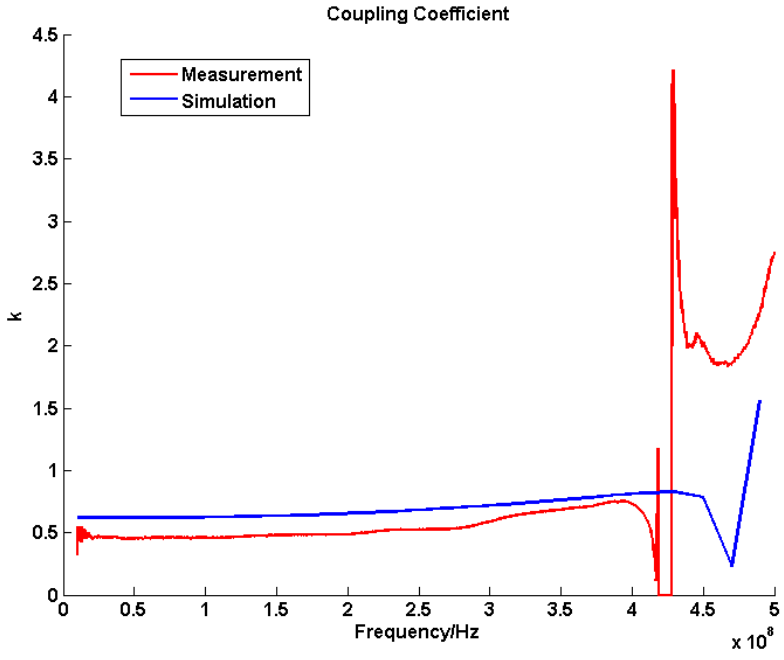
(a)


Primary Q-factor
Q-factor
Frequency/Hz
x 10^8
Measurement
Simulation

(b)


Secondary Q-factor
Measurement
Simulation
Q-factor
Frequency/Hz
x 10^8

(c)


Coupling Coefficient
Measurement
Simulation
k
Frequency/Hz
x 10^8

(d)

Figure 23: Measurement and Simulation Results Comparison: (a) Primary and Secondary Inductance, (b) Primary Q, (c) Secondary Q and (d) Coupling Coefficient [18]

It is shown that the coupling coefficient decreases to 0.46 at around 100MHz, which is much lower than the simulation results. The reason for this is the additional inductance contribution of the bond wires and the PCB routing traces. For example, the PCB traces contribute around 10nH for each side while having no mutual inductance between the two sides. Thus, according to equation (5), the k is decreased.

CHAPTER 4 CIRCUITS IMPLEMENTATION

System architecture is shown as fig. 24. Due to the process variation in the peak power transfer frequency in the isolation transformer, a peak power transfer frequency detection circuit at the primary side sweeps the switching frequency of the driver to detect the maximum power transfer, while the spread spectrum function is used to reduce output peak voltage ripple and on-chip EMI. The proposed on-chip ring oscillator based EMI sensor acts as a frequency modulator to the EMI noise and provides an accurate measurement of sensed EMI noise distribution.

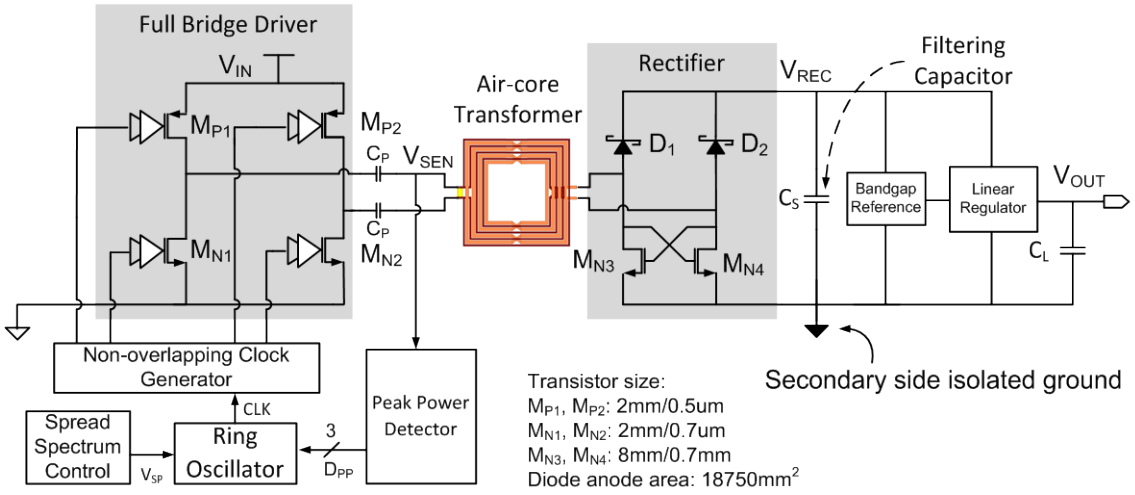


Figure 24: Block Diagram of Proposed 4-phase Hysteretic-controlled Quasi-current-mode Buck Converter

4.1 Mixed Signal Peak Power Search

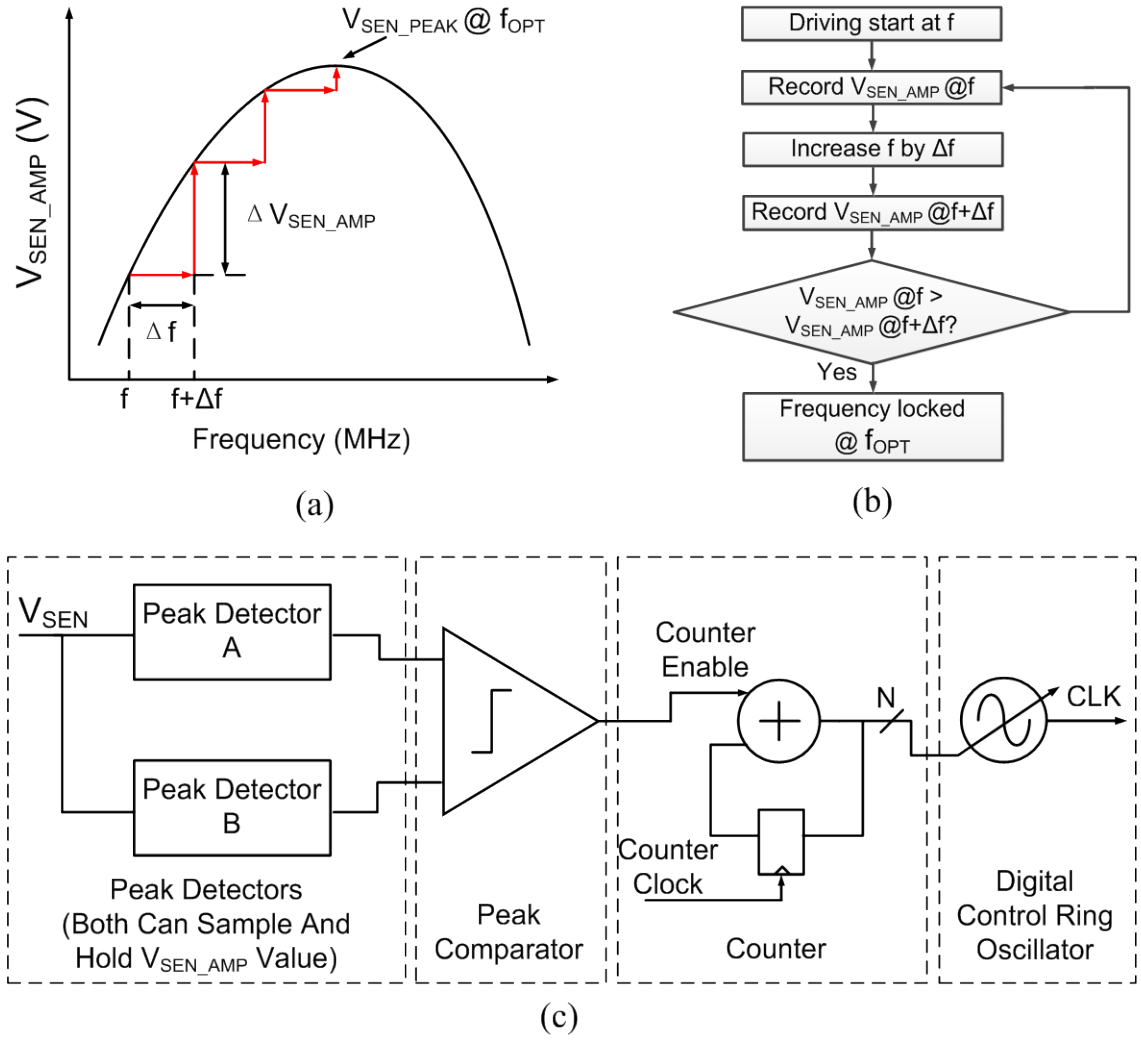


Figure 25: Analog Perturb-And-Observe Based Peak Power Frequency Detection Algorithm and Block Diagram

The operations of the analog perturb and observe based peak power frequency detector circuit is discussed in Fig. 25. The converter reaches its peak power transfer when the transformer coupled resonator is excited at its resonance frequency (f_{RES}) [21].

If the driver switching frequency is higher or lower than f_{RES}, the signal amplitude (V_{SEN_AMP}) at primary side of the transformer is lower than the peak V_{SEN_AMP} (V_{SEN_PEAK}) at f_{RES} as shown in Fig. 25(a). An analog perturb-and-observe search algorithm is used to detect the resonance frequency by sweeping the driver frequency and detecting the primary side voltage V_{SEN_AMP} for each frequency step. The algorithm flow chart along with system level implementation is shown in Fig. 25b and 25c. The peak power detector circuit detects and records the current sensed voltage V_{SEN_AMP} at driver switching frequency $f+\Delta f$. The recorded present V_{SEN_AMP} is compared with the recorded one step earlier V_{SEN_AMP} detected at f switching frequency. If the present amplitude is higher than the past value, switching frequency is increased by Δf and the process continues until the present amplitude becomes lower than the past recoded amplitude. When the V_{SEN_PEAK} is detected and the corresponding frequency is locked as driver optimum switching frequency (f_{OPT}). The start frequency is set at 100 MHz ensuring peak power frequency is within frequency searching range.

The detailed circuit implementation of the peak power detector and its control signals are shown in Fig. 26. Its input V_{SEN} is connected to one end of the transformer primary side and its output D_{PP} is used to change the ring oscillator frequency. It consists of two identical CMOS peak detectors, a comparator and a counter. Two non-overlapped clocked signals φ_1 and φ_2 select two detectors in peak amplitude sensing and hold modes alternately. Signals φ_4 and φ_5 are used to reset peak detector for next sensing cycle. In

order to reduce the power consumption, a clocked comparator followed by an SR-latch is utilized and its schematic is also shown in Fig. 26.

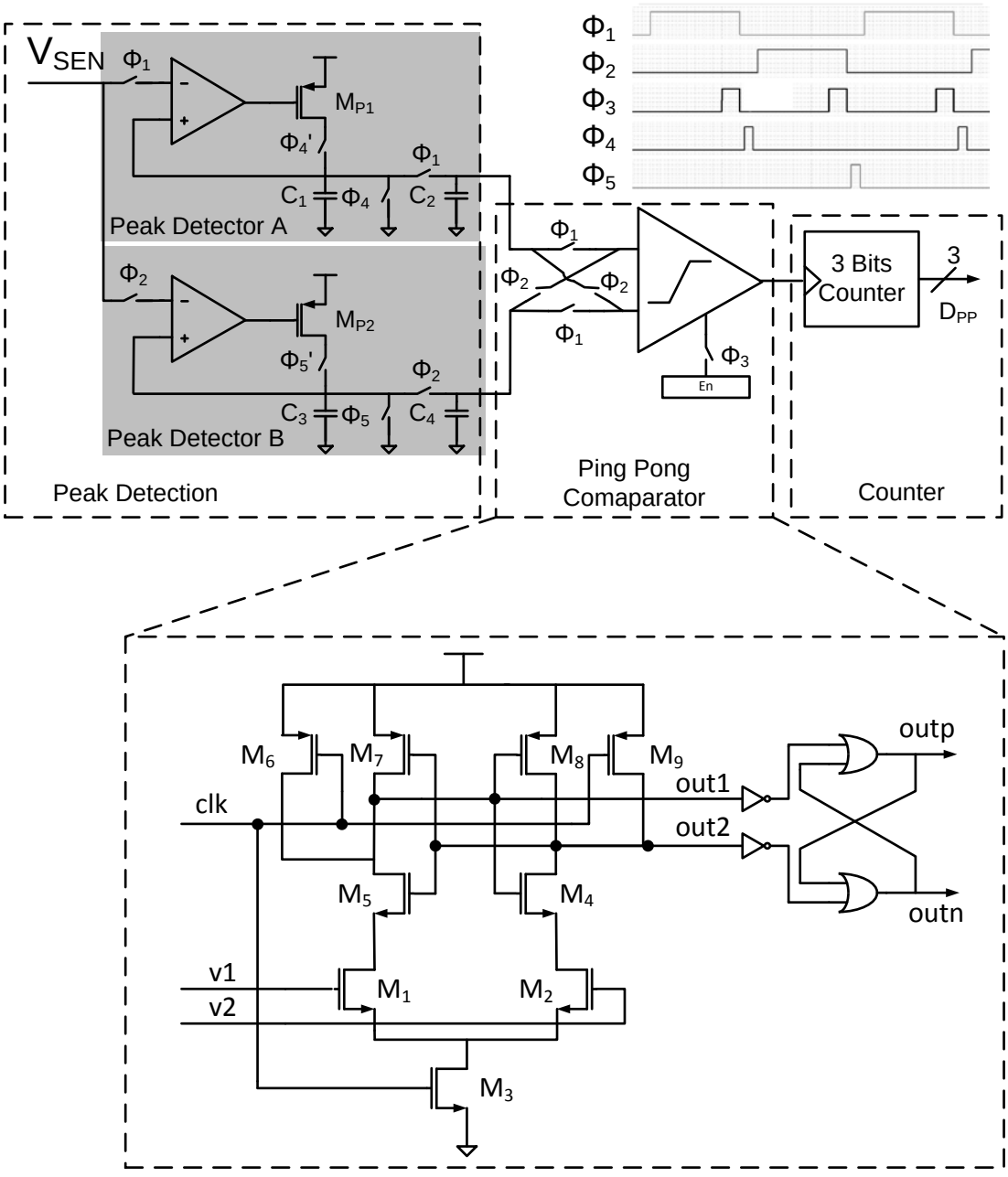


Figure 26: Peak Power Detector Circuit Implementation With Control Signal

When the clock signal φ_3 is low, transistor M_3 is off, and transistors M_6 and M_9 are on. Both outputs of the comparator are pulled up to supply, and the SR-latch outputs (outp, outn) hold the previous state. When the clock signal is high, the comparator detects voltage difference between its two inputs (*v1* and *v2*) and the latch sets logic low/high at outp and outn based on the input voltage difference.

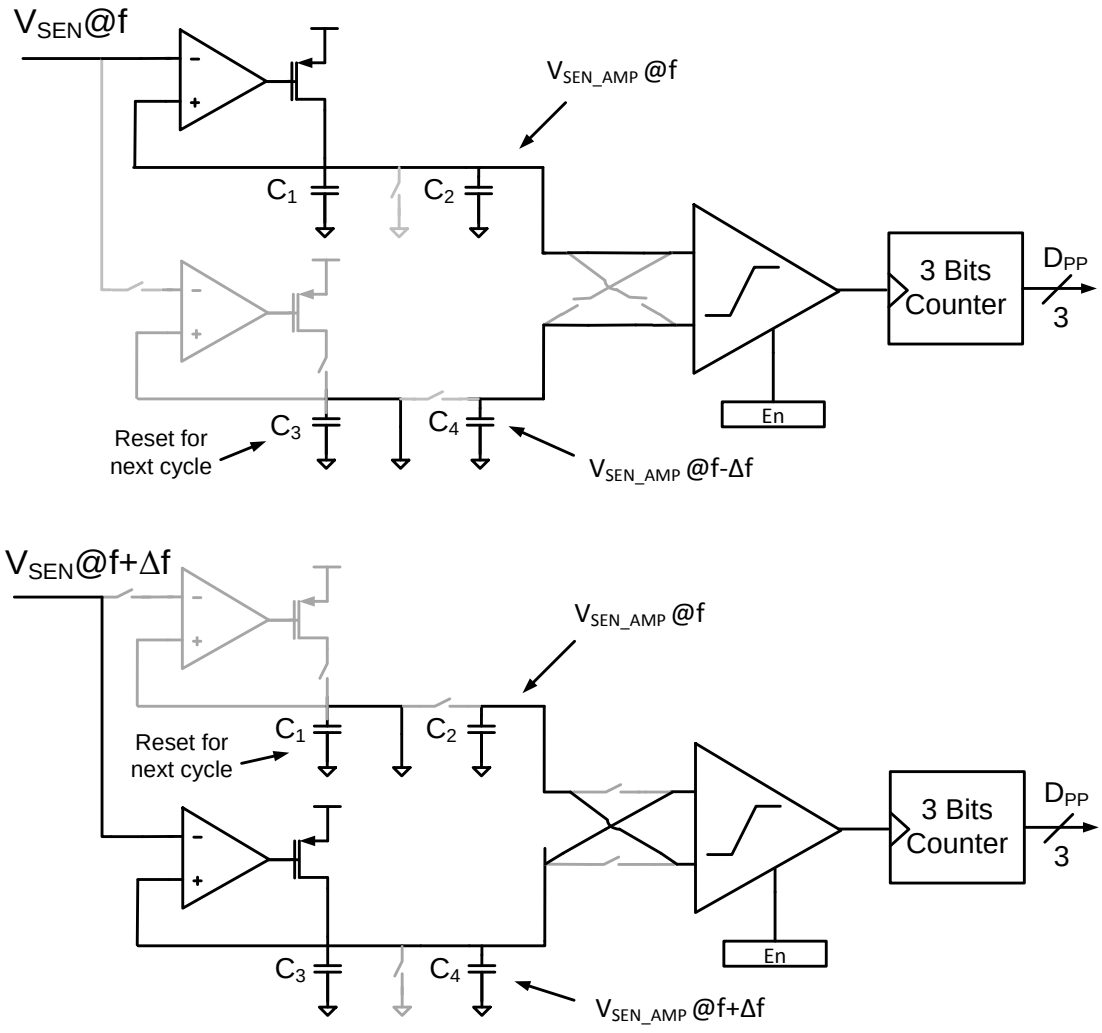


Figure 27: Peak Power Frequency Detector Working Flow

Two phases of operation for the peak power detector is shown in Fig. 27. When φ_1 is high the top detector in the figure detects V_{SEN_AMP} for switching frequency f and the bottom detector holds the past V_{SEN_AMP} for f-Δf switching frequency. For high φ_1, the top detector stores V_{SEN} signal amplitude on capacitors C_1 and C_2. When φ_1 becomes low, signal φ_4 discharges C_1, and the capacitor C_2 holds V_{SEN_AMP} which is compared with the past V_{SEN_AMP} on C_4 during φ_3 using a ping-pong clocked comparator. If the voltage on C_2 is higher than the voltage on C_4, the comparator enables the counter to increase its value by one, resulting in the increment of oscillator frequency by Δf. When φ_2 becomes high, the bottom peak detector, similar to the top detector in high φ_1, detects V_{SEN} signal amplitude for f+Δf switching frequency and the top detector holds V_{SEN_AMP} for f switching frequency. If the voltage on C_4 is higher than the voltage on C_2, the oscillator frequency is increased by Δf. Signals φ_4 and φ_5 are used to reset capacitors C_1 and C_3 to ensure proper detection of V_{SEN} amplitude when V_{SEN_AMP} starts falling. The analog perturb-and-observe search algorithm continues with increasing the frequency until the f_{RES} frequency is detected. At f_{RES} frequency the counter holds its value, and the oscillator frequency is locked.

4.2 DCO and Spread Spectrum Control

Previously reported resonant type power converters have suffered from higher noise interference. On a single chip solution, where the mixed signal die have to be powered at a much higher ground potential, EMI interference may affect surrounding signal chain

circuits' dynamic range. In order to solve this issue, we utilized spread spectrum technique to reduce EMI noise level.

Fig. 28 shows not only the power reduction of the main peak, but also the flatter aspect of the modulated signal. The minimum level of the second signal is higher than the minimum level of the first signal. This effect is normal and is due to the noise added for the modulation.

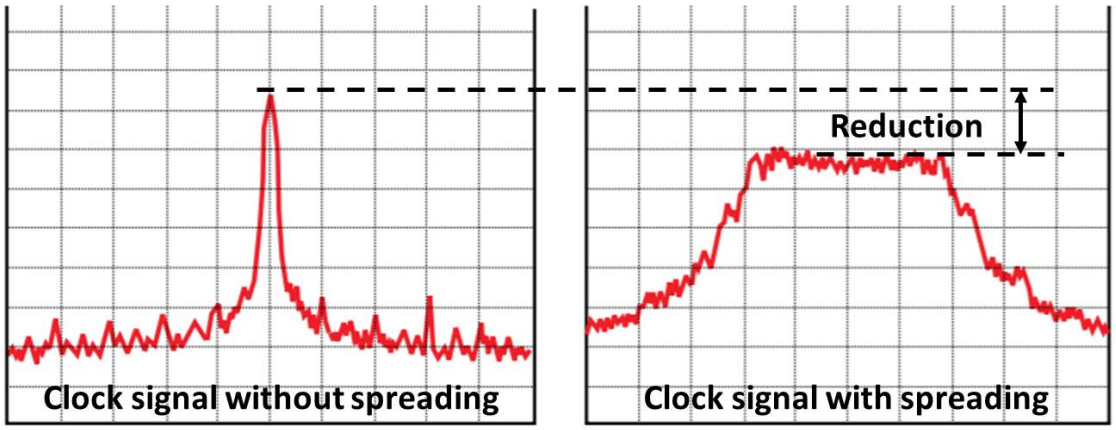


Figure 28: Effect of the SSC in Frequency [22]

The aim of spread spectrum is to add a variation in the frequency of an original clock, which spreads the generated interferences over a larger band of frequency. In theory, spread spectrum means that the clock signal is varied around the desired frequency. For example, for a 100MHz clock, the frequency might be 99.5 MHz at one moment and 100.5 MHz at another. Doing this constantly causes the power of the tone to be spread out more over a broader band of tight frequencies. To realize this constant variation on the original signal, a modulation with an additional signal is realized. Creating a spread

spectrum by spreading the initial clock frequency is done by defining the following parameters [22]: The spreading frequency, which is the ratio of the range of spreading frequency over the original clock frequency. The modulation rate (fm), which is used to determine the clock-frequency spreading-cycling rate and is the time during which the generated clock frequency varies through Δf and returns to the original frequency and the modulation waveform, which describes the variation curve in terms of time. [22]

The shape of the generated clock signal depends on the modulation waveform that is used during the frequency modulation. Several profiles can be used, according to the desired shaping for the energy spreading. Fig. 29 shows three examples of modulation waveforms and the spectrum of the corresponding modulated clock signal.

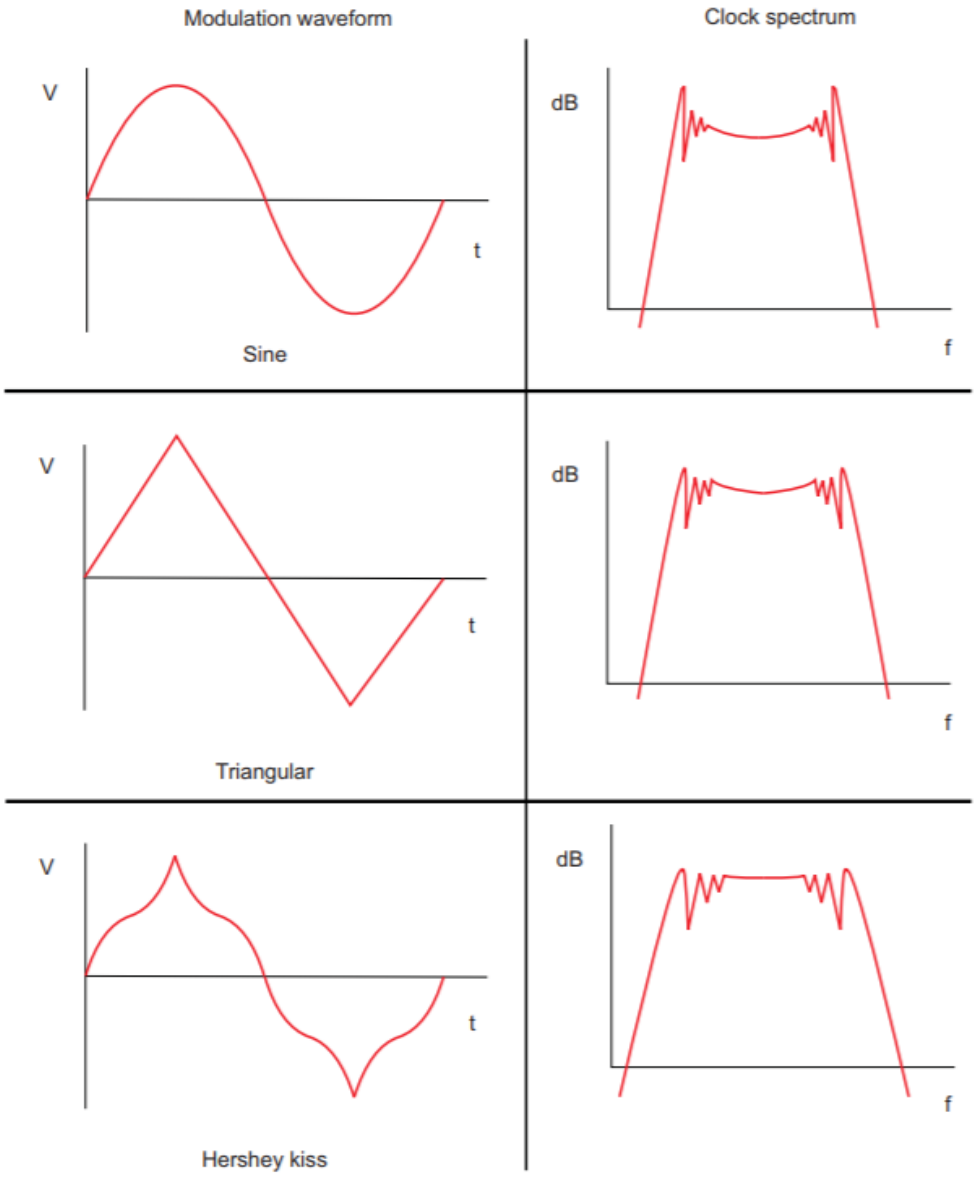


Figure 29: Modulation Profiles [22]

The electromagnetic interference reduction can be estimated with the following equation: [22]

$$\text{Peak power reduction} = 10 * \log\left(\frac{\text{Deviation} * \text{fc}}{\text{fm}}\right) \qquad (16)$$

where fc is Deviation in % of the initial clock frequecy, equals Δf / fc, fc is the original clock frequency and fm is the spreading frequency

For example: For fc=100 MHz, deviation =1% peak from fc (Δf = 1MHz) and fm=100kHz; the estimated peak power reduction is 10dB.

A current starved digitally controlled ring oscillator as shown in Fig. 30 is used to generate driver switching frequency. Its oscillation frequency is proportional to current I_D. A fixed bias current $I_{B\text{-}FIX}$, a variable analog bias current $I_{B\text{-}ANA}$, and a variable 3-bit binary weighted digital current source $I_{B\text{-}DIG}$ are used to set the total bias current I_D. The binary weighted current source determines the frequency tuning range for the peak power transfer frequency detection circuit. The $I_{B\text{-}ANA}$ bias current is realized using a resistive degenerated common source stage and is varied according to the injected spread-spectrum modulating input signal V_{SP} [23]. With the injection of V_{SP} the oscillator generates spread spectrum clock for the driver. Here, V_{SP} is generate by apply matched charge and discharge current pair I_{B_TRI} to a known capacitor C_{TRI}. The frequency and amplitude of V_{SP} are controlled by signal V_{SEL} and I_{B_TRI} to C_{TRI} ratio respectively.

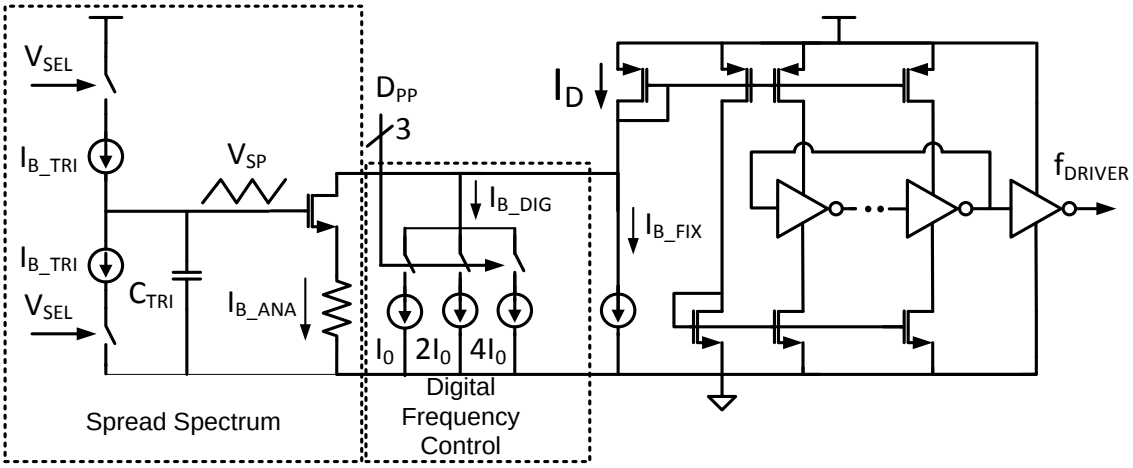


Figure 30: Current Starved Oscillator With Frequency Control

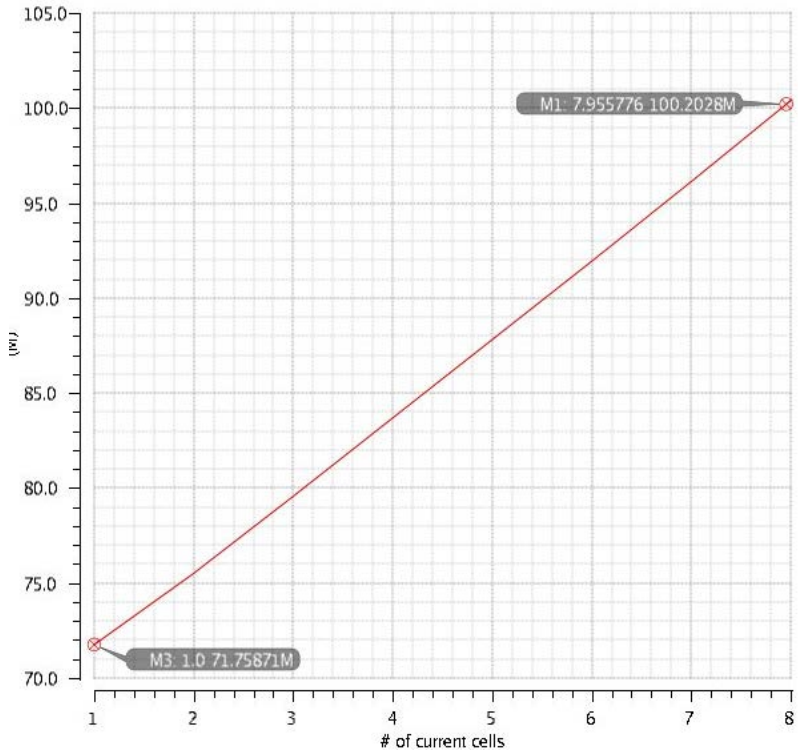


Figure 31: VCO Frequency Vs. Biasing Current

Primary side peak power point detect function is designed and simulated. Fig.32 shows the amplitude of transformer is increasing with operation frequency. The counter represents the frequency is increasing digitally. Frequency control unit compare the amplitude of present frequency with amplitude of previous frequency. For each comparison, if amplitude keeps increasing, we increase frequency by a step, until frequency control signal is changed. Converter reaches peak power transfer frequency at this point.

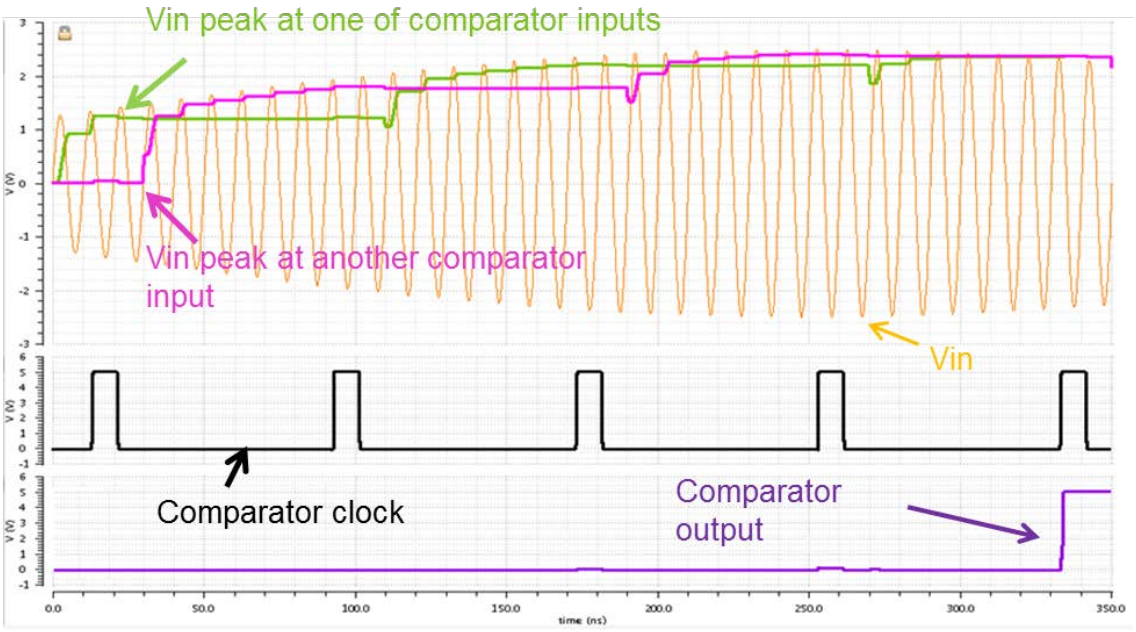


Figure 32: Frequency Control Simulation Results

4.3 LDO With Schottky Diode Based Band Gap Reference

To build an isolated bandgap reference, an isolated Schottky diode based bandgap reference is used. The voltage across a single Schottky diode is approximately 300mV, resulting in a 600mV V_{REF} voltage. In order to provide a higher reference voltage for the

LDO error amplifier, and achieve better power supply rejection ratio (PSR) for the reference voltage, another pair of diodes (D_3 and D_4) is added as shown in Fig. 33 to increase the V_{REF} to about 1.2V.

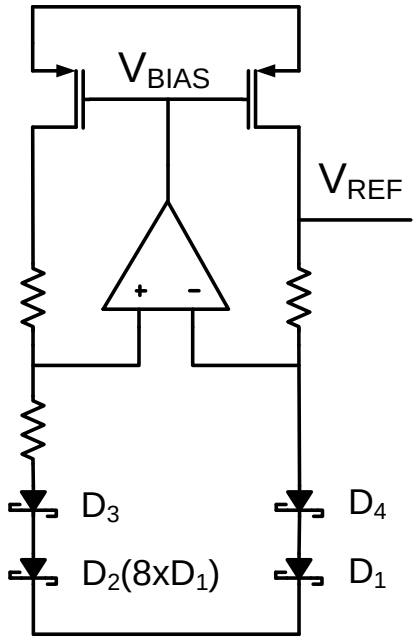


Figure 33: Schottky Diode Based Bandgap Structure

A low drop-out (LDO) regulator as shown in Fig. 34 is used at the rectifier output to provide regulated voltage at the load. A two stage error amplifier is used to provide high gain and good driving range for the pass device. The LDO output capacitor C_L is set to 10uF to meet for ADC power supply capacitor requirement. A dominant pole is created at LDO output node A. The large C_L and high impedance at node A make sure the dominant pole is always located at less than 200Hz. There are two non-dominant poles B and C. B is the first non-dominant pole and located at the gate of pass device and C is the second non-dominant pole and located between two amplifier stages. The stability of the LDO is

achieved by firstly pushing the second non-dominant pole C to greater than 7Mhz while the system unity gain frequency which is less than 1Mhz. By doing this, the stability effect by the second non-dominant pole is minimized. Secondly, a zero is introduced at V_{OUT} using a 0.3Ω ESR resistance R_{ESR} in series with the load capacitor C_L. The zero frequency is around 53 kHz and close to the first non-dominant pole which is around 40 kHz to boost phase margin. The isolated DC/DC converter provide just 10mA current, the added 0.3Ω resistor at LDO output contribute very small ripple to the output. The Reference voltage (V_{REF}) for LDO is generated by an isolated bandgap reference circuit. Although substrate based diode device is commonly utilized in bandgap references, substrate based devices can't be isolated from primary side ground.

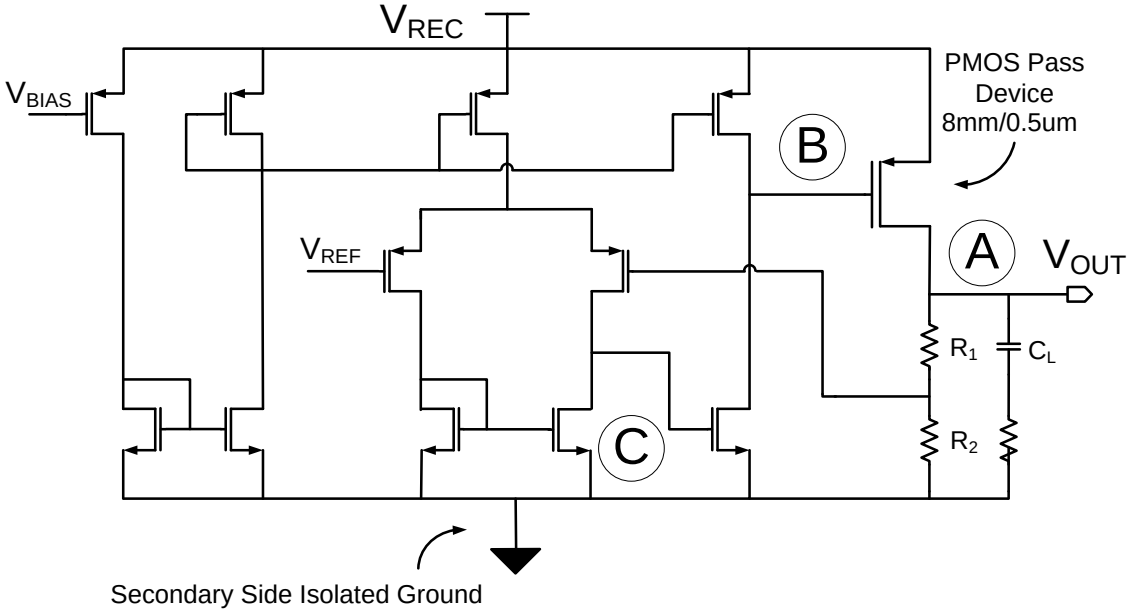


Figure 34: LDO With PMOS Pass Transistor

4.4 Conducted and Radiated EMI Sensor Design

Radiation from on-chip transformer is a major concern for both on-chip and off-chip components. Considering the air-core transformer as a loop antenna, the radiation is primarily perpendicular to top metal plane. The wavelength λ_{RES} of the radiated signal for operating frequency f_{RES}=100MHz is

$$\lambda_{RES} = \frac{c}{\mathrm{f}_{RES}} = \frac{3 * 10^8}{1 * 10^8} = 3m \tag{17}$$

where c is velocity of light. The size (radius) of an effective loop antenna should be in the order of signal wavelength [24]. The radius of the outmost loop of the implemented transformer is 0.85mm which is about $5.6\text{x}10^{-5}$ times of λ_{RES} (3m). Therefore, the EMI noise induced by radiated power is too small to be a concern for off-chip components. The 3-D electro-magnetic field plot of transformer excited at 100MHz is shown in Fig. 35. As shown in the figure, the magnetic flux essentially concentrates within the center of the transformer. To measure the on-chip distribution of EMI induced noise, distributed on-chip EMI sensors are designed.

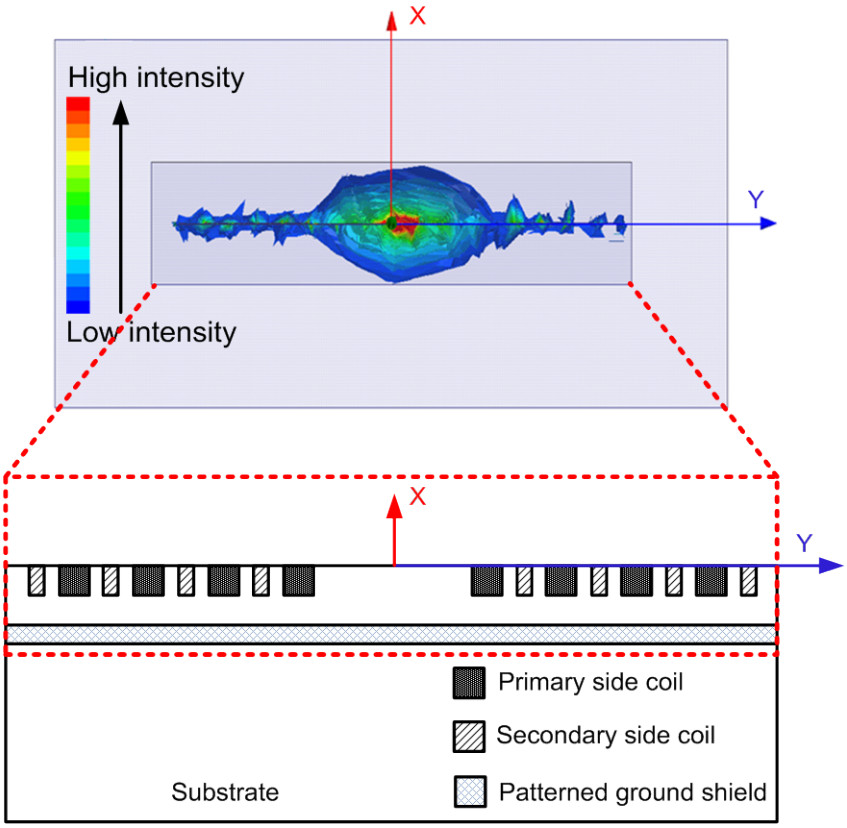


Figure 35: Transformer Cross-Section View and Simulated Electro-Magnetic Field Distribution

An array of EMI sensors are placed at the secondary side as shown in Fig. 36(a). The proposed EMI sensor acts as a frequency modulator and its output signal $v_{OUT}(t)$ can be expressed as [25]

$$v_{OUT}(t) = A_{OSC}\, cos\left\{2\pi f_{OSC}\mathrm{t} + \mathrm{K}\int v_{EMI}(t)\, dt\right\} \qquad (18)$$

where f_{OSC} and A_{OSC} are ring oscillator based sensor free running frequency and output signal amplitude respectively, $v_{EMI}(t)$ is sensed EMI, and K is the modulation index. The EMI can be simplified by its fundamental component as

$$v_{EMI}(t) = A_{EMI} cos(2\pi f_{EMI} t) \tag{19}$$

where f_{EMI} and A_{EMI} are EMI fundamental frequency and amplitude respectively. The sensor output signal $v_{EMI}(t)$ is rewritten as

$$v_{OUT}(t) = A_{OSC}\, cos\left\{2\pi f_{OSC} \mathrm{t} + \frac{\mathrm{K}A_{EMI}}{2\pi f_{EMI}} sin(2\pi f_{EMI} t)\right\} \tag{20}$$

Since noise modulation frequency is much smaller than the carrier frequency,$KA_{EMI}/2\pi f_{EMI} \ll 2\pi f_{OSC} t$, using narrowband FM approximation, $v_{OUT}(t)$ is represented by

$$v_{OUT}(t) = A_{OSC}\left[cos(2\pi f_{OSC} t) - \frac{\mathrm{K}A_{EMI}}{2\pi f_{EMI}} sin(2\pi f_{OSC} t)\, sin(2\pi f_{EMI} t)\right]$$

$$= A_{OSC}\, cos(2\pi f_{OSC} t)$$

$$+ \frac{\mathrm{K}A_{OSC}A_{EMI}}{4\pi f_{EMI}} [cos(2\pi(f_{OSC}+f_{EMI})t)$$

$$- cos(2\pi(f_{OSC}-f_{EMI})t)] \tag{21}$$

From (21), we can observe that the sensed EMI noise is up-converted to the oscillator carrier frequency as noise sidebands $f_{OSC} \pm f_{EMI}$ as shown in Fig. 36(b). The amplitude of the sensed EMI at $f_{OSC} \pm f_{EMI}$ frequency is proportional to A_{EMI}. Due to FM nature of the EMI sensor output, the measurement is not affected by the undesired EMI pick-up at f_{EMI} frequency, resulting in an accurate measurement of EMI distribution across the die.

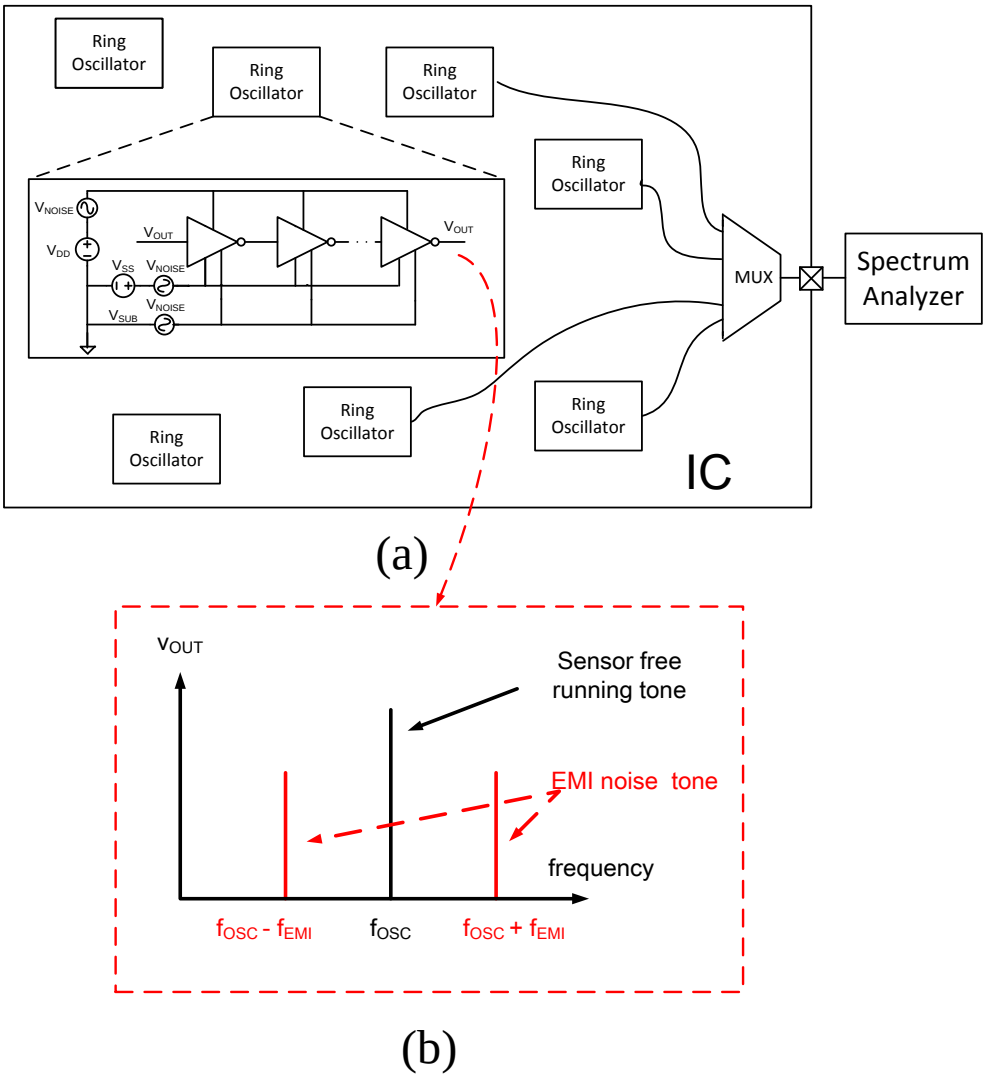


Figure 36: EMI Noise Sensors and Its Output Spectrum With EMI Noise

CHAPTER 5 TEST SETUP AND TEST RESULTS

The proposed fully integrated isolated DC-DC converter is designed and fabricated in an 180nm CMOS technology with 5V compliant transistor option and its die micrograph is shown in Fig. 37. The converter core occupies 5.2mm^2. The isolation between primary and secondary side is realized by designing all necessary circuits on secondary side, inside a deep nwell. The reverse breakdown voltage of the junction diode between the deep nwell and the bulk limits the maximum isolation voltage level between primary and secondary voltage domains, which is 50V in this technology. The converter supplies 0 to 25mA output current at 2V regulated output V_{OUT} with input voltage V_{IN} ranging from 3V to 5V.

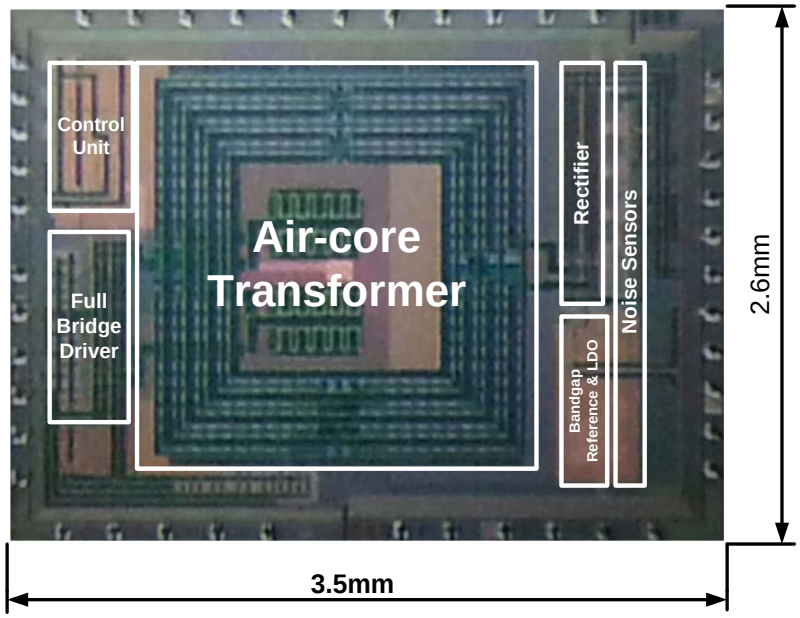


Figure 37: Die Micrograph

5.1 Test Board Design

Test board has two voltage domain, one for primary side and another one for secondary side. H-bridge consume most of the power at primary side, it makes ground noisy. One the other hand, primary side control circuits are very sensitive to ground noise. In order to minimize the noisy ground noise goes to sensitive circuits like, peak detector and comparator, another analog ground pin is added at primary side. Power supply for H-bridge and analog control circuits has the similar issue, so two power supply pins are used at primary side as shown in Fig. 38.

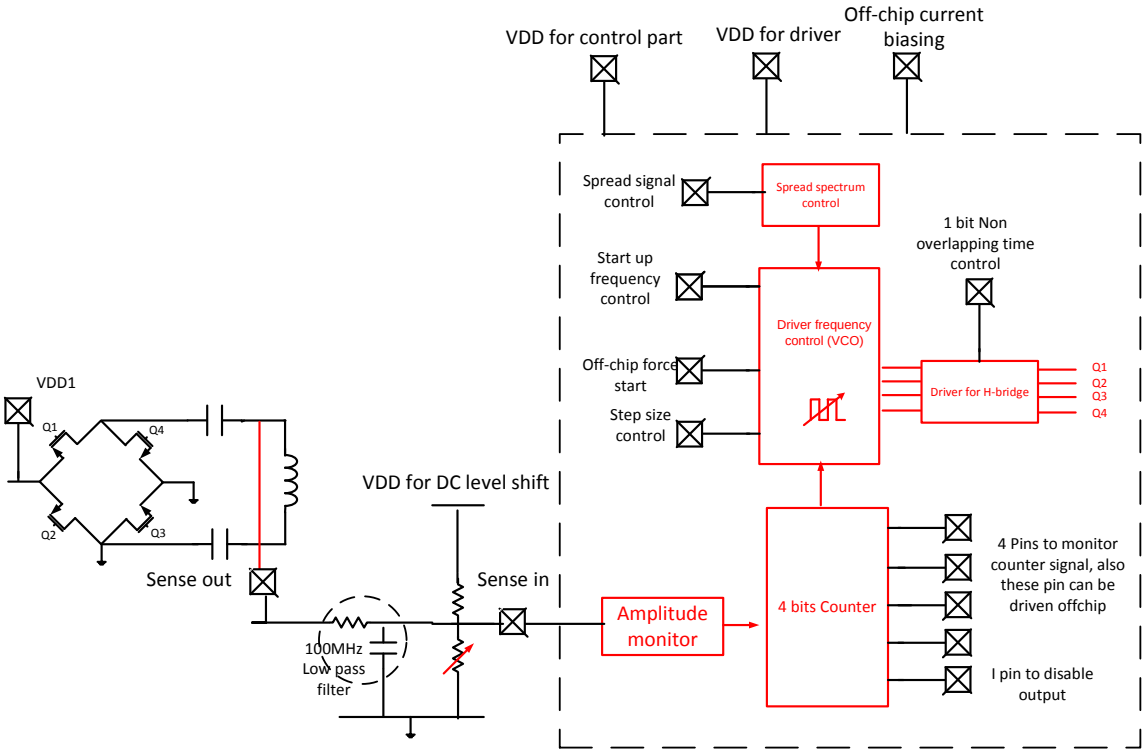


Figure 38: Primary Side Pin Out

There's concern about high frequency noise at resonant tank. Optional off-chip filter is added to the test board for better signal sensing for the comparator input signals. To monitor frequency control bits, 4 pins are also added.

At secondary side, a on board filter is needed at rectifier output, it's output is the power supply for flowing circuits like bandgap and LDO as shown in Fig. 39. A separate power supply is added for EMI noise sensor. This clean supply is critical for sensor to pick up only EMI noise and no power supply noisy.

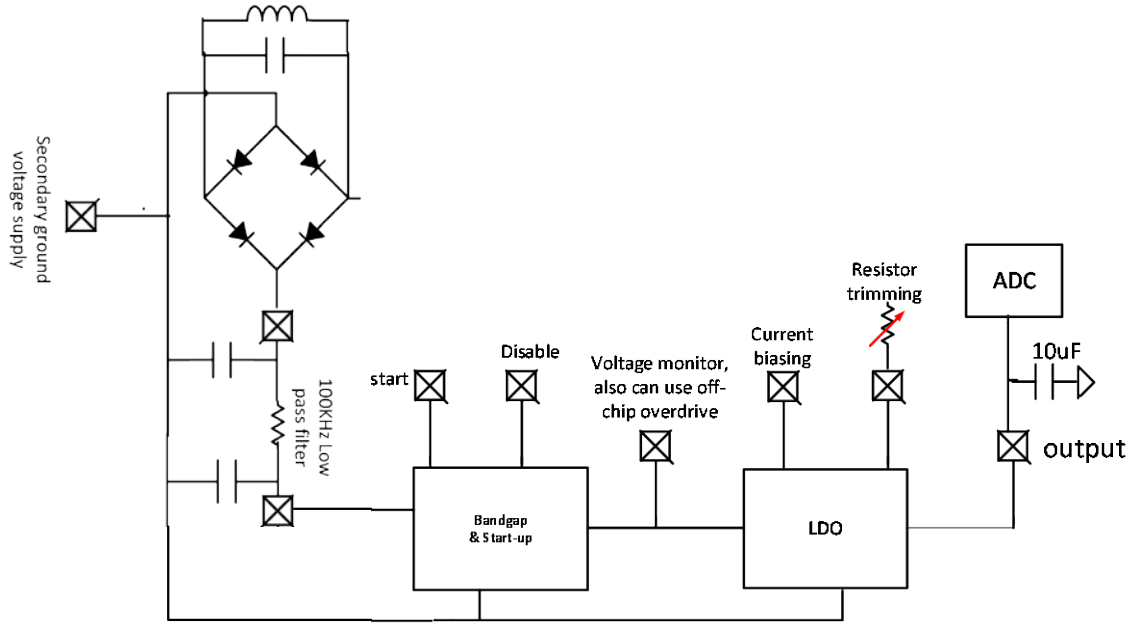


Figure 39: Secondary Side Pin Out

There are three pins added for the input of EMI noise sensor selection MUX. Only one of the sensor output is selected each time. Sensor output is buffered by strong

inverter to achieve adequate off chip driving ability. Off-chip supply is used for the buffer inverters as shown in Fig. 40.

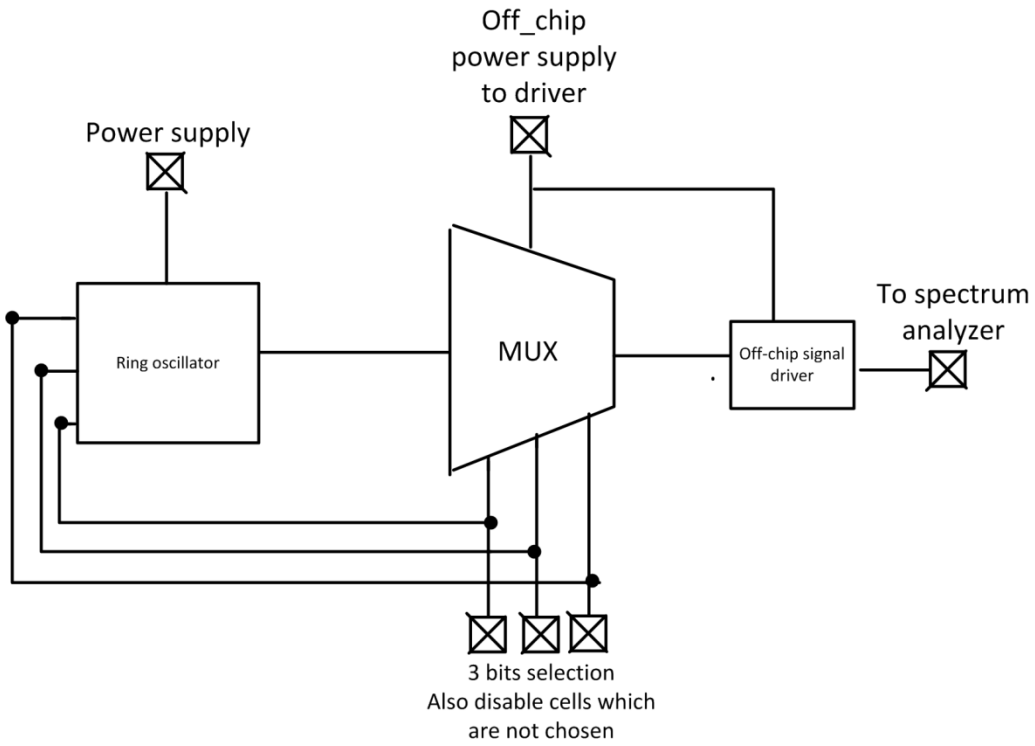


Figure 40: EMI Noise Sensor Pin Out

Detail ground arrangement is shown in fig. 41. To avoid noise interference at primary side, only small connection is added for noisy and quite ground. Also two capacitors are added between primary and secondary ground, that's because input-to-output dipole radiation is generated by driving a current source across a gap between ground planes. This is the predominant mechanism for radiation for isolated DC-DC converter. Isolated power supplies, by their very nature, drive energy across gaps in ground planes. The inability of high frequency image charges associated with the power

signal to cross the boundary causes differential signals across the gap driving the dipole. This type of radiation is predominantly perpendicular to the gap in the ground planes. When current flows along PCB traces, an image charge follows along the ground plane beneath the trace. If the trace crosses a gap in the ground plane, the image charge cannot follow along. This creates differential currents and voltages in the PCB leading to radiated and conducted emissions. The solution is to provide a path for the image charge to follow along with the signal. Standard practice is to place a stitching capacitor in proximity to the signal across the split in the ground plane. A stitching capacitance can be implemented with a simple ceramic capacitor across the barrier. Capacitors with guaranteed creep-age, clearance, and withstand voltage can be obtained from many major capacitor manufacturers such as Murata and Vishay. Safety rated capacitors are available in several grades depending on their intended use. [26]

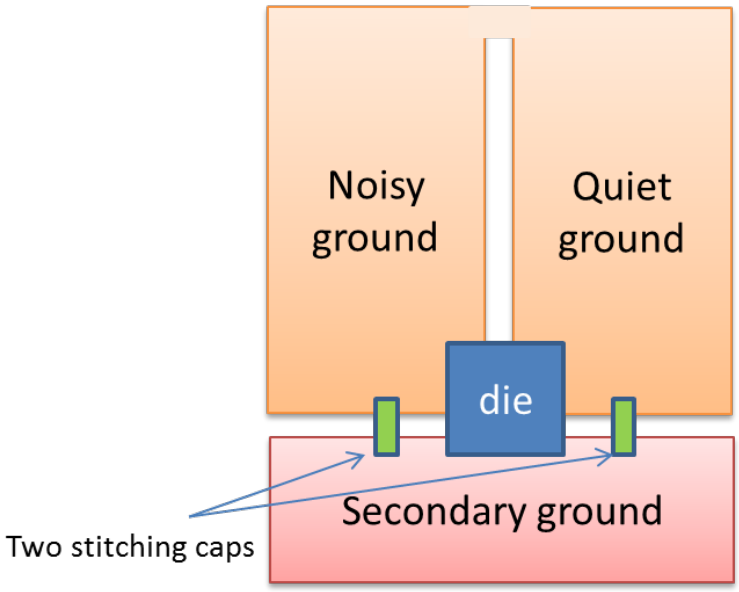


Figure 41: Ground Plan Arrangement

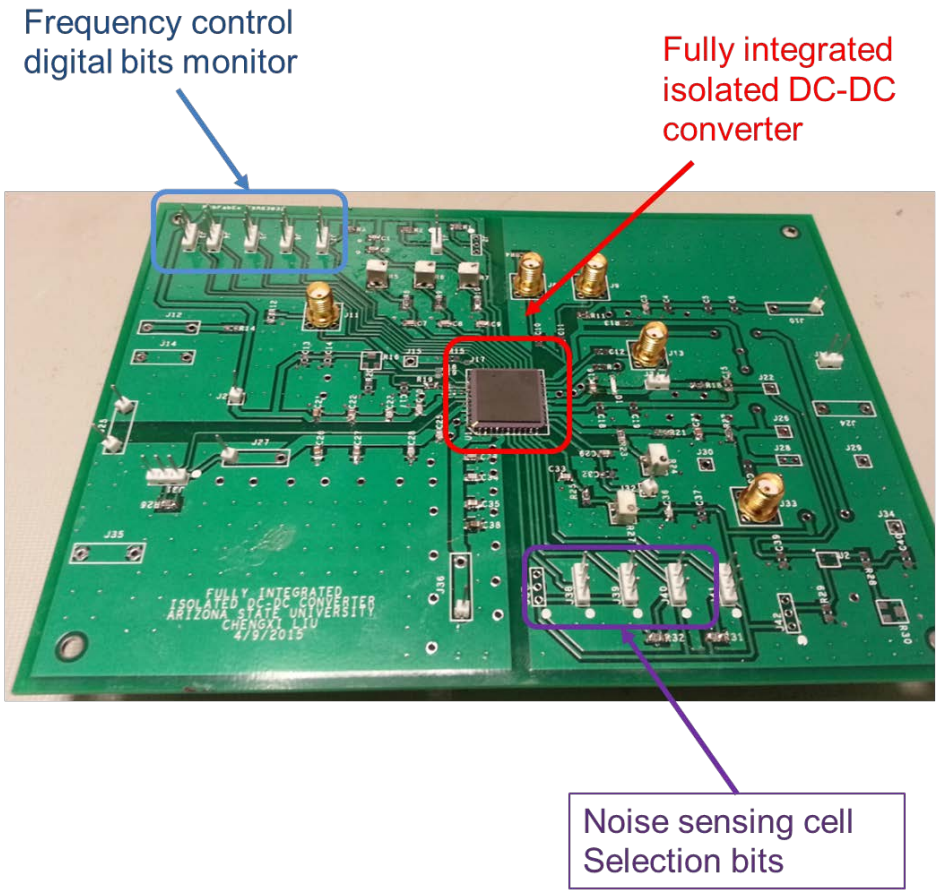


Figure 42: PCB Board for Testing

5.2 Test Setup and Measurement Results

Test setup is shown in Fig. 43. Oscilloscope is used to monitor converter output waveform. Spectrum analyzer is used to analyze EMI noise distribution and spread spectrum results. Signal generator is used to control generate spread spectrum control signal.

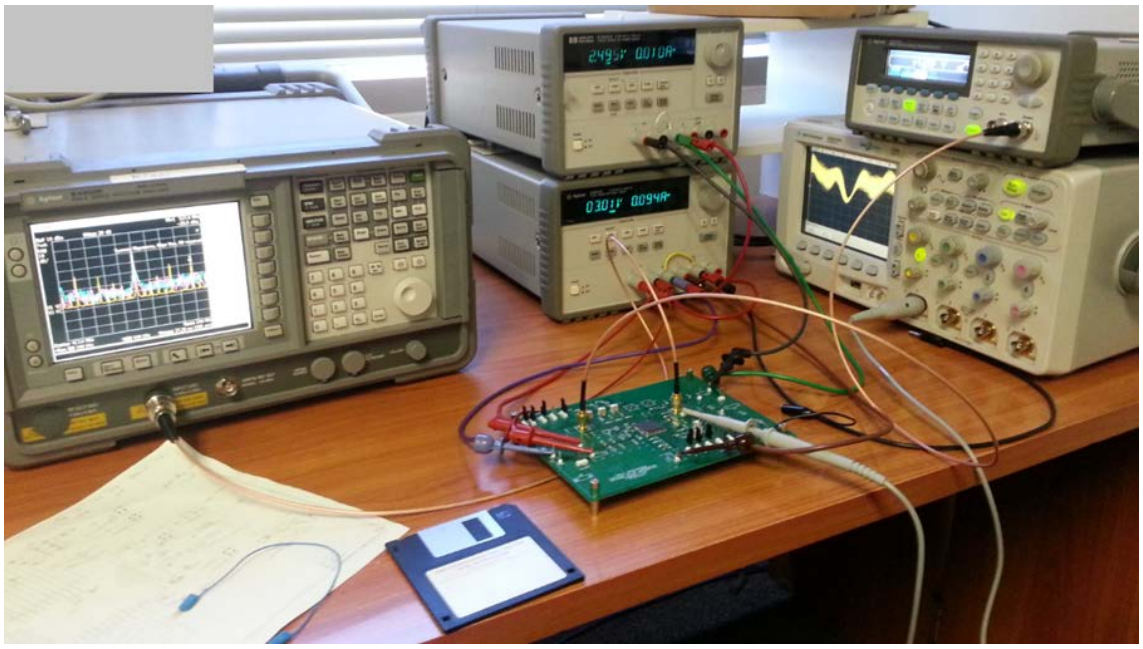


Figure 43: Test Equipment Setup

5.2 Converter Performance Measurement Results

The measured received power of the converter for different driving frequencies is shown in Fig. 44. In the average, the peak power transfer occurs at 111MHz which is the resonant frequency of the primary side, f_{RES}. The transferred power at 100MHz is 60% lower than the peak value, making the peak power search an effective approach to increase overall converter efficiency. With 4.5V input voltage, 2V output voltage and 25mA loading current, the converter achieves 7% efficiency.

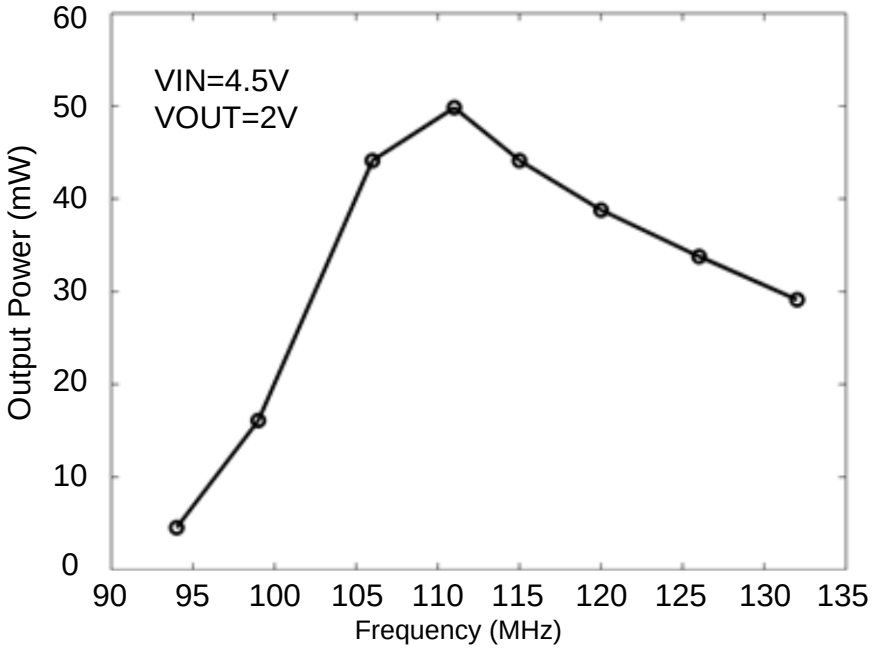


Figure 44: Measured Output Power at Different Switching Frequencies

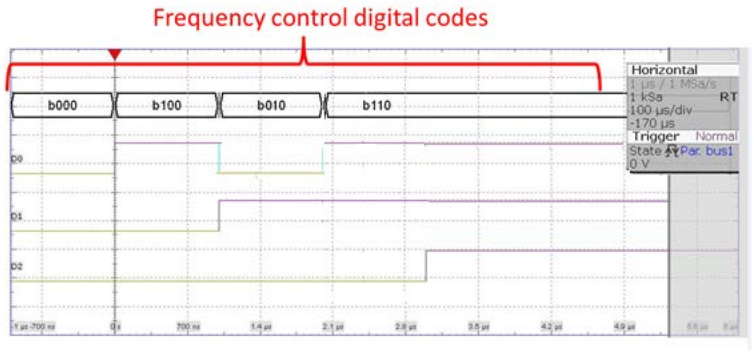


Figure 45: Real Time Frequency Control Bits Changing

Fig. 45 shows after reset, peak detection unit starts digitally increase driving frequency until reach primary side peak frequency @ 111Mhz and corresponding code is

B001. Due to loading sensitivity, primary side resonant amplitude cannot be directly tested.

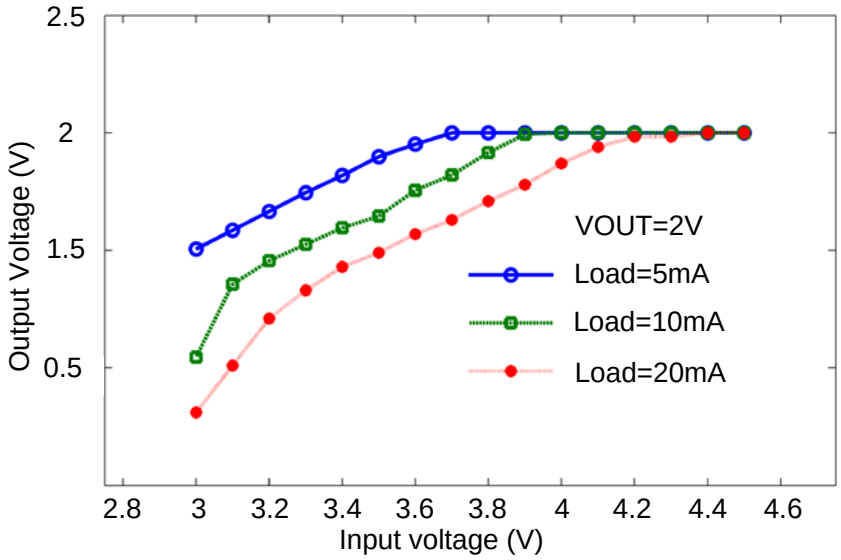


Figure 46: Measured Output Power With Different Input Voltages and Different Loads

Secondary side current goes through one Schottky diode and one MOSFET before driving the load, both these two elements has voltage drop. Higher current causes higher voltage drop across the rectifier. As shown in Fig. 46, compared to 5mA and 10mA load conditions, to reach the same output voltage level, input voltage is 0.2V higher for 10mA load condition. In comparison to the Schottky diode, MOSFET has a higher voltage drop contribution at higher load conditions. This is due to MOSFET channel resistance at different loading conditions. The voltage drop across this MOSFET increases linearly with the loading current.

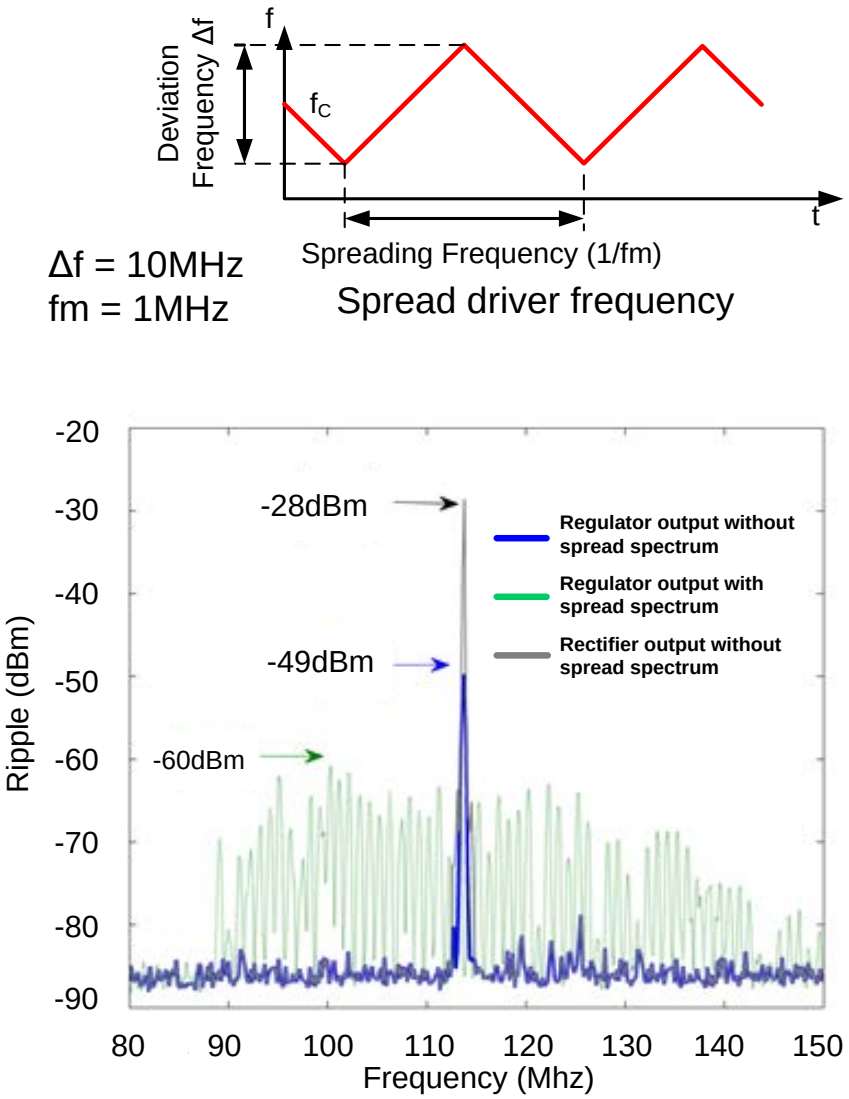


Figure 47: Measured Output Ripple Spectrum With and Without LDO And Spread Spectrum

Fig. 47 shows the measured spectrum of rectifier and regulator output signals, which indicates 21dB peak ripple amplitude reduction at 111MHz switching frequency (f_{RES}) by using a LDO. A 1MHz triangular signal is used as spread spectrum signal which gives

10MHz maximum frequency deviation (Δf) in driver oscillator frequency. After using spread-spectrum technique, the output ripple power is spread to wider frequency range and the peak ripple power is reduced by additional 11dB. Both high power level and low ripple level are achievable by choosing right frequency deviation range.

5.3 EMI Noise Sensor Measurement Results

The ring oscillator based on-chip EMI sensor is used to sense the on-chip EMI induced noise, and the noise power is measured using a spectrum analyzer from the sensor output spectrum. The measured sensor output spectrum is shown in Fig. 48.

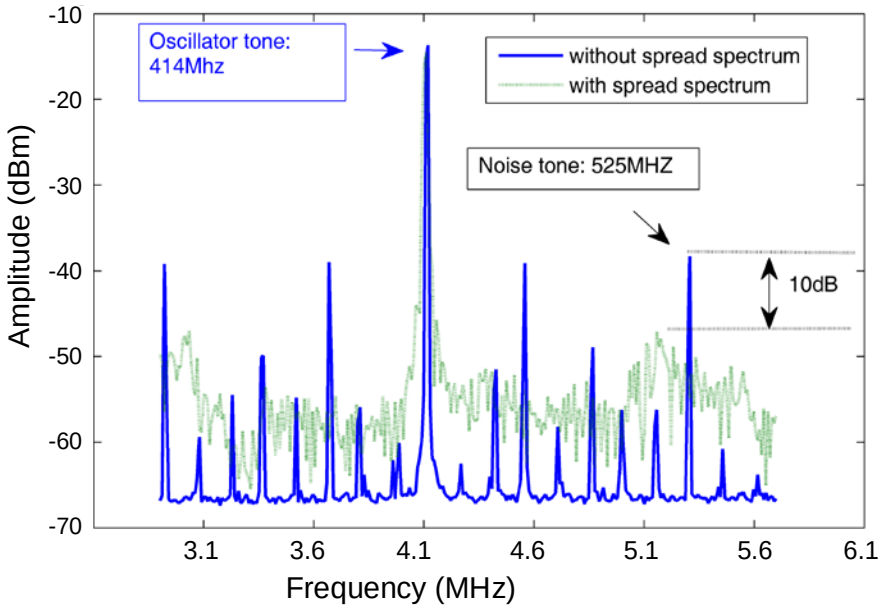


Figure 48: Measured EMI Noise Without and With Spread Spectrum

The figure shows that the free-running frequency of the oscillator based sensor (f_{OSC}) is located at 414MHz. The EMI noise signal is located at 525MHz and 303MHz as the

driver switching frequency (f_{RES}) is 111MHz, which is discussed in section III.D. The spread spectrum technique reduces the peak ripple at output V_{OUT} as well as it reduces the on-chip EMI noise power. The same spread spectrum signal V_{SP} applied for the ripple reduction at V_{OUT} node is used for this measurement. Fig. 48 shows 10dB reduction in EMI noise power at 525MHz frequency after enabling the spread spectrum. The proposed sensor shows 68dBm sensitivity.

The on-chip EMI noise distribution is obtained by measuring EMI noise power at the output of EMI sensors located at transformer secondary side. The on-chip sensor locations are shown in Fig. 49. The EMI noise power at the output spectrum of the proposed sensor is proportional to the EMI noise intensity at the sensor location. Therefore, the comparison of EMI noise power at different sensor outputs provides the relative EMI noise distribution information as shown in the Fig. 49. Measurements show that three locations close to the rectifier region has 2-3dB noise increase compared to other locations. Performance of the implemented isolated DC-DC converter is summarized in the Table 2.

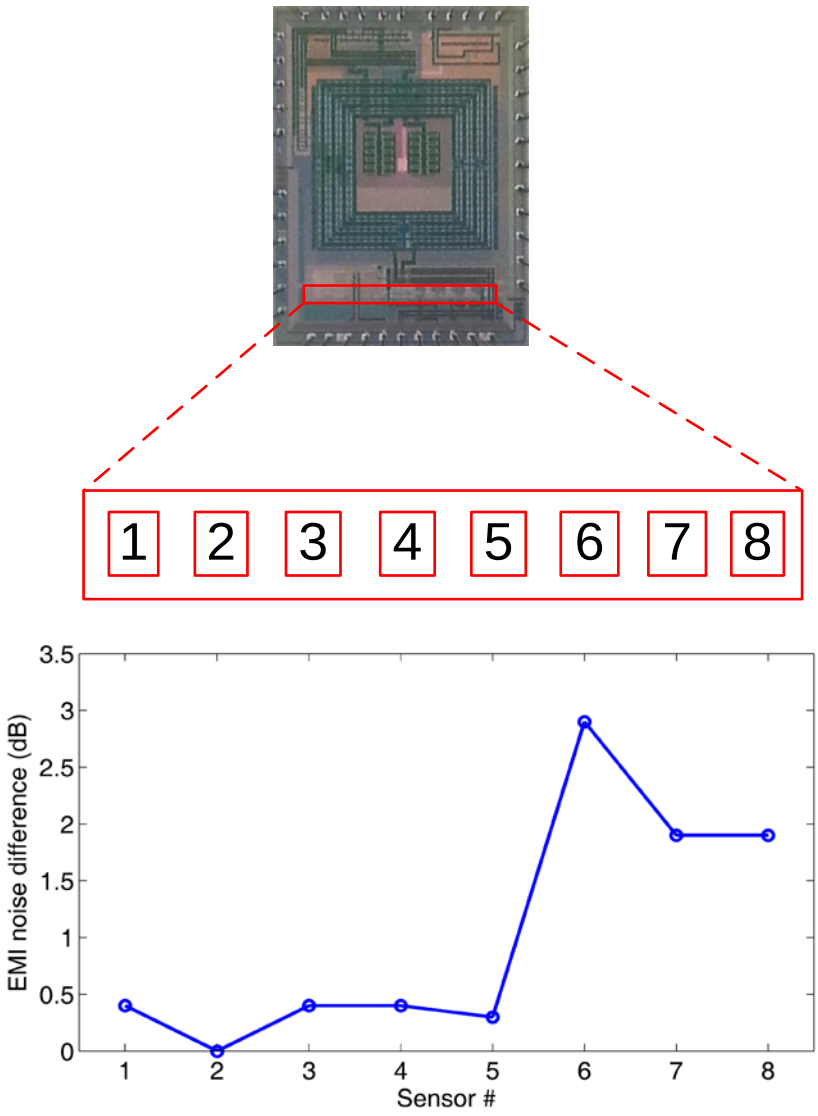


Figure 49: Measured On-Chip EMI Noise Distribution

Table 4： Performance Summary

DC-DC Converter Parameters	
Technology	AMS H18 180nm CMOS
V_{IN}	3V-5V
V_{OUT}	2V-3V
Max output power	50mW
Output voltage ripple	≤60mV
Switching frequency	~110MHz
Peak efficiency	~7%
Isolation	50V
Peak ripple reduction performance	
Peak ripple at output	-32dB,
On-chip EMI noise reduction performance	
On-chip EMI noise	-11dB

Power transfer efficiency of different blocks of the implemented converter is shown in Fig. 50. To measure the transformer and rectifier performance, a separate test chip is fabricated and these two components are measured separately and independently. To measure driver and control circuit power performance, no load is added to transformer output and power consumption is recorded. The LDO power performance is obtain by record voltages at its input and output node. The main contributors of power loss are H-

bridge loss (30%), transformer loss (56%) and rectifier loss (6%). The main reason for large transformer loss is low coupling factor k, low coil quality factor and low coil inductance value. The loss in H-bridge driver is limited by conduction loss and switching loss. Larger switch dimension reduces conduction loss; however it increases switching loss in high frequency (100MHz). The rectifier power loss is mainly due to diode forward voltage drop and reverse leakage current.

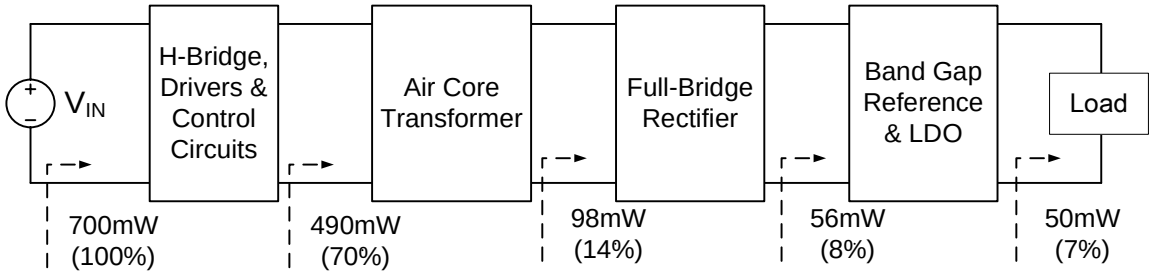


Figure 50: Transferred Power Efficiency Across Different Blocks

A performance comparison of the proposed regulator is presented in Table 3. The proposed converter's main application area is providing low noise, low EMI supply for mixed signal sensor signal chains on the same piece of silicon. It can provide isolated power for mixed-signal sensor signal chains that require isolation and level shifted regulators with total load range of 20mA-40mA. It has advantage of PCB die area, silicon area, noise, EMI performance over other designs.

Table 5： Performance Comparison

Reference	[1]	[3]	[4]	This Work
Technology	NA	NA	0.35 um BCD	0.18um CMOS
Non-Standard Process	No	Yes	No	No
Isolation Type	External magnetic	Integrated magnetic	Integrated magnetic	Integrated magnetic and junction isolation
Driving Method	Fixed f_{SW}=100Khz-2Mhz	Self-resonant f_{SW}=180Mhz	Fixed f_{SW}=300Mhz	Automatic frequency search $f_{SW}\approx$ 100Mhz
Output Power	2W	150mW	30mW	50mW
Efficiency (P_{OUT}<50mW)	< 25%	<25%	10.8%	7%
With LDO	No	No	No	Yes
EMI	No	No	No	Yes

reduction included				
Single chip solution	No	No	No	Yes
Chip area	NA	$25mm^2$ (Package)	$5mm^2$ (Active area only)	$9mm^2$

CHAPTER 6 CONCLUSION

A single chip fully integrated isolated DC-DC converter using transformer coupled resonator is proposed. On-chip maximum power transfer is achieved by driving transformer coupled LC resonator at its resonant frequency.

The HFSS-based transformer design flow is introduced. Design target is to let the transformer operate at around 100MHz with high efficiency. Both primary and secondary side of transformer coil is optimized for Quality Factor, Inductance and coupling coefficient. Transformer test results show transformer's additional bond wire and PCB routing is the factor for lower coupling coefficient compare to transformer itself.

The switching frequency of the converter automatically tunes to the resonant frequency by using an on-chip peak power transfer frequency search algorithm. Compared to preset switching frequency, the adaptive peak power transfer approach improves the transferred power efficiency by 60%. An analog perturb-and-observe search algorithm is used to detect the resonance frequency by sweeping the driver frequency and detecting the primary side voltage. Peak power frequency detector, digital controlled oscillator are the main components of the system. Peak power frequency detector consists of two identical CMOS peak detectors, a comparator and a counter. A current starved digitally controlled ring oscillator is used to generate driver switching frequency. The binary weighted current source determines the frequency tuning range for the peak power transfer frequency detection circuit. This oscillator is also used as an interface to generate spread spectrum clock for the driver.

By using an isolated linear regulator and spread spectrum clocking together, the output peak ripple is reduced by 32dB and the EMI noise is reduced by 11dB. An on-chip EMI noise distribution sensor based on a ring oscillator with a noise detection sensitivity of 68dB is implemented for detecting the higher noise spots on the same chip of monolithic isolated converter. Measurements show that three locations close to the rectifier region has 2-3dB noise increase compared to other locations.

This converter is suitable for applications requiring minimum area and high level of integration, such as isolated power supply for sensors or high voltage compliant ADCs. Higher isolation and efficiency can be achieved by using advanced process like SOI process with low on-resistance Schottky diodes for rectifiers.

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