Parallel Doherty RF Power Amplifier

For WiMAX Applications

by

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ABSTRACT

This work covers the design and implementation of a Parallel Doherty RF Power Amplifier in a GaN HEMT process for medium power macro-cell (16W) base station applications. This work improves the key parameters of a Doherty Power Amplifier including the peak and back-off efficiency, operational instantaneous bandwidth and output power by proposing a Parallel Doherty amplifier architecture.

As there is a progression in the wireless communication systems from the first generation to the future 5G systems, there is ever increasing demand for higher data rates which means signals with higher peak-to-average power ratios (PAPR). The present modulation schemes require PAPRs close to 8-10dB. So, there is an urgent need to develop energy efficient power amplifiers that can transmit these high data rate signals.

The Doherty Power Amplifier (DPA) is the most common PA architecture in the cellular infrastructure, as it achieves reasonably high back-off power levels with good efficiency. This work advances the DPA architecture by proposing a Parallel Doherty Power Amplifier to broaden the PAs instantaneous bandwidth, designed with frequency range of operation for 2.45 – 2.70 GHz to support WiMAX applications and future broadband signals.

ACKNOWLEDGMENTS

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LIST OF ACRONYMS AND ABBREVIATIONS

3GPP	Third generation partnership project
4G	Fourth Generation
5G	Fifth Generation
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design Ratio
CAD	Computer aided design
CCDF	Complementary Cumulative Distribution Function
DC	Direct current
DPA	Doherty Power Amplifier
DPD	Digital pre-distortion
EER	Envelope elimination and restoration
ET	Envelope tracking
FET	Field Effect transistor
GaN	Gallium Nitride
HEMT	High electron Mobility transistor
IDPA	Inverted Doherty Power Amplifier
IC	Integrated circuit
IIP3	Third order input intercept point
IMD	Intermodulation distortion
IMD3	Third order intermodulation distortion
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long term evolution
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise figure
OFDMA	Orthogonal frequency division multiple access
OIP3	Third order output intercept point
P1dB	Output Power at 1 dB compression
P3dB	Output Power at 3 dB compression
PA	Power amplifier
PAE	Power added efficiency
PAPR	Peak-to-average power ratio
Psat	Saturated output power
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency

CHAPTER 1

INTRODUCTION

1.1 Motivation

With the growth of smartphones and Internet of Things (IoT), the demand for devices with high data-rates and broadband technologies is driven higher [1]. It continues to grow even further with the deployment of fifth-generation (5G) which supports pico-cells base stations [2]. Pico-cells are low power units which can be deployed at multiple locations in densely populated areas. It helps in spectrum reuse and more bandwidth.

The current telecom spectrum is already crowded with the 4G systems and it employs complex modulation schemes as OFDMA, CDMA etc. So, the concept of macro/pico/femto cells faces a huge challenge for linear amplification of signals and reduced power consumption.

To overcome such challenges, Doherty Power amplifier is an excellent technique to efficiently provide the linear amplification with maintaining high efficiency as well at large back-off power levels. But the linearity is achieved at the cost of power efficiency as in case of the RF power amplifier [3]. So, the tradeoffs between all the requirements to meet the design requirements are discussed in section 1.3.

1.2 Importance of RF Power Amplifier

The RF Power amplifier is usually the final block before the antenna in the transmitter chain. It is a critical block as RF PA needs to transmit the output power from a cellphone or base-station. As we can see from Figure 1 below which shows a general transmitter architecture. In Figure 1, I and Q (digital signals) are converted to analog

domain with the DAC blocks. After that the baseband signal is up-converted to RF signal with the help of a mixer block. The LO signal is generated from the VCO which goes to the mixer for up-conversion. At the end, the RF signal finally passes through some filtering and it comes at the input of the RF power amplifier block. Finally, the RF PA block amplifies the signal and transmits a high power through the antenna.

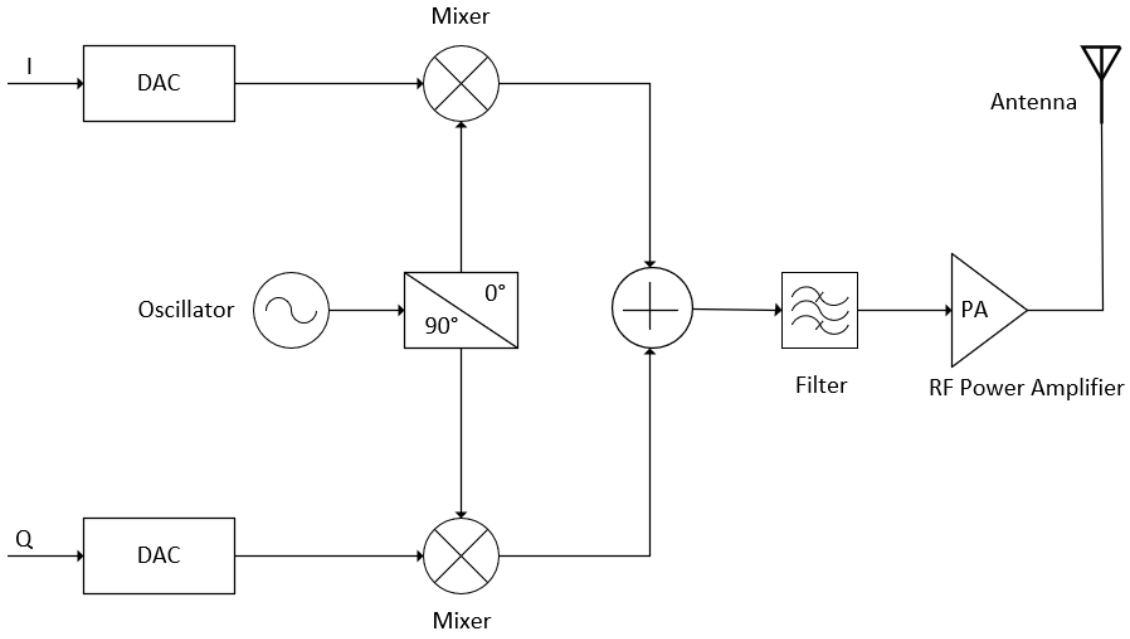


Figure 1 : A general Transmitter chain showing different modules

In the complete transceiver chain, RF Power amplifier is the most critical block. As we can see from Figure 2 which shows the power breakdown of a general transmitter [4], the RF PA consumes most of the power. So, if there is any improvement in terms of efficiency, output power for the RF PA block, it will have a significant impact on the overall transmitter performance. The other modules are also important in the transceiver chain but their impact on the overall performance is less compared to PA. The most critical specification for any RF PA block is efficiency, output power and linearity. With the current 4G-LTE standards and with the advent of 5G and IOT (internet of things), the RF

PA market seems to boom in upcoming years with new challenges and technologies. So, there is a significant growth in the field of RF power amplifier as can be seen from Figure 3 shown below. It can be seen there is lot of potential of RF PA design in the base-station, SATCOM, smartphones, military etc. There is especially a strong interest in base-station market with the advent of 5G market. Depending upon the applications and market needs, different classes of PA can be designed.

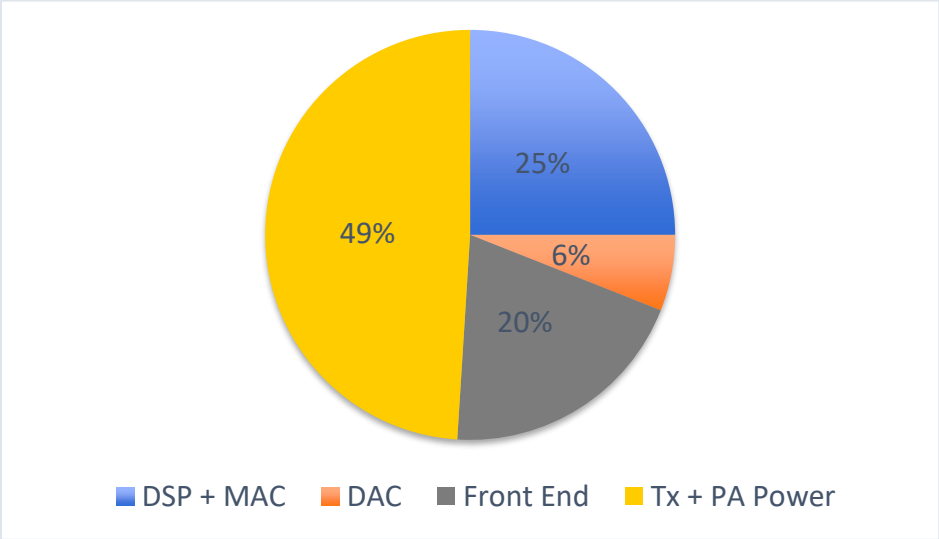


Figure 2 : Power breakdown of a typical RF Transmitter

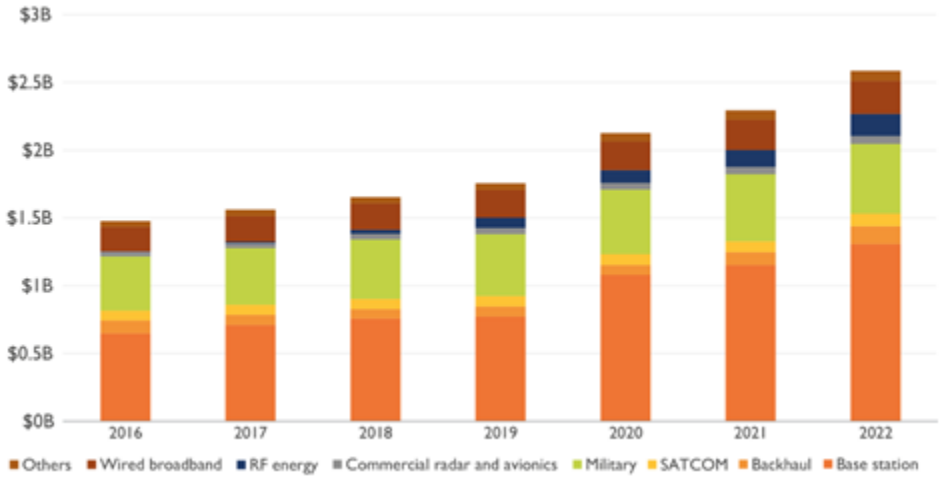
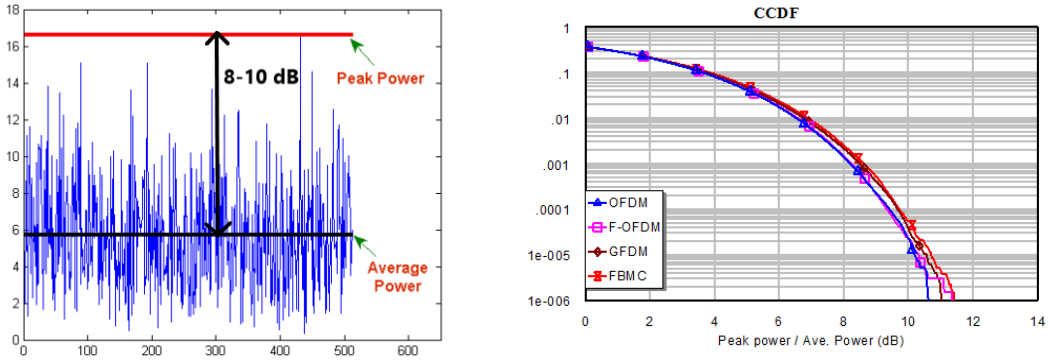


Figure 3 : RF Power Amplifier growth projections

1.3 RF Power Design Challenges

The RF Power Amplifier is a device that converts a low power radio frequency signal into high power signal. In this case, to efficiently amplify the signal with maintaining high linearity and operating bandwidth is still a challenge. There are inherent tradeoffs involved in this and designers are often challenged to decide among the most important requirements of the device. For example, the 4G standards as LTE needs to support bandwidths up to 20MHz and PAPRs [5] of 8 -10 dB for frequencies up to 2.6 GHz. Therefore, the RF Power amplifier operating within these frequency ranges needs to support the current requirements of the spectrum as mandated by FCC and achieve linear amplification.



(a) (b)

Figure 4 : (a) Signal with high PAPR, (b) CCDF of different high PAPR signals

The RF Power amplifier is classified into several categories depending upon design requirements. The basic is Class-A which provides high linearity, but the efficiency is low. To improve upon this, Class-AB, Class-B and Class-C have come up with better efficiency, but the linearity becomes poor. There are other switched-mode classes of PA as well to improve upon the efficiency. So, the designer needs to design the RF PA as per the requirement as there are tradeoffs involved between efficiency, output power and linearity.

1.3.1 Linearity of RF Power Amplifier

The linearity is one of the important aspects of the PA and many techniques have been developed to meet the stringent linearity requirements. Several linearization techniques such as Feed Forward Linearization, Cartesian Feedback, LINC (Linear Amplification using Nonlinear components) and DPD (Digital Predistortion) have been developed and implemented. Since the power amplifiers possesses memory-effects and non-linear capacitances, the linearity is not good. Some circuit level techniques are also used to reduce memory effects. In DPA, the linearity can be enhanced by choosing the correct bias of both the amplifiers and cancelling out their relative gm3 components [6].

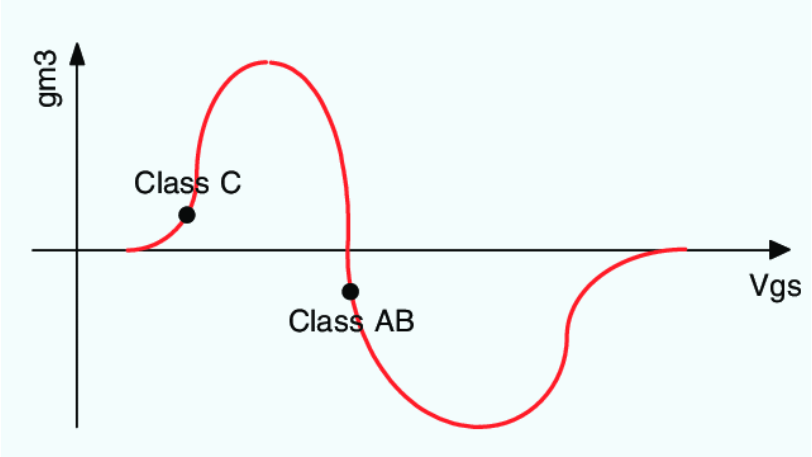


Figure 5 : gm3 component value for class-AB (Main) and class-C (Peaking)

1.3.2 Bandwidth of RF Power Amplifier

The Bandwidth which is usually the instantaneous bandwidth of RF Power amplifier is a major concern as most of the RF circuits are narrowband. So, using a complex technique for the RF Power Amplifier design and using it for wide bandwidth is a big challenge along with achieving high efficiency and linearity. The benefit of designing a RF Power amplifier for wide bandwidth saves area as we don’t need to use multiple PAs for

different bands. Also, the complexity of the circuit is reduced. So currently there are lot of publications coming up in RF power amplifier domain based on broadband PA design.

1.3.3 Efficiency of RF Power Amplifier

The Efficiency of RF Power amplifier is a major performance metric in the PA design. As RF Power amplifier is the final block in the transmitter chain, it transmits a lot of power. The major power of the whole transceiver is consumed by the PA. Therefore, efficiency is a major concern in the RF PA design. As less efficiency leads to more DC power dissipation which is generally dissipated in the form of heat. Also, high efficiency is achieved for maximum power level in linear PAs. This means efficiency degrades with lower power levels or in other terms efficiency degrades in the back-off. So, maintaining high efficiency at peak and higher back-off levels is a big challenge for the RF Power amplifier design.

1.3.4 Output Power of RF Power Amplifier

It is important that we get maximum power out of the RF Power amplifier with the use of matching networks. As we know the input and output impedances of the PA are generally complex. So, proper matching networks are employed to match complex impedance to 50 Ω load or source. Multiple ways of matching are possible which involves waveform engineering [7], load and source pull. So, Doherty power amplifier is a very popular technique which is typically used to get maximum power out of PA along with maintaining high efficiency. There will be always some loss associated with the matching networks, combiner network and output matching in the DPA. So, obtaining the maximum power out of a transistor is a very challenging task in the Doherty design.

1.3.5 Gain of RF Power Amplifier

High Transducer Gain is also an important requirement of the RF Power amplifier. It is always desirable to get maximum output power, but gain is also needed at the same time. Since, the GaN devices are highly non-linear due to intrinsic properties (like non-linear capacitances and diodes) and memory effects, maintaining a linear gain across the varying power levels is also a challenge. The linearity of gain is very important as it directly correlates with linearity of the PA device which needs to comply with the spectrum requirements. Although high gain is desirable for any RF PA circuit but there is a limit on the maximum value of gain known as G_{MAX} and maximum stable gain M_{SG} [8] which we can achieve for a given transistor.

1.3.6 Stability of RF Power Amplifier

The stability of a RF Power amplifier is very critical especially with the GaN devices. Figure 6 shows the source, load, input and output reflection coefficients seen on a general transistor amplifier circuit.

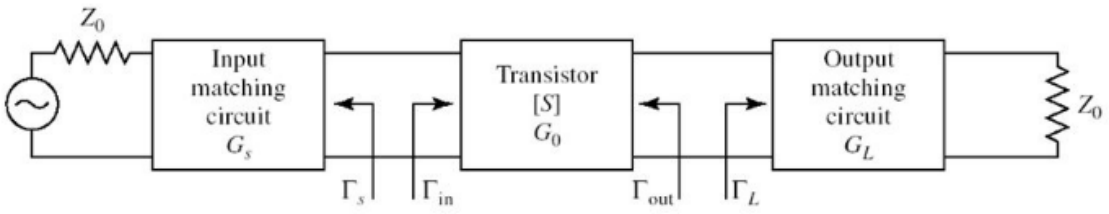


Figure 6: A general Transistor amplifier circuit

We can see some oscillations if either the input or the output port impedance has negative real part. This is due to fact that either $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$ which means positive feedback. There are some sets of equations for unconditional stability that can be expressed from Rollet's stability factor (k-factor) where the $k > 1$ and determinant matrix $|\Delta| < 1$ [9].

Apart from this there are two other factors of stability known as Mu1 and Mu2 which measure the radius from the center of the Smith chart to the nearest unstable point in the output and input plane respectively. The Mu factors adds an extra piece of information apart from K-factor as it tells which side of the circuit the instability is coming from. For the stability of an amplifier, the K-factor should be greater than one and same criteria goes with the Mu-factors as well.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12} \cdot S_{21}|} > 1$$

$$|\Delta| = |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}| < 1$$

Figure 7 : K and |Δ| factor criteria for unconditional stability

1.3.6 GaN Transistor for RF Power Amplifier Design

There is an increasing use of the GaN technology in the RF Power amplifier design these days. This is because GaN technology gives some advantages [10] over other which makes it a better choice for the power amplifier design. Firstly, GaN is used for high power devices. This is because it got high breakdown voltage, high peak current (saturated velocity) and higher current capability. Secondly, we can expect higher efficiencies with the GaN devices. This is because it got lower knee voltage (Vmin), higher breakdown voltage (Vmax), it can cutoff current at high voltage (lower Imin), lower semiconductor and circuit losses and lower parasitic capacitances. Thirdly, GaN devices are highly reliable because they sustain high reliability operation, high reliability process and low thermal resistance. All these advantages make GaN an excellent choice for the RF power amplifier design and therefore, in our design, we have also used the same devices for the research.

In nutshell, the comparison between the GaN and other technologies is shown below in Figure 8, and it can be clearly seen that GaN is an excellent choice for the RF PA design as it out-performs other technologies on various parameters.

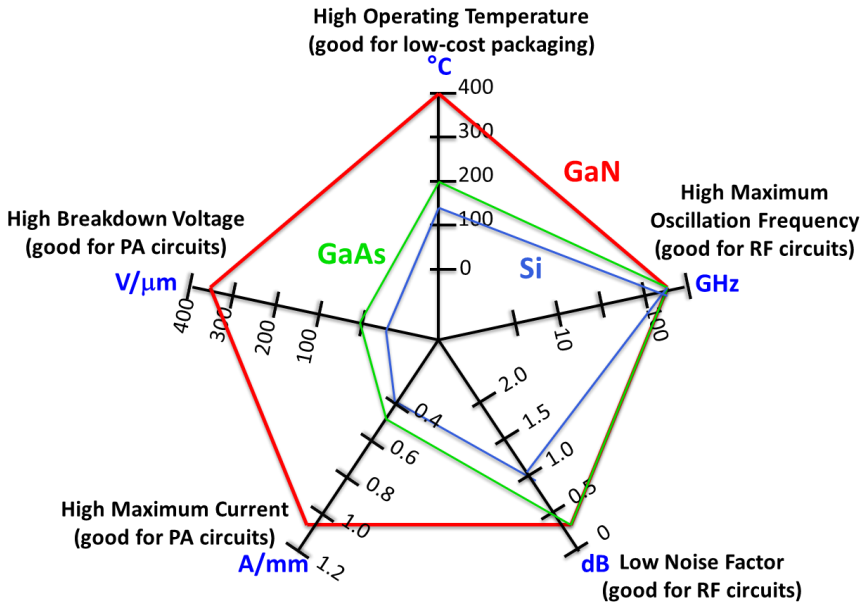


Figure 8: GaN vs other Process Technologies

1.4 Research Goals

The bandwidth of RF Power amplifier is a major concern as most of the RF circuits are narrowband. So, using a complex technique for RF Power Amplifier design and using it for wide bandwidth is a big challenge along with achieving high efficiency and linearity. Designing a RF Power amplifier for wide bandwidth saves area as we don't need to use multiple PAs for different bands. Also, maintaining high efficiency for large back-off power levels is also a concern in the RF PA design. So, the main goal of this research is to come up with some different and enhanced architecture compared to the conventional Doherty PA which can give wider bandwidth and along with that maintain higher efficiencies at peak and back-off output power levels. Along with these two requirements,

the new PA should be able to maintain the correct impedance transformation ratio (ITR) in the back-off as well as peak power levels. Basically, the ITR should remain same as conventional Doherty along with high efficiency at peak and back-off power level.

1.5 Thesis Organization

The Thesis is being organized into six chapters. Chapter 1 presents the introduction to the motivation and research thrust of this thesis. Chapter 2 presents the overview of different classes of single stage PAs. Motivation for Doherty PA and working principle is being explained in that section. Chapter 3 presents the main aspects of the Parallel Doherty design with some small signal stability and DC-IV results. Chapter 4 presents the EM Simulation results and comparison of the results with other state of art work. Chapter 5 presents the final Board design and measurement results of the design. Chapter 6 shows the conclusion of the results obtained, proposes the future scope of this thesis. Table 1 shows the target specifications of the Parallel DPA to be designed in this thesis.

Parameter	**Target**
Application	Macro-Cells
Doherty Type	Symmetric (1:1)
Frequency Range	2.45 – 2.70 GHz
Instantaneous Bandwidth	250 MHz
Process Technology	GaN HEMT (CGH60008D)
Power Range	16 W (42.04 dBm)
Efficiency (Peak)	>70 %
Efficiency (8-dB OBO)	>50 %
Gain	>10 dB

Table 1: Parallel Doherty PA design Target

CHAPTER 2

BASICS OF RF POWER AMPLIFIER DESIGN

2.1 Different Classes of RF Power Amplifier

The RF Power amplifier can be classified into different classes based upon the DC gate bias applied to the transistor. The class of operation [11] determines the portion of RF signal for which there is an output current in the transistor. The conduction angle is the period of the waveform when the device is conducting. The classes range with highly linear to non-linear with increase in efficiency.

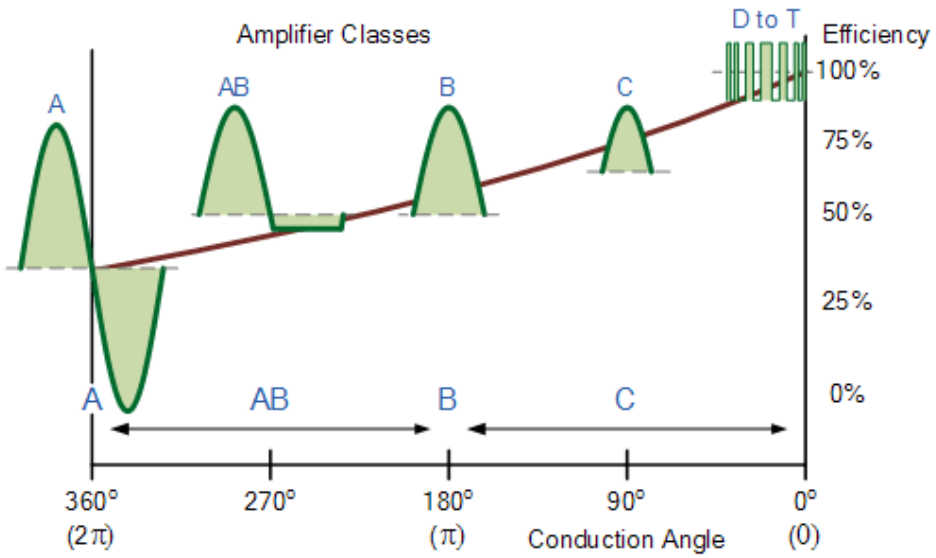


Figure 9 : Different RF Power Amplifier Classes and Efficiency

Figure 9 shows the graph for the different classes of RF power amplifier and their maximum theoretical efficiency achieved. As we move from class A and class C (linear PAs), the load line moves out of saturation. Class F, D and E are mainly in the ohmic or pinch-off regions. These kinds of PA work in the on-off mode and are famously known as switch-mode power amplifiers. These classes of PA basically try to reduce the current and

voltage overlap to reduce the power dissipation and increase efficiency. For simplicity purpose, we will consider a FET (field-effect transistor) device for explanation but same concepts go for other devices as well like BJT (bipolar-junction transistor).

2.1.1 Class A

This is the basic class of operation in which we set the gate bias (Q-point) at the center of load line such that there is a constant DC current flow in the transistor. The conduction angle of the output current is 360º (without any clipping). The current and voltage waveforms contain frequency content only at DC and at the operating frequency.

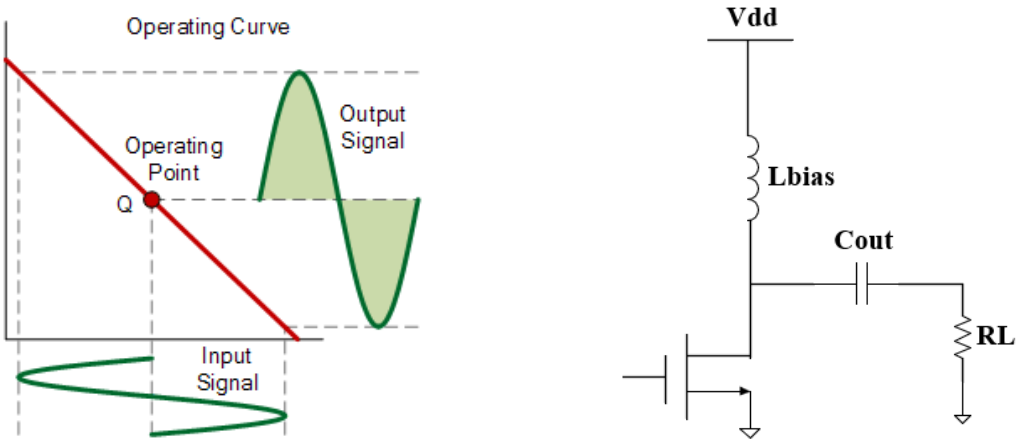


Figure 10 : Class-A RF power amplifier operation

Ideally no harmonic content is present in the output current and no external filtering is required. So, the linearity for the class-A operation is excellent and better than other classes of PA. But since there is always some constant DC current flow even if there is no RF signal, the efficiency for this class of operation is less. Theoretical maximum efficiency is 50% which means half of the output power is lost as heat. This not only wastes power and limits the operation of batteries but also increase operating costs and require high-rated output devices. While obtainable efficiency rarely exceeds 30-40% due to the nonlinear

effects of the transistor and finite quality factors of passive components. Mostly the baseband analog circuits work in class-A configuration but since RF PA is the power-hungry block in the transceiver chain, it needs to be biased in other higher efficiency class.

2.1.2 Class B

In this class of operation, we set the gate bias (Q-point) exactly at the threshold point of the device such that there is no constant DC current flow in the transistor which means ideally class B amplifier operates at zero quiescent current. The conduction angle of the output current is 180^{o} with current waveform half rectified. The current and voltage waveforms contain frequency content at other RF frequencies as well due to harmonics.

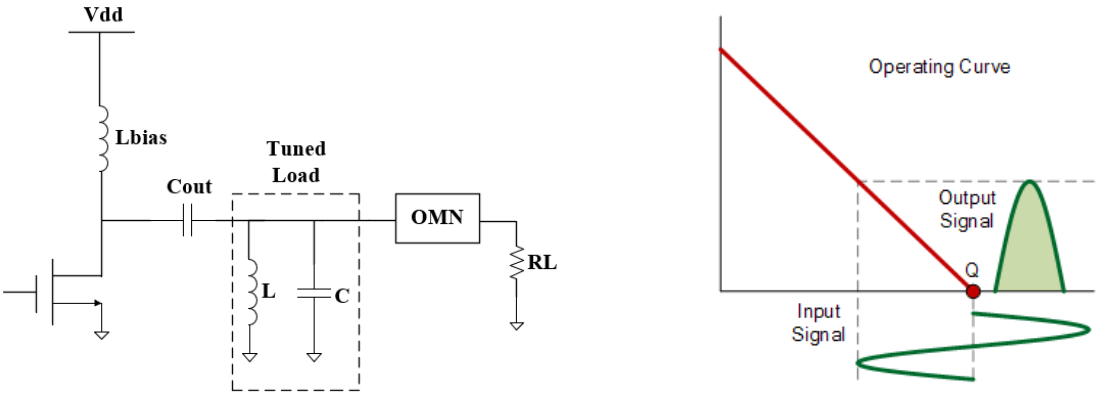


Figure 11 : Class-B RF power amplifier operation

Harmonic content is present in the output current and external filtering is required at the output. So, the linearity for the class-B operation is poorer than class-A but the efficiency is better than class-A because the output current is present only when there is an input RF signal. Theoretical maximum efficiency for the class-B operation is 78.5 %. As the class B amplifiers generate only half of the sine-wave when used, therefore they are generally used in push-pull structure. In this configuration, one transistor conducts during positive half cycle of the input signal and the second transistor conducts during the negative

half cycle. This method ensures that the entire input signal is amplified and reproduced at the output load with a complete full cycle as can be seen from Figure 12 below.

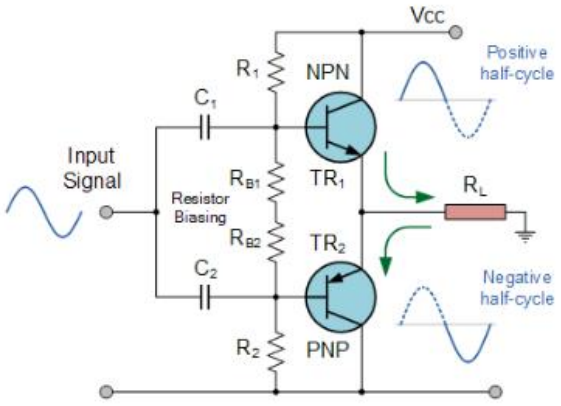


Figure 12 : Push-Pull Class-B RF Power amplifier operation

2.1.3 Class AB

In this class of operation, we set the gate bias (q-point) just above the threshold point of the device such that there is a small constant DC current flow. The conduction angle of the output current is between 180^{o} and 360^{o}. The current and voltage waveforms contain frequency content at DC and at other RF frequencies due to generation of harmonics. Most of the RF PA devices operate in the class-AB mode to achieve a good tradeoff between efficiency, power and linearity.

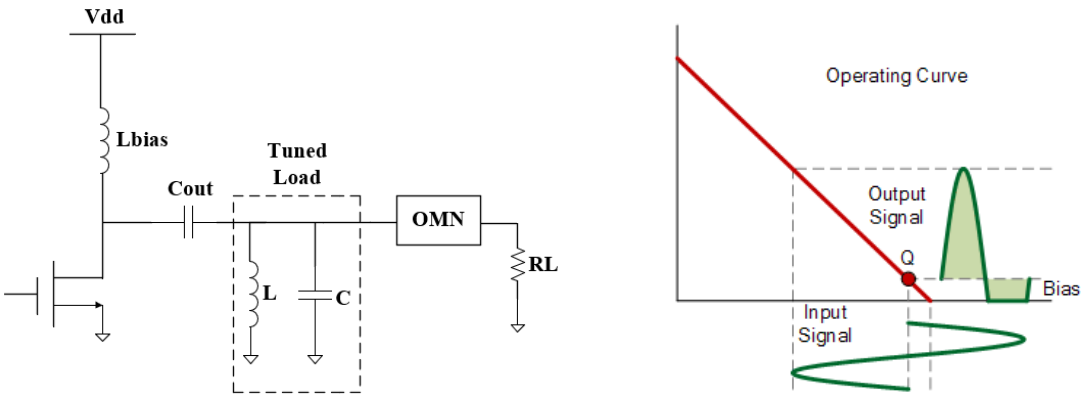


Figure 13: Class-AB RF power amplifier operation

Harmonic content is present in the output current and external filtering is required at the output. So, the linearity for the class-AB operation is better than class-B but poorer than class-A. Theoretical maximum efficiency is between 50% - 78.5%.

2.1.4 Class C

In this class of operation, we set the gate bias (q-point) below the threshold point of the device such that there is no constant DC current flow in the transistor. The conduction angle of the output current is between 180^{o} and 0^{o}. The current and voltage waveforms contain frequency content at other RF frequencies as well due to generation of harmonics.

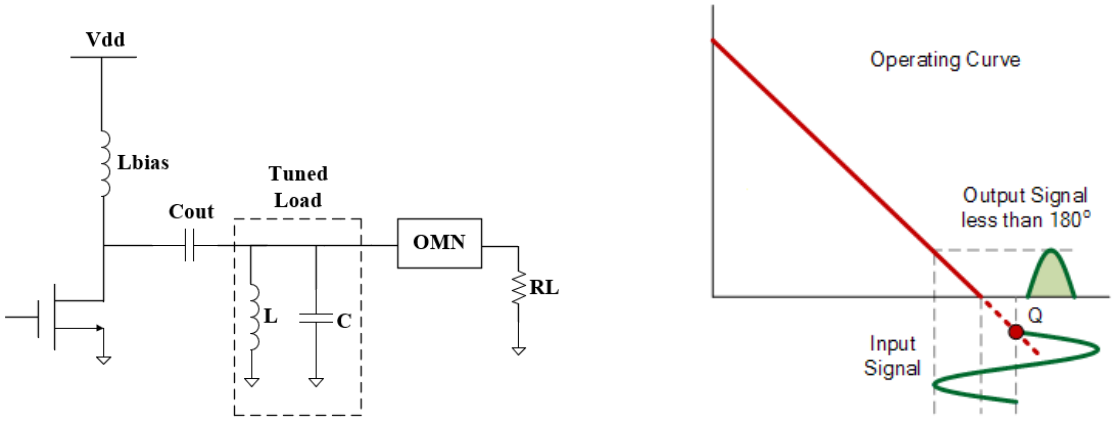


Figure 14 : Class-C RF power amplifier operation

Harmonic content is present in the output current and external filtering is required at the output. So, the linearity for the class-C operation is poorer than class-B but the efficiency is better than class-B. Theoretically, we can achieve maximum 100% efficiency, but the output will be highly non-linear, and the output power of device decreases as we move much deeper into class-C. Since the transistor is biased below the threshold voltage and is active for less than half of the input cycle, there exists a very high distortion at the

output signal. Although the efficiency of class-C amplifier is high, the swing of the input becomes large to conduct for less portion of input signal and it can sometimes exceed the gate source voltage breakdown. Therefore, implementation of class-C amplifiers becomes challenging for low breakdown devices. Also, the output power of these amplifiers is usually less, and these types of amplifiers are generally used in non-linear applications where the information is carried on the phase of the signal.

2.1.5 Other Classes of PA

There are additional classes of RF power amplifiers such as F, D, E, G, H and S. These PA are mainly targeted for high efficiency operation. In class-F, harmonic tuning at the output network is used to shape the voltage and current waveforms. This waveform shaping can be done by adding harmonics to the actual fundamental voltage or current [12]. In case of class-D [13], E [14] and S, they use the switching techniques. This is basically done to reduce the current and voltage overlap which saves the dissipated power and increases efficiency. In class-G [15] and H, it uses resonators and multiple power supplies to reduce the drain voltage and current product.

2.2 RF Power Amplifier Performance Metrics

The performance or figure of merit of a general RF Power amplifier can be decided based on various factors like output power, efficiency, gain, power-compression point, non-linearity, ACPR/ACLR, spurious emissions etc. Tradeoffs can obviously be made for achieving some better performance metrics over another. For this purpose, the various metrics like ffficiency, output power and linearity are explained below. The performance metrics varies from RF PA design depending upon the application it is used. For e.g. a PA

used in a smartphone may not have that as much stringent linearity requirements as compared to a PA used for a base-station application.

2.2.1 Output Power

Output power is the power delivered to the load (usually antenna 50Ω) at a desired fundamental frequency. Ideally, no power should be dissipated in harmonics.

$$P_{OUT} = \frac{Vout_{rms}^2}{RL}$$

$$P_{OUT\_AVG} = \frac{\int_0^T p(t)dt}{T}$$ For modulated RF signals

Where p(t) is the instantaneous power

$$P_{DC} = \frac{\int_0^T Vdd(t) * I(t)dt}{T}$$ Power from supply with Vdd varying with time

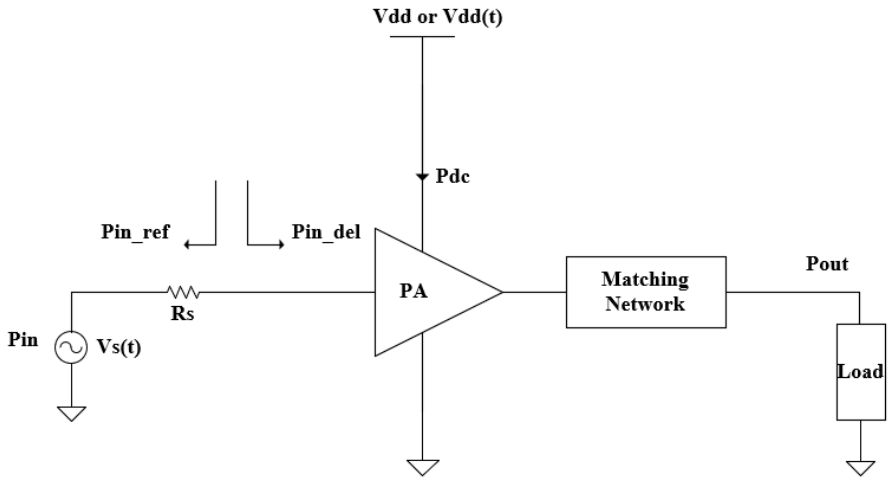


Figure 15 : Input and Output Power specifications for a PA device

P_{IN} = Input Power from Source

P_{IN_DEL} = Power delivered to the input of PA

P_{IN_REF} = Power reflected from input of PA

P_{DC} = DC power dissipated

P_{OUT} = Power delivered to the load

2.2.2 Efficiency

The Efficiency of a RF Power Amplifier is measured in terms of conversion of dc power to RF power. Higher efficiency is required at peak power and back-off power levels. Typically, the efficiency of any RF PA device decreases with back-off power and there are several efficiency enhancement techniques to address this issue.

Drain efficiency (DE) is a commonly used term which is termed as the output RF power delivered to load to the DC power dissipated.

$$\eta_{drain} = \frac{Pout}{Pdc}$$

Another commonly used term is Power Added efficiency (PAE) which is defined as difference of the output power and input power to the DC power.

$$PAE = \frac{Pout - Pin}{Pdc}$$

2.2.3 Gain

The Gain of a RF Power Amplifier is measured in terms of difference of output power delivered to load and input power available from the source (in dBm). High gain is always desirable, but we need to consider the stability of the device at the same time especially with the GaN devices. The difference between the output and the input power is generally known as Transducer gain (G_T).

$$G_T = P_{out}\ (dBm) - P_{in}\ (dBm)$$

Also, Power Gain (G_P) relates to the difference of output power delivered to the load and input power delivered to the PA.

$$G_P = P_{out}\ (dBm) - P_{in\_del}\ (dBm)$$

2.2.4 Gain Compression

In general, the PA will produce output power as the input power increases. But as the input drive increases up to a certain point, the gain of the power amplifier starts compressing and non-linearities become active.

P_{sat} = The power at which the PA starts compressing and further increase in input power does not result in increase in output power.

P_{1dB} = The power at which the Gain of power amplifier compresses by 1dB.

P_{3dB} = The power at which the Gain of power amplifier compresses by 3dB.

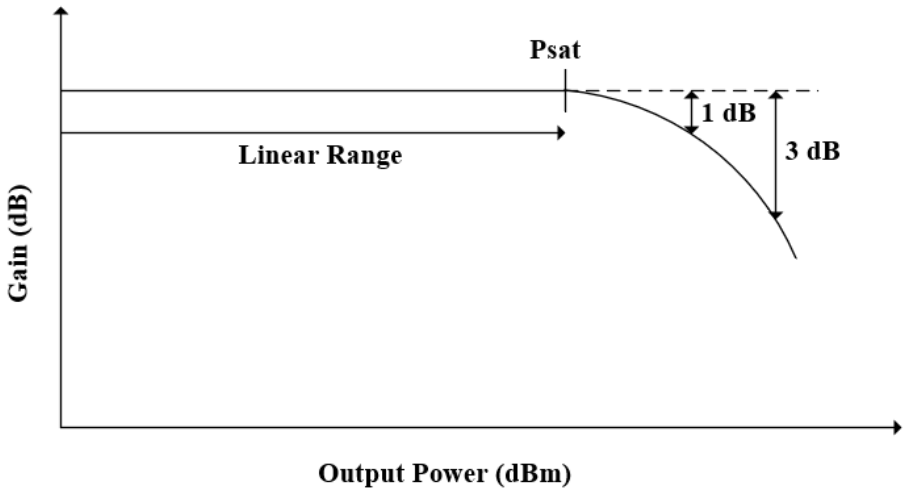


Figure 16 : Gain Compression vs Output Power

2.2.5 Linearity

In baseband analog, the amplifiers work in the small signal domain. But RF Power Amplifier is a block which deals with large signal excursions. So, it generates distortion because of non-linear behavior of PA. This non-linear behavior occurs due to gain compression in PAs. Intermodulation (IMD) distortion and Intercept Points are most commonly used to quantify non-linearity. Another non-linearity comes from the fact that

when we drive the PA into compression by increasing the input power and the linear gain of device goes into the compression. These days digital predistortion (DPD) is being used to improve the linearity of RF PA but the tradeoff associated with it as it leads to decrease in efficiency by adding more to the dissipated power.

Intermodulation Distortion (IMD) : When a RF Power Amplifier is excited with multiple signals separated in frequency simultaneously, then we can see multiple frequency components apart from harmonics. Harmonics can be filtered out from the output spectrum, but Intermodulation products [16] are difficult to filter out as they occur very closed to actual frequency signals. A filter with a very high-Q (sharp narrowband response) is required in case of filtering the in-band IMD products. The odd order intermodulation harmonics are close to the actual fundamental frequencies f1 and f2.

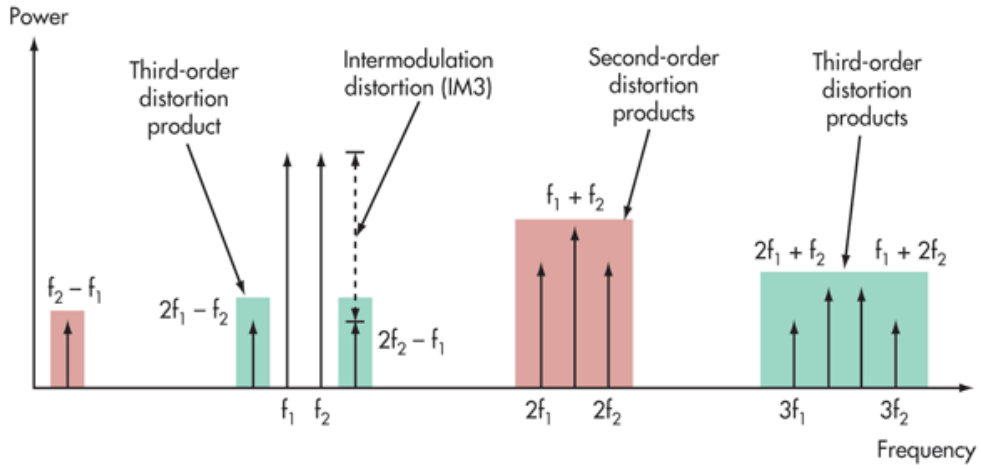


Figure 17 : Intermodulation Frequency Products

Intercept Point : As the input power of the RF Power amplifier increases, the amplitude of the harmonics also increases. If the amplitudes of the fundamental and higher order products are plotted, then the point at which third order intermodulation product intersects the fundamental power referred to as IIP3. Higher the IIP3 value, better will be

the linearity of the device as the third order intermodulation products intersects the fundamental tone at higher input powers.

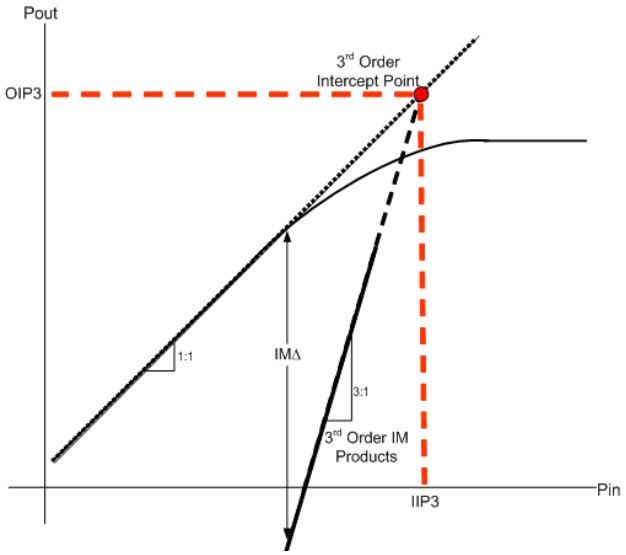


Figure 18 : Third-Intercept Point

Gain Non-linearity (AM/AM) : The gain of RF PA is dependent upon the input signal amplitude. Whenever a change in the input signal amplitude causes a non-linear change in the output amplitude, it is called AM/AM distortion. It is mostly due to the 3rd, 5th and higher odd order terms. This effect is more prominent when we increase the input drive levels and the PA goes into saturation at the 3-dB gain compression point.

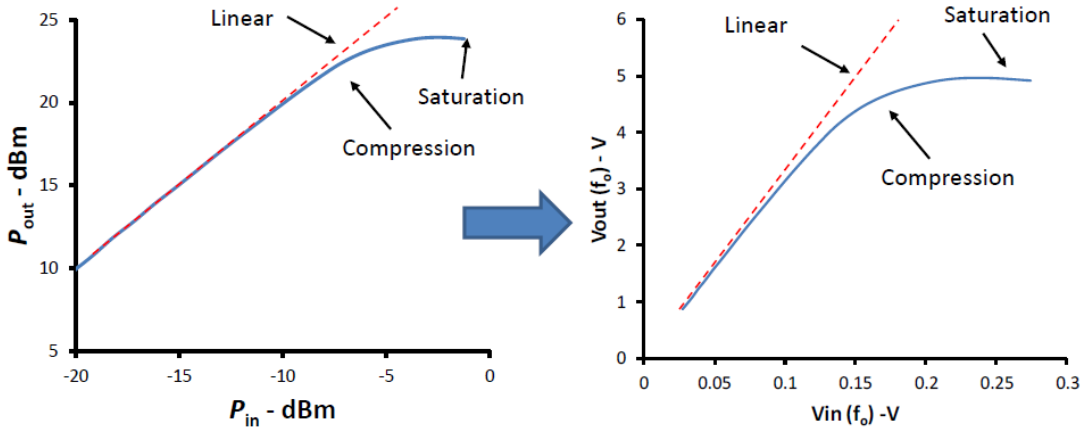


Figure 19 : AM/AM response when device goes into compression [17]

Phase Non-linearity (AM/PM) : The phase of the output signal depends upon the input signal. Any change in the input signal amplitude causes a change in the output signal phase and this form of distortion is called AM/PM. The effect becomes more prominent when we increase the input drive.

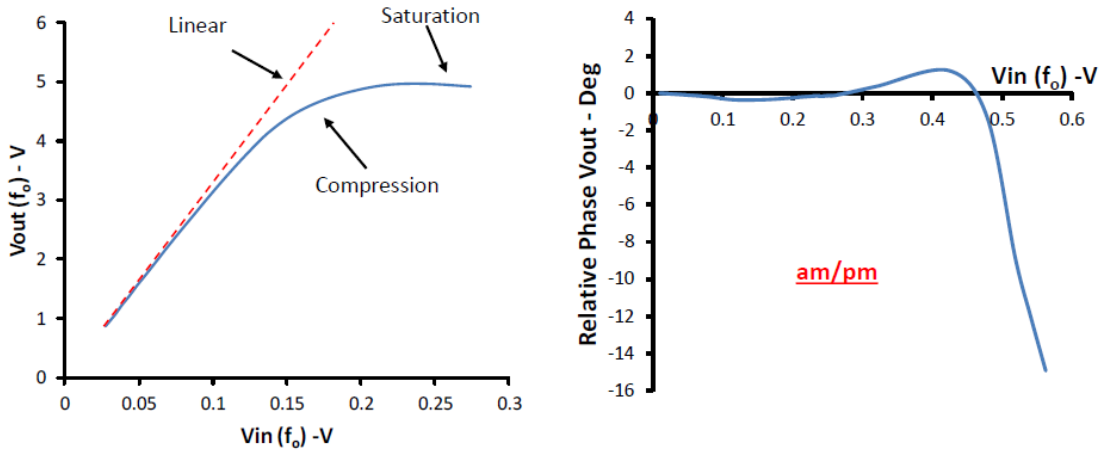


Figure 20 : AM/PM response when device goes into compression [17]

2.3 Efficiency Enhancement Techniques

There are few techniques for efficiency enhancement for large back-off power levels in RF PAs. Single stage PAs are good for achieving high efficiency at max power, but it is difficult to maintain the same efficiency performance at back-off levels. This is needed because the non-constant envelope signals have large peak to average power ratios (PAPRs) of around 8 dB. Also, in the 4G-LTE standards and with the new 5G technology, the PAPR level of the signal is increasing. So, for linear amplification of the signals, the PA needs to operate more at large back-off levels. To improve upon this several techniques [18] have been proposed like Envelope elimination and restoration (EER), Envelope tracking (ET), Chireix Outphasing and Doherty Power Amplification. All the techniques are explained in the next section with its associated advantages and disadvantages.

2.3.1 Envelope elimination and restoration (EER)

The envelope elimination and restoration (EER) is also known as Kahn method. It consists of a highly efficient non-linear amplifier and a limiter that eliminates the envelope. An envelope detector and a limiter configuration split a modulated RF input into its polar form. The output signal maintains a constant amplitude, but the phase information is modulated. A constant envelope enables the non-linear amplifier to operate near compression without any distortion which enhances its efficiency. The envelope information is restored at the output by modulating the supply voltage of the Power amplifier and the modulating signal is extracted from the envelope detector. EER is an excellent technique for efficiency enhancement but it comes with its own challenges and problems like the phase and gain mismatch between RF and envelope path due to two different paths working at different frequencies. The efficiency and bandwidth of the drain modulator also add to its limitations. From the implementation side as well, the drain modulator design is complex and costly. Figure 21 shows as a general EER [19] system.

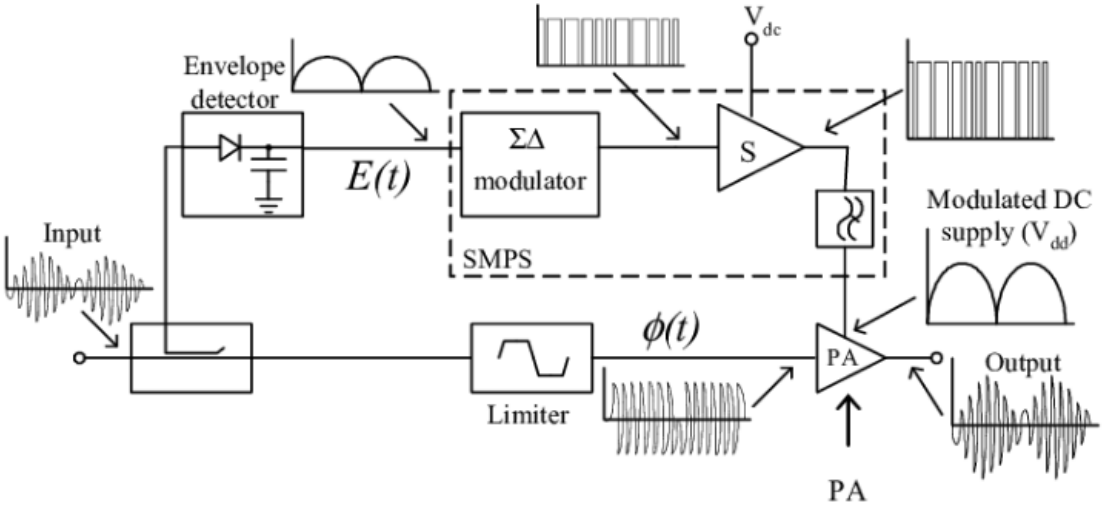


Figure 21: A conventional Envelope elimination and restoration system level diagram.

2.3.2 Envelope Tracking (ET)

Envelope tracking is similar method to the EER technique but in this the RF input signal contains both amplitude and phase information. Also, the transistor is operated in a linear condition where the DC supply is modulated with the input signal envelope. The DC power consumption is proportional to the signal envelope. In this system, the drain modulator does not need to be perfectly matched with the input signal envelope. This allows the ET technique to be more error and design relaxed as compared to the EER technique. But the main challenge is again the design of highly efficient dc modulator with high output voltage and current. The bandwidth of modulator is also a big challenge. In terms of efficiency, an envelope tracking system is less efficient than EER system, but it is a better scheme to implement due to its simplicity and usage. Due to this factor, it is widely implemented in several RF applications. Below shows the block level diagram of an envelope tracking system.

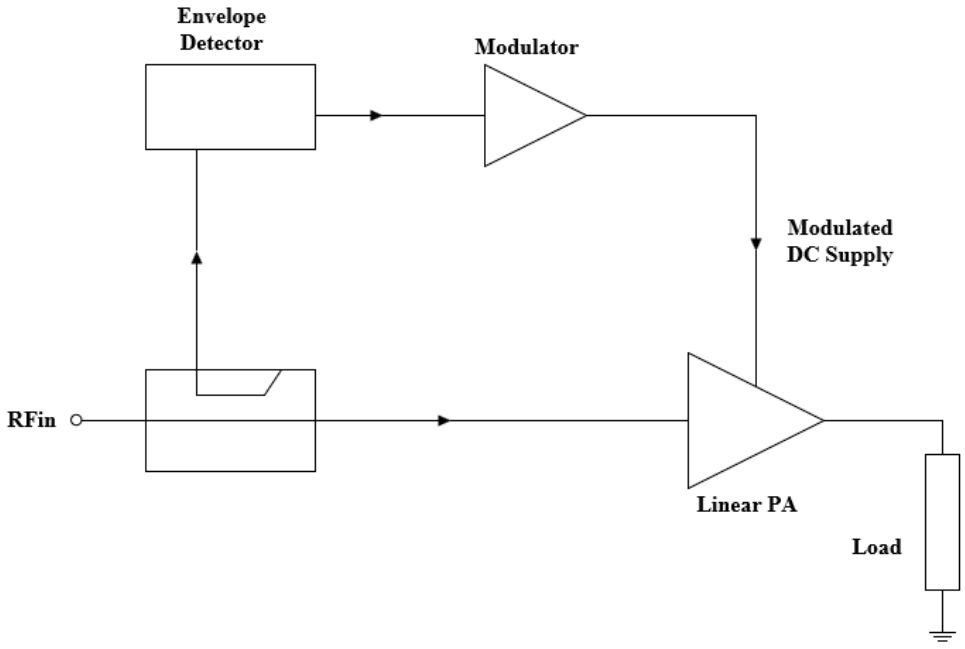


Figure 22 : Envelope Tracking system level diagram

This is a good technique to maintain high efficiency at peak and back-off power levels. Also, the complexity of design is less compared to EER which makes it more appealing choice for RF applications.

2.3.3 Chireix Outphasing

Chireix Outphasing power amplification method was first introduced by Henri Chireix in 1930s [20]. In this method, we use two nonlinear amplifiers to amplify two input signals with different phases and finally combine them using a power combiner to regain amplitude and phase modulated signal. The important components in this technique are the AM-PM modulator and the output design of power combiner. In the conventional output power combining, the output could result in loss when the phases of two input signals vary (non-synchronous phase characteristics). Therefore, to overcome this issue usually a reactance compensation load design technique is used which results in improved efficiency in the back-off power level region.

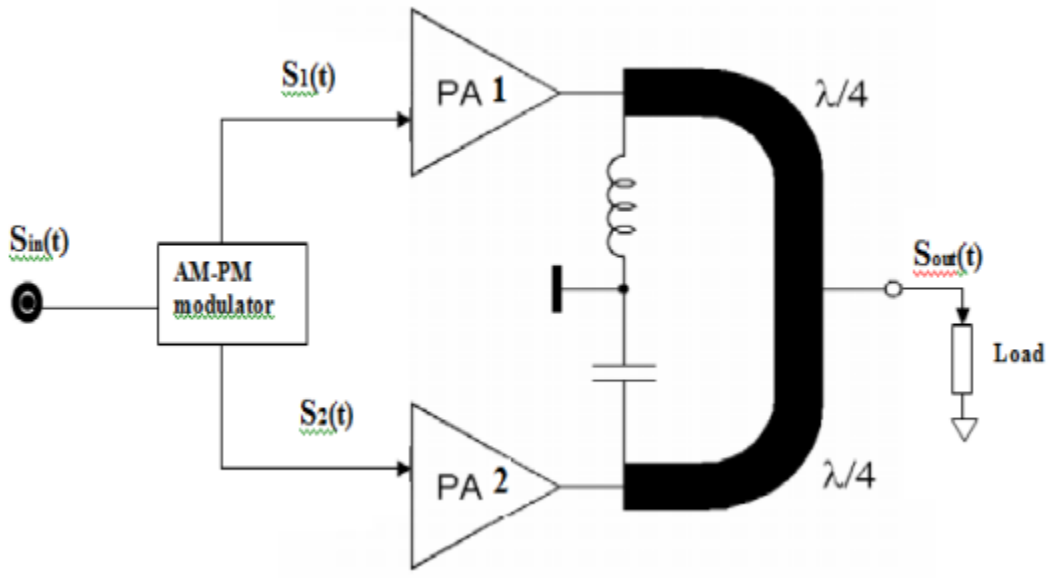


Figure 23 : A general Chireix Outphasing system [21]

2.3.4 Doherty Power Amplifier (DPA)

In 1936, William H. Doherty introduced a novel technique [22] to enhance the efficiency of a RF Power amplifier at back-off power levels. It was originally designed with vacuum tubes. Due to Doherty technique, the RF power amplifier provides linear amplification with high efficiency. It uses a very simple circuit to achieve high efficiency linear amplification.

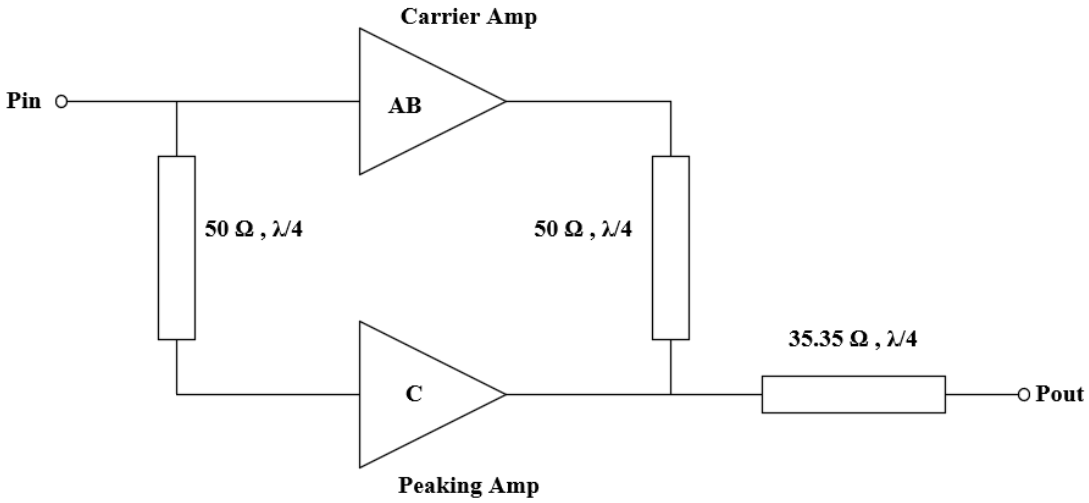


Figure 24 : A generalized Doherty-Power Amplifier Architecture

As shown in the circuit above, Doherty Power amplifier consists of two amplifiers namely main and peaking, connected in a parallel way with their outputs combined with a quarter-wave transformer. The main amplifier is also known as carrier and the peaking amplifier is also known as auxiliary. The main and peaking amplifiers are biased in class-AB and class-C respectively. The main motivation of biasing in this manner is that only the main will conduct for the low power and the peaking is off due to class-C biasing. But when the input power becomes high, the peaking also starts conducting with the main to achieve maximum efficiency. Since the efficiency and linearity performance of the main

and peaking amplifier are different, appropriate tradeoffs are made to achieve the effective optimized performance of the Doherty power amplifier.

DPA works on the principle of load modulation. In this, the load (or impedance) of the main amplifier is modulated by the current of peaking amplifier. The main amplifier is designed in such a way that it saturates after a certain point of desired back-off power level. As the main amplifier saturates, the peaking starts sourcing the current which modulates the load of main and ultimately reduces its impedance to source more current. The impedance of peaking amplifier is initially high, and it reduces later due to the current from main amplifier. Doherty technique is further sub-categorized into various architectures which includes Symmetric Doherty, Asymmetric Doherty (N-way) and N-stage Doherty.

2.4 Different Types of Doherty PAs

Depending upon the ratio of the peaking to the carrier amplifier, the Doherty design can be broadly categorized into three main sub-categories. When we take equal power PA devices in Doherty for both carrier and peaking, it is known as symmetric Doherty. And when the peaking power PA is different from the carrier PA, it comes under the category of asymmetric Doherty which is usually further categorized into N-way or N-stage. In the case of symmetric DPA, the first efficiency peak occurs at 6dB back-off and second at maximum power level. But in the applications where more than 6dB back-off efficiency is required, we go for the asymmetric DPA design. There are several issues associated with the asymmetric DPA like the design of large peaking amplifier. Also, there is reduction in gain as we need to make asymmetric power split at the input. The overall gain of DPA also becomes nonlinear due to the more nonlinear behavior of the peaking amplifier (class-C) .

2.4.1 Symmetric Doherty

In this architecture, the main and peaking are of equal size (1:1) or equal power. Both main and peaking contribute the same to the maximum output power. This is mainly designed for 6dB back-off power levels as the Doherty power amplifier will reach maximum efficiency at 6dB back-off and at the maximum power. In this DPA, the main and peaking are combined with the quarter-wave transformer and there is another impedance inversion from the load to the combiner node. In case of wideband matching, there can be low-Q matching network from the load to the combiner node. The quarter-wave transformer is usually responsible for presenting correct impedances to the main PA in back-off and max power level. If correct impedances are not presented, then it leads to power and efficiency loss. There is an additional offset line at the beginning of peaking PA to compensate for the phase difference between the main and peaking currents as both the currents should combine in the same phase to achieve maximum performance.

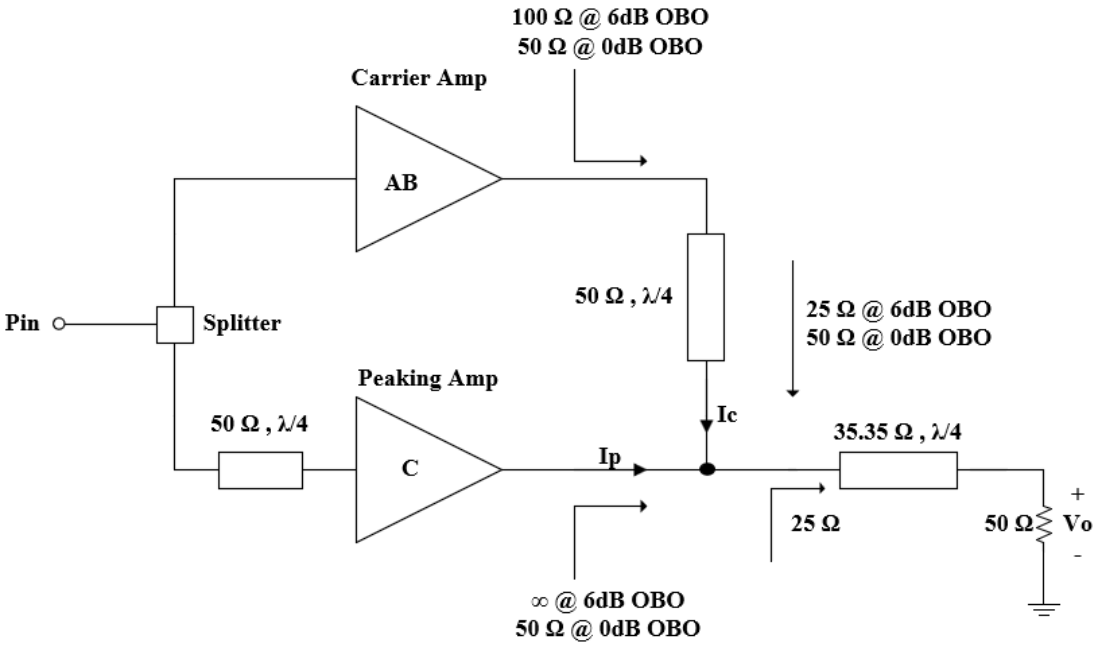


Figure 25 : A Symmetric (1:1) Doherty PA for 6dB back-off

2.4.2 Asymmetric Doherty (N-way)

In this architecture, the main and peaking are in different size or power ratios (1: N). The peaking amplifier delivers more power than main amplifier in this scheme and it turns on early at low input power levels. This is mainly designed for higher back-off power levels as the DPA reaches first maximum efficiency peak at 20log(N+1) dB and other at maximum power. There can be two ways of designing the asymmetric Doherty. Either we can take a peaking device which is 'N' times the main amplifier or we can connect 'N' equal size peaking amplifiers in parallel and turn those on simultaneously [17].

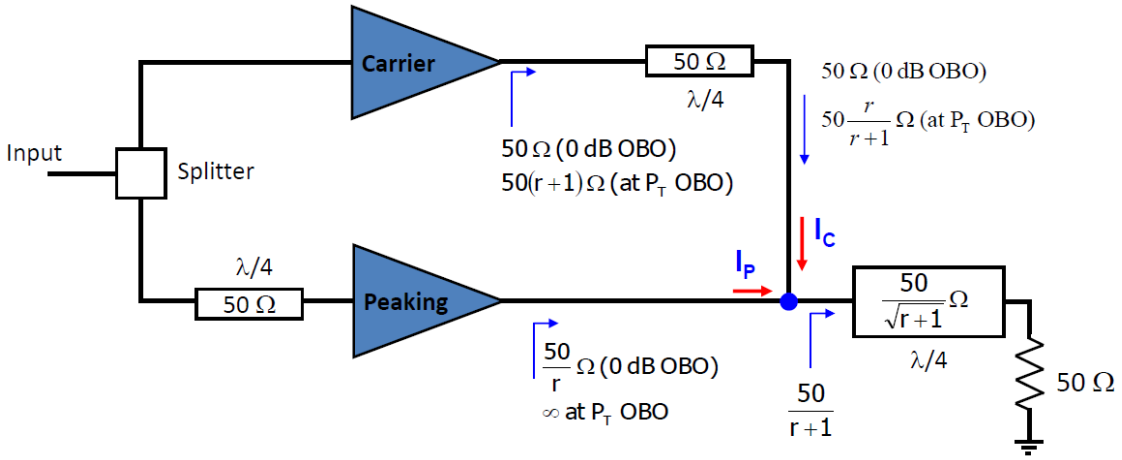


Figure 26 : An Asymmetric (1: r) Doherty PA

where, $r = \frac{Pp}{Pc}$ (ratio of peaking / carrier PA)

$\alpha = \frac{1}{r+1}$ (peaking amp on/off transition voltage)

For different values of r which is the ratio of peaking to the carrier PA, we can obtain different back-off power levels. For example, when r = 1 which is the symmetric DPA case, we obtain a 6dB back-off. When r = 2 , we get 9.5dB back-off and when r = 3, we can get 12dB back-off and so-on. The same behavior can be seen from the efficiency

graph below for different values of r. But increasing the value of r puts the size constraint on the peaking amplifier. Also, we need to split the input power asymmetrically which makes the Doherty power amplifier design more complicated.

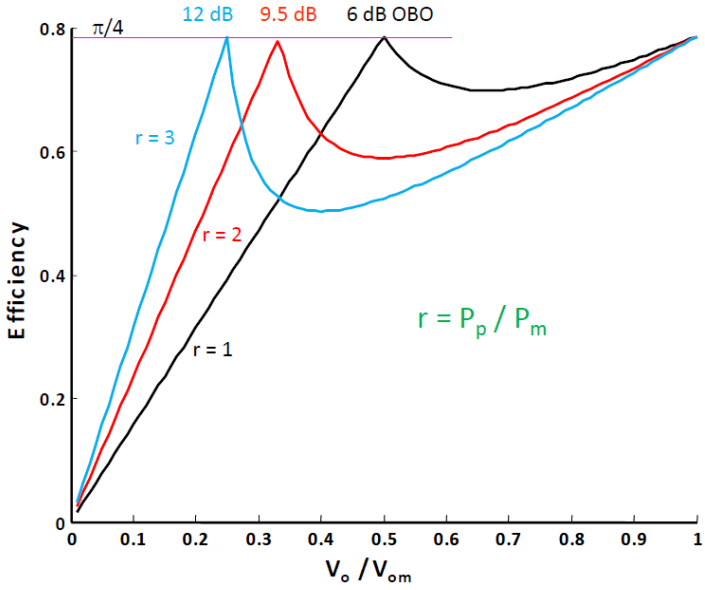


Figure 27 : Efficiency graph for different ‘r’ values [17]

2.4.3 N-stage Doherty

In this architecture, there are ‘N’ number of peaking amplifiers. The main and peaking are of equal size and are connected in one stage. The other peaking amplifiers are connected in other stages via quarter-wave transformers. This is mainly designed for multiple efficiency peaks before the maximum efficiency at maximum power. The main difference between N-way and N-stage Doherty is the turning on point of the peaking amplifiers. In N-way Doherty, the peaking amplifier (or multiple peaking PAs) usually turn on at the same biasing point. So, there is just one efficiency peak at back-off and one at maximum power level. But in the N-stage Doherty, multiple peaking PAs are connected in different stages via quarter-wave transformers and all the peaking PAs have different biasing and turn on point which basically leads to multiple efficiency peaks between the

back-off power level and maximum power level. Although N-stage Doherty seems to be better choice for efficiency enhancement but complexity wise, the N-stage Doherty is more difficult to design as compared to N-way Doherty due to multiples quarter-wave transformers in the path. Also, maintaining the correct phase between the main and peaking at different combiner nodes is a big challenge in design of N-stage DPA.

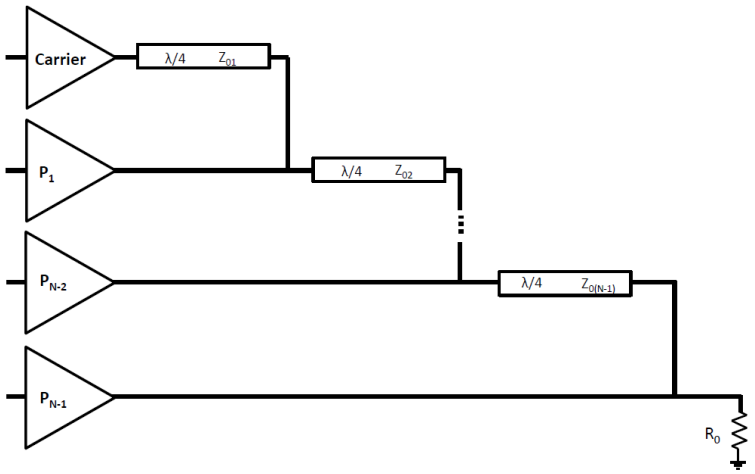


Figure 28 : A generalized N-stage Doherty Power Amplifier [17]

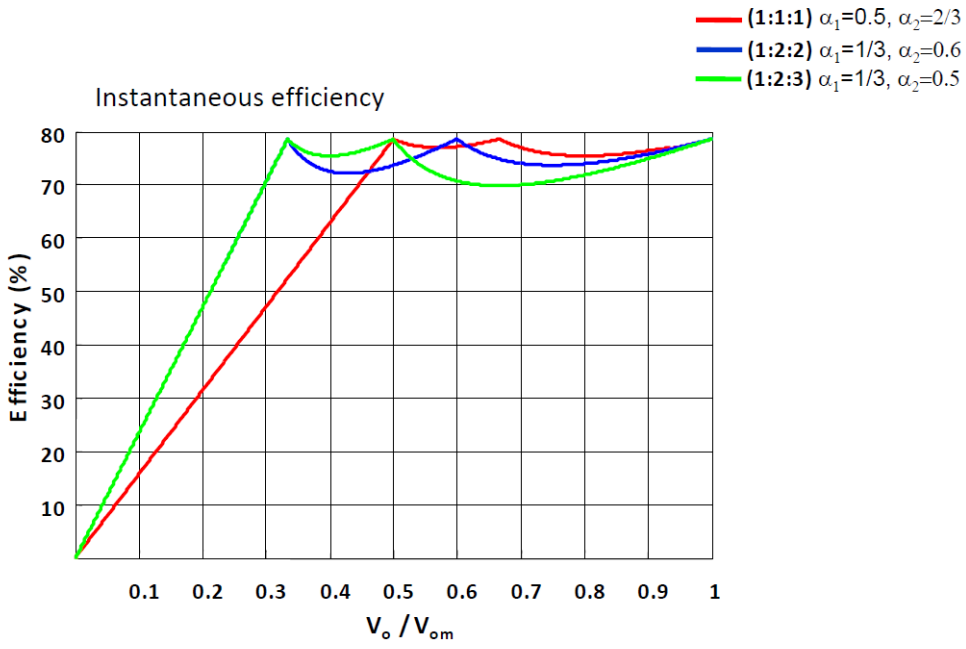


Figure 29 : Efficiency graph for N-stage Doherty Power Amplifier [17]

2.5 Doherty Power Amplifier Operation

The basic introduction to the Doherty Power Amplifier is given in section 2.3.4 already. In this section, the operation of Doherty power amplifier is explained in detail along with the load modulation concept. Doherty power amplifier was first introduced by William H. Doherty in 1936. He suggested a new high efficiency power amplifier for modulated waves with his work at Bell laboratories. Usually classical power amplifier architecture shows poor efficiency at large power back-off levels. Doherty PA architecture overcomes this problem and it promises high efficiency, output power and good linearity at large power back-off levels. Doherty PA technique is very popular technique these days especially in the infrastructure applications [23] for efficiency enhancement at back-off power levels due to its simplicity and using very few components to design.

2.6 Active Load Modulation

The basic idea of active load modulation is basically that the load impedance of one side of the source is modulated from the current of another source. Both the sources are connected to a common load and each source is sourcing current into that common load. Each current source can be assumed to be a FET device.

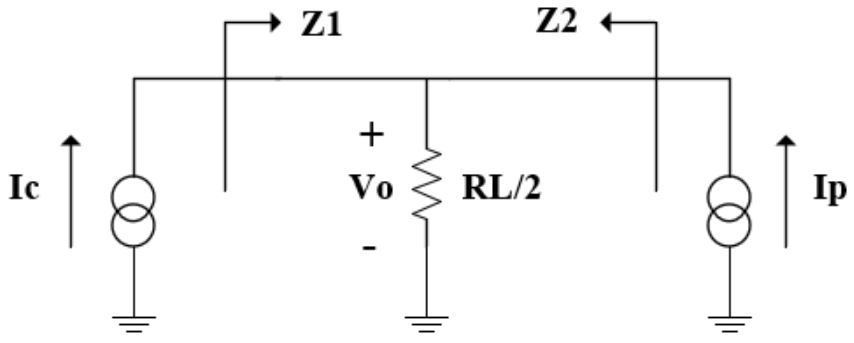


Figure 30 : Active Load-modulation

As we can see from Figure 30 above, there are two current sources connected to a common load. The two current sources are basically the main and peaking amplifiers without taking any device parasitics into account. The impedance seen by source 1 depends upon the current from source 2. The two current sources can be assumed to provide the same amount of current value at the peak input power level.

$$Z_1 = \frac{RL}{2}\left(1 + \frac{I2}{I1}\right)$$

$$Z_2 = \frac{RL}{2}\left(1 + \frac{I1}{I2}\right)$$

From Figure 30, I1=Ic= Main amplifier current and I2=Ip=Peaking amplifier current.

In the low-power case, when only the main is on and when the peaking is off i.e I2 = 0.

Therefore, $Z_1 = RL/2$ and $Z_2 = \infty$

In the high-power case, when both main and peaking are on i.e I1 = I2 = I.

Therefore, $Z_1 = RL$ and $Z_2 = RL$

The concept of active load modulation seems to be easy to understand. But there is a small problem with this arrangement for Doherty PA implementation. As we can see once the peaking turns on, I2 increases. With the increase in current I2, the impedance Z_1 also increases which is not desirable if main also needs to source more current at higher powers. Therefore, the direction of load trajectory needs to be reversed i.e., we need Z_1 to decrease with increase in I2 to supply more current.

To overcome this problem, an impedance inverter is included on the main amplifier's side which makes the impedance Z_1 to decrease with increase in I2. Due to this addition, high Z_1 at low power level and low Z_1 at high power level is achieved which is in accordance to the requirement for the proper working of Doherty PA.

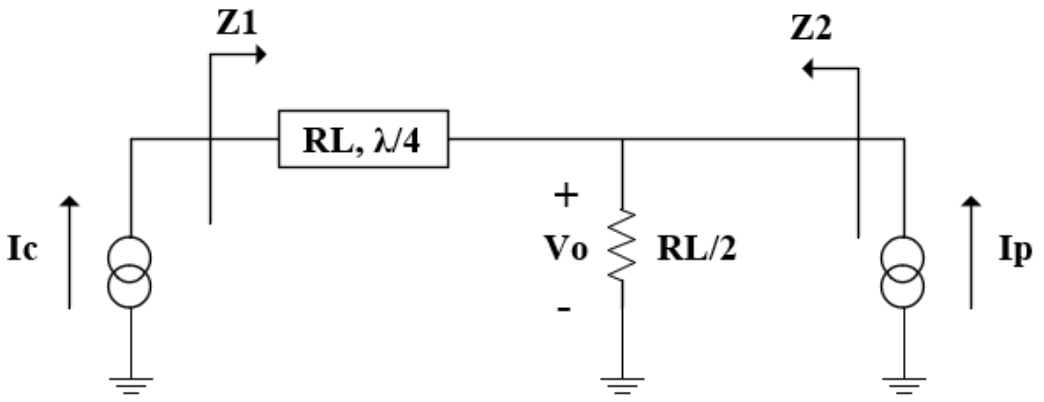


Figure 31 : Active Load-modulation in Doherty PA

From the Figure 31 above, we can see that a quarter-wave impedance transformer is added in the main path and both main and peaking amplifiers are combined to a common node with a RL/2 load. At Low power, the peaking is off i.e. I_P=0.

Z_1 = 2*RL and Z_2 = ∞

At High power, both main and peaking are on and I_C = I_P = I.

Z_1 = Z_2 = RL

In general, the load impedances of main and peaking amplifiers for the operating regions can be specified in the form equations shown below where V_{IN} is the signal voltage level and $V_{IN,MAX}$ is the maximum voltage level :

$$Z_C = \begin{cases} \dfrac{Z_T^2}{Z_L} & 0 < V_{IN} < V_{IN,\,Max/2} \\ \dfrac{Z_T^2}{Z_L\left(1+\frac{I_P}{I_C}\right)} & V_{IN,\,Max/2} < V_{IN} < V_{IN,\,Max} \end{cases}$$

$$Z_P = \begin{cases} \infty & 0 < V_{IN} < V_{IN,\,Max/2} \\ Z_L\left(1+\dfrac{I_C}{I_P}\right) & V_{IN,\,Max/2} < V_{IN} < V_{IN,\,Max} \end{cases}$$

Figure 32 : Main and Peaking impedances as Vin varies from 0 to Vin,max

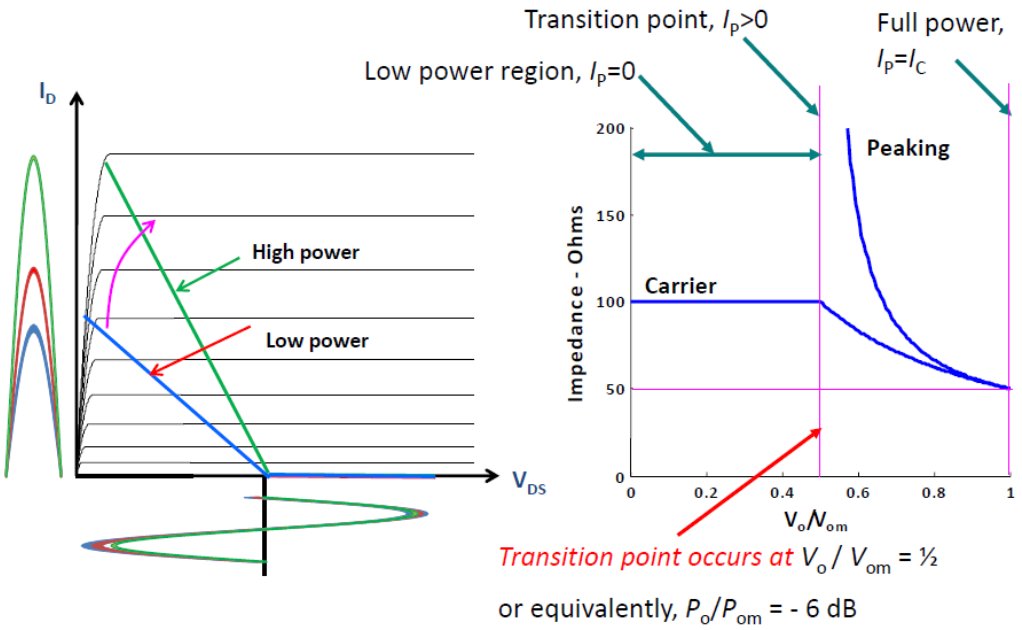


Figure 33 : Active Load-Modulation for a Symmetric Doherty PA [17]

As we can see from Figure 33, the impedance of the carrier is being modulated from 100Ω to 50Ω (Ropt = 50Ω) at peak power level due to the current from peaking. Similarly, the impedance of peaking is changing from ∞ to 50 Ω due to current from main.

2.6.1 Low Power Region

In the low power region, the input power level is low. So, only the main amplifier (biased in class-AB) is working while the peaking amplifier is off (biased in class-C). The peaking is intentionally made off with the help of offset lines. In this region, only half of the input power is used by the main amplifier as the peaking amplifier is off. The impedance seen by main is 2*Ropt and the current flowing is $I_{MAX/2}$. So, the main amplifier saturates at half of its total maximum power and the amplifier ideally achieves theoretical maximum efficiency of 78.5% (assuming close to class-B biasing). The first efficiency peak occurs at 6dB back-off from the maximum power.

2.6.2 High Power Region

In the high-power region, the input power level starts increasing beyond a certain level. So, now both the main and peaking starts sourcing the current. Due to this load of the main is modulated by the current of the peaking and vice-versa. Both the amplifiers source the current till the point when both amplifiers reach their maximum output power. The impedance seen by both amplifiers becomes Ropt and current flowing is I_{MAX}. So, the Doherty PA shows another maximum efficiency peak of 78.5% at maximum power level.

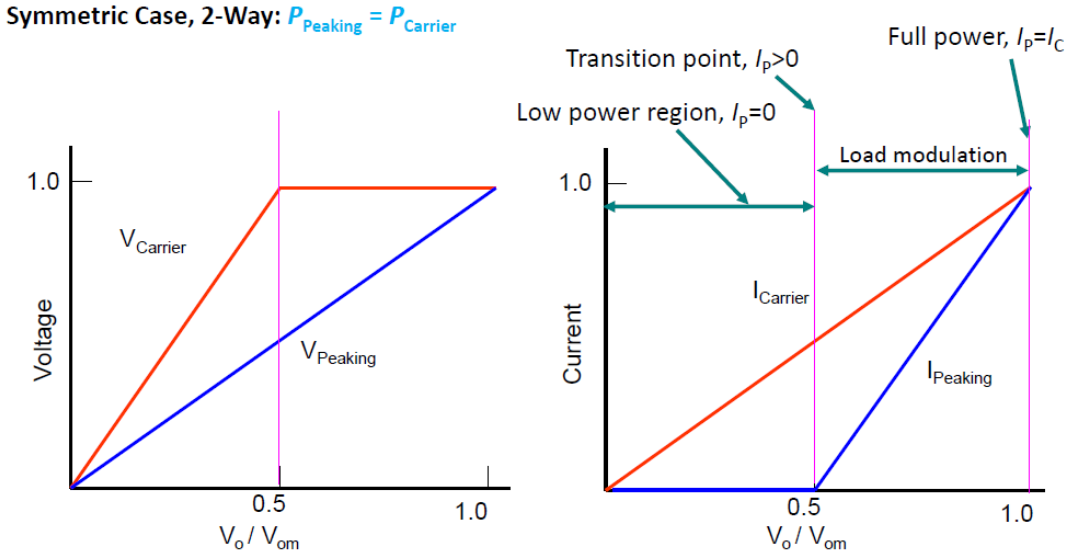


Figure 34 : Symmetric DPA voltage and current waveforms [17]

2.7 Other Doherty Power Amplifier Architecture

Apart from the conventional Doherty architectures which include symmetric, asymmetric (N-way) and N-stage, there are other architectures as well like Inverted Doherty, Digital Doherty and Parallel Doherty which use the same principle of active load modulation as that of conventional Doherty. But there is some difference in the architecture from the conventional Doherty. Depending upon the application, different Doherty configurations can offer several benefits and improvements with some associated tradeoffs.

2.7.1 Inverted Doherty

We can see the basic architecture of Inverted Doherty as shown in Figure 35. The inverted Doherty is different from the conventional Doherty in that the λ/4 impedance transformer is now used in the peaking path instead of carrier path. Due to this, instead of open circuit at the combining node in the peaking path, there is a short circuit. It is easier to make short circuit on the smith chart rather than open circuit as the output impedance of PA device is capacitive. This helps in reducing the length of offset line in the peaking path.

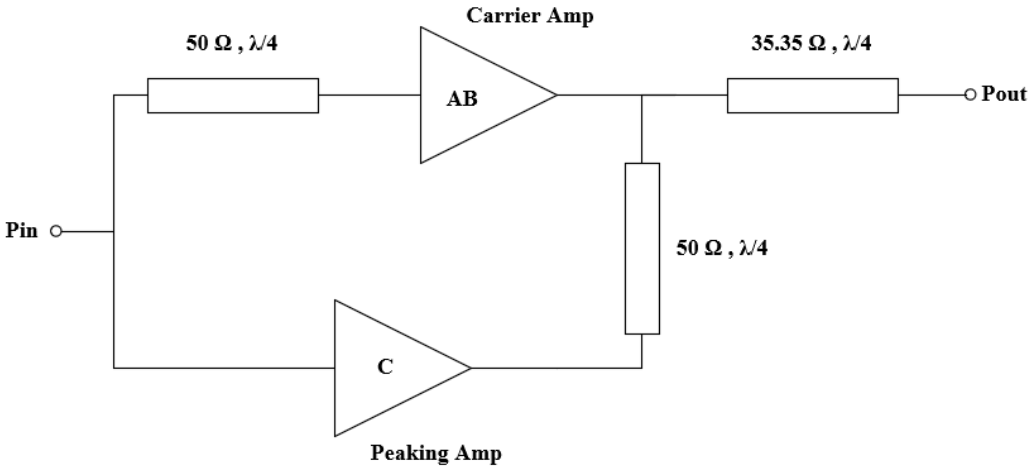
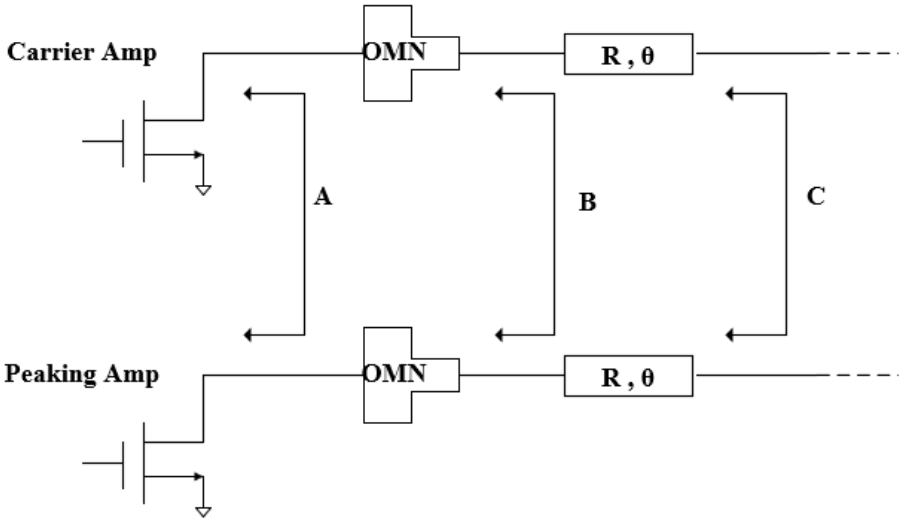
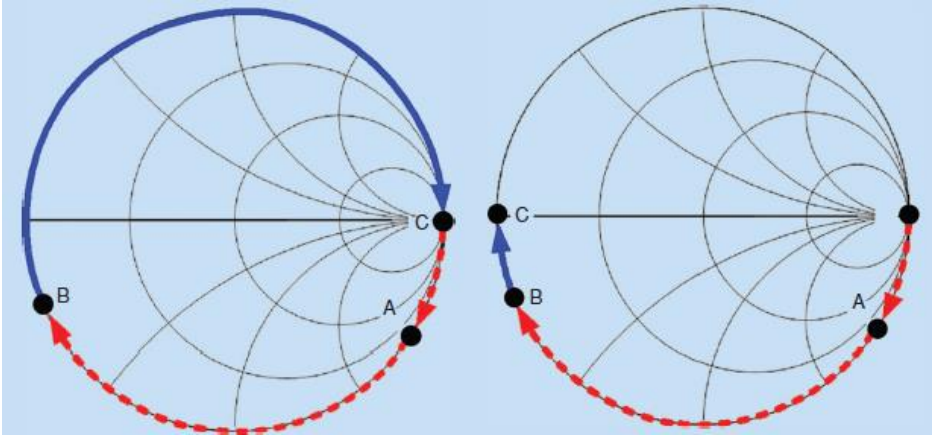


Figure 35 : A generalized Inverted-Doherty Power Amplifier Architecture



(a)



(b) (c)

Figure 36 : (a) Schematic diagram of simplified conventional and inverted DPA , (b) Γ_{OUT} trajectories for conventional DPA, and (c) inverted DPA [24]

As we can see from Figure 36 (a), the impedance at the output of device is usually capacitive which is marked by point A on the smith chart in Figure 36 (b) and (c). After the output matching, the impedance point moves to point B. After this we need an offset line to move from point B to point C on smith chart. As we can see, it takes more length of the offset line if move to open circuit Figure 36 (b) rather than short circuit Figure 36 (c). This shows that technique used in Figure 36 (c) is known as Inverted Doherty. It is called Inverted because of the reason as the λ/4 impedance transformer is now used in peaking path instead of carrier path. Also, the offset line in peaking path is now used to make the impedance as short circuit instead of open circuit.

2.7.2 Digital Doherty

Although the conventional Doherty offers some benefits over the other efficiency enhancement techniques due to its simple architecture, it still suffers from inherent limitations that compromises efficiency and instantaneous bandwidth. The Doherty PA

offers optimum performance when the carrier and peaking currents at the combiner node add up in the correct magnitude and phase. But since matching networks are usually implemented by transmission lines whose phase and magnitude tend to vary over frequency, the current combining will not occur in the desired phase. Also, we do not have control over the amplitude of signal in the peaking PA due to its class-C biasing. This leads to loss in maximum efficiency and output power when the designed Doherty PA is operated over different frequencies. Below shows a general architecture comparison of a conventional Doherty PA(analog) and a Digital Doherty PA (digital).

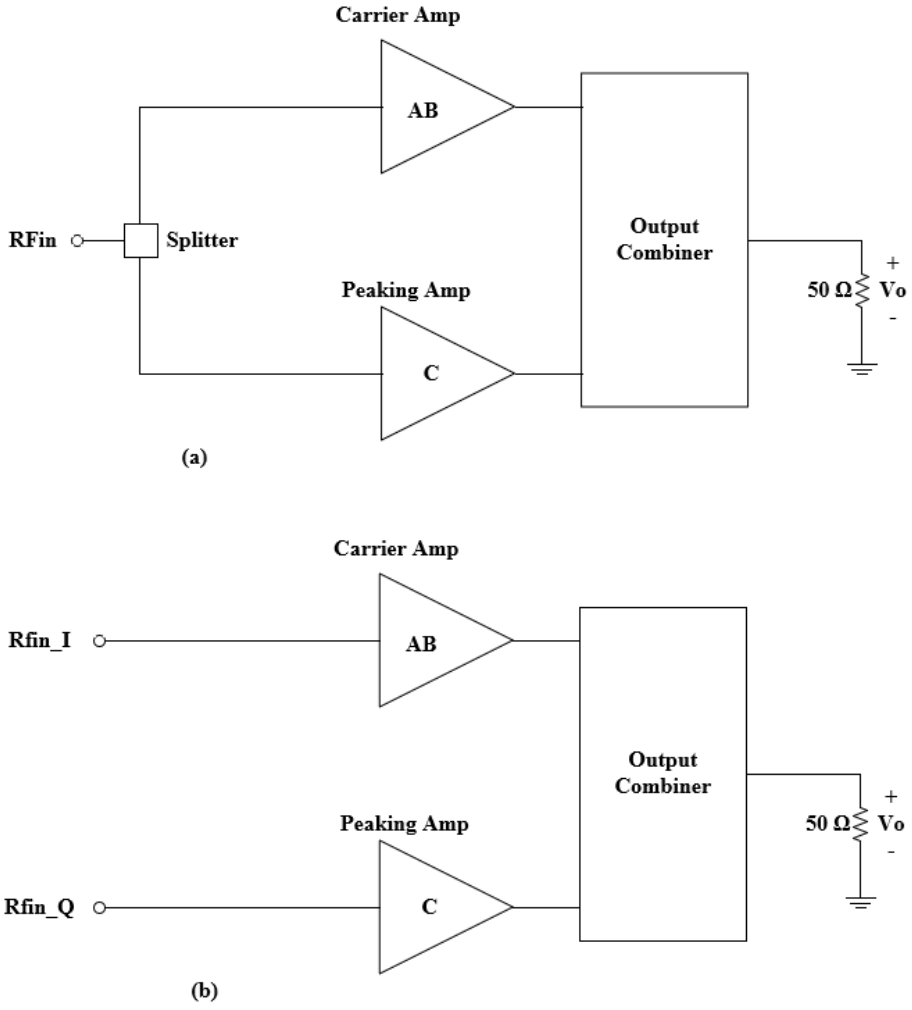


Figure 37 : (a) Conventional Doherty and (b) Digital Doherty

Another problem in the conventional Doherty is the input splitter. Because of this splitter, we always have a 3dB loss in the gain (in symmetric 1:1 Doherty architecture). Also, we don't have much flexibility to split the current as per requirement to achieve best Doherty performance over wide bandwidth. To overcome these challenges in conventional Doherty (also known as Analog Doherty), a new technique has been proposed called as Digital Doherty to improve performance over the conventional Doherty. Figure 37 (a) which shows a conventional Doherty and Figure 37 (b) shows the general architecture for the Digital Doherty. From Figure 37 (b), both carrier and peaking are controlled individually. The biggest benefit is that we can change the amplitude and phase of peaking amplifier dynamically when we operate the same DPA over different frequency to achieve maximum performance. By removing the input splitter, we can get increase in gain as well. But the main drawback is that we need an external hardware to get individual control for the I and Q channels which control the main and the peaking path.

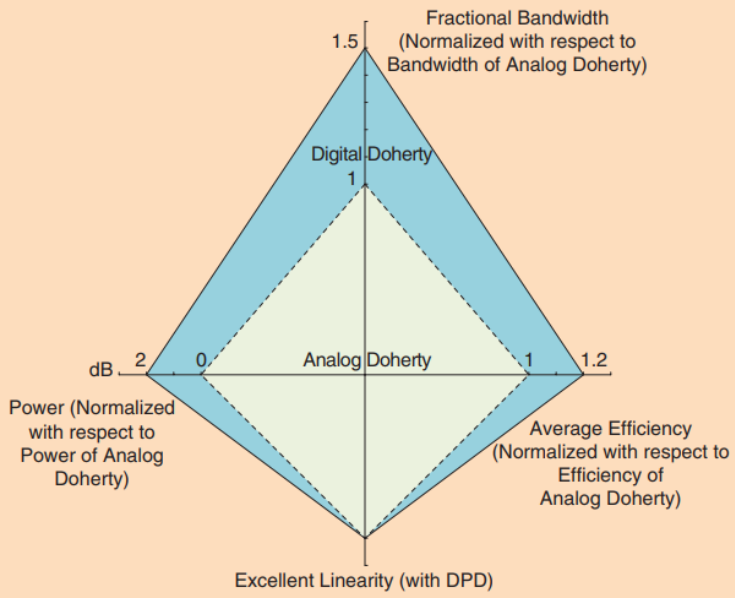


Figure 38: Improvements in RF performance in Digital Doherty as compared to Conventional (Analog) Doherty [25]

2.7.3 Parallel Doherty

This is a different architecture compared to the conventional Doherty. In this, we remove the output matching network from the combining node and directly connects the load at the combining node. Also, we need to put an extra λ/4 line in the peaking path for correct load modulation. The load-modulation transformation ratio will not change at back-off and peak power level. So, the operation of Parallel Doherty [26] is same as that of conventional Doherty. But it is more useful for the back-off power level as it gives wider bandwidth in back-off region rather than peak power level. Since a RF Power amplifier mostly operates in back-off region, so Parallel Doherty is a better choice.

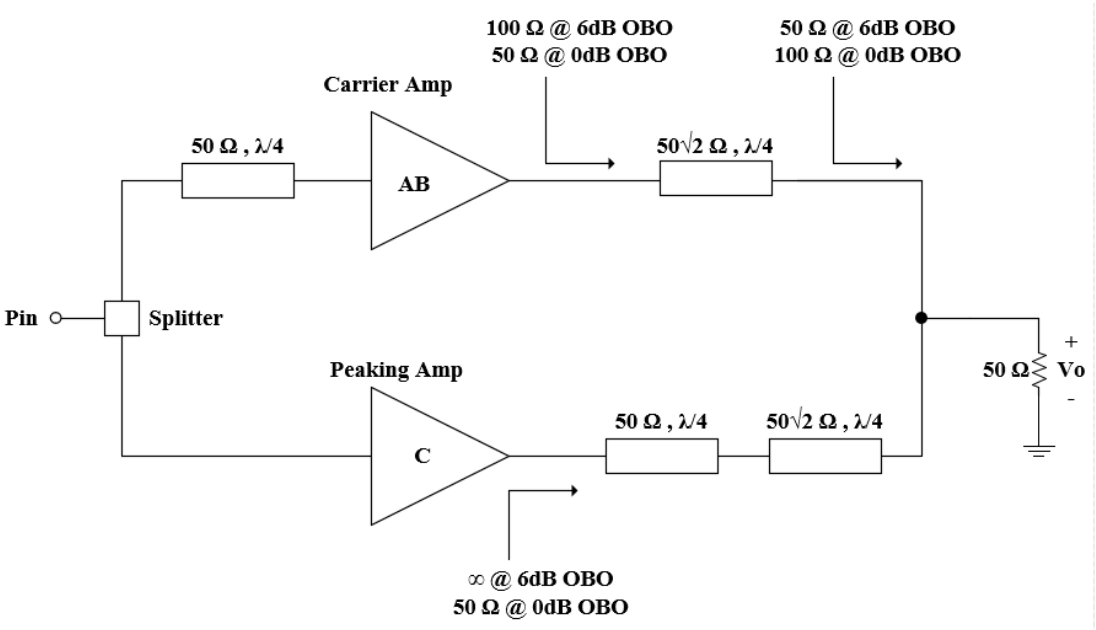


Figure 39 : A generalized symmetric Parallel-Doherty Power Amplifier Architecture

As can be seen from Figure 39 above, a Parallel Doherty architecture is simpler than the conventional Doherty arrangement. This is because there is no output matching network from the combiner node to the output load. The main advantage of the Parallel Doherty is that the impedance transformation ratio for the back-off powers is less as

compared to conventional Doherty which gives more bandwidth enhancement advantage to the Parallel Doherty. As mostly the PA operates in the back-off power levels, having a wider bandwidth is always an advantage.

In conventional symmetric Doherty at the 6 dB back-off level, the peaking amplifier is off and only the main is conducting. Due to this the impedance seen at the combiner node is Ropt/2.

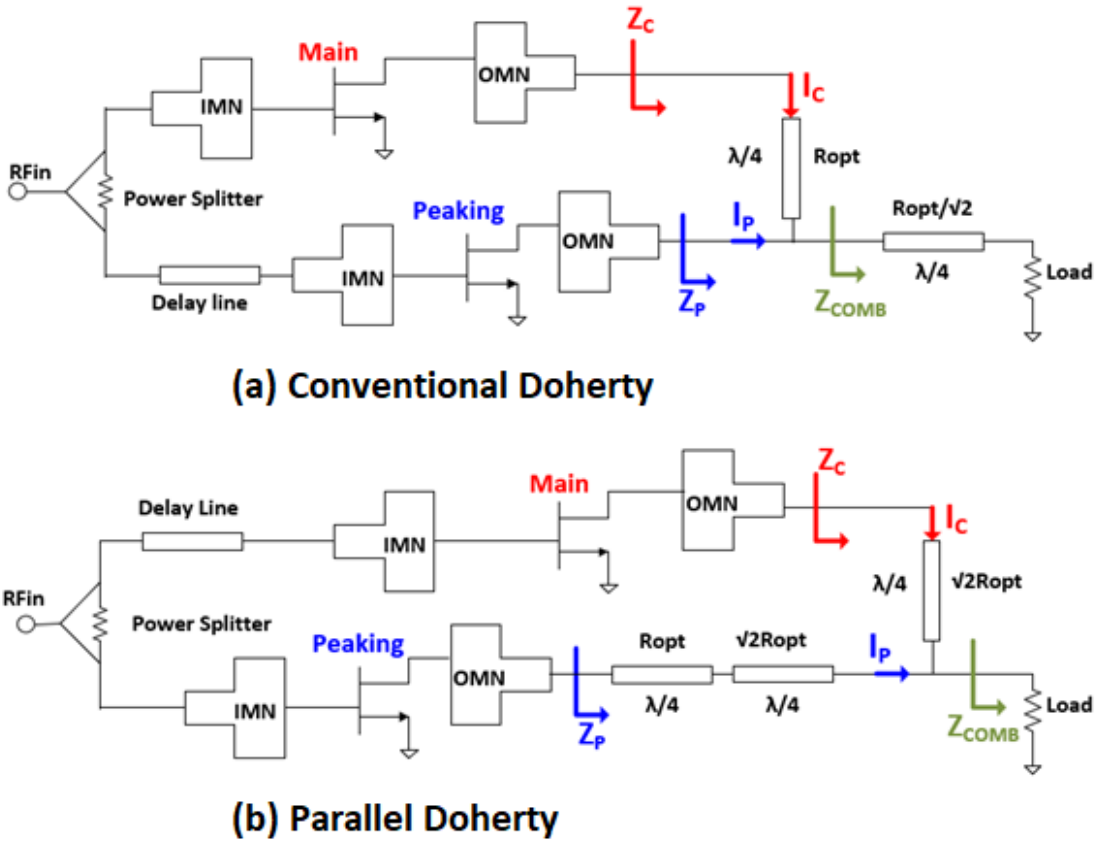


Figure 40: Comparison of Conventional Doherty vs Parallel Doherty architecture

The λ/4 transformer at the output of main, transforms Ropt/2 to 2*Ropt. This makes the transformation ratio to 4:1. Since, high transformation ratio leads to high quality factor, this leads to narrower bandwidth from the Bode-Fanno criteria [27]. But if we compare this back-off transformation in Parallel Doherty, the quality factor is less which leads to wider

bandwidth for back-off power levels. The combiner impedance at the back-off power level in Parallel Doherty is Ropt. The λ/4 transformer at the output of main, transforms Ropt to 2*Ropt. This makes the transformation ratio to 2:1. So, a low transformation ratio leads to a low quality factor which leads to wider bandwidth. This makes Parallel Doherty a better choice for back-off power operations as compared to other Doherty architectures.

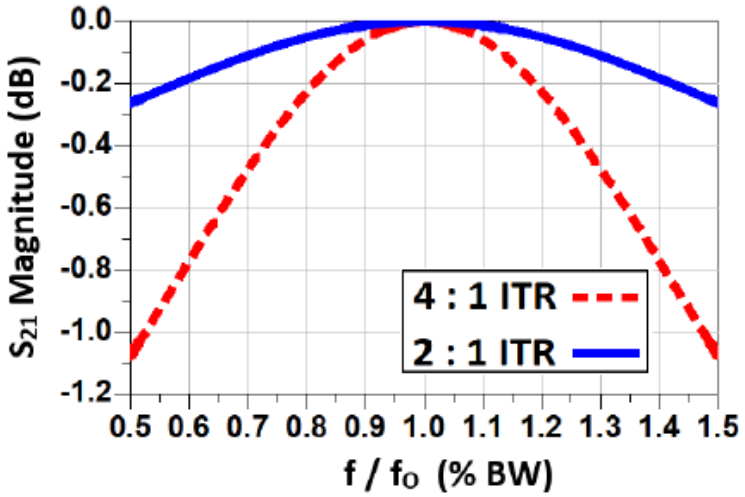


Figure 41: Gain versus fractional bandwidth with respect to ITR

From Figure 41 shown above, we can see the S_{21} response versus the fractional bandwidth for 4:1 and 2:1 impedance transformation ratio. It can be seen clearly that lower Impedance transformation ratio leads to wider bandwidth. Hence, Parallel Doherty is a better choice as compared to the conventional Doherty for the back-off power levels. Although the Parallel Doherty promises some advantages, it comes with associated tradeoffs. Firstly, since there is an additional λ/4 transformer in the peaking path which increases the area of the board. This increases the physical form factor as compared to the conventional DPA. Secondly, although Parallel Doherty reduces the impedance transformation ratio at back-off from 4:1 to 2:1, but the ITR increases to 2:1 as compared

to conventional 1:1 ITR at peak power level. This would imply lower BW for Parallel DPA at peak power level and its implication is the headroom as P3dB is now difficult to maintain across frequencies which could impact DPA linearization. Thirdly, as compared to conventional DPA, the linearity is poor for the Parallel DPA. So, there are associated tradeoffs with each topology.

In the back-off mode, the impedance seen by the main (carrier) and the peaking can be given as (assuming a symmetric Parallel DPA case for 6dB back-off)

$Z_C = (\sqrt{2}\ RL)^2 / RL$ $\quad V_{in} = V_{MAX/2}$
$= 2*RL$

$Z_P = \infty$ $\quad V_{in} = V_{MAX/2}$

For the peak power level, the impedance seen by the main (carrier) and the peaking can be given as (assuming a symmetric Parallel DPA case for 6dB back-off)

$Z_C = (\sqrt{2}\ RL)^2 / (2*RL)$ $\quad V_{in} = V_{MAX}$
$= RL$

$Z_P = RL^2 / (\sqrt{2}\ RL)^2 / (2*RL)$ $\quad V_{in} = V_{MAX}$
$= RL$

As we can see from the equations above, at back-off the impedance presented to main is $2*R_{opt}$ and impedance presented to peaking is ∞. At the peak power level, the impedance presented to both main and peaking is R_{opt}. So, the impedance transformation at back-off and at peaking is same as that of conventional DPA. The only difference is the reduced transformation ratio which leads to wider bandwidth.

CHAPTER 3

DPA DESIGN AND IMPLEMENTATION

3.1 Design of Doherty PA

The design of a Doherty Power amplifier is itself a challenge as we need to take care of multiple parameters while designing. Firstly, an input power splitter was designed. After that the input and output matching networks of the main and peaking amplifier were designed. It was followed by the design of power combiner where the powers from main and peaking amplifiers combine and then finally an output load connected to the combining node. The complete procedure is explained below step by step to design the Doherty power amplifier and key parameters to take care while designing it.

3.2 Main aspects of Doherty PA design

This section describes the process for designing the Doherty PA and the respective simulations to run. We used Cree's bare die CGH60008D (8W) [28] large signal device model to perform all the simulations in Agilent's Advanced Design system (ADS) 2017 and ADS Momentum was used to run EM simulations. Substrate properties such as height (20 mil), loss tangent (0.0035) and relative dielectric constant (3.66) were used in the simulations with Rogers 4350 material. The impedance matching, impedance inverter, harmonic terminations were designed using the micro-strip line material. To determine the performance of the CGH60008D large signal model the gain, drain efficiency and output power were characterized with the simulation and measurement setup. The measurement setup was fully calibrated to accurately determine the large signal performance of the transistor. We can expect some difference from simulation to the measured results due to

the fact there can be some coupling effects, parasitic effects of lumped components, SMA connectors and lead cables etc. Therefore, tuning inductors were also added in the gate and the drain path to tune the performance of Doherty PA on board.

3.2.1 DC I-V characteristics of the Transistor

Generally, in most of the Doherty amplifiers, we use two transistors which are biased in class-AB and other in class-C. So, it is important to plot the DC I-V characteristics to calculate the Ropt value and DC biasing point of the devices. Figure 42 shows the testbench used for running the DC bias for the used PA device.

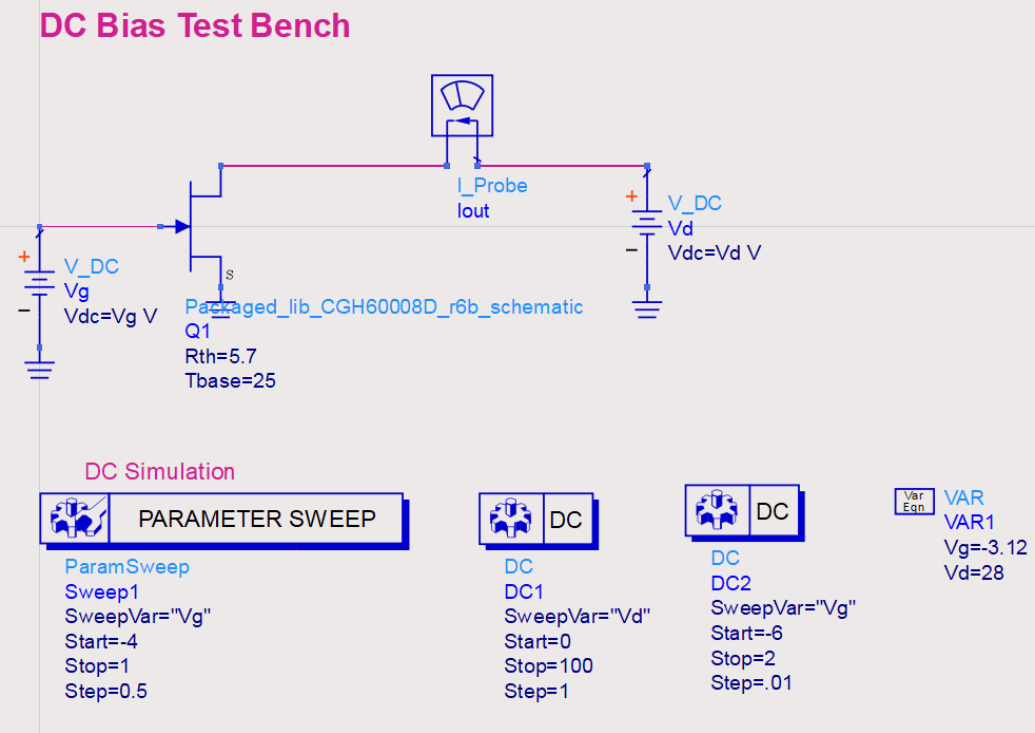


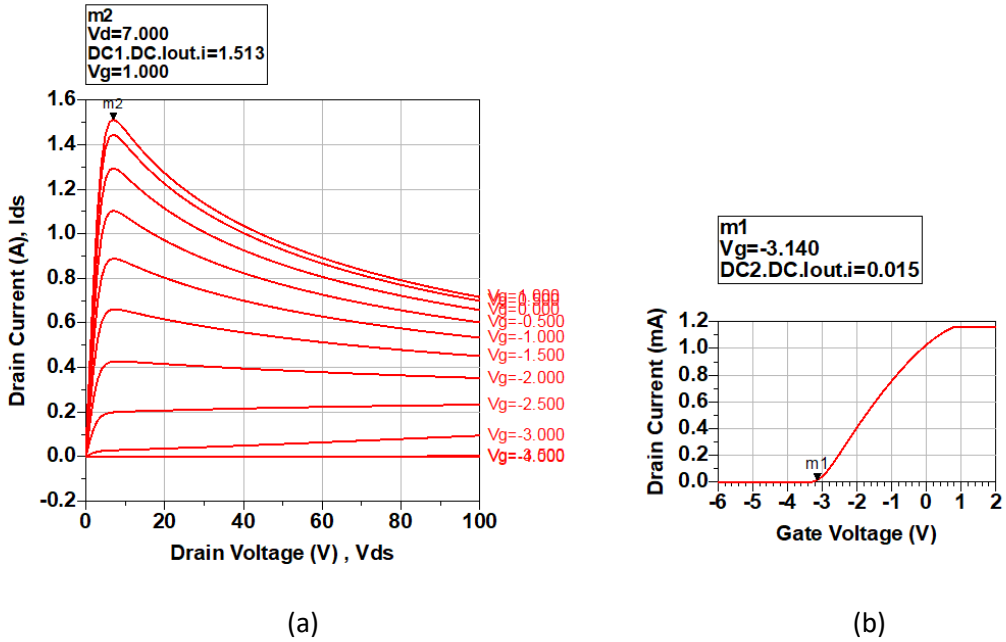
Figure 42 : Testbench for DC I-V characteristics for CGH60008D device

From Figure 43(a) we can calculate the Ropt and from Figure 43(b), we can select the bias point for class-AB and class-C depending upon the dc bias current requirement. Since, the value of I_{MAX} = 1.513A ,V_{DD}=28V, V_{KNEE}=7V

So, Ropt = 2*(V_{DD}-V_{KNEE}) / I_{MAX}

Ropt = 2*(28-7) / 1.513

Ropt = 27.76 Ω



(a) (b)

Figure 43: I-V graphs for calculating Ropt and Bias point

3.2.2 Load Pull and Source Pull

The Load pull and Source pull is an important step in the design of a power amplifier. Since the PA device is highly nonlinear and especially at higher power levels, it is important to present the correct impedances to the load and source of the device to meet the desired objective like efficiency, power, linearity, gain etc. So, this technique is known as impedance pulling and it is referred to as load-pull and source-pull at the device output and input respectively. In this process we sweep the fundamental and harmonic impedances of the output and input at the devices packaged plane multiple times till we reach to a point where we get the desired performance. Apart from sweep of the fundamental impedances,

we also need to sweep the 2nd and 3rd harmonic values of impedances as in the GaN devices as the impact of harmonics (especially 2nd) [29] is significant on efficiency and output power. Also, we need to specify which input power level, frequency and bias level of the device we need to measure the performance. Figure 44 below shows a general testbench setup used for load and source pull in the lab.

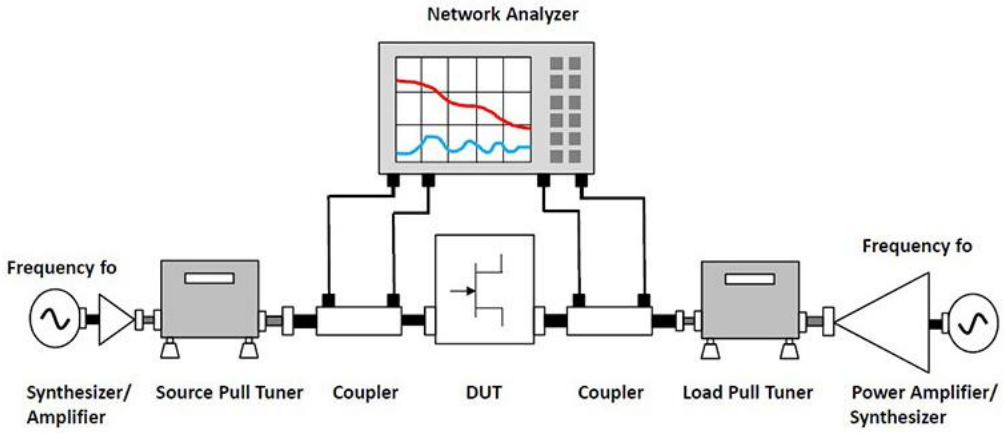


Figure 44 : A general Load pull and Source pull setup

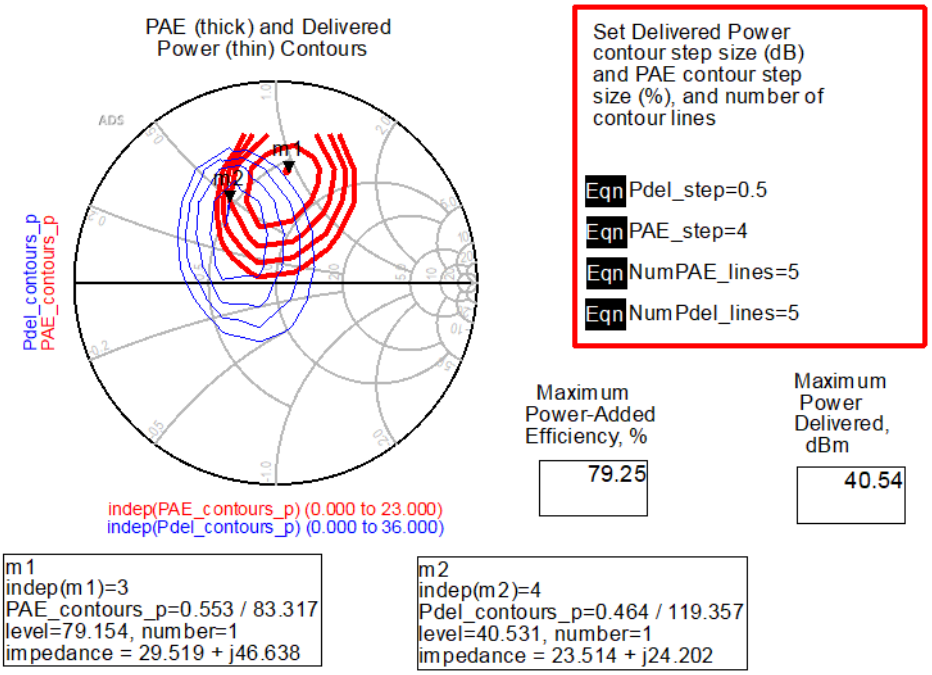


Figure 45: Efficiency and Output Power contours for GaN device used

3.2.3 Stability

The RF Power amplifier devices are usually unstable especially at low frequencies and we need to ensure the device is unconditionally stable. Usually we add a parallel RC circuit at the gate of transistor. The resistor is basically added to reduce the gain at lower frequencies and make the device stable. To verify the stability, we need perform the K-|Δ| test. Apart from K and |Δ|, we have an additional criterion for the stability which is mu_factor and mu_prime_factor. For the device to be unconditionally stable, the K > 1 , |Δ| < 1 where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$$

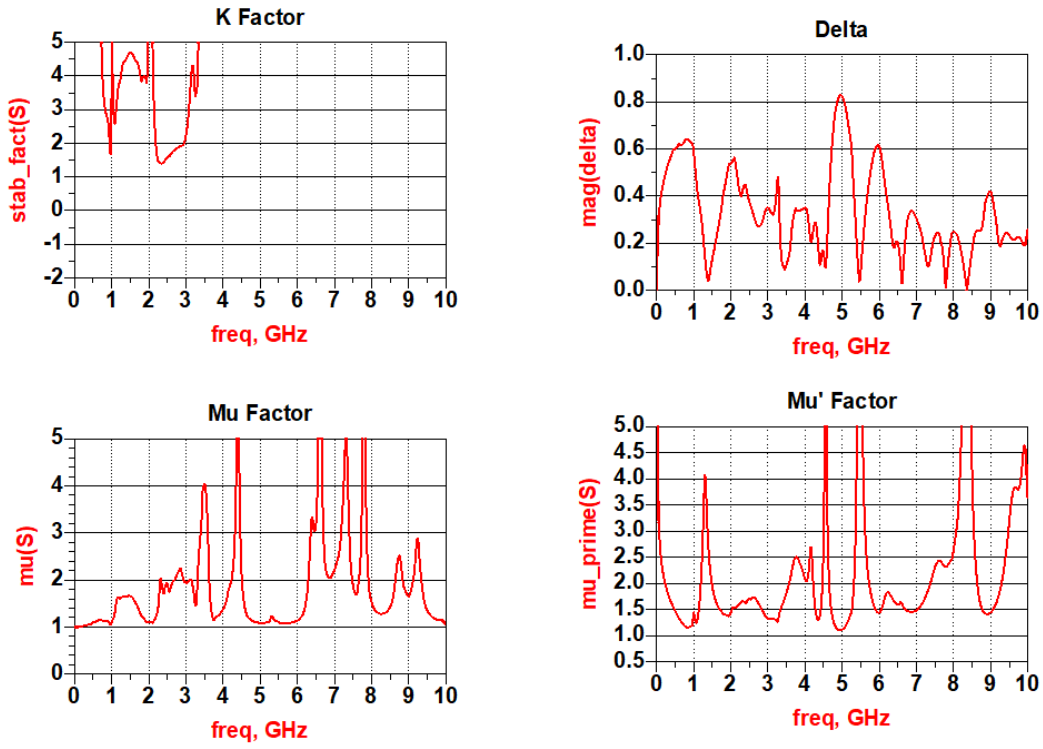
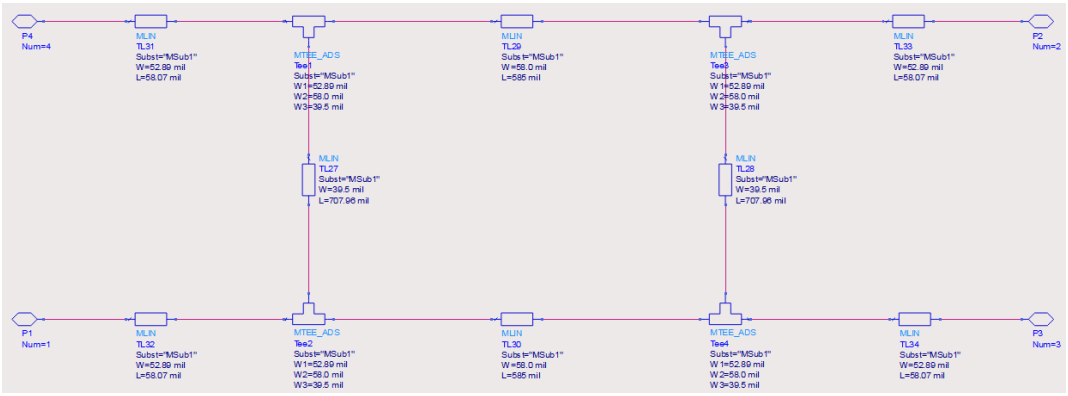


Figure 46: K - |Δ| stability results for the Parallel Doherty Power Amplifier

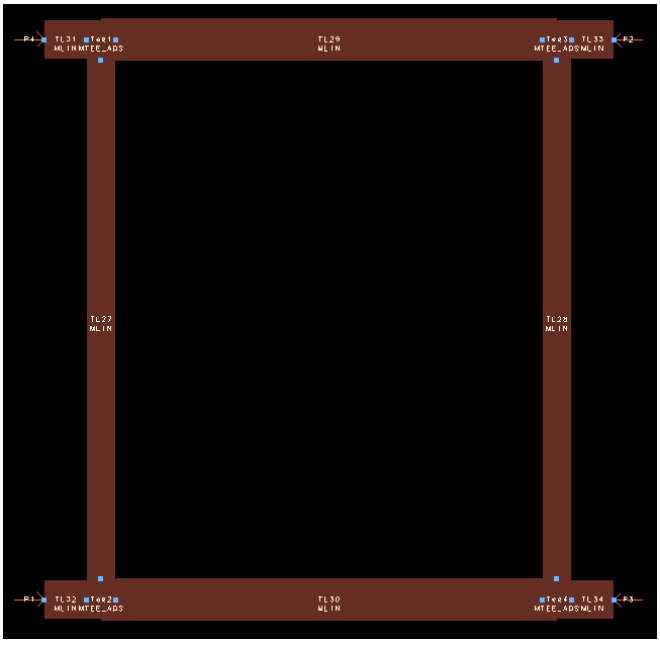
From Figure 46 shown above, we can say that the Doherty PA is unconditionally stable as we can see that K>1, |Δ| < 1, mu_factor>1 and mu_prime_factor>1.

3.2.4 Input Power Splitter

In this Thesis, a 3-dB 90° hybrid coupler was used at the input to split the input power signal into two paths (main and peaking) along with maintaining 90° phase shift.



(a)



(b)

Figure 47: (a) Schematic (b) Layout of the Splitter

3.3 Schematic and Layout of Design

Once the schematic level design of the Parallel DPA was ready and tested for performance, the layout of schematic was completed using ADS momentum and extensive EM simulations were run using the Microwave Momentum option. There was some tuning required once we imported the schematic into layout and ran EM sims. The schematic of the Parallel DPA and the stack-up used for running EM simulations is shown below.

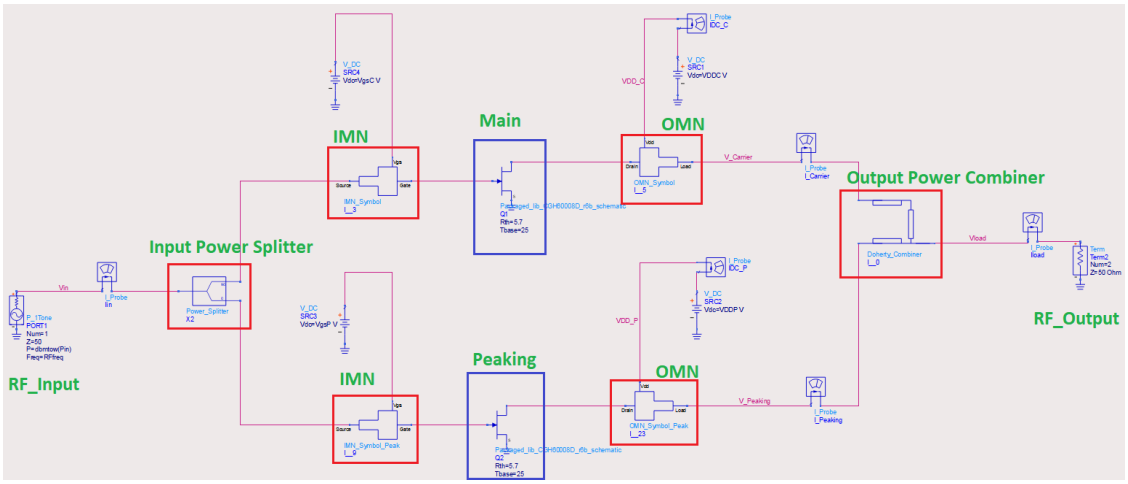
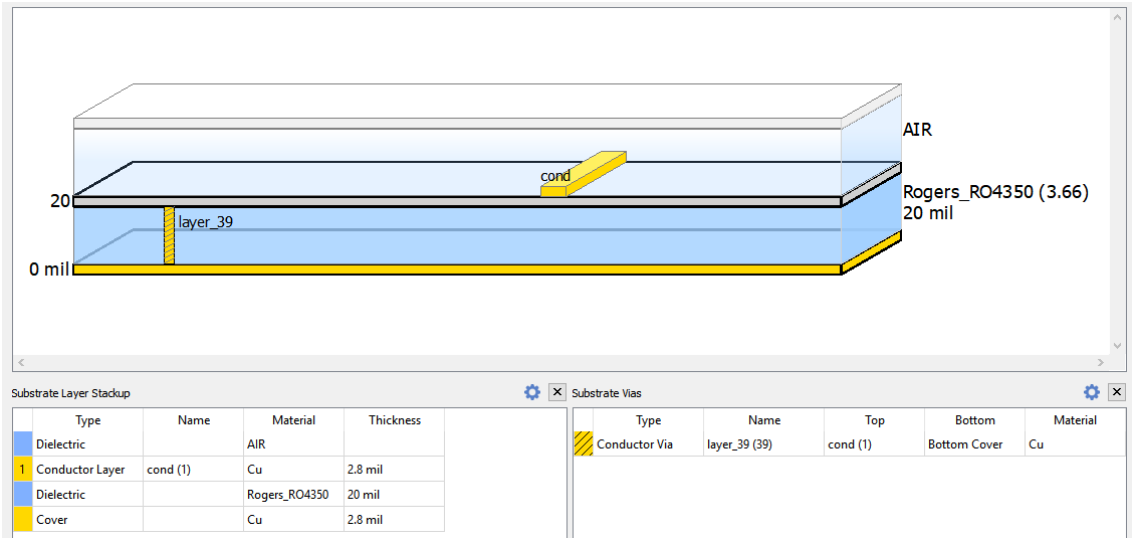


Figure 48 : Schematic of the Parallel DPA



Type	Name	Material	Thickness
Dielectric		AIR	
1 Conductor Layer	cond (1)	Cu	2.8 mil
Dielectric		Rogers_RO4350	20 mil
Cover		Cu	2.8 mil

Type	Name	Top	Bottom	Material
Conductor Via	layer_39 (39)	cond (1)	Bottom Cover	Cu

Figure 49 : Stack-up of material

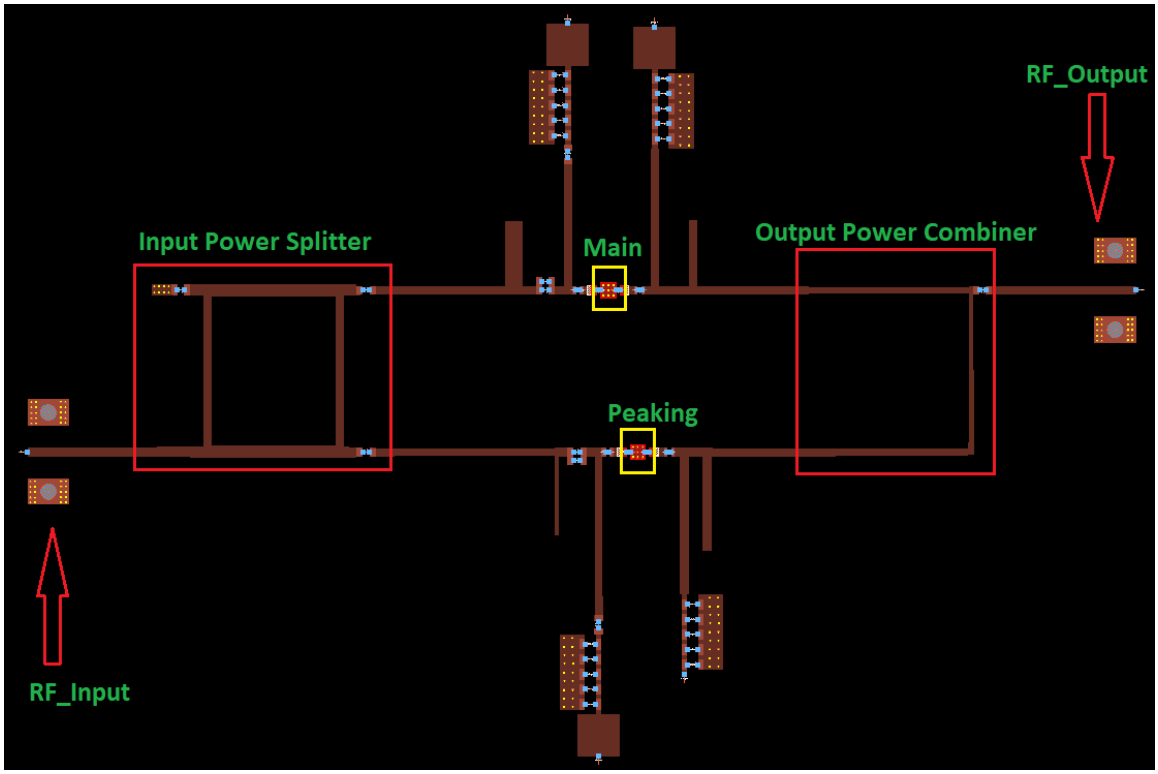


Figure 50 : Layout of the Parallel DPA

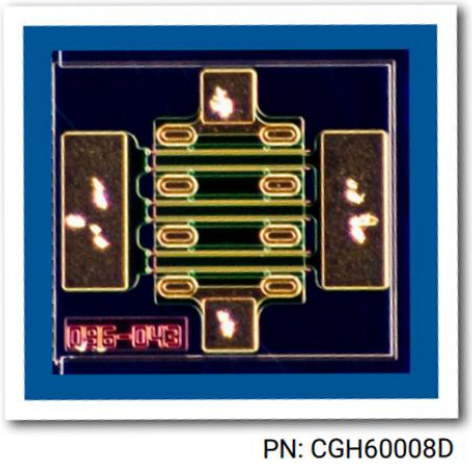


Figure 51 : Actual die of the Cree's CGH60008D device

CHAPTER 4

SCHEMATIC AND EM SIMULATION RESULTS

4.1 EM Simulation Results

The EM sims were run on the layout as shown in Figure 50. The simulations were run from 1 Hz to 20 GHz in steps of 60 MHz to account for the harmonic frequencies as well. The simulations were run on the em_model and using the actual ADS models for the smd components. It was observed that the Parallel DPA designed was operational for a fractional bandwidth of 250 MHz. The output power was close to 42 dBm across the band of frequency from 2.45 – 2.70 GHz. The maximum efficiency achieved varies from 74 -71 % and the back-off efficiency at 8 dB output power back-off was reported 51 - 49 %. Also, the gain of the parallel DPA designed varies from 12 - 10 dB which is a good number for the WiMAX band of operation. This certainly proves Parallel DPA is a promising technique for the existing and future wireless communication applications.

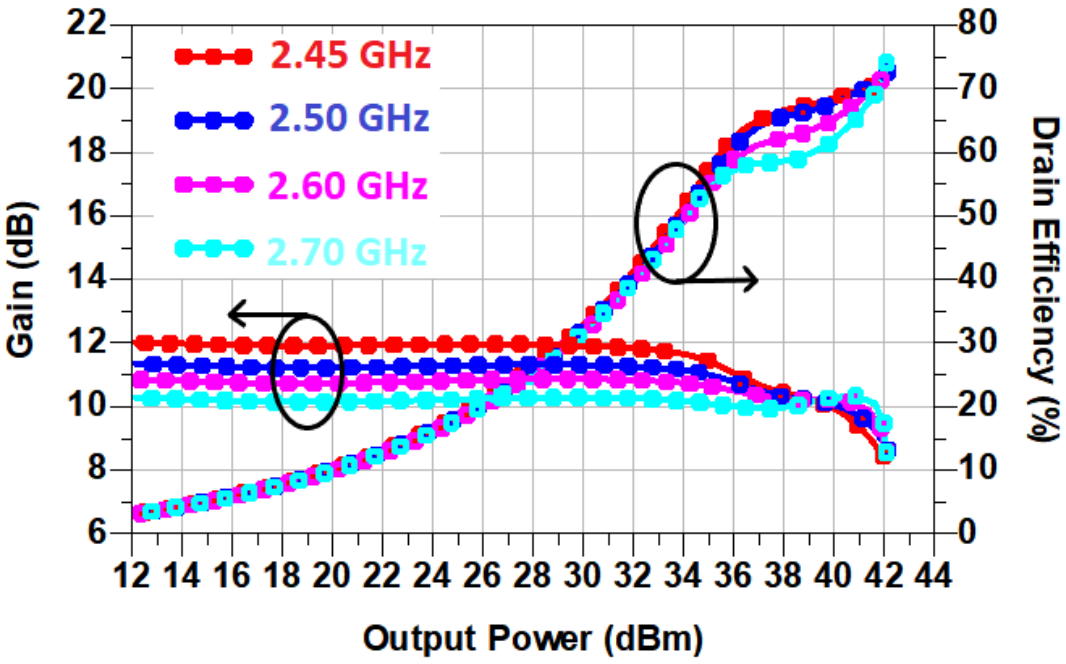


Figure 52 : Gain and Drain Efficiency vs Output Power

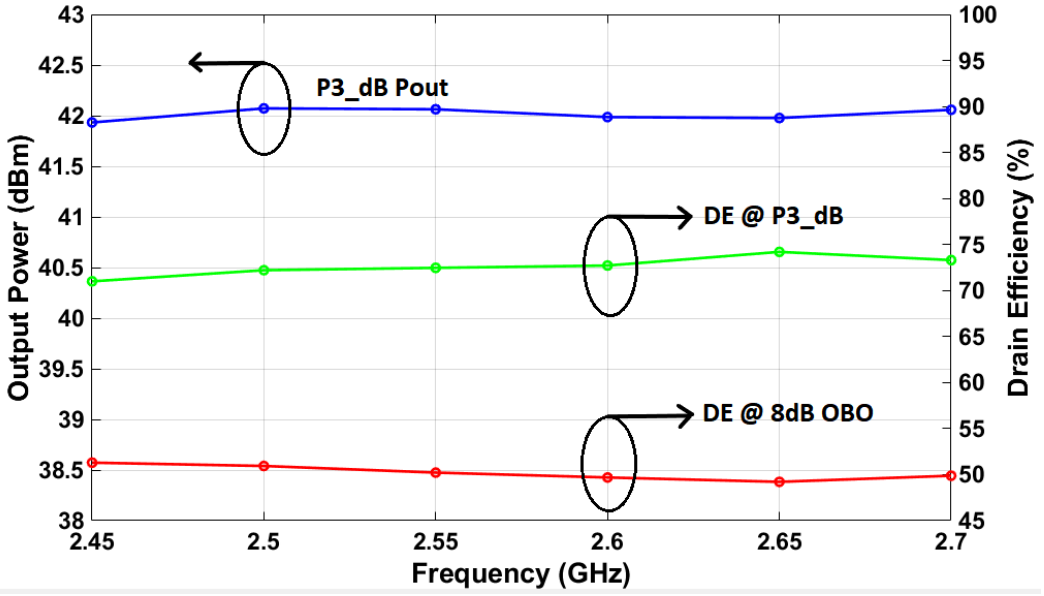


Figure 53 : P3_dB Pout, Drain Efficiency at Peak and 8 dB Output Back-off

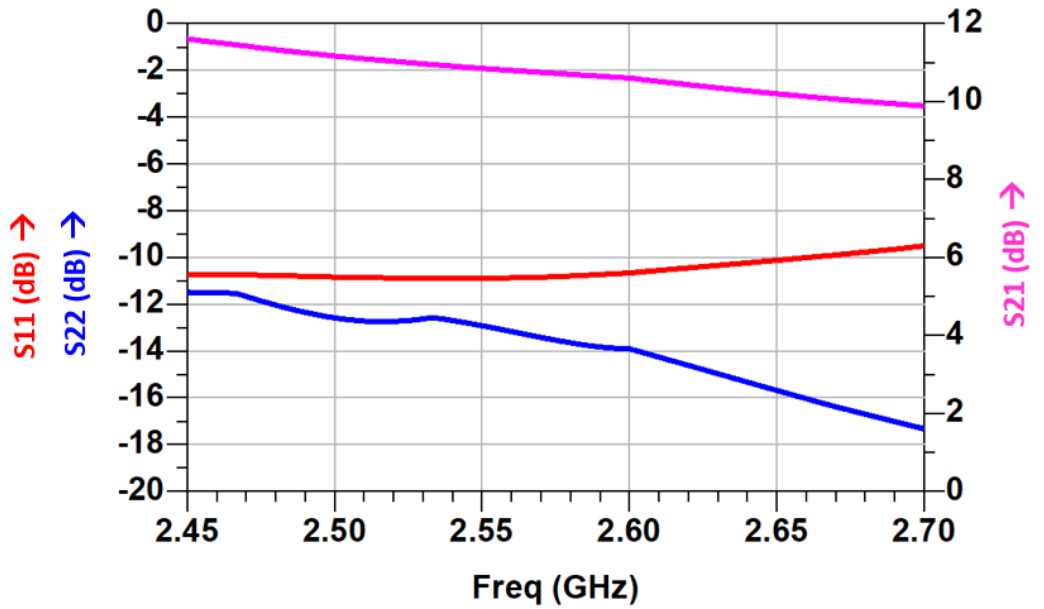


Figure 54 : Small signal parameters : S11 , S22 and S21 over Frequency

From Figure 54, we can analyze the small signal parameters for the Parallel DPA designed. As far as input and output matching is concerned, we can observe that the input (S11) and output (S22) return loss is almost less than -10 dB over the band of frequency for the designed DPA. Also, the small signal transmission gain S21 varies from 12-10 dB which directly correlates with the large signal gain of the designed DPA.

4.2 Comparison of Results

The EM simulation results for the Parallel Doherty shown above makes it an excellent choice for the medium power base-station for the WiMAX. It can be clearly seen that it is better than conventional Doherty PA. A comparison table is also added to compare the performance of the designed Parallel DPA with the other state of art DPA (which uses the conventional quarter-wave transformer). For a fair comparison of the results, all the devices chosen are of the same technology and almost same output power level.

Reference	Process	Frequency (GHz)	Saturated Output Power (dBm)	Peak DE (%)	DE @ OBO (%)	Gain (dB)
[30]	GaN	1.96 / 3.5	42.8 / 41.8	59.5 / 49.6	39.2 / 29.1 (6.7 dB OBO)	9.8 / 9
[31]	GaN	1.95–2.25	42.0	68 – 65	50 - 48 (6 dB OBO)	9
[32]	GaN	0.85 / 2.33	42.5 / 44.0	62 / 55	48 / 38 (6 dB OBO)	19 / 13
[33]*	GaN	2.3–2.825	41.8 – 40.6	69 – 58	53 – 40 (6 dB OBO)	8.8
This work**	**GaN**	**2.45–2.70**	**42.07–41.93**	**74 – 71**	**51 – 49 (8 dB OBO)**	**12 - 10**

*version-1
**EM results

Table 2 : Comparison of the results for Parallel DPA with other state of art DPAs

As we can see from table above, the work done in this thesis reports a high bandwidth using the λ/4 output transformation. Also, the efficiency numbers reported are higher at peak and especially at back-off as compared to the other state of art DPAs. The output power achieved was also around the maximum value which is another advantage. The linearity numbers were not shown in the comparison data due the fact that other DPAs used digital pre-distortion (DPD) and met the spectrum linearity requirements.

CHAPTER 5

BOARD DESIGN AND MEASUREMENT RESULTS

5.1 Board Design & Measurement

The layout of the Parallel DPA was completed and followed by EM simulations. The designed DPA was fine-tuned after running extensive EM simulations to achieve the desired performance. Once the EM sims were completed and showed the performance in accordance to the requirement, the board was made. The board typically takes around two weeks for the manufacturing and assembly of smd components. Due to the deadline for the Master's Thesis defense in the first week of November and submission of Thesis report to the grad college, only the EM simulations were presented in this Thesis report. So, unfortunately there were no measurement results available for the Parallel Doherty PA design presented in this Thesis. But the board measurement will be completed in future which was counted as a future scope of work.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

The Parallel Doherty power amplifier designed in this thesis demonstrated the feasibility of high efficiency at the back-off power levels as well as at the peak power level. But the great benefit that we can get from Parallel Doherty design is the bandwidth because of the fact the impedance transformation ratio is less in the back-off as explained in Chapter-2. Also, the output power levels achieved were good as we were getting almost the maximum available power across the band of frequency of operation. The linearity of the Parallel DPA was not that great to satisfy the spectrum of LTE or WCDMA etc. but Digital Pre-distortion (DPD) linearization will be used to meet the linearity requirements. The results when compared to previous works done for similar power levels and similar technology, this design gives an advantage over the other state of art work done previously. So, in nutshell Parallel Doherty promises a better performance in terms of bandwidth, efficiency (at back-off and peak power levels), output power and reasonable linearity.

6.2 Future Work

As the author of this Thesis will continue for Ph.D. within the same university under same advisor, so first the measurement results of the board will be taken. Secondly, the concept of Parallel Doherty will be explored in much detail from the theoretical perspective as well. Currently only the practical implementation was realized. Thirdly, although the Parallel Doherty amplifier gives better performance than conventional Doherty in terms of bandwidth but still more options will be explored to make the peaking amplifier off during

the low power levels to achieve wider bandwidth for high back-off power levels. With the current standards of wireless communication such as 4G LTE and recently introduced 5G, the PAPR levels will go on till 10dB. So, there is still lot of scope to improve the efficiency in the back-off region while maintaining the peak efficiency. Therefore, asymmetric Parallel Doherty is another option to explore. Since the linearity of Parallel Doherty was not good as compared to conventional Doherty. So, emphasis will be laid to improve the linearity of Parallel DPA without the use of digital pre-distortion linearization. Also, the same concept of Parallel will be explored to the IC design implementation as well.

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