High-Efficiency Doherty-Based Power Amplifiers Using GaN Technology For Wireless Infrastructure Applications

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved November 2018 by the
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ARIZONA STATE UNIVERSITY

December 2018

ABSTRACT

The continuing advancement of modulation standards with newer generations of cellular technology, promises ever increasing data rate and bandwidth efficiency. However, these modulation schemes present high peak to average power ratio (PAPR) even after applying crest factor reduction. Being the most power-hungry component in the radio frequency (RF) transmitter, power amplifiers (PA) for infrastructure applications, need to operate efficiently at the presence of these high PAPR signals while maintaining reasonable linearity performance which could be improved by moderate digital pre-distortion (DPD) techniques. This strict requirement of operating efficiently at average power level while being capable of delivering the peak power, made the load modulated PAs such as Doherty PA, Outphasing PA, various Envelope Tracking PAs, Polar transmitters and most recently the load modulated balanced PA, the prime candidates for such application. However, due to its simpler architecture and ability to deliver RF power efficiently with good linearity performance has made Doherty PA (DPA) the most popular solution and has been deployed almost exclusively for wireless infrastructure application all over the world.

Although DPAs has been very successful at amplifying the high PAPR signals, most recent advancements in cellular technology has opted for higher PAPR based signals at wider bandwidth. This lead to increased research and development work to innovate advanced Doherty architectures which are more efficient at back-off (BO) power levels compared to traditional DPAs. In this dissertation, three such advanced Doherty architectures and/or techniques are proposed to achieve high efficiency at further BO power level compared to traditional architecture using symmetrical devices for carrier and peaking

PAs. Gallium Nitride (GaN) based high-electron-mobility (HEMT) technology has been used to design and fabricate the DPAs to validate the proposed advanced techniques for higher efficiency with good linearity performance at BO power levels.

ACKNOWLEDGMENTS

I would like to express my gratitude to Dr. Jennifer Kitchen for giving me the opportunity to work in her group. Her continuous motivation, guidance and encouragement helped me immensely during my PhD research work. I am also grateful to Dr. Sayfe Kiaei, Dr. James Aberle and Dr. Bertan Bakkaloglu for their suggestions and comments at various stages of the research work. I also would like to express my gratitude towards Joseph Staudinger, whose suggestions, insightful discussions and guidance helped me since the beginning of my research work. I am ever grateful to my colleagues at ASU and at NXP semiconductors, namely Soroush Moallemi, James Krehbiel and Mir Masood for their helps specially during the measurement phase.

Finally, I would like to thank my wife Tahrima for her enormous support and sacrifice during this whole period. I am always in debt to my parents for showing their confidence in me and pushing me towards my goal. I am thankful to my brother for his suggestions and motivations during the times of difficulty to overcome various challenges.

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CHAPTER – I

INTRODUCTION

1.1 Background:

Rapid growth of the wireless communication industry inspired new modulation schemes (e. g. WCDMA, OFDMA) to accommodate more users within a certain bandwidth. These modulation standards promise high data rate with high bandwidth efficiency, which imposes stringent linearity requirement on wireless transceiver designers. Being the final stage in any transmitter architecture, the power amplifier's (PA) linearity is critical to satisfying adjacent channel leakage ratio (ACLR) requirements for the specified modulation standard. Moreover, high peak to average power ratio (PAPR) of these modulation schemes forces the PA to operate at a lower average power level than conventional modulation schemes such as FM. This phenomenon has motivated different PA architectures such as Doherty, Envelope elimination and restoration (EER) and Envelope tracking (ET) to enhance back-off (BO) efficiency of the PA [1]-[4]. However, this improvement of efficiency comes at the cost of linearity, as highly linear PAs typically have low efficiency at BO power levels. Switched-mode PAs such as Class D, Class E and Overdriven PAs like Class F, Class J operate at very high efficiency compared to conventional linear PA classes. But, these PAs require additional processing such as polar architectures, LINC, and complex Digital Pre-Distortion (DPD) system to linearize the PA. Since Doherty PA has the simplest architecture compared to other load modulated PAs and does not require any complex processing or additional element for its operation, it became the most popular solution for wireless infrastructure application all over the world. The

motivation of this research is to investigate and innovate various advanced Doherty PA architectures with wider load modulation to achieve efficiency enhancement at further BO power levels compared to conventional architectures for wireless infrastructure applications. High performance GaN-on-SiC based Doherty Power Amplifiers (DPA) are designed based on the proposed techniques. Finally, The DPAs are fabricated and measured to validate the presented concept. Characterization and computation of the DPA performance has been done with high peak-to-average power ratio (PAPR) based modulated signals.

1.2 Doherty Power Amplifier Fundamentals:

The demands for higher data rate have led to many generations of modulated signals with high PAPR. Such new generations of mobile data have high crest factors exceeding 8.0 dB. Due to this phenomenon, RF PAs operate at power backed-off regions to achieve expected linearity performance.

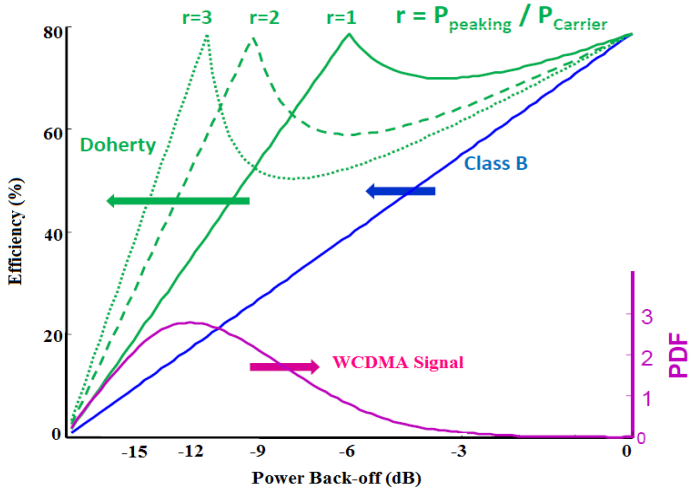
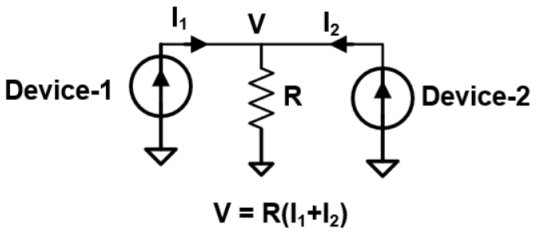


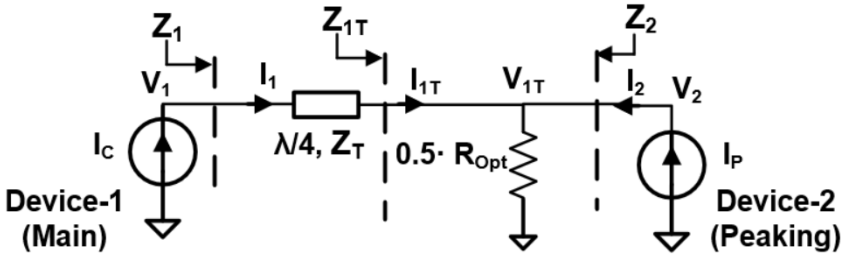
Fig. 1.1: Efficiency comparison of Doherty PA with Class B PA [5].

However, efficiency degrades significantly when most of the linear PAs are operated at backed-off power levels. This necessitates a solution for efficiency enhancement at these backed-off power levels. Advanced architectures like Doherty can improve efficiency at backed-off power levels compared to linear PAs, as shown in Figure 1.1.

A Doherty PA is a combination of two PAs, namely carrier PA and peaking PA. This architecture maintains high efficiency throughout a larger span of power levels by applying the load modulation technique. Before explaining the load modulation phenomenon in a Doherty PA, consider the following generalized example about load modulation. Suppose two devices are connected in parallel [Fig 1.2(a)], namely Device-1 and Device-2. Initially Device-1 is *on* and Device-2 is *off*. Impedance seen from the drain of Device-1, $R_1 = R$. As soon as Device-2 turns *on*, impedance seen from the drain of Device-1, $R_1 = R \cdot (1 + I_2/I_1)$.



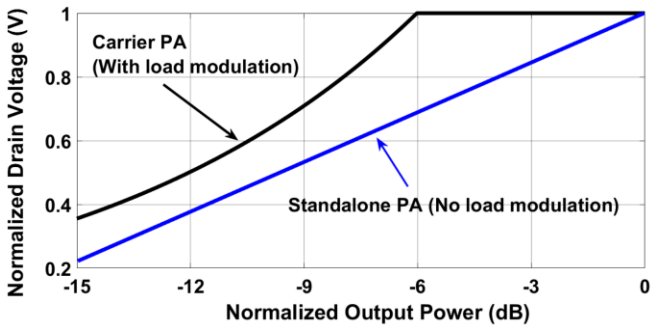
(a)



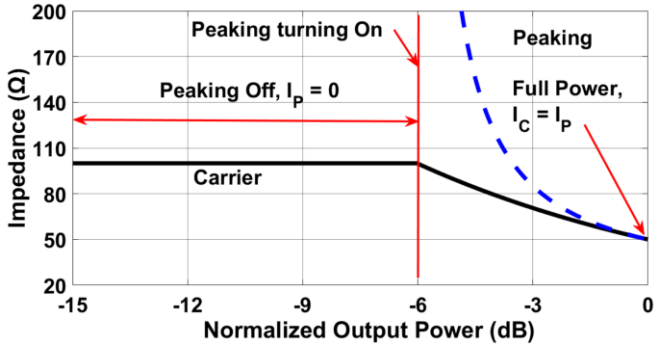
(b)

Fig. 1.2: (a) Diagram illustrating the concept of Load Modulation. (b) Load modulation in Doherty PA.

That means impedance seen from Device-1 will increase as current from Device-2 increases when I_1 is fixed. This phenomenon is called load modulation. Figure 1.2(b) shows an equivalent circuit for a typical Doherty PA. If the characteristic impedance of the quarter-wave impedance transformer is $Z_T = R_{0pt}$, $Z_1 = 2 \cdot R_{0pt}$ when only carrier PA is *on*. As soon as peaking PA turns on, load modulation starts, and the impedance seen from carrier PA starts to move towards R_{0pt} from $2 \cdot R_{0pt.}$ Notice that Z_1 remains at $2 \cdot R_{OPT}$ before peaking PA turns *on*.



(a)



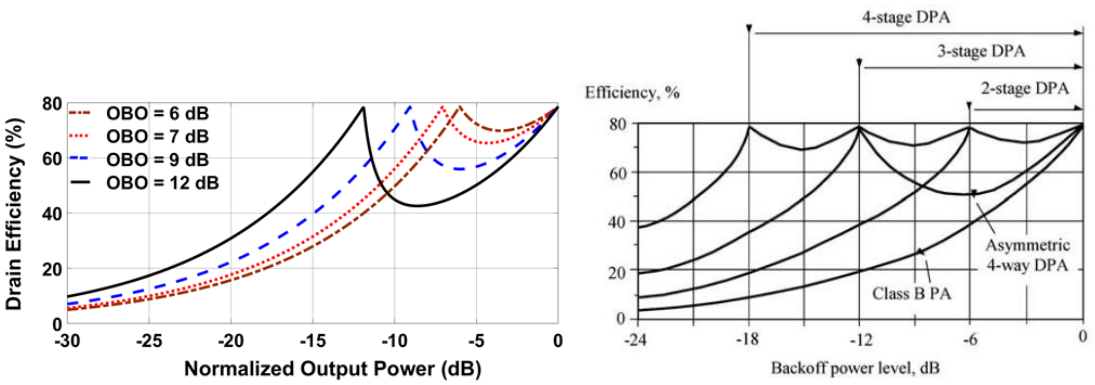
(b)

Fig. 1.3: (a) Comparison between drain voltage of Class B PA in standalone architecture and in a Doherty architecture. (b) Load Modulation in a Doherty PA (when Z_T = 50 ohms).

If the voltage across carrier PA is V_1 and current from main PA is I_1, then $V_1 = I_1.2 \cdot R_{Opt}$, which is twice any standalone linear PA. This means that in a Doherty architecture, voltage excursion across the carrier PA will reach the maximum value at lower power levels than the standalone PA [Figure 1.3(a)]. This early rise to the highest voltage excursion causes the efficiency enhancement of the Doherty PA at BO power level. As peaking PA turns *on*, it decreases the impedance across main PA through load modulation so that the voltage across carrier PA does not reach compression, as current I_1 continues to increase. Figure 1.1 shows the efficiency plot of a typical Doherty PA. It is seen that the efficiency reaches maximum at a certain backed-off power level, then it slowly starts to degrade. This degradation is caused by the peaking PA, because peaking PA just started to turn *on* and far lower from its optimal operational condition. As peaking PA nears the optimal condition, overall Doherty efficiency starts to increase until it reaches at maximum again.

1.3 Alternate Doherty Architectures:

Typically, in a Doherty PA, both the carrier PA and peaking PA have the same device size. This type of Doherty PA is called a symmetrical Doherty PA. However, this ratio between the carrier PA and peaking PA devices may vary. Such architectures are discussed next. An asymmetrical multi-way Doherty architecture [6]-[8] is used to generate peak efficiency at larger than 6 dB output back-off (OBO) power level. It is achieved by connecting a peaking device that is α times larger than the carrier device. The achievable OBO level is related to α by the relation: $20\log_{10}(\alpha + 1)$. That means the BO efficiency peak would be at 6 dB, 9.5 dB and 12 dB OBO when peaking device is equal to, twice and thrice the size of the carrier device respectively.



(a) (b)

Fig. 1.4: (a) Efficiency profile of symmetrical and multi-way asymmetrical Doherty PA. (b) Asymmetrical multi-stage Doherty PA efficiency plot [9].

Figure 1.4(a) shows the generic efficiency profile of symmetrical and multi-way asymmetrical Doherty PAs with respect to the normalized output power. As it is observed from Figure 1.4(a) that, multi-way asymmetrical Doherty PAs have significant efficiency drop between the peak efficiency points, a multistage Doherty architecture has been proposed [10]-[12]. Multi-stage DPAs use multiple peaking devices that turn on at various power levels to provide multiple efficiency peaks at and beyond 6 dB OBO, as shown in Figure 1.4(b). This eventually improves the efficiency significantly between the peak efficiency points. A multistage Doherty requires careful biasing of the individual peaking PAs to get desired efficiency peaks at different back-off power levels. However, multistage Doherty suffers from incomplete load modulation which is caused by fixed offset lines at the output of each stage. This limitation of multistage Doherty asks for alternate solution to improve the efficiency between the peak efficiency points.

1.4 Research Motivation:

Recent generations of cellular communication networks has necessitated radio hardware to support signals with PAPR greater than 6 dB. To process these high PAPR signals and maintain reasonable transmitter efficiency, various advanced Doherty topologies have been used to achieve efficiency enhancement beyond 6 dB OBO, such as multi-way [6]-[8] DPAs, multi-stage DPAs [10]-[12], and dual-input based digital DPAs [13]-[14]. As mentioned in the last section multi-way DPAs use asymmetric carrier and peaking amplifiers, related to differences in die periphery and/or supply voltage. On the other hand, multi-stage DPAs use multiple peaking devices that turn on at various power levels to provide multiple efficiency peaks at and beyond 6 dB OBO. Dual-input digital DPAs use two separate inputs for the carrier and peaking devices and dynamically control the phase and amplitude of the input signal to achieve wider load modulation than conventional symmetrical DPAs. However, these DPAs have disadvantages compared to symmetrical DPAs, including lower gain due to the higher split ratio at the input of DPA, realizability of an uneven power splitter, increased circuit complexity, and/or higher manufacturing cost. Many techniques [15] have been introduced to improve the gain of the asymmetrical DPAs, however these techniques increase circuit complexity and manufacturing variances.

To eliminate the disadvantages associated with multi-way or multi-stage DPAs without compromising the efficiency at the desired OBO power level, there has been new research efforts to achieve wider load modulation (> 6 dB) using symmetrical DPAs. This dissertation presents three advanced symmetrical Doherty architecture that aims to obtain wider load modulation using symmetric carrier and peaking devices.

1.5 Dissertation Outline:

This dissertation is organized as follows,

- Chapter 2: This chapter presents a symmetrical Doherty architecture that uses a varactor network to widen the load modulation beyond 6 dB OBO. To verify the functionality of the architecture, a GaN based symmetrical Doherty PA (DPA) operating from 1.6-2.2 GHz has been fabricated and measured which utilized Macom 90V varactor diodes in the carrier PA's output matching network. This PA demonstrated competitive BO efficiency compared to other varactor-based PAs.
- Chapter 3: This chapter presents a theoretical analysis which illustrates that certain phasing constraints placed at the Doherty combining node can achieve extended load modulation and enhanced efficiency for a symmetrical DPA. This proposed design approach has been validated with measurements on a symmetrical GaN DPA operating at 2.2 GHz which demonstrates competitive BO efficiency with excellent linearity performance compared to prior state of the art symmetrical DPAs.
- Chapter 4: This chapter presents an optimized load trajectory for symmetrical DPA with finite peaking off-state output impedance. Based on theoretical analysis and large signal simulation, it is proposed that the transistor's nonlinear phase distortion could be utilized to enhance the average drain efficiency of the DPA with proper choice of carrier and peaking power amplifier (PA) load trajectories. To validate this design methodology, a GaN based DPA operating

at 2.2 GHz has been designed and fabricated, which exhibits excellent BO efficiency and linearity performance.

- Chapter 5: Finally, this chapter summarizes the research works and recommends future research opportunities.

CHAPTER – II

VARACTOR BASED DOHERTY POWER AMPLIFIER

2.1 Background:

As discussed in the previous chapter, the Doherty PA is the most common amongst the load modulated PA architectures for transmitting high PAPR signals in cellular infrastructure applications. This is primarily due to the simplicity of the Doherty architecture, which does not require any other additional module for enhanced efficiency at the OBO power levels. Typically, an asymmetrical Doherty PA is preferred compared to the symmetrical DPA due to the need for enhanced efficiency beyond 6 dB OBO. But, recently varactor-based PA architecture has been introduced in the literature [16]-[17], which uses varactor diodes at the output of the carrier PA to dynamically modulate the load for enhanced BO efficiency. This chapter will discuss the basic theory of this dynamic load modulated (DLM) PA and will introduce its application in a symmetrical Doherty PA (DPA) to eliminate some of the limitations of asymmetrical DPAs.

2.2 Symmetrical and Asymmetrical DPA Comparison:

In a traditional DPA, the carrier (main) amplifier is typically biased at class-B or deep class-AB and peaking amplifier is biased at class-C. Since the fundamental component of the drain current is smaller in class-C biased PA compared to class-AB, peaking PA needs more input power compared to the carrier PA to deliver required output power at reasonable compression level. This is achieved through uneven analog power split at the input of the DPA. However, this uneven power split causes lower gain of the carrier PA which in-turn affects the overall gain of the DPA. All of these challenges are amplified

when asymmetrical DPA is used to achieve enhanced efficiency beyond 6 dB OBO. In asymmetrical DPA, the peaking PA device is larger in size compared to the carrier PA and this asymmetric ratio increases as efficiency enhancement requirement at OBO increases. Moreover, this asymmetric ratio causes further uneven power split ratio at the input of the DPA which worsens the overall gain degradation of the DPA. Apart from degraded overall gain of the DPA, highly uneven input power splitters are difficult to realize in traditional PCB substrate technology. For higher uneven split ratio, the transmission lines become very thick or thin which raises concerns like allowable impedance tolerance and power handling capacity of the traces. Another significant limitation of asymmetrical DPA compared to symmetrical DPA, is the usage of two different transistors for the carrier and peaking PA which requires separate manufacturing, characterization, testing, packaging and assembly resources that significantly increases the overall product cost of the asymmetrical DPAs. This chapter will discuss varactor based DPAs as one of the PA architectures to achieve enhanced efficiency range similar to asymmetrical DPA with two symmetric devices.

2.3 Varactor Based Load Modulated PA:

Varactor based dynamically load modulated PA is a recently reported architecture [16]-[17] that uses high breakdown voltage-based varactors at the output of the carrier PA. This varactor capacitance is varied with a control voltage as a function of the input signal amplitude to achieve enhanced efficiency at OBO power levels. The theoretical analysis of varactor-based PA is initiated in this section with an ideal transistor characteristic that is shown in Figure 2.1.

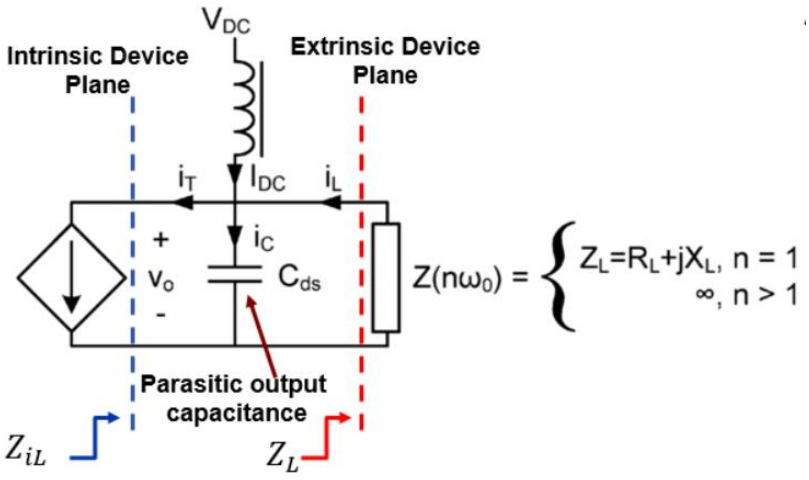


Fig. 2.1: Conceptual Schematic of ideal transistor [16].

This ideal transistor is demarcated at two planes, namely intrinsic and extrinsic device plane. Here i_T is the total current flowing through the device, Vo is the voltage across the device, C_{DS} is the parasitic drain to source capacitance, I_{DC} is the DC current and i_L is the RF current flowing through the load. Following equations are applicable for the ideal transistor at the intrinsic plane:

$$i_T = \begin{cases} \beta I_{max} \sin\theta \,; 0 \leq \theta \leq \pi \\ 0, \ \pi \leq \theta \leq 2\pi \end{cases} \tag{2.1}$$

Here, β is the drive level factor ($0 \leq \beta \leq 1$); I_{max} is transistor saturation current.

$$I_T = \frac{\beta I_{max}}{2} \tag{2.2}$$

I_T is the Fundamental component of i_T.

$$I_{DC} = \frac{\beta I_{max}}{\pi} \tag{2.3}$$

I_{DC} is the DC component of i_T.

$$R_{Opt} = \frac{2.(V_{DC} - V_{knee})}{I_{max}} \tag{2.4}$$

Here, R_{Opt} is the Optimum load for maximum output power and V_{DC} is the drain voltage.

$$Z_{iL} = \frac{Z_L}{j.\omega C_{DS}.Z_L + 1} \tag{2.5}$$

Similarly following equations are applicable for the ideal transistor at the extrinsic plane:

$$I_L = I_T.\frac{Z_{iL}}{Z_L} \tag{2.6}$$

$$Z_L = R_L + j.X_L \tag{2.7}$$

$$i_L = I_1.\sin(\theta + \phi) \tag{2.8}$$

$$I_1 = |I_L|;\phi = \arg(I_L) \tag{2.9}$$

$$i_C = I_{DC} - i_T + i_L \tag{2.10}$$

$$P_{out} = \mathrm{Re}\left(\frac{I_1^2.Z_L}{2}\right) \tag{2.11}$$

$$P_{DC} = V_{DC}.I_{DC} \tag{2.12}$$

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.13}$$

Using equations 2.1-2.13 and varying the load $R+j\cdot X_L$ across the real and imaginary impedance plane, the output power and efficiency contours at the extrinsic plane at 0 dB compression can be derived as shown in Figure 2.2. It can be seen from the figure that efficiency remains fairly constant at back-off power levels when R_L/R_{Opt} is 0.35, 0.46 and 0.68 for X_{CDS}/R_{Opt} of 1,2 and 4 respectively. This high efficiency load conditions for

constant resistive load but variable reactive load paves the way for new load modulated PA architecture.

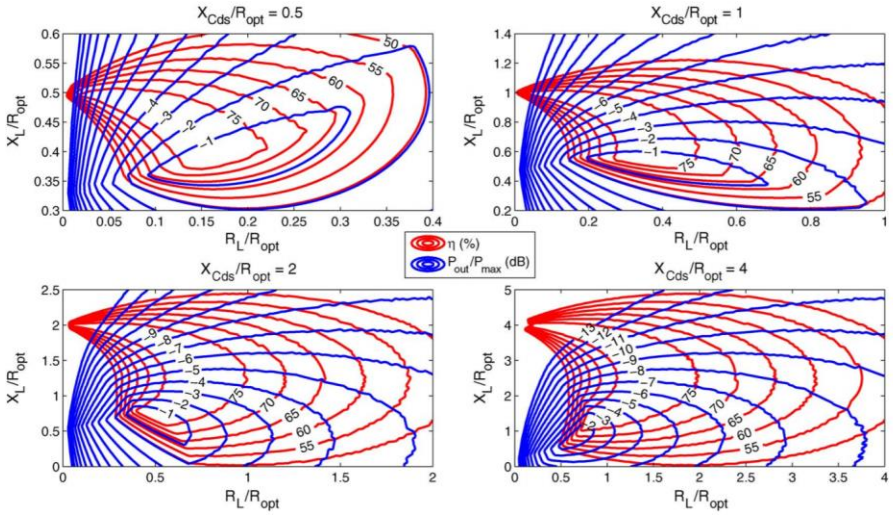


Fig. 2.2: Output Power and Efficiency contours of ideal transistor at 0 dB compression at extrinsic device plane [16].

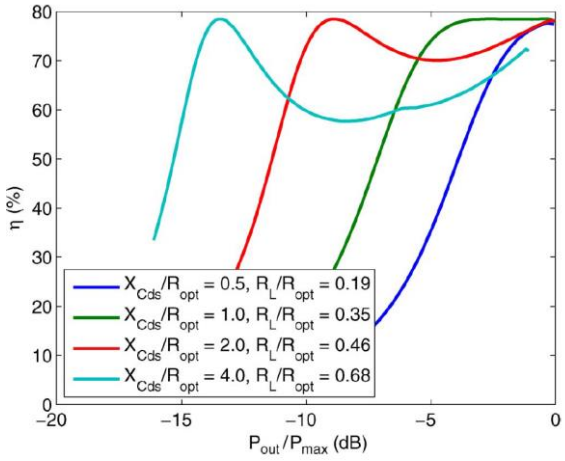


Fig. 2.3: Efficiency vs Normalized Output Power [16].

If the reactive load of the PA can be varied as a function of the input power level with the desired resistive component, then high efficiency could be achieved at higher than

6 dB OBO power levels. Figure 2.3 shows the drain efficiency vs normalized output power plot for an ideal transistor. It is seen that high efficiency can be maintained as far as 12 dB OBO for X_{CDS}/R_{Opt} of 4. Varactor based load modulated PAs take advantage of this characteristics and uses a varactor to modulate the reactive load with the input power drive.

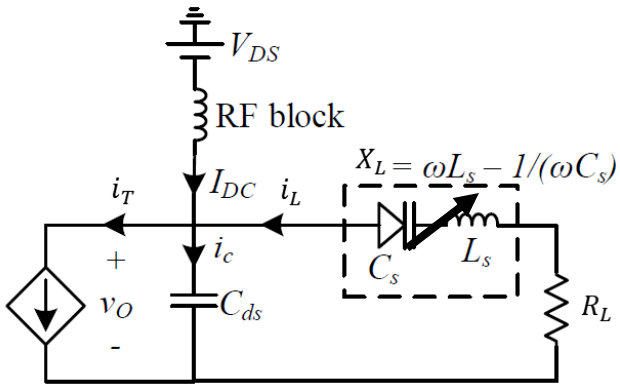


Fig. 2.4: Ideal varactor-based load modulated power amplifier [17].

2.3.1 High Breakdown Voltage Varactors:

As discussed in the previous section, varactor is the key element for this kind of load modulated PAs. For cellular small cell applications these varactors need to have high breakdown voltage due to the high transmit power requirements. Under the RF excitation the voltage across the varactor should not exceed the breakdown voltage neither should disturb the reverse bias condition and become forward bias. If the varactor becomes forward bias, it no longer works as a capacitor rather acts as a diode which has high insertion loss. On the other hand, if the varactor reverse bias voltage exceeds the breakdown voltage then permanent damage occurs which destroys the varactor's ability to modulate the load anymore.

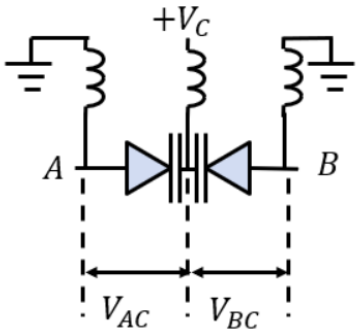
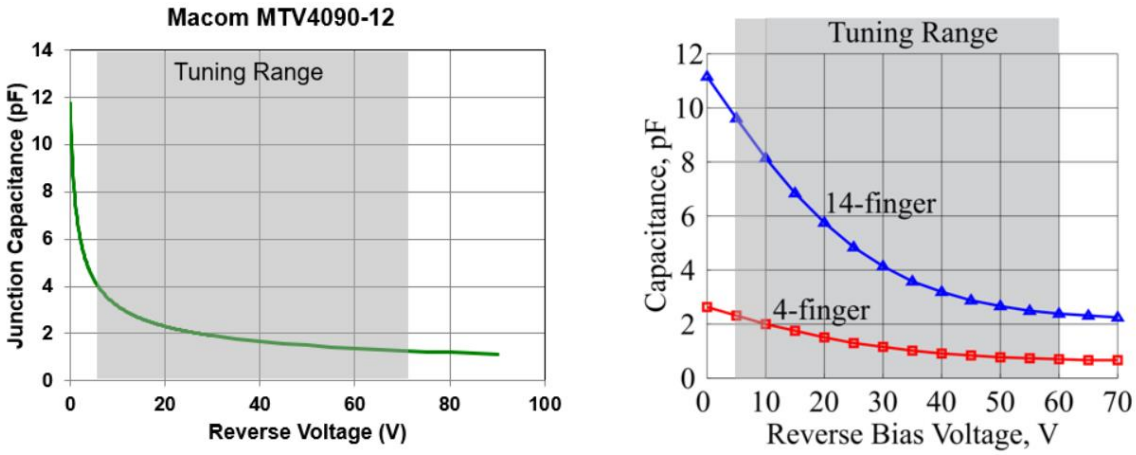


Fig. 2.5: Anti-series varactor biasing.

One of the ways to reduce the voltage across each varactor is to bias two varactors in anti-series connection. This not only reduces the voltage across each varactor by half, it also reduces the distortions generated from the non-linear parasitic elements of the varactors under large signal RF excitation as shown in [18].

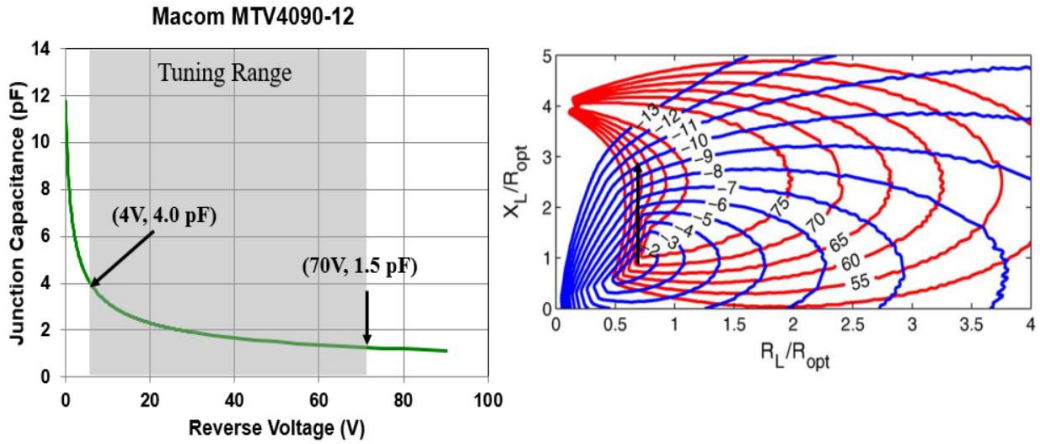
For cellular infrastructure applications, there are two kinds of high breakdown voltage varactors available. These are: abrupt tuning varactor, and non-abrupt tuning varactor diodes. As it can be seen from Figure 2.6 that non-abrupt tuning varactors have much higher tuning range compared to the abrupt ones which makes it more suitable for high power varactor-based load modulated PAs. But unfortunately, these varactors are not commercially available and only found in various research labs for experimental purposes. This unavailability of the non-abrupt tuning varactors causes significant reduction in the tuning range of the load modulated PA, which reduces the efficiency enhancement at the OBO power levels. Figure 2.7 shows that the achievable tuning range with the Macom MTV-4090-12 90 V varactors is 2.67:1. However, tuning range of 3.5:1 is required to achieve efficiency enhancement up to 10 dB OBO for $X_{CDS}/R_{Opt} = 4$.



(a) (b)

Fig. 2.6: (a) Commercially available Si abrupt tuning varactor characteristics [19].

(b) Commercially not available SiC non-abrupt tuning varactor characteristics [20].



(a) (b)

Fig. 2.7: (a) Si abrupt tuning 90 V varactor with tuning range of 2.67:1. (b) Normalized efficiency and output power contours showing required tuning range of 3.5:1 at 10 dB OBO [16].

2.4 Varactor Based Load Modulated Doherty PA:

Varactor based Doherty PA is a newly proposed architecture that combines the concept of Doherty PA with varactor-based PA to extend the efficiency enhanced OBO power level using symmetrical carrier and peaking amplifiers. It was shown in the previous section that the use of abrupt tuning varactors seriously limits the tuning range of the PA which directly shortens the load modulation range to achieve enhanced BO efficiency. Combining the varactor-based load modulation with Doherty PA, alleviates some of these limitations and enables wider load modulation range for efficiency enhancement up to 10 dB OBO.

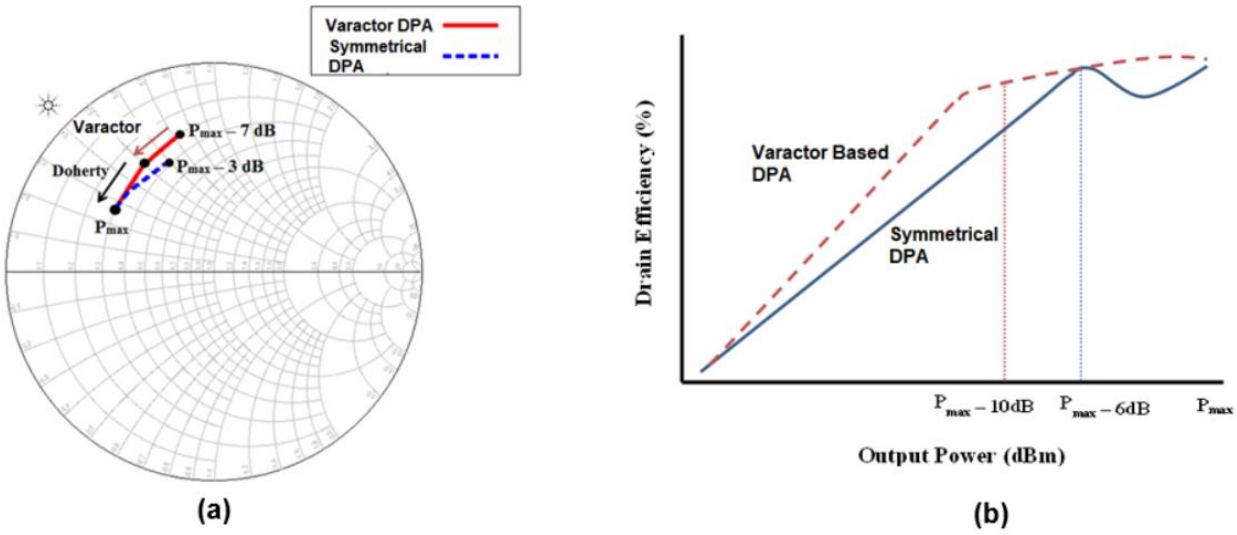
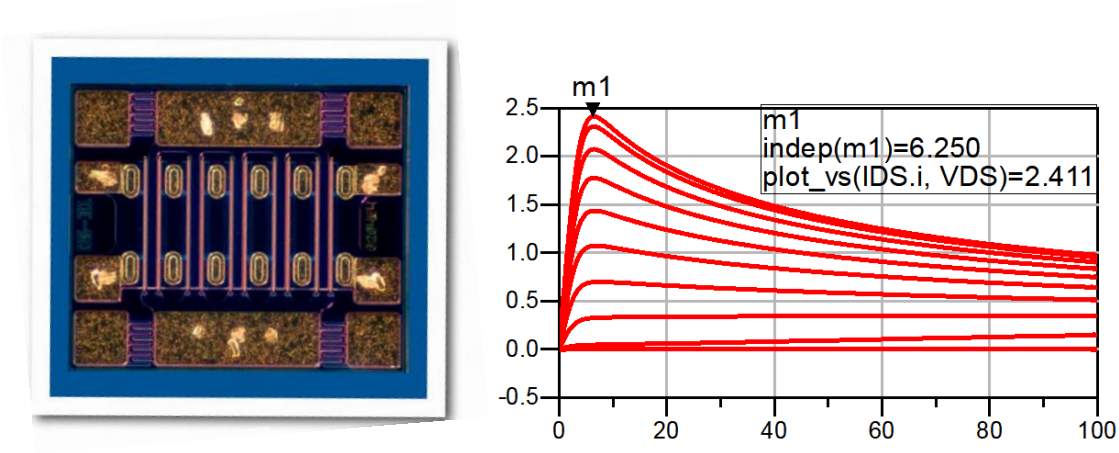


Fig. 2.8: (a)Load Tracking: Varactor based Doherty vs Traditional Symmetrical DPA. (b)Conceptual Drain Efficiency (%) vs Output Power (dBm).

A conceptual load trajectory and drain efficiency vs normalized output power plot is shown in Figure 2.8. Since the varactor alone cannot tune the load for the required load modulation at 10 dB OBO, symmetrical Doherty architecture modulates the load up to 6 dB OBO while the other 4 dB comes from the varactor tuning.

2.4.1 Circuit Design:

To validate the concept of varactor-based Doherty PA, a GaN based PA has been designed using Cree's 15W bare die, CGH60015D for both the carrier and peaking PA. This GaN die is 100 µm thick with dimensions of 1060 x 920 µm with operating range of DC-6.0 GHz. It can provide better than 15 W output power with better than 15 dB gain up to 4.0 GHz [21]. This die has back side metal connection for source connection whereas drain and gate connections are made through gold or silver wire bonding. Electrically and thermally conductive epoxy is needed for die attach and proper source grounding. Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) plating is recommended for die pad. For this design, the frequency range of interest is at 1.8-2.2 GHz. For 28 V drain voltage operation, the R_{Opt} is found to be 18.05 Ω (V_{knee} = 6.25 V and I_{max} = 2.41 A).



(a) (b)

Fig. 2.9: (a) Cree CGH60015D GaN bare die [21]. (b) DC-IV characteristic of CGH60015D die.

Since drain to source parasitic capacitance is 1.3 pF then X_{CDS} / R_{Opt} = 3.8 - 3.1 in the frequency of interest. Figure 2.9 shows the Cree GaN bare die and its DC-IV characteristics.

For this design, loadpull simulation at the extrinsic device plane has been performed for the frequency range of interest. Figure 2.10 shows the loadpull simulation results at 2.0 GHz at the extrinsic device plane. It is clear that if load can be modulated along the black arrow, efficiency enhancement up to 10 dB OBO could be achieved.

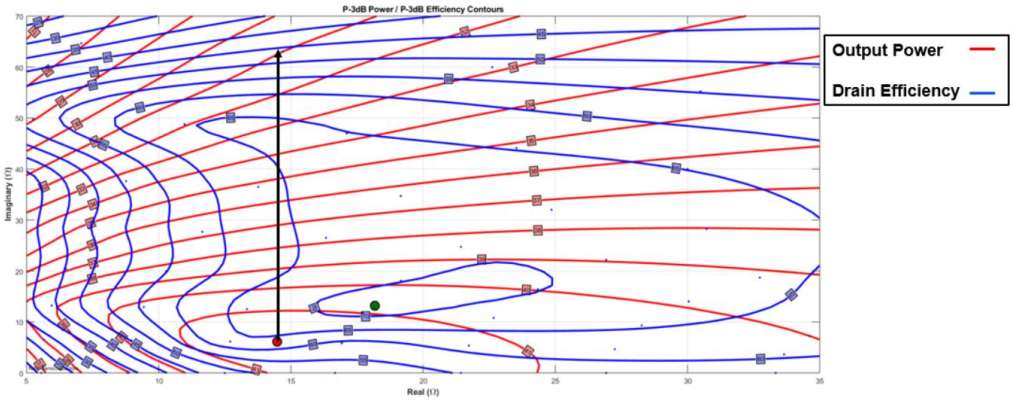
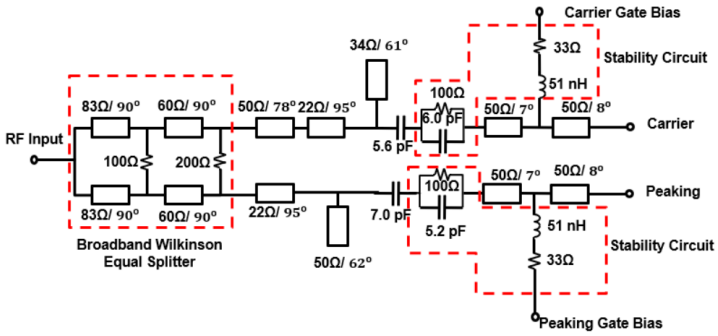
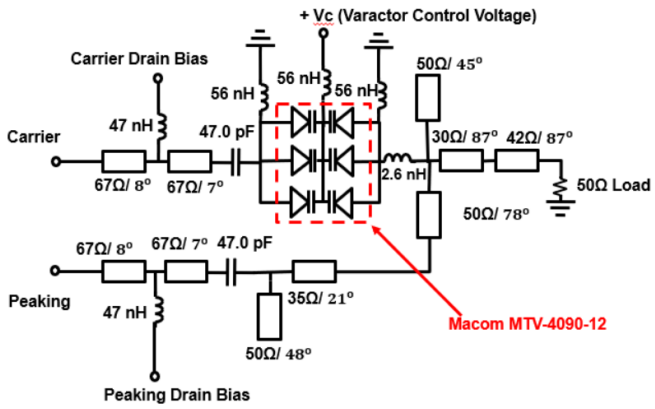


Fig. 2.10: Output Power and Efficiency contours of at 3 dB compression at extrinsic device plane at 2.0 GHz.



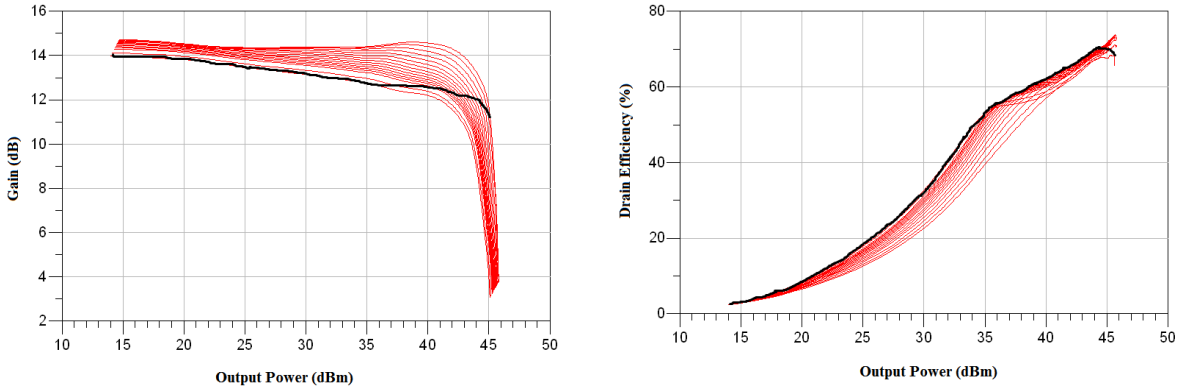
(a)



(b)

Fig. 2.11: (a) Input Matching Network of the Varactor based DPA at 1.9 GHz. (b) Output Matching Network of the Varactor based DPA at 1.9 GHz.

Based on the loadpull simulation results, input and output matching networks for the carrier and peaking PAs have been designed. Figure 2.11 shows the schematic of the networks at 1.9 GHz. At the input of the circuit, a two-stage broadband Wilkinson power splitter has been used for equal power split to the both of the PAs. Following the input splitter, there is single section distributed element based matching network for input impedance matching which also includes the stability circuits and gate biasing mechanism. Similarly output network also uses single section matching network for the output match. The carrier PA output network uses a varactor array that includes three anti-series varactor pairs connected in parallel for the load modulation. A RF choke inductor of 47 nH has been used for drain bias for both the PAs. Finally, two section impedance matching is used after the Doherty combining node to transform the impedance to 50 Ω. All the distributed elements were modelled in Keysight Advanced Design System (ADS) using the 3-D FEM simulator.



(a) (b)

Fig. 2.12: (a) Simulated Gain (dB) vs Output Power (dBm) and (b) Drain Efficiency (%) vs Output Power (dBm) at 1.9 GHz.

After modelling the distributed elements, a harmonic balance simulation has been performed for all frequencies in the band of interest. Figure 2.12 shows the gain and drain efficiency as a function of output power at 1.9 GHz. Figure 2.13 shows the summary of simulation results over the frequency range of 1.8-2.2 GHz. Clearly, the load modulation range has increased due to the combination of two different load modulation techniques.

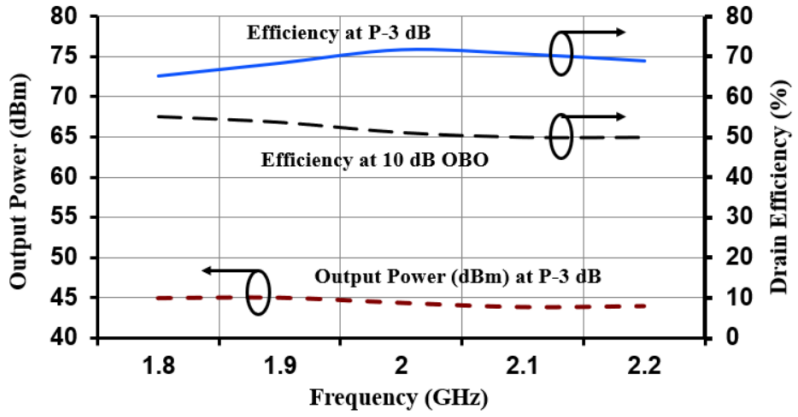


Fig. 2.13: Output Power (dBm) and Efficiency (%) performance over Frequency (GHz)

This PA maintains more than 50% drain efficiency at 10 dB OBO based on the simulation results. Output Power remains better than 43.5 dBm over the above mentioned frequency range.

2.4.2 Measured Results:

Based on the simulated structures, the varactor-based load modulated Doherty PA has been fabricated on Rogers 04350B PCB substrate material (ε_r = 3.66, H = 20 mil) as shown in Figure 2.14. This PA is characterized with continuous-wave (CW) excitation. CW measurements were taken for various varactor voltages. Figure 2.15 shows measured gain and drain efficiency as a function of output power at 1.88 GHz. It is clear that the output power and efficiency at 3 dB compression point is very similar to the simulated results. However, the efficiency at 10 dB OBO is drastically degraded compared to the simulation results. There is 15% efficiency shift in the drain efficiency at the 10 dB OBO. This large shift is attributed to the poor modelling of the varactor diodes and the high loss induced by the diodes. This insertion loss does not only induce losses, but it also shifts the PA output impedance from the optimum load trajectory, which also affects the efficiency at OBO power levels.

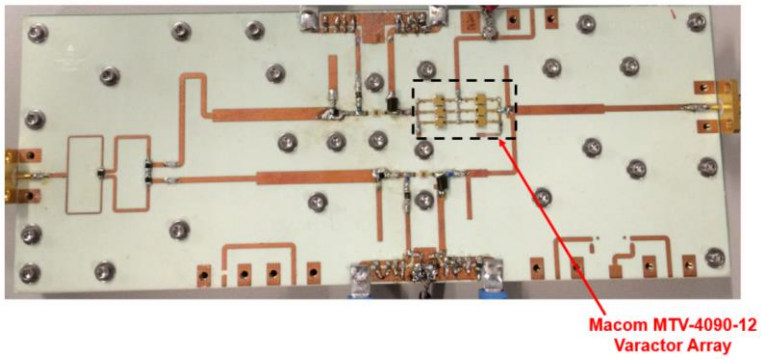


Fig. 2.14: Fabricated varactor-based Doherty power amplifier.

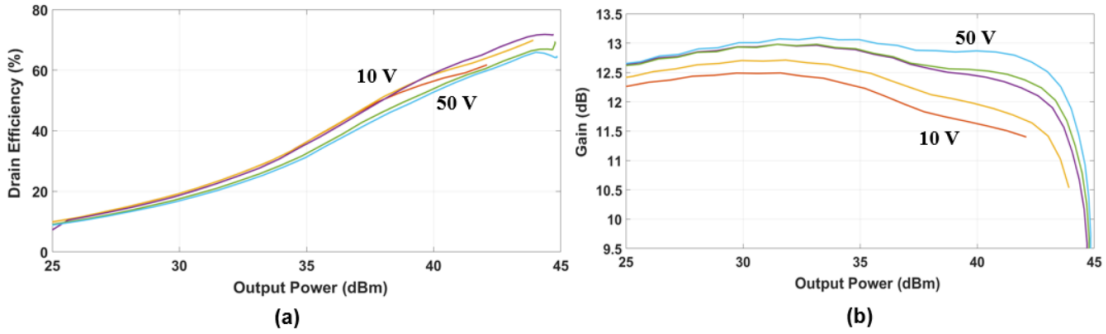


Fig. 2.15: Measured (a) Drain Efficiency (%) vs Output Power (dBm) and (b) Gain (dB) vs Output Power (dBm) at 1.880 GHz.

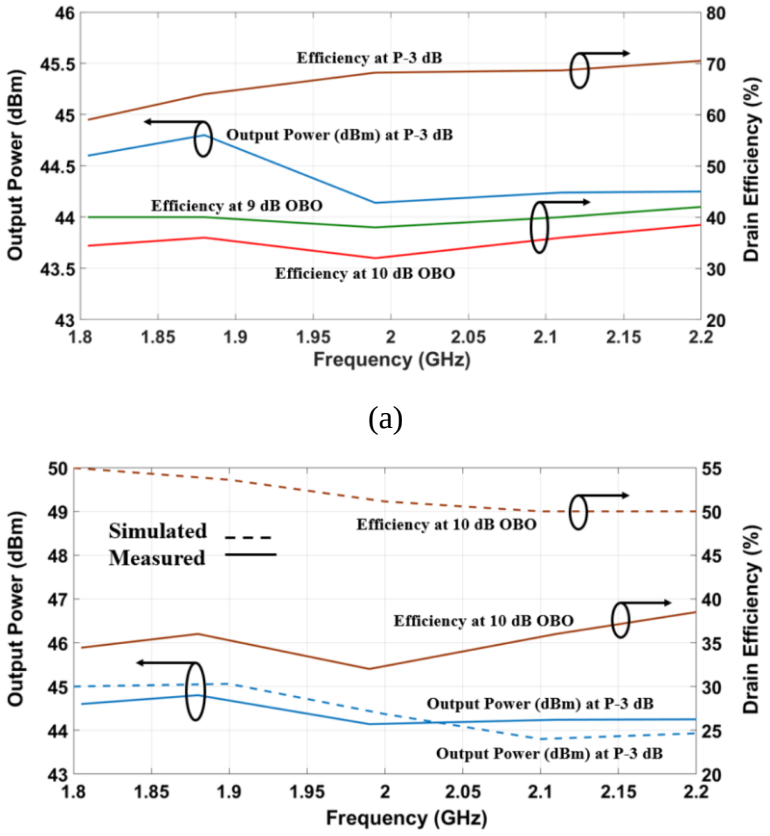


Fig. 2.16: (a) Summary of measured results (dBm) and (b) Comparison of simulated and measured results.

Figure 2.16 shows a summary of the measured results over the frequency of interest. Table 2.1 summarizes the state-of-the-art varactor-based power amplifiers. The presented varactor-based DPA clearly demonstrates competitive efficiency with good bandwidth performance compared to prior works.

TABLE 2.1

COMPARISON OF VARACTOR BASED POWER AMPLIFIERS

Ref.	Freq. (GHz)	P-3 dB (dBm)	DE at P-3 dB (%)	DE at 10 dB OBO (%)	Varactor Type
[22]	0.68, 1.84	>41	> 61.3	> 43.5	Non-Abrupt
[23]	0.9 – 2.0	40 -41	> 50	20 -45	Abrupt
[24]	1.7 -2.3	>36	42 -52	32 -39 (at 6 dB OBO)	Abrupt
[25]	1.8 – 2.2	40.1 – 41.5	> 45	27 -33	Non-Abrupt
This work	1.8 -2.2	43.7 - 45	58 -70	32 -39	Abrupt

2.5 Conclusions:

A novel load modulated PA architecture has been proposed, designed and fabricated which combines the concept of varactor-based PA and Doherty PA to achieve extended efficiency range at back-off power levels. Fabricated PA shows a significant degradation of OBO efficiency compared to simulation results, due to the high loss of the varactor array that is placed at the output network of the carrier PA. Following chapters will propose novel Doherty PA architecture/techniques that will achieve better performance without the use of any varactor diodes at the output of the Doherty PA.

CHAPTER – III

PHASE EXPLOITED DOHERTY POWER AMPLIFIER

3.1 Introduction:

As detailed in previous chapters, traditional symmetrical DPAs provide efficiency enhancement up to 6 dB OBO with 2:1 voltage standing wave ratio (VSWR). Recent development in wireless telecommunication industry has initiated the need for PA modules capable of amplifying signal with PAPR greater than 6 dB. Multi-way, multistage and digital DPAs have been considered as a potential solution to this new challenge. However, all of these architectures have their own limitations which is well described in chapter-I. This lead to the need of further investigation in to the symmetrical DPA with an aim to widen the load modulation to achieve efficiency enhancement beyond 6 dB OBO. To eliminate the disadvantages associated with multi-way or multi-stage DPAs without compromising the efficiency at the desired OBO power level, several new design techniques have been recently introduced to achieve wider load modulation (> 6 dB) using symmetrical DPAs. These include generalized load network synthesis [26]-[28], complex combining at the load [29], and DPA design with modified offset lines [30]. Generalized load network synthesis based DPA utilizes the non-infinite output impedance of the peaking PA to achieve wider load modulation. It defines the DPA's output load network as a lossy 2-port network and derives necessary design parameters to obtain the back-off efficiency peak at an arbitrary power level using symmetric carrier and peaking devices. Symmetrical DPAs with complex impedance at the Doherty combining node have achieved larger VSWR between the modulating loads compared to a traditional DPA configuration.

In [30], an explicit circuit model is developed for the DPA and modified offset lines are used to achieve an extension of the high efficiency range of the DPA.

This work presents an alternative design methodology for symmetrical DPAs, which uses the phasor relationship between the carrier and peaking currents at the Doherty combining node to extend the dynamic load modulation range beyond the traditional 2:1 VSWR.

3.2 Theoretical Analysis:

The operation of a conventional DPA has been explained in detail in many articles [6]-[12]. This section will focus on the working principle and network synthesis of the phase exploited DPA. First, the critical relationships between phase of the currents at the Doherty combining node, OBO, VSWR, saturated power, and efficiency of the DPA are established. Next, these relations are used to derive the network parameters of the Doherty combiner for a given set of boundary conditions for the proposed phase exploited DPA (PE-DPA). Based on the standard methodology in prior literature [26]-[30], all analysis in this section assumes both the carrier and peaking devices as equal sized ideal current sources with no device parasitic, knee voltage, channel length modulation, or harmonic content.

3.2.1 Working Principle of the PE-DPA:

A simplified DPA architecture is shown in Fig. 3.1. The carrier and peaking PA's intrinsic device planes are denoted as Z_C and Z_P, whereas the planes at the Doherty combining node seen from the carrier and peaking sides are marked as Z_{C1} and Z_{P1}, respectively. $I_C\angle\theta_C$ and $I_P\angle\theta_P$ are the currents at the intrinsic device plane, and $I_{C1}\angle\theta_{C1}$, $I_{P1}\angle\theta_{P1}$ are the currents at the Doherty combining node. R_{Opt} is the optimum impedance

to generate maximum output power from the carrier PA. A conventional DPA at saturated power level can be generally described at the combining node by the following equations:

$$Z_{C1} = \left(1 + \frac{I_{P1}\angle\theta_{P1}}{I_{C1}\angle\theta_{C1}}\right)R_{Comb} \tag{3.1}$$

$$\Gamma_{C1} = \frac{Z_{C1} - R_{Comb}}{Z_{C1} + R_{Comb}} \tag{3.2}$$

$$VSWR = n = \frac{1 + |\Gamma_{C1}|}{1 - |\Gamma_{C1}|} \tag{3.3}$$

$$\alpha = \frac{|I_{P1}|}{|I_{C1}|} = \frac{P_{SAT,P}}{P_{SAT,C}} \tag{3.4}$$

$$OBO_{CDPA} = 20\log_{10}(n) \tag{3.5}$$

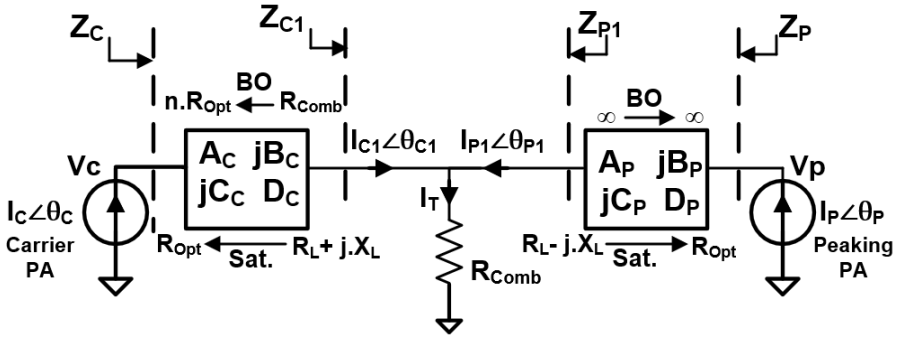


Fig. 3.1: Conceptual diagram illustrating proposed Doherty power amplifier's operation.

For a conventional DPA, the currents at the Doherty combining node are always in-phase ($\theta_{C1} = \theta_{p1}$) at saturation. This in-phase current combining allows carrier PA load modulation of R_{Comb} at BO to $n \cdot R_{Comb}$ in saturation at the Z_{C1} plane, with VSWR of n:1, where the current or saturation power (P_{SAT}) ratio of the carrier and peaking PA is expressed as $\alpha = n - 1$. This load modulation at the Doherty combining node is translated to a load modulation of $n \cdot R_{Opt}$ at BO to R_{Opt} in saturation at the Z_C plane using the carrier PA's output matching network (OMN), which is a quarter wave transmission line with characteristic impedance of $\sqrt{n \cdot R_{Opt} \cdot R_{Comb}}\ \Omega$. For a symmetrical DPA configuration, α

is equal to unity, and the α ratio is greater than one in an asymmetrical DPA. If n is the VSWR of the carrier load modulation, then the VSWR and OBO are related by (5) for a conventional DPA (CDPA). The peaking PA's OMN provides optimum matching of $[n/(n-1)]R_{Comb}$ at the Z_{P1} plane to R_{Opt}/n at the peaking intrinsic device plane (Z_P) at the saturation. The peaking OMN presents high off-state impedance at the Doherty combining node at back-off power levels.

This section presents a novel DPA architecture that intentionally mismatches the phase of the currents at the Doherty combining node ($\theta_{C1} \neq \theta_{p1}$) at saturation to achieve wider load modulation. It proposes that if the same magnitude can be maintained with specific phase difference ($\Delta\theta_1 = \theta_{P1} - \theta_{C1}$) between the two combining currents (I_{C1}, I_{P1}) in a symmetrical DPA configuration at saturation, the VSWR can be extended beyond 2:1. Furthermore, the PA's maximum (saturated) output power is not affected by the mismatch in phase. A symmetrical PE-DPA at saturated power level can be described at its combining node by the following equations:

$$|I_{C1}| = |I_{P1}| \text{ and } \Delta\theta_1 = \theta_{P1} - \theta_{C1} \tag{3.6}$$

$$Z_{C1} = R_L + j \cdot X_L \tag{3.7}$$

$$Z_{P1} = R_L - j \cdot X_L \tag{3.8}$$

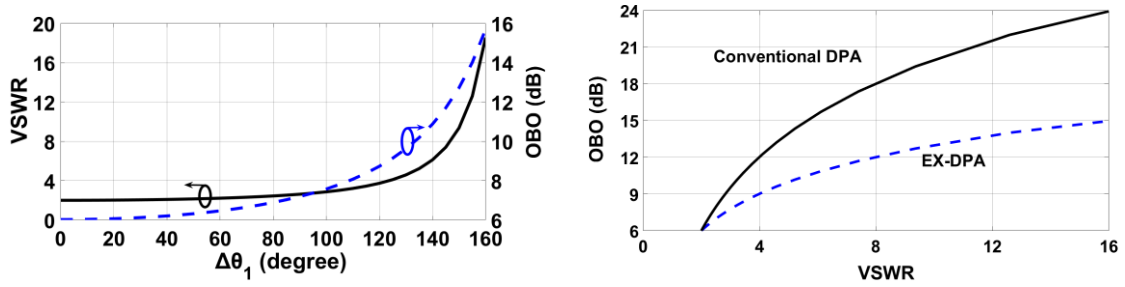
$$R_L = R_{Comb} \cdot [1 + \cos(\Delta\theta_1)] \tag{3.9}$$

$$X_L = R_{Comb} \cdot [\sin(\Delta\theta_1)] \tag{3.10}$$

$$OBO_{PE-DPA} = 10 \log_{10}(2 \cdot n) \tag{3.11}$$

In the proposed DPA, the carrier PA experiences load modulation of R_{Comb} at BO to $R_L + j \cdot X_L$ in saturation at the Z_{C1} plane, and the carrier OMN ensures load modulation of

$n \cdot R_{Opt}$ at BO to R_{Opt} in saturation at the Z_C plane. For the peaking PA, the load modulates from an open circuit when the peaking PA is off to $R_L - j \cdot X_L$ at saturation at the Z_{P1} plane. The peaking OMN transforms $R_L - j \cdot X_L$ to R_{Opt} at the Z_P plane and ensures high impedance at the Doherty combining node when the peaking PA is off. Fig. 3.2(a) shows the theoretically achievable VSWR and OBO of the PE-DPA for various $\Delta\theta_1$ using (3.6) - (3.11). It is shown that a VSWR of 2:1 results in an efficiency peak at 6 dB OBO when both currents are in-phase, and both the VSWR and OBO level increase as phase difference $\Delta\theta_1$ increases, thus confirming the advantage of the presented technique. The required VSWR for any given OBO level is higher for any extended high efficiency range symmetrical DPA (EX-DPA) [26]-[31], including the PE-DPA, when compared to a conventional asymmetrical DPA, as illustrated in Fig. 3.2(b). This is due to the equal power contribution of the peaking PA in a symmetrical configuration compared to an asymmetrical DPA where the peaking PA contributes more power than the carrier PA. For any EX-DPA, the relationship between OBO and VSWR is given in (3.11), whereas it follows (3.5) in a conventional asymmetrical DPA.



(a) (b)

Fig. 3.2. (a) VSWR and OBO versus $\Delta\theta_1$. (b) OBO versus VSWR for the asymmetrical DPA and extended efficiency range symmetrical DPA.

3.2.2 Closed Form Analysis of the Doherty Combiner:

The theory and basic functionality of the PE-DPA has been explained in the previous section. In order to achieve the desired performance from the PE-DPA, the carrier and peaking PA OMNs must present the appropriate impedances at BO and saturated power levels at the intrinsic device planes. This section derives closed form analytical expressions of the Doherty output combiner in order to obtain the correct OMN parameters for PE-DPA design. The analysis is based on the following boundary conditions:

1) Maintain $|I_{C1}| = |I_{P1}|$ and a desired phase difference of $\Delta\theta_1 = \theta_{P1} - \theta_{C1}$ at the Doherty combining node, based on the required OBO level at the saturated power level.
2) When the peaking PA is off: The carrier OMN needs to match R_{Comb} to $n \cdot R_{Opt}$, and the peaking OMN needs to present an open circuit at the Doherty combining node.
3) At saturation: The carrier OMN needs to match $R_L + j \cdot X_L$ to R_{Opt}, and the peaking OMN needs to match $R_L - j \cdot X_L$ to R_{Opt}.

Based on the boundary conditions, the following relationships between the ABCD parameters of the carrier and peaking output networks and the design parameters (R_L, X_L, n, R_{Opt}, $\Delta\theta_1$) are established. Subscript 'c' and 'p' refer to the carrier and peaking PAs, respectively.

$$n \cdot R_{Opt} = \frac{A_C \cdot R_{Comb} + j \cdot B_C}{j \cdot C_C \cdot R_{Comb} + D_C} \tag{3.12}$$

$$R_{Opt} = \frac{A_C \cdot [R_L + j \cdot X_L] + j \cdot B_C}{j \cdot C_C \cdot [R_L + j \cdot X_L] + D_C} \tag{3.13}$$

$$R_{Opt} = \frac{A_P \cdot [R_L - j \cdot X_L] + j \cdot B_P}{j \cdot C_P \cdot [R_L - j \cdot X_L] + D_P} \tag{3.14}$$

$$\infty = \frac{j \cdot D_P}{C_P} \tag{3.15}$$

Equations (3.12)-(3.13) describe the carrier OMN, and (3.14)-(3.15) describe the peaking OMN. Since the impedance at both BO and saturated power levels at the Z_C and Z_P planes are purely resistive, and the carrier and peaking OMNs are ideally lossless and reciprocal networks, the following expressions are derived from the relations given in (3.12)-(3.15).

$$A_C \cdot C_C = \frac{B_C \cdot D_C}{R_{Comb}^2} \tag{3.16}$$

$$\left[\frac{R_L^2 + X_L^2}{R_{Comb}^2} - 1\right] \cdot D_C - \left[\frac{X_L}{R_{COmb}^2 \cdot C_C}\right] \cdot D_C^2 + [C_C \cdot X_L] = 0 \tag{3.17}$$

$$[D_C^2 + R_{Comb}^2 \cdot C_C^2] \cdot n \cdot R_{Opt} = [A_C \cdot D_C + B_C \cdot C_C] \cdot R_{Comb} \tag{3.18}$$

$$A_C \cdot D_C + B_C \cdot C_C = 1 \tag{3.19}$$

$$A_P \cdot D_P + B_P \cdot C_P = 1 \tag{3.20}$$

$$A_P \cdot C_P \cdot R_L^2 = [B_P - (A_P \cdot X_L)] \cdot [D_P + (C_P \cdot X_L)] \tag{3.21}$$

For the carrier OMN, the four unknown network parameters (A_c, B_c, C_c, and D_c) are determined from the four equations given in (3.16)-(3.19). Similarly, network parameters for the peaking OMN are derived from (3.14)-(3.15) and (3.20)-(3.21). All network parameters for the carrier and peaking PA OMNs are summarized below for proper PE-DPA functionality.

$$A_C = Q \cdot n \cdot R_{Opt} \cdot R_{Comb} \cdot C_C \tag{3.22}$$

$$B_C = n \cdot R_{Opt} \cdot R_{Comb} \cdot C_C \tag{3.23}$$

$$C_C = 1/[\sqrt{n \cdot R_{Opt} \cdot R_{Comb}((Q \cdot R_{Comb})^2 + 1)}] \tag{3.24}$$

$$D_C = Q \cdot R_{Comb}^2 \cdot C_C \tag{3.25}$$

$$Q = -[\left(1 - \frac{R_L^2 + X_L^2}{R_L^2}\right) \pm \sqrt{\left(1 - \frac{R_L^2 + X_L^2}{R_L^2}\right)^2 + 4 \cdot \left(\frac{X_L^2}{R_L^2}\right)}]/[2 \cdot X_L] \tag{3.26}$$

$$A_P = \pm\sqrt{R_{Opt}/R_L} \tag{3.27}$$

$$B_P = \pm\sqrt{R_{Opt}/R_L} \cdot X_L \tag{3.28}$$

$$C_P = 0 \tag{3.29}$$

$$D_P = \pm\sqrt{R_L/R_{Opt}} \tag{3.30}$$

Using the above derived network parameters, the voltages (V_C, V_P) and currents (I_{C1}, I_{P1}) at the device plane and Doherty combining plane respectively are expressed as:

$$\begin{bmatrix} V_C \\ I_C \end{bmatrix} = \begin{bmatrix} A_C & j \cdot B_C \\ j \cdot C_C & D_C \end{bmatrix} \cdot \begin{bmatrix} R_{Comb}(I_{C1} + I_{P1}) \\ I_{C1} \end{bmatrix} \tag{3.31}$$

$$\begin{bmatrix} V_P \\ I_P \end{bmatrix} = \begin{bmatrix} A_P & j \cdot B_P \\ j \cdot C_P & D_P \end{bmatrix} \cdot \begin{bmatrix} R_{Comb}(I_{C1} + I_{P1}) \\ I_{P1} \end{bmatrix} \tag{3.32}$$

By expanding (3.31) -(3.32), V_C, V_P, I_{C1} and I_{P1} are expressed in terms of network parameters and device intrinsic currents (I_C, I_P), as listed below.

$$V_C = \frac{I_C \cdot [(A_C \cdot R_{Comb}) + j \cdot B_C] + I_P \cdot [\frac{R_{Comb}}{D_P}]}{[D_C + (j \cdot C_C \cdot R_{Comb})]} \tag{3.33}$$

$$V_P = \frac{I_C \cdot [R_{Comb}]}{D_P \cdot [D_C + (jC_C \cdot R_{Comb})]} + \left[\frac{(A_P \cdot D_C \cdot R_{Comb})}{D_P \cdot [D_C + (jC_C \cdot R_{Comb})]} + \frac{j \cdot B_P}{D_P}\right] \cdot I_P \quad (3.34)$$

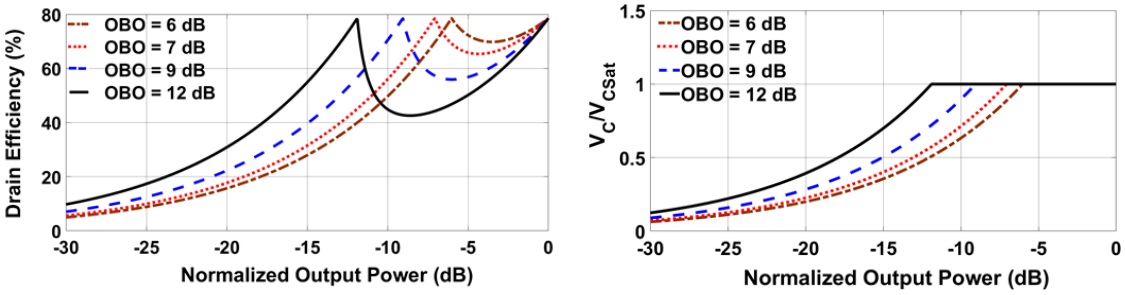
$$I_{C1} = \frac{D_P \cdot I_C - (j \cdot C_C \cdot R_{Comb}) \cdot I_P}{D_P \cdot [D_C + (j \cdot C_C \cdot R_{Comb})]} \quad (3.35)$$

$$I_{P1} = \frac{I_P}{D_P} \quad (3.36)$$

Finally, the intrinsic device currents (I_C, I_P) must maintain an appropriate phase difference ($\Delta\theta = \theta_P - \theta_C$) at saturation to achieve the desired $\Delta\theta_1$ at the Doherty combining node for wider load modulation. From (3.31) and (3.32), the carrier and peaking intrinsic currents are expressed as:

$$I_C \angle\theta_C = j \cdot C_C \cdot R_{Comb} \cdot [I_{C1} \angle\theta_{C1} + I_{P1} \angle\theta_{P1}] + D_C \cdot I_{P1} \angle\theta_{P1} \quad (3.37)$$

$$I_P \angle\theta_P = D_P \cdot I_{P1} \angle\theta_{P1} \quad (3.38)$$



(a) (b)

Fig. 3.3: (a) Drain Efficiency and (b) Normalized carrier drain voltage versus Normalized Output Power.

When the $|I_{C1}| = |I_{P1}|$ and $\Delta\theta_1 = \theta_{P1} - \theta_{C1}$, boundary conditions are applied to (3.37) and (3.38), the required $\Delta\theta$ is defined in terms of the DPA's design and network parameters as:

$$\Delta\theta = \pi - \arctan\left(\frac{-(C_C \cdot R_{Comb}) - (C_C \cdot R_{Comb} \cdot \cos[\Delta\theta_1]) + (D_C \cdot \sin[\Delta\theta_1])}{-(C_C \cdot R_{Comb} \cdot \sin[\Delta\theta_1]) - (D_C \cdot \cos[\Delta\theta_1])}\right) \quad (3.39)$$

Once the design and network parameters are determined as a function of the required OBO levels, the overall performance of the PE-DPA can be predicted over varying $\Delta\theta_1$. To analyze the PE-DPA performance, linear I_C, I_P with respect to input voltage signal (V_{in}) and class B operation for DC power consumption for both the PAs are assumed. The profile of I_C, I_P with respect to normalized input voltage signal (V_{in}) is shown in (3.40) -(3.41), where I_{max} is the maximum drain current through each device at saturation.

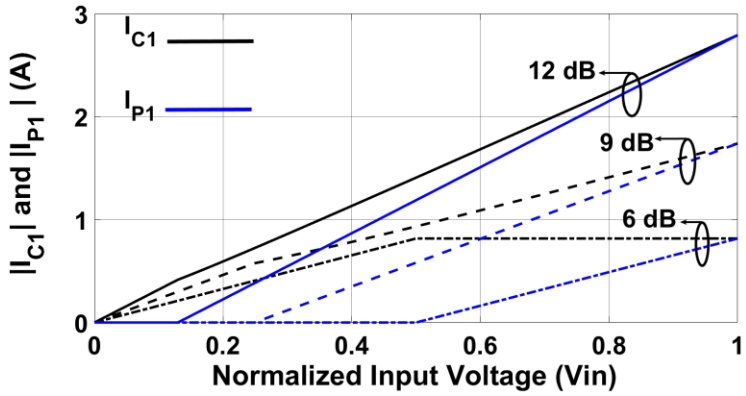
$$I_C = V_{in} \cdot \frac{I_{max}}{2} \angle \Delta\theta, \quad 0 \le V_{in} \le 1 \tag{3.40}$$

$$I_P = \begin{cases} 0, & 0 \le V_{in} \le C \\ \frac{V_{in}-C}{1-C} \cdot \frac{I_{max}}{2}, & C < V_{in} \le 1 \end{cases}; \qquad C = \frac{1}{n} \tag{3.41}$$

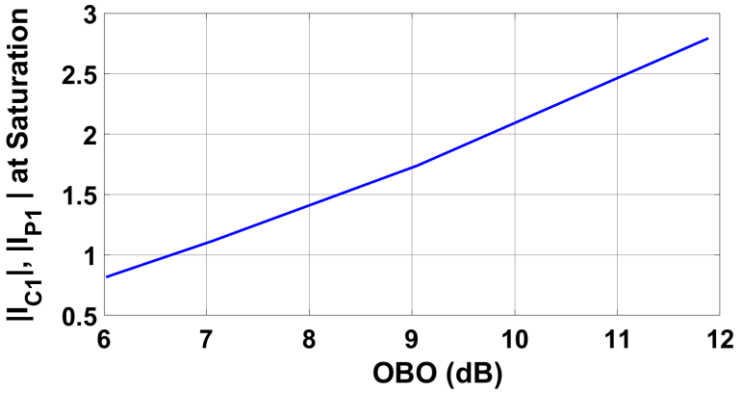
Since the voltages and currents at the intrinsic device plane of the carrier and peaking PAs are known from (3.33)-(3.34) and (3.40)-(3.41), the output power and efficiency of the PE-DPA for various $\Delta\theta_1$ is calculated, and Fig. 3.3(a) plots the drain efficiency of the PE-DPA for varying normalized output power when $\Delta\theta_1$ is 0º, 86º, 124º and 146º. Fig. 3.3(b) plots the normalized drain voltage at the carrier device intrinsic plane versus the normalized output power, which shows the drain voltage maintains maximum excursion during the active load modulation, ensuring the PA's proper Doherty operation.

Moreover, the PE-DPA maintains its saturated output power level despite having phase mismatch at the Doherty combining node. This constant saturated output power is explained from the plots shown in Fig. 3.4. Fig. 3.4(a) shows the currents I_{C1} and I_{P1} at the Doherty combining node as a function of the normalized input drive voltage when the

normalized intrinsic device drain currents (I_C, I_P) vary from 0 to 1. From Fig. 3.4(b) that plots the magnitude of the combining currents at saturated power for various OBO levels, the magnitude of the currents at the Doherty combining node (I_{C1} and I_{P1}) are observed to be higher for the PE-DPA with higher designed OBO level.



(a)



(b)

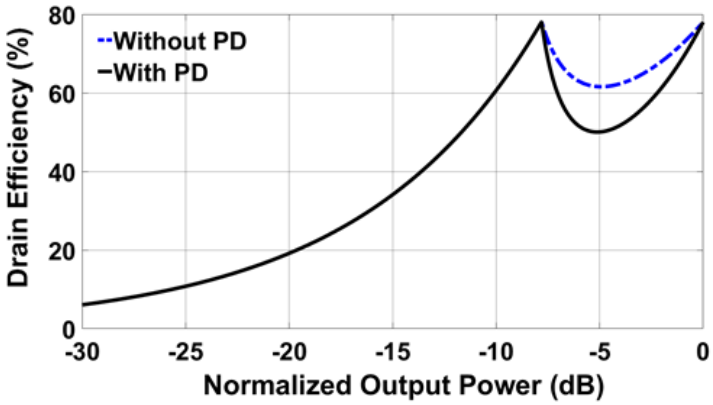
Fig. 3.4: (a) Magnitude of the currents at Doherty combining node versus normalized input voltage. (b) Magnitude of currents at the combining node at saturated power level versus designed OBO of the PE-DPA.

For example, when the currents are in-phase and efficiency enhanced up to 6 dB OBO, the magnitude of the currents at saturated power level reached 0.8 while this magnitude is

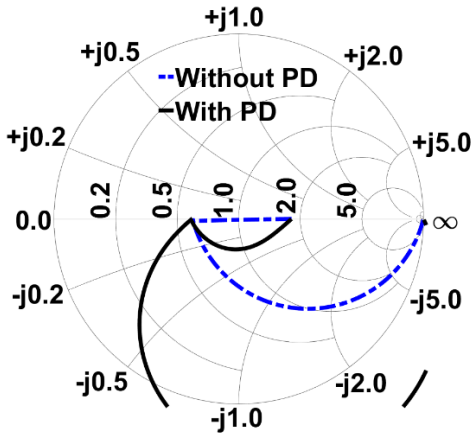
2.7 when the currents are 146º out of phase for efficiency enhancement up to 12 dB OBO. Since the magnitude of the currents increases at the Doherty combining node with higher $\Delta\theta_1$, it ensures the resultant current flowing (I_T) to the final load is constant, hence keeping the total power delivered to the load constant regardless of the currents combining phase.

3.3 Optimum Load Trajectory:

The working principle of the PE-DPA has been explained in detail in the previous section. However, this analysis did not include the effect of the peaking PA's nonlinear phase distortion. The class C biased peaking amplifier experiences significant variation of the input capacitance with the input power drive, which causes deviation in the dynamic load trajectories of both the carrier and peaking PA, thus resulting in efficiency degradation. The effect of nonlinear phase distortion (PD) in DPAs has been explained in [32]-[33]. To further illustrate the effect of phase distortion, Fig. 3.5 shows the drain efficiencies and load trajectories of an ideal PE-DPA with 40º of PD (extracted from a Cree CGH60015D device simulation) and without the PD effect.



(a)

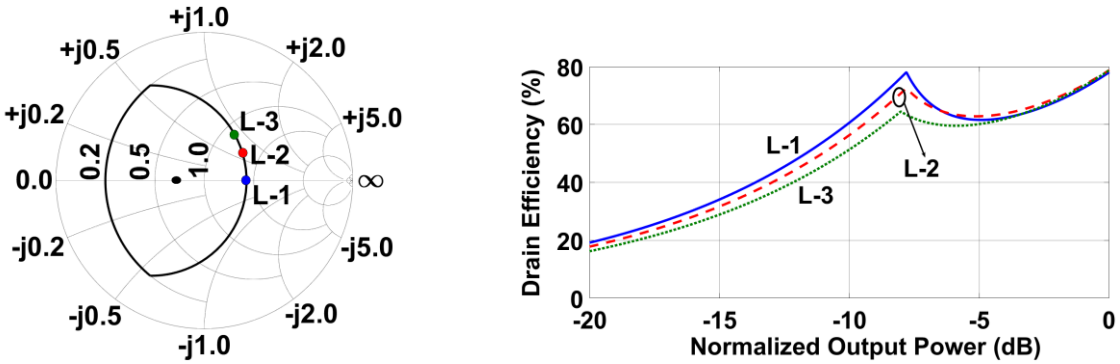


(b)

Fig. 3.5: (a) Drain Efficiency and (b) load trajectory of an ideal DPA with and without the effect of the nonlinear PD.

It is clear from the plots that nonlinear PD shifts the load trajectory for both the carrier and peaking PA away from the real impedance axis on the smith chart, which causes higher generated reactive power and lower drain efficiency. This section discusses the optimum load trajectory required for the PE-DPA to minimize this effect of nonlinear PD on the drain efficiency of the DPA. In the analysis of the previous section, the carrier PA BO impedance at the Z_C plane is a real impedance that moves away from real axis with the effect of nonlinear PD and causes the DPA efficiency dip between the two efficiency peaks. However, this BO impedance could be a complex one, if it falls on the device's required BO power contour. Fig. 3.6(a) shows an ideal loadpull contour at 5 dB BO power level. As the BO impedance moves away from the real axis, the BO efficiency gradually degrades as illustrated in Fig. 3.6(b). However, at the presence of nonlinear PD, the load trajectory moves towards the real axis instead of moving away from it. Therefore, an optimal choice of complex BO impedance can lead to higher average efficiency compared to a design

using the real BO impedance, even though the efficiency at a particular BO power level is lower.

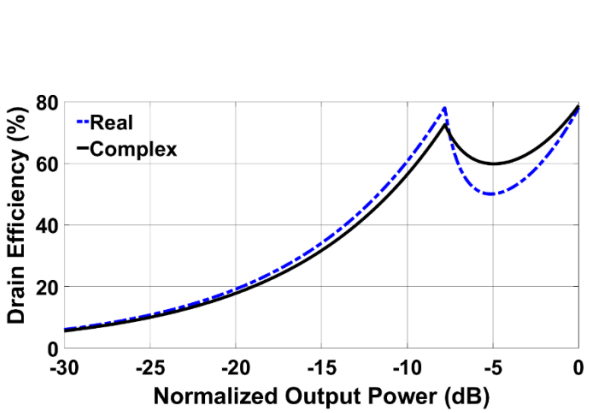


(a) (b)

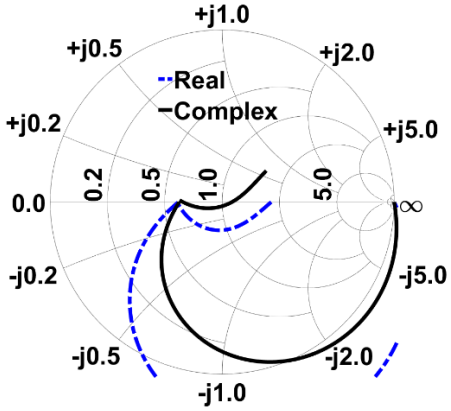
Fig. 3.6: (a) Ideal loadpull contour at 5 dB BO power. (b) Drain efficiency for various loads as denoted in the loadpull contour.

To clarify further, Fig. 3.7 plots the drain efficiency and load trajectory of the PE-DPA with second efficiency peak at 8 dB OBO in the presence of 40^0 of nonlinear PD when the BO impedance is purely resistive and complex. For complex BO impedance, both the carrier and peaking PA load trajectories experience significantly lower reactive impedance at the intrinsic device plane compared to the case when the BO impedance is purely resistive. This phenomenon ensures less reactive power generation in between the two efficiency peaks, which results in significantly higher efficiency in that output power range. To demonstrate the effect of nonlinear PD on average efficiency with real and complex BO impedance, simulations with a 20-MHz 8.0 dB PAPR based LTE signal are performed for real BO impedance and multiple complex BO impedances located on the constant BO power contour. Fig. 3.7(c) plots the difference in average efficiency compared to the nominal case of purely resistive BO impedance at 8 dB OBO power level, where x-axis is the resistive component of the BO impedance that is normalized to the purely resistive BO

impedance. As the real component of the BO impedance decreases [moves towards L-3 from L-1 in Fig. 3.6(a)], it is seen from Fig. 3.7(c) that average efficiency improves up to 4% before rolling off as the complex BO impedance becomes more reactive and less resistive. This analysis demonstrates that even though complex BO impedance causes some efficiency degradation at the specific BO power level [8 dB in this example], substantially higher efficiency in between the efficiency peaks enables higher average efficiency.



(a)



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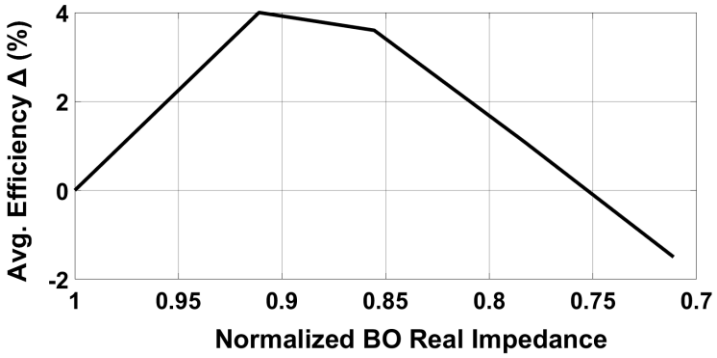


(c)

Fig. 3.7: (a) Drain Efficiency and (b) load trajectory of an ideal DPA with 40^0 of nonlinear PD with real and complex BO impedance. (c) Average drain efficiency with respect to normalized BO real impedance.

TABLE 3.1

MODIFIED NETWORK PARAMETERS OF THE CARRIER PA

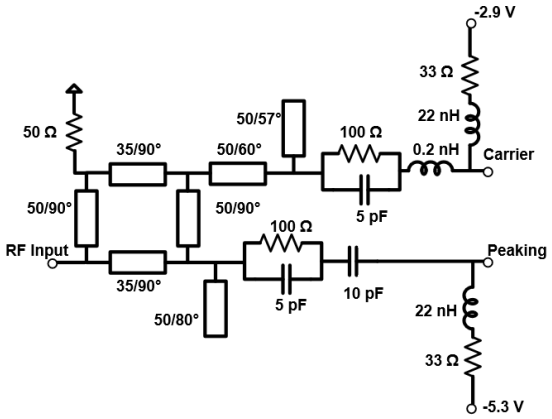
Carrier PA BO impedance, $Z_{C,BO} = R_B + j \cdot X_B$
$A_C = \frac{1 - C_C \cdot D_C \cdot X_B - C_C^2 \cdot R_{Comb} \cdot R_B}{D_C}$
$B_C = D_C \cdot X_B + C_C \cdot R_{Comb} \cdot R_B$
$C_C = \pm \sqrt{\frac{\left[\frac{R_{Comb}}{R_B}\right] \cdot M^2}{K^2 + [R_{Comb} \cdot M]^2}}$
$D_C = \pm \sqrt{\left[\frac{R_{Comb}}{R_B}\right] - [C_C \cdot R_{Comb}]^2}$
$K = R_L^2 + X_L^2 - \frac{R_{Comb} \cdot R_B \cdot R_L}{R_{Opt}}; \quad M = X_L + \frac{X_B \cdot R_L}{R_{Opt}}$

Since the network analysis presented in the previous section assumes resistive BO impedance for the carrier PA, it is necessary to re-derive the network parameters for the carrier PA OMN for complex BO impedance. However, the peaking PA's network parameters remain the same, since there is no change in its operation. Table 3.1 shows the modified network parameters for the carrier PA OMN with complex impedance.

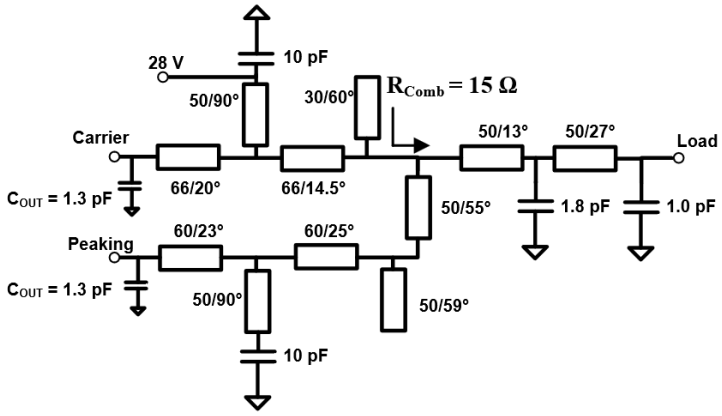
3.4 Experimental Validation and Measured Results:

To verify the concept of the PE-DPA, a symmetrical DPA at 2.14 GHz is designed using a pair of Cree GaN (CGH60015D) high-electron-mobility (HEMT) bare-die discrete devices integrated on a Rogers 04350B board material. The DPA is designed to exhibit an

extended efficiency range of 8 dB OBO. From Fig. 2(a), a VSWR of 3:1 with $\Delta\theta_1$ of 105 degrees at the Doherty combining node is required to achieve an efficiency peak at 8 dB OBO. Based on the load-pull simulation data, an R_{Opt} of 30 Ω has been chosen to deliver 41.0 dBm output power for both the carrier and peaking PA.



(a)



(b)

Fig. 3.8: (a) Input matching network, and (b) Output combiner network of the DPA at 2.14 GHz.

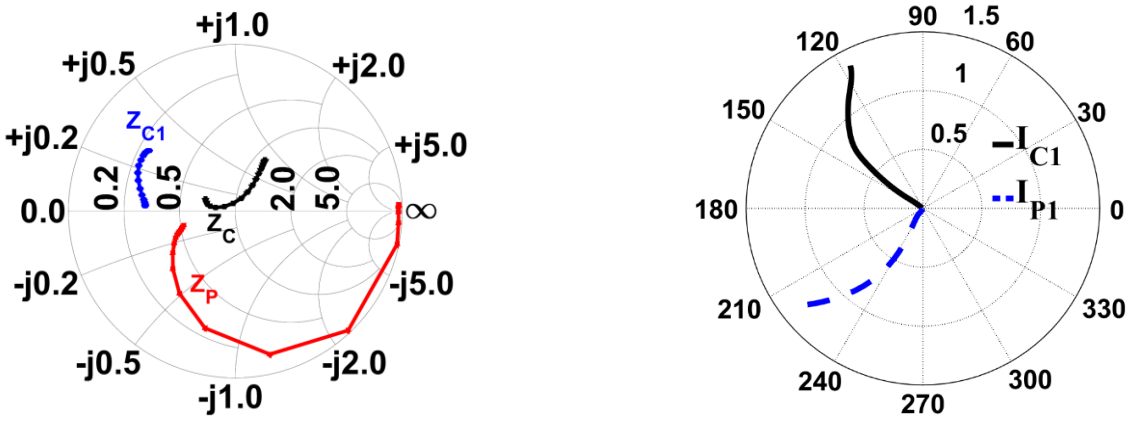
Since the DPA is intended for 8 dB OBO efficiency enhancement, the BO power level would be 36.0 dBm. Ideally, the BO resistive impedance would have been 90 Ω. However, based on the analysis presented in the previous section, a complex load of 65 + j·40 Ω is

selected as the BO impedance to optimize the carrier PA's load trajectory. Both of the PAs are combined atR_{Comb} of 15 Ω. After all the design parameters (R_{Opt}, R_B, X_B, R_L, X_L, R_{Comb} and $\Delta\theta_1$) are defined, network parameters for the carrier and peaking PA OMN are derived using (3.27) -(3.30) and Table 3.1. The required phase difference ($\Delta\theta$) between intrinsic device currents (I_C, I_P) is evaluated from (3.39).

For this design, negative roots have been used for the carrier PA network parameter D_C and all of the peaking PA's network parameters, and positive root is used for parameter C_C. These ABCD parameter-based networks are converted to transmission line-based networks using the technique described in [26]. At the OMNs, quarter-wave stubs at 2.14 GHz are used as DC feed lines and second harmonic traps. A two-section matching network is used after the Doherty combiner to transform the combining impedance of 15 Ω to the desired output load of 50 Ω. For the input side, a 90° branch-line coupler and input offset line are used for equal power split and phase adjustment to achieve the desired $\Delta\theta$ at the intrinsic drain planes of the PAs. Additionally, single section matching networks are used for impedance matching and gain optimization at the input side. Moreover, a parallel RC network in the input RF path and a series resistance in the input DC path are used to stabilize both the carrier and peaking PAs.

In this design, the carrier PA is biased with drain voltage of 28 V and quiescent current of 34 mA, whereas the peaking PA is biased in deep class C with a gate voltage of -5.3 V and drain voltage of 28 V. Fig. 3.8 shows a schematic diagram of the designed input matching network and output load network, which absorbs the device's output parasitic capacitance (C_{OUT} = 1.3 pF) at the drain node at 2.14 GHz. Fig. 3.9(a) shows the simulated

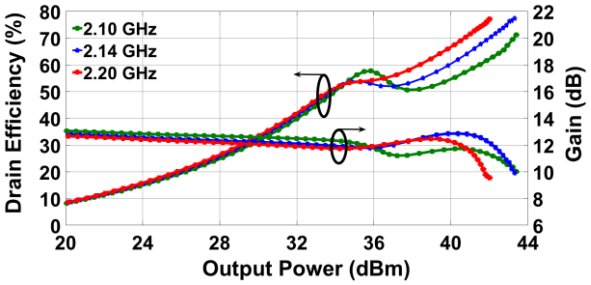
load modulation at the intrinsic device planes of the carrier PA (Z_C) and peaking PA (Z_P), as well as the load modulation at the combining node seen from the carrier (Z_{C1}) side. Additionally, Fig. 3.9(b) shows the phase difference between the carrier and peaking PA currents at the combining node to be 100 degrees. This simulated load trajectory and phase difference closely correlate to the theoretical analysis and confirm that the DPA has been correctly designed. Moreover, Fig. 3.10(a) shows the simulated RF performance of the DPA at 2.1-2.20 GHz. The DPA achieves output power of 43.5 dBm at 3-dB compression from 2.1-2.14 GHz, with drain efficiency better than 53% at 8 dB OBO. Fig. 3.10(b) is a picture of the fabricated PE-DPA, which realizes the input and output networks of Fig. 3.8.

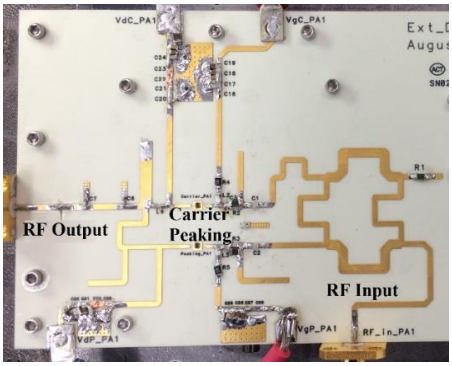


(a) (b)

Fig. 3.9: (a) Load modulation at various planes of the DPA at 2.14 GHz. (b) Phasor plot of carrier and peaking currents at the combining node at 2.14 GHz

The measured DPA's gain and drain efficiency (DE) are plotted as a function of output power under continuous-wave (CW) excitation in Fig. 3.11(a). At 3 dB gain compression (P-3dB) within 2.14-2.25 GHz operating frequency range, the DPA exhibits more than 43.3 dBm of output power with DE higher than 53% at 8 dB OBO and 52% at 9 dB OBO.

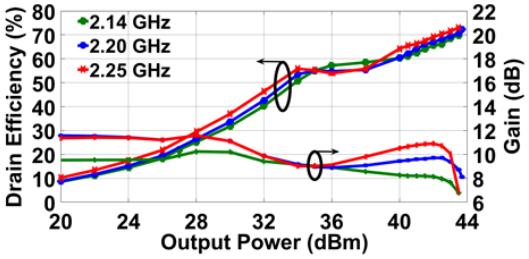


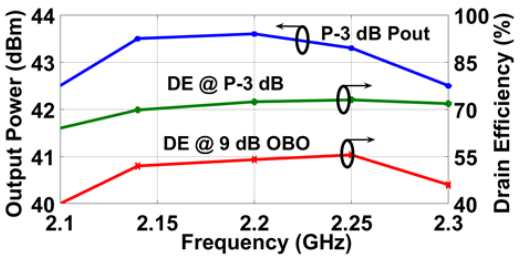


(a) (b)

Fig. 3.10: (a) Simulated performance of the DPA at 2.10-2.20 GHz. (b) Top view of the fabricated DPA.

Fig. 3.11(b) shows the DE at P-3dB and 9 dB OBO, as well as P3-dB over the 2.1-2.3 GHz range. This DPA maintains an output power higher than 42.5 dBm with DE more than 45% at 9 dB OBO in the 2.14-2.3 GHz range. It is clear that the performance peaks at 2.2 GHz with P-3dB of 43.6 dBm at 71.0% DE, and 54% DE at 9 dB OBO. Measurements using a single carrier 20 MHz LTE input signal with PAPR of 9.0 dB are used to quantify the DPA's performance for cellular infrastructure applications.





(a) (b)

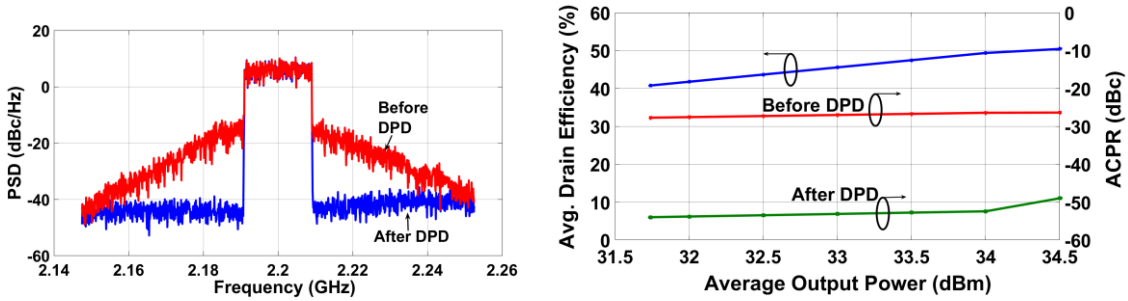
Fig. 3.11: (a) Measured drain efficiency and gain from 2.14-2.25 GHz, (b) Measured performance summary from 2.1-2.3 GHz.

TABLE 3.2

COMPARISON OF EXTENDED EFFICIENCY RANGE DPAS

REF.	TOPOLOGY	FREQ. (GHZ)	P-3 dB (dBm)	OBO (dB)	AVG. DE (%)	ACPR (dBc)	SIGNAL/ BW (MHZ)
[10]	SYMMETRICAL	1.95	44	9.0	55.0	-49	LTE/20
[13]	SYMMETRICAL	2.0	42	9.1	57.4	-23*	WCDMA/ 5
[14]	SYMMETRICAL	2.1	42	9.5	58.0	-47	WCDMA/ 5
[17]	SYMMETRICAL	2.2	45	8.7	47.2	-50.3	LTE/20
[18]	ASYMMETRICAL	1.55	42	8.6	55.0	-50.0	LTE/20
THIS WORK	SYMMETRICAL	2.2	43.6	9.0	50.7	-50.3	LTE/20

* Without DPD



(a) (b)

Fig. 3.12: (a) Normalized PSD before and after DPD correction at 2.2 GHz, and (b) Measured average drain efficiency and ACPR before and after DPD correction at 2.14 GHz.

The DPA achieves an average DE of 50.7% at 2.2 GHz with gain of 9.5 dB at 34.5 dBm of average power and has an adjacent channel power ratio (ACPR) of -24.8 dBc. A generalized memory polynomial based digital pre-distortion (DPD) technique (with order of 9 and nonlinear function of 10 that includes 3 memory taps) is used to linearize the DPA to an ACPR of -50.3 dBc. Fig. 3.12(a) shows the measured normalized power spectral density (PSD) of the DPA before and after applying the DPD. Fig. 3.12(b) shows average

drain efficiency and ACPR before and after DPD correction, as a function of average output power when excited with the 9.0 dB PAPR 20 MHz LTE signal at 2.14 GHz. Table 3.2 summarizes the state-of-the-art extended efficiency range based DPAs.

The presented DPA clearly demonstrates competitive efficiency with excellent linearity performance compared to prior extended efficiency based symmetrical DPAs, and the presented work uses a simpler circuit analysis and design technique.

3.5 Conclusion:

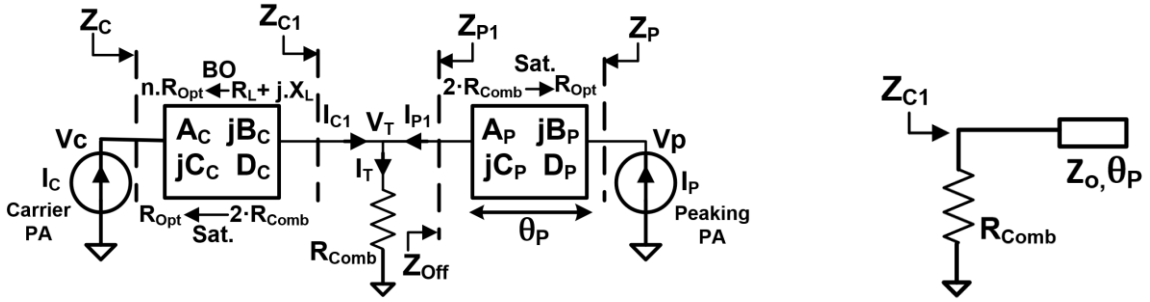
This work presents a new approach to design an extended efficiency range DPA. This approach uses the phasor relationship between the carrier and peaking PAs at the Doherty combining node to extend the dynamic load modulation and achieve efficiency enhancement over wider range of OBO power levels compared to a conventional symmetrical DPA. Closed-form analytical expressions have been derived to design the presented PE-DPA architecture, and the technique has been demonstrated through fabrication and measurement of a GaN-based DPA at 2.2 GHz operating frequency. The DPA demonstrates enhanced efficiency over 9.0 dB OBO with excellent linearity performance, and competitive DE compared to prior state of the art symmetrical DPAs.

CHAPTER – IV

OPTIMIZED LOAD TRAJECTORY FOR FINITE PEAKING OFF-STATE IMPEDANCE BASED DOHERTY POWER AMPLIFIER

4.1 Introduction:

The ability to maintain high efficiency at the back-off (BO) power levels with relatively simpler architecture compared to other load modulated PAs, has made Doherty power amplifier the most commonly used PA for wireless infrastructure application. In a traditional DPA architecture, peaking PA output matching network is designed as such it presents an open circuit at low power region [34]-[35]. However recently, modified DPA architectures were reported [26]-[28] that presents finite peaking output impedance at the low power region which helps to achieve wider dynamic load modulation resulting in efficiency enhancement beyond 6 dB output power back-off (OBO) in a symmetrical DPA configuration.



(a) (b)

Fig. 4.1: (a) Conceptual diagram of a Doherty power amplifier. (b) Impedance seen from the carrier PA at the Doherty combining node.

On the other hand, nonlinear phase distortion (NPD) primarily caused by the variation of the peaking PA's parasitic input capacitance with the input drive, has degrading effect

on the drain efficiency of a DPA as reported in [33]-[34]. In this chapter, closed form equations are derived for the finite peaking off-state impedance based DPA with modified load trajectories for both the carrier and peaking PA to improve the DPA performance at the presence of nonlinear phase distortion.

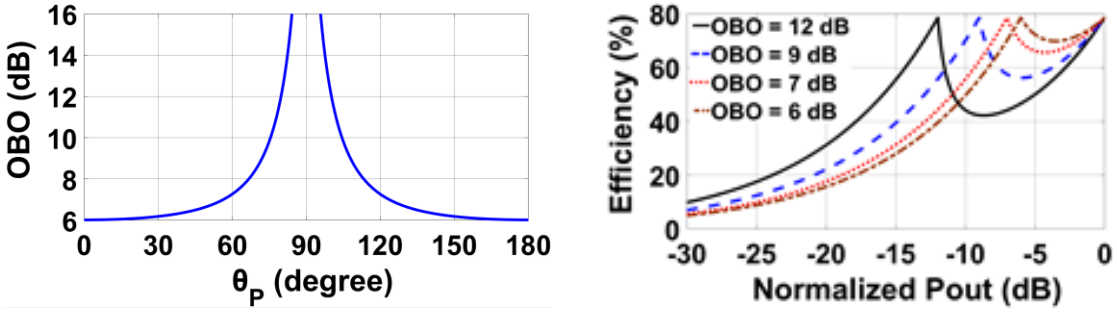
4.2 Theoretical Analysis:

Fig. 4.1(a) shows a generic DPA architecture where carrier and peaking devices are represented by the ideal current sources (I_C and I_P respectively) which does not include any non-idealities. In a conventional DPA, the peaking PA's output matching network (OMN) is designed to present an open circuit so that the impedance seen at the Z_{C1} plane is R_{Comb}. Traditionally there are two different approaches to achieve this high impedance at the Doherty combining node, as shown in [34] and [35]. Fig. 4.1(b) shows the equivalent circuit seen from the Z_{C1} and the effective θ_P is 180º and 0º respectively for the two cases referenced above. However, choosing a θ_P between 0º and 180º moves the BO impedance at Z_{C1} plane away from R_{Comb} as shown in (4.1). But as soon as peaking PA turns on, the impedance seen at the Z_{C1} plane becomes a function of the two currents (I_{C1}, I_{P1}) at the combining node and the effect of θ_P on the Z_{C1} plane impedance fades away. This phenomenon allows for wider load modulation hence efficiency enhancement at larger OBO level for a given ratio of I_C and I_P.

$$Z_{C1,\,BO} = \frac{Z_0 \cdot R_{Comb}}{Z_0 + j \cdot R_{Comb} \cdot \tan(\theta_P)} \tag{4.1}$$

$$Z_{C1,\,SAT} = \left(1 + \frac{I_{P1}}{I_{C1}}\right) \cdot R_{Comb} \tag{4.2}$$

Using (4.1)-(4.2), Fig. 4.2(a) plots OBO versus θ_P for a symmetrical DPA where R_{Comb}=15Ω, Z_0=50Ω, $\Gamma_{C1}=\frac{Z_{C1,SAT}-Z_{C1,BO}}{Z_{C1,SAT}+Z_{C1,BO}}$, $n=\frac{1+|\Gamma_{C1}|}{1-|\Gamma_{C1}|}$ and $OBO = 10\log_{10}(2\cdot n)$. Fig. 4.2 shows that there are two solutions available to achieve same OBO performance. To ensure the proper functioning of the DPA, the carrier OMN and peaking OMN should transform to the required BO and saturation impedance as shown in Fig. 4.1(a) where R_{Opt} is the optimum impedance to generate maximum power from the devices and peaking off-state impedance, $Z_{Off} = -j\cdot Z_0\cdot \cot(\theta_P)$. To satisfy these conditions along with phase coherent combination of the currents (I_{C1}, I_{P1}), required ABCD parameters and phase difference (ϕ_0) between intrinsic device currents (I_C, I_P) are derived and presented in Table I where $R_L = \text{real}(Z_{C1,BO}), X_L = \text{imaginary}(Z_{C1,BO}), X_T = \text{imaginary}(Z_{Off})$. Assuming class B operation for DC power consumption for both the PAs and linear I_C, I_P with respect to input voltage, drain efficiency is plotted in Fig. 4.2(b) for various θ_P ($90^o<\theta_P\leq 180^o$) based on Table-I. Since there are two solutions available, identical plot could be achieved for $0^o\leq\theta_P<90^o$.



(a) (b)

Fig. 4.2: (a) OBO versus θ_P. (b) Efficiency versus normalized output power.

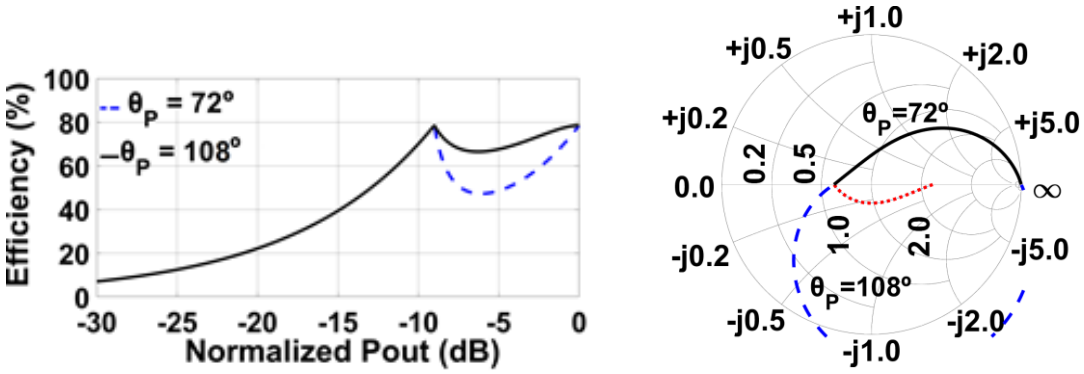
TABLE 4.1

NETWORK PARAMETERS OF THE FINITE OFF-STATE IMPEDANCE BASED DPA

$A_C = Q \cdot B_C;\ \ B_C = 1/[C_C \cdot (1 + [Q \cdot 2 \cdot R_{Comb}]^2)]$
$C_C = \sqrt{\frac{R_L}{n \cdot R_{Opt} \cdot [(Q \cdot [2 \cdot R_{Comb}]^2 - X_L^2) + R_L^2]}};\ D_C = Q \cdot 4 \cdot R_{Comb}^2 . C_C$
$A_P = \frac{-X_T}{C_P \cdot (X_T^2 + [2 \cdot R_{Comb}]^2)};\ B_P = \frac{1}{C_P \cdot (1 + [\frac{X_T}{2 \cdot R_{Comb}}]^2)}$
$C_P = \sqrt{\frac{2 \cdot R_{Comb}}{R_{Opt} \cdot (X_T^2 + [2 \cdot R_{Comb}]^2)}};\ D_P = -X_T \cdot C_P$
$Q = -[\left(1 - \frac{R_L^2 + X_L^2}{[2 \cdot R_{Comb}]^2}\right) - \sqrt{\left(1 - \frac{R_L^2 + X_L^2}{[2 \cdot R_{Comb}]^2}\right)^2 + \left(\frac{X_L^2}{R_{Comb}^2}\right)}]/[2.X_L]$
$\Delta\phi_0 = \arctan(\frac{2 \cdot C_C \cdot R_{Comb}}{D_C}) - \arctan(\frac{2 \cdot C_P \cdot R_{Comb}}{D_P}) - \pi;$
$I_{P1} = \frac{I_P \cdot (D_C + j \cdot C_C \cdot R_{Comb}) - j \cdot C_P \cdot R_{Comb} \cdot I_C}{j \cdot C_P \cdot R_{Comb} \cdot D_C + D_C \cdot D_P + j \cdot D_P \cdot R_{Comb} \cdot C_C};\ I_{C1} = \frac{I_C - j \cdot C_C \cdot R_{Comb} \cdot I_{P1}}{D_C + j \cdot R_{Comb} \cdot C_C}$
$V_C = A_C \cdot R_{Comb} \cdot (I_{C1} + I_{P1}) + j \cdot B_C \cdot I_{C1}$
$V_P = A_P \cdot R_{Comb} \cdot (I_{C1} + I_{P1}) + j \cdot B_P \cdot I_{P1}$

The analysis presented so far does not include the effect of the NPD. To demonstrate the effect of NPD, Fig. 4.3 shows the drain efficiency and load trajectory of the DPA at θ_P of 72º and 108º with 15º of NPD (extracted from a Cree CGH60015D simulation). It is clear from the plots that both θ_P provide second efficiency peak at 9 dB OBO, but θ_P of 108º benefits from the NPD while the θ_P of 72º degrades compare to the nominal case of no NPD. This opposite effect on drain efficiency is observed because higher NPD brings the peaking load trajectory closer to the real axis in smith chart generating less reactive power

and more efficient at θ_P =108º but it becomes more capacitive at θ_P=72º, hence less efficient. Although it is evident from Fig. 4.3 that 90º<θ_P≤180º delivers higher efficiency compared to 0º≤θ_P<90º at the presence of NPD but carrier PA load trajectory moves away from real axis for both the cases causing efficiency degradation. However, it is found from the large signal simulation of the PA device that the NPD is also a function of the carrier PA's load trajectory, it increases as the BO impedance becomes more reactive and less resistive.

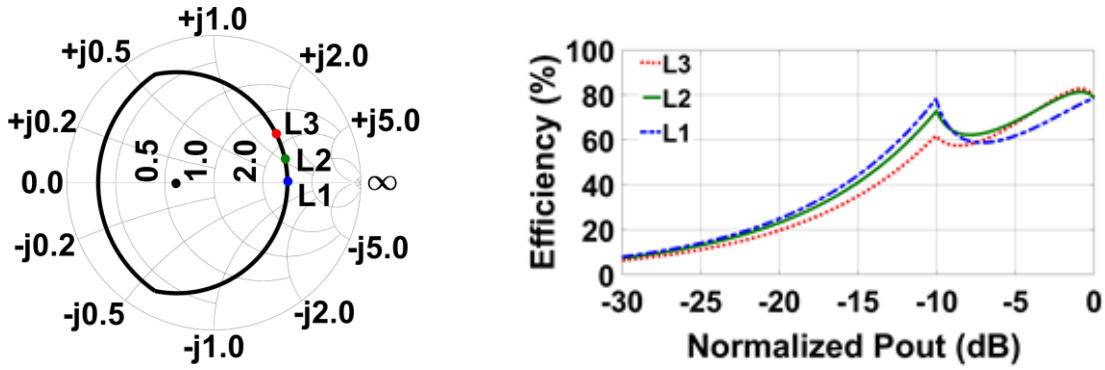


(a) (b)

Fig. 4.3: (a) Drain Efficiency versus normalized output power with NPD and (b) Load Trajectories for θ_P =108 º and θ_P =72 º.

Hence an optimum complex BO impedance, which falls on the device's required BO power contour, would increase the NPD which helps the peaking load trajectory (for 90º<θ_P≤180º) and the carrier load trajectory will also move closer to the real axis instead of moving away from it. Fig. 4.4. plots the ideal load-pull contour at 7 dB BO and corresponding simulated drain efficiency with NPD of 15º, 30º and 40º (Large signal simulation of CGH60015D) for L1, L2 and L3 respectively. It is clear from the plot that the second efficiency peak suffers as load becomes more reactive, however an optimum complex impedance of L2 can deliver higher efficiency in between the efficiency peaks

compared to resistive impedance of L1 with minimum degradation at the BO. Based on the presented analysis, this letter proposes peaking load trajectory with $90^{o}<\theta_{P}\leq 180^{o}$ and optimum complex carrier BO impedance to optimize the DPA performance at the presence of NPD. Table-4.2 presents the modified network parameters of the carrier PA for complex BO impedance of $Z_{C,BO} = R_B + j \cdot X_B$.



(a) (b)

Fig. 4.4: (a) Ideal load-pull contour at 7 dB BO power (b) Drain efficiency for various loads as denoted in the load-pull contour with variable NPD.

TABLE 4.2

MODIFIED NETWORK PARAMETERS OF THE CARRIER PA

$A_C = \frac{R_{Opt} \cdot D_C}{2 \cdot R_{Comb}}; \quad B_C = C_C \cdot 2 \cdot R_{Comb} \cdot R_{Opt};$
$C_C = \sqrt{\frac{(P+R)}{S}}; \qquad D_C = \sqrt{\left[\frac{2 \cdot R_{Comb}}{R_{Opt}}\right] - [C_C \cdot 2 \cdot R_{Comb}]^2};$
$P = \frac{2 \cdot R_{Comb} \cdot X_B \cdot R_L - 2 \cdot R_{Comb} \cdot R_B \cdot X_L}{R_B \cdot R_{Opt} \cdot ([2 \cdot R_{Comb}]^2 - R_L^2 - X_L^2)}; \; R = \frac{R_{Opt} \cdot R_L - 2 \cdot R_{Comb} \cdot R_B}{2 \cdot X_L \cdot R_{Opt} \cdot R_B}$
$S = \frac{R_L^2 - [2 \cdot R_{Comb}]^2}{2 \cdot X_L} - \frac{2 \cdot [2 \cdot R_{Comb}]^2 \cdot X_L}{[2 \cdot R_{Comb}]^2 - R_L^2 - X_L^2};$

4.3 Experimental Validation and Measured Results:

To verify the proposed architecture, a symmetrical DPA at 2.14 GHz is designed for efficiency enhancement at 10 dB OBO using a pair of Cree GaN (CGH60015D) high-electron-mobility (HEMT) bare-die discrete devices integrated on a Rogers 04350B board material. From Fig. 4.2(a), a θ_P of 105° is required to achieve the second efficiency peak at 10 dB OBO. Based on the load-pull simulation data, an R_{Opt} of 30 Ω has been chosen to deliver 41.0 dBm output power for both the carrier and peaking PA. Since the DPA is intended for 10 dB OBO, the resistive BO impedance would be 144Ω at BO power of 34.0 dBm. However, based on the analysis presented in the previous section, a complex impedance of 85 + j·69 Ω is selected as the complex BO impedance to optimize the carrier PA's load trajectory. Both PAs are combined at R_{Comb} of 15 Ω. After all the design parameters (R_{Opt}, R_B, X_B, R_L, X_L, R_{Comb} and θ_P) are defined, ABCD parameters of the OMNs for two DPAs are derived using Table 4.1 and 4.2 where DPA-I and DPA-II are using complex and resistive BO impedance respectively. These ABCD parameter-based networks are then converted to transmission line-based networks using the technique described in [26]. At the OMNs, quarter-wave stubs at 2.14 GHz are used for second harmonic traps. A two-section matching network is used after the Doherty combiner to transform 15Ω to 50Ω. For the input side, a 90° branch-line coupler and input offset line are used for equal power split and phase adjustment to achieve the desired $\Delta\phi_0$. Additionally, single section matching networks are used for impedance matching and gain optimization at the input side. For both DPAs, the carrier and peaking PA drain is biased with 28V. For the gate side, carrier PA is biased at quiescent current of 34 mA, and peaking PA is biased at -6V. Fig. 4.5 shows the schematic diagram of DPA-I, which absorbs the

device's output parasitic capacitance (1.3 pF) into the OMN. Fig. 4.6(a) compares the drain efficiency of carrier and peaking PAs for DPA-I and II. It demonstrates that DPA-I (complex BO impedance) has up to 7% higher carrier PA efficiency while maintaining similar peaking PA efficiency compared to DPA-II, verifying the advantage of the optimized load trajectory for the DPA. Fig. 4.6(b) shows the simulated performance of DPA-I which achieves output power of 43.7 dBm at P3dB from 2.1-2.2 GHz, with drain efficiency better than 45% at 10 dB OBO. The fabricated DPA-I is shown in Fig. 4.7(a).

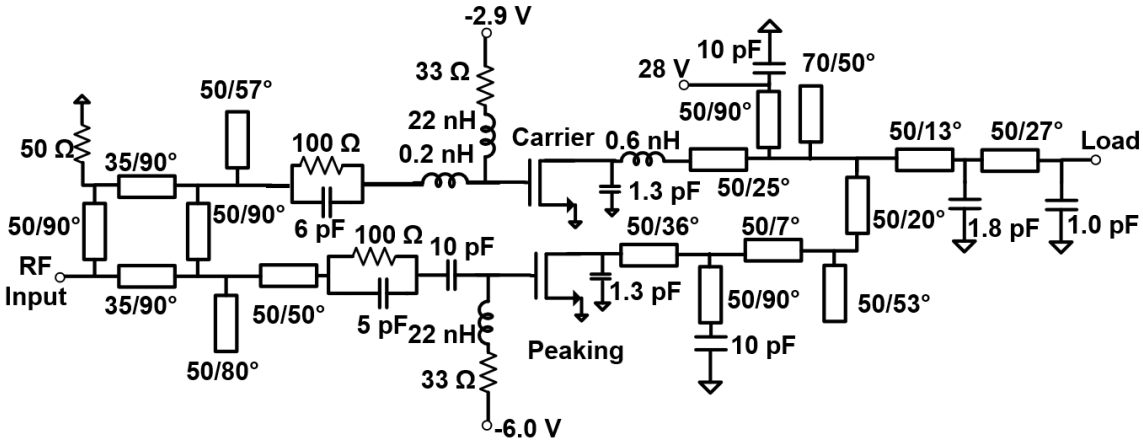
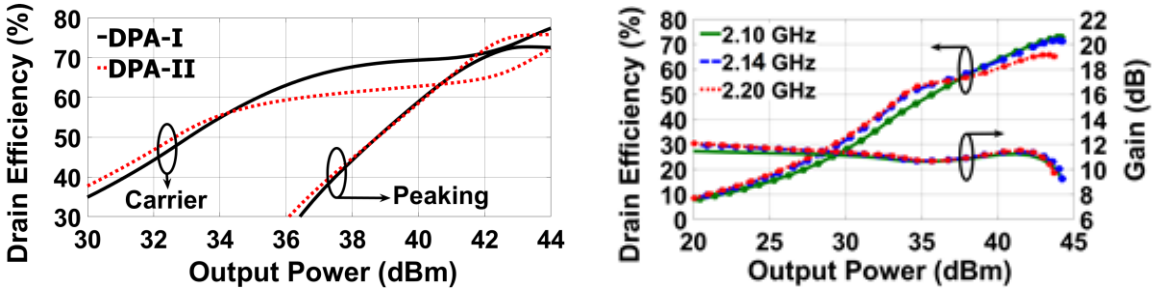


Fig. 4.5: Schematic diagram of DPA-I at 2.14 GHz.



(a) (b)

Fig. 4.6: (a) Simulated comparison of DPA-I and DPA-II. (b) Simulated performance of DPA-I.

The measured DPA's gain and drain efficiency (DE) are plotted as a function of output power under CW excitation in Fig. 4.7(b). At P-3dB within 2.10-2.20 GHz operating frequency range, the DPA exhibits more than 43.0 dBm of output power with DE higher than 48% at 9 dB OBO. Fig. 4.7(c) shows the DE at P-3dB and 9 dB OBO, as well as P3-dB over the 2.05-2.25 GHz range. This plot shows that BO efficiency peaks at 2.2 GHz with P-3dB of 43.0 dBm at 55.5% DE at 9 dB OBO.

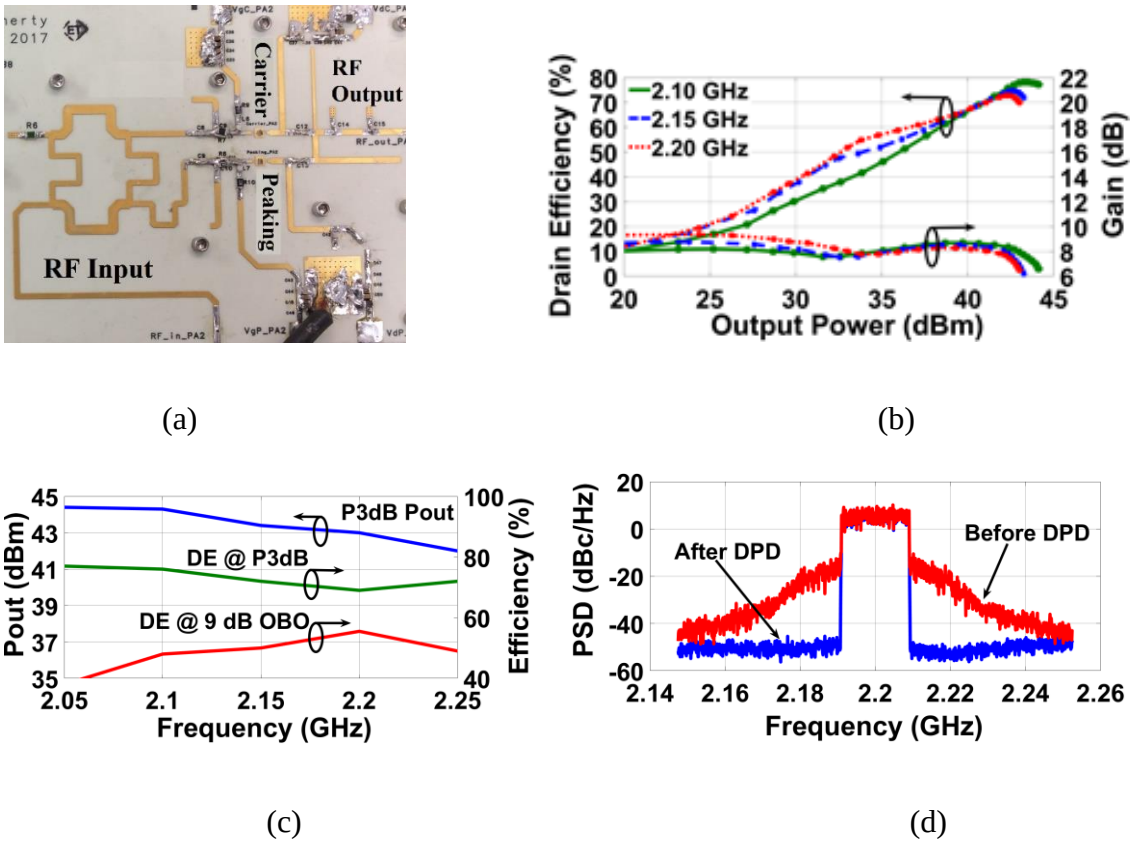


Fig. 4.7: (a) Top view of the assembled DPA. (b) Measured drain efficiency and gain from 2.1-2.2 GHz, (c) Measured performance summary from 2.05-2.25 GHz, (d) Normalized PSD before and after DPD correction.

Measurements using a single carrier 20 MHz LTE input signal with PAPR of 9.0 dB are used to quantify the DPA's performance for cellular infrastructure applications. The DPA

achieves an average DE of 55.5% at 2.2 GHz with gain of 9.0 dB at 34.0 dBm of average power and has an ACPR of -27 dBc. A generalized memory polynomial based digital pre-distortion (DPD) technique (with order of 9 and nonlinear function of 10 that includes 3 memory taps) is used to linearize the DPA to an ACPR of -56 dBc. Fig. 4.7(d) shows the measured normalized power spectral density (PSD) of the DPA before and after applying the DPD. Table 4.3 summarizes the state-of-the-art finite peaking off-state based DPAs. The presented DPA clearly demonstrates excellent efficiency and linearity performance compared to prior DPAs.

TABLE 4.3

COMPARISON OF EXTENDED EFFICIENCY RANGE SYMMETRICAL DPAS

REF.	FREQ. (GHZ)	P-3 dB (dBm)	OBO (dB)	AVG. DE (%)	ACPR (dBc)	SIGNAL/ BW (MHZ)
[26]	1.95	44	9.0	55	-49	LTE/20
[30]	2.1	42	9.5	58	-47	WCDMA/5
[31]	2.2	45	8.7	47.2	-50.3	LTE/20
THIS WORK	2.2	43.0	9.0	55.5	-56	LTE/20

4.4 Conclusion:

An optimized load trajectory for carrier and peaking PA has been proposed in this letter for finite peaking off-state impedance based DPA. Theoretical analysis and large signal simulation predicted superior performance than traditional design methodology.

Advantage of the proposed technique has been verified through design and measurement of a GaN-based DPA at 2.2 GHz which demonstrates excellent efficiency and linearity performance over 9.0 dB OBO.

CHAPTER – V

SUMMARY AND FUTURE WORK

5.1 Summary of the Works:

This dissertation has investigated three different types of advanced symmetrical Doherty PA architecture. Primary objective of this investigation, is to extend the load modulation compared to traditional 6 dB OBO using symmetrical devices for the carrier and peaking PA. First design is a varactor-based Doherty PA which uses an anti-series bank of abrupt tuning based varactor diodes at the output matching network of the carrier PA. The varactor voltage is controlled as a function of the input drive level to add an additional load modulating functionality to widen the overall load modulation to achieve efficiency enhancement up to 10 dB OBO. Simulation results show promising BO efficiency which is better than 50% at 10 dB OBO at operating frequency range of 1.6-2.2 GHz. However, the high insertion loss and poor modelling of the varactor diodes caused significant degradation at BO efficiency in the desired frequency range.

Since the varactor-based Doherty PA needed an additional control voltage and introduced significant insertion loss at the output combiner, next Doherty architecture presented in this dissertation, aims to achieve wider load modulation without introducing any such lossy component. This has been achieved by utilizing the combining phase of the two currents at the Doherty combining node. It has been shown through rigorous theoretical analysis that the phase of the two currents at the Doherty combining node can be intentionally kept out of phase to achieve load modulation greater than traditional 2:1. This proposed idea has been validated through the design, fabrication and measurement of a

GaN based Doherty PA which measured drain efficiency of 51% at 9 dB OBO with linearized ACPR of -50.3 dBc at 2.2 GHz using symmetrical carrier and peaking devices.

Finally, this research work proposes an optimized load trajectory for the carrier and peaking PA for a finite peaking off-state impedance-based Doherty architecture. It has been demonstrated through theoretical analysis and large signal simulation that the carrier PA and peaking PA's load trajectories could be modified compared to more conventional design to incorporate the effect of nonlinear phase distortion to enhance the BO efficiency. To validate this design methodology, a GaN based Doherty PA is designed using symmetrical devices, which delivered P-3dB output power of 43 dBm with average efficiency of 55.5% with linearized ACPR of -56 dBc when excited with a LTE 20 MHz 9.0 dB PAPR based signal at 2.2 GHz. This PA demonstrated excellent BO efficiency and linearity compared to prior state-of-the art PAs.

5.2 Future Work:

This research work solely focused on improving the BO efficiency of the symmetrical Doherty PAs. However, with the advancement of the newer cellular technologies, the instantaneous bandwidth of the high PAPR based modulated signal has become wider. All of the presented work focused improving the RF performance with a narrow band 20 MHz LTE signal. A good investigation would be to evaluate the potential of these architectures and modify the networks to accommodate signal bandwidths of 200-400 MHz and still maintain competitive BO efficiency.

REFERENCES

[1] F. H. Raab and D. J. Rupp, "High efficiency single-sideband HF/VHF transmitter based upon envelope elimination and restoration," *Proc. Sixth Int. Conf. HF Radio Systems and Techniques*, York, UK, pp. 21-25, July 4-7, 1994.

[2] A. A. M. Saleh and D.C. Cox, "Improving the power-added efficiency of FET amplifiers operating with varying envelope signals," *IEEE Trans. Microwave Therory Tech*, vol. 31, no. 1, pp. 51-55, Jan, 1983.

[3] F.H. Raab, "Efficiency of Doherty RF-power amplifier systems," *IEEE Trans. Broadcasting*, vol. BC-33, no.3, pp. 77-83, Sept, 1987.

[4] T. Johansson, J. Fritzin, "A Review of Watt-level CMOS RF Power Amplifiers," *IEEE Trans. Microwave Therory Tech*, vol. 62, no. 1, pp. 111-124, Jan, 2014.

[5] J. Staudinger, "EEE 598: RF Transmitters and Amplifiers", Class lectures, Fall 2014, Arizona State University.

[6] M. Iwamoto, A. Williams, P. Chen, A. G. Metzger, L. E. Larson, and P.M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," IEEE Trans. Microwave Theory Tech., vol. 49, no. 12, pp. 2472–2479, Dec. 2001.

[7] J.-Y. Lee, J.-Y. Kim, J.-H. Kim, K.-J. Cho, and S. Stapleton, "A High Power Asymmetric Doherty Amplifier with Improved Linear Dynamic Range," in IEEE MTT-S Int. Dig., pp. 1348–1351, 11-16 June 2006.

[8] Y.S. Lee, M. W. Lee, and Y. H. Jeong, "Unequal-cells-based GaN HEMT Doherty amplifier with an extended efficiency range," IEEE Microw. Wireless Compon. Lett., vol. 18, no. 8, pp. 536–538, Aug. 2008.

[9] A. Grebennikov, N.O. Sokal and M.J. Franco, "*Switchmode RF and Microwave Power Amplifiers*", Academic Press, Waltham, MA, USA, 2012.

[10] W.C. E. Neo, J. Qureshi, M. J. Pelk, J. R. Gajadharsing, and L. C. N. de Vreede, "A mixed-signal approach towards linear and efficient N-way Doherty amplifiers," IEEE Trans. Microw. Theory Techn., vol. 55, no. 5, pp. 866–879, May 2007.

[11] M.J. Pelk, W. C. E. Neo, J. R. Gajadharsing, R. S. Pengelly, and L. C. N. de Vreede, "A high-efficiency 100-W GaN three-way Doherty amplifier for base-station applications," IEEE Trans. Microwave Theory Tech., vol. 56, no. 7, pp. 1582–1591, July 2008.

[12] N. Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Laskar, “Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications,” IEEE Trans. Microw. Theory Tech., vol. 53, no. 3, pp. 852–860, Mar. 2005.

[13] R. Darraji and F. M. Ghannouchi, ‘‘Digital Doherty amplifier with enhanced efficiency and extended range,’’ IEEE Trans. Microw. Theory Techn., vol. 59, no. 11, pp. 2898–2909, Nov. 2011.

[14] R. Darraji, F.M. Ghannouchi, and O. Hammi, “A dual-input digitally driven Doherty amplifier architecture for performance enhancement of Doherty transmitters,” IEEE Trans. Microw. Theory Tech., Vol. 59, no. 3, Apr. 2011.

[15] L. Piazzon, P. Colantonio, F. Giannini, and R. Giofre, “Asymmetrical ´ doherty power architecture with an integrated driver stage in the auxiliary branch,” Int. J. of RF and Microwave Computer-Aided Engineering, vol. 24, no. 4, pp. 498–507, 2014.

[16] C. M. Andersson, D. Gustafsson, K. Yamanaka, E. Kuwata, H. Otsuka, M. Nakayama, Y. Hirano, I. Angelov, C. Fager, and N. Rorsman, “Theory and design of class-J power amplifiers with dynamic load modulation,” IEEE Trans. Microw. Theory Tech., vol. 60, no. 12, pp. 3778–3786, Dec. 2012.

[17] “A Class-J Power Amplifier with Varactor Based Dynamic Load Modulation”, Master’s thesis in Wireless, Photonics and Space Engineering, William Hallberg, Chalmers University of Technology, 2014.

[18] K. Buisman, L.C.N. de Vreede, L.E. Larson, M. Spirito, A. Akhnoukh, T.L.M. Scholtes, and L.K. Nanver, “Distortion Free Varactor Diode Topologies for RF Adaptivity,” IEEE MTT International Microwave Symposium, 2005.

[19] R. Quaglia, V. Camarchia, C.M. Andersson, M. Pirola, C. Fager and D. Kuylenstierna, “Design and characterization of SiC varactor-based phase shifters”, IEEE MTT European Micowave Integrated Circuits Conference, , Oct 2012.

[20] Macom MTV 90 V High Voltage Si Varactor Datasheet.

[21] “CGH60015D 15 W, 6.0 GHz, GaN HEMT Die Datasheet”, Wolfspeed, Cree.

[22] Sanchez-Perez, M. Ozen, C.M. Andersson, D. Kuylenstierna, N. Rorsman and C. Fager, “Optimized Design of a Dual-Band Power Amplifier With SiC Varactor-Based Dynamic Load Modulation,” IEEE Trans. Microwave Theory Tech., vol.63, no.8, pp.2579-2588, 2015.

[23] K. Chen and D. Peroulis, “Design of adaptive highly efficient GaN power amplifier for octave-bandwidth application and dynamic load modulation,” IEEE Trans. Microw. Theory Techn., vol. 60, no. 6, pp. 1829–1839, Jun. 2012.

[24] R. Amirpour, R. Darraji, F. Ghannouchi and R. Quay, “Enhancement of the Broadband Efficiency of a Class-J Power Amplifier With Varactorbased Dynamic Load Modulation,” IEEE Microw. Wireless Compon. Lett., vol. 27, no. 2, pp. 180–182, Feb. 2017.

[25] W. Hallberg, D. Gustafsson, M. Ozen, et al, “A Class-J Power Amplifier with Varactor-based Dynamic Load Modulation across a Large Bandwidth,” 2015 IEEE MTT-S Int. Microwave Symp. Dig., pp. 1–4, May. 2015.

[26] M. Özen, K. Andersson, and C. Fager, “Symmetrical Doherty power amplifier with extended efficiency range,” IEEE Trans. Microw. Theory Techn., vol. 64, no. 4, pp. 1273–1284, Apr. 2016.

[27] W.Hallberg, M. Özen, D. Gustafsson, K. Buisman, and C. Fager, “A Doherty power amplifier design method for improved efficiency and linearity,” IEEE Trans. Microw. Theory Techn., vol. 64, no. 12, pp. 4491–4504, Dec. 2016.

[28] M. Özen and C. Fager, “Symmetrical Doherty amplifier with high efficiency over large output power dynamic range,” in IEEE MTT-S Int. Microw. Symp. Dig., Jun. 2014, pp. 1–4.

[29] X. H. Fang and K.-K. M. Cheng, “Extension of high-efficiency range of Doherty amplifier by using complex combining load,” IEEE Trans. Microw. Theory Techn., vol. 62, no. 9, pp. 2038–2047, Sep. 2014.

[30] X.H.Fang, H.-Y Liu and K.-K. M. Cheng, “Extended efficiency range, equal-cell Doherty Amplifier design using explicit circuit model”, IEEE Microw. Wireless Compon. Lett., vol. 27, no. 5, pp. 497–499, May 2017.

[31] W.Shi, S.He, N. Gideon, “Extending high-efficiency power range of symmetrical Doherty power amplifiers by taking advantage of peaking stage” IET Microwaves, Antennas and Propagation, vol. 11, no. 9, pp. 1296–1302, July 2017.

[32] S. Kim, J. Moon, J. Lee, Y. Park, D. Minn, and B. Kim, “Mitigating phase variation of peaking amplifier using offset line,” IEEE Microw. Wireless Compon. Lett., vol. 26, no. 2, pp. 149–151, Feb. 2016.

[33] S. Kim, J. Moon, J. Lee, Y. Park, D. Minn, and B. Kim, “Accurate offset line design of Doherty amplifier with compensation of peaking amplifier phase variation,” IEEE Trans. Microw. Theory Techn., vol. 64, no. 10, pp. 3224–3231, Oct. 2016.

[34] M. Akbarpour, M. Helaoui, and F. M. Ghannouchi, “A transformer-less load-modulated (TLLM) architecture for efficient wideband power amplifiers,” IEEE Trans. Microw. Theory Tech., vol. 60, no. 9, pp. 2863- 2874, Sep. 2012.

[35] D.Y. Wu, and S. Boumaiza, “A modified Doherty configuration for broadband amplification using symmetrical devices,” IEEE Trans. Microw. Theory Techn., vol. 60, no. 10, pp. 3201-3213, Oct. 2012.