Characterization of Electrically Active Defects at Nb/Si Interface Using Current Transport and Transient Capacitance Measurements

by

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ABSTRACT

In this project, current-voltage (I-V) and Deep Level Transient Spectroscopy (DLTS) measurements are used to (a) characterize the electrical properties of Nb/p-type Si Schottky barriers, (b) identify the concentration and physical character of the electrically active defects present in the depletion region, and (c) use thermal processing to reduce the concentration or eliminate the defects. Barrier height determinations using temperature-dependent I-V measurements indicate that the barrier height decreases from 0.50 eV to 0.48 eV for anneals above 200 C. The electrically-active defect concentration measured using DLTS (deep level transient spectroscopy) drops markedly after anneals at 250 C.

A significant increase in leakage currents is almost always observed in near-ideal devices upon annealing. In contrast, non-ideal devices dominated by leakage currents annealed at 150 C to 250 C exhibit a significant decrease in such currents.

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CHAPTER 1 INTRODUCTION

There has been an increased interest in devices containing semiconductor-superconductor interfaces in recent years. Examples include mixers, detectors, quantum computing and information, and superconducting Josephson Junction circuits [1].

Defects in the band gap of the semiconductor in the active region of the device affect the system's performance [2]. Thus, the choice of material, and methods used to prepare the interface and nearby surfaces of the devices play an important role in device and system optimization. [3]. For this reason, the investigation of such systems has recently taken on a new urgency.

1.1 Defects

Every material contains defects; perfect materials simply do not exist. While it may cost enthalpic energy to create a defect, configurational entropy renders it favorable to incorporate defects as a result of a reduced free energy [4]. Therefore, even in equilibrium we can expect defects to be present; kinetic limitations sometimes lead to formation of additional defects and these dominate in the structures that we will be studying[4].

Since defects are unavoidable, we must consider the effects they have on material properties. Point defects affect the physical and chemical properties of semiconductors [4]. If a defect level in the bandgap is likely to be thermally ionized at room temperature, it is conventionally referred to as a shallow level [2,4,6]. Otherwise, it is called a deep level. Electrically active deep-level defects can act as recombination centers or generation centers [2,4,5]. Compensation by native or impurity point defects can decrease the doping

concentration [2,4]. The creation and diffusion of defects during device operation can cause device degradations.

1.2 The Nb/Si interface

The design of a high-quality super Schottky contact is strongly dependent on the materials used [3]. Transition metals in silicon can have different charged states within the band gap and can strongly degrade the device properties of devices [7,8]. Although the data base available for transition metals in silicon is quite large, there are still many transition metals in silicon that have not been adequately characterized [8]. Niobium is one such metal. For this material, there is little information in the literature on niobium-containing defects and what is available is contradictory [8,9].

For the work reported here, we will provide a comprehensive description of (a) the electrical characteristics of Nb/Si Schottky barriers, (b) the properties of the electrically active defects, and (c) methods that can reduce the concentration of electrically active defects.

CHAPTER 2 BACKGROUND

2.1 Schottky Contact/Barrier

Metal/semiconductor contacts that exhibit electrical rectification are called Schottky Barriers. The presence of a potential barrier in the semiconductor to electrons, for n-type material, or holes, for p-type materials is responsible for the rectifying behavior. Mott Theory states that the diffusion potential in the depletion region is equal to the difference between the metal work function and the electron affinity of the semiconductor [10]. The dominant role of surface states in determining the diffusion potential and thus the Schottky barrier height was later described in a model by Bardeen [10, 11].

The electrostatics of a Schottky barrier can be best illustrated with the aid of figure 1. In case (a), the metal and n-type semiconductor are electrically neutral and are not in contact with each other. Assuming absence of surface states, the energy band diagram is show in figure 1 (a). When the metal and semiconductor are connected electrically by means of a wire, electrons flow from the semiconductor into the metal, causing the two fermi levels to align, as seen in figure 1 (b). There is an energy imbalance between the electrons at rest on the two surfaces. Each negative charge on the metal surface is balanced by a positive charge in the semiconductor. For an n-type semiconductor, the positive charge is provided by the electrons withdrawing from the surface, leaving behind positive donor ions in the depletion region. The uncompensated donor ions occupy a width of region comparable to the depletion region in a p-n junction, with the bands bent upwards as seen in figure 1 (b). The difference between the electrostatic potential between the outside of the semiconductor and the metal is given by $V_i = \delta\varepsilon_i$, where δ is the separation and ε_i is the

field gap. As the metal and semiconductor tend to approach each other V_i tends to zero for constant ε_i. When they meet each other the barrier due to vacuum is dispersed leaving behind an idealized metal semiconductor contact i.e. a junction without interface states [5,10]. This has never been realized, to our knowledge.

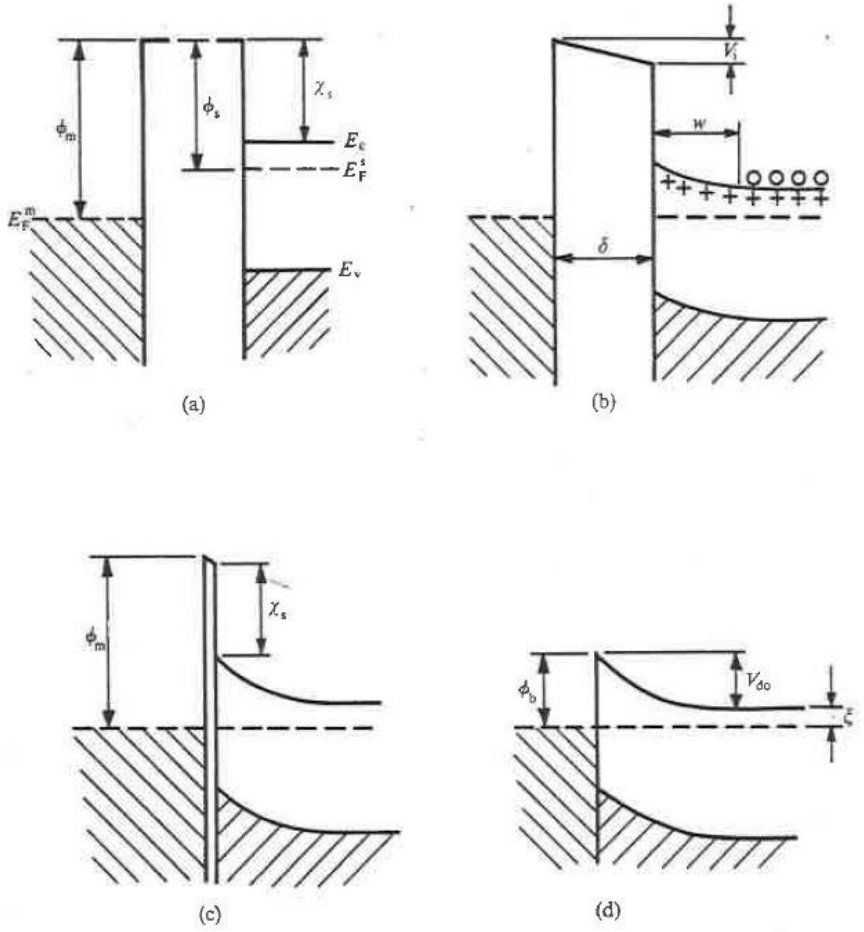

Figure 1. Potential energy diagrams illustrating the formation of a electrostatic barrier between metal and semiconductor (a) neutral and isolated, (b) electrically connected, (c) separated by narrow gap, (d) in perfect contact [10]

2.2 Current Transport Process

Current transport in Schottky contacts are mainly due to majority carriers. The current transport is dominated by one or more of the following 5 processes, namely, 1.

Thermionic emission 2. Quantum mechanical tunneling of electrons, 3. Recombination, and 4. Carrier diffusion. [5,10]

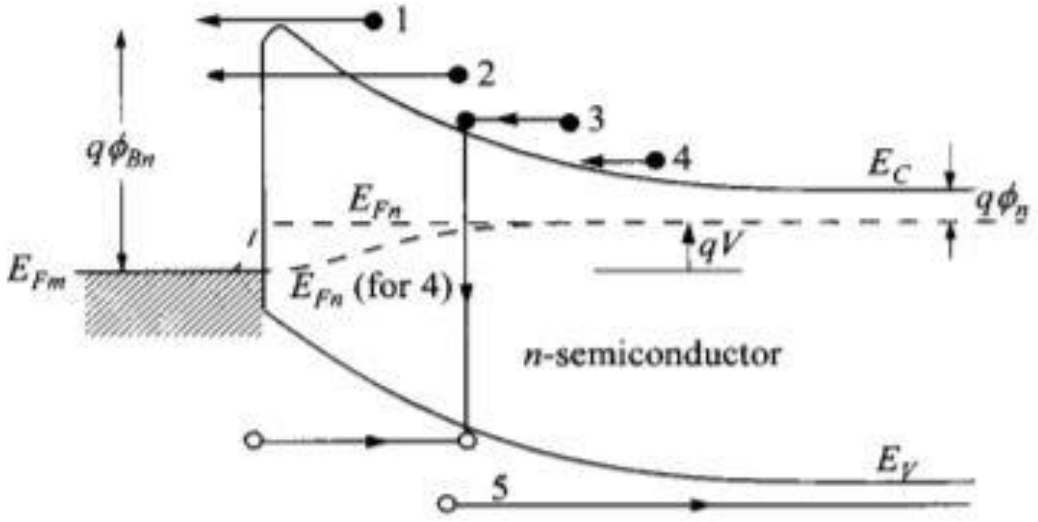

Figure 2. The five basic processes of current transport 1. Thermionic emission, 2. Quantum mechanical tunneling of electrons, 3. Recombination, 4. Diffusion of electrons and 5. Diffusion of holes [5].

2.3 Thermionic emission:

Thermionic emission occurs when carriers with high thermal energy exceeds the barrier height, causing flow of charges over a potential energy barrier.

Assuming the barrier height is much larger than *kT*. The thermionic emission current is characterized with the following equation:

$$I = AA^*T^2e^{-\frac{q\emptyset_b}{kT}}(e^{\frac{qV}{nkT}} - 1)$$

Where, I is the current, A is the area of the device, A^* is the Richardson constant, T is the temperature, q is the charge, ϕ_b is the barrier height, k is Planck's constant, V is the applied voltage and n is the ideality factor [2,5,10,11].

In near-ideal devices measured in this study, thermionic emission dominated at biases starting at 0.1 eV and ending at about half the barrier height. For the non-ideal devices, thermionic emission typically dominated only at near half the barrier height. Above that voltage, the voltage drop across the series resistance became significant.

2.4 Deep Level Defects

Defects are an inherent part of any material system. Defects can be introduced intentionally or unintentionally. They can form during the synthesis of the semiconductor, during the formation of the Schottky barrier, or at any other time before or after such processes [2,4,5]. Any deviation from the perfect crystal lattice such as lattice defect (vacancy, self-interstitial), intentionally and unintentionally introduced impurities or defect complexes may create electrically-active levels in the bandgap [2,6,12]

The defects in the semiconductor determine the conduction type (n or p). For almost all practical applications, shallow impurity atoms are intentionally introduced in the crystal to dope the crystals to make it n- or p-type with the desired carrier concentration. The Fermi-level, and the conductivity of a given semiconductor material are determined by the temperature and by the concentration, location and energy of the defect levels [2,4,12].

The deep levels are, as the name indicates, located deeper in the forbidden band. Though their concentration is usually five to six orders of magnitude lower than the dopants in active devices [2,5], they play a vital role in determining the above-mentioned parameters and the recombination lifetime [2]. If the deep level can emit and/or capture both electrons and holes during normal operation, the level is called a recombination center [2,4,6]. Deep level centers often increase the probability of the recombination process and

hence reduce the recombination lifetime [6,12]. If the deep level can emit or capture only one of the carriers, then the level is referred to as a hole or an electron trap [6].

2.5 The Emission and Capture Process

One of the fundamental ways of investigating the electrically active impurities is the measurement of the thermal emission or trapping of charge carriers. The emission and the capture processes have the same probability in thermal equilibrium, which is given by [6]:

$$e_n = \frac{V_{th}\sigma_n N_c}{g_n}\ e^{-(E_c - E_T)/kT}$$

where e_n is the probability of the deep level emitting electrons to the conduction band, σ_n is the capture cross section, E_T is the energy of the deep level or the activation energy.

Assuming a degeneracy factor of 1 and accounting for the free carrier concentration, the equation can be reduced to:

$$e_n = V_{th}\sigma_n n\ e^{-\frac{E_F - E_T}{kT}}$$

where $n = N_C\ e^{-\frac{E_C - E_F}{kT}}$

The transient results from the emission and the capture processes. Each of these processes can be characterized with a time constant. The values of the two-time constants determine the velocity, the ratio of them determines the direction of the resulting transient.

$$\tau_e = 1/e_n$$

where τ_e is the rate of emission.

The capture time constant is:

$$\tau_c = \frac{1}{V_{th}\sigma_n n}$$

2.6 Deep Level Transient Spectroscopy (DLTS)

2.6.1 Principle

In DLTS, the space charge region (scr) serves as the detector in the DLTS measurement [2,6,12,13]. The scr can be in a reverse biased metal-semiconductor junction (e.g. Schottky diode), a pn junction or a MOS capacitor. Considering an n-type Schottky barrier with a semiconductor having a shallow donor dopant and a deep level that acts as an electron trap. Under reverse biased condition, there is a relatively wide scr in the semiconductor near the surface, as shown in figure 3a. The barrier height, the applied voltage, the charge on the metal contact and the shallow level concentration determine the width of the scr region [6,12] . Assuming a homogenous distribution of the donor level: At the beginning the junction is reverse biased so the deep level below the Fermi level (x>LR) is completely filled and it is practically empty above the Fermi level (x<LR), as shown in figure 3 a. Then a positive pulse reduces the reverse bias, causing a decreased scr width as shown in figure 3b. During this excitation pulse, also called the filling pulse, deep levels which are brought below the Fermi level (LP<x< LR) can be filled by electrons from the conduction band (capture process) [2,6]. On removal of the filling pulse and the restoration of the original applied reverse bias conditions, the width of the scr is larger than at that time as result of the newly-formed filled traps [figure 3 c] [2,6]. The negative charge of the captured electrons is compensated for by the positive charge of the localized donor ions in the L(t)-LR region of the scr [6]. While the deep level is emitting the electrons to the

conduction band (LP <x<L(t)), the width of the scr is returning to its original value via the emission process [2,6].

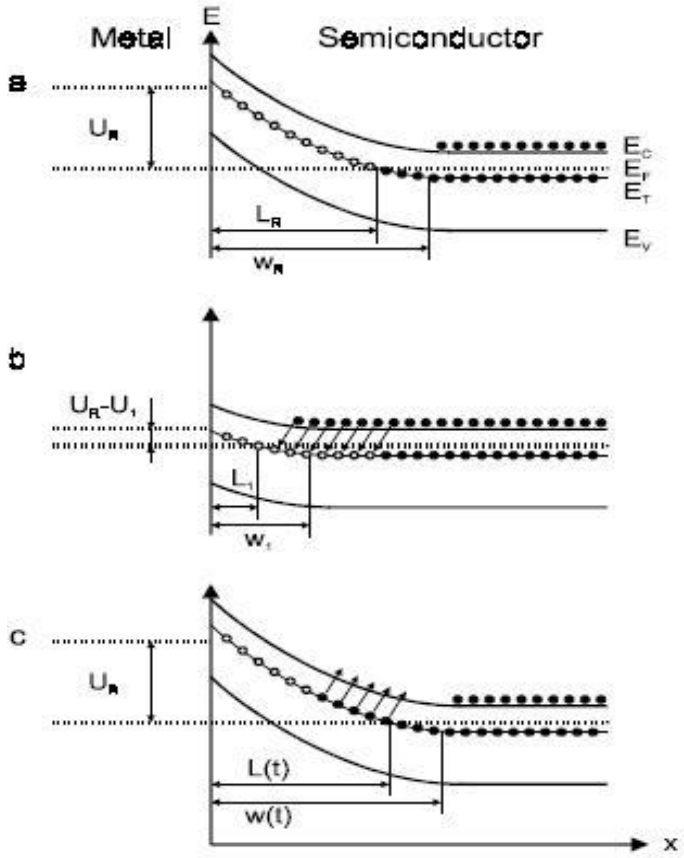

Figure 3. Defect occupation in a Schottky barrier before the filling pulse (a), during the filling pulse (b), just after the filling pulse (c) [6]

The capacitance of the Schottky diode is inversely proportional to the scr width, hence the changes in the space-charge width can be detected as a capacitance transient [figure 4] [6]. It is assumed that the scr width instantaneously follows the change in the charge within the scr. Note that the relaxation time of the scr is much less than the filling pulse [6].

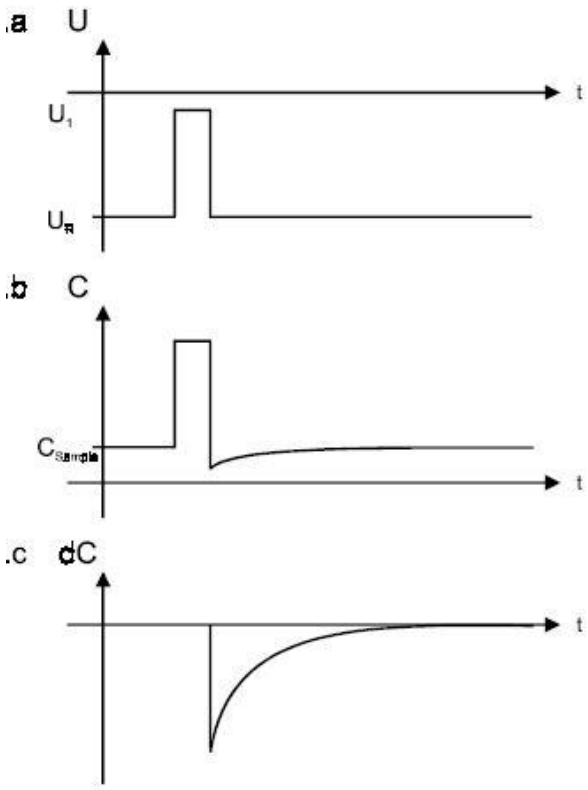

Figure 4. Applied voltage (a), capacitance (b), magnified transient (c) used during a DLTS measurement [6]

2.6.2 Arrhenius Plot

Activation energy (E_{act}) and capture cross section (σ) determination

The spectrum measured during a DLTS temperature scan plots the change in DLS (Deep level signal) as a function of temperature.

For temperature scans, the frequency is maintained at a constant value and the temperature is varied. When evaluating a measured spectrum, the amplitude, the position and the shape of the peaks are determined. It is sufficient to only determine the amplitude and the position of the peaks, as the shape of the peaks does not typically change markedly [2,6,13]. After performing and evaluating several measurements with different frequencies, frequency-temperature data pairs belonging to each peak are compiled. The obtained f-T

i.e. (en-T) data pairs can be illustrated according to the equation below, which is the logarithmic form of the expression of the emission rate [6,13]. The emission is on the Y axis, 1/T is on the X axis (K is a constant).

$$\ln(e_n/T^2) = \ln(K\,\sigma_n) - E_{act}/kT$$

The resulting line is the Arrhenius plot whose slope provides the activation energy of the defect and the abscissa (Y intercept at zero inverse temperature) provides the capture cross section [6]. The activation energy and the capture cross section are calculated from an Arrhenius Plot, the concentration of the level is determined from the amplitude of the peak [6]. Using this procedure, DLTS can determine three defect parameters: the activation energy, the capture cross section and the concentration of the level [2,13].

CHAPTER 3 SAMPLE PREPARATION AND MEASUREMENTS

P-type silicon was chosen as the semiconductor since low-resistance contacts can be readily formed without the need for advanced processing methods (i.e. ion implantation and annealing). For the metal, niobium was chosen for the metal since it is the most common superconductor used in low-temperature superconducting electronic devices [14]. Schottky barriers formed on an epitaxial layer with 7 x 10^{17} /cm^3 deposited on an n+ substrate would be expected to form high quality diodes. The doping level of the epilayer ensures that tunneling does not dominate the transport in the Schottky barrier, while there is sufficient doping in the epilayer and the n+ silicon substrate to have a very low series resistance from the neutral regions of the semiconductor.

Sample requirements for DLTS:

- Presence of a space charge region, that is any diode or junction.
- Sample/ junction capacitance of 10 pF ~ 100 pF
- Good ohmic contact with low series resistance (<100 Ω)
- Low reverse leakage currents of 100 μA or lesser

3.1 Schottky contact

The Schottky contacts were obtained by sputter deposition of niobium on boron doped p-type silicon. The substrates were first cleaned in an ultra-sonic bath of acetone, followed by ethanol. HF etch was then performed on the substrates to get rid of oxide layer. The substrates were then introduced into an ultra-high vacuum chamber with a base

pressure of ~$5x10^{-9}$ Torr. Ion milling was performed on the substrates prior to sputter deposition to obtain a clean interface.

3.2 Ohmic Contact

After the Schottky contact deposition, Ohmic contacts on the back side of the Si substrate are formed by scratching the semiconductor surface with a diamond pen, followed by pressing of indium onto the same area. The substrate is then cleaned with ethanol and the indium is brought into contact with the tip of a 450 C solder gun for about 30 seconds. The resulting ohmic contacts exhibit a series resistance of less than 10 Ω.

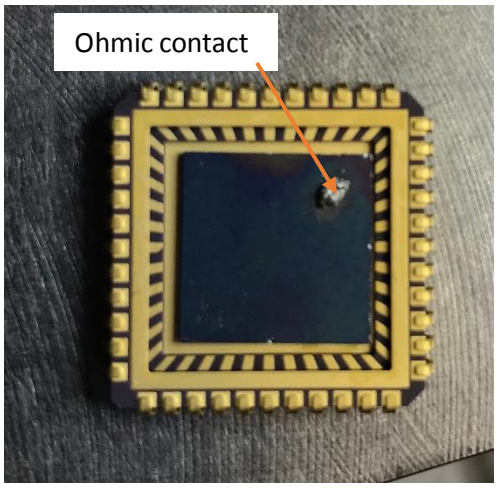

Figure 5. Picture of chip carrier, semiconductor and ohmic contact made to the back of the substrate.

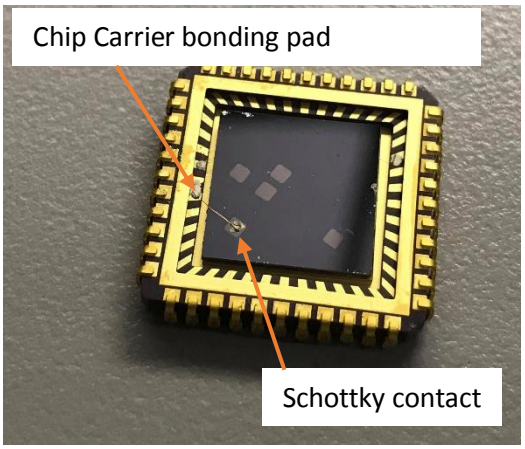

Figure 6. Picture illustrating the sample mounted in the chip carrier.

3.3 Measurement Procedure

In the measurement described below, the Schottky contact (Nb/Si) is connected to the negative terminal and the ohmic contact (indium) is connected to the positive terminal of the source.

The Current-Voltage (I-V) characteristics measurements were carried out using a HP4140B pico-Ammeter DC voltage source. The I-V characteristics of the sample are first measured at intervals of 50 K starting from ~300 K till 50 K. The barrier height and ideality factor of the device under test are determined.

Devices with

- ideality factors of 1.02 – 1.20 at 200 K are studied further,
- very high series/contact resistance are not studied further, and
- very high reverse leakage currents are also not studied further (>100μA).

Capacitance- Voltage (C-V) measurements are performed next, to determine the barrier heights for comparison to those obtained with I-V measurements and to infer the

semiconductor carrier concentration. Devices with capacitances less than 15 pF are omitted from further measurements.

Semilab DLS 83D instrument is used to perform DLTS on devices which satisfy the above criteria.

Similar electrical connection configuration is used for DLTS as for I-V and C-V measurements.

Procedure to operate the DLS 83D to perform DLTS measurements:

- Switch on the main power of the DLS-83 main unit. About 30 min. warm-up time is recommended before performing measurements.
- Switch on the main power of the temperature controller.
- Switch on the main power of the computer and the monitor.
- Start the DLS-83 Operating Software (DLS83.bat or DLS83.exe). The main window appears where you can choose the operation mode you need and set the temperature controller.
- Select the appropriate temperature controller.
- Select the temperature scan operating mode either by pressing its button.
- Initialize the system either by activating the Measure/ Initialize menu command or by pressing the button at the upper left corner of the bottom window.
- Put the sample on the sample holder and connect.

- Close the sample holder
- Press comp button to compensate for sample capacitance.
- Set reverse bias (U_R) to appropriate reverse bias voltage (in our case -1.00 V)
- Set the appropriate positive pulse voltage (in our case 1.10 V)
- Set the appropriate pulse width, determined to be 20 μs for Nb. [8]
- Set the required frequency and start measurement.
- Warm up the stage to room temperature on completion of measurement.
- Smooth the curve and fit it to detect peaks.
- Save data and initiate new measurement.
- Set the next frequency and repeat for desired number of curves on DLTS spectra.

On completion of all measurements for the device, a graph of the DLTS spectrum [6] is plotted by the system's commercial software. Press the view Arrhenius Plot option to obtain the Arrhenius plot for the device which displays the capture cross section and the activation energy for the defect along with the Arrhenius plot.

CHAPTER 4 RESULTS AND DISCUSSION

4.1 Overview

Current Voltage (I-V) characteristics of the devices were measured from room temperature (~298 K) to ~ 50 K, in steps of ~50 K. The devices exhibited strong rectification, with the currents increasing exponentially with voltage in the forward direction and remaining relatively smaller and nearly constant in the reverse direction. This is characteristic of a Schottky barrier whose current transport is dominated by thermionic emission over a potential barrier in the semiconductor. The thermionic emission equation is:

$$I = AA^*T^2e^{-\frac{q\emptyset_b}{kT}}(e^{\frac{qV}{nkT}} - 1)$$

Where, I is the current, A is the area of the device, A^* is the Richardson constant, T is the temperature, q is the charge, ϕ_b is the barrier height, k is Planck's constant, V is the applied voltage and n is the ideality factor.

In all diodes at high currents, a deviation in the exponential behavior occurs because of series resistance [10,11,15].

The series resistance was determined by applying a high forward bias, larger than the barrier height. The reciprocal of the differential slope of the I-V plot (i.e. dV/DI) at high forward bias values gives a reasonably accurate determination of the magnitude of the series resistance [10,11].

The barrier height is calculated from the equation:

$$\emptyset_B = \frac{kT}{q}\ln(\frac{AA^*T^2}{Io})$$

Where T is the temperature at which the I-V measurement was performed, I_o is the intercept of the log I-V characteristic, and A^* is the Richardson constant with a value of 8.1 A/K^2cm^2 [11].

Another important parameter associated with Schottky contacts is the ideality factor. The ideality factor of a Schottky contact is a measure of how closely the Schottky contact follows the ideal thermionic emission equation. Ideality factors closer to 1 indicate a good or ideal Schottky contact with current transport dominated by thermionic emission, while those that approach larger values are usually dominated with emission processes other than thermionic emission [10,11].

Devices were then classified into ideal (I) and non-ideal (NI) devices based on the linearity of the curves in the forward bias on a log (I) vs V plots and their associated ideality factors at 200 K. Devices with a linear slope and ideality factors of 1.02 ~ 1.10 were categorized as ideal devices and devices which exhibited non-linear slopes and ideality factors greater than 1.2 were categorized as non-ideal devices. The electrical properties measured at 200 K were studied in the most detail. At this temperature, the thermally-activated thermionic current is sufficiently small that the influence of the relatively-temperature independent series resistance affects the characteristics only over a small range at high current bias [11]. Also, the temperature is not so low that the influence of the recombination and other forms of leakage currents dominate [11]. These currents typically have a smaller activation energy, so they tend to become much more dominate at low temperatures [11].

Shown below are the I-V characteristics of a typical ideal device and a non-ideal device determined.

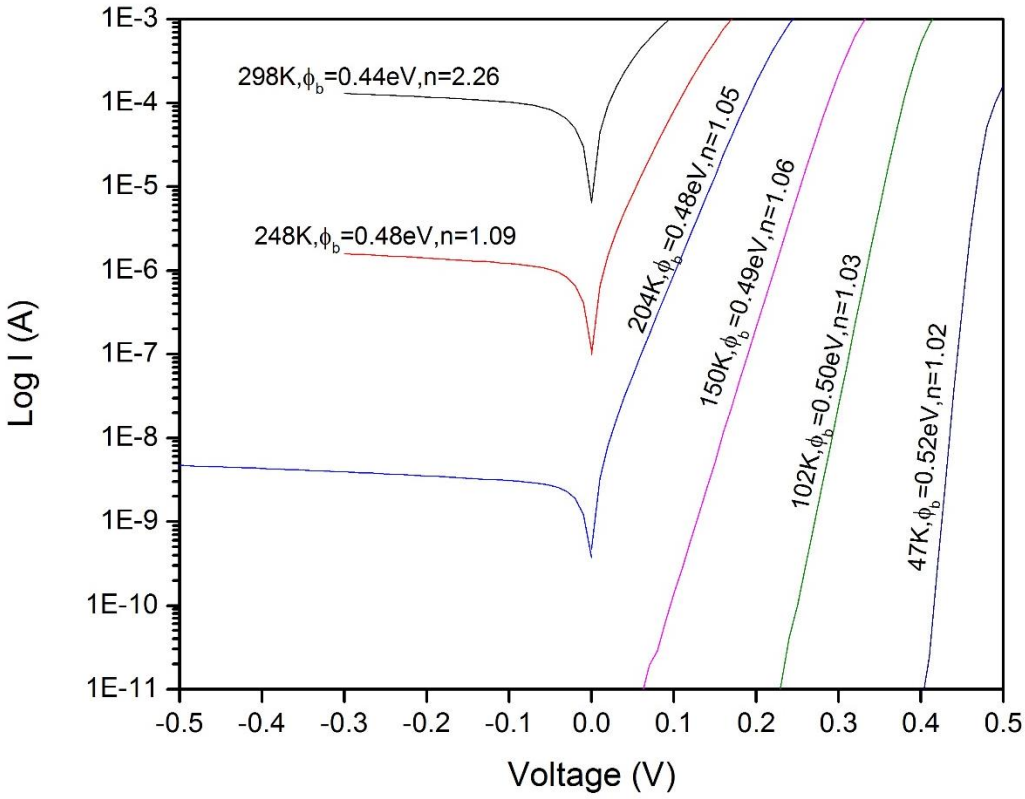

Figure 7. I-V characteristics of a near-ideal Nb/Si device with ideality factors of ~1.05.

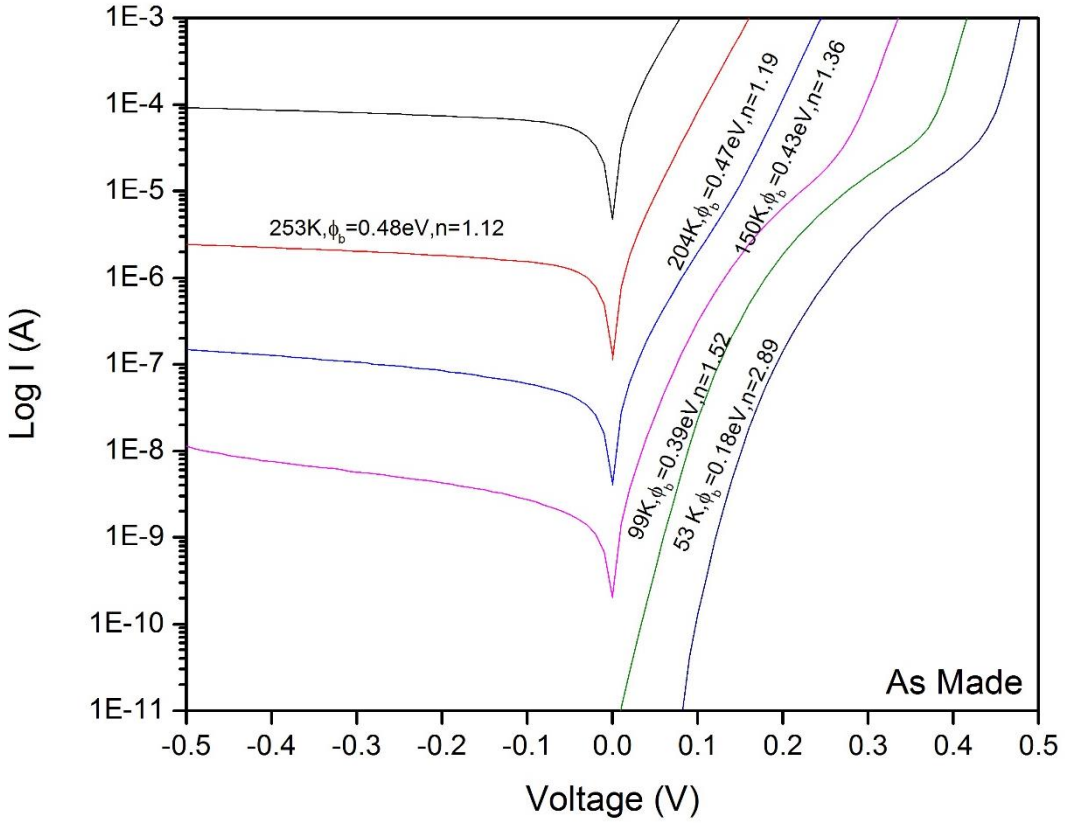

Figure 8. Non-Ideal I-V characteristics of a Nb/Si device which do not exhibit an exponential dependence of current with voltage in the forward bias mode and have large ideality factors significantly greater than 1 (i.e. >1.2).

Following the I-V characterization, the capacitance at -1.00 V was then measured. For devices with capacitances greater than 15 pF, Deep Level Transient Spectroscopy (DLTS) was performed to characterize the activation energy, capture cross section and density of defects in the depletion region and near the interface. Typical device capacitances were in the range of 300 pF to 500 pF.

Initial DLTS measurements were performed with 4 cool down sweeps from room temperature (~298 K) to ~45 K. However, to increase the accuracy of the defect parameters, the number of sweeps was increased to a minimum of 10. Shown below is a typical DLTS spectra obtained on our ideal devices.

An Arrhenius plot is then generated with emission vs 1/T to obtain the defect activation energy and capture cross section.

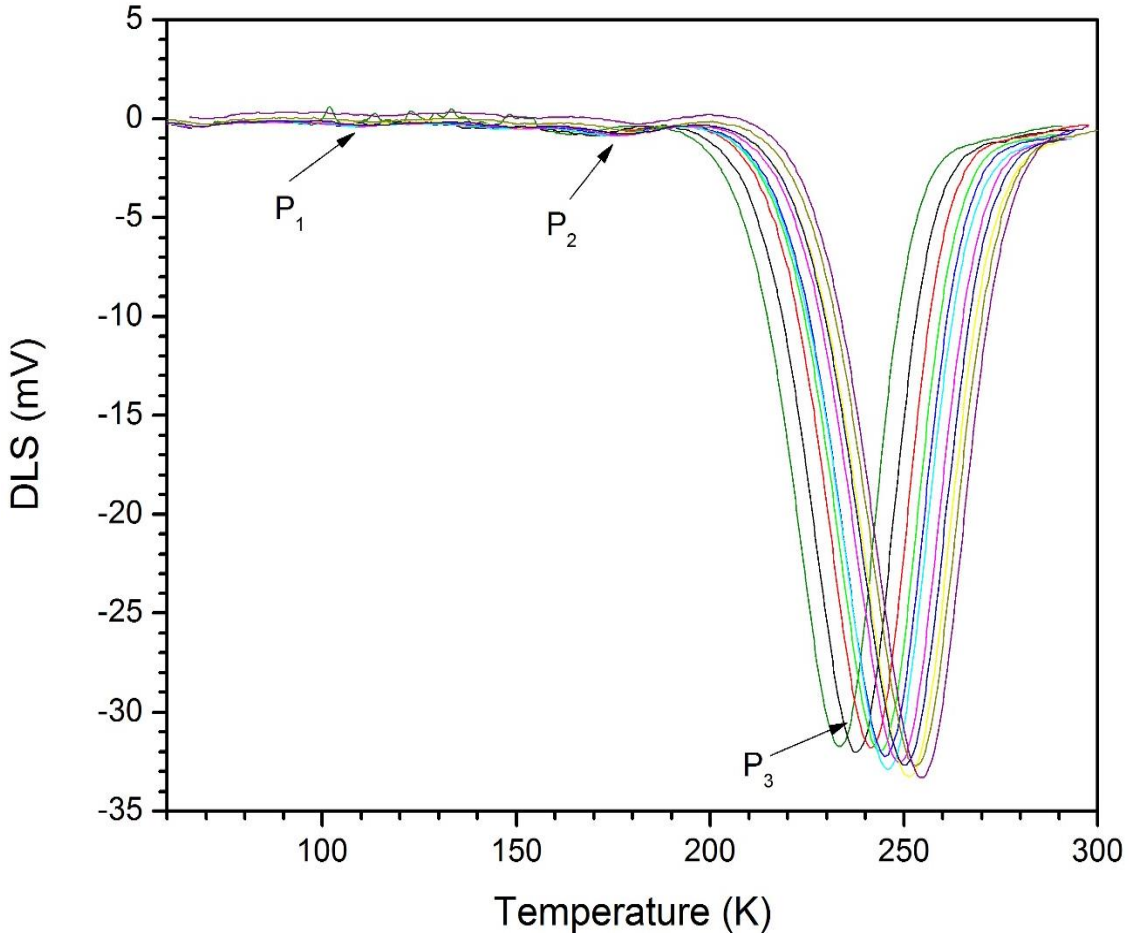

Figure 9. Typical DLTS spectra obtained on our as made/deposited ideal devices. This spectrum shows 3 peaks, located at ~110 K, ~ 170 K and ~250 K.

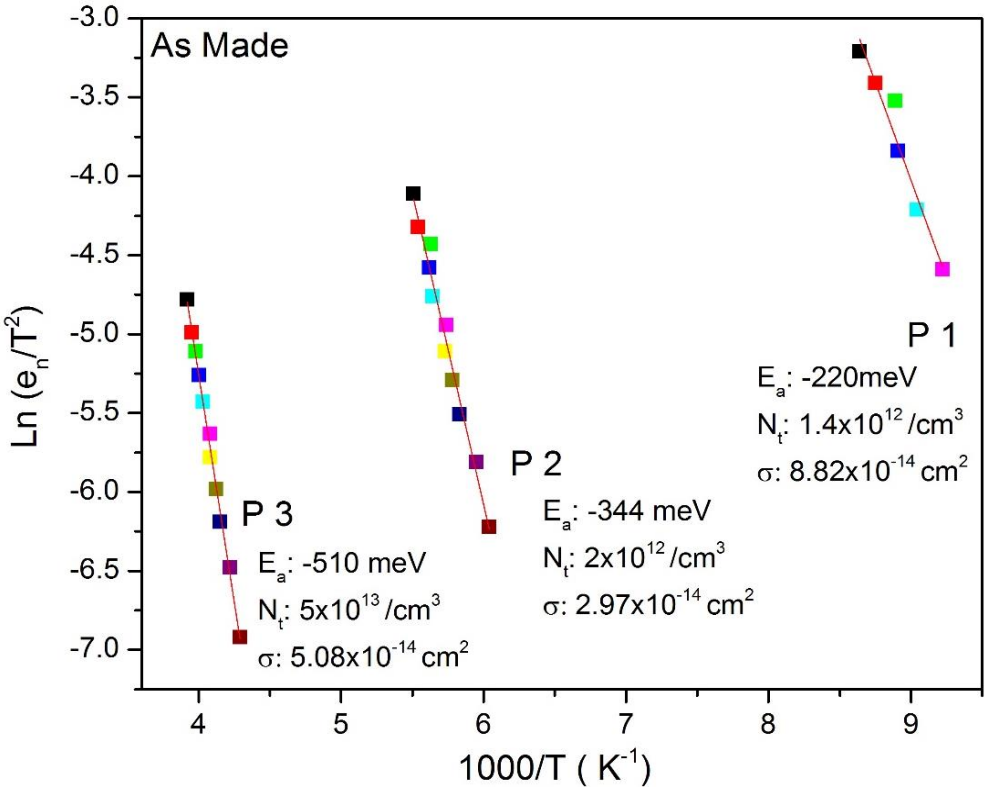

Figure 10. An Arrhenius plot of the emission rate divided by the temperature squared, as determined using DLTS.

The purpose of using DLTS is to identify the physical nature of the electrically active defects. This is typically accomplished in Si structures using well-established databases, including the compilations in References [16], [17], [18], [19], [20], [21] and [22]. Despite the extensive knowledge for most native and impurity point defects and complexes, there is scant information on Nb-related defects. Petterson *et al* did report in a conference paper, but the authors only provide information on the defect energy [8]. And there are not any additional studies that have validated their findings and conclusions.

Time Of Flight Secondary Ion Mass Spectrometry (TOF-SIMS) measurements were performed on the devices to identify impurities present in the Nb and Si regions of the device structures. The detection limit of the SIMS operating under the conditions used

is ~ 10^{14} to $10^{15}/cm^3$. As we found, many of the defects observed in our DLTS study fall below this concentration range, hence we must not exclude the possibility that some defects undetected by SIMS are present in our device. We also recognize that all the impurities detected with SIMS may not be electrically active and thus would not be detected in the DLTS measurements.

TOF-SIMS was performed on the devices before and after annealing. The lack of knowledge of the ionization probability in the chemical environment at and near the interface prevents us from accurately determining the concentrations of the various elements.

Elements detected by SIMS are listed in the following table:

ELEMENT	ELEMENT
niobium	silicon
oxygen	nitrogen
carbon	hydrogen
fluorine	chlorine

Table 1: Elements detected by SIMS

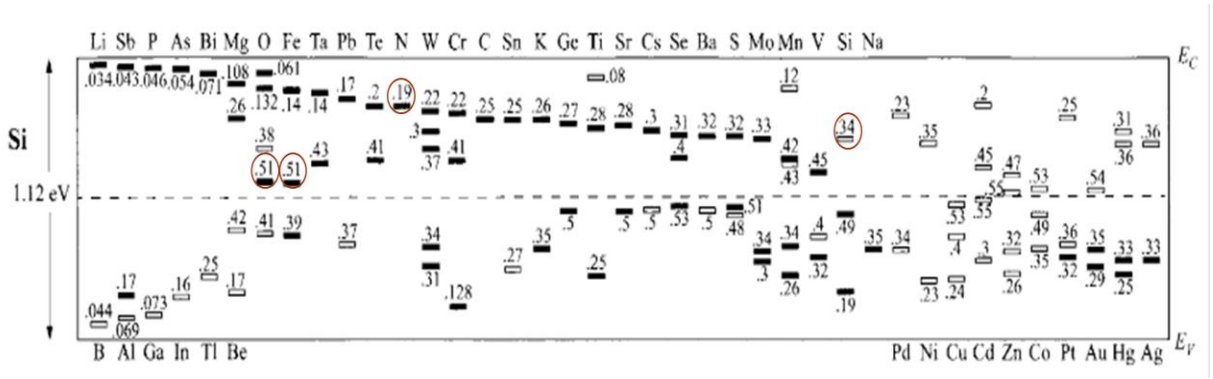

Fig11: Energy levels within the bandgap of various point defects in Si. Donors are in solid black rectangles and acceptors in hollow rectangles. [5]

Activation energy (meV)	**Capture cross section (cm^2)**	**Defect density (cm^{-3})**	**Possible defects**
-184±5	3.49×10^{-17}	4×10^{12}	N_{Si}, $\boldsymbol{V}_{Si}$
-220±5	8.2×10^{-14}	1.2×10^{12}	W_{Si}, Cr_{Si}, N_{Si}
-344±5	2.97×10^{-14}	2×10^{12}	$\boldsymbol{V}_{Si}$
-431±5	2.04×10^{-16}	2.0×10^{13}	~~Mn~~ $\boldsymbol{I}_{Fe}$
-510±5	5.08×10^{-14}	5×10^{13}	Fe_{Si}, O_{Si}

Table 2: List of the defect properties observed using DLTS in the as-made and annealed Nb/p-type Si devices, along with defects have energies and their capture cross-sections.

The capture cross sections of the electrically active defects are obtained by extrapolating the data in the Arrhenius plot to the y-axis intercept [19,20]. Since the 1/T values corresponding to the measurements are far from the intercept, errors in the capture cross-section can be significant. In contrast, the slope of the Arrhenius graph, that is used to infer the emission energy for the defect, can be reasonably accurately determined. For

instance, the reported values of the Si vacancy defects all fall near ~ 190 meV, however, their cross sections vary drastically from 2.59 $x10^{-16}$ cm^2 [21] to 2.00 $x10^{-14}$ cm^2 [22].

Possible defects in the as made devices are shortlisted from comparison of activation energy values obtained to the ionization energy values obtained from Sze [5], the result of SIMS performed on the devices and various sources from literature.

Activation energy (meV)	**Capture cross section (cm^2)**	**Defect density (cm^{-3})**	**Possible defects**
-220±5	8.2 x 10^{-14}	1.2 $x10^{12}$	W_{Si}, $\boldsymbol{I}_{Cr-}$, N_{Si}
-344±5	2.97 x 10^{-14}	2 $x10^{12}$	$\boldsymbol{V}_{Si}$
-510±5	5.08 x 10^{-14}	5 $x10^{13}$	Fe_{Si}, O_{Si}

Table 3: List of the defect properties observed using DLTS in the as-made Nb/p-type Si devices, along with defects have energies and their capture cross-sections.

The defect with defect energy of -344 meV is tentatively identified as $\boldsymbol{V}_{Si}$ as the defect energy corresponds to vacancy defects in silicon [5, 17].

The defect with the -510 meV activation energy could correspond to Fe_{Si} or O_{Si} [5]. There exists a peak at ~60 K in the DLTS spectra of the as made device, although noise in the data prevented us from extracting out the defect energy, capture cross-section, and concentration. Fe impurities in B doped p type Si are known to form electrically active Fe-B pairs with E_a of 74 meV [18]. This unidentified peak could correspond to Fe-B electrically active defects.

Nitrogen is detected to be present at the Nb/Si interface by SIMS. The defect with E_a of -220 meV has a similar energy to that of a nitrogen atom on a silicon site, $N_{Si,}$[16], but the cross section is five times larger than reported ($1.2x10^{-14}$ cm^2) [16], making this assignment questionable. The 220 meV, has energies similar to $\boldsymbol{I}_{Cr}$ [5, 23] and W_{Si} [5, 24], which are not detected at the interface by SIMS, but are present in the various stainless-steel parts in the system, including the tungsten-filament ion mill used to clean the silicon surface before metal deposition.

Niobium defects in Si have been reported to have 185, 297, and 576, meV. [8], quite different than the energies observed in our DLTS study on as made samples.

4.2 Annealing study

An annealing study using temperatures ranging from 150 C to 300 C was carried out on our devices to investigate the changes in the near-interfacial defects. The devices were annealed in a forming gas atmosphere for 15 mins.

4.2.1 Annealing Study of Ideal Devices

4.2.1.1 I-V Results

An annealing study on devices with those dominated by thermionic emission current, which we labeled ideal diodes, at temperatures ranging from 200 C to 300 C. The barrier height determinations of all diodes measured were found to decrease by ~0.02 eV upon annealing. Also, in most circumstances, the leakage current in the device also increases significantly.

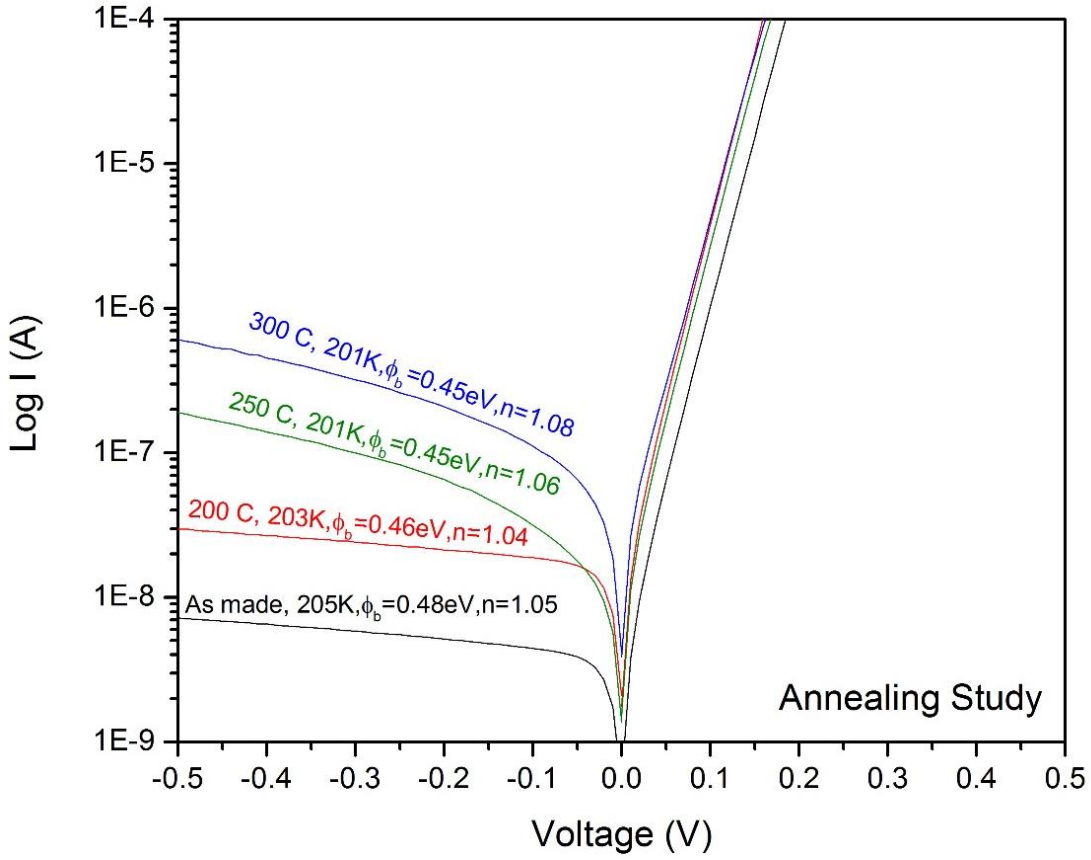

Figure 12: Consolidated I-V results of annealing study on ideal devices at 200 K.

4.2.1.2 DLTS Results

DLTS measurements of samples after 250 C anneals found that the defect concentrations in the Nb/p-Si devices are below the detection limit of DLTS.

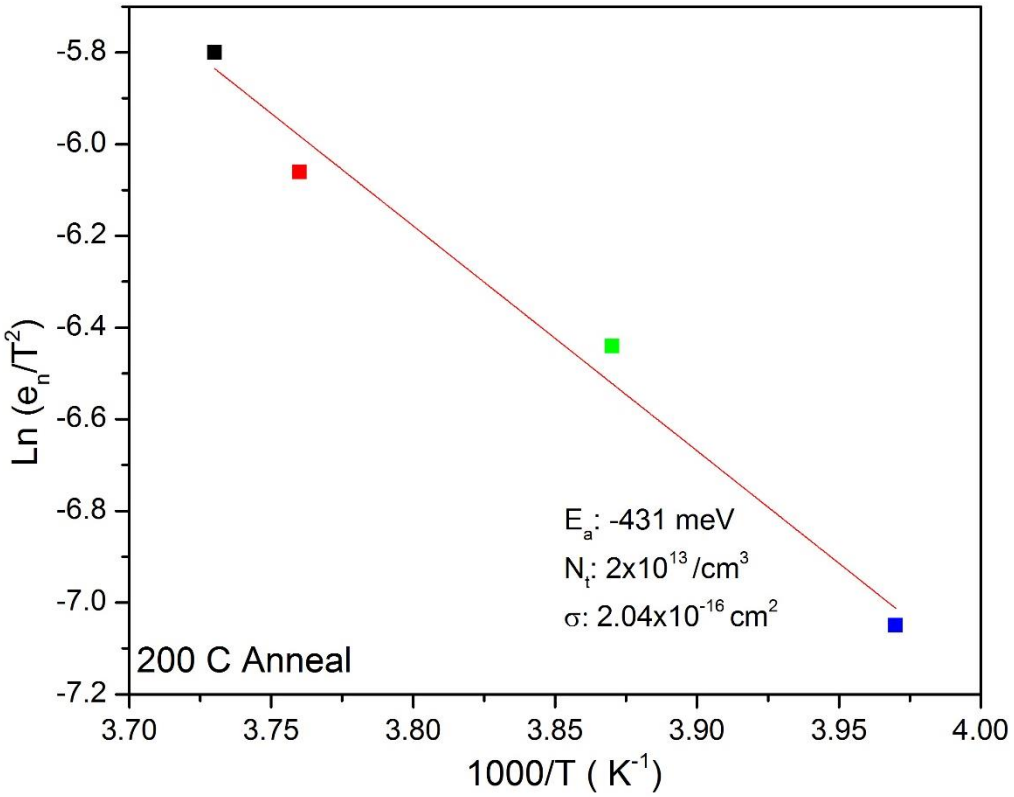

Figure 13. An Arrhenius plot of the emission rate divided by the temperature squared, as determined using DLTS. From this, we can infer the defect activation energy, capture cross section and the defect density of electrically active defects after 200 C anneal.

The defect activation energies and their capture cross section for an ideal device annealed at 200 C differs from that of the as-made devices. This indicates the formation of new and different defects form upon annealing. The literature reports that Fe-B pairs with activation energies of -74 meV are broken to form interstitial Fe, i.e. $\boldsymbol{I}_{Fe}$, with an E_a of -430 meV after annealing at 200 C [18]. Although we could not confirm or deny that the 60 K peak in the DLTS data was from Fe-B pairs, it seems very plausible that the defect that would form after annealing and falls in the expected range of energies and capture cross-sections is indeed the $\boldsymbol{I}_{Fe}$.

However, since Nb-related defects, presumably the Nb_{Si}, also has been reported to have similar energy levels within Si and would be expected to diffuse into the Si upon annealing,

we should not exclude that this defect at 431 meV could be a Nb_{Si} defect. The report in the literature on the energy level of Nb in Si has not been duplicated and we question the accuracy of the reported values.

Activation energy (meV)	**Capture cross section (cm^2)**	**Defect density (cm^{-3})**	**Possible defects**
-431±5	2.04×10^{-16}	2.0×10^{13}	~~Mn~~ I_{Fe}

Table 4: List of the defect properties observed using DLTS in Nb/p-type Si devices annealed at 200 C, along with defects have energies and their capture cross-sections.

4.2.2 Annealing Study of Non-Ideal Devices

4.2.2.1 I-V Results

Successive anneals were made on non-ideal devices starting at 150 C and ending with 250 C. It was observed that with each anneal the slope of the log I vs V curve in the forward bias changed from being non-linear and approached a straight, linear curve after the 250 C anneal. The leakage current decreases and the ideality factor is also observed to reduce from ~1.20 to 1.10.

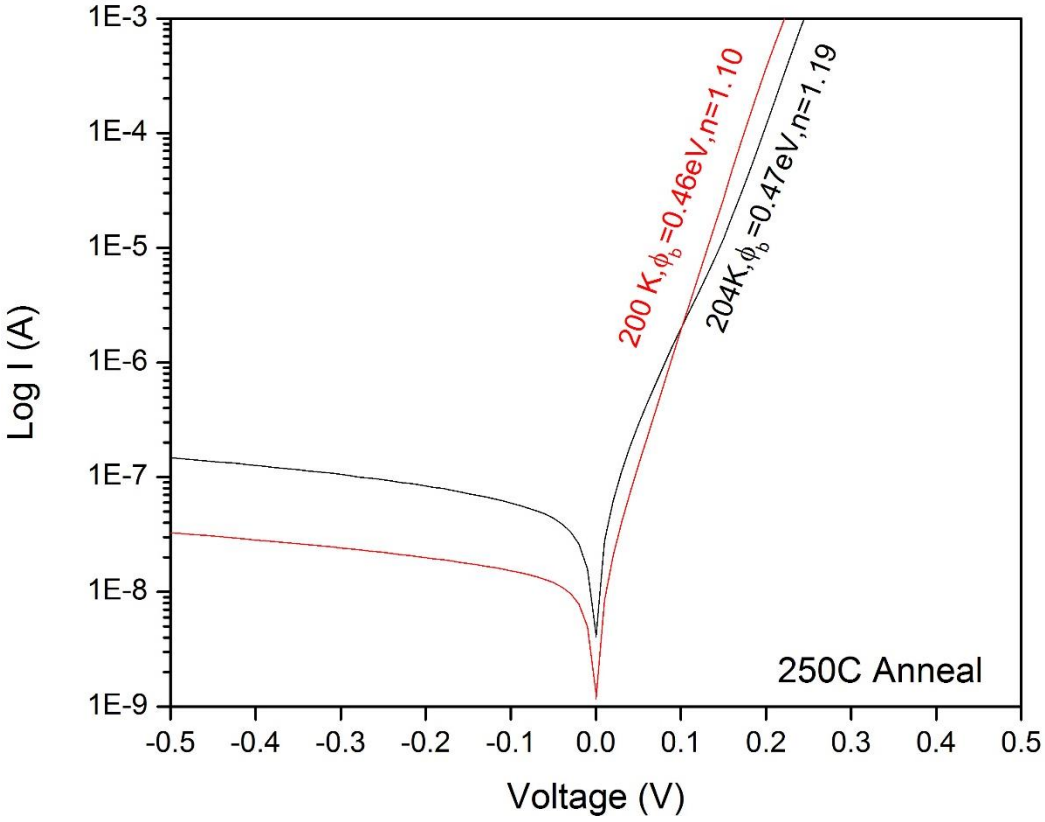

Figure 14. The I-V characteristics of a non-ideal device measured before and after a 250 C anneal measured at 200 K.

4.2.2.2 DLTS Results

Similar to the situation in annealing an ideal device, annealing a non-ideal device at 250 C in an atmosphere of forming gas either removed or reduced the number of electrically active defects to below the detection level of DLTS (~10^{10}-10^{11}/cm^3 defects).

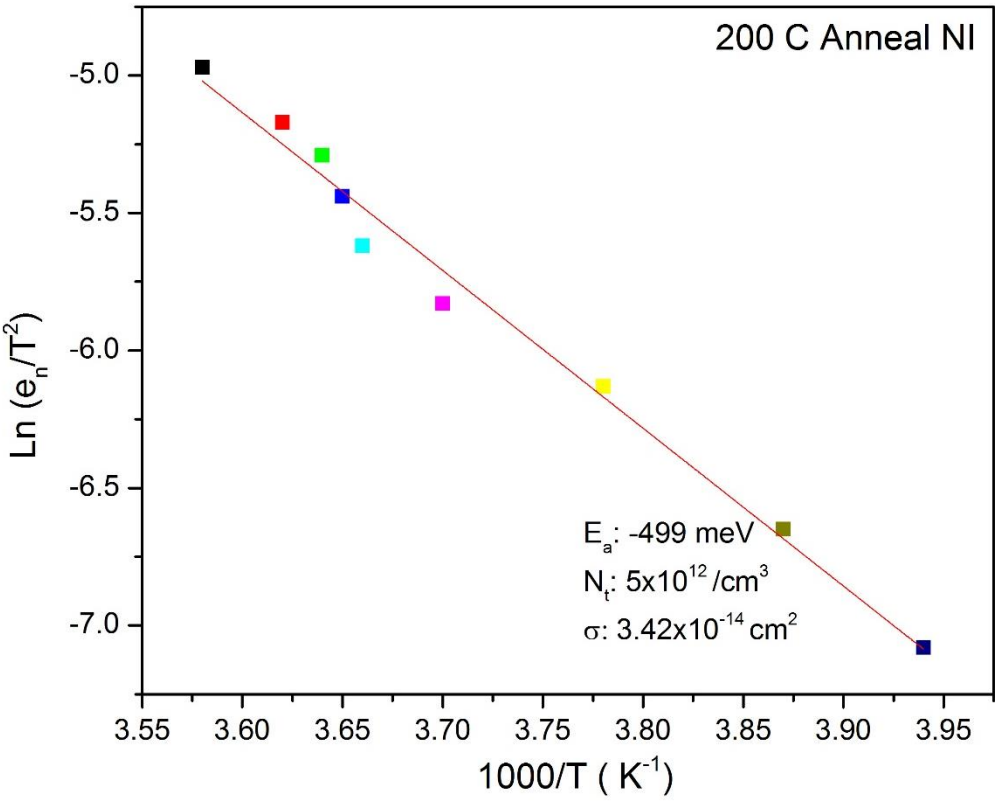

Figure 15. An Arrhenius plot of the emission rate divided by the temperature squared, as determined using DLTS. From this, we can infer the defect activation energy, capture cross section and the defect density of the electrically active defects for a non- ideal device annealed at 200 C

The activation energy and the defect capture cross section of defects detected by DLTS in an non-ideal device annealed at 200 C is similar to that of as made ideal device (-510 meV). The reader is referred to the earlier discussion on the physical origin of these defect levels.

Activation energy (meV)	**Capture cross section (cm^2)**	**Defect density (cm^{-3})**	**Possible defects**
-499$\pm$5	3.42×10^{-14}	5×10^{12}	Fe_{Si}, O_{Si}

Table 5: List of the defect properties observed using DLTS in the non-ideal Nb/p-type Si devices annealed at 200 C, along with defects have energies and their capture cross-sections.

4.3 Irradiation Study

We determined the electrical properties of an ideal device before and after exposure to 2 MeV alpha particles. The irradiation is used to systematically introduce defects in the Nb and Si and enhance intermixing at the interface.

The I-V properties of the device show a marked difference in properties of the device after the initial irradiation of $3.5x10^{13}$ ions/cm^2. For further irradiation steps, the I-V properties exhibit a decrease in reverse leakage current and increase in the barrier height by ~0.02 eV

The DLTS results show an increase in the defect density of the electrically active defects after each irradiation.

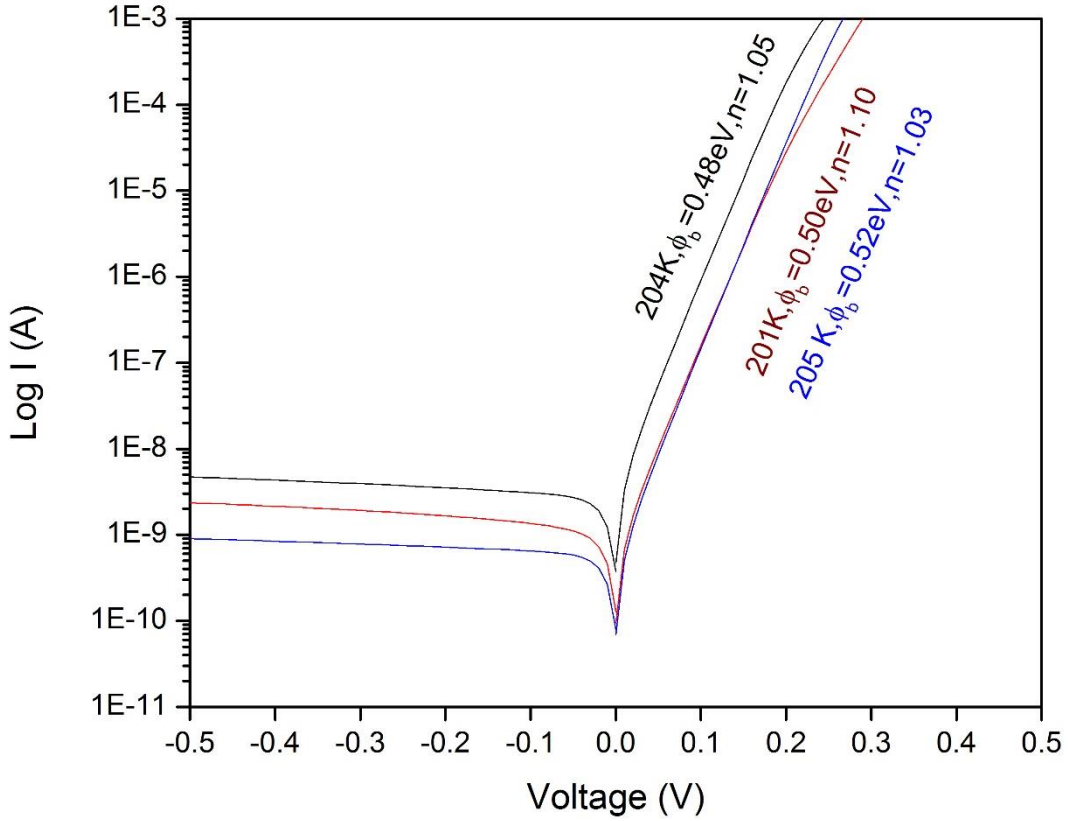

Figure 16. IV characteristics of an ideal device subject to sequential irradiation steps. The black, red and blue lines indicate the properties of the devices in as-made form and after $3.5x10^{13}$ and $2x10^{15}$ of 2 MeV α particles/cm^3 irradiation, respectively.

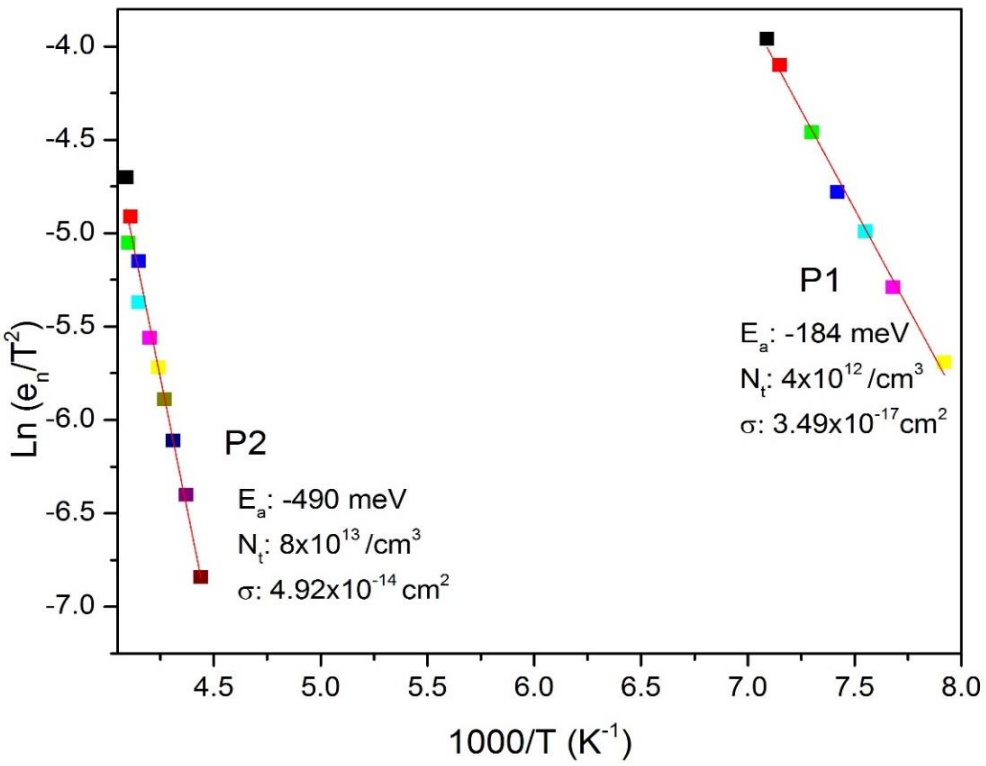

Figure 17. An Arrhenius plot of the emission rate divided by the temperature squared of an ideal device exposed to an irradiation of $2x10^{15}$ ions/cm^3, as determined using DLTS. From this, we can infer the defect activation energy, capture cross section and the defect density of the electrically active defects.

The DLTS results show a clear marked increase in defect density from as made device. Also a new additional defect with activation energy of -184 meV is observed. The activation energy of this defect falls at the ionization energy of N on a Si-site, i.e. N_{Si} [5]. Once again possible defects are $\boldsymbol{V}_{Si}$, N_{Si}, Fe_{Si}, O_{Si} and Nb_{Si}.

Activation energy (meV)	**Capture cross section (cm^2)**	**Defect density (cm^{-3})**	**Possible defects**
-184±5	3.49×10^{-17}	4×10^{12}	N_{Si} , $\boldsymbol{V}_{Si}$
-490±5	4.92×10^{-14}	8×10^{13}	Fe $_{Si}$, O $_{Si}$

Table 6: List of the defect properties observed using DLTS in an ideal Nb/p-type Si devices after irradiation of $2x10^{15}$ ions/cm^3, along with defects have energies and their capture cross-sections.

CHAPTER 5 CONCLUSIONS

A systematic study using current-voltage (I-V) and Deep Level Transient Spectroscopy (DLTS) measurements was carried out to characterize the electric properties and electrically-active defects in niobium-silicon Schottky barrier devices. Barrier height determinations using temperature-dependent I-V measurements at -125 to 25 C indicate that the barrier height decreases from 0.50 eV to 0.48 eV for anneals above 200 C. A significant increase in leakage currents in most cases is most often observed. Successive anneals on devices dominated by leakage currents annealed at temperatures ranging from 150 C to 250 C exhibit a significant decrease in leakage currents, resulting in a near ideal device after annealing at 250 C. In both cases, DLTS measurements of samples after 250 C anneals found that the defect concentration in the depletion region drops markedly after annealing.

CHAPTER 6 FUTURE WORK

In preliminary studies, annealing the defects in a forming gas atmosphere for 15 mins has been proved to reduce the defect concentration to undetectable levels by DLTS (i.e. $<\sim 10^{10}$-$10^{11}/cm^3$) after 250 C anneals in both ideal and non-ideal devices. Annealing the devices in vacuum to observe and understand the role of forming gas, particularly the role of hydrogen in the removal of defects needs to be investigated.

Particle irradiation on the device is used to cause intermixing at the interface and the formation of point defects and vacancies in the Nb electrode and the Si semiconductor. Further studies in this direction should be carried out.

The lack of an established database for Nb defects in Si has been a major handicap towards identifying the Nb defects in Si. The use of ion implantation of Nb in Si and subsequent annealing to better characterize the defect energy and capture-cross section is also planned.

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