Passive Loop Filter Zoom ADCs:

by

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ABSTRACT

This dissertation proposes and presents two different passive sigma-delta modulator zoom Analog to Digital Converter (ADC) architectures. The first ADC is fully-differential, synthesizable zoom-ADC architecture with a passive loop filter for low-frequency Built in Self-Test (BIST) applications. The detailed ADC architecture and a step by step process designing the zoom-ADC along with a synthesis tool that can target various design specifications are presented. The design flow does not rely on extensive knowledge of an experienced ADC designer. Two example set of BIST ADCs have been synthesized with different performance requirements in 65nm CMOS process. The first ADC achieves 90.4dB Signal to Noise Ratio (SNR) in 512µs measurement time and consumes 17µW power. Another example achieves 78.2dB SNR in 31.25µs measurement time and consumes 63µW power. The second ADC architecture is a multi-mode, dynamically zooming passive sigma-delta modulator. The architecture is based on a 5b interpolating flash ADC as the zooming unit, and a passive discrete time sigma delta modulator as the fine conversion unit. The proposed ADC provides an Oversampling Ratio (OSR)-independent, dynamic zooming technique, employing an interpolating zooming front-end. The modulator covers between 0.1 MHz and 10 MHz signal bandwidth which makes it suitable for cellular applications including 4G radio systems. By reconfiguring the OSR, bias current, and component parameters, optimal power consumption can be achieved for every mode. The ADC is implemented in 0.13 µm CMOS technology and it achieves an SNDR of 82.2/77.1/74.2/68 dB for 0.1/1.92/5/10MHz bandwidth with 1.3/5.7/9.6/11.9mW power consumption from a 1.2 V supply.

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TABLE OF CONTENTS

Page

CHAPTER Page

CHAPTER Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

CHAPTER 1

INTRODUCTION

1.1 Motivation

Traditionally, analog devices are tested based on parametric measurements wherein the measured parameters are compared with designer-defined specifications and a pass/fail decision is made. While it has been effective, there are several issues with the traditional approach that requires a new way of thinking. First, this approach results in high engineering and test application cost, requiring long test development cycles, long test times, and expensive test equipment. Second, some analog Devices Under Tests (DUTs), such as DC/DC converters, data converters, and sensor front-ends, are not easily accessible from the pinouts. While these devices are generally tested as parts of an entire system, relying on system-level tests increases the likelihood of missing small or latent defects and stability-related problems that arise later in the field or under different input/environment conditions.

In high-complexity mixed-signal circuits, there are severe restrictions on accessibility to the various parts of the DUT as well as a serious limitation on the number of test pins. A BIST solution is the most promising test technique because it allows elimination of expensive mixed-signal testers and increases the number of test points while minimizing the number of required pins and reducing the test time. Recently, a great deal of research has been devoted to developing BIST techniques for mixed-signal circuits [1-10]. Most of the time, the BIST response is in the low-frequency or DC domain even if the DUT is in the high-frequency domain [4]. In order to reduce the test time and improve the

test coverage, a compact, low-latency analog-to-digital converter (ADC) is required in high-volume testing.

While there are many options for implementing ADCs in BIST applications, the most challenging aspect of BIST is that a dedicated engineer needs to design the BIST ADC in addition to the functional units of the primary design. This is generally an unpalatable option for design managers since it takes away a very critical resource while the team is trying to meet time-to-market deadlines. Hence, BIST is generally an underutilized process unless a generic ADC can be used to digitize the analog signals. Generic ADCs however, rarely provide the optimum solution for BIST since the requirements in terms of resolution, bandwidth, and linearity vary widely with respect to the application. Analog BIST can benefit greatly from an automated design process for BIST ADCs that does not heavily rely on the experience of a dedicated design engineer. In order to develop an automated design, we have to choose an ADC architecture with building blocks that can be implemented in a streamlined fashion with preferably analytically determined design parameters. Furthermore, it would be advantageous for the ADC to be able to adapt with respect to multiple resolutions, bandwidth, and measurement time requirements to service many analog blocks with one design. In addition to automated synthesis requirement, BIST ADCs need to provide low area overhead, high resolution/accuracy, low power consumption in case BIST is needed for in-field calibration, and adequate bandwidth. While many ADC architectures provide excellent trade-offs between resolution, power consumption, and bandwidth, zoom-ADCs provide the best flexibility from the design-space perspective for BIST applications.

Optimizing the design of the zoom-ADC based on both low-power and high-resolution requirements is a challenging task. Designers spend the extensive time to determine a suitable noise transfer function (NTF), fit the required coefficients, verify the stability of the system, acquire the specifications of the circuit and desired operational-amplifier (OPAMP), and determine the transistor sizes of the OPAMP. The design cycle is long and requires a significant analog design experience. Design automation/synthesis of incremental zoom-ADCs is another challenging task due to the need for active integrators, which employ OPAMPs. OPAMP-based designs are problematic for synthesis since OPAMP non-idealities result in incomplete charge transfer, leading to non-linear behavior [12]. Thus, zoom-ADC architectures that have been explored thus far do not meet the automation requirement for BIST applications. However, passive sigma-delta (SD) modulators do not require any OPAMPs or OTAs [13, 14]. As a result, they can be synthesized easier than their active counterparts. Furthermore, since the sampling clock frequency of passive SD modulators will not be dependent on OPAMP limitations of maximum gain/bandwidth (GBW), the resulting zoom-ADCs will satisfy all the requirements for BIST applications, namely, area efficiency, high speed, low power, and synthesizable design.

Testing of RF systems is another challenge. With the rapid development of wireless and wireline communications, a variety of new standards and applications are emerging in the marketplace. In order to achieve higher levels of integration, RF circuits are frequently embedded into System on Chip (SoC) or System in Package (SiP) products. These developments, however, lead to new challenges in manufacturing test time and cost. Use

of traditional RF test techniques requires expensive high-frequency test instruments and long test time, which makes test one of the bottlenecks for reducing IC costs.[80][81][82] Most of the time, these System on Chip (SoC) includes an ADC for functional operating conditions. When the high bandwidth /high accuracy signals need to be tested functional ADCs can also be employed as a BIST ADC in order to save from area and additional design efforts. Thus, functional ADCs also needs to satisfy built-self test conditions such as programmability and high conversion rate [81]. In wireless applications ADC performance measured by efficiency and speed at which analog information can be converted into digital signals. Since an energy efficient operation is required by modern electronic systems, there has been a great push to reduce energy consumption in all relevant system building blocks, including ADCs [54]. The perpetual sizing of CMOS technologies has derived the increase of the transition frequency of CMOS transistors, but it has also resulted in the reduction of the intrinsic gain of these devices [55]. As a consequence, it has become more difficult to design high gain and high bandwidth amplifiers with reduced power dissipation, making the design of ADCs that require such amplifiers, including ΣΔMs, more challenging. Sigma-delta analog to digital converters (ADC) are popular for high resolution. The primary reasons for their popularity are the heavy reliance on digital components, low cost, and ease of implementation. Currently, most ∑-Δ ADCs use active integrators based on amplifiers. The rationale for this is to achieve resolutions predicted by ideal equations and simulations. Unfortunately, the use of an active integrator results in sacrificing a high portion of a power budget to biasing circuitry required by the amplifier [56].

Passive sigma-delta modulators provide simpler (have less hardware complexity), area efficient and low power solutions for sigma-delta ADC applications due to the elimination of power-hungry OTAs. However passive integrators provide signal attenuation and therefore, are more sensitive to noise coupling and lack of the loop filter gain limits the options for reducing quantization noise power for passive ΔΣ modulators.

The research question of this thesis is: how one can take advantage of the passive structures in order to resolve the issues mentioned above while achieving competitive performance and power efficiency with active ΣΔM counterparts. Therefore, this thesis intends to use the passive modulators for BIST and configurable wireless receiver applications and investigates the usage of passive modulator architectures along with zoom ADC architectures in order to achieve comparable performance with active counterparts. In this theses, we propose two different passive loop filter based and fully-differential zoom-ADC architectures in order to resolve the mentioned challenges in previous paragraphs. First ADC is a synthesizable BIST zoom ADC while second ADC is a reconfigurable flash ADC based zoom ADC for wireless applications.

1.2 Contributions

The primary contributions of this research are summarized as follows:

• Proposed a fully synthesizable, small footprint, passive, fully-differential, zoom-ADC architecture with two-step zoom-in conversion. (Chapter 3)

• A hybrid passive loop filter incremental second order sigma-delta ADC is used for fine conversion. (Chapter 3)

• A synthesis algorithm proposed for the ADC design and explained in detail. (Chapter 3)

• Two different design examples are presented and compared with state of the art designs. The Walden and Schreier Figure-of-Merits (FoM) are calculated for comparison with published designs. (Chapter 3)

• A novel reconfigurable interpolating flash ADC based DT passive dynamically zooming ΔΣ modulator is presented. (Chapter 4)

• A dynamic zooming technique is proposed which can be used independently of OSR value while enabling the multi-bit feedback DAC option for passive ΔΣ modulators and reducing quantization noise significantly. (Chapter 4)

• The proposed ADC implemented in 130nm technology covers bandwidths between 100KHZ and 10MHz which makes it a good candidate for GSM/EDGE up to LTE bandwidths. (Chapter 4)

• Showed that measurement results of the proposed ADC design achieve much better FoM values compare to active DT counterparts and competitive FoM values compared to continuous time modulators. (Chapter 4)

1.3 Organization of the Thesis

This thesis is organized into four chapters other than the introduction chapter; Chapter 2 discusses the previous work. Chapter 3 introduces a passive loop filter based, fully-differential, synthesizable zoom ADC architecture, along with an automated flow that can synthesize BIST ADCs for different applications and design targets. Furthermore, it presents a design automation procedure, shows experimental results with two ADCs that have been synthesized with different performance requirements. Chapter 4 proposes a novel Reconfigurable Dynamic Zoom Passive Sigma-Delta Modulator for Cellular

applications, provides the information about background, the previous circuit techniques, and modulator architectures, explains the detailed design of the proposed ADC, describes the design challenges and presents the measurement results associated with prosed ADC. Finally, conclusions are discussed in Chapter 5.

CHAPTER 2

PREVIOUS WORK

Analog-to-digital converters (ADCs) used in BIST applications have requirements similar to ADCs in instrumentation applications with high absolute accuracy and linearity. These ADCs also need to be designed considering flicker noise and DC offset. Fulfilling all these requirements often results in power hungry and large die area ADCs due to typically complex designs with several operational amplifiers (OPAMPs). These attributes are unacceptable for BIST applications which need to be simple and area efficient in order to decrease cost. Moreover, including several OPAMPs increases design effort, requires experienced designers, and makes full design automation of ADCs time consuming and unreliable. This paper proposes a new BIST ADC architecture and a fully automated design flow for the BIST ADC that takes into account multiple factors for BIST insertion, including area and performance overhead, test time, and test accuracy.

Several ADC architectures can be considered for BIST ADCs. SAR ADCs are area and energy efficient and their design effort can be automated, making them a good candidate for BIST applications. However, SAR ADC resolution is typically limited to 10 to 12 bits due to the nonlinearity of multiple Digital to Analog Converters (DACs) [15, 16, 17]. Cyclic ADCs do not require multiple-bit DACs but require highly accurate OPAMPs [18, 19, 20]. Zero Crossing Detection based Cyclic ADCs can be designed using only passive elements and comparators [21]. However, their resolution is limited to 8 to 10 bits. Instrumentation applications extensively use dual slope ADCs. Although dual slope ADCs achieve high resolution, the resolution is linearly proportional to their conversion time,

making them relatively slow [22]. High oversampling rate, noise-shaping, sigma-delta ADCs can provide high resolution in a shorter time. [23,25]. For low-frequency operations, SD ADCs are generally used in incremental mode, in which they are first reset and then operated for a fixed number of cycles. Unfortunately, attaining high resolution still requires a relatively long conversion time. Using higher order modulators or multi-bit quantizers results in faster response. However, this architecture can only achieve moderate energy efficiency and presents a large area overhead [23, 24, 25, 26]. Compact sigma delta analog to digital converters play an important role for some BIST applications [6, 7, 10, 27]. Nevertheless, compact sigma-delta ADCs can achieve a maximum of 9 bits accuracy. Two-step extended counting ADC is another alternative which uses a Nyquist rate ADC in the first step and an SD ADC in the second step to digitize residue of Nyquist ADC [28]. While this dual architecture leads to faster conversion, the overall linearity of the ADC is limited by the linearity of the Nyquist ADC. Another recent two-step implementation [29] extends the order of a conventional IADC (Incremental ADC) from 2 to 3 while requiring only the circuitry of a 2nd-order IADC. However, the linearity of this circuit is also limited.

Zoom ADC is another two-step architecture. A coarse ADC is used together with a fine incremental ADC. First, a Nyquist rate ADC makes a coarse conversion with a low resolution. Next, the fine conversion step uses the coarse ADC result to adjust the references of the incremental ADC in order to zoom into a small range around the input signal. Unlike traditional two-step ADCs, the fine converter does not digitize the residue of the coarse converter, making the accuracy of the conversion exclusively dependent on the accuracy of the fine converter [32, 33].

Generally, CMOS circuit synthesis can be classified as (a) knowledge-based, (b) simulation based, and (c) equation-based. The knowledge-based method adopts circuit design knowledge and theoretical equations to generate the design rules [32, 33]. The simulation-based method employs circuit simulators along with a search algorithm and runs circuit-level simulations until the optimum point is reached [34,36]. The equation-based method uses several equations in theory, creates a goal function with the combination of these equations, and uses optimization algorithms to solve for the roots of the goal function [36, 37, 38]. The knowledge synthesis method requires a capturing circuit design expertise in a series of well-defined design steps. Relying purely on equations is not feasible for designing ADCs. The simulation-based approach provides accurate results at the expense of long simulation time and may not be feasible to attain at the system level. The knowledge-based approach can be used for the system-level. However, the steps in circuit-level design, i.e. setting transistor parameters, are typically very interdependent and thus not conducive to a step-by-step prescription.

Several high-level design tools are proposed [39, 40, 41, 42, 43] for ADC design. However, these existing techniques do not provide synthesis down to the circuit level. Some techniques are proposed for the complete design process. However, these rely heavily on time consuming iterative transistor level simulations and require OPAMPS with a large area and power consumption overhead [32, 35, 38, 44]. In chapter 3, we propose fully synthesizable passive incremental zoom ADC from a high level to circuit netlist level, intended specifically for BIST applications. The proposed architecture does not require any OPAMPs, thus requiring smaller area overhead and faster design cycles.

Doubling functionality is another important aspect in BIST applications, mostly used in RF/Wireless IC test applications due to the requirement of high bandwidth/accuracy measurement [81][82]. Most of the time, RF System on Chip (RFSoC) includes an ADC for functional operating conditions. When the high bandwidth /high accuracy signals need to be tested functional ADCs can also be employed as a BIST ADC in order to save from area and additional design efforts. Thus, this ADCs also needs to satisfy built-self test conditions such as programmability and high conversion rate as well as RF system requirements [81]. The Delta-Sigma (ΔΣ) ADC architecture is the preferred solution due to its easy reconfigurability for better performance or less power consumption by just changing the OSR. The ΔΣ architecture is less dependent on analog component values and its noise shaping property helps attenuate a significant amount of quantization noise and out of band interferers. Multiple continuous-time (CT) and discrete-time (DT) multi-mode ΔΣ modulators have been reported in the literature [63-70]. Even though CT ΔΣ modulators have many advantages over DT ΔΣ modulators, such as implicit anti-aliasing filtering and power efficiency, they are more prone to non-idealities such as clock jitter, excess loop delay, and integrator coefficient (RC time constant) variation which can be as high as ±%20. Furthermore, multi-mode CT modulators are more sensitive to parasitic effects and are more complex because CT loop filters are designed for a single operating clock frequency and they need multiple switchable passive RC combinations in order to satisfy multi-mode operation. Comparatively, DT modulators are robust with respect to process variations as their transfer functions rely on capacitor ratios. Furthermore, the multi-mode operation can be realized by just adjusting clock frequency.

However, active DT ΔΣ modulators consume much more power compared to their CT counterparts due to the higher unity gain bandwidth (UGBW) requirements for the Operational Transconductance Amplifiers (OTAs). The UGBW of the OTAs used in active DT modulators needs to be much higher than the sampling frequency to ensure proper settling in switched capacitor integrators. Compared to the active ΔΣ modulators, passive ΔΣ modulators provide low power solutions for DT operation due to the elimination of power-hungry OTAs [58][59]. Nevertheless, known passive ΔΣ architectures are limited to applications with relatively narrow signal bandwidth and/or medium dynamic range requirements due to limited options to suppress quantization noise

A dynamic zoom-ADC architecture is presented in [61] for audio applications. A coarse 5b SAR (Successive Approximation Register) ADC and a 1b active ΔΣ modulator, which are clocked at the same clock edge, constitute the zoom-ADC. The ΔΣ modulator includes a 5b feedback DAC. Every 5 clock cycles, the SAR ADC yields a coarse conversion result and this coarse conversion is used to dynamically update the reference voltages of the ΔΣ modulator using a multi-bit DAC. Therefore, similar to multi-bit quantizer-based ΔΣ modulators, quantization noise power decreases significantly. In this architecture, if the ΔΣ OSR value is not high enough, the input signal can move out of the zoom range during the 5 clock cycles, which are required for SAR ADC. This is especially true for ΔΣ modulators which are used for wireless communications. They are required to work with lower OSR values due to wide bandwidth, low power consumption and/or technology driven constraints on maximum sampling frequency.

In chapter 4, we propose a DT passive dynamic zooming ADC which supports multi-mode EDGE-to-LTE bandwidths. The overall architecture of the proposed ADC consists of a 5b interpolating flash ADC as the zooming unit, and a passive discrete time ΔΣ modulator as the fine conversion unit. Unlike SAR ADC, interpolating flash ADC requires only one clock cycle to measure input voltage and to update DAC values. Since ΔΣ modulator DAC values are updated every clock cycle, dynamic zooming technique can be used independently of OSR value. The proposed ADC enhances passive sigma-delta modulator performance significantly by enabling the multi-bit feedback DAC option for passive ΔΣ modulators and reducing quantization noise. The proposed ADC achieves between 13.5 bits and 11 bits of resolution.

CHAPTER 3

SYNTHESIS OF PASSIVE ZOOM-ADC FOR BUILT-IN SELF-TEST APPLICATIONS

3.1 Introduction

In this chapter, we propose a passive loop filter based, fully-differential, synthesizable zoom ADC architecture, along with an automated flow that can synthesize BIST ADCs for different applications and design targets. Figure 1 shows the top-level architecture of this two-step zoom ADC. In the first step, a coarse converter performs the zooming function whereas, in the second step, a fine converter resolves additional bits within the zoom window. A passive incremental second order sigma-delta ADC is used for

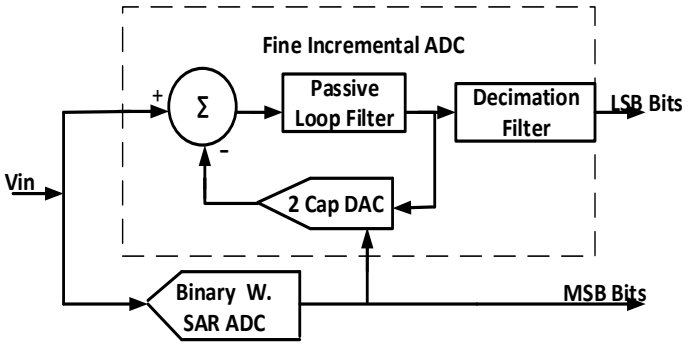


Fig. 1. System-level diagram of zoom incremental ADC

fine conversion. The fine converter of the proposed zoom ADC enables higher frequency operation, does not include any OPAMPs or OTAs, and employs a novel zooming DAC with two capacitors. The proposed clocking scheme is specially customized for passive delta sigma modulators, resulting in a small area. For the coarse ADC, a successive approximation ADC with a charge sharing capacitor DAC is employed. Coarse ADC

reuses the elements of the passive incremental ADC, providing the zooming function with the minimal additional area. We present the details of the architecture, the analytical expressions governing the relations between the parameters of the building blocks and the ADC performance, and a streamlined, step-by-step process for designing the zoom-ADC that does not require extensive experience in ADC design. The synthesis flow uses a hybrid approach, where system-level synthesis is based on analytical formulations and circuit-level synthesis combines knowledge-based and simulation-based approaches. This chapter is organized as follows. Section 3.2 describes the passive zoom ADC architecture, while Section 3.3 presents design automation procedure. Section 3.4 is devoted to experimental results with two ADCs that have been synthesized with different performance requirements.

3.2 Discrete Time PSDM Incremental ADC with Two Capacitor Zoom DAC

3.2.1 Passive Sigma Delta Modulators

Passive sigma-delta modulators (PSDMs) provide area efficient and low power solutions for sigma-delta ADC applications due to the elimination of power-hungry OPAMPs. Figure 2 shows the model of the first-order sigma-delta modulator with an active integrator. Comparatively, Figure 3 represents the model of a first order passive sigma-delta loop filter which can be implemented either using continuous time or discrete time approach. For illustrative purposes, the continuous time implementation is shown in Figure 3.

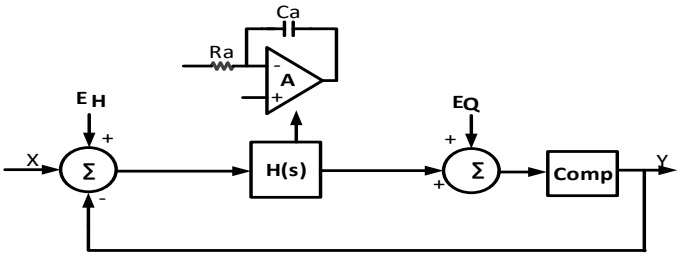


Fig. 2. System-level modeling of the first-order modulator with active integrator

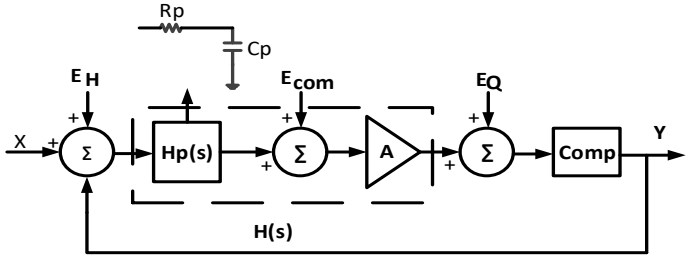


Fig. 3. System-level modeling of the first-order modulator with active integrator

In the passive SD architecture, the loop filter does not provide any gain due to the lack of active integrators that also provide the loop gain. Luckily, unlike traditional active SD modulators, the comparator gain in passive modulators is not unity. The signal swing at the comparator input will be relatively small due to the significant attenuation in the filter. However, at the output, the comparator can provide full swing. Thus, the small signal gain of the comparator can provide adequate gain for the loop.

Equation (1) represents the s-domain transfer function of the active delta SD modulator while Equation (2) represents the loop filter transfer function of the passive SD modulator along with comparator gain. In Equations (1) and (2), A is the integrator or comparator gain, H(s) is the loop transfer function, R_a, R_p, C_a, and C_p are passive components in the filter.

$$H_{active}(s) = \frac{A}{1 + sAR_aC_a} \quad (1)$$

$$H_{passive}(s) = \frac{A}{1 + sR_pC_p} \quad (2)$$

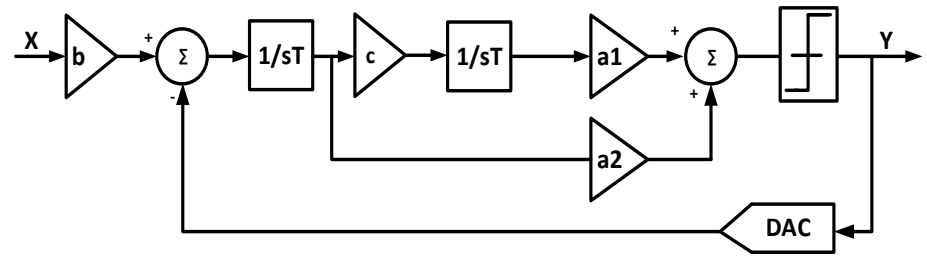
The loop gain of PSDM can be equalized to the transfer function of an active sigma delta integrator by matching the small signal gain of the comparator to the gain of an OPAMP. However, in order to obtain an equivalent transfer function for the same loop gain, the passive filter RC product should be larger than the RC product of the active integrator by a factor of the integrator gain, as illustrated in Equation (3).

$$R_pC_p = AR_aC_a \quad (3)$$

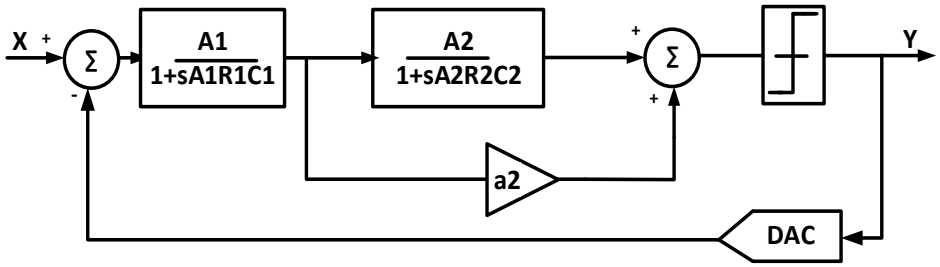
Thus, R and C values for the passive filter strongly depend on the comparator gain while active integrator R and C values are independent of the OPAMP gain. The output signal of passive SD modulator in Figure 3 can be expressed as in Equation (4), where $E_{H,}$ $E_{COM,}$ and E_Q represents noise powers associated with passive filter comparator and quantization, A represents gain and HP represents passive filter transfer function

$$Y \approx X + E_H + \frac{E_{COM}}{Hp} + \frac{E_Q}{AH_P} \quad (4)$$

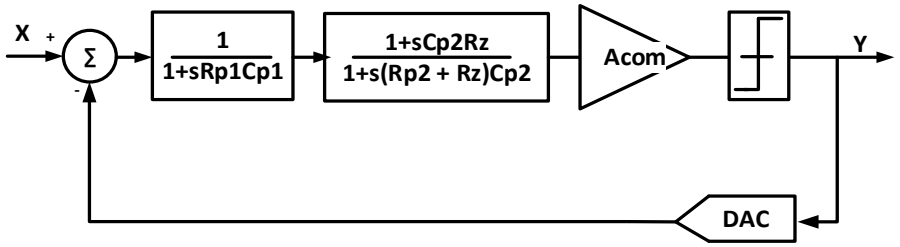
Equation (4) shows that the quantization noise can be suppressed with a high loop gain which is required for high-resolution ADCs. Thus, higher comparator gain is required for higher quantization noise suppression. As shown in Equation (3), to obtain a similar loop filter function, the pole capacitor of passive integrator needs to be bigger than the integrator capacitor of the active counterpart by a factor of the OPAMP gain. Clearly, this is not an advisable solution since it would result in an extremely large area, which is anathema in BIST



(a) Ideal Sigma Delta modulator linear model



(b) Linear model with active integrators



(c) Linear model with passive integrators

Fig. 4. Linear System Level Modulator Models

design. We propose to solve this problem by using a second-order loop filter, which divides the necessary loop gain over two different poles. A continuous time implementation of the proposed second-order passive SD modulator (PSDM) is illustrated in Figure 4, where R_{pi} is the resistor and C_{pi} is the integrating capacitor of the *ith* pole stage.

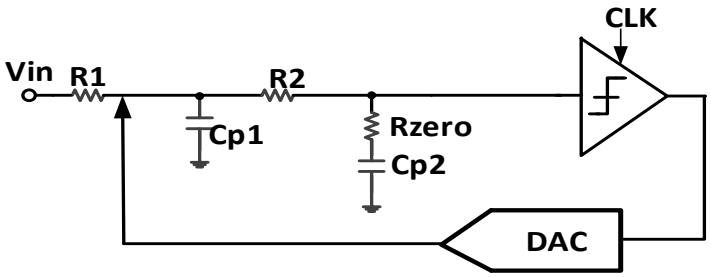


Fig. 5. The second order continues time sigma delta modulator

Figure 5 shows the system level models of three different second order continuous time SD modulators. Figure 5(a) shows the model of the ideal SD modulator, Figure 5(b) shows the model of a second-order implementation with an active integrator that uses Cascade of Integrators Feed Forward (CIFF) architecture, and Figure 5(c) shows the model of the proposed second-order passive sigma-delta modulator. T represents the sampling time period for the ideal integrator, a1, a2, b and c are coefficients. In active and passive sigma-delta modulators, coefficients and sampling time period are mimicked with R and C values. R_i is the resistor and Ci is the integrating capacitor of the i_{th} active RC integrator. In the active integrator model (Figure 5(b)), each continuous time integrator has a transfer function of A/1+AsRC. The feedforward path is used to ensure the stability of the system in ideal and active integrator based models; an additional resistor is required to generate the zero in the passive counterpart to ensure stability. In the passive SDM model, the equivalent gain of the comparator is expressed as A_{com}; the inter-stage loading is neglected for this model. If we assume that the comparator gain of the first order modulator in Figure 3 is equal to the second order modulator comparator gain in Figure 5(c), we can easily conclude that R and C values will be much smaller for the second order design. This is due to the fact that comparator gain will be divided into two different filter stages instead of

just one stage. As illustrated in Figure 5, the partitioning of the loop gain is the main distinction between passive SDM and active SDM. While the loop gain is partitioned into each pole sector among the integrators for active sigma-delta modulators, the comparator is the only gain provider for passive integrators. As a result, unlike the OPAMP based integrator in active modulators which need decisive linearity and gain, the preamplifier used in the PSDM does not need to be linear and DC gain requirement is relaxed.

This is one of the major advantages of the PSDM in terms of design automation since designing highly linear OPAMPs is challenging and requires extensive attention from the designers.

Noise Transfer Function (NTF) for a single feedback path sigma-delta modulator can be expressed as 1/1+H(s) where H(s) is the loop filter transfer function. Equations (4)-(6) summarize noise transfer functions for three different models for ideal, active, and passive sigma-delta modulators respectively.

$$NTFI(s) = \frac{Ts^2}{Ts^2 + Ta_2 s + ca_1} \quad (4)$$

$$NTFA(s) = \frac{A_1 A_2 R_1 R_2 C_1 C_2 s^2 + (A_1 R_1 C_1 + A_2 R_2 C_2)s + 1}{A_1 A_2 R_1 R_2 C_1 C_2 s^2 + (A_1 A_2 a_2 R_2 C_2 + A_1 R_1 C_1 + A_2 R_2 C_2)s + A_1 A_2 + A_1 a_2 + 1} \quad (5)$$

$$NTFP(s) = \frac{R_{P1}(R_{P2} + R_Z)C_{P1}C_{P2}s^2 + (R_{P1}C_{P1} + (R_{P2} + R_Z)C_{P2})s + 1}{(R_{P1}(R_{P2} + R_Z)C_{P1}C_{P2})s^2 + (A_{com}C_{P2}R_Z + R_{P1}C_{P1} + (R_{P2} + R_Z)C_{P2})s + A_{com} + 1} \quad (6)$$

In order to equate the noise transfer function of PSDMs to that of the active SDMs, we need to ensure that $A_1 = A_2 = \sqrt{Acom}$, $R_{p1}C_{p1} = R_1C_1\sqrt{Acom}$, $(R_{p2} + R_z)\, C_{p2} = R_2C_2\sqrt{Acom}$, and $RzC_{p2} = a_2R_2C_2$. Moreover, assuming $R_{p2} >> R_z$, and using ideal model

coefficients, sampling time, and quantizer gain, and passive filter elements can be directly calculated as presented in Table 1. PSDM RC product needs to be only $\sqrt{\text{Acom}}$ times larger compared to the active counterpart, while the RC product of the first order PSDM needs to be A_{com} times larger compared to the active counterpart. For even better area efficiency, switched-capacitor resistors can be used instead of area consuming MΩ range resistors [5, 22]. Figure 6 illustrates the full switched-capacitor implementation of the second-order PSDM.

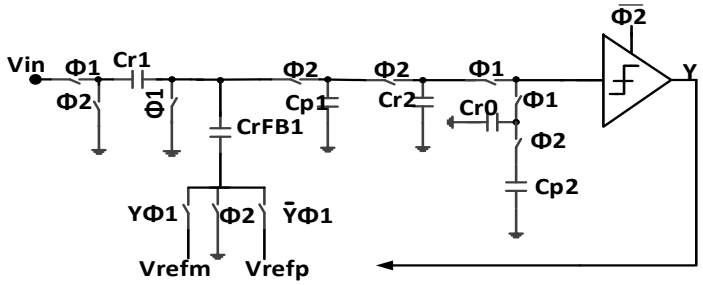


Fig. 6. Discrete-time PSDM

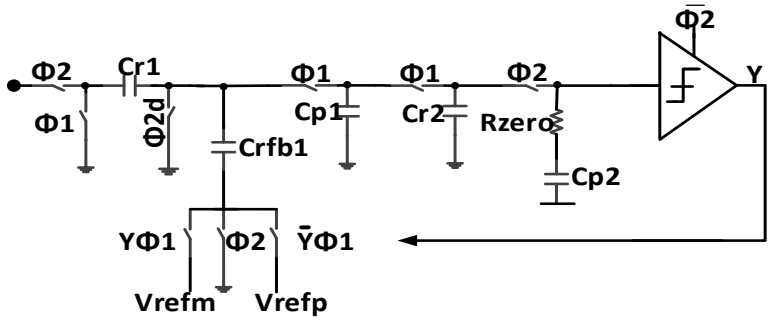


Fig. 7. Hybrid PSDM

In order to increase the gain of the PSDM with an appropriate noise transfer function, C_{p1} and C_{p2} need to be increased. Moreover, C_{r0} value is important because it sets the zero location in the loop transfer function. For PSDM implementation, the pole location needs to shift as the gain value changes, however, the zero resistor value, R_{zero}, is dependent

on C_{p2}. If we assume C_{r2} remains constant due to thermal noise specifications, the C_{p2} value needs to increase as much as gain increases. As a result, the equivalent resistance of C_{r0} needs to decrease in order to keep the NTF pole at the same location. Thus, the area of C_{r0} increases with the gain, clearly resulting in higher area overhead. In order to avoid this increase in the area overhead, while satisfying all the other requirements, we propose a hybrid second order loop filter which uses an actual resistor instead of a switched capacitor, C_{ro}, while other resistors, C_{r1} and C_{r2}, are implemented as switch capacitors, as shown Figure 7. Table 2 shows a discrete-time implementation of the loop filter, while Table 3 is showing the implementation details of the hybrid loop filter.

Table 1. CT Passive Filter

Comp.	Equation
R_{P1}	$\frac{T\sqrt{A_{com}}}{bC_{P1}}$
R_{P2}	$\frac{T(\sqrt{A_{com}}-a_2)}{a_1C_{P2}}$
R_{zero}	$\frac{a_2T}{a_1C_{p2}}$
C_{P1}	$\frac{T\sqrt{A_{com}}}{bR_{P1}}$
C_{P2}	$\frac{T(\sqrt{A_{com}}-a_2)}{a_1R_{P2}}$

Table 2. DT Passive Filter

Comp.	Equation
C_{R1}	$\frac{bC_{P1}}{\sqrt{A_{com}}}$
C_{R2}	$\frac{a_1C_{P2}}{(\sqrt{A_{com}}-a_2)}$
C_{R0}	$\frac{a_1C_{P2}}{a_2}$
C_{P1}	$\frac{C_{R1}\sqrt{A_{com}}}{b}$
C_{P2}	$\frac{C_{R2}(\sqrt{A_{com}}-a2)}{a1}$

Table 3. Hybrid Passive Filter

Comp.	Equation
C_{R1}	$\frac{bC_{P1}}{\sqrt{A_{com}}}$
C_{R2}	$\frac{a_1C_{P2}}{(\sqrt{A_{com}}-a_2)}$
R_{zero}	$\frac{a_2T}{a_1C_{p2}}$
C_{P1}	$\frac{C_{R1}\sqrt{A_{com}}}{b}$
C_{P2}	$\frac{C_{R2}(\sqrt{A_{com}}-a2)}{a1}$

3.2.2 Two Capacitor Serial Input Feedback DAC

Accurate and area efficient ADC design is crucial for BIST systems. Accuracy depends on two specifications, namely, SNR and linearity. Area efficient and high SNR design can be achieved using a high oversampling ratio, which enables us to use small input capacitors. However, if we employ the input capacitor as zooming DAC [32], the unit

capacitor size would be very small. For example, if we use 128fF input capacitor for 5-bit zooming, DAC unit capacitor is supposed to be only 4fF and this will cause high mismatch and nonlinearity problems where the implementation becomes infeasible. Dynamic Element Matching algorithms such as data weighted averaging will not be sufficient to overcome the mismatch and non-linearity generated by this small capacitor size.

Using a larger input capacitor is a solution to this problem with the penalty of the high area. Thus, we use a two-capacitor DAC architecture [47] in order to overcome this issue. The two-capacitor DAC architecture does not use an additional capacitor other than input capacitor and feedback capacitor but mimics the DAC operation by a special clocking scheme and additional switches. The feedback capacitor is used as the charging capacitor and the input capacitor is used as the redistribution capacitor. Algorithmic conversion is executed by employing charge redistribution over equal-valued capacitors. The two-capacitor DAC is also called as Serial DAC since the digital input is applied as a serial sequence to the redistribution capacitor starting from the LSB bit. Equation (7) expresses the change of the output voltage, where Vref is the reference voltage, di equals 0 or 1, and i stands for the i_{th} bit.

$$V_{i+1} = \frac{1}{2}(V_i + d_i V_{ref}) \quad (7)$$

When the sampling and charge is shared n times, the output voltage, Vout, can be obtained as in Equation (8)

$$V_{out} = \sum_{i=0}^{n-1} 2^{i-n} d_i V_{ref} \quad (8)$$

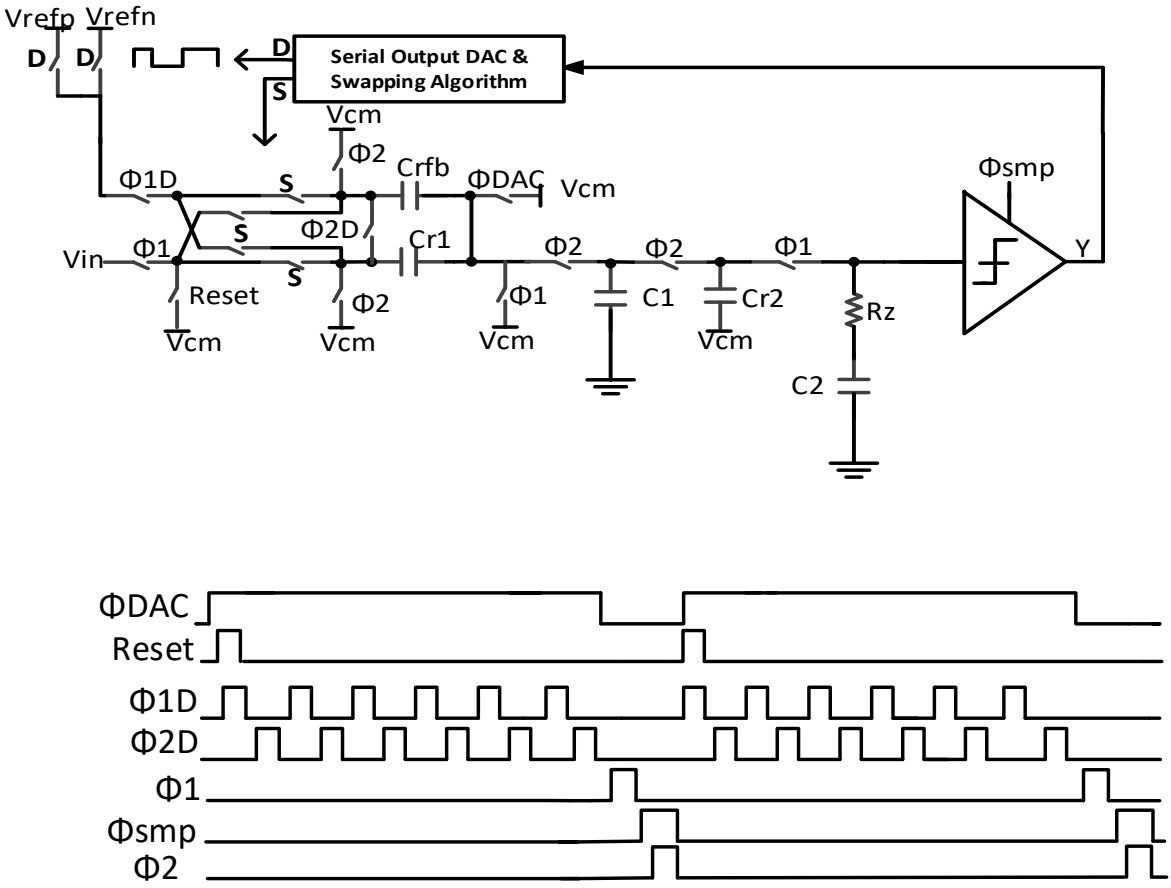


Fig. 8. Proposed PSDM with serial DAC

Algorithm 1. **CAPACITOR SELECTION ALGORITHM**

Input: Comparator output bit
Output: Input capacitor select bit (CapSel)
Initial assignments for the first run
CapSelOld [1:0] = "*Logic Low "* ; CapSel ="*Logic Low " ;*
repeat *each posedge clock*
if (*CompOut* = = "*Logic Low "*)
if (*CapSelOld* [0] = = *CapSel*)
toggle *CapSel* ;
toggle *CapSelOld [0]* ;
else
CapSel = *CapSelOld* [0] ;
toggle CapSelOld [0]
end
else
if (*CapSelOld* [1] = = *CapSel*)
toggle *CapSel* ;
toggle *CapSelOld [1]* ;
else
CapSel = *CapSelOld* [1] ;
toggle CapSelOld [1]
end
end

Although the capacitor mismatch between the two capacitors leads to a nonlinear DAC response, the compensative switching technique used in [25] resolves this issue. In this technique, the role of capacitors are interchanged for one full cycle and finally, two results are averaged using an operational amplifier. In our design, we do not need an operational amplifier for sampling and averaging due to the inherent averaging property of the sigma-delta modulator. Instead, we swap input and feedback capacitors for two consecutive runs for the same comparator output. The swapping algorithm is outlined in Algorithm 1.

Figure 8 shows the proposed PSDM and clock timing for the two-capacitor DAC PSDM. Initially, for the first cycle, on Reset or on $\Phi_{1D,}$ redistribution capacitor is reset to the ground while the charging capacitor is charged with the first digital bit and charge is shared between these two capacitors during Φ_{2D}. Next, on $\Phi_{2D\ D,}$ the charging capacitor is either charged with V_{refp} or V_{refn} depending on the next serial digital DAC bit. Then, the charge

is shared with redistribution capacitor on Φ_{2D}. This process is repeated 6 consecutive times until the zooming DAC value is stored in both capacitors. Next, the input capacitor is sampled with VIN (Φ_1) and the total charge in both capacitors is transmitted to the integrating capacitor in the next clock cycle (Φ_2). Finally, one cycle for PSDM is completed when the comparator output is stored in the latch during the Φ_{smp} phase.

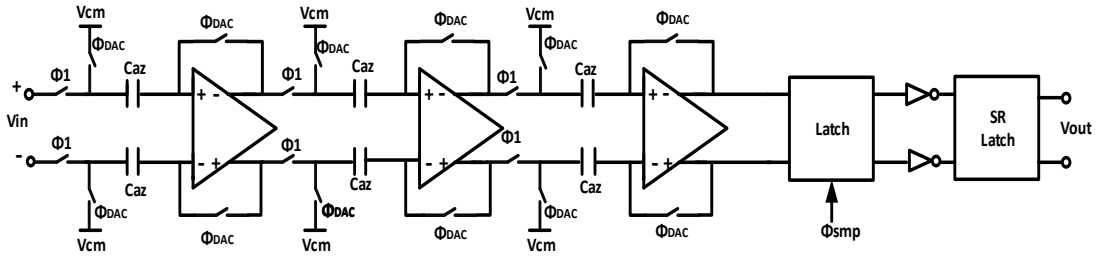


Fig. 9. Comparator Architecture

3.2.3 Single Bit Quantizer

A regenerative latch preceded by three preamplifier stages constitutes the comparator, as represented in Figures 9 and 10. Each preamplifier has a resistive load and uses auto-zeroing for offset and flicker noise cancelation.

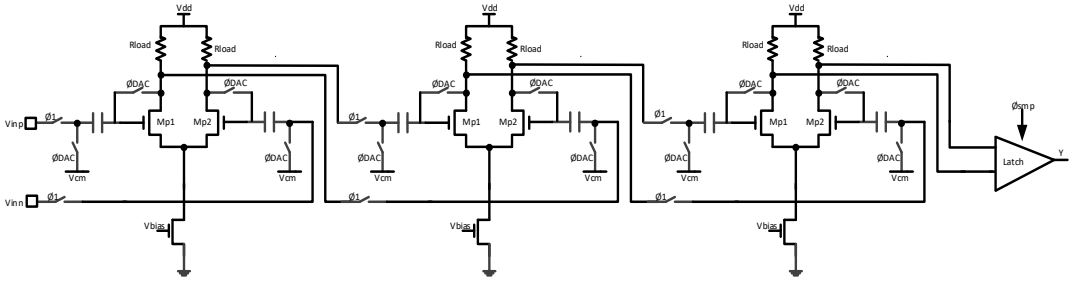


Fig. 10. Preamplifier Schematic level view

During the clock phase Φ_{DAC}, preamplifiers are in unity gain mode and the DC offset is stored in capacitors. During clock phase Φ_1, the input signal is amplified by preamplifiers, and at clock phase Φ_2, the latch captures the comparator output bit. For the feedback to be available in time, the valid digital code Y has to be determined before the beginning of next phase, Φ_{1D}. Using the simplified MOS transistor model, the gain of the single preamplifier stage can be expressed as in Equation (9).

$$G_p = g_m(R \,\|\, r_o) \approx gmR \approx \sqrt{K \frac{W}{L} I_{CM}} \left(\frac{VDD}{I_{CM}} \right) \quad (9)$$

The total gain of the comparator will be equal to the product of the gains of the three preamplifiers and the latch. We use the well-known Strong Arm latch architecture [25], shown in Figure 11, in our design. The strong arm latch is followed by an inverter

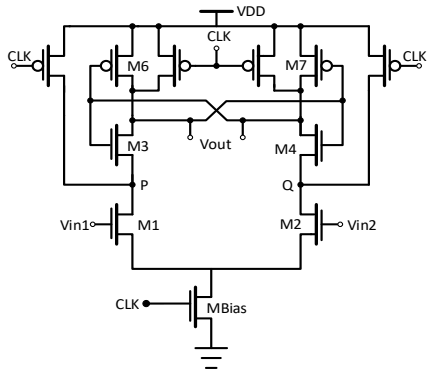


Fig. 11. Strongarm Latch

and SR latch stages. The gain of the strong arm latch is expressed in Equation (10) [46, 47], where I_{cm} is the common mode current drawn from each equivalent capacitance at P and Q points, $g_{m1,2}$ is the transconductance, and V_{THN} is the threshold voltage of transistors M1 and M2. Thus, the total gain can be evaluated as in Equation (11).

$$G_l = \frac{g_{m1,2} V_{THN}}{I_{CM}} \quad (10)$$

$$G = (g_{mpreamp} R_{load})^3 + \frac{g_{mlatch1,2} V_{THN}}{I_{CM}} \quad (11)$$

For the proposed design, Flicker noise is not an issue due to the auto-zeroing flicker noise cancelation approach. However, a disadvantage associated with auto-zeroing is that any noise component above the auto-zero bandwidth will alias into signal band due to the sampling action of auto-zeroing operation [48]. The in-band noise is expressed in Equation

(12), where v_n(white) is the thermal noise voltage, BW is the bandwidth of the auto-zeroing loop, and f_{az} is the frequency of the auto-zeroing operation [49].

$$v_{naz} = v_n(white)\sqrt{\frac{BW}{f_{az}}} \quad (12)$$

For complete cancellation of 1/f noise in amplifiers, the auto-zero frequency should be higher than the 1/f noise corner frequency. Since the oversampling ratio of the proposed ADC is expected to be high, noise folding effect will be neglected. Thus, the total input referred thermal noise of the comparator can be expressed as in Equation (13), where T is temperature, k is Boltzmann constant and gm is the transconductance of the gain stage.

$$v_{nth} = \sqrt{\frac{8kT\gamma\Delta_f}{g_m} + \frac{8kT\Delta_f}{g_m{}^2 R_D}} \approx \sqrt{\frac{8kT\gamma\Delta_f}{g_m}} \quad (13)$$

Another important parameter for the comparator is its propagation delay. During Φ_1, while the input signal is amplified by preamplifiers, the propagation delay should be less than Φ_1 pulse time. The latch delay, however, is not an issue since it is working during Φ_{smp} and minimum size devices can be used for the latch. The signal propagation delay through three preamplifiers can be expressed as in Equation (14), where C_{di} is the parasitic capacitor associated with *ith* stage of the preamplifier, C_{gi+1} is the gate capacitance of the next preamplifier stage, and I is the tail current[50].

$$t_d \approx \frac{VDD}{2}\sum_{i=1}^{3}\frac{C_{d_i} + C_{g_{i+1}}}{I} \quad (14)$$

3.2.4 Noise Analysis

Three noise sources are important for passive sigma-delta ADCs designed for low-frequency applications: quantization noise, flicker noise, and thermal noise. In this work,

flicker noise will be neglected thanks to the usage of precision techniques such as auto-zeroing and digital chopping. Thus, the total input referred noise power can be expressed as in Equation (15) [15, 16], where V^2_{nH1} and V^2_{nH2} are the thermal noise powers associated with first and second pole, respectively, V^2_{ncom} is the comparator input referred noise power, E^2_Q is the quantization noise power, H1 and H2 are transfer functions for first and second passive filters, respectively, and A is the comparator gain.

$$V^2_{n,total} = V^2_{n,H_1} + \frac{V^2_{n,H_2}}{H_1^2} + \frac{V^2_{n,COM}}{H_1^2 H_2^2} + \frac{E^2_Q}{A_{com} H_1^2 H_2^2} \quad (15)$$

For SNR calculations, in-band noise after the decimation filter is important. Thus, we focus on in-band noise, V^2_{nH1}, which can be evaluated as in Equation (16), where $V^2_{n\Phi 1D}$ and $V^2_{n\Phi 2D}$ are generated during two capacitor DAC clock phases and $V^2_{n\Phi 1}$ and $V^2_{n\Phi 2}$ are generated during PSDM operating clock phases, which is six times slower than the DAC operating frequency. Since there are two different clock frequencies, we need to use two different OSR values while calculating the in-band noise power. The noise generated during Φ1D for fully differential input is expressed in Equation (17), and the noise generated during Φ2D, due to two parallel capacitors, can be expressed in Equation (18). Finally, the noise generated during Φ1 is expressed in Equation (19).

$$V^2_{n,H_1} = V^2_{n,\Phi_{1D}} + V^2_{n,\Phi_{2D}} + V^2_{n,\Phi_1} + V^2_{n,\Phi_2} \quad (16)$$

$$V^2_{n,\Phi_{1D}} = \frac{2kT}{C_{rfb} OSR_{DAC}} = \frac{2kT}{C_{r1} OSR_{DAC}} \quad (17)$$

$$V^2_{n,\Phi_{2D}} = \frac{kT}{C_{r1} OSR_{DAC}} \quad (18)$$

$$V^2_{n,\Phi_1} = \frac{2kT}{C_{r1} OSR} \quad (19)$$

During Φ2, feedback and input capacitors are parallel and connected to C_{p1} in series. C_{p1} is much larger than C_{r1}. Thus, the noise generated during Φ2 can be approximated as in Equation (20).

$$V^2_{n,\Phi_2} \approx \frac{kT}{C_{r1}OSR} \quad (20)$$

There are 6 OSR_{DAC} cycles in one sigma-delta modulator oversampling ratio OSR. Thus, the whole pole one sector associated noise can be expressed as in Equation (21):

$$V^2_{n,H_1} \approx \frac{21kT}{6C_{r1}OSR} \quad (21)$$

Similarly, for the second pole sector, total in-band noise V^2_{nH2} can be obtained the as in Equation (22), where R_z represents zero resistor in series to $C_{p2,}$ C_{r2} represents the zero emulating resistor, and thermal noise associated with the comparator is expressed in Equation (23).

$$V^2_{n,H_2} = V^2_{n,\Phi_1} + V^2_{n,\Phi_2} + V^2_{nR_Z} \approx \frac{2kT}{C_{r2}OSR} + \frac{2kT}{C_{r2}OSR} + 4kTR_Z\Delta_f = \frac{4kT}{C_{r2}OSR} + 4kTR_Z\Delta_f \quad (22)$$

$$V^2_{n,com} = \frac{16kT\Delta_f}{3g_m} + \frac{8kT\Delta_f}{g_m{}^2R_D} \quad (23)$$

The system is designed to have negligible quantization noise since the quantization noise will be suppressed due to loop gain and zooming.

3.2.5 ADC Driving Conditions for DUT

A common problem for ADCs is driving capabilities of DUT (Design Under Test). Mostly this issue is resolved by adding a buffer stage between ADC and DUT. However, since area efficiency is very crucial for BIST applications, we investigated a buffer-less solution option for the synthesis. In order to employ a buffer-less solution, the output

impedance of the DUT should be small enough to drive the ADC without any performance degradation. In other words, the output impedance of DUT (Z_{out}) should be very small compared to the ADC input impedance (Z_{in}) in order to avoid any loading on the primary circuit. In this context, a maximum ratio of 1/10 is often used as a design rule of thumb. Although Zin (Input Impedance) is frequency dependent, in our topology, the worst case Zin occurs when the pole capacitor impedance is minimum (at high frequencies). In this case, the input impedance can be approximated as $Z_{in} \approx R_{eq}$. As the resistor, Req is implemented by a switched capacitor circuit (Cr1), the worst case Z_{in} can be expressed as in Equation (24).

$$Z_{in} \approx \frac{T}{C_{r1}} \quad \text{where} \quad Z_{in} \geq 10 * Z_{out} \qquad (24)$$

Thus, the maximum acceptable capacitance (C_{r1}) can be extracted as in Equation (25).

$$C_{r1} \leq \frac{T}{10 * Z_{out}} \qquad (25)$$

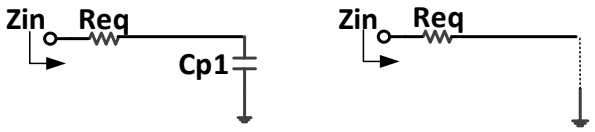


Fig. 12. Worst Case Zin

3.2.6 Precision Techniques

DC offset is a very important phenomenon which directly affects ADC accuracy. There are two major causes of the DC offset; mismatch and flicker noise. Flicker noise is dominant at lower frequencies compared to thermal noise. DC offset can be decreased simply by increasing the device sizes, which will decrease their flicker noise. However, it

will result in large area overhead and speed degradation due to increased parasitic capacitances. Instead of using larger input transistors, we use two-step protection to resolve flicker noise and DC offset problems. The auto-zeroing technique is used to effectively cancel offset in comparators. Digital system level chopping is employed to cancel remaining system level offset. In this procedure, after the initial conversion, first results are saved. Then, input signal polarities are swapped and the overall conversion is performed once more. Finally, conversion results are averaged digitally. Although system level chopping doubles the conversion time by an extra conversion step, it also improves the overall SNR by 3dB [14].

Another important phenomenon which effects ADC accuracy is linearity. Due to the highly linear nature of passive sigma-delta modulator with single bit quantizer, the main source of nonlinearity is the two-capacitor serial DAC. Nonlinearity is caused by the mismatch between the capacitors. As explained in Section 2.2, we use the swapping method to overcome the mismatch. The total mean square error for averaging of two consecutive runs with swapped capacitors can be determined using Equation (26) [51].

$$E_{RMS} \approx 0.21\delta^2 2^n LSB \quad (26)$$

Equation (26) shows with a worst case mismatch of 0.1% and for a 6-bit DAC, we can theoretically achieve an error level of 2 ppm.

3.2.7 Digital Decimation Filter

The digital decimation filter takes the 1-bit modulator output as its input and filters out the out-of-band quantization noise and unwanted out-of-band signals present in the modulator's analog input. We use the well-known sinc^n filter for our design, which can be

represented with the transfer function as in Equation (27), where z is associated with the high output sampling frequency of the stage, N is the interpolation factor, k the ratio of the output and input sampling rates, it can be also called decimation ratio. In this work, we use a third order $sinc^3$ filter. The decimation filter is not implemented at the transistor level as this function can be implemented at the tester.

$$H(z) = \left[\frac{(1 - z^{-N})}{N(1 - z^{-1})} \right]^k \quad (27)$$

3.2.8 Coarse SAR ADC

For BIST applications, the input is low-frequency, it will remain constant during conversion time. Therefore, coarse and fine conversion operations can perform sequentially and share the required circuit blocks in order to save area. As explained earlier, using a unit capacitor-based charge sharing DAC will not be a viable solution since the resulting unit capacitor will be too small and the mismatch will cause high nonlinearity. Instead, we can employ the two capacitor DAC for SAR conversion and total conversion time will be cycles where N is a number of bits. Thus, instead of employing a small Cri as a unit capacitor DAC, we use Cp1 and Cp2 capacitors in parallel as a binary sized DAC, as shown in Figure 13. The quantizer is also shared between the two conversions. The

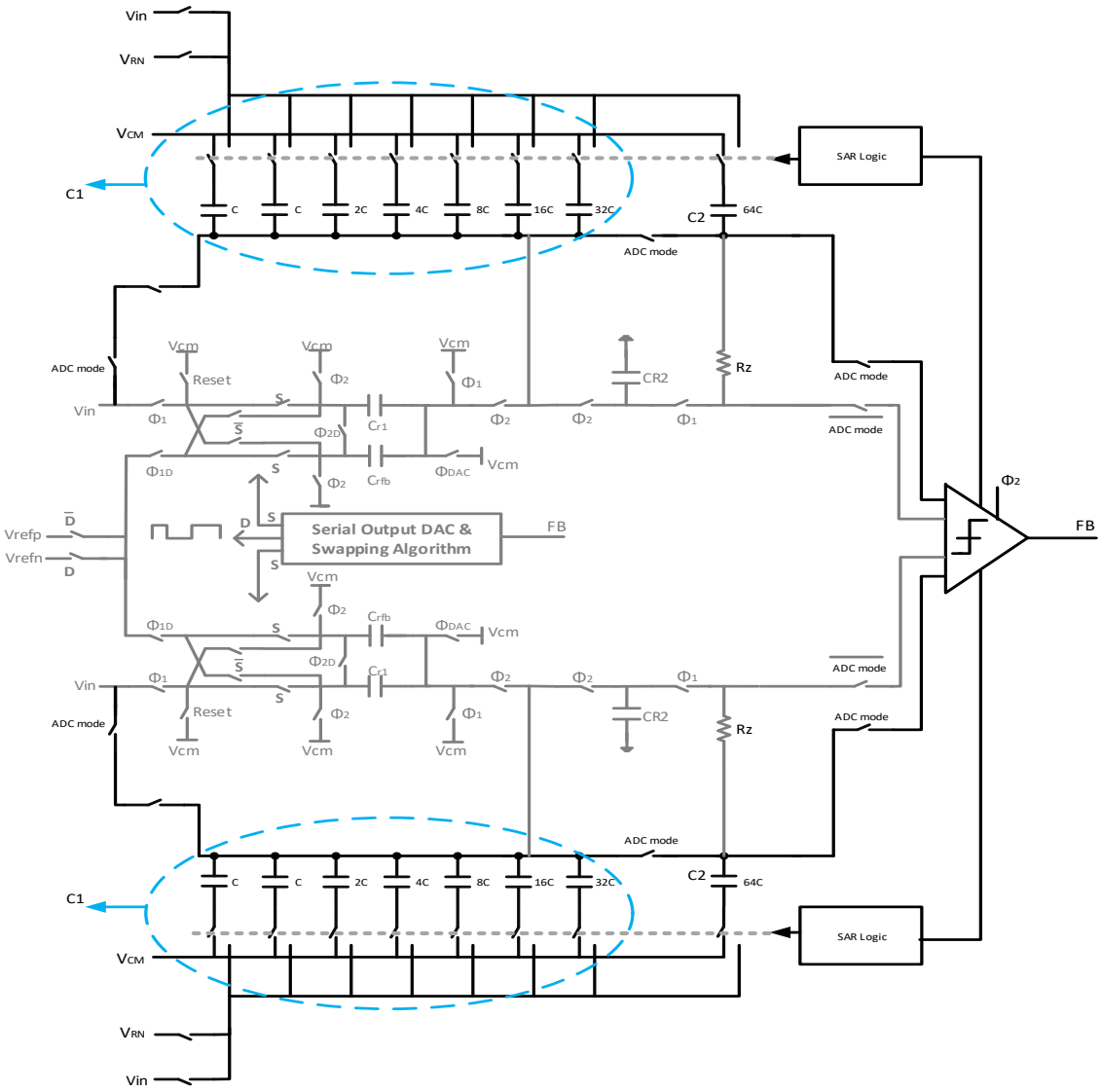


Fig. 13. Fine Zoom PSDM and Coarse SAR ADC

actual implementation employs a differential configuration. Although the feedback DAC resolution is 6 bits, we use a 7 bit coarse ADC to make VI approximately in the middle of the zooming range. At the start of each comparison step, the input signal is sampled on all the capacitors of the Capacitor-DAC, while comparator is auto-zeroed and reset. The sampled value is then compared to a weighted sum of the references. In seven comparison

steps, the coarse result is obtained such that the condition is given in Expression (28) [30] is met.

$$k.V_{LSB,SAR} < V_i < (k+1)V_{LSB,SAR} \quad (28)$$

In Expression (28), if *k* is an odd number, we add 1 and then divide the sum by 2 to find *n*, *i.e.* the coarse DAC setup coefficient. If *k* is an even number, we directly divide *k* by 2 to find *n*. Then, the coefficient *n* is stored in the SAR register and used to reconfigure the references of the sigma-delta ADC DAC as (*n – 1*) and (*n+1*).

3.3 Design Automation

Ideally, the design of the BIST ADC would not require an experienced designer. The steps involved in the design of the proposed architecture are: (a) determining a suitable noise transfer function (NTF), (b) fitting the required coefficients, (c) verifying the stability of the system, and (d) acquiring the specifications of the circuit and desired active and passive element sizes.

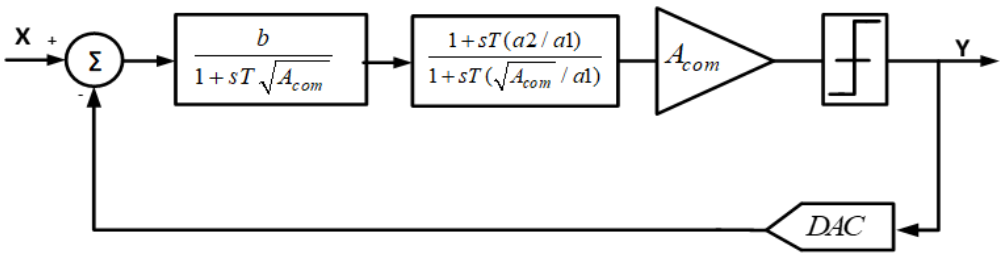


Fig. 14. The model used for system level simulations

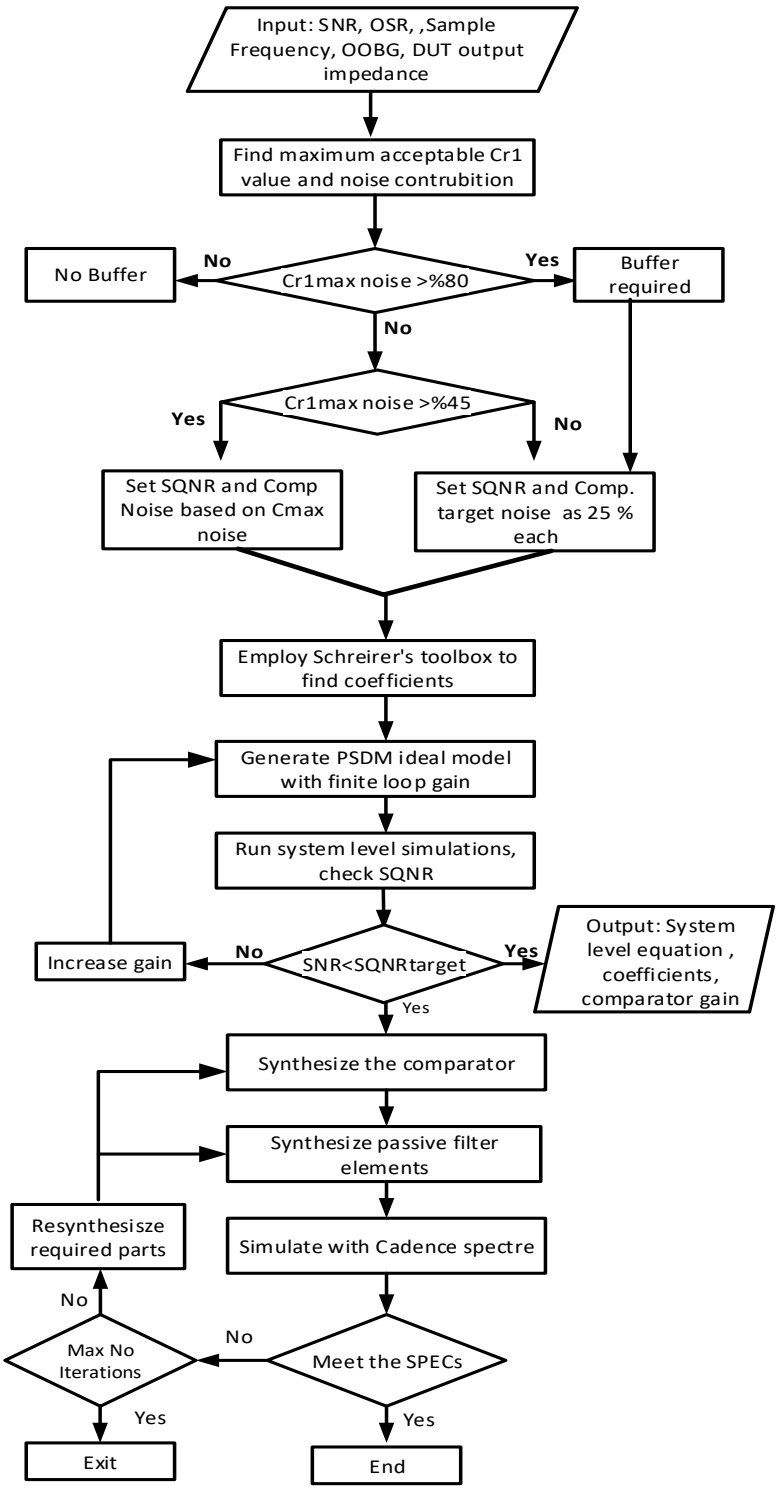


Fig. 15. Top level flow chart

3.3.1 System Level Synthesis

The proposed synthesis flow uses Matlab with Cadence Spectre APS simulation environment to complete the entire design. Figure 15 illustrates the hierarchical top-down design flow for the proposed ADC.

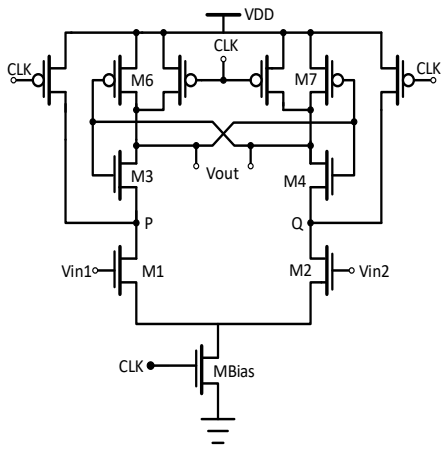
As a starting point, we set an SNR margin of 3dB to account for non-idealities, such as layout parasitics. Next, based on the DUT output impedance, we find the maximum acceptable C_{r1} value (C_{r1max}) and associated passive element noise contribution. Using passive element noise contribution percentage, we determine the target quantization noise and comparator noise and whether a buffer will be necessary between the DUT and the ADC. If the noise contribution of passive elements for C_{rmax} is more than 80%, we decide that a buffer is required. Otherwise, a buffer is not necessary. Since this paper mainly focuses on ADC synthesis, we do not concentrate on buffer synthesis. In the rare case where the DUT has a high output impedance and the buffer becomes necessary, it will have to be designed separately after the design of the DUT and ADC are complete. Next, we set target noise contributions for quantization and comparator noise. If the noise contribution of passive elements is less than 80% but more than 50% when C_{rmax} is used, we calculate the target noise contributions as in Equation (29). In Equation (29), $E_{Qtarget}$ and $E_{COMtarget}$ represent quantization and comparator target noise powers, E_{Total} represents total noise power, and E_{Hmax_cap} represents noise power of passive filter when the maximum acceptable capacitor is used.

$$E_{Q_{target}} = E_{COM_{target}} = \frac{E_{Total} - E_{H_{max\_cap}}}{2} \quad (29)$$

If the noise contribution of passive elements is more than 80% or less than 50%, there is room to use smaller capacitors. Therefore, both quantization and comparator target noises are set to 25%. The design process is completed using MATLAB modeling. After determining the NTF, the ideal system level coefficients (a1, a2, b) are extracted using Schreier`s toolbox "synthesizeNTF" and "realizeNTF" functions [41]. The CIFF (Cascade Integrator Feed Forward) architecture and 2^{nd} order loop filter are used as default inputs for the functions. Passive modulator components are determined using a custom MATLAB code. Figure 14 shows the system level *S* domain model of the PSDM after initial coefficient synthesis step. This model is used for system level simulations. *S* domain modeling is used for simulations since it provides faster simulation results compared to Z domain transfer function simulations. As explained in Section 2, the loop gain is the crucial parameter to suppress quantization noise. Thus, we need to determine the minimum loop gain required for sufficient SQNR, for which we use an iterative method. The design specifications are target Signal to Quantization Noise Ratio (SQNR), clock frequency, input capacitors, and OSR. We first start with 50dB comparator gain and run system-level simulations to obtain the corresponding SQNR value. The gain is progressively decreased or increased by 3dB depending on the resulting SQNR value. This process yields the system level transfer function, coefficients, loop gain, and maximum acceptable noise power as outputs.

3.3.2 Comparator Synthesis

There are three important specifications for the comparator, namely, comparator gain, input referred noise, and propagation delay. In this work, we use a hybrid synthesis



Device sizes	
W_{M1M3}	8xLmin
L_{M1M3}	Lmin
W_{tail}	16xLmin
L_{tail}	Lmin
W_{M4M5}	2xLmin
L_{M4M5}	Lmin
W_{pmos}	4xLmin
L_{pmos}	Lmin

Fig. 16. Strongarm Latch and Device sizes

method combining knowledge-based and simulation-based approaches for comparator synthesis, as shown in Figure 16. The comparator synthesis tool uses Cadence Spectre APS for circuit-level simulations and a custom MATLAB code to process the output and make the required changes to the circuit components. We use a single bit quantizer consisting of three preamplifiers followed by a latch. Synthesis of the comparator starts with determining g_m to meet noise requirements. As a starting point, the tool with the help of target comparator noise and Equation (13) extracts the required preamplifier g_m value. Next, the latch is synthesized using minimum device length sizes for both NMOS and PMOS transistors in order to minimize the delay. Latch devices are generated as a rule of thumb and are not subject to change. All device widths are presented in Figure 16 and they are generated independently of ADC design requirements. Once the latch gain is determined using simulations, the required total gain for preamplifiers can be calculated by subtracting Latch gain from target gain. In our architecture, we used three cascaded equivalent preamplifier stages, thus, the required gain for one preamplifier stage will be one-third of the total preamplifier gain. Next, the R_{load} value is determined using Equation (9) and

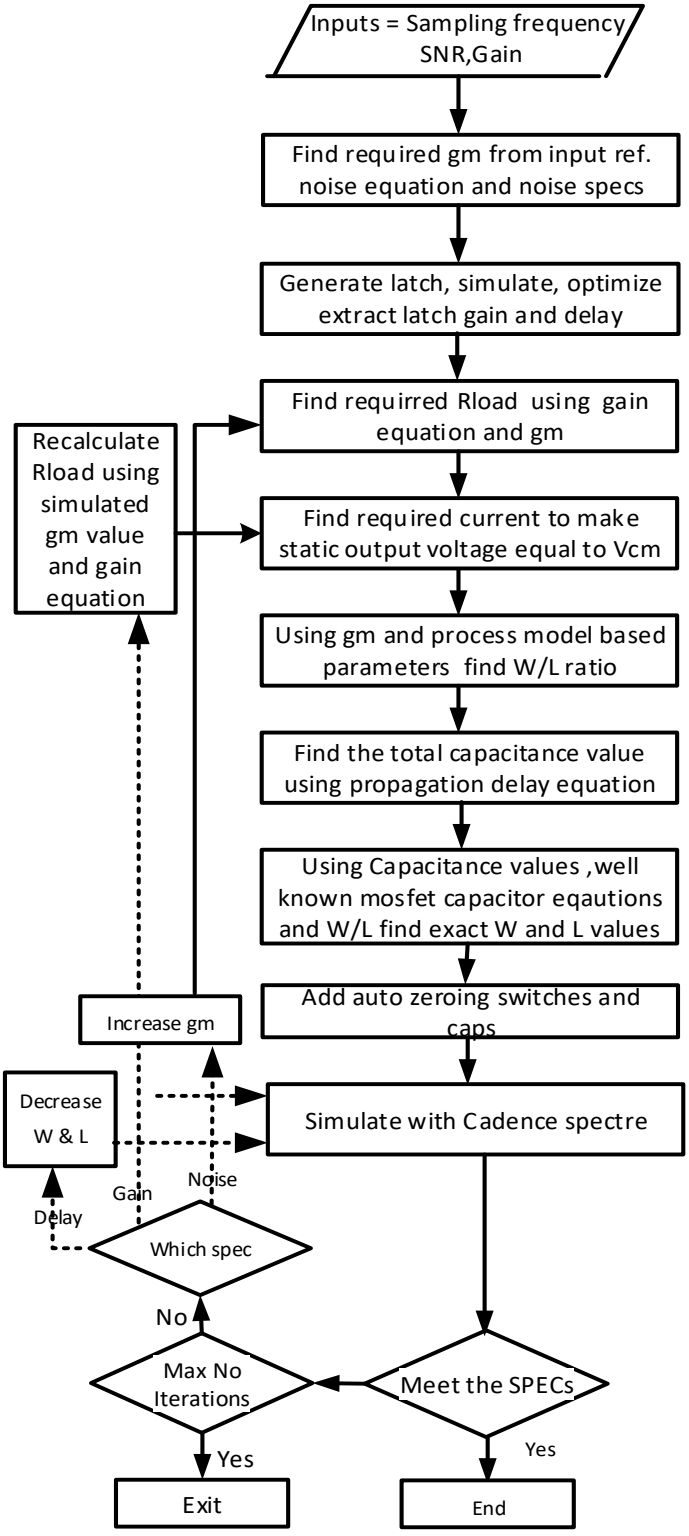


Fig. 17. Comparator synthesis flow chart

preamplifier gm value. The total current consumption for a single preamplifier can be formulated as $I = VDD/R_{load}$ to make output common mode voltage equal to V_{cm} (VDD/2). The required current is calculated using this equation. Next, the W/L ratio is determined to provide the target current and gm values. The propagation delay needs to be less than the Φ1 pulse duration. On the one hand, using smaller input transistor length will result in faster operation, which is desirable. On the other hand, using very small sized transistors leads to higher mismatch and flicker noise, which is not desirable. However, since flicker noise will be canceled to some degree thanks to auto-zeroing and digital chopping techniques, it is less of a concern. Therefore, we use the biggest W and L values that will still result in an acceptable delay. After adding auto zeroing switches in the netlist, the initial design of the comparator is completed. Next, the entire comparator circuit is simulated to determine comparator performance. If the target performance is not met, circuit components are modified based on which specification has not been met, as shown in Figure 17. To improve propagation delay, W and L values need to be decreased while keeping W/L ratio same. If the gain specification is not met, the R_{load} value is increased. Finally, if noise specification is not met, gm value can be increased.

3.3.3 Passive Elements Synthesis

Based on comparator synthesis results, the loop transfer function might be updated due to loop gain change. Passive elements synthesis starts with noise optimization. As the comparator noise is extracted through simulations, remaining noise budget can be calculated using Equations (14) through (23), where flicker noise can be neglected as

previously explained. The tool calculates the required C_{r1} and C_{r2} values to meet the SNR requirements. Next, the tool checks if C_{r1} is larger than C_{rmax}. If it is larger, then C_{r1} is set to C_{rmax} and equations in Table 3 are used to calculate the values of the rest of the passive devices. C_1 needs to be equal to C_2 to generate the Binary weighted SAR ADC. If a buffer is required, the tool sets the C_{rmax} value to infinity, hence there is no limitation on C_{r1} value.

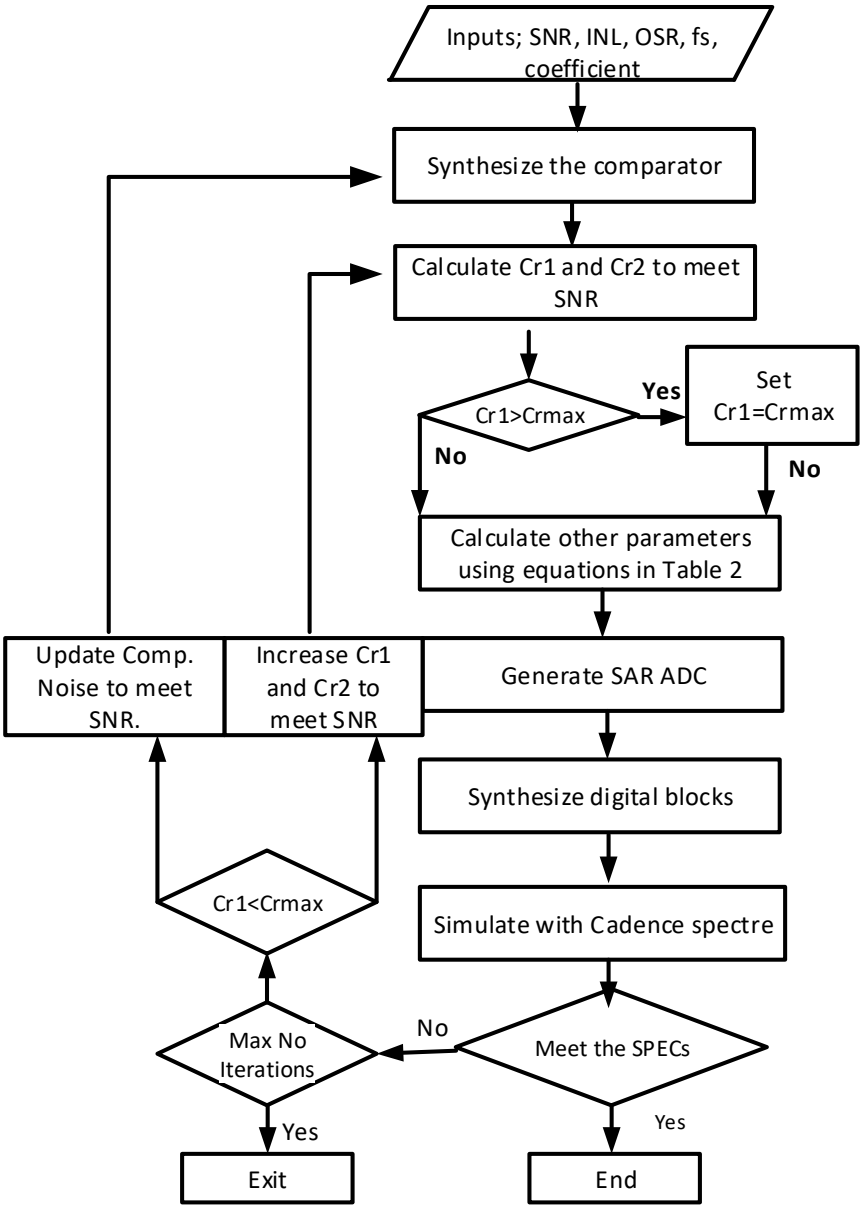


Fig. 18. Passive filter synthesis flow chart

In order to leave enough margin for additional noise due to layout parasitics, the SNR target is set at 3dB above the actual target. In order to realize the SAR ADC, the capacitor C1 is separated into binary segments and required switches are placed on the netlist. Next, all digital circuits are synthesized using RTL synthesis tools. Finally, the entire ADC is simulated using Cadence Spectre APS (Accelerated Parallel Simulator). SNR and INL parameters are extracted and compared with the specifications. If specifications are not met, and the capacitor values did not reach to C_{rmax}, capacitor values are increased. If the capacitor value is already at C_{rmax}, the required noise specification for the comparator is recalculated and the comparator is resynthesized. Simulations are repeated until design specifications are met. Increasing capacitor size helps improve both SNR and INL results. Figure 18 illustrates the Passive elements synthesis algorithm.

3.4 Example Designs

In this section, we present two different ADCs designed in 65nm CMOS process using our design automation system. In the first design, the required SNR is 90dB (15 bits), the required measurement time is 512μs and the DUT output impedance is set as 100kΩ. In the second design, the required SNR is 78 dB (13 bits), the clock frequency is 16 MHz, and the

Table 4. ADC Input Specs

ADC	SNR	OSR	Fs	INL	O0BG	DUT-Max Out Impedance
1	90 dB	1024	4 MHz	<1 LSB	2	100K
2	78 dB	256	16 MHz	<1 LSB	2	100K/10M

required measurement time is 31.25μs. We set the DUT output impedance to 100kΩ and 10MΩ in two different runs. Table 4 summarizes the target specifications for both ADCs.

A UNIX server with a Quad-Core Intel Xeon X3210 2.13 GHz processor is used to synthesize the ADCs. The entire synthesis time including the computation of system coefficients and comparator and passive filter synthesis is 313s for the first ADC and 286s for the second ADC. The synthesized ADC is simulated at the system level as a final verification. The simulation time for this step is long (72hr), as it would be in a regular

Table 5. ADC 1 Synthesis Results

System coefficients		Preamplifier		Latch		Passive Filter		Noise Contribution	
a1	1.2	Wp	4um	W_{M1M3}	520nm	Cr1	250fF	Passive Filter	56%
a2	0.66	Lp	130nm	L_{M1M3}	65nm	Cr2	211fF	Quantization	22%
b	1	Rload	650K	W_{tail}	1.04μm	C1	10.5pF	Comparator	22%
c	1	Icm	2μm	L_{tail}	65nm	C2	10.5pF		
T	25μs	VDD	1.3 V	W_{M4M5}	130nm	Rz	13K		
Acom	65 dB			L_{M4M5}	65nm	Input Impedance	1 M ohm		
Crmax	250fF			W_{pmos}	260nm				
Buffer	NO			L_{pmos}	65nm				

Table 6. ADC 2 Synthesis Results

System coefficients	100k	10M	Preamplifier		Latch		Passive Filter		Noise Contribution	
a1	1.2	1.2	Wp	2μm	W_{M1M3}	520nm	Cr1	50f	Passive Filter	48%
a2	0.66	0.66	Lp	130nm	L_{M1M3}	65nm	Cr2	43f	Quantization	26%
b	1	1	Rload	200K	W_{tail}	1.04um	C1	1.5p	Comparator	26%
c	1	1	Icm	6.5μA	L_{tail}	65nm	C2	1.5p		
T	6.25 μs	6.25 μs	VDD	1.3	W_{M4M5}	130nm	Rz	23K		
Acom	59 dB	59 dB			L_{M4M5}	65nm	Input Impedance	1 .25M ohm		
Crmax	65 fF	0.65 fF			W_{pmos}	260nm				
Buffer	NO	YES			L_{pmos}	65nm				

ADC design process. However, transistor-level simulation of the entire ADC is encountered only at the end of the synthesis step. Usually, when a similar schematic level

ADC is designed by a designer , design time is subject to change 2 to 10 weeks depending on designers experience. Compare to a circuit designers manual design time, automation tool completes the desing between 75 to 95 percent faster productivity rate. Thus the tool gives 75 to 95 percent much better productivity rate.

Performance parameters for the synthesized designs are presented in Table 5 and Table 6. The first ADC is an example for a slower but more accurate design while the second ADC is faster and more area efficient, albeit with a smaller SNR. The first ADC passive filter noise contribution is more than 50% hence target noise contributions are set using Expression (28) and a buffer is not required. For the second ADC, the tool returns two different C_{rmax} values for two different loading conditions. For the 100KΩ DUT output impedance condition, E_{Hmax_cap} is less than %50, a buffer is not required. However, for the

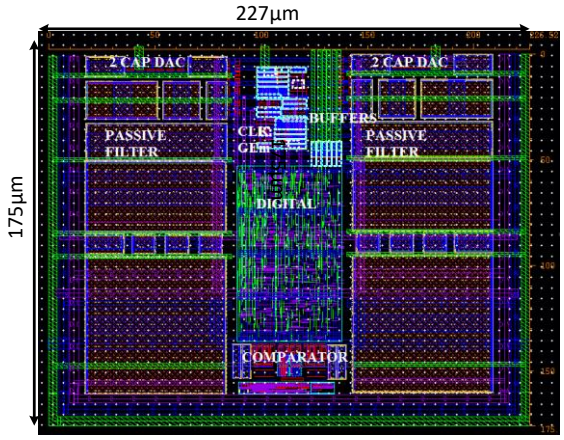


Fig. 19. ADC1 Layout

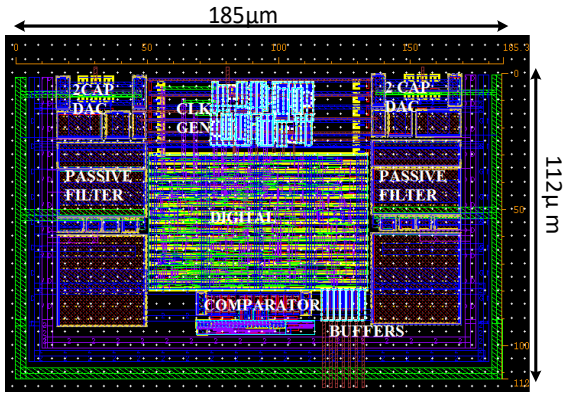


Fig. 20. ADC2 Layout

10MΩ DUT output condition, E_{Hmax_cap} is more than %80 requiring a buffer between the DUT and the ADC input. Note that this output impedance value is extremely high, but it is

used for demonstration purposes. Other ADC parameters are identical since quantization and comparator target noise contributions are set to 25% for both loading conditions. Both ADCs are designed at the layout level in order to estimate the total layout area and to run extracted level simulations. MIM (Metal Insulator Metal) caps used for area efficiency. The layout for the two ADCs is given in Figure 19 and Figure 20. The total area of first ADC is 0.0397 mm^2 and the total area of the second ADC is 0.02 mm^2

Post-layout simulations are conducted to confirm that the ADCs meet the desired performance. Both ADCs are driven by a voltage source with 100KΩ impedance to model the specified DUT loading conditions. Figure 21 shows the FFT plot for ADC 1 for full scale (2.4 Vpp) input and 0V differential input while Figure 22 shows the FFT plot for ADC 2. Simulated SNR is equal to 91.5dB and 78 dB respectively. In order to evaluate the dynamic performance of the ADCs, sine-wave signals applied to the ADC. The simulated power spectrum is illustrated in Figure 23 and Figure 24 for -1dBFS full-scale input. 100-Hz and 500 Hz sine wave inputs are applied to ADC 1 and ADC2 respectively. Another important parameter is integral non-linearity.

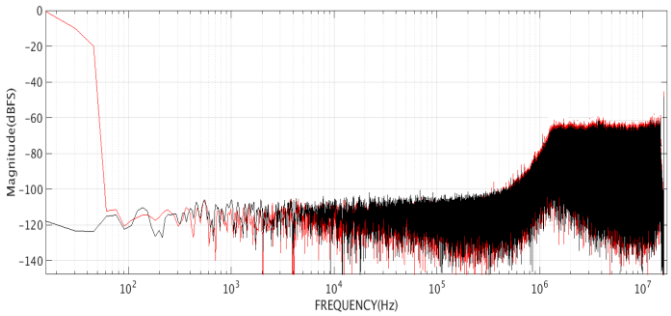


Fig. 21. ADC1 SNR 91.2dB (Red full-scale input, black no input, 2^{20} samples FFT)

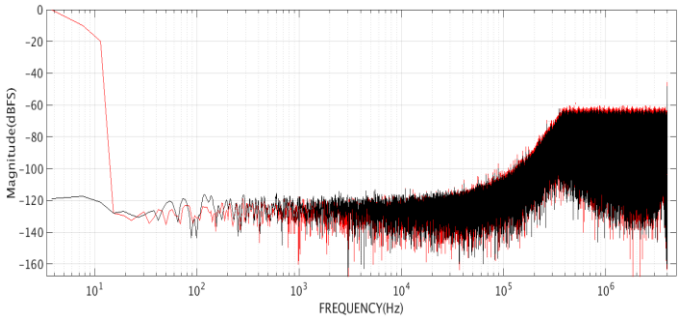


Fig. 22. ADC1 SNR 78.8dB (Red full-scale input, black no input, 2^{20} samples FFT)

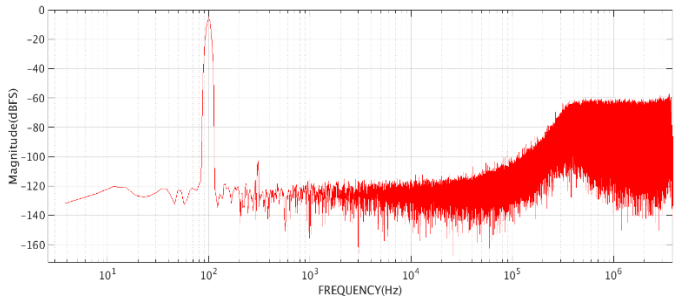


Fig. 23. ADC1 Simulated SNDR 87.9dB at -1.dBFS input, 2^{20} samples FFT

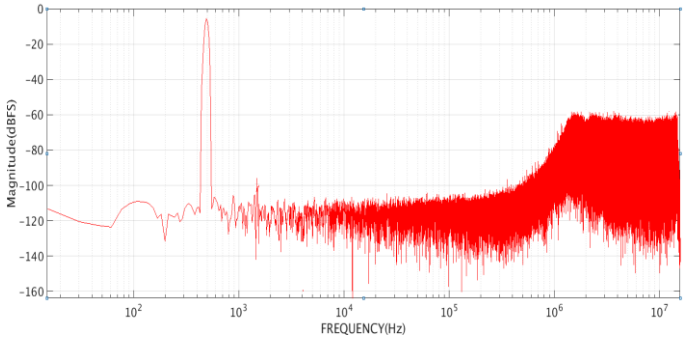


Fig. 24. Simulated SNR 76.9dB at -1dBFS input, 2^{20} samples FFT

Figures 25 through 28 show INL results for 250 Monte Carlo runs with swapping algorithm and without swapping algorithm. DC offset Monte Carlo simulation results for 250 runs for both ADCs are presented in Figures 29 and 30. Thanks to digital chopping and auto-zeroing approaches, the DC offsets are in µV range.

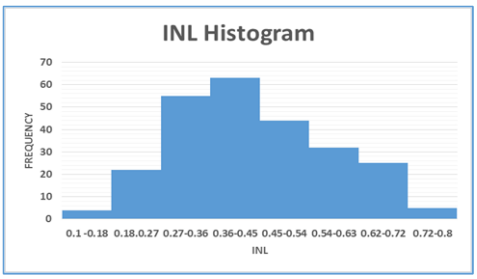


Fig. 25. 15 b. ADC INL with swapping

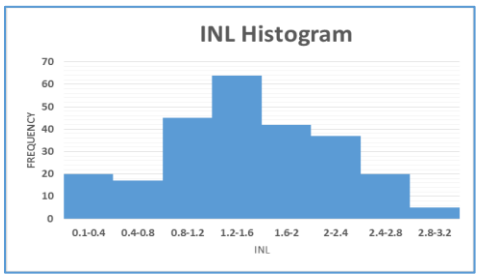


Fig. 26. 15 b. ADC INL without swapping

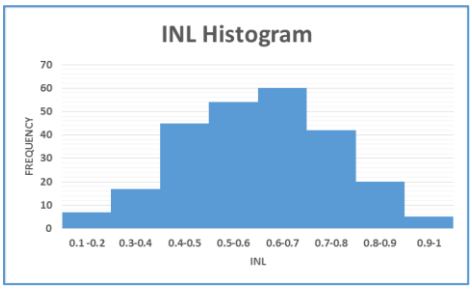


Fig. 27. 13 b. ADC INL with swapping

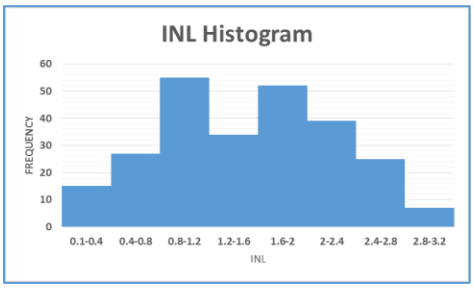


Fig. 28. 13 b. ADC INL without swapping

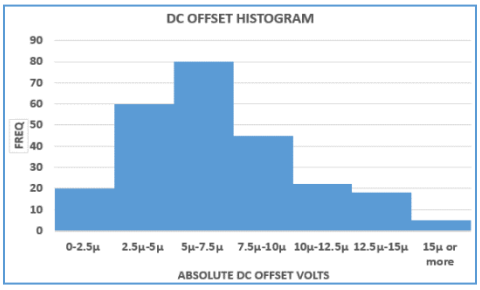


Fig. 29. DC offset Histogram for ADC1

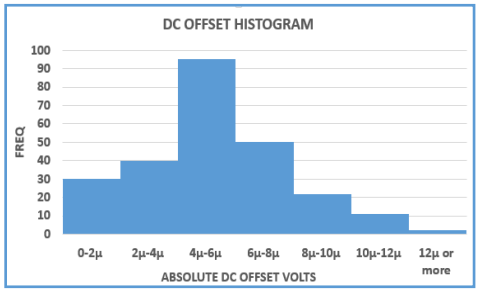


Fig. 30. DC offset Histogram for ADC2

The synthesized ADCs consume 12µW and 48µW respectively. The power consumption is broken down into various components, as presented in Figures 31 and 32. Power consumption is mostly due to dynamic switching, which includes all digital components and latches. Due to the higher percentage of dynamic power, power consumption is highly scalable with technology. The area share of digital circuits is around 13% and 25% of the total area for ADC1 and ADC2 respectively. Therefore, the overall area of the ADC is not as scalable as power. Scaled power and area estimates are presented

in Figures 33 and 34 with respect to technology node. For these estimations, the area and power associated with analog blocks assumed to be constant, whereas the area and power of digital blocks are scaled based on Moore`s law and Intel process technology measurement data [52]

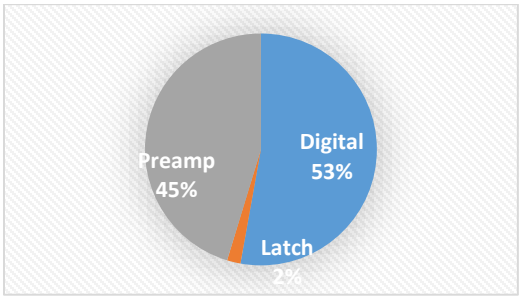


Fig. 31. Power Breakdown ADC1

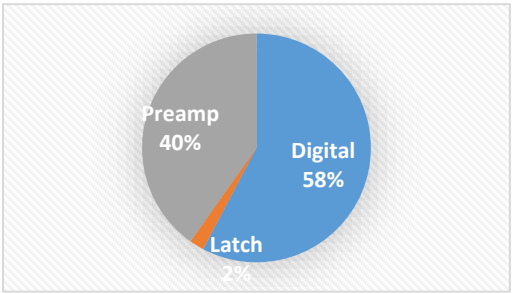


Fig. 32. Power Breakdown ADC2

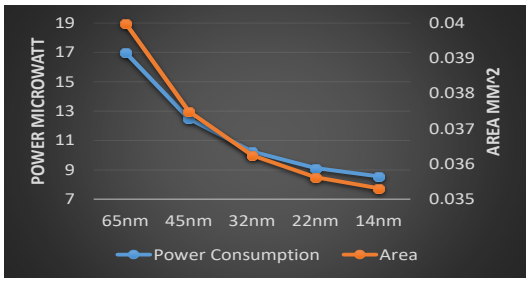


Fig. 33. Technology Scale ADC1

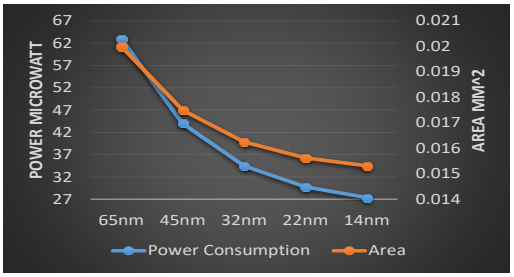


Fig. 34. Technology Scale ADC2

The tool provides the full schematic design of passive sigma-delta ADC. The analog layout is done manually. Although the tool provides 3 dB margin to overcome layout related nonidealities, the layout needs to be implemented very carefully in order to achieve maximum performance. If specs are not met with the extracted simulations, the layout can be improved before attempting to redesign. Moreover, initial design specifications should be chosen carefully, considering tradeoffs between area, speed, SNR, and power consumption. Increasing the capacitor sizes improves SNR performance. However, this also increases area and dynamic power consumption. Similarly, increasing

clock speed will decrease conversion time for a target SNR or will improve SNR result for the same conversion time, but will increase both dynamic and static power consumption due to the high-speed clock and a faster-operating comparator. Therefore, SNR, OSR and sampling frequency need to be chosen carefully, considering these tradeoffs. Design examples are presented and compared with state of the art designs in Table 7. The Walden and Schreier Figure-of-Merits (FoM) are calculated for comparison with published designs. Finally, the BIST ADC needs to be tested before it can be used. Luckily, there are a plethora of solutions for testing ADCs efficiently without requiring an external stimulus or precise stimulus generation [53].

Table 7. Comparison with Other Works

Parameter	This Work	This Work	Chae 2013	Quiquempoix 2006	Agah 2010	C H Chen 2013	F Chen 2014
Architecture	Passive Zoom	Passive Zoom2	Zoom ADC	3rd order	(DS+11bSAR)	ZCD DS	Two stage
Technology	65nm	65nm	0.16µm	0.6µm	0.18µm	0.16 µm	65nm
Chip area	0.04mm²	0.02mm²	0.33mm²	2.8mm²	3.5mm²	0.45mm²	0.2mm²
Supply current	13.25µA	49.µA	3.5µA	120µA	21.1mA	20 µA	9 µA
Supply voltage	1.3 V	1.3	1.8V	3V	1.8V	1V	1.2V
Power	17µW	63uW	6.3µW	300µW	38.1 mW	20 µW	10.7 µW
Conversion time	512µs	31.25us	40ms	66.7ms	1µs	0.75ms	4ms
Sampling frequency	4M	16M	25.6k	30.72 kHz	45.2M	750 kHz	96 kHz
OSR	1024	256	512	512	45	500	192
Bandwidth	1.953 kHz	31.248kHz	25 Hz	7.5Hz	500kHz	667 Hz	251 Hz
Input range	2.6Vpp	2.6Vpp	1.8Vpp	6Vpp	3.6Vpp	0.7Vpp	2.2Vp
Measured Noise	24.7uVrms	98.2µVrms	0.65µVrms	2.5µVrms	-	19.9µVrms	
SNR	90.4dB	78.2 dB	119.8dB	123dB	90.1dB	81.9dB	99.8
SNDRmax	87.9B	76.5 dB		123dB	86.3dB	81.9dB	90.8
INL	±13.5 ppm (mean value)	±60 ppm (mean value)	±6ppm	±5ppm	±61ppm	±36ppm	
Fomw (pJ/conv.-step)	0.12	0.116	0.12	24.46	1.4	1.48	0.76
FoM_s	170 dB	173 dB	182.7dB	164dB	161.3dB	157.1	173.5

FoMW = power/(2^ENOB*(fs/OSR)) and FoMS =SNR+10*log(BW/power).

Crest-factor corrected SNRmax = 20.log((Max DC Input/ 2√2)/ Output Noise)

CHAPTER 4

A RECONFIGURABLE 0.1-10 MHZ DT PASSIVE DYNAMIC ZOOM ADC FOR CELLULAR RECEIVERS

4.1 Introduction

Although 4G cellular communications systems are most prevalent for higher data rates, 2G and 3G modes continue to be used throughout the world [57]. In order to support multiple standards efficiently, mobile devices are required to have programmable, low-power, low-cost, highly integrated transceivers compatible with the corresponding cellular technologies. Therefore, Analog to Digital Converters (ADCs) used in such transceivers are also required to be flexible and optimizable in terms of resolution, bandwidth, and power consumption (depending upon the mode). The Delta-Sigma (ΔΣ) ADC architecture is the preferred solution due to its easy reconfigurability for better performance or less power consumption by just changing the OSR. The ΔΣ architecture is less dependent on analog component values and its noise shaping property helps attenuate a significant amount of quantization noise and out of band interferers. Multiple continuous-time (CT) and discrete-time (DT) multi-mode ΔΣ modulators have been reported in the literature [63-70]. Even though CT ΔΣ modulators have many advantages over DT ΔΣ modulators, such as implicit anti-aliasing filtering and power efficiency, they are more prone to non-idealities such as clock jitter, excess loop delay, and integrator coefficient (RC time constant) variation which can be as high as ±%20. Furthermore, multi-mode CT modulators are more sensitive to parasitic effects and are more complex because CT loop filters are designed for a single operating clock frequency and they need multiple

switchable passive RC combinations in order to satisfy multi-mode operation. Comparatively, DT modulators are robust with respect to process variations as their transfer functions rely on capacitor ratios. Furthermore, the multi-mode operation can be realized by just adjusting clock frequency. However, active DT ΔΣ modulators consume much more power compared to their CT counterparts due to the higher unity gain bandwidth (UGBW) requirements for the Operational Transconductance Amplifiers (OTAs). The UGBW of the OTAs used in active DT modulators needs to be much higher than the sampling frequency to ensure proper settling in switched capacitor integrators. Compared to the active ΔΣ modulators, passive ΔΣ modulators provide low power solutions for DT operation due to the elimination of power-hungry OTAs [58][59]. Nevertheless, known passive ΔΣ architectures are limited to applications with relatively narrow signal bandwidth and/or medium dynamic range requirements due to limited options to suppress quantization noise.

A dynamic zoom-ADC architecture is presented in [61] for audio applications. A coarse 5b SAR (Successive Approximation Register) ADC and a 1b active ΔΣ modulator, which are clocked at the same clock edge, constitute the zoom-ADC. The ΔΣ modulator includes a 5b feedback DAC. Every 5 clock cycles, the SAR ADC yields a coarse conversion result and this coarse conversion is used to dynamically update the reference voltages of the ΔΣ modulator using a multi-bit DAC. Therefore, similar to multi-bit quantizer-based ΔΣ modulators, quantization noise power decreases significantly. In this architecture, if the ΔΣ OSR value is not high enough, the input signal can move out of the zoom range during the 5 clock cycles, which are required for SAR ADC. This is especially

true for ΔΣ modulators which are used for wireless communications. They are required to work with lower OSR values due to wide bandwidth, low power consumption and/or technology driven constraints on maximum sampling frequency.

In this chapter, we propose a DT passive dynamic zooming ADC which supports multi-mode EDGE-to-LTE bandwidths. The overall architecture of the proposed ADC consists of a 5b interpolating flash ADC as the zooming unit, and a passive discrete time ΔΣ modulator as the fine conversion unit. Unlike SAR ADC, interpolating flash ADC requires only one clock cycle to measure input voltage and to update DAC values. Since ΔΣ modulator DAC values are updated every clock cycle, dynamic zooming technique can be used independently of OSR value. The proposed ADC enhances passive sigma-delta modulator performance significantly by enabling the multi-bit feedback DAC option for passive ΔΣ modulators and reducing quantization noise. The proposed ADC achieves between 13.5 bits and 11 bits of resolution.

This chapter is organized as follow. Section 3.2 introduces a system-level implementation of the proposed passive dynamic active and passive modulators. Implementation of zooming ADC architecture including a comparison between key circuits is described in Section 3.3. Finally, experimental Implementation of zooming ADC architecture including a comparison between results and conclusions are given in Section 3.4 and Section 3.5 respectively.

4.2 System Implementation

4.2.1 Passive vs Active $\Delta\Sigma$ Modulators

Passive sigma-delta modulators provide area efficient and low power solutions for sigma-delta ADC applications due to the elimination of power-hungry OTAs. However, the lack of the loop filter gain limits the options for reducing quantization noise power for passive $\Delta\Sigma$

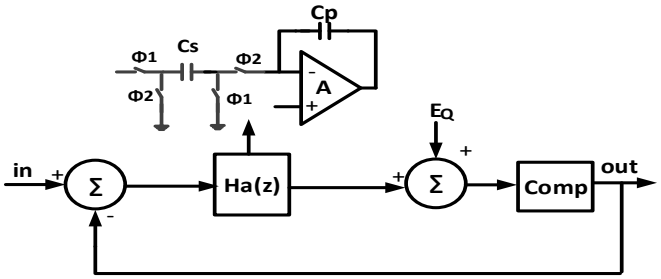


Fig. 35. System-level modeling of the 1st order modulator with active filter

modulators. Figure 35 shows the model of a first-order delta-sigma modulator with a discrete time integrator. Comparatively, Figure 36 represents the model of a first order passive sigma-delta loop filter which can be implemented either using continuous time or discrete time approach. For illustrative purposes, the discrete time implementation is shown in Figure 36.

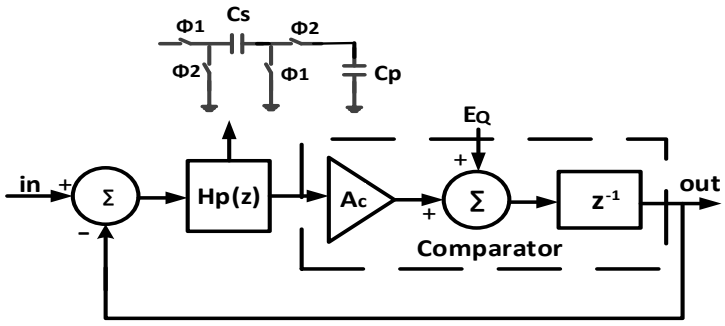


Fig. 36. System-level modeling of the first-order modulator with passive

In the passive SD architecture, the loop filter does not provide any gain due to the lack of active integrators, which results in zero or negative gain. Negative filter gain is the main obstacle for reducing quantization noise in passive sigma-delta modulators. Luckily, the comparator gain in passive modulators is not unity. The signal swing at the comparator input will be relatively small due to the significant attenuation in the filter. Thus, the small signal gain of the comparator can provide adequate gain for the loop.

Equation (30) represents the z-domain transfer function of first-order active SD modulator while Equation (31) represents first order passive SD modulator loop filter transfer function, including its comparator gain. In Equation (30), A_i represents the integrator gain, C_{sa} is a sampling capacitor, and C_i is the integrating capacitor for the active integrator. Similarly, Equation (31), represents the ideal transfer function of the passive filter, including the comparator gain (A_c) and neglecting any parasitic capacitance, C_{sp} is the sampling capacitor and C_p is the pole capacitor for the passive filter.

$$H_{active}(z) \approx \frac{A_i(C_{sa}/(C_{sa}+A_iC_i))z^{-1}}{1-z^{-1}(A_iC_i/(C_{sa}+A_iC_i))} \quad (30)$$

$$H_{passive}(z) \approx \frac{A_c(C_{sp}/(C_{sp}+C_p)z^{-1}}{1-z^{-1}(C_p/(C_{sp}+C_p)} \quad (31)$$

The loop gain of PSDM (Passive Sigma Delta Modulator) can be equalized to the loop gain of an active SD integrator by matching the small signal gain of the comparator (Ac) to the gain of the integrator $A_i = A_c$ To achieve a similar thermal noise performance, we need to set $C_{sp} = C_{sa}$. In order to obtain an equivalent transfer function between the active and passive modulators, the passive filter pole capacitor should be larger than the integrating capacitor of the active integrator by a factor of the comparator gain, as illustrated in Equation (32).

$$C_p = A_i C_i \quad (32)$$

Assuming all above-mentioned conditions are satisfied and using the linear model as well as the filter transfer function of 35 or 36, the quantization noise transfer function (NTF) can be calculated as in Equation 4 where $H(z) = H_{passive}(z) = H_{active}(z)$.

$$NTF(z) = \frac{1}{1+H(z)} \quad (33)$$

Equation (33) shows that the quantization noise can be suppressed with a high loop gain which is required for high-resolution ADCs. Thus, a high comparator gain is required for better quantization noise suppression. As shown in Equation (32), to equalize PSDM loop transfer function to the active counterpart, the pole capacitor of passive integrator needs to be bigger than the integrator capacitor of the active counterpart by a factor of the OPAMP gain. This requirement clearly imposes a larger area overhead. However, with a 2nd-order filter implementation, this area overhead can be alleviated since the loop gain

can be divided over the poles of the passive filter. As we can observe from Equation 33, previously published passive modulators can provide equivalent solutions to active counterparts for low order and single bit active modulators [58, 59].

Multiple techniques exist for suppressing the quantization noise and improving the signal to quantization noise ratio (SQNR) for active ΔΣ modulators. These techniques include increasing loop filter order, increasing oversampling ratio (OSR), and increasing quantizer resolution. The theoretical peak SQNR can be determined based on the loop filter order (L), the oversampling ratio (OSR), and the quantizer number of bits (N) as in Equation 34.

$$SQNR \approx \frac{3(2L+1)}{2\pi^{2L}} OSR^{2L+1}(2^N - 1)^2 \quad (34)$$

However, the lack of the loop filter gain limits the options for reducing quantization noise power for passive ΔΣ modulators. In high order active ΔΣ modulators, the loop gain is distributed across multiple integrators. Comparatively, the comparator is the only gain source for the passive modulator, and required gain is mostly provided by a high gain pre-amplifier and needs to be scaled with increasing loop filter order in order to achieve an equivalent NTF (Noise Transfer Function) with the active counterpart. Furthermore, 3 dB bandwidth of the preamplifier should be large enough to ensure loop stability. The high gain-bandwidth and low noise requirements necessitate high power consumption for the comparator which diminishes low power consumption benefits of passive ΔΣ modulators [60]. Moreover, in high order active ΔΣ modulators, only the noise contribution of the first integrator is significant. The noise introduced by later stages is attenuated by the gain

provided by prior stages. Therefore, increasing loop order does not introduce significant noise contribution. In contrast, in passive ΔΣ modulators, with the increase of loop filter order, the number of passive elements, which are thermal noise sources, increases. Since these passive devices are at the input of the modulator, there is no attenuation and they directly affect the signal to noise ratio. Increasing the loop order creates a tradeoff between thermal and quantization noise contributions. Therefore, increasing the order of the loop filter beyond second order only provides a diminished return in terms of SNR while considerably increasing the power consumption. Designing a multi-bit quantizer is also very difficult due to the extremely small signal swing at the quantizer input. Thus, increasing the oversampling ratio (OSR) remains as the single effective method to increase the SQNR of a traditional passive ΔΣ modulator [60]. Therefore, known passive ΔΣ architectures are limited to applications with relatively narrow signal bandwidth and/or medium dynamic range requirements [58, 59].

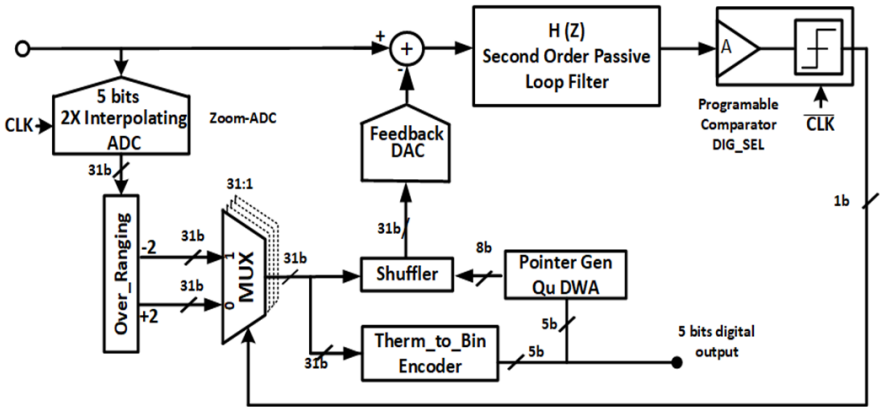


Fig. 37. Reconfigurable Dynamic Passive Zoom ADC

Table 8 Summary of ADC Modes

DIG SEL	MODE	BW(MHz)	FCLK(MHz)	DR(dB)
00	EDGE	0.1	26	> 87
01	UMTS	1.92	245.8	> 78
10	LTE	5	480	> 75
11	LTE	10	640	> 70

4.2.3 Multimode Passive Dynamic Zoom ADC

In this chapter, we propose a flash ADC based zoom ADC which can be used in wireless communication applications. Figure 37 shows the block diagram of the proposed dynamic-zoom passive ADC. It consists of a 5b interpolating flash ADC and a simultaneously free-running passive second order single-bit ΔΣ modulator. At the positive clock edge, the interpolating ADC outputs a coarse conversion and yields a 31b thermometer code. During the same clock phase, the digital logic prepares two sets of driving options for ΔΣ DACs. At the negative clock edge, the single-bit ΔΣ modulator operates and based on the modulator output, selects the driving bits for the DAC, which completes one cycle of operation. Unlike SAR ADC, interpolating flash ADC requires only one clock cycle to measure input voltage and to update DAC values. Since ΔΣ modulator DAC values are updated every clock cycle, dynamic zooming technique can be used independently of OSR value while enabling the multi-bit feedback DAC option for passive ΔΣ modulators and reducing quantization noise significantly. Thus, this architecture presents a viable option for wireless applications which require wider bandwidth and lower OSR.

In traditional multi-bit modulators, in every clock cycle, the flash ADC returns a thermometer coded output value, n, which is equal to a total number of logic high bits. The n value is used the drive a multi-bit unit cap DAC. Unlike traditional multi-bit modulators, the coarse interpolating flash ADC output is not directly used to drive the feedback DAC. In order to handle interpolating ADC non-idealities, the digital over-ranging block first takes the 31b thermal output code and detects the last logic high bit, n. Then, it prepares two sets of 31b DAC codes, (n – 2) and (n + 2), and stores them in two sets of register blocks. The DAC code, (n - 2), is generated by simply flipping the last two logic high bits before nth bit in the thermometer code sequence. Similarly, the DAC code, (n + 2), is generated by flipping the next two logic low bits after the nth bit in the thermometer code. Depending on the ΔΣ modulator output code, one of these DAC codes is selected and used to drive the 31 elements DAC. Alternatively, the over-ranging operation can be conducted after the ΔΣ modulator bit is decided in order to compute just one of the DAC codes. However, this would add extra loop delay, affecting the loop stability and limit the maximum sampling frequency. Therefore, we compute both DAC codes before the modulator output is decided with the cost of extra area and power. The over-ranging operation relaxes coarse Flash ADC accuracy requirements and ensures that the input voltage, Vin, is always in the zooming range. The over-ranging operation also ensures that

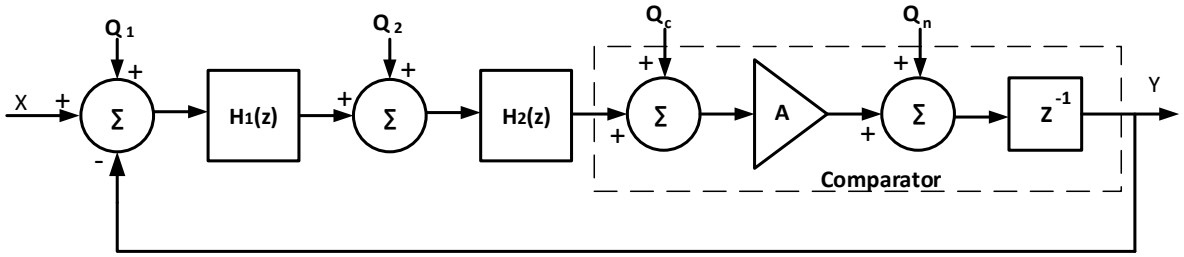


Fig. 38. System Level model of second order single bit passive modulator

the linearity of the proposed ADC is only limited by the linearity of the passive ΔΣ modulator. Hence, the linearity of the ΔΣ modulator is primarily determined by the feedback DAC nonlinearity. In order to suppress this non-linearity, a DWA (Data Weighted Averaging) block is used.

Proposed ADC uses a second order passive loop filter. Figure 38 shows a linearized model of a second-order PSDM with a two-pole passive low-pass filter and a 1-bit quantizer. The inter-stage loading is neglected for this model. While the loop gain is partitioned into each pole sector among the integrators for active sigma-delta modulators, the comparator is the only gain provider for passive integrators. The passive modulator transfer function can be expressed as in Equation 35.

$$Y \approx X + Q_{H_1} + \frac{Q_2}{H_1} + \frac{Q_c}{H_1 H_2} + \frac{Q_n}{A H_1 H_2} \quad (35)$$

$H_1(z)$ and $H_2(z)$ are first and second passive filter transfer functions. Thermal noise associated with each passive integrator is represented with Q_1 and Q_2, while Q_c and O_n denote the comparator noise and quantization noise respectively. It is assumed that $H_2(z)$ contains a zero for ensuring the loop's stability. This zero is introduced by a resistive path to ground and causes attenuation unless a current feedback path is used. Even though

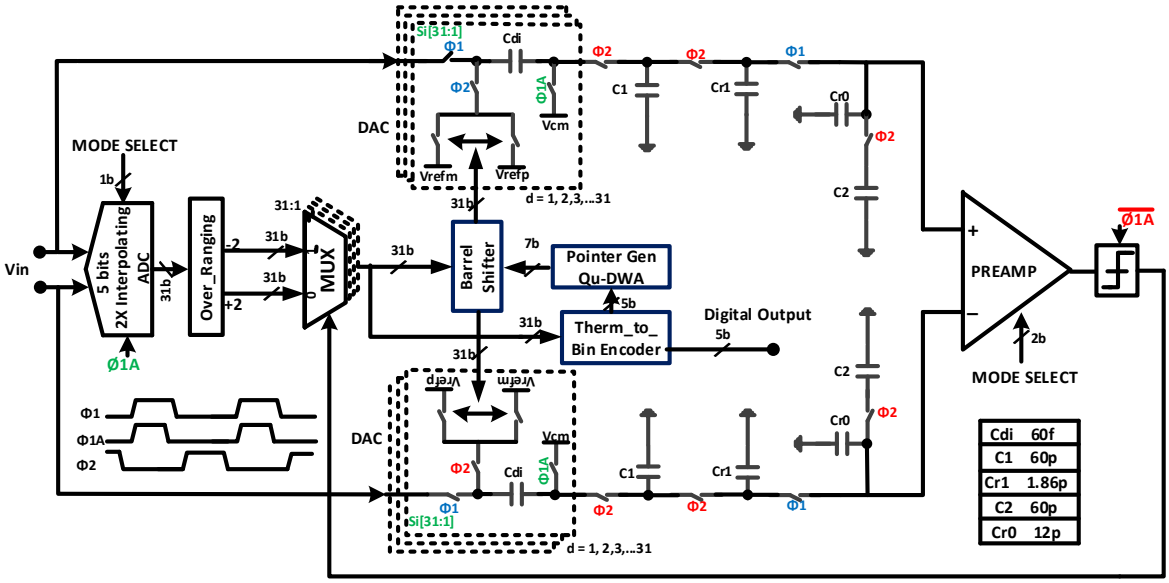


Fig. 39. Reconfigurable Dynamic Passive Zoom ADC

H1*H2 is limited to unity at DC, the quantization noise Q_n is still suppressed in the baseband by the comparator gain A. Other noise sources experience different filtering and attenuation. The same modulator architecture can be dynamically adapted to the different DR and BW requirements of multiple wireless standards by simply adjusting its OSR and sampling frequency. With the proposed architecture, neglecting loading effect, the z-domain NTF and STF are constant regardless of the mode selection and are given in Equation 36 and 37 respectively.

$$NTF(z) = \frac{1}{1 + AH_1(z)H_2(z)} \quad (36)$$

$$STF(z) = \frac{AH_1(z)H_2(z)}{1 + AH_1(z)H_2(z)} \quad (37)$$

Based on Figure 39 schematic and neglecting loading effect, we can obtain $H_1(z)$ as in Equation 38.

$$H_1(z) \approx \frac{(C_d / (C_d + C_1)z^{-1}}{1 - z^{-1}(C_1 / (C_d + C_1)} \quad (38)$$

Similarly, we can obtain $H_2(z)$ as in Equation 39.

$$H_2(z) \approx \frac{1 - (C_2 / (C_{r0} + C_2)z^{-1}}{(\frac{C_2C_{r1} + C_2C_{r0} + C_{r1}C_{r0}}{C_{r1} / (C_{r0} + C_2)})[1 - z^{-1}\frac{C_2 / (C_{r0} + C_{r1})}{C_2C_{r1} + C_2C_{r0} + C_{r1}C_{r0}}]} \quad (39)$$

Since the signal bandwidth scales with the sampling frequency, the multi-bandwidth operation is realized by changing the clock frequencies based upon the mode as presented in Table1. In the EDGE mode, the clock frequency is set to 26 MHz, in the UMTS mode it is set to 245.8 MHz, in the LTE_5MHz mode, it is set to 480MHz, and in the LTE_10MHZ mode, it is set to 640MHZ. The programmable comparator block is used to enable different noise and sampling frequency requirements per mode. For a given standard, the ADC used in the receiver needs enough dynamic range (DR) to satisfy two main requirements: 1) provide the required signal sensitivity (i.e., minimum detectable4 signal strength to maintain the required bit error rate) at the antenna and 2) process the maximum signal power at the ADC input without being saturated [66]. The DR budget for the ADC is associated with the gain distribution in RF frontends. Table I gives the receiver architecture for various standards and the corresponding parameters defined for the ADC in this paper. Energy scalability feature is satisfied with the programmable comparator block as well as sampling frequency change.

4.3 Circuit Implementation

4.3.1 Passive Loop Filter and DAC

Top level switched capacitor implementation of the proposed ADC is presented in Figure 39 together with its relative timing diagram. The modulator runs under two non-overlapping clock phases. A programmable two-phase clock generation circuit is used to adjust non-overlap time based on the sampling frequency. In order to decrease signal-dependent charge injection errors, bottom plate sampling is used. Capacitor, Cd, is shared between the input sampling and the feedback paths. Therefore, Cd is used to perform the feedback DAC functionality as well. For the same noise budget, the proposed architecture uses capacitors that are half as large as the capacitors of an architecture with a separate capacitor for the feedback DAC. Hence, the proposed architecture consumes less power [64]. A sampling capacitor of 1.86 pF is selected to satisfy dynamic range and linearity requirements. The multi-bit feedback DAC is realized by separating Cd into 31 equivalent parallel unit capacitors. MIM capacitors are used for area efficiency. Due to passive filter suppression and zooming architecture, proposed ADC can support rail to rail signal. Since they see rail-to-rail signals, the input switches Si[1..31] which are connected to the input signal directly are bootstrapped to improve their linearity [71]. Bootstrapping on the input switch eliminates the signal-dependent modulation of the switch on-resistance and preserve high linearity [71]. Simple transmission gate structure is used for remaining switches, which are optimized for linearity. Transmission gate's on-resistance is designed to be around 50 ohms to yield small enough Ron to work properly at the maximum clock frequency. Capacitor, CR1, should sample from capacitor, C1, during clock phase Ø1 and

the comparator should generate a valid digital code before the next clock phase Ø1 to limit the overall loop delay to a one clock cycle. Any additional delay inside the loop will degrade the performance. This limits the maximum sampling rate to 640 MHz for the chosen process, 130nm.

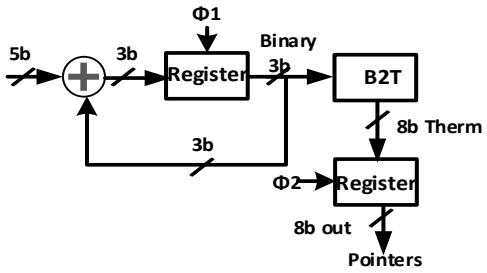


Fig. 40. Qu-DWA pointer generation

4.3.2 Dynamic Element Matching

DWA (Data Weighted Averaging) systems are used to remove mismatch related non-linearity and improve the linearity of feedback DAC. A DWA system contains two important building blocks. The first one is the pointer which indicates which unit element will be used as the starting point in a DAC operation. The second one is a data shuffler which maps the relationship between the thermometer code and DAC unit elements. In order to minimize the loop delay, DWA pointer generation block is placed outside the loop and barrel shifters are used instead of logarithmic shifters. Pointer generation block needs binary code, so there is a thermometer-to-binary code converter; next adds all previous quantizer outputs in the binary code domain, and stores them as the pointer for the next DWA operation; to perform these, an accumulator and a register are needed. A 3b Qu-DWA [72] is used instead of the regular 5b DWA. This structure works similar to regular

DWA pointer generation. However, it uses a truncated adder in pointer generation block, hence adder gives most significant 3 bits output instead of 5 bits. Finally, register output is converted to thermometer code and decides a total number of shifts from the current starting point of unit DAC element. Figure 40 represents system-level implementation of 3 bits Qu-DWA pointer generation block. There are totally 31 shift options for each unit element

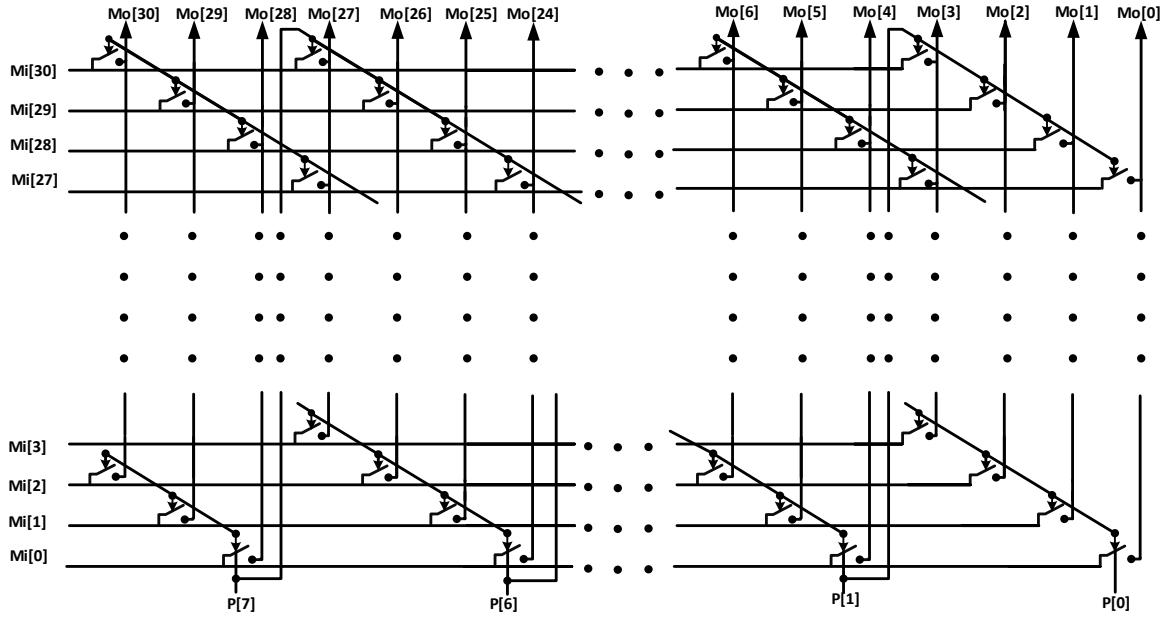


Fig. 41. Qu-DWA Barrel Shifter

DAC capacitor for regular DWA and only 8 shift options for Qu-DWA. Since last two bits of 5 bits output is truncated, there are only 8 shift options in Qu-DWA, which are equal to 28, 24, 20, 16, 12, 8, 4 and 0. Although this architecture causes some performance degradation on the linearity of the DAC for low oversampling ratios compared to regular DWA, performance degradation can be alleviated by increasing the oversampling ratio of sigma-delta ADC [62]. Moreover, it has two advantages over regular DWA. Firstly, using

a Qu-DWA decreases complexity and power consumption of pointer generation block. Secondly, barrel shifter uses 248(31x8) switches instead of 961(31x31) switches and saves area and power. Switches are implemented with transmission gates since they are able to pass both logic “0” and logic “1”. Transmission gates are optimized for speed by using minimum channel length transistors. Resulting propagation delay is around 200ps. Figure 41 shows shuffler block, where $M_o[30:0]$ represents outputs of the shuffler, $M_o[30:0]$ represents inputs of the shuffler block and P[7:1] pointer block output.

4.3.3 Comparator

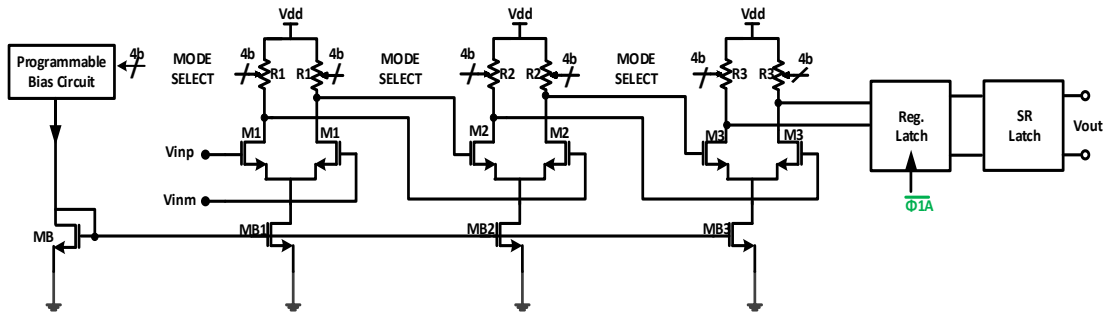


Fig. 42. Programmable Comparator

Comparator design requirements are different for different modes. A programmable single bit quantizer is required to support different bandwidth and noise requirements with the minimum power consumption while keeping the preamplifier gain within an acceptable range. A regenerative latch preceded by three cascaded equivalent preamplifier stages constitutes the comparator. Each preamplifier has resistive loads. Reconfigurable bias currents and resistive loads are used to adapt the performance of the preamplifiers to the noise and propagation delay requirements of each mode, as represented in Figure 42. Input signal is amplified by preamplifiers during clock phase Ø1. Regeneration operation starts

at the falling edge of clock Ø1A and the logic level is decided. The valid digital code must be available before the beginning of clock phase Ø2 to avoid glitches [58].

An important parameter for the comparator is its propagation delay. During Φ1, while the input signal is amplified by preamplifiers, the propagation delay should be less than Φ1 pulse time. The signal propagation delay through three preamplifiers can be expressed as in Equation (40), C_{di} is the parasitic capacitor associated with ith stage of the preamplifier and C_{gi+1} is the gate capacitance of the next preamplifier stage. I_{CM} is the common mode current drawn from each preamplifier.

$$t_d \approx \frac{VDD}{2} \sum_{i=1}^{3} \frac{C_{d_i} + C_{g_{i+1}}}{I_{CM}} \quad (40)$$

Each mode has different delay requirements due to different sampling frequencies. In order to control propagation delay, common mode current is changed by programmable biasing control circuitry. Based on common mode current, the load resistance is also updated to ensure next stage common mode voltage will be equal to VDD/2. The latch delay is another issue, minimum length devices are used to minimize delay and width sizes are optimized for minimum delay and no programmability is required.

In multi-stage amplifiers, the first stage is the dominant noise source. For the proposed design, flicker noise is not very critical due to relatively high operation bandwidth and properly sized input transistors. The total input referred thermal noise of comparator can be approximated as in Equation (41) where k is the Boltzmann constant, T is the absolute temperature. Noise density decreases with biasing current. Hence increasing biasing current also helps to decrease noise density for high bandwidth modes.

$$v_{nth} = \sqrt{\frac{8kT\gamma\Delta_f}{g_m} + \frac{8kT\Delta_f}{{g_m}^2 R} + \frac{2K}{WLC_{ox}f}} \approx \sqrt{\frac{8kT\gamma\Delta_f}{g_m}} \quad (41)$$

Using the simplified MOS transistor model, the gain of the single preamplifier stage can be expressed as in Equation (42). where I_{cm} is the common mode current, g_m is the transconductance of each differential transistor pair, R is the load resistance, W and L are transistor width and length respectively.

$$G_p = g_m(R \| r_o) \approx gmR \approx \sqrt{K\frac{W}{L}I_{cm}}\left(\frac{VDD}{I_{cm}}\right) \quad (42)$$

The total gain of the comparator will be equal to the product of the gains of the three preamplifiers and the latch. We use the well-known Strong Arm latch architecture [72] in our design. The strong arm latch is followed by inverter and SR latch stages. Latch gain is constant over different ADC modes. As the common mode current increases with a change of bandwidth mode, preamplifier gain decreases inversely proportional to square root of common mode current. Hence, 10 MHz mode gives minimum gain. However, even in the 10 MHz mode comparator provides enough gain which is equal to 54dB to suppress quantization noise.

4.3.4 Circuit Noise Estimation

Three noise sources are important for passive sigma-delta ADCs designed for low-frequency applications: quantization noise, flicker noise, and thermal noise. In this work, flicker noise will be neglected thanks to the usage of precision techniques such as auto-zeroing and digital chopping. Thus, the total input referred noise power can be expressed as in Equation (43) [58],

$$V^2_{n,total} = V^2_{n,H_1} + \frac{V^2_{n,H_2}}{H_1^2} + \frac{V^2_{n,COM}}{H_1^2 H_2^2} + \frac{E^2_Q}{A_{com} H_1^2 H_2^2} \quad (43)$$

where V^2_{nH1} and V^2_{nH2} are the thermal noise powers associated with first and second pole, respectively, V^2_{ncom} is the comparator input referred noise power, E^2_Q is the quantization noise power, isH1 and H2 are transfer functions for first and second passive filters, respectively, and A is the comparator gain.$V^2_{n\Phi 1,}$ and $V^2_{n\Phi 2}$ are generated during PSDM operating clock phases Ø1 and Ø2. The system is designed to have a negligible quantization noise since the quantization noise will be suppressed due to loop gain and zooming.

$$V^2_{nH_1} = V^2_{n\Phi_1} + V^2_{n\Phi_2} = \frac{2kT}{C_d} + \frac{2kT}{C_d(C_d + C_1)/C_1} \quad (44)$$

$$V^2_{nH_2} = V^2_{n\Phi_1} + V^2_{n\Phi_2} = \frac{2kT}{C_{R1}(C_{R1} + C_1)/C_1} + \frac{2kT}{C_{R1}(C_{R1} + C_2)/C_2} \quad (45)$$

$$V^2_{nCOM} \approx \frac{8kT\gamma\Delta_f}{g_m} \quad (46)$$

V^2_{nCOM} represents comparator noise. Where T is absolute temperature, k is Boltzmann constant, gm is the transconductance of differential pair and Δ_f is noise bandwidth. SNR can be calculated as in Equation (46).

4.3.5 Interpolating FLASH ADC

A full differential interpolating flash ADC is used for zoom ADC (Figure 43). It employs a resistive ladder DAC and single stage preamplifier based comparators. Preamplifiers are useful to suppress offset and kickback noise from dynamic comparators. However, they consume static power. An interpolating ADC works similar to a regular

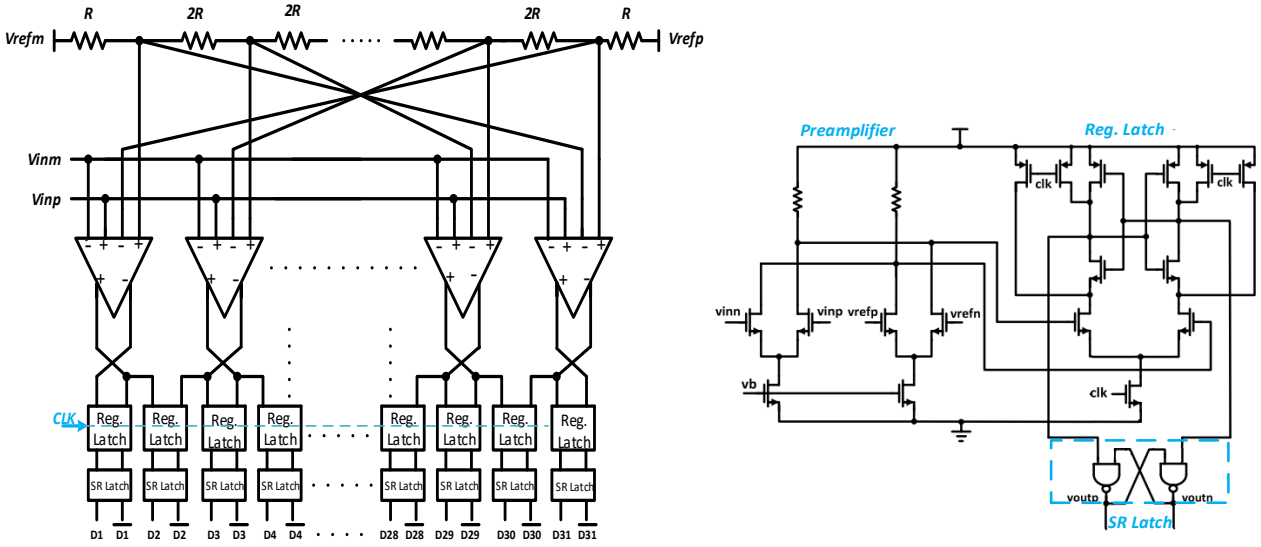


Fig. 43. Coarse Interpolating ADC

flash with a reduced number of preamplifiers and an equivalent number of latches, hence decreases power consumption and area. We used an interpolating ADC with a 2X interpolating factor instead of a higher order interpolating factor. This minimizes interpolating non-idealities and helps improving differential nonlinearity. To generate the reference voltages, an on-chip resistive reference ladder has been used. On one hand, the resistance value of the ladder needs to be small due to the well-known problem of ladder feedthrough. On the other hand, a small resistance results in high power consumption. The worst case feedthrough, which is from the input to the midpoint of the ladder, can be calculated as in Equation 47 [66]:

$$\frac{V_{MID}}{V_{IN}} = \frac{\pi}{4} f_{IN} RC \quad (47)$$

Where C is the total capacitance from the input to the resistive ladder R and fin is the input frequency, which is equal to 10 MHz in the worst case scenario. With this formula, the

maximum ladder resistance can be calculated for which the feedthrough does not degrade the performance. A disadvantage of regular flash ADC is the usage of a larger number of comparators and resistors. While comparators increase input capacitance, a mismatch in the resistors results in inconsistency in the output. As an improvement, interpolation is used to reduce the number of comparators and resistors that are used to generate the reference voltages. Due to half number of preamplifiers, input capacitance decreases and a bigger ladder resistor can be used. The total ladder resistance value is approximately equal to 10Kohms. Another important aspect is offset voltage. Offset voltage must be low enough to guarantee linearity. The preamplifier input devices are sized to maintain a DC offset less than 0.25 LSB. Generally, DC offset calibration circuits are designed to ensure DC offset less than a certain value, in our design, it is not required due to over-ranging block.

4.4 Measurement Results

4.4.1 Prototype Measurements

The proposed modulator has been fabricated in a 130nm 1P8M mixed-signal CMOS technology with a MiM-capacitor option. It is assembled in QFN-28A package. The converter occupies an area of $0.3\mu m^2$. A chip micrograph is shown in Fig. 44. In the layout, guard rings are employed to isolate the sensitive analog parts from noisy digital circuits. The analog and digital blocks use separate power supplies and grounds; on-chip decoupling capacitors are employed to make the analog power supply clean.

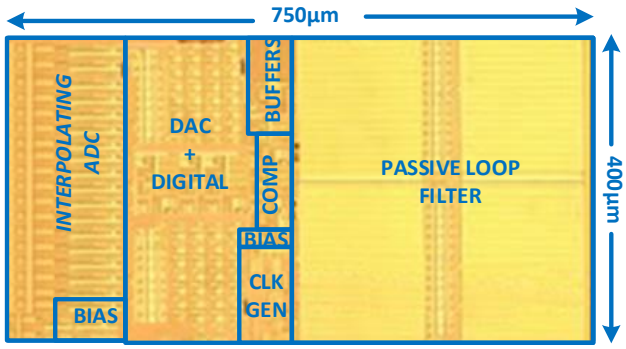


Fig. 44. Chip Micrograph

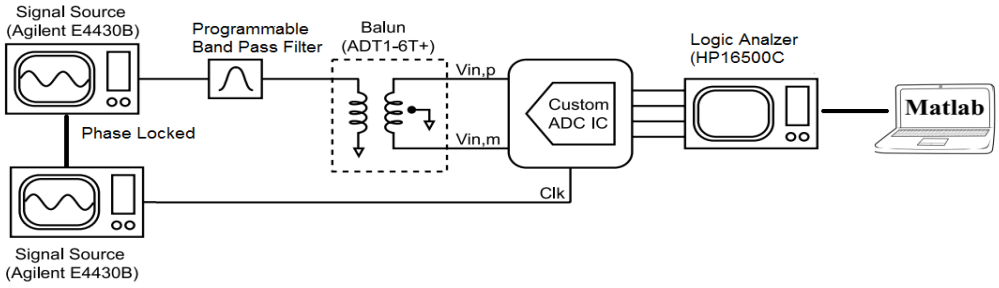
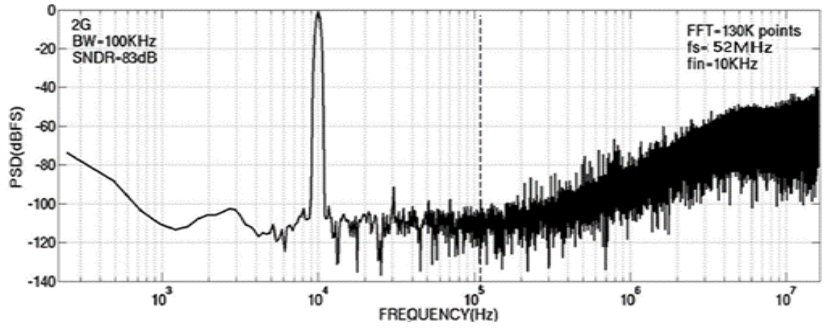


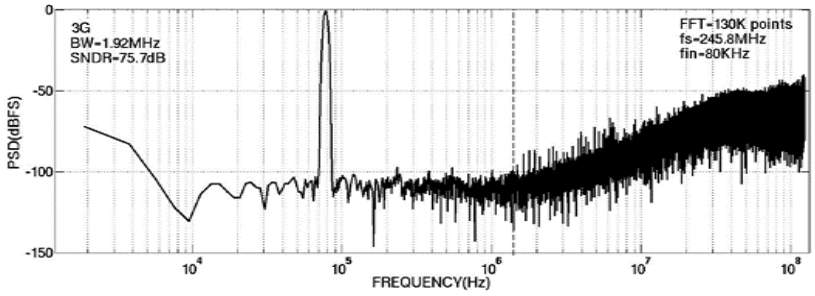
Fig. 45. Measurement Setup

Measurement setup is shown in Figure 45. The clock is supplied from an off-chip signal source. An external transformer converts the single-ended analog signal to a balanced differential input signal. Sinusoidal input signals with a maximum input voltage of 2.2-Vpp differential are supplied to the ADC. Digital output signals are captured by a logic analyzer. The captured output data is windowed by a Blackman-Harris window and a Fourier transformation is applied. Notice that the input signal frequencies are passed through external bandpass filters to remove harmonics from the source signal. Figure 46 shows the measured spectra for different modes at -1.5dB below full-scale voltage. The spectrum reveals the peak SNDR. Mode swap is achieved by changing input clock

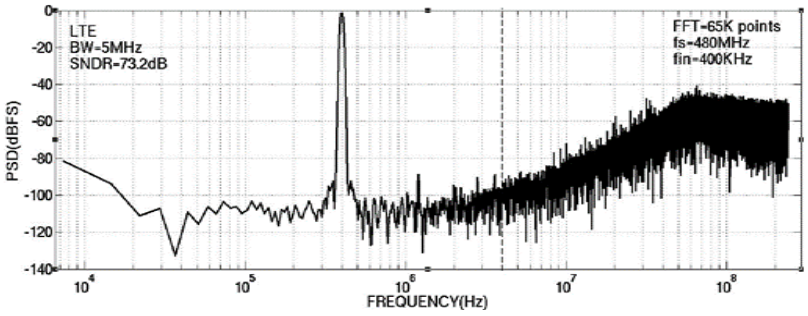
frequency, programming the bias currents and a load resistance of preamplifiers. The dynamic weighted averaging algorithm runs in the background during normal operation to correct the large harmonics resulting from the DAC non-linearity. Harmonic performance degrades at 10MHz bandwidth for multiple reasons. Firstly, at 640 MHz sampling clock, the non-overlap time between the two phases becomes proportionally significant compared to the time available for settling. This requires additional effort to settle correctly within the desired accuracy. Secondly, input bond wires cause sampling switch kick-back and signal dependent ringing at the input.



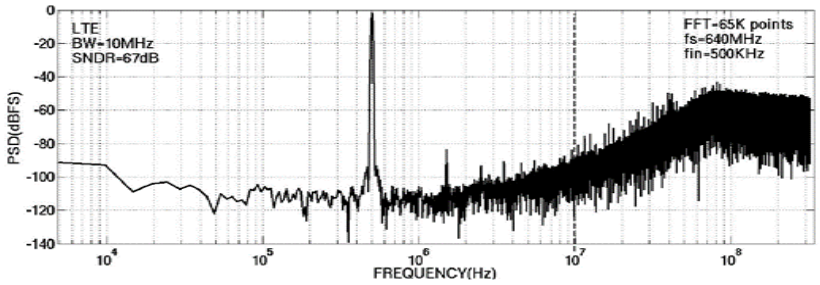
(a) EDGE 100KHz BW, 260kFFT fin=20kHz, fs=52MHz SNDR=83dB



(b) UMTS(1.92MHz BW, 130kFFT fin=100kHZ, fs=245.8MHz,SNDR=75.8dB



(c) LTE(5MHz BW), 65kFFT fin=400kHz, fs=480MHz, SNDR=73dB



(d) LTE(10MHz BW), 65kFFT fin=500kHz ,fs=640MHz, SNDR=67dB

Fig. 46. Measured output spectra at -1.5dBFS

In Fig. 47, the SNDR is plotted vs. the input amplitude for different modes to extract the dynamic range. Table II summarizes the performance. The modulator achieves peak SNDR of 83/75.8/73/67 dB over 0.1/1.92/5/10 MHz bandwidth with power consumption of 1.6/5.7/9.6/11.9 mW from the 1.2V supply. The respective figures of merit (FOMs) are 568/293/258/320 fJ/conv.

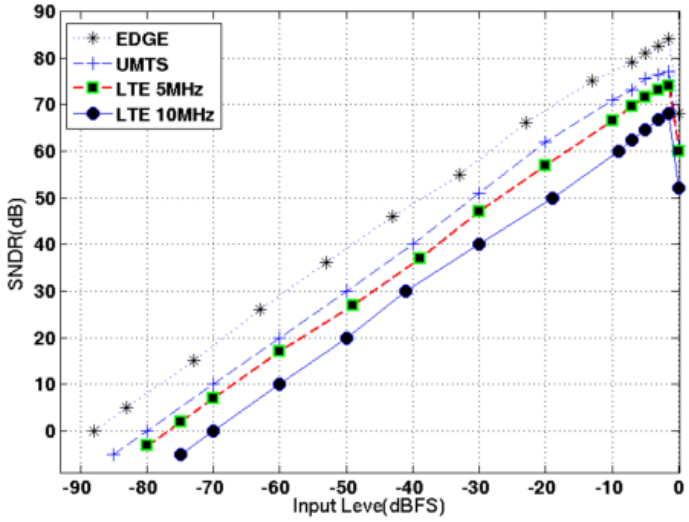


Fig. 47. SNDR vs Input Amplitude

Table 9. Performance Summary

Passive Zoom ADC	2G (EDGE)	3G (UMTS)	4G (LTE)	
BW(MHz)	0.1	1.92	5	10
fs(MHz)	52	245.8	480	640
Full Scale Input (Vpp)	2.4	2.4	2.4	2.4
Peak SNDR(dB)	83.2	75.8	73.2	67
Peak SNR(dB)	85.1	77.2	75.1	69.2
DR(dB)	87.1	80.2	77.1	72.5
IM3@-6dBFS	92	87.2	85	75
PDC(mW)	0.876	1.176	1.776	1.776
PAC(mW)	0.78	4.52	7.81	10.12
PTOTAL(mW)	1.616	5.696	9.586	11.896
FOM(pj/conv)	0.56	0.29	0.26	0.32

The performance of the modulator is summarized by calculating the Schreier FOM

$$FOM = \frac{Power}{2BW \times 2^{ENOB}} \quad (19) \text{ with}$$

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (20)$$

Measured power breakdown from a 1.2 V supply for different operating modes are shown in Fig. 48. These graphs summarize power consumption results by differentiating power consumption as static or dynamic as well as in which block power is consumed. The power consumption is mostly dynamic power due to switching activity in comparator latches and digital blocks, such as clock generation circuitry and DWA. Thus, power consumption is highly scalable with technology. Since no input offset cancellation is used for this PSDM, around 10 mV DC offset is measured, however, this can be calibrated digitally and does not pose any system implications.

4.4.2. Comparison with State-of-the-Art

The performance of the modulator is summarized by calculating the FOM. Table III shows the comparison of the performance of our ADC with the state of the art configurable wireless ΔΣ ADCs designed with similar technologies which can support at least 10MHz bandwidth. The modulator achieves peak SNDR of 83/75.8/73/67 dB over 0.1/1.92/5/10 MHz bandwidth with power consumption of 1.6/5.7/9.6/11.9 mW from the 1.2V supply. The respective FOMs are 568/293/258/320 fJ/conv. The proposed ADC provides better figures of merit in all modes compared to its several DT published

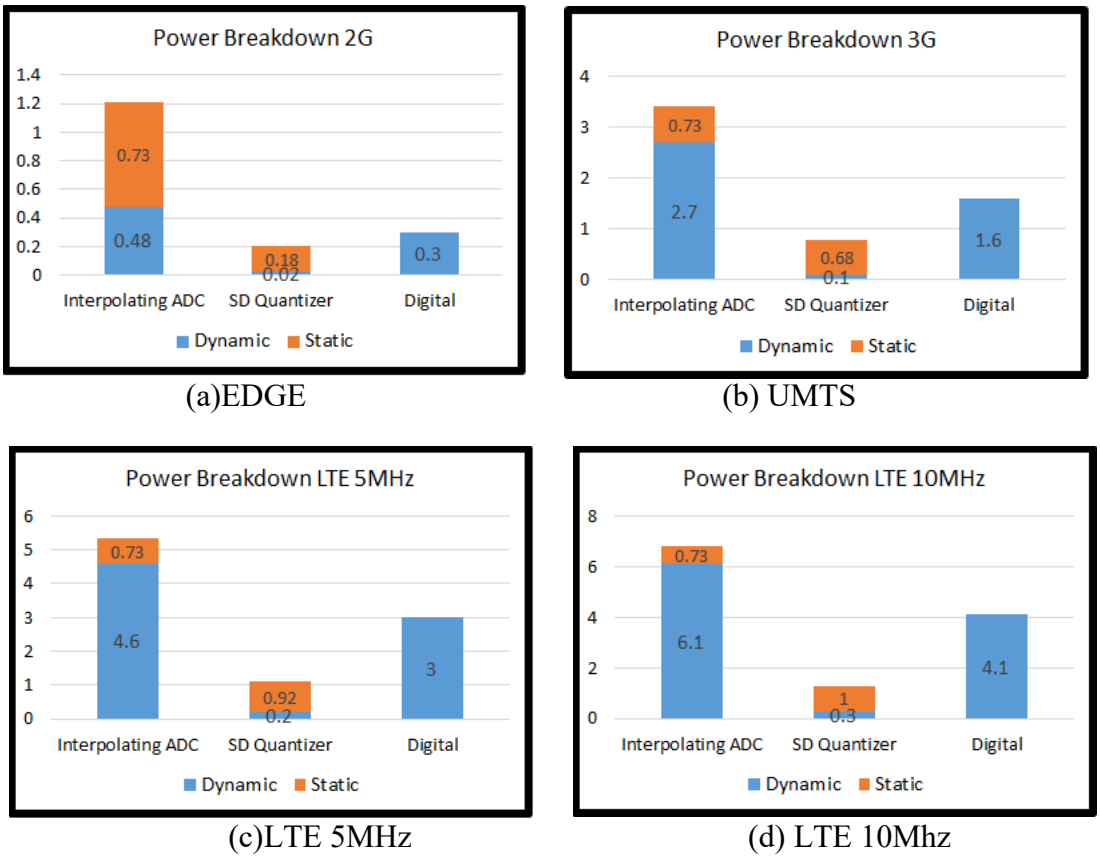


Fig. 48. Measured power breakdown for different modes in mW

counterparts. Even when compared to published CT implementations, the proposed ADC performance is competitive. Moreover, simulation results show that the power consumption is mostly dynamic power due to comparator latches and digital blocks, such as clock generation circuitry and DWA. Thus, power consumption is highly scalable with technology. Finally in Figure 49 plot of FOM versus signal bandwidth of several published configurable wireless ΔΣ ADCs [63]-[70] and single bandwidth wireless ΔΣ ADCs [73]-[79] is shown. In order to make a fair comparison ADCs which are designed in either 90nm or 130nm CMOS process are chosen.

Table 10. Comparison with State of the Art

REF	Mode	BW (MHZ)	ENOB	P [mW]	FOM [pJ/conv]
Bettini [64] 130nm DT Active	EDGE	0.1	13.2	2.4	1.28
	UMTS	1.92	12	5.8	0.35
	LTE	5	11.2	15.9	0.67
		10	11	18.5	0.44
	LTE-A	20	10.4	35.7	0.6
Christen[65] DT Active 130nm	EDGE	0.1	14.3	2.9	0.7
	UMTS	1.92	12.8	7.4	0.3
	WLAN	10	10.8	20.5	0.9
Morgado[66] DT Active 90nm	GSM	0.1	12.7	4.6	3.5
	BT	0.5	11.1	5.3	2.1
	GPS	1	10.6	6.2	1
	UMTS	2	10.2	8	1.2
	DVB-H	4	9.5	8	0.9
	WiMAX	10	7.8	11	1.6
Ouzunov[68] CT Active 90nm	GSM	0.2	13.3	1.4	0.35
	BT	1	12.2	3.4	0.37
	WLAN	10	7.8	7	1.07
Crombez[69] CT Active 90nm	BT	0.5	12.5	5	0.43
	UMTS	1.92	12	6.44	0.39
	DVB	4	11.3	5.5	0.21
	WLAN	10	10.5	6.8	0.19
Li[70]	LTE	5	11.8	8	0.23

CT Active 130nm	LTE-A	10	10.7	14.7	0.44
		15	9.7	16	0.66
		20	9.4	21	0.77
Xu[67] CT Active 130nm	TDsCDMA	0.8	13.7	8.4	0.41
	LTE	2.5	12.2	8.4	0.37
		10	10.7	10.2	0.31
Chen[58] DT Passive	EDGE	0.1	12	1.275	1.55
	UMTS	2	7.2	1.275	2.16
This work DT Passive 130nm	EDGE	0.1	13.6	1.6	0.56
	UMTS	1.92	12.5	5.7	0.29
	LTE	5	12	9.6	0.26
		10	11	11.9	0.32

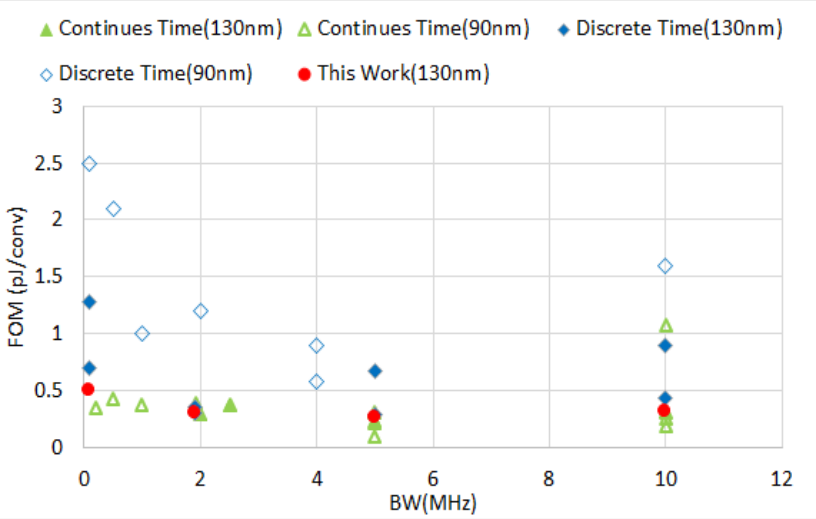


Fig. 49. FOM vs bandwidth of state of the art ADCs

CHAPTER 5

CONCLUSIONS

In this thesis, we proposed two different passive zoom ADC architectures. First ADC is a fully synthesizable, small footprint, passive, fully-differential, zoom-ADC architecture with two-step zoom-in conversion. The proposed BIST ADC provides all required conditions such as automated synthesis, low area overhead, high resolution/accuracy, low power consumption in case BIST is needed for in-field calibration, and adequate bandwidth. In the first step, a coarse converter performs the zoom-in function whereas, in the second step, a fine converter resolves additional bits within the zoom window. A passive loop filter based incremental second order sigma-delta ADC is used for fine conversion. The synthesis algorithm and the ADC architecture are explained in detail. Two different design examples are presented and compared with state of the art designs. The Walden and Schreier Figure-of-Merits (FoM) are calculated for comparison with published designs.

Second ADC is a novel reconfigurable interpolating flash ADC based DT passive dynamically zooming ΔΣ modulator. With the proposed architecture, dynamic zooming technique can be used independently of OSR value while enabling the multi-bit feedback DAC option for passive ΔΣ modulators and reducing quantization noise significantly. The proposed ADC implemented in 130nm technology covers bandwidths between 100KHZ and 10MHz which makes it a good candidate for GSM/EDGE up to LTE bandwidths. Measurement results show that the proposed ADC design achieves much better FoM values compare to active DT counterparts and competitive FoM values compared to continuous

time modulators. Due to the elimination of power-hungry OPAMPs, power consumption is mostly dynamic power consumption. Therefore, the power consumption of the proposed architecture is highly scalable with the technology. Proposed ADC takes advantage of the passive structures in order to design ΣΔMs while achieving competitive performance and power efficiency with active counterparts.

REFERENCES

[1] K. Arabi, B. Kaminska and M. Sawan 1998. “On-Chip Testing Data Converters Using Static Parameters IEEE Transactions On VLSI Systems”, Vol. 6, No. 3, September 1998

[2] M.F. Toner; G.W. Roberts “A BIST scheme for an SNR test of a sigma-delta ADC” IEEE International Test Conference 1993

[3] G. W. Roberts, F Taenzler, M Burns, “An Introduction to Mixed-Signal IC Test and Measurement”, Oxford U Press, 2011

[4] J Woong Jeong, A Nassery, J.Kitchen, and S. Ozev, ”Built-In Self-Test and Digital Calibration of Zero-IF RF Transceivers”, IEEE Transactions On VLSI Systems, Vol. 24, No. 6, June 2016

[5] B.R. Veillette; G.W. Roberts “A built-in self-test strategy for wireless communication systems: IEEE ITC 1995

[6] T. Oshita et al, “A Compact First-Order ΣΔ Modulator for Analog High-Volume Testing of Complex System-on-Chips in a 14 nm Tri-Gate Digital CMOS Process” IEEE Journal of Solid-State Circuits, vol. 51, no. 2, February 2016

[7] T. Liu, C. Fu, S Ozev, B. Bakkaloglu 2014. “A Built-In Self-Test Technique for Load Inductance and Lossless current sensing of DC-DC Converters” 2014 VLSI Test Symposium (VTS) 2014

[8] H Hong, J. Huang, K. Cheng, C. Wu D. Kwai 2003. “Practical Considerations in Applying SD Modulation-Based Analog BIST to Sampled-Data Systems” September 2003 IEEE Transactions on Circuits and Systems—ii:

[9] M. Hafed, G. W. Roberts 2003. “Techniques for High-Frequency Integrated Test and Measurement IEEE Transactions On Instrumentation And Measurement”, Vol. 52, No. 6, December 2003

[10] J. Huang and K. Chen, “A Sigma-Delta Modulation Based BIST Scheme for Mixed-Signal Circuits” Design Automation Conference 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific 2000

[11] C. S. Taillefer, G. Roberts “Delta-Sigma A/D Conversion Via Time-Mode Signal Processing” 2009. IEEE Transactions On Circuits And Systems -1:Regular Papers, VOL. 56. NO. 9 SEPTEMBER 2009

[12] N. Chandra and G.W. Roberts, “Top-Down Analog Design Methodology Using Matlab and Simulink” 2001 IEEE. ISCAS

[13] F. Chen, S. Ramaswamy, B. Bakkaloglu .” A 1.5V 1mA 80dB Passive ΣΔ ADC in 0.13μm Digital CMOS Process”. In IEEE Integrated Solid State Circuits Conference Dig. Tech. Papers, Feb. 2003

[14] AF Yeknami, F Qazi, A Alvandpour 2015. “Low-power DT modulators using SC passive filters in 65 nm CMOS” In IEEE Transactions on Circuits and Systems I: Regular Papers 61 [2), 358-370

[15] P. Harpe, E. Cantatore, and A. van Roermund. 2013 “A 2.2/2.7 fJ/conversion-step 10/12b 40 kS/s SAR ADC with data-driven noise reduction” In IEEE Integrated Solid State Circuits Conference Dig. Tech. Papers, February 2013

[16] P. Allen, P.Barton.” A Silicon Compiler for Successive Approximation A/D and D/A Converters” In IEEE CICC 1986

[17] C.-Y. Liou and C.-C. Hsieh 2013. “A 2.4-to-5.2 fJ/conversion-step 10b 0.5-to-4 MS/s SAR ADC with charge-average switching DAC in 90 nm CMOS,” in IEEE ISSCC Dig. Tech. Papers, Feb. 2013, pp.280–281.

[18] J Kim et al 2012. “A 14b Extended Counting ADC Implemented in a 24MPixel APS-C CMOS Image Sensor” IEEE Integrated Solid State Circuits Conference Dig. Tech. Papers, February 2012

[19] M. Seo et al. “A Low-Noise High Intrascene Dynamic Range CMOS Image Sensor With a 13 to 19b Variable-Resolution Column-Parallel Folding-Integration/Cyclic ADC” In IEEE Journal of Solid-State Circuits [January 2012]

[20] Nikola Katic et al. 2013 “Power-Efficient CMOS Image Acquisition System based Compressive Sampling” In IEEE 56th International Midwest Symposium on Circuits and Systems 2013

[21] Fang Tan et al 2016 “A Column-Parallel Inverter-Based Cyclic ADC for CMOS Image Sensor With Capacitance and Clock Scaling” In IEEE Transactions on Electronic Devices January 2016

[22] E. W. Owen. 1980 “The elimination of offset errors in dual-slope analog-to-digital converters,” IEEE TCAS 1980

[23] V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Markus, J. Silva, and G. C. Temes. 2006. “A low-power 22-bit incremental ADC” In IEEE Journal of Solid State Circuits [December 2006)

[24] Z. Tan, Y. Chae, R. Daamen, A. Humbert, Y. V. Ponomarev, and M.A. P. Pertijs, 2012. “A 1.2 V 8.3 nJ energy-efficient CMOS humidity sensor for RFID applications,” in IEEE Symp. VLSI Circuits Dig., 2012, 24–25

[25] A. Agnes, E. Bonizzoni, and F. Maloberti. 2011. “High-resolution multi-bit second-order incremental converter with 1.5- V residual offset and 94-dB SFDR”. In Analog Integrated Circuits and Signal Processing, August. 2011

[26] H Hong, J. Huang, K. Cheng, C. Wu D. Kwai 2003. “Practical Considerations in Applying SD Modulation-Based Analog BIST to Sampled-Data Systems” IEEE Transactions on Circuits and Systems—ii: Analog and Digital Signal Processing

[27] C. S. Taillefer, G. Roberts “Delta-Sigma A/D Conversion Via Time-Mode Signal Processing 2009”. IEEE Transactions On Circuits And Systems -1:Regular Papers, VOL. 56. NO. 9 SEPTEMBER 2009

[28] A. Agah, K. Vleugels, P. B. Griffin, M. Ronaghi, J. D. Plummer, and B.A. Wooley 2010.”A high-resolution low-lower oversampling ADC with extended-range for bio-sensor arrays” IEEE J. Solid-State Circuits, vol.45, June. 2010

[29] C. H. Chen, Yi Zhang, and G.C.Temes. 2014. “11 μW 250Hz BW Two Step Incremental ADC with 100dB DR and 91dB SNDR for Integrated Sensor Interfaces”. In IEEE Custom Integrated Circuits Conference (March 2014)

[30] J. Y. Chae, K. Souri, and K.A. Makinwa. 2013. “A 6.3 μW 20 bit Incremental Zoom-ADC with 6ppm INL and 1μV offset” In IEEE Journal of Solid-State Circuits (December 2013]

[31] K. Souri and K. A. A. Makinwa 2011. “A 0.12 mm 7.4 W micropower temperature sensor with an inaccuracy of 0.2 C from 30 C to 125 C,” IEEE J. Solid-State Circuits, vol. 46, no. 7, pp. 1693–1700, Jul. 2011

[32] M. Degrauwe, et al. IDAC: “an interactive design tool for analog CMOS circuits “, IEEE Journal of Solid-State Circuits 1987

[33] R. Harjani, R. Rutenbar, L. Carley 1998. OASYS: a framework for analog circuit synthesis, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 8 (1989] 1247–1266

[34] S. Jyuo-Min, A. Sangiovanni-Vincentelli 1998. “ECSTASY: a new environment for ic design optimization“, in: IEEE International Conference on Computer-Aided Design, Santa Clara, CA, USA, 1988, pp. 484–487.

[35] W. Daems, G. Gielen, W. Sansen 2003. “Simulation-based generation of polynomial performance models for the sizing of analog integrated circuits“, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 22 (2003]

[36] J.P. Vanderhaegen, R.W. Brodersen 2004. “Automated Design Of Operational Transconductance Amplifiers Using Reversed Geometric Programming“, in Proceedings of the 41st Annual Design Automation Conference, 2004

[37] P. Mandal, V. Visvanathan 2001. “CMOS op-amp sizing using a geometric programming formulation“, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 20 (2001) 22–38

[38] M. Maghami, F. Inanlou, R. Lotfi 2008, “Simulation-equation-based methodology for the design of CMOS amplifiers using geometric programming, “ in 15th IEEE International Conference on Electronics, Circuits, and Systems, 2008, pp. 360–363

]39] H. Tang, A. Doboli, “High-level synthesis of DS modulator topologies optimized for complexity, sensitivity, and power consumption“, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 25 (2006) 597–607

[40] J. Kenney, L. Carley 1988. “ CLANS: a high-level synthesis tool for high-resolution data converters, “ in IEEE International Conference on Computer-Aided Design, Santa Clara, CA, USA, 1988, pp. 496–499

[41] R. Schreier, Delta sigma toolbox, 2000

[42] J. Ruiz-Amaya et al. “ High-level synthesis of switched-capacitor,switched-current and continuous-time SD modulators using SIMULINK-based time-domain behavioral models“, IEEE Transactions on Circuits and Systems I: 2005

[43] T.-H. Kuo, K.-D. Chen, J.-R. Chen 1996. “Automatic coefficients design for high-order sigma-delta modulators“, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing 46 (1999) 6–15

[44] F. Medeiro, B. Perez-Verdu, A. Rodriguez-Vazquez, J. Huertas 1995. “A vertically integrated tool for automated design of SD modulators“, IEEE Journal of SolidState Circuits 30 (1995)

[45] Suarez, R.E., Gray, P.R., and Hodges D.A. 1975 “AII-MOS charge redistribution analog-to-digital conversion techniques- Part 2”, IEEE J. Solid-state Circuits, 1975, SC-10, (6),

[46] J. Montanaro, R. Witek, K. Anne, and A. Black, 1996. “A 160-MHz 32-b 0.5-W CMOS RISC microprocessor,” In IEEE Journal of Solid State Circuits, vol. 31, pp. 1703–1714, Nov. 1996

[47] B. Razavi 2015. “The StrongARM Latch [A Circuit for All Seasons]”, IEEE Solid-State Circuits Magazine, Issue. 2 2015.

[48] ATK Tang. “A 3 µV-offset operational amplifier with 20 nV /√ Hz input noise PSD at DC employing both chopping and autozeroing”. In Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International, volume 1, pages 386–387. IEEE, 2002.

[49] E. Christian and G.C. Temes. “Circuit techniques for reducing the effects of op-amp imperfections: auto-zeroing, correlated double sampling, and chopper stabilization“. Proc IEEE, 84(11):1584–1614, 1996

[50] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, “Noise analysis of regenerative comparators for reconfigurable ADC architectures“, In IEEE Trans. Circuits Syst. I, vol. 55, pp. 1441–1454, July 2008.

[51] P. Rombouts and L. Weyten 1996 “Linearity Improvements on Switch Capacitor DAC“ IEEE Electronic Letters 1996

[52] White Paper 2017 “Intel’s 10 nm Technology: Delivering the Highest Logic Transistor Density in the Industry Through the Use of Hyper Scaling”

[53] K. Parthasarathy, T. Kuyel, D. Price, Le Jin, D. Chen, and R. L.Geiger, “BIST and Production Testing of ADCs Using Imprecise Stimulus”, ACM Tran. on Design Automation of Electronic Systems, October 2003.

[54] B. Murmann, "Energy limits in A/D converters," in Faible Tension Faible Consommation (FTFC), 2013 IEEE, 2013, pp. 1-4.

[55] L. Yao, M. Steyaert, and W. Sansen, "Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS," ed: Springer, 2006

[56] Blajez Nowacki “Design of Sigma-Delta Modulators for Analog-to-Digital Conversion Intensively Using Passive Circuits “ Ph.D. Thesis Universidade Nova de Lisboa May 2016

[57] The Mobile Economy 2017, GSMA, [Online]. Available: http://www.gsma.com

[58] F. Chen, S. Ramaswamy, B. Bakkaloglu “A 1.5V 1mA 80dB Passive ΣΔ ADC in 0.13µm Digital CMOS Process ”in IEEE ISSCC Dig. Tech. Papers, Feb. 2003

[59] Philippe BENABES, Richard KIELBASA, “Passive Sigma-Delta converters design,” IEEE Instrument and Measurement Technology May 2002

[60] T. Song, Z. Cao, S. Yan “A 2.7-mW 2-MHz Continuous-Time ΔΣ Modulator with a Hybrid Active–Passive Loop Filter” IEEE J. Solid-State Circuits, vol. 43, no. 2, Feb. 2008.

[61] B. Gonen, Fabio Sebastiano, Robert van Veldhoven, Kofi A. A. Makinwa “A Dynamiz Zoomin ADC ”in IEEE JSSCC Dig. Tech. Papers, Feb. 2017

[62] C. Jabbour, H. Fakhoury, V. Nguyen, and P. Loumeau “Delay-Reduction Technique for DWA Algorithms,” in IEEE Transactions on Circuits and Systems –II, Oct. 2014, Vol. 61, No. 10

[63] T. Christen, T. Burger, and Q. Huang, “A 0.13 CMOS EDGE/UMTS/WLAN tri-mode ADC with THD,” in IEEE Int.Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2007, pp. 240–241.

[64] L. Bettini, T. Christen, T. Burger and Q. Huang, “A Reconfigurable DT Modulator for Multi-Standard 2G/3G/4G Wireless ” in Proc. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Dec. 2015, Vol.5 No.4

[65] Y. Ke, P. Gao, J. Craninckx, G. Van der Plas and G. Gielen “A 2.8-to-8.5 mW GSM/Bluetooth/UMTS/DVB-H/WLAN fully reconfigurable with 200 kHz to 20 MHz BW for 4G radios in 90 nm digital CMOS,” in IEEE VLSI Symp. Dig. Tech.Papers, Jun. 2010, pp. 153–154

[66] A. Morgado et al., “A 100 kHz-10 MHz BW, 78-to-52 dB DR, 4.6-to-11 mW flexible SC modulator in 1.2-V 90-nm CMOS,” in Proc. IEEE Eur. Solid-State Circuits Conf., Sep. 2010, pp. 418–421

[67] Ken Xu et al, “A 10.2 mW multi-mode continuous-time DR ADC with 70–87 dB DR and 0.7–10 MHz bandwidth for TD-SCDMA and LTE digital receivers” in Analog Integrated Circ Sig Process (2016) 89:395–410

[68] S. Ouzounov et al., “A 1.2V 121-Mode CT ΔΣ Modulator for Wireless Receivers in 90nm CMOS,” ISSCC Dig. Tech. Papers, pp.242-243, Feb. 2007

[69] P. Crombez, G. Van der Plas, M. Steyaert and J. Craninckx, “A 500 kHz-10MHz multimode power-performance scalable 83-to-67dB DR CTΔΣ in 90 nm digital CMOS with flexible analog core circuitry”. IEEE VLSI Circuits Symp. Digest of Technical Papers, pp. 70-71, 2009

[70] J. Li, R. Zhu, T.Yi1, B. Liu, Z. Hong, “An energy-efficient 5-MHz to 20-MHz, 12-bit reconfigurable continuous-time modulator for 4G-LTE applications, ”inProc. IEEE Int. Symp. Low Power Electron. Design, Sep. 2013, pp. 163–168

[71] A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” IEEE J. Solid-State Circuits, vol. 34, no.5, pp. 599–606, May 1999

[72] B. Razavi, the StrongARM Latch [A Circuit for All Seasons], IEEE Solid-State Circuits Magazine, Issue. 2, pp. 12-17, Spring 2015

[73] Y. Fujimoto, Y. Kanazawa, P. L. Re, and K. Iizuka, “A 100 MS/s 4 MHz bandwidth 70 dB SNR ΔΣ ADC in 90 nm CMOS,” IEEE J. Solid-State Circuits, vol. 44, no. 6, pp. 1697–1708, Jun. 2009.

[74] S. Z. Asl, S. Saxena, P. K. Hanumolu, K. Mayaram, and T. S. Fiez, “A 77dB SNDR, 4MHz MASH ΔΣ modulator with a second-stage multirate VCO-based quantizer,” in Proc. IEEE Custom Integr. Circuits Conf., Sep. 2011, pp. 1–4.

[75] T. Oh, N. Maghari, and U.-K. Moon, “A 5MHz BW 70.7dB SNDR noise-shaped two-step quantizer based ΔΣ ADC,” in Proc. IEEE Symp.
VLSI Circuits, Jun. 2012, pp. 162–163.

[76] R. Zanbaghi, S. Saxena, G. C. Temes and T. S. Fiez, “A 75-dB SNDR, 5-MHz bandwidth stage-shared 2–2 MASH ΔΣ modulator dissipating 16 mW power,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 8, pp. 1614–1625, Aug. 2012

[77] C. Weng, Y. Lin and T. Lin, “A 1-V 5-MHz Bandwidth 68.3-dB SNDR Continuous-Time Delta-Sigma Modulator With a Feedback-Assisted Quantizer” IEEE Trans. Circuits Syst. I, Reg. Papers, 2017

[78] Radha Rajan, Shanthi Pavan, “A 5mW CT ΔΣ ADC with Embedded 2nd-Order Active Filter and VGA Achieving 82dB DR in 2MHz BW”

[79] Rudolf Ritter, John G. Kaufman, Joachim Becker “A 10 MHz Bandwidth, 70 dB SNDR Continuous-Time Delta-Sigma Modulator With Digitally Improved Reconfigurable Blocker Rejection” IEEE J. Solid-State Circuits, vol. 51, no. 3, Mar. 2016.

[80] Chaoming Zhang “Built-In Self-Test of RF Subsystems” Ph.D. thesis UT Austin

[81] Afsaneh Nassery, Osman Erol, Marian Verhelst, Sule Ozev, “Test signal development and analysis for OFDM systems RF front-end parameter extraction “ IEEE Transactions on Computer-Aided Design, 2012 March

[82] A. Valdes-Garcia ; J. Silva-Martinez ; E. Sanchez-Sinencio “On-Chip Testing Techniques for RF Wireless Transceivers” IEEE Journal of Design & Test of Computers