DFT Solutions for Automated Test and Calibration

of Forthcoming RF Integrated Transceivers

by

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ABSTRACT

As integrated technologies are scaling down, there is an increasing trend in the process,voltage and temperature (PVT) variations of highly integrated RF systems. Accounting for these variations during the design phase requires tremendous amount of time for prediction of RF performance and optimizing it accordingly. Thus, there is an increasing gap between the need to relax the RF performance requirements at the design phase for rapid development and the need to provide high performance and low cost RF circuits that function with PVT variations. No matter how carefully designed, RF integrated circuits (ICs) manufactured with advanced technology nodes necessitate lengthy post-production calibration and test cycles with expensive RF test instruments. Hence design-for-test (DFT) is proposed for low-cost and fast measurement of performance parameters during both post-production and in-field operation. For example, built-in self-test (BIST) is a DFT solution for low-cost on-chip measurement of RF performance parameters. In this dissertation, three aspects of automated test and calibration, including DFT mathematical model, BIST hardware and built-in calibration are covered for RF front-end blocks.

First, the theoretical foundation of a post-production test of RF integrated phased array antennas is proposed by developing the mathematical model to measure gain and phase mismatches between antenna elements without any electrical contact. The proposed technique is fast, cost-efficient and uses near-field measurement of radiated power from antennas hence, it requires single test setup, it has easy implementation and it is short in time which makes it viable for industrialized high volume integrated IC production test.

Second, a BIST model intended for the characterization of I/Q offset, gain and phase mismatch of IQ transmitters without relying on external equipment is introduced. The proposed BIST method is based on on-chip amplitude measurement as

in prior works however,here the variations in the BIST circuit do not affect the target parameter estimation accuracy since measurements are designed to be relative. The BIST circuit is implemented in 130nm technology and can be used for post-production and in-field calibration.

Third, a programmable low noise amplifier (LNA) is proposed which is adaptable to different application scenarios depending on the specification requirements. Its performance is optimized with regards to required specifications e.g. distance, power consumption, BER, data rate, etc.The statistical modeling is used to capture the correlations among measured performance parameters and calibration modes for fast adaptation. Machine learning technique is used to capture these non-linear correlations and build the probability distribution of a target parameter based on measurement results of the correlated parameters. The proposed concept is demonstrated by embedding built-in tuning knobs in LNA design in 130nm technology. The tuning knobs are carefully designed to provide independent combinations of important performance parameters such as gain and linearity. Minimum number of switches are used to provide the desired tuning range without a need for an external analog input.

To My Exceptional Mother

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1 INTRODUCTION

1.1 Motivation

Expanding demand for RF system-on-chip (SoC) devices has fueled the integration of various RF components, such as low-noise amplifiers (LNA), mixers and antennas together with the baseband, analog, and digital subsystems into a single chip. However, this level of integration, while essential to meet increasing performance/power requirements, brings about challenges in terms of test and calibration of RF devices. These highly integrated RF transmitters are increasingly susceptible to process, voltage, and temperature (PVT) variations. The simultaneous constraints of low cost and high-performance places a burden on the design, manufacturing, and test of these components. Accounting for these variations during the design phase requires tremendous amount of time for prediction of RF performance and optimizing it accordingly. During circuit design, a designers primary goal is to meet circuit specifications under given process variations. In doing so, designers spend significant effort to minimize the effect of process variations or in other words, they try to de-sensitize their design with respect to process variations.Thus, there is an increasing gap between the need to relax the RF performance requirements at the design phase for rapid development and the need to provide high performance RF circuits that function with PVT variations. No matter how carefully designed, RF integrated circuits (ICs) manufactured with advanced technology nodes necessitate lengthy post-production calibration and test cycles with expensive RF instruments [1,2]. Hence, there is a growing interest in on-chip measurement of performance parameters for both post-production and in-field calibration purposes[3]. Built-in self-test (BIST) and calibration of RF circuits can

potentially enable production of low cost and robust electronics on rapidly evolving digital IC processes. BIST can replace the expensive RF test instrumentation and can be used for post-production and in-field testing of the device under test (DUT) to improve performance via digital or analolg calibration routines. The calibration is realized by built-in tuning knobs allowing for trade-offs between RF specifications. Different calibration mechanisms are introduced in the literature in the form of bias current, bias voltage, and passive bank adjustments [4-6].

One of the major attraction of integrated RF transmitters lies on the uprising field known as Internet of Things (IOT). IOT nodes are rapidly being integrated into our daily lives in diverse applications ranging from health care to home automation, smart city to environmental monitoring [8-11] with over $200B projected market potential[7]. These nodes typically employ one-way communications using a high-end transmitter without a corresponding receiver. Testing of such transmitter-only systems poses an additional challenge. Furthermore, IOT devices have their own application-specific requirements which demands for multi-standard multi-mode transceivers. Conventionally the IOT interconnected objects are realized by existing commercial off-the-shelf components (COTS) which are designed and optimized for a certain communication standard or a specific use [12-13]. However, using separate radios is power hungry, costly and the interconnections are not optimized with regards to an application-specific requirement. On the other hand, using customized radio transceiver ICs for each specific application is not practical due to high overall product costs (OPC). A cost-effective solution is a single radio transceiver adaptable to localized IOT applications. Reconfigurability and in-field calibration enables power optimal interconnections within IOT devices. The reconfigurable transceiver is tweaked on the spot based on application-specific requirements such as gain, linearity, BER, etc. Having such adaptable RF ICs in the marketplace will enable IoT developers to

optimize the overall system performance without having a deep RF design experience and without having to incur the cost of taping out an entirely new design for each product.There are some form of post-production calibration and reconfiguration for RF devices [14-16]. The calibration is realized by built-in tuning knobs allowing for trade-offs between RF specifications. In general, RF circuits are designed to include calibration hooks in bias or passive components to meet target specifications. These techniques employ fine and continuous tuning using analog control signals generated by simple low-speed digital to analog converters (DACs). However, DACs are power hungry and require notable dedicated silicon area. Besides, the DAC settling time and conversion rate limits the critical in-field adaptation pace. Hence,analog input signals are not desirable in RFIC design. Besides, these methods typically provide limited calibration space.

Due to process variations, the performance parameters of the DUT are not fixed for all parts. This necessitates an in-field verification of reconfiguration state with respect to the target performance. The reconfiguration and verification procedure can be iterative or one-time. The iterative procedure makes a measurement with each adjustment of the tuning knobs until the target performance is achieved [15,5,17]. This procedure is time consuming.Also the general trend of the performance with respect to the tuning knob value must be known which makes this approach difficult for more complicated and nonlinear trends. In one-time procedure, tuning knobs are programmed only once with respect to a Mean-Squared-Error(MSE) curve obtained from characterization of some number of samples[4]. , this results in calibration error if there is deviation from the DUT performance and the MSE curve at a chosen knob value. In [4], the DUT calibration knobs are adjusted using the performance curves. The performance curve represents the relation between performance parameter and the knob value of a golden DUT. Since it is only obtained for one sample (Golden

DUT) and is used for tuning the rest of samples, it does not take into account the process variation between DUTs for knob value selection hence causes significant calibration error. Furthermore, the number of tuning parameters are limited using the above methods.

An intermediate approach is proposed using statistical modeling. The statistical based method on the other hand, develops a nonlinear prediction model to adjust the tuning knobs realizing easy simultaneous tuning of parameters[18,19]. This method requires a training set and is fast since it is usually done in one or two steps. This methodology can be used for on-chip self-testing and calibration. Statistical modeling allows for easier model generation by relying on machine learning [20].

Our proposed statistical modeling approach addresses an automated fully digital reconfiguration scheme which sensitizes the tuning range to process variation.

Cartesian transmitters have several important performance parameters, including I/Q gain and phase imbalance and baseband DC offsets. If these impairments can be measured at production time or in the field, they can be digitally calibrated in the baseband with minimum computational overhead. Researchers have presented several techniques in the literature for the characterization of RF transceivers which target the entire transmitter-receiver chain. In [20-24], loop-back mode testing is proposed for specification test of RF transceivers. The analytical model for the entire path is extracted and analytical/numerical techniques are used to simultaneously solve transmitter and receiver parameters. In [24], a self-test method for zero-IF transceivers using loop-back and a small BIST circuitry is proposed to determine critical parameters, such as I/Q imbalance. However, techniques that rely on the presence of a full I/Q receiver are not applicable to transmitter-only systems. Another approach is measuring the output power of the transmitter using RF amplitude measurement techniques [25-27]. RF amplitude detection methods use additional cir-

cuitry to generate a DC or low frequency signal which is highly correlated to the DUT performance parameters. Conventional detectors, such as root mean square (RMS) detectors or envelope detectors, are subject to similar process variations as the DUT, which affects the measurement accuracy. To address this problem, other techniques for on-chip amplitude measurement that are independent of process variations are introduced recently in the literature [25]. However, since the I and Q signals are combined, amplitude measurement only does not provide adequate information for calibration. Moreover, in order to account for BIST variations, majority of amplitude measurement techniques would require a calibration phase that involves an external source. Also detectors do not provide system-level measurements.

Future RF transceivers are expected to integrate the entire system, from base band to antenna. Many emerging applications use beam forming, which necessitates RF phased arrays and multiple antennas integrated on the same die. This integration presents a challenge in testing the entire system including antennas.Design and manufacturing of integrated phased arrays have been widely explored and demonstrated in the past decade [28-30]. Integration of antennas together with the phased arrays eliminates the need for additional off-chip interconnects which contributes to more loss and introduces additional phase error. At the higher target frequencies, even a small deviation in interconnect dimensions would result in significant phase shift [30]. Silicon integration solves the problems that exist with resolution and dimensional control but brings about new challenges. Increasing process variations in finer geometries makes it difficult to match the gains and phases of the phase shift elements which are typically implemented using active circuitry [28]. Even a few degrees of error could degrade the phased array operation hence necessitates calibration. Existing BIST methods employ an electrical connection to the array elements. In [31], the BIST operates with antenna ports open during post production test and with

antennas connected in the field however antennas are excluded from the BIST measurement loop. In [32], a 77GHz phased array transceiver with on-chip antennas is introduced. Similarly, for testing the transceiver, the antennas are bypassed.In [33], the authors present a phased array BIST method using a simple self-mixing down-converter. Using resistive couplers and a matched switch network, the RF signal is first applied to each element separately. The next step is to apply the RF signal to a pair of antennas and measure the combined signal power. Using a mathematical model, the phase and gain mismatches are extracted from three measurements for each antenna pair. The BIST work in [33] also requires and electrical connection (via a directional coupler) to the phase array output and bypasses the antennas.While there is extensive work on testing integrated phased arrays using electrical connections [31,33,34,35], contact-less near-field testing of integrated phased array systems including the antenna has not garnered much attention. This is due to the fact that until recently, phased array systems with many antennas have been primarily used in military applications where more resources can be devoted to testing.

The effective calibration process requires direct measurement of phase and gain mismatches between phased array elements in the RF domain, which includes the active phased array as well as the antennas. This is a challenging problem due to two reasons. First, the phase and gain mismatches between RF elements have a non-linear effect on the radiated power in the desired direction. However, calibration requires decoupling them from one another. Second, due to the integration of the antenna, the signal is no longer accessible via an electrical connection, which necessitates measuring radiated power. Unfortunately, the effective combination of antenna signals occurs only in the far field, which can be tens of multiples of the wavelength. For instance, for a 60 GHz 16-element array system with half-wavelength separation, the effective far field region starts at a distance of approximately 56cm. Clearly, placing

the measurement equipment at this distance is not practical. Hence, the radiated power needs to be measured in the near-field while in the normal mode of operation, the RF system is likely to be used in the far-field. Hence, it is also necessary to include the effect of near-field measurement and extrapolate the measurements to far field.It is more convenient to measure phased array transmitter and receiver signals in a close distance with respect to each other. Near-field measurement techniques have been developed to provide a more effective method to cut down the production and development costs of antenna systems [36]. Application of this technique includes element failure diagnosis and phased array calibration [37]. The methods proposed in [36,37] also require a mechanically moving RF probe. Due to the need for mechanical movement and time-consuming data collection, these techniques require both expensive test set-up and long test times.Unfortunately, none of the existing methods address the problem of fast and cost-effective contact-less near-field testing of integrated RF phased array mismatches including the antennas. Testing on-chip antennas integrated with phased-arrays requires new methods to include antenna mismatches as well as phased-array mismatches. Since the output power is combined in radiated form and cannot be separated, a new approach is desirable to detect all mismatches based on radiated measurements.

1.2 Outline

In chapter 2, We present a methodology for contact-less near-field testing of phased array systems that is suitable for high volume production environment. We propose a fast and cost-efficient test method to characterize active phased array antenna elements in terms of their gain, gain and phase mismatch. Our proposed technique uses near-field measurement of radiated power from antennas, thus the test path includes mismatches in the antennas as well as in active modules[38]. Unlike existing

contact-less measurement methods, our approach requires a single test setup and a short test duration. These qualities makes the proposed approach viable for high volume production testing. Our proposed method is based on analytical derivation of mutual impedances of radiated signals and measuring the amplitude and phase of the signals at the receiver end. Using this mathematical model and the measured signal power, we decouple the contribution of each phased array element on the transmitter side. We determine the gain and phase mismatches using analytical solutions. We evaluate the accuracy of the proposed approaches using MATLAB and ANSYS HFSS simulations under various environment noise and process variation scenarios.

In chapter 3, we present a low-overhead BIST method intended for the characterization of I/Q offset, gain and phase mismatch of IQ transmitters without relying on external equipment. Due to the lack of a receiver, low-cost test techniques, such as loop-back, cannot be used. The proposed BIST uses simple circuitry and a single test setup. The target parameters are analytically computed independent from internal BIST parameters which eliminates the need for initial calibration phase. All measurements are in DC and no external RF signal generation is required. Results show that the proposed method provides adequate estimation accuracy for digital calibration.The BIST circuit can be used for both post-production and in-field calibration[39]. The proposed BIST method is based on on-chip gain measurement as in prior works. However, in the proposed technique, variations in the BIST circuit do not affect the target parameter estimation accuracy since measurements are designed to be relative and independent of the BIST parameters. The proposed BIST method uses full DC excitation in the baseband and DC measurements at the BIST output. This technique, unlike the previous approaches in literature [25-27], does not need any initial calibration for the BIST. Since performance characterization is independent of the internal BIST parameters, no knowledge of the BIST parameters is required. The

simulation and hardware measurement results show consistency and accuracy of the proposed method.

As opposed to post-production calibration which is optimizing the device with respect to a single application, in chapter 4, we develop existing mechanisms to reconfigure the RF device for optimized performance with respect to multiple IOT applications. We will exploit existing calibration approaches and mechanisms and enhance them to further sensitize the circuit to process/layout variations. This sensitization is expected to spread and shift the circuit performance distribution over process variation. Our technique proposes a programmable device which adapts to different situations depending on the application requirements for optimized performance with respect to multiple IOT applications. Its performance is optimized with regards to required specifications e.g. distance, power consumption, BER, data rate, etc. We propose to use statistical models to capture the correlations among measured performance parameters and reconfiguration modes. We employ machine learning technique to capture these non-linear correlations and collapse the probability distribution of a target parameter based on measurements of correlated parameters. We have demonstrated the concept by designing an LNA with built-in tuning knobs. The tuning knobs are carefully designed to provide independent adjustment of important performance parameters such as gain and linearity. Minimum number of switches are used to provide the desired tuning range without a need for an external analog input. The simulation and hardware measurement results show consistency and proves the applicability of the proposed technique.

Last, chapter 5 summarized this dissertation and its achievements for modern RF transceivers.

CHAPTER 2

2 CONTACT-LESS NEAR-FIELD TEST OF ACTIVE INTEGRATED RF PHASED ARRAY ANTENNAS

2.1 Phased Array Overview

A phased array antenna is composed of several radiating elements each with a phase shifter and a variable gain amplifier. Beams are formed by shifting the phase of the signal emitted from each radiating element, to provide constructive or destructive interference so as to steer the beams in the desired direction. The inherent phase difference between each element is equal to:

$$\Delta\phi = \frac{2\pi cos(\theta)}{\lambda} \qquad (2-1)$$

By controlling the phase difference between the elements, the maximum radiation can be achieved in any desired direction to form a scanning array[40].

Phased-array antennas play a significant role in communication systems that rely on beam forming. Due to improved signal-to-noise ratio, effective isotropic radiated power, antenna pattern shaping, wider channel bandwidth, and spatial interference cancellation, phased arrays have been widely used in high end communications equipment (i.e. military systems) and are proliferating into the consumer electronics domain [41]. It is expected that future communications systems will employ beam forming at several tens of GHz frequencies [42,43]. Beam forming is enabled via RF phased arrays where the phase shift of each antenna element is adjusted to steer the beam in the desired direction. Design and manufacturing of integrated phased arrays have been widely explored and demonstrated in the past decade [28-30]. Integration of antennas together with the phased arrays eliminates the need for additional off-chip

interconnects which contributes to more loss and introduces additional phase error. At the target frequencies, even a small deviation in interconnect dimensions would result in significant phase shift [30]. Silicon integration solves the problems that exist with resolution and dimensional control however it is also challenging. Increasing process variations in finer geometries makes it difficult to match the gains and phases of the phase shift elements due to larger process variations. Even a few degrees of error could degrade the phased array operation. Hence, it is necessary to calibrate the phase and gain imbalances.

2.2 Physical Model

2.2.1 Mutual Impedance of Two Dipoles

Finding the mutual impedance between elements requires knowledge of the near-field radiations since they are usually a fraction of the wavelength apart. The geometry of the two identical ($l_1 = l_2 = l$) parallel diploes in the near field is shown in Figure 2.1. The antennas are placed within a horizontal distance D, and a vertical distance d from each other. For a finite dipole with a sinusoidal current distribution, the magnitude of the tangential electric field can be expressed in terms of its geometric properties and the current that is flowing through it. Eqn. (2-2) defines the current distribution of a thin dipole and Eqn. (2-3) defines the electric field of the dipole [40].

$$I(z') = I_m sin[k(l/2 - |z'|)] \qquad (2-2)$$

$$E_z = -j\frac{I_m}{4}[\frac{e^{-jkR_1}}{R_1} + \frac{e^{-jkR_2}}{R_2} - 2cos(\frac{kl}{2})\frac{e^{-jkr}}{r}] \qquad (2-3)$$

Where l is the length of the dipole, $R_1 = \sqrt{x^2 + D^2 + (z - |l/2|)^2}$, $R_2 = \sqrt{x^2 + D^2 + (z + |l/2|)^2}$, and $r = \sqrt{x^2 + D^2 + z^2}$.

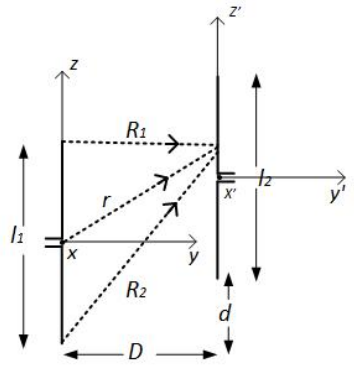


Figure 2.1: Two dipole antennas in staggered parallel position

The induced open circuit voltage at antenna 2, referred to its current at input terminals, due to radiation from antenna 1 is given by Eqn.(2-4).

$$V_{2_1} = \frac{-1}{I_{2_i}} \int_{\frac{-l}{2}}^{\frac{l}{2}} E_{z_{21}}(z') I_2(z') dz' \qquad (2-4)$$

Where $E_{z_{21}}(z')$ is the electric field component radiated by antenna 1 along antenna 2, $I_2(z')$ is the current distribution of antenna 2, and $z' = z - d$. Hence, the mutual impedance, referred to the input current at antenna 1 is given by Eqn. (2-5).

$$Z_{2_{1i}} = \frac{-1}{I_{1i} I_{2i}} \int_{\frac{-l}{2}}^{\frac{l}{2}} E_{z_{21}}(z') I_2(z') dz' \qquad (2-5)$$

By substituting $E_{z21}(z')$ from Eqn. (2-3) and $I_2(z')$, I_{1i},I_{2i} from Eqn. (2-2), the expression for the mutual impedance, referred to the input current, is obtained in Eqn. (2-6).

$$Z_{21i} = j \frac{30}{sin^2(kl/2)} \int_{\frac{-l}{2}}^{\frac{l}{2}} sin[k(l/2 - |z'|)][e^{-jkR_1}/R_1 + e^{-jkR_2}/R_2 - 2cos(kl/2)e^{-jkr}/r] dz' \qquad (2\text{-}6)$$

Therefore, the mutual impedance referred to the current maxima is achieved in Eqn.

(2-7).

$$Z_{2_{1m}} = Z_{2_{1i}} sin^2(kl/2) \qquad (2-7)$$

The closed form solution for the integral in (2-6) is presented in [44] for any arbitrary length dipole both for parallel and collinear configurations. To simplify the complex expressions, a dipole length of $\lambda/2$ is assumed as it is the case for most phased arrays. The closed form expression for mutual impedance of a $\lambda/2$ dipole is presented using induced EMF method [18]. It is shown that the mutual impedance is reliant on the antennas type (dipoles here), antenna length, and horizontal and vertical distances between antennas.

2.2.2 Test Setup

The proposed phased array test setup is depicted in Figure 2.2. It consists of two identical arrays. The transmitting phased array antenna is the DUT. An identical phased array antenna system, coplanar with the DUT, is used as the probe antenna on the receiver side. The probe antenna is a with fully characterized good die. Since the test set-up is shared by many thousand dies, the cost of this characterization is not an issue. The DUT is placed on the load board via a socket and the probe antenna is fixed onto the load board. The input RF signal is applied at the input of the phased array via a direct electrical connection. The RF signal is captured at the output of the probe antennas via directional couplers or direct electrical connection, whichever one is available. The captured output is processed with respect to the mathematical model to determine gain and phase mismatches in the DUT.

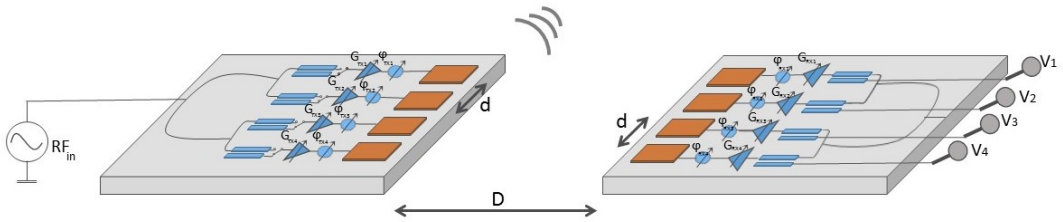


Figure 2.2: Test setup for the proposed technique

2.3 Mathematical Model

Considering the test setup configuration in Figure 2.2., the measurements are performed at the ports of the receiving probe antennas($O_1 - O_4$) which are assumed fully characterized. The phase and amplitude of the signals at the port of the transmitting phased array antennas ($i_1 - i_4$) are target parameters. The coupling between antennas is described by the mutual impedance matrix. An analytical modeling approach is used to solve for the target parameters.

The proposed approach is based on determining the transfer matrix which links source currents to the output voltages using the mutual impedance model explained in Section II. The coupling matrix between the transmitter and the receiver which corresponds to the test setup in Figure 2.2, is a 4×4 matrix and has the following form:

$$Z_{m_T R} = \begin{bmatrix} Z_{i_1,O_1} & Z_{i_2,O_1} & Z_{i_3,O_1} & Z_{i_4,O_1} \\ Z_{i_1,O_2} & Z_{i_2,O_2} & Z_{i_3,O_2} & Z_{i_4,O_2} \\ Z_{i_1,O_3} & Z_{i_2,O_3} & Z_{i_3,O_3} & Z_{i_4,O_3} \\ Z_{i_1,O_4} & Z_{i_2,O_4} & Z_{i_3,O_4} & Z_{i_4,O_4} \end{bmatrix} \qquad (2-8)$$

Where Z_{i_n,O_m} represents the mutual impedance between nth antenna at the transmit-

ter side and mth antenna at the receiver side. Due to the symmetry, $Z_{i_n,O_m} = Z_{i_m,O_n}$. It can be expressed by the real and the imaginary parts as shown in Eqn. (2-10).

$$Z_{i_n,O_m} = R_{i_n,O_m} + jX_{i_n,O_m} \qquad (2-9)$$

$$R_{i_n,O_m} = -\eta/8\pi cos(w0_n, m)[-2C_i(w_{1_n,m}) - 2C_i(w'_{1_n,m})$$
$$+C_i(w_{2_n,m}) + C_i(w'_{2_n,m}) + C_i(w_{3_n,m}) + C_i(w'_{3_n,m})]$$
$$+\eta/8\pi sin(w_{0_n,m})[2S_i(w_{1_n,m}) - 2S_i(w'_{1_n,m}) - S_i(w_{2_n,m})$$
$$+S_i((w'_{2_n,m}) - S_i(w_{3_n,m}) + S_i(w'_{3_n,m})] \qquad (2-10a)$$

$$X_{i_n,O_m} = -\eta/8\pi cos(w0_n, m)[S_i(w_{1_n,m}) + S_i(w'_{1_n,m})$$
$$-S_i(w_{2_n,m}) - S_i(w'_{2_n,m}) - S_i(w_{3_n,m}) - S_i(w'_{3_n,m})]$$
$$+\eta/8\pi sin(w_{0_n,m})[2C_i(w_{1_n,m}) - 2C_i(w'_{1_n,m}) - C_i(w_{2_n,m})$$
$$+C_i((w'_{2_n,m}) - C_i(w_{3_n,m}) + C_i(w'_{3_n,m})] \qquad (2-10b)$$

Where $C_i(x)$ and $S_i(x)$ are the cosine and sine integrals and $w_{0_n,m}$, $w_{1_n,m}$, $w'_{1_n,m}$, $w_{2n,m}$, $w'_{2_n,m}$,$w_{3_n,m}$, $w'_{3_n,m}$ are functions of the physical properties of the test setup. Equations (2-11a) to (2-11g) expresses this dependency. Due to the symmetry of the array configuration and identical antenna elements, extracting the first column of the matrix of Eqn. (2-7), gives us the rest of the elements as well.

$$w_{0_1,m} = k((m-1)d + (m-1)l) \qquad (2-11a)$$

$$w_{1_1,m} = k(\sqrt{D^2 + ((m-1)d + (m-1)l)^2} + (m-1)(d+l)) \qquad (2-11b)$$

$$w'_{1_1,m} = k(\sqrt{D^2 + ((m-1)d + (m-1)l)^2} - (m-1)(d+l)) \qquad (2-11c)$$

$$w_{2_1,m} = k(\sqrt{D^2 + ((m-1)d + (m-2)l)^2} + (m-2)(d+l)) \qquad (2-11d)$$

$$w'_{2_1,m} = k(\sqrt{D^2 + ((m-1)d + (m-2)l)^2} - (m-2)(d+l)) \qquad (2-11e)$$

$$w_{3_1,m} = k(\sqrt{D^2 + ((m-1)d + ml)^2} + (m-1)d + ml) \qquad (2-11f)$$

$$w'_{3_1,m} = k(\sqrt{D^2 + ((m-1)d + ml)^2} - (m-1)d - ml) \qquad (2-11g)$$

2.4 Test Flow

The flow of the proposed near-field test methodology is shown in Figure 2.3. Prior to high volume manufacturing testing, in the off-line phase, the mutual coupling is established based on the antenna physical properties, and dimensions of the test set-up. The receiver probe antenna is characterized in terms of its mismatches and mutual antenna impedance. These mismatches are included in the measurements which can be de-embedded from the mutual impedance model. This characterization is done once per tester load board and the same probe antenna is used during the test process. During production testing (the online phase), the RF signal is applied at the input of the phased array. If the phased array is integrated with an active transmitter, a directional coupler can be used to inject the RF signal, as in prior test approaches [34,38,45]. The output of each antenna element is measured at the output of the probe antenna. The source currents at the transmitting array are obtained by multiplying the mutual impedance inversed matrix by the measured voltage at each probe antenna in the receiving array, as expressed in (2-12).

$$\vec{I_s} = Z^{-1}_{m,TR}\vec{V_m} \qquad (2-12)$$

Each element of $\vec{V_m}$ is represented by an amplitude A_{rxj} and a phase α_{rxj}, plus the gain factor, G_{rxj}, and a path phase ϕ_{rxj} due to the on-chip circuitry on the signal path to the probe.

$$V_{m_j} = G_{rxj}A_{rxj}e^{-j(\alpha_{rxj}+\phi_{rxj})} \qquad (2-13)$$

As shown in Eqns. (2-9) to (2-11), $Z_{m,TR}$ depends on physical properties of the test setup including antenna separation, d, distance between the transmitting array and the receiving array, D, antenna element dimension, l, and antenna element type. Next, source voltages are obtained by Eqn. (2-14) by employing the self and mutual couplings between antennas within the DUT.

$$\vec{V_s} = Z_{m,T}\vec{I_s} \qquad (2-14)$$

Where $Z_{m,T}$ is a 4×4 matrix as well and is correlated to the dimensions of the transmitting array. Each element of $\vec{V_s}$ is represented by a source amplitude A_{in}, a gain factor G_{txj}, a phase ϕ_{txj} and a phase mismatch $\Delta\phi_j$.

$$V_{s_j} = G_{txj}A_{in}e^{-j(\phi_{txj}+\Delta\phi_j)} \qquad (2-15)$$

The G_j and $\Delta\phi_j$ are our target parameters and are estimated as explained in the next section.

The proposed technique requires four measurements over a single time frame and several matrix multiplications. The size of the matrix is determined by the phase array element size. Currently, for commercial systems, these matrices are 16x16, and for military systems, these matrices can be as large as 256x256. Since the number of elements is limited by physical dimensions, the matrices will not grow significantly regardless of application. For our experimental set-up, including computation time, for an 4x1 array, the overall test time is estimated to be less than 5ms.

2.5 Evaluation of The Measurement Method

In order to demonstrate and evaluate the proposed test methodology, we have derived the mathematical model and emulated a 4-element array. Although we experiment

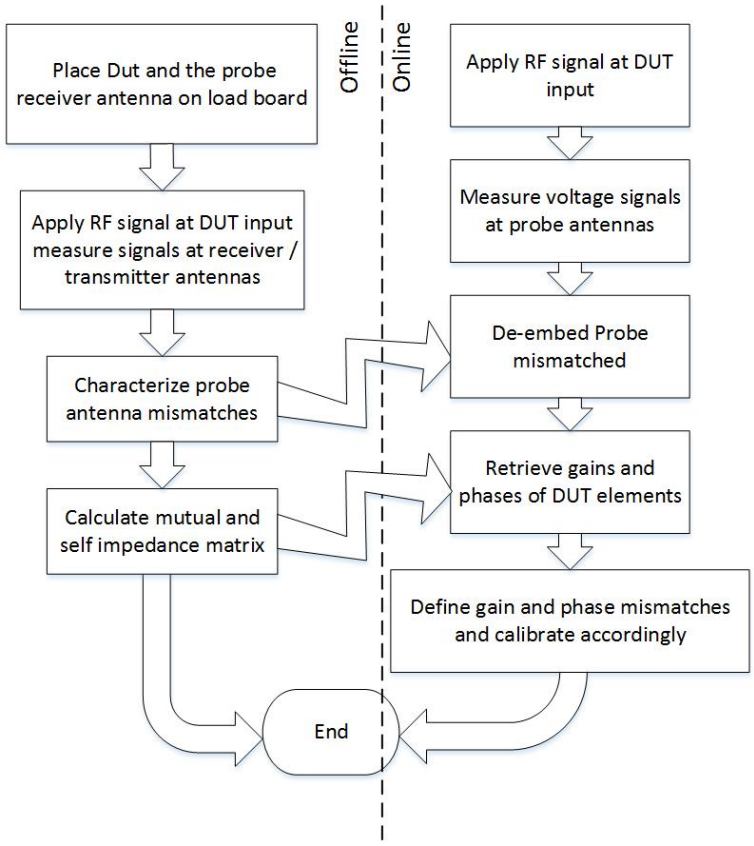


Figure 2.3: Test flow diagram

with a 4-element system, we strive to obtain a test accuracy that can be suitable up to 32-element systems. Table 2.1 shows reported post-calibration element gain and phase errors for various 16-element and 32-element systems reported in the literature. Note that, measurement and calibration are either conducted using electrical connection [35,36-48], or over the air by measuring main lobe and side lobe powers using a movable RF probe in the far field [49]. We strive to provide measurement accuracy that can enable this level of calibration with the antenna in the loop, and in the near field. In order to achieve this, we set our maximum error goal as half the calibrated phase and gain error for the reported work. Thus, our goal is to measure gain mismatch within 4% error and phase error within 2° error.

Table 2.1: Reported phased arrays and calibrated performance

Ref	[35]	[48]	[46,47]	[49]
#Element	16	16	32	32
Gain Error	N/A	16%	9%	8%
Phase Error	4°	9°	5°	5°

The operation frequency used in the experiments is 30GHz with a 10MHz bandwidth. Antennas are laid out as $\lambda/2$ dipoles, separated with $d = \lambda/4$ on-chip distance. With these variables, the far field of the antenna system is established approximately beyond 10cm. The distance between the arrays in the test environment (D) is set as $D = 2\lambda$ (2cm) , which places the receive antenna system in the near-field of the transmit antenna system. Phased array noise figures reported in the literature are generally below 10dB [31,35]. To account for additional environment noise, the thermal noise in the test environment is set at 20dB above the thermal noise level at -84dBm (KTB+20dB). We have experimented with up to 10 phase mismatch and 25% gain mismatch for the DUT. Figure 2.4 shows the MATLAB emulation platform for the proposed method. In order to evaluate the methodology for a wide set of random gain and phase mismatches, we use Monte-Carlo simulations for 100 samples. Figure 2.5 shows the comparison between estimated and actual gain and phase mismatches between transmitter array elements for various steering beam directions. Table 2.2 shows the phase difference between elements for each desired beam steering direction for a uniform linear array with $\lambda/2$ dipole elements by finding the total array factors maxima.

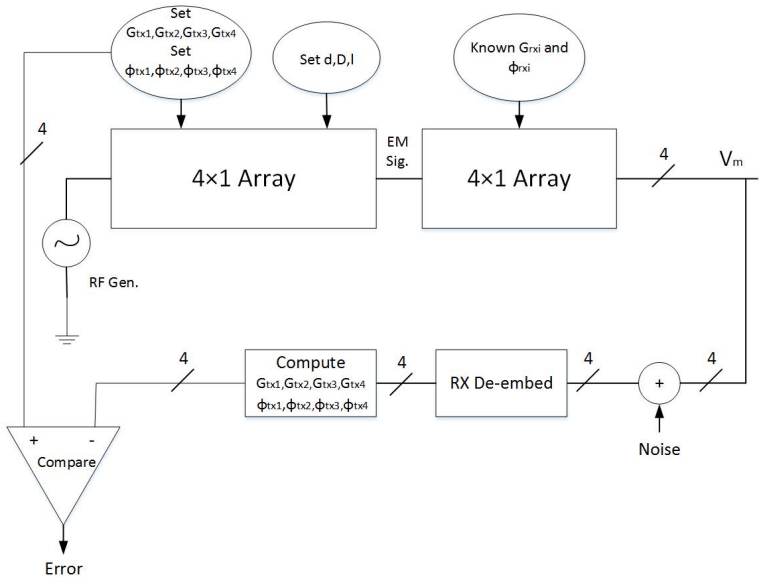
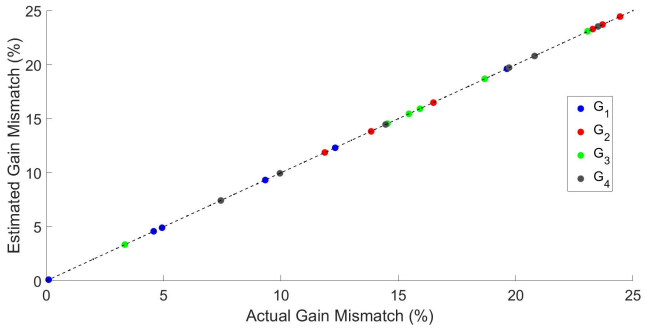


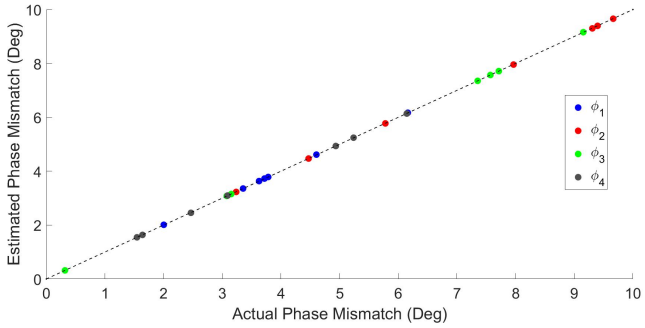
Figure 2.4: Matlab emulation platform

Table 2.2: Directionallity vs. elements phase difference

θ_s	$\Delta\phi$
$40°$	$-120°$
$64°$	$-60°$
$90°$	$0°$
$116°$	$60°$
$140°$	$120°$



(a)

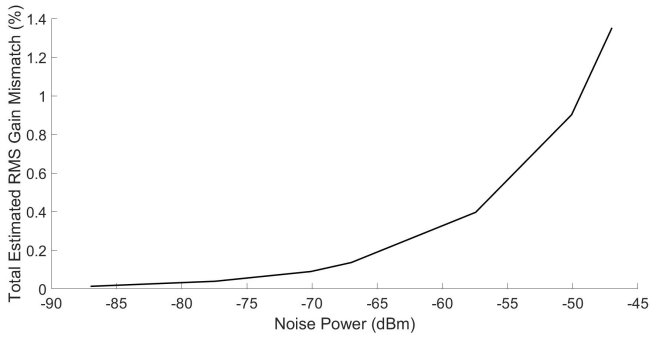


(b)

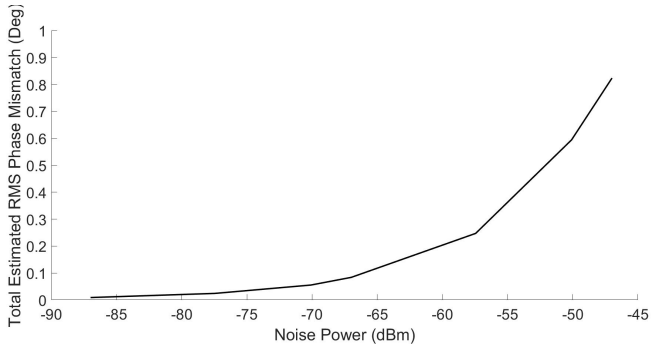
Figure 2.5: Estimated vs. actual a) gain mismatch b)phase mismatch at -80dBm noise power

2.5.1 Effect of Measurement Noise

The effect of measurement noise power on estimated source voltages is investigated at $\theta_s = 60°$. Figure 2.6(a) shows the total amplitude RMS error of the source voltages with respect to the noise power. Figure 2.6(b) shows the total phase RMS error of the source voltages with respect to the noise power. Based on our accuracy target, the proposed method works well up to -50dBm noise power, which is much larger than what we expect in a production test environment even when multiple such devices



(a)



(b)

Figure 2.6: (a) Total estimated gain mismatch (b) Total estimated phase mismatch

are tested on the same floor. Despite the fairly low SNR at -50dBm noise power, the proposed technique produces the desired accuracy. We conclude that environment noise is not a significant source of error for the proposed technique.

We have further investigated the effect of error in distance between antennas, D, and error in antenna separation, d, on gain and phase estimation RMS errors. Figure 2.7 shows the effect of errors in distance between transmit and receive antennas. In order to meet the outlined accuracy requirement (2° error in phase mismatch measurement and 2% error in gain mismatch measurement), D needs to be known within less than 1% error. This distance is set by the tester load board, as well as

the DUT socket dimensions.The variation in the device interface board (DIB) is in the order of few μm. Thus, $10\mu m$ variation in D translates to 0.05% error for which the corresponding estimated gain and phase mismatch error can be found from the graphs in figure 2.7.

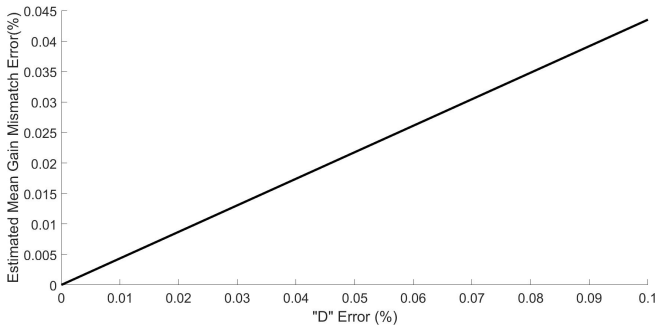
The effect of error in antenna separation, d, is shown in Figure 2.8. Antenna separation, d, is a design parameter and will be affected by lithographic process variations. However, this separation is typically in the order of millimeters for higher frequencies, where lithographic errors are in terms of nano-meters. Hence, we do not expect that the antenna separation would deviate significantly from the design-specified value.

The proposed technique is applicable to any arbitrary setup and array configuration as long as the mutual impedance is characterized. The mutual impedance between antennas depend only on the physical characteristic of the test setup such as antenna type, antenna dimension, distances between antennas, etc. For instance, the mutual impedances between elements of an array of patch antennas, are demonstrated in [50,51].

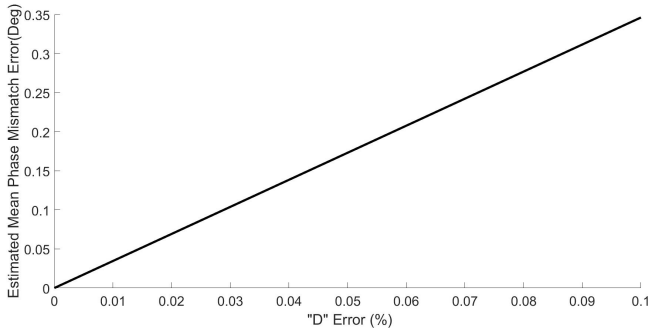
2.5.2 Effect of Process Variation

Since the mutual impedance obtained during production test is fixed for all chips, the accuracy of our method is subject to chip-to-chip process variations. To illustrate the effect of process variation on the accuracy of the proposed method, the test setup of Figure 2.1 is simulated in ANSYS HFSS. The patch antenna array of 4-by-1 is designed at 30GHz on a Rogers3006 substrate. Up to 10 phase mismatch and 25% gain mismatch are injected into the DUT.

Further, the process corner is extracted from 130nm CMOS process design manual



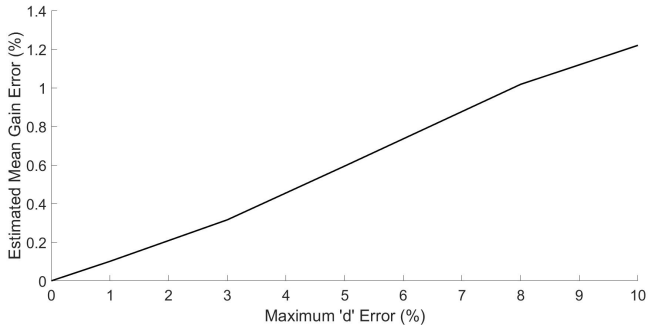
(a)



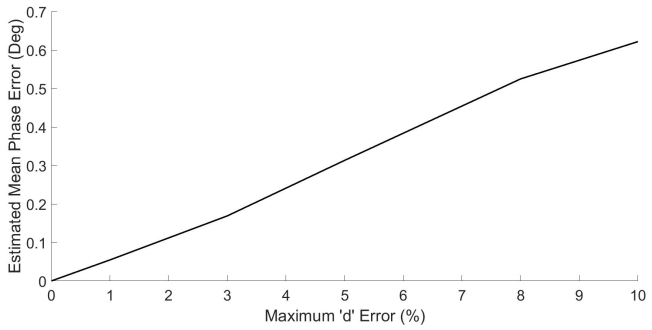
(b)

Figure 2.7: Effect of error in 'D' on(a)Estimated mean gain mismatch (b) Estimated mean phase mismatch

[52]. Length variation equal to the half of required minimum space (600nm) is injected in all the dimensions. Metal thickness variation is also inserted ($4\mu m \pm 0.5\mu m$). Figure 2.9 shows the patch antenna structure and geometric variations. The impedance matrices $Z_{m,T}$ and $Z_{m,TR}$ are obtained before and after process variation and the gain and phase mismatches are calculated in both cases to find the estimation error due to process variation. On top of process variations, other sources of error including thermal noise, receiver noise figure, quantization noise and load board variation, are added and the DUT antennas mismatches are calculated. The estimation errors are



(a)



(b)

Figure 2.8: Effect of error in 'd' on(a)Estimated mean gain mismatch (b) Estimated mean phase mismatch

tabulated in Table 2.3. It is observed that the maximum phase mismatch estimation error is within 2° and gain mismatch estimation error is within 4%. Thus, this measurement technique is suitable to replace the costly, far-field measurements with mechanical moving arm RF probe, at least up to 32-element systems.

Finally, the effect of overall measurements error and process variation is investigated in the array far-field pattern. Figure 2.10 illustrates the antennas E-plane pattern without and with estimated mismatches error at three main beam directions. For this 4-element system, it is observed that for 2° error in phase mismatch estima-

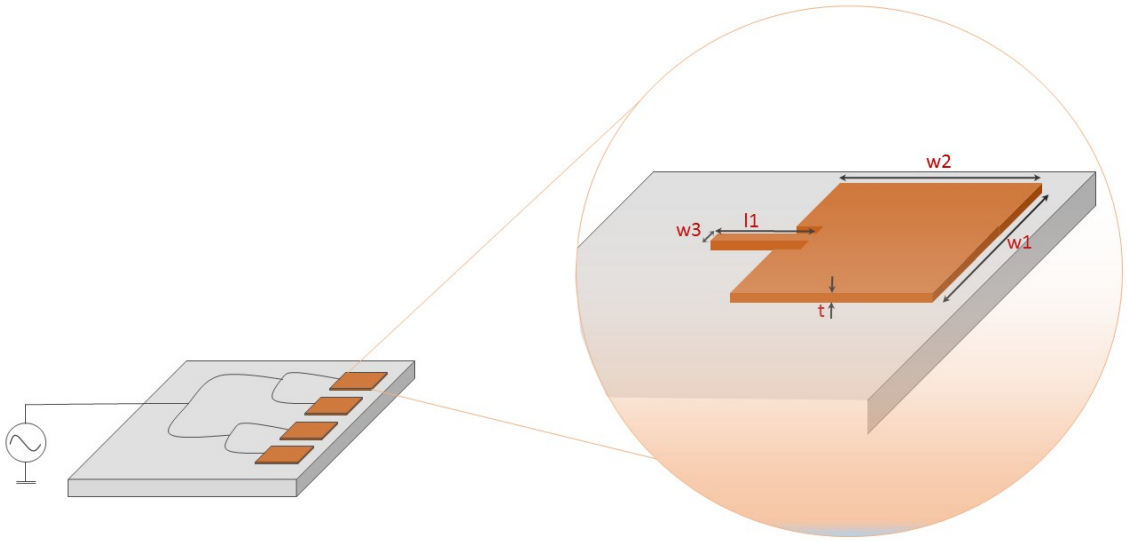
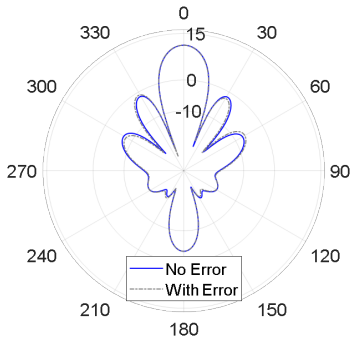


Figure 2.9: Patch antenna geometry under process variation

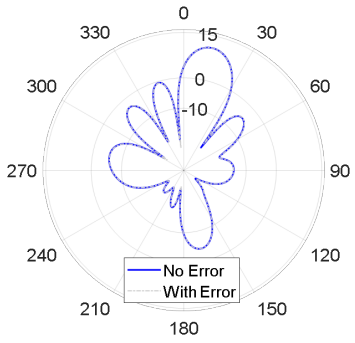
tion and maximum 2% error in gain mismatch estimation, the main beam direction misplacement is $\Delta\theta_s < 0.1^\circ$. Its difference on array gain is $|\Delta G| < 0.1dB$ which is very insignificant in practice.

2.6 Conclusion

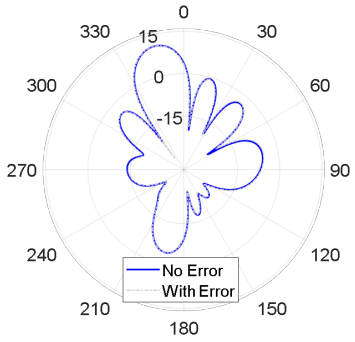
Integration of the entire transmitter system, including the phased array and antennas on the same die is the only viable solution to meet the stringent requirements of future wireless systems. Examples of phased array/antenna integration have already been demonstrated for radar systems. These integrated systems pose a significant test challenge as the RF phased arrays which need to be calibrated for effective beam forming. This calibration requires detailed characterization of the phased array ele-



(a)



(b)



(c)

Figure 2.10: Array pattern with and without estimation errors (a) $\Delta\phi = 0°$ (b) $\Delta\phi = 60°$ (c) $\Delta\phi = -60°$

Table 2.3: Gain and phase mismatches estimation error accounting for process variation, load board variation and noise power

$\Delta w_1, \Delta w_2, \Delta w_3, \Delta l_1 = 0.6\mu m$ $\Delta t = 0.5\mu m, D = 1\mu m$,Noise Floor=-84dBm				
$\Delta\phi = 0°$	ΔG_1	1.5%	$\Delta\phi_1$	0.64°
	ΔG_2	0.87%	$\Delta\phi_2$	0.77°
	ΔG_3	1.42%	$\Delta\phi_3$	1.05°
	ΔG_4	1.34%	$\Delta\phi_1$	0.51°
$\Delta\phi = 60°$	ΔG_1	0.97%	$\Delta\phi_1$	0.86°
	ΔG_2	1.43%	$\Delta\phi_2$	0.65°
	ΔG_3	2.0%	$\Delta\phi_3$	0.65°
	ΔG_4	2.1%	$\Delta\phi_3$	1.79°
$\Delta\phi = -60°$	ΔG_1	1.62%	$\Delta\phi_1$	1.01°
	ΔG_2	1.82%	$\Delta\phi_2$	0.33°
	ΔG_3	1.7%	$\Delta\phi_3$	1.53°
	ΔG_4	1.45%	$\Delta\phi_1$	1.05°

ments. While phased array testing and even built-in self-test has been demonstrated in the literature, there has been scant work on characterizing phased arrays when there is no physical connection to the antennas output. For a low-cost test solution, it is desirable to place the test set-up in the near field in a fixed location. However, the measured result needs to be extrapolated to the far field. Mismatches in the phased array and the antennas make this extrapolation even more difficult. In this chapter, we presented a method for modeling the near-field radiation of phased array

antennas. This model is then used to extract the gain and phase mismatches with the aim of calibrating them at the transmitter. We conclude that with the proposed test method, the total gain mismatches can be estimated with less than 2% error and total phase mismatches can be measured with less than 2° error at 20dB above the ambient noise level. We also conclude that based on analysis of phased array antennas, this accuracy is more than adequate to calibrate todays and future phased array systems in the commercial domain. The proposed method is further explored in a coplanar environment to investigate the effect of the process variation on the accuracy of mismatch estimation.It shows that the accuracy is beyond adequate for up to 32-element systems. Current silicon based high frequency phased array applications include up to 32 elements [46-49].

CHAPTER 3

3 A BUILT-IN SELF-TEST TECHNIQUE FOR TRANSMITTER-ONLY SYSTEMS

3.1 Cartesian Transmitter Overview

In a Cartesian transmitter the I(t) and Q(t) data are generated in the baseband. The carrier signal is modulated with this information to be transmitted through the power amplifier and antenna.The RF modulated signal is expressed in Eqn.(3-1).

$$V_{RF}(t) = I(t)cos(\omega t)Q(t)sin(\omega t) \qquad (3-1)$$

The transmitter must send RF modulated signal which satisfies spectral mask and Error Vector Magnitude (EVM) requires by a specific target standard while the receiver needs to recover in-phase and quadrature components from the RF input signal. Impairments due to the non-linearities as well as process variations cause distortion in the transmitted and received signals.

3.2 Proposed Methodology

We propose a BIST method with simple circuitry that uses a single test setup to characterize the I/Q gain and phase mismatch as well as the DC offsets of transmitter-only systems. The transmitter can be characterized after production or periodically in the field.

Figure 3.1 shows the overview of the BIST system block diagram. The transmitter output is sensed via a directional coupler. The majority of the signal power is conducted to the antenna and a trivial amount is fed to the self-mixing circuit to

Table 3.1: List of Unknowns

$\Delta\phi$	Phase mismatch
g	Gain mismatch
I_{DC}	In-phase DC offset
Q_{DC}	Quadrature-phase DC offset
G_p	Path gain
V_{DC}	DC offset at BIST output

generate a DC signal at the BIST output. The generated baseband signal (BIST DC output), which is proportional to the input RF stimulus, is then further processed to compute the transmitter imbalances.

3.2 Analytical Derivations

Having the baseband input set at DC values of I_{in} and Q_{in}, the BIST DC output is given as in Eqn.(3-2), where the unknown parameters include gain (g) and phase ($\Delta\phi$) mismatches, DC offsets (I_{DC}, Q_{DC}, V_{DC}) and BIST path gain (G_p). Four of these are target parameters while the other two (V_{DC} and G_p) are part of the equations and are needed to be known. They are tabulated in Table 3.1.

$$V_{O_{DC}} = V_{DC} + G_p \times \sqrt{((I_{in} + I_{DC}) + (1+g)Qsin(\Delta\phi))^2 + (1+g)^2(Q_{in} + Q_{DC})^2(cos\Delta\phi)^2)} \tag{3-2}$$

To determine all six unknown parameters, we need six linearly independent equations. The transmitter baseband inputs ($I_{in} and Q_{in}$) are the only test parameters we can set. The required linearly independent equations are constructed based on varying the input baseband levels by a known offset, Δ. Since the baseband inputs are set digitally, adding a pre-determined offset to the inputs I_{in} and Q_{in} will also generate

an equivalent offset in the effective baseband inputs $(I_{in} + I_{DC}, Q_{in} + Q_{DC})$ without knowing the I_{DC} and Q_{DC} values. Since equation (1) has a quadratic dependency on the baseband inputs, adding offset to both or either input will generate linearly independent equations. To obtain the six equations, the baseband inputs are set as follows for each measurement:

$$(I_{in}, Q_{in}) \rightarrow M1, (I_{in} + \Delta, Q_{in}) \rightarrow M2$$

$$(I_{in}, Q_{in} + \Delta) \rightarrow M3, (I_{in}, Q_{in} + 2\Delta) \rightarrow M4$$

$$(I_{in} + \Delta, Q_{in} + \Delta) \rightarrow M5, (I_{in} + 2\Delta, Q_{in} + 2\Delta) \rightarrow M6$$

Where M_i indicates the DC measurement for the i^{th} step. Note that the BIST circuit DC offset is independent of the input and the path gain, Gp, is a scalar that multiplies all signals in identical fashion. In order to remove the unknown BIST DC offset, we only process difference between two measurements. Equations (3-3) to (3-7) show the intermediate variables, E_1 through E_5, where the BIST DC offset is automatically removed.

$$E_1 = (M_2 - M_1)^2 \qquad (3-3)$$

$$E_2 = (M_4 - M_1 - 2(M_3 - M_1))^2 \qquad (3-4)$$

$$E_3 = (4(M_3 - M_1) - (M_4 - M_1))^2 \qquad (3-5)$$

$$E_4 = (M_6 - M_4 - 2(M_2 - M_1))^2 \qquad (3-6)$$

$$E_5 = (M_5 - M_2 - (M_3 - M_1))^2 \qquad (3-7)$$

Furthermore, to remove the unknown path gain, G_p, we only process the ratios of the intermediate variables. By solving Equations above, we can analytically determine the target parameters.The solution for the target parameters is independent of the

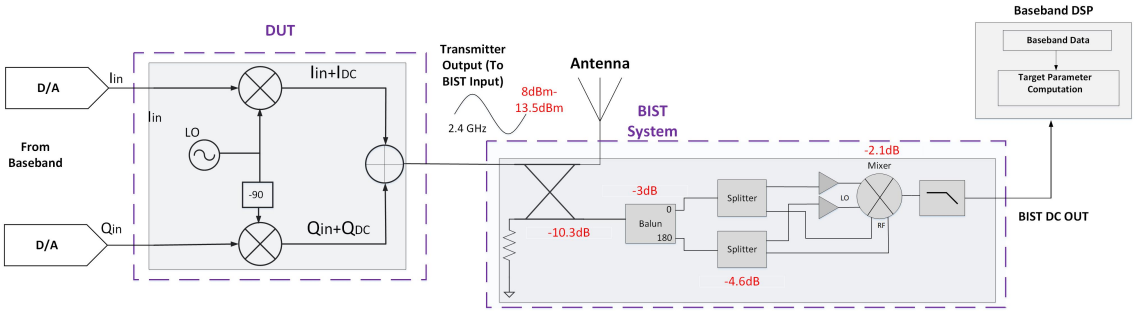


Figure 3.1: Simplified transmitter and BIST diagram

circuit architecture since it can be used for any Cartesian transmitter. Equations (3-8) to (3-11) describe each target parameter with respect to relative measurements.

$$g = \sqrt{(E_2/((E_4 - 4E_5)))} - 1 \qquad (3-8)$$

$$\Delta\phi = sin^{-1}(E_5/E_2(1+g)) \qquad (3-9)$$

$$I_{DC} = \Delta\frac{(E_3/E_2 - 2E_1/E_5 + E_4/E_5 - 4)}{(2E_5/E_2 - 2E_4/E_5 + 8)} - I_{in} \qquad (3-10)$$

$$Q_{DC} = \frac{\Delta}{E_5}(E_1 - \frac{(E_4 - 4E_5)I_{in}}{\Delta} - \frac{E_4}{2} + 2E_5) - Q_{in} \qquad (3-11)$$

3.3 BIST Circuit Design

The analytical derivation assumes that the BIST circuit works linearly and there are no additional unknowns due to the BIST circuit. The design of the BIST circuit is challenging due to these constraints. The presented BIST circuit (shown in Figure 3.1) is implemented in 0.13m CMOS technology. The supply voltage is 1.2V. Results are obtained at 2.4GHz although the method is extendable to any frequency. Since the input amplitude varies in a relatively wide range during test phase due to Δ step variations, the challenges in designing this BIST circuit are keeping the entire system in its linear region and keeping the voltage offset, gain, and phase offset of the BIST circuit independent of its input amplitude.

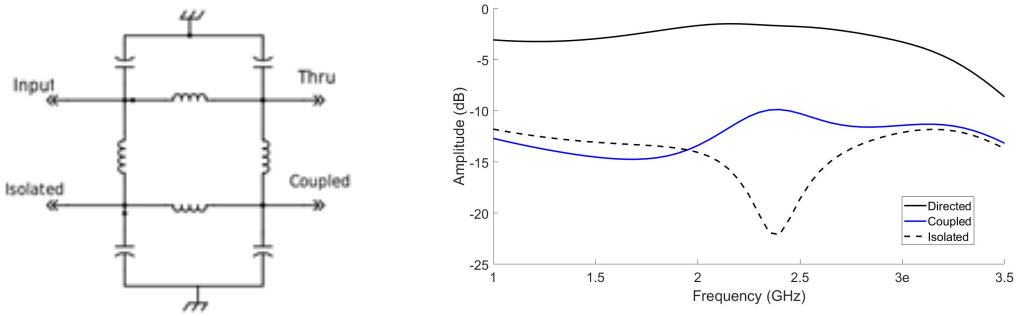
The circuit building blocks details are discussed in the following sections.

3.3.1 Unequally Split Directional Coupler

The directional coupler has asymmetric coupling factor between the primary path and the BIST path for two purposes. First, in the primary path, it imposes a small insertion loss with minimum impact on the transmitter nominal operation and provides in-field testing possibility. Second, in the coupling path, it attenuates the strong transmit signal to prevent saturating the BIST circuit. The narrowband unequal-split coupler is designed using lumped components [53]. The circuit realization and the S-parameters are shown in Figure 3.2. The coupler imposes a 1.2dB insertion loss with a coupling gain of -10.3dB. The insertion loss of the coupler is mainly due to inductors finite Q-factor.

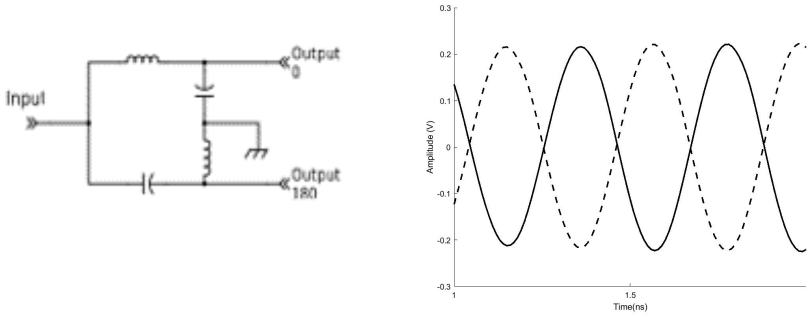
3.3.2 Balun

Since we do not need to provide gain in the BIST path, a passive structure can be used for balun to ensure the linearity of the BIST system over a wide range of input levels. The outputs of the balun are 180° out of phase, as shown in Figure 3.3, which also shows the circuit implementation. Any mismatch between the balun output appears as a DC offset at the BIST output and would not affect the accuracy of our method.



(a) (b)

Figure 3.2: (a) Unequal-split coupler circuit (b) Coupler simulation results



(a) (b)

Figure 3.3: (a) Passive balun circuit (b) Balun simulation results

3.3.3 Splitter and Rail to Rail Amplifier

A source follower topology is used for the splitter to branch out each of baluns output signals. It is then followed by amplifiers in the LO path to provide rail to rail signals at switching transistors. These amplifiers are required to make the mixer gain independent of the input signal power. Figure 3.4(a) shows the circuit topology for the rail to rail amplifier. The rail to rail amplifier block uses a common source amplifier followed by an inverter chain. A known aspect of the inverter chain is varying

output rise/fall time with respect to the input amplitude due to change in the slew rate. This causes a delay between inverter chains output signals, which reflects as a phase offset in the signals. If this phase offset depends on the input amplitude, it will not be canceled by relative measurements. Hence, keeping the phase offset constant while the input amplitudes vary is essential. Thus, the common source amplifier is employed to amplify smaller amplitude inputs closer to supply margins such that the delay difference between outputs at different input levels reduces to minimum. The output of the amplifier and the change in the phase shift due to varying input voltages for minimum and maximum input limits are depicted in Figure 3.4(b) and Figure 3.4(c) respectively. It is observed that the maximum phase change for the test input range is within $0.6_{\circ|}$ which is one of the major error source for the proposed method.

3.3.4 Mixer

A conventional Gilbert cell mixer is designed to perform the self-mixing task. A resistive degeneration is employed to increase the linearity of the mixer. Since gain is not a concern for BIST, we sacrificed gain for more linearity. The mixer circuit realization is shown in Figure 3.5(a). Linearity of the mixer is evaluated by calculating the third order intercept point (IIP3) as illustrated in Figure(3-5b). The IIP3 of the mixer is equal to 12dBm which guarantees a linear operation for the given test input range, which is depicted with the red arrow in Figure 3.5(b).

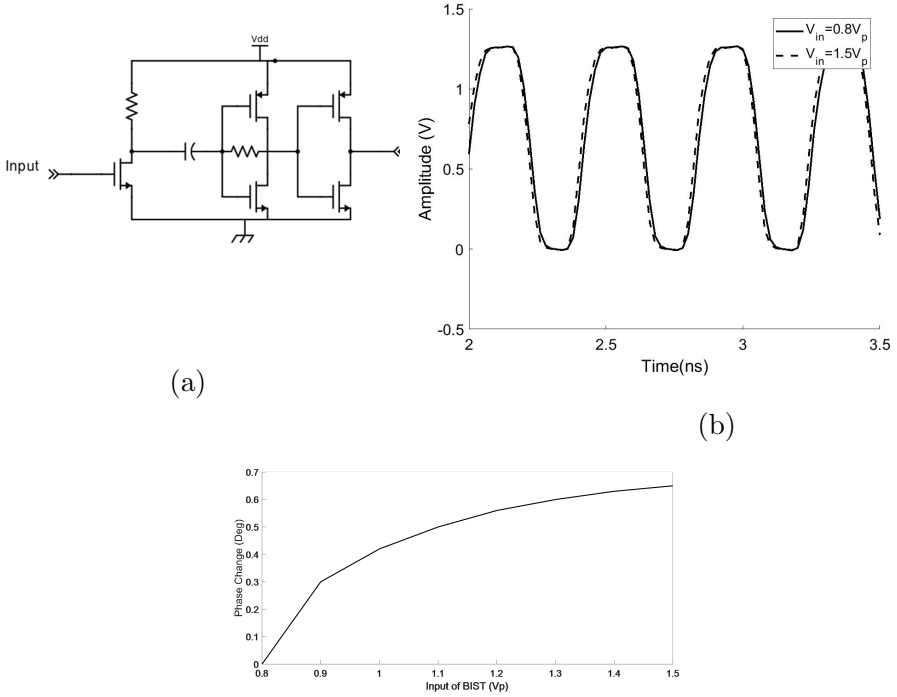


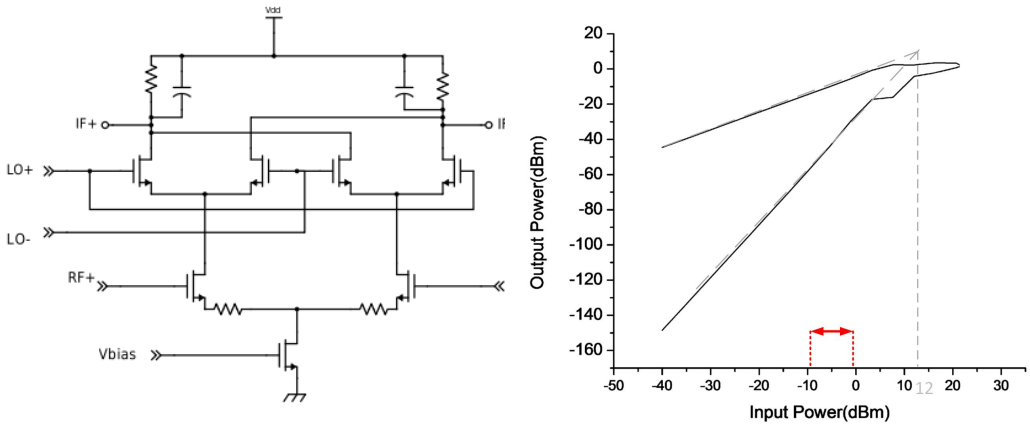
Figure 3.4: (a) Rail to rail amplifier circuit (b) Switching signal (c) Phase difference due to varying input

3.3.5 Low-Pass Filter

A passive off-chip filter is placed at the chain end to filter out the small high frequency components of the output signal.

3.3.6 Link Budget

The proposed technique is only valid within the linear operation of the BIST hence it is very important to assure a wide dynamic range for the BIST circuit while testing. The BIST input (transmitter output) range is required to place between 8dBm and 13dBm to cover the necessary span for maximum $\Delta = 0.4V$. The gains and losses of



(a) (b)

Figure 3.5: (a) Gilbert cell mixer circuit (b) IIP3 plot

the BIST building blocks are designed such that the entire chain works in the linear region. The corresponding gains of each block are shown in Figure 3.1. The signal at RF port of the mixer must be below the IIP3 and P1dB (IIP3-9.8dB) of the mixer. The RF signal span is highlighted in the graph which shows it is well below IIP3.

3.4 Experimental Results

In order to evaluate the proposed BIST technique, we use three experimental setups: (a) Matlab model based experimental evaluation for a large range of impairment and environmental conditions, (b) Hardware demonstration using off-the-shelf components, and (c) post-layout circuit simulations.

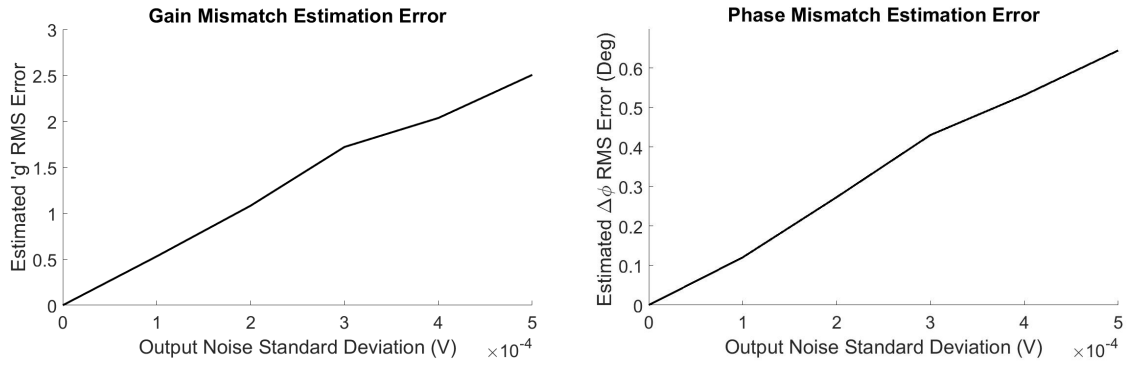
3.4.1 Matlab Model Simulation

The system model and proposed BIST technique are implemented in MATLAB and accuracy analysis is conducted.by simulations. First, we investigate the effect of output noise on estimation accuracy. The output measurement noise is varied and the phase and gain mismatch estimation RMS error is calculated accordingly. Fig.6 shows the characterization error in gain and phase mismatch with increasing environmental noise. The baseband step variation is set to $\Delta = 0.4V$. The injected gain mismatch is 5% and the injected phase mismatch is 3°. These values are selected based on EVM limit for WiFi standard which is less than 5.6%. The EVM for injected gain and phase mismatch is obtained using (3-12).

$$EVM = \sqrt{(1 - cos(\Delta\phi) + g^2/4)} = 4.5\% \qquad (3-12)$$

Normally, the frame to frame EVM variation is 1%-2% [54]. Figure 3.6 shows for 0.5 mV measurement error, the gain mismatch estimation error is g=2.5% and the phase mismatch estimation error is $\Delta\phi = 3°$ which results in EVM=1.4%. Thus we strive to attain this estimation accuracy for which the EVM is within the measurement uncertainty of EVM [54].

Next, we investigate the effect of Δ on the accuracy of the proposed technique. The gain mismatch is set to %5, the phase mismatch is set to 3° and the measurement error standard deviation is set to 0.5mV. As we increase the value in our measurements, the accuracy of the proposed technique increases. Figure 3.7 shows the accuracy of the BIST technique with varying input offset (Δ) value. The Δ level however, cannot be raised to any arbitrary value. The limiting factor here is keeping the transmitter and the BIST circuits in their linear operating region and to avoid saturation of the transmitter/BIST path.



(a) (b)

Figure 3.6: Effect of measurement noise on (a) Gain mismatch estimation error (b) Phase mismatch estimation error

3.4.2 Hardware Demonstration Using Discrete Components

The BIST method is also verified using lab equipment and off-the-shelf components as shown in Figure 3.8. The measurement setup includes, a signal generator to produce I and Q signals at 1GHz, a discrete combiner ZF-2-4+ to add the two signals and a discrete mixer, ZFM-150+, to down convert two signals to DC. The resulting signal is then down converted to DC using discrete mixer ZFM-150+. The value is set to 0.4V. The measurement data is tabulated in Table 3.2. It is observed that the gain mismatch estimation error is less than 1.7% and phase mismatch estimation error is 0.2°. This estimation error is within the discussed error limits.

3.4.3 Post-Layout Simulation

Chip layout of the proposed BIST circuit is shown in Figure 3.9. The total area overhead is $0.247mm^2$ which is less than 4.2% of a Cartesian transmitter manufactured in the same process and in the same frequency band [55]. Figure 3.10 shows the BIST output for varying input amplitude levels. The DC offset is taken out from the output. The BIST circuit behavior is adequately linear within the test signal range. The BIST circuit adds no significant additional error to the I/Q imbalance computation. To prove the concept, the transmitter is emulated in Matlab and transmitter output voltages for M1-M6 is applied to the BIST circuit. The target parameters then are retrieved and compared with actual values. Table 3.3 shows the results. The total power consumption of the BIST is equal to 12.1mW. Compare to the transmitter in[55] which consumes 133mW,our proposed BIST imposes extra 9% power dissipation on the entire system.

3.4.4 Chip Fabrication

The chip is sent out to MOSIS wafer lab for fabrication in IBM 8Rf 130nm technology. Die thickness is 10.0 Mils. The measurement results will be reported in future publications.

3.5 Test Time

The proposed technique requires six DC measurements over six baseband input frames and simple mathematical calculations. Each frame is below 20s which is sufficient time for the filter settling and sampling. Including computation time, the overall test time

Table 3.2: Estimated target parameters v.s actual using hardware measurement

Parameter	Actual	Estimated
$\Delta\phi$	16°	15.8°
$1+g$	1.001	0.984
I_{DC}	968mV	958mV
Q_{DC}	881mV	896mV
G_p	0.688	0.692

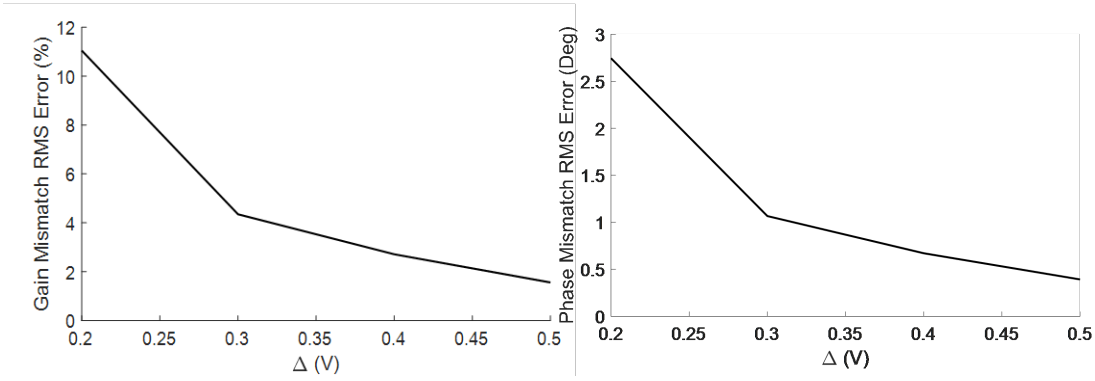
is estimated to be less than 0.5ms.

3.6 Conclusion

In this chapter, we propose a fast and process-robust BIST technique to characterize Cartesian transmitters. The mathematical model is simulated in Matlab for accuracy analysis of the method. Hardware measurements are performed to validate the BIST methodology. The measurements show that the gain mismatch estimation error is less than 1.7% and phase mismatch estimation error is 0.2°. The BIST circuit is designed in 0.13um process. The circuit implementation of each block is presented. The post extraction results show that the design works in the linear region for the desired test input span and the BIST circuit poses only a slight degradation in the accuracy compared with MATLAB simulations.

Table 3.3: Estimated target parameters v.s actual using post-layout simulation

Parameter	Actual	Estimated
$\Delta\phi$	3°	3.45°
$1+g$	0.95	0.931
I_{DC}	1.1V	1.088V
Q_{DC}	1.1V	1.118V
G_p	0.091	0.0911



(a) (b)

Figure 3.7: (a) Gain mismatch estimation error (b) Phase mismatch estimation error vs. Δ variation

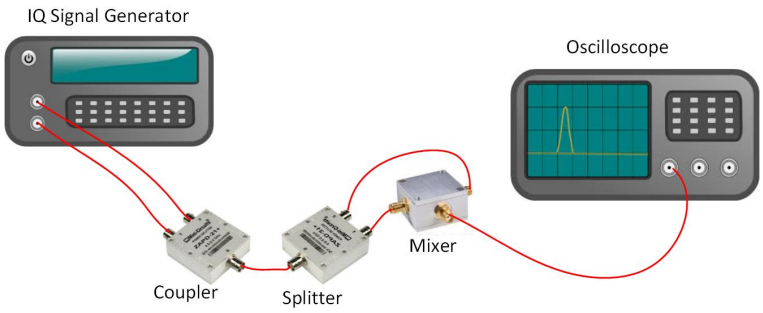


Figure 3.8: Measurement setup using off-the-shelf components

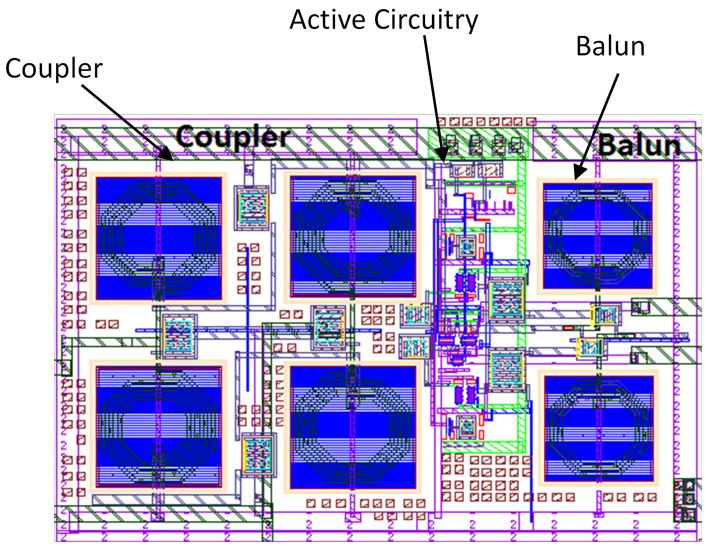


Figure 3.9: Layout of the proposed BIST

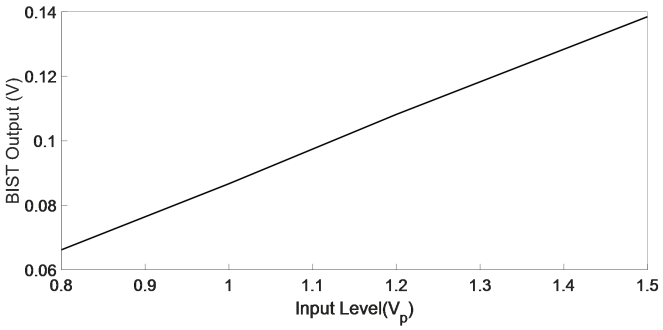


Figure 3.10: Post-layout BIST circuit simulation

CHAPTER 4

4 IN-FIELD PROGRAMMABLE ADAPTIVE CMOS LNA FOR INTELLIGENT IOT SENSOR NODE APPLICATIONS

4.1 Proposed Post-Production Optimization Technique

While designers strive for process robustness at nominal operating conditions, such as supply voltage, noise, temperature, same robustness is generally difficult to maintain over a large variation in operating conditions. By modifying these operating conditions during testing, we can increase sensitivity to process parameters.This process sensitization is expected to spread and shift the circuit performance distribution over process variation, as illustrated in Figure 4.1. Spreading the performance parameters is performed using different reconfiguration setups. Our proposed reconfiguration approach uses transistor sizing and bias control. It uses coarse tuning of performance parameters which is realized by only switches and is fully performed in digital. Hence it is low cost and low overhead. The performance distribution over process variation for each setup has overlap with others. This brings a level of uncertainty which necessitates the verification of the performance of the DUT at potential switching combinations.To decide on the optimum switch combination, instead of lengthy testing of the performance at each potential reconfiguration state, we have used a fast statistical-based prediction procedure using Joint Probability Distribution Function (JPDF) algorithm. Our approach predicts the performance parameters of all switch combinations of the DUT and based on the prediction result, selects the switch combination closest to the target. Therefore, unlike previous works, the selection of the switch combination, takes into account the DUT to DUT variations.

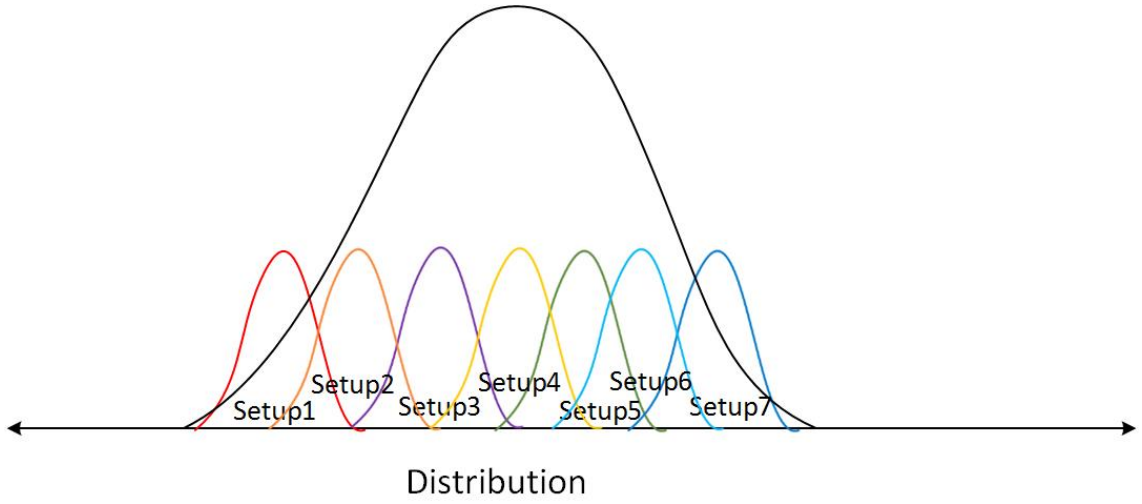


Figure 4.1: Sensitization over process variation using different calibration setups

4.1.1 Optimization Flow

Using simulations, we will construct local statistical models that relate circuit-level calibration parameters to circuit performances. We conduct Monte-Carlo simulations to obtain parameter profiles. These profiles will help in selecting and guiding the training process. It is important to select the inputs to the prediction algorithm that are highly correlated to the target and these correlations are altered by potential process and circuit modifications. As it is depicted in the flow chart of Figure 4.2(a), using JPDF algorithm, the performance parameters are predicted for each switch combination while input parameters are assumed to be known at one or more switching combinations (e.g. at combination where all switches are off).Set P at switch combination zero, i.e. all switches off, is input to the prediction model. The model predicts the set P for the rest of the switching combinations Eventually, for a specified target performance and based on predicted performance parameters, the optimized

operation is obtained by setting the correct digital code to the calibration network.

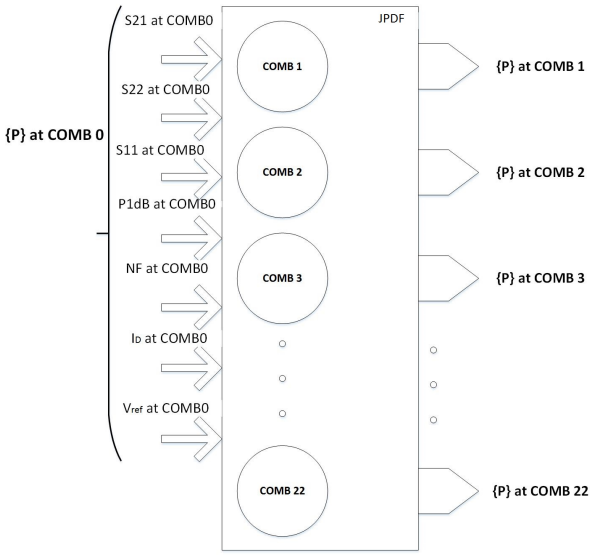
For better understanding of the optimization flow, a diagram is shown in Figure 4.2(b). The statistical model is formed during characterization phase.Decision is made by statistical mapping during online phase. This procedure can be one-time or iterative.Due to overlap between performance distribution of switching combinations, it might be required to redo the prediction with more than one input if it results in a closer to target combination selection. This means adding another measurement phase to the prediction procedure hence increasing reconfiguration time.

4.1.2 Optimization Hardware

Figure 4.3 shows the topology of the reconfigurable wide-band LNA. A current re-use technique is used to comply with the low voltage design. It provides high gain while driving high impedance of the second stage [56]. A DC feedback loop is used to define the operating points and keep ML1A and ML2 in saturation [57].L_i, L_s1 and L_s2 are tuned to obtain the optimum noise figure and input matching. The two-stage topology helps with the independent tuning of the performance parameters.

First stage primarily controls the noise figure while the second stage is mainly responsible for the linearity of the LNA. The gain control is conducted in three modes; High gain, medium gain and low gain, each obtainable with different combinations of noise figure and linearity. Hence, gain modes are available independent of the noise figure and linearity configurations.

The LNA is implemented in a 130 nm CMOS technology. The sizing of the transistors is listed in Table 4.1. The varactors are added to compensate for bond wire inductances.



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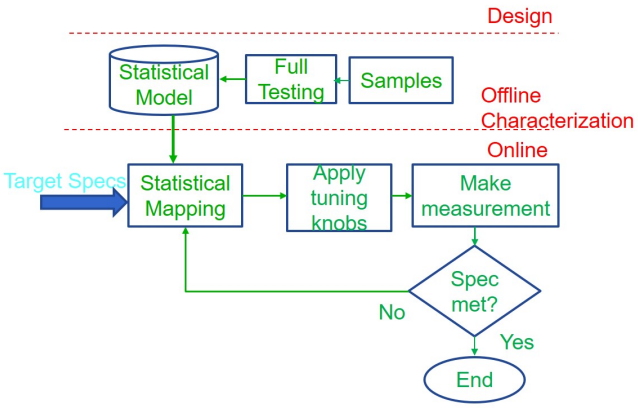


(b)

Figure 4.2: (a)JPDF prediction algorithm diagram (b) Proposed optimization flow

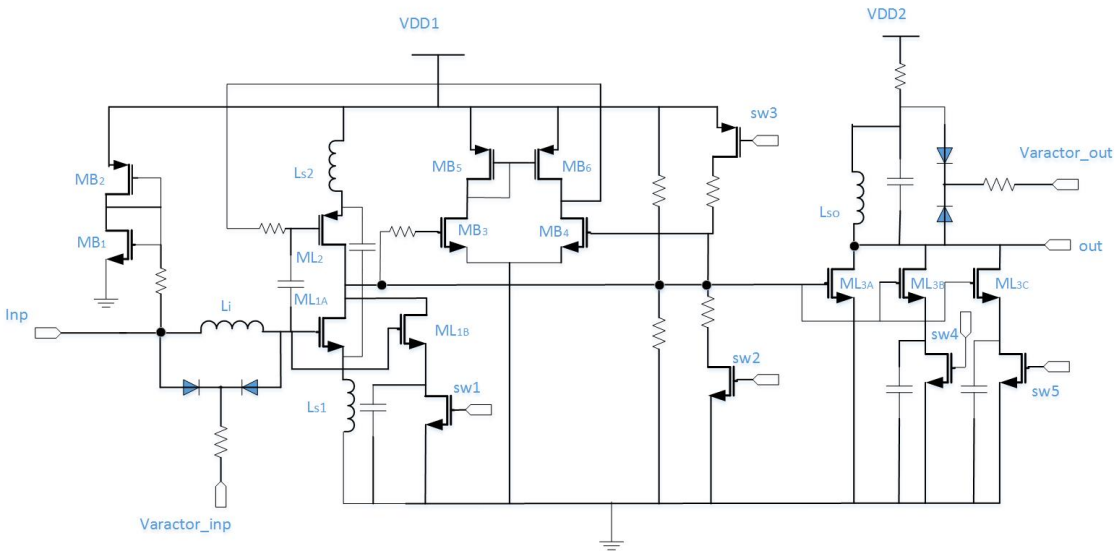


Figure 4.3: Reconfigurable LNA architecture

The tuning knobs include switches SW1 to SW5, VDD1 and VDD2 as it is shown in Figure 4.3. The tuning hooks are selected such that they cover the desired reconfiguration range. VDD1 and VDD2 are supply voltages which are provided by a low-drop-out regulator since these knobs are controlled digitally too. Five switches are embedded into the design to control the performance parameters. SW_1 connects gate of transistor ML_{1B} to ML_{1A} resulting in increase in gain and improving noise figure but aggregates input matching to some extent. SW_2 and SW_3 add a parallel resistance which consecutively changes the reference voltage of the differential amplifier which affects the DC bias voltages of ML_{1A}, ML_2 and ML_{3A}. SW_2 reduces the reference voltage hence reduces gain, linearity and power consumption.

Whereas, SW_2 increases the reference voltage hence increases linearity and power consumption but aggregates noise figure. SW_4 and SW_4 add transistors ML_{3B} and ML_{3C} in parallel with ML_{3A} to resulting in increased gain and power consumption. Twelve programmable combinations are chosen to optimize performance with respect

Table 4.1: Device sizing

Device	$w/l(\mu m)$	Device	$w/l(\mu m)$
ML_{1A}	80/0.12	SW_2/SW_3	2/0.12
ML_{1B}	70/0.12	$SW_1/SW_4/SW_5$	10/0.12
ML_2	100/0.12	M_{B1}	1/0.12
ML_{3A}	30/0.12	M_{B2}	2.5/0.12
ML_{3B}	30/0.12	M_{B3}/M_{B4}	3/0.12
ML_{3C}	70/0.12	M_{B5}/M_{B6}	8/0.12

to requirements. For instance, if higher linearity is required, SW_3 is turned on however in order to reduce the noise figure SW_1 is switched on too. The desired performance can be achieved by setting the correct digital codes to the reconfiguration network.

4.2 Simulation Results

4.2.1 Circuit Characterization

The LNA is characterized by running a 200-sample Monte-Carlo run at combination zero where all switches are off. Figure 4.4 depicts the distribution of each performance parameter over process variation.

The proposed reconfiguration scheme is used to sensitize the LNA circuit to the process variation. Hence, a Monte-Carlo simulation is performed to characterize the performance parameters range for each switching combination.

The performance corners are achieved by running Monte-Carlo simulation for 200 samples for all the switching combinations over process variation. Figure 4.5 shows

Table 4.2: Tuning range for adaptable LNA

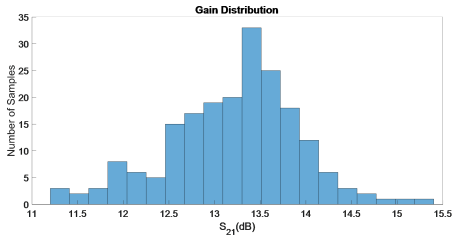
Performance Parameters	NF	P1dB	Gain	Power Diss.
Tuning Range	≈1.5 dB	≈10 dB	≈12 dB	≈18 mW

the histogram for each performance parameter of the programmable LNA. It reveals the sensitization effect on widening the circuit performance parameters span over process variation. Table 4.2 shows the tuning range for targeted performance parameters obtained from histogram plots. The reconfiguration feature provides a wide tuning range for gain, obtainable at a broad linearity span, makes it suitable for adaptation to localized application-specific requirements. Yet, noise figure variations is kept small providing the low noise figure requirement for the LNA.

4.2.2 Validation in Matlab

Twelve switching combination are used for the adaptation purpose.
As an example, different scenarios are investigated to show the adaptation of our design to the specific requirements. Figure 4.6 shows different four scenarios where each has a particular performance parameter needs. Four different switching combination provides a close match for each situation. Table 4.3 lists the possible switch combinations which are the fits for each case.

As discussed earlier, the JPDF learning algorithm is used in our proposed method to predict the performance parameters of the device. The RMS prediction error is calculated and plotted in Figure 4.7 for gain, noise figure and P_{1dB}.



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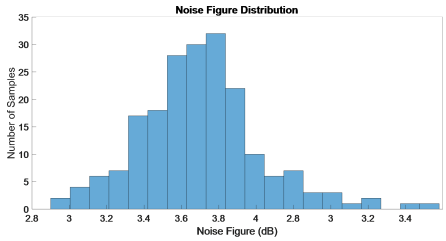

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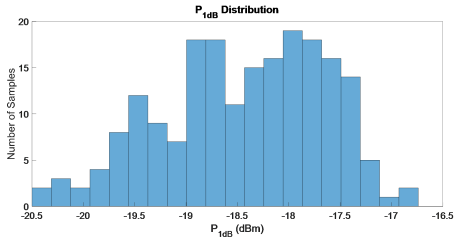

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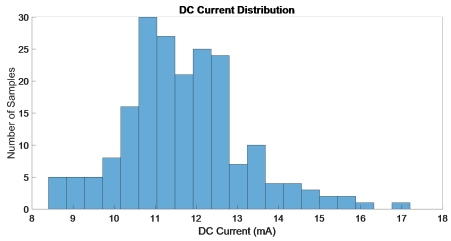
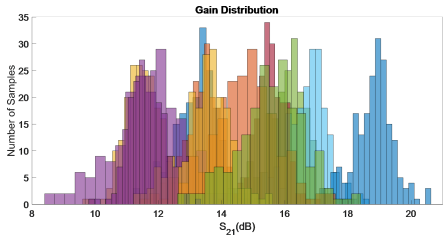


(d)

Figure 4.4: Distribution of (a) Gain (b) Noise figure (c) P_{1dB} d) DC current over process variation for non-adaptable LNA



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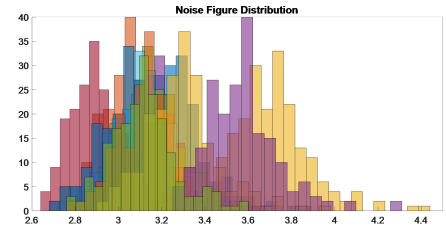

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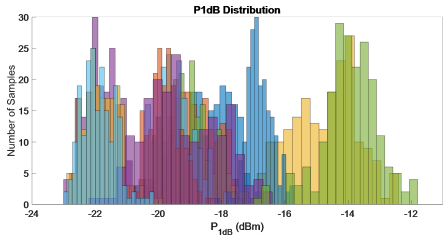

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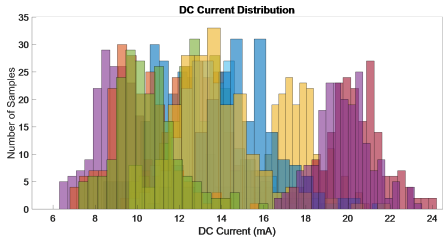

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Figure 4.5: Distribution of a) Gain b) Noise figure c) P_{1dB} d) DC current over process variation for adaptable LNA

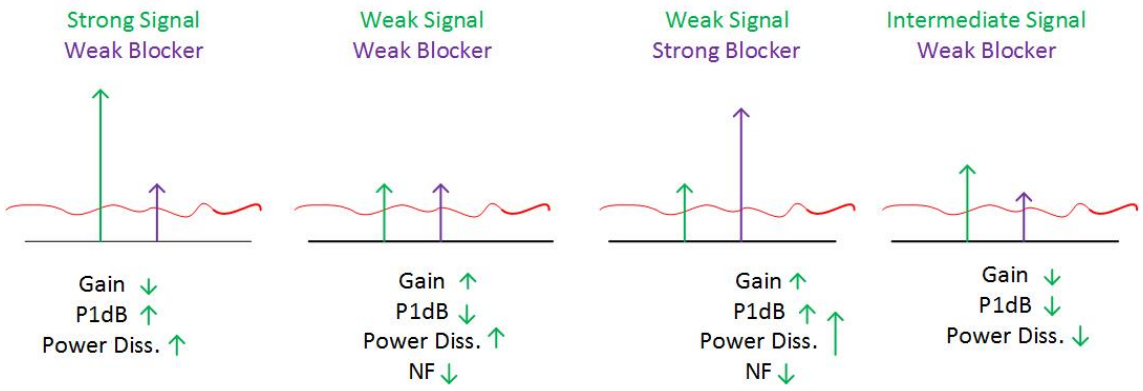


Figure 4.6: Sensitization over process variation using different calibration setups

Table 4.3: Four switch combinations for four different scenarios

Switch Combo	Gain(dB)	$S_{11}(dB)$	$S_{22}(dB)$	$NF(dB)$	$P_{1dB}(dB)$	$I_{DC}(mA)$
SW_3	11.5	-10.0	-27.8	3.9	-14.5	17.4
$SW_4 - SW_5$	19	-11.4	-25.6	3.2	-20.0	15
$SW_1 - SW_3 - SW_4$	16.5	-9.9	-30.7	3.0	-16.5	20.3
$1.05 * VDD1 - SW_2$	13.5	-14.4	-26.5	3.5	-19.2	13.5

4.2.3 Adaptation Flow

To illustrate the optimization and adaptation procedure, we review an example. We assume a target performance: gain 15dB-16dB, $P_{1dB} > -20dBm$, $NF < 3.7dB$. Using statistical mapping we know that three switching combinations satisfy the target requirements simultaneously as illustrated in Figure 4.8. Instead of testing all three switch combinations, to save time, we apply the prediction algorithm. In this example, performance at combination 4 is characterized for a part and is fed to the algorithm as the known input to predict performance parameters at combination 5 and combination 6. Therefore, the test time is reduced to one-third of the conventional

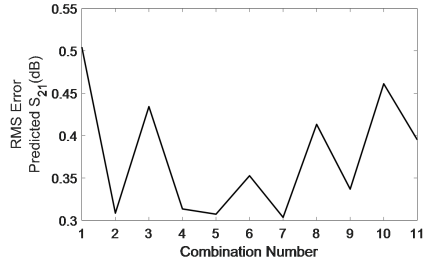
iterative approach where all potential switch combinations are being tested.However, there is a trade-off between the adaptation time and the adaptation error. As shown in Table 4.4,the target gain is not met. Alternatively, we may double the test time and characterize the DUT at two switching combinations and predict the third combination only. In this case, we assumed that the DUT performance at combination 4 and combination 5 are tested and are known; These are applied as the inputs to the prediction algorithm to predict the parameters at combination 6. After running our optimization algorithm, a switch combination which fits the desired performance is selected. The results for both cases are tabulated in Table 4.4. In this table measurement error is neglected. In case 1, the predicted gain for combination 6 is above the desired target range, hence it is removed from the choices. However in case 2, the prediction error is reduced and lies within the desired range hence combination 6 will be selected.

In case two switch combinations satisfy the desired performance, the one with lower power consumption can be selected.

4.3 Chip Implementation

4.3.1 Layout

The proposed adaptable LNA is designed in 130nm technology. Overall, the LNA occupies $0.16mm^2$ area. The complete reconfiguration network, including the additional tuning modes occupies less than $0.0002mm^2$ area. Thus, the entire reconfiguration network imposes no more than 0.1% area overhead. Figure 4.9 depicts the layout and the microphotograph of the fabricated adaptable LNA including the pad ring.



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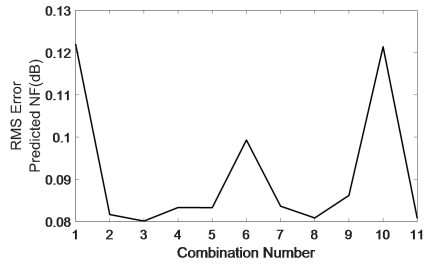

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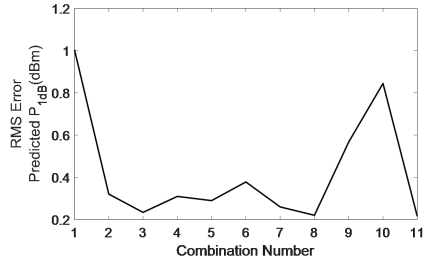

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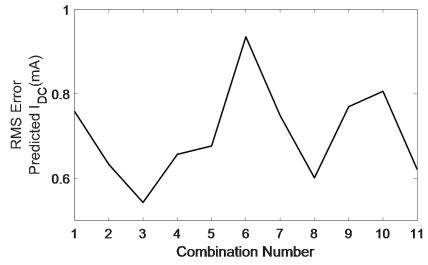
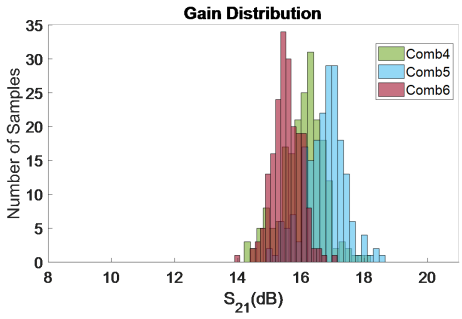


(d)

Figure 4.7: Predicted gain RMS error (b) Predicted P1dB RMS error (c) Predicted noise figure RMS error (d) Predicted DC current RMS error



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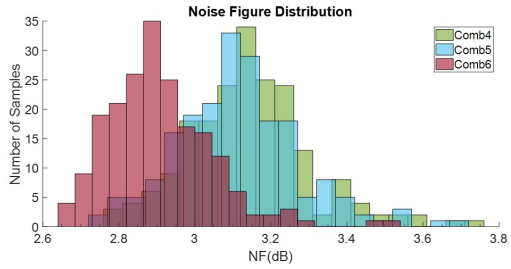

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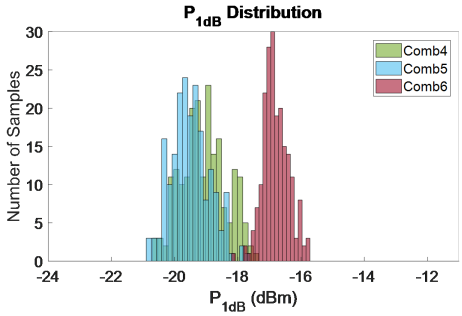

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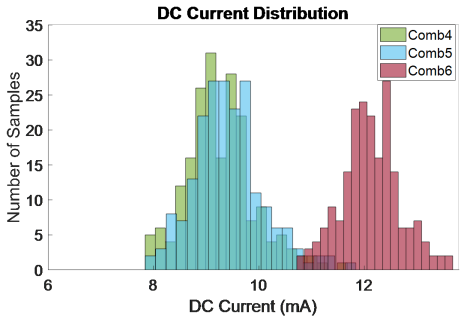
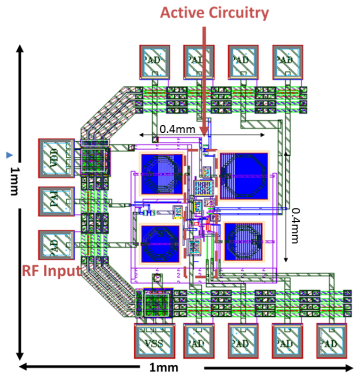


(d)

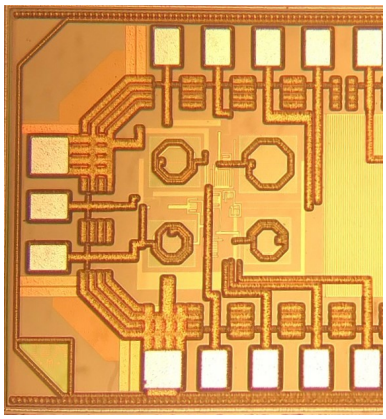
Figure 4.8: Performance parameters of three switching combinations over process variation (a) Gain (b) Noise figure (c)P1dB (d) DC current

Table 4.4: Optimization result for specified target parameters

$S_{21} = 15dB - 16dB, P_{1dB} > -20dBm, NF < 3.7dB$		Combination 4				Combination 5				Combination 6			
		$S_{21}(dB)$	NF (dB)	$P_{1dB}(dBm)$	I_{DC} (mA)	S_{21}(dB)	NF (dB)	$P_{1dB}(dBm)$	$I_{DC}(mA)$	$S_{21}(dB)$	NF (dB)	P_{1dB} (dBm)	$I_{DC}(mA)$
Case I	Measured	16.3	3.65	-18.45	15.0	-	-	-	-	-	-	-	-
	Predicted	-	-	-	-	17.0	3.4	-19.9	13.7	16.1	3.1	-17.3	20.9
	Error	-	-	-	-	0.1	0	0.2	0.6	0.2	0.1	0.5	0.1
Case II	Measured	16.3	3.65	-18.45	15.0	17.1	3.4	-19.7	14.3	-	-	-	-
	Predicted	-	-	-	-	-	-	-	-	16.0	3.1	17.3	21.0
	Error	-	-	-	-	-	-	-	-	0.1	0.1	0.5	0
Actual		16.3	3.65	-18.45	15.0	17.1	3.4	-19.7	14.3	15.9	3.0	-16.8	21.0



(a)



(b)

Figure 4.9: (a) Proposed LNA chip layout in 0.13um process (b) The fabricated chip microphotograph

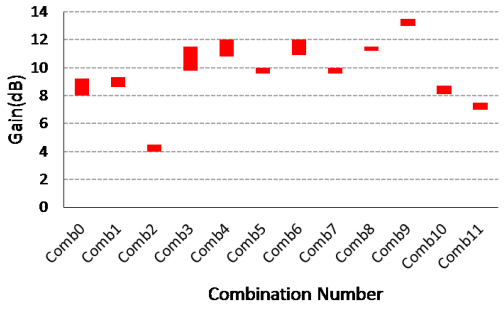
4.3.2 Chip Measurement Results

The fabricated chip is measured in the lab. A network analyzer is used to measure the S-parameters. A spectrum analyzer is used to measure P1dB of the device. To measure the noise figure, the Y-factor method is applied using a noise source and the spectrum analyzer. Four LNA chips are returned from the foundry and are measured to account for the process variation. Figure 4.10 shows the variations in performance parameters for each switching combination. It is observed that there is consistency

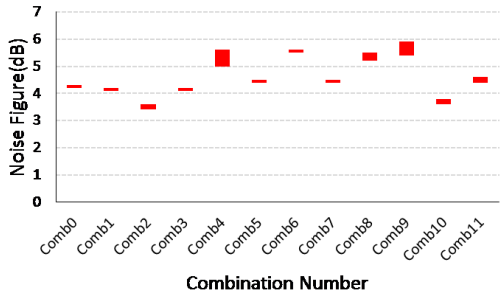
among the boards. The available gain range is 10dB, P1dB range is 11dB and noise figure range is 2.6dB. Due to low sample size, prediction cannot be demonstrated in hardware on fabricated samples. 200 random samples generated by imposing random variations on each of the four samples. JPDF trained with resamples of 3 out of 4 chips and RMS prediction errors estimated for different switch combinations are obtained as shown in Figure 4.11 for the 4th chip. It is observed that the maximum gain prediction error is 0.3dB, maximum noise figure prediction error is 0.16dB, maximum P_{1dB} prediction error is 0.8dB and maximum current prediction error in 0.76mA; All below 10% of the tuning range. The variation of performance parameters among the boards can be justified according to the Monte-Carlo simulation results in Figure 4.4.

4.4 Conclusion

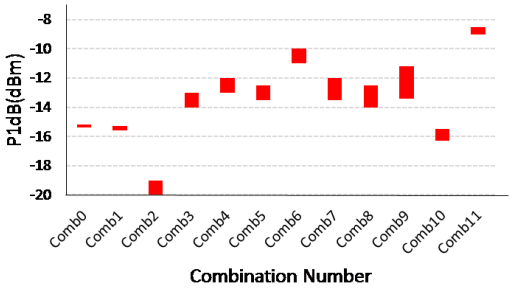
In this chapter, we proposed an automated adaptable sensor node for IOT applications. The machine learning technique is used for automatic adaptation. We demonstrated the proposed reconfigurability concept by implementing it on a CMOS LNA with built-in tuning knobs. The performance range over process variation is obtained. Using the statistical model formed by learning algorithm over Monte-Carlo samples, the performance parameters are predicted and a switch combination selection algorithm presented. A case study of the in-field adaptation shows the effect of prediction error on the switching combination selection. By characterizing more combinations in the field and hence sacrificing the test time, a closer-to-target combination can be selected. The prediction algorithm applied to chip measurement results and the prediction error obtained.



(a)

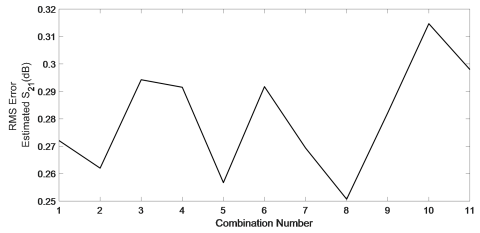


(b)

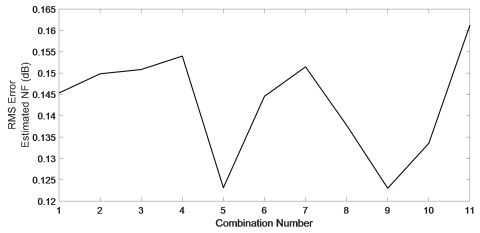


(c)

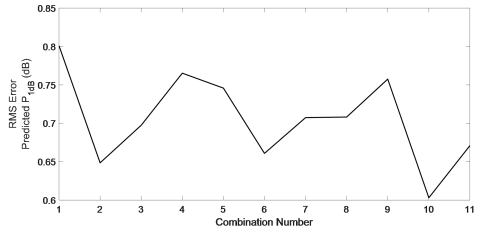
Figure 4.10: Performance parameters variation over four identical chips (a) gain (b) noise figure (c) P1dB



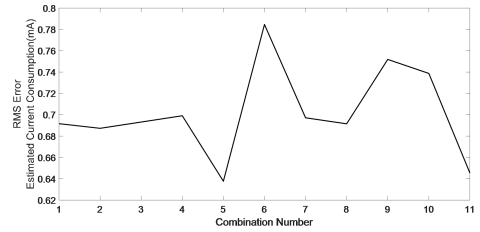
(a)



(b)



(c)



(d)

Figure 4.11: Predicted gain RMS error (b) Predicted noise figure RMS error (c) Predicted P1dB RMS Error (d) Predicted current RMS error

CHAPTER 5

5 SUMMARY AND CONCLUSION

In this dissertation, DFT solutions for automated test and calibration of advanced RF transceivers are proposed and discussed in order to achieve low cost and low overhead with high accuracy.

In chapter 2, we proposed an accurate cost-efficient post-production test solution for integrated phased array antenna mismatches. For a low-cost test solution, it is desirable to place the test set-up in the near field in a fixed location. we presented a method for modeling the near-field radiation of phased array antennas. This model is then used to extract the gain and phase mismatches with the aim of calibrating them at the transmitting site. We established a maximum tolerable estimation error based on reported acceptable array mismatches in prior works for 16-element and 32-element arrays. We conclude that with the proposed test method, the total gain mismatches can be estimated within 2% error and total phase mismatches can be measured with less than 2° error at 20dB above the ambient noise level.We also conclude that based on analysis of phased array antennas, this accuracy is more than adequate to calibrate todays and future phased array systems in the commercial domain. The proposed method is further explored in a coplanar environment to investigate the effect of the process variation on the accuracy of mismatch estimation. It shows that the accuracy is beyond adequate for up to 32-element system.

In chapter 3, we presented a fast, low-cost and process-robust BIST technique for IQ transmitter-only systems. The BIST mathematical method is established and it is verified using hardware measurements by off-the-shelf components.The post-layout simulation show that the gain mismatch estimation error is less than 1.9% and phase mismatch estimation error is 0.5° which is whithin the accuracy limit for standard

EVM requirement. Further, the BIST circuit is implemented in 130nm technology and occupies less than 5% of an IQ transmitter. The BIST measurement time is mostly defined by the output filter settling time and the ADC speed and is in order of few micrometers.

In chapter 4, an automated reconfigurablity method developed for post-production and in-field adaptability purposes. A fully digital adaptable LNA is designed in 130nm technology.The calibration hardware occupies less than 0.1% of the LNA circuit. he calibration circuit adds up to 0.2 dB to the overall LNA noise figure. A prediction algorithm is established by statistical characterization and is employed for fast adaptation. Applying the algorithm on simulation and measurement results proves the validity of the proposed method with prediction error less than 10/% of the tuning range. In most cases the calibration can be done in one shot.

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