Ultra-low Quiescent Current NMOS Low Dropout Regulator With Fast Transient response for Always-On Internet-of-Things Applications

by

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ABSTRACT

The increased adoption of Internet-of-Things (IoT) for various applications like smart home, industrial automation, connected vehicles, medical instrumentation, etc. has resulted in a large scale distributed network of sensors, accompanied by their power supply regulator modules, control and data transfer circuitry. Depending on the application, the sensor location can be virtually anywhere and therefore they are typically powered by a localized battery. To ensure long battery-life without replacement, the power consumption of the sensor nodes, the supply regulator and, control and data transmission unit, needs to be very low. Reduction in power consumption in the sensor, control and data transmission is typically done by duty-cycled operation such that they are on periodically only for short bursts of time or turn on only based on a trigger event and are otherwise powered down. These approaches reduce their power consumption significantly and therefore the overall system power is dominated by the consumption in the always-on supply regulator.

Besides having low power consumption, supply regulators for such IoT systems also need to have fast transient response to load current changes during a duty-cycled operation. Supply regulation using low quiescent current low dropout (LDO) regulators helps in extending the battery life of such power aware always-on applications with very long standby time. To serve as a supply regulator for such applications, a 1.24 µA quiescent current NMOS low dropout (LDO) is presented in this dissertation. This LDO uses a hybrid bias current generator (HBCG) to boost its bias current and improve the transient response. A scalable bias-current error amplifier with an on-demand buffer drives the NMOS pass device. The error amplifier is powered with an integrated dynamic frequency charge pump to ensure low dropout voltage. A low-power relaxation oscillator (LPRO) generates the

charge pump clocks. Switched-capacitor pole tracking (SCPT) compensation scheme is proposed to ensure stability up to maximum load current of 150 mA for a low-ESR output capacitor range of 1 - 47µF. Designed in a 0.25 µm CMOS process, the LDO has an output voltage range of 1V – 3V, a dropout voltage of 240 mV, and a core area of 0.11 mm^2.

DEDICATION

To Appa, Amma, Vinu, Ganu and all the wonderful teachers I have been blessed with!

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CHAPTER 1

INTRODUCTION AND RESEARCH BACKGROUND

1.1. Need For Low Power Consumption

In the recent times, the influence of electronics on our everyday life has increased dramatically with the adoption of Internet of Things (IoT), where everything is interconnected. Smart home devices, medical instrumentation, industrial automation, automotive, etc. are just a few examples of the applications which have seen explosive growth in the number of internet connected electronic devices. Typically, sensor systems in such IoT devices have to be placed virtually anywhere and therefore have to be powered by a battery. Therefore, low power consumption between either successive recharge cycles or battery replacement is a necessity, particularly when the batteries are expensive, not easily accessible or when they are used in sensitive systems which have to be always-on [1]. The operating life of the battery powering an application can be given by

$$Battery\ Life = \frac{Battery\ Capacity}{Average\ load\ current} \tag{1}$$

From equation (1), we can see that for a given capacity, the only way to increase the battery life is by reducing the average load current consumption.

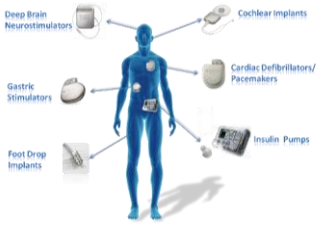
1.2. System-level Techniques for Low Power Consumption

Always-on IoT sensor systems and other portable devices with low-power micro-controller unit system-on-chip (SoC) ICs, rely on various power saving schemes to increase their battery life. Fig. 1.1 highlights some of these applications and their important characteristics. Dynamic supply voltage scaling and on/off supply schemes have been presented in [2] and [3] for low-power operation. Another increasingly common technique

is sleep/standby mode operation which is used to enable the system periodically only for short periods of time (duty cycled mode) or only when a trigger event (event driven mode) occurs. Otherwise, the system remains in off or very low power state of operation. This reduces the average current consumption dramatically. Clock driven or on-demand event driven fast wake-up schemes ensure fast response time for these systems. Due to these schemes, the standby power consumption of such systems is dominated by their supply regulators which have to invariably kept on all the time. Fig. 1.2 shows the load current profile of the regulator powering such an application. Two critical features of such a

Smart Home Devices

- Sensors placed virtually anywhere
- Not always powered by AC
- Mostly always-on



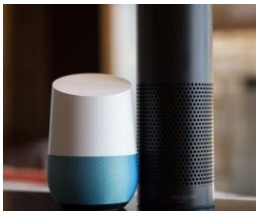
Medical and fitness monitors

- Very long battery life a necessity
- Charged for life – IMDs
- Reliable operation is critical
- Mostly duty – cycled operation

Power Management

Smartphones and Wearables

- Minimum power consumption between charging cycles
- Always battery powered
- Event – driven or duty – cycled operation



Voice activated assistants

- Minimum power consumption between charging cycles
- Event – driven operation
- Reliable communication with cloud or in-memory computing

Figure 1.1: Importance of low power consumption in common IoT applications.

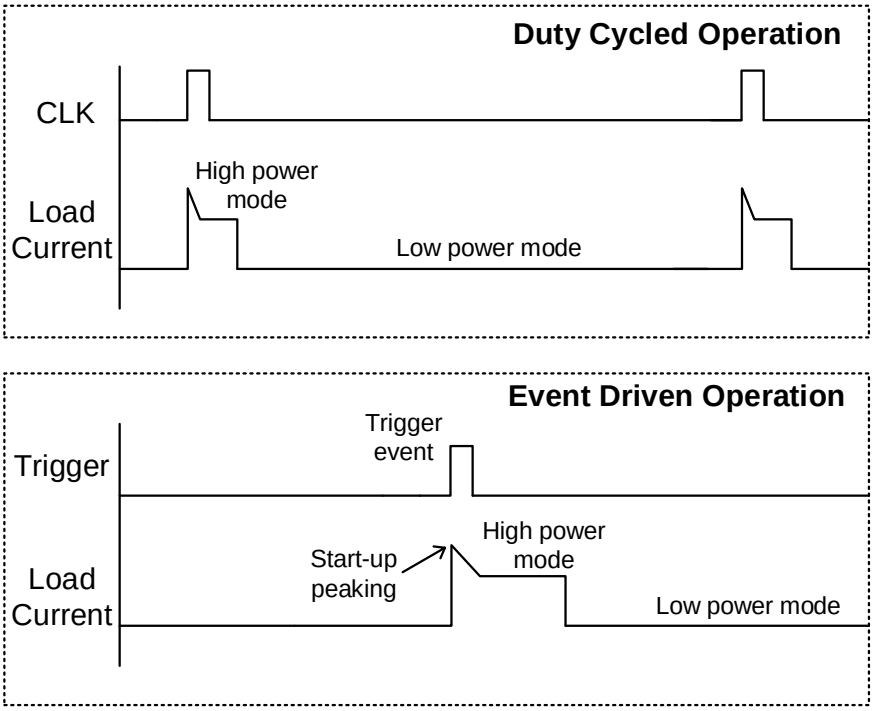


Figure 1.2: Load current profile for low power operation.

regulator are: very low power consumption during standby mode and fast response to transient load currents during fast wake-up.

1.3. Low Quiescent Current Low Dropout Regulator – Design Tradeoffs

In comparison to switching regulators, low dropout (LDO) regulators are preferable for applications which need fast transient response for a relatively low quiescent current (I_Q). Output capacitor stabilized low dropout regulators powering such applications must have low power dissipation for better efficiency when the load current (I_{LOAD}) is close to zero and achieve good transient response to switching load current with minimum variation in their output voltage (V_{OUT}). Since the time spent in the high load current state for IoT

applications is very low as shown in Fig 1.2 earlier, the losses due to dropout voltage also scale down significantly and the overall power consumption is dominated by the stand-by I_Q.

Fig. 1.3 shows the block level description of a typical LDO with a PMOS pass device. Output voltage (V_{OUT}) regulation with respect to varying supply and load current conditions is achieved by using an error amplifier in negative feedback. The gate voltage of the pass device is modulated to ensure that V_{OUT} is a predetermined ratio of the input reference voltage (V_{REF}). The transient response of an LDO which is a critical feature under consideration, can be measured by looking at the variation in V_{OUT} during a sudden step change in the load current (ΔI_{LOAD}). The undershoot/overshoot voltage (ΔV_O) during a load transient event is given by

$$\Delta V_O \cong \frac{\Delta I_{LOAD}}{C_{LOAD}} * t_R + I_{LOAD} * R_{ESR} \quad (2)$$

where t_R is the recovery time of the LDO and, C_{LOAD} and R_{ESR} are the output storage

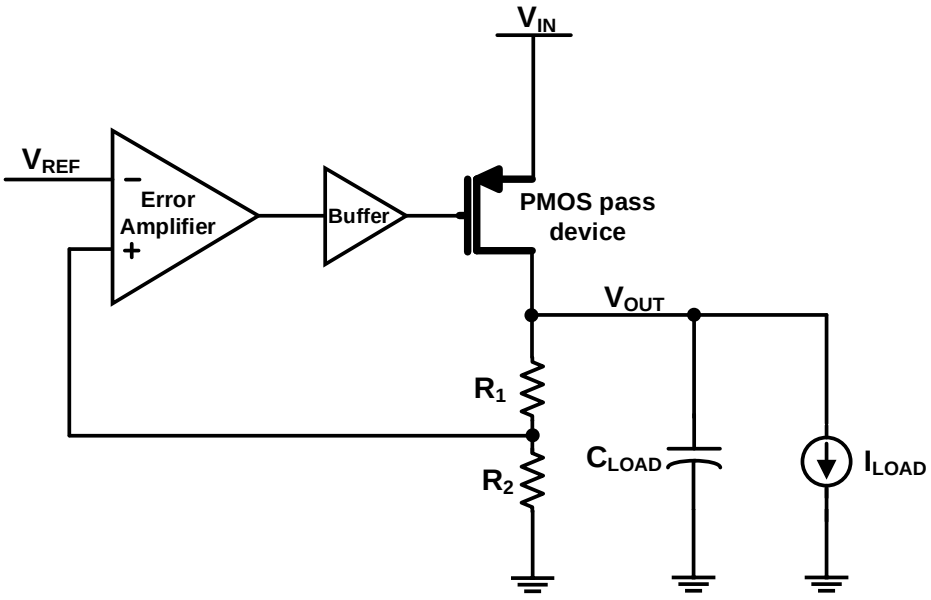


Figure 1.3: Block diagram of a typical low dropout regulator.

capacitance and its equivalent series resistance respectively. t_R is governed by two distinct mechanisms [5] namely the loop bandwidth associated delay (t_{BW}) and the internal slew rate associated delay (t_{SR}). Effectively, t_R is given by

$$t_R = t_{BW} + t_{SR} \tag{3}$$

Assuming a single-pole response for the loop gain with a 3-dB bandwidth of f_{-3dB}, t_{BW} can be estimated to be

$$t_{BW} \approx \frac{2.3}{2\pi f_{-3dB}} \tag{4}$$

However, since load transients are large signal events, slewing of large parasitic capacitances inside the loop, adds even more delay to transient response. The biggest parasitic capacitance is at the gate of the pass device (C_{par}). Therefore t_{SR} can be estimated to be

$$t_{SR} \approx \frac{C_{par} * \Delta v_{par}}{I_{O,EA}} \tag{5}$$

where Δv_{par} is the required change in the gate capacitance voltage to address the load current change of ΔI_{LOAD} and $I_{O,EA}$ corresponds to the maximum slew-rate limited output current of the error amplifier stage. For a pass device transconductance of $G_{M,PASS}$, (5) can be re-written as

$$t_{SR} \approx \frac{C_{par} * \Delta I_{LOAD}}{I_{O,EA} * G_{M,PASS}} \tag{6}$$

Using (3), (4) and (6) we have

$$t_R \approx \frac{2.3}{2\pi f_{-3dB}} + \frac{C_{par} * \Delta I_{LOAD}}{I_{O,EA} * G_{M,PASS}} \tag{7}$$

Thus, t_R which is inversely proportional to f_{-3dB} and $I_{O,EA}$, can only be reduced at the expense of higher bias current. This shows that the LDO suffers from the traditional "Transient response vs. Power consumption tradeoff" which is addressed in this research to ensure better transient response while maintaining very low stand-by no-load I_Q, both of which are critical for powering always-On applications.

1.4. Applications of Low I_Q LDOs

This section discusses two applications to highlight the importance of a low I_Q LDO in improving the battery life of a portable and IoT system which uses either duty – cycling or event – driven schemes or both to reduce power consumption.

Application 1: Wireless consumer medical devices such as blood glucose monitors, heart rate monitors or an insulin pump, not only enable patients to monitor their health at home or on the go, but also help the doctors in remote monitoring and data logging of the vital signs to assist in early detection and treatment of medical conditions [4]. Such devices monitor, collect and send data to the medical cloud in short bursts periodically and then enter sleep/stand-by mode to save power. Apart from ease of use, high measurement accuracy, secure connectivity, small form factor and long battery life are some of the necessary features of such devices.

Application 2: A wall mounted wireless dimmer switch featuring a touchpad for dimming the lights in a smart home application [1]. The light bulb itself is connected to the AC mains supply, but the switch is battery-operated so that it can be placed anywhere in the room or relocated depending upon the user convenience. The switch wakes up on detection of finger

touch on the touchpad and a valid finger gesture is communicated to the lights wirelessly and then goes back to sleep-mode till the next user activity.

A block diagram description for both of these applications look similar and is given in Fig. 1.4. The most commonly used Li-Ion battery is used to power a very low I_Q LDO which powers the always-on real time clock (RTC). In case of an event driven application like the dimmer switch, the capacitive touchpad sensor is the always-on sensor which is also powered by this LDO. The rest of the circuitry is typically turned off using a load switch [4]. This load switch is enabled either when an activity is detected (as in the dimmer switch) or periodically based on RTC (as in medical monitors) and turns on the more efficient buck converter. The converter powers noise insensitive digital blocks like the microcontroller unit, memory and display while maintaining high conversion efficiency.

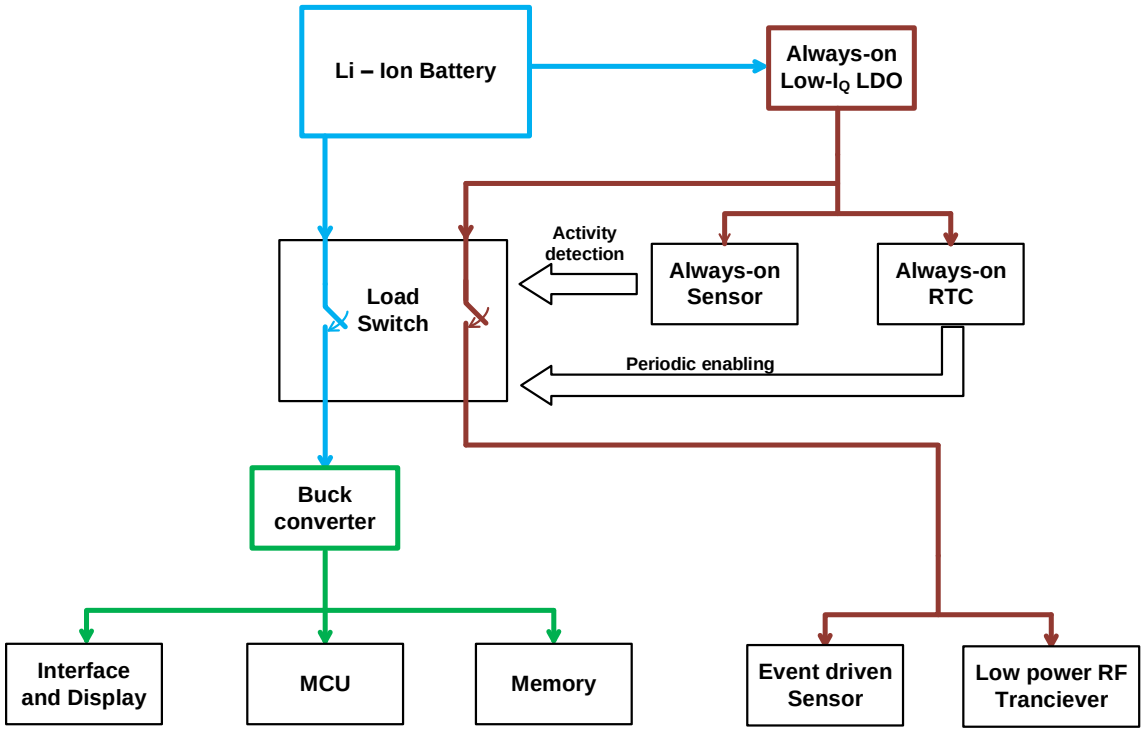


Figure 1.4: Block diagram of a typical battery powered always-on IoT application.

Medical devices which use the RTC to turn on for short bursts enable the event – driven sensor during their on time to capture the patient vitals. This sensor and the RF transceiver, both of which are noise sensitive, are powered by the same low I_Q LDO during the on time periods. Based on these applications, it is clear that low I_Q LDO would be an appropriate fit as long as it features good transient response to the load current variations.

To put it in numbers, let us revisit the dimmer switch application described in [1]. The active current (I_{Active}) is primarily dominated by the low power RF circuitry which gets activated during a user input to transmit data to the lights. However, the sleep mode current $\left(I_{Sleep}\right)$ is primarily dominated by the power management and the always-on capacitive sensor with $I_{Active} = 2.2\ mA$ and $I_{Sleep} = 6\ \mu A$. Even if we assume a worst-case active time (T_{Active}) of 2 seconds per user input and 20 such events in a day, the overall average consumption $\left(I_{Avg}\right)$ is given by $I_{Avg} = \frac{2.2mA*2*20}{60*60*24} + 6\mu A = 1\mu A\ (I_{Active}) + 6\mu A\ \left(I_{Sleep}\right)$. As can be clearly seen, I_{Avg} is majorly a function of I_{Sleep} rather than I_{Active}. Therefore, low I_Q power management is critical in reducing I_{Avg} and improving battery life.

1.5. Organization of the Dissertation

The rest of the thesis is organized as follows: Chapter 2 captures an overview of the past research literature on current scaling schemes for improving the transient response in low I_Q LDOs and describes the motivation for this research. Chapter 3 introduces the proposed NMOS LDO solution at block level and gives a brief overview of system level considerations for the design. Chapter 4 discusses the design details of the proposed current scaling approach along with the variable bias current error amplifier and the associated

charge-pump. Chapter 5 gives a detailed description of the proposed ultra-low power current or voltage tunable relaxation oscillator with very low switching losses and Chapter 6 discusses the novel switched-capacitor pole tracking compensation scheme used in this LDO. Chapter 7 shows the simulated and measured results of the LDO and compares its performance with the prior-art. Chapter 8 concludes the thesis with the research conclusion and gives an account of the future improvements which can be done for complete product development.

CHAPTER 2

LITERATURE SURVEY AND RESEARCH MOTIVATION

For solving the transient response vs. I_Q trade-off presented in section 1.3, various current scaling schemes have been presented in the past to boost the bandwidth and slew-rate of the LDO. These techniques can be broadly classified into 3 categories: adaptive biasing, dynamic slew-rate enhancement and a combination of both.

2.1. Adaptive Biasing

Adaptive biasing is a more simpler and straight-forward current scaling scheme in an LDO where the bias current is proportional to I_{LOAD} [6]-[8]. This is typically achieved using a current mirror at the pass device as shown in Fig. 2.1 where a scaled version of the load current (1 : k) is obtained and mirrored to boost the bias current in the error amplifier. This approach gives the benefit of better slew rate and better loop bandwidth at higher I_{LOAD}. However, the increase in bias current is only possible after the error amplifier has

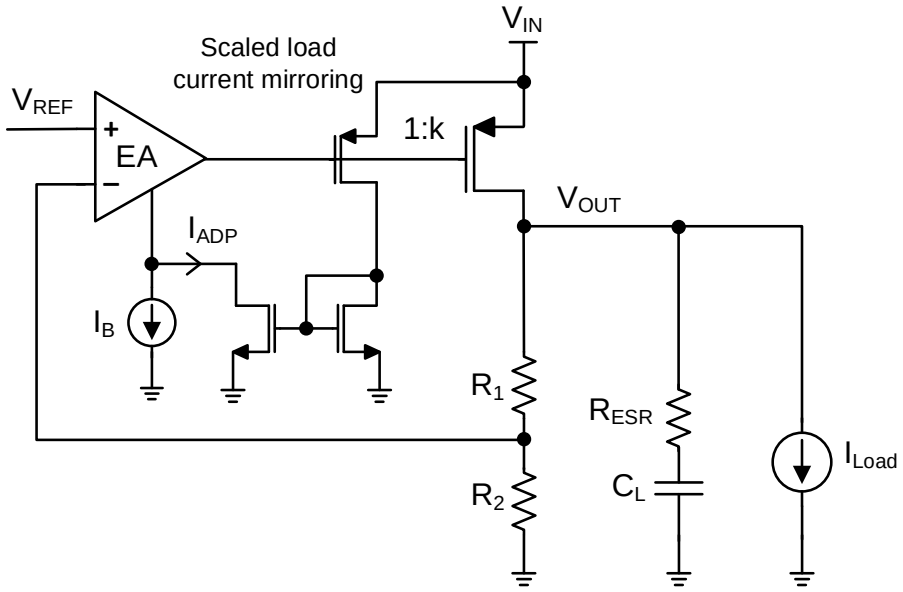


Figure 2.1: Adaptive bias current scaling scheme.

reacted to the load current change and provided the gate voltage change (Δv_{par}) as shown in equation (4), which makes this scaling scheme inherently slow to begin with due to low bias current at light load conditions. Therefore, the recovery time and undershoot for zero to full load transition of low-I_Q LDOs, cannot be minimized with this scheme and requires faster current scaling approaches.

2.2. Dynamic Slew-rate Enhancement

Monitoring the error in output voltage during a load transient provides a faster way of scaling the bias current in comparison to adaptive biasing. Dynamic slew-rate enhancement schemes are presented in [9]-[15] where the slew rate at the gate of the pass device is scaled only during the load transient event, thereby reducing undershoot voltage. Fig. 2.2 shows two commonly used techniques to detect fast output voltage changes. First approach (a) presented in [9] and [12], monitors the error voltage between the output voltage and a reference voltage using an amplifier and translates this error voltage into an

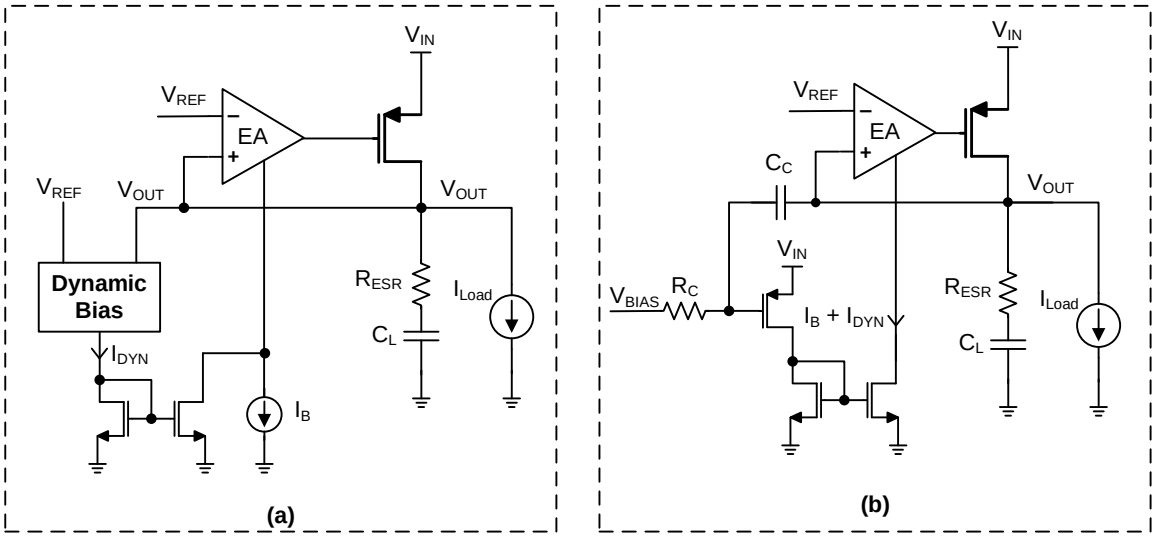


Figure 2.2: Dynamic slew-rate enhancement scheme.

increased bias current in the main error amplifier. The second technique (b) presented in [10], [11], [13]-[15] uses high pass filter schemes to capacitively couple the transient voltage error signal, amplify it and use it to boost the bias current momentarily. Dynamic slew-rate enhancement technique alone is very effective in output capacitor-less LDOs where the parasitic gate capacitance tends to decide the dominant pole as well as the required slew rate. In general, low I_Q output capacitor-less LDOs offer limited maximum load current capability and suffer from large undershoot voltage during zero to full-load current step due to the absence of output storage capacitance. Moreover, not utilizing adaptive biasing will reduce the overall performance of the LDO at mid to high I_{LOAD} conditions. The capacitive coupling scheme is only efficient in tracking fast variations in V_{OUT} and does not react to slow changes. This is governed by the pole location of the RC high pass filter and therefore is ineffective in improving transient response for steps in I_{LOAD} which are slower than the pole frequency.

2.3. Combination of Adaptive Biasing and Dynamic Slew-rate Enhancement

Recently, LDOs which employ dynamic slew enhancement along with adaptive biasing have been reported in [16]-[18]. Although increased slew rate helps in reducing t_{SR} as shown in equations (3) to (5), high t_{BW} due to limited loop bandwidth at light load currents can still limit the total recovery time t_R for zero to full load current transients, especially in output capacitor stabilized LDOs. Therefore, a more effective approach is to use the adaptively and dynamically scaled current to improve the loop bandwidth as well as the slew-rate. This in-turn reduces the t_R and improves the overall transient response of the LDO.

2.4. Other low I_Q LDO techniques

Apart from the above mentioned three categories, few other low I_Q LDO design approaches have been presented in the past for better transient performance. In [19], an LDO which uses multiple small-gain stages as a substitute for high-gain single stage amplifier is presented. Such stages are claimed to provide well-controlled gain enhancement without introducing low-frequency poles before the loop unity gain frequency (UGF) and simplify the overall compensation process even with low I_Q. Although it achieves competitive transient response, the LDO still depends heavily on the output capacitor ESR zero for its stability. The ESR zero is not guaranteed when low cost ceramic capacitor is used and therefore such an LDO would be unsuitable. A dual pass-transistor multi-stage approach is presented in [20]. A small pass transistor is used in conjunction with an adaptively biased amplifier as a two stage design, for regulating small load currents. As the load current increases above a certain threshold value, the LDO transforms itself into a 3-stage structure biased by a fraction of the load current conducted by the small pass device. This helps the output capacitor-less LDO achieve stability even with a low I_Q. However, the maximum output capacitance is limited to 100pF making this scheme unsuitable for output capacitor stabilized LDOs. [21] presents a fully-integrated NMOS LDO which generates a low-ripple regulated output voltage. It efficiently manages the available supply voltage for the error amplifier and then uses the switched capacitor DC-DC converter output as the supply for pass device of the LDO. However, due to unavailability of a good output storage capacitance in this fully integrated scheme, it suffers from large undershoot voltage for a relatively small load current transient.

2.5. Research Motivation

As seen from the analysis in chapter 1 and from all the prior-art in the field, the key considerations of low I_Q LDO design are mainly the transient response and stability across all load current conditions. As highlighted earlier, a better way to solve the I_Q vs t_R trade-off is to ensure that a fast current scaling scheme is utilized to improve both bandwidth and slew-rate while maintaining very low no-load I_Q. This presents a challenging problem for the current scaling methodology. A bias current scalable fast response architecture for error amplifier and pass device is also critical for achieving fast load transient response. Moreover, achieving stability of the LDO for a range of C_{LOAD} values across all I_{LOAD} conditions, without depending upon the availability of an ESR zero, requires development of a novel-approach for compensation. These major challenges serve as the motivation for this research with an end goal of developing a very low no-load I_Q LDO, which can be a favorable choice for supply regulation of battery powered and long standby time applications.

CHAPTER 3

BLOCK LEVEL OVERVIEW OF THE PROPOSED NMOS LDO

Fig. 3.1 shows the block diagram of the proposed LDO with a very low I_Q of 1.24 µA. The LDO uses an NMOS pass device instead of the more common PMOS pass device for supply regulation as it offers three distinct and highly favorable advantages:

1) Superior transient response due to inherent change in gate-source voltage V_{GS} during load transient undershoot/overshoot
2) Lower output impedance even at light load current condition and,
3) Smaller physical size and lower parasitic gate capacitance for a given maximum load current capability and dropout voltage due to higher electron mobility.

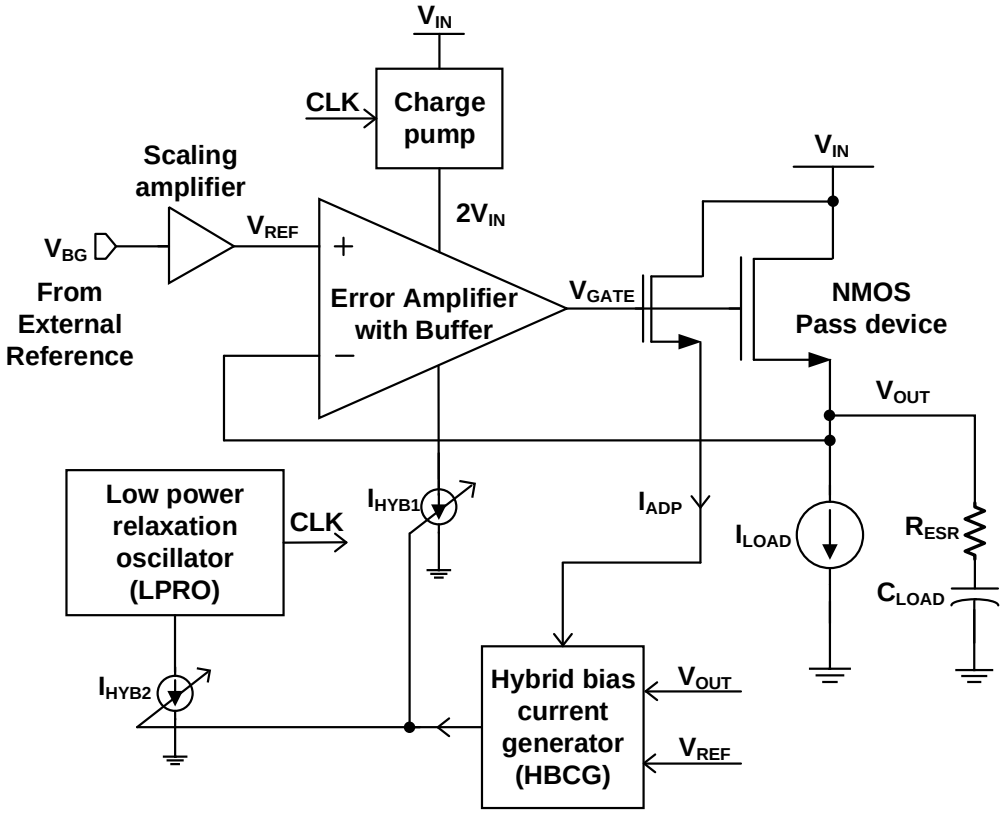


Figure 3.1: Block diagram of the proposed low I_Q NMOS LDO.

A bias-current scalable, two stage error amplifier with an on-demand pull-up/pull-down buffer is designed to drive the gate of the NMOS pass-device. A hybrid bias-current generator (HBCG) that scales the bias current dynamically during load transients and adaptively with I_{LOAD} is proposed for improved transient response. This HBCG scheme achieves fast I_Q scaling which improves both loop bandwidth and slew-rate of the error amplifier even at light I_{LOAD}. Fig. 3.2 shows a comparison of the bias current profile of the HBCG scheme in this LDO with current scaling techniques presented earlier.

In order to avoid higher dropout voltage due to limited overdrive at the gate of the NMOS pass device, the error amplifier is powered with a charge-pump voltage doubler.

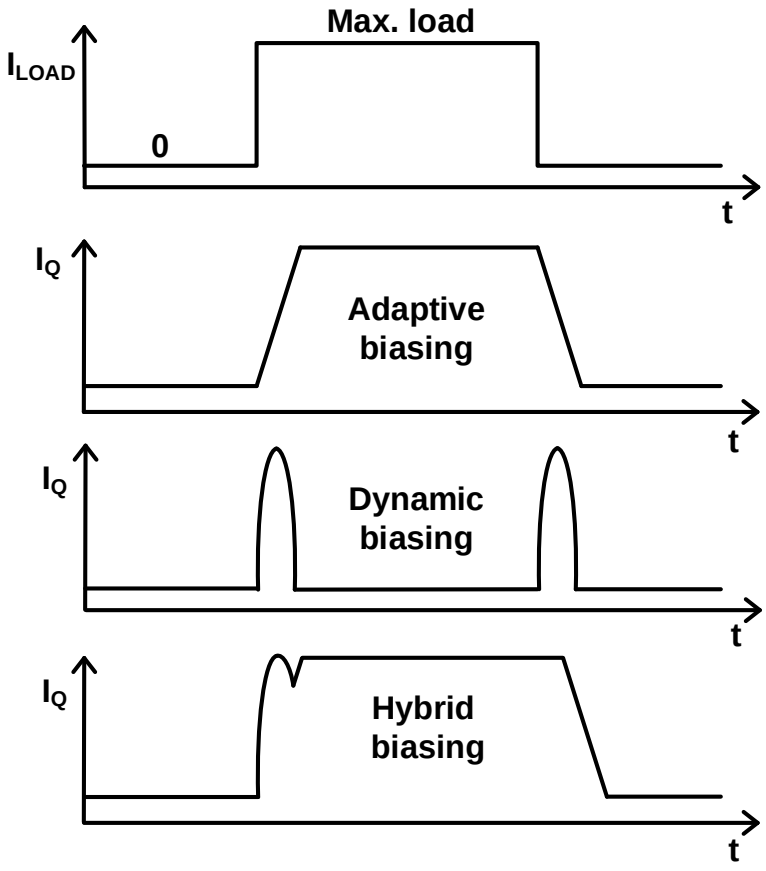


Figure 3.2: Comparison of hybrid biasing with previously presented I_Q scaling schemes.

This charge-pump provides sufficiently higher supply voltage ($\approx 2 * V_{IN}$) and ensures that the pass device has sufficient gate voltage to keep the dropout voltage to 240mV. In the past literature, native NMOS which offers negative or close to zero threshold voltage have been used as the pass device for maintaining low dropout voltage. However, additional mask cost, larger area due to higher minimum length and well separation and, very high sub-threshold drain-source leakage which can be significant in such low I_Q LDO designs are the three major reasons for preferring the regular NMOS and charge-pump combination over native NMOS.

Due to the hybrid biasing scheme for the error amplifier, its overall current consumption changes with load current and during a transient step. In terms of the charge-pump, the error amplifier acts as a variable load current at its output. In order to mitigate the drop in the $2 * V_{IN}$ voltage output, a dynamic frequency charge-pump is employed to power the hybrid-mode biased error amplifier. A low-power relaxation oscillator (LPRO) is proposed to generate the charge pump clocks with clock frequency proportional to the I_{LOAD}. This LPRO's bias current is controlled by the HBCG output current and therefore, tracks the steady change as well as transient changes in load current. This variable frequency clock is re-used for LDO compensation in the proposed switched-capacitor pole tracking (SCPT) compensation scheme for loop stability across all load conditions.

This LDO provides a maximum I_{LOAD} of 150 mA while using a low-ESR 1 µF load capacitor (C_{LOAD}). The LDO is shown to be stable even for load capacitance up-to 47 µF. A low-power scaling amplifier shifts the external reference voltage of 0.8 V to an internal reference (V_{REF}) equal to the required output voltage (V_{OUT}) using a feedback resistor divider. The scaling amplifier ensures that the error amplifier is operated in unity-gain

configuration which provides the highest possible bandwidth across output voltage combinations. The input supply voltage range is from 1.5 V to 3.3 V and the LDO output voltage is programmable from 1.0 V to 3.0 V. The following three chapters discuss the design details of each of the constituent blocks inside the LDO.

CHAPTER 4

ERROR AMPLIFIER WITH HYBRID BIASING

4.1. Hybrid Bias-current Generator (HBCG)

The major considerations while designing the HBCG circuit apart from current scaling are quick response to load current transients and very low contribution to I_Q. Since fast dynamic current scaling is critical for the overall transient response of the LDO, it has to respond quickly. Adaptive biasing on the other hand, is naturally a slow loop since the current scaling only happens after the overall loop responds and modulates the gate voltage in accordance with change in I_{LOAD}.

Load current dependent adaptive biasing is usually obtained by mirroring a fraction (1:k) of the pass device current using a current mirror. However, in the case of an NMOS pass device, the source voltage of the mirror NMOS needs to be matched to the source

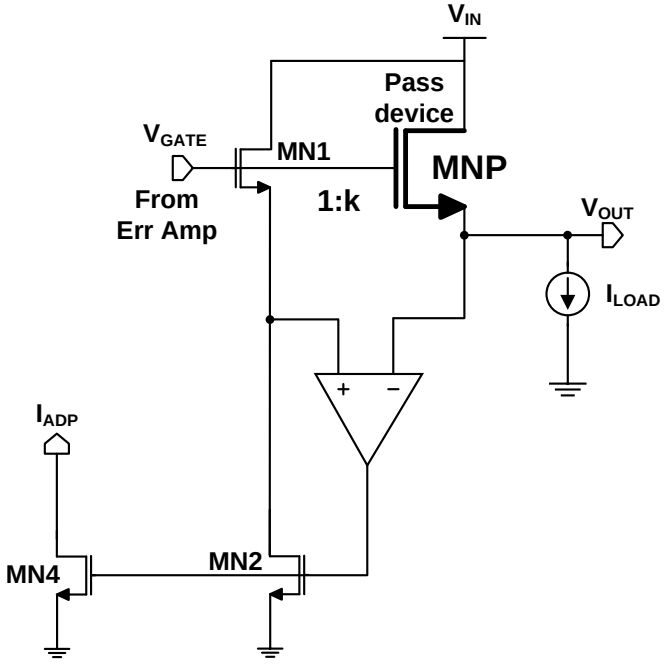


Figure 4.1: Adaptive biasing current mirror with feedback amplifier.

voltage of the pass device which is V_{OUT}. Typically, a negative feedback amplifier is used to track the output voltage and regulate the source node of the mirror MN1 as shown in Fig. 4.1. However, such an amplifier will contribute to the already limited I_Q budget of the LDO and is not favorable.

In order to avoid this additional amplifier, a zero I_Q load dependent adaptive current scaling is proposed as shown in Fig. 4.2. A fraction (1:4000) of the I_{LOAD} in pass device MNP is mirrored by the mirror MN1. In order to ensure accurate mirroring, the source voltage of MN1 needs to be equal to V_{OUT} and this voltage mirroring is ensured using the current mirrors MN2 and MN3 along with MP1 and MP2. As I_{LOAD} increases, drain-source current in MN1 also increases and current mirror pair MN2-MN3 ensures equal current flow in both branches, forcing MP1 and MP2 to have the same V_{GS}. As the gate terminal is

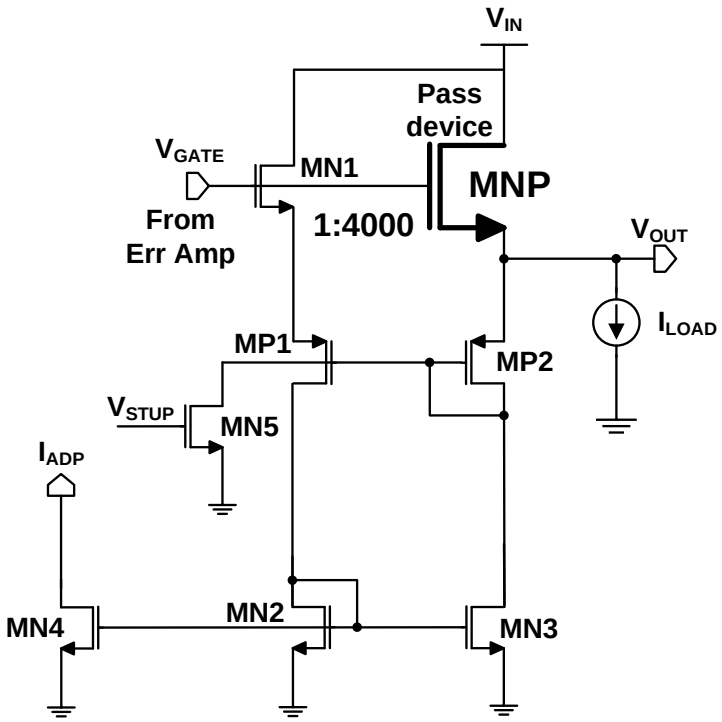


Figure 4.2: Proposed zero I_Q adaptive current scaling circuit.

common to both MP1 and MP2, the source voltage of MP2 which is V_{OUT} is copied onto the source terminals of MP1 and MN1. MN4 mirrors the final adaptive current (I_{ADP}). At zero I_{LOAD}, MN1 is in deep sub-threshold region and does not conduct any current. Effectively, the entire adaptive scaling implementation has no contribution in the overall I_Q of the LDO and serves as a major advantage in such low I_Q LDOs. During power-up of the LDO, the gate voltage of MN2 and MN3 is pulled down to ground by diode connected MN2. However, the common gate voltage of both MP1 and MP2 is indeterministic at start-up and if it is close to V_{DD}, the entire adaptive scaling circuit may fail to turn on even when I_{LOAD} increases as MP1 and MP2 will remain in off state. In order to avoid this faulty case, their gate node is discharged to ground by MN5 using a short pulse V_{STUP} at start-up.

Fast dynamic current scaling is based on virtual ground error voltage ($\Delta V = V_{OUT}$ - V_{REF}) which is obtained by monitoring the input voltages of the error amplifier. Fast detection is achieved by utilizing PMOS common-gate differential pair with source

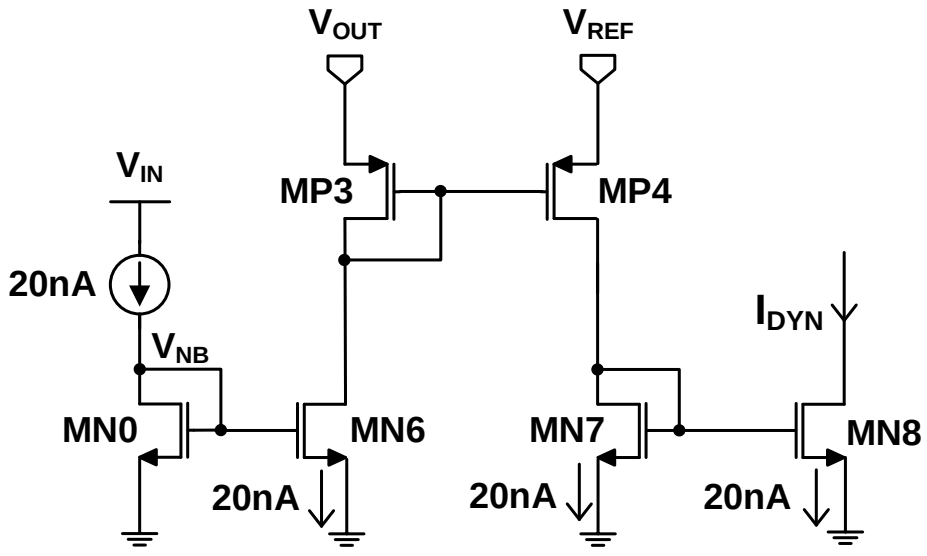


Figure 4.3: Error voltage dependent dynamic current scaling circuit.

terminals as inputs. As shown in Fig. 4.3, the input pair consists of highly matched MP3 and MP4 transistors operating in sub-threshold region. When the LDO is in steady state, the error voltage $\Delta V \cong 0$ and the 20 nA bias current is mirrored to generate I_{DYN} = 20 nA through MP3-MP4 and MN7-MN8 current mirrors. However, during an output undershoot event ($\Delta V < 0$) caused due sudden step-up of I_{LOAD}, the undershoot in V_{OUT} produces an increased gate drive (ΔV_{SG}) for MP4 through diode connected MP3. Effectively, current through MP4 which is biased in sub-threshold region increases exponentially and is mirrored by MN7-MN8 resulting in an exponential increase in I_{DYN}. Due to absence of high impedance paths, this scheme provides instantaneous current scaling during load transients. Fig. 4.4 shows the transient response of the dynamic biasing circuit during an output undershoot event. It can be seen that the bias current scales exponentially as the

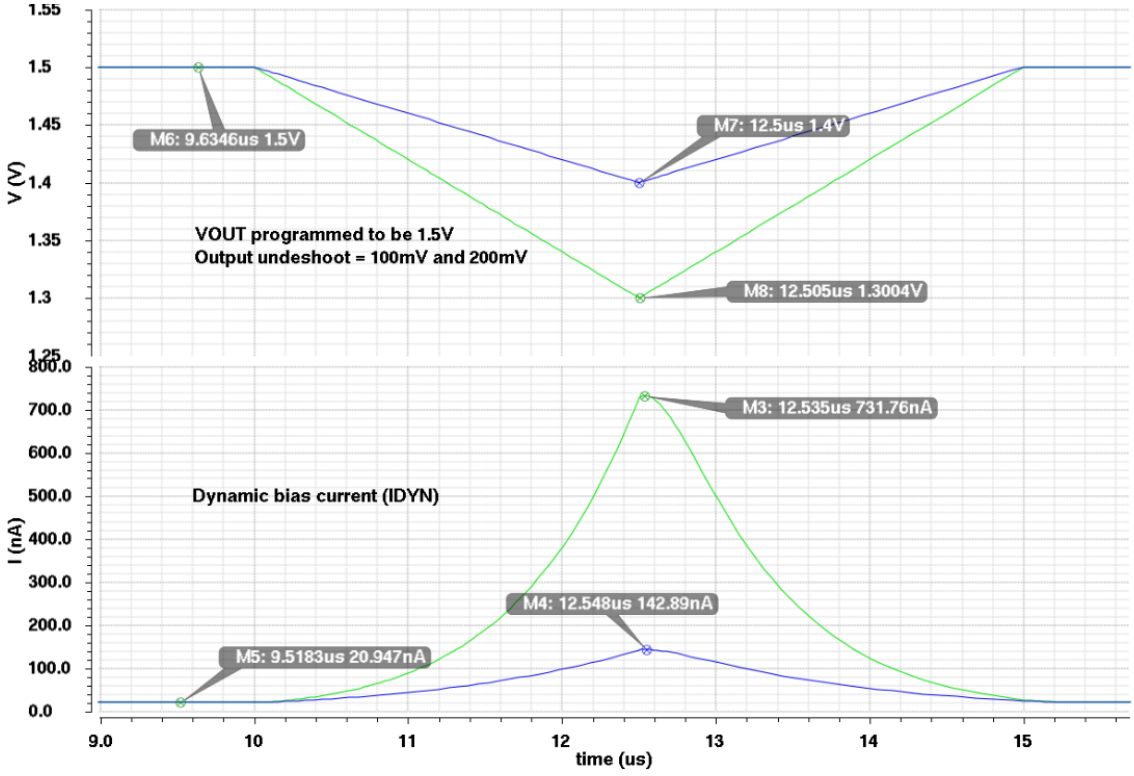


Figure 4.4: Transient response of the dynamic current scaling circuit.

undershoot voltage increases and is very quick to respond. There is a continuous increase in current for increase in undershoot voltage thereby increases the bias current for all load transient events as long as there is a voltage error.

The overall HBCG circuit is shown in Fig. 4.5 where the adaptive current (I_{ADP}) is added to dynamic current (I_{DYN}) and then mirrored by MP5-MP6,MP7 to generate the bias currents of the error amplifier (I_{HYB1}) and oscillator (I_{HYB2}). Additionally, a current-comparator based, on-demand pull-down circuit is added to discharge the load capacitor (C_{LOAD}) during an overshoot event ($\Delta V > 0$) caused due to sudden step-down of I_{LOAD}. A sub-threshold biased PMOS pair MP8-MP9, similar to that of dynamic scaling circuit with reversed input voltage terminals is used as shown in the pull-down circuit segment of Fig. 4.3. In comparison to MN9, a 4x stronger current source MN10 is used to hold the gate of pull-down device MN11 to less than 15 mV which is much lower than the NMOS threshold voltage of 550mV. Such low gate voltage ensures that there is no unexpected leakage current through MN11 during steady state operation of the LDO. However, during V_{OUT} overshoot, higher gate drive (ΔV_{SG}) increases the current through MP9. This current overpowers the current source MN10 and pulls the gate of MN11 high, thereby discharging C_{LOAD}. This pull-down circuit is triggered only when the ΔV exceeds ~ 35 mV.

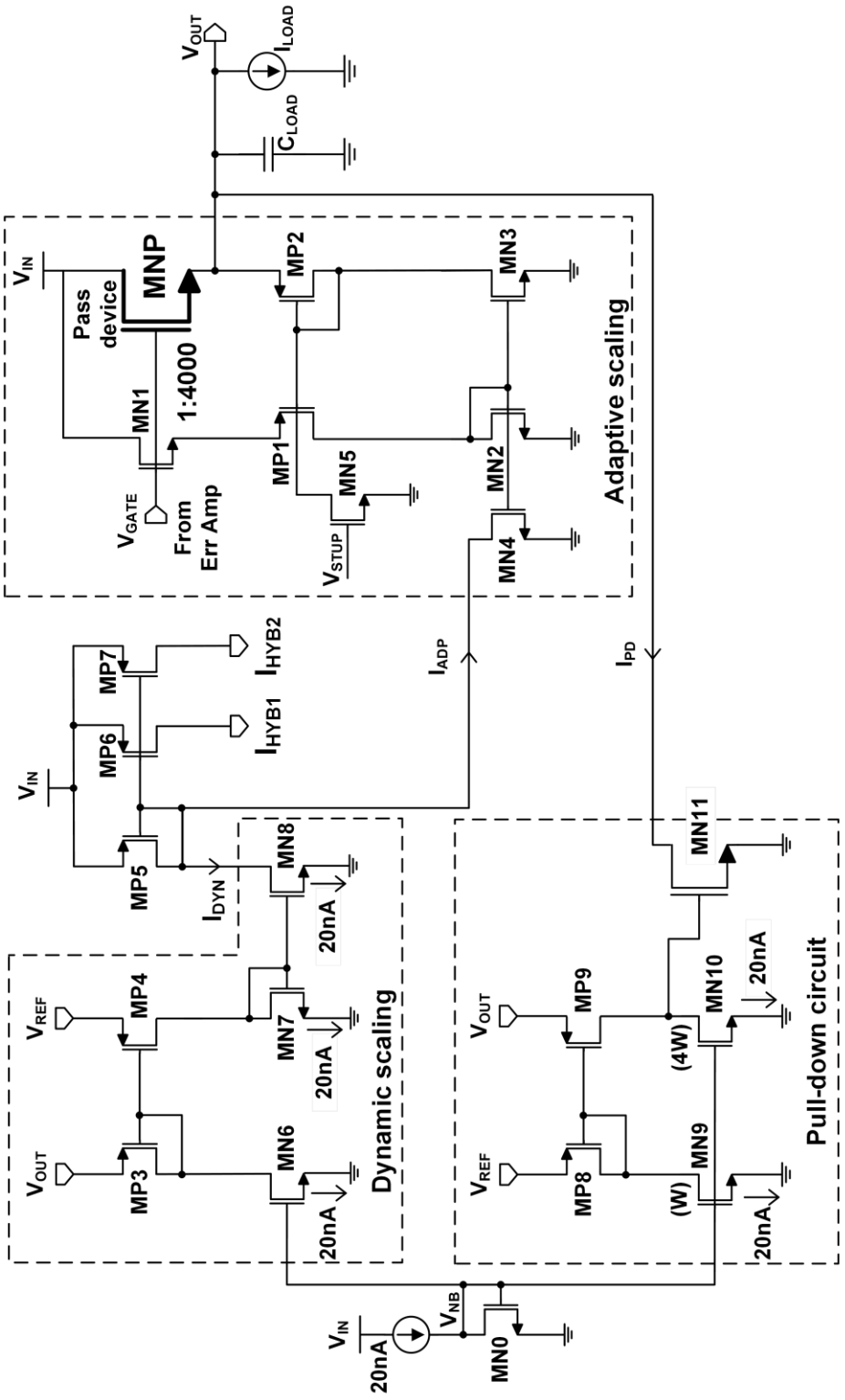


Figure 4.5: Hybrid bias current generator (HBCG) with on-demand output capacitor pull-down circuit.

4.2. Reference Scaling Amplifier

Fig. 4.6 shows the scaling amplifier which generates the scaled reference voltage V_{REF} from the external reference V_{BG} which is set to 0.8 V. This scaling amplifier needs to provide the dynamic current increase of the HBCG circuit and therefore has to be capable of sourcing current. It consists of simple two-stage design with a differential amplifier as its first stage and a PMOS common source amplifier as its second stage driving a 2pF output capacitance (C_{SA}). Such a configuration looks similar to a PMOS LDO which is capable of sourcing any amount of current required by the HBCG circuit. To keep the current branches to minimum, the bias voltage (V_{NB}) for the tail current source (MN1) is derived from MN0 of the HBCG circuit in Fig. 4.4 and both devices are closely matched in layout to minimize mismatch. The scaling amplifier is stabilized using miller capacitance C_C and resistor R_C is used to cancel the right half plane zero associated with miller

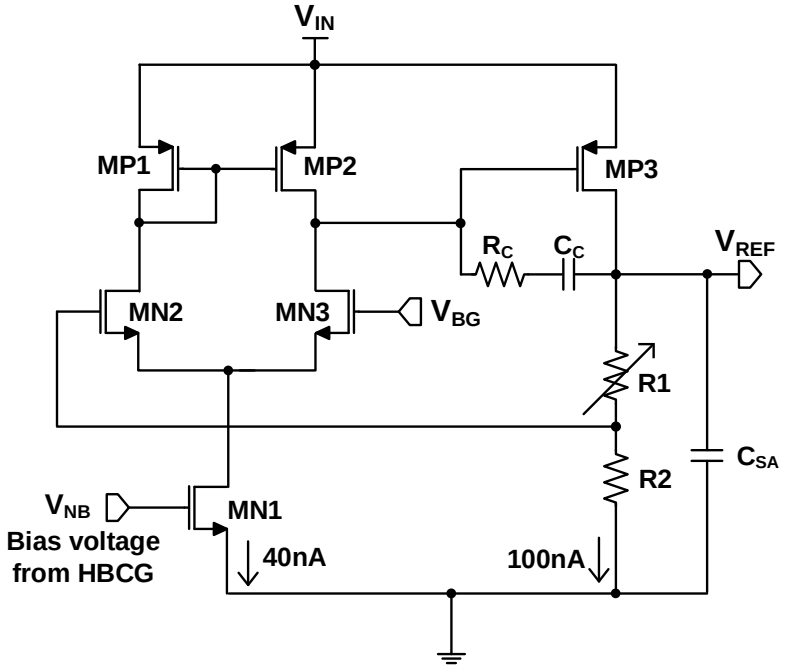


Figure 4.6: Scaling amplifier with programmable feedback resistor divider.

compensation. Digitally programmable resistor divider with fixed R_2 and variable R_1 is used to generate V_{REF} corresponding to the LDO output voltage range of 1.0 V – 3.0 V.

4.3. Error Amplifier with On-demand Pull-up/Pull-down Buffer

The regulation feedback loop consists of a two-stage error amplifier which is shown in Fig. 4.7. The 2x charge-pump provides the supply voltage to this bias current scalable error amplifier. Due to this 2*V_{IN} voltage supply which can go as high as 6 V when V_{IN} = 3.3 V, the error amplifier uses 7 V devices instead of 3.3 V devices. The pass device also is a 7 V regular NMOS. The bias current (I_{HYB1}) of the error amplifier is generated by the HBCG circuit.

The first stage of the amplifier is chosen to be a symmetrical operational transconductance amplifier (OTA) which provides ease of current scalability due to its automatic biasing voltage adjustments, merely by changing the input bias current. Small signal analysis of this amplifier shows that the gain of the amplifier (G_{AMP}) and its 3-dB pole location (P_{AMP}) are given by

$$G_{AMP} \cong gm_{MN2} * \left(r_{ds,MP4} || r_{ds,MN5}\right) \tag{8}$$

$$P_{AMP} \cong \frac{1}{2\pi\left(r_{ds,MP4} || r_{ds,MN5}\right) C_{AMP}} \tag{9}$$

where C_{AMP} is the effective load capacitance at the output of the first stage. With increase in I_{HYB1}, although output impedance ($r_{ds,MP4} || r_{ds,MN5}$) drops, increase in gm_{MN2} compensates for this drop, thereby maintaining a DC gain higher than 50 dB for all possible I_{HYB1} values. However, its 3-dB bandwidth increases proportionally with I_{HYB1} as P_{AMP} moves to a higher frequency due to the reduction in output impedance.

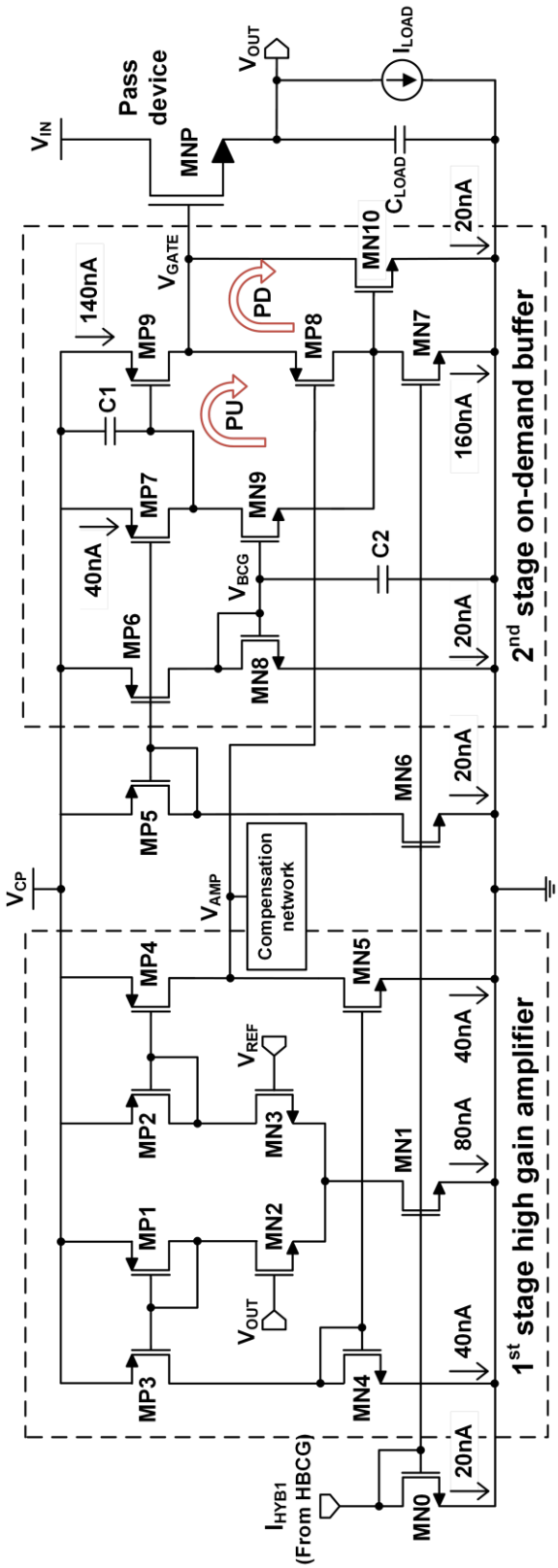


Figure 4.7: Two-stage error amplifier with on-demand pull-up/pull-down buffer.

A second stage bias current scalable dual-loop CMOS voltage buffer is placed in between the first stage and the pass device in order to increase the slew rate at the gate of the pass device and improve the load transient response. Unlike the voltage buffer with only on-demand pull-up capability as shown in [5] and super-source follower buffer with only on-demand pull-down presented in [6], the proposed buffer achieves on-demand fast pull-up (PU) as well as fast pull-down (PD) capability improving the transient response to I_{LOAD} step-up and step-down respectively.

At the core, the buffer consists of a PMOS source follower (MP8). For simplicity, the PU and PD loops are analyzed separately. Instead of a regular source follower biased with a fixed current source, dynamic fast pull-up is achieved through a negative feedback loop realized using common gate stage (MN9 and MP7) and common source stage (MP9) which constitute a cascoded flipped-voltage follower. This feedback loop not only provides the required on-demand sourcing current to charge the gate of pass device during a load step-up but also reduces the small-signal output impedance of the buffer. The effective output impedance can be calculated using the small signal equivalent diagram as shown in Fig. 4.8 (a) for the PU loop. Small signal test voltage Δv_x is applied at the output of the buffer with input v_{in} shorted to ground. The effective output impedance is given by

$$r_{0,PU} = \frac{\Delta v_x}{\Delta i_x} = \frac{\Delta v_x}{\Delta i_1 - \Delta i_2} \tag{10}$$

The small signal current $+\Delta i_1$ is translated to $-\Delta i_1$ onto the CG stage MN9, drops across the equivalent impedance of $(r_{ds,MP7}||r_{ds,MN9})$ and is converted to voltage Δv_{GP}. This Δv_{GP} is converted to Δi_2 using MP9 and is given by

$$\Delta i_2 = gm_{MP9} * \Delta v_{GP} \cong gm_{MP9} * -\Delta i_1 * \left(r_{ds,MP7}||r_{ds,MN9}\right) \tag{11}$$

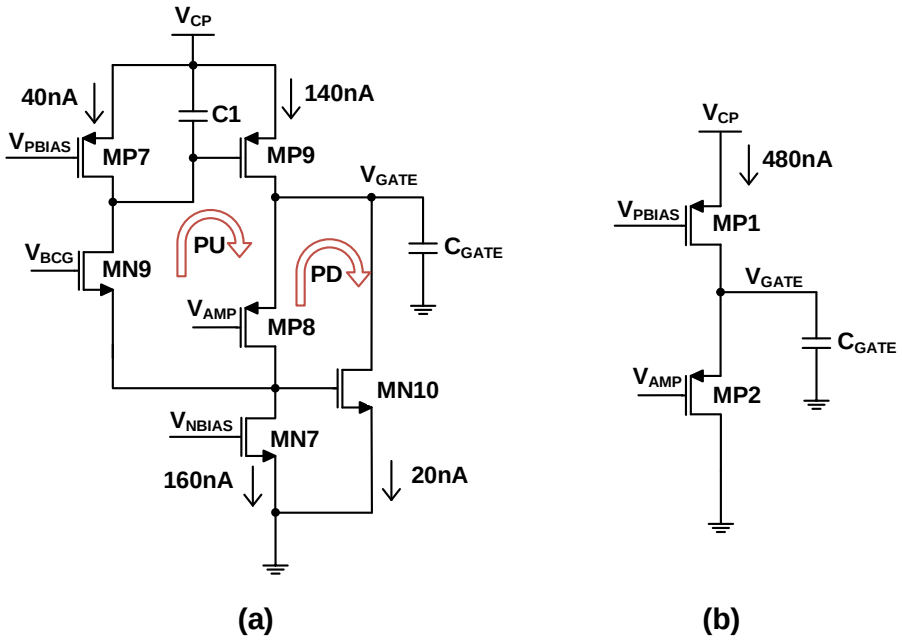


Figure 4.8: Small signal equivalent circuits for determining output impedance for active (a) pull-up loop and (b) pull-down loop of the proposed buffer.

Using (10) and (11) we get

$$r_{0,PU} \cong \frac{\Delta v_x}{\left[1 + gm_{MP9}(r_{ds,MP7}||r_{ds,MN9})\right]\Delta i_1} \tag{12}$$

Substituting $\Delta i_1 = gm_{MP8} * \Delta v_x$ in (12), we get

$$r_{0,PU} \cong \frac{1}{gm_{MP8} * gm_{MP9} * (r_{ds,MP7}||r_{ds,MN9})} \tag{13}$$

Thus the effective output impedance is reduced by a factor of loop gain given by $A_{PU} = gm_{MP9} * (r_{ds,MP7}||r_{ds,MN9})$ in comparison to a simple source follower in which case it would have been just $\frac{1}{gm_{MP8}}$, thereby pushing the parasitic pole at the gate of pass device (P_{GATE}) to higher frequency. Similar analysis can be done for the fast PD loop which is a super source follower formed by MP8, MN7 and MN10 as shown in Fig. 4.8 (b) where the effective output impedance is given by

$$r_{0,PD} = \frac{\Delta v_x}{\Delta i_x} = \frac{\Delta v_x}{\Delta i_1 + \Delta i_2} \tag{14}$$

The small signal current Δi_1 drops across the effective impedance $(r_{ds,MP8}||r_{ds,MN7})$ producing voltage Δv_{GN} which is translated to Δi_2 given by

$$\Delta i_2 = gm_{MN10} * \Delta v_{GN} \cong gm_{MN10} * \Delta i_1 * \left(r_{ds,MP8}||r_{ds,MN7}\right) \tag{15}$$

Using (14) and (15) and substituting $\Delta i_1 = gm_{MP8} * \Delta v_x$, we get

$$r_{0,PD} \cong \frac{1}{gm_{MP8} * gm_{MN10} * (r_{ds,MP8}||r_{ds,MN7})} \tag{16}$$

reducing the effective output impedance by a factor of loop gain given by $A_{PD} = gm_{MN10} * (r_{ds,MP8}||r_{ds,MN7})$. At steady state, gate voltage of MN10 is held at a threshold voltage lower than V_{BCG} and it conducts approximately 20 nA of drain-source current as shown in Fig. 4.7.

Since $r_{0,PU}$ is reduced by using the cascoded flipped voltage follower approach, P_{PU2} is pushed to a higher frequency even at light bias current conditions. The effective impedance looking-in at the drain of MP8 is reduced due to the low impedance of MN9 $\left(\frac{1}{gm_{MN9}}\right)$. This accompanied with the low equivalent parasitic capacitance $\left(C_{par}\right)$ at this node, ensure that P_{PU3} is at a much higher frequency. Therefore, the entire PU loop is stabilized using C_1 (= 1 pF), which is connected to the gate of MP9 making P_{PU1} the dominant pole. P_{PU2} and P_{PU3} remain beyond the PU loop unity gain bandwidth (UGB) even at light bias current condition providing a minimum phase margin of 45º across all load conditions. C_2 (= 1 pF) acts as a glitch filter capacitor to keep the gate voltage of MN9 constant during large signal variations at its drain and source nodes. The PD loop gain is weak compared to PU loop in normal operation and is dominant only during I_{LOAD} step

down. It is naturally stabilized with the gate capacitance of MNP. As the variable biasing current I_{HYB1} increases with I_{LOAD}, the output impedance of the buffer is reduced further and pushes P_{GATE} to higher frequency.

The entire two stage error amplifier is powered by a cross coupled voltage doubler charge pump in order to maintain a low dropout voltage for the LDO. However, variable I_{HYB1} which biases the error amplifier, modulates the current drawn from the charge pump with I_{LOAD} and ultimately, changing its 2x output voltage. In order to maintain a constant output voltage of $\approx 2V_{DD}$, the charge pump clock frequency (F_{CLK}) is modulated to counteract its load current variations. A current tunable low power relaxation oscillator is proposed to generate the charge pump control clocks.

4.4. Charge-pump Voltage Doubler

Fig. 4.9 shows the employed cross-couple voltage doubler charge-pump [24]. It uses non-overlapping clock phases and two inverters INV1 and INV2 to drive two charging capacitors (C_{CH}). Due to the combined effect of NMOS switches MN1 and MN2 along with the inverters, the node voltages V_1 and V_2 swing between V_{IN} and $2 * V_{IN}$. This higher voltage in-turn drives the NMOS switches such that their on-resistance is low. This charge is then transferred onto storage capacitance C_{ST} in every clock phase and maintains the output voltage of the charge-pump close to $2 * V_{IN}$. As noted earlier, the error amplifier which is biased by HBCG circuit, is powered by this charge-pump to maintain low dropout voltage for this NMOS LDO. However, bias current scaling of the error amplifier means that the overall current drawn from the charge-pump, scales with I_{LOAD}. In order to ensure that output voltage ripple is kept low across all load current conditions, the clock frequency

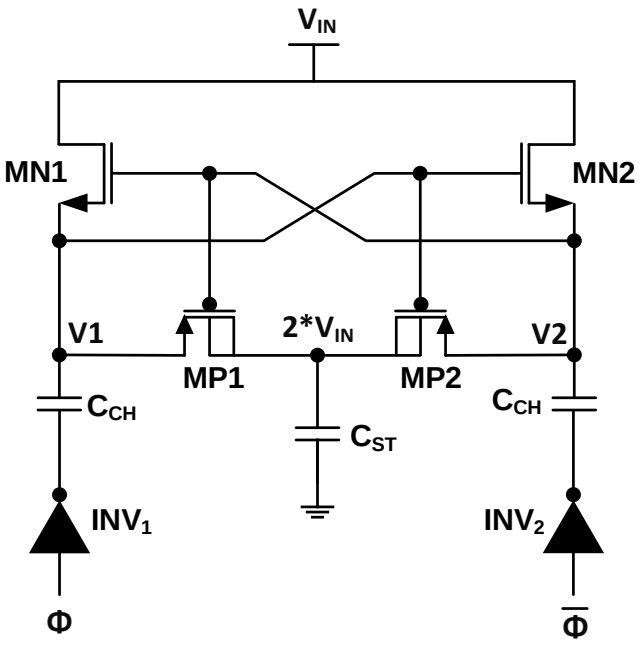


Figure 4.9: Voltage doubler charge-pump.

needs to be scaled linearly with I_{LOAD}. Therefore, a current controlled oscillator with scalable clock frequency is necessary to generate the control clocks for this charge-pump. Moreover, both C_{CH} and C_{ST} are sized slightly higher to be 8pF each to maintain low ripple voltage across all conditions.

CHAPTER 5

ULTRA-LOW POWER RELAXATION OSCILLATOR

As noted at the end of the previous chapter, the charge-pump needs to operate at a dynamic frequency to ensure low ripple at its output while powering the bias current scalable error amplifier. A relaxation oscillator using a fixed current source to charge-up a capacitor, which in turn decides the clock frequency is commonly used in integrated applications. Moreover, scaling the bias current of relaxation oscillator naturally scales its frequency linearly. Therefore, relaxation oscillator would be an ideal fit for this NMOS LDO. However, steady current consumption and switching losses in such an oscillator, have to be minimized to keep its contribution to the overall I_Q to a minimum which presents an opportunity for innovation.

A typical relaxation oscillator architecture is shown in Fig. 5.1. A bias current (I_{BIAS}) charges the capacitor (C) until its voltage (V_C) exceeds a reference voltage (V_{REF}) at which the comparator momentarily changes its output state to logic high to discharge the capacitor. As soon as the capacitor is discharged, the comparator outputs a logic low and the same sequence repeats periodically to produce an output clock. The approximate output clock frequency (F_{CLK}) of this oscillator is given by

$$F_{CLK} \cong \frac{I_{BIAS}}{2C * V_{REF}} \tag{17}$$

revealing that it is directly proportional to bias current. Although a preferred option for low power clock generation, the major limitation for nano-power operation of this circuit comes from the power consumption in comparator. This comparator typically consists of just a Schmitt Trigger or an OTA followed by a Schmitt Trigger. The long charging time of the

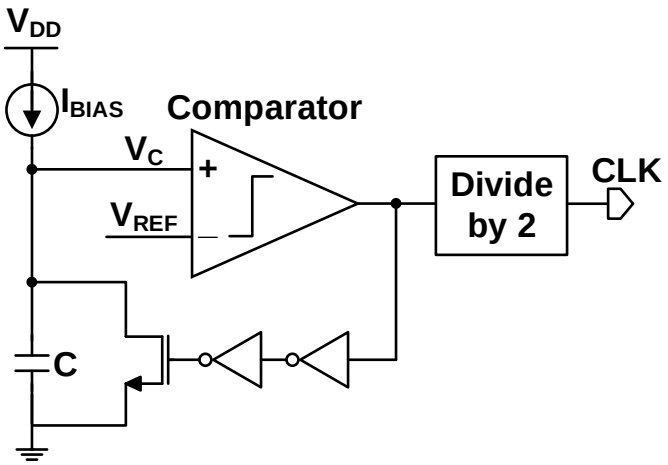


Figure 5.1: Block diagram of typical relaxation oscillator.

capacitor due to small I_{BIAS} results in higher switching losses and the OTA if used, consumes steady DC power. [22] presents the use of current comparator instead of OTA. The oscillator uses equal bias currents for generation of reference voltage and for capacitor charging and claims lower power consumption due to reduced number of current-conducting branches.

In this dissertation, a very low-power relaxation oscillator (LPRO) that does not use an OTA or an additional reference generator is proposed for charge-pump clock generation. Instead it uses the available external reference voltage and a fully digital current comparator for ultra-low power operation. The response time of this current comparator is proportional to the input current [23] which directly benefits the frequency scalability of the oscillator with its bias current.

Fig. 5.2 shows the overall schematic of the proposed LPRO circuit. The second output from HBCG circuit (I_{HYB2}) acts as the charging current. An NMOS switch MN3 is placed in between current source I_{HYB2} and the capacitor (C_S) with its gate controlled by V_{REF}. A

T-filter is placed in between the external reference voltage (V_{BG}) and V_{REF} to avoid switching noise coupling onto V_{BG}. Initially, the capacitor voltage V_C and therefore the drain voltage of MN3 (V_D) are at zero after the previous discharge cycle. At this state, output of inverter I1 in the current comparator is at logic high while the output of I2 is at logic low due to which transistor MP1 and MN1 are on and MP2 and MN2 are off. As I_{HYB2} charges C_S, V_C increases linearly. This pushes MN3 into sub-threshold region where its drain – source current is given by

$$I_{DS,MN3} \propto e^{\left(\frac{V_{GS}}{\eta V_t}\right)}\left(1 - e^{-\left(\frac{V_{DS}}{V_t}\right)}\right) \tag{18}$$

where $V_t = \frac{kT}{q} \approx 26mV$ at T = 27ºC and η is a process constant. As V_C increases further, both V_{GS} and V_{DS} of MN3 reduces ensuring $e^{\left(\frac{V_{GS}}{\eta V_t}\right)} \to 0$ and $\left(1 - e^{-\left(\frac{V_{DS}}{V_t}\right)}\right) \to 0$ thereby

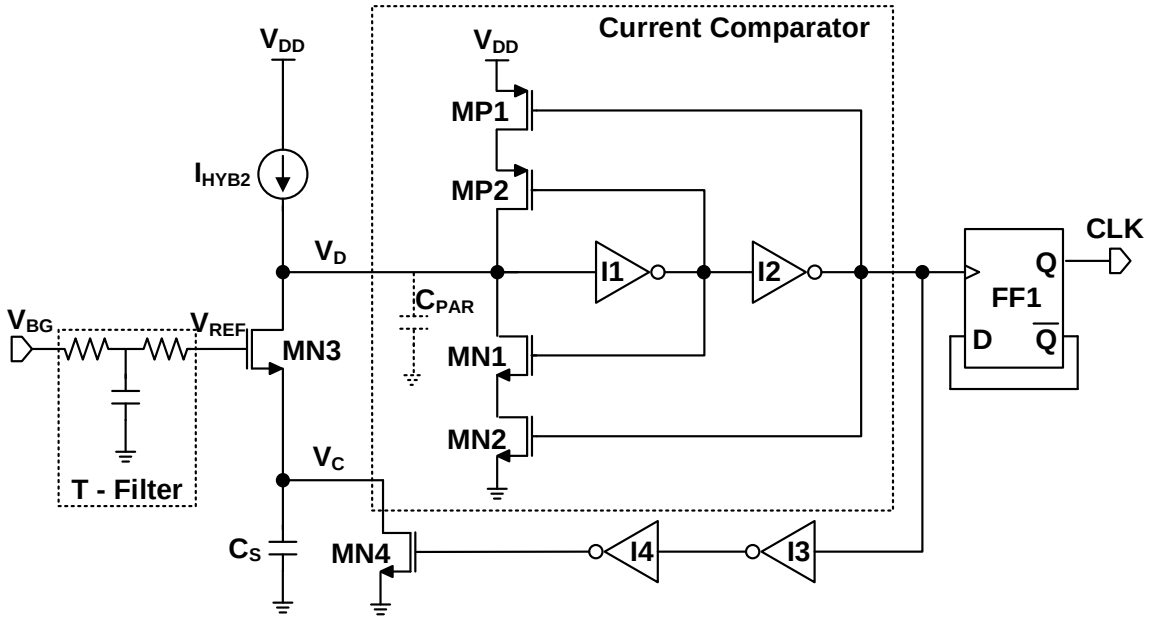


Figure 5.2: Proposed low power relaxation oscillator (LPRO) with current comparator and NMOS switch.

exponentially reducing $I_{DS,MN3}$. The difference current $\left(I_{HYB2} - I_{DS,MN3}\right)$ increases exponentially and charges the small parasitic input capacitance C_{PAR}. Therefore V_D increases exponentially from zero and output of I1 changes to logic low turning on MP2. However, I2 is designed to be weak so that its output transition to logic high happens after a small delay. During this momentary period, both MP1 and MP2 are on and quickly charge C_{PAR} such that V_D shoots up instantaneously and speed-up the switching activity even for very low values of I_{HYB2}. I3 and I4 buffer the output of I2 to discharge C_S through switch MN4. As V_C drops, MN3 turns on. MN3 and MN4 along with the regenerative feedback of MN1 and MN2 discharges C_{PAR} and V_D is pulled down to zero. This cycle repeats to produce a periodic clock whose output duty cycle error is corrected by using a clock divider FF1 to obtain the output clock. Instead of current mode, the entire comparator can be analyzed in voltage mode similar to a Schmitt trigger circuit and can be considered as a voltage mode comparator with threshold voltage determined by the device sizing. The effective clock frequency of the output clock is given by

$$F_{CLK} \cong \frac{I_{HYB2}}{2C_S * (V_{BG} - V_{THN})} \tag{19}$$

Since I_{HYB2} changes with I_{LOAD}, the clock frequency also changes proportionally to generate a load current dependent frequency as required by the dynamic frequency charge-pump.

Fig. 5.3 shows a comparison between the simulated transient capacitor voltage and supply current profiles for different types of oscillator. Even in case of an oscillator with Schmitt trigger, the effective area under the supply current curve is reduced when a switch is introduced in between the capacitor and bias current. This is reduced further by

introduction of the fast switching current comparator as in the case of LPRO. It can be seen that the switching time is cut down significantly by the addition of the switch. Moreover, during the entire charging operation, the current comparator only sees a max voltage of around 400mV which keeps the shoot-through current in the inverter I1 to a very minimal level. Since, the transition from 400mV to the trip point of the comparator is very quick, the impact of variation in the comparator trip point, does not impact the frequency of the oscillator reducing the overall variation of the clock frequency across PVT.

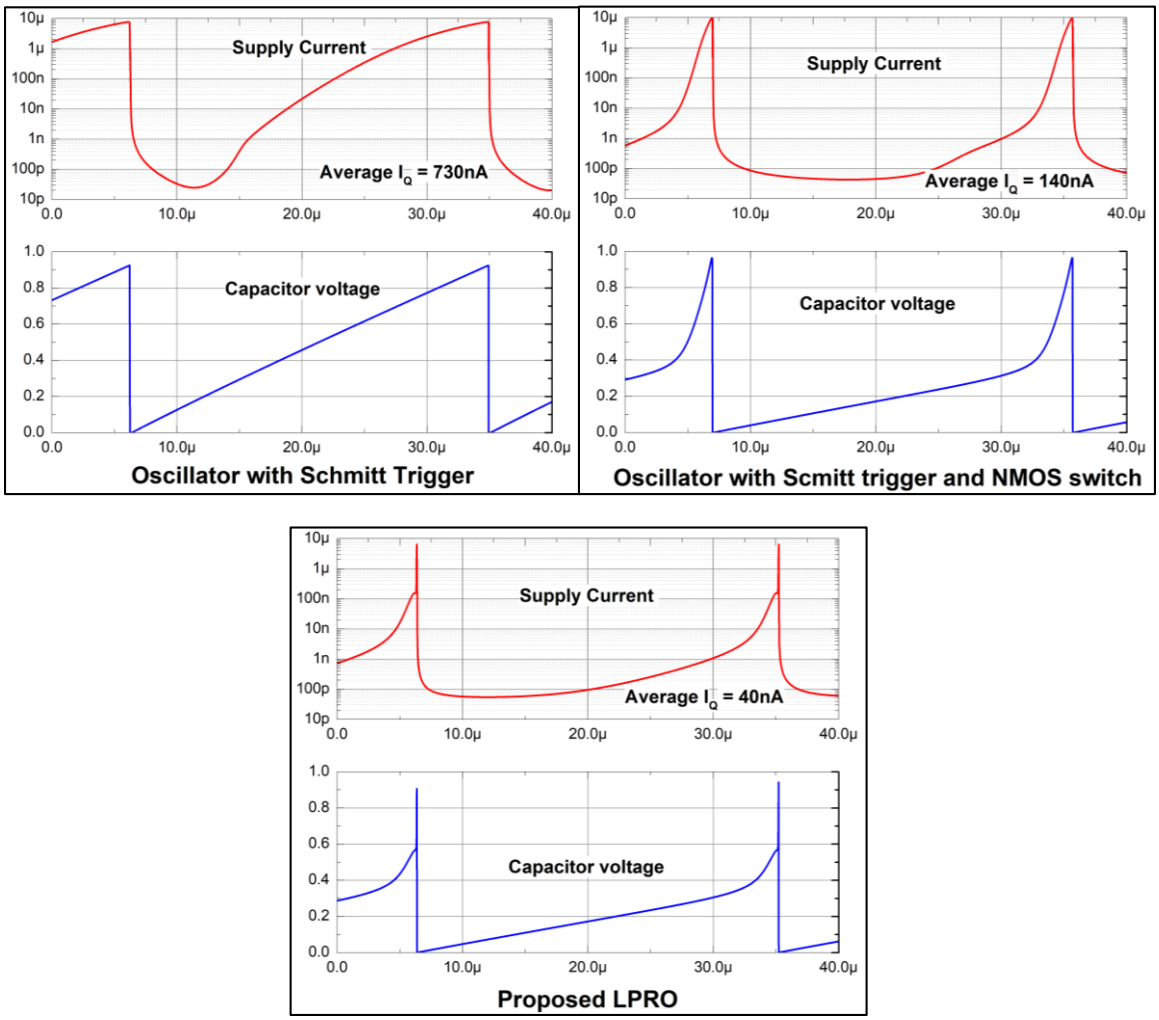


Figure 5.3: Comparison of the transient profile of supply current and capacitor voltage for the proposed LPRO with other architectures.

The average I_Q of the proposed LPRO is only 40 nA for an output frequency of 22 kHz which translates to an oscillator figure-of-merit of only 2.7 nW/kHz for a supply voltage case of 1.5 V. Monte-Carlo simulation results with N = 100 samples for the output frequency and average I_Q of the LPRO are captured in Fig. 5.4 at I_{LOAD} = 0. A 3σ variation of ±10 nA is a negligible variation when compared to the overall I_Q of the LDO. The 3σ frequency variation of about ±8kHz does not impact the charge-pump output ripple as the storage capacitors are slightly oversized to counteract this variation.

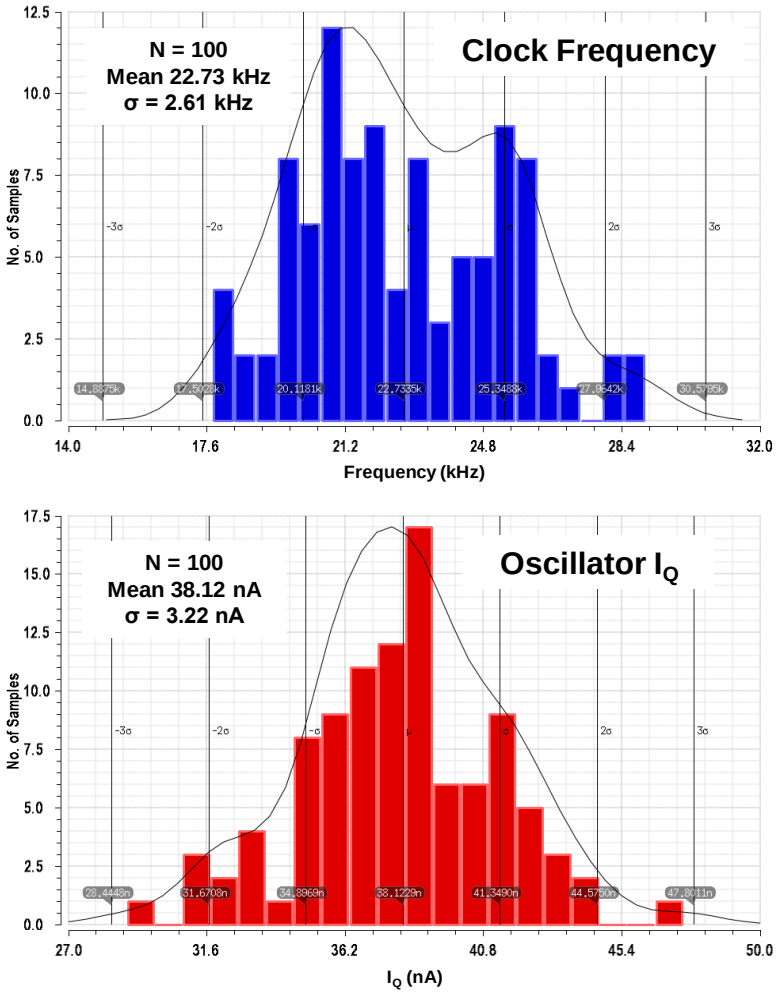


Figure 5.4: Histogram of clock frequency and average I_Q of the proposed LPRO for MonteCarlo simulation (N=100).

It is important to note that both I_{HYB1} and I_{HYB2}, generated from the HBCG circuit, scale-up during a load transient event due to dynamic biasing loop. Due to increase in I_{HYB1}, the error amplifier draws more current from the charge-pump momentarily due to increased bias current. However, since I_{HYB2} also increases, F_{CLK} increases with it and therefore the output ripple of the charge-pump is not increased during a load transient event.

CHAPTER 6

SWITCHED CAPACITOR POLE TRACKING COMPENSATION

The stability of this LDO is determined by the location of 3 distinctive poles: the LDO output pole P_{OUT}, amplifier output pole P_{AMP} and the pass device gate pole P_{GATE}. Since the NMOS pass device acts like a source follower, the output impedance of the LDO is given by

$$R_{OUT} \cong \frac{1}{g_{m,MNP}} || R_{LOAD} \tag{20}$$

where R_{LOAD} is the load current equivalent resistance connected at the output of the LDO. Thus P_{OUT} is given by

$$P_{OUT} \cong \frac{1}{2\pi \left(\frac{1}{g_{m,MNP}} || R_{LOAD} \right) C_{LOAD}} \tag{21}$$

P_{AMP} is given in (9) and P_{GATE} is obtained by using (13) and parasitic pass device gate capacitance C_{GATE} as

$$P_{GATE} \cong \frac{1}{2\pi (gm_{MP8} * gm_{MP9})(r_{ds,MP7} || r_{ds,MN9}) C_{GATE}} \tag{22}$$

P_{OUT} changes with I_{LOAD} and due to adaptive biasing, P_{AMP}, P_{GATE} and the loop UGB also change with I_{LOAD}. Fig. 6.1 shows the typical movement of these poles with I_{LOAD}. The proposed buffer design makes sure that P_{GATE} is always beyond the loop UGB and hence does not influence the overall loop stability. At zero to light load currents (I_{LOAD1}), P_{OUT} is at a very low frequency (~1 Hz) and is very close to P_{AMP} (~10 Hz). As I_{LOAD} increases to about 1 mA (I_{LOAD2}), P_{OUT} drastically shifts to higher frequency. Due to very minor increment in bias current, P_{AMP} also moves slightly. Hereafter, as the I_{LOAD} increases, P_{OUT}

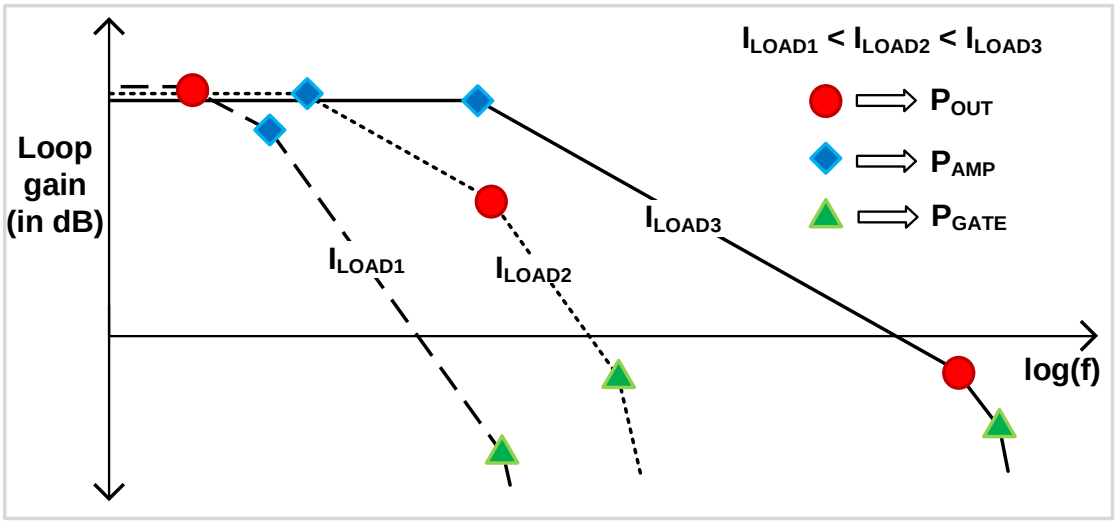


Figure 6.1: LDO pole locations and their movement with increasing load current.

shifts to higher frequency eventually moving outside the UGB for close to maximum I_{LOAD} conditions (I_{LOAD3}). P_{AMP} also shifts to higher frequency due to proportional increase in bias current thereby increasing the loop UGB. Closely spaced low frequency poles at light I_{LOAD} and constantly frequency shifting poles with increase in I_{LOAD} result in challenging considerations for the compensation scheme.

6.1. Previously presented LDO compensation schemes

Current buffer compensation or Ahuja compensation as presented in [6] is very effective in pole splitting where an indirect miller capacitor C_C is used as shown in Fig. 6.2. This capacitance provides pole-splitting by pushing out P_{OUT} and pushing in P_{AMP} in frequency. This separation provides a single pole response for the loop and achieves a high phase margin as long as P_{GATE} is maintained out of the loop UGB for all conditions. This technique can achieve stability with a relatively small sized C_C as long as the output pole location is at a higher frequency ($\geq 1kHz$). However, in this case, since the two poles of interest are at very low frequency (1Hz to 10Hz), an unreasonably high compensation

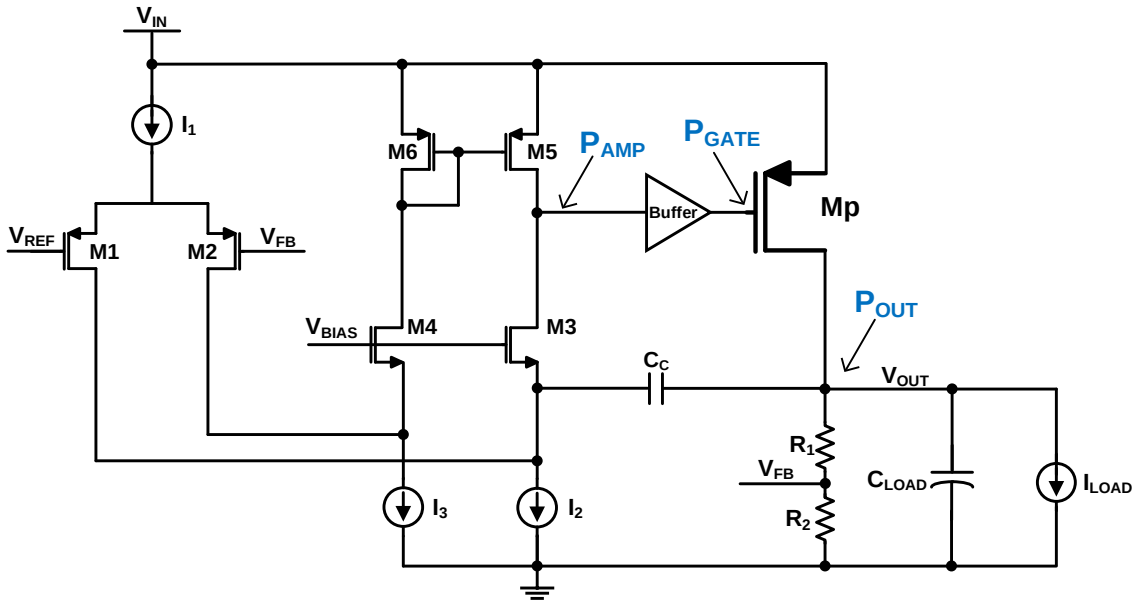


Figure 6.2: Current buffer compensation scheme presented in [6].

capacitance is required for pole splitting, which results in a huge area penalty for integration and therefore is ineffective for this design. The single miller compensation technique presented in [25] uses pole-splitting and feed-forward techniques to achieve stability in 3-stage amplifiers which can be used as the error amplifier in LDOs. Although stability is achieved by using a single miller capacitance, the overall I_Q consumption of the error amplifier is close to 200 µA which is prohibitively high for this application.

An active-frequency compensation scheme is presented in [26] to minimize the value of the required compensation capacitance by using current amplification method. Instead of a regular load current mirror, an amplifier is used to boost the effective current and therefore pushing the introduced zero to a very low frequency. However, the current consumption in such an additional stage adds to the overall LDO I_Q and is unfavorable. A weighted current feedback technique along with miller compensation is presented in [27] where a weighted function of the load current is used for smart management of the output

impedance as well as the gain from the inter-gain stage. This technique claims to avoid any right-half plane pole and pushes the left-half plane non-dominant complex pole pair to a higher frequency. However, it is suitable only for load capacitance up-to 10 nF and is not applicable for output capacitor stabilized LDOs. [28] presents a signal-current feedforward and amplification technique called dominant-pole substitution is used to introduce an ultralow-frequency zero to cancel the dominant pole, while a higher frequency pole substitutes in and becomes the new dominant pole. In doing so, a triple input error amplifier is used and the overall I_Q of the LDO is 135 µA which is significantly higher than the target I_Q consumption for this research.

Pole tracking compensation is presented in [29] - [30] where the movement of P_{OUT} is tracked and used for compensation. Fig. 6.3 shows the details of the scheme implemented

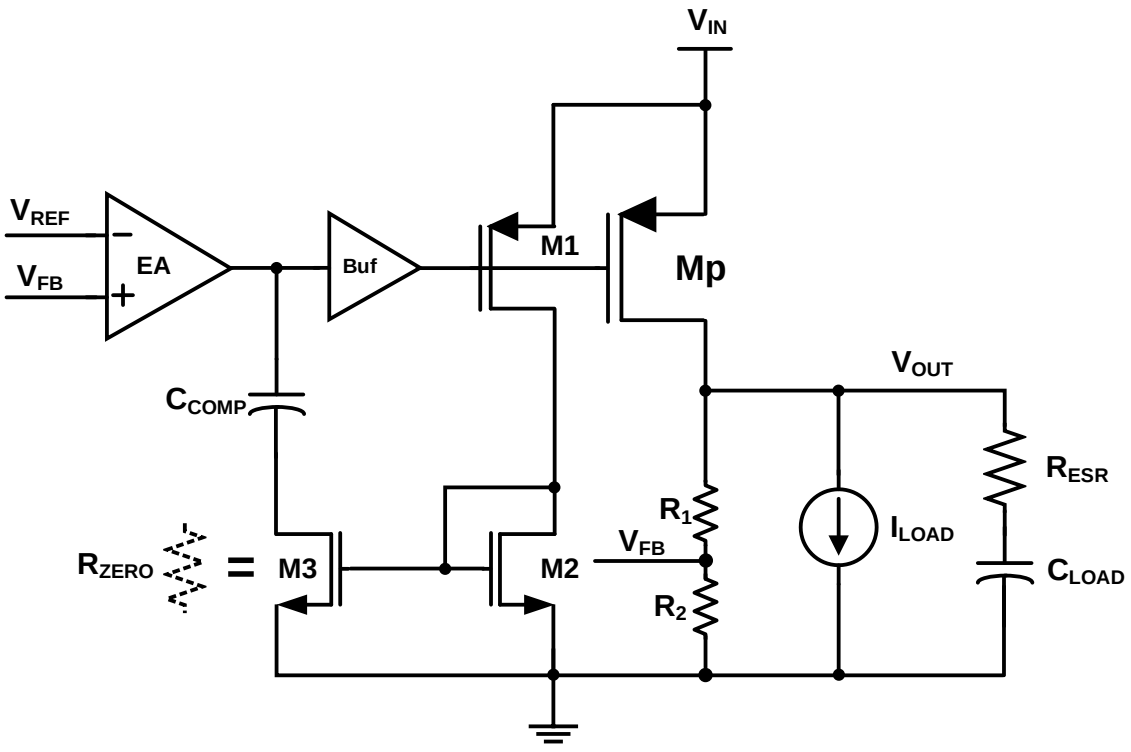


Figure 6.3: A variant of pole-zero tracking compensation scheme presented in [29].

in [29]. A zero is introduced by using a MOS resistor (M3) along with compensation capacitance (C_{COMP}) and is given by

$$s_{zero} = \frac{1}{Resistance(M3) * C_{COMP}} = \frac{1}{R_{ZERO} * C_{COMP}} \quad (23)$$

The location of s_{zero} is controlled by modulating R_{ZERO} with I_{LOAD} using a load current mirror M1 and M2. Therefore as P_{OUT} varies with I_{LOAD}, s_{zero} also shift proportionally, thereby providing phase boost for all load current conditions. Although the zero tracks P_{OUT}, the variation in the MOS resistance can be significant especially at light load current conditions due to poor sub-threshold current matching and process variations. This variation can impact the overall stability of the LDO. In [30], a distributed pass device network consisting of 3 stages is used to obtain smooth pole tracking. Incremental sizing is used to ensure smooth turn-on and turn-off sequence of these pass transistors, while ensuring stable operation during load transients. However, the minimum value of I_{LOAD} for this LDO is limited to 100 µA which can pose a limitation on its use case for a I_Q application. Moreover the overall I_Q of the LDO is also 100 µA and is on the higher side.

For a compensation scheme to be applicable for this low I_Q LDO, it needs to meet the following criteria

i. Ensure good LDO stability at all load current conditions even at $I_{LOAD} = 0$ when the pole locations are at a very low frequency
ii. Should not contribute significantly to the overall I_Q
iii. Area and cost efficient
iv. Should not depend on the output ESR zero for stability

These conditions present challenging considerations for compensating this LDO.

6.2. Proposed switched-capacitor pole tracking (SCPT) compensation

In this research, a P_{OUT} tracking zero is introduced to provide a phase boost and ensure stability. A zero can be introduced in the loop by using a resistor R_Z as shown in Fig. 6.4. However with C_{AMP} = 2.5pF, in order to introduce a zero at around UGB for no-load, the required resistance can be as high as 100 MΩ which results in large area penalty. Moreover, R_Z needs to track P_{OUT} and hence needs to be variable resistor. This is achieved using a novel switched capacitor pole tracking (SCPT) compensation scheme where a switched capacitor resistor (R_{SC}) is placed instead of R_Z to introduce a zero (Z_{SC}). The same oscillator clock is used to control R_{SC} with its effective value given by

$$R_{SC} = \frac{1}{F_{CLK} * C_{SC}} \tag{24}$$

where C_{SC} is the capacitance used to implement R_{SC} and the SCPT zero Z_{SC} is given by

$$Z_{SC} = \frac{F_{CLK} * C_{SC}}{2\pi C_{AMP}} \tag{25}$$

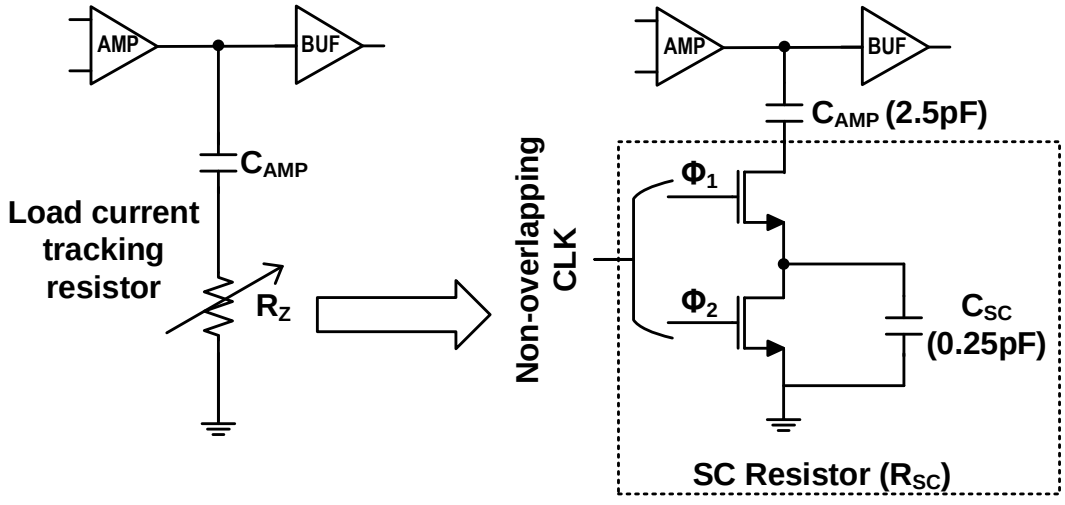


Figure 6.4: Proposed switched capacitor pole tracking (SCPT) compensation scheme.

However, from (19) we know that $F_{CLK} \propto I_{HYB1}$ and due to adaptive biasing we have $I_{HYB1} \propto I_{LOAD}$. Therefore from (25) we have

$$Z_{SC} \propto I_{LOAD} \tag{26}$$

Thus, Z_{SC} tracks P_{OUT} which is proportional to I_{LOAD} and provides a phase boost for the entire range of load currents. A small capacitance C_{SC} = 0.25 pF is used to implement R_{SC}, providing an area efficient solution. Non-overlapping clocks control the switches used in this SC resistor. Fig. 6.5 shows the simulated gain and phase response of the LDO loop obtained using periodic steady state (PSS) followed by periodic AC (PAC) simulation for different load current values for a load capacitance of 1 µF. The impact of hybrid biasing can be seen as the UGB shifts with load current. The phase margin is always above 30º and demonstrates the effectiveness of the SCPT compensation. The 3σ variation of ±8 kHz in oscillator frequency might cause a minor change in the actual value of the phase margin but does not affect the stability. This scheme ensures that the LDO is stable even for

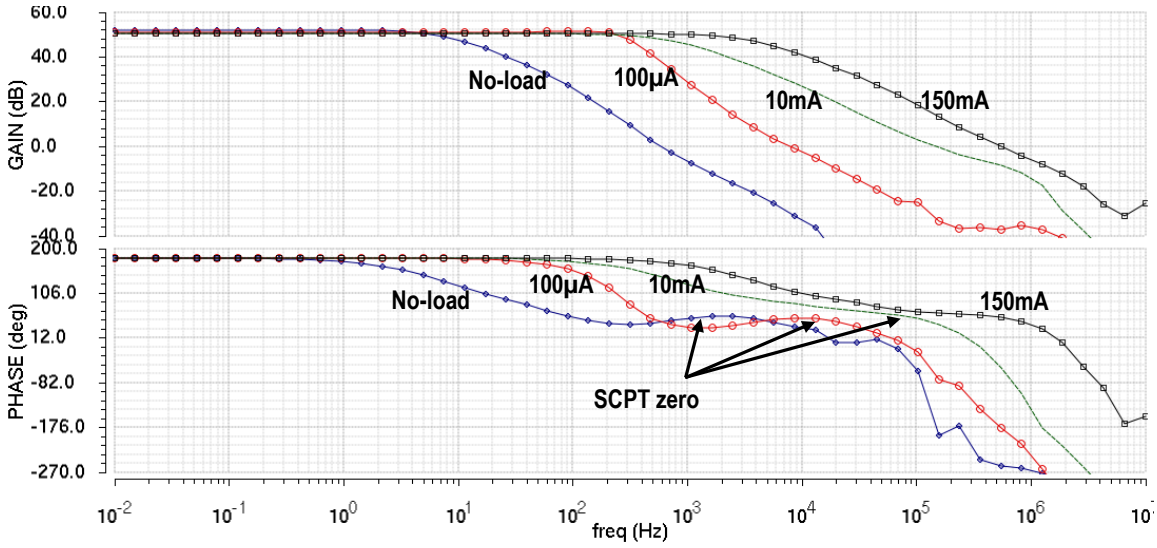


Figure 6.5: LDO loop gain and phase response with the pole tracking SCPT zero movement highlighted.

increments in load capacitance up-to 47 µF. The zero introduced by SCPT compensation also increases the UGB of the loop thereby improving its transient response. It is to be noted that in this compensation scheme, the clock frequency is always at least 50 times the loop UGB ($F_{CLK} \geq$ 50*UGB) for all load current conditions. Therefore, any pole (P_{par}) formed due to R_{SC} and net parasitic capacitance (C_{par}) attached to it, given by

$$P_{par} = \frac{1}{R_z * C_{par}} = \frac{F_{CLK} * C_{SC}}{C_{par}} \tag{27}$$

will always be much beyond the loop UGB and does not affect the stability of the LDO.

CHAPTER 7

MEASUREMENT RESULTS

This LDO is fabricated in a 0.25µm single-poly four-metal CMOS process. Fig. 7.1 shows the die micrograph. The core area is 400 µm x 260 µm excluding the test pads and the additional circuitry used for programming and testing. This LDO uses an external voltage reference. Although bandgap reference is not integrated within the LDO, sample-and-hold approaches presented in [31] can be used to reduce its current consumption to few nano-Amperes and therefore its contribution to the overall I_Q of the LDO can be made negligible. The LDO has a digitally programmable output voltage range of 1.0 V to 3.0 V and a maximum output current capability of 150 mA at a dropout voltage of 240 mV. MCP2210 serial peripheral interface (SPI) module is used for digital programmability of

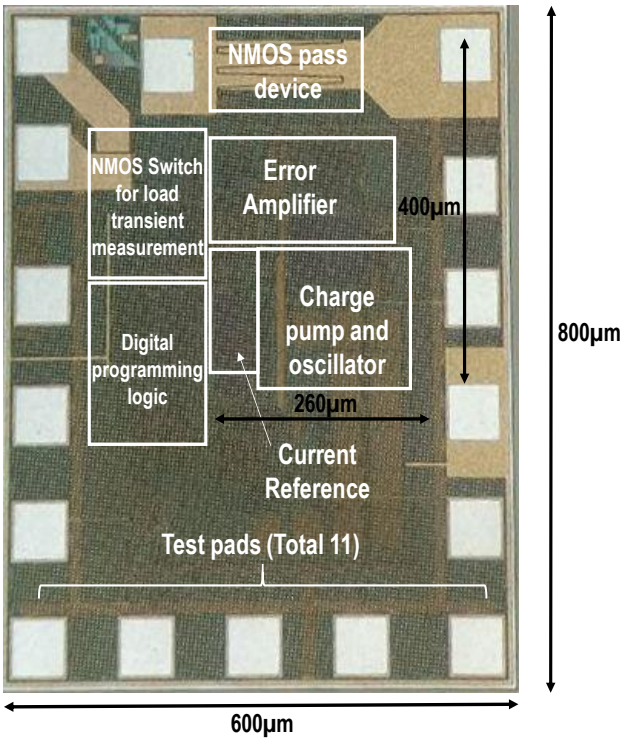


Figure 7.1: Die Micrograph.

the LDO by sending data into an internal shift register network and latching it onto shadow latches. The load capacitance range is from 1 µF to 47 µF. A single bond-wire is used to bond the output of the LDO to the package pin and impacts the DC load regulation which is 25 mV as I_{LOAD} increases from 0 to 150 mA.

Fig. 7.2 shows the PCB test-board used for characterizing this LDO. Low-ESR ceramic capacitance soldered close to the LDO is used as the C_{LOAD}. A fast switching NMOS power FET is used for transient response. A voltage buffer Opamp with 200 mA current capability is used for PSR analysis. The actual measurement setup is shown in Fig. 7.3. A high accuracy source-measure unit (SMU) is used to measure the I_Q of the LDO at various load current conditions. A signal generator provides the clock for switching the power MOS during load transient measurements. The SPI module is programmed using a data transfer software. This data is then converted into Serial_Data and Serial_Clk for programming the internal shift register. The external reference is obtained by filtering a

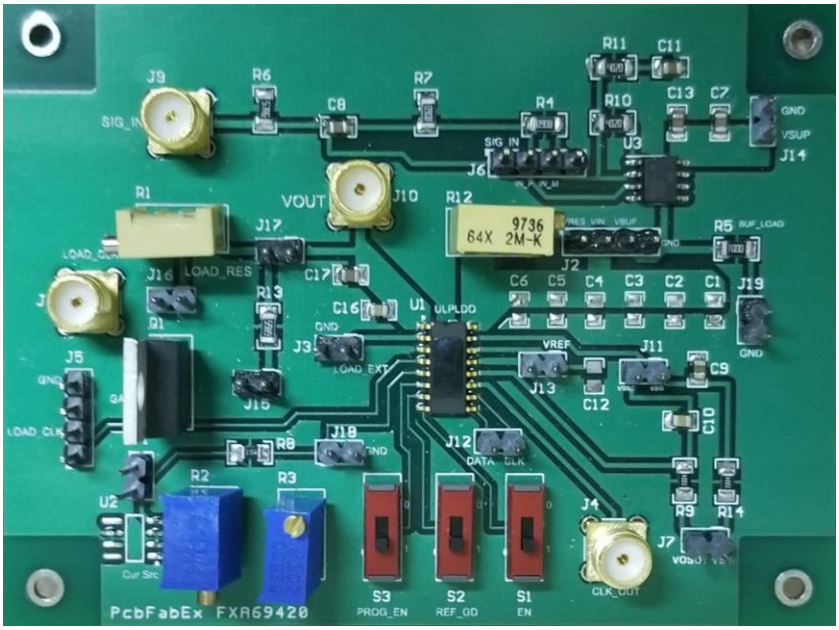


Figure 7.2: PCB for LDO performance measurement.

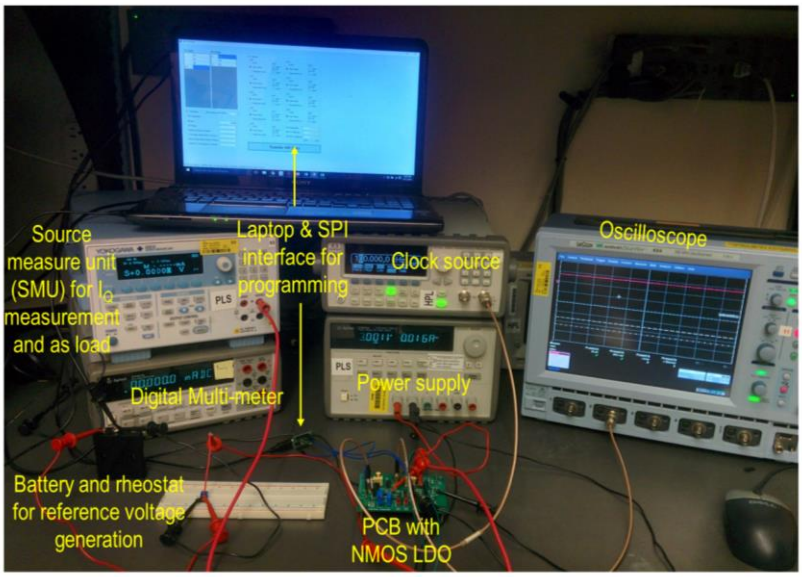


Figure 7.3: Measurement setup for the proposed LDO along with the PCB.

battery powered resistor divider output (0.8 V) with an on-board RC filter for low noise reference which is fed directly to the LDO.

Table I shows the simulated block level no-load I_Q consumption break-down of the LDO. In order to ensure good transient response, a major portion of the overall I_Q is alloted

Table I: Simulated block-level no-load I_Q break-down

Block	**I_Q (nA)**
Error amplifier with buffer	400
Hybrid bias-current generator (HBCG)	100
Low power relaxation oscillator (LPRO)	40
Reference scaling amplifier	40
Programmable resistor divider	100
Charge-pump	480
Constant-gm current reference	40
Total	**1200**

to the error amplifier and associated charge-pump. The programmable resistor divider which is critical for output voltage programmability consumes 100 nA which is significant portion of the overall budget. An internal constant-gm current reference is used to generate the bias current of 20 nA going into the HBCG circuit. This current reference consumes a total of 40 nA.

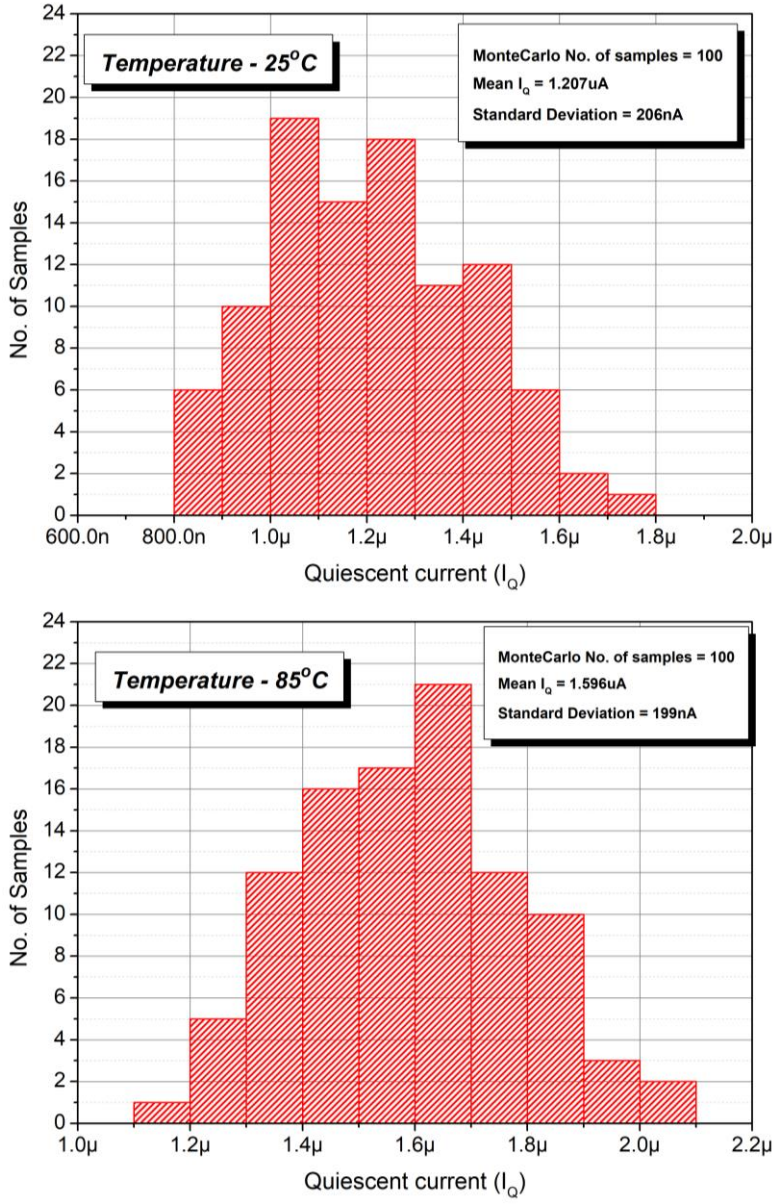


Figure 7.4: Simulated no-load I_Q using MonteCarlo 50 samples at 25ºC and 85 ºC.

Fig. 7.4 shows MonteCarlo simulation results for the overall I_Q of the LDO for 25º C and 85º C with process variation and device mismatch. The standard deviation σ = 200 nA results in a 3σ variation of only 600 nA. This variation can be further reduced by using programmability for the internal current reference. Fig. 7.5 captures the I_Q of the LDO and its current efficiency vs. I_{LOAD}. The no-load I_Q of the proposed LDO is only 1.24 µA. It stays below 2 µA for I_{LOAD} < 200 µA and is only about 5 µA even when I_{LOAD} goes up to 1 mA thereby consuming very low supply current even at light load conditions. The current efficiency is above 95% even for I_{LOAD} as low as 50 µA and is above 99% for 200 µA and above. The measured I_Q of 1.24 µA shows that the design is centered across the mean value as shown in the MonteCarlo simulation results in Fig. 7.4 and achieves a high current efficiency which is the critical feature for its applicability in always-on applications. Fig. 7.6 shows the measured I_Q of 5 different testchips along with their output undershoot

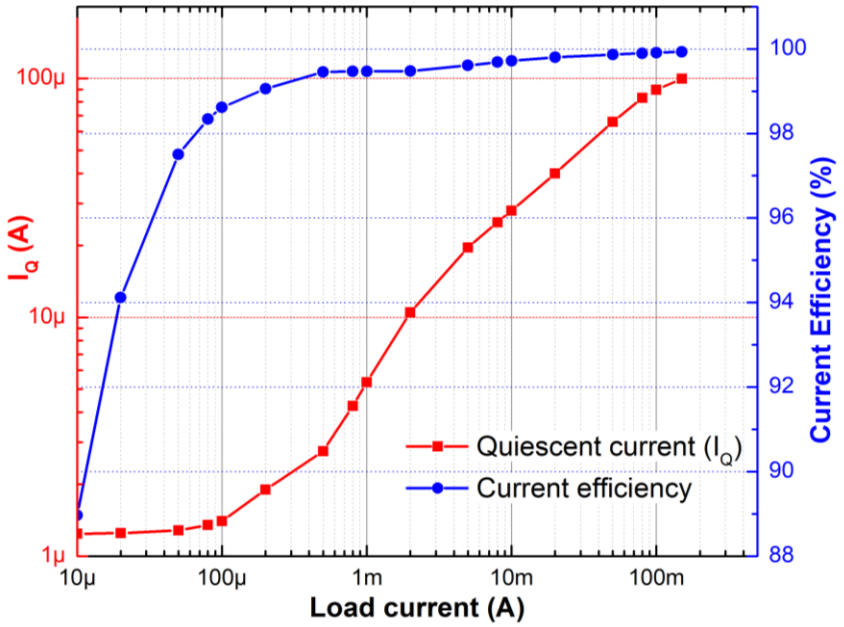


Figure 7.5: Quiescent current and current efficiency of the LDO vs. load current.

voltage for a 0 to 150 mA load current step. The results show consistency in both I_Q and undershoot voltage with less than 3% variation.

The measured load transient response for different load steps and output capacitor combinations is shown in Fig. 7.7. For C_{LOAD}= 1 µF, the undershoot and overshoot voltage for load step of 0 to 50 mA and vice-versa are 76 mV and 32 mV respectively and are 135 mV and 65 mV respectively for a load step of 0 to 150 mA after subtracting the impact of DC load regulation which is 25 mV. The output recovers to tolerable error limit of ±1% within 10 µs showing very fast transient recovery from zero to full load transient and therefore, providing another critical feature of fast transient response required in supply regulation of fast wake-up systems. Further reduction in both undershoot and overshoot voltages is observed when C_{LOAD}= 10 µF and C_{LOAD}= 47 µF, which also confirms the

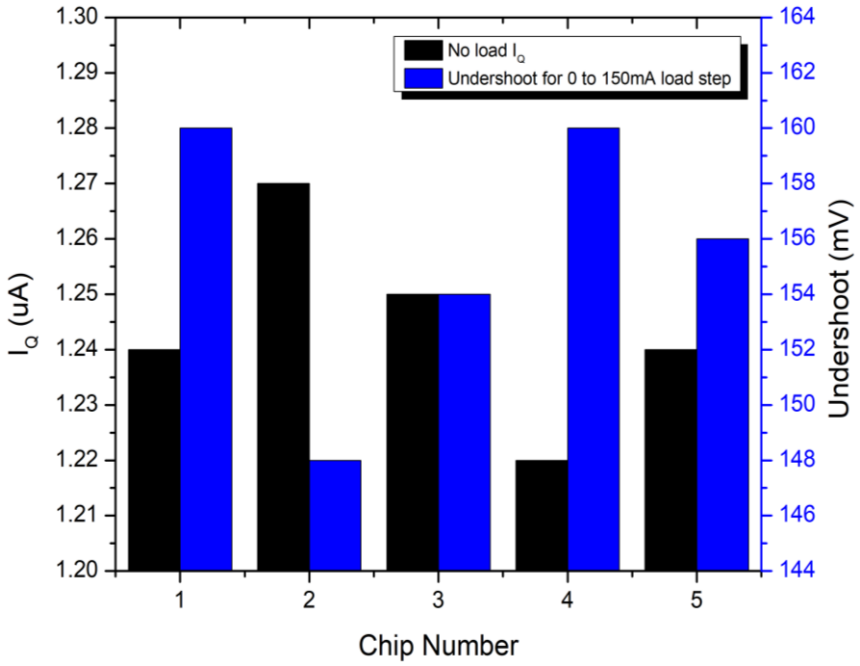


Figure 7.6: Measured no-load I_Q for 5 different chips along with the undershoot voltage for a load transient of 0mA to 150mA.

stability of the LDO at these load capacitance levels. Besides using an NMOS pass device, low overshoot/undershoot and fast recovery performance of this low I_Q LDO is only possible due to the hybrid biasing working alongside the on-demand pull-up/pull-down buffer and SCPT compensation. Although choice of NMOS pass device results in additional requirement of charge-pump and associated oscillator for ensuring low dropout voltage, improved transient response and effective usage of the oscillator for SCPT compensation scheme overpowers this limitation. The impact of output capacitor pull down

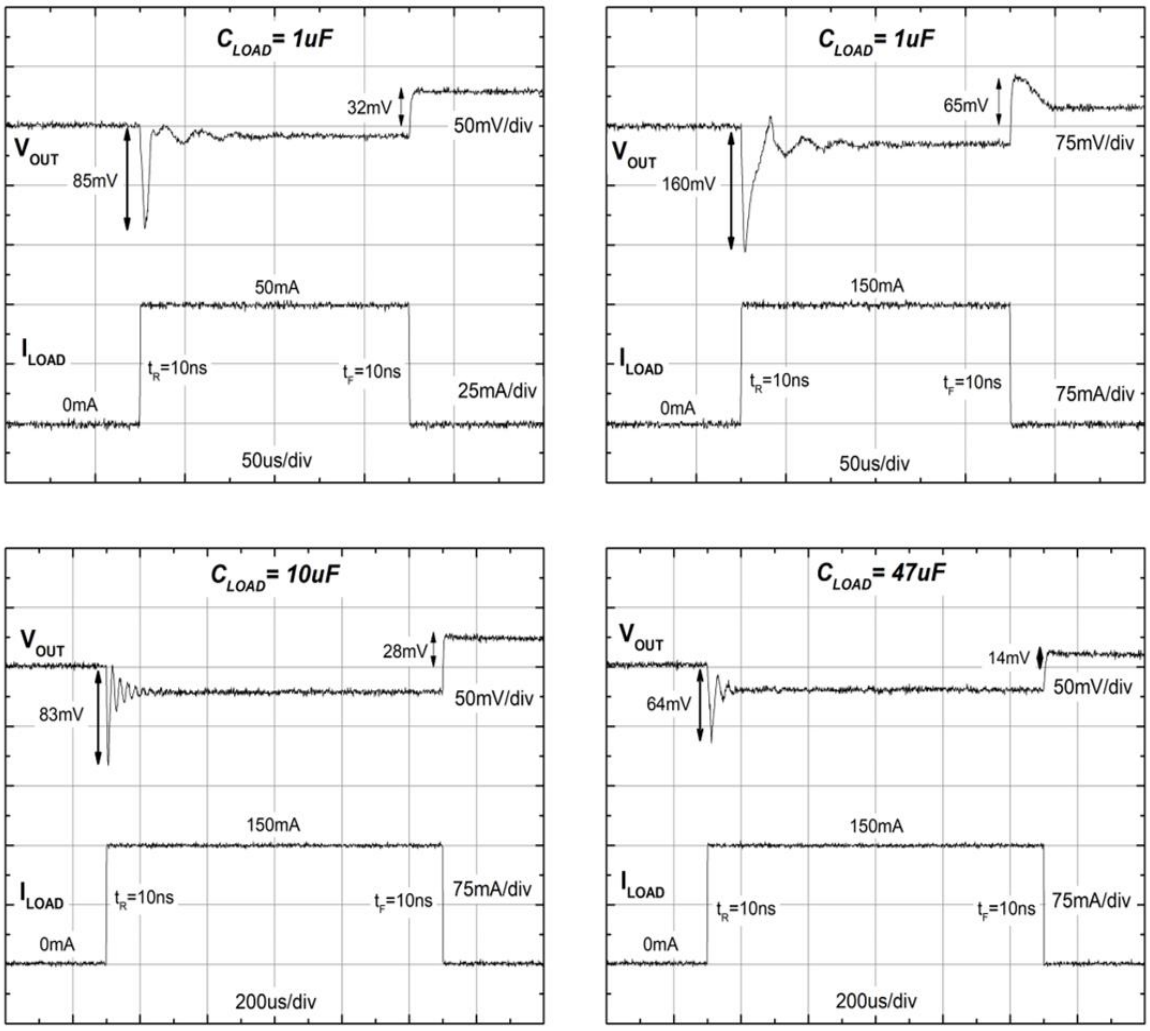


Figure 7.7: Measured load transient response of the proposed LDO for different load steps and output capacitor values.

circuit can be seen in the case of 0 to 150mA transition with C_{LOAD}= 1 µF as the high output overshoot of 65 mV is quickly discharged and brought down to a tolerable error voltage. In all other cases when the output voltage overshoot is less than 35mV, the pull down circuit does not kick-in for capacitor discharge. However the worst case voltage error is less than 3% in such cases and is negligible.

Fig. 7.8 shows the line transient response of the LDO at maximum load condition (I_{LOAD} = 150 mA) for output voltage of 1.8V. The initial step-up and step-down in the supply voltage is 0.75V and results in an undershoot of 35 mV and overshoot of 25 mV. This constitutes less than 2% error for an output voltage of 1.8V. The power supply rejection (PSR) of the LDO is shown in Fig. 7.9 at I_{LOAD}= 150 mA. The UGB improvement achieved due to hybrid biasing enables higher than 20 dB rejection for frequencies up-to 20 kHz.

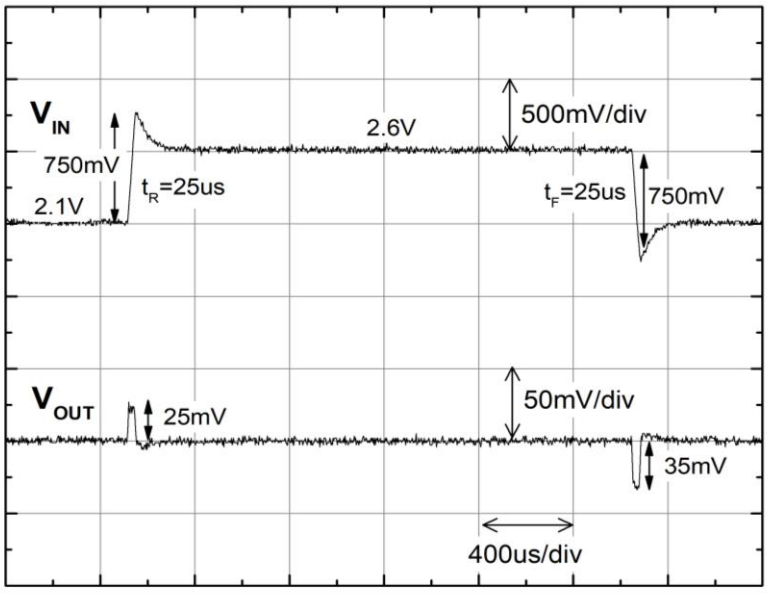


Figure 7.8: Measured line transient response of the LDO at full load current.

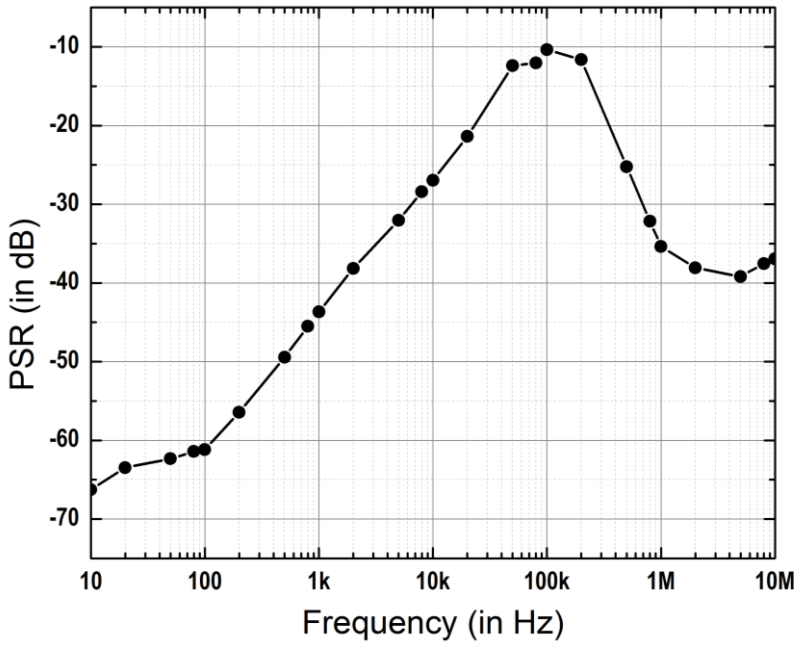


Figure 7.9: Measured power supply rejection (PSR) of the LDO at full load current.

Table II provides a comprehensive comparison of the proposed LDO with previously published work highlighting its major advantages. In comparison, this LDO has the lowest I_Q which is critical for low power consumption during stand-by and light load conditions. The SCPT compensation not only ensures stability of the LDO from zero to entire range of load current, but also for a capacitance range of 1 µF to 47 µF without depending on an external ESR zero thereby providing the widest output capacitor range. The figure of merit (FOM) defined as

$$FOM = T_R * \frac{I_Q}{I_{LOAD,MAX}} \tag{28}$$

is incorporated from [6] for a proper baseline comparison where T_R is the recovery time given by

$$T_R = \frac{C_{LOAD} * \Delta V}{I_{LOAD,MAX}} \tag{29}$$

where ΔV is the undershoot voltage. A lower FOM suggests an overall better performing LDO. The proposed LDO achieves at least 66% reduction in FOM when compared to LDOs with maximum load current capability of 100mA or above. Although [18] has a comparable no-load I_Q, its maximum load current is limited to 50 mA and it has a 2.5 times higher FOM.

Table II: Performance comparison of the proposed LDO with previously published output capacitor stabilized LDOs

Parameter	[6] 2007	[26] 2008	[32] 2009	[12] 2010	[19] 2010	[28] 2016	[18] 2017	This work
Technology (µm)	0.35	0.35	0.35	0.35	0.09	0.18	0.18	**0.25**
Area (mm^2)	0.264	0.409	0.188	0.225	0.00274	0.0245	0.028	**0.108**
Input voltage V_{IN} (V)	2.0	2.0	2.1 – 5.0	2.0	1.0	1.2 – 1.8	1.4	**1.5 – 3.3**
Output voltage V_{OUT} (V)	1.8	1.8	2.0	1.8	0.9	1.0	1.2	**1.0 – 3.0**
Max. load current (mA)	200	150	100	100	50	100	50	**150**
Dropout voltage (mV)	200	200	60	200	100	200	200	**240**
C_{LOAD} (µF)	1.0	1.0	4.7 – 10	1.0 – 10	1.0	1.0	1.0	**1.0 – 47**
ESR zero requirement	No	No	0.3Ω – 0.5Ω	0.1Ω – 0.4Ω	0.35Ω	0.35Ω	No	**No**
I_Q (µA)	20 – 340	27	40	4	9.3	135.1	1.6 – 200	**1.24 – 100**
Current efficiency @ max. load	99.5	N.A.	N.A.	99.996	N.A.	99.86	99.6	**99.93**
PSR (dB)	>45dB (0 – 20kHz)	>40dB (0 – 20kHz)	N.A.	N.A.	>54dB (0 – 100kHz)	>35dB (0 – 100kHz)	>30dB @10MHz	**>22dB (0 – 20kHz)**
Undershoot (mV)	54	65#	40#	55	6	25	24	**135**
Overshoot (mV)	15	70#	54#	25	8	~0	5	**65**
T_R (µs)	0.27	0.43*	12	0.55*	0.16*	0.25*	0.48	**0.9**
FOM (ps)	27	78*	4800	22*	74.4*	338*	18.5	**7.4**

* Calculated from the results shown by the paper

Measured for load transient from non-zero minimum value to maximum load current

CHAPTER 8

CONCLUSION AND FUTURE WORK

8.1. Conclusion

This dissertation presents an NMOS LDO with a very low I_Q of 1.24 µA for supply regulation of always-on IoT applications. It is designed in a 0.25 µm CMOS process and has a maximum output current capability of 150 mA. Hybrid bias current scaling scheme which achieves load dependent adaptive current scaling as well as fast dynamic current scaling during load transient event, is proposed to improve the bandwidth and slew rate of the LDO for fast response to load current transients. A dynamic frequency charge-pump powered, bias current scalable two-stage error amplifier is implemented for LDO regulation. The proposed on-demand pull-up/pull-down buffer ensures high slew-rate at the gate of the pass device. The dynamic frequency scheme for the charge-pump, helps to maintain very low ripple at its output voltage.

A low power relaxation oscillator with load current controlled clock frequency is proposed to generate the control clocks for the charge-pump. This oscillator consumes only 40 nA of I_Q at light load currents. A novel switched capacitor pole tracking compensation scheme is employed for LDO stability. This technique uses the already available load dependent clock frequency to achieve stability for a load capacitance range of 1 to 47 µF without the requirement of an ESR zero.

A totally current scalable approach for different blocks of the LDO, ensures fast transient response while maintaining a very-low no-load I_Q. Measurement results show that the LDO has a recovery time of less than 10 µs for zero to full load current step-up and

achieves higher than 95% current efficiency even for small load current of 50 µA. Due to its very low I_Q and highly competitive transient figure-of-merit (FOM), this LDO is highly favorable for supply regulation of battery powered, long standby time and short wake-up time IoT applications.

8.2. Future Work

In terms of the system level improvement of the LDO, the major addition would be to integrate an on-chip bandgap reference. By using the switched-RC bandgap approach presented in [31], a very low I_Q, low noise and high-PSR bandgap can be integrated onto the chip without any major change in the overall I_Q of the LDO. Additionally, features like current limit and thermal shutdown can be integrated easily to this LDO, to make it a complete standalone LDO product.

Few other improvements can be made for the existing LDO design to bring its I_Q lower without affecting its transient response. These are listed as below:

1. *Reducing the circuitry powered by charge-pump:* As can be seen from Table I, majority of the I_Q is currently consumed in the charge-pump. This is primarily due to the fact that the entire error amplifier is powered by the LDO. Any 1x amount of reduction in the load of charge-pump would result in a 2x reduction in the overall I_Q. Therefore, a low impedance, level-shifting buffer design for the driving the pass device gate can be a key area for innovation. This buffer will be the only circuit powered by charge-pump ad therefore can virtually cut down the I_Q by roughly 320 nA.
2. *Eliminate the current consumption in resistor divider:* Currently, the feedback divider in the scaling amplifier consumes roughly 8% of the overall LDO I_Q. This is a

significant portion of current budgeted just for the sake of output voltage programmability. This can be cut down by using a duty-cycled resistor divider or a capacitive divider which can bring down the current consumption from 100nA to a single digit nano-Ampere. This combined with the point above, can bring about 30% reduction in the overall I_Q of this LDO.

3. *Duty-cycling for error amplifier circuitry:* The error amplifier and the associated circuity, can themselves be duty cycled to bring down the power consumption significantly. This will push the LDO I_Q towards the regime of 100nA and below.

However, once the I_Q of the LDO is lowered down to about 100nA or below, few major challenges tend to affect the overall applicability of the LDO. The main challenges are listed below:

a. *Device leakage:* As the technology scales down, the FET leakage especially drain-source sub-threshold leakage tends to increase. This can become a noticeable portion of the overall I_Q of the LDO at nano-Ampere levels.

b. *Battery and on-board capacitor and other circuitry leakage:* The battery itself has a self-discharge current associated with it. This self – discharge current plus the on-board decoupling capacitor leakage can become a significant disadvantage at lower I_Q levels.

c. *Electromagnetic interference:* As the bias current is very low in these low I_Q LDOs, almost all of the nodes are high – impedance nodes. Therefore, any crosstalk or interference close to the LDO, can easily modulate these nodes and corrupt the performance of the LDO. This is a major drawback especially if the LDO is used in very high power transceiver applications.

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