Characterization of Thermo-Mechanical Damage

in Tin and Sintered Nano-Silver Solders

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved April 2018 by the
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ARIZONA STATE UNIVERSITY

May 2018

ABSTRACT

Increasing density of microelectronic packages, results in an increase in thermal and mechanical stresses within the various layers of the package. To accommodate the high-performance demands, the materials used in the electronic package would also require improvement. Specifically, the damage that often occurs in solders that function as die-attachment and thermal interfaces need to be addressed. This work evaluates and characterizes thermo-mechanical damage in two material systems – Electroplated Tin and Sintered Nano-Silver solder.

Tin plated electrical contacts are prone to formation of single crystalline tin whiskers which can cause short circuiting. A mechanistic model of their formation, evolution and microstructural influence is still not fully understood. In this work, growth of mechanically induced tin whiskers/hillocks is studied using *in situ* Nano-indentation and Electron Backscatter Diffraction (EBSD). Electroplated tin was indented and monitored in vacuum to study growth of hillocks without the influence of atmosphere. Thermal aging was done to study the effect of intermetallic compounds. Grain orientation of the hillocks and the plastically deformed region surrounding the indent was studied using Focused Ion Beam (FIB) lift-out technique. In addition, micropillars were milled on the surface of electroplated Sn using FIB to evaluate the yield strength and its relation to Sn grain size.

High operating temperature power electronics use wide band-gap semiconductor devices (Silicon Carbide/Gallium Nitride). The operating temperature of these devices can exceed 250°C, preventing use of traditional Sn-solders as Thermal Interface materials (TIM). At high temperature, the thermomechanical stresses can severely degrade the reliability and life of the device. In this light, new non-destructive approach is needed to understand the damage

mechanism when subjected to reliability tests such as thermal cycling. In this work, sintered nano-Silver was identified as a promising high temperature TIM. Sintered nano-Silver samples were fabricated and their shear strength was evaluated. Thermal cycling tests were conducted and damage evolution was characterized using a lab scale 3D X-ray system to periodically assess changes in the microstructure such as cracks, voids, and porosity in the TIM layer. The evolution of microstructure and the effect of cycling temperature during thermal cycling are discussed.

To my parents Alejandro and Irene

for encouraging me in every step of my life

and for teaching me to work hard for what I want.

ACKNOWLEDGMENTS

First, I would like to thank God, for life and for so many blessings.

I would also like to acknowledge my advisor, Dr. Nikhilesh Chawla for taking me into his group and providing me the opportunity to work on these projects, for his constant guidance, and support, throughout the past few years and for giving me the tools to achieve my Ph.D.

I would like to express my gratefulness toward my committee members, Dr. Jagannathan Rajagopalan, Dr. Yang Jiao, and Dr. Darrel Frear for taking time in evaluating my doctoral research and providing valuable feedback. I would like to acknowledge the financial support from the National Council of Science and Technology of Mexico (CONACyT- Consejo Nacional de Ciencia y Tecnologia) and from the Toyota Research Institute of North America (TRINA).

I would like to thank our collaborators at TRINA, Dr. Shailesh Joshi, Dr. Eric Dede and Leo Liu.

I would like to specially thank our group's Research Scientist Dr. Jason Williams for all his technical advice and support.

I would also like to express my gratitude to my family away from home, my friends in the research group: Arun, Carl, Chris, Jacob, James, Marion, Qingdong, Renu, Shashank, Somya, Sridhar, Sudhanshu, Tyler and Yongfeng. Thanks for all the moments we've shared together, you'll be forever in my heart.

And finally, I would like to thank the most important people in my life: my family. Thanks to Mom Irene and my dad Alejandro, for always believing in me, supporting me in everything I did, and for making me the person that I am today. To my sister Ale for keeping my feet in the ground, for making me a better person and for always being by my side. And, to my fiancé Antony, for all his help and patience in difficult times, for sharing my dreams and for reminding me that the best is yet to come.

TABLE OF CONTENTS

Page

LIST OF TABLES x

LIST OF FIGURES…………………………………………………………………....xi

INTRODUCTION 1

REVIEW OF RELEVANT LITERATURE 6

Growth Mechanisms of Tin Whiskers.. 6

Tin [Sn] Whiskers and Industrial Concern 6

Sources of Compressive Stresses 9

Externally Applied Mechanical Stresses 10

Intermetallic Compound Formation 12

Electromigration 15

Oxidation… 15

Coefficient of Thermal Expansion 16

Influence of Microstructure in Whiskers Growth 17

Crystallographic Effect.. 17

Grain Size. 18

Thermal Cycling of nano-Ag solders 19

Power Electronic Devices 19

Page

Traditional Die attach materials in Power Electronic Devices............................ 20

Novel High Temperature Solders.. 24

Au-based Systems 24

Transient Liquid Phase Sintering (TLPS) 25

Nano-Ag Solder.. 26

Failure Mechanisms of Power Electronic Devices.. 28

Characterization of Thermal Induced Damage 29

Research Objectives 31

EFFECT OF CRYSTAL ORIENTATION AND MICROSTRUCTURE ON THE NUCLEATION AND GROWTH OF SN HILLOCKS BY IN SITU NANOINDENTATION.. 32

Overview 32

Introduction 33

Materials and Experimental Procedure 39

Sample Preparation... 39

Focused Ion Beam (FIB) and Electron Backscattered Diffraction (EBSD)........ 40

In Situ Nanoindentation.. 42

Micropillar Compression…………………………………………………………..44

Results and Discussion... 45

Page

Intermetallic Compound (IMC) thickness evolution 45

In Situ Nanoindentation 499

Microstructure and Grain Orientation Analysis 52

Finite Element Modeling of Nanoindentation 60

Micropillar Compression..63

Hillock growth mechanism 66

Conclusions 68

X-RAY MICROTOMOGRAPHY OF THERMAL CYCLING DAMAGE IN
SINTERED NANO-SILVER JOINTS 70

Overview 70

Introduction 71

Experimental Procedures 75

Sample Preparation 75

Shear Testing 78

Thermal Cycling Tests 78

X-Ray Tomography 81

Nanoindentation 82

Results and Discussion 83

Page

Microstructural Characterization 83

Mechanical Properties of Microconstituents by Nanoindentation 84

Bond Quality Analysis by Shear Testing 87

Effect of Peak Temperature on Solder Degradation 89

Test 1- ΔT=230°C 90

Test 2- ΔT=180°C 106

Test 3- ΔT=155°C 118

Thermal Cycling Warpage and Solder Constraint 125

Conclusions 128

SUMMARY AND CONCLUSIONS. 130

Effect of Crystal Orientation and Microstructure on the Nucleation and Growth of Sn Hillocks by In Situ Nanoindentation 130

X-Ray Microtomography of Thermal Cycling of Silver-based Thermal Interface Materials 132

REFERENCES..134

LIST OF TABLES

Table Page

I. Misorientation Values for Grain Boundaries Surrounding Hillocks……………….59

II. Parameters Used for Finite Element Modeling……………………………...…...62

III. Young's Modulus and Hardness Obtained by Nanoindentation for Microconstituents of Sample...86

IV. Coefficient of Thermal Expansion for Microconstituents of the Solder Joint...125

V. Comparison Between Original Stack and Transformed Stack……………………127

LIST OF FIGURES

Figure Page

1. Most Commonly Found Types of Sn Whiskers, a) Filament, b) Hillock, c) Columnar, d) Mound…………………………………………………………………...............7
2. a) Accelerator Position Sensor Board Connections, b) Tin Whiskers on the Surface of the Acceleration Position Sensor Board Connection Terminals of the 2005 Toyota Camry……………………………………………………………………………….9
3. SEM Images of Growth on a Sn Nodule at a Berkovich Indentation in Sn Film. The Film Was Kept Under Vacuum During and After Indentation…................................12
4. Schematic Illustration of Interdiffusion and Intermetallic Formation at Sn–Cu……...14
5. Schematic of a Cross-Section of Traditional Power Semiconductor Module. Arrows Indicating the Most Important Components of the Device……………….…………..19
6. Operating Temperatures of High-Temperature Solder Materials as a Function of their Homologous Melting Temperature. Most of These Solder Materials Cannot Perform at Temperatures Beyond 250°C……………………..…………………………………21
7. Melting Point of Die Attach Materials as a Function of Their Processing Temperature. The Processing Temperature Refers to the Temperature at Which the Solder Bond is Made, the Melting Temperature can be Understood as the Temperature of Melting of the Die Attach Material After the Bonding Has Been Made…….……………………23
8. (a) Milled trenches on either side of the indentation zone to obtain a slab, (b) Tungsten needle welded to the slab for lift-out and placing on a Cu TEM grid, (c) Cutting of the tungsten needle using ion beam after welding the slab to the Cu grid, (d) Ion channeling image of the slab after final polishing in FIB…………………………………………41

Figure Page

9. (a) SEM Image of a Linear Array of Indentations With 100 μm Spacing (view at 76º) (b) Typical Curve of Load Vs Displacement Obtained During Nanoindentation. The 3 Stages of Indentation Can be Seen – Loading up to 15 mN, Followed by Holding for 10 Seconds and Unloading…………………………..………………..………..43

10. FIB Cross-Section Through the Thickness of the Sample Showing Different Phases after Being Aged at 150°C for 72 Hours……….……………………………………..45

11. Total Intermetallic Thickness as a Function of Aging Time at 150ºC. The Growth Exponents Indicate that Cu_3Sn Forms Through Bulk Diffusion and Cu_6Sn_5 Forms Through a Mixed Grain Boundary and Bulk Diffusion Mechanism.……..…………..46

12. IMC Evolution at Different Aging Times, (a) As-Plated, (b) 3 Days Aged, (c) 15 Days Aged. After 15 Days in Can Be Seen That the Cu_6Sn_5 Nodules Extended Through the Entire Thickness of the Electroplated Sn…………………………………………...48

13. View at 76° of an As-Plated and Indented Sample (a) Immediately After Indentation, (b) After 20 Days in the SEM Vacuum Chamber…………………………………...49

14. (a) Faceted Hillocks Growing Right After Indentation (76° view), (b) Hillocks Growing in the Indentation Pit Showing Faceted Structure (52° View)………………………..50

15. Hillock Growth Over Time, (a) Right After Indentation (Day 0), (b) 2 Days After Indentation Showing Growth of the Faceted Hillocks in the Indentation Center, (c) After 3 Days – Showing Arrested Growth, (d) After 20 Days……...…………………51

16. (a) Ion Channeling Image of an As-Plated Sample, the Dotted Lines Roughly Indicate Indentation Zone, (b) OIM Map of the Slab Showing Elongated Grains Away From the Indentation Zone and Equiaxed Grains Below the Indentation………….…………53

Figure Page

17. (a) Segmented Grain Structure of an As-Plated Slab, (b) Aspect Ratio of Top Layer of the Slab, (c) Aspect Ratio of Middle Layer of the Slab, (d) Aspect Ratio of Bottom Layer of the Slab. Grains Present Within the Dotted Line Have the Lowest Aspect Ratio in Each Regime…..…………………………………………………………..54

18. (a) Ion Channeling Image of an Aged Sample, the Dotted Lines Roughly Indicate the Indentation Zone, (b) OIM Map of the Slab Showing Orientation of the Large Sn Hillocks…………………...……………………………………………………….55

19. (a) Segmented Grain Structure of an Aged Slab, (b) Aspect Ratio of Top Layer of the Slab, (c) Aspect Ratio of Middle Layer of the Slab, (d) Aspect Ratio of Bottom Layer of the Slab. Grains Present Within the Dotted Line Have the Lowest Aspect Ratio in Each Regime……………………………………………………………...….56

20. (a) Binary Image of Segmented Hillocks (Top View of an Indentation), (b) Number Density of Hillocks as a Function of Distance Showing Hillock Presence Up to 15 μm From the Indentation Edge, (c) Aspect Ratio of Hillocks as a Function of Distance Around the Indentation……………………………………………………………58

21. Magnified OIM Map an Area Surrounding a Hillock in an Aged and Indented Sample………………………………………………………………………..…59

22. Inverse Pole Figures Showing No Preferred Grain Orientation on the FIB Slab Away From the Indentation and Below the Indentation……………………………………..60

23. Finite Element Mesh and Boundary Conditions Used in the Model. Axis 1,2 and 3 Correspond to axis X, Y and Z Respectively……………………………………...61

Figure Page

24. PEEQ from FEM Simulation at an Indentation Load of 15 mN for Pure Sn……………………………………………………………………………..…62

25. a) 5 x 10 μm Sn Pillar Before Micropillar Compression Experiment, b) Pillar After Compression, c) Cross-Section of the Compressed Pillar, d) Overlay of EBSD Map. Bright Layer on Top of Pillar is Platinum Which was Deposited to Obtain a Smooth Cross-Section……..……………………………………………………………..63

26. Pillar Compression Results Showing the Yield Stress for 0.8 μm, 0.5 μm and 0.2 μm Width. Each Color Represents a Pillar Size, Blue Represents 2x4 μm Pillars, Orange Shows Results for 3x6 μm Pillars and Gray Indicates 5x10 μm Pillars……..………...64

27. Schematic Diagram Showing Mechanism of Hillock Growth. (a) Initial Microstructure with Columnar Sn Grains, (b) Nanoindentation Using Berkovich Tip, (c) Dynamic Recrystallization During Indentation, (d) Diffusion of Sn Atoms to Free Surface and forming Sn Hillocks to Relieve Compressive Stress, (e) High Angle Grain Boundaries Around Recrystallized Grains Act as Fast Diffusion Pathway for Sn Atoms, (f) The Case of Thicker IMC: Back Stresses in Aged Samples Due to Thicker IMC Result in More Extensive Hillock Growth at Indentation Center, and Sides, After Removing the Load……………………………………………………………………………….66

28. Traditional Power Package of a Hybrid Vehicle Showing Stresses at Interfaces……..71

29. Die Attachment Structure Consisting of a DBC Substrate, Nano-Ag Solder Paste as a Die Attach Material and a Single Side Polished Si Die….……………………………77

Figure Page

30. Sintering Profile Used for Sample Preparation. A Heating Rate of 4°C/min Was Used Until Reaching a Maximum Temperature of 250°C and Held for 30 Minutes. A Load of 1 Kg (0.4 MPa) was Applied During Sintering……………………….………………77

31. Schematic of Shear Testing Fixture. The Lower Shear Bar (Marked by 2) Holds the Substrate with Clamping Plates. The Upper Shear Bar (Marked by 1) is Connected to a Moving Actuator that Applies the Shear Load. End Plate (Marked by 3) is Adjustable Based on the Thickness of the Si Die...………………………………………………78

32. Setup Used for the Thermal Cycling Experiments. A Ceramic Heater was Used as the Heat Source and Placed on Top of the Si Die. A Control Cooling Rate was Achieved by Using Forced Air Through a Nozzle Placed Closer to the DBC Side...……………79

33. Thermal Cycling Test Parameters. The Heating and Cooling Rate were Kept Constant at 4°C/min. A Dwell Time of 1 min at Peak Temperature was Applied in Each Test……………………………………………………………………………...80

34. a) ZEISS X-radia 520 Versa CT System, b) Sample Mounted Inside the System for Tomography…………………………...…………………………………………..82

35. a) 30 μm-thick Nano-Ag solder Bondline, Good Adhesion Can Be Seen at the Si-Solder and Solder-DBC Interfaces, b) Zoomed Image of Nano-Ag Bondline, Homogenous Distribution of Pores Can Be Observed………………………………………………83

36. Representative Load Vs Displacement Curve for the Microconstituents of the Stack. Each Layer was Indented up to a Depth of 1 μm……………………….………………..85

37. Nanoindentation Behavior of the Different Layers in the Nano-Ag Stack, a) Modulus Vs Displacement, b) Hardness vs Displacement…………………………...…………86

Figure Page

38. Shear Stress Vs Displacement Curve of a Nano-Ag Solder Joint……………..……...87

39. Fractography SEM Image of Nano-Ag Solder Joint After Shear Testing, a) Fracture Occurred Through the Thickness of the Solder as Seen in this Image of the Si Die Side, b) Delamination Occurring at Few Places on the Si Die-Solder Interface, c) Magnified View of the Nano-Ag Solder Showing Coalescence of Nano-Ag Spheres…………...89

40. Slice of 3D X-Ray Tomography Scan Showing Nano-Ag Solder Prior to Thermal Cycling. The Red Square Indicates the Position of the 5 mm x 5 mm Si Die that is Placed on Top the Solder……………………………………………………………..90

41. Microstructural Damage Evolution of Nano-Ag Solder During Thermal Cycling from 20°C to a Peak Temperature of 250°C, a) 0 Cycles, b)300 Cycles, c) 750 Cycles, d) 1000 Cycles, e) 3000 Cycles………………………………………………………….93

42. a) Microstructure of Nano-Ag Solder After 3000 Thermal Cycles with ΔT=230°C, the Blue Box Shows the Region where the Delamination Damage was Seen, b) Magnified View of the Region of Delamination of Solder………………………………………94

43. Nano-Ag Solder Joint After 3000 Thermal Cycles at ΔT=230C° Viewed at Different Planes, a) XY View of Sample Showing Nano-Ag Solder, b) XZ View of the Solder Stack Showing the Multiple Layers in the Solder Joint, c) YZ Plane View of Sample………………………………………………………………………………..95

44. Crack Formation and Growth on Cu Layer of DBC Substrate as a Result of Thermal Cycling, a) 300 Cycles, b) 500 Cycles, c) 750 Cycles, c) 1000 Cycles, e) 3000 Cycles……………………………………………………………………………...96

Figure Page

45. Solder Joint Stack Viewed in the XZ Plane. Red Box Shows Crack Formation at the Cu Layer in the DBC Substrate……………………………………………………….………97

46. Image Segmentation Procedure in Avizo, a) 3D Stack is Imported into the Software, b) The Tool 'Region Growth' is Selected to Select Cracks/Pores Based on its Grey Scale Value, c) Final Segmented Image…………………………………………..……...98

47. Cracks in the Solder are Segmented and Color Coded From 0-3000 Cycles. a) 0 Cycles, b) Overlay of 0-300 Cycles, c) Overlay of 0-750 Cycles, d) Overlay of 0-1000 Cycles and e) Overlay of 0-3000 cycles…………………………………………………...99

48. Solder Area Divided into 9 Segments for Analysis of Crack Density per Region..…101

49. Increase of Crack Density Per Quadrant, a) Actual Crack % for Each Cycle/Step, b) Increase in Crack % with Respect to 0 Cycles…………………………………...102

50. Decrease in Young's Modulus According to a) Wachtman and MacKenzie Relation b) O'Connell and Budiansky Relation. A Clear Effect of Thermal Cycling is Observed on the Mechanical Properties of Nano-Ag Solder, Where Crack Formation Results in a Decrease of Young's Modulus…………………………………………………..105

51. a) FIB Cross-Section of As-Sintered Nano-Ag Solder Showing a Network of Fine Pores Uniformly Distributed Within the Solder Volume, b) Binary Image of Fine Pores Obtained Using Grayscale Thresholding Technique……………………………..106

52. X-Ray Images Showing the Initial Microstructure of Sample 2, with an Initial Pore Volume Fraction of 8.25%...107

Figure Page

53. Microstructural Damage Evolution of Nano-Ag Solder During Thermal Cycling From 20°C to a Peak Temperature of 250°C, a) 0 Cycles, b)300 Cycles, c) 750 Cycles, d) 1000 Cycles, e) 3000 Cycles…………………………………………………...108

54. a) Microstructure of Nano-Ag Solder After 3000 Thermal Cycles with ΔT=180°C, the Blue Box Shows the Region where the Delamination Damage was Seen, b) Magnified View of the Region of Delamination of Solder………………………………..….109

55. Crack Formation and Growth on Cu Layer of DBC Substrate Because of Thermal Cycling, a) 500 Cycles, b) 1000 Cycles, c) 3000 Cycles………………..…………...110

56. Cracks in the Solder are Segmented and Color Coded From 0-3000 Cycles. a) 0 Cycles, b) Overlay of 0-300 Cycles, c) Overlay of 0-500 Cycles, d) Overlay of 0-1000 Cycles and e) Overlay of 0-3000 cycles…………………………………………………112

57. Solder Area Divided into 9 Segments for Analysis of Crack Density Per Region……………………………………………………………………………113

58. Increase of Crack Density Per Quadrant, a) Actual Crack % for Each Cycle/Step, b) Increase in Crack % with Respect to 0 Cycles………………………………………115

59. Decrease in Young’s Modulus According to a) Wachtman and MacKenzie Relation b) O’Connell and Budiansky Relation. A Clear Effect of Thermal Cycling is Observed on the Mechanical Properties of Nano-Ag Solder, Where Crack Formation Results in a Decrease of Young’s Modulus…………………………………………………...117

60. X-Ray Images Showing the Initial Microstructure of Sample 2, with an Initial Pore Volume Fraction of 3.5%...118

Figure Page

61. Microstructural Damage Evolution of Nano-Ag Solder During Thermal Cycling from 20°C to a Peak Temperature of 250°C, a) 0 Cycles, b)1500 Cycles, c) 3000 Cycles...119

62. Analysis of Increase of Crack Density as a Function of Number of Thermal Cycles for Sample 1 (ΔT=230°C), Sample 2 (ΔT=180°C) and Sample 3 (ΔT=155°C). The Red Circle on the Plot Indicates Delamination Occurring at the Solder-Si Interface…….120

63. Cracks in the Solder are Segmented and Color Coded from 0-3000 Cycles. a) 0 Cycles, b) Overlay of 0-3000 Cycles…………………………………………………………...121

64. Solder Area Divided into 9 Segments for Analysis of Crack Density Per Region…...122

65. Increase of Crack Density Per Quadrant, a) Actual Crack % for Each Cycle/Step, b) Increase in Crack % with Respect to 0 Cycles……………………………………....123

66. Decrease in Young's Modulus According to a) Wachtman and MacKenzie Relation b) O'Connell and Budiansky Relation…………………………………………...…….124

67. a) Solder at the Edges is Unconstraint and Hence Less Deformation is Seen, b) Delamination Induced by Warpage of the Si Die, c) Schematic Showing the Solder at the Edges Free to Expand Whereas Solder at the Center is Constraint and Hence Experiences More Stresses Leading to Cracking of the Solder……………..………126

68. Transformed Solder Stack for Analysis of Composite Beam Using the Transformed Area Method……………………………………………………………………...128

1. INTRODUCTION

1.1. Growth Mechanisms of Tin Whiskers

Tin whiskers have been a serious industrial concern in microelectronic packaging for several decades. They are usually found on relatively thin (0.5 to 50 microns) metal films that have been deposited onto a substrate material. Whiskers have been reported to grow as long as 500 microns in length with diameters typically about 5 microns (Galyon 2005).

It is understood that these single crystalline filaments grow because of a variety of factors, including the relief of compressive stresses (Tu 1994), changes in grain structure due to recrystallization of the electroplated films (Sampson Michael 2009) and the combination of an applied electric field and humidity (Vasko, Grice et al. 2015).

For long time, Sn-rich alloys have been the most important type of solder in electronic packages. For years Pb was incorporated to the solder to decrease the melting point, improve the mechanical properties of the solder and to inhibit whisker growth. However, due to the requirement to eliminate use of Pb in electronic devices by the Restriction of Hazardous substances (RoHS) (Warwick 1999) and the implementation of Pb-free solders, pure Sn became the substitute due to its good wettability (Grossmann and Zardini 2011), good conductivity (Dimitrovska and Kovacevic 2009) and low cost (Illés, Horváth et al. 2010). Since then, Sn whiskers have been considered a major reliability issue since they can grow long enough to cause short circuits in fine pitch electrical components (Williams, Chapman et al. 2013). They have the potential to be catastrophic. Sn whiskers have been reported to

have caused major failures in equipment used for earth and space applications many of which have been documented by NASA (NASA-Webpage). Hence, it is necessary to develop mitigation strategies for tin whiskers for which understanding their growth mechanisms as well as properties is important.

Over the years, numerous investigations have proposed mechanisms describing the growth behavior of tin whiskers. Several factors act as sources of compressive stresses, commonly IMC formation (Weil 1970, Boettinger, Johnson et al. 2005, Xu, Zhang et al. 2005), mechanical stresses (Xu, Zhang et al. 2005, Shibutani, Yu et al. 2006), electromigration (Tu, Chen et al. 2007), corrosion/oxidation (Tu 1994), thermal expansion and thermal cycling (Boettinger, Johnson et al. 2005). However, none of these mechanisms fully explains the growth of Sn whiskers.

The proposed work on this dissertation is focused on investigating whisker/hillock growth influenced by localized compressive stresses induced by nanoindentation and IMC formation through thermal aging. To avoid the influence of oxide layer formation after nanoindentation, the tests will be done *in situ* in a Scanning Electron Microscope [SEM]. Also, the effect of grain orientation on whiskers growth will be studied through Electron Backscattered Diffraction [EBSD].

The first part of this thesis is focused on understanding the growth of Sn whiskers which are mechanically induced using *in situ* nanoindentation in a controlled vacuum environment. SEM and EBSD analyses were used to characterize the deformation occurring in the microstructure of the film that lead to the nucleation and growth of Sn whiskers. A better understanding of the growth mechanisms of the Sn whisker phenomenon

would eventually lead to the progress in mitigation techniques that are efficient and at a low cost.

1.2. X-Ray Microtomography of Thermal Cycling of Silver-based Thermal Interface Materials

Thermal interface materials are essential components in semiconductor devices. They are required to efficiently conduct heat and electricity while maintaining their mechanical strength. In power electronic devices, the operating temperature can exceed 200°C (Buttay, Planson et al. 2011). At these elevated temperatures, most of the traditional solders like Sn-based solders are unable to perform, since premature failure has been observed due to excessive IMC formation, creep and oxidation. The increasing demand for efficiency and reduction in package size led to the development of wide bandgap (WBG) semiconductor devices. WBG semiconductors such as SiC and GaN devices have the potential to operate at temperatures well over 300°C (Manikam and Cheong 2011).

To be able to operate efficiently, as a rule of thumb, the operating temperatures of solder materials is calculated as 80% of the homologous melting temperature. High temperature Sn based solders such as SnAgCu solders cannot perform above 125°C. Gold based AuSn solders are able to perform at a higher temperature, 175°C, however the disadvantage it presents is its high material cost. Zinc based ZnAl are able to function at temperatures as high as 250°C, but it has its disadvantages with difficulties in processing (Knoerr, Kraft et al. 2010).

The existing limitation between processability, operating temperature and cost has driven the search for more stable high-temperature solders that have a lower processing temperature. Sintered nano-Ag solder is currently a strong candidate for high temperature thermal interface material because of its good electrical (2.6μΩ·cm) (Bai, Zhang et al. 2006) and thermal conductivity (2.4 W/cmK) (Manikam and Cheong 2011).

In electronic packages, the lifetime of the device is affected by the transition from low to high operating temperature (Manikam and Cheong 2011). In the case of thermal interface materials, the leading cause of failure is the damage induced by thermal cycling. Jiang et al. studied the degradation in the microstructure of nano-Ag and Sn-rich solders after thermal cycling the samples from -40°C to 125°C by analyzing in an SEM the cross-section of the sample after 800 cycles (Jiang, Lei et al. 2014). SEM images revealed delamination occurring at the interfaces between Sn-rich solder and substrates. Additional work by Bai et. al (Bai, Calata et al. 2006) studied the thermal induced damage on nano-Ag solder by cycling samples from 50°C to 250°C and shear testing them later to study the decrease in shear strength caused by thermal fatigue. While these studies shed light on the final microstructure after thermal cycling, the destructive nature of these characterization techniques makes it impossible to visualize and quantify the evolution of thermal fatigue damage as a function of time within the same sample. X-ray tomography on the other hand, has been proven to be an excellent technique to evaluate time-resolved quantitative understanding of deformation in several material systems, since it eradicates destructive cross-section analysis of samples and because it requires negligible sample preparation to give high resolution imaging (Williams, Flom et al. 2010). Padilla et al. (Padilla, Jakkali et

al. 2012) used 3D X-ray tomography to quantify the evolution of porosity in a Sn-based alloy as a function of strain. The research also evaluates the experimental results using a microstructure based Finite Element Modeling which further validates the microstructural evolution and the fundamental understanding of deformation behavior.

The second part of this research work focuses on understating the evolution of thermal induced damage in the microstructure of sintered nano-Ag samples. 3D x-ray tomography was used to non-destructively study the formation and growth of microcracks as a function of time. The effect of peak temperature on microstructural damage over time was also studied. A better understanding of thermal induced damage on nano-Ag solder will provide a better insight into the reliability of nano-Ag solder as a promising thermal interface material.

2. REVIEW OF RELEVANT LITERATURE

2.1. Growth Mechanisms of Tin Whiskers

2.1.1. Tin [Sn] Whiskers and Industrial Concern

Tin whiskers are electrically conductive single crystalline filaments that grow from the surface of Sn-rich films. The incubation time can vary from tens of hours to tens of thousands of hours (Osenbach, DeLucca et al. 2007). They can grow up to 10 mm and have diameters that range up to 10 microns (NASA-Webpage). The grow of Sn whiskers is from the base of the whisker and not from the tip, and this was first shown by Koonce and Arnold, after observing that the morphology of the tip remained unchanged as the whisker grew longer (Cheng, Chen et al. 2010). There are several types of whiskers being the most common straight, kinked, hooked and hillock. Whiskers that have mound type morphology are called Hillocks, and these protrude from the surface of the electroplated film (Chen 2016). The common straight whiskers grow longitudinally, maintaining a constant diameter while hillocks don't have a defined shape and the diameter changes as they grow (Shibutani, Yu et al. 2006). Fig. 1 shows the different shapes of whiskers that are commonly reported in literature.

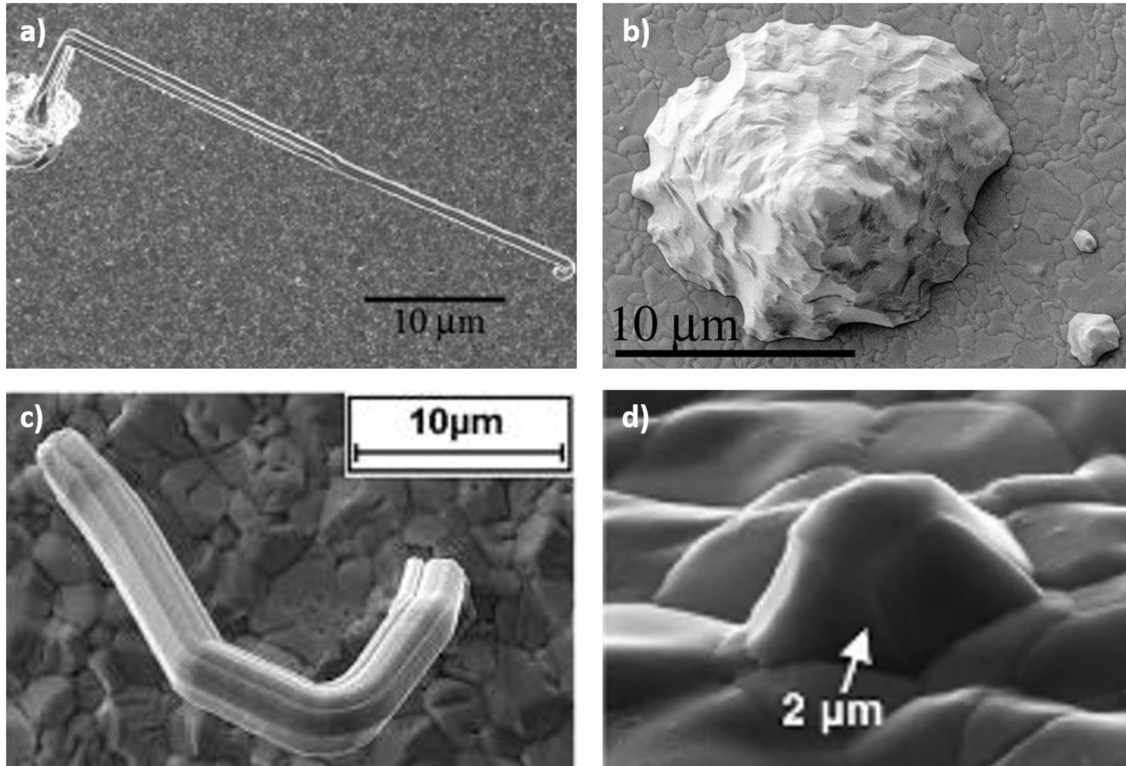

Figure 1. Most commonly found types of Sn whiskers, a) Filament (Moon, Williams et al. 2001), b) Hillock (Sobiech, Welzel et al. 2008), c) Columnar (Beauchamp 2008), d) Mound (Zhang 2011).

It can be assumed that the most harmful type are the filament and columnar shapes. Even though their diameters are small, their length can reach millimeters and by touching other Sn whiskers can cause electrical short circuits. Hillocks or nodules are less problematic than whiskers because many of them are too short to cause short circuits. A fundamental understanding of mechanically induced whisker formation requires the analysis of microstructural differences between columnar whiskers and mound-type/hillocks (Mizuguchi, Murakami et al. 2012). Understanding the spontaneous growth process and how to mitigate it's growth, is critically important specially to the electronics industry, as tin-based coatings are routinely applied to copper conductors to improve solderability and

reduce corrosion (Galyon 2005). In flexible electronic packages, frequent bending of substrates results in the accumulation of compressive forces in solder joints and this could facilitate whisker formation (Lin, Yorikado et al. 2007). With the developing use of Sn and Sn alloy plating on flexible electronics, it has become of crucial importance to understand the mechanism of formation and growth of Sn whiskers (Lin, Yorikado et al. 2007).

Sn whiskers have been an interesting industrial problem for many years. Boettinger et al. (Boettinger, Johnson et al. 2005) postulated that whiskers are known to cause short circuits in fine pitch pre-tinned electrical components. Whiskers can cause short circuits between the leads in printed circuits boards (PCB), failure can also occur when a whisker causes an electric current that ends up melting the whisker (Huang, Nunez et al. 2018). Since 1988 several weapons systems have failed due to Sn Whiskers, examples are the Phoenix Missile, F - 15 Radar, Patriot Missile and Avionics relays. Some of the most know documented cases of failure of a system due to Sn whiskers are listed next:

- On-Orbit commercial (non-NASA) satellite failures: failures in satellite control processors (SCP) were reported due to whiskers that short circuited electromagnetic relays that had pure Tin electroplating (NASA-Webpage).
- Military Failures: these include military airplanes, the missile “Patriot”, F-15 radar (NASA-Webpage).
- Medical equipment failures: it includes the recall of heart pacemakers (NASA-Webpage), and apnea monitor failures. An apnea monitor is a medical device that sounds an alarm if the patient monitored stops breathing. The presence of whiskers on the switch caused the alarm of the monitors to fail (Downs and Francis 1994).

- Industrial/Power: such as reactor shutdown and radio receiver sensitivity issue (NASA-Webpage).
- Sudden acceleration in Toyota vehicles: Tin whiskers were found to cause short circuiting in the electronic systems that control the acceleration of Toyota Camry cars. Fig. 2 shows accelerator position sensors and whiskers nucleating on their surface in a Toyota Camry (NASA-Webpage).

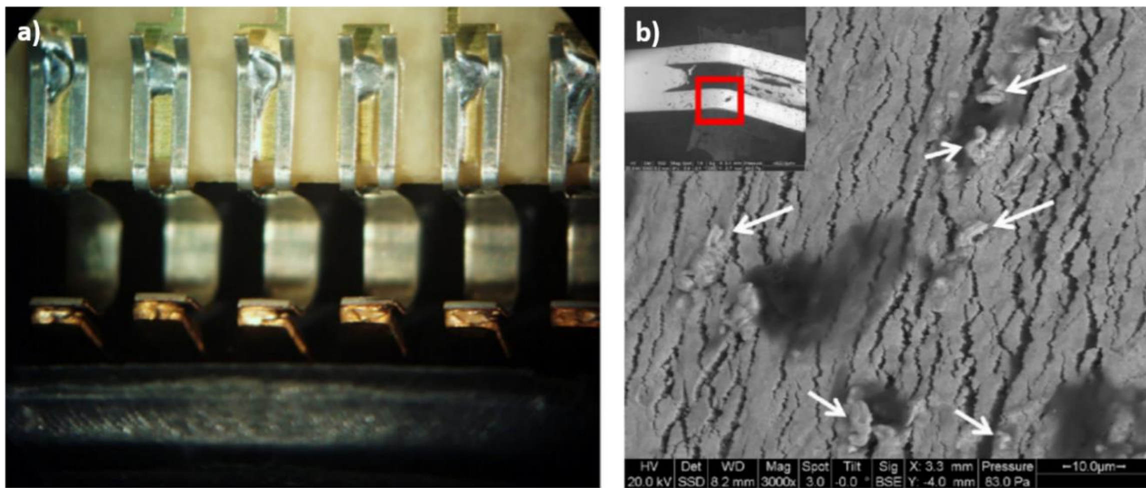

Figure 2. a) Accelerator Position Sensor Board Connections, b) Tin whiskers on the surface of the acceleration position sensor board connection terminals of the 2005 Toyota Camry (Sood, Osterman et al. 2011).

2.1.2. Sources of Compressive Stresses

Although there is no single theory that fully explains the mechanism(s) for Sn whiskers growth, there seems to be an agreement on whiskers being a local response to the existence of compressive residual stress (Boettinger, Johnson et al. 2005). There are several factors

that have been proposed as sources of compressive stresses which initiate whisker growth. The most common sources of compressive stresses are described next.

2.1.2.1. Externally Applied Mechanical Stresses

Compressive stresses within a Sn film are a necessary condition for whisker growth, however, these stresses might not be sufficient (Galyon and Palmer 2005). Additional compressive stresses can be generated by mechanical operations during the insertion of connectors. For applications, such as flexible electronics, the semiconductor device is required to perform under load conditions such as bending, rolling and stretching. Under these loads, mechanically induced Sn whisker growth has been observed by researchers (Lin, Yorikado et al. 2007, Dudek and Chawla 2009, Kang, Chang et al. 2013, Williams, Chapman et al. 2013, Doudrick, Chinn et al. 2015).

Work done by Amin et al. (Amin, Yusof et al. 2017) showed the effect of introducing compressive stresses through bending of a Sn coated sample. In this work, Sn coated samples were bent at 45° until a crack occurred. It was observed that a larger number of whiskers formed away from the crack region. The cracked area is highly stressed. Hence, to release stresses, Sn atoms migrated to regions of higher stresses to regions of lower stresses resulting in whiskers formation.

Whisker growth can also be induced by contact pressure between connectors, which in turn produces whisker growth induced by pressure (Shibutani, Yu et al. 2008). Work by Lin et al. (Lin, Yorikado et al. 2007) establishes that IMC growth is not necessary for pressure induced whiskers to nucleate and grow.

To study the effects of mechanical loading, indentation is commonly used for inducing local controlled plastic deformation and accelerating whisker nucleation and growth (Lin, Yorikado et al. 2007, Kang, Chang et al. 2013, Williams, Chapman et al. 2013).

Mechanically induced whisker growth by indentation has been studied in the past using large indenters (900 μm ZrO_2 ball indenter (Lin, Yorikado et al. 2007, Doudrick, Chinn et al. 2015) and large loads (>100 gf (Lin, Yorikado et al. 2007, Kang, Chang et al. 2013, Doudrick, Chinn et al. 2015) (Lin, Yorikado et al. 2007, Kang, Chang et al. 2013, Doudrick, Chinn et al. 2015)) (Vallabhaneni, Izadi et al. 2017). However, using large indents involves the effects of several factors that influence whisker growth. Due to the large deformation zone, these indents often span several grains and thus any orientation effect is lost.

To localize the stress field, the indentation size needs to be very small, comparable to the microstructural features. Williams et al. (Williams, Chapman et al. 2013) used nanoindentation to correlate the growth rate of hillocks with stress relief using an *in situ* nanoindenter in a scanning electron microscope. Fig. 3 shows the evolution of Sn nodules (or hillocks) observed *in situ*, for periods over 1200 hours.

Additionally, Dudek et al. (Dudek and Chawla 2009) used nanoindentation for rare earth (RE) containing solders and showed that the oxidation of RE IMC caused whisker formation and the whiskers density was enhanced by indentation.

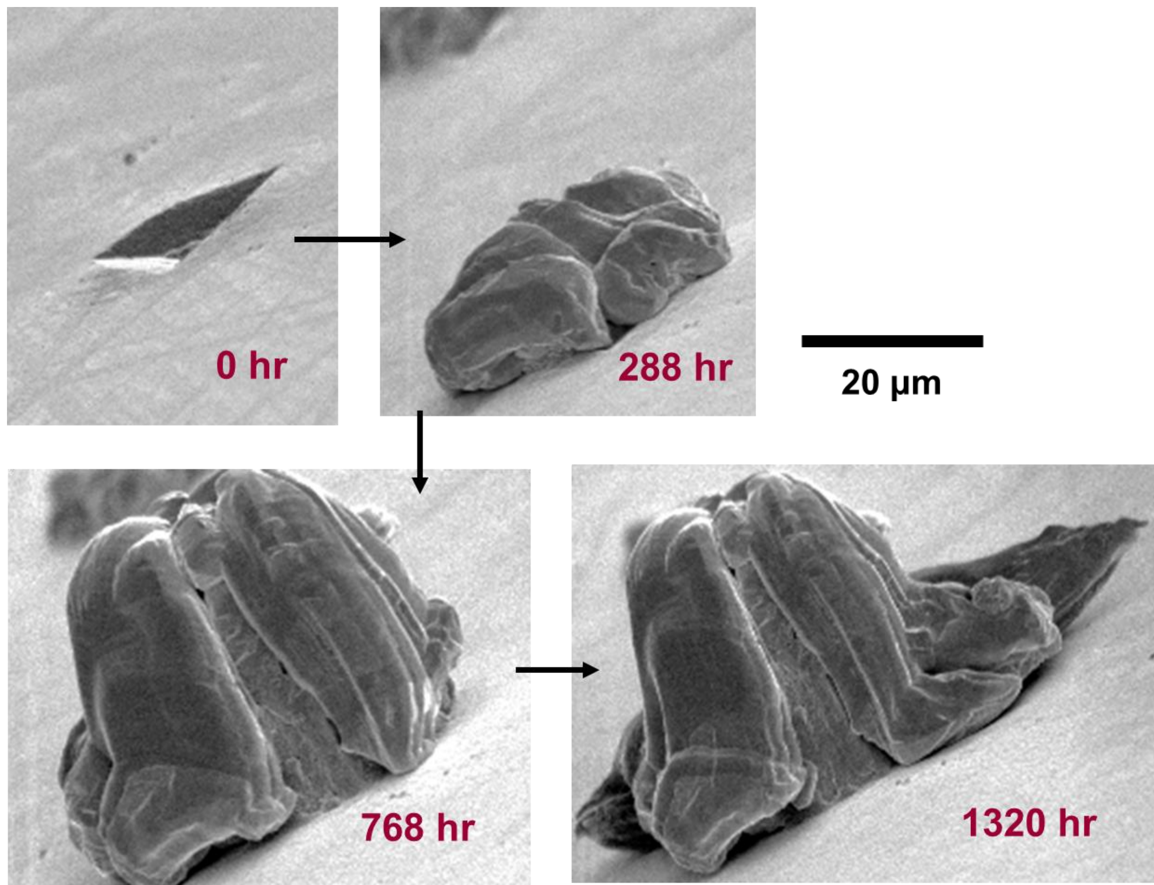

Figure 3. SEM images of growth on a Sn nodule at a Berkovich indentation in Sn film. The film was kept under vacuum during and after indentation (Williams, Chapman et al. 2013).

2.1.2.2. Intermetallic Compound Formation

One of the most commonly discussed sources of compressive stress in Sn electrodeposits is Intermetallic compound (IMC) formation due to the reaction of Sn with Cu in the substrate metal (Boettinger, Johnson et al. 2005). Diffusion of Cu metallization into the Sn plating forms IMC phases (Cu_6Sn_5 and Cu_3Sn) which generate compressive stresses that continue growing over time resulting in whisker formation.

Both interdiffusion and intermetallic compounds (IMC) formation occur at the Cu substrate–Sn solder interface. Interdiffusion occurs through bulk (vacancy and interstitial, slow), grain boundary (fast) and surface diffusion (crack or pores, very fast) pathways. IMC formation occurs directly at the Sn–Cu interface as well as in grain boundaries. Depending on the temperature and time at elevated temperature, both Cu_6Sn_5 and Cu_3Sn can be formed. It has been demonstrated that the overall interfacial process occurs by Cu preferentially moving into Sn, whereas very little Sn moves into Cu as schematically represented in Fig. 4.

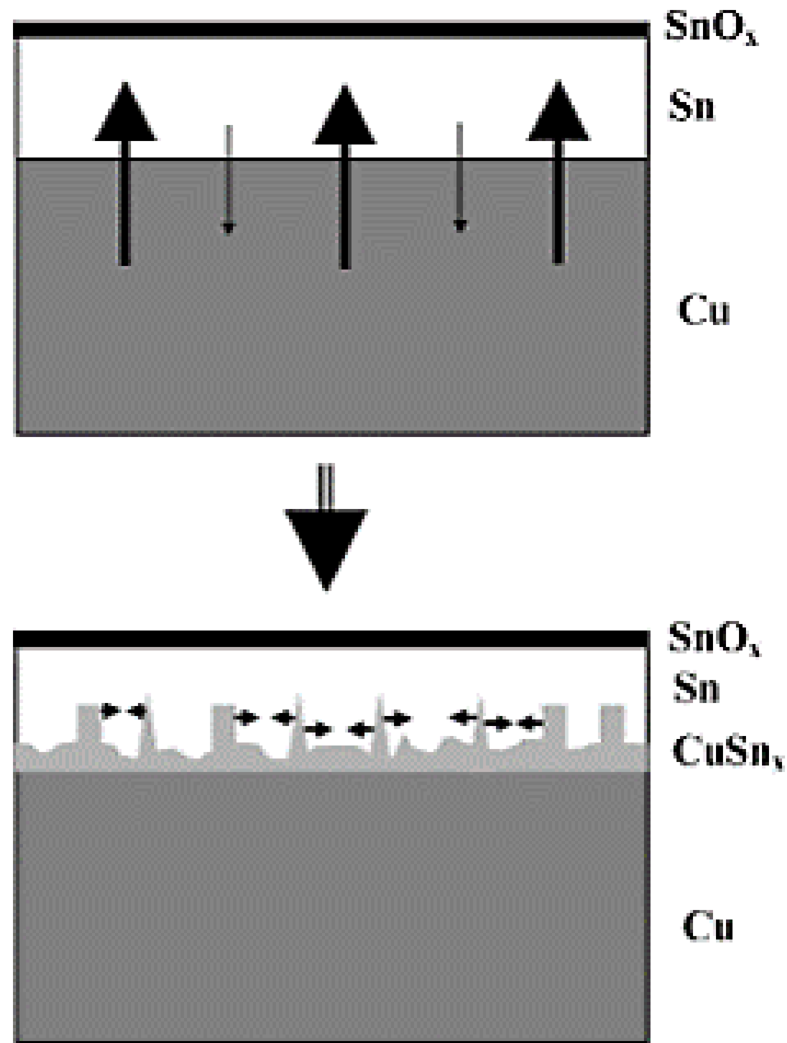

Figure 4. Schematic illustration of interdiffusion and intermetallic formation at Sn–Cu (Xu, Zhang et al. 2005).

Work done by Endo (Endo 1997) suggests that the interstitial diffusion of Cu and formation of Cu_6Sn_5 may alter the lattice spacing in the Sn plating and generate compressive stress. It is also hypothesized that IMC formation causes a volume change which in turn results in generation of compressive stresses. Due to its HCP crystal structure, Cu_6Sn_5 occupies more

volume compared to the Tin it replaces, thus generates compressive stress in the electroplating (Illés, Horváth et al. 2010).

2.1.2.3. Electromigration

Whisker growth due to electrical current differs from whiskers produced by mechanical stressing. Whisker growth by electrical currents appears to originate from the bombardment of electrons moving in the electric field from the cathode to the anode, pushing Sn atoms toward the anode. This creates voids on the cathode and material build up at the anode, and thus results in compressive stress within the Sn film, which is relieved by whisker production throughout the film and hillocks near the anode end (Crandall 2012). This mechanism is further accelerated at higher current densities.

2.1.2.4. Oxidation

Work done by Tu et al. (Tu 1994) concluded that weak spots in the oxide film on the tin surface act as stress relief spots for whisker/hillock growth. Similarly Illes et al. (Illés, Horváth et al. 2010) observed that by storing electroplated Sn samples with a Ag underlayer under extreme oxidizing conditions whiskers nucleated and grew from cracks present in the oxide layer. Oxidation alters whisker growth behavior by inducing compressive stresses through diffusion of oxygen in Sn, or by corrosion of the surface (Hillman, Kittlesen et al. 2011). Formation of weak spots in the oxide layer would enhance the nucleation and growth of whiskers (Tu 1994) by providing a localized stress relief region in the Sn film, which in turn will give a stress gradient where we have compressive stresses in the film and no stresses present at the plating's surface. This enables Sn atoms to diffuse to the surface to result in whisker formation. A requirement for diffusional flow is a gradient of

hydrostatic pressure (Mahapatra and Dutta 2017). High humidity affects the thickness of the oxide film on the Sn leading to compressive stress, it is also thought to increase the rate of grain boundary or surface diffusion, and can also lead to corrosion, which introduces additional stress within the film. The stress states in the electroplated Sn film is also affected by localized corrosion leading to uneven oxide film thickness (Crandall 2012). In the absence of an oxide layer, the compressive stresses within the Sn film are relieved homogenously and thus no whisker formation will be observed (Illés, Horváth et al. 2010). However, Sn whiskers have been observed to grow in vacuum which contradicts the existence of a Sn oxide layer as mandatory for whisker growth (Williams, Chapman et al. 2013).

2.1.2.5. Coefficient of Thermal Expansion

The compressive stress is typically generated by the differential thermal contraction of the deposit and substrate during cooling from deposition temperature (Boettinger, Johnson et al. 2005). This mismatch can cause stress in the constrained tin layer, when temperature cycling is applied (Dittes, Oberndorff et al. 2003).

Pure Sn has a high linear thermal expansion coefficient (22 x 10^{-6} K^{-1}). Cu on the other hand, has a much lower linear thermal expansion coefficient (17 x 10^{-6} K^{-1}). When Sn is plated over Cu and subjected to thermal cycling, the expansion of Cu and Sn will be different causing alternating tensile and compressive stresses during thermal cycling (Xu, Zhang et al. 2005).

2.1.3. Influence of Microstructure in Whiskers Growth

Sn grain size and structure is thought to influence whisker formation. On specimens that exhibit whisker formation, only a select few grains promote whisker formation. However, the reason behind this preferential growth of certain grains is not known. It could be the effect of neighboring grains and the orientation of grain boundaries that facilitates diffusion on atoms favorably for whisker growth. Hence understanding this open question and correspondingly tailoring the microstructure is crucial for inhibiting whisker growth (Pei, Jadhav et al. 2012).

2.1.3.1. Crystallographic Effect

Work by Pei et al.(Pei, Jadhav et al. 2012) showed that the cracking of the oxide layer is not sufficient to initiate whisker growth, this indicates that there is something special about the underlying structure of the Sn film that promotes whisker growth. If a strong correlation between grain orientations and whisker/hillock propensity can be found, strategies can be developed to modify the microstructure or suppress formation of grains with the most susceptible orientations.

Pei et al. showed that hillocks, grown on Sn that was deposited by electron beam evaporation on a Cu layer, originate from orientations close to (001) surrounded by (010) grains, although there were several of such combinations that did not show any growth. In the case of Sn samples electroplated over Cu, it was shown that the preferred orientation was (321) (Choi, Lee et al. 2003, Frye, Galyon et al. 2007, Sobiech, Wohlschlögel et al. 2009) or (111) (Sarobol, Pedigo et al. 2010). The orientation of such grains might not be the same for mechanically induced whiskers. Mizuguchi et al.(Mizuguchi, Murakami et al.

2012) found that in the case of Sn-2%Cu electroplated on a phosphor bronze connector with 2-μm thick Ni underplating whisker nucleation was observed from newly formed 301 twinned grains after applying a mechanical stress of 240 MPa for 3 days, however specific crystal orientations that lead to twin and whisker formation are yet to be studied.

2.1.3.2. Grain Size

Most researchers agree that as the grain size decreases, the tendency for a Sn film to grow whiskers increases (Lu and Hsieh 2007, Cheng, Yang et al. 2011). Work by Tu et. al (Tu 1994) and Sobiech et. al (Sobiech, Teufel et al. 2011) showed that grain boundaries in vertical grains are the main diffusion pathway for Sn atoms to grow whiskers. However, work by Mahapatra et. al (Mahapatra and Dutta 2017) showed that the presence of horizontal grain boundaries associated with equiaxed grains is not essential to eliminate whisker formation.

Work done by Mizuguchi et al. (Mizuguchi, Murakami et al. 2012) and Schetty (Schetty 2014) showed that a possible method to mitigate mechanically induced Sn whiskers is employ a plating which has long columnar grains for which is difficult to cause microstructural change during mechanical deformation. Contradicting this theory, Shibutani (Shibutani 2010) showed grain size dependence for nanoindendation induced Tin whiskers. In this work, it was shown that as the grain size increases, the number of whiskers/hillocks increases. Bright Sn finishes (grain size smaller than 1 μm) are understood to be more susceptible to whisker formation than those of matte Sn (grain size larger than 1 μm) (Kakeshita, Shimizu et al. 1982).

2.2. Thermal Cycling of nano-Ag solders

2.2.1. Power Electronic Devices

An essential component in power electronic devices is the electronic package, which serves as a mechanical framework, provides electrical connectivity and acts as a thermal heat dissipater for the power electronic devices (Zheng 2012). Over the past years, the demand for miniaturization of components, increase in performance, processing speed and need to extend lifetime have led to denser devices that have to perform at higher current densities and temperatures (Manikam and Cheong 2011). Currently, for devices operating at powers exceeding 1 KW and temperatures over 250°C the material technology is not fully developed (Bajwa 2015) and hence premature failure is experienced by traditional devices.

A cross-sectional schematic of a typical power semiconductor device is shown in Fig. 5. It usually is composed of 7 parts, a brief description of each is given below.

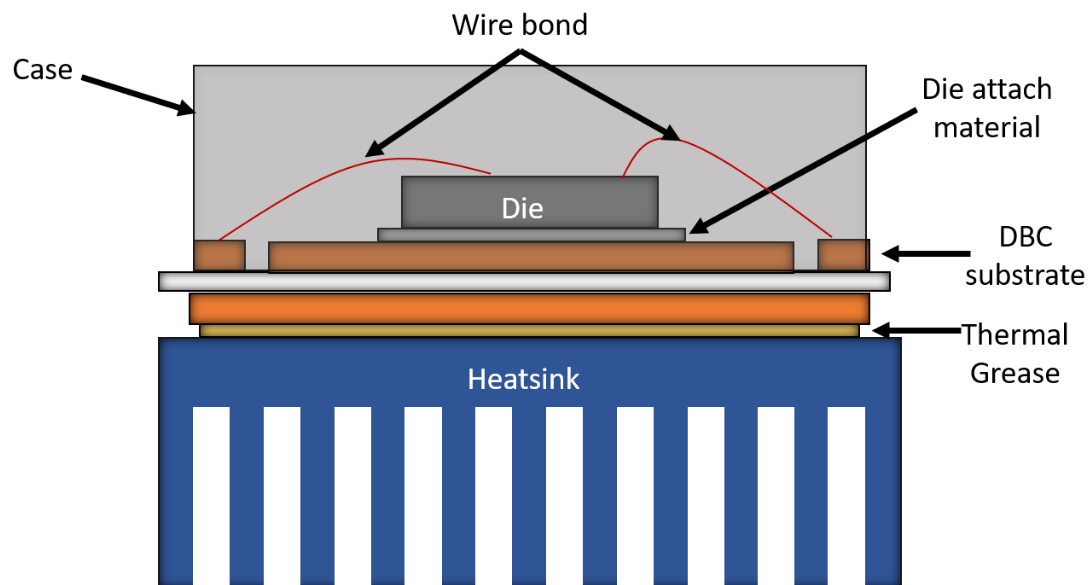

Figure 5. Schematic of a cross-section of traditional power semiconductor module. Arrows indicating the most important components of the device.

- Wire bonding: Al or Au wire connecting substrates to metallization on the Si device (Elshabini and Barlow 2006).
- Encapsulant: Epoxy for sealing the package.
- Power Semiconductor die: Die/device made of Si, SiC or GaN.
- Substrate (base): Usually direct-bonded-Copper (DBC) or direct-bonded-Aluminum (DBA), which serves as mechanical support and electrical platform for the module (Elshabini and Barlow 2006).
- Die attach solder: Thermal interface material capable of processing at low temperature which serves as die attachment, and bonding between base-plate and heat-sink. Provides electrical interconnection, mechanical strength between layers, and heat spreading.
- Heat-sink: Metal plate (Cu or Al) with cooling fins to remove heat generated in the power module.

2.2.2. Traditional Die attach materials in Power Electronic Devices

Die attach materials in power electronic devices have very stringent requirements. They should possess good electrical and thermal conductivity, good stiffness, resistant to corrosion, capable of performing under thermos-mechanical fatigue, among others. There are several types of die attach materials, they can be divided into the following categories: epoxy adhesives, alternative resins, eutectic die attach solders, soft soldering, and silver-glass material (Manikam and Cheong 2011).

Fig. 6 shows the maximum operating temperatures of different high-temperature solders as a function of its melting point. As a rule of thumb, the maximum operating temperature is

taken as 80% of the homologous melting temperature. Beyond this temperature, creep deformation in the solder would be excessive leading to lead to failure of the solder stack (Knoerr, Kraft et al. 2010).

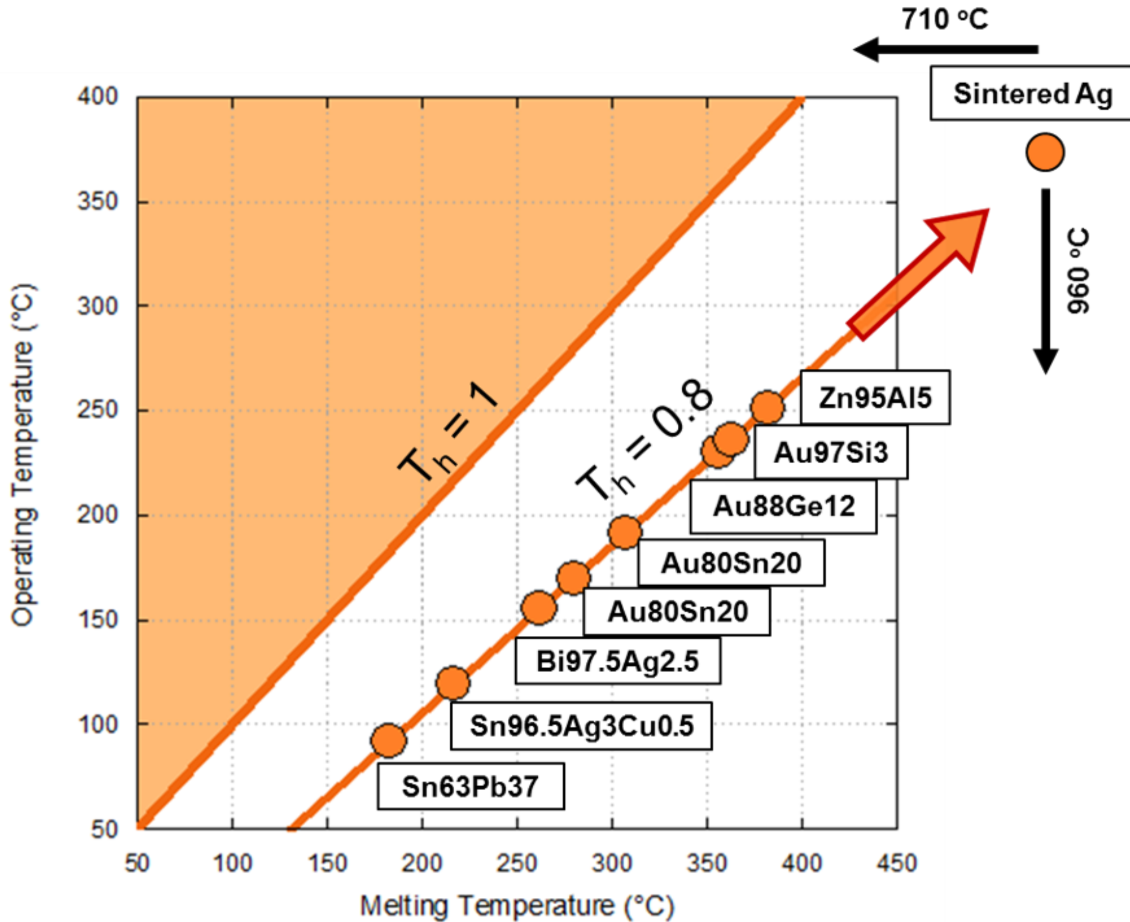

Figure 6. Operating temperatures of high-temperature solder materials as a function of their homologous melting temperature. Most of these solder materials cannot perform at temperatures beyond 250°C.

Sn-rich solders such as SAC305 and Sn3.5Ag are the most commonly used die attach materials in recent times. They have low melting points at around 200°C-250°C and hence have low operating temperatures below 150°C. Pb-Sn and other Pb-based alloys have been used extensively in the power sector due its low cost, easy processibility and good

performance at elevated temperatures (Manikam and Cheong 2011). However, due to the requirements of the RoHS to eliminate Pb from electronic devices, Pb-based solders can no longer be used. Sn-Au based systems are another alternative for high-temperature die attach materials, these have been of interest due to its low processing temperature (below 320°C) and good thermal conductivity (0.57 W/cm·K). The drawback of these Sn-Au based solders are its mechanical properties. Sn-Au solders have high stiffness and due to the formation of Sn-Au IMCs, the alloy becomes brittle leading to easy crack propagation (Ivey 1998).

Another newer alternative to the use of solders for high temperature applications is the Transient Liquid Phase Sintered (TLPS) bonds. With bonds prepared this way, the re-melting temperature is higher than the initial bonding temperature, however the temperatures in most TLPS material systems oscillate around 400°C-600°C. Fig. 7 shows a comparison between the processing and melting temperature. The processing temperature can be understood as the temperature at which the bond is originally made while preparing a solder stack, and the melting temperature corresponds to the temperature at which the bonding material melts once the bond has been made.

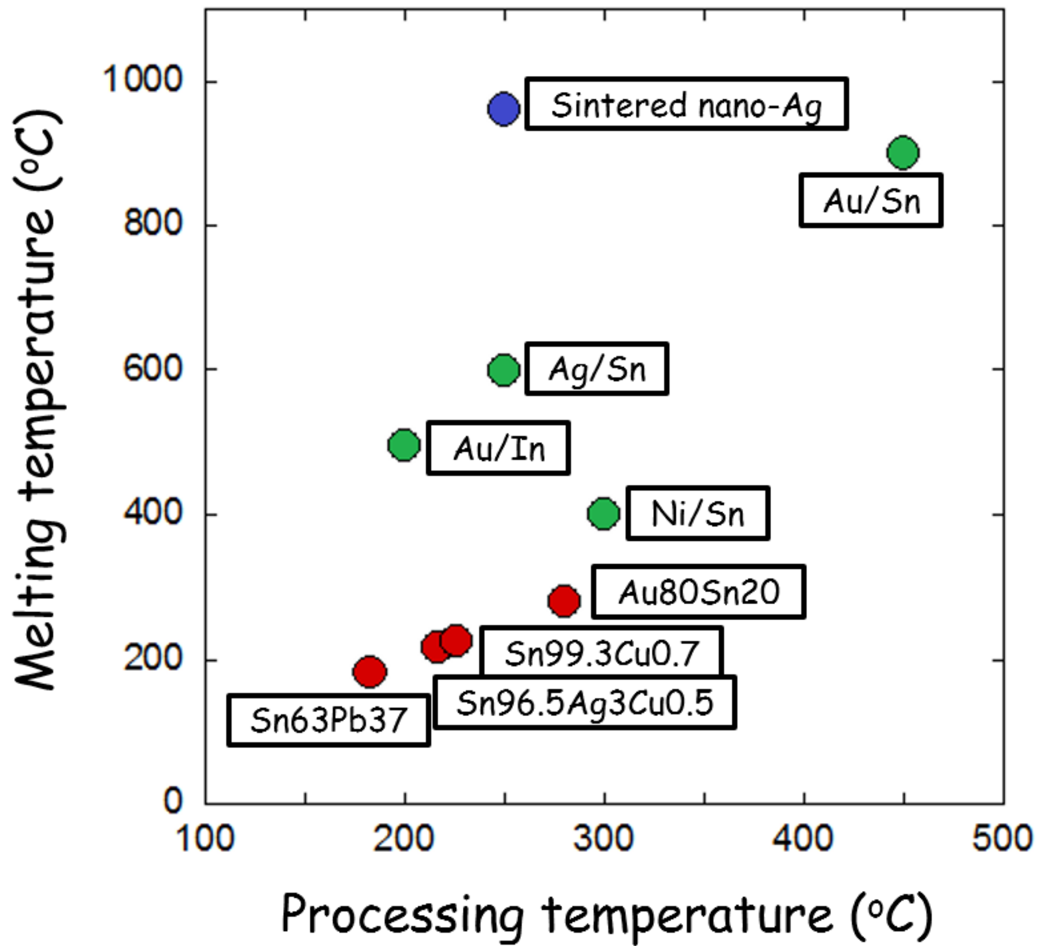

Figure 7. Melting point of die attach materials as a function of their processing temperature. The processing temperature refers to the temperature at which the solder bond is made, the melting temperature can be understood as the temperature of melting of the die attach material after the bonding has been made (Manikam and Cheong 2011, Yoon, Shiozaki et al. 2012).

It is shown in Fig. 7, that Sn-rich solder materials have low processing temperatures, around 150°C-300°C, however, the melting temperature is just as low since their melting point is the same as their processing temperature. TLPS bonds also have low processing temperatures like Sn-rich solders and a higher melting point of about 400°C-600°C.

Sintered Nano-Ag solder has a low processing temperature of 250°C and a high melting temperature of 960°C, making it an ideal candidate for high temperature applications.

2.2.3. Novel High Temperature Solders

The growing need for improved performance in electric vehicles and electronic devices is pushing the boundaries in the research of power electronics specifically trying to suit electronic packages to the high operating temperatures of such devices (Yoon, Shiozaki et al. 2012).

Commonly used die attach technologies have a very short lifetime at high temperatures since the maximum operating temperature of these devices exceeds the melting temperature of die attach solders (Yoon, Shiozaki et al. 2012). Packaging plays an important role in optoelectronics, power electronics and communication systems and hence materials should be able to withstand elevated temperatures and provide support to the package (Manikam and Cheong 2011). Hence the requirements in these devices has led efforts to develop and evaluate novel materials for die attachment. Some of the commonly used alternatives for high temperature die attach materials will be described in the following sections.

2.2.3..1. Au-based Systems

Au based solders are hard solders that have a low processing temperature and high strength, and they have good resistance to creep during thermal fatigue (Lee, Wang et al. 1993). Eutectic Au-Sn solders have a melting temperature of 280°C. Recent advances in microelectronics along with RoHS legislation have increase the number of applications for

Au-Sn solders. Eutectic Au-Sn solder has good mechanical strength and thermal (57W/Mk) and electrical conductivities and has the advantage that it can be used without flux during reflow. However this material has the disadvantage of having an elevated cost (Hartnett and Buerki 2009). However, eutectic Au-Sn solders are brittle due to the formation of intermetallics (Ivey 1998).

Chidambaram et. al (Chidambaram, Hald et al. 2010) explored Au-Ge solders as a possible alternative for high-temperature solders, due to its low tendency to form intermetallics with a eutectic melting point of 360°C. The as-prepared solder alloy was soft and became softer after thermal aging at 150°C for 1 day. Increasing the aging temperature from 150°C to 200°C, the solder became even softer as indicated by microhardness testing. Added drawbacks in the Au-Ge material system includes high cost of Au, and the difficulty in electrodepositing Ge at commercial scale.

2.2.3..2. Transient Liquid Phase Sintering (TLPS)

TLPS is a method that can withstand temperatures higher than its process temperature (Welch, Chae et al. 2005). It does this through a combination low temperature melting solder and diffusion bonding with a high melting temperature second phase (Yoon, Glover et al. 2013). Although a disadvantage would be, if the film quality is poor, the solder would lead to voiding, making it impractical for some packages (Welch, Chae et al. 2005).

TLPS process can be split up in 4 stages (Mustain, Brown et al. 2010). At first, the high melting temperature metal and the low melting temperature metal interlayers come in contact. Once the bond is heated, the low melting metal melts and reacts with the high

melting temperature metal. The molten phase is consumed by the formation of IMC and the bond is now completely solidified. The last step involves additional heating for diffusion to aid in reducing unreacted phases in the microstructure.

Among the disadvantages of the TLP bonding technique we found that it requires several hours for bonding and it works good only with fast diffusor materials. For age-hardening alloys, a post-bonding heat is required (MacDonald and Eagar 1992). Moreover, damage to the substrate's surface has also been reported as a result of the TLP bonding process due to long exposures to high temperatures (Gale and Butts 2004).

2.2.3..3.Nano-Ag Solder

Nano-scale particles have extremely high surface to volume ratio. Due to this reason they tend have lower processing temperatures than their bulk counterparts. Bulk silver has good thermal and electrical conductivity and could prove to be a good candidate for nanoscale particle sintering (Manikam and Cheong 2011). Work by Lu et. al. (Lu, Calata et al. 2007) shows sintered nano-Ag solder paste, sintered without pressure, as a die attach material with excellent thermal (240W/Mk) and electrical conductivities (41MS/m) (Scheuermann 2009) as well as superior mechanical strength. A usual concern in joint reliability is the formation of IMCs that embrittle the interfaces between solders and substrates, in the case of the sintered joint this is not a problem since it is single phase.

- Nano-Ag Sintering process

Sintering is a heating process that causes compacted particles to bond while in the solid state resulting in a densified bond with an increase in mechanical properties and thermal and electrical conductivities (Kingery, Bowen et al. 1976).

Sintering of nano-Ag solder paste is a solid-state process since there's no melting or phase transition during sintering. Melting point of bulk silver is 961°C, however, nano-Ag particles melts at much lower temperatures making low temperature sintering feasible. In the first stage of sintering, particles re-arrange thus giving a higher particle-particle contact leading to the formation of necks between particles (Bell, DiAntonio et al. 2002, Zheng 2012). In the second stage, the initial porous structure becomes smooth and an interconnected structure forms between the particles giving larger grains and thus decreasing the number of grains. Densification takes places by the decrease in cross-sectional area of the pores (Mayo 1996, Zheng 2012). The densification rate is dependent on particle size (Scherer 1977), hence the use of nano-Ag particles. On the third and final stage, pores start to close and grain growth occurs during this stage (Zheng 2012).

- Reliability of Sintered Nano-Ag solder joints

Power electronic devices are required to perform reliably at high operating temperatures and high currents for several operating cycles. To evaluate the reliability, accelerated thermal cycling and power cycling experiments are considered as standard evaluation tests. In work done by Bai et al. (Bai, Yin et al. 2007) samples were thermal cycled from 50°C to 250°C, and the sintered nano-Ag bond was able to withstand 4000 cycles before failure.

In additional work by Lu et al.(Lu, Calata et al. 2007) it was shown that after 600 thermal cycles, form -40°C to 150°C, the shear strength of the sample decreased from an average of 25 MPa to 20 MPa (after thermal cycling), which is a mere 20% drop.

Thermal and power cycling tests have demonstrated that sintered nano-Ag has a better thermal fatigue resistance than Pb-free and Sn-Pb solders (Amro, Lutz et al. 2005, Scheuermann 2009). In work done by Scheuermann (Scheuermann 2009) it was seen that a sintered nano-Ag power module had a lifetime of over 69,000 cycles of failure after being cycled from 0 to 209A, in comparison, power modules with a Sn-Ag solder layer had a lifetime of 40,000 cycles under the same testing conditions.

Nano-Ag solder is easy to apply to the substrates using several methods for example, dispensing (Mertens, Rudzki et al. 2004), stencil printing (Früh, Günther et al. 2010) and dipping (Yato, Nakajo et al. 2011). Furthermore, no liquid-phase transition occurs hence the Si die doesn't move during sintering (Scheuermann 2009). An improved reliability can be expected on sintered nano-Ag solder due to these characteristics. Among the disadvantages of the use of nano-Ag solder we find that an appropriate metallization layer on the bonding side of the substrates is essential for a strong bond (Siow 2014), the escalating price of silver (Siow 2012) and the large porosities present in the pressure-less sintered layers (Bajwa 2015).

2.2.4. Failure Mechanisms of Power Electronic Devices

A traditional power module was described in Fig. 5. It is fabricated using different materials with different coefficient of thermal expansion (CTE). During service, the

package undergoes temperature changes, thus subjecting the different materials to thermal stresses resulting in the failure of the electronic package (Lu, Bailey et al. 2009).

The weakest links in a wire-bonded power module are (Teodorescu, Blaabjerg et al. 2011):

- Wire-bond chip interconnection
- Chip-DBC solder joint
- DBC-base plate solder joint

The solder joint fatigue is the main failure mechanism in power modules, which is caused by the large mismatch in the CTEs between the chip, solder and DBC layers. Work by Mitic et al. (Mitic, Beinert et al. 1999), shows crack formation on the Cu layer of an Cu-AlN-Cu DBC substrate and on the chip after being cycled from -55°C to 155°C, where Cu cracks were the result of thermal cycling damage. However, this uncommon failure is not expected to affect the lifetime of the module (Ciappa 2002).

In accelerated thermal and power cycling, the sample experiences strains and stresses being inflicted on the multiple layers that form the electronic package leading to the failure of the module (Lu, Bailey et al. 2009).

2.2.5. Characterization of Thermal Induced Damage

Traditional methods of characterizing thermal induced damage on die attach solders in power modules involve the analysis of sample cross-sections in a scanning electron microscope (SEM) after thermal cycling. Work by Jiang et al. (Jiang, Lei et al. 2014) studies the microstructural degradation of SAC305, SN100C and sintered nano-Ag solders after thermal cycling from -40°C to 150°C. In this work crack propagation was observed

in the solder samples whereas no crack formation was observed for nano-Ag samples cycled under the same conditions. This was characterized post-mortem by destructive cross-section analysis. Work by Bai et. al (Bai, Calata et al. 2006) studied the degradation of solder during thermal cycling by studying the decrease on the shear strength of the die attach nano-Ag solder after thermal cycling from 50°C to 250°C. Chuang et al. (Chuang and Lee 2002) used Scanning Acoustic Microscopy (SAM) to study the reliability of Ag-In solder after continuous storage in an oven at 500°C. even though SAM is a non-destructive technique, the lateral resolution is not sufficient to resolve microcracks forming during accelerated reliability testing.

Due to the destructive nature of these techniques, cross-sectional analysis and shear testing analysis and the poor resolution of SAM analysis is it impossible to visualize and quantify damage evolution as a function of time within the same sample. For this, is it important to use non-destructive techniques which have been proven to be excellent to evaluate time-resolved, quantitative understanding in several materials systems. Work by Mertens et al. (Mertens, Kirubanandham et al. 2016) used 3D X-ray tomography to study the electromigration mechanisms in Sn-0.7Cu solders to clearly show damage evolution as a function of time and also quantify amount IMC formed due to electromigration.

2.3. Research Objectives

With the critical issues discussed with regards to Tin whiskers and Thermal cycling reliability of sintered nano-silver solder, this research focuses on the following objectives:

- Sn whiskers:
  1. Probe the driving force of whisker formation by in situ nanoindentation and characterize the crystal orientation using electron backscattered diffraction.
  2. Studying long-term whisker/hillock growth in Tin film plated on Copper using in situ nanoindentation under vacuum.
  3. Assess the mechanical properties of the Tin film using micropillar compression technique.
- Nano-Ag solder:
  1. Characterize sintered nano-Silver bonds and evaluate their mechanical properties.
  2. Develop fundamental understanding of thermo-mechanical behavior of nano-silver TIM.
  3. 3D microstructural evolution using X-ray tomography by analysis of voids, cracks and delamination.
  4. Evaluate thermal cycling performance at various temperature ranges (ΔT).

3. EFFECT OF CRYSTAL ORIENTATION AND MICROSTRUCTURE ON THE NUCLEATION AND GROWTH OF SN HILLOCKS BY *IN SITU* NANOINDENTATION.

3.1 Overview

For several decades, tin whiskers have been a major reliability issue in the microelectronics industry. These single crystalline tin filaments can grow long enough to cause short circuiting and device failure. Although tin whisker/hillock growth is driven by compressive stresses, a mechanistic model of their formation, evolution, and microstructural influence has not been fully developed. In this work, the growth of mechanically induced tin whiskers/hillocks was studied using an *in situ* nanoindenter and Electron Backscatter Diffraction (EBSD) in a dedicated scanning electron microscope (SEM). Electroplated Sn-on-Cu samples were indented and monitored in vacuum to study their growth behavior without the influence of atmosphere. Aging experiments were conducted to study the effect of intermetallics on hillock growth. The grain orientation of the hillocks and the plastically deformed area surrounding the indentation were studied on slabs lifted out of the sample with the use of Focused Ion Beam (FIB). High angle grain boundaries were seen to favor the formation of Sn hillocks. An FEM model was developed to study the evolution of the compressive stress state in the Sn plating and the results showed good agreement with the experimental results.

3.2 Introduction

Tin whiskers have been a serious industrial concern in microelectronic packaging for several decades. Tin whiskers are single crystalline filaments that grow because of a variety of factors, including the relief of compressive stresses (Tu 1994), recrystallization processes that affect the microstructure of the electroplated films (Sampson Michael 2009), and an applied electric field at high humidity, that favors whisker growth due to migration of tin atoms to reduce the energy gain from formation of electric dipoles (Karpov 2015, Vasko, Grice et al. 2015). Sn whiskers have been reported to grow with different morphologies, with the most common being single crystalline filaments with high aspect ratio. Other morphologies of Sn whiskers include single crystalline nodules or hillocks which have relatively low aspect ratio (Schlesinger and Paunovic 2000). Following the requirement to eliminate the use of Pb in electronic devices by the Restriction of Hazardous Substances (RoHS) (Warwick 1999) and the implementation of Pb-free solders, Sn whiskers have been considered a major reliability issue because of the fact that that they can grow long enough to cause short circuits in fine pitch electrical components (Williams, Chapman et al. 2012).

Over the years, numerous investigations have proposed mechanisms describing the growth behavior of tin whiskers. Several factors act as sources of compressive stresses, such IMC formation (Weil 1971, Boettinger, Johnson et al. 2005, Xu, Zhang et al. 2005), applied mechanical stresses (Xu, Zhang et al. 2005, Shibutani, Yu et al. 2006), electromigration (Tu, Chen et al. 2006), corrosion/oxidation (Tu 1994), thermal expansion and thermal cycling (Boettinger, Johnson et al. 2005). Work done by Tu et al. (Tu 1994) concluded that

weak spots in the oxide film on the tin surface acts as stress relief spots for whisker growth. Alternatively, grain boundary diffusion of Sn atoms has been suggested as the dominant mechanism for stress relief, usually in thin Sn films. Diffusion of Cu metallization into the Sn plating forms IMC phases (Cu_6Sn_5 and Cu_3Sn) which generate compressive stresses that continue growing over time resulting in whisker formation (Jadhav, Buchovecky et al. 2010). An investigation by Boettinger et al. (Boettinger, Johnson et al. 2005) concluded that recrystallization of Sn grains occurs at the film surface through grain boundary diffusion and segregation of tin atoms, thereby forming whiskers. However, a single mechanism that clearly describes the growth mechanism has not yet been established.

Indentation has been used to induce local controlled plastic deformation and accelerating whisker nucleation and growth (Lin, Yorikado et al. 2007, Williams, Chapman et al. 2012, Kang, Chang et al. 2013). Work done by Lin et al. (Lin, Yorikado et al. 2007) showed that mechanical loading induces formation of grains due to recrystallization, that are elongated horizontally and favor whisker growth due to diffusion of tin atoms through grain boundaries. Mechanically induced whisker growth by indentation has been studied in the past using large indenters (900 μm ZrO_2 ball indenter (Lin, Yorikado et al. 2007, Doudrick, Chinn et al. 2015) and large loads (>100 gf (Lin, Yorikado et al. 2007, Kang, Chang et al. 2013, Doudrick, Chinn et al. 2015, Vallabhaneni, Izadi et al. 2017)). Large indentations results in a large plastic zone spanning several grains. While it is an excellent technique for generating large whiskers, it is not suitable for studying individual grain orientation effects. To obtain a localized stress field, the indentation size needs to be much smaller, i.e., comparable to the microstructural features. Nanoindentation is a versatile technique that

has been used extensively to study the mechanical properties of materials in the nanoscale. Williams et al. (Williams, Chapman et al. 2012) used this technique to correlate the growth rate of hillocks with stress relief using an *in situ* nanoindenter in a scanning electron microscope. The evolution of Sn nodules (or hillocks) was observed *in situ*, for periods of over 1200 hours. Additionally, Dudek et al.(Dudek and Chawla 2009) used nanoindentation for rare earth (RE) containing solders and showed that the oxidation of RE IMC caused whisker formation and that the whiskers density was enhanced by indentation.

Due to its small indentation size, nanoindentation can be used to probe the effect of crystallographic orientation of Sn grains on whisker growth. β-Sn is highly anisotropic because of its body-centered tetragonal crystal structure. Whisker growth is a diffusion-dependent process and it has been seen that grain boundaries act as fast diffusion pathways for Sn atoms to facilitate the growth of whiskers (Lin, Yorikado et al. 2007). In some cases, twinned grains form as a result of mechanically induced recrystallization and act as stable roots for whisker growth (Mizuguchi, Murakami et al. 2012).

Oxidation alters whisker growth behavior by inducing compressive stresses through diffusion of oxygen in Sn, or by corrosion of the surface (Hillman, Kittlesen et al. 2011). Formation of weak spots in the oxide layer would enhance the nucleation and growth of whiskers (Tu 1994). In order to isolate these effects, indentation needs to be done in a controlled atmosphere such as vacuum. *In situ* nanoindentation technique in a scanning electron microscope is best suited to induce localized compressive stresses in vacuum, especially for thin films, because it provides a means for controlling environment as well as studying growth mechanisms in real-time.

In this work, state-of-the-art *in situ* nanoindentation technique was used to induce localized controlled compressive stresses and investigate whisker/hillock growth in a controlled environment inside an SEM vacuum chamber. The combined influence of applied mechanical stress and IMC formation was studied through isothermal aging and nanoindentation. In addition, the relationship between crystal orientation, grain boundaries, and hillock growth was investigated using FIB lift-out and Electron Backscatter Diffraction (EBSD).

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3.3 Materials and Experimental Procedure

3.3.1 Sample Preparation

The test vehicle used for this study was an electroplated Sn film on an oxygen-free high conductivity (OFHC) Cu pellet (McMaster-Carr, Cu alloy 101, Rockwell F84-94, 9.5 mm diameter, 3 mm thick). The pellets were cut precisely from a Cu rod using Electrical Discharge Machining (EDM). The pellets were polished to final finish of 0.3 μm Alumina and 0.05 μm colloidal silica solutions. The Cu pellet serves as the cathode and a tin cube (99.99%, Indium Corp., polished and cleaned similar to the Cu) was used as the anode. The

tin cube was partly exposed to the electrolyte with an exposed area of 50 mm^2 to maintain a current density of 212 A/m^2. The electrolytic solution was sulfate based with commercial brightening agents (Electrochemical Products Inc., E-Brite 180B and 180M). Electrolytic deposition was done for 15 minutes to obtain a Sn film thickness of about 7-8 μm. Film thickness measurement was measured using optical profilometry (Bruker Dektak XT) and focused ion beam (FIB) (FEI NOVA 200 NanoLab FEGSEM/FIB) cross-sections. The polishing procedure used for FIB cross-sectioning is discussed in detail in the FIB section below. To remove any residual contamination after electroplating, the sample was polished gently using 0.05 μm colloidal silica for 15 to 20 seconds without damaging the sample's surface. Following this, to minimize the formation of a thick oxide layer, the samples were loaded immediately in the SEM for *in situ* nanoindentation. To study the evolution of IMC, a set of samples was thermally aged at 150° C in a box furnace for different periods of time and the layer thickness was measured using FIB cross-sections.

3.3.2 Focused Ion Beam (FIB) and Electron Backscattered Diffraction (EBSD)

To study the microstructure and the grain orientation of the samples, slabs were lifted out from the region of interest using FIB lift-out technique. Slab lift-out was done using a dual beam FEI Focused Ion Beam NOVA 200 NanoLab FEG-SEM/FIB. Fig. 8 (a-d) illustrates the procedure followed. As a first step, a thin layer of platinum was deposited to minimize ion beam damage on the sample surface. A Ga^+ ion beam at an accelerating voltage of 30 KeV was used to mill trenches on both sides of the area of interest, in our case, the indentation (Fig. 8 (a)). A current of 7 nA was used to mill the trenches. After milling the trenches, a tungsten needle was welded to the top part of the slab using platinum. Then,

using the ion beam, the slab was cut off from the base, along the sides and bottom, after which it was lifted-out and placed on a Transmission Electron Microscopy (TEM) Cu grid (Fig. 8 (b)). Next, the needle was cut off from the slab using the ion beam (Fig. 8 (c)). As a final step, the slab was polished using the ion beam (Fig. 8 (d)) using currents from 1 nA to 50 pA.

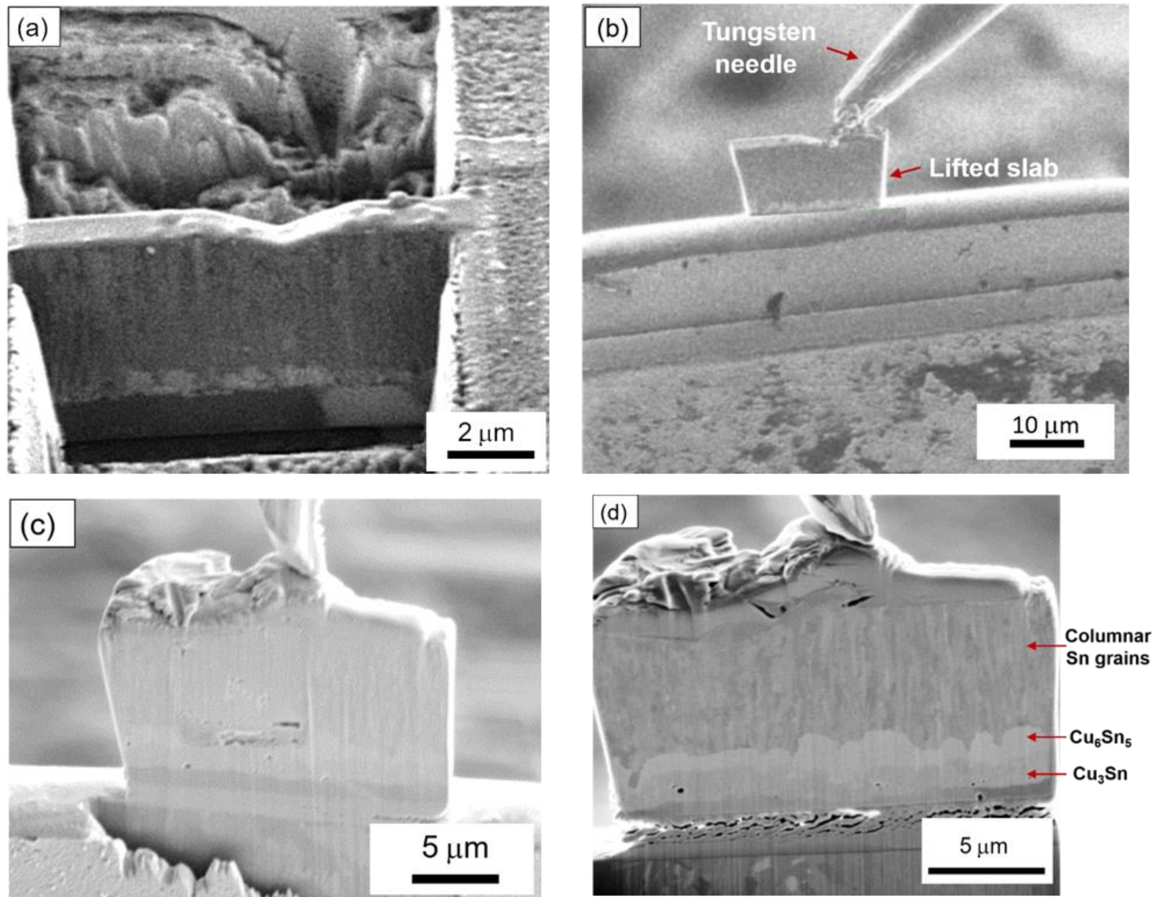


Figure 8. (a) Milled trenches on either side of the indentation zone to obtain a slab, (b) Tungsten needle welded to the slab for lift-out and placing on a Cu TEM grid, (c) Cutting of the tungsten needle using ion beam after welding the slab to the Cu grid, (d) Ion channeling image of the slab after final polishing in FIB.

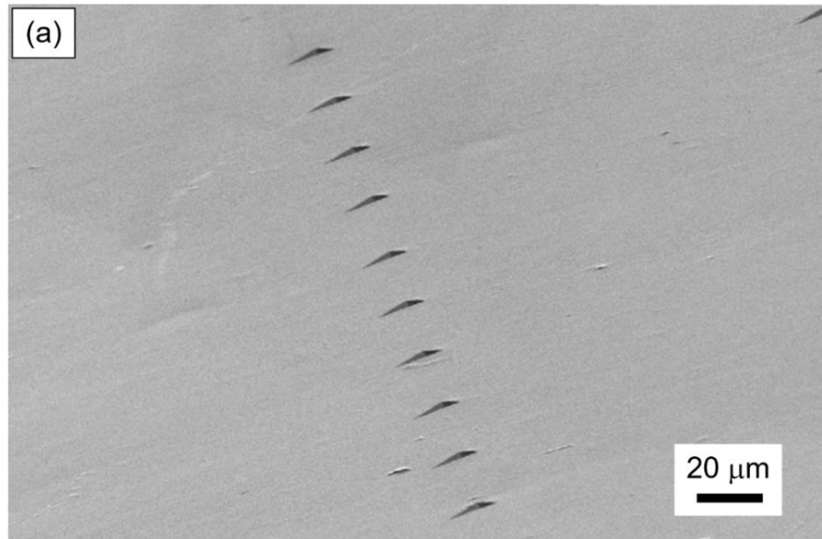
The JEOL SEM described previously is also equipped with an EBSD system (TSL™-EDAX, Mahwah, N.J.) for crystallographic orientation analysis. Orientation Image Mapping (OIM) was conducted with a step-size of 0.3 μm on the entire cross-section of the slab. OIM maps were analyzed using TSL OIM Data Collection and Analysis software. Raw OIM data often contains noise pixels due to sample surface artifacts, which were cleaned using 'Neighbor CI correlation' and 'Grain Dilation', as previously done by Kirubanandham et al. (Kirubanandham, Lujan-Regalado et al. 2016).

To analyze and quantify the Sn grain structure, the OIM maps were imported in to commercial image analysis software AVIZO® (FEI, VSG, Hillsboro, USA) for image segmentation. By converting the color OIM map to an 8-bit gray scale image, grains were segmented using a 'Magic Wand' tool, which segments a single grain based on a selected gray value range. By referring to OIM phase maps, the Cu, Cu_6Sn_5 and Cu_3n phases were omitted and only the Sn grains were segmented for quantification purposes. These segmented images were used to calculate the aspect ratio and the distribution of the grains and hillocks in the deformed areas of the Sn film.

3.3.3 I*n Situ* Nanoindentation

A SEM (JEOL JSM-6100 SEM) with an *in situ* nanoindentation stage (Nanomechanics Inc., Oak Ridge, TN) was used to perform the nanoindentation experiments (Williams, Chapman et al. 2012). For nanoindentation, the sample was mounted on a 76° SEM stub with respect to the electron beam. A linear array of 10 indentations with a spacing of approximately 100 μm was made on the surface of the sample, as can be seen in Fig. 9 (a). The indentation was performed with a Berkovich tip using a load of 15 mN with a hold

time of 10 seconds. A loading rate of 3 mN/s was used. Fig. 9 (b) shows a typical load vs displacement curve where 3 stages can be observed: loading, hold, and unloading. After indentation, the samples were kept in vacuum for monitoring hillock growth and to avoid any oxidation.



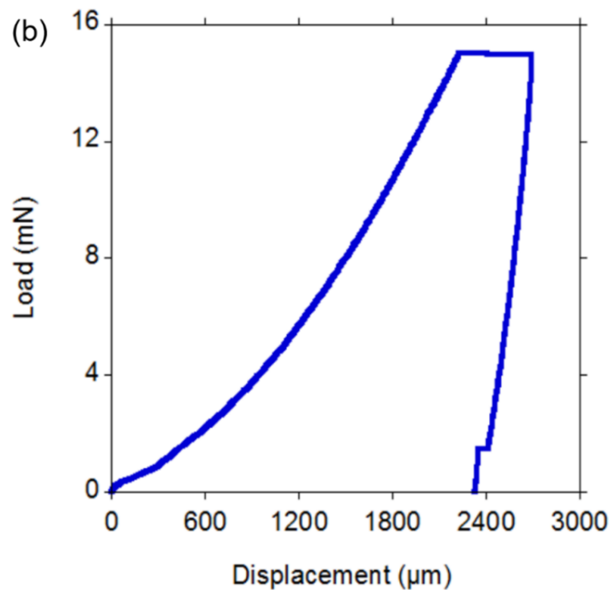


Figure 9.(a) SEM image of a linear array of indentations with 100 µm spacing (viewed at 76°) (b) Typical curve of load vs displacement obtained during nanoindentation. The three stages of indentation can be seen – Loading up to 15 mN, followed by holding for 10 seconds and unloading.

3.3.4 Micropillar Compression

Grain boundaries in crystals present an intriguing mystery in the materials sciences because of a lack of reports on their atomic structure, morphology, and deformation properties (Aitken, Jang, Weinberger, & Greer, 2014). For this work, micropillar compression was used to study the deformation behavior of polycrystalline Sn pillars.

Three different sizes of pillars were milled using FIB in a 20 μm thick electroplated Sn sample, 3 Sn grain sizes will be studied. Pillar fabrication, post-compression imaging and cross-sectioning was made on a dual beam operated at 30 keV ion beam accelerating voltage, which provides a high milling rate, and 5 keV electron beam accelerating voltage, which provides high imaging resolution (Mayer et al., 2016). Pillar fabrication was performed using an annular milling procedure. Pillars were milled with dimensions 5 x10 μm, 3 x 6 μm and 2 x 4 μm (diameter by height) with a spacing of minimum 20 μm surrounding the pillar to allow clearance for the nanoindenter. Five pillars were made for each size. These pillar sizes were used to study the pillar size effect on observed yield strength. Different ion beam currents will be used depending on the Sn removal rate and precision needed, but final polishing of the surfaces was always be carried out using ion currents below 50 pA.

Pillar compression was carried out using a commercial nanoindenter (Nanoindenter XP-II, Agilent) equipped with a diamond flat punch. Tests were performed with an approximate strain rate of $3 \times 10^{-3}\ s^{-1}$. After pillar compression, EBSD analysis of the cross-sections of the pillars were performed to observe the deformed microstructure.

3.1 Results and Discussion

3.1.1 Intermetallic Compound (IMC) thickness evolution

It is well known that the presence of IMC formation at the Cu-Sn interface has a strong influence on whisker/hillock growth by contributing to the build-up of compressive stresses. Formation of IMCs at the interface due to the reaction between Cu and Sn atoms results in a volume increase which causes compressive stress to build-up in the Sn film (Illés, Horváth et al. 2010). Fig. 10 shows a FIB cross-section of an electroplated Sn sample that was aged for 72 hours at 150°C. Here, the contrast between the layers gives a clear picture of the IMC phases that form at the Cu-Sn interface. Cu_3Sn forms next to the copper substrate and has a planar growth front, while Cu_6Sn_5 forms as nodules growing through the Sn layer.

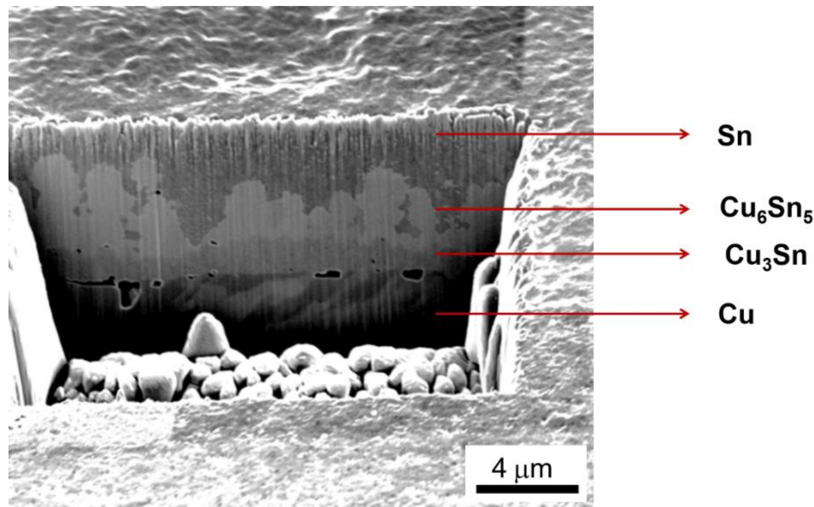


Figure 10. FIB cross-section through the thickness of the sample showing different phases after being aged at 150°C for 72 hours.

Cu_6Sn_5 IMC grew with a nodular morphology from the Cu interface. The average thickness of Cu_6Sn_5 was 3.4 ± 0.6 μm. Cu_3Sn IMC grew with a planar front and had a mean thickness of 1.4 ± 0.3 μm. On the as-plated sample however, no discernible intermetallic layer was observed (Fig. 12 (a)).

To study the growth kinetics of the IMC layers, a set of aging experiments was conducted. Electroplated Sn samples were prepared using identical plating conditions as described previously and aged at 150°C in a box furnace. The samples were removed at regular intervals and the thickness of the IMC was measured using FIB cross-sectioning and SEM imaging for a total aging time of 500 hours, as shown in Fig. 11.

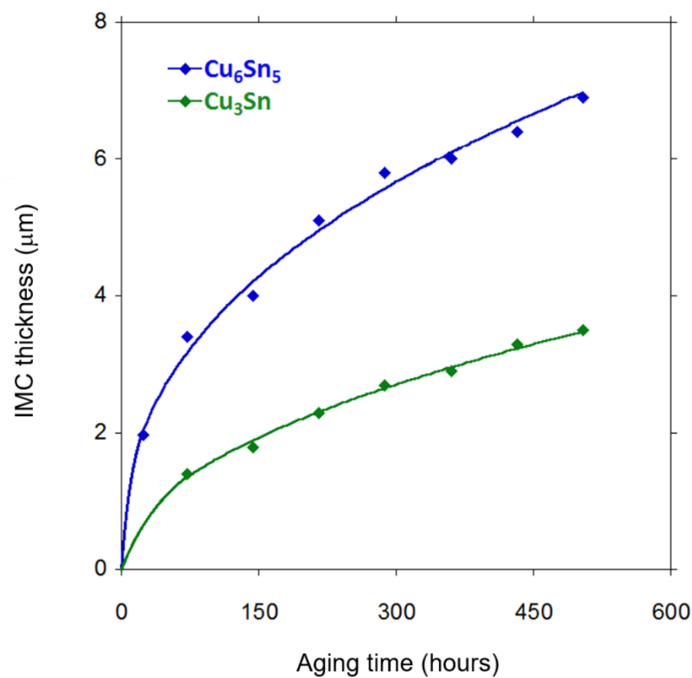


Figure 11. Total intermetallic thickness as a function of aging time at 150°C. The growth exponents indicate that Cu_3Sn forms through bulk diffusion and Cu_6Sn_5 forms through a mixed grain boundary and bulk diffusion mechanism.

The diffusion kinetics of the growth of Cu_6Sn_5 and Cu_3Sn IMC layers follows an Arrhenius relationship (Hsiao, Liu et al. 2012),

$$h = kt^n$$

where h is the thickness of the IMC, k is the coefficient of growth rate and n is the growth exponent which indicates the type of diffusion occurring during IMC growth. The theoretical value for growth exponent is, n=0.33 when diffusion is grain boundary controlled (Gusak and Tu 2002), and n=0.5 when the IMC growth occurs through bulk-diffusion mechanism (Li, Mannan et al. 2006).

In this study, the growth exponents for the Cu_6Sn_5 and Cu_3Sn intermetallics were 0.4 and 0.48 respectively. These values suggest that the Cu_3Sn phase forms through a bulk diffusion mechanism, hence the planar morphology and that the Cu_6Sn_5 phase forms through a mixed grain boundary and bulk diffusion mechanism. Work done by Deng et al. (Deng, Piotrowski et al.) showed a comparable value of 0.41 for Cu_6Sn_5. However, the Cu_3Sn growth exponent was reported as 0.36 indicating grain boundary diffusion. This difference could be the result of different microstructures due to fabrication technique i.e. reflow process used in Deng's work resulting in large Sn grains vs electroplating method used in current work which produces small columnar grains. Additionally, the solder joint in Deng's work was reflowed at 240°C for 40 seconds which forms a thick initial IMC layer. The presence of an initial thick IMC layer slows down the diffusion process and since electroplated Sn films very little IMC formation prior to aging, the calculated growth exponent for electroplated Sn is higher.

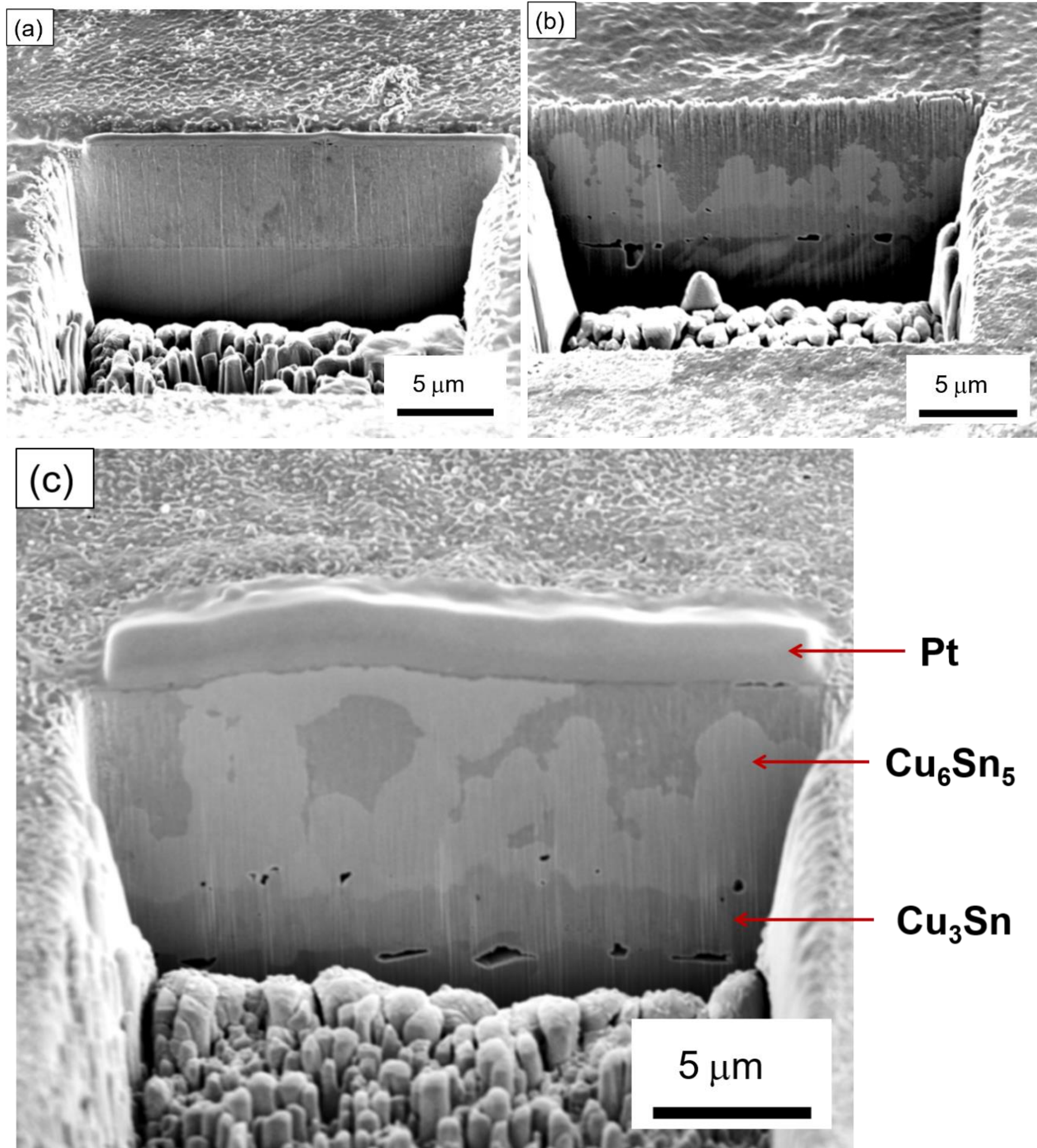


Figure 12. IMC evolution at different aging times, (a) As-plated, (b) 3 days aged, (c) 15 days aged. After 15 days in can be seen that the Cu_6Sn_5 nodules extended through the entire thickness of the electroplated Sn.

The evolution of the IMC thickness due to aging can be observed in Fig. 12 (a-c). Here we can observe that no IMC discernible formation of Cu_6Sn_5 can be seen on the as-plated sample. As aging progresses, Cu_6Sn_5 IMC grows with a nodular morphology, which can be observed after 3 days in Fig. 12 (b). After 15 days of aging, some of the Cu_6Sn_5 nodules spanned the thickness of the Sn plating forming a layer just below the platinum layer deposited prior to FIB cross-sectioning.

3.1.2 In Situ Nanoindentation

To study the influence of mechanically induced compressive stresses on whisker/hillock growth, two types of samples were used for nanoindentation: as-plated and aged. Fig. 13 (a) shows the surface of an as-plated sample immediately after nanoindentation in vacuum (day 0) and after being kept in vacuum for 20 days in Fig. 13 (b).

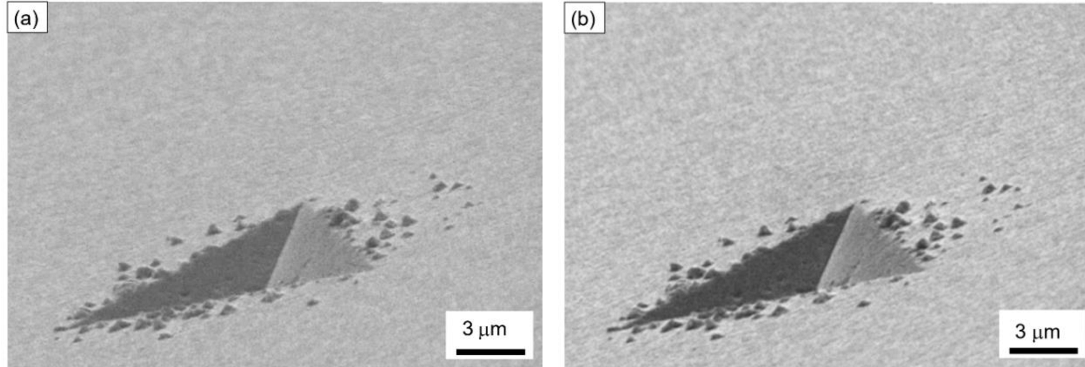


Figure 13. View at 76° of an as-plated and indented sample (a) immediately after indentation, (b) after 20 days in the SEM vacuum chamber.

Our experiments revealed the presence of several hillocks, about 100 nm in diameter, that formed instantly around the indentation. These hillocks showed no growth in vacuum for a period of 20 days. The hillocks formed only at the edges of the indentation pit suggesting

that compressive stresses may have been relieved dynamically while the indenter was still in contact with the sample surface. Nonetheless, there was no post-indentation stress relief even after 3 weeks within vacuum chamber.

Unlike the as-plated sample, the aged sample showed a more severe growth of hillocks larger than a micron in diameter (Fig. 14 (a)). Apart from the several hillocks around the indentation, there were also large faceted mounds at the indentation edge and center – these features can be observed in Fig. 14 (b). Schlesinger and Paunovic (Schlesinger and Paunovic 2000) reported these hillocks as single crystalline mounds which are also a noted growth feature and are considered as a type of whisker.

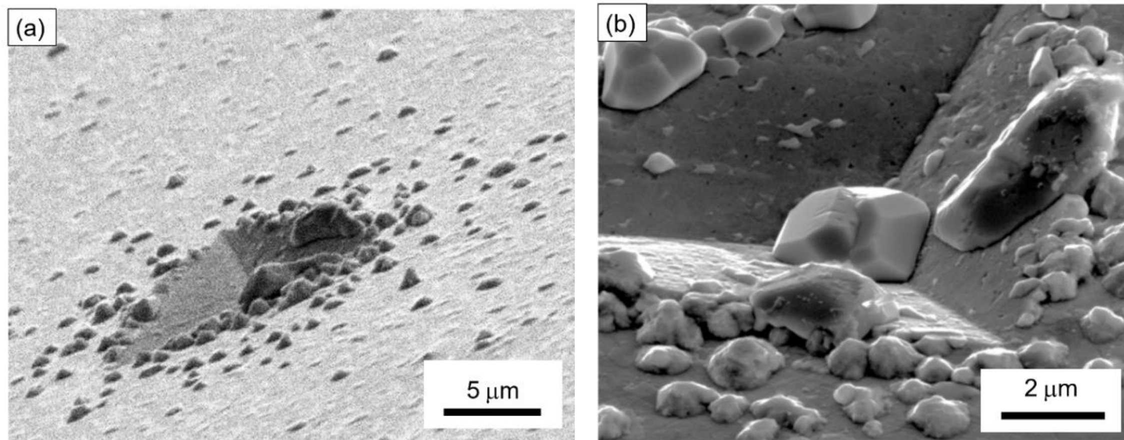


Figure 14. (a) Faceted hillocks growing right after indentation (76° view), (b) Hillocks growing in the indentation pit showing faceted structure (52° view).

After aging and indenting *in situ*, the samples were kept in vacuum to monitor hillock growth with time. Unlike the hillocks in the as-plated samples, the large hillocks in the aged sample showed some growth. Fig. 15 (a-d) show the evolution of the hillocks over a

period of 20 days kept in vacuum and the growth of the large faceted hillocks can be seen in Fig. 15 (a-b). Beyond 2 days in vacuum, the hillock growth was arrested.

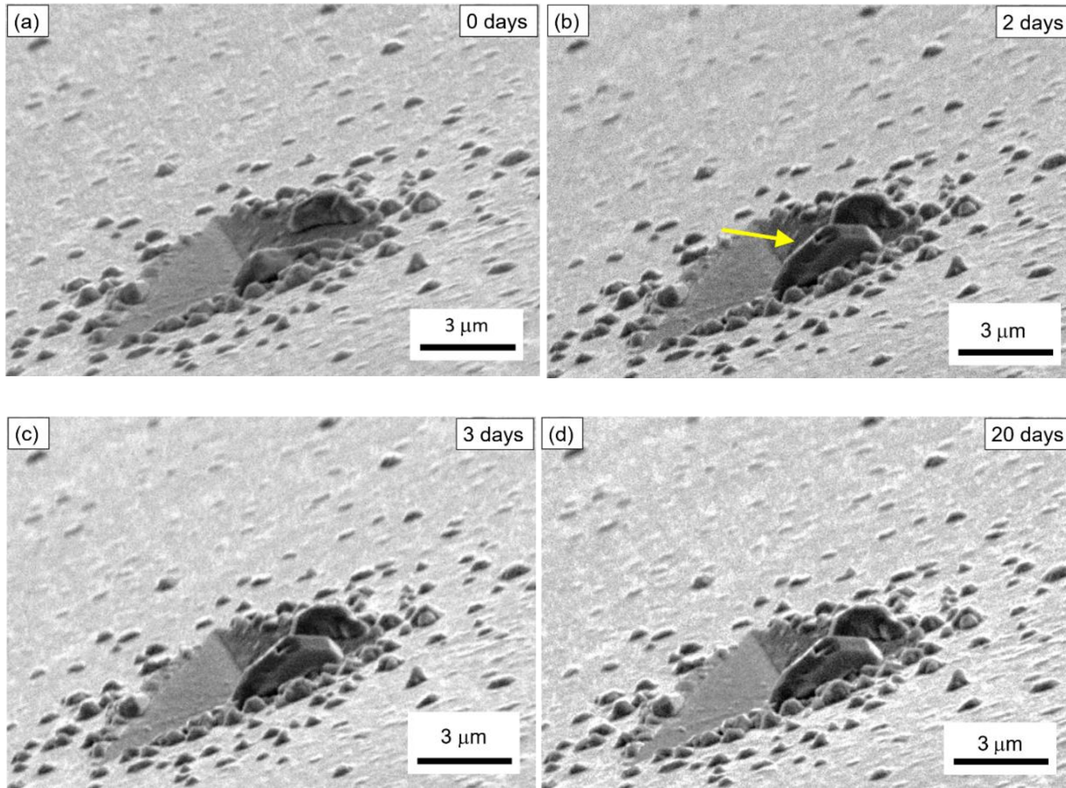


Figure 15. Hillock growth over time, (a) Right after indentation (day 0), (b) 2 days after indentation showing growth of the faceted hillocks in the indentation center, (c) after 3 days – showing arrested growth, (d) after 20 days.

Like the as-plated sample, the small hillocks surrounding the indentation in the aged sample showed arrested growth after indentation. The difference in growth of hillocks seen between the as-plated sample and the aged sample can be attributed to the thicker IMC layer found in the aged sample. The as-plated sample does not have IMCs at the time of indentation and hence experiences relatively less stress. Thicker IMC in the aged sample would generate additional compressive stress and contributes to back stress directly below

the indenter during indentation. Hence, we see that hillock growth continues at the indentation center, after the load is removed. A similar observation was seen by Williams et al.(Williams, Chapman et al. 2012), where a single large hillock grew from the indentation center and some of the hillocks showed arrested growth after 100 hours.

3.1.3 Microstructure and Grain Orientation Analysis

Ion Channeling imaging and EBSD were done to acquire the grain structure from the FIB lift-out slab. The ion channeling image shown in Fig. 16 (a) shows the different phases through the thickness of an as-plated sample as well as some contrast difference between the Sn grains. The microstructure of the electroplated tin consists of columnar Sn grains oriented perpendicular to the Cu-Sn interface with Cu_6Sn_5 IMC forming between Cu and Sn due to diffusion over time. The approximate region below the indentation zone is marked by the dotted black lines and the grains appear finer here than in the surrounding areas, suggesting possible recrystallization due to deformation. This was inferred due to the presence of an equiaxed grain structure at the deformation zone. Away from the indentation zone, the base microstructure showed the presence of elongated grains running perpendicular to the Cu-Sn interface. The mean grain size over the entire slab was 0.6 ± 0.2 μm and the mean grain size near the recrystallized zone was measured as 0.4 ± 0.02 μm. This indicates the occurrence of dynamic recrystallization. As Sn has a low melting point, it experiences high homologous temperature even at room temperature and thus forms recrystallized grains easily. Moreover, nanoindentation induces high strain in the microstructure, which would additionally favor recrystallization of new strain-free grains.

The OIM map on Fig. 16 (b) shows the grain orientation of the different phases. No preferred grain orientation was observed on the as-plated samples.

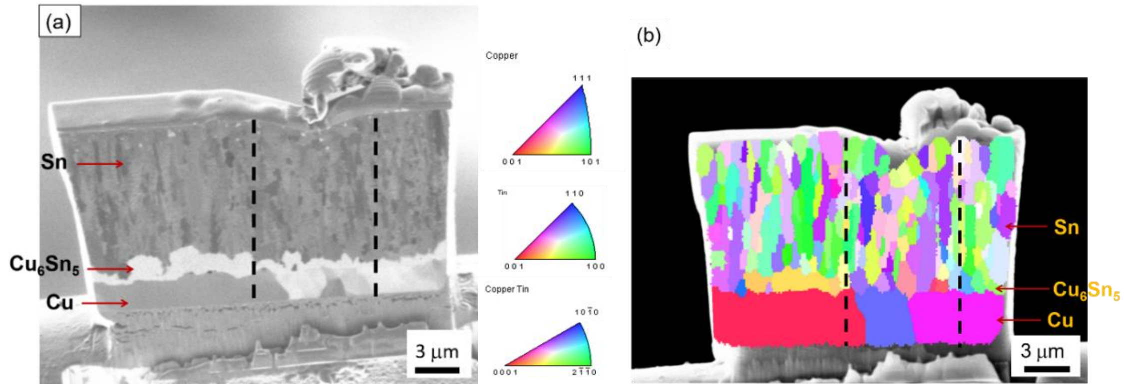


Figure 16. (a) Ion Channeling Image of an as-plated sample, the dotted lines roughly indicate indentation zone, (b) OIM map of the slab showing elongated grains away from the indentation zone and equiaxed grains below the indentation.

The aspect ratio of the grains was measured after segmenting the grains from the OIM map. For aspect ratio analysis, the grains were separated into 3 regimes based on their centroids. The slab was divided as 3 regimes from top to bottom, as shown in Fig. 17 (a). Sn grains with centroids within the top 3um height of the slab represent the grains closest to the surface. Regions 2 and 3 belong to the middle and bottom 3um height sections of the slab. The top layer, in red, has the least mean aspect ratio of about 3.2. This layer includes most of the recrystallized grains that formed due to deformation (Fig. 17 (b)). Measurements closer to the indentation marked by the vertical dotted lines have a mean aspect ratio of 2.7 ± 0.8. Whereas Sn grains away from the indentation have a higher mean aspect ratio of 3.8 ± 1.2. The middle layer was composed of the columnar grains and had the highest mean aspect ratio at 4.2. The bottom most layer also had several grains with low aspect ratio

which could be a result of nucleation at the Cu interface. The mean aspect ratio was measured as 3.4, which is slightly higher than the top layer (Fig. 17 (d)).

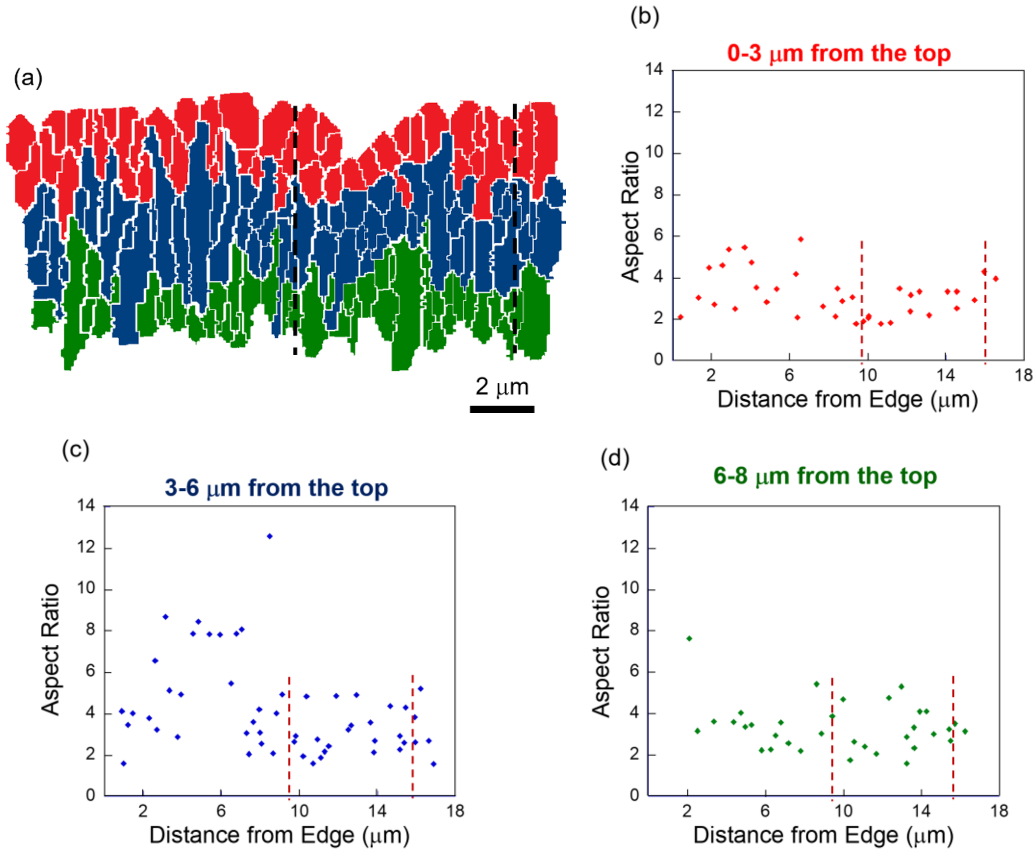


Figure 17. (a) Segmented grain structure of an as-plated slab, (b) Aspect ratio of top layer of the slab, (c) Aspect ratio of middle layer of the slab, (d) Aspect ratio of bottom layer of the slab. Grains present within the dotted line have the lowest aspect ratio in each regime.

Like the as-plated sample, slabs were lifted out from the aged sample as well. The ion channeling image and the OIM map of an aged sample are shown in Fig. 18 (a-b). Since the faceted hillocks at the edge and center of the indentation pit were larger (marked in the dotted circles in Fig. 18), it was possible to cross-section them in the FIB slab and thus able to analyze their crystal orientation.

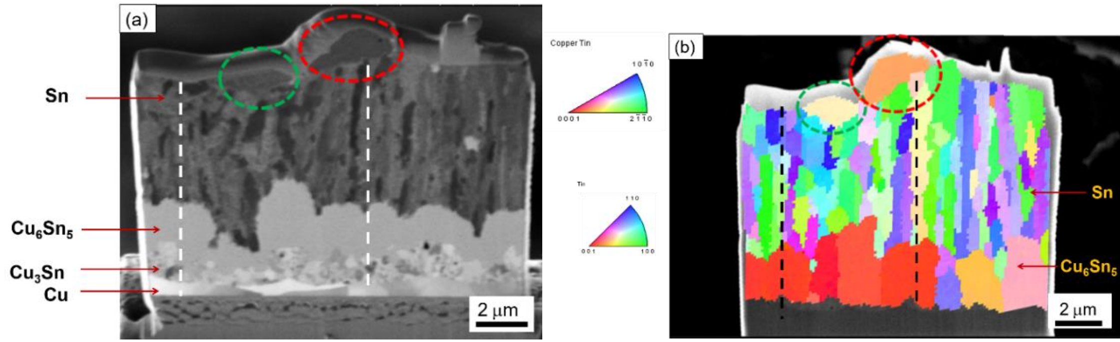


Figure 18. (a) Ion Channeling Image of an aged sample, the dotted lines roughly indicate the indentation zone, (b) OIM map of the slab showing orientation of the large Sn hillocks.

The grain structure from the ion channeling image and OIM map clearly show the recrystallization occurring due to deformation near the indentation zone, with grain sizes of about 0.4 ± 0.1 μm. This grain size is comparable to the size of the equiaxed grains formed due to deformation and recrystallization in the unaged indented sample. The presence of large columnar grains away from the indentation is also evident with grain sizes of about 0.8 μm, which is slightly coarser than the as-plated and indented sample.

Analyzing the aspect ratio of the Sn grains for the aged samples, we can observe a binary distribution of aspect ratio values. Grains near the indentation zone have a much lower mean aspect ratio compared to region away from the indentation. Since aging coarsened the microstructure, the columnar grains are larger and sometimes even span the entire thickness of the plating. Several columnar grains with aspect ratio exceeding 6 were seen in the center of the slab's cross-section. Considering the low aspect ratio grains, their presence close to the indentation zone is evident as marked by the dotted lines in Fig. 19 (a). Following the same trend as the as-plated and indented sample, the top layer is

composed of small equiaxed grains especially close to the indentation zone (aspect ratio of 2.6 ± 1.3). And the bottom layer grains have a mean aspect ratio much higher than the top layer (aspect ratio of 3.5 ± 1.5) which can be attributed to the coarsening due to aging and IMC formation.

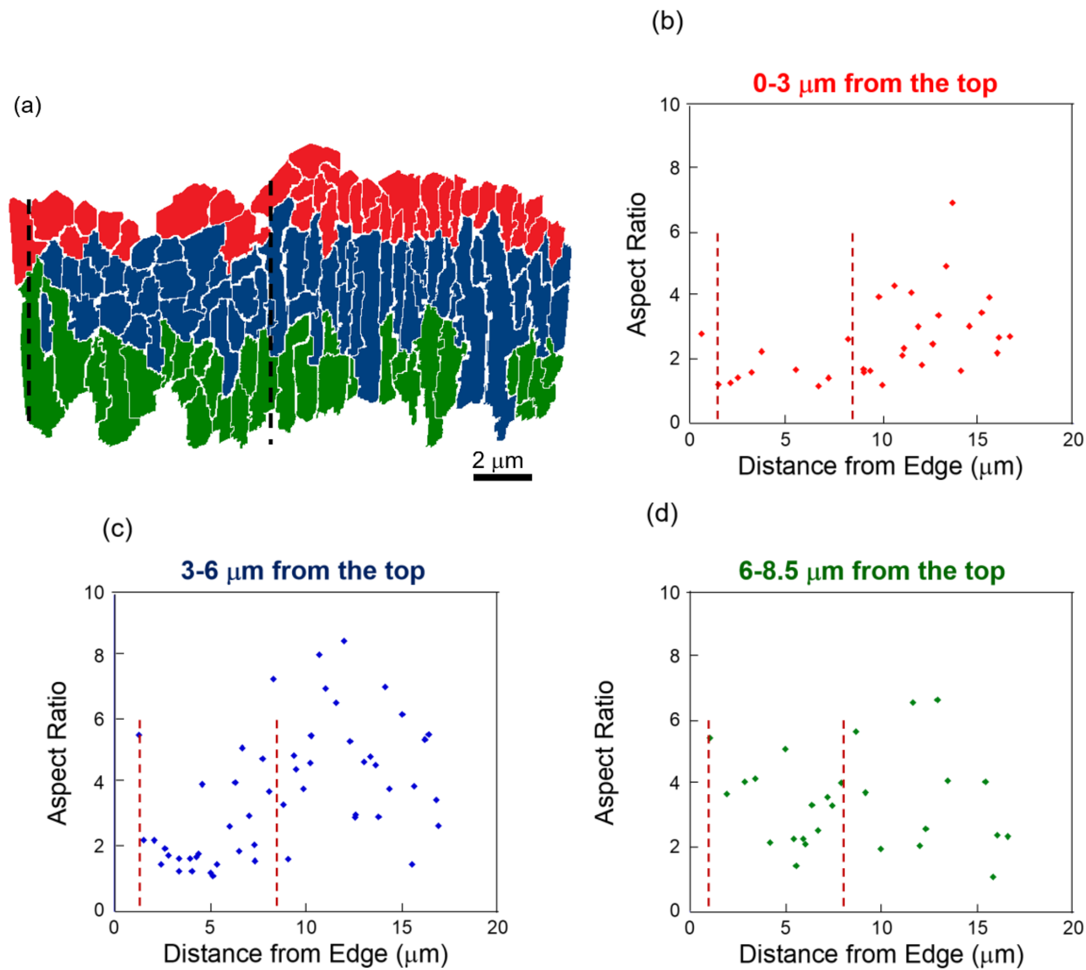


Figure 19. (a) Segmented grain structure of an aged slab, (b) Aspect ratio of top layer of the slab, (c) Aspect ratio of middle layer of the slab, (d) Aspect ratio of bottom layer of the slab. Grains present within the dotted line have the lowest aspect ratio in each regime.

As the gray values of the hillocks and the Sn surface are similar, a direct gray scale thresholding technique is ineffective. Since the edges of the hillocks appeared brighter, an

‘unsharp mask’ filter in AVIZO® software was used to enhance the edge contrast so they could be identified by gray scale thresholding. This step is followed by a ‘grow’ procedure which connects incomplete edges. A ‘fill’ process is then used to select an entire hillock by filling the selected edges. Finally, any excessive dilation and noise pixels are corrected for, by using a ‘shrink’ process. This gives a clear segmented binary image of the hillock distribution (Fig. 20 (a)) and any minor errors can be removed by further processing or by manual cleaning.

A top view image of an indentation and the hillocks surrounding the indentation edges can be observed in Fig. 20 (a). Analyzing the number density of the hillocks, it was observed that hillock formation extended up to 15 μm from the indentation edge, as shown in Fig. 20 (b). This distance was almost identical in every indentation and it is very interesting as it shows the extent of the stress field around the indentation for this specific load and how it decreases away from the indentation. The hillocks have a nearly spherical cross-section with a mean aspect ratio 1.4 ± 0.3 which is represented in the aspect ratio plot in Fig. 20 (c).

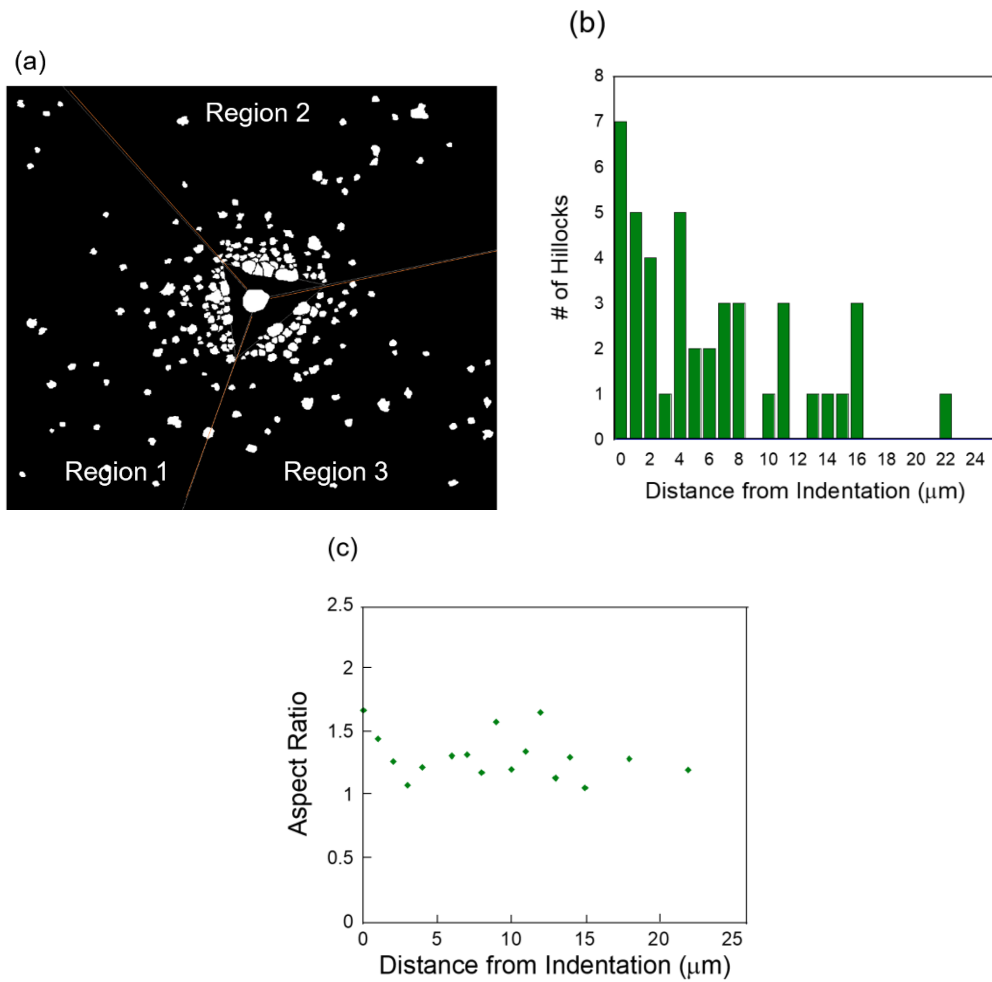


Figure 20. (a) Binary image of segmented hillocks (Top view of an indentation), (b) Number density of hillocks as a function of distance showing hillock presence up to 15 μm from the indentation edge, (c) Aspect ratio of hillocks as a function of distance around the indentation.

Interestingly, the grain boundary misorientation analysis from the OIM maps revealed that every grain boundary adjacent to the hillock were high angle grain boundaries with misorientations greater than 20°. A magnified OIM map of the area surrounding a hillock in an aged sample is shown in Fig. 21, the misorientation values for grain boundaries surrounding 'hillock #1' are shown in Table I. The first set of values correspond to those

that are adjacent to the large hillock (grain 1 in Fig.21). The misorientation angles given in the second set of values are between grains that are adjacent to the hillock. This result agrees with findings in the work done by Jagtap et al. (Jagtap, Chakraborty et al. 2017) and Sarobol et al. (Sarobol, Chen et al. 2013) who also suggest that high angle grain boundaries are a pre-requisite for whisker growth.

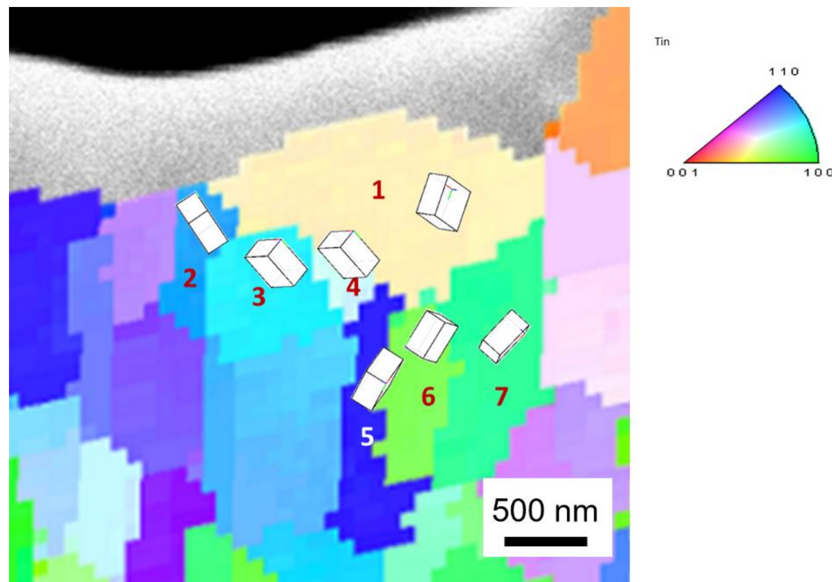


Figure 21. Magnified OIM map an area surrounding a hillock in an aged and indented sample.

Table I. Misorientation Values for grain boundaries surrounding hillocks.

Between grains #	Misorientation	
1-2	61.4	
1-3	39.2	
1-4	89	
1-5	55	
1-6	30.26	
1-7	44.34	

2-3	59	High Angle Grain Boundaries
3-4	72.6	
4-5	91.8	
5-6	41.1	
6-7	26.8	

With regards to the overall orientation of Sn grains in the FIB slab, inverse pole figures were obtained for both aged and unaged samples, close to and away from the indented region (Fig. 22). As it can be seen, there's no strong texture or orientation preference close to the indent or away from the indent. In both cases the grains near the indentation are equiaxed with random orientation which suggests formation of strain free grains.

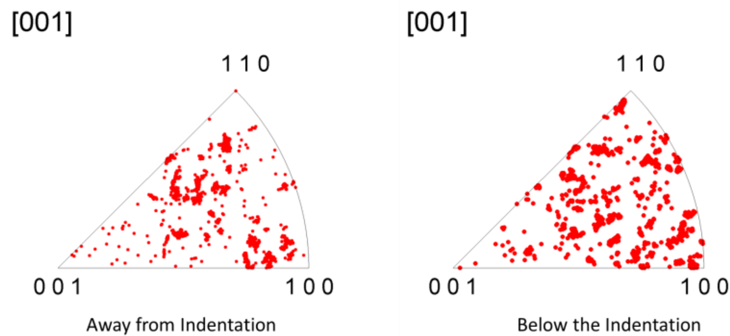


Figure 22. Inverse pole figures showing no preferred orientation on the FIB slab away the indentation or below the indentation.

3.1.4 Finite Element Modeling of Nanoindentation

To better understand the stress state within the Sn matrix, Finite Element Modeling (FEM) was attempted using ABAQUS software (Providence, RI) to simulate the experimental indentation process. The model was designed to match the layer thicknesses of the aged

sample with inputs for thicknesses of Sn, Cu_6Sn_5, Cu_3Sn and Cu layers, as shown in Fig. 23 and listed in Table II. Data for Young's modulus, yield stress and Poisson ratio were adapted from the literature using similar geometry samples (Table II). The model was 2D axisymmetric with a conical indenter with an equivalent semi-angle of 70.3°. Since the geometry of the Berkovich indenter is more complicated, an equivalent angle for conical indenter was used based on the projected area of contact as described elsewhere (Deng, Chawla et al. 2004). In this model the indenter was assumed to behave as an undeformable solid. A loading rate of 3 mN/s was used, which is the same used for the experimental test. A finer mesh was used in the area below the indenter in the contact area and extended almost entirely through the thickness of the Sn layer. A coarser mesh was used away from the contact area and the mesh was refined until computational convergence is achieved. The simulation was conducted as a load-control test. The symmetry axis was fixed horizontally (U1=0) but allowed to displace vertically. The bottom of the sample was fixed in every direction.

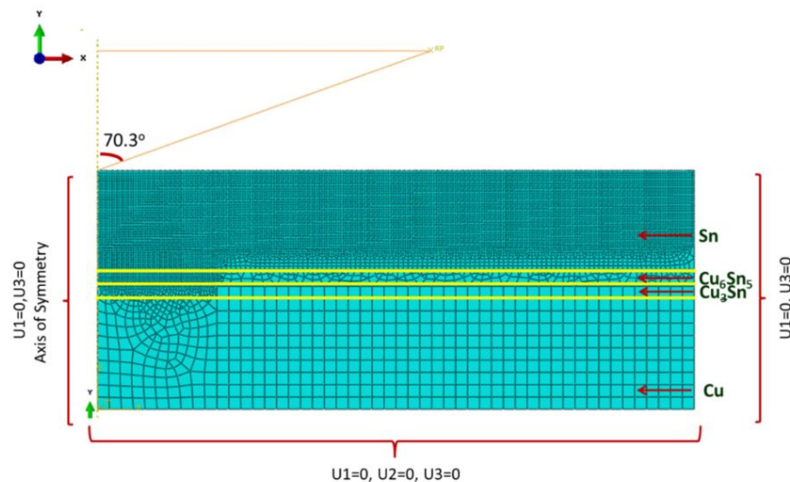


Figure 23. Finite element mesh and boundary conditions used in the model. Axis 1,2 and 3 correspond to axis X, Y and Z respectively.

Table II. Parameters used for Finite Element Modeling

	Sn	Cu_6Sn_5	Cu_3Sn	Cu
Young's modulus (GPa)	50 (Jeong, Murata et al. 2009)	110 (Jeong, Murata et al. 2009)	132 (Tanida, Umemoto et al. 2004)	120 (Deng, Chawla et al. 2004)
Yield Stress (MPa)	34 (Yazzie, Williams et al. 2012)	2009 (Deng, Chawla et al. 2004)	1787 (Deng, Chawla et al. 2004)	180 (Deng, Chawla et al. 2004)
Poisson ratio	0.34 (Sawada, Shimizu et al. 2010)	0.29 (Yang, Lai et al. 2008)	0.29 (Jang, Lee et al. 2004)	0.33
Thickness (μm)	6.7 ± 0.5	1.4 ± 0.4	1.6 ± 0.2	10

Comparison of the FE model with experimental results showed good agreement with an indentation depth of 2 μm for the model and 2.4 μm for the experimental result. A zoomed-in image showing the equivalent plastic strain generated during nanoindentation at a load of 15 mN is shown in Fig. 24. From the image, it can be seen that the indentation tip produces the maximum plastic deformation which is expected. However, towards the edge of the indentation, the equivalent plastic deformation is less as the surface has no constraint and a slight pile up can be observed.

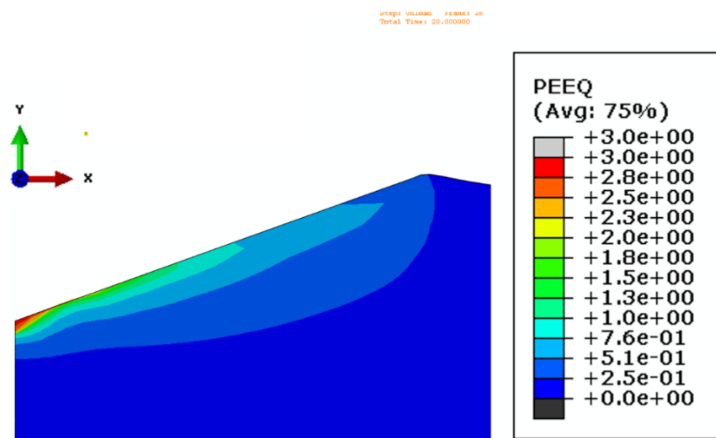


Figure 24. PEEQ (Equivalent plastic strain%) from FEM simulation at an indentation load of 15 mN for pure Sn.

3.1.5 Micro-pillar Compression

Three sets of samples were analyzed: mean grain size 0.8 μm, 0.5 μm and 0.2 μm. Fig. 25 shows SEM images before and after compression of a 5 x 10 μm that was milled on a sample with a grain width of 0.8 μm. The protrusions on the top of the pillars are believed to be a result of a grain boundary sliding mechanism. Fig. 25(c) shows a cross-section of the compressed pillar. The OIM map for the cross-sectioned pillar is shown in Fig. 25(d). No preferred orientation was seen in this pillar or any of the compressed pillars in all samples.

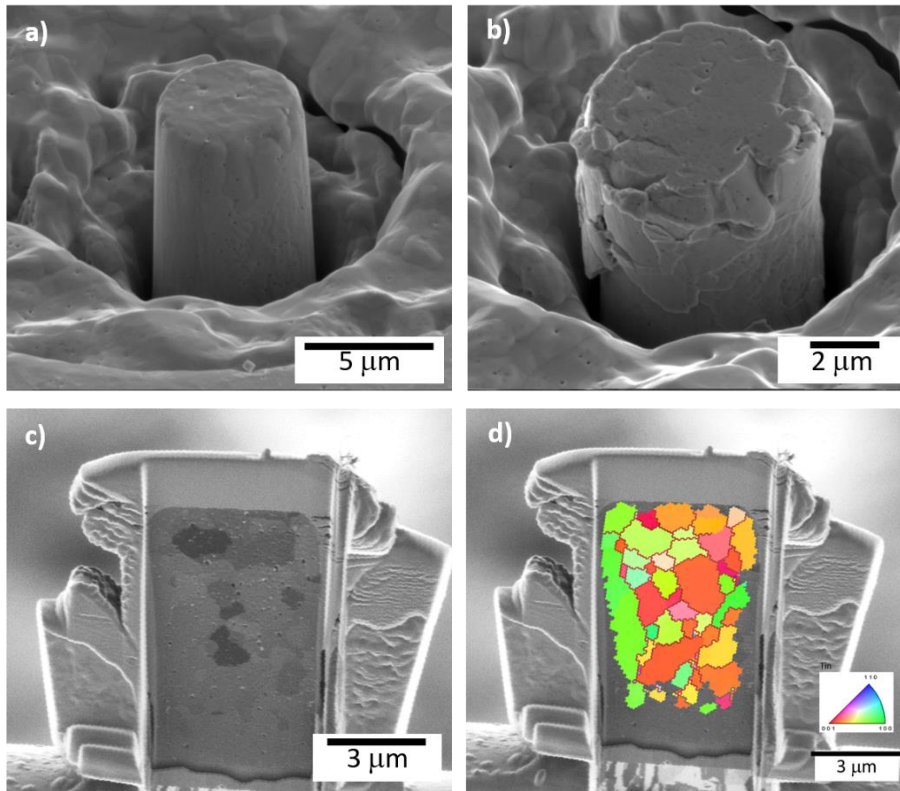


Figure 25. a) 5 x 10 μm Sn pillar before micropillar compression experiment, b) Pillar after compression, c) Cross-section of the compressed pillar, d) Overlay of EBSD map. Bright layer on top of pillar is platinum which was deposited to obtain a smooth cross-section.

For the sample with the largest grain size (0.8 µm wide), micropillar compression results showed an inverse size effect on the pillar's strength, where the largest pillar 5x10 µm had the highest yield stress and the smallest size (2 x 4 µm) had the lowest yield stress (Fig. 26). This behavior is contrary to what is expected since a smaller volume would mean a less number of defects. In the case of the sample with an average grain width of 0.5 (Fig. 26) the inverse size effect was not observed; the yield stress was seen to be very similar for all 3 sizes. The same trend was observed for the sample with the smaller grain size (Fig. 26).

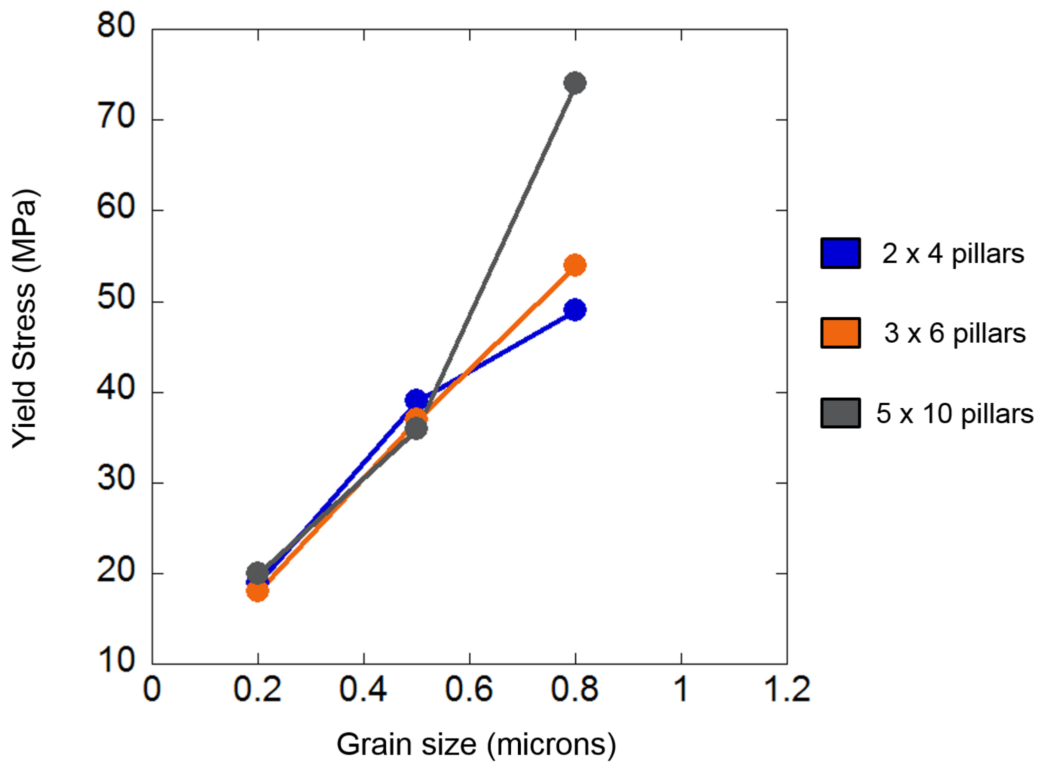


Figure 26. Pillar compression results showing the yield stress for 0.8 µm, 0.5 µm and 0.2 µm width. Each color represents a pillar size, blue represents 2x4 µm pillars, orange shows results for 3x6 µm pillars and gray indicates 5x10 µm pillars.

From Fig. 26 it can be observed that as the grain width of the sample decreases so does the value of the yield stress.

Grain boundary sliding is a deformation mechanism that is grain size sensitive (favors small sizes) and is promoted at high homologous temperature and slow strain rates (Rösler, Harders, & Baeker, 2007). Sn creeps at room temperature since it has a high homologous temperature (0.6 Tm). Pillars with smaller grains (more grain boundaries) tend to deform easier through grain boundary sliding and hence have lower yield strength. Due to smaller grains, dislocation glide and grain boundary sliding are the dominant deformation mechanisms.

3.1.6 Hillock growth mechanism

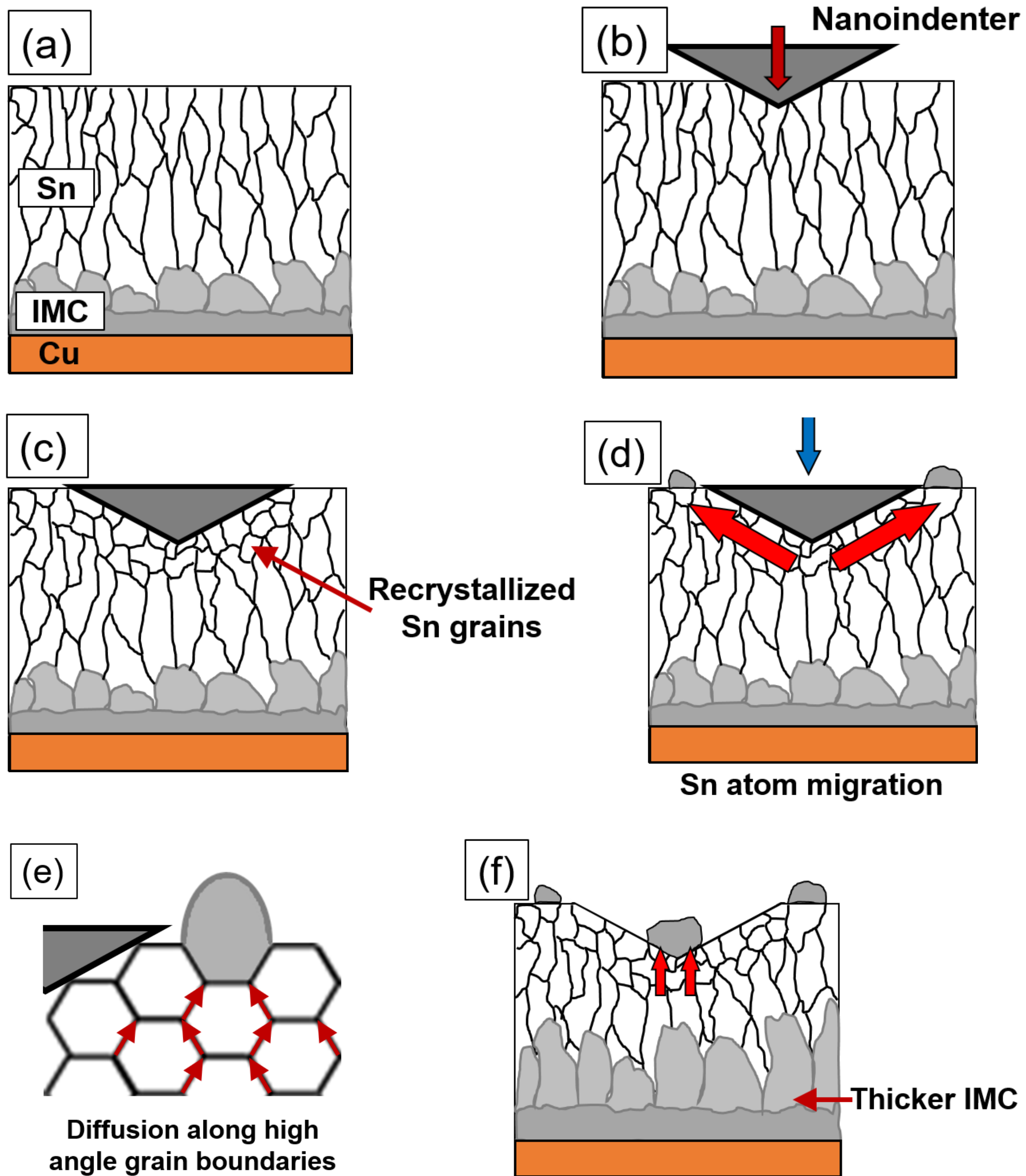


Figure 27. Schematic diagram showing mechanism of hillock growth. (a) Initial microstructure with columnar Sn grains, (b) Nanoindentation using Berkovich tip, (c) Dynamic recrystallization during indentation, (d) Diffusion of Sn atoms to free surface and forming Sn hillocks to relieve compressive stress, (e) High angle grain boundaries

around recrystallized grains act as fast diffusion pathway for Sn atoms, (f) The case of thicker IMC: Back stresses in aged samples due to thicker IMC result in more extensive hillock growth at indentation center, and sides, after removing the load.

The mechanism for growth of indentation induced Sn whiskers can be explained in 2 stages as shown in Fig. 27 (a-f). It starts from an initial microstructure with elongated Sn grains that run perpendicular to the Sn-Cu interface. In stage 1, as the sample is indented using a Berkovich indenter, the deformation results in dynamic recrystallization of Sn grains around the indenter. The new recrystallized grains have an equiaxed microstructure with high-angle grain boundary misorientation (as shown using EBSD). Due to the severe deformation under the indenter, Sn atoms migrate from highly stressed region towards regions of lower stress around the indenter (stage 2). Stress relief is fastest at the free unconstrained surface of the Sn film, adjacent to the indentation (as seen in FEM simulation), where several Sn hillocks form. The high angle grain boundaries surrounding the recrystallized grains act as fast diffusion pathway for Sn atom migration. In the case of aged samples, as seen in Fig. 27 (f), larger hillock growth is favored by the thicker IMC layer, which could additionally contribute back stresses, and thus enabling hillock growth even after the load is removed.

3.2 Conclusions

The influence of microstructure and crystallography in the formation and evolution of mechanically induced tin whisker/hillocks was investigated in vacuum using an *in situ* nanoindenter and EBSD. Based on the experimental results and FEM analysis, the following conclusions could be drawn:

As-plated electroplated Sn samples do not have native IMC layer formation within the first 24 hours of plating. Nanoindentation of samples in this condition results in formation of ~100 nm sized hillocks surrounding the indentation which seem to form dynamically during indentation. On the other hand, nanoindentation of samples aged at 150°C for 3 days revealed slightly larger hillocks around the indentation, in addition to large faceted hillocks / single crystalline mounds at the edge and center of the indentations indicating the strong influence of IMC layer beneath the Sn film.

Aging tests revealed morphological differences in Cu_6Sn_5 and Cu_3Sn IMCs and their growth exponents confirmed the different diffusion mechanisms influencing these morphologies. Cu_6Sn_5 showed growth exponent 0.4 indicating a mixed grain boundary and bulk diffusion mechanism thus resulting in a nodular morphology, while Cu_3Sn showed growth exponent of 0.48 indicating bulk diffusion resulting in a planar growth front.

FIB-slab lift-out technique was used to fabricate slabs from the Sn plating to investigate the grain structure and crystallography. Aspect ratio analysis on both as-plated and aged samples revealed a mechanically induced recrystallized zone forming near the indentation with equiaxed grains as compared to elongated grains away from the indentation.

The extent of stress field around the indentation and how it decreases with distance was elucidated by analyzing the number density of hillocks. The smaller hillocks were seen to form up to 15 μm from the indentation with the highest density at the indentation edge.

Crystallographic analysis using EBSD revealed the presence of high angle grain boundaries around the large faceted hillocks. These high angle grain boundaries serve as fast diffusion pathways for Sn atoms to migrate to the surface forming hillocks and thus relieving the compressive stresses.

An FEM model was developed to simulate the nanoindentation test using a 2D axisymmetric conical indenter and it was seen that largest plastic deformation is close to the indenter tip, where the large faceted hillocks were seen and the stress field decreases gradually away from the indenter which compared well with experimental findings.

4. X-RAY MICROTOMOGRAPHY OF THERMAL CYCLING DAMAGE IN SINTERED NANO-SILVER JOINTS

4.1. Overview

High operating temperature thermal interface materials (TIMs) in power electronics are required to realize performance gains from the use of wide band-gap (WBG) semiconductor devices, such as Silicon Carbide (SiC) or Gallium Nitride (GaN). Additionally, the operating temperature of these devices is higher than 250°C, preventing use of traditional solder material for packaging. At high temperature, the thermomechanical stresses induced inside the electronic package can severely degrade the reliability and life of the device. In this light, new non-destructive approach is needed to understand the damage mechanism when subjected to reliability tests such as power and thermal cycling. In this work, sintered nano-silver TIM was identified as the most promising high temperature bonding candidate. The sintered nano-silver samples were fabricated and their shear strength are reported. Thermal cycling tests were conducted and damage evolution was characterized using a lab scale 3D X-ray system to periodically assess changes in the microstructure such as cracks, voids, and porosity in the TIM layer. The evolution of microstructure and the effect of cycling temperature during thermal cycling will be discussed.

4.2. Introduction

The increasing demand for smaller, faster and more efficient electronic packages in automotive applications such as power modules, has led to the development of high density devices. The devices are required to operate at extreme power and temperature conditions, without compromising its lifetime. Technological advancements with wide band gap materials such as Silicon carbide (SiC) and Gallium nitride (GaN) has pushed the maximum operating temperatures to over 300ºC, while supporting voltages over 600V and high frequencies (Bajwa 2015).

At these extreme conditions, the packages are required to exhibit mechanical, thermal and electrical stability. Differences in strength/modulus, electrical conductivity and thermal expansion coefficients between the various layers in a module, are critical in determining the package lifetime. Schematic of a traditional power package is shown in Fig. 28. The device (Si, SiC or GaN) generates heat during operation, which is conducted through the bond towards the substrate and finally dissipated at the heat sink. To efficiently dissipate the heat generated, the bonding materials need to exhibit long-term stability and reliability.

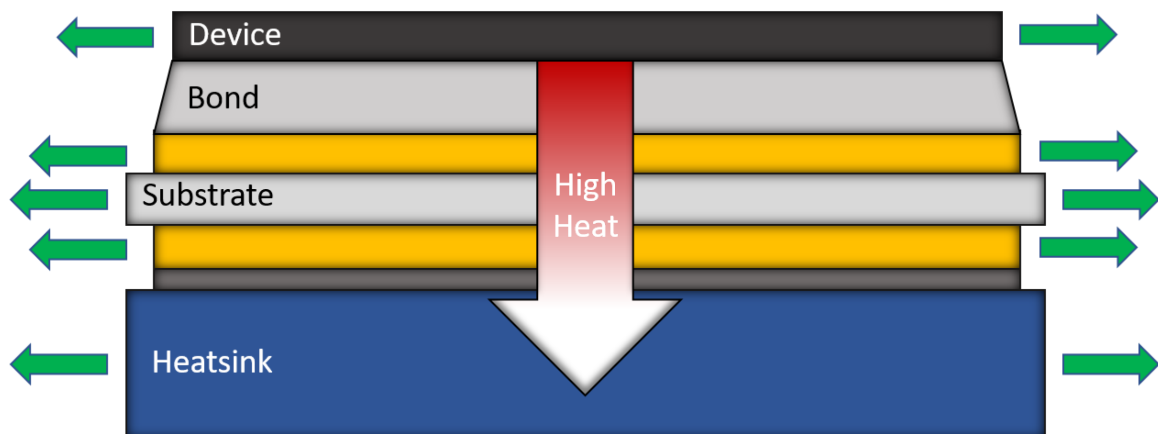


Figure 28. Traditional power package of a hybrid vehicle showing stresses at interfaces.

The die attachment/interconnections are the most important parts of the electronic package, since they provide chip-substrate connection and substrate-base plate connection. Demands to improve the existing technology in microelectronics comes from industries such as automotive (Kassakian and Perreault 2001), aerospace (Nieberding and Powell 1982) and military (Khazaka, Mendizabal et al. 2015). They require the systems to be able to operate under high temperature and high-power conditions. To achieve this, the bonding materials (die-attach materials / thermal interface materials) in the electronic packages of power modules are required to possess the following characteristics:

1) Low processing temperatures, typically under 300ºC.
2) Stable at operating temperatures over 300ºC after bonding.
3) Mechanical stability, under shear loads.
4) Good thermal cycling performance.
5) Good power cycling performance.

Traditionally, solder alloys have been used as die attach materials in semiconductor devices, since they can be processed at low temperatures, however, their melting points are also low. Very few solder alloys have melting temperatures sufficiently high to work at temperatures above 250°C (which is the limitation of Si based devices (Bai, Zhang et al. 2006)). Furthermore, they have the tendency to form IMCs, thus making the interfaces brittle leading to premature failure of the devices (Hwang 2004).

Among the high-temperature solders that are commonly used in the microelectronics industry, we have Au-based solders such as Au80-Sn20. This alloy has been used as die

attach on a SiC die which can operate up to 400°C (Pittroff, Erbert et al. 2001, Liu, Hu et al. 2004).

It possess excellent corrosion resistance, good thermal and electrical conductivities and does not require the use of flux during the soldering process (Chin, Cheong et al. 2010). The drawbacks in the used of Au-based solders is that, it is much more expensive than ordinary solders due to its high Au content (Bai, Calata et al. 2006), and the low melting temperature of eutectic Au-Sn (280°C). In order to operate at higher temperature, an off-eutectic alloy needs to be used which would require a higher processing temperature, which in turn increases the cost of the soldering process (Chin, Cheong et al. 2010).

Another method that's gaining popularity for obtaining high temperature die attach materials is Transient Liquid Phase Sintering (TLPS). In this technique, a low melting metal and a high melting metal are used together as a mixture. The low melting layer will diffuse into the higher melting layer, forming an alloy which will have significantly higher melting point than the initial mixture (Buttay, Planson et al. 2011). An added benefit is that the majority of the TLP materials are low cost, commonly used in power electronics and well known in the semiconductors industry (Yoon, Glover et al. 2013). This method has been applied to Au-Sn alloys (Johnson, Wang et al. 2007), In-Ag (Quintero, andy Oberc et al. 2008), Ni-Sn (Yoon, Glover et al. 2013), etc. The drawback of TLP materials is the long time required for bond homogenization and the formation of IMC layers which can cause decrease in strength in the bond (Bajwa 2015).

A third promising material for high-temperature die attach is sintered nano-Ag solder. Sintered nano-ag bonds have excellent thermal and electrical conductivities, low processing temperature (250°C) and high melting temperature – approaching bulk silver properties. Work by Schwasrzbauer et al. shows that sintered nano-silver joints had better thermomechanical reliability than traditional solder attach materials (Schwarzbauer and Kuhnert 1989). The porous microstructure of the nano-Ag bond gives it good ductility to resist damage from thermomechanical stresses (Jiang, Lei et al. 2014).

Among the advantages in the use of nano-Ag as high-temperature die attach material is its good reliability during thermal and power cycling and compatibility with Si, SiC and GaN devices. Some of the disadvantages of this die attach material system are longer processing times in comparison with traditional solders and the variability in material properties as it is highly dependent on the processing conditions (Bajwa 2015).

Since thermal induced damage is the leading cause of failure in power electronics, the common methods to evaluate the reliability of die attach materials involves thermal and power cycling reliability tests. Samples are subjected to cyclic heating and cooling to induce damage on the solder after which the microstructural damage is analyzed. The common characterization techniques are destructive in nature such as cross-sectional analysis of the bond line using a Scanning Electron Microscope (SEM) (Jiang, Lei et al. 2014) or studies on the decrease of shear strength in samples after specific number of thermal fatigue cycles (Bai, Calata et al. 2006). The use of such approaches makes it impossible to quantify the evolution of damage such as crack formation and growth within the same sample as a function of time. Other characterization methods such as Scanning

Acoustic Microscopy (SAM) have a low resolution and unfortunately, don't allow, a detailed analysis of formation and growth of cracks. 3D X-Ray tomography on the other hand has been proved to be an excellent technique to analyze and quantify, non-destructively the degradation of solder material systems (Padilla, Jakkali et al. 2012, Singh 2015, Mertens, Kirubanandham et al. 2016).

In this work a novel 4D approach was used to study the degradation of the solder as a function of time and temperature. 3D X-Ray tomography was used to study the thermal induced degradation on sintered nano-Ag solder, a promising high-temperature die attach material.

4.3. Experimental Procedures

4.3.1. Sample Preparation

Test vehicles were prepared using bare Silicon dice (diced and metallized) and low-sintering temperature nano-Ag paste (NBE Tech, Blacksburg, VA, USA) as die attach material. 21 mm x 21 mm x 1 mm Direct Bonded Copper (DBC) (Stellar Ceramics, Millbury, MA, USA) coupons were used as substrates. The DBC consisted of a 600 μm AlN layer bonded to 200 μm Cu layer on either side. 5 mm x 5 mm single side polished Si dice with a thickness of 500 μm were used. Both the DBC and Si dice were metallized to enhance good bonding of the die attachment. Prior to deposition, Si dice were sputter cleaned to remove any residual organic contamination from handling. Single side metallization on DBC and Si dice consisted of 50 nm layer of Titanium, followed by 1 μm Ag layer and 50 nm Gold to prevent oxidation.

The Ti layer serves as an adhesive by reacting to the native oxides on the Si die and DBC substrate. The 1 μm Al layer provides a strong base for bonding with the dispensed nano-Ag paste. To protect the Ag layer from oxidation a 50 nm layer of Au was deposited. It is important to point that the DBC and Si wafer were diced prior to metal deposition to avoid film stress relief during dicing which could result in delamination of metallization.

The die attachment structure prepared in this study is shown in Fig. 29. Samples were prepared using a low temperature-low pressure sintering procedure. Prior to sintering a 30-50 μm thick bond line of nano-Ag solder was dispensed on the metallized DBC substrate after which, the Si die was placed on the same area making sure there is good contact between solder and Si. Sintering was done on a programmable hot plate (Torrey Pines Scientific EchoTherm HS30) mounted with a load cell that allows the application of pressure during sintering. A heating ramp rate of 4°C/ min was used to allow the activation of the organic binder in the Ag-paste. A peak temperature of 250 °C was held for 30 minutes, for achieving maximum densification of the solder, after which the bond was cooled at a rate of 20°C/ min. A constant pressure of 0.4 MPa was applied from the beginning of sintering till the end of cool down to favor densification of the solder. Fig. 30 shows the sintering profile used.

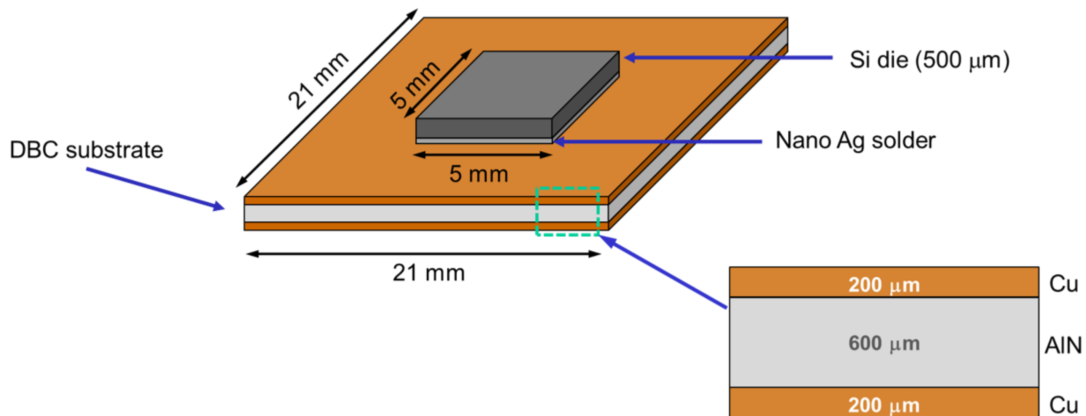


Figure 29. Die attachment structure consisting of a DBC substrate, nano-Ag solder paste as a die attach material and a single side polished Si die.

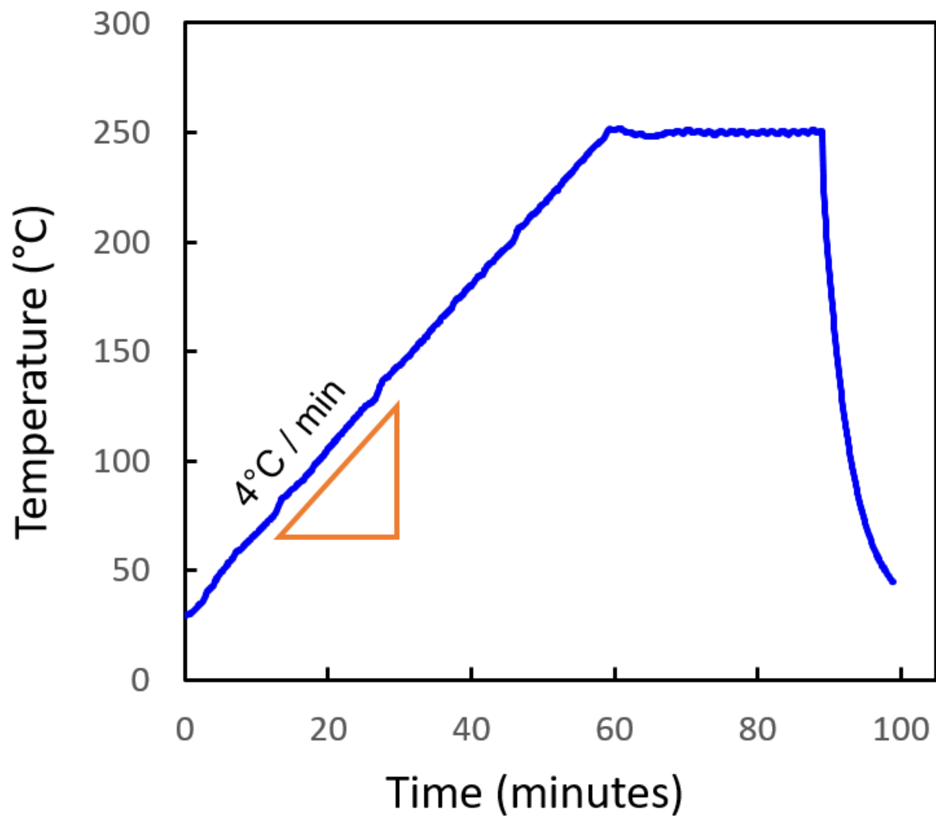


Figure 30. Sintering profile used for sample preparation. A heating rate of 4°C/min was used until reaching a maximum temperature of 250°C and held for 30 minutes. A load of 1 Kg (0.4 MPa) was applied during sintering.

4.3.2. Shear Testing

To evaluate the bond quality, shear tests were done to measure the strength of the sintered nano-Ag bonds. A custom shear testing setup was built for this purpose. Fig. 31 shows the shear testing setup used in this study. The setup consists of a top clamp that is connected to a moving actuator for loading the sample. The top clamp is adjustable to suit variations in thickness between samples. The bottom clamp is a fixed support that holds the substrate in place. A strain rate of 10^{-4} s^{-1} was used. Analysis of fractography after shear testing was carried out in an SEM (Zeiss Auriga, Carl Zeiss XRM, Pleasanton, CA, USA).

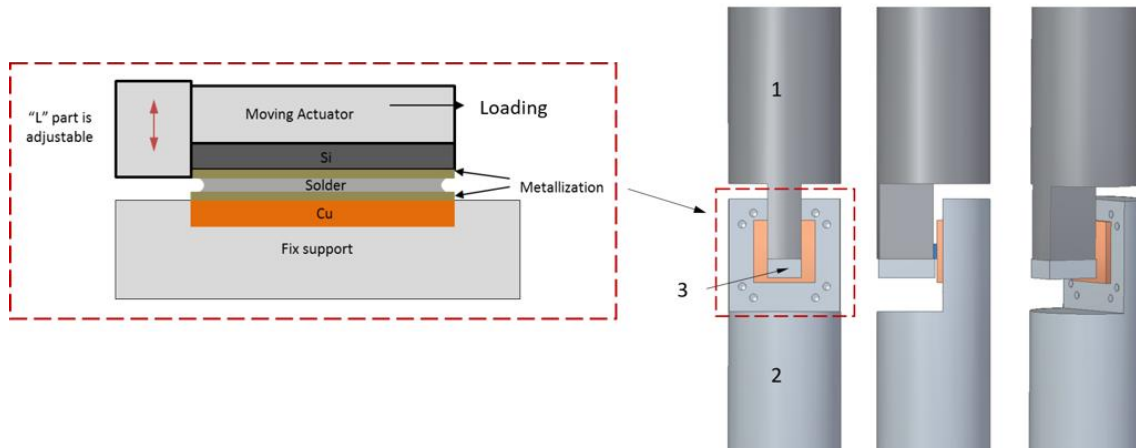


Figure 31. Schematic of shear testing fixture. The lower shear bar (marked by 2) holds the substrate with clamping plates. The upper shear bar (marked by 1) is connected to a moving actuator that applies the shear load. End plate (marked by 3) is adjustable based on the thickness of the Si die.

4.3.3. Thermal Cycling Tests

For assessing thermo-mechanical behavior of the nano-Ag solder, the bonded samples were subjected to thermal cycling tests. Fig. 32 shows the thermal cycling setup used for the tests. The setup consists of a resistive ceramic heater (8 mm x 8 mm x 3.5 mm, Watlow

Ceramics, Saint Louis, MO, USA) with an in-built thermocouple that was used as a heat source on top of the Si die. Forced air was supplied through a nozzle to cool the sample at a controlled rate from the substrate side for the cooling cycle.

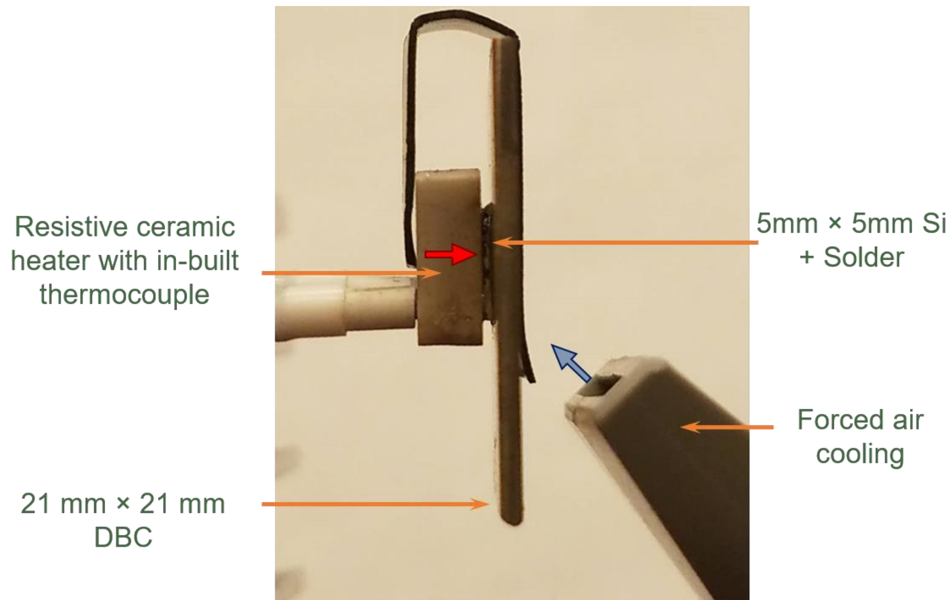


Figure 32. Setup used for the thermal cycling experiments. A ceramic heater was used as the heat source and placed on top of the Si die. A control cooling rate was achieved by using forced air through a nozzle placed closer to the DBC side.

Three different thermal cycling conditions were used to study the effect of peak temperature. In test 1, as shown in Fig. 33(a), samples were heated to 250°C from room temperature giving a ΔT=230°C. In test 2, shown in Fig.33(b), samples were heated from room temperature to a maximum temperature of 200°C, achieving a ΔT=180°C. Test 3, Fig.33(c), samples were heated to a peak temperature of 175°C, with ΔT=155°C. For all the thermal cycling tests, the heating and cooling rates were kept constant at 4°C/min with a dwell time at peak temperature of 1 minute. The total cycle time in each test was 4 min/cycle.

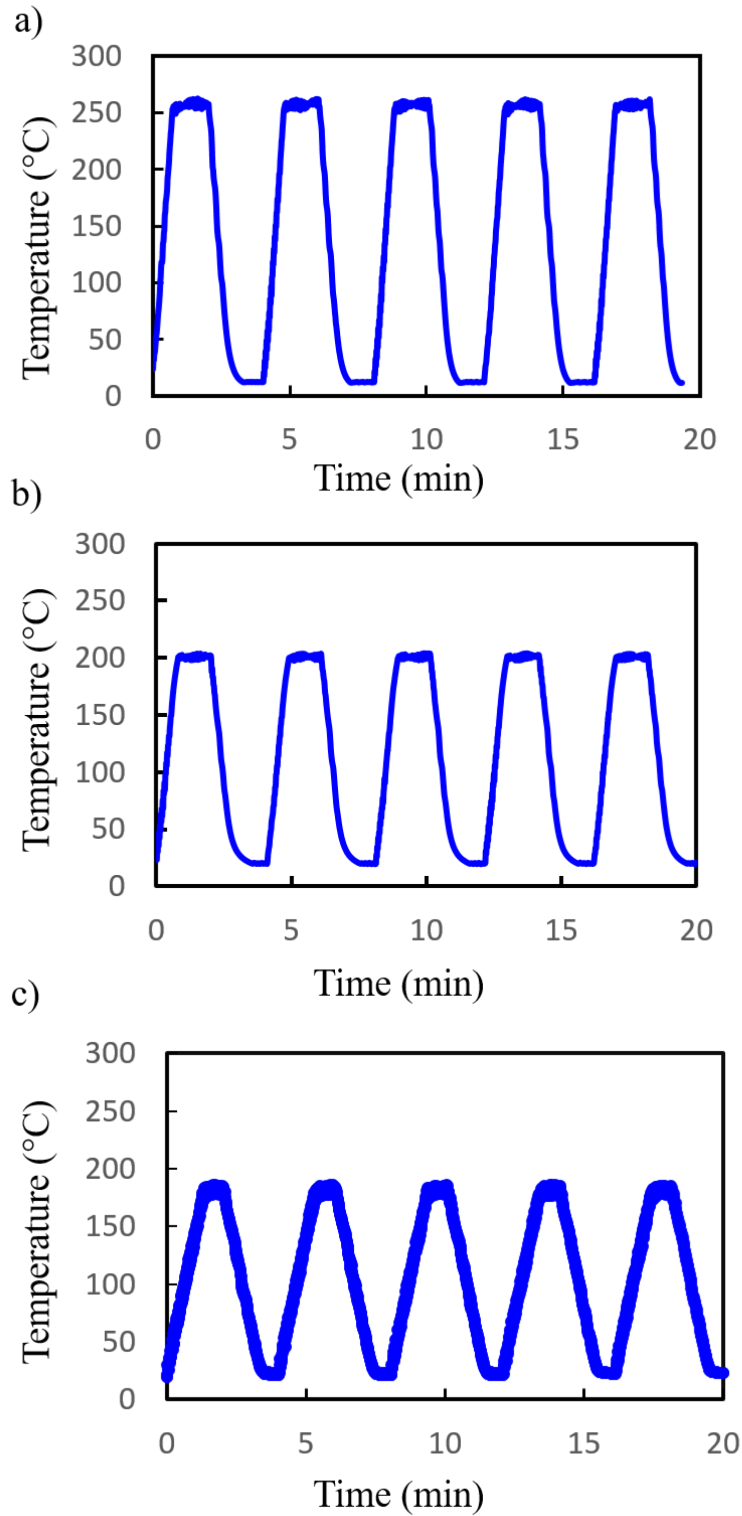


Figure 33. Thermal Cycling test parameters. The heating and cooling rate were kept constant at 4°C/min. A dwell time of 1 min at peak temperature was applied in each test.

4.3.4. X-Ray Tomography

Prior to thermal cycling tests, 3D X-Ray tomography scans of the solder volume were taken, to have a baseline comparison of the initial microstructure. Additionally, the tests were interrupted after specific number of cycles to study the evolution of crack growth as a function of time by using 3D X-Ray tomography. This technique was also used to measure the area of contact and accurately calculate the shear strength of the sample.

3D X-ray tomography was done on a lab scale X-ray CT system (Zeiss Xradia 520 Versa, Carl Zeiss XRM, Pleasanton, CA, USA) as seen in Fig.34. Absorption contrast tomography scans were performed at 120 kV with a low energy filter (LE2 equipped inside the machine), resulting in tomograms with a voxel size of 3 µm. 3200 projections were taken and the exposure time was 7 s for a single projection. The transmission images from all the scans were reconstructed using a commercial software package (Zeiss XMReconstructor), which uses an algorithm based on standard filtered back-projection. SEM Fractography analysis after shear testing was carried out in a ZEISS Auriga Crossbeam system (Carl Zeiss Microscopy, München, Germany).

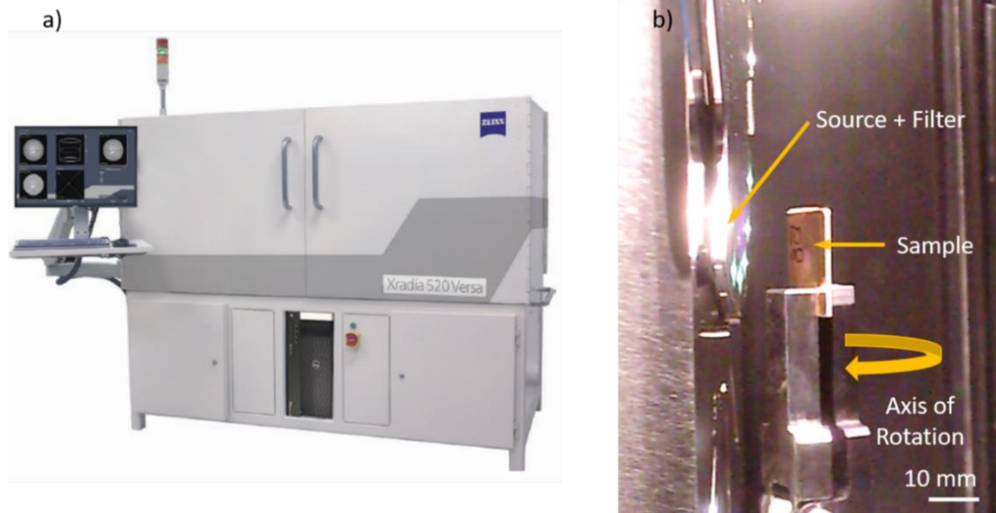


Figure 34. a) ZEISS X-radia 520 Versa CT system, b) Sample mounted inside the system for tomography.

4.3.5. Nanoindentation

To analyze the mechanical properties of the individual microconstituents in the stack nanoindentation was used. Each layer was indented up to a depth of 1um to obtain the young's modulus and hardness using a commercial nanoindenter (Nanoindenter XP-II, Agilent) with a Berkovich tip. Cross-sections of the specimens were prepared and polished to a 0.05 μm colloidal silica finish for nanoindentation. Samples were firmly fixed on stubs using Crystalbond™ adhesive (Westchester, Pennsylvania). 10 indentations were made on each layer with at least 30 μm spacing between each indent. Silica standards were used for calibration prior to nanoindentation tests. Tests were done using controlled strain rate which was set at 0.05 s^{-1}. The Nanoindenter utilizes Continuous Stiffness Measurement (CSM) which applies an oscillating load, smaller than the nominal load, as the indenter approaches the sample. This technique allows measurement of young's modulus and harness as a function of indentation depth. The values for modulus and harness for the

microconstituent phases are taken from the modulus vs displacement and hardness vs displacement plots as the average of values not affected by indentation depth.

4.4. Results and Discussion

4.4.1. Microstructural Characterization

To evaluate the quality of sintering, cross-sections of sintered samples were studied using Focused Ion Beam (FIB) and Scanning Electron Microscopy (SEM) images. Fig. 35 shows a cross-section of a sample that was sintered using the profile described previously. It is observed that the thickness of the bond line is about 30 μm. A higher magnification SEM image of the nano-Ag bond can be seen in Fig. 35(b). It shows that the sintering profile gave good densification of the sintered solder. Small porosities were seen to be homogenously distributed through the solder volume. At the interfaces of Si-solder and solder-DBC, good adhesion was seen, this because of the metallization layers deposited on the bonding side of the chip and DBC substrate.

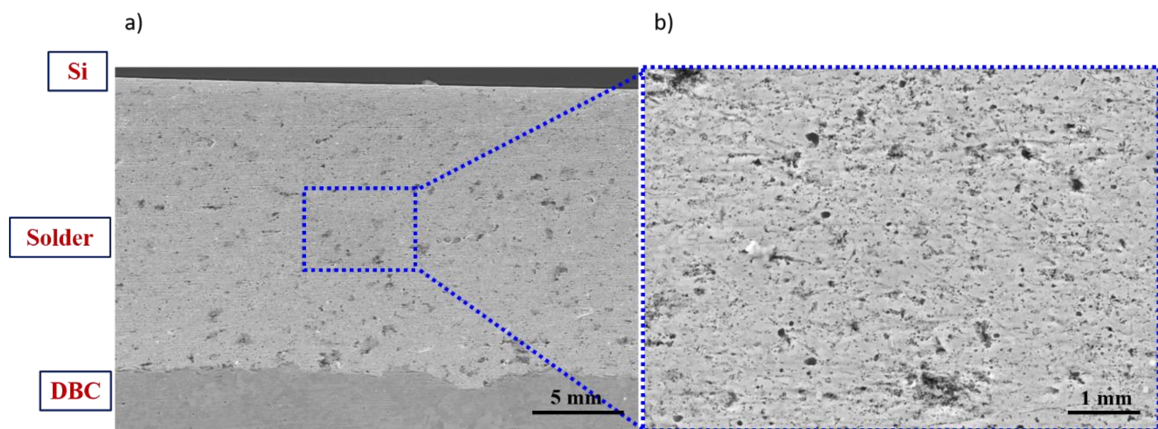


Figure 35. a) 30 μm-thick nano-Ag solder bondline, good adhesion can be seen at the Si-solder and solder-DBC interfaces, b) zoomed image of nano-Ag bondline, homogenous distribution of pores can be observed.

4.4.2. Mechanical Properties of Microconstituents by Nanoindentation

A typical load vs displacement curve is shown in Fig.36, the maximum depth reached for each test was 1 µm. Young's modulus and hardness curves obtained through nanoindentation are shown in Fig. 37(a-b). The Young's modulus of the material is calculated from equations 1-2, where stiffness (S) is given by the slope of the unloading curve in the load vs displacement plot. E_r corresponds to the reduced modulus, E and ν are the Young's modulus and Poisson ratio of the material, E_i and ν_i correspond to the values of the indenter, A is the contact area and β is the geometry factor of the indenter (Hay 2009).

$$E_r = \frac{\sqrt{\pi}}{2\beta}\frac{S}{\sqrt{A}} \quad \text{Equation 1}$$

$$\frac{1}{E_r} = \frac{1-v^2}{E} + \frac{1-v_i^2}{E_I} \quad \text{Equation 2}$$

The hardness (H) of the material is calculated by equation 3,

$$H = \frac{P}{A} \quad \text{Equation 3}$$

Where P corresponds to the load at maximum displacement and A is the contact area.

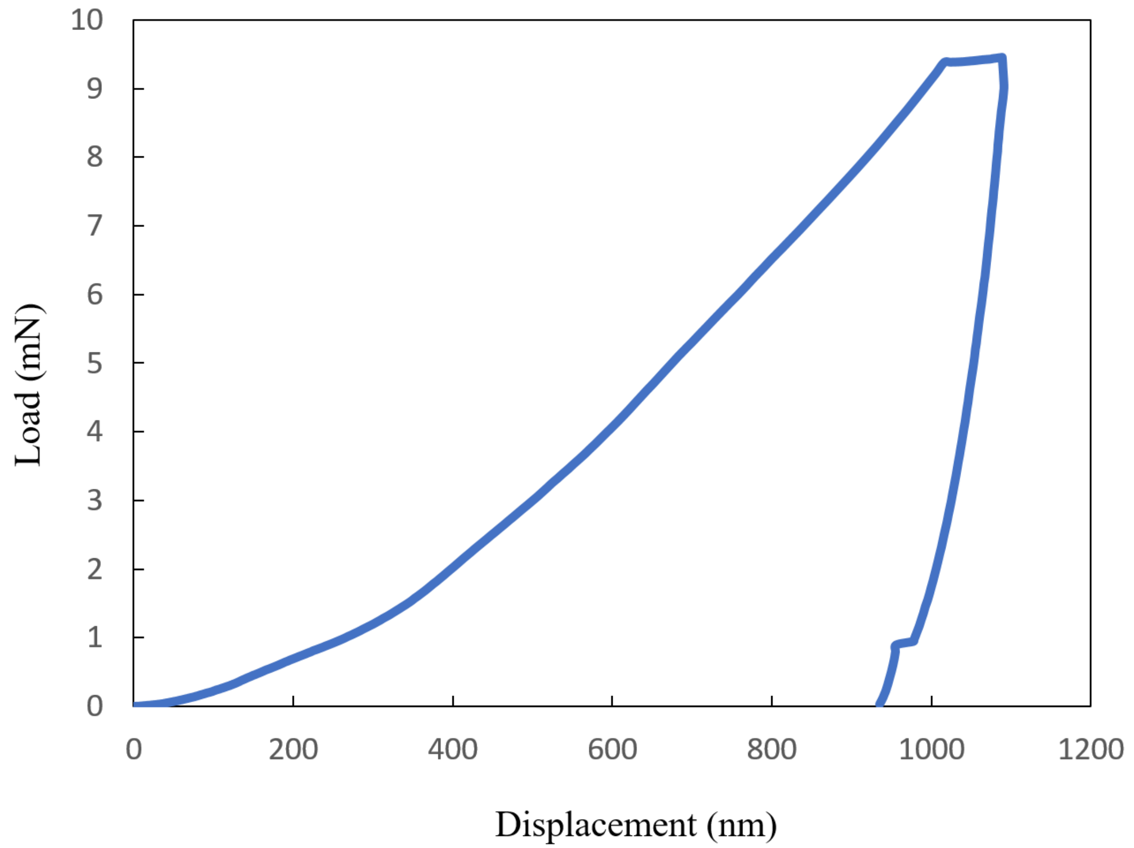


Figure 36. Representative load vs displacement curve for the microconstituents of the stack. Each layer was indented up to a depth of 1 μm.

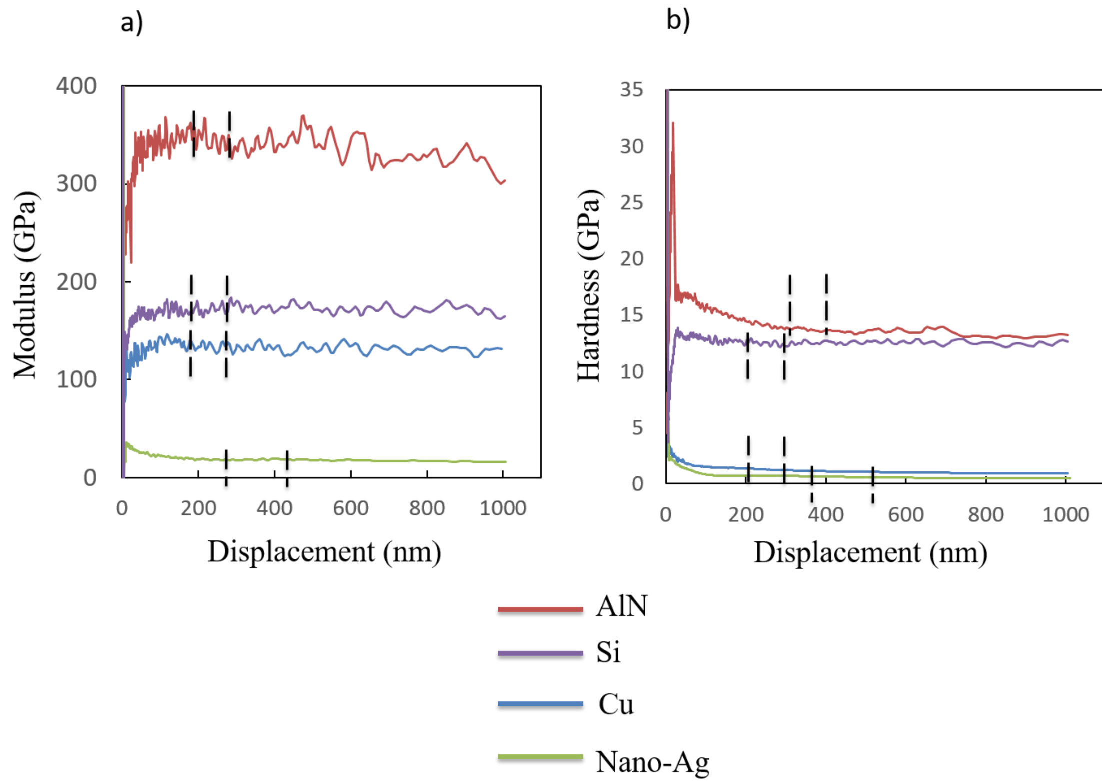


Figure 37. Nanoindentation behavior of the different layers in the nano-Ag stack, a) Modulus vs Displacement, b) Hardness vs Displacement.

Table III. Young's modulus and Hardness obtained by nanoindentation for microconstituents of the sample.

	Cu	**AlN**	**Nano-Ag**	**Si**
Young's Modulus (GPa)	129 ± 5	347.4 ± 7	20.3 ± 1.2	172 ± 1.3 [100] orientation
Hardness (GPa)	1.31 ± 0.07	15.2 ± 0.8	0.5 ± 0.04	12.5 ± 0.1

The nanoindentation results can be seen in Fig. 37 (a-b) and in Table III. The dotted lines marked on the modulus and hardness plots correspond to the plateau region of the curve

from which the average values were taken. The AlN layer in the DBC substrate showed the highest Young's modulus at 347.4 GPa, whereas nano-Ag solder showed the lowest value at 20 GPa. A similar trend was followed for the hardness values of the multiple layers in the stack, where AlN had the highest value at 15.2 GPa and nano-Ag had the lowest hardness value at 0.5 GPa.

4.4.3. Bond Quality Analysis by Shear Testing

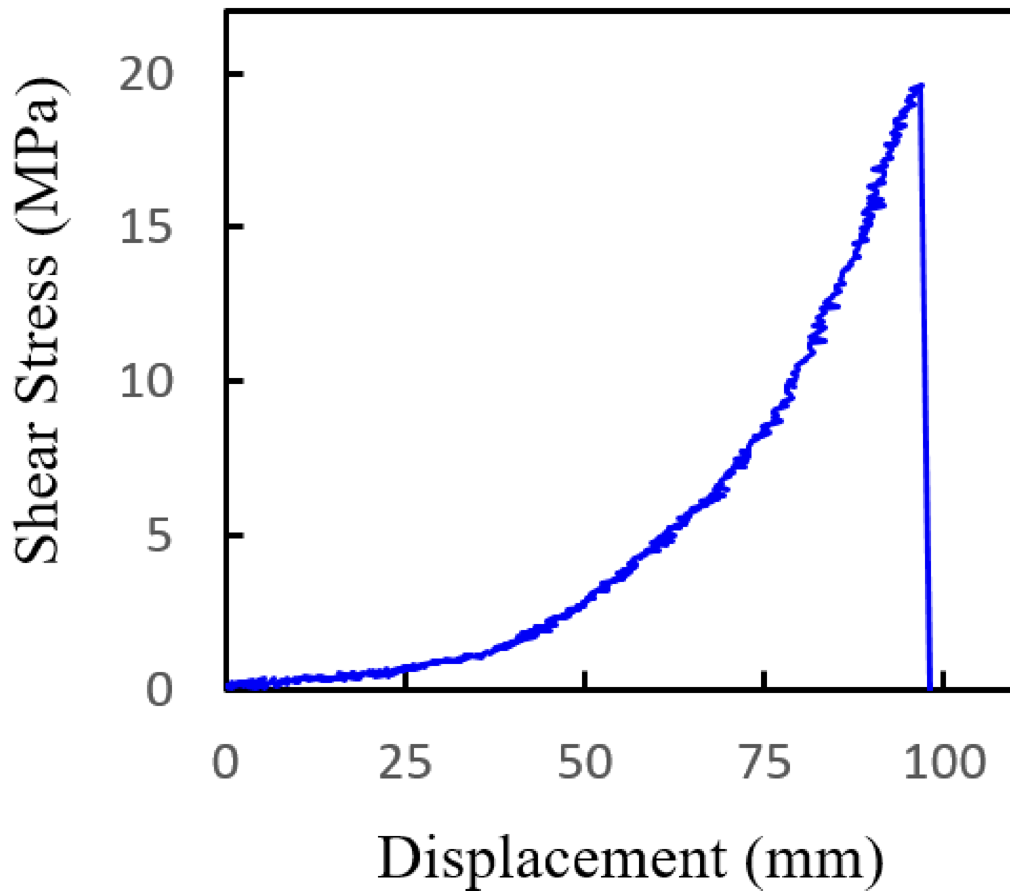


Figure 38. Shear stress vs displacement curve of a nano-Ag solder joint.

Fig.38 shows a characteristic shear stress vs displacement curve. The initial part of the curve which appears flat represents the portion of the test before the shear blade made full contact with the Si die. As the die comes in full contact with the shear testing blade, the shear stress increases. In the case of the nano-Ag samples the shear strength was 15±2.5 MPa, this value is comparable to shear strengths reported previously by Chua et al. (Chua and Siow 2016) and Wang et al. (Wang, Chen et al. 2007) where a shear strengths of 15-18 MPa for nano-Ag joints on DBC substrates were obtained. For all the samples tested, the fracture occurred through the thickness of the solder, indicating good bonding at the interfaces, as seen in Fig.39(a). Delamination was seen to occur at few places at the Si interface (Fig. 39(b)). A magnified image of the solder after shear testing is shown in Fig. 39(c).

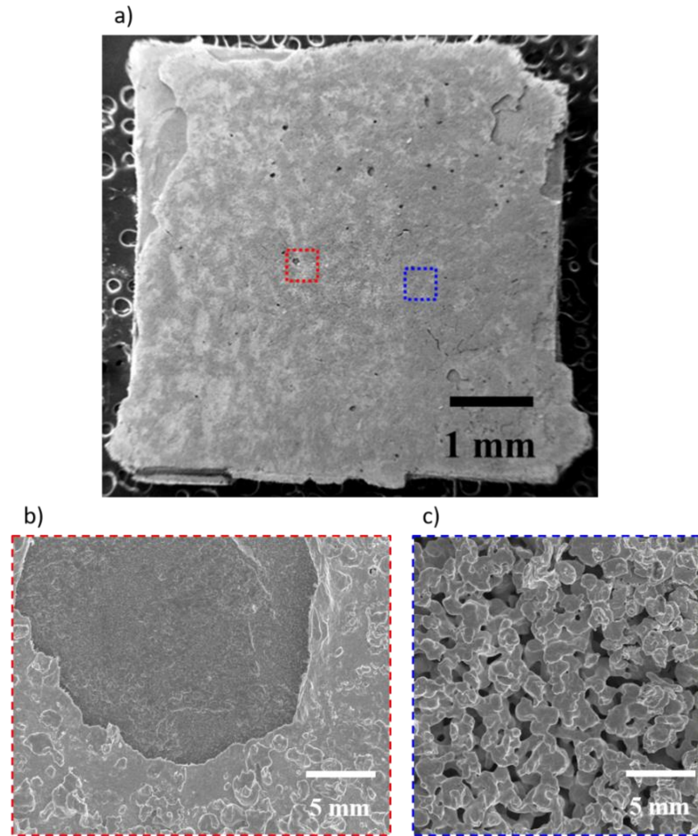


Figure 39. Fractography SEM image of nano-Ag solder joint after shear testing, a) fracture occurred through the thickness of the solder as seen in this image of the Si die side, b) delamination occurring at few places on the Si die-solder interface, c) magnified view of the nano-Ag solder showing coalescence of nano-Ag spheres.

4.4.4. Effect of Peak Temperature on Solder Degradation

Three thermal cycling tests were conducted to study the degradation of solder as a function of time. In all cases the sample was cycled from room temperature (20°C) to a peak temperature of 250°C (Test 1), 200°C (Test 2) and 175°C (Test 3). As discussed previously, the sample's microstructure was analyzed using 3D X-ray tomography, scans of the complete volume of the solder joint were taken prior to the thermal fatigue tests and after specific number of thermal cycles when the tests were stopped for scanning of the sample.

4.4.4..1.Test 1- ΔT=230°C

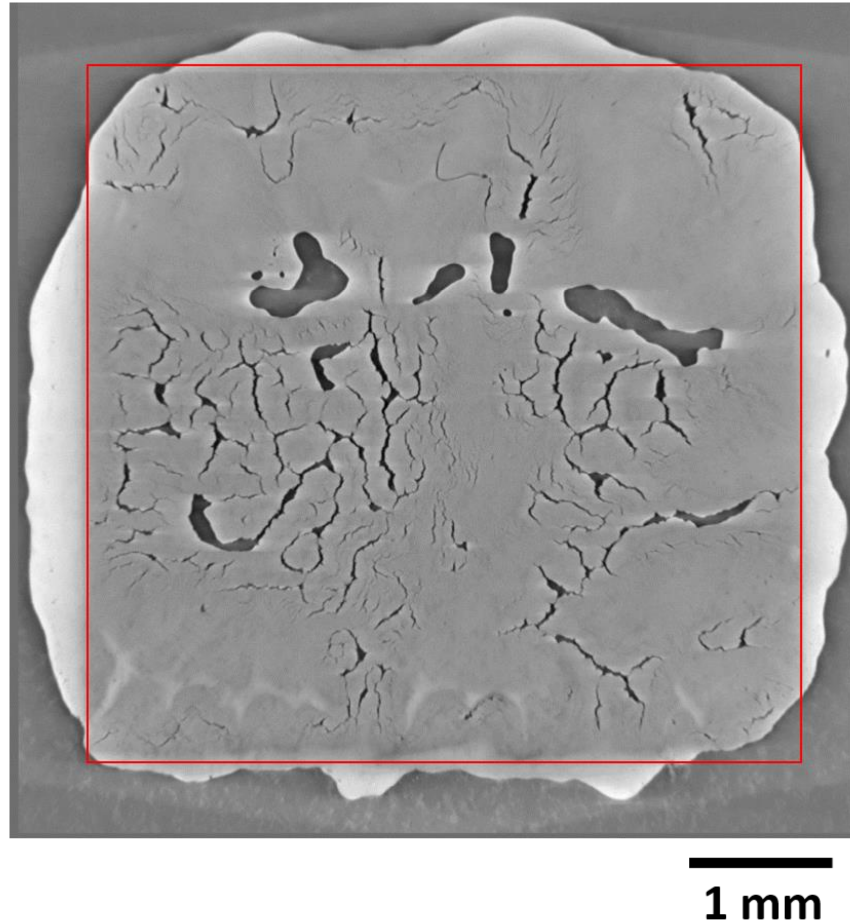


Figure 40. Slice of 3D X-Ray tomography scan showing nano-Ag solder prior to thermal cycling. The red square indicates the position of the 5 mm x 5 mm Si die that is placed on top the solder.

The initial solder microstructure of sample 1 (refers to sample tested under condition 1) is seen in Fig.40. The red box indicates the outline of the 5 mm x 5 mm Si die on top of the solder (as shown in Fig. 29). The white phase surrounding this box is solder that squeezed-out during sintering upon application of load. The light gray phase is the nano-Ag solder, the darker phase inside the box and within the solder show pores that are present in the as-

fabricated solder due to shrinkage of the solder or due to residual evaporated organics. The initial porosity of the solder volume was 6.9%.

After the initial X-Ray tomography scan, the sample was thermal cycled and additional scans were taken after 300, 750, 1000 and 3000 cycles to evaluate the degradation of the solder as a function of time. Degradation of the solder was seen in the form of cracks or delamination.

Given that the voxel size of the scan is 3 μm and the thickness of the bond line is about 30 μm, a total of 9 X-Ray 2D slices corresponded to the volume of the nano-Ag solder bond. The sample was removed from the thermal cycling setup and mounted for X-ray at every step. Because of this handling, a slight misalignment in the scans was observed. To correct for this misalignment, and to accurately compare data sets from one scan to another, a Matlab based alignment procedure was followed, and is described below.

1. The full 3D stack for 2 cycles (0 cycles and the 'X' cycles being compared) are imported as *.raw file in ImageJ (Bethesda, MD, USA).
2. Using ImageJ, fiducial marks that are identical in both stacks are selected in each stack and their coordinates in X,Y,Z are recorded. For accuracy in the alignment, a minimum of 10 pairs was taken in the solder, and 5 pairs at each Cu-AlN interface.
3. The X,Y,Z coordinates will be used as input in a Matlab code developed in our lab. The code converts the coordinates in the form of a matrix and transposes the 'X' cycles matrix to match the position for each fiducial mark in the 'X' cycles stack to the location of the corresponding fiducial marks in the 0 cycles stack.

4. A new stack is generated by Matlab, and this is used for the comparison of features before and after thermal cycling.

Fig. 41(a-e) shows individual aligned images of a slice in the nano-Ag solder layer. The evolution of damage in the microstructure over 3000 cycles can be observed. The initial microstructure of the nano-Ag solder is shown in Fig. 41(a), the sample's microstructure contains initial porosity as discussed earlier. The microstructure after 300 thermal cycles at $\Delta T=230°C$ is shown in Fig. 41(b), minimal crack formation was seen in the solder within the 5 mm x 5 mm region. Fig. 41(c) shows the sample after 750 thermal cycles. A slightly higher density of cracks is observed in the solder, most of the crack formation is seen in the center of the 5 mm x 5 mm region. After 1000 cycles the damage in the form of cracks is more evident in the solder, Fig. 41(d), the same trend was seen with crack formation concentrating in the center portion of the solder. After 3000 thermal cycles (Fig. 41(e)) crack formation was more severe and some dark spots were seen to have form in the solder.

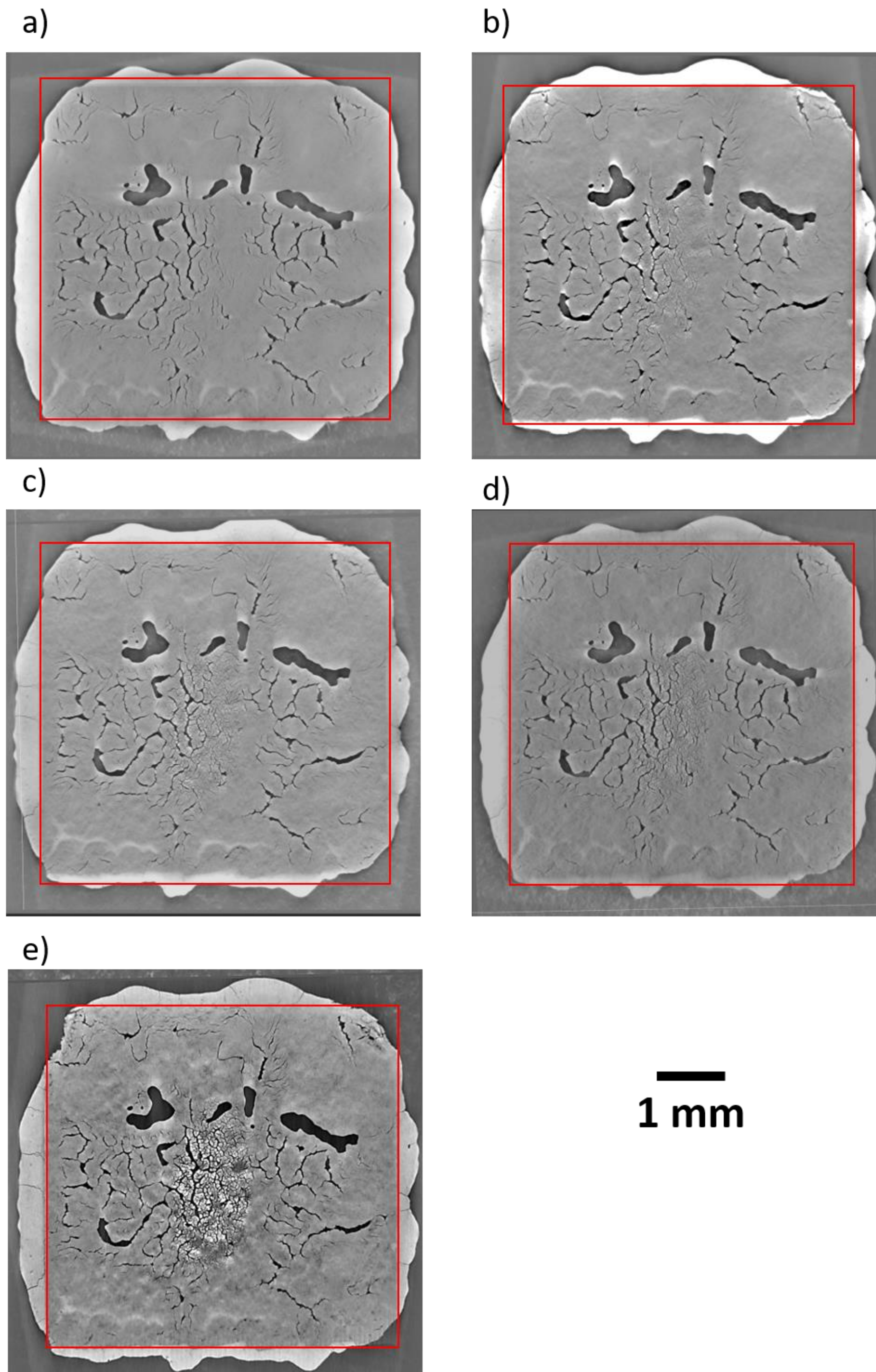


Figure 41. Microstructural damage evolution of nano-Ag solder during thermal cycling from 20°C to a peak temperature of 250°C, a) 0 Cycles, b)300 Cycles, c) 750 Cycles, d) 1000 Cycles, e) 3000 Cycles.

- Solder Delamination

After 3000 thermal cycles, dark spots within the solder were observed as seen in Fig. 42 (a-b). These spots were only found close to the center portion of the 5 mm x 5 mm solder area and was an indication of possible delamination occurring at the interfaces.

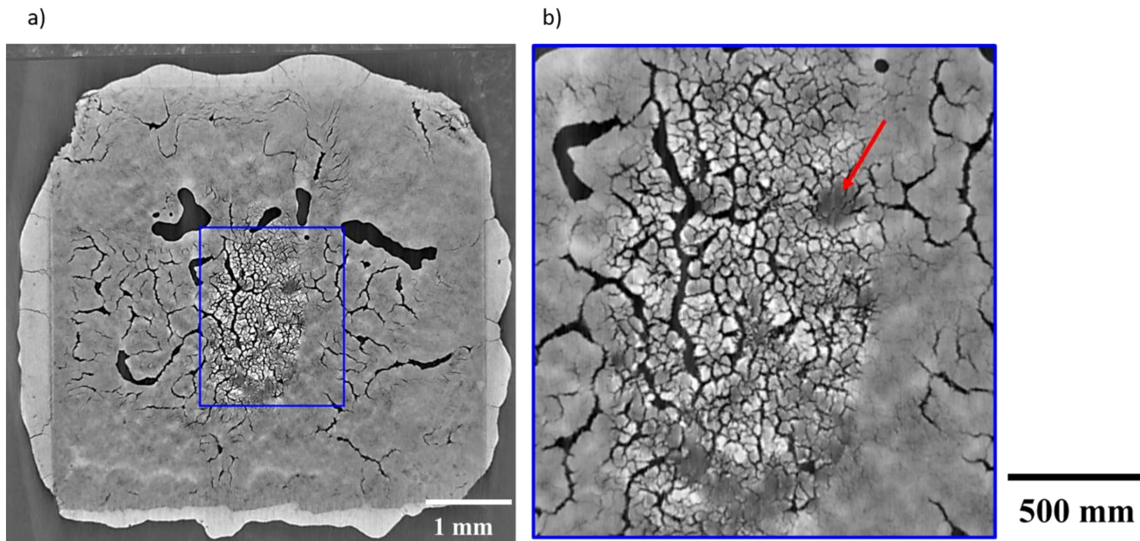


Figure 42. a) Microstructure of nano-Ag solder after 3000 thermal cycles with ΔT=230°C, the blue box shows the region where the delamination damage was seen, b) Magnified view of the region of delamination of solder.

To verify if the black spots within the solder were in fact solder delamination (Fig. 43(a)), the 3D X-Ray stack was analyzed on different orthogonal planes to observe these spots on a different plane. The stack was re-sliced using ImageJ, to digitally cross-section along the XZ (Fig. 43(b)) and YZ planes (Fig. 43(c)). This enabled the visualization and confirmation of the delamination of the solder. This type of analysis is only possible in a time resolved, non-destructive characterization technique such as 3D x-ray tomography.

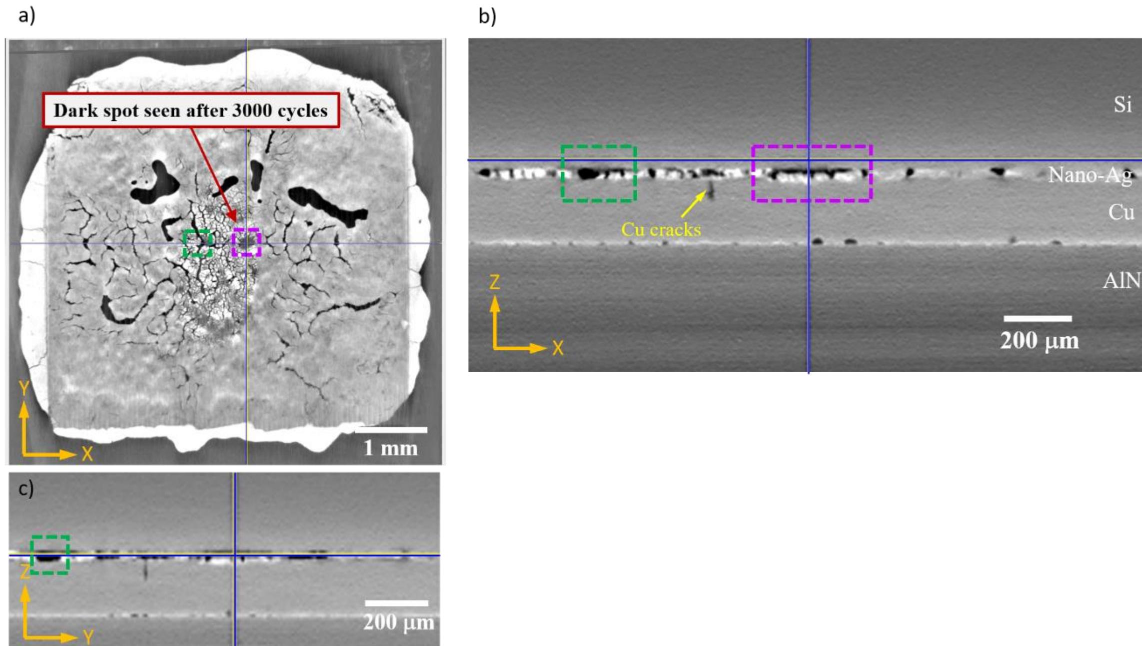


Figure 43. Nano-Ag solder joint after 3000 thermal cycles at ΔT=230C°viewed at different planes, a) XY view of sample showing nano-Ag solder, b) XZ view of the solder stack showing the multiple layers in the solder joint, c) YZ plane view of sample.

The purple box in Fig. 43(a) is showing the dark spot of delamination in the solder, viewed on the XY plane, the same feature is shown on the XZ plane. It can be clearly seen that delamination occurred at the interface between Si and solder. The excessive micro-crack formation seemed to have severely weakened this region to cause localized failure at the Si-solder interface.

The green box shown in Fig. 43(a) shows a pore that was present in the initial microstructure of the sample. In Fig. 43(b) the same pore is shown in a green box, here it can be seen that it spans the entire thickness of the solder.

- Crack formation on DBC substrate

In addition to crack formation on the solder and delamination at the Si-solder interface, cracks were also seen to form within the Cu layer in the DBC substrate. These Cu cracks were seen to form as early as 300 thermal cycles and they formed directly below the region where most of the damage accumulated on the solder. The cracks seemed to extend as far as 30-50 μm below the solder interface. Fig. 44(a-e) show the growth of these cracks from the first time they were observed at 300 cycles up to 3000 cycles. Fig. 45 shows the cracks at the Cu layer viewed on the XZ plane.

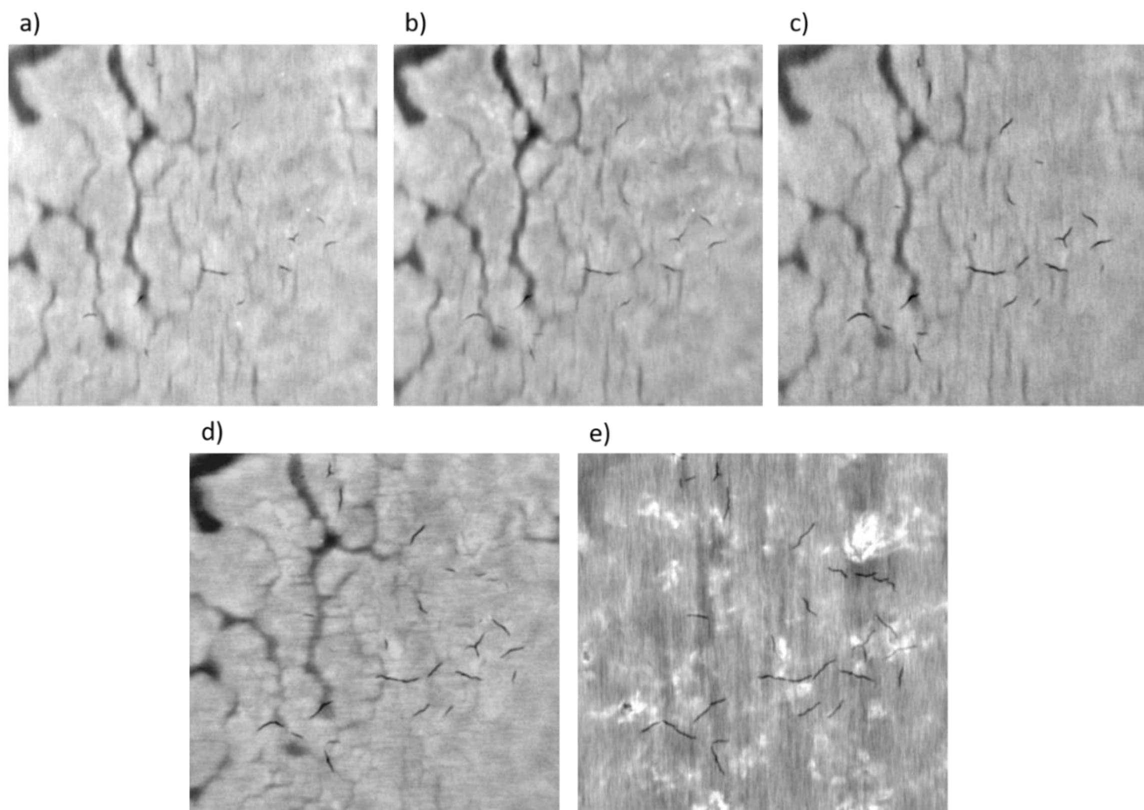


Figure 44. Crack formation and growth on Cu layer of DBC substrate as a result of thermal cycling, a) 300 Cycles, b) 500 Cycles, c) 750 Cycles, c) 1000 Cycles, e) 3000 Cycles.

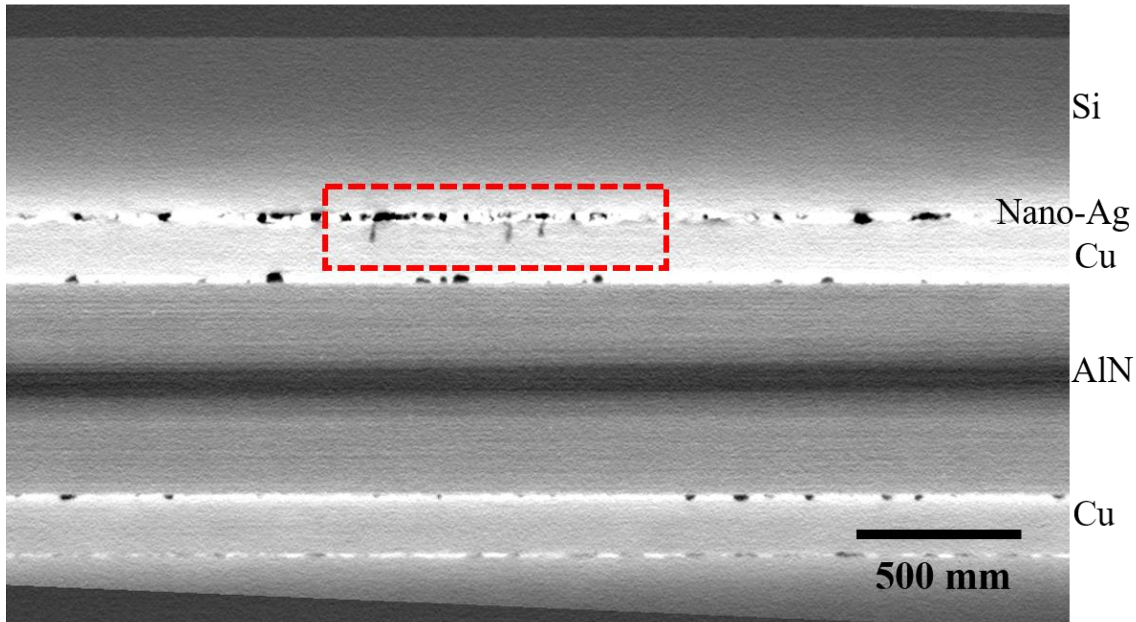


Figure 45. Solder joint stack viewed in the XZ plane. Red box shows crack formation at the Cu layer in the DBC substrate.

- Quantification of Damage/crack growth

To quantify the damage induced on the solder, the software Avizo® (VSG, Burlington, MA, USA) was used to segment the voids and microcracks in 3 dimensions, that formed because of thermal cycling. Fig. 46(a-c) shows the procedure followed for image segmentation. As a first step, the stack of slices to be segmented are imported into the software (Fig. 46 (a)). Then, using the 'Region Growth' tool, multiple pores/cracks can be selected based on their gray scale value (Fig. 46(b)). The region grow tool selects all connected features (cracks) based on the user defined gray scale range. A fully segmented image is shown in Fig. 46(c).

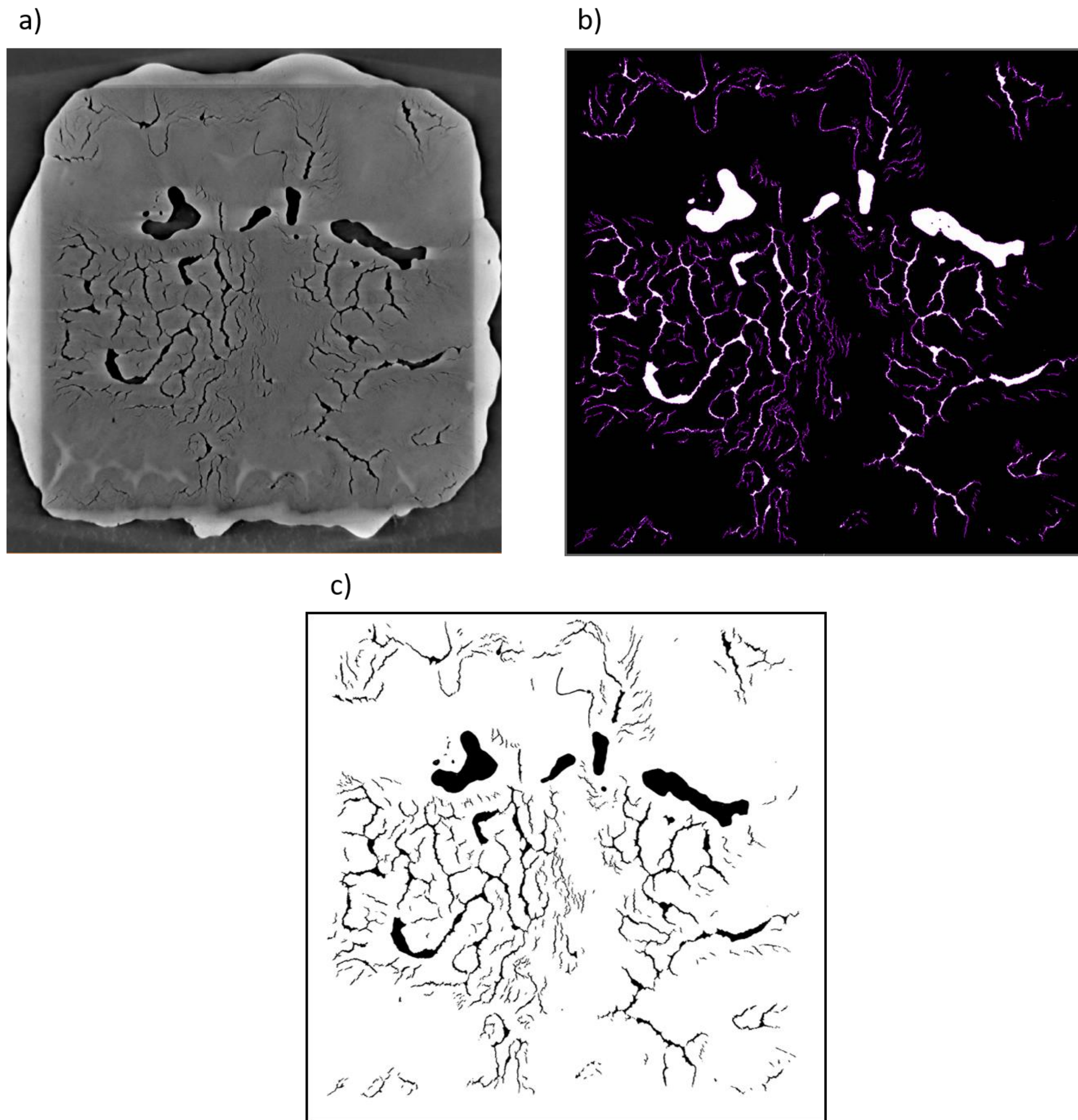


Figure 46. Image segmentation procedure in Avizo, a) 3D stack is imported into the software, b) The tool 'Region Growth' is selected to select cracks/pores based on its grey scale value, c) Final segmented image.

The above-mentioned procedure was followed for the segmentation of all cycles in all tests. Fig. 47 (a-e) shows an overlay of the segmented images for Sample 1 at 0, 300, 750, 1000 and 3000 cycles. With the help of these segmented images it can be seen how most of the damage is concentrated in the center of the Si die region on the solder.

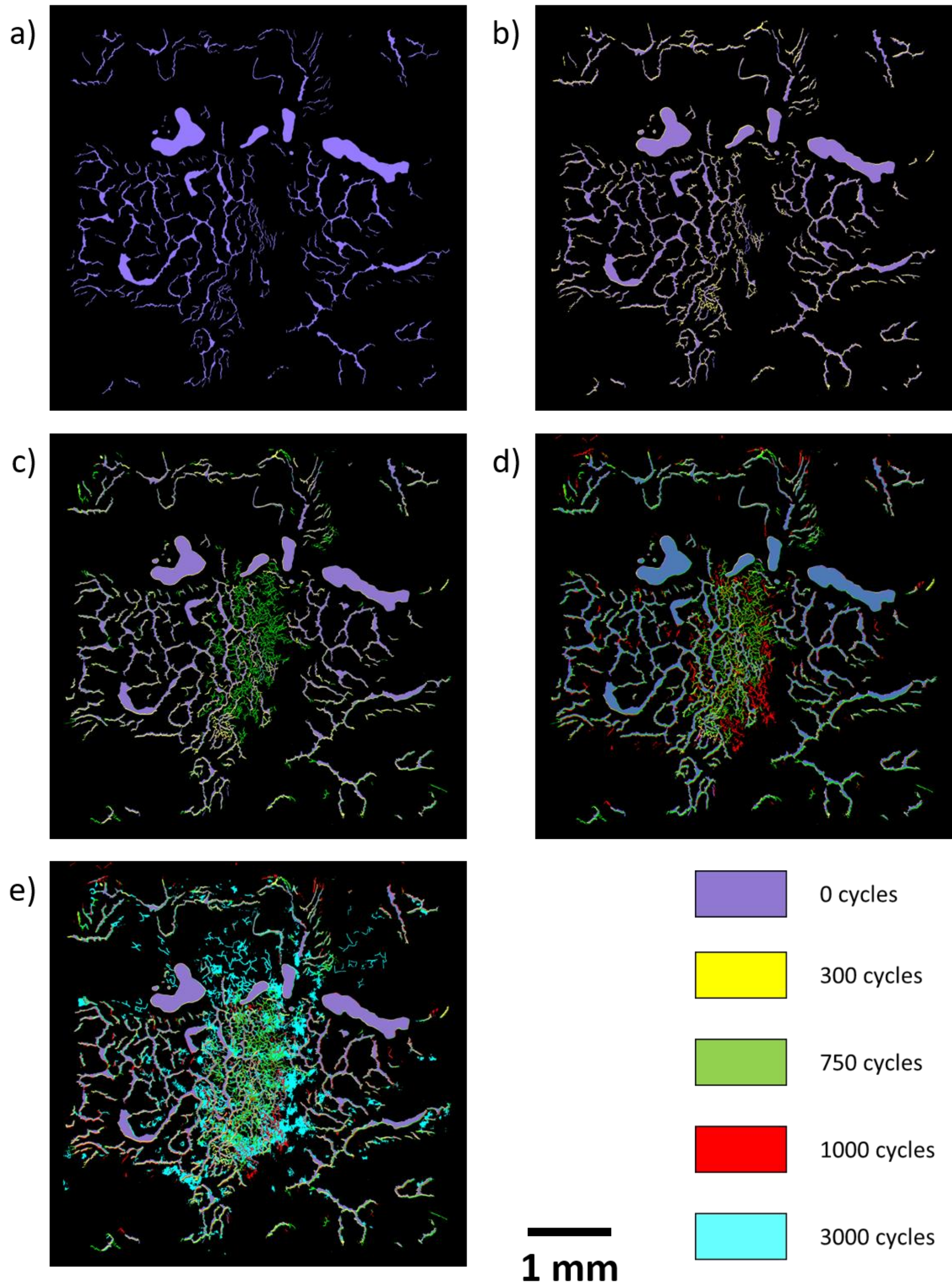


Figure 47. Cracks in the solder are segmented and color coded from 0-3000 cycles. a) 0 Cycles, b) Overlay of 0-300 Cycles, c) Overlay of 0-750 Cycles, d) Overlay of 0-1000 Cycles and e) Overlay of 0-3000 cycles.

Using the segmented images is possible to quantify the damage through the volume of the sample. For a more thorough analysis of microstructural degradation on the solder the volume of the sample was divided into 9 sections as shown in Fig. 48. The volume fraction of cracks as well as the increase in cracks per individual sector are shown in Fig. 49(a-b). In these plots it can be seen, that most of the damage on the sample was localized at the center region of the sample. An increase of 35% in crack density was seen on region 5 of the sample after 3,000 thermal cycles. The least increase in crack density was seen in sectors 1, 3, 7 and 9 which are in the corners of the sample.

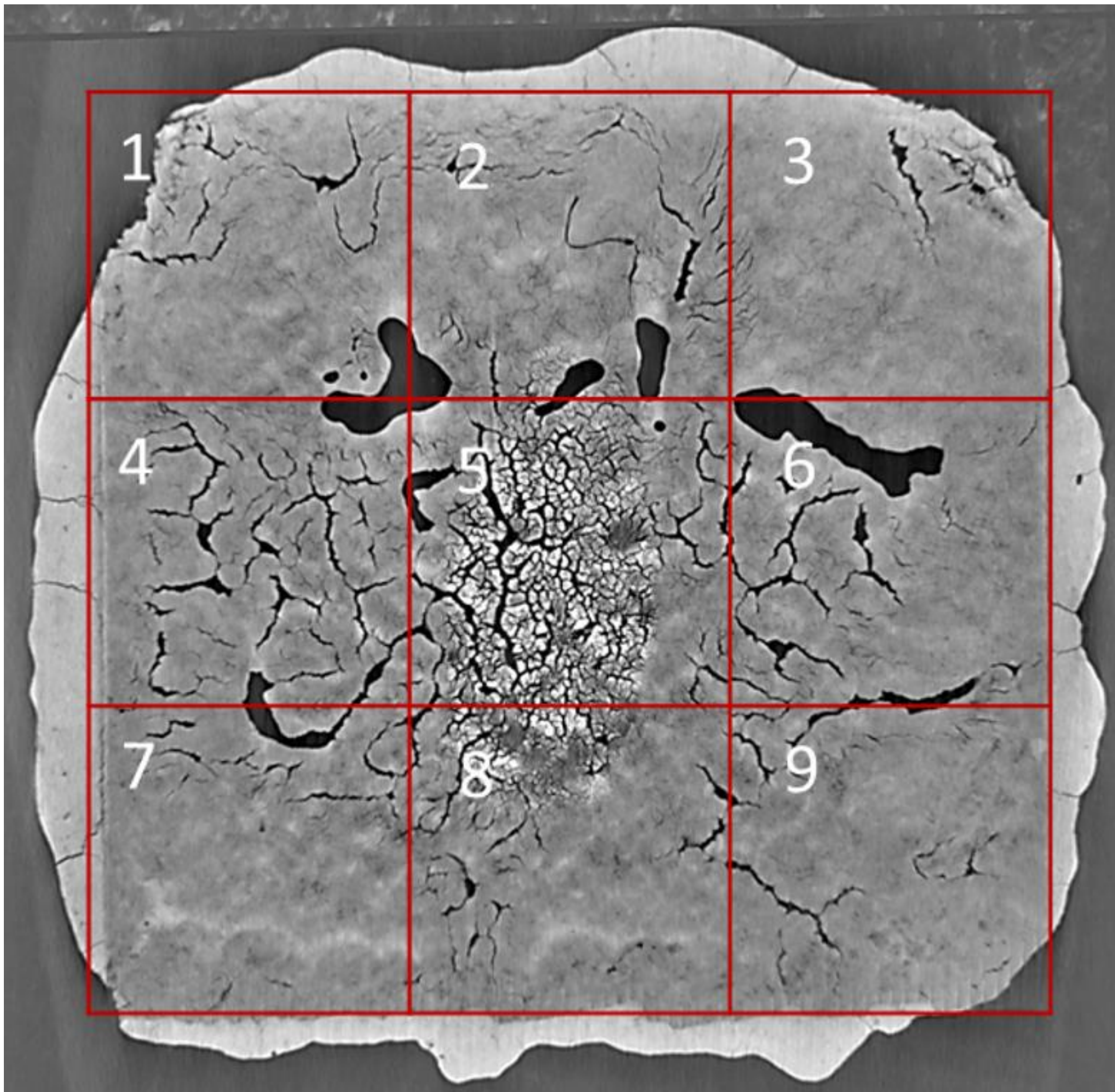
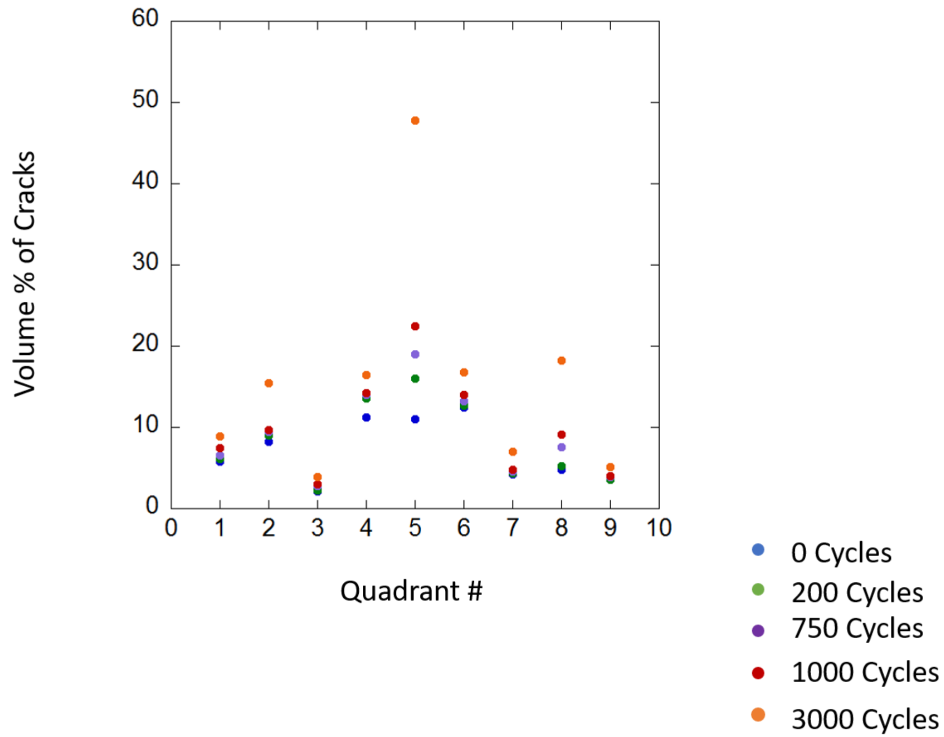


Figure 48. Solder area divided into 9 segments for analysis of crack density per region.

a)



b)

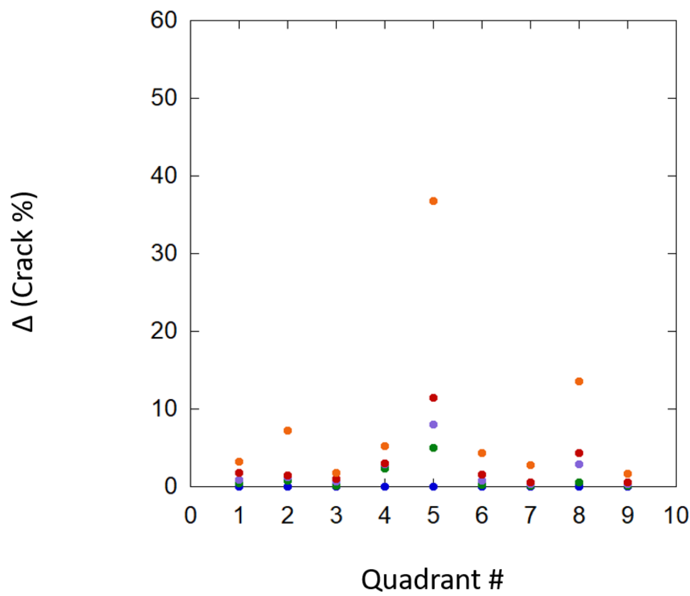


Figure 49. Increase of crack density per quadrant, a) Actual crack % for each cycle/step, b) Increase in crack % with respect to 0 cycles.

- Decrease in Effective Young's Modulus as a function of crack density

To quantify the effect of the damage induced by crack formation on the mechanical properties of the nano-Ag solder, the decrease in effective Young's modulus for each sector of the sample at different number of cycles was calculated (Fig. 50(a-b)). Two approaches were used to calculate the decrease in effective Young's modulus – the first one corresponds to the Wachtman and MacKenzie method (Mackenzie 1950, Wachtman Jr 1969), (equation 4).

$$E = E_0(1 - 1.9p + 0.9p^2) \qquad \text{Equation 4}$$

Where,

E_0= Young's modulus

E= Reduced Young's modulus

p= Void fraction

The second approach used to calculate the decrease of Young's modulus with crack formation corresponds to the O'Connell and Budiansky method (O'Connell and Budiansky 1974), (equation 5).

$$\frac{E}{E_0} = 1 - \frac{16(10-3\nu)(1-\nu^2)}{45(2-\nu)} f_s \quad \text{Equation 5}$$

Where,

E_0= Young's modulus

E= Reduced Young's modulus

ν= Poisson's ratio of porous material

f_s= Volume fraction of cracks

$$\nu = \nu_0\left(1 - \frac{16f_s}{9}\right) \text{ Equation 6}$$

Where,

ν_0= Poisson's ratio of fully dense material

ν= Poisson's ratio of porous material

f_s= Volume fraction of cracks

The Young's modulus of the nano-Ag solder was taken from nanoindentation results. The volume fraction of cracks/void fraction was taken from segmented 3D scans, and Poisson's ratio was taken from literature as 0.367. It should be noted that in MacKenzie relationship the constants 1.9 and 0.9 are accurate for Poisson's ratio of 0.3. Hence the results for Young's modulus reported here are close estimates. For O'Connell relationship, the moduli approach zero with increasing crack density and vanishes for fs=9/16. The accuracy of effective Young's modulus near fs= 9/16 is not known(O'Connell and Budiansky, 1974).

As-sintered nano-Ag solder has inherent pores that are in the micron to submicron scale. Focused Ion Beam cross-sections were done in as-sintered samples to quantify these pores. Fig. 51(a-b) shows a FIB cross-section with network of fine pores. Grayscale thresholding was done to segment these pores, and results showed a porosity fraction of 32%. This area fraction was consistent over multiple samples. During Young's modulus analysis the total

porosity was taken as the sum of large pore fraction obtained from 3D X-Ray and a uniform fine porosity fraction of 32% in the remaining solder volume which were not resolved in X-Ray.

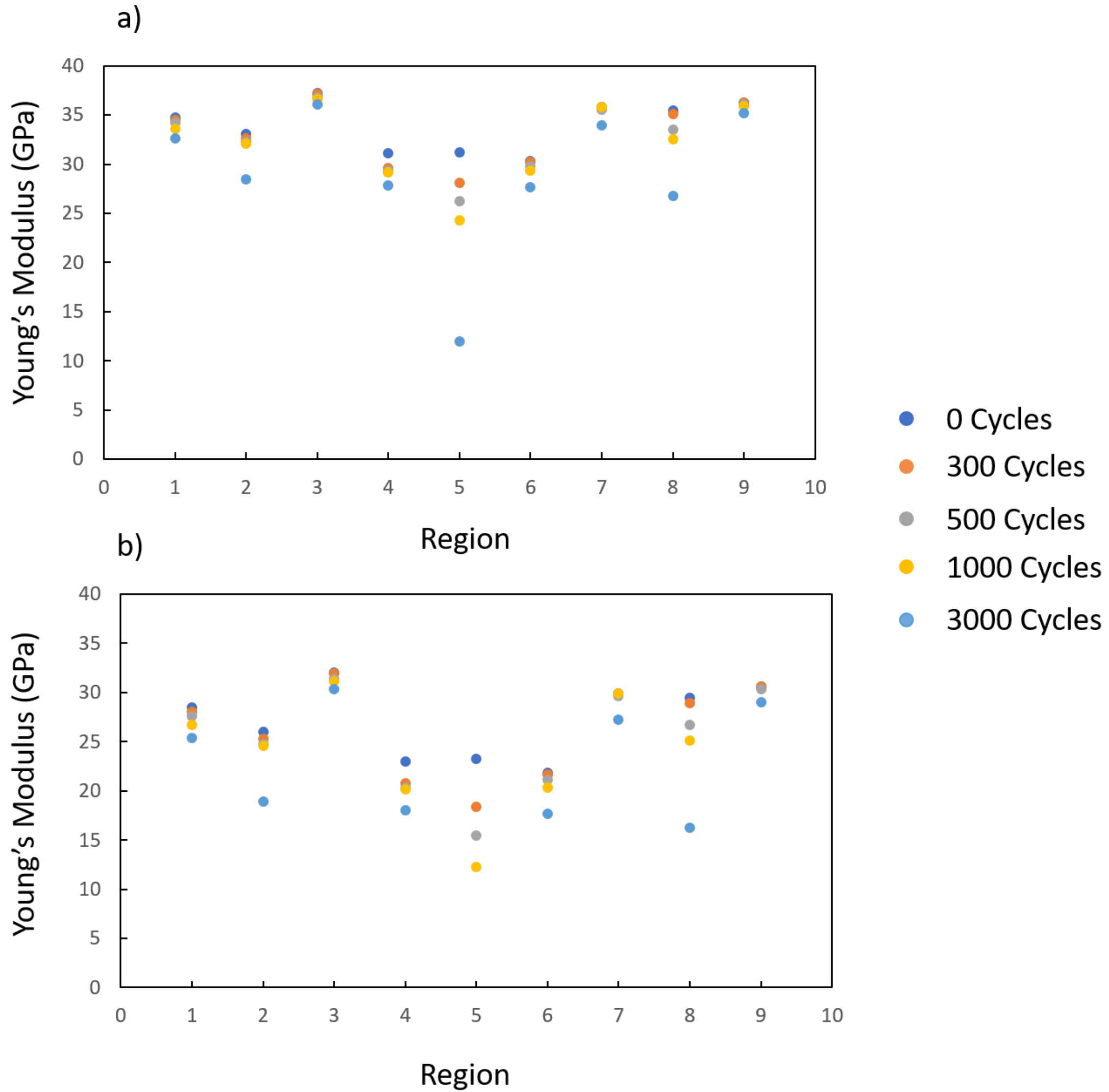


Figure 50. Decrease in effective Young's modulus according to a) Wachtman and MacKenzie relation b) O'Connell and Budiansky relation. A clear effect of thermal cycling is observed on the mechanical properties of nano-Ag solder, where crack formation results in a decrease of Young's modulus.

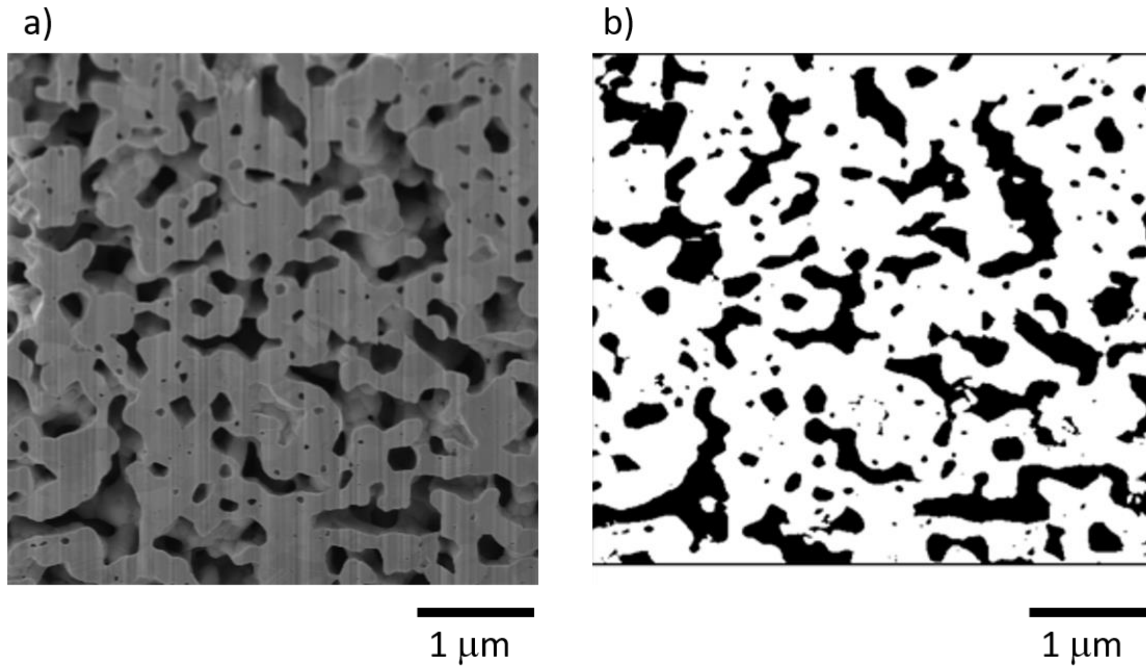


Figure 51. a) FIB cross-section of as-sintered nano-Ag solder showing a network of fine pores uniformly distributed within the solder volume, b) Binary image of fine pores obtained using grayscale thresholding technique.

4.4.4..2.Test 2- ΔT=180°C

A similar analysis to the one done for Test 1 was done for to study the sample in Test 2. For this test, the sample was thermal cycled from 20°C to 200°C. Fig. 52 shows an X-Ray scan with the initial microstructure of the nano-Ag solder. Like sample 1, this sample showed the presence of initial porosity in its microstructure, the initial void content in the 3D volume of the solder was 8.25%.

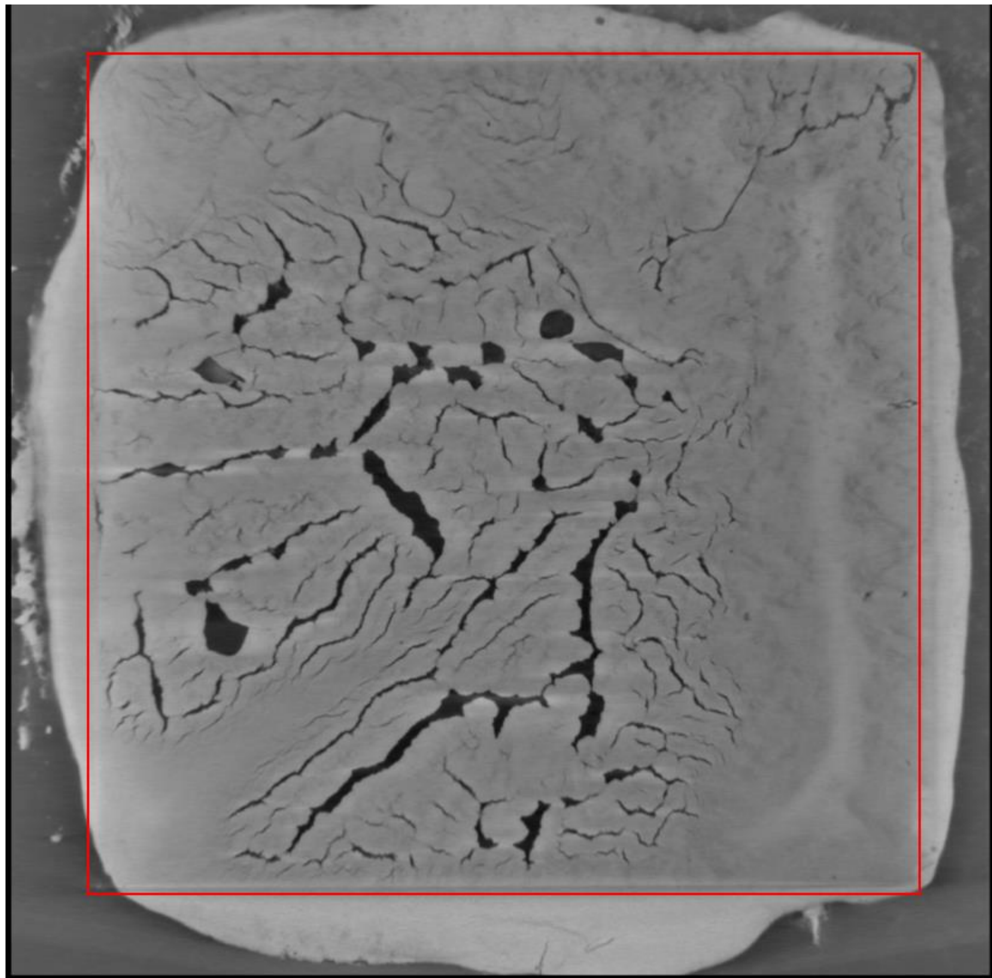


Figure 52. X-Ray images showing the initial microstructure of Sample 2, with an initial pore volume fraction of 8.25%.

After the initial scan the thermal cycling test was carried out. The test was stop periodically to take 3D X-Ray scans of the volume of the solder joint to study the degradation of the sample. Fig. 53 (a-e) shows the evolution in the solder's microstructure from 0-3000 thermal cycles.

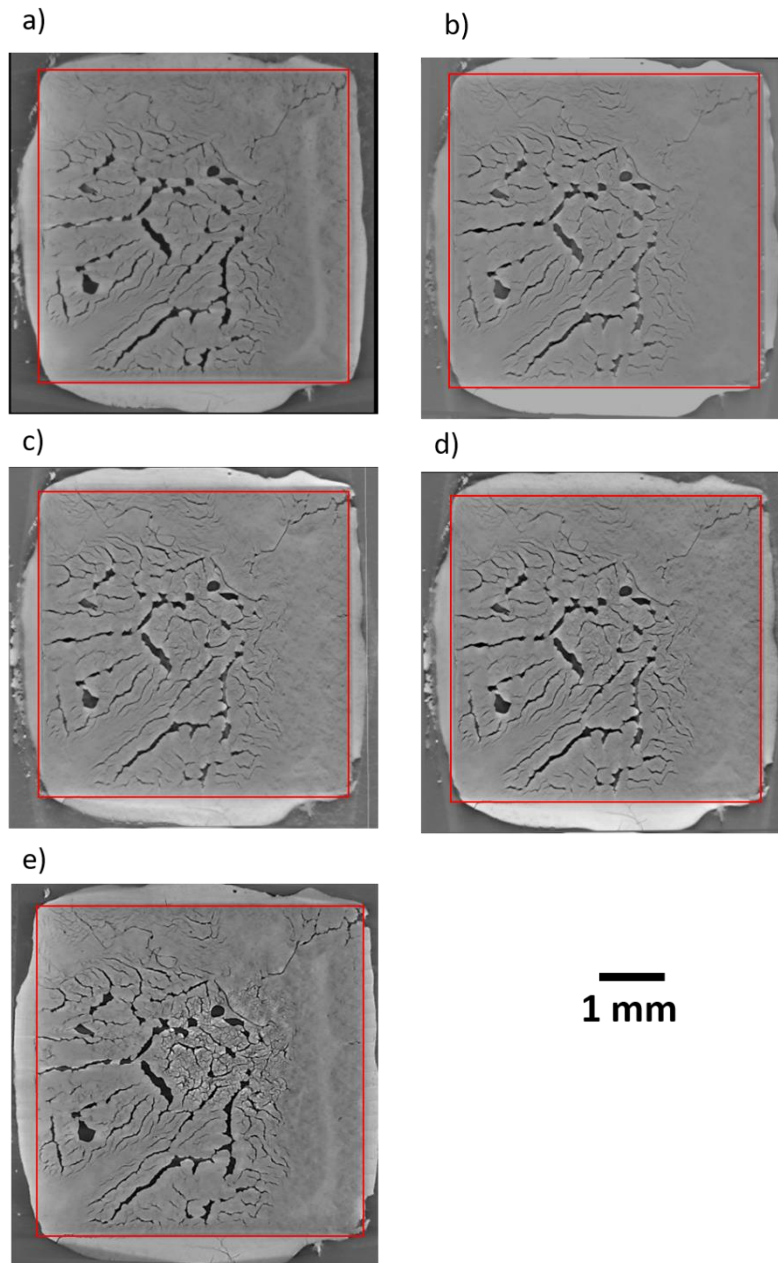


Figure 53. Microstructural damage evolution of nano-Ag solder during thermal cycling from 20°C to a peak temperature of 250°C, a) 0 Cycles, b)300 Cycles, c) 750 Cycles, d) 1000 Cycles, e) 3000 Cycles.

A similar trend as described in the previous section was seen as Sample 2 showed most of the microcracks forming close to the center region of the sample after 3000 cycles. The crack formation during the first 750 cycles (Fig. 53(a-c)) seems to be minimum, however

after 1000 cycles the microstructural damage becomes more evident by looking at the X-Ray scans. This can be verified by quantifying crack density in the sample, and will be addressed in the upcoming sections.

- Solder Delamination

Minimum solder delamination was observed delamination was observed on the sample after 3000 cycles. Fig. 54(a-b) shows delamination occurring on the solder after 3000 cycles as seen in the XY plane.

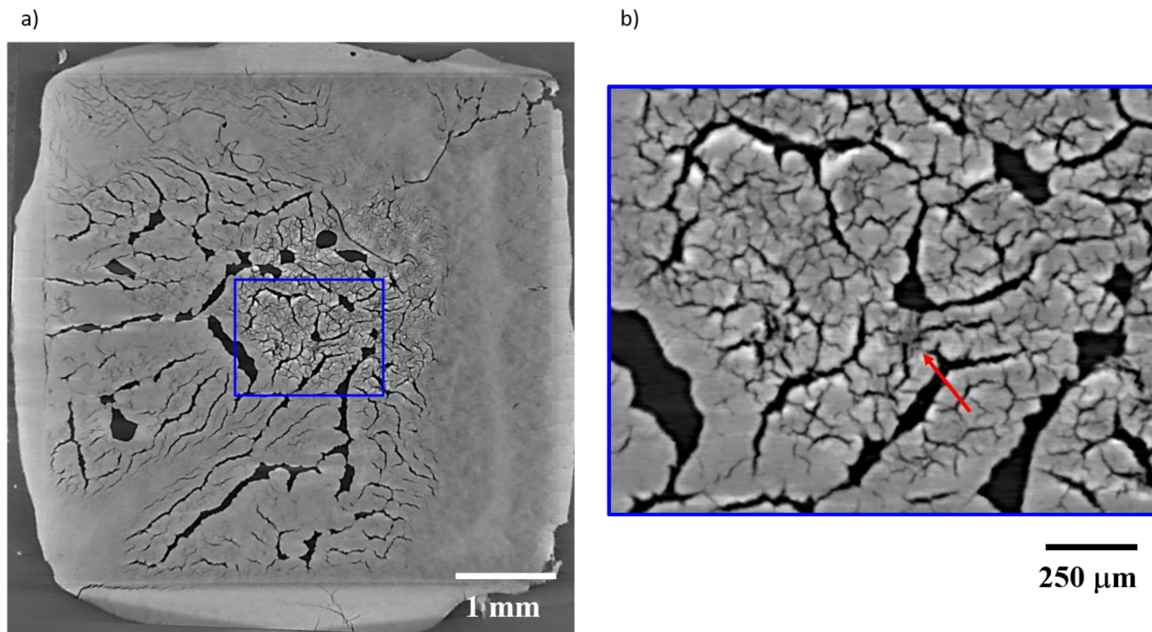


Figure 54. a) Microstructure of nano-Ag solder after 3000 thermal cycles with ΔT=180°C, the blue box shows the region where the delamination damage was seen, b) Magnified view of the region of delamination of solder.

- Crack formation on DBC substrate

Crack formation was observed on the top Cu layer of the DBC substrate. Cracks were first seen to appear after 500 thermal cycles (ΔT=180C°). As the number of thermal cycles increased, the number of cracks increased. Fig. 55(a-c) shows the evolution of these cracks as a function of time. The region of the Cu where these cracks formed seemed to align well with the region of the solder where crack formation was localized.

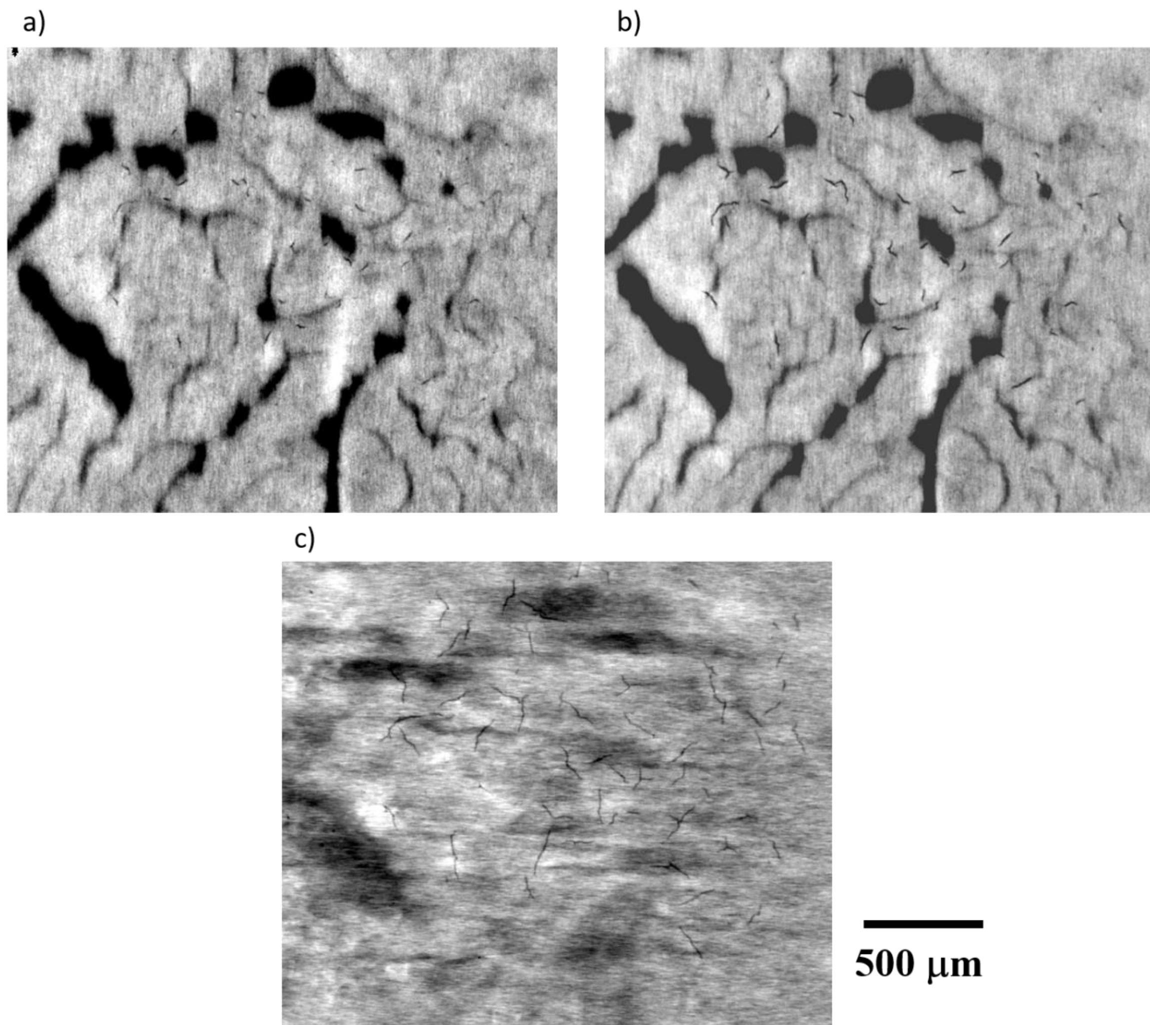


Figure 55. Crack formation and growth on Cu layer of DBC substrate because of thermal cycling, a) 500 Cycles, b) 1000 Cycles, c) 3000 Cycles.

- Quantification of Damage

Image segmentation for the 3D X-Ray scans was done. All cracks present in the volume of the nano-Ag solder were segmented and used for quantification of thermal induced damage as a function of time. The segmentation was done in Avizo following the segmentation procedure described before, Fig. 56(a-e) shows an overlay of the segmented images from 0-3000 cycles. Microcrack formation and delamination in this sample was seen to be less severe as compared to the damage observed in the sample with the highest temperature.

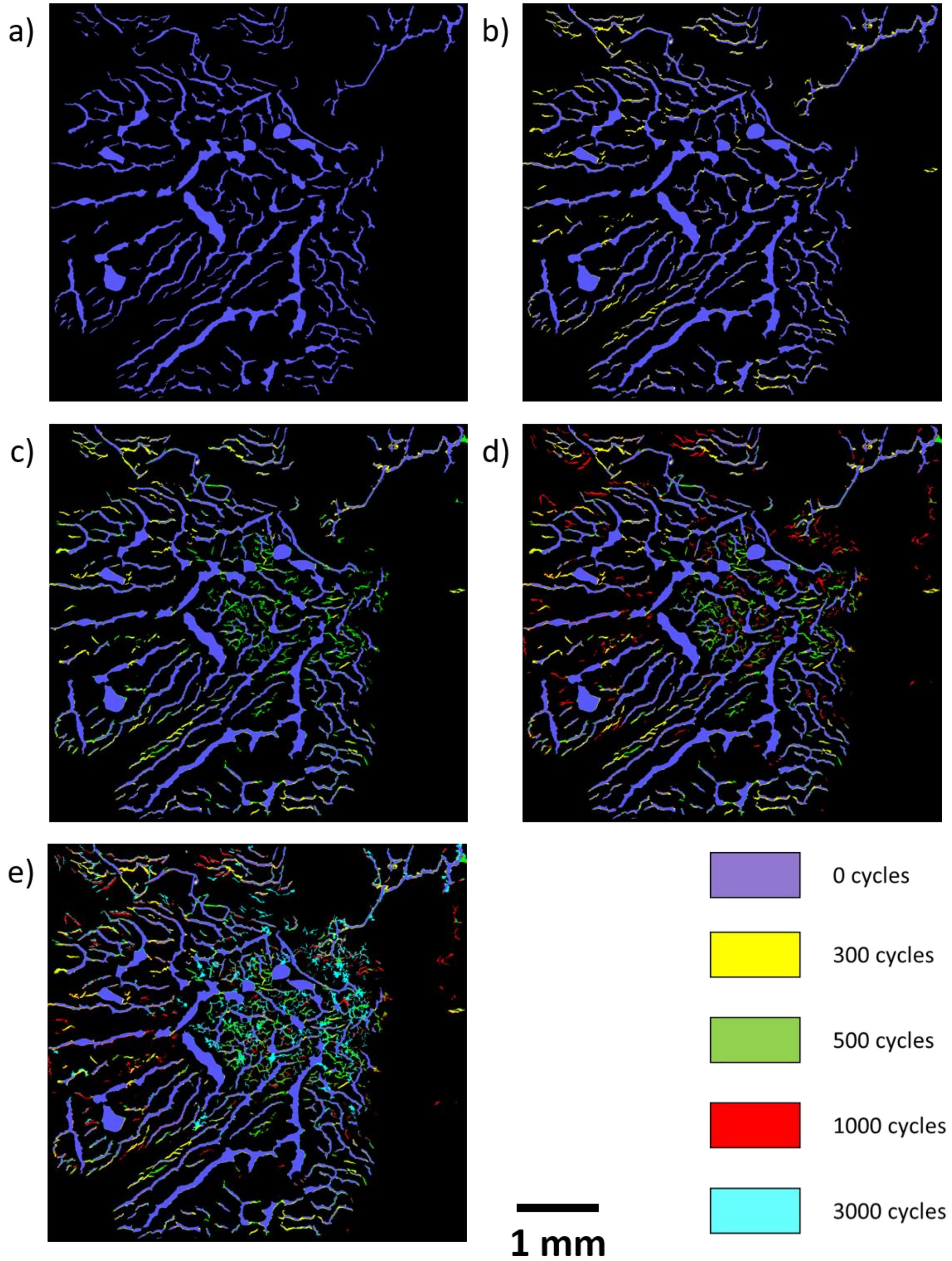


Figure 56. Cracks in the solder are segmented and color coded from 0-3000 cycles. a) 0 Cycles, b) Overlay of 0-300 Cycles, c) Overlay of 0-500 Cycles, d) Overlay of 0-1000 Cycles and e) Overlay of 0-3000 cycles.

The segmented images were used to quantify the volume fraction of pores within the solder layer, Fig.57 shows the sample divided into 9 segments to analyze where crack formation was localized.

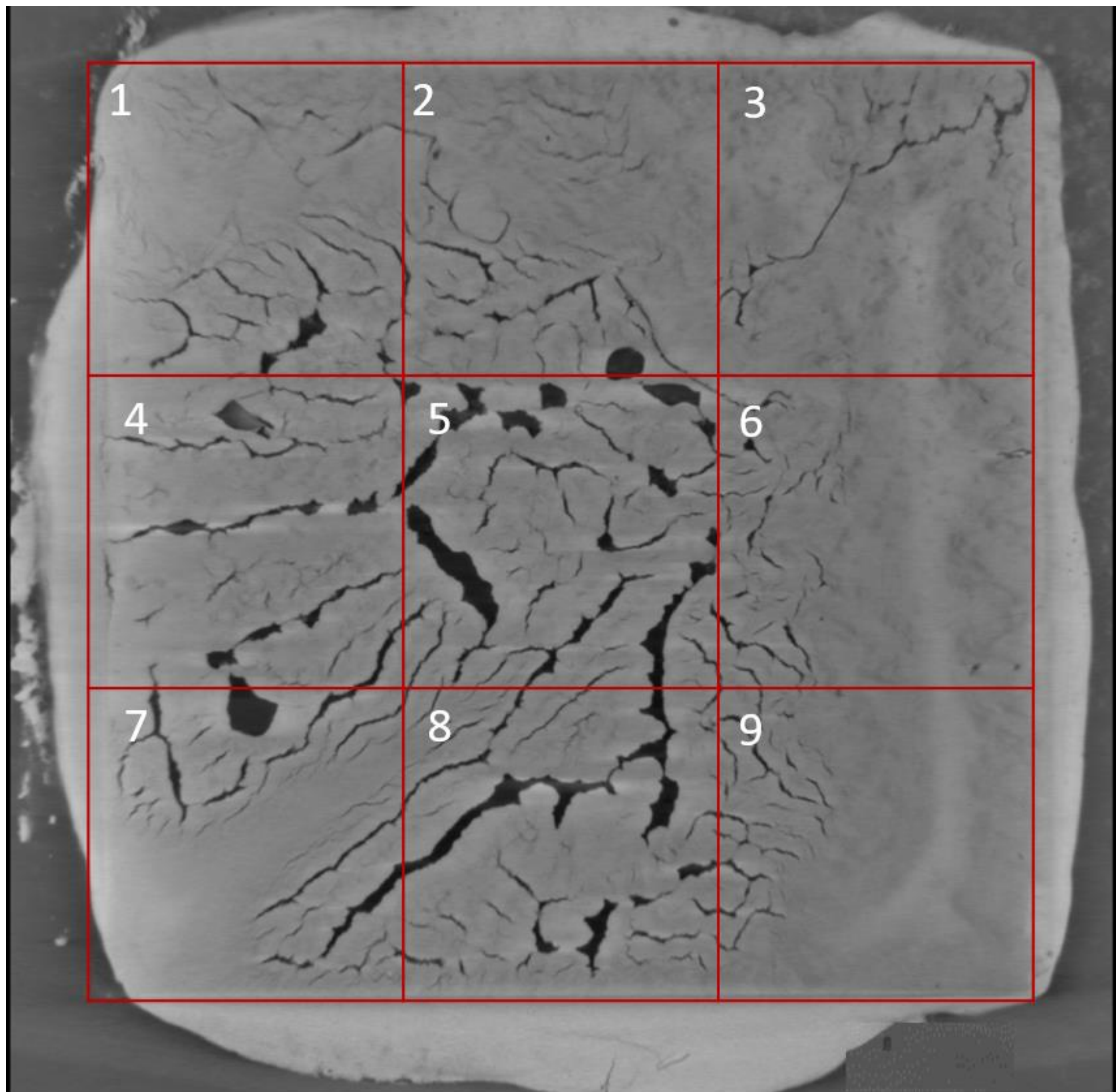


Figure 57. Solder area divided into 9 segments for analysis of crack density per region.

The volume of cracks was obtained for each segment in the sample the results are plotted in Fig. 58 (a-b). The actual volume of cracks is shown in Fig. 58(b) and the increment of cracks with respect to the initial microstructure of the sample. The largest increase in crack density was observed in region 5 similar to what was observed for Test 1.

After 3000 cycles region 5 in Test 2 had an increase of about 15% in crack volume, whereas Test 1 had an increase of 36% in crack density, which indicates an effect of peak temperature in microstructural damage.

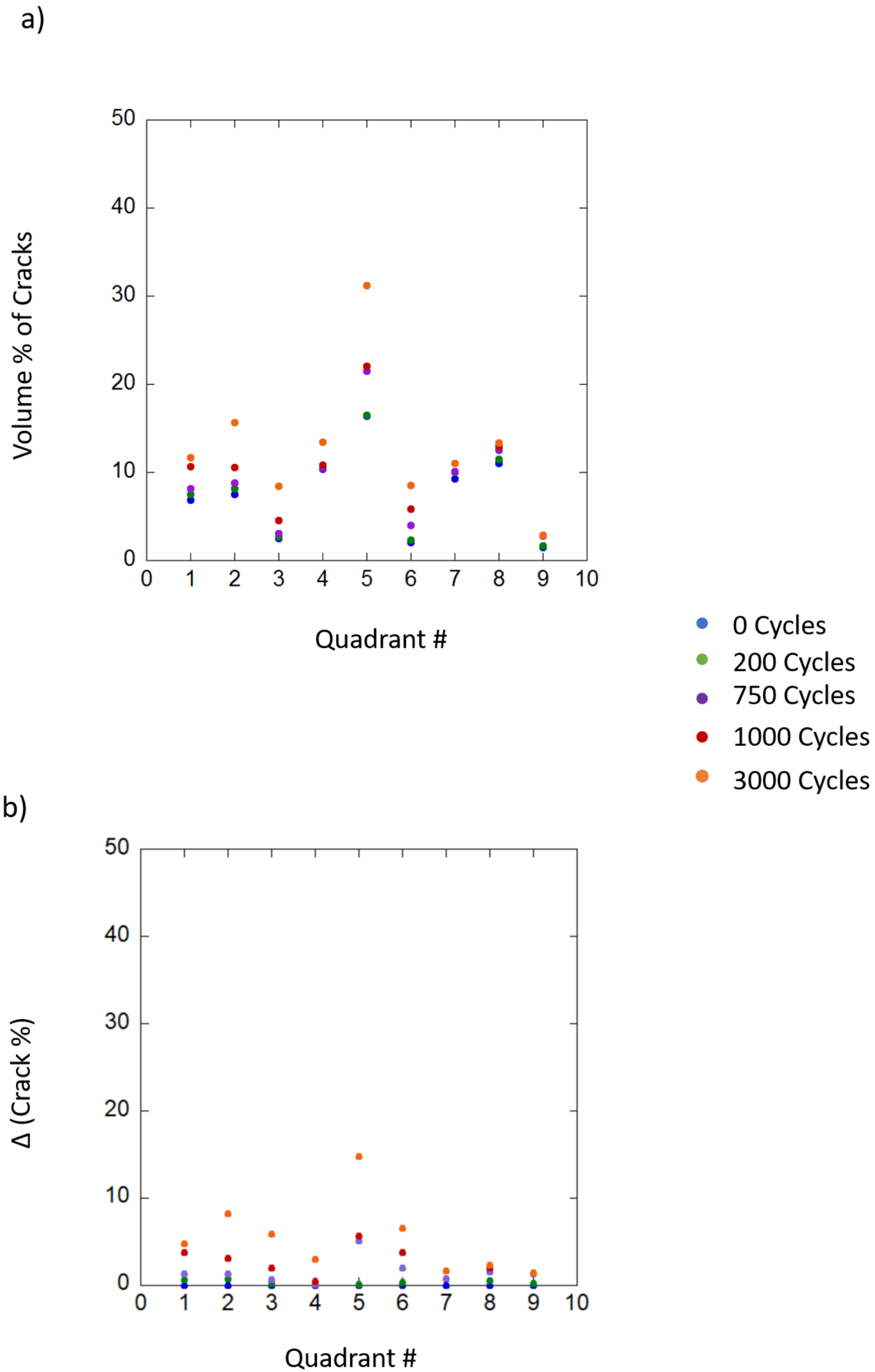


Figure 58. Increase of crack density per quadrant, a) Actual crack % for each cycle/step, b) Increase in crack % with respect to 0 cycles.

- Decrease in Effective Young's Modulus as a function of crack density

The decrease in effective Young's modulus was calculated using the MacKenzie method (Mackenzie 1950, Wachtman Jr 1969) and the O'Connell and Budiansky method (O'Connell and Budiansky 1974) described earlier. It was observed that most of the thermal-induced damage on the sample was seen on region 5 of the solder (center portion of the 5 mm x 5 mm solder area) and hence the greatest decrease of Young's modulus was also observed in this region. As to Young's modulus, the same trend was followed as in Test 1 where the loss of stiffness was localized at the center of the solder area as a result of the increase in cracks in these regions. Fig. 59(a-b) shows the calculated decrease in Young's modulus as a function of microcrack formation.

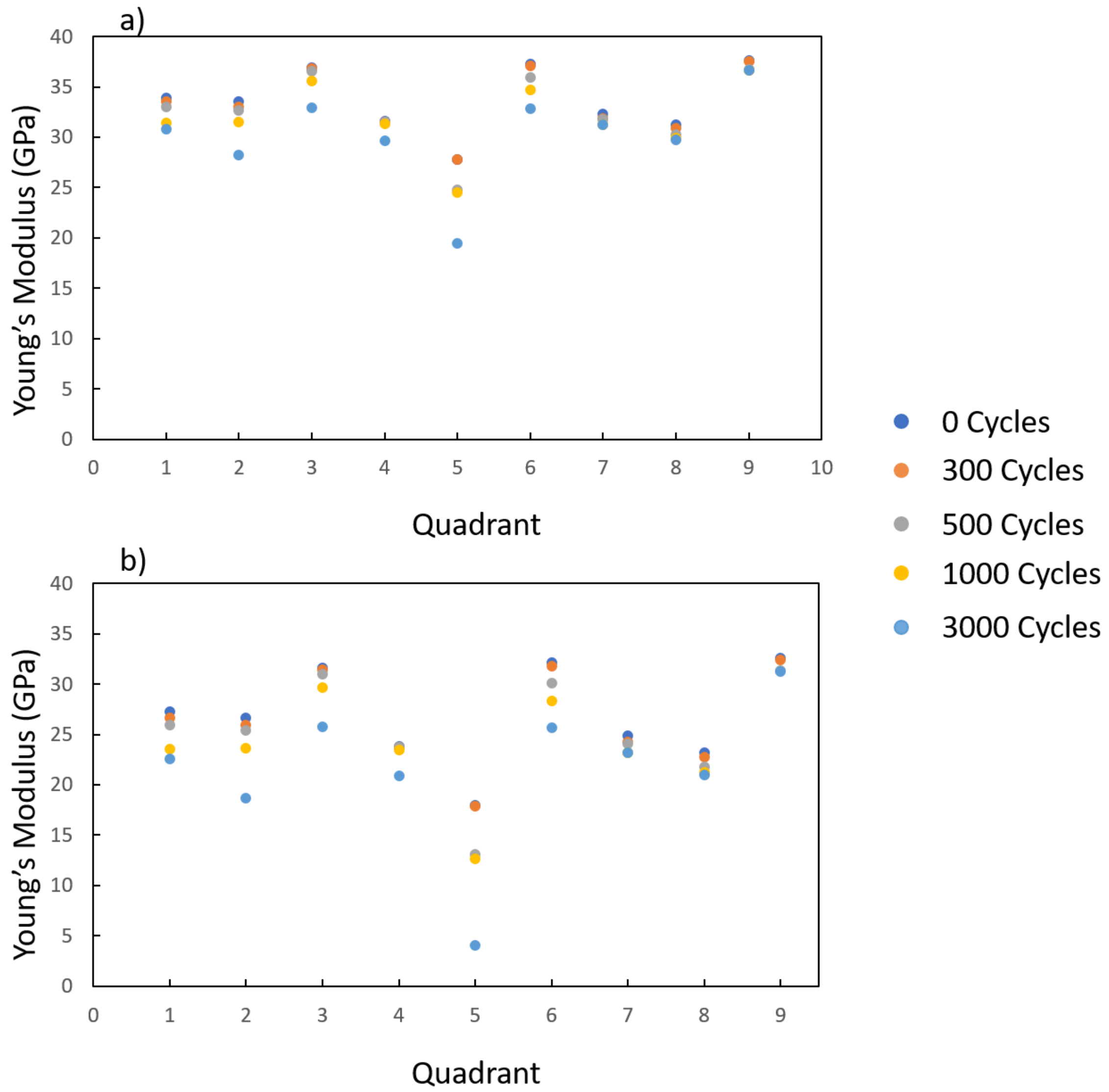


Figure 59. Decrease in Young's modulus according to a) Wachtman and MacKenzie relation b) O'Connell and Budiansky relation. A clear effect of thermal cycling is observed on the mechanical properties of nano-Ag solder, where crack formation results in a decrease of Young's modulus.

4.4.4..3.Test 3- ΔT=155°C

A third thermal cycling test was conducted at lower temperature. The sample was cycled from 20°C to a maximum temperature of 175°C. The initial microstructure of the sample is shown in Fig. 60.

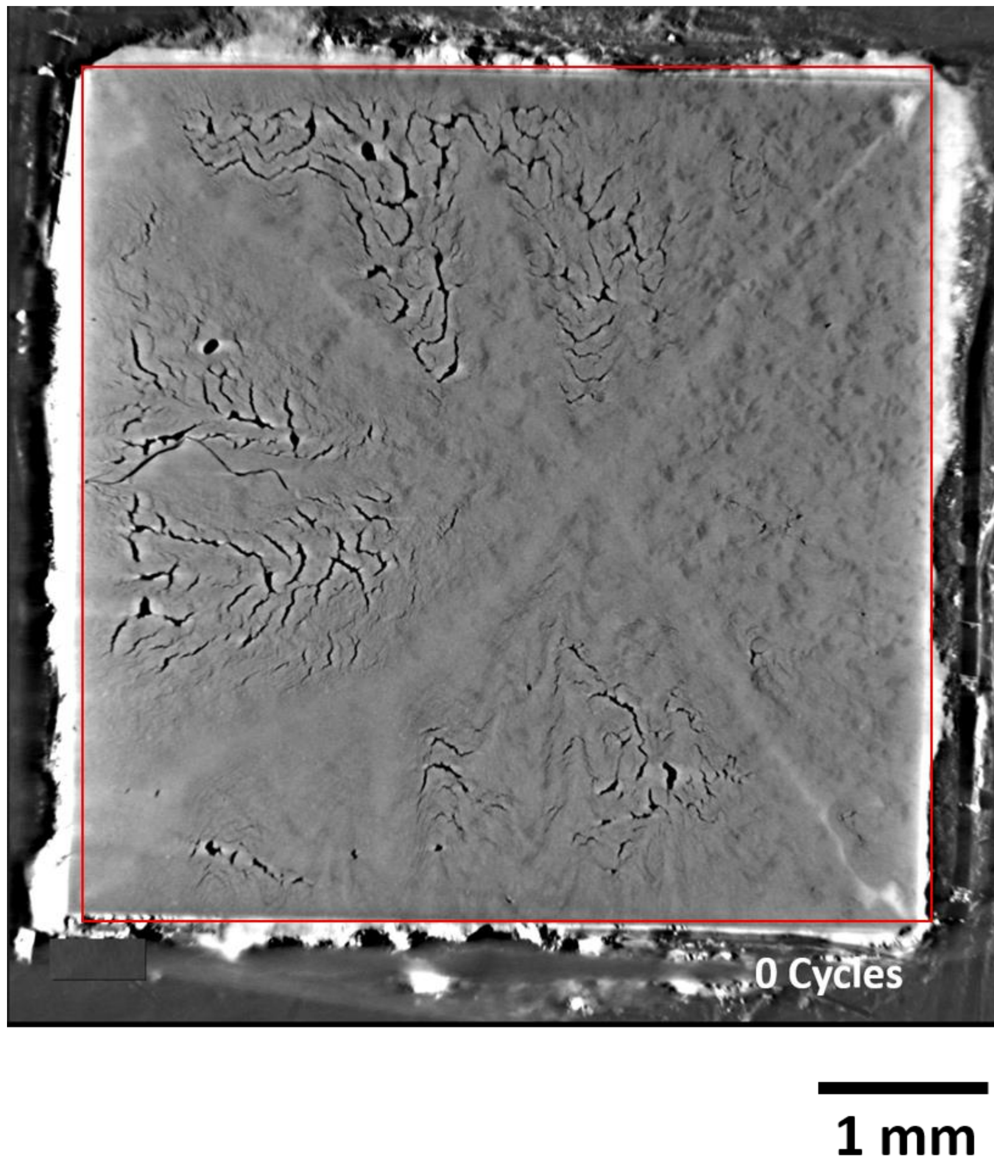


Figure 60. X-Ray images showing the initial microstructure of Sample 2, with an initial pore volume fraction of 3.5%.

As seen in previous samples, some initial porosity was observed in the microstructure of the sample. The initial pore volume for Sample 3 was 3.5%.

Thermal cycling of the sample revealed the effect of peak temperature on the solder degradation. The rate of crack formation went significantly down, with microcracks initiating only after 3000 thermal cycles. Fig. 61(a-c) shows the evolution of damage in the nano-Ag solder at 0, 1500 and 3000 thermal cycles.

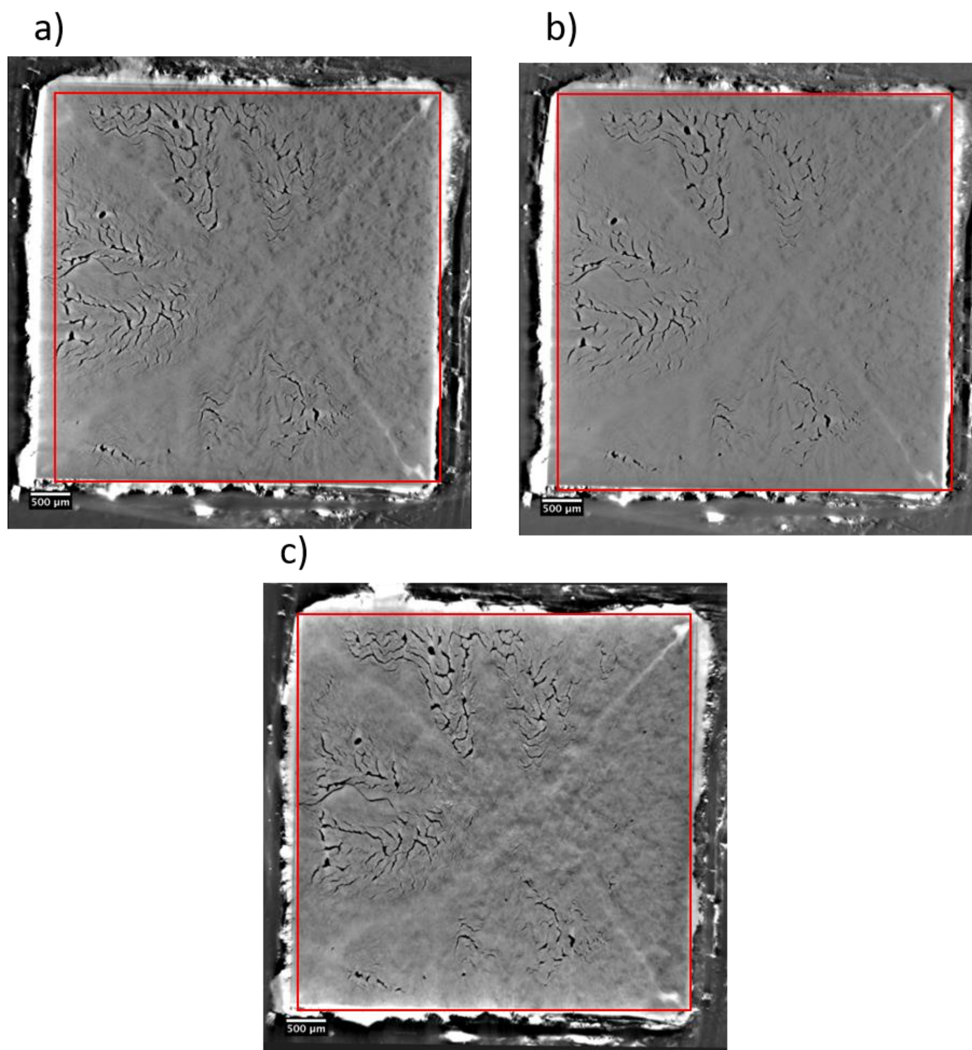


Figure 61. Microstructural damage evolution of nano-Ag solder during thermal cycling from 20°C to a peak temperature of 250°C, a) 0 Cycles, b)1500 Cycles, c) 3000 Cycles.

- Solder Delamination

Due to the low peak temperature to which Sample 3 was subjected, minimal crack formation was seen. Unlike samples 1 and 2, Sample 3 did not show any delamination even after 3,000 thermal cycles. Fig. 62 shows a comparison in crack density within region 5 of each sample (since it's this region where delamination on the solder was observed). Here it can be observed that, delamination became a serious issue once the crack density increased by 30 percent.

No crack formation on the Cu layer of the DBC substrate was observed for Sample 3, this could be attributed to the lower temperature of the test.

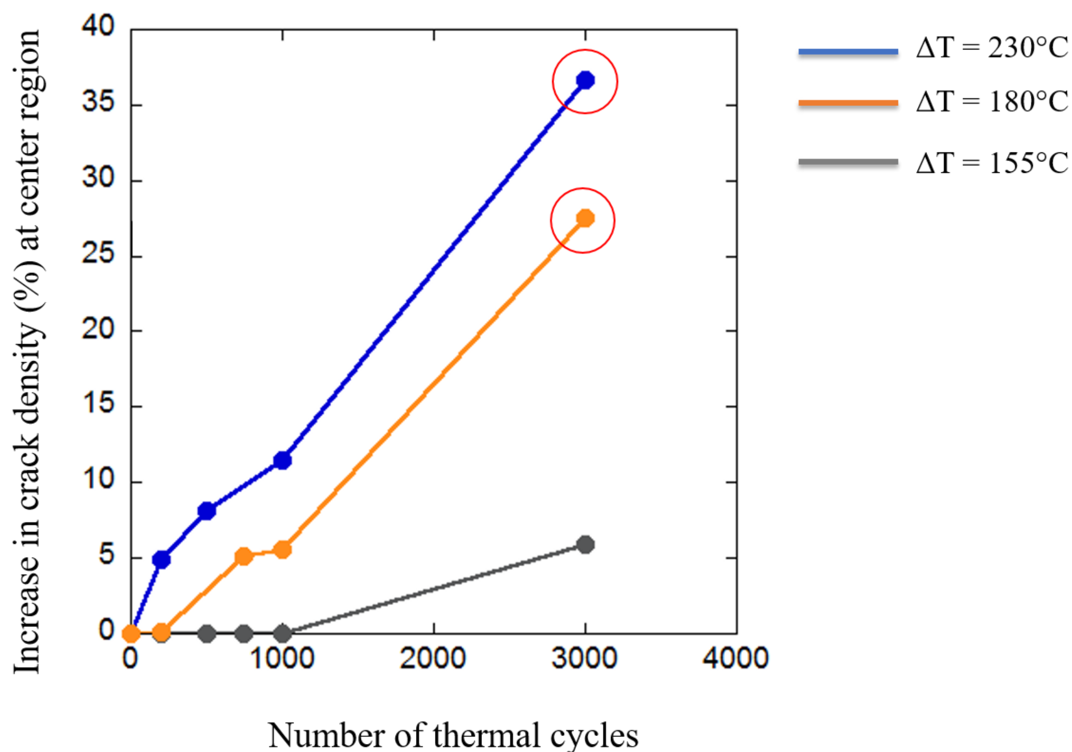


Figure 62. Analysis of increase of crack density as a function of number of thermal cycles for Sample 1 (ΔT=230°C), Sample 2 (ΔT=180°C) and Sample 3 (ΔT=155°C). The red circle on the plot indicates delamination occurring at the solder-Si interface.

- Quantification of Damage

Cracks in 3D X-Ray scans were segmented using Avizo® following the segmentation procedure described previously, an overlay of the segmented cracks is shown in Fig.63.

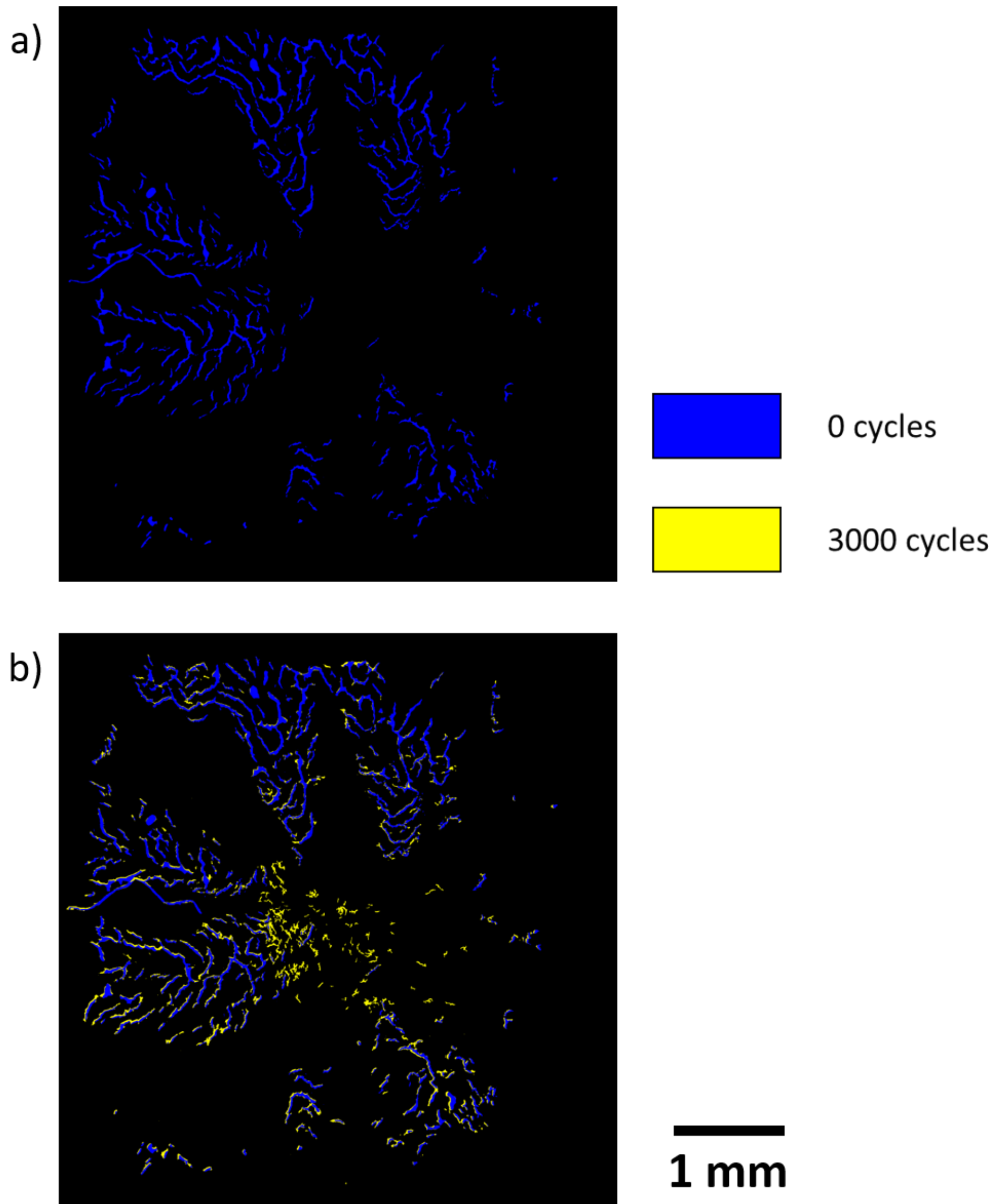


Figure 63. Cracks in the solder are segmented and color coded from 0-3000 cycles. a) 0 Cycles, b) Overlay of 0-3000 Cycles.

For analysis of crack formation in different regions of the solder, the scans were divided into 9 segments as shown in Fig. 64. The volume fraction of cracks for each individual segment was obtained and used for the calculation of the decrease in Young's modulus and is shown in Fig. 65(a-b).

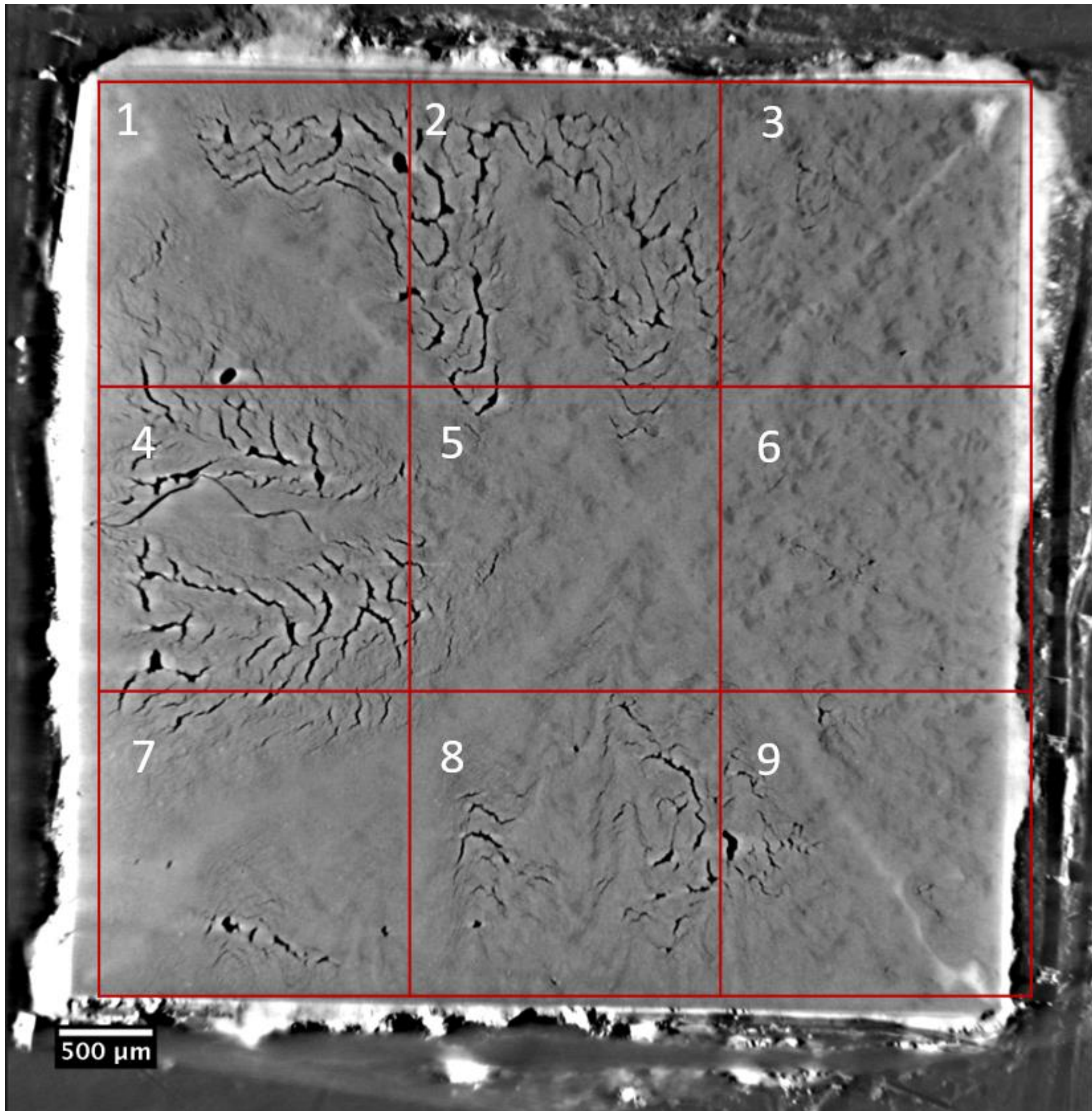


Figure 64. Solder area divided into 9 segments for analysis of crack density per region.

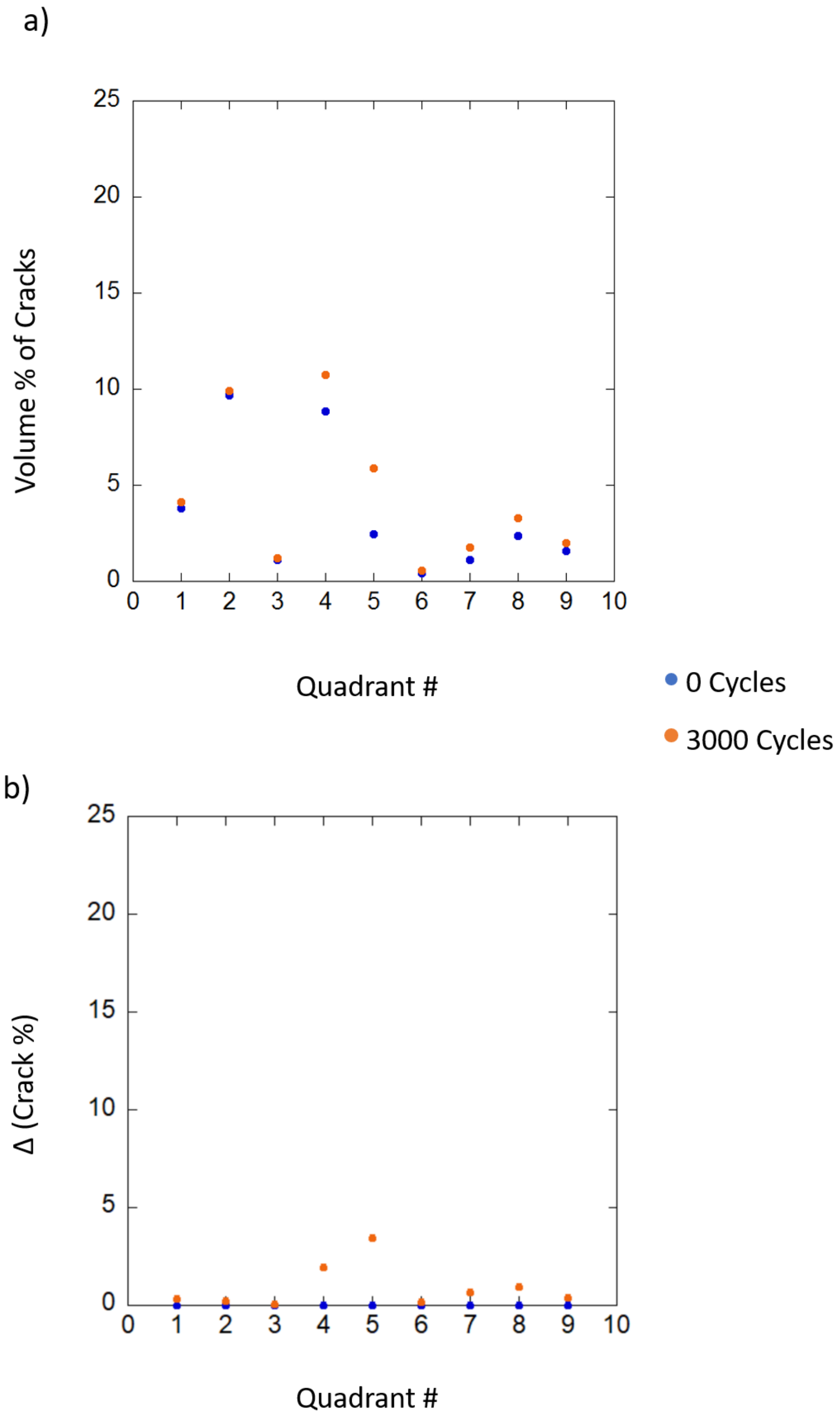


Figure 65. Increase of crack density per quadrant, a) Actual crack % for each cycle/step, b) Increase in crack % with respect to 0 cycles.

- Decrease in Effective Young's Modulus as a function of crack density

The effective Young's modulus for each segment of the solder was calculated as a function of crack density. In the case of sample 3, the decrease in stiffness of the solder was not as severe as in Samples 1 and 2. Since less crack formation is observed at lower ΔT, the change in effective Young's modulus would also be less. Fig. 66(a-b) shows the individual Young's modulus for the 9 segments into which the sample was divided.

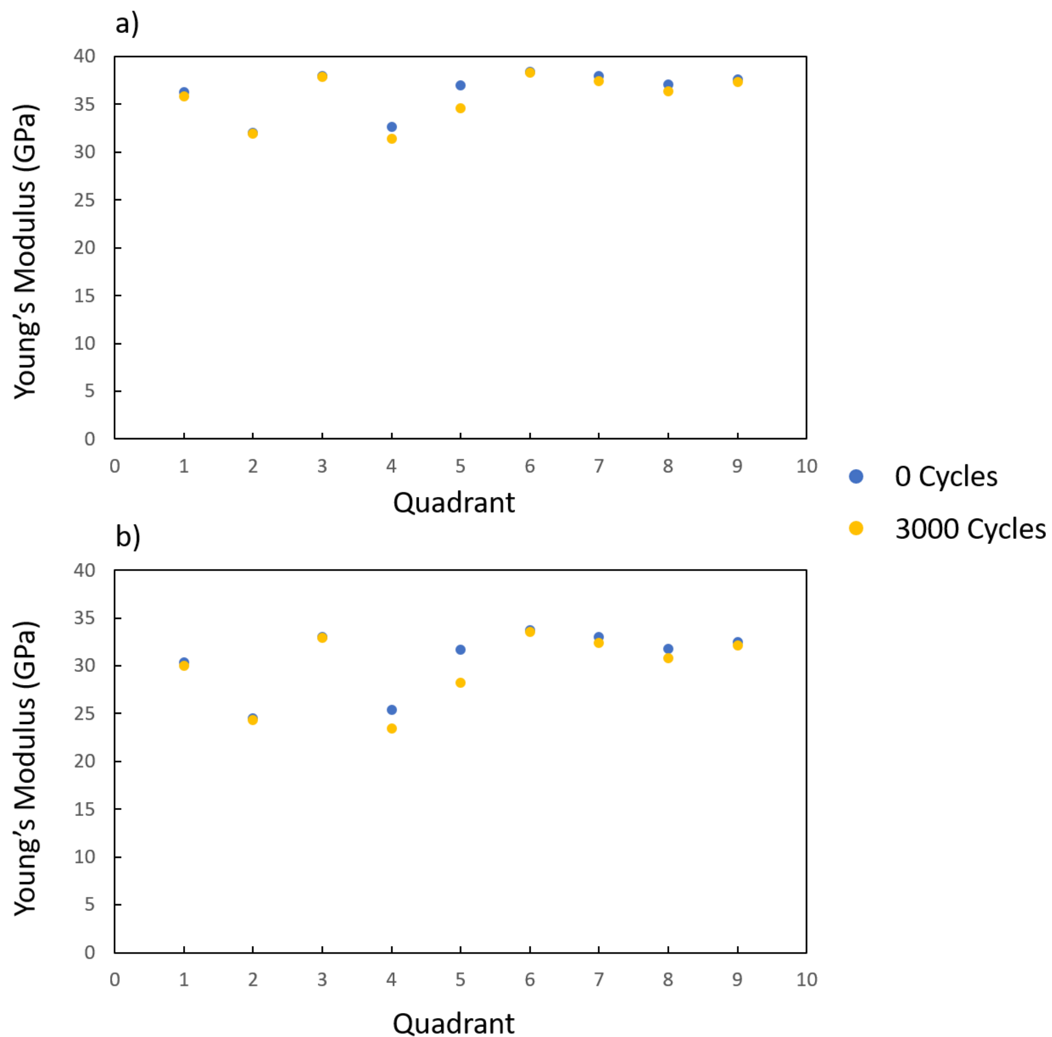


Figure 66. Decrease in Young's modulus according to a) Wachtman and MacKenzie relation b) O'Connell and Budiansky relation.

4.4.5. Thermal Cycling Warpage and Solder Constraint

The damage in the solder that seemed to be concentrated at the center region, could be a result of a combination of warpage due to CTE mismatch and solder constraint. Table IV shows the CTE values of the different layers of the solder joint.

Table IV. Coefficient of Thermal Expansion for microconstituents of the solder joint.

	Cu	**AlN**	**Nano-Ag**	**Si**
CTE (/°C)	17.7×10^{-6}	4.6×10^{-6}	19.6×10^{-6}	2.6×10^{-6}

During sintering, the individual layers in the sample stack are unconstrained and hence expand linearly. As the solder solidifies, the stack is unconstrained at high temperature and the layers are flat. As the sample cools, due to the several metallic layers below the Si die, the silicon warps inducing high strains and constraint in the nano-Ag bond. And as the solder joint is thermally cycled, the Si die oscillates between warped and flat positions, thus inducing cyclic stresses on the sample.

Additionally, the solder at the edges have less constraint with more room to expand. However, the solder at the center is constrained on all sides and thus would experience higher stresses. This would result in higher density of microcracks at the center and in worse cases result in delamination at the interface (Fig. 67(a-c)).

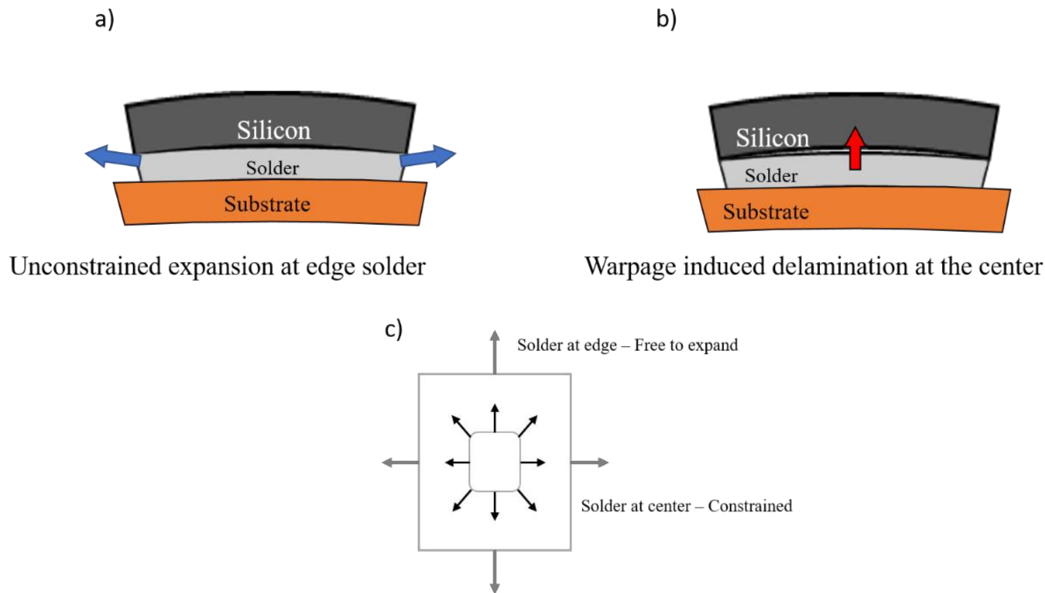


Figure 67. a) Solder at the edges is unconstraint and hence experiences less stress and hence less deformation is seen, b) Delamination induced by warpage of the Si die, c) Schematic showing the solder at the edges free to expand whereas solder at the center is constraint and hence experiences more stresses that leading to cracking of the solder.

To quantify the stress state (tensile/compressive) at any layer within the sample stack, the neutral axis of the entire sample can be identified. To obtain the neutral axis, the stack can be analyzed as a composite beam and using the transformed area method.

Transformed area method is useful for analyzing composite beams which are made of materials with different Young's moduli. In this method, the cross-section of the beam is transformed into an equivalent cross-section, where the resultant beam is composed of only one reference material. In the case of this analysis, Cu (from the DBC) was chosen as the reference material for Young's modulus comparision. To obtain the transformed structure, a ratio of the Young's modulus for each layer with respect to the base material (Cu) is calculated and the transformed stack is constructed using equation 7.

$$b = \frac{E_2}{E_1} * b_0 \quad \text{Equation 7}$$

Where,

b = transformed width of layer

$E_{1,2}$= Young's modulus

b_0= transformed width of layer

The dimensions for the original stack and the transformed stack are shown in Table V. A schematic of the transformed stack is shown in Fig. 68. The width of layers in the composite beam, are modified based on the modulus ratio. It is important to note that the height is maintained the same as original in order to maintain the strain profile in the layers. Any change in height will also affect the position of the neutral axis, thus making the method invalid.

Table V. Comparison between original stack and transformed stack.

	Cu	**Si**	**Ag**	**AlN**
E (GPa)	129	129	129	129
b (mm)	21	6.7	0.78	56.5
h (mm)	0.2	0.5	0.03	0.6
b0 (mm)	21	5	5	21

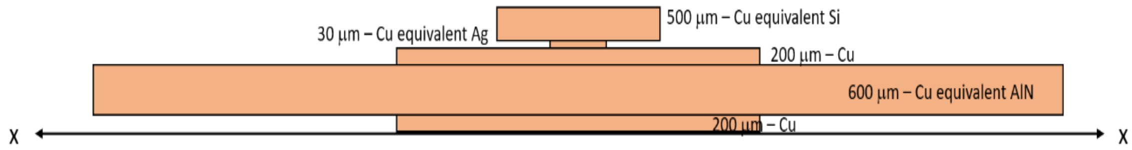


Figure 68. Transformed solder stack for analysis of composite beam using the Transformed Area Method.

After obtaining the transformed structure, the neutral axis can located based on the centroid. Equation 8 is used to calculate distance 'y' from the bottom/reference axis-xx as shown in Fig. 68.

$$y = \frac{\Sigma YA}{\Sigma A_{total}} \qquad \text{Equation 8}$$

For the sample geometry used in this study, the neutral axis was obtained to be at 0.555 mm from the reference xx axis. Neutral axis lies close to the center of the DBC. At 355 mm from the bottom Cu/AlN interface (55 mm above the centroid of AlN). With the location of neutral axis known, the stresses in the layers of the solder stack can be obtained from bending moment equations which are a function of applied ΔT and coefficient of thermal expansions.

4.4.6. Conclusions

Sintered nano-Silver bonds were fabricated and the microstructure and mechanical properties were characterized. Homogenously distributed pores were seen at the cross-section of the nano-Ag bondline. Shear testing results showed a shear strength of 15-20 MPa, and the analysis of the sample's fractography revealed that fracture occurs through

the thickness of the solder, indicating good bonding at the Si-solder and solder-DBC interfaces.

3D X-ray tomography scans revealed the presence of pores in the initial microstructure of the sample, which can be attributed to the organic binder in solder that got trapped while degassing during the sintering process. Tomography scans were also used to study and quantify crack growth at various ΔT conditions in thermal cycling.

Microcrack formation was seen to be the result of thermal cycling and it lead to localized failure (delamination) in the case of the samples where the crack density exceeding 30%.

Crack formation was seen to be localized at the center of the sample, although minor crack formation was also observed in other locations of the sample. Warpage due to CTE mismatch between the multiple layers in the solder joint, is hypothesized to be the cause of degradation at the center of the sample. Additionally, the solder at the center of the sample could experience more constraint than solder at the edges of the sample, hence causing more stresses and crack formation in the center region.

5. SUMMARY AND CONCLUSIONS.

5.1. Effect of Crystal Orientation and Microstructure on the Nucleation and Growth of Sn Hillocks by In Situ Nanoindentation

The influence of microstructure and crystallography in the formation and evolution of mechanically induced tin whisker/hillocks was investigated in vacuum using an in situ nanoindenter and EBSD. Based on the experimental results and FEM analysis, the following conclusions could be drawn:

- As-electroplated Sn samples do not have native IMC layer formation within the first 24 hrs of plating. Nanoindentation of samples in this condition results in formation of ~100 nm sized hillocks surrounding the indentation which seem to form dynamically during indentation. On the other hand, nanoindentation of samples aged at 150ºC for 3 days revealed slightly larger hillocks around the indentation, in addition to large faceted hillocks / single crystalline mounds at the edge and center of the indentations indicating the strong influence of IMC layer beneath the Sn film.
- Aging tests revealed morphological differences in Cu_6Sn_5 and Cu_3Sn IMCs and their growth exponents confirmed the different diffusion mechanisms influencing these morphologies. Cu_6Sn_5 showed growth exponent 0.4 indicating a mixed grain boundary and bulk diffusion mechanism thus resulting in a nodular morphology, while Cu_3Sn showed growth exponent of 0.48 indicating bulk diffusion resulting in a planar growth front.

- FIB-slab lift-out technique was used to fabricate slabs from the Sn plating to investigate the grain structure and crystallography. Aspect ratio analysis on both as-plated and aged samples revealed a mechanically induced recrystallized zone forming near the indentation with equiaxed grains as compared to elongated grains away from the indentation.
- The extent of stress field around the indentation and how it decreases with distance was elucidated by analyzing the number density of hillocks. The smaller hillocks were seen to form up to 15 μm from the indentation with the highest density at the indentation edge.
- Crystallographic analysis using EBSD revealed the presence of high angle grain boundaries around the large faceted hillocks. These high angle grain boundaries serve as fast diffusion pathways for Sn atoms to migrate to the surface forming hillocks and thus relieving the compressive stresses.
- An FEM model was developed to simulate the nanoindentation test using a 2D axisymmetric conical indenter and it was seen that largest plastic deformation is close to the indenter tip, where the large faceted hillocks were seen and the stress field decreases gradually away from the indenter which compared well with experimental findings.

5.2. X-Ray Microtomography of Thermal Cycling of Silver-based Thermal Interface Materials

- Sintered nano-Silver bonds were fabricated and the microstructure and mechanical properties were characterized. Homogenously distributed pores were seen at the cross-section of the nano-Ag bondline.
- Shear testing results showed a shear strength of 15-20 MPa, and the analysis of the sample's fractography revealed that fracture occurs through the thickness of the solder, indicating good bonding at the Si-solder and solder-DBC interfaces.
- 3D X-ray tomography scans revealed the presence of pores in the initial microstructure of the sample, which can be attributed to the organic binder in solder that got trapped while degassing during the sintering process. Tomography scans were also used to study and quantify crack growth at various ΔT conditions in thermal cycling.
- Microcrack formation was seen to be the result of thermal cycling and it lead to localized failure (delamination) in the case of the samples where the crack density exceeded 30%.
- Crack formation was seen to be localized at the center of the sample, although minor crack formation was also observed in other locations of the sample. Warpage due to CTE mismatch between the multiple layers in the solder joint, is hypothesized to be the cause of degradation at the center of the sample.

- Additionally, solder at the center of the sample could experience more constraint than solder at the edges of the sample, hence causing more stresses and crack formation in the center region.

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