Capable Copper Electrodeposition Process for Integrated Circuit - Substrate Packaging Manufacturing

by

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ABSTRACT

This work demonstrates a capable reverse pulse deposition methodology to influence gap fill behavior inside microvia along with a uniform deposit in the fine line patterned regions for substrate packaging applications. Interconnect circuitry in IC substrate packages comprises of stacked microvia that varies in depth from 20µm to 100µm with an aspect ratio of 0.5 to 1.5 and fine line patterns defined by photolithography. Photolithography defined pattern regions incorporate a wide variety of feature sizes including large circular pad structures with diameter of 20µm - 200µm, fine traces with varying widths of 3µm - 30µm and additional planar regions to define a IC substrate package. Electrodeposition of copper is performed to establish the desired circuit. Electrodeposition of copper in IC substrate applications holds certain unique challenges in that they require a low cost manufacturing process that enables a void-free gap fill inside the microvia along with uniform deposition of copper on exposed patterned regions. Deposition time scales to establish the desired metal thickness for such packages could range from several minutes to few hours. This work showcases a reverse pulse electrodeposition methodology that achieves void-free gap fill inside the microvia and uniform plating in FLS (Fine Lines and Spaces) regions with significantly higher deposition rates than traditional approaches. In order to achieve this capability, systematic experimental and simulation studies were performed. A strong correlation of independent parameters that govern the electrodeposition process such as bath temperature, reverse pulse plating parameters and the ratio of electrolyte concentrations is shown to the deposition kinetics and deposition uniformity in fine patterned regions and

gap fill rate inside the microvia. Additionally, insight into the physics of via fill process is presented with secondary and tertiary current simulation efforts. Such efforts lead to show “smart” control of deposition rate at the top and bottom of via to avoid void formation. Finally, a parametric effect on grain size and the ensuing copper metallurgical characteristics of bulk copper is also shown to enable high reliability substrate packages for the IC packaging industry.

DEDICATION

The love and constant support of my daughter, my wife, my parents, my brother and sister have always been the motivator for me to succeed in life. I'm grateful for all their sacrifices. The love and support of my university friends at Ames, IA have been a constant source of inspiration and support through some of my toughest of phases of life.

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BACKGROUND AND LAYOUT OF THIS REPORT

Section 1 Motivation for this work

Manufacturing challenges are becoming the prominent decision making factors on choosing the right technologies and where high volume manufacturing factories are built. Today majority of corporations have moved their factories to low cost geographies to ensure cost competitive products[1]. However, the goals of attaining low cost feasible products can be easily accomplished through advances in technology rather than taking advantage of cheaper human labor. This alludes us to the question of what should we do differently across the board to attain cost effectiveness and improved efficiency? The answer is simple and common sense! Reduce the cost of every single factors involved in product manufacturing. For example, reduce workforce through automation, reduce materials cost through innovation, reduce process cost through understanding of all involved parameters and their interactions to make process more predictable, eliminate waste, improve throughput, etc[1]. Through this work, we identify novel and innovative technical solutions to an important process in semiconductor industry. The area of interest is electrodeposition process which is being used in wide variety of products such as silicon processing, substrate manufacturing, packaging, board manufacturing, SMT (Surface Mount Technology) process, and many more other applications.

Section 2 State of the art and problem statement

IBM introduced what is commonly now known as the "damascene process" in the late 1990s to form copper IC interconnects [2]. Later, a variation of the damascene process

known as dual damascene process was developed for cost effectiveness. Different flavors of damascene processes exist in IC manufacturing today based on feature types and application[3]. In all cases, a line or via pattern is defined by photolithography or through LASER (Light Amplification by Stimulated Emission of Radiation) drill into a dielectric film. Copper seed layer is then deposited onto the dielectric film. This seed layer provides the conductivity across the surface necessary for the electrodeposition process, as well as a surface upon which nucleation of the deposited film can begin. Copper is then electrodeposited to form the desired circuitry by filling the seeded recesses in the dielectric. High density IC packages have fine patterned regions in the scale of 3µm to features as large as 77µm along with many large plane area regions. They are supported with underlying microvia usually with via opening size 20µm to 100µm and an aspect ratio of 0.5 to 1.5. Enabling void-free gap fill and uniform FLS (Fine Lines and Spaces) deposition in a single plating step is beneficial and key for these applications to ensure product integrity and performance. State of the art systems utilize organic polymer additives to enable differential via fill capability. With such methods, in order to achieve uniform copper thickness and void-free fill, it is often required to slow the deposition process significantly and/or live with variations in feature to plane thicknesses across the entire electrodeposited surface. Deposition time scales range on the order of several minutes to few hours. Such limitations cripple process manufacturability. Furthermore utilization of polymer additives as electrolyte components generates undesired byproduct and limits the life of the bath and poses significant risks to process viability. Concerted new approaches are needed to enable low cost electroplating process for substrate

packages. A much straightforward approach would be to enable bottom-up fill and uniform deposition in the absence of additive species. In this study we provide one such logical approach utilizing reverse pulse plating methodology. However, various challenges exist in making this process viable. Some of the key challenges include achieving void-free fill, complete fill by eliminating any recess, uniform deposition of copper on the surface and features, optimized process time to improve throughput, etc[3].

Section 3 Layout of chapters in this report

In order to achieve faster uniform fill and realize higher throughput additional insight into the physics of via fill is required. Furthermore, once a process is finalized, repeatability of such processes and extrapolation to high volume manufacturing are desired. Such capability is only possible through establishing key learnings on a fundamental scale (molecular level interactions) and developing a predictive capability to modulate deposition parameters such as waveform, additive concentration etc. for desired gap fill. This report provides various experimental and simulation data focused primarily on identifying a capable electrodeposition process for substrate via fill and uniformity. Chapter I introduces integrated circuit, and packaging in integrated circuit. The critical need to scale packaging features in concert with IC transistor architecture scaling and the demand for developing advanced packaging technology is discussed further. Advantages of copper metal and the ability to achieve that through electrodeposition process is introduced. In chapter II we discuss the physics of electrodeposition and identify the key parameters that govern the deposition process. Chapter III provides a literature survey on

existing methodologies of via fill and various challenges associated with them. The criticality of TP (Throwing power) ratio for void-free bottom-up fill is discussed. In Chapter IV we introduce reverse pulse methodology and discuss how reverse pulse deposition addresses some of the key challenges discussed thus far along with a detailed literature survey on existing state of the art. Chapter V reviews the design of test coupon and the makeup of IC substrate with various stacked via geometry such as Via0, Via1 and Via5. The uniqueness of the via size, shape and gap fill challenges for each of these via geometry is briefly discussed. This chapter also reviews the experimental set up and make up of reverse pulse waveform. In chapter VI we study the application of reverse pulse methodology for Via0 and Via1 geometry and showcase a capable process for void-free gap fill for these feature geometries. In chapter VII, we provide a simulation capability for reverse pulse methodology and outline the mechanism and the critical throwing power needed for void-free fill with Via0 and Via1 geometry utilizing diffusion transport effects. The distribution of an electroplated deposit depends upon which transport phenomenon controls the plating rate. We need to consider the overall ohmic and mass transfer effects present inside the system to determine which transport mechanism dominates the distribution of copper inside the via region. Ohmic resistance of the metal film leads to variations of potentials in the film, and solution resistance leads to variations of potential in the plating solution. Mass-transfer effects lead to variations in concentration of cupric ion and additive species across the metal surface. Generally, non-uniform reaction rates are caused by either inadequate mixing, so that reactant concentrations are not uniform (convection effect), or by spatial variations in the

electrical-potential difference across the electrode/electrolyte interface or due to concentration gradient (diffusion). Due to the large concentration of acid present in the electrolyte, migration effects are negligible. In chapter VIII, microstructure of the electrodeposited copper is characterized with various analytical techniques such as SEM, EBSD, XRD and AFM to analyze grain size, crystal orientation / texture, and intrinsic stress build up with different experimental conditions such as bath temperature, electrolyte composition and Anneal. In chapter IX, challenges of void-free fill with Via5 geometry and the need to identify additional knobs to prevent void entrapment for this geometry is discussed. A comprehensive design of experiments with optimization of six different additive ratio's with different bath temperature and reverse pulse waveform is studied to show TP improvement and the generic TP improvement trend with increased suppression. In chapter X, similar set of studies were performed for Via1 geometry to show how increased suppression with reverse pulse methodology yields significantly better fill. Chapter XI attempts a 2D simulation model to incorporate the effect of additives for gap fill with Via5 and Via1 geometry and corroborates the finding with experimental data. The model also predicts to incorporate additional leveling agents to improve the throwing power further. Chapter XII showcases a capable reverse pulse methodology for all via geometries with the newly identified reverse pulse methodology at optimized additive concentrations. Improvements with uniformity for patterned features across each layer of substrate with different via geometry is explored. Microstructure comparison of the new bath composition is also summarized with some of the data collected thus far to showcase high reliable substrate packages.

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CHAPTER I

INTRODUCTION

Integrated circuits play a vital role in our day to day life. Applications for integrated circuits include anything from complex cloud servers or high speed computers that require fast computing speeds to a simple wearable technology like fitness watch or a tablet computer that requires low cost build up elements and smart architecture to enable a lean footprint. The invention of transistor revolutionized the history of mankind in the past century. Ultra-fast computing speeds, high memory storage capabilities, versatile network and data connectivity are made possible today due to the ever shrinking cost and size of transistor nodes[1, 2]. The drive to lowered cost has been primarily enabled through miniaturization or "scaling down" of the transistor architectures and the subsequent explosion of I/O signals (input/output signals) in a very small footprint.

Section 1.0 Integrated Circuits and Interconnects

Market analysis and various technical studies [2-5] argue that the success of the industry over the past several years has been primarily due to its frequent cadence in transistor scaling utilizing Moore's Law. As shown in Figure 1.1[5], while a 100nm transistor node technology used to drive ~500 I/O per cm^2 a few years ago, we are in the 14-7nm node generation today that drives >20000 I/O per cm^2.

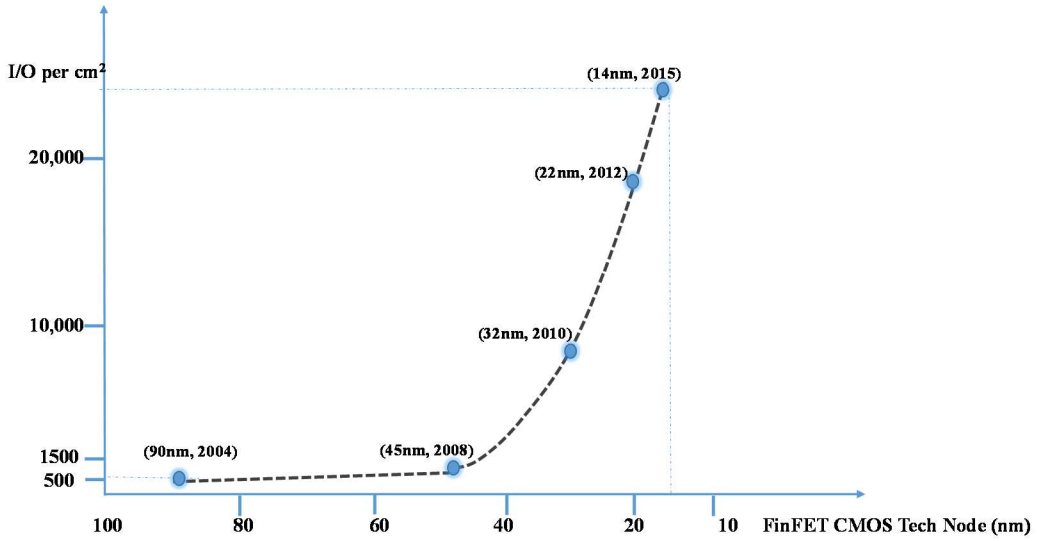

Figure 1.1: Plot of transistor node scaling with I/O per unit area

[Figure adapted from reference[5]]

An "interconnect" in an integrated circuit is a stack up of planes that integrates the transistor with the additional components necessary for system operation in an external circuit. Usually, interconnect features closer to the transistor are extremely small (consistent with the size of transistor node technology) primarily made up of nanometer size via's and traces. They eventually fan out and connect much larger micro and macro power planes as they approach closer to components that connect to external circuits. Figure 1.2 shows a stack up of copper interconnects. Typically, in an industrial scale, wafer level processing is utilized to build nanoscale features and board level processing is utilized to build mesoscale to microscale power planes.

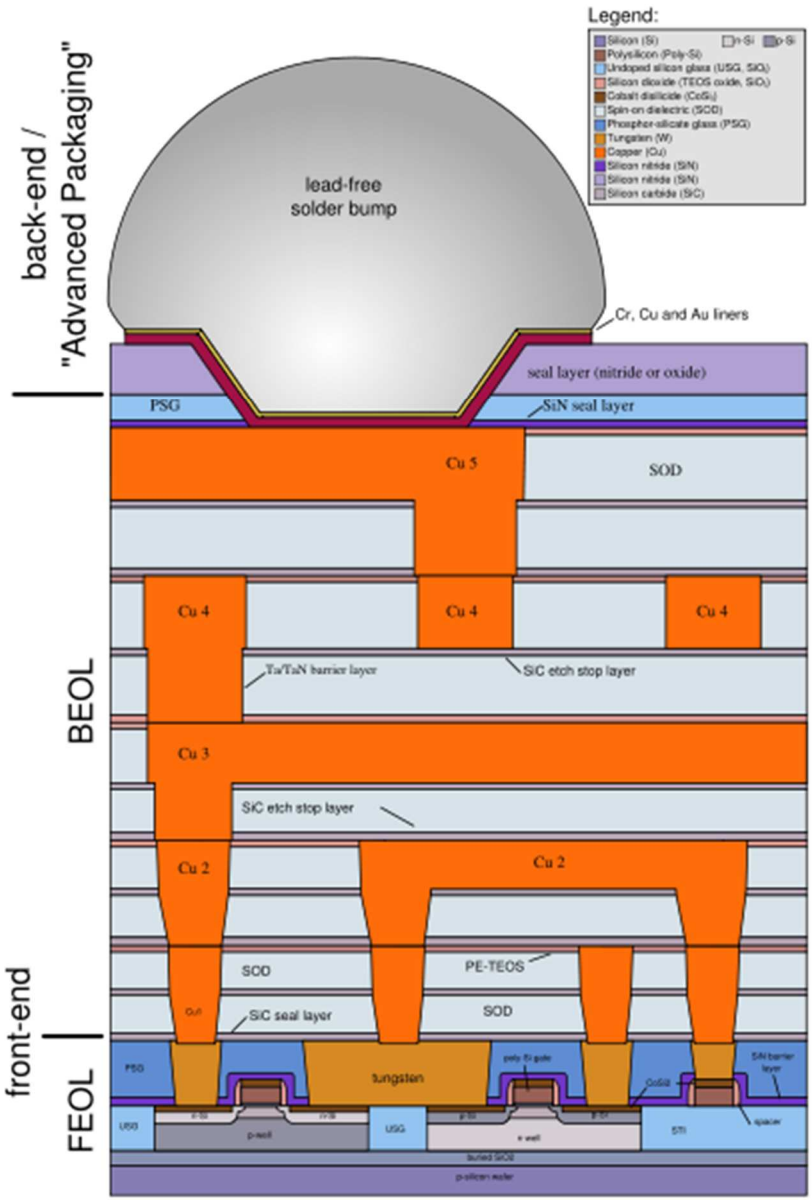

Figure 1.2: Stack up of copper interconnects

[Figure adapted from Reference[6]]

IC packaging technology has not revolutionized over the past decade with the design rules remaining mostly stagnant. Figure 1.3[2] shows the chronology of feature size transition for the transistor nodes (black line) and package assemblies (red line). It is notable here that the packaging features size have remained steady over the past several

decades while the transistor node features sizes have reduced on the order of ~1000x. With the recent transistor node technology suffering from serious technical and yield challenges due to the complexity in manufacturing of the shrinking node sizes, it is argued that any further growth and improvement in I/O density & bump pitch scaling that requires high density interconnects needs to happen on the packaging side of business. Some key packaging assembly concepts that are being considered today include high density organic interposers and multichip package assemblies with high density interconnects. These advanced packaging assembly methods not only need to enable high density interconnects but need to facilitate them at lowered cost at the same order as traditional packages.

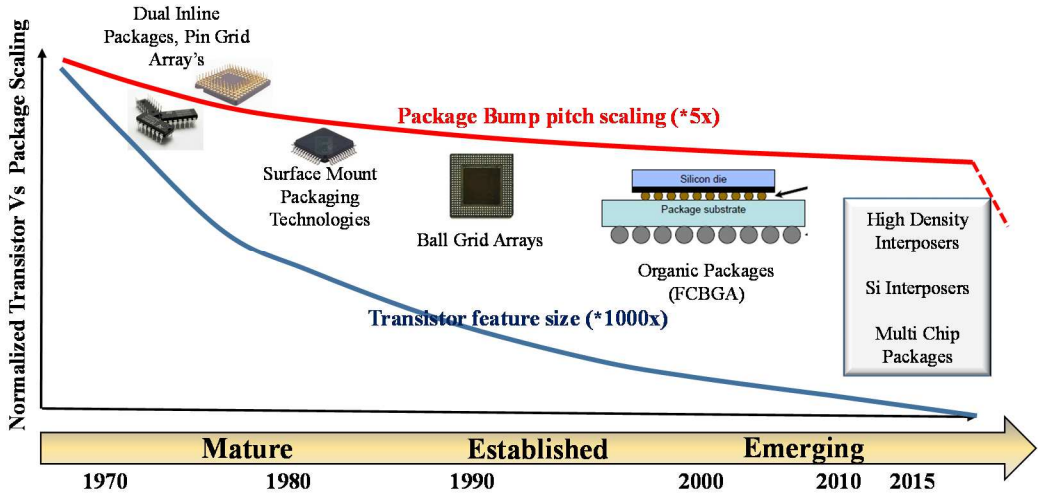

Figure 1.3: Chronological plot of transistor node and PCB feature scale

[Figure adapted from Reference[2]]

Section 1.1 IC assembly and packaging process

In simple terms, IC packages connect the IC transistors and the ensuing build up architecture to the outside word. IC packages ensure mechanical protection, provide thermal management and enable reliable and efficient signal and power delivery. Key requirements of microelectronic IC packages include signal integrity (minimizing RC delay), reduced form factor, scaling, mechanical and environmental support, thermal management against heat dissipation in the circuit, etc. Packaging needs vary widely for different application segments. Based on the market segments they serve and the complexity in the manufacturing of the package, packaging for various IC applications can be broadly classified to four main categories. Such applications include, integrated systems for mobile markets (1), flexible and new revolutionary markets (2), complex / high power market segments like gaming computers (3) very highly complex to top notch processing needs of servers and supercomputers (4). Based on the needs of these market segments, some key objectives for packaging can be quickly identified as low packaging height (Z height) to establish a lean foot print, reduced warpage to enable compatibility with any chip material they are attached, increased I/O density and efficient power delivery.

Historically, there are two primary ways to connect the silicon die to the package: Wire bond (Figure 1.4) and Flip Chip (Figure 1.5). In a wire bond package (conventional package) the back of the processed die is attached to the package and electrical connection is made through wires connecting the die to the package.

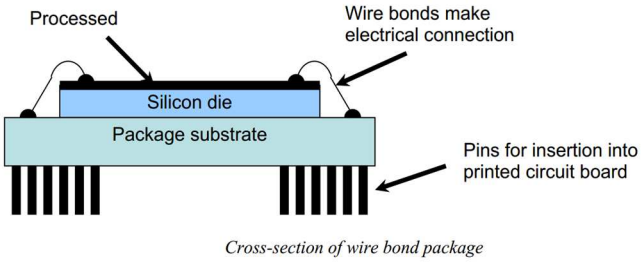

Figure 1.4: Wire bond packaging process

[Figure adapted from Reference[9]]

Wire bonding is cost-effective, but wires can be attached only on the periphery, limiting the number of interconnects possible. On the other hand, with Flip-chip– Bumps (packages utilized today) the chip is flipped over and the bumps are soldered to the package forming mechanical and electrical connections.

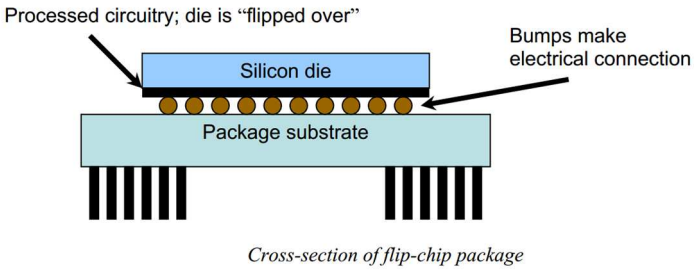

Figure 1.5: Flip Chip packaging process

[Figure adapted from Reference[9]]

Flip chips provide better performance at high frequency plus the bumps can be located anywhere on the surface of the die rather than just on the periphery. There are 3 primary ways to attach packages to printed circuit boards. Pin Grid Array, (PGA), Ball Grid Array

(BGA), Land Grid Array (LGA). The discussion of such package types is beyond the scope of this work.

Section 1.2 Substrates in packaging

There are two distinct interconnect segments in Flip chip packaging process show in Figure 1.6 below.

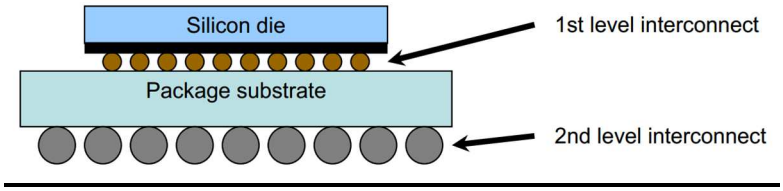

Figure 1.6: Interconnects in Flip Chip packaging process

[Figure adapted from Reference[9]]

In a 1st level interconnect, the interconnect is made between the die and the package. In a 2nd level interconnect, the interconnect is made between the package and the board. It also includes the interconnect between the package and capacitors (not shown) that are added to filter out spikes in electrical signals. A substrate is the intermediate that enables both 1st and 2nd level interconnect.

Substrate is the base material supporting the die and surrounding parts in IC packages shown in Figure 1.7. It fulfills several important purposes including, (1) It provides a mechanically robust package for the die (2) It connects the very small electrical interconnects on the die to the larger connections of the motherboard, (3) It can provide important electrical benefits to the die, (4) It can assist in thermal dissipation of

the heat from the die. Together with other items (underfill, integrated heat spreader, etc.), the substrate comprises the total electronic package that connects the die to the rest of the electronic system and the motherboard [7, 10, 11]. Substrate designs and architectures are customized for each product following industry standards (JEDEC - Joint Electron Device Engineering Council) [12]. The layout and design of the substrate must be done in conjunction with the die architecture to ensure that the package works. Formation of a substrate is normally accomplished through either subtractive or additive or semi additive processing. A substrate is made up of multiple layers of copper conductors, built up on polymeric dielectric layers which are laminated onto a fiberglass/epoxy matrix core utilizing semi additive processing methods.

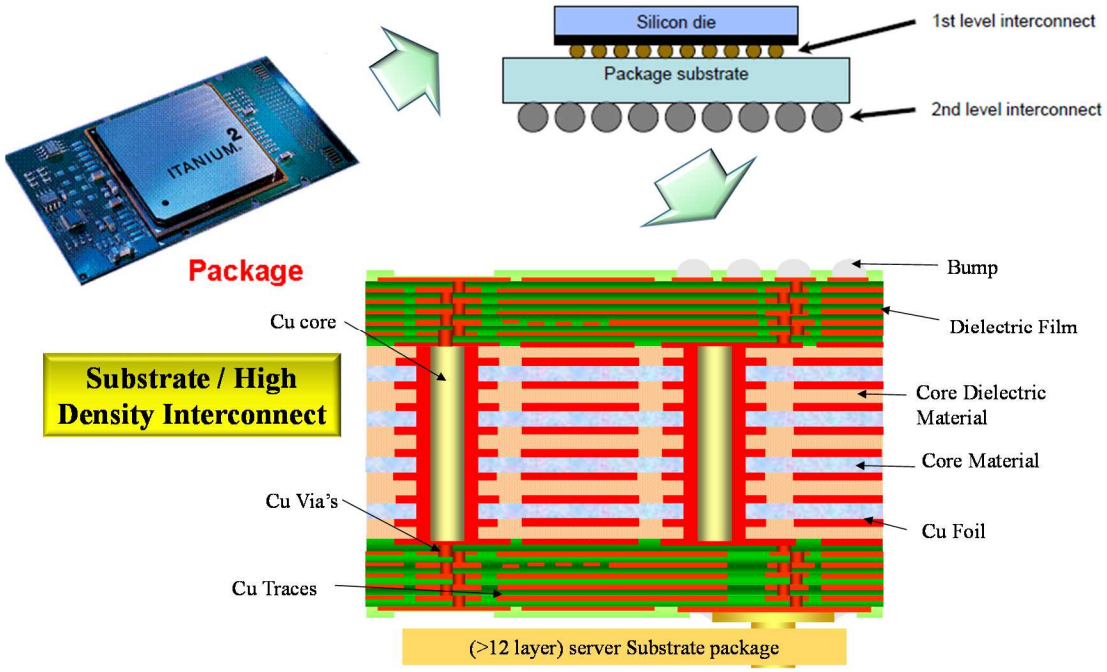

Figure 1.7: Architecture of an IC packaging substrate

[Figure adapted from Reference[7, 10, 11]]

Section 1.3 Electrodeposition in IC substrate Packages

IC substrate packages are usually manufactured utilizing a semi additive process that includes alternating stacks of dielectric and copper routing metal layers as shown in Figure 1.7 above. Layer to layer connection is made possible through via stacks. This alternating stack termed build up layer is formed as follows. A dielectric film is laminated on top of an underlying core or bottom layer. LASER drill is done to expose the via region and the underlying copper. A thin metal seed covering a dielectric surface is then established followed by generation of a circuit pattern utilizing photolithography process. Copper is next deposited, usually by electrodeposition, to fill the via and enable patterned copper deposit on the seed surface defined by the photoresist pattern. Finally, the photoresist and seed layer are removed leaving only the metal circuit pattern with via pads and traces. These process steps are repeated to enable a multilayer stack. In the make-up / manufacturing of a substrate, copper electrodeposition process plays a key role in establishing the substrate. The electrical connectivity and power delivery is done through via's and traces that are filled with copper metal[7, 10, 11]. Figure 1.8a shows a cartoon of an photoresist patterned layer with open via's and traces prior to electrodeposition and Figure 1.8b and 1.9 shows the same substrate layout after electrodeposition is accomplished inside the via and trace regions (identified as filled region in Figure 1.9 above).

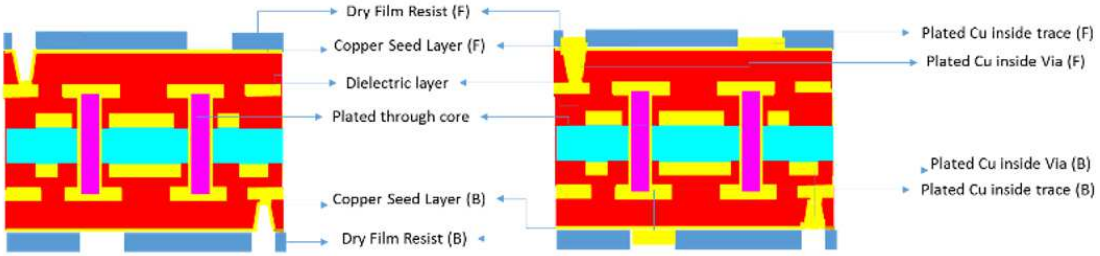

Figure 1.8: (a) Substrate layout without copper deposit and (b) with copper deposit

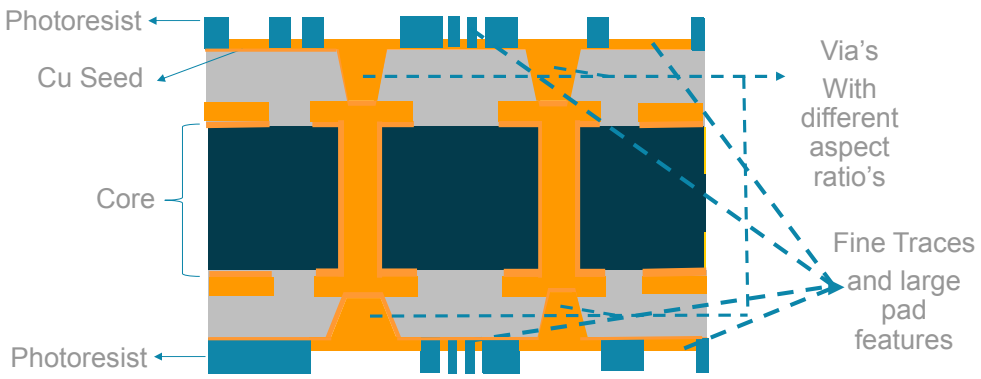

Figure 1.9: Substrate layout with copper deposit on microvia and fine pattern

Synthesis of copper through electrodeposition techniques have proven to be versatile, cost effective and readily scalable to high volume manufacturing. Alternative methods such as CVD (Chemical Vapor Deposition), Electroless deposition, PVD (Physical Vapor Deposition) methods have been developed but not utilized for bulk Cu deposition for cost considerations[3]. Electroless process has highly unstable electrolyte compounds and requires frequent bath dump for process stability. The process also needs expensive catalyst material for the copper to seed to dielectric. Electrodeposition of copper for IC substrate applications holds certain unique challenges. For example,

entrapment of voids and defects in via structures limits overall package power delivery and reliability. Presence of non-uniform copper deposit results in package assemblies with high warpage and poor compatibility to downstream processes which in turn results in significantly lowered assembly yield[7]. IC substrate packages require void-free gap fill inside via regions with an extremely small recess along with deposition of uniform copper film in fine line spaces (FLS). The choice of the native chemistry species, electrolyte composition, deposition parameters (temperature, bath composition, deposition current, etc.) utilized in electrodeposition process largely influences the metallurgy of the plated film. Furthermore, gaining insight into thin film properties such as film purity, grain orientation, grain size, intrinsic stress build up and understanding their relationship to different plating conditions is key to establish the desired metallurgy of the plated film.

Section 1.4 Introduction to Copper

Today, copper is the unanimous industry choice for interconnect build up. IBM introduced what is commonly now known as the "damascene process" in the late 1990s to form copper IC interconnects[3]. Later, a variation of the damascene process known as dual damascene process was developed for cost effectiveness. Different flavors of damascene processes exist today based on feature types and application[3, 7]. In all cases, copper is electrodeposited to form the desired circuitry. Thickness of the film deposit ranges in mesoscale to nanoscale depending on the need of the process. To date, copper metal has been the material of choice due to its clear technical advantages and lower cost.

For example, copper shows low electrical resistance, high thermal conductivity as summarized in the table below. [3, 7, 8]

Table 1.1: Comparison of conductivity, resistivity, density and melting point for various metals

Metal Types	Electrical conductivity (10.E6 S/m)	Electrical resistivity (10.E-8 Ohm.m)	Thermal Conductivity (W/m.k)	Density (g/cm3)	Melting point (°C)
Silver	62,1	1,6	420	10,5	961
Copper	58,5	1,7	401	8,9	1083
Gold	44,2	2,3	317	19,4	1064
Aluminum	36,9	2,7	237	2,7	660

Along with those advantages, Cu thin films also show improved electromigration (EM) life and tend to be easier to manufacture for IC applications[3]. Although silver is one of the best-known metal conductor, its high cost limits its use to IC circuits. Table 1.1[8] compares some of the key bulk properties of copper to some of the well-known metals. Aluminum metal was preferred in the early days, but copper is now the ubiquitous choice in interconnect applications due to it high conductivity and ease of manufacturability at shrinking node sizes. A comparison of some of the key bulk characteristics of bulk Cu and Al is given in Table 1.2[8].

Table 1.2: Comparative Characteristics of Copper and Aluminum

S.No	CHARACTERISTICS	COPPER	ALUMINUM
1	Yield Strength (Mpa)	216	55
2	Hardness (HV)	51	15
3	Electrical resistivity (μΩ-cm)	1.67	2.65
4	Young's Modulus (Gpa)	129.8	70.6
5	Resistive Capactive Delay in Intel Chip (ns)	0.3	1.0

As shown in Table 1.2, copper shows relatively high tensile strength. The lower electrical resistivity of copper makes it an excellent conductor of electricity which in turn significantly reduces interconnect signal delays (as shown in Table 1.2)[6].

Section 1.5 Summary

In summary, IC packages needs to incorporate high density interconnects made of fine copper traces and large aspect ratio via. Electrodeposition is the preferred industrial methodology to enable such advanced architecture. The fundamental principles that guide electrodeposition of process needs to be understood in order to enable advanced electrodeposition. In chapter II we discuss some of those fundamental principles to identify key pathways that enables electrodeposition for IC substrate packages.

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CHAPTER II

FUNDAMENTALS OF ELECTRODEPOSITION

The process of deposition and removal of a material from a metal surface is guided through electrochemical principles. Various kinetic and thermodynamic phenomenon facilitate electrodeposition reaction at the metal-solution interface during electrodeposition. There are several pathways of a electrode reaction to occur as shown in Figure 2.0. As shown in Figure 2.0, there needs to mass transfer of the reactants from the bulk of the solution to the interface. Several chemical reactions happens at the electrode–electrolyte interface. The reduced atoms then needs to adsorb to the metal lattice. Any non-reduced ions needs to quickly desorb or move away from the surface to allow the electrode reaction to continue further. Depending on the applied potential, the sustained electrode reaction can be controlled by the principles of one or more of these effects such as mass transport, chemical reaction, adsorption, migration, etc.

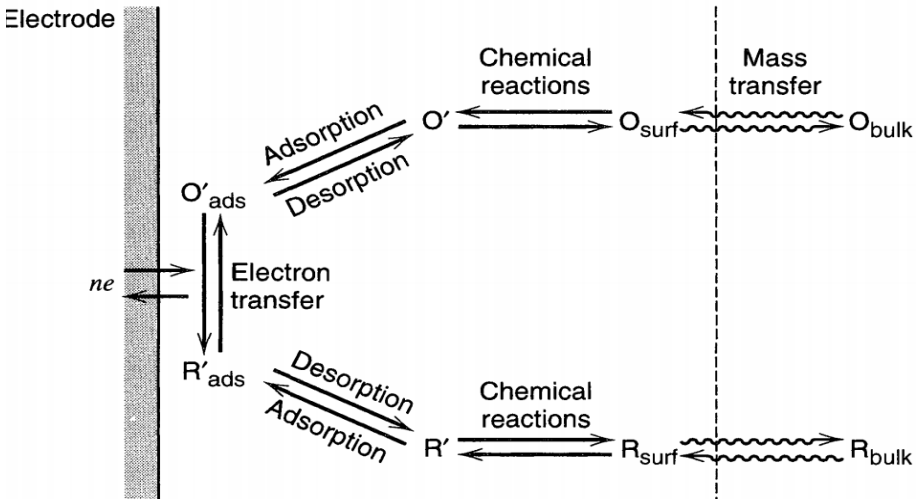

Figure 2.0: Pathway of a general electrode reaction

Section 2.0 Introduction

The distribution of an electroplated deposit depends upon which transport phenomenon controls the plating rate. In order for the reaction to continue uninterrupted and to achieve the desired deposit thickness, we need to consider the overall ohmic and mass transfer effects present inside the system. Furthermore, we need to determine which transport mechanism dominates the deposition reaction. Ohmic resistance of the metal film leads to variations of potentials in the film and solution resistance leads to variations of potential in the plating solution. Mass-transfer effects lead to variations in concentration of metal ion and other electrolyte species across the metal surface. Generally, non-uniform reaction rates are caused by either inadequate mixing, so that reactant concentrations are not uniform (convection effect), or by spatial variations in the electrical-potential difference across the electrode/electrolyte interface or due to concentration gradient (diffusion). Therefore, in order to establish a capable electrodeposition process, fundamental understanding of these principles and their impact is key. In this chapter we will discuss on some of the fundamentals of the electrodeposition process utilizing those principles.

Section 2.1 Process of electrodeposition

Typically, electrodeposition is performed by immersing a conductive surface (wafer / panel / any conductive metallic crystal lattice) termed cathode in an electrolyte solution comprised of metal ions (G) that needs to be deposited. To begin with, a metallic crystal lattice is immersed in an electrolyte with metal ions (G). An external power supply is

utilized to drive the electrons (e^-) from the anode towards the cathodic surface. The ensuing reaction between the metallic ions on the solution and the electrons on the cathode generates species H on the cathode as shown below.

$$\mathbf{G + n}e^- \rightarrow \mathbf{H} \quad \textbf{(2.1)}$$

where n is the number of electrons. For example, the above simplification can be extended to Cu deposition reaction as shown below.

$$Cu^{2+} + 2e^- \rightarrow \mathbf{Cu} \quad \textbf{(2.2)}$$

where, two moles of electrons are added to the cathodic surface that leads to reduction of one mole of cuprous (Cu^{2+}) ion to copper metal on the surface. Thus, in the absence of any secondary reactions, the amount of metal deposited (m) is easily estimated by utilizing Faraday's law[5] in terms of the no of moles of electrons supplied (n), amount of current driven by the power supply (I) to the reaction and deposition time (t) as,

$$m = ItA_w/nF \quad \textbf{(2.3)}$$

Here F is Faraday's constant, A_w is the atomic weight of the metal deposited and n is the number of electrons utilized for that reaction. For electronic applications, estimation of increase in metal thickness with the deposition process is a more desired parameter than the mass of the metal obtained [2]. This estimation is easily obtained by taking the density of the metal ion deposited in a given two-dimensional area and converting the amount of metal deposited to the thickness of the metal. For example (if we assume the deposition for copper metal in a well-mixed copper electrolyte solution), per faraday's law, a current of 1A when deposited over a period of 60s will theoretically yield 0.02g of Cu metal

based on equation 2.3. When deposited on a 1dm^2 surface area of the cathode surface the ensuing mass can be converted to predict 0.22μm of additional deposited copper (as thickness = mass / (area * density)). Practically however, the measured copper thickness varies due to various kinetic and thermodynamic limitation of the deposition process termed as losses. The current efficiency is then calculated as the ratio of measured weight (or thickness) to theoretically calculated value based on the equation 2.3 explained above.

Section 2.2 Kinetic and thermodynamic principles of electrodeposition

In order to best understand the kinetic and thermodynamics principles of electrodeposition, it's easier to break the electrodeposition process into three stages such as electrode immersion (prior to start of the deposition), initial phase of the deposition (process in the first few milliseconds) and deposition process thereafter.

Section 2.2.1 Stage 1: Equilibrium potential and exchange current density

Let's define the 1st stage as when the cathode surface (metal layer to be deposited) is immersed in the electrolyte solution before the external power supply is turned ON. In this case, as soon as the metal is immersed in the solution there will be an exchange of metal ions between the electrode – electrolyte interface and some ions from the cathodic metal lattice will enter the solution and vice versa until an equilibrium is established. Thus, a dynamic interface is created between the electrolyte and the metal surface. An exchange of ions happens between the two interface setting up an equilibrium. Even

though there is no applied potential or current to the metal electrode or electrolyte, the metal surface and the electrolyte exists in an equilibrium potential and there is exchange of charge due to the EMF acting as the driving force. This equilibrium potential is termed as rest potential or open circuit potential (OCP). This equilibrium potential (E_{rest}) is easily estimated using Nernst equation as a function of activity of the species as[1],

$$E_{rest} = E^0 + \frac{RT}{nF} \ln \frac{[G]}{[H]} \quad \textbf{(2.4)}$$

Where [G] is the activity of the oxidized species (Cu^{2+} for example in copper deposition) and H is the reduced species (Cu metal). R is a gas constant and T is the temperature. E^0 is the standard reduction potential estimated using Gibb's relationship as,

$$E^0 = -\frac{\Delta G^0}{nF} \quad \textbf{(2.5)}$$

Where ΔG^0 is the standard free energy of the reaction. For practical purposes, E^0 is estimated against a SHE (Standard Hydrogen Electrode) in a 1M solution at 298K [2]. The Standard Hydrogen Electrode has a reduction potential of 0V in a 1M solution at 298K [2] on a platinum electrode surface and is utilized as a reference scale for estimating all reduction potentials [4]. To best understand this SHE reference scale, a similar analogy can be given to another metric such as atomic mass. Atomic mass of all elements in the periodic table is referenced to the mass of a C^{12} atom. Reference to SHE potential for a given electrochemical reaction follows a similar analogy. For any reaction, deviations of standard reduction potential E^0 to E_{rest} based on actual concentrations utilized in the reaction can then be estimated utilizing Nernst equation. For example, for a divalent metal ion the equilibrium potential shifts by 29mV per decade of metal ion activity $[G]^2$.

For reference, the standard reduction potential of Cu^{2+} in a 1M solution against SHE at 298K is 0.337V and 0.521V for Cu^{1+} ion reduction[3].

$$Cu^{2+} + 2e^{-} \rightarrow Cu \qquad E^{0} = 0.337\ vs\ SHE \qquad \textbf{(2.6a)}$$

$$Cu^{+} + e^{-} \rightarrow Cu \qquad E^{0} = 0.521\ vs\ SHE \qquad \textbf{(2.6b)}$$

As discussed in various textbooks [1-3], thermodynamically unstable materials such as potassium and sodium exhibit negative potentials for reduction while noble metals such as gold and platinum, exhibit positive reduction potentials. When a potential more negative than the E_{rest} value of a metal/ion couple is applied at a surface immersed in a solution containing ions of the metal, electrodeposition (reduction) of the metal ion to the metal happens. Henceforth, species that exhibit more positive potentials are easier to deposit than thermodynamically unstable materials such as alkali metals. Electrodeposition of alkali metals incorporates other challenges because various other side reactions side (unfavorable reduction of various impurities) occur first before deposition of alkali metals leading to a poor deposit.

Section 2.2.1.1 Exchange current density

When the cathodic metal is initially immersed in the electrolyte, despite the absence of any measured current, there is still an exchange of charge at the interface. This exchange of charge is equated in terms of exchange current density i_0. To best understand this, let us take the example of copper metal immersed in a copper sulfate solution, Cu^{2+} ions will leave the metal surface faster than the ionic movement from the electrolyte towards the

Cu lattice. This leaves the metal lattice deprived of Cu^{2+} ions at the solution interface leading to accumulation of excess electrons on the interface and a negative charge.

This accumulation of negative charge subsequently enables rearrangement of charges (ions) on the solution side of the interface. The solution side now has accumulation of Cu^{2+} ions or positive charge on the interface as shown in Figure 2.1

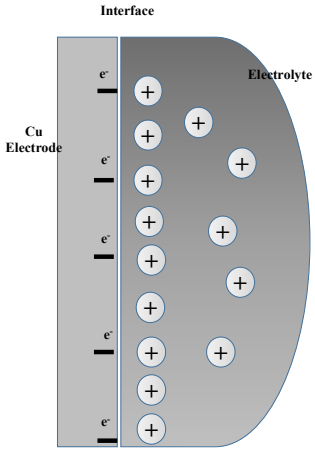

Figure 2.1: A simple schematic to show metal solution interface after immersion and before start of electrodeposition [3]

This accumulation further slows the movement of ions from the cathodic crystal lattice and increases the rate of ions entering the lattice. After a certain period, an equilibrium is established. We discussed the potential measured at this stage as equilibrium potential with no net current flow but exchange of charge. This exchange of charge is estimated as exchange current density and is determined as follows. For a generic reaction explained below, where species H is formed, let k_c be the rate constant of the forward reaction (cathodic) and k_r for the reverse reaction.

$$G + ne^- \underset{k_r}{\overset{k_c}{\rightleftharpoons}} H \quad (2.7)$$

Utilizing Arrhenius equation, the rate constant of forward and reverse reaction rate is express as[1]

$$k_c = A_c \exp\left(-\frac{\Delta G_c}{RT}\right) \quad (2.8)$$

and

$$k_r = A_r \exp\left(-\frac{\Delta G_r}{RT}\right) \quad (2.9)$$

Where A_C and A_r are the Arrhenius constants for the forward and reverse reactions and ΔG_c and ΔG_r are the gibb's free energy for the forward and reverse reactions. The rate of forward cathodic reaction can be expressed in terms of current as[1],

$$\frac{I_c}{nFA} = \text{reaction rate} = k_c C_G \quad (2.10)$$

Where A is the active surface area, C is the concentration and C_G and C_H are the concentrations of the respective species G and H and F is Faraday's constant. Similarly, the rate of the reverse reaction can be expressed in terms of current as,

$$\frac{I_r}{nFA} = \text{reaction rate} = k_r C_H \quad (2.11)$$

The net current for the above generic reaction is calculated as

$$I = I_c - I_r \quad (2.12)$$

By substituting the above expressions, the net current equation is expressed as[1]

$$I = nFA[k_c C_G - k_r C_H] \quad (2.13)$$

At equilibrium the reaction rates are matched where $k_cC_G = k_rC_H$ and I = 0. We can simplify, $k_c = k_r$ to k^0 when the system is at equilibrium potential E^0, as the activity and concentration $C_G = C_H = C$. Here C is the concentration of ion in the bulk. Even though the net current I is zero at equilibrium, there is still a balanced faradaic activity between the solution and the interface. This balanced activity is expressed as exchange current "I_0" which based on all the above equation simplifies to[1]

$$\boldsymbol{I_0 = FAk^0C} \text{ or } \boldsymbol{i_0 = Fk^0C}, \text{ where } \boldsymbol{i_0 = \frac{I_0}{A}} \qquad \textbf{(2.14)}$$

Thus, the exchange current (I_0) or the exchange current density (i_0) is directly proportional to k^0 the reaction rate constant and is often substituted or utilized to express the rate of the reaction in kinetic equations. For electrochemical reactions, exchange current density can be easily determined with Butler-Volmer expressions for cathode and anode reactions (discussed in the next section below) which in turn allows us to directly gauge the rate of the reaction without actually computing the rate constants. As discussed in various text books[1-3], reactions with large exchange currents correspond to very rapid and usually reversible metal reduction charge transfer kinetics and result in strong dependence of the deposition current on mass transfer and applied potential.

Section 2.2.2 Stage 2: Kinetics of early stage of deposition

When the external power supply is turned on, an excess potential or overpotential is applied to the electrode surface as the electrons move towards the cathode. This increase in applied potential results in an exponential increase in the deposition current at a given

interfacial ion concentration and the resulting current density is best determined by the relationship developed by Butler- volmer[1-3]

$$\boldsymbol{i = i_0\left[exp\left(\frac{(1-\alpha)nF(E-E^0)}{RT}\right) - exp\left(\frac{(-\alpha)nF(E-E^0)}{RT}\right)\right]} \quad \textbf{(2.15a)}$$

where α is the symmetry factor between cathodic and anodic reaction, i is the current density and i_0 is the exchange current density, n is the number of electrons, R is a gas constant, T is the temperature of the reaction and E and E^0 are the applied potential and standard reduction potential. This equation essentially represents the net current flowing through the system for a reversible reaction when an anodic (oxidation) and cathodic (reduction) reaction are happening reversibly and in parallel. For α = 0, this reaction simplified to $i = i_0$ which indicates the cathodic and anodic reaction are in equilibrium and symmetric. Similarly when $\eta = 0$, $i = i_0$, that is in the absence of an applied overpotential an equilibrium is established with the net current density operating as the exchange current density. Once an overpotential is applied, the α shifts towards either cathodic or anodic reaction based on the standard reduction potential and determines the net value and direction of current flowing. For irreversible electrodeposition reaction that happens at high enough cathodic potentials, Butler volmer equation can be simplified to equation 2.15b discarding any anodic contributions.

$$\boldsymbol{i = i_0\left[-exp\left(\frac{(-\alpha)nF(E-E^0)}{RT}\right)\right]} \quad \textbf{(2.15b)}$$

Expression 2.15b is widely utilized to simulate the observed current density based on applied potential. The transfer coefficient α for the cathodic process (deposition of Cu^{2+}) is obtained from the slope of the plot of applied potential vs the observed current density

$\eta\ Vs\ log\ (i)$ or mathematically noted as $d\eta\ /\ d\ (log\ i)$. Overall, the current dependence on potential can be considered analogous to a reaction rate dependence on temperature in an Arrhenius equation [2]. Alternatively, the metal solution interface can be considered as a resistance element in an equivalent circuit, which decreases in value as the applied voltage increases. The above stage of the deposition process is termed to happen in kinetic or activation controlled regime. However, the kinetic phase of deposition applies only when the concentration of the ion at the interface is matched to the bulk concentration C (a key assumption that relates k^0 to i_0). In reality, the concentration of the ions varies as deposition process proceeds further [3]. For example, the metal ions are consumed during electrodeposition with an applied potential and the concentration of metal ions decreases at the interface. In order for the electrodeposition process to continue, further transfer of ions from the bulk of the solution needs to happen. Figure 2.2[3] shows how concentration profile varies across at the interface especially around the metal interface called the diffusion layer. The stagnant diffusion layer and the mass transfer effect is discussed in the following section.

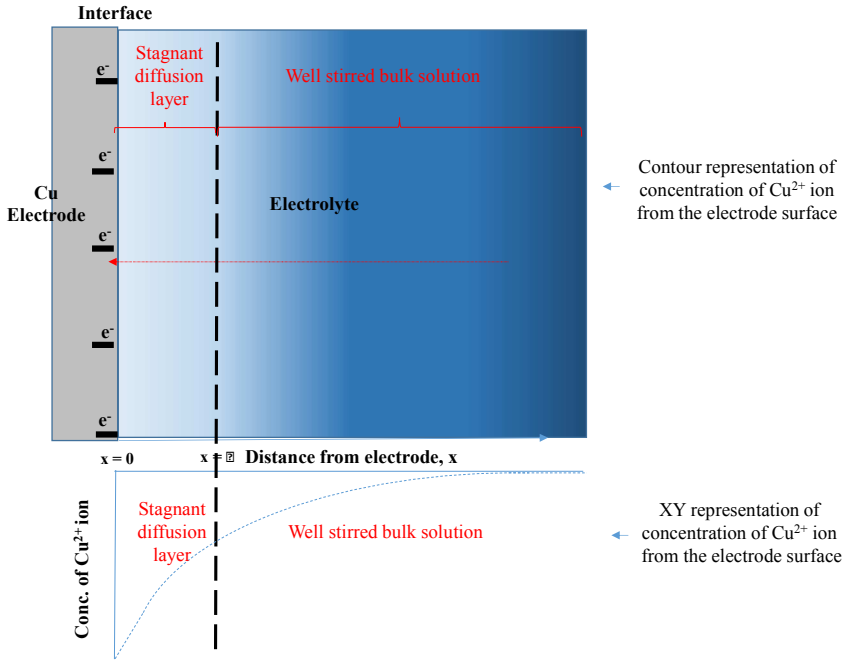

Figure 2.2: A schematic to show concentration profile in the bulk and in the diffusion layer

[*Figure adapted from reference*[2]]

Section 2.2.3 Stage 3: Helmholtz double layer and mass transfer effects

In order to best understand the effects of mass transfer, let us briefly describe the setup of electrolyte ions close to the interface and far from the interface. As previously explained, when a metal is immersed in an electrolyte there is movement and rearrangement of charges on interfaces on both the solution side and metallic surface. This double layer charge arrangement has been experimentally proven to behave like a capacitor with capacitance measured on the order of Farads that varies based on the experimental setup. The solution side of this double layer is hypothesized to be made of multiple layers as shown in the Figure 2.3[1] below. The inner layer (IHP – Inner Helmholtz plane) is described as layer closest to the electrode with adsorbed solvent molecules and

specifically oriented adsorbed redox ions without the solvation shell. The subsequent outer layer (OHP – Outer Helmholtz plane) is then arranged with the solvated cations.

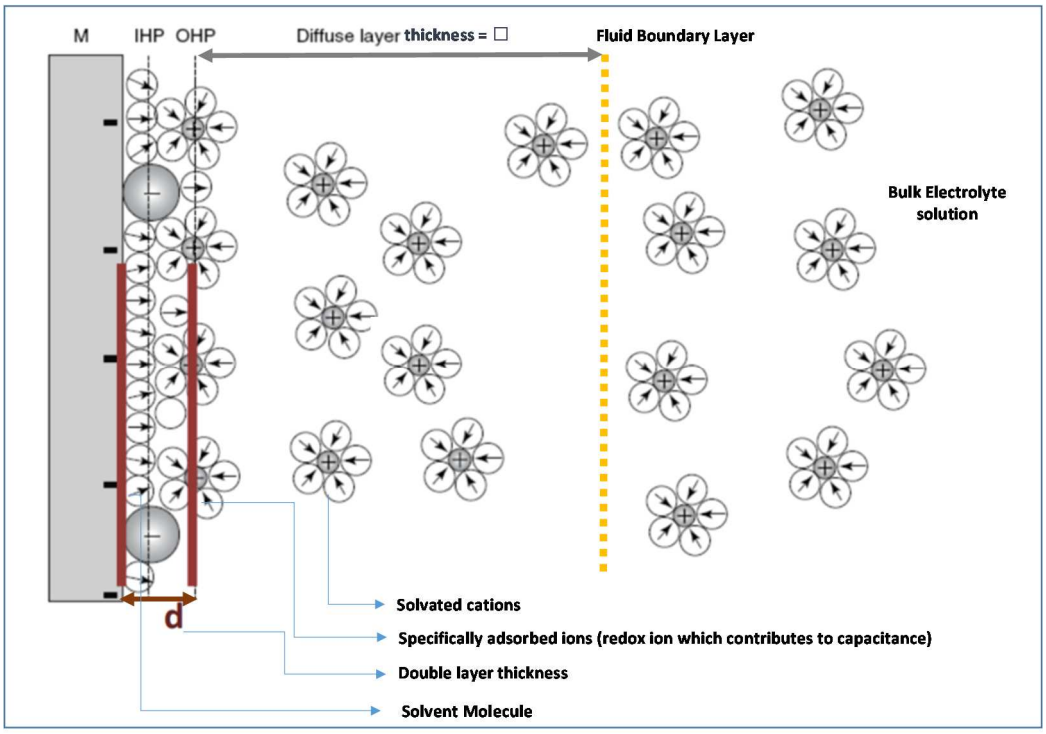

Figure 2.3: A schematic to show double layer and ionic behavior far and close to the interface

[Figure adapted from reference[5]]

The distance "d" between the OHP and the metal layer is termed as double layer thickness [3]. Typically, IHP thickness ranges to length scales on the order of few angstroms and OHP thickness ranges to a few nanometer [1]. The solvated ions in OHP interact through electrostatic force in a nonspecific manner [1]. Because of thermal agitation in the bulk solution, non-specifically adsorbed ions distribute around the OHP in a diffusion layer that extends to the bulk of the solution. Diffusion layer thickness is usually on the order of few microns to about 1000µm based on the convection in the

boundary layer[2]. Convection due to mixing and thermal /mechanical agitation enables uniform concentrations of species across distances much greater than a distance of about 1mm [2]. Increasing convection decreases the thickness of the stagnant diffusion layer at the cathode interface. Transfer of ions from the bulk of the solution to the interface happens though three different transport mechanism such as migration, diffusion and convection [3]. These distinct ion transport mechanism is represented mathematically using Nernst Planck equation[3] as follows,

$$\boldsymbol{N_i} \;=\; -\boldsymbol{Z_i D_i c_i \frac{F}{RT} \nabla \emptyset} \;-\; \boldsymbol{D_i \nabla c_i} \;+\; \boldsymbol{c_i v} \qquad \textbf{(2.16)}$$

Flux = Migration + Diffusion + Convection

where N_i is the molar flux of the species *i*, Z_i is the charge number of the ionic species *i*, F is the Faraday's constant (96485 C/mol), D_i is the diffusion coefficient (m^2/s), $\emptyset$ is the electrostatic potential (V), c_i is the concentration of species (mol/m^3), v is the velocity of the species *i*, R is the Ideal gas constant (8.3145 J / K. mol), T is the temperature (K).

Migration represents movement of the ions due to an applied electric field. Cations move towards the cathode and anion towards the anode due to this ionic migration. Migration is easily evaluated with the estimation of ionic conductivity (ƙ) using the equation[1],

$$ƙ = \frac{\boldsymbol{F^2}}{\boldsymbol{RT}} \sum_i \boldsymbol{Z_i^2 D_i c_i} \qquad \textbf{(2.17)}$$

Solutions with large conductivity show minimal ohmic loss. Therefore, migration effects are usually negligible when excess charge carriers are present in the system or when the solution conductivity is high. During electrodeposition a supporting electrolyte such as sulfuric acid or an alkaline solution is purposely added to negate any migration effects. In the absence of appropriate mixing and convection, migration effects can dominate if the current carrying capacity of the ion is a significant portion of the entire solution. This is estimated using transference number. The transference number[1] represents the fraction of the current carried by that ion in a solution of uniform composition.

$$t_i = \frac{z_i^2 D_i c_i}{\sum_i z_i^2 D_i c_i} \qquad \textbf{(2.18)}$$

In copper deposition for IC substrate applications with a well-mixed sulfuric acid-based electrolytes, the transference number of protons (H^+) is so large that migration effects are negligible compared to diffusion limitations[2].

Diffusion represents movement of ions due to a concentration gradient and usually plays a large role in determining the deposition characteristics for IC applications. As previously explained, because of thermal agitation in the bulk solution, non-specifically adsorbed ions distribute around the OHP in a diffusion layer that extends to the bulk of the solution. The stagnant layer between OHP and the fluid boundary layer defined in Figure 2.3 is termed diffusion layer. Thickness is usually on the order of few microns to about 1000µm based on the convection in the boundary layer.

The diffusion term in the Nernst Planck equation[4] ($-D_i \nabla C_i$) can be simplified to calculate diffusional flux J_i of a particular chemical species using Fick's first law of diffusion in x-direction as[4],

$$j_i = -D_i \frac{\partial C_i}{\partial x} \quad \textbf{(2.19)}$$

This diffusion represents a key component of ion transport that cannot be neglected under any conditions during electrochemical consumption at an electrode[3]. At room temperature, copper ions in an electrolyte solution generally have a diffusion coefficient of order ~$5x10^{-6}$ cm^2 /s that roughly results in a 0.1ms diffusion time for a 0.1µm distance and a 1s diffusion time across a 25µm distance[1]. As shown in Figure 2.4 below, at low overpotential (when the applied potential E is closer to E^0) current density increases exponentially per Butler Volmer equation as explained in the previous section (Region 2) and stays linear at very low overpotential (Region1). However, at sufficiently high overpotential there is no increase in current density with increase in applied potential potential. In the absence of any migration effects in a well-mixed system, this effect is likely due to diffusion. This effect can also be seen for long deposition times since the interface region is depleted of metal ions and the rate of ion transport in the diffusion layer from the bulk determines the rate of deposition. Thus, the process now shifts from activation (kinetic control) to diffusion (thermodynamic control) and becomes diffusion limited. This steady state diffusion control enables a constant current or limiting current with any increase in applied potential as shown in (Region 4) in the graph below

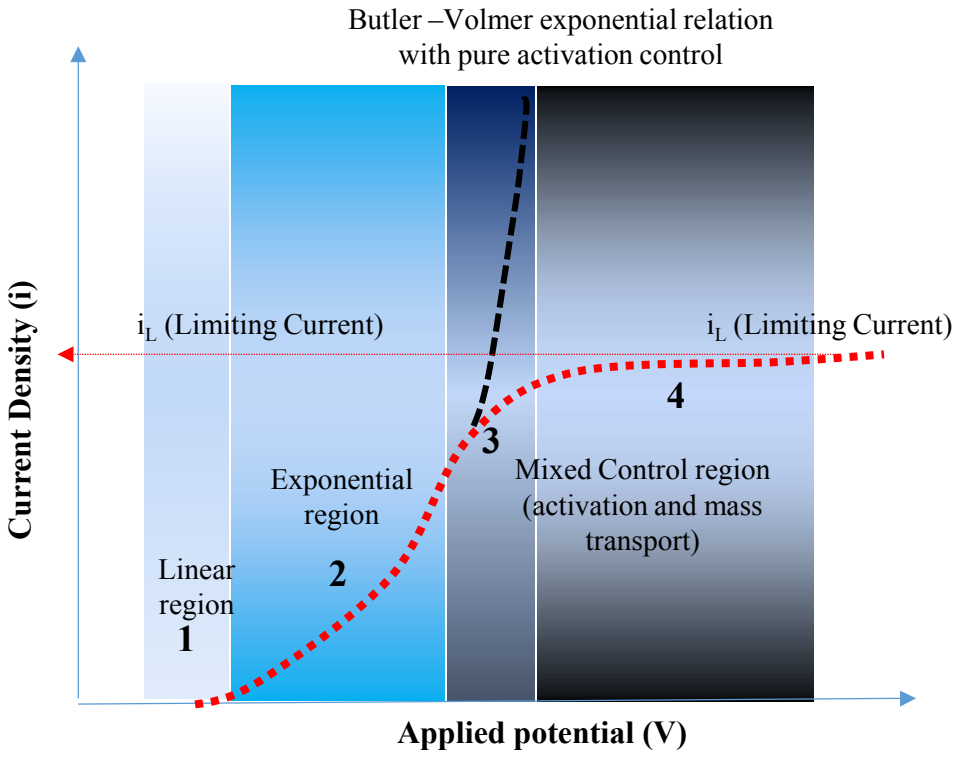

Figure 2.4: A schematic to show current density to applied potential relationship

[Figure adapted from reference[2]]

Mathematically, this limiting diffusion current density (i_L) can be determined using Cottrell equation as

$$i_L = \frac{nFD_i^{\frac{1}{2}}c_i}{(\pi t)^{0.5}} \qquad (2.20)$$

Where t is the deposition time. If we approximate diffusion length for $(Dit)^{0.5}$ then the above equation simplifies to,

$$i_L = \frac{nFD_i c_i}{} \qquad (2.21)$$

When operating at limiting current density, the species are reduced as soon they reach the interface. Increase in applied potential at limiting current density will cause non faradaic reactions such as rearrangement of ions in the electrode than the metal ion reduction. Region 3 in the fixture above is termed a mixed region when the transition from activation control to diffusion control happens.

Lastly, convection includes movement of ions in the bulk solution by agitation, pumping etc. to maintain a well-mixed solution. Once the diffusion layer is established metal ions travel by diffusion and migration. The ionic flow at a given point on the surface is proportional to the concentration of metal ions at the interface regardless of other factors. Typically, the interfacial concentration is increased by faster mass transfer and higher bulk concentrations of metal ion in solution.

Section 2.3 Current distribution with electrodeposition for planar and non-planar (via) surfaces

So far, we discussed the Butler Volmer kinetic effects that predicts kinetically control current density (or deposit profile) and Nernst Planck effects to predict the mass transfer effects that affect the flux (or) transport of ions in the electrolyte and eventually the current density / deposit thickness. To proceed further, it is necessary to classify the electrodeposition process utilized in real systems into some simple categories (primary, secondary and tertiary) based on their operating parameters in order to best understand which losses / stages of electrodeposition previously described dominates the current

distribution. We can then utilize those identified key knobs to tweak the process parameters and obtain the desired deposit profile.

For example, if we assume a frequently use case system where the reduction reaction happens at a very fast rate then the kinetic effects can be neglected. The criteria here is that the reaction is so fast that there is no electrodeposition in activation region (kinetically controlled). Metal ions are quickly reduced as they approach the interface. If the electrolyte solution is assumed to be well mixed (no convective effects) and if the concentration of reductant metal ions is very high in the electrolyte (no diffusion effects) then losses due to convection and diffusion term can also be considered negligible. Thus, the Nernst Planck equation simplifies to the migration portion only or ohm's law as the movement of ions is dictated by the solution conductivity or solution resistance, which is constant for a given electrolyte. This case can be classified as a primary current distribution model in that it accounts only for the electric field present in the process which is dictated by the geometry of the anode and cathode surface and the distance between the electrodes (the length of electric field) along with the solution resistance which is constant for a given electrolyte [3,6].

For systems that undergo slow reduction kinetics, secondary current distribution is utilized to model current distribution. This case is the most popular in simulating industrial applications in electrochemistry. Unlike primary current distribution, in this case, losses due to activation caused by the slowness of the reduction process is thought to be significant. Rest of the assumptions in primary case including (good mixing enabled by convection) and high concentration of the ion (no diffusion) still applies. Essentially,

in this case activation losses due to polarization of the electrode is taken into consideration along with solution resistance[3]. In this situation electrode kinetics losses are not found to be negligible compared to the ohmic losses. This model can be applied to predict uniform deposition on a non-planar surface. Consider a non-planar via surface as shown in figure 2.5[7] below let us assume $l = 25\mu m$ (depth of the via) After initial deposition with the deposition conditions aligning to the assumptions defined above uniform conformal deposition is obtained at the top and bottom of the feature. For such cases, Wagner[7] devised a new notation called "Wagner number" to predict the extent of uniformity in current distribution with a secondary current distribution model.

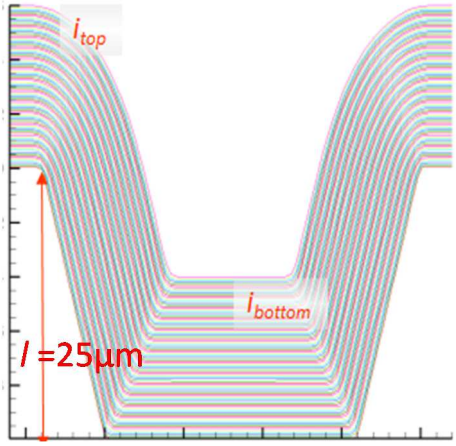

Figure 2.5: A simple schematic to show conformal plating with non-planar surface

This Wagner number is denoted as,

$$Wa = \frac{\kappa\left(\partial\eta/\partial i\right)}{l} \tag{2.22}$$

Where l is the length of the non-planar surface, κ is the solution conductivity and $(\frac{\partial \eta}{\partial i})$ is the polarization ratio or slope of the polarization curve. For fast reaction kinetics, $\frac{\partial \eta}{\partial i} = 0$ and hence Wa = 0 indicating the secondary reaction simplifies to primary current distribution model[7]. For more realistic case where there is limited kinetics, Wa number can be used to predict the degree of uniformity even on a non-planar surface. Higher the Wagner number obtained, the process simplifies to more uniform deposit with secondary current distribution assumptions.

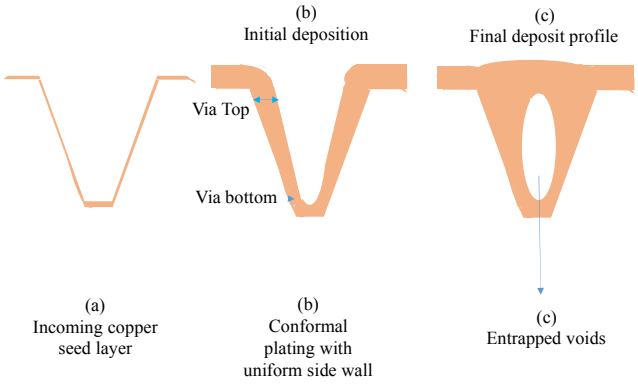

Figure 2.6: Void formation with mass transfer limitation on a non-planar via region

For IC substrate packages, uniform deposit is desired on the top of the via surface while super fill is desired inside the via. Thus, this case is more accurately reflected utilizing tertiary current distribution model that also considers concentration variation at the interface. In other words, mass transfer limitation due to consumption of reducing species at the electrode surface leads to diffusion limitation. Diffusion of reducing species from

the bulk of the solution to the interface limits the overall reaction. Although during the initial stages of the deposition reaction, the concentration is uniformly distributed inside the top and bottom of the via leading to conformal deposition, reduction in concentration of the species (more so at the via bottom than at the via top) due to length of the diffusion layer being small at the Via top than at the Via bottom (as the bulk solution fluid boundary layer is way further from the bottom of the feature) the diffusion times are longer and becomes limiting at the via bottom. This leads to non-uniform current distribution of higher deposition rate at the via top than at the via bottom which in turn leads to voids entrapment. A cartoon showing this effect is shown in figure 2.6.

Section 2.4 Summary

As previously explained, non-planar surfaces undergo uniform deposition rates during the initial stages of deposition as shown for a via feature example in Figure 2.6. That is, via sidewalls at the top undergo reduction at the same rate as via sidewalls at the bottom. However, a sustained deposition reaction in such scale could lead to a void entrapment. In summary, the understanding the principles of electrodeposition can explain which transport mechanism dominates current distribution and the effective thickness deposition on planar and non-planar surfaces such as via's. Discussion on how void entrapment occurs along with some key methodologies to enable void-free fill inside the via is discussed further in chapter III.

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CHAPTER III

VIA FILL MECHANISM AND CHALLENGES

This chapter focusses on various mechanisms that facilitate bottom–up fill to achieve void-free via fill. The role of cupric and cuprous ions, mechanism and fill challenges with the incorporation of organic additives is further elaborated. The mechanism that leads to void entrapment is first discussed.

Section 3.0 Introduction to voids in copper electrodeposition

As shown in Figure 3.1, during the initial stages, the deposition happens under kinetic regime (Figure 3.1b) and the thickness of the copper is still uniform at the top and bottom of the via sidewalls [14]. Incoming seed layer prior to the start of deposition is shown in Figure (3.1a). As the deposition process continues from the initial stages, (as deposition process usually happens for t >10s to achieve the desired thickness) the concentration of Cu^{2+} that is getting consumed at the via bottom and via top of the sidewalls needs to be adequately replenished. If adequate replenishment does not happen, side walls of the via top will show higher Cu^{2+} concentration and increased thickness / deposition rate compared to the sidewalls of the via bottom as shown in Figure 3.1c. As previously discussed this phenomenon is due to diffusion limited mass transfer of Cu^{2+} from the bulk of the solution to via bottom. Sidewalls at the via top are unlikely to see this behavior because of their proximity to the bulk solution. The diffusion limitation at the via bottom leads to reduced deposition rate at the sidewalls of the via bottom. As mass transfer limitation of the process takes over further, the deposition transitions completely from

kinetic to diffusion regime. In that case, deposition rate becomes slow at the side walls of the via bottom while the via top continues at a sustained rate. As the deposition process continues even further, this condition exaggerates leading to a condition termed "pinch off", where in the sidewalls at the top of via start to collide[14]. Figure 3.1d shows the plated profile inside the via prior to pinch-off where the thickness of the sidewall is much higher compared to the thickness of the side walls at the via bottom. Further extension in deposition process leads to entrapment of voids in the middle due to "pinch-off" as shown in Figure 3.1e.

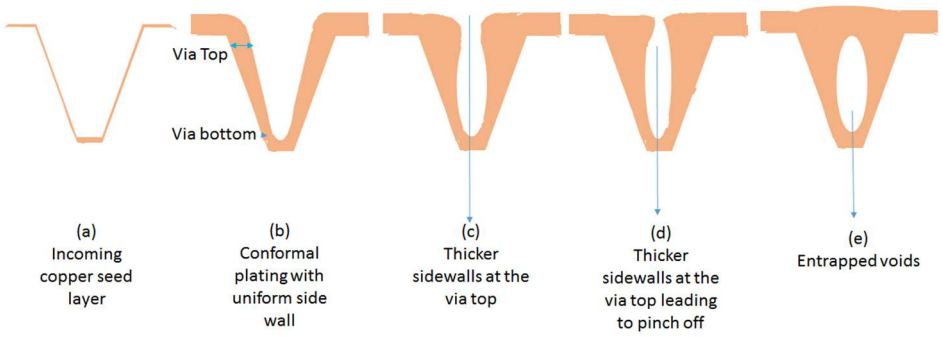

Figure 3.1: Electrodeposition of copper to show void formation

Void entrapment is a significant risk for overall package reliability and IC circuit functioning [1-4]. For industrial applications, there is a critical need to establish completely filled via features with copper metal that is void-free in order to ensure signal and IC substrate package integrity [1-4]. In order to establish a void-free process, a differential plating rate needs to be established as there is a risk of void entrapment. To establish a void-free process, this differential plating rate needs to happen in such a way where the deposition rate at the bottom of the via (i_{bottom}) has to be at a rate that is much higher compared to the top of the via ($i_{top.}$)[3, 24, 14]. This challenging process requirement to

enable bottom-up fill where $i_{bottom} > i_{top}$ (deposition rate or current density higher at the bottom of the feature compared to the top) has been the focus of various scientific studies for decades [1-4].

To quantify the goal discussed above, a key ratio parameter of "i_{top} / i_{bottom} " is utilized in various literatures named as "throwing power" or "BUF" (bottom-up fill ratio) or " Gap fill ratio" and needs to be greater than a value of 1 for bottom-up fill to be established inside the feature[1-4,] . IC substrate applications require even smaller throwing power for void-free fill due to the tapered nature of the Via. A critical aspect to consider here is that establishment of an process that achieves throwing power greater than 1 (i_{top} / i_{bottom} ratio >1) doesn't necessarily guarantee a void-free fill. Minimum gap fill ratio to enable void-free fill is dictated by geometry of the incoming non-planar surface (via / trench). This geometry is defined as "aspect ratio" which is widely accepted in the scientific world as the ratio of depth of the via (height of the via) to the via bottom diameter [3, 4]. The minimum required ratio to establish a void-free fill process varies based on the type of application or aspect ratio. Different feature types utilized in copper electrodeposition applications are classified based on this incoming aspect ratio of the via / trench surface. It is imperative that the likelihood of obtaining void-free fill on via's with higher aspect ratio is far more difficult compared to lower aspect ratio via's. In other words via features with large aspect ratio require advanced process capability that enables very high throwing power (i_{top} / i_{bottom} ratio >>>>1). Typically, i_{top} and i_{bottom} are estimated by measuring the thickness of the sidewalls at the top and bottom of the via.

Faraday's law enables this calculation as the proportionality of mass/ deposit thickness to the applied current density[55].

Section 3.1 Introduction to via fill in copper electrodeposition

The process of obtaining a void-free fill with a bottom-up fill inside the via feature is termed as "super fill" or in simplified terms "via fill" or "gap fill" process[3-5]. This process is also referred in some cases as "super - conformal" process[16]. When a via feature that needs to undergo super fill is immersed in an electrolyte solution, prior to to the start of deposition process, a metal- solution interface across various points in the via region (via top sidewalls as well as via bottom sidewalls) is established. All the points along the via features (top and bottom) are electrically connected (shorted) with a continuous copper seed layer (cathodic surface). Therefore, any potential difference of copper seed layer at the top and bottom of the via can be assumed to be negligible. This is especially true for extremely thick Cu seed layers where sheet resistance is negligible. Via features utilized in IC substrate applications utilize seed thickness in the range of 7000Å to 15000Å which eliminates any ohmic potential difference contribution from the seed layer[1,3,4]. In order to establish a differential deposition rate, majority of the scientific efforts have focused their innovation efforts on the solution side of the interface. Typically, organic additives are added to the electrolyte bath to enhance the the growth rate of copper inside features relative to the top of the via. [3,5,14] For very thin seed layers (1000Å or less) sheet resistance of the seed influences deposition kinetics leading to even higher probability of void entrapment, necessitating a more robust approaches for differential plating and

superfill[3]. Besides establishing a differential via fill, organic polymer additives are added in trace amounts to the electrolyte to influence the grain structure and purity of the deposited copper. Therefore, key parameters such as ductility, hardness, surface roughness, stress and tensile strength of the deposited film also need to be evaluated when utilizing an organic additive based approach for via fill[3].

Copper deposition technology has evolved through generations and application to IC circuits has happened as recently as a decade ago. Significant "prior art" exists for additive based fill approach for copper damascene process specifically for large aspect ratio via's where plating time scales are in the range of few minutes to seconds. The manufacturing extendibility of such process has also been achieved to bath volumes as high as 300L or so with a bath life of few weeks[2,3]. For IC substrate packaging applications, the composition of electrolyte involved in copper electrodeposition includes acidic aqueous electrolyte bath with dissolved copper sulfate, sulfuric acid, chloride ions and various organic additives to enable via fill [3,4,14].

Section 3.2 Inorganic components in copper electrodeposition

Cu^{2+} supplied as copper sulfate pentahydrate ($CuSO_4.5H_2O$) solution and sulfuric acid H_2SO_4 along with Cl^- (supplied as HCl) are the primary inorganic constituents of the copper plating bath. Mechanism and role of each of these components is further discussed below. As previously discussed, high concentration of Cu^{2+} (sourced from $CuSO_4.5H_2O$) eliminates diffusion limitation. As shown in equation 2.22, deposition rate of copper metal and its distribution is strongly correlated to conductivity of the

electrolyte solution (ƙ). In copper electrodeposition, ionic conductivity is determined through the concentration of protons (H^+ ions) supplied from H_2SO_4. A high concentration of H_2SO_4 decreases solution resistance and mitigates any migration effects. As discussed in scientific literature, the unique transport mechanism of ions that aids in ionic conductivity with increased H^+ ions is explained with Grotthuss mechanism[4].

Separately, considerations of solubility of $CuSO_4.5H_2O$ in sulfuric acid solution limits the peak concentration that could be utilized for Cu^{2+} in the electrolyte. The trade-off here is that if very high concentration of $CuSO_4.5H_2O$ is utilized to eliminate diffusion (mass transfer limitation) this could limit the maximum concentration of sulfuric acid in the electrolyte due to solubility concerns. A high concentration of H_2SO_4 in the electrolyte is often desired for improved conductivity from the electrolyte as that in turn facilitates uniform distribution of copper deposit across features of various geometry. Various scientific studies tabulate the range of use of these components based on application type[3,4]. Besides these two key components, a small amount of catalyst in the form of Cl^- is added to catalyze various reactions (that will be discussed below) especially in the presence of organic additives.

Section 3.3 Criticality of cuprous ion in copper electrodeposition

Reduction reaction of copper deposition is described as

$$\boldsymbol{Cu^{2+} + 2e^- \rightarrow Cu} \qquad \textbf{(3.1)}$$

Various scientific studies [4,6] have shown that Cu^{2+} reduction follows a three step pathway shown as reactions (3.2a), (3.2b) and (3.2c) and Figure 3.2. Of these three identified

reaction mechanisms, the rate controlling step of conversion of Cu^{2+} to Cu^{1+} (reaction in equation 3.2a) is determined to be the most critical due to the formation of Cu^{1+} intermediate that is present in a reversible equilibrium at the copper surface[4,41,44,]. Formation of Cu^{1+} is strictly defined by the applied potential in order for this reaction to be rate limiting. Bockris *et al* [41,44] have shown that the reduction of Cu^{1+} to Cu (reaction in equation 3.2b) happens very fast due to the high value of exchange current density observed and it is mostly accepted that this reaction is unlikely to be the rate controlling step. Cupric reduction to Cu reaction has also a large rate constant observed.[4,41,44]

Formation of Cu^{1+} can happen in multiple pathways. In equation 3.2 (a), formation of Cu^{1+} happens through the reduction of Cu^{2+} with an applied potential. However, Cu^{1+} is also formed even in the absence of any applied potential due to the interaction of Cu metal surface with Cu^{2+} as shown in equation 3.3a [4,6]

$$\boldsymbol{Cu^{2+} + e^{-} \rightleftharpoons Cu^{+}} \quad \textbf{(3.2a)}$$

$$\boldsymbol{Cu^{+} + e^{-} \rightleftharpoons Cu_{ad}} \quad \textbf{(3.2b)}$$

$$\boldsymbol{Cu_{ad} \leftarrow\rightarrow Cu_{lattice}} \quad \textbf{(3.2c)}$$

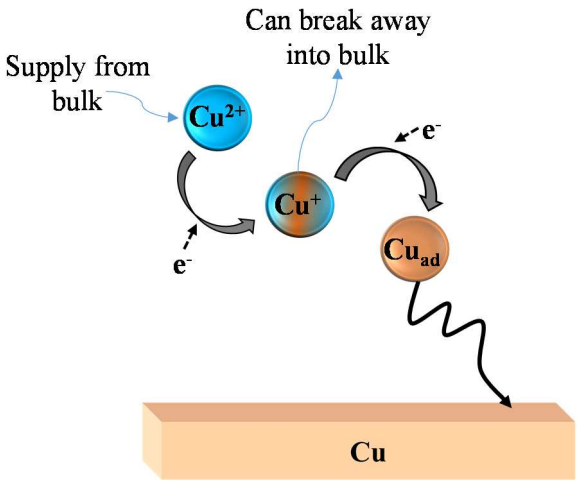

Figure 3.2: Reduction of Cu^{2+} with the formation of Cu^{1+} and Cu_{ad} intermediates

It has been reported that Cu^{1+} can easily diffuse away from the interface into the bulk of the solution [6,10]. In such cases Cu^{1+} is easily oxidized back to Cu^{2+} in the presence of dissolved oxygen or with the addition of O_2 (introduced with an O_2 bubbler) inside the electrolyte solution[10]. Besides the formation of Cu^{1+}, other intermediates such as $CuCl_{ad}$ adsorbate is also formed on the surface in the presence of Cl^- at OCP (Open Circuit Potential) as shown in equation 3.3a and 3.3b. Reactions shown in equation 3.3a and 3.3b are termed as comproportionation reaction[6].

$$Cu + Cu^{2+} \rightleftharpoons 2Cu^{+} \quad \textbf{(3.3a)}$$

$$Cu + Cu^{2+} + 2Cl^{-} \rightleftharpoons 2CuCl_{ad} \quad \textbf{(3.3b)}$$

In summary, generation of Cu^{1+} happens both at OCP as well as during the rate controlled reduction of Cu^{2+} ion. In all cases, the formation of Cu^{1+} further leads to the formation of $CuCl_{ad}$ adsorbate film due to the strong interaction of Cu^{1+} ion with Cl^- ion. Equation

3.4a through equation 3.4e summarizes all the reactions that happens once the reduction process proceeds in the absence of any organic additives [6].

$$Cu^{2+} + e^- \rightleftharpoons Cu^+ \quad \textbf{(3.4a)}$$

$$Cu^+ + e^- \rightleftharpoons Cu \quad \textbf{(3.4b)}$$

$$Cu^{2+} + 2e^- \rightleftharpoons Cu \quad \textbf{(3.4c)}$$

$$Cu^{2+} + Cl^- + e^- \rightleftharpoons CuCl_{ad} \quad \textbf{(3.4d)}$$

$$CuCl_{ad} + e^- \rightleftharpoons Cu + Cl^- \quad \textbf{(3.4e)}$$

In the presence of organic additives, presence of Cu^{1+} ion and the $CuCl_{ad}$ plays a vital role in complexing and enabling a differential rate of deposition, i.e., increase or decrease rate of deposition when compared to the normal rate. Via fill or gap fill is established due to the difference in the Cu^+ amount between the inside and outside of the via hole [11].

Section 3.4 Role of chloride ion in copper electrodeposition

The role of Cl^- and the kinetics of $CuCl_{ad}$ film formation in the absence of additives is discussed below. Yokoi [4] describes the role of Cl^- ion in electrodeposition with the establishment of a quasi-reversible Cl^- adsorption reaction that further facilitates the reduction of Cu^+ ions to Cu_{ad} or reversibly the dissolution of Cu_{ad} to Cu^+ at the surface. Essentially in the presence of Cl^- and at operating potentials positive than -0.1V Vs SHE. it's been proven that there is an ordered adsorption layer of Cl^- formed on the surface for both deposition and dissolution reversible reactions. At potentials below -0.1V the fast movement of Cl^- ions is considered as a disordered adsorption rate. Nagy Z *et al* [28] have

demonstrated that the Cu^{2+} ions present on the metal - solution interface coordinate with Cl^- adsorbed on the copper surface to reduce to Cu^{1+} [45]. With reduced concentrations or in the absence of Cl^- ions in the electrolyte, irregular nodular growth happens across the surface. Kondo *et al* [30] have shown that the formation of the Cu(I)Cl is critical for super fill mechanism. $CuCl_{ad}$ species complex with polymer additives that are added to enable super fill and facilitate their adsorption on the surface. Hayase *et al*[9] have also shown experimentally that consumption of Cl^- happens during the reduction of Cu^{2+} ions. For electrolytes operating with very low concentration of Cl^- this consumption could lead to diffusion limitation at the via bottom than at the via top.

Section 3.5 Organic components in copper electrodeposition

Almost in all cases, copper electrodeposition for electronic applications includes the presence of an organic additive mixture in the electrolyte. Organic additives are added to the plating bath to enhance / suppress the growth rate of copper in features relative to the planar surface. Figure 3.3[3] shows the effect on deposition current (deposition rate) when additives are present. Chemicals which act to increase the current at a given voltage namely the accelerators and the other class of molecules that act to reduce current at a given voltage are termed the suppressors / leveler comprise these polymeric additives.

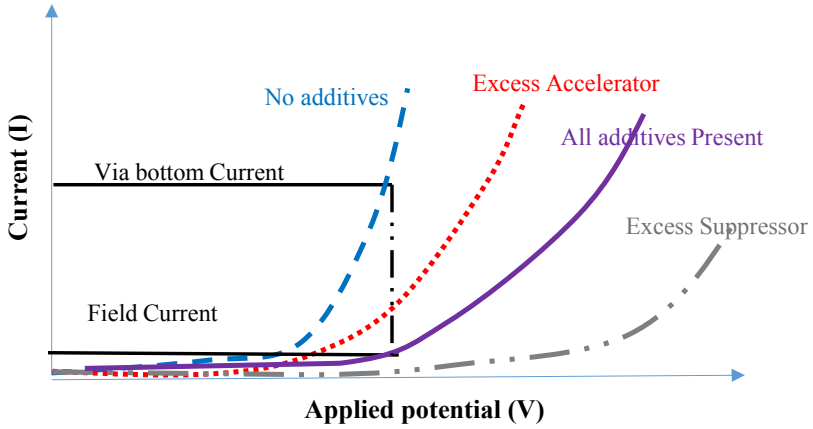

Figure 3.3: Schematic to show the effect of additives on deposition current[3]

Differential deposition is enabled with the concurrent addition of large molecular weight suppressor and fast diffusing accelerator molecules. Strongly adsorbing suppressor molecules can inhibit / reduce deposition rate at the top of via (as they are diffusion limited to reach via bottom) while the accelerator molecules promote accelerated copper growth from via bottom. Competitive adsorption and reaction of these species on the copper surface enables enhanced differential copper deposition with higher rate at the bottom of via relative to the suppressed deposition rate on the planar surface (top of the via) and the upper side walls of the features. Leveler molecules are added to offset the accelerated growth effect provided by the accelerators and to fine tune deposition uniformity. For copper IC packaging applications the true nature and concentration of the additive components remains largely proprietary and a closely guarded secret. A large amount of scientific literature spanning since 1950[2-47] for gap fill have identified a typical set of additives that exhibits superfilling. We will further look into the typical makeup of these molecules and their principle role in copper electrodeposition.

Section 3.5.1 Suppressors

Suppressors [13, 27, 25, 31, 32,35,36, 38] are long chain, large molecular weight polymers that are water soluble. Typically, polymers such as polyethylene glycol (PEG) or polypropylene glycol (PPG) or their copolymers [27,] are utilized as suppressors as shown in Figure 3.4

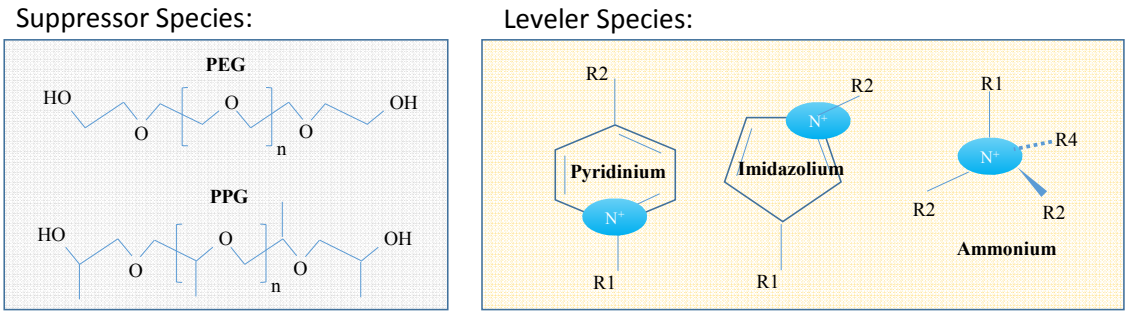

Figure 3.4: Example of Suppressor and Leveler molecules utilized in copper electrodeposition

These molecules suppress Cu^{2+} ion reduction by adsorbing and blocking the metallic surface that are normally available for Cu^{2+} reduction. The adsorption of the suppressor is mediated through a $CuCl_{ad}$ film on the surface as shown in reaction 3.5 below [6].

$$\boldsymbol{nCuCl_{ad} + HO\,((CH_2)_xO)_y\mathrm{H} \rightleftharpoons}$$

$$\boldsymbol{[\mathrm{HO}((\mathrm{CH_2})_xOCuCl)_n\,((CH_2)_xO)_{y-n}\,H]_{ad}} \qquad \textbf{(3.5)}$$

Essentially the suppression of these molecule is enabled due to the formation of a dense layer of the complexed species (identified in reaction 3.5) at the interface that is facilitated by the presence of adsorbed Cl^- to the copper surface. The Cu^+ ion that is ionically binded to the Cl^- on one side is attached to the oxygen atom of the suppressor molecule as shown in simulated model by Feng *et al*[40] in Figure 3.5. These adsorbed

species adsorb and desorb on top of the freshly formed copper surface during the copper deposition without being incorporated in significant amounts[30]. The adsorbed layer act as diffusion barriers physically limiting the access of cupric ions and other additives (e.g., the "accelerators") to the copper surface. These adsorbed species are eventually knocked off by the accelerators depending on the local current density due to the competitive adsorption of the accelerator molecules causing desorption. Boeckmann *et al* [31, 32,35,36] have categorized suppressor activity according to their interaction with SPS (bis(3-sulfopropyl) disulfide) by performing various potential transient measurements.

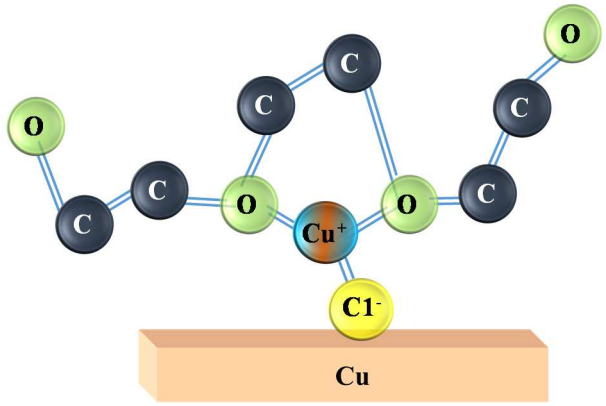

Figure 3.5: Model of PEG - Cu^{+}- Cl^{-} complex with the Cu^{+} ion attached to the oxygen atom of the PEG and the Cl^{-} adsorbed on copper surface

In the absence of Cl^{-} any adsorption of suppressor molecule to block the deposition process is unlikely. As discussed before formation of Cl^{-} adsorbed layer to the copper surface is strictly determined with the applied potential. The adsorption of suppressor is thus related to the applied potential and shown in the Figure 3.6 as a cartoon below.

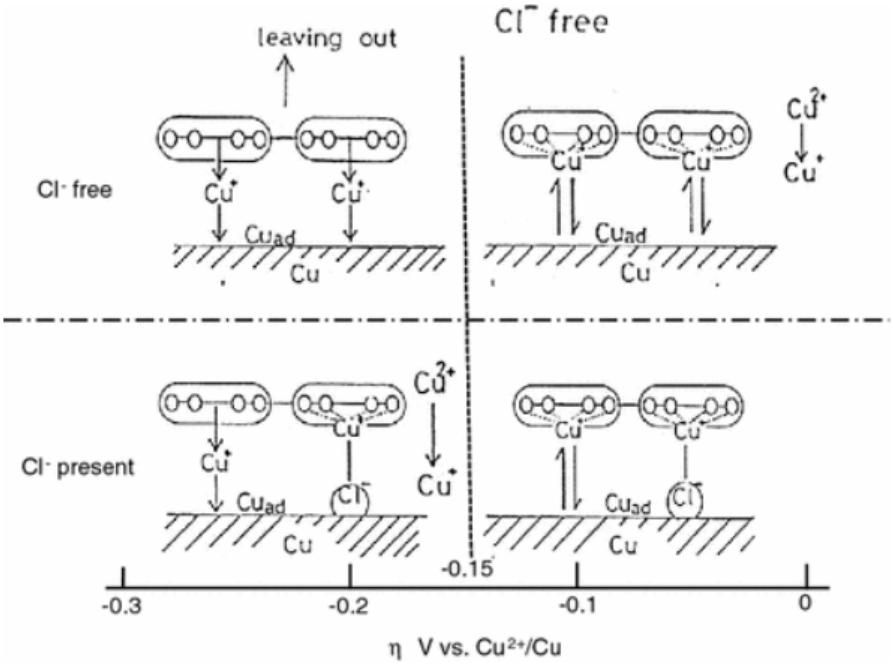

Figure 3.6: Model of PEG - Cu^{+}- Cl^{-} complex with the Cu^{+} ion attached to the oxygen atom of the PEG and the Cl^{-} adsorbed on copper surface as a function of applied potential[4]

The time-dependent interplay of accelerator and suppressor on the non-planar copper electrode surface and their complexation with reaction intermediates leads to the desired gap fill behavior. In the early stage of deposition, suppressor adsorption happens on the surface. However, in order for the deposition process to continue, the blocked surfaces by the suppressors needs to be displaced at some point. The displacement of the suppressor–chloride complex by cuprous thiolate [intermediate formed by accelerator] in the reaction shown below in equation 3.6 is likely the equivalent of the competitive adsorption of suppressor and accelerator species[6].

$$[\boldsymbol{HO}\,((\boldsymbol{CH_2})_x\boldsymbol{OCuCl})_n\,((\boldsymbol{C}\mathbf{H_2})_x\boldsymbol{O})_{y-n}\,\boldsymbol{H}]_{ad} + \mathbf{nMPS} \rightleftharpoons$$

$$[\mathbf{HO}((\mathbf{CH_2})_x\boldsymbol{O})_y\,\boldsymbol{H} + \boldsymbol{nCl^-} + \boldsymbol{nCu(I)(thiolate)}_{ad} \quad \textbf{(3.6)}$$

The makeup of accelerator molecule and the formation of cuprous thiolate that facilitates suppressor removal is discussed further.

Section 3.5.2 Accelerators

Accelerators[6,7,17,37,43] are usually molecules of smaller size (compared to Suppressor) and are usually fast diffusing species. In the presence of Cl^- adsorbed on the surface, accelerators increase the current density or the deposition rate on the copper seed surface. Almost in all cases, a sodium salt of bis(3-sulfopropyl) disulfide (SPS) or its reduced monomer, 3-mercaptopropylsulfonate (MPS) are utilized as accelerator for copper electrodeposition. Figure 3.7 shows the chemical structure of the SPS & MPS molecules [37]. As shown there, these molecules are characterized by the presence of the sulfonate functional group ($R\text{-}SO_3$) and the sulfur–sulfur disulfide bond ("S-S") in SPS and the thiolate (R -SH) group in MPS. These groups play a critical role in the acceleration mechanism. Accelerator reactions are very complex due to the formation of various intermediates and byproducts. Some of those studied reactions are discussed further in the discussion of via fill mechanism below. In general, copper has strong affinity for sulfur "S" and the (–C–S–S–C–) portion of the molecule is believed to interact with the copper surface and result in strong adsorption. While on the copper surface, SPS and MPS form a super accelerating Cu (I) thiolate species that eventually is reduced to Cu regenerating the SPS and MPS molecules. This regeneration helps preventing the

incorporation of accelerator molecule inside the film. However, accelerator molecules do get consumed in the course of the reaction due to the formation of irreversible byproducts that eventually needs to be drained. Thus, reducing the life of the bath in an industrial scenario.

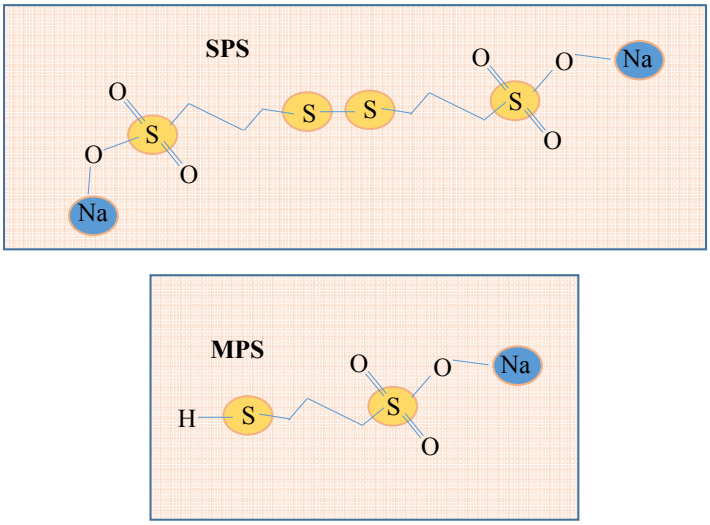

Figure 3.7: Chemical structure of the SPS & MPS molecules that are utilized as accelerator.

As previously explained in the absence of any applied potential at OCP, Cu^{1+} intermediates are readily formed due to the interaction of Cu metal surface with Cu^{2+}. These Cu^{1+} intermediates can interact with accelerators even at OCP react to form Cu(I)thiolates. Various redox reactions involving SPS / MPS at OCP are shown in reactions 3.7a – 3.7d below.

$$\boldsymbol{Cu^{2+} + Cu \rightleftharpoons 2Cu^{+}} \quad \textbf{(3.7a)}$$

$$\boldsymbol{2Cu^{+} + SPS + 2H^{+} \rightleftharpoons 2Cu^{2+} + 2\ MPS} \quad \textbf{(3.7b)}$$

$$\boldsymbol{4Cu^{+} + SPS \rightleftharpoons 2Cu^{2+} + 2Cu(I)thiolate} \quad \textbf{(3.7c)}$$

$$2Cu^{2+} + 4MPS \rightleftharpoons 2\text{Cu(I)thiolate} + \text{SPS} + 4H^{+} \quad \textbf{(3.7d)}$$

Verckeen *et al* [6] captures a more complex set of reactions involving SPS/ MPS with Cu^{1+} and other surface intermediates that eventually lead to the formation of either Cu(I)thiolate or $Cu(I)(thiolate)_{ad}$. Discussion on each of those reactions is beyond the scope of this work. With an applied potential, in the presence of applied electric field, the thiolate group acts as super accelerating species and reduces to Cu as shown in equation 3.8a – 3.8h below. [6,43]

$$Cu^{2+} + e^{-} \rightleftharpoons Cu^{+} \quad \textbf{(3.8a)}$$

$$Cu^{+} + e^{-} \rightleftharpoons \text{Cu} \quad \textbf{(3.8b)}$$

$$Cu^{2+} + 2e^{-} \rightleftharpoons \text{Cu} \quad \textbf{(3.8c)}$$

$$Cu^{2+} + Cl^{-} + e^{-} \rightleftharpoons CuCl_{ad} \quad \textbf{(3.8d)}$$

$$CuCl_{ad} + e^{-} \rightleftharpoons Cu + Cl^{-} \quad \textbf{(3.8e)}$$

$$Cu^{2+} + \text{MPS} + e^{-} \rightleftharpoons Cu(I)(thiolate)_{ad} + H^{+} \quad \textbf{(3.8f)}$$

$$Cu(I)(thiolate)_{ad} + H^{+} + e^{-} \rightleftharpoons \text{Cu} + \text{MPS} \quad \textbf{(3.8g)}$$

$$SPS + 2H^{+} + 2e^{-} \rightleftharpoons 2\text{MPS} \quad \textbf{(3.8h)}$$

In all cases discussed above, there is a strong interaction of SPS / MPS species with Cu^{1+} / Cl^{-} ion on the surface[52, 34]. Potentiostatic experiments performed by Tan *et al* [52] show that in the absence of any Cl^{-} ion present in the electrolyte, accelerators behave as suppressors. This has been previously confirmed in other studies as well [17]. Besides

thiolates, Schultz *et al*[53] reported formation of a CuCl-SPS complex with sulfonate group that also has an accelerant effected similar to the thiolate species.

In summary, accelerator molecular family with unique functional groups such as sulfonate and thiols can accelerate copper deposition on a pure copper surface. As discussed in reaction 3.6 they can even displace adsorbed suppressor molecules on other copper surfaces to undergo rapid deposition. However, this rapid deposition needs to be regulated eventually to achieve a planar deposit. This is achieved through the addition of a third additive component termed leveler which is discussed below.

Section 3.5.3 Leveler

Leveler[8, 19, 33, 38,47] are actually a type of suppressor molecule that are charged. Typically, these molecules are nitrogen-containing cationic organic additives and are utilized in polymeric or sometimes in monomeric form. Examples of typical leveler molecules are shown in Figure 3.4. Levelers regulate super-fill and play an important in the later stage of copper deposition process to enable a uniform deposit. In the present work the effect of leveling agents is not discussed any further.

Section 3.6 Via fill mechanism with organic additives in copper electrodeposition

Various models have been developed by researchers to explain the competitive interaction of these organic additives that enables void-free fill [5,14 -16,26]. The validity of the model and the mechanism varies based on feature size and the type of application that

they are intended. For large feature applications, in the early 2000, diffusion adsorption model was utilized to explain super fill with the polymer additives. [5,14]. In this model a single additive agent (suppressor) was utilized to explain the via fill mechanism. In the earlier case, in the absence of any additives with copper electrodeposition, establishment of a large diffusion region inside the via. If the copper electrodeposition proceeds such that the operating current density (applied potential) is well below diffusion limitation, then the reduction of cupric ion will happen under kinetic regime rather than in diffusion limited regime. In that case, if a strongly adsorbing, large molecular weight suppressing species is added in dilute amounts such that the consumption of suppressor becomes mass transfer limited then a diffusion layer is established for the suppressor species from the bulk of the solution to the top and bottom of the non-planar interface (Via top, for example). This enables differential suppression with more suppression at the top of the feature compared to the bottom due to the adsorption of the suppressor. This phenomenon enables the via bottom to plate at a faster rate than the via top to enable bottom-up fill.

In summary, with this mechanism, the amount of polarization / suppression is varied along seed surface creating different deposition rates and overpotential along the surface of the via sidewalls. While this mechanism could explain the inhibition kinetics of copper deposition to initiate differential plating in a non-planar surface very well, extrapolation of the model to larger current density applications and extension to longer process time in the presence of accelerator along with suppressor that leads to momentum plating and rounded growth on top of the via sidewalls that eventually causes a bump formation (Figure 8e, for example) was largely absent.

Later, Reid and West *et al* [26], refined the model and explained this rapid growth in via bottom by taking into account the phenomenon of accumulation of accelerator species at the via bottom at the corners. The selective accumulation of accelerator in the via bottom was correlated to the presence of increased surface area at the corners of the via bottom. Suppression adsorption observed only at the via top was correlated to diffusion limitation at the bottom of the feature. Elimination of bumps at the end of the process was explained to the accumulation of Leveler. Reid's trench fill mechanism is shown in Figure 3.8[3].

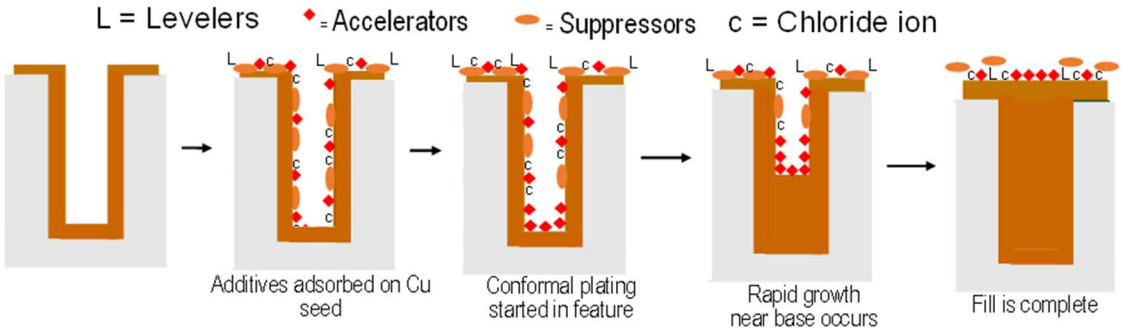

Figure 3.8: Via fill inside a trench feature with time evolution[3]

In the similar time frame, Moffat *et al*[16] proposed the popular "curvature-enhanced accelerator coverage" or CEAC model. This model is widely accepted in the scientific world and has a similar approach as Reid and West [3,26] . It is also defined based on accelerator accumulation at the via bottom to explain the bottom-up fill. This mechanism utilizes a competitive adsorption between the accelerator and suppressor molecules [23]. As Moffat[16,18,22,23,39,54] explains, the key factors involved in detailing CEAC mechanism includes the growth velocity (deposition rate) that is proportional to the local coverage of the accelerator on the surface and the fact that accelerator remains segregated (not

lumped) at the metal/electrolyte interface during deposition. For growth inside via / trench features, this phenomenon is explained to the enrichment of the accelerator on advancing concave surfaces (corner of trench / via bottom) and dilution of the coverage of accelerator on convex sections (corner sections at the top of the via). This capability leads to distinct bottom-up filling of via / trench features. Furthermore, the enrichment and dilution processes continues to be dynamic as the via filling process proceeds necessitating a continuous change in accelerator / catalyst coverage based on the inside surface area and further enabling the localized accumulation of accelerator. This highly localized concentration of accelerator species leads to displacement of adsorbed suppressor species and allowing the via fill process to continue further. Moffat's experimental and simulation data to explain CEAC-based bottom-up trench filling as applied to copper electrodeposition is shown in Fig. 3.9[22].

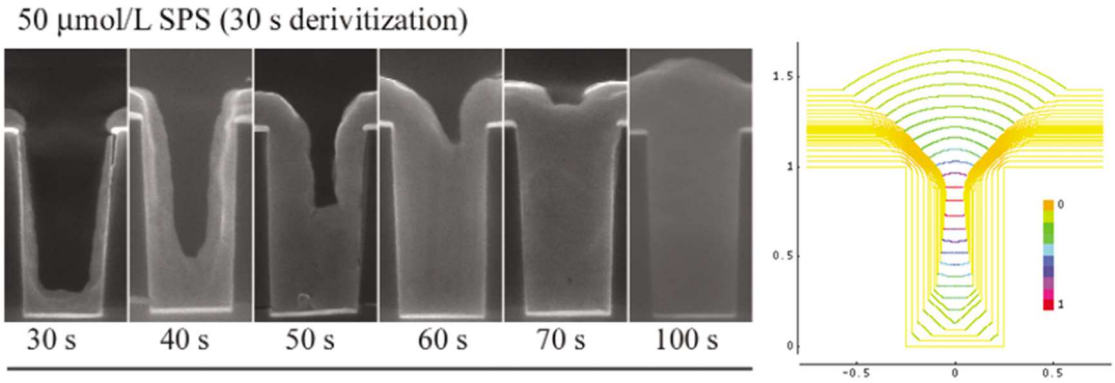

Figure 3.9: Super Filling of trenches obtained by Moffat *et al*[22] with accelerator pretreated surfaces prior to copper plating in a PEG-Cl electrolyte at –0.25 V. Simulation of super fill by depicting catalyst coverage with a SPS derivatized 0.5um wide trench during copper deposition from an acid copper sulfate electrolyte containing PEG-Cl is shown on the right (experimental and simulation results from Moffat *et al)*[16,18,22, 39,54].

Experimental and simulation of super fill by Moffat *et al* [16,18,22, 39, 54] depicting local catalyst coverage with a SPS derivatized 0.5um wide trench during copper deposition from an acid copper sulfate electrolyte containing PEG-Cl is shown in Figure 3.9. As shown here, initially, the accelerator is distributed uniformly along the trench profile. Similar to the Reid's proposed mechanism [2,3,26,] the accumulation initially continues in a conformal fashion due to the uniform coverage of accelerator on the side walls. This is followed by enrichment of accelerator on the concave corners and the nearby inclined surface of the side walls. As bottom-up fill continues, further enrichment of accelerator occurs and accelerated growth entails leading to a flat bottom profile. In contrast, the growth velocity on the convex upper corners is mitigated by dilution of the accelerator concentration. As the bottom surface approaches the upper corners, an inversion of curvature occurs and the growth slows as the highly accelerated growth front dilates and forms a bump above the feature. Although this model is widely accepted for via fill mechanism, this model does not taken into account any concentration or convection dependent effects of the additives for long term deposition process.

Later Akolkar *et al*[15,20] extrapolated the effects of suppressor by incorporating transport and adsorption behavior. Specifically, Akolkar and Dubin[12] showed that the rate of the bottom-up growth depends strongly on the short time-scale suppressor concentration field present near the surface using tertiary current distribution models. Later Dow *et al* [42,46] incorporated the effect of leveler utilizing a convection dependent adsorption model.

Section 3.7 Challenges with additive based via fill for IC Substrate applications

Although additive based bottom-up fill approaches are highly suitable for filling microvia's in IC substrate packages, utilization of these organic additives poses other constraints. For example, some of these organic polymer additives are highly unstable molecules and rapidly degrade at high over-potentials or when readily exposed to the anodic surface [48-51]. The breakdown products of these additives tend to be more active in the plating bath than the parent species and disrupt the overall bottom-up fill mechanism. For example, large suppressor species could break down to smaller molecular fragments[3]. These fragmented breakdown products of suppressors tend to be more active in the bath than the parent species due to their reduced size and increased diffusion rate. Electrodeposition in the presence of these fragmented additives then leads to uniform polarization / overpotential, as the fragments tend to inhibit the nucleation sites for deposition uniformly everywhere than just at the via top surface. In most cases irregular adsorption / desorption kinetics happens due to the random nature of the byproduct formation which in turn results in poorly controlled bottom-up fill leading to reduced throwing power and eliminates repeatable stable performance. Similarly, when accelerator molecules break down, some of their byproducts tend to be highly charged metastable species that promote deposition process in a completely different operating regime when compared to the native species. Nodular growth with poor bottom-up fill is observed with such byproducts [48-51].

In order to to sustain the capability of the process and preserve the dynamics of gap fill mechanism with the parent species, the electrolyte needs to be frequently drained

to arrest the accumulation of excess byproducts. This frequent drainage and make up of new chemistry drives high consumption of the organic additives and poses a major cost challenge for IC substrate applications. To mitigate this scenario, it is important to have non-degrading additives or we need to effectively remove the degrading byproducts.

Electrodeposition for IC substrate applications happens in reactor tanks with very large footprint. The reactor includes a stationary plating bath with regular infeed of panels in horizontal / vertical fashion (VCP – Vertical Continuous Plater). Typical bath volume range anywhere from 1000L - 15000L based on the tank design. These large volume tanks were primarily designed in such fashion to enable high factory output with minimal cost. As discussed before, the accumulation of byproducts and their disruptive effect on the overall process capability negates any cost advantage originally realized with those large industrial footprints.

Furthermore, high density substrate packages require both gap fill and uniform copper thickness on the patterned regions in a single manufacturing process step. Uniform deposition in patterned regions is usually attained by increasing the conductivity of the electrolyte. Reid *et al* [2,3] summarize that electrolytes with high sulfuric acid concentrations (>80g/L) are predominantly utilized for PCB (Printed Circuit Board) and damascene applications to mitigate electrolyte resistance effects on thickness distribution. With thick seed layers, (as the sheet resistance is reduced) any reduction in electrolyte resistance enabled with the introduction of high electrolyte conductivity tends to homogenize the electric field and enable uniform deposition across isolated and dense patterned regions of the cathode. Ohmic drop in potential is significantly reduced with

increased electrolyte conductivity. However, the capability of additives to generate bottom-up fill is severely compromised at those very high acid concentrations [3,21,]. High over-potentials generated due to the additive interaction is significantly reduced at high acid concentrations when compared to similar low acid concentrations. As the high density substrate packages necessitate both gap fill and uniform deposition in patterned regions a high acid plating approach without any additive optimization is unlikely to work. There is always a compromise in gap fill performance (throwing power) Vs deposition uniformity in the two different acid regimes. Conversely, these two processes can be carried out independently in two separate plating baths with each chemistry tuned to target the desired fill capability / uniform FLS deposition requirements. Such efforts are least preferred, given the large plating tank footprint in the factory floor and added cost with dual processing. Concentration of the Cu^{2+} ions in the electrolyte needs to be significantly reduced with large increase in sulfuric acid concentrations to prevent precipitation of the copper sulfate crystals in the electrolyte. With reduced Cu^{2+} ion concentrations in the electrolyte, concerns of plating reaction operating in a diffusion limitation regime is likely to occur and could limit the overall current density utilized to drive the plating reaction. In such cases, careful design of reactor geometry with strong agitation profile characteristics needs to happen to reduce the thickness of the boundary layer at the interface. Limitation of the overall current density conversely extends the total deposition time needed to achieve the target fill, leading to reduced factory outputs and additional cost.

Section 3.8 Alternative approaches from additive based via fill

High density packages have fine patterned regions in the scale of 9µm to features as large as 77µm along with many large plane area regions. They are supported with underlying microvia's usually with via opening size 20µm to 100µm and an aspect ratio of 0.5 to 1.5. Enabling void-free gap fill and uniform FLS deposition in a single plating step is beneficial and key for these applications. With the additional capability required with the state of the art systems discussed thus far, concerted new approaches are needed to enable low cost electroplating process for substrate packages. For example, identification of new additive formulations that promotes bottom-up fill at high acid concentrations without compromising deposit uniformity is the easiest approach. Such approach enables single tank processing and guarantees the necessary process requirements for IC substrates. On the contrary, the risks of byproduct accumulation and their detrimental effect on fill still exist with such additive based approach.

Section 3.9 Summary

Clearly there is a strong need to identify a novel solution space where in the the formation of byproduct or the cycle of byproduct generation is systematically disrupted. Such an effort requires basic understanding of factors that cause creation of undesirable byproducts in a plating bath (to enable stability of the additive species). With such capability electrolyte bath life can be extended for a longer time period and consumption of the additives can be significantly reduced. Alternatively, a much straightforward approach would be to enable bottom-up fill and uniform deposition in the absence of

additive species. In the absence of any byproducts generated in the electrolyte, concerns of byproduct effect on fill is eliminated with such approaches. The process operates in a stable state along the life of the bath. However, the via fill capability still needs to be achieved with the incorporation of innovative methodologies / concepts. Alternative approach could include finding additional methods to augment the bottom-up fill mechanism for gap fill even in the presence of additive break downs. In tandem with organic additives, these additional process knobs could offset for reduced gap fill with the break down products and continue to show sustained high quality, reliable process. Chapter IV introduces one such approach utilizing reverse pulse plating methodology. In reverse pulse mode, the cathodic current is pulsed to enable bottom-up fill in the absence of any additives. Presence of additives could further augments this bottom-up fill mechanism. In Chapter IV reverse pulse methodology is introduced. The advantages and the mechanism of reverse pulse methodology for gap fill is further discussed.

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CHAPTER IV

REVERSE PULSE DEPOSITION METHODOLOGY AND PRESENT WORK

This chapter focusses on the application of reverse pulse deposition process to achieve void-free via fill. The impact of reverse pulse current density and durations, the advantages of such process and the underlying mechanism are further elaborated blow.

Section 4.0 Reverse pulse plating, introduction, advantages

In electrodeposition, growth rate of copper is directly proportional to the applied plating current. In (Direct Current) DC plating mode, cathodic current is continuously fed while in pulsed or reverse pulse mode, the cathodic current is applied in short pulses[1,6]. The very first application of pulse plating for copper deposition is traced back to 1981[8] and extension of reverse pulse for through hole fill applications was observed in 1988[9]. Further extension of reverse pulse to PCB applications has been shown by Kobayashi *et al* and Kenny *et al* [7,14] We have also investigated the extendibility of reverse pulse methodology for IC substrate applications as part of this thesis study.[12] Reverse pulse plating has been shown to enable bottom-up fill in the absence of any additives for TSV applications[20]. Presence of additives could further improve the bottom-up fill process [11, 14-26]. Surprisingly, the impact of forward-reverse pulses for bottom-up fill plating has been investigated only in very few literatures since its conception in early days. Primarily these efforts were driven by the work of West *et al* [2-4], Hayase and Kondo *et al*[15-19] and Kim *et al*[21-26]. The effect of pulsed reverse current on the structure and hardness of copper deposits obtained from acidic electrolytes containing organic additives to enable

smaller grain size immediately post plating and grain refinement was shown by Pearson[10] and Hu *et al*[13]

Section 4.1 Reverse pulse mechanism

In the absence of any additives, local plating rate is directly proportional to local cuprous and cupric ion concentration inside the features. Under direct current plating conditions the bottom of the feature sees much lower concentration of the Cu^{2+} ions than the top due to diffusion limitation. Therefore, the average current density (deposition rate) at the top (i_T) remains larger than that of via bottom (i_B) leading to pinch off voids. This mechanism is very pertinent for IC substrate packages as the features have very large feature depths and plating reaction happens for an extended time periods (several minutes / hours) given the large via geometry. Enabling reverse pulse addresses this gap and helps to establish "gap fill". The mechanism of reverse pulse methodology enabling gap fill inside the via in the absence of additives has been under investigation only recently with very few scientific studies to explore the mechanism thus far.

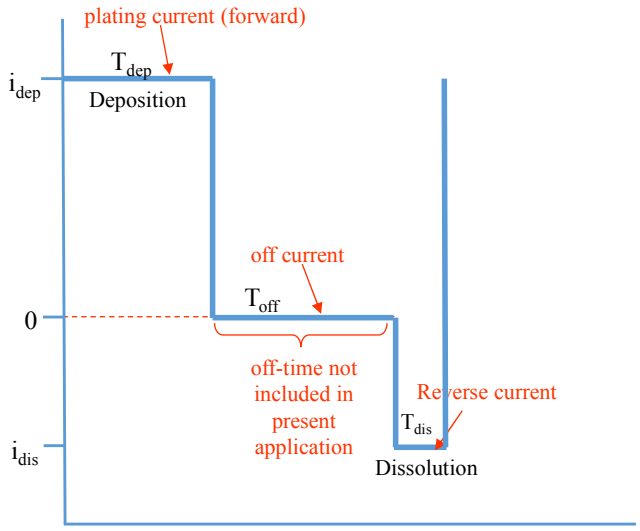

Figure 4.1: Schematic of forward, off current and reverse pulse waveform

Section 4.1.1 Reverse pulse mechanism – Addition of "Off " pulse

As discussed before, for deposition reactions happening at high enough current density, the local plating rate inside feature is proportional to concentration of local Cu^{2+} ion concentration. During forward reaction, application of forward pulse (i_{dep}) for a duration of T_{dep} , the bottom of feature is likely to see lower concentration of Cu^{2+} species than the via top which has a higher Cu^{2+} concentration that are readily supplied from the bulk of the solution leading to pinch off voids. Plating at lower average current densities decreases this difference but still $i_B < i_T$ remains. However, when an off time is enabled post a forward current as shown in the cartoon for a duration of T_{off}, there is no consumption of Cu^{2+} either at the top / bottom of the via during this off time period. However, during this offtime period (T_{off}) replenishment of the Cu^{2+} from the bulk solution to the via bottom region (which is starved of Cu^{2+}) is likely to happen, mainly due to diffusion considerations. If the duration of offtime is set such that $T_{off} > t_D$ where

t_D is defined as required diffusion time of Cu^{2+} , then the via bottom will be replenished back with enough Cu^{2+} and can continue electrodeposition such that it is no longer diffusion limited. This simple incorporation of an off time would allow the sidewall of the via bottom to now plate at the same rate as sidewall of the via top which enables a maximum throwing power of 1. A schematic of the above discussion in off-pulse mode is shown in Figure 4.2. However, the choice of "off-time" poses certain constraints. The maximum throwing power with an off time induced process cannot be greater than 1. Furthermore, the duration of the off time process needs to be such that it is much higher than the time needed for diffusion to the via bottom such that those regions are not Cu^{2+} starved (T_{off} needs to be greater than t_D) . Normally, this diffusion time is directly proportional to the length of diffusion which in our case translates to the depth of the via. In the absence of strong additives, it is mainly the large relaxation time (diffusion time) needed for the ions to reach the bottom of via. As an example, a feature that has a depth of ~25µm likely has a diffusion time (t_D) that is order of a few second as shown in Table 4.1.

Table 4.1: Estimation of diffusion time with ~5.3ASD (A/dm^2 or Ampere per Square Decimeter) deposition for Via0 feature geometry

Ion	D (cm^2/s)	h (cm) = depth	t_D (s)
Cu^{2+}	7.2E-06	0.0025	0.87

For a feature that has a depth of ~70μm this duration is likely much longer. Therefore, a frequent interruption in the deposition process happens with an off-time induced methodology and this in-turn extends the overall process time and limits the factory output and adds overhead cost.

In summary, incorporation of an off pulse helps to improve throwing power but other limitations persist. Optimal fill results (max i_B/i_T) can only be obtained when the pulse durations match diffusion time which are determined based on feature depth, meaning $T_{FWD} = T_{OFF} \sim t_D$. Careful considerations of other critical parameters such as agitation, choice of bulk concentration of copper, operating current density all play a significant role in the appropriate choice of the off-time duration to prevent diffusion limited deposition at the via bottom. If T_{FWD} is much larger than t_D, most of the deposition at the via bottom happens in a depleted Cu^{2+} ion state as shown on the left cartoon on Figure 4.2. This condition leads to smaller i_B/i_T ratio (throwing power) that eventually leads to voids. If T_{OFF} is too short, bottom of feature is not replenished with adequate Cu^{2+} ions and leads to void entrapment as well.

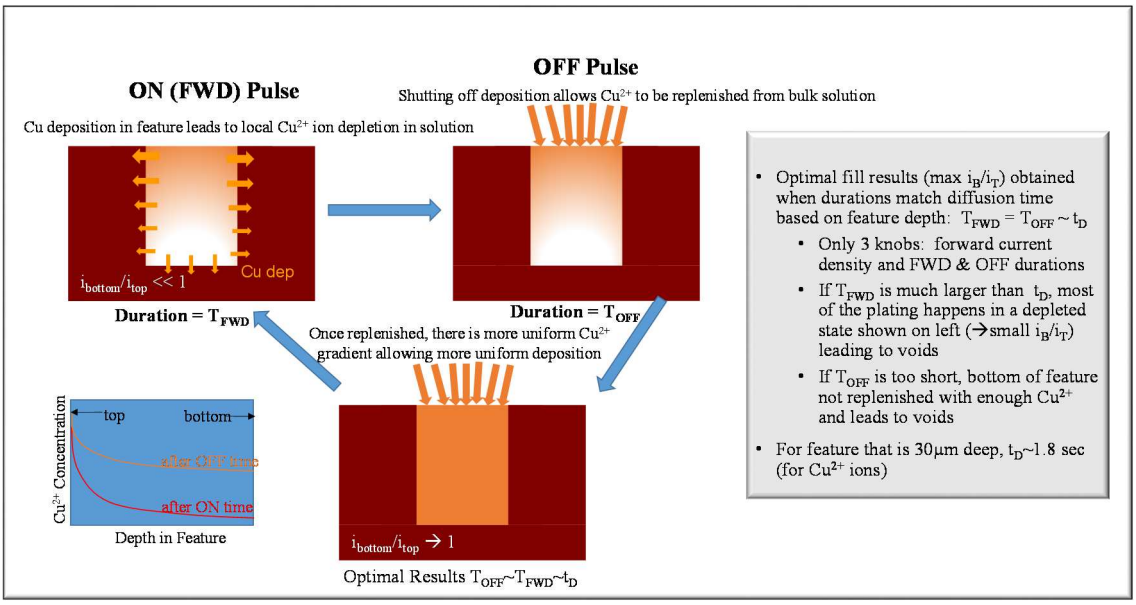

Figure 4.2: Schematic to explain via fill with an incorporation of off pulse during deposition

Section 4.1.2 Reverse pulse mechanism – Addition of "Reverse" pulse

As explained earlier, during forward reaction when the application of forward pulse (i_{dep}) happens for a duration of T_{dep}, the bottom of feature is likely to see lower concentration of Cu^{2+} species than the via top which has a higher Cu^{2+} concentration that are readily supplied from the bulk of the solution leading to pinch off voids. In order to take throwing power >>1 and eliminate the constraint of dependence on t_D, incorporation of reverse pulse into a forward waveform is proposed. When a reverse pulse for a duration of T_{REV} is enabled post a forward pulsed current as shown in the Figure 4.1 for a duration of T_{REV}, there are multiple mechanisms that happens in parallel as shown in Figure 4.3.

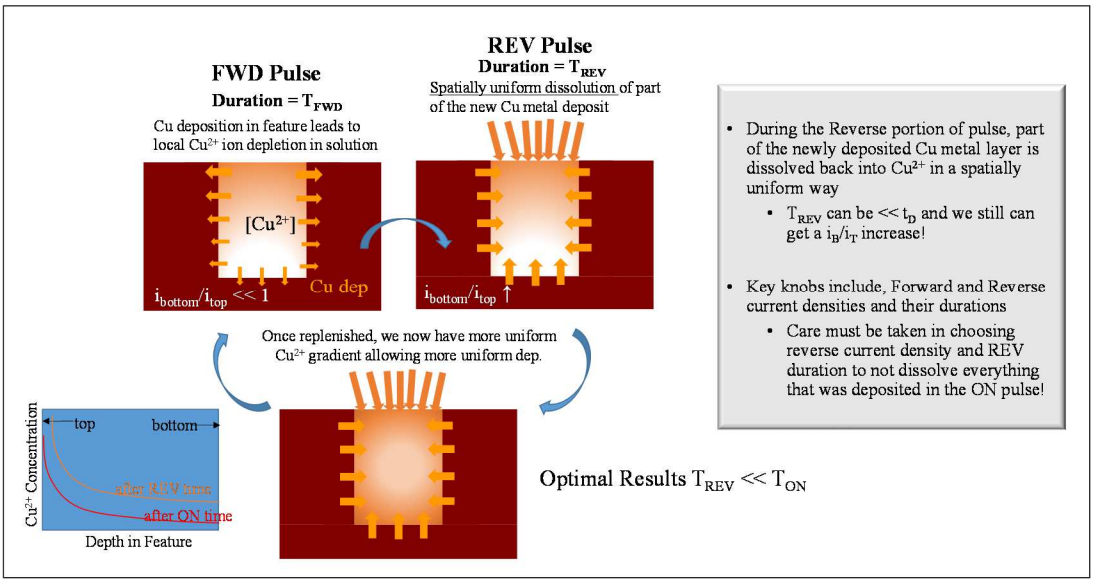

Figure 4.3: Schematic to explain via fill with an incorporation of Reverse pulse during deposition

To begin with, there is no consumption of Cu^{2+} either at the top / bottom of the via during the reverse pulse duration. Secondly and more importantly, during this reverse pulse duration (T_{REV}) there is more spatially uniform dissolution of Cu^{2+} ions on the via walls. This replenishment of Cu^{2+} happens uniformly inside the via region due to the dissolution from the freshly deposited metal that just happened during the forward pulse duration.

Due to this replenishment, we now have more uniform Cu^{2+} gradient along both the via top and bottom region which in turn allows both these regions to operate away from a diffusion limited regime. If the forward current density and duration of the forward pulse is carefully chosen such that via bottom is not completely deprived of Cu^{2+} ions during forward deposition, an introduction of reverse waveform at this stage with a carefully devised reverse current density and reverse pulse duration could adequately replenish the via bottom region with Cu^{2+} ions enabling the via bottom and sidewall

regions to plate at the same rate as via top region. As discussed before, for IC substrate applications, the diameter of the via opening is always larger at the via top than at the via bottom due to the inherent nature of the LASER drill process that enables these geometries. For such geometry, a uniform plating on the sidewall could be enough to prevent the propensity of pinch-off voids or side wall collusion at the top of the via before the via bottom fill ups that could eventually lead to void entrapment. The advantage of reverse pule methodology over an "off-time" process is in that the duration of reverse pulse can be set such that T_{REV} can be << t_D and the via bottom could still be adequately replenished with Cu^{2+} ions to prevent pinch off at the via top.

Recently Hayashi *et al* [16,18,19] also reported that reverse pulse enables differential distribution of Cu^{1+} at the top and bottom of via which enables the via bottom region to plate at a much faster rate than the via top leading to very high throwing power for through mask applications. We had discussed earlier that Cu^{2+} reduction to Cu metal is a two-step process with the formation of Cu^{1+} intermediate. In order to establish a higher throwing power, Hayashi argues that reverse pulse plating enables a differential distribution of Cu^{1+} inside the via region. During the application of the reverse pulse waveform which immediately follows a forward pulse deposition step as show Figure 4.1, dissolution of Cu from the metal surface is likely to happen generating excess Cu^{1+} species rather than Cu^{2+} species. Hayashi *et al*[16,18,19] explains and validates that the concentration of this excess Cu^{1+} generated during reverse pulse is much more at the via bottom than via top.

In order to develop a reverse pulse methodology for bottom-up via fill and to electrodeposit copper, other plating process parameters needs to be carefully designed and optimized and their operating window needs to be taken into consideration to ensure a capable deposition process. We will briefly look into the some of those considerations now.

Section 4.2 Considerations with reverse pulse waveform - mass transfer limitation (Cu^{2+} Concentration)

Incorporation of Reverse Pulse waveform enables the plating process to happen at a much higher overall deposition rates than with traditional forward current only deposition process. In the choice of this waveform, adequate care must be taken with reactor and process design such that the system operates far away from diffusion limited current density. Namely, the the proximity of i_{AVG} (the average current density accounting for the forward and reverse condition) to the mass transport limiting current density (i_L) for a given system needs to be avoided. Feature length scales and reactor design and the electrolyte concentration determine the functionality. For example, IC substrates are comprised of relatively large features (20µm to 100µm depth) with an aspect ratio of 0.5 to 1.5. Gap fill of such large geometry require plating time scales in the range of several minutes to few hours. With large feature depth and increased deposition times, mass transfer transfer limitation of cupric ions can occur and constrain the deposition process. For example, throwing power inside the feature is calculated as a ratio of the deposition rate at bottom (i_B) to deposition rate at top (i_T). For Cu^{2+} reduction, this is calculated as,

throwing power (i_B / i_T). The magnitude of this ratio is also a function of the average applied current density i_{app} on the cathode. Therefore, we can indicate the throwing power (i_B/i_T) as function of limiting current density function (i_{app}/i_L). The larger the i_{app}/i_L ratio, the more likely the feature is depleted of Cu^{2+} ions at via bottom. Therefore, smaller the throwing power (i_B / i_T). The relation of mass transport limited current density to bulk Cu^{2+} concentration is given by the Levich equation[5],

$$\boldsymbol{i_L = 0.62nFD_i^{\frac{2}{3}}\omega_i^{\frac{1}{2}}\vartheta_i^{\frac{-1}{6}}C} \quad \textbf{(4.1)}$$

Where, i_L is the Levich current density (mass transport limited current density), n is the number of moles of electrons, F is the faraday's constant, D is the diffusion coefficient, ω is the angular rotation rate of the electrode, ϑ is the kinematic viscosity and C is the bulk concentration of the Cu^{2+} ions. Therefore, as the bulk concentration of copper is increased, the magnitude of mass transport limited current density also gets larger. At large Cu^{2+} bulk concentrations with same applied current density (i_{app}), the ratio of i_{app}/i_L is now reduced indicating a better margin for throwing power (i_B / i_T). Even though i_B / i_T cannot be increased to >1 with increase in just copper electrolyte concentration without the addition of additives or reverse pulse, such transition is likely to buy more margin and enable the system to operate in a more benign regime with throwing power ~1. Therefore, large Cu^{2+} bulk concentrations enables less Cu^{2+} depletion inside the via and smaller propensity of voids. The mechanism discussed above was numerically simulated and verified by West *et al*[3,4] to correlate throwing power to the ratio of i_{app}/i_L for various diffusion length scales. Therefore, careful consideration of agitation profile, electrolyte flow, and electrolyte concentration needs to happen to ensure there is adequate supply of

bulk concentration of Cu^{2+} ions to drive the reduction reaction at via bottom. Previous studies have already shown that low Cu^{2+} ionic concentration in the electrolyte and poor agitation are likely to impact gap fill even with DC plating process[1]. Plating at lower current densities can alleviate some of this difference but still $i_B < i_T$ condition is likely to persist even in those cases.

Section 4.3 Considerations with reverse pulse waveform - flash plating

The incoming surface layer is a thin layer of copper seed. Prior to the application of the reverse pulse this seed layer needs to be protected such that the thickness of the seed layer is increased and seed dissolution during the early stage of deposition is prevented.

Seed dissolution during early stages of deposition will prevent electrical continuity along the via surface and pose other unintended risks and challenges to the via fill process. Copper dissolution on the cathode surface will occur during reverse pulse time periods. Therefore, seed dissolution can also occur early in the plating process when operating under strong reverse pulse plating conditions. Utilization of strong pulse amplitudes early in the deposition stage can exaggerate the dissolution behavior leading to excessive seed dissolution and discontinuity of the deposition process. Therefore, a flash plating step with direct current or reduced reverse charges is always performed before the introduction of a strong reverse pulse early in the process to increase the thickness of the incoming seed layer. Separately, when reverse pulse deposition happens in the presence of additives, careful consideration of anode material, anode and reactor

geometry, bath temperature needs to happen to protect against any detrimental effect of byproduct formation.

Section 4.4 Considerations with reverse pulse waveform - momentum plating

As discussed earlier, high throwing power could be established with the reverse pulse plating process during the reverse charge periods. IC substrates have large via sizes that require a strong reverse pulse waveform with high reverse charge to enable bottom-up fill. In the absence of strong leveler or other additive species to arrest the accelerated growth of copper, bottom-up fill process is likely to continue uncontrollably leading to a phenomenon termed as “momentum plating”. Momentum plating is likely to cause non-uniform metal deposit across finely patterned regions. Given the need of uniform FLS deposition in conjunction with gap fill, optimization of reverse pulse waveform to arrest momentum plating and enabling uniform deposition is necessary.

Section 4.5 Summary

In summary, given the advantage of a large throwing power and the ability to generate a bottom-up via fill, reverse pulse methodology seems to be an attractive approach for IC substrate applications. Incorporation of reverse pulse duration on the order of milliseconds to a process that operates for few minutes / hours should have minimal impact to the overall process duration that otherwise happen with forward current deposition only. Furthermore, this methodology could also be extended to various via sizes and aspect ratios, a key element of IC substrate stack-up. In the following chapter

(chapter V) we will discuss how a how a test coupon is fabricated for this study. Chapter V will further discuss the methodology and preparation of IC substrate samples with various via geometries for this study. Discussion of the experimental set up conditions that are utilized for the application of reverse pulse methodology along with the design of experiments that was planned and executed to evaluate the gap fill behavior is discussed.

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CHAPTER V

EXPERIMENTAL SETUP AND DETAILS

Section 5.0 Design of test coupons

A test coupon as shown in Figure 5.1 was generated utilizing a standard process flow well known for packaging substrate architectures[1]. A roughened blanket Copper Clad Film (CCL) after sonication in deionized water was utilized as a base layer and a layer of dielectric film was laminated on top. The film was subsequently cured post lamination. Desired via opening inside the dielectric film was then established with a LASER drill process.

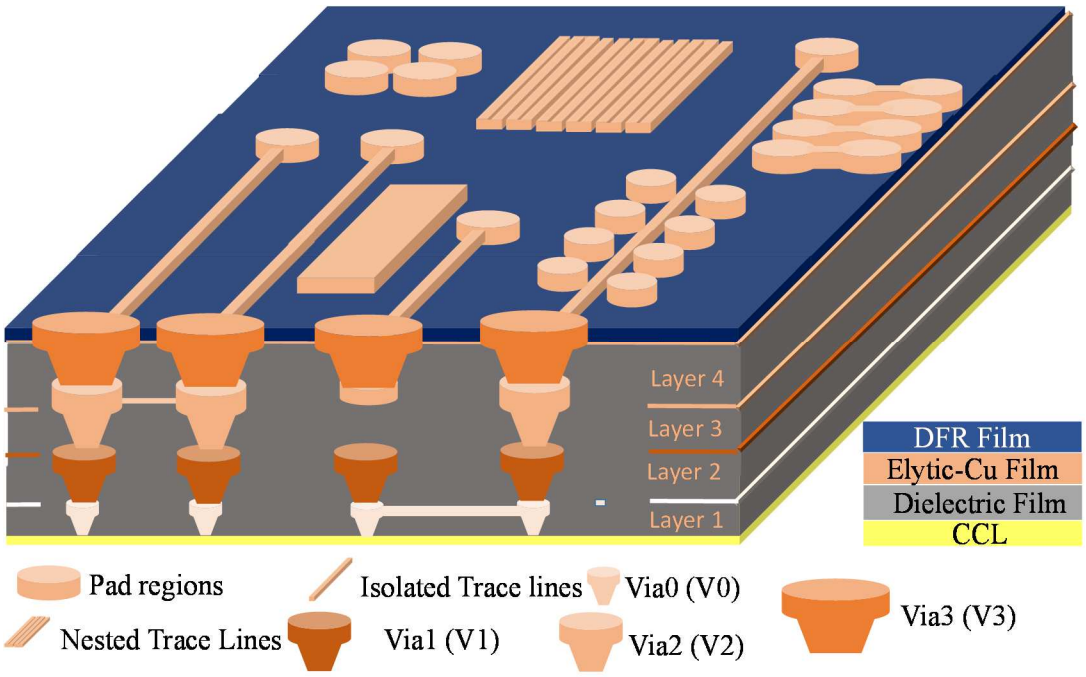


Figure 5.1: Schematic of test coupon with electrodeposited copper along with a patterned resist film and an underlying via stack.

Post roughening and cleaning of via surface, an electroless copper seed layer with an average seed thickness of 0.7µm ~1.0µm was then deposited. After annealing the Cu seed and a mild acid clean, a dry photoresist film (DFR) was laminated. The photoresist film was then exposed and developed to establish the fine line pattern circuitry. These DFR and LASER defined coupons were then utilized for plating evaluation. Prior to copper deposition, exposed copper density post patterning was verified to be in the range of ~40% for the bottom stack layer and ~70% for the subsequent top metal layers. A thorough plasma clean inside an oxygen chamber and an acid clean in 10% sulfuric acid was always performed before each plating experiment. The process flow utilized in generation of the test coupon for each of the experiments is shown in Figure 5.2.

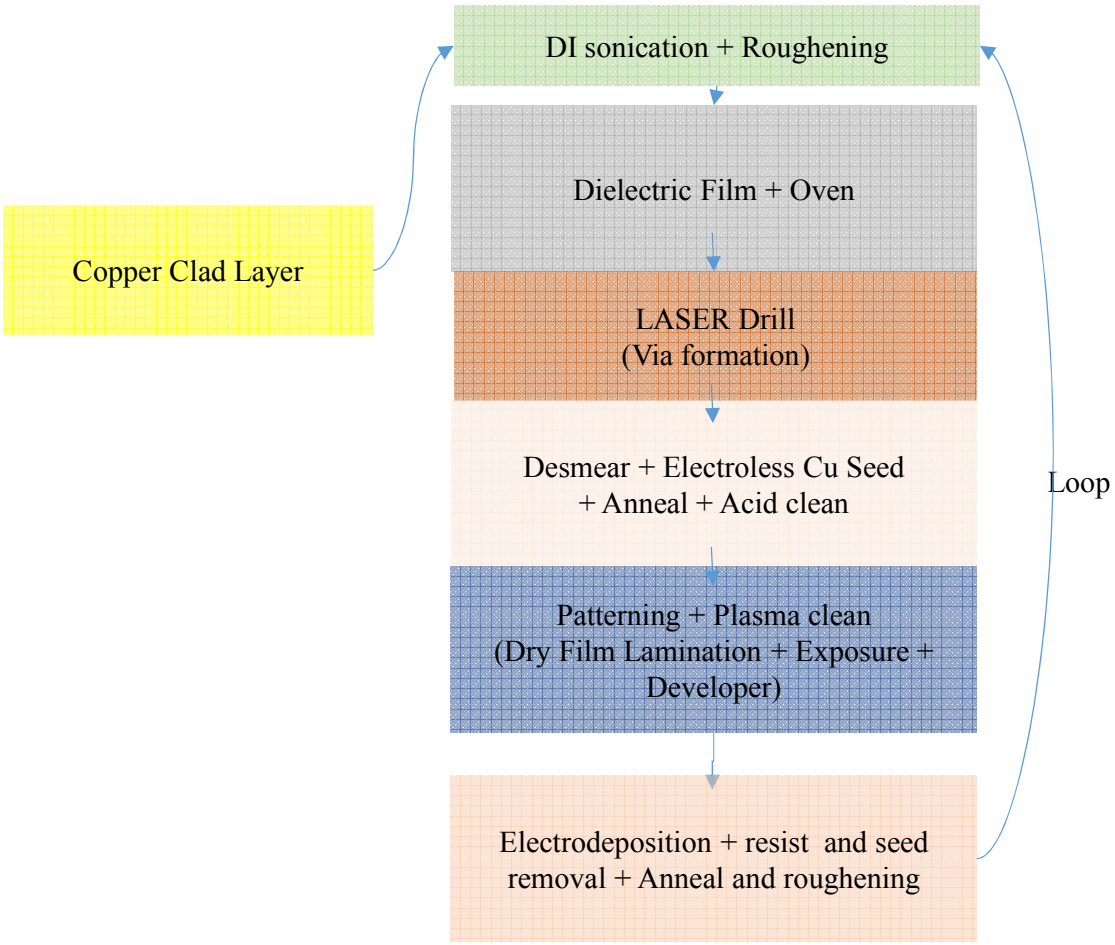


Figure 5.2: Process flow for test coupon generation

Some of the process steps were looped as shown in Figure 5.2 to establish additional layer of interest to generate a stacked via.

Section 5.1 Discussion of via geometries and pattern features for this study

Table 1 summarizes via geometries and line space dimensions studied of each layer with the test coupon. The bottom via layer generated on the copper clad layer is referred to as via0 or V0 and the corresponding bottom metal stack layer is referred as Layer1 (white

colored features shown in Figure 5.1). The via dimensions for this layer are captured in Table 5.1 For example, plating process happens to fill both Via0 and uniformly deposit patterned regions of Layer1. Although the final package included a four layer stack, in order to develop a capable gap fill process for each layer and for quick turnaround of results, short loop process flows were created to study Layer 2 through Layer 4. Each substrate layer has different via geometries and the electrodeposition process for each of those geometries was studied independently. In the creation of short process flows, via geometry of the required layer and their pattern was created rather than building a full stack till that layer. Table 5.1 summarizes via geometries and FLS (Fine Line Space) dimensions studied of each layer with the test coupon.

Table 5.1: Summary of via dimension and FLS structures with the test coupon

Plating Summary	Via bottom diameter	Via Depth	FLS widths studied
V0 / Layer 1	25µm	25 -30µm	9µm, 13µm, 77µm, Planes
V1 / Layer 2	50µm	25µm	9µm, 13µm, 77µm, Planes
V2 / Layer 3	50µm	25µm	9µm, 13µm, 77µm, Planes
V5 / Layer 4	75µm	65µm	13µm, 77µm, Planes

Section 5.2 Experimental setup: reactor setup

Figure 5.3 shows a simplified schematic of electroplating cell utilized for the study. The electrolyte solution was made by dissolving copper sulfate pentahydrate crystals in a

sulfuric acid solution to generate an initial inorganic concentration of 25g/l Cu^{2+}, 80g/l H_2SO_4 and 50ppm chloride and 1g/l Fe^{3+}. Oxidation of Fe^{3+} to Fe^{2+} as shown in Figure 5.2 was utilized as the anodic reaction. Hydrochloric acid was utilized as the source of chloride ions. All plated experiments were performed at modification of these concentrations that would be stated during the discussion of those results. Early in the study, Cu^{2+} concentration was targeted at 25g/l and 50 g/l that was later increased to 65g/l to eliminate diffusion barriers for void-free fill. 65g/l is the highest concentration of Cu^{2+} that can be reached with the existing electrolyte set up as any further increase caused precipitation of copper. Experiments performed with Cu^{2+} concentration of 25g/l are annotated carefully as required. Sodium Chloride crystals were utilized for the replenishment of the chloride component in the bath. Bath compositions were closely monitored and kept within <1% deviation of the target values. Electrodeposition was performed with a commercially available plating equipment. All plating experiments were performed at Intel Corporation, Chandler, AZ fab facility. A commercial Fe^{2+}/ Fe^{3+} redox reagent and regenerator was utilized for driving the anodic reaction and keeping the ionic concentration of ferric ions in check. Concentration of ferric ions generated during the plating process was frequently monitored to keep the total conc. of ions to a minimum (<1.0g/l). Fe^{3+} concentration was initially targeted at 1g/l. Specific concentrations utilized for each of those experiments will be stated as needed. Commercially available organic additives, purchased from Atotech Inc., namely SMP Inpulse Leveller and SMP Inpulse Brightener were also added to the plating bath. The consumption and target concentration of these species were closely monitored and kept

within the operating window. Exact molecular structure and details of this chemistry is proprietary to the supplier and unknown for this study. The nomenclature of these commercial species can be confusing to the reader since we discussed the role of accelerator and suppressor molecules in the introductory part of the chapter. This confusion will be easily clarified in the later part of the discussion during the discussion on results from various experimental and simulation studies. Some of those results would duly confirm that the overall behavior of these commercial species would closely match that of some of the generic species of accelerator and suppressor discussed earlier. Henceforth in the rest of the discussion these species would be termed as accelerator and suppressor only. For the initial part of the study, the accelerator species was targeted at 12ml/l and the suppressor was targeted at 16ml/l. Thus, the net ratio of the species was maintained at 0.75. Any change in target concentration or change from this nominal ratio that was later optimized to further improve the fill process will be clearly stated during the discussion of those results. Nominal temperature of the plating bath was maintained at 36°C. Initially, depositions with high copper concentration was performed at 48°C. Specific temperature carried out for each experimented will be clearly annotated.

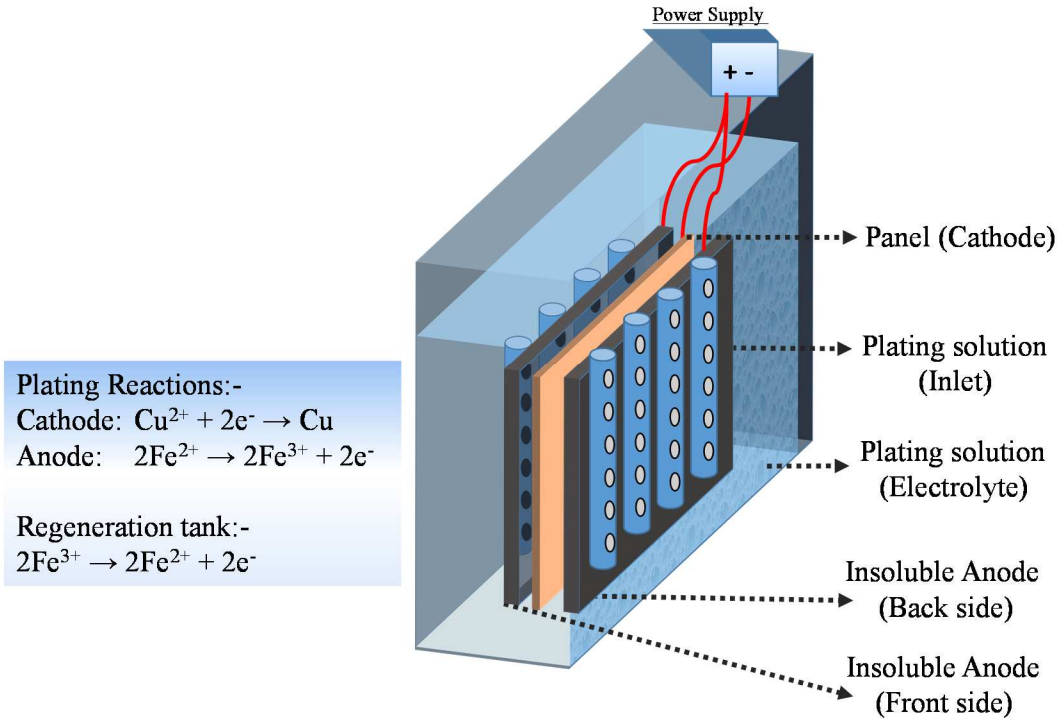


Figure 5.3: Schematic of the plating cell

For all plating experiments, the thickness of the incoming copper seed was further increased with a flash plating process in the same plating bath where rest of the plating process happens. This was done to prevent any increase in resistivity due to seed loss or discontinuity in the early stages of plating from the application of reverse waveform, acid etch or Fe^{2+}/Fe^{3+} redox couple present in the electrolyte. Flash plating was performed for 450s – 750s as required for a given via feature. Adequate circulation and strong agitation were performed to ensure complete mixing of the electrolyte and elimination of any dead

zones inside the reactor. Post deposition, the copper surface was annealed before any metrology measurements. In all cases, thickness measurements and void analysis were performed with an in-house profilometer (VEECO) or with SEM (Hitachi), wherever applicable. 3D X-ray (X-Raida) techniques were utilized to verify elimination of trapped voids. Materials characterization utilizing SEM, were performed both at Intel Corporation and at Arizona State University, Tempe AZ.

Section 5.3 Experimental setup: Choice of reverse pulse plating waveform

A schematic of reverse pulse waveform utilized in this study is shown in Figure 5.4. i_1 & i_2 marked on the Y-scale are the forward and reverse pulse current density amplitudes and T_1 & T_{2*} are the corresponding time periods for those amplitudes. Time duration T_{total} of the waveform that equals T_1+T_2 is the length of the total waveform and is always in the range of 80ms to 100ms. This waveform was then repeated for the established plating period to achieve the required fill. Average current density for each waveform is calculated as $A_0 = [(i_1 \times T_1)-(i_2 \times T_2)]/T_{total}$, and could vary anywhere between 2ASD to 5ASD (A/dm^2).

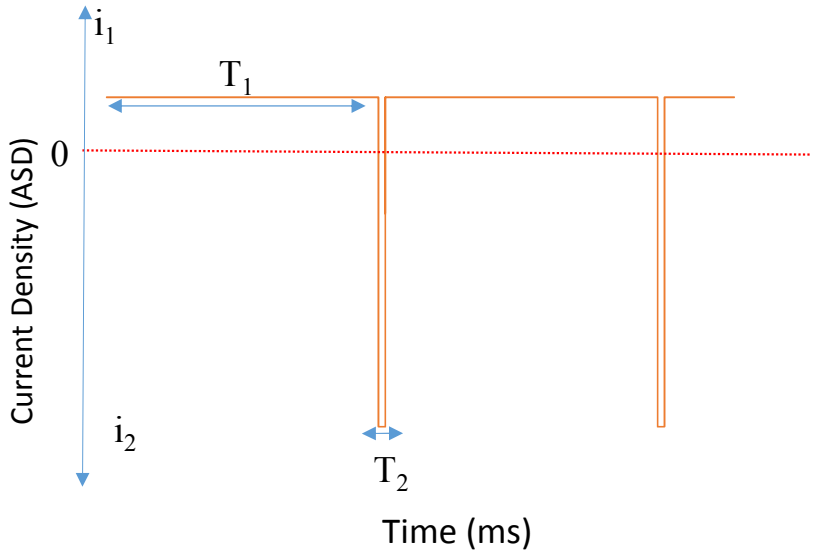


Figure 5.4: Schematic of forward-reverse pulse waveform

In this study, the amplitude of reverse pulse current and time period were varied independently to establish a stronger reverse pulse effects. To begin with, three different reverse pulse waveforms were utilized for our testing initially as shown below. The parameters of various reverse pulse waveforms are summarized in Table 5.2.

Table 5.2: Summary of reverse pulse waveforms utilized in this study

	Average Current density and Time period		Reverse Current density and Time period		Forward Current density and Time period	
	i_{total} (A/dm^2)	T_{total} (s)	i_2 (A/dm^2)	T_2 (s)	i_1 (A/dm^2)	T_1 (s)
Pulse Waveform # 1	5.0	0.08	10	0.002	5.3	0.078
Pulse Waveform # 2	3.4	0.08	40	0.004	5.7	0.076
Pulse Waveform # 3	5.0	0.08	24	0.004	6.5	0.076
Pulse Waveform # 4	5.0	0.08	24	0.002	5.75	0.076

As shown in Table 5.2, pulse waveform #1 with a reverse current density of 10ASD is considered a soft pulse. Pulse waveform # 2 with a reverse current density of 40ASD is indicated as a hard / strong pulse waveform and pulse waveform #3 with reverse current density of 24ASD as an intermediate waveform. These soft, intermediate and strong reverse pulse cover the entire spectrum of reverse pulse duration and current possible for testing with the current equipment set up. For all waveforms, reverse current were included only for a very short time period (few millisecond). Layout of the different reverse pulse waveform that were tested initially is shown in Figure 5.5 below.

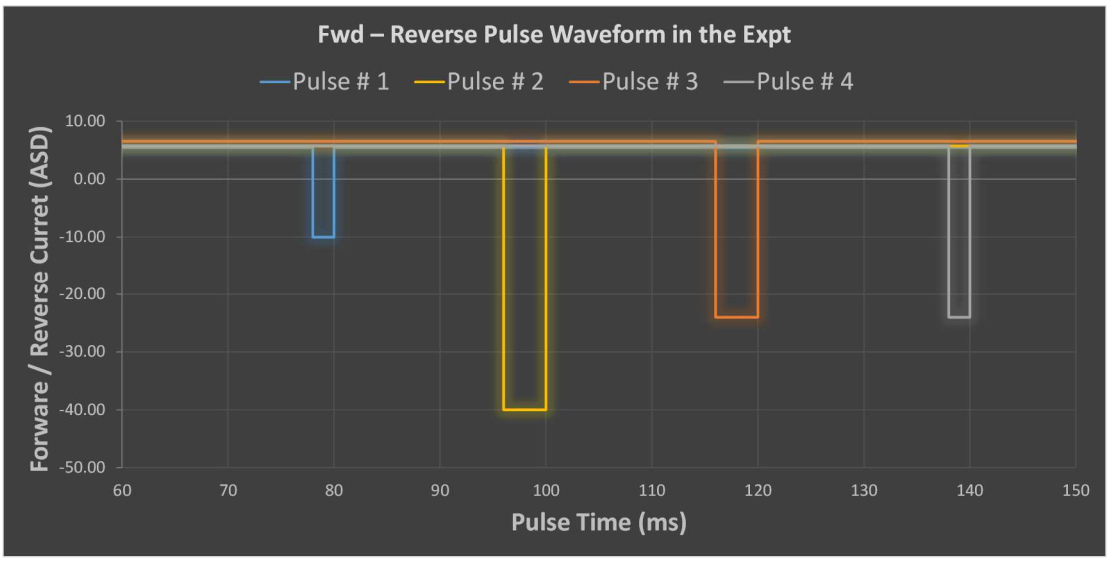


Figure 5.5: Schematic of different pulse waveforms experimented

Section 5.4 Summary

So far we discussed the construction of test coupon with various via geometry and fine pattern features for IC substrate applications. Each via geometry requires a unique approach to establish a gap fill methodology along with generation of uniform deposit on pattern regions. Earlier in chapter II, we had discussed that the distribution of an electroplated deposit depends upon which transport phenomenon controls the plating rate. Therefore, we need to consider the overall electrical and chemistry effects present inside the system to determine which transport mechanism dominates the distribution of copper inside via region. Ohmic resistance of the metal film leads to variations of potentials in the film while solution resistance leads to variations of potential in the plating solution. In the presence of a thin conductive seed layer, charge transfer resistance cannot be ignored either. These effects are termed electrical effects and the "Butler–Volmer" equation

simplifies accordingly based on the given rate limiting parameter as shown in Figure 5.6 (left side of the flow chart).

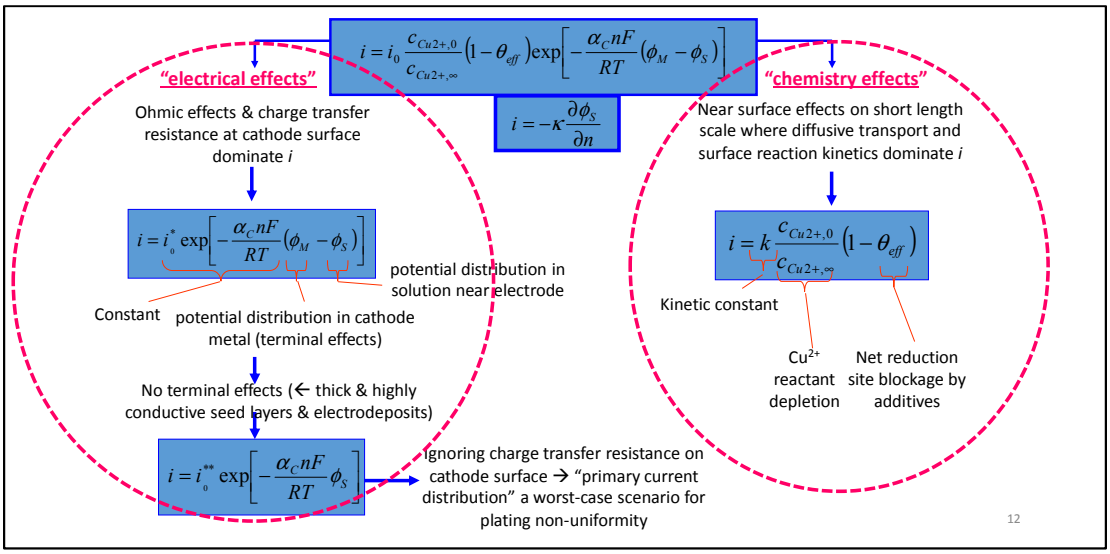


Figure 5.6: Flow chart to show simplification of "Butler-Volmer" equation with electrical and chemistry effects

Alternatively, mass-transfer effects leads to variations in concentration of cupric ion and other additive species present in the electrolyte. Domination of such effects across the metal surface is termed, chemistry effects as shown in Figure 5.6 (right side of the flow chart). Generally, non-uniform reaction rates are caused by either inadequate mixing so that reactant concentrations are not uniform (convection effect), or by spatial variations in the electrical-potential difference across the electrode/electrolyte interface or due to concentration gradient (diffusion). Due to the large concentration of acid present in the electrolyte, migration effects are negligible. For the purpose of enabling void free via fill, the true diffusion effect on the gap fill process needs to be understood. Convection effects play an equally important role as well. When diffusion and chemistry effects dominates the fill process, the deposition current density determined from "Butler-Volmer" equation

simplifies to a proportional limit of kinetic rate constant, concentration gradient and availability of active surface sites for the reduction process to happen as shown in Figure 5.7. Several factors can influence the parameters in these equations and optimizing of such parameters can facilitate bottom-up fill. For example, as shown in Figure 5.7, increased temperature can offset for depletion of Cu^{2+} ions at the via bottom due to the increased mobility of ions at higher temperature and improve bottom fill rate.

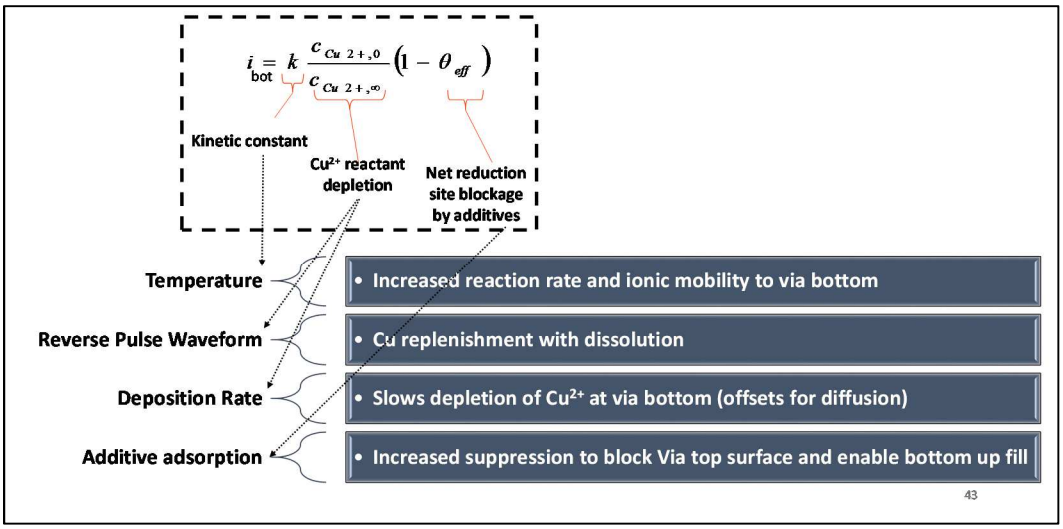


Figure 5.7: Key parameters to modulate "chemistry effects" with simplified "Butler-Volmer" relationship

Incorporation of reverse pulse methodology establishes additional amount of Cu^{2+} ions from the freshly dissolved metal due to the application of reverse pulse. Reduction in the overall deposition rate leads to slow depletion of Cu^{2+} ions which in turn allows for diffusing Cu^{2+} ions to play catch-up with the fill process preventing depletion. Incorporation of additives selectively blocks surface sites at the via top and enables

bottom-up fill. Therefore, a capable deposition process can be established utilizing each of these available parameters for IC substrate fill applications.

Earlier in this chapter, we have identified several reverse pulse waveforms that could be extensively applied to optimize gap fill for various via geometries. A design of experiments was henceforth set-up to study the capability of these reverse pulse methodology for void free fill in IC substrate via geometries. Early into development of reverse pulse process we ran into several challenges that are not normally seen with DC (direct current) plating process. Experimental studies with the incorporation of reverse pulse methodology for Via0 and Via1 geometry along with the optimization efforts to enable void free fill is captured in Chapter VI.

In order to best explain the experimental limitations observed with reverse pulse methodology and to better predict throwing power that can be obtained with reverse pulse process for these via geometries a simulation effort was undertaken. Simulation set up and the results from simulation studies are captured in Chapter VII.

Chapter VIII covers the microstructure obtained with reverse pulse methodology. In this part of the study, we showcase the ability to tune microstructure with the application of reverse pulse waveform along with other identified process conditions from the relationship in Figure 5.7, such as bath temperature and electrolyte concentration.

While extending the reverse pulse process from Via0 to Via5 we ran into additional challenges of enabling void free gap fill due to the presence glass cloth fiber protrusions inside the via that impede bottom-up fill. A comprehensive DOE was then

established to encompass the interaction of all possible process parameters including organic additives based on the relationship identified in Figure 5.7 to improve TP and enable void free fill. Learning's from such studies are shown in Chapter IX and X. Finally a simulation effort was undertaken to identify the extent of TP improvement that can be obtained with organic additives along with reverse pulse and the results from those simulation studies are shown in Chapter XI.

Experimental results from the the application of reverse pulse methodology for via0 and Via1 geometries is now discussed further.

CHAPTER VI

REVERSE PULSE METHODOLOGY FOR VOID-FREE FILL ACROSS VIA0 AND VIA1 GEOMETRY

Section 6.0 Introduction to via0 and via1 geometry

Via0 geometry includes a via with a depth of ~25μm. The via top and bottom diameter can vary slightly due to the variation with the drilling process but normally the via bottom diameter ranges around ~20μm and via top diameter around ~40μm. Via1 geometry accommodates similar depth but the via opening size is larger with the bottom diameter around 50~55μm and via top opening to be much larger (~70μm). Due to the presence of large opening area inside the via that requires gap fill of copper, electrodeposition with much higher deposition rate (current density) are desired to reduce the total time for deposition and increase factory output. To enable high deposition rates, electrodeposition process conditions such as electrolyte composition, bath temperature, deposition waveform needs to be designed carefully. The distribution of Cu metal utilizing an electrodeposition process depends upon which transport phenomenon controls the net deposition rate. We need to consider the overall ohmic and mass transfer effects present inside the system to determine which transport mechanism dominates the distribution of copper inside the via region. Ohmic resistance of the metal film leads to variations of potentials in the film, and solution resistance leads to variations of potential in the plating solution. Mass-transfer effects lead to variations in concentration of cupric ion and additive species across the metal surface. High deposition rates lead to mass

transfer limitation that eventually could lead to the via bottom deprived of any Cu^{2+} ions for deposition while the via top plating at a higher deposition rate due to the easy supply of Cu^{2+} ions from the bulk. This phenomenon leads to entrapment of voids. In order to improve the deposition rate at the via bottom and establish high throwing power (increased deposition rate at the via bottom compared to via top) definition of novel methodologies are needed. In this section, incorporation of a novel reverse pulse methodology is attempted to gap fill Via0 and Via1 geometry. Experimental results obtained with Via0 geometry is discussed first followed by the experimental results obtained with Via1 geometry.

Section 6.1 Design of experiments with via0 geometry for gap fill

Table 6.1 summarizes the eight different experiments that were performed to enable void-free bottom-up fill with the incorporation of reverse pulse methodology for via0 geometry. For all plating experiments, the thickness of the incoming copper seed was further increased with a flash plating process in the same plating bath where rest of the plating process happens. This was done to prevent any increase in resistivity due to seed loss or discontinuity in the early stages of plating from the application of reverse waveform, acid etch or Fe^{2+}/Fe^{3+} redox couple present in the electrolyte. Flash plating was performed for 450s – 750s as required for a given via feature. Key electrodeposition parameters are tabulated for each of those experiments. Fill and deposit results obtained with these experiments will be discussed further below.

Table 6.1: Design of experiments for Via0 geometry

Steps	Parameters	Expt 1	Expt 2	Expt 3	Expt 4	Expt 5	Expt 6	Expt 7	Expt 8
Flash Cu	Cu2+ (g/l)	25	25	25	25	65	65	65	65
	Temp ©	36	36	36	36	36	36	36	36
	Pump Agitation (Hz)	15	15	15	15	15	30	30	30
	Reverse Pulse CD	10	10	10	10	10	10	10	10
	Reverse Pulse Duration (ms)	2	2	2	2	2	2	2	2
	Forward Pulse Duration (ms)	78	78	78	78	78	78	78	78
	Reverse Pulse Waveform ID	1	1	1	1	1	1	1	1
	Total Duration (s)	450	450	450	450	450	450	450	450
Via Fill	Cu2+ (g/l)		25	25	25	65	65	65	65
	Temp ©		36	36	36	36	36	36	36
	Pump Agitation (Hz)		15	15	15	15	15	15	30
	Reverse Pulse CD		10	24	24	24	24	40	10
	Reverse Pulse Duration (ms)		2	2	4	4	4	4	2
	Forward Pulse Duration (ms)		78	78	76	76	76	76	78
	Reverse Pulse Waveform ID		1	4	3	3	3	2	1
	Total Duration (s)		1000	450	450	450	450	450	1000

Section 6.2 Results and discussion with via0 geometry for gap fill

Figure 6.1a shows a SEM cross-section of an incoming via surface covered with a copper seed layer. The depth of the via was measured to be around 24.11µm and the via top diameter was measured to be 34.12 µm while the via bottom diameter was measured to be 17.12 µm. The coverage of the seed layer was found to be continuous and uniform along the length of the via with the thickness of the copper seed to be measured around ~1um. Henceforth, the via of this geometry will be referred to as via0 or V0 and will the focus for further discussion below.

Figure 6.1b shows the SEM cross-section of a Via0 after flash copper deposition (Expt #2). Flash plating is always performed because of concerns of seed dissolution during early part of the process. Flash plating of this layer was performed for a duration

of 450s utilizing reverse pulse waveform #1 with the concentration of the Cu^{2+} ion maintained at 25g/l, 36°C. The pump agitation was controlled at 15Hz that corresponds to a flow rate of ~130LPM. Overall, the thickness of the deposit looks continuous with the thickness of the deposit measured at the via top region at ~2X higher than at via bottom.

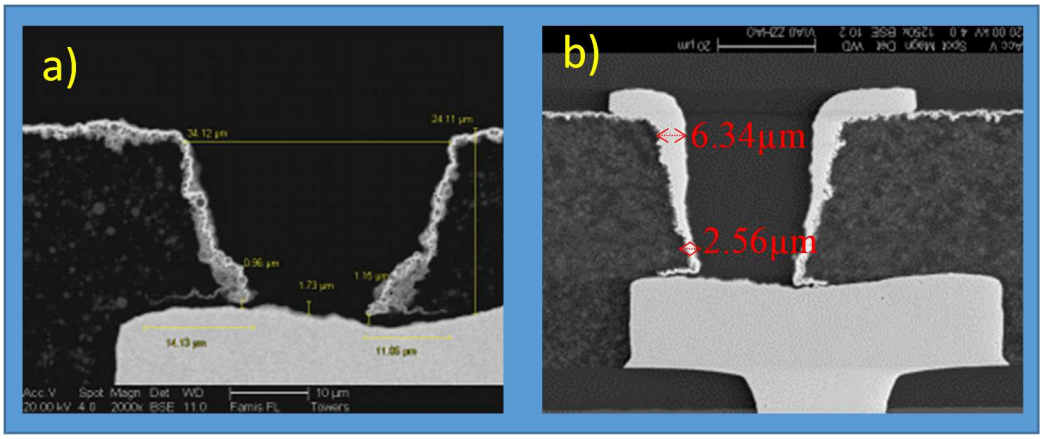


Figure 6.1: a) Incoming copper seed layer: Via depth of ~25um and via bottom opening of ~20um and b) POST Flash Cu deposition (25g/l of Cu^{2+} for a duration of 450s, 36°C, 15Hz of Pump frequency)

Figure 6.2 shows the gap fill profile from Expt #3 that was performed with reverse pulse waveform #1 for a duration of 1000s post flash Cu plating. Presence of key-hole voids confirms the lack of gap fill. The thickness of the deposit at via bottom region is reduced than at the via top region likely leading to sidewall collusion at the via top and entrapment of voids. It is to be noted that a small amount of organic additives were added in the electrolyte, as discussed in Chapter V to generate a bright deposit. Unsurprisingly, trace amount of organics added in the electrolyte did not show any positive impact on the via fill process confirming their reduced impact in the fill process so far.

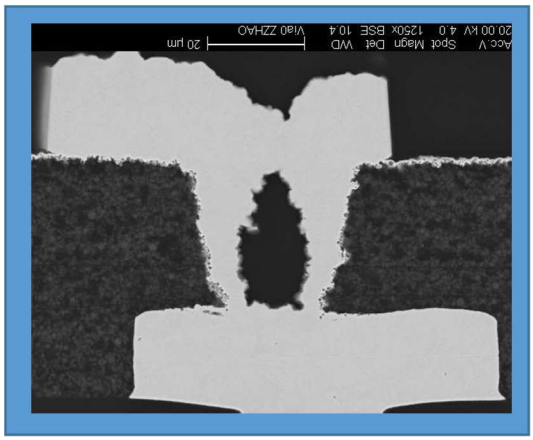


Figure 6.2: SEM Cross-section of Via0 post complete deposition with reverse pulse waveform #1 (25g/l of Cu^{2+} for a duration of 1000s, 36°C, 15Hz of Pump frequency)

Section 6.2.1 Results: Effect of copper concentration for via0

In experiments #2, #3, #4 the reverse pulse duration and current density was varied independently during via fill process. Surprisingly, when the magnitude of reverse current density was increased to larger values to increase the concentration of local Cu^{2+} ion at via bottom, no change in fill profile was observed. Figure 6.3 shows SEM cross-section after complete deposit with higher reverse pulse current density and durations.

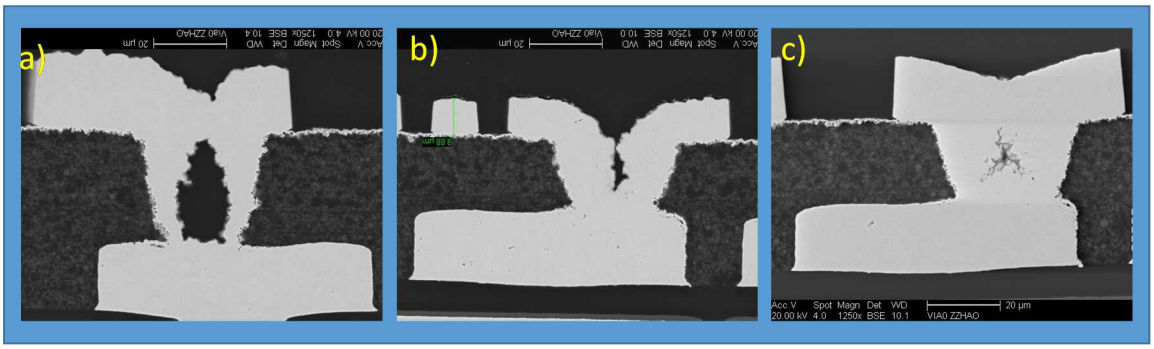


Figure 6.3: SEM Cross-section of Via0 post complete deposition with the following conditions: a) Post Via fill (1000s, 8ASD, 2ms [Reverse pulse # 1], b) POST Via fill (450s, 24ASD, 2ms [Reverse pulse # 4], c) POST Via fill (450s, 24ASD, 4ms [Reverse pulse # 3]

In all cases pinch off and key hold voids were observed. As shown in Figure 6.3a & 6.3b even after significant increase in reverse pulse current density from 10ASD to 24ASD there was no impact in throwing power with the top of the via still plating at a significantly higher rate. As shown in Figure 6.3b & 6.3C increasing the reverse pulse duration from 2ms to 4ms at a reverse current density of 24ASD also did not generate adequate bottom-up fill. In all these cases, thickness of via sidewalls at the top of via seems to be much higher than the bottom region of the via indicating poor bottom-up fill.

This behavior can be likely attributed to the applied current operating near the diffusion limited current density. Under mass transfer limitations, excess Cu^{2+} ions generated with the reverse charge is readily consumed at the via top surface before diffusing to via bottom due to the lack of adequate replenishment of Cu^{2+} ions from the bulk. Low throwing power condition with $i_B < i_T < 1$ is likely to persist and cause pinch-off or void entrapment. Reduction in applied current density mitigates some of this effect. However, such approaches will increase the overall processing time and limit factory

outputs. Therefore, in order to move the deposition process from mass transfer limited regime, Cu^{2+} concentration in the electrolyte was increased from 25g/l to 65g/l. Gap fill capability of reverse pulse waveform was re-evaluated without reducing the applied current density as experiment # 5 with the data shown in Figure 6.4.

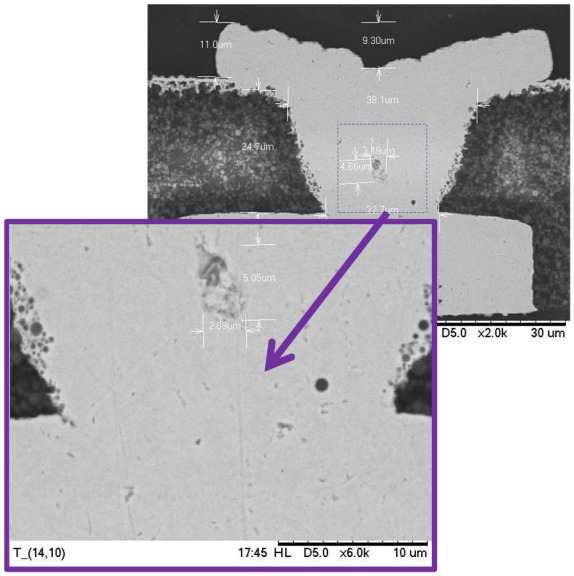


Figure 6.4: SEM Cross-section of Via0 post complete deposition with the following conditions: Flash Cu plating with 65g/l Cu $^{2+}$ and via fill utilizing 65g/l Cu $^{2+}$, Reverse Pulse # 3

As shown in Figure 6.4, pinch off voids were still observed but the size of the voids have been drastically reduced. An increase in pump flow rate for the flash Cu plating process from 13Hz [115LPM] to 30Hz [230LPM] was performed to provide better agitation and circulation inside the reactor and another experiment was executed in experiment # 6 with the rest of parameters unchanged. This condition completely eliminates the voids as shown in Figure 6.5.

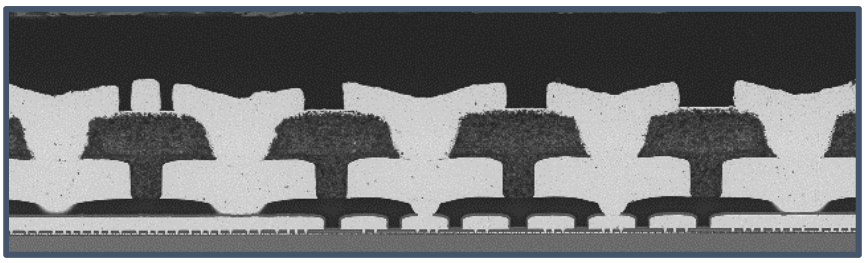


Figure 6.5: SEM Cross-section of Via0 post complete deposition with the following conditions: Flash Cu plating with 65g/l Cu $^{2+}$ 30Hz and via fill utilizing 65g/l Cu $^{2+}$, Reverse Pulse # 3

Section 6.3 Results and discussion with non-uniform deposition for via0 geometry

In a conventional DC plating process, accelerator molecules (fast diffusion species) are added in the plating bath to enhance bottom-up fill behavior. Accelerators catalyze the reduction of Cu^{1+} to Cu during Cu deposition[1]. Other additive species such as suppressors / levelers modulate the local deposition rate through adsorption or by coupling with the polarized accelerator molecules to provide uniform deposition and level the final deposit. Similarly, in the case of reverse pulse based process, with the application of reverse current, deposition rate at the bottom of via is dramatically accelerated leading to higher throwing power value. In the absence of leveler molecule to attenuate the accelerated deposition, the deposition process happens in a "momentum plating" or extreme "super fill" regime. Although void-free fill is obtained, such unchecked momentum plating could lead to non-uniform deposition of copper in the Via pad and FLS regions. In this study, with the induction of reverse pulse methodology to improve bottom-up fill momentum plating is established with accelerated growth of copper from the via bottom. Such a phenomenon is likely to persist on fine traces and pad regions as well. Therefore,

momentum plating induced with reverse pulse methodology will provide a very non-uniform deposit overall. A strong reverse pulse waveform introduces a condition termed as “Ski-slope” meaning the surrounding trace and pad features show sloped deposit than a flat deposit that is desired. Fine trace and large pad regions tend to plate at a different rate and show non-uniform surface.

Expt #8 incorporates reverse pulse waveform #1, that has a reverse current density of 8ASD for a duration of 2ms. The gap fill deposition time was increased significantly to ~1000s. As shown in Figure 6.6b1 and 6.6b2 even after such prolonged plating duration the via shows a large dimple at the top, indicating a largely unfilled via. The contour maps also show a largely unfilled via. The surrounding fine traces plate slightly thinner than the via pad regions.

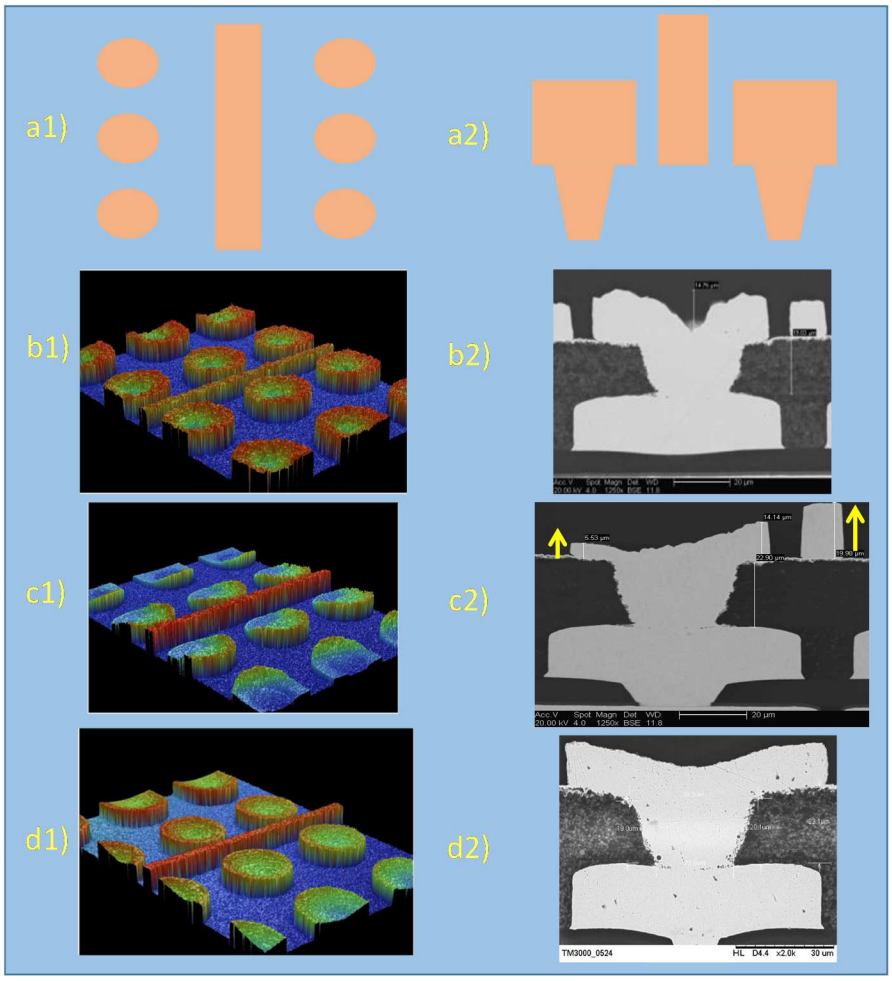


Figure 6.6: (a1) Top view and (a2) side view of FLS and via feature layout (b1) Thickness contour map with reverse pulse waveform # 1 waveform at layer1 (b2) SEM images of Via0 and a 9µm trace feature at layer1 plated with reverse pulse waveform # 1(c1) Thickness contour map with reverse pulse waveform # 2 waveform at layer1 (c2) SEM images of Via0 and a 9µm trace feature at layer1 plated with reverse pulse waveform # 2 (d1) Thickness contour map with reverse pulse waveform # 3 waveform at layer1 (d2) SEM images of Via0 and a 9µm trace feature at layer1 plated with reverse pulse waveform # 3

Figure 6.6c1 and 6.6c2 show the results obtained from Expt #7 where the maximum allowed current density of 40ASD was utilized with a time duration (T_{REV}) of 4ms with reverse pulse waveform #2. Thickness contour and SEM image depict a momentum plating phenomenon being established.

Fine trace regions plate thick while the surrounding large pad regions show significantly lower thickness, in a non-uniform fashion. Non-uniform "ski slope" topography is observed with the large via pads. These large non-uniform deposit confirm that it is difficult to achieve a uniform deposit of trace and pad features with the incorporation of a very strong reverse pulse for these via geometry. Figure 6.6d1 and 6.6d2 show the results obtained from Expt #6 where a nominally allowed reverse current density of 24ASD was utilized with reverse pulse waveform #3. Void-free bottom-up gap fill is present and any presence of "Ski-sloped" pads is eliminated. Figure 6.7 summarizes the measured plating thickness across a trace and via pad feature around the via region with different reverse current density. A top and side view schematic of the pattern in the test coupon for the measured thickness contour maps is shown in Figure 6.6a and 6.6b.

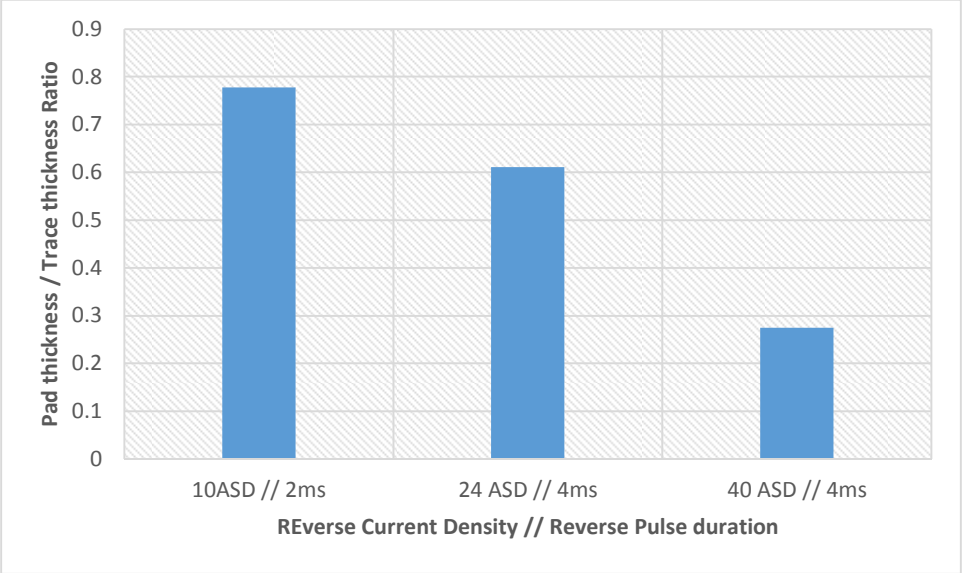


Figure 6.7: Summary of plating thickness with different reverse pulse current density and durations

Ideally all the features need to plate to the same target height with the ratio to 1. As seen from Figure 6.7, with the introduction of a larger reverse pulse conditions, this ratio decreases significantly to generate non-uniform surfaces.

We will now move onto the experimental studies and the results obtained with incorporation of reverse pulse methodology for Via1 geometry

Section 6.4 Design of experiments with via1 geometry

Table 6.2 summarizes the different experiments that were performed to enable void-free bottom-up fill with the incorporation of reverse pulse methodology for via1 geometry. Key electrodeposition parameters are tabulated for each of those experiments. Fill and deposit results obtained with these experiments will be discussed further below.

Table 6.2: Design of experiments for Via1 geometry

Steps	Parameters	Expt 9	Expt 10	Expt 11	Expt 12	Expt 13
Flash Cu	Cu2+ (g/l)	25	25	25	25	65
	Temp ©	36	36	36	36	36
	Pump Agitation (Hz)	15	15	15	15	30
	Reverse Pulse CD	10	10	10	10	10
	Reverse Pulse Duration (ms)	2	2	2	2	2
	Forward Pulse Duration (ms)	78	78	78	78	78
	Reverse Pulse Waveform ID	1	1	1	1	1
	Total Duration (s)	750	750	750	750	750
Via Fill	Cu2+ (g/l)		25	25	25	65
	Temp ©		36	36	36	36
	Pump Agitation (Hz)		15	15	15	15
	Reverse Pulse CD		10	24	24	24
	Reverse Pulse Duration (ms)		2	2	4	4
	Forward Pulse Duration (ms)		78	78	76	76
	Reverse Pulse Waveform ID		1	4	3	3
	Total Duration (s)		750	750	750	750

Section 6.5 Results and Discussion with via1 Geometry

Figure 6.8a shows a SEM cross-section of an incoming via surface covered with a copper seed layer. The depth of the via was measured to be around 23.22µm and the via top diameter was measured to be 63.43 µm while the via bottom diameter was measured to be 54.62 µm. The coverage of the seed layer was found to be continuous and uniform along the length of the via with the thickness of the copper seed to be measured around ~1um. Henceforth, the via of this geometry will be referred to as via1 or V1 and will the focus for further discussion below.

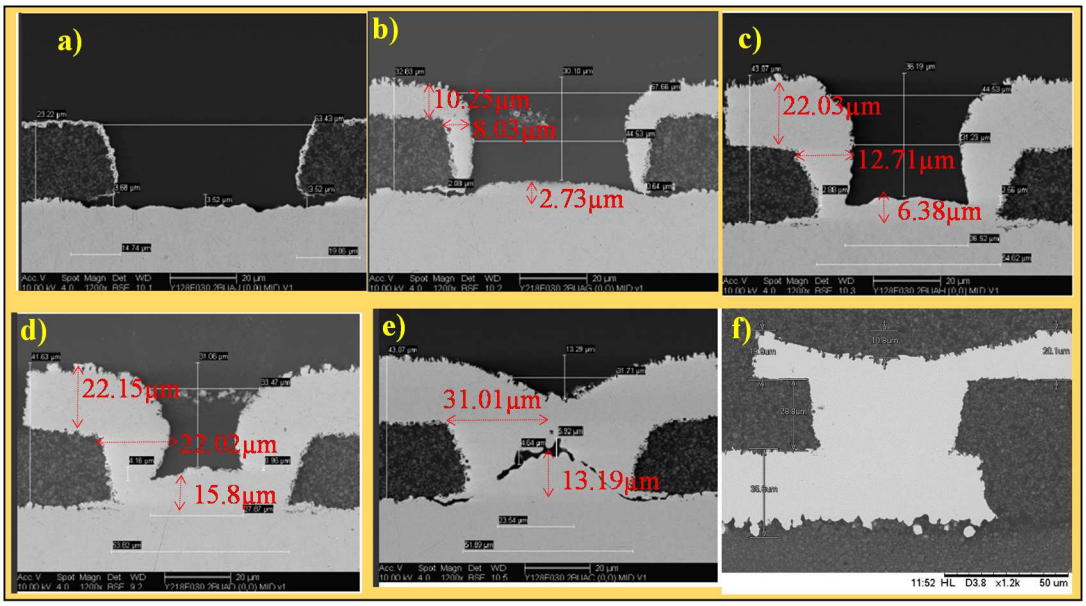


Figure 6.8: a) SEM Cross-section of Via1 with a copper seed layer; Figure 6.8b) SEM Cross-section of Via1 post Flash Cu plating process with 25g/l of bulk Cu^{2+} ions and 36°C bath temperature; Figure 6.8c) SEM Cross-section of Via1 post Flash Cu plating and Via fill with 25g/l of bulk Cu^{2+} ions and 36°C bath temperature and reverse current density of 8ASD for 2ms; Figure 6.8d) SEM Cross-section of Via1 post Flash Cu plating and Via fill with 25g/l of bulk Cu^{2+} ions and 36°C bath temperature and reverse current density of 24ASD for 2ms; Figure 6.8e) SEM Cross-section of Via1 post Flash Cu plating and Via fill with 25g/l of bulk Cu^{2+} ions and 36°C bath temperature and reverse current density of 24ASD for 4ms; Figure 6.8f) SEM Cross-section of Via1 post Flash Cu plating with 65g/l of bulk Cu^{2+} ion and Via fill with 65g/l of bulk Cu^{2+} ions and 36°C bath temperature and reverse current density of 24ASD for 4ms

Figure 6.8b shows the SEM cross-section of a Via1 geometry after flash plating deposition (Expt #9) . Flash plating of this layer was performed for a duration of 750s utilizing reverse pulse waveform #1 with the concentration of the Cu^{2+} ion maintained at 25g/l, 36°C. The pump agitation was controlled at 15Hz. The thickness of the deposit looks continuous with the thickness of the deposit measured at the via top region at ~2X higher than at the via bottom.

Figure 6.8c shows the gap fill profile of Expt #10 that was performed with reverse pulse waveform #1 for a duration of 750s post flash Cu plating. The via looks completely unfilled for this duration. Deposit thickness is also higher at the via top region that at via bottom indicating a side wall collusion at the via top if the deposition process continues further and high propensity of void entrapment.

Section 6.5.1 Effect of copper concentration for via1 geometry

In experiments 11 and 12 the reverse pulse duration and current density were varied to obtain via fill. Surprisingly, when the magnitude of reverse current density was increased to larger values to increase the concentration of local Cu^{2+} ion at via bottom, no change in fill profile was observed. Presence of key-hole voids confirms the lack of gap fill. Figure 6.8d and 6.8e shows SEM cross-section after complete deposit with higher reverse pulse current density and durations. In all cases pinch off and key-hole voids were still observed. As shown in Figure 6.3c & 6.3d even after significant increase in reverse pulse current density from 10ASD to 24ASD there was no impact in throwing power with the top of the via still plating at a significantly higher rate. As shown in Figure 6.8d & 6.8e increasing the reverse pulse duration from 2ms to 4ms at a reverse current density of 24ASD also did not generate bottom-up fill. In all these case thickness of the via sidewalls at the top of the via seems much higher than the bottom region of the via indicating poor bottom-up fill. As discussed with the via0 geometry, this behavior can be attributed to the applied current operating near the diffusion limited current density. Therefore, in order to move the deposition process from mass transfer limited regime,

Cu^{2+} concentration in the electrolyte was increased from 25g/l to 65g/l. Gap fill capability of reverse pulse waveform was re-evaluated without reducing the applied current density as experiment # 13 with the data shown in Figure 6.8e. As shown in Figure 6.8e, pinch off voids were eliminated. Correction in pump frequency for the flash Cu plating process from 13Hz to 30Hz was accommodated in expt #13 based on the learning's from Via0 geometry.

Section 6.6 Results and discussion with non-uniform deposition for via1 geometry

Given the clear learning's earlier on Via0 geometry with the impact of high reverse pulse current and to a non-uniform deposit with fine trace regions plating thicker and the surrounding large pad regions with significantly lower thickness, repeat measurements of such features were not done for this layer. It is clear that reverse pulse duration and current density needs to optimized to obtain uniform copper deposit wherein the variation in thickness of the feature is minimized, all in while ensuring void-free gap fill inside the via.

Section 6.7 Summary with via0 and via1 geometries

In summary, void-free via fill process is obtained with the introduction of reverse pulse methodology for Via0 geometry. Optimization of process conditions such as electrolyte Cu^{2+} concentration, agitation and the reverse pulse amplitude was necessary to generate a completely filled Via. A larger reverse amplitude degrades the thickness distribution across the features.

For Via1 geometry, void-free via fill process is obtained with the introduction of reverse pulse methodology. Optimization of process conditions such as electrolyte Cu^{2+} concentration, agitation and the reverse pulse amplitude was necessary to generate a completely filled Via. A larger reverse pulse amplitude is likely to degrade the thickness distribution across the features with these ratios as well. So far we discussed the results obtained from experimental studies with different reverse pulse waveforms and attempted to mitigate the mass transfer effect with increased bulk concentration of copper. In chapter VII, a simulation effort is undertaken to validate the concentration gradient effect seen with the present system. The simulation effort aims to identify critical throwing power needed to generate void-free bottom-up fill and how reverse pulse methodology helps to enable that.

REFERENCES

1. P. M. Vereecken, R. A. Binstead, H. Deligianni, and P. C. Andricacos, IBM Journal of Research and Development, 49(1), 3 (2005)

CHAPTER VII

SIMULATION OF REVERSE PULSE PROCESS

Section 7.0 Introduction

Simulation for gap fill inside via features for applications such as dual damascene and TSV (Through Silicon Via) have already been extensively studied in various literatures[1-4]. In the present effort a simulation case study was undertaken to explain the mechanism of gap-fill data under different pulse and reverse pulse plating conditions for Via0 geometry on IC substrate applications. Via0 geometry includes via of ~20µm depth and a diameter of ~35um as shown in Figure 7.1 below.

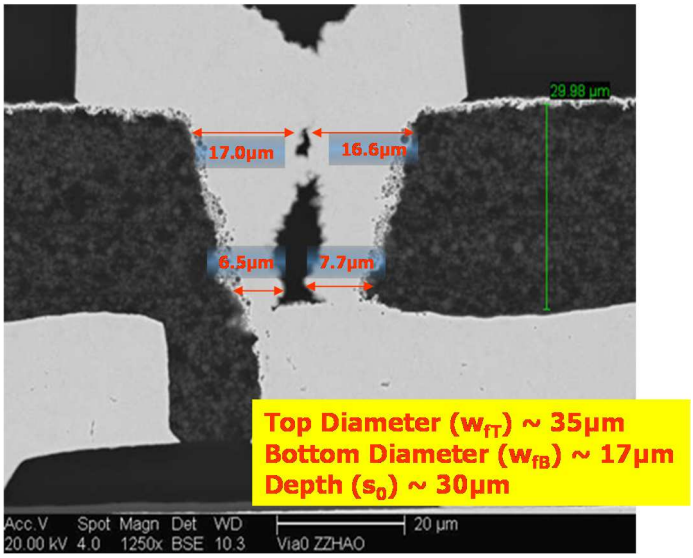


Figure 7.1: Via0 geometry utilized for simulation case study

Takahashi and Gross have previously outlined which phenomena dominate current distribution on ≤1micron feature scales.[1] Earlier in chapter II, we had discussed that the

distribution of an electroplated deposit depends upon which transport phenomenon controls the plating rate. We need to consider the overall ohmic and mass transfer effects present inside the system to determine which transport mechanism dominates the distribution of copper inside the via region. Ohmic resistance of the metal film leads to variations of potentials in the film, and solution resistance leads to variations of potential in the plating solution. Mass-transfer effects lead to variations in concentration of cupric ion and additive species across the metal surface. Generally, non-uniform reaction rates are caused by either inadequate mixing, so that reactant concentrations are not uniform (convection effect), or by spatial variations in the electrical-potential difference across the electrode/electrolyte interface or due to concentration gradient (diffusion). Due to the large concentration of acid present in the electrolyte, migration effects are negligible. For the purpose of understanding the true diffusion effect on the gap fill process, in this simulation, the spatial variations in the electrode –potential difference across the electrode-electrolyte interface and inadequate mixing effects were assumed to be minimal and negligible. This was assumption in Takahashi's work[1]. Similar to the work of Takahashi[1], our own work suggests that these assumptions hold for the larger features (10s of microns) currently encountered in package build-up applications. A quick analysis of the process conditions will show that this justification is valid for the Via0 geometry systems we have studied thus far.

Section 7.1 Convection effects

The relative importance of convection vs. diffusion is represented by the Peclet number[1] where,

$$\mathbf{Pe = vL/D} \qquad \textbf{(7.1)}$$

where ν is a fluid velocity in the via, L is a via depth, and D is the diffusivity of the Cu^{2+} species. If Pe >> 1, then convection plays an important role in the transport of cupric ion and additive species into the via. If Pe << 1, convection effects are negligible and diffusion transport dominates the ion transport mechanism. For our system, the fluid velocity was roughly determined by solving for laminar flow using Navier-Stoke's equation with the Fluent SW system.

A simple 3D geometry was constructed to mimic the submerged jet flow of fluid inside the plating reactor as shown in Figure 7.2. Essentially this simple geometry represents the flow coming out of a single nozzle (injectors) to determine the velocity of the fluid at the mouth of the via.

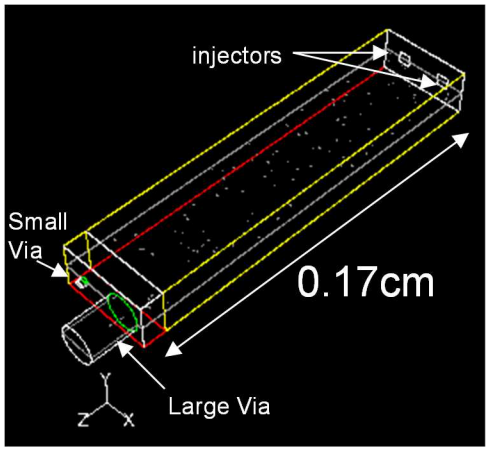


Figure 7.2: 3D Geometry of impingement Jet flow

In the actual system that was utilized for experiments in Chapter VI, the flow nozzles were positioned very close to the test coupon surface. The position of the coupon was roughly determined to be about 1.7mm away from the tip of the nozzle. Four different cases were tested to determine the velocity magnitude along the center line of the via as shown in Table 7.1 below.

Table 7.1: Summary of simulation tests performed with different inlet velocity.

Via Size	Inlet Velocity	
V0 (Small via)	0.1 m/s	1 m/s
Large Via	0.1 m/s	1 m/s

A small via is defined in this chapter as a via with a depth of ~25µm and a top diameter of ~35µm. A large via is defined as via with a depth of ~200µm and a top diameter of ~150µm. The actual system was estimated to operate between an inlet velocity of 0.5~1m/s which falls within the range of the simulation tests conducted. Figure 7.3 shows the velocity magnitude obtained at the mouth of the via for each of the inlet velocity conditions on small and large via geometry.

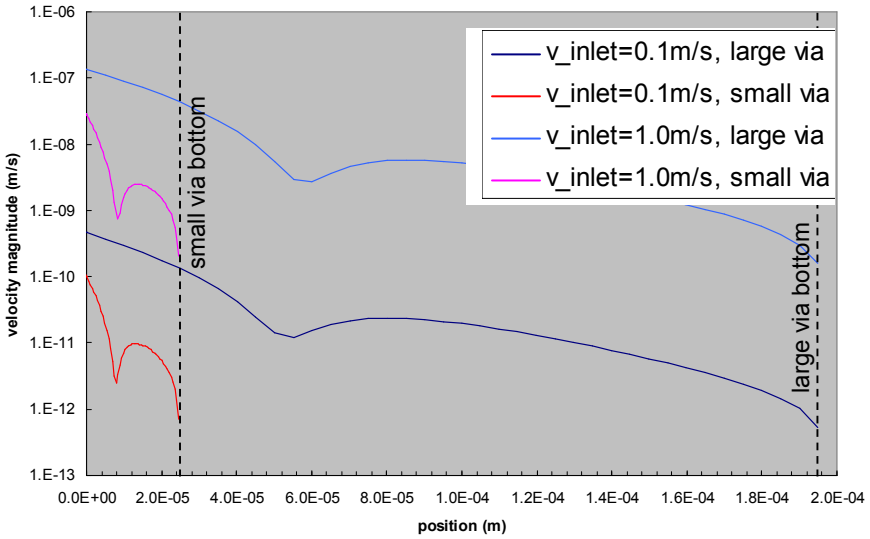


Figure 7.3: Velocity Magnitude along the center line of the via

Computing the Pe number now becomes straight forward with the availability of these velocity magnitudes. Table 7.2 summarizes the fluid velocity at the mouth of the via and the corresponding Pe number for different inlet velocity.

Table 7.2: Summary of Peclet number with different inlet velocity

Via Size	Inlet Velocity	Fluid Velocity at the mount of the Via (m/s)	Via Depth (m)	Diffusion Cofficient of Cu (m2/s)	PE (Peclet number)
V0 (Small via)	0.1 m/s	1.00E-11	2.50E-05	7.20E-10	3.47E-07
V0 (Small via)	1 m /s	5.00E-09	2.50E-05	7.20E-10	1.74E-04
Large Via	0.1 m/s	5.5E-10	2.00E-04	7.20E-10	1.53E-04
Large Via	1 m /s	1.00E-07	2.00E-04	7.20E-10	2.78E-02

For a via of 25µm depth with the Cu^{2+} diffusion coefficient around 7.2E-06 cm^2/s , Pe number measures <<1 for different via sizes and inlet velocity. Given that Pe <<1, for the purposes of this simulation study the impact of flow velocities / convection inside vias can be considered to be very small and negligible.

Section 7.2 Ohmic potential distribution effects

Migration represents movement of the ions due to an applied electric field. Given the presence of a supporting electrolyte with high concentration of protons, the migration effects can be considered negligible overall. Furthermore, Tafel kinetics can be utilized to determine the degree of non-uniformity caused by ohmic potential distribution. For larger cathodic overpotential 5mV, Wagner number can be estimated to indicate the degree of importance of the electrode kinetics. A low Wagner number ~0 indicates electrical potential differences are important in determining the overall thickness distribution. Wagner number value >1 indicates electrical potential differences do not play a critical role in determining the overall current / thickness distribution. In the present system, the solution conductivity was measured to be around 140 mS/cm. W The Wagner number, assuming Tafel kinetics is

$$Wa_T = \frac{RT\kappa}{\alpha_c FL\left|i_{avg}\right|} \tag{7.2}$$

Utilizing values of $\alpha_c = 0.5$ and $\kappa = 140mS/cm$, $L = 25\mu m$, $i_{avg} = 500A/m^2$, $T = 309K$, the Wagner number in equation 7.2 solves to a value of ~60. As the wagner number value of 60 is not extremely small, the above calculations indicate that in the current system, non-

uniformity in the electric potential is somewhat important at these feature scale levels. For the ease of modeling efforts, the electric potential effects where considered to be small and negligible for this simulation study. With these considerations, the simulation effort was primarily aimed to determine if the reverse pulse methodology accommodates adequate TP (throwing power) to enable void-free gap fill along with the evaluation of concentration gradients of the cupric ion species present within the via after the application of these reverse pulses.

Section 7.3 Simulation set up and discussion

The simulation process assumes that the plating reactor is well designed and operates at nearly ideal operating conditions. The current distribution on a flat substrate in the absence of via's is considered be uniform. Focus is primarily on the deposition distribution inside the Via regions. Effects or organic additives, catalyzing oxidizers etc. are not included in the simulation. For Via0 geometry, the characteristic via depth is approximately 25μm. Conservation of cupric ions species for such a geometry gives the relationship,

$$\frac{\partial c}{\partial t} = D\left(\frac{\partial^2 c}{\partial x^2} + \frac{\partial^2 c}{\partial y^2}\right) \tag{7.3}$$

Thus, this equation is solved utilizing the appropriate boundary conditions as follows. The boundary conditions are set up as follows.

At t = 0,

$$\mathbf{C = C_{bulk}} \tag{7.4}$$

$$\boldsymbol{\delta = 30\mu m} \tag{7.5}$$

$$\boldsymbol{h = 25\ \mu m} \tag{7.6}$$

at n = h(t),

$$\boldsymbol{D\frac{\partial c}{\partial n} = \frac{i}{2F}} \tag{7.7}$$

Where, n represents the derivative taken normal to boundary. When n= 0,

$$\boldsymbol{c = c_{bulk}} \tag{7.8}$$

Figure 7.4 summarizes the equations that were solved for the pulse and reverse pulse plating study. Ansys Fluent software (License purchased with Intel Corporation) was utilized to solve this problem.

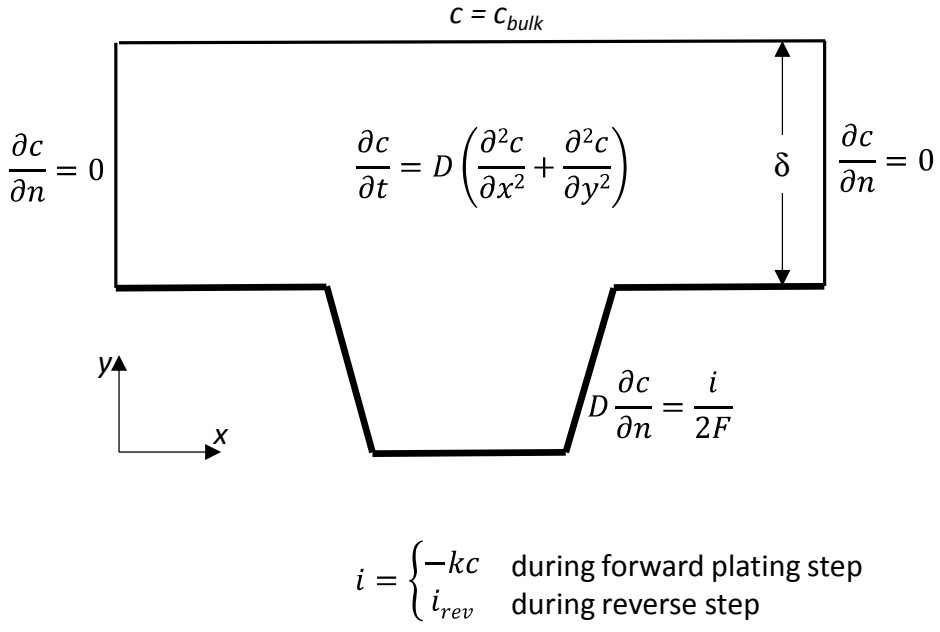


Figure7.4: Simulation set up that was utilized for simulating Reverse Pulse plating study

Here,
c = concentration of Cu^{2+} ions
c_{bulk} = bulk concentration of Cu^{2+} ions
t = time
n = represents the derivative taken normal to boundary
k = is the kinetic constant for Cu deposition
F = Faraday constant
i_{rev} = recipe-prescribed (constant) current density during reverse pulse
D = diffusion coefficient of Cu^{2+} ions
d = diffusion boundary layer thickness

The underlying physics for this problem including the assumed one step Cu deposition kinetics were taken from already published work of West *et al*.[2] In the present study, however, a 2D transient diffusion problem is solved and shape change effects of the feature as it fills with metal is ignored. The focus of the simulation is on early deposition stages only. As we are only considering the effect of concentration on *i*i at this point, the butler volmer kinetics simplifies to Tafel Kinetics which further simplifies to a linear equation as the effect of overpotential in this approach is found to small and negligible. In that case the current density i settles to a simple relationship as shown below.

$$i = \begin{cases} -kc & \text{during forward plating step} \\ i_{rev} & \text{during reverse step} \end{cases} \quad \textbf{(7.9)}$$

The goal of this study is to evaluate the throwing power or bottom-up fill performance of three reverse pulse waveform that were experimented earlier. Furthermore, a steady state capability is implemented whereby cathode overpotential at every time step is adjusted so as to maintain the target mean current density called for by the recipe. This effectively means that the kinetic constant in the first order Cu reduction expression is modulated at

every time step. Our simulation domain also includes an assumed diffusion boundary layer thickness of 30 microns – a very approximate estimate of what the actual thickness can be in actual plating reactors. However, this assumption is not likely to affect the relative performance results of plating recipes but only the magnitude of the differences among them. Figure 7.5 shows a simple schematic of the Via0 geometry that is about to be plated. Two critical time scales are key in the assumptions we have made for this simulation are described below.

(A) Diffusion time scale is based on the initial depth of the feature, l = 30μm; D=5E-06cm^2/s is the diffusion coefficient of Cu^{2+} in water: Therefore, diffusion time (t_D) approximates per equation 7.9 to ~1.8s

$$\mathbf{t_D = l^2/D} \qquad \textbf{(7.9)}$$

(B) The other relevant time scale is the time required to fill the feature which we assume is similar to the total processing time for the panel.

$$\mathbf{t_{proc} = 1800\text{-}3600s} \qquad \textbf{(7.10)}$$

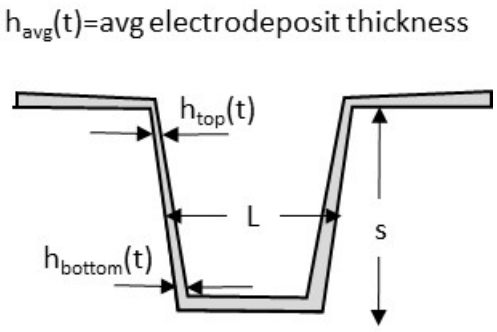


Figure 7.5: A feature with a depth s and width L prior to electrodeposition process

In our model, the shape change of the feature due to Cu metallization on its surfaces is neglected. The study only evaluates the robustness of a given reverse pulsed plating waveform to show the improvement in throwing power obtained during the early stages of deposition process ($t << t_{proc}$). At this stage, electrodeposit growth is not likely to appreciably alter the shape of the feature. In other words, if $h_{avg}(t)$ is the mean thickness deposited in the feature at given time t, this parameter is set such that $h_{avg}(t) << L$ or s of feature at all times. Adequate care has been taken to extend the the time of interest in the simulation to be long enough such that the initial diffusion transport transients effects dissipate and a a quasi-steady state is achieved. The time of interest chosen for the quasi steady state satisfies the condition: $t > t_D$ for all experiments. In order to evaluate the robustness of a fill process, the evolution of the ratio $h_{bottom}(t)/h_{top}(t)$ is tracked with time. To achieve a void-free fill, it is desirable to maximize this value.

For features that show wider diameter at the top region than at bottom, this ratio can be significantly less than 1 and still produce a good bottom-up fill result (this can be thought of as geometric levelling effect)[3]. At t=0, this ratio is unity (no depletion). With the assumed kinetics of one step Cu cation reduction and no additives present in the system, the ratio decreases with time due to a net consumption of Cu ions along the sidewall to a quasi-steady state values. Some oscillations are seen (with frequency that matches the given reverse pulse waveform recipe) around a steady average value. For recipes that lead to void-free fills, this ratio would slowly (over the fill time) approach unity as the feature fills. Hence, the argument holds true that investigation at this early

period in the process ($t_D < t << t_{proc}$) is a good indicator for evaluating the robustness of a overall plating recipe.

Section 7.4 Simulation results – DOE discussion

Simulation were carried for two specific reverse pulse waveforms that were experimentally studied earlier. Table 7.3 captures the parameters of the two waveforms that were studied.

Table 7.3: Parameters of reverse pulse WF# 1 and WF#2 utilized for simulation study

	Average Current density and Time period		Reverse Current density and Time period		Forward Current density and Time period		$\frac{T_{diss}}{T_{dep}}$	$\frac{i_{diss}}{i_{dep}} \approx (\frac{i_d}{i_p})$ West *etal*[2]
	i_{total} (A/dm^2)	T_{total} (s)	i_2 (A/dm^2)	T_2 (s)	i_1 (A/dm^2)	T_1 (s)		
WF # 1	5.0	0.08	10	0.002	5.3	0.078	0.026	1.887
WF # 2	3.4	0.08	40	0.004	5.7	0.076	0.053	7.018

WF#1 has a reverse current density of 10ASD and has a T_{diss}/T_{dep} ratio of 0.026 while WF#2 has a reverse current density of 40ASD with T_{diss}/T_{dep} ratio of 0.053. The corresponding i_{diss}/i_{dep} for each of the studied waveforms is captured in Table 7.3. Simulation efforts were then carried out on Ansys fluent systems by solving equations 7.3 through 7.9. Figure 7.4 captures the process that was solved to determine the distribution of the Cu^{2+} concentration field inside the feature. Total of 12 simulation runs were performed. Ten legs were run for 25g/l Cu^{2+} bulk concentration system. The first leg was

stopped after 1st FWD only pulse and then continued till the application of 1st REV pulse. Third simulation leg was run till a quasi-steady state was achieved. Table 7.4 captures the design of experiments.

Table 7.4: Design of Experiments for simulation tests

	Expt # 1	Expt # 2	Expt # 3	Expt # 4	Expt # 5	Expt # 6	Expt # 7	Expt # 8	Expt # 9	Expt # 10	Expt # 11	Expt # 12
Cu^{2+}(g/l)	25g/l	25g/l	25g/l	25g/l	65g/l	65g/l	25g/l	25g/l	25g/l	25g/l	25g/l	25g/l
WF #1	FWD+ REV		Steady state		Steady state							
WF #2		FWD +REV		Steady state		Steady state						
OFF #1							FWD	FWD + OFF				
OFF #2									FWD	FWD + OFF		
OFF #3											FWD	FWD + OFF

Section 7.5 Simulation results – WF #1 and WF#2 with 25g/l Cu^{2+}

Contour maps shown in Figure 7.6 includes the gradient in Cu^{2+} concentration seen after the application of the FWD duration of the first pulse (T_{FWD}) in Figure 7.6a1 followed by the REV duration of the first pulse (T_{REV}) in Figure 7.6b1 with the bulk Cu^{2+} concentration targeted at 25g/l (0.4mol/l) for a Via0 via geometry that has 30µm depth and a bottom diameter of 25µm and top diameter of 30µm. In the experimental run, these pulses are cycled and continuously till the entire deposition process is completed. (T_{total} = Duty cycle * (T_{FWD} + T_{REV})).

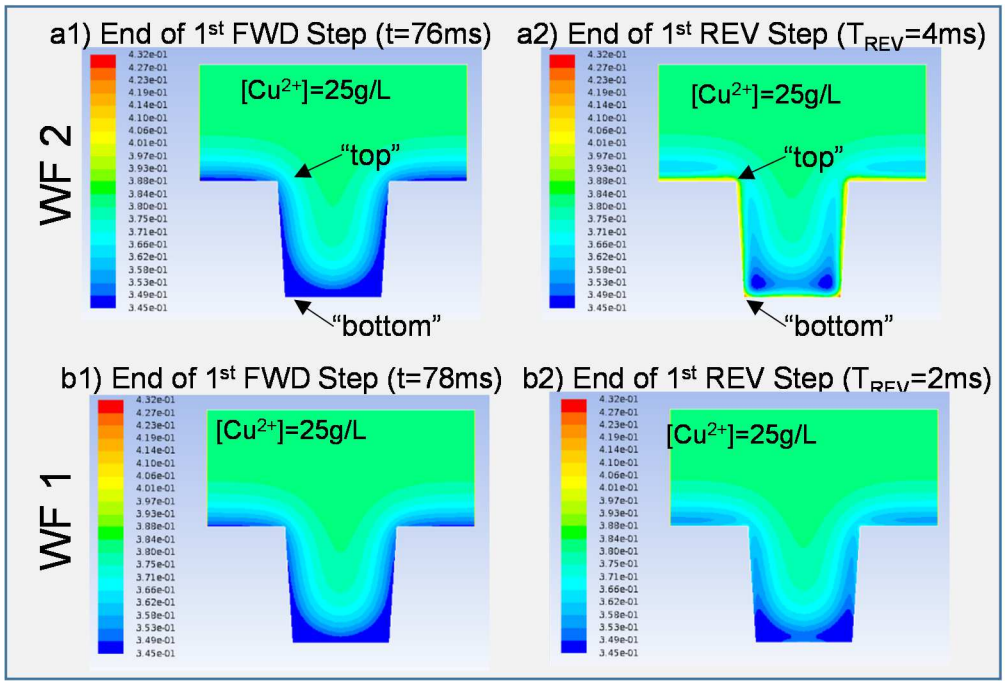


Figure 7.6: Contour maps of Cu^{2+} concentration distribution after the application of reverse pulse WF# 1 and WF#2 with 25g/l bulk Cu^{2+} concentration

As seen in the qualitative contour maps in Figure 7.6a1 and 7.6b1 after the end of 1st FWD pulse step, the bottom of the features is heavily depleted of Cu^{2+} ion (shown in blue) compared to the top. After the application of reverse pulse with WF#1, there is no adequate replenishment of copper and the bottom region still shows low amount of Cu^{2+} ion concentration. This depletion leads to thin deposit profile at the via bottom compared to the via top. WF#2 shows attenuated profile compared to WF#1 with a high local Cu^{2+} concentration generated near feature bottom surface confirming the replenishment of Cu^{2+} ion with the application of a higher reverse current compared to WF#1. However, the via bottom region is still depleted of Cu^{2+} ion confirming the via voids that were seen experimentally.

Section 7.6 Simulation results – OFF #1, OFF#2 and WF#2 with 25g/l Cu^{2+}

Experiments 7 through 12 were run with off pulse recipes OFF #1, OFF#2 and OFF#3. Figure 7.7 captures the contour map of these off pulse recipes after the 1st FWD pulse followed by an off time duration.

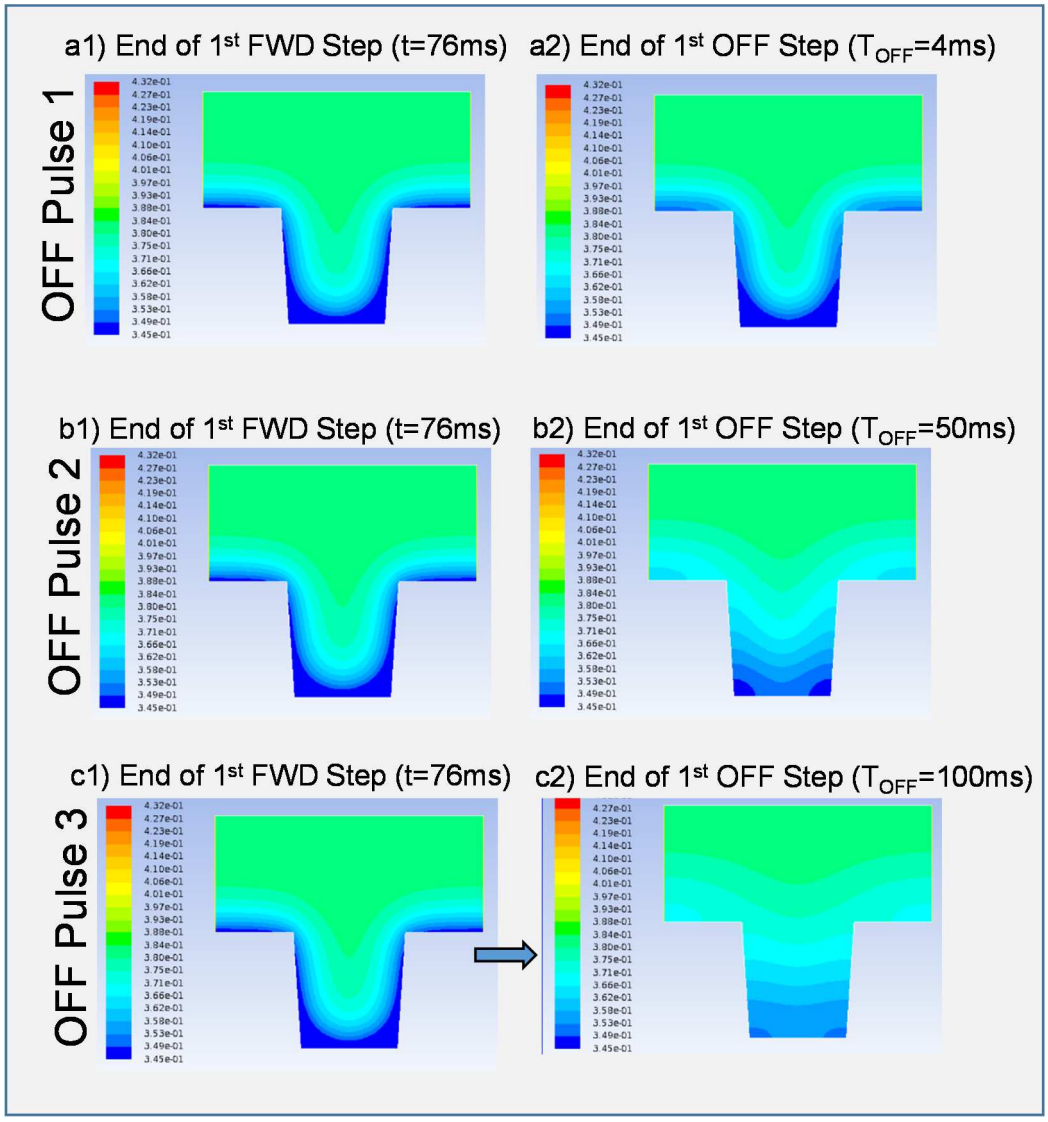


Figure 7.7: Contour maps of Cu^{2+} concentration distribution after the application of pulse recipes OFF# 1, OFF #2 and OFF#3 with 25g/l bulk Cu^{2+} concentration

As shown in Figure 7.7a1, 7.7b1 and 7.7c1 after the application of the 1st FWD only pulse, the via bottom is depleted of Cu^2 especially at the corners. When an off time duration of 4ms was applied following the 1st FWD pulse there was little change in the Cu^{2+} gradient at the bottom. However, as the off time duration is increased to 50 and 100ms [OFF #2 and OFF#3] the off time allows for some replenishment of Cu^{2+} species. Longer off times are needed to show more relaxation as the diffusion time of Cu^{2+} ions across a 30µm depth is ~1.8s.

Section 7.7 Simulation results –WF#1 and WF#2 at 25g/l and 65g/l Cu^{2+}

Before proceeding with the results from steady state simulation, the critical throwing power needed before pinch-off voids can form is estimated. Via0 geometry has a via top diameter of 38µm and a via bottom diameter of 22µm as shown in Figure 7.8. Pinch-off voids happen when the via top sidewalls collide before the via bottom is filled up. At 38µm diameter, the bottom needs to fill before via top sidewall reaches 19µm. Via bottom meanwhile has to reach a maximum radii of 11µm before the top reaches 19 µm. Therefore, the critical throwing power needed for X-section shown in Figure 7.8 is 11/19 = 0.57. Given the variation in LASER drill and lamination process, we can set the critical throwing power band region to be on the order of 0.55 – 0.6 for Via0 geometry. Any process that shows throwing power >0.6 is likely to be void-free, while those below the throwing power <0.55 are confirmed to be show voids.

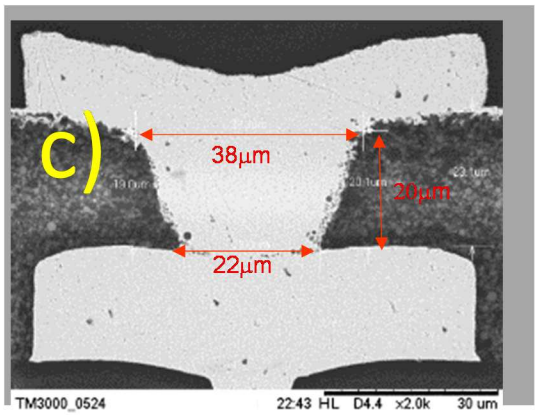


Figure 7.8: SEM X-section of Via0 geometry for critical TP calculation

Figure 7.9a and 7.9b shows the steady state data obtained for both 25g/l and 65 g/l Cu^{2+} ion concentration with WF #1 and WF #2. It is evident from from Figure 7.9a with Cu^{2+} concentration at 25g/l, at steady state both reverse pulse waveforms #1 and #2 fall well below the critical throwing power requirement of 0.55-6 and hence show pinch –off voids. Experimental SEM image results corresponding to those waveforms are captured in Figure 7.9 below. However, when the bulk Cu^{2+}concentration is increased to 65g/l, the steady state profile stay above the critical threshold of 0.55- 0.63 and do not show any pinch-off voids. The simulation shows that throwing power with WF#2 to be better than WF#1 that is confirmed with experimental data.

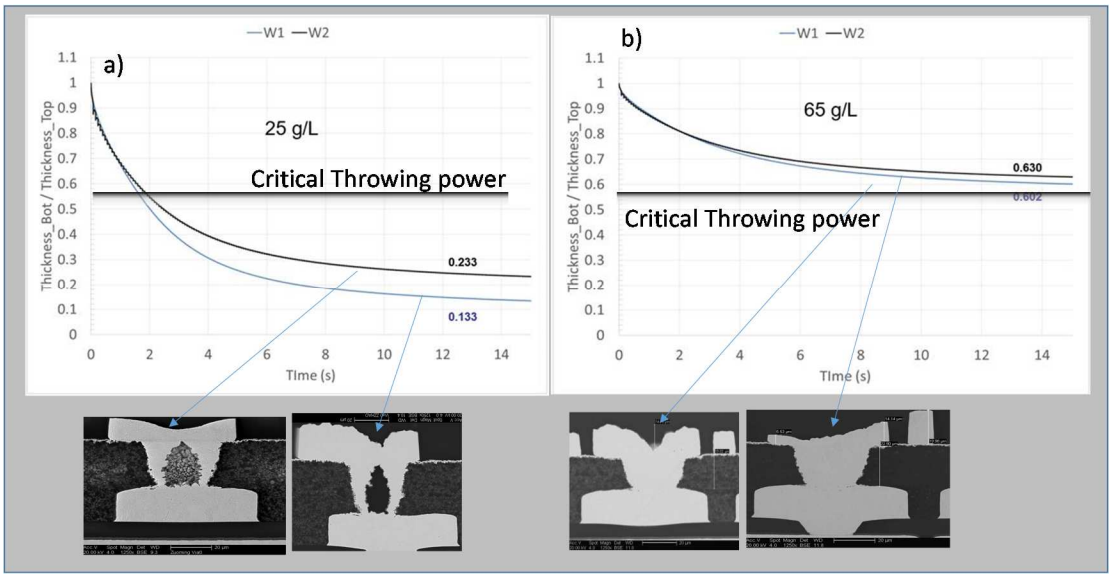


Figure 7.9: Graph of Thickness distribution ratio (Throwing power) for steady state after the application of pulse # 1 and pulse #2 with 25g/l (a) and 65g/l (b) bulk Cu^{2+} concentration

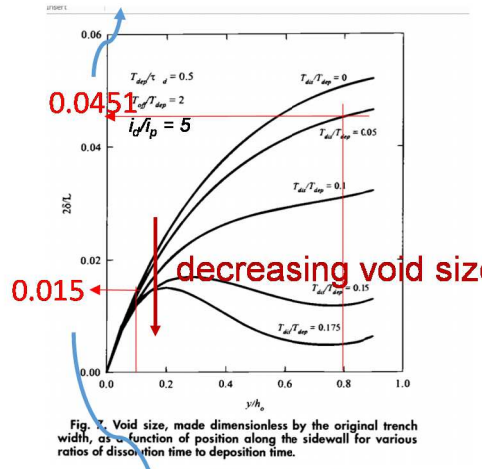
It is important to note that the simulation data accounts for bottom-up and plating behavior with reverse pulse only while the experimental data has added contribution from organic additives and oxidizers that further augment the bottom-up fill process with higher TP and buy additional margin to avoid any void entrapment.

Section 7.8 Simulation results – Comparison of results with work of West *et al*

This section compares the throwing power predicted with the present study to that of the numerical simulation work published by West *et al*[2] in their 1D approximation model to explain the role of reverse pulse electrodeposition in High aspect ratio via's. In that work[2], as shown in Figure 7.10a they plot the void size (made dimensionless by the trench width L) along the depth of the trench with X=0 as the top of the trench and

X=1 being the bottom most region of the trench. The plot shown in Figure 7.10a was simulated for the reverse pulse waveform that has $i_d / i_p = 5$. In our case, reverse pulse WF #2 has a similar ratio of $i_d / i_p = 7$ as shown in Figure 7.10b. Taking some approximate extrapolations from the curve for trench top and trench bottom for the T_{diss}/ T_{dep} ratio of 0.05 and lining them up to be the via top and via bottom in the graph to be ~20% from the absolute via top and bottom (X = 0.2 and X =0.8), we infer the via top thickness (accounting for larger opening at the via top) as 35.46μm and via bottom thickness as 22.92μm. This equates to a throwing power of 0.65 (i_{bottom} / i_{top}) which is well consistent with the value of 0.63 that is predicted with this study (Figure 7.10b).

Bottom deposit thickness (dia -2δ) = 24 – (0.0451*24) = 22.92µm



Top deposit thickness (dia -2δ) = 36 - (0.015*36) = 35.46µm

Throwing power = $\frac{i_{bottom}}{i_{top}} = \frac{23.87}{36.45} = 0.65$

a) *West *etal*[2]

b) *Present Work

	Reverse Current density and Time period		$= \frac{T_{diss}}{T_{dep}}$	$\frac{i_{diss}}{i_{dep}} \approx (\frac{i_d}{i_p})^{west\ (2)}$
	A2 (A/dm^2)	T2 (s)		
Pulse Waveform # 1	10	0.002	0.026	1.887
Pulse Waveform # 2	40	0.004	0.053	7.018

Settings of the "best case recipe" match with the recommendation that would come out of West *etal*[2] analysis.

Figure 7.10: Compare the throwing power results obtained from this simulation with that of West *et al*[2]

Section 7.9 Summary

Simulation study with WF #1 and WF#2 confirm the concentration gradient observed with low concentration of bulk copper leading to pinch off voids. At 25g/l of bulk Cu^{2+} concentration, the via bottom is severely depleted of Cu^{2+} ions leading to pinch –off voids. WF#2 with higher reverse current density helps to replenish much more Cu^{2+} ions than WF#1. At high concentrations the via bottom has even larger amount of Cu^{2+} ions leading to a steady state throwing power value of 0.63 for WF#2 and 0.6 for WF#1. Simulations with OFF time pulses show that the the off-time duration needs to be significantly longer for relaxation of Cu^{2+} ions at the via bottom region. Comparison of throwing power with WF#2 show consistent result with that from the work of West *et al*[2]. More importantly the TP obtained from WF#1 and WF#2 at 65g/l of bulk concentration of Cu^{2+} ions show that such values are well above the critical TP needed for the Via0 geometry and show a void-free, bottom-up gap fill process. Besides enabling gap fill, the choice of additives and the type of deposition parameters (temperature, bath composition, reverse pulse current, etc.,) utilized in electrodeposition process largely influences the metallurgy of the plated film. Gaining insight into grain orientation, grain size, and intrinsic stress build up and understanding their relationship to different plating conditions are key to establish the desired metallurgy of the plated film. In Chapter VIII, we investigate the impact to microstructure and mechanical properties of electrodeposited copper with different electrodeposition parameter set up and identify the critical deposition conditions that enable desired microstructure for better mechanical reliability and electrical performance.

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CHAPTER VIII

MICROSTRUCTURE CHARACTERIZATION OF ELECTRODEPOSITED FILM

Section 8.0 Introduction

Preferred crystallographic orientation of the grains developed in material processing, such as electrodeposition could result in texturing and potential anisotropic properties. Texturing and/or preferentially orientated grains can develop in electrodeposited film is based on the type of deposit parameters. Study of microstructure and texture of an electrodeposited layer enables prediction of the overall metallurgical properties of the film. In general, they are of great significance in establishing the physical and mechanical properties of the film. For example, Lee *et al* [1, 2] in their study of electrodeposited copper for IC applications show that the electrodeposited copper interconnect metals are usually polycrystalline and that grain boundary diffusion characteristics limit electro migration and stress-induced void formation. Vaidya *et al*[3] propose that migration rates are affected by three key thin film properties such as grain size, grain size distribution and texture of the film and these parameters eventually determine the electromigration lifetime. Specifically, their work prove that a strong (111) texture is associated with improved electromigration lifetime. Masataka *et al*[4] prove that hardness can be improved with reduced grain size utilizing 'Hall-Petch equation' with a threshold on grain size. Hall – Petch equation relates yield stress to grain size. This relationship suggests increase in grain boundary strengthening if there are more grain boundaries after a threshold in grain size. Schiotz *et al*[5] show that metal softening happens at very small grain sizes below a

certain threshold with "reverse Hall-Petch" coming into play. Therefore, it is needless to emphasize that study of microstructure of copper deposit could play a critical role in the industrial scale wafer and board manufacturing process for IC applications. In these applications, electrodeposited copper is usually polished / etched in various downstream operations to establish the desired circuitry[6,7]. Compatibility of copper morphology to such downstream process is key for high yield manufacturing process. Patrick *et al*[8] show that the local etch removal rate is lower for grains whose surface normals are near the (111) direction and increases as the angle between the surface normal and the (111) direction increases. Reid *et al*[6] show that the purity of copper films directly correlate to microvoid density.

Section 8.1 Literature study

Song *et al*[9] discuss that a high strength of polycrystalline copper is usually achieved with a compromise in other critical properties such as reduced conductivity. They go on to show that a film of single crystal Cu (111) can have a high density of twin growth and higher yield strength than bulk copper. The electrical resistivity of such films is also matched to bulk copper. Reid *et al*[6] & Harper *et al*[10] show increase in grain size due to self-annealing. They also show various undesired changes in crystallographic texture properties due to self –annealing. However, Lee *et al*[1,2,11] and Harper *et al*[10] went on to prove that grain coalescence / self-annealing occurs at room temperature and established that such characteristics define the surface morphology for each of the plating waveforms. In their study copper films plated with a current density of 5ASD (Amperes

per Square Decimeter) show smaller grain sizes compared to films plated at 10ASD and continue to evolve at different rate with time until a steady state is reached (~60hr). In order to properly compare the effect of different plating parameter conditions it is necessary to lock the evolution time post deposition or wait for long enough time such that a steady state is reached. Lee *et al*[1,2,11] continue to show that (111) peak intensity decreases rapidly with inreased current density and (200) signal inreases. This behavior is believed to be due to the higher energy state of the films plated at higher current densities. Finch *et al*[12] in the early 50's show that the preferred orientation of an electrodeposit mainly depends upon the substrate on which crystal is deposited and on the plating bath conditions. Panagrov *et al*[13] summarizes the influence of electroplated bath conditions on texture and preferred orientation. In his summary, he corroborates that for samples that were electrodeposited at low overpotential, the preferred orientation that was observed for FCC metals was (111). This preferred orientation changes to (100) at intermediate overvoltage's and at very high overpotential the preferred orientation further changes to (110). In the reverse pulse methodology that was discussed earlier, we should expect the various reverse pulse waveforms with increased reverse current density to show different texture and preferred grain orientation based on this analysis.

Section 8.2 Characterization methods

Majority of the literature study for copper microstructure utilize scanning electron microscope (SEM) for morphological characterization[14]. Grain size distribution and grain orientation analysis were performed through X-ray diffraction techniques. Ibanez *et*

al[15] perform micro hardness characterization with tester equipped with Vickers indenter. Hardness value (*HU*) is then calculated utilizing a formula. Lee *et al*[1] perform film textures analysis with X-ray diffraction using the Bragg-Brentano method and Schulz reflection method. In most studies, grain diameters are calculated from the measurement of each grain area assuming circular grain shape. The grain area is computed by analyses of traced images utilizing a software. Reid *et al*[6] utilize TOFSIMS analysis for surface purity.

Section 8.3 Details of present study - Focus on microstructure of flash deposited copper

In general, the electrodeposited crystals that grows from the substrate preferentially orient towards the surface upon which they are deposited or upon the bath conditions in which they were deposited. For the present study applications, an electro-less copper seed that has a preferred (220) orientation with a thickness of $1000A^0$ is utilized as the surface upon which electrodeposited Cu is built. As seen in the previous chapter VI, a flash plating process is performed on top of this seed layer to prevent dissolution of copper with reverse pulse waveforms. Utilization of strong pulse amplitudes early in the deposition stage can exaggerate the dissolution behavior leading to excessive seed dissolution and discontinuity of the deposition process. Therefore, a flash plating step with reduced reverse charge is performed to increase the thickness of the incoming seed layer before the introduction of a strong reverse pulse early in the process. Therefore, rest of this chapter will focus on the thin film properties of this flash

deposited copper than on the final film stack that was deposited with reverse pulse waveforms. The results from our ensuing experiments will show that the thin film of electrodeposited flash copper preferentially orients in (111) orientation even though they are deposited on a (220) copper seed surface and modifications of deposition parameters can significantly alter this orientation. Henceforth, the rest of this study will focus on impact of electrodeposited parameters on the above identified thin film properties.

Section 8.4 Experimental details

There were a total of 9 experiments performed for micro-characterization of the thin copper films that were deposited with reverse pulse methodology. Table 8.1 captures the process conditions that was varied between the different experiments.

Table 8.1: Experimental details for microstructure analysis

	Expt # 1	Expt # 2	Expt # 3	Expt # 4	Expt # 5	Expt # 6	Expt # 7	Expt # 8	Expt # 9
Bath Temp (C)	36	36	48	36	48	36	48	48	48
Cu^{2+} Conc.	25g/l	65g/l	65g/l	65g/l	65g/l	65g/l	65g/l	50g/l	50g/l
Reverse Pulse Current Density	8ASD	8ASD	8ASD	10ASD	10ASD	10ASD	10ASD	8ASD	8ASD
REverse Pulse Duration	2ms	2ms	2ms	2ms	2ms	2ms	2ms	2ms	2ms
Average Current Density [FWD +REV]	5ASD	5ASD	5ASD	5ASD	5ASD	5ASD	5ASD	5ASD	5ASD
Fe^{3+} Conc.	1g/l	1g/l	1g/l	1g/l	1g/l	1g/l	1g/l	1g/l	3g/l
Roughnening process	N	N	N	N	N	N	N	Y	Y
Bake	N	N	N	N	N	Y	Y	N	N

Key parameters that were adjusted include the bulk concentration of copper, bath temperature, annealing conditions and the concentration of Fe^{3+} oxidizer. An in-house SEM (Hitachi) analysis was performed to obtain images with two different

magnifications as shown in the later figures. All samples were analyzed after idling for 15+ days at room temperature. This was done to eliminate any noise in the data due to self-annealing as it is difficult to perform these analyses immediately after plating. We have discussed self-annealing behavior with electrodeposited and long idle durations (>10 days) are needed at room temperature to attain steady state grain growth. External bake could offset this limitation and a bake at 180°C for 30min was performed for some of the samples. Samples with such conditions (Expt #6 and Expt #7) would be specifically annotated during the results discussion. Copper grain structure of the all the samples were characterized by EBSD (Philips / FEI XL30 with Nordlys Nano EBSD Detector). In some cases X-ray diffraction was done to obtain details of the texture of the film. AFM (Atomic Force Microscope) analysis was done to determine the roughness of the film and Nano-indentation studies were performed to characterize the hardness of the thin films.

Section 8.5 Results and Discussion

To begin with two separate thin films were generated by varying the bulk concentration of Cu^{2+} ions in the electrolyte from 25g/ to 65g/l. All other deposition parameters were kept constant. SEM micrograph images obtained from Expt # 1 and #2 are shown in Figure 8.1.

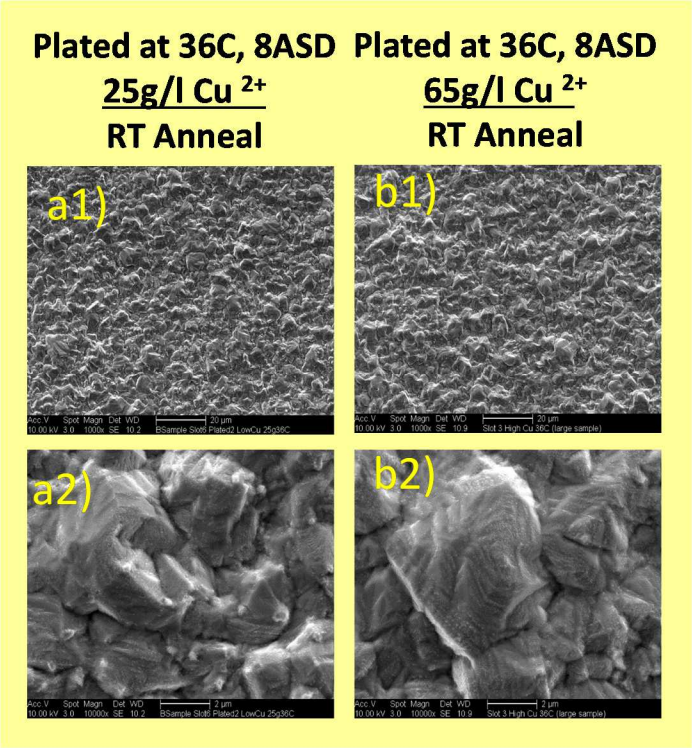

Figure 8.1: SEM micrograph of electrodeposited copper after RT anneal with a) 25g/l of bulk Cu^{2+} ion and b) 65g/l of bulk Cu^{2+} ion

From the SEM micrograph of the samples obtained with different bulk Cu^{2+} concentration experiments, it is clear that no significant variation in the characteristic of the thin film can be ascertained. No further analysis was conducted with these films. In the second set of experiments, bath temperature was varied from 36°C to 48°C. Bulk concentration of Cu^{2+} ions in the electrolyte was maintained at 65g/l for both temperature conditions and all other deposition parameters were kept constant. SEM micrographs obtained with Expt #2 and Expt #3 are the summarized in Figure 8.2.

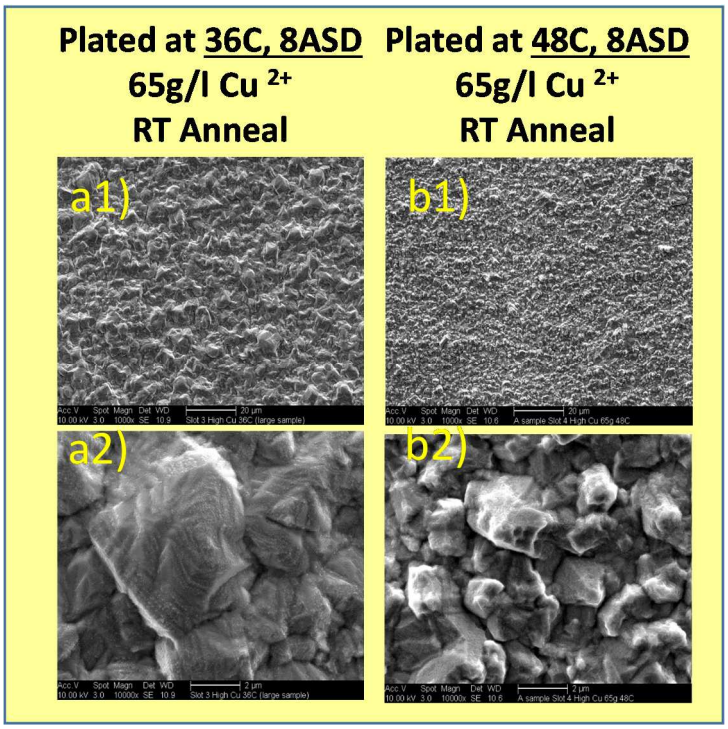

Figure 8.2: SEM micrograph of electrodeposited copper after RT anneal with 65g/l of bulk Cu^{2+} ion a) 36°C and b) 48°C

It can be inferred from the micrograph at both 2um and 20um resolutions, the films plated with 48°C show significantly smaller grain size (~x2 order of magnitude) compared to the electrodeposited copper films generated at 36°C. In order to understand if this reduced grain size effect is real, the same set of experiment conditions were repeated at a slightly higher reverse current density of 10ASD as Expt #4 and Expt #5. Here again only the temperature of the bath was changed between the two experimental conditions, whose results are compared. Comparison of SEM micrographs shows consistent results with grain size reduced at 48°C compared to 36°C as shown in Figure 8.3.

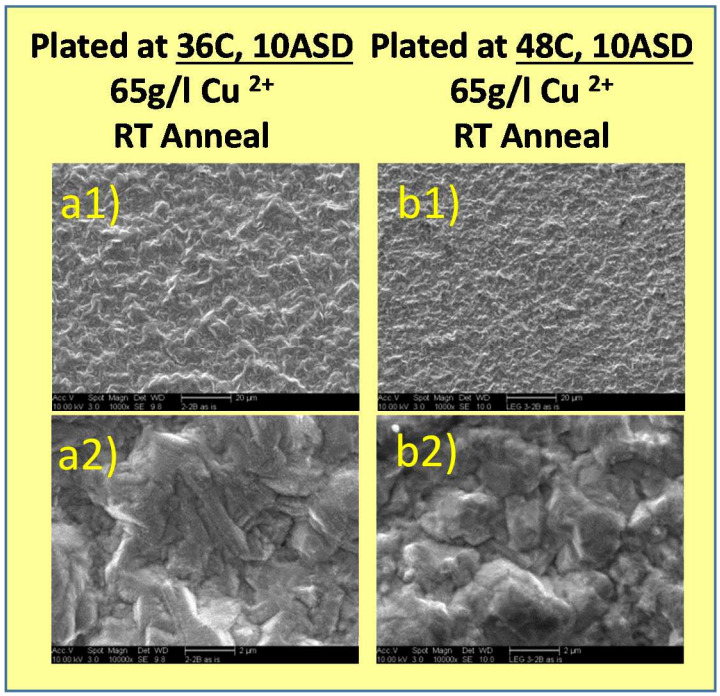

Figure 8.3: SEM micrograph of electrodeposited copper after RT anneal with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C and b) 48°C

In the next set of experiments, annealing was done to enable the samples to steady state grain growth with the same experimental conditions. Annealing was performed to confirm if the different temperatures applied during electrodeposition affects nucleation or the ensuing grain growth characteristics post electrodeposition. Therefore, two different samples were generated with identical deposition parameters as Expt #4 and Expt #5, but this time the samples were immediately baked at 180°C for 30min post electrodeposition. Figure 8.4 captures the SEM micrographs from those experiments and the results continue to show consistent behavior with earlier tests were grain size is smaller at higher plating bath temperatures. The increased nucleation that led to smaller grain size at 48°C can be attributed to the increased activity of the accelerator at those temperatures[16]. Many literatures show a columnar grain growth at high concentrations of

accelerator but it is difficult to decipher from the SEM micrographs here if columnar growth is present.

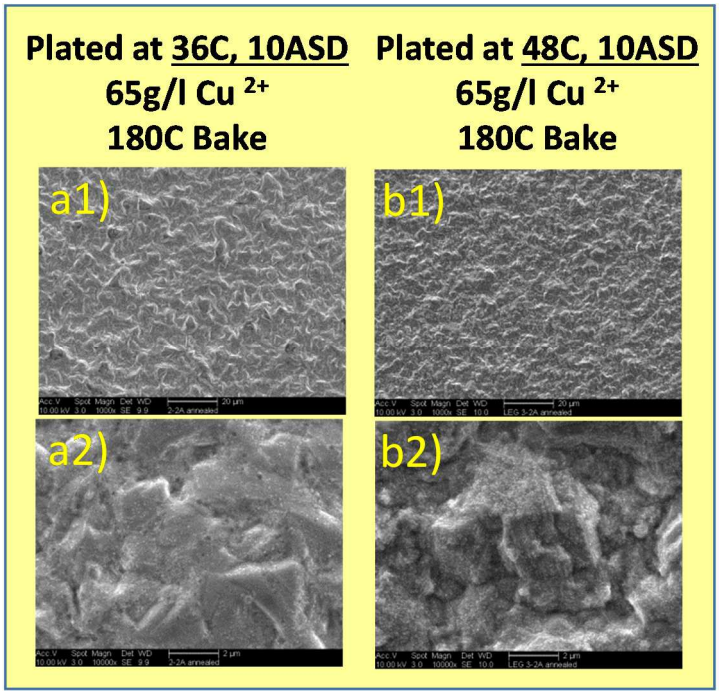

Figure 8.4: SEM micrograph of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C and b) 48°C

To further understand the texture and morphology differences at the different bath temperatures, an EBSD (Electron back scatter diffraction) analysis was performed to ascertain the difference in grain sizes. The data obtained with EBSD measurements are shown in Figure 8.5. Electron Back-scatter diffraction data confirms that samples electrodeposited with 48°C bath temperature show much finer grain sizes especially near foot while the samples plated at 36°C bath temperature show significantly larger grain sizes. Average grain sizes after accounting for variation in grain diameter indicates that the 36°C bath has >2X order increase at low temperature than at high temperature. Pole

diagrams shown on the left for both cases also show (111) preferential orientation at both temperatures.

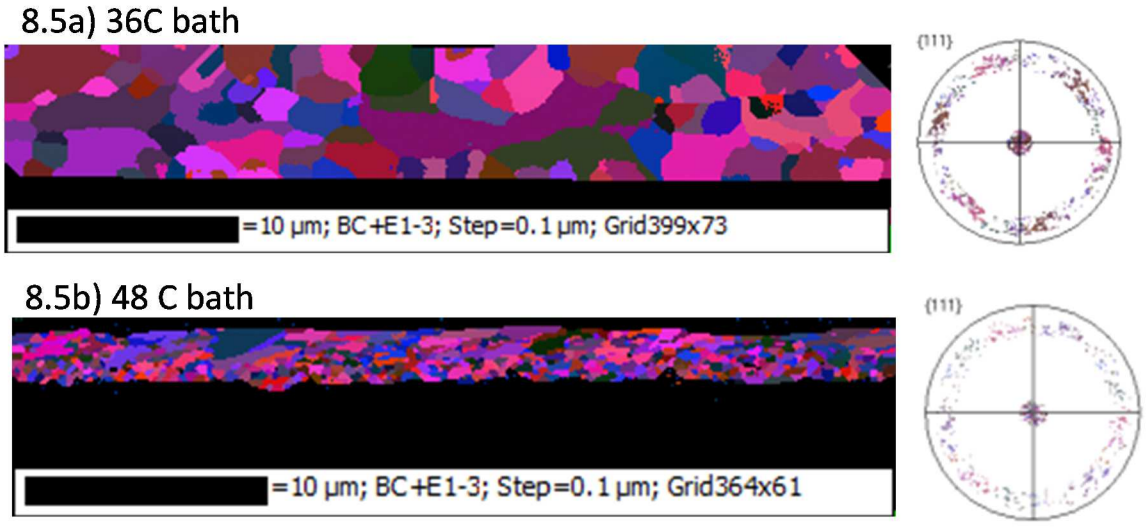

Figure 8.5: EBSD of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C and b) 48°C

XRD (X-ray diffraction) analysis were then performed to analyze the texture of the two films. Figure 8.6 shows the summarized data obtained after XRD analysis. PANalytical XPert Pro MRD system with X-ray wavelength CuKα of 1.54nm operating at 45kV currently at LeRoy Eyring Center at Arizona State University was utilized for this measurement. As shown in Figure 8.6, a strong (111) preferential orientation is observed for 36°C (86%) and a slightly reduced (111) orientation (66%) was observed for 48°C with a corresponding uptick in (311) family of planes (25% Vs 11%) at 48°C compared to 36°C.

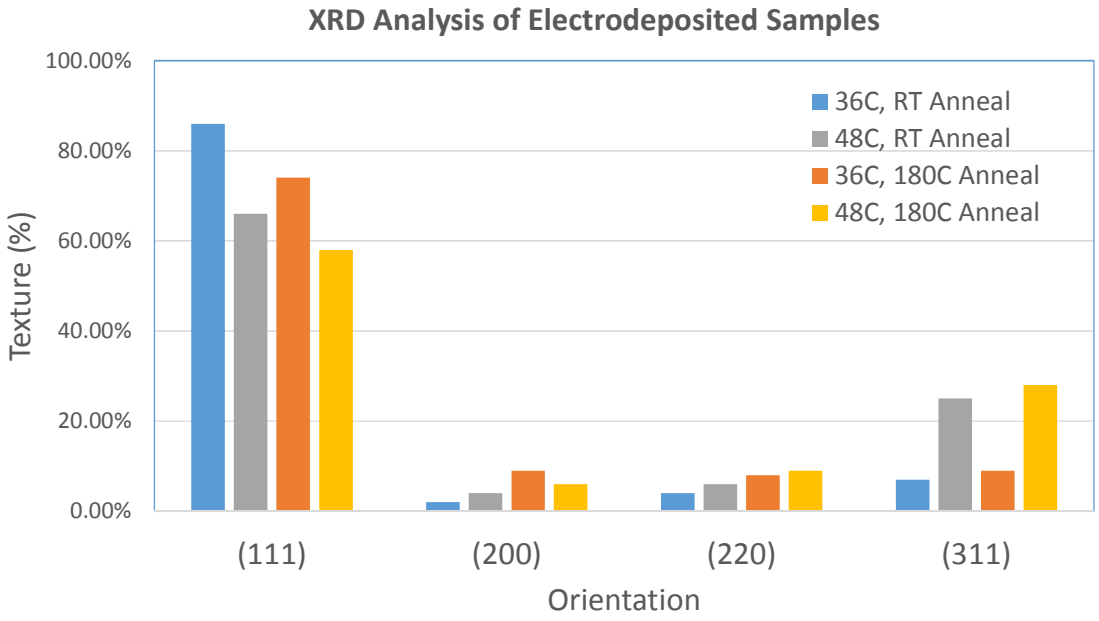

Figure 8.6: Texture of electrodeposited copper after 180°C bake and RT anneal with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C and b) 48°C obtained from XRD

AFM top down images shown in Figure 8.7 further confirm that samples with 36°C bath temperature have nearly >2x increase in grain size compared to samples at 48°C. These datasets are consistent with EBSD data that was collected earlier. Furthermore, roughness measurements of the samples were done with AFM and it was found that the plated film overall has very roughness with the samples plated at 36°C showing much higher roughness (415nm) than those plated at 48°C bath temperature (330nm). This variation in roughness is likely attributed to the larger grain size and due to less dense nucleation at 36°C compared to 48°C. The AFM analysis was conducted with an in-house measurement system at Intel Corporation, Chandler, AZ, facility. The roughness images obtained with AFM are shown in Figure 8.8.

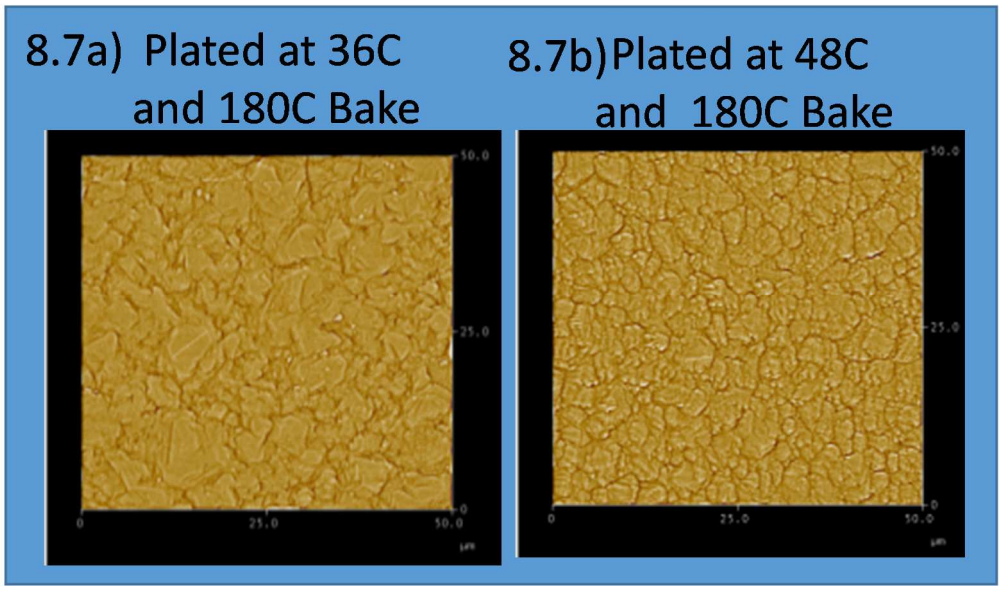

Figure 8.7: AFM Top down image of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C and b) 48°C

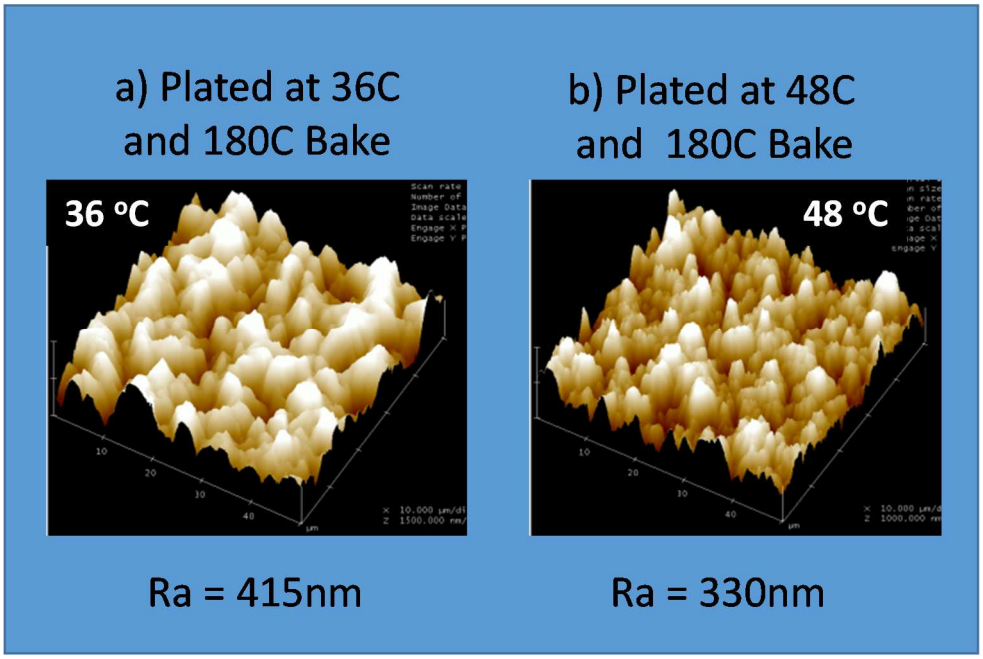

Figure 8.8: AFM roughness map of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C and b) 48°C

Lastly, intrinsic stress values were computed from XRD analysis on the flat surfaces using the conventional $\sin^2\Psi$ method [17,18]. The calculated stress numbers are plotted in Figure 8.9. A cartoon on the left shows how a compressive stress on a substrate could lead to buckling of the substrate.

Figure 8.9: Residual stress chart of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C and b) 48°C

Surprisingly, a sharp distinction in stress behavior was observed at 36°C and 48°C. For example, a compressive stress was observed at (111) orientation for 48°C with lower grain size microstructure while a tensile stress with larger grain size was observed for the same orientation at 36°C. This data confirms that the choice of plating bath temperature has a significant impact on the intrinsic stress built in the film. The reduced hardness for 36°C samples is hypothesized to its larger grain size, and the larger hardness at 48°C is attributed to the fine grains based on "Hall-Petch effect" relationship of yield stress to grain size.

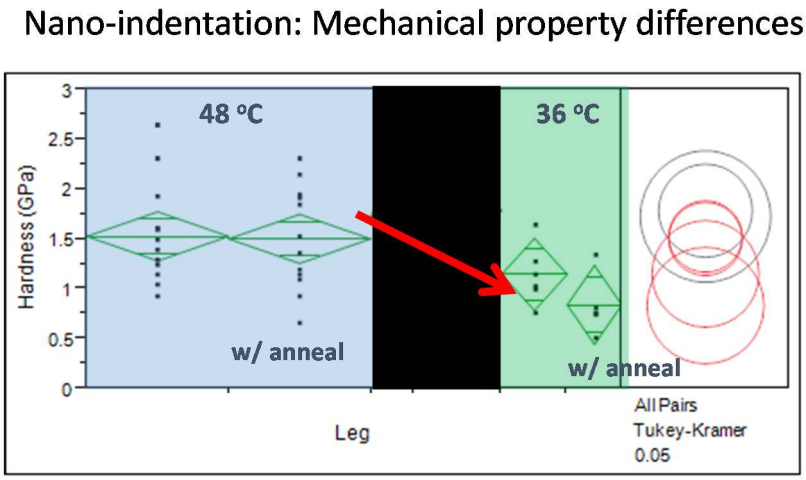

Figure 8.10: Hardness of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C and b) 48°C

Lastly, in order to understand the impact of Fe^{3+} oxidizer, two different experiments were performed with the bulk concentration of Cu^{2+} ions maintained at 50g/l and the bath temperature at 48°C. Fe^{3+} concentration was varied between 1g/l and 3g/l for experiments Expt #8 and Expt #9. The increase in the oxidizer concentration is expected to limit the growth rate of the copper grains, as Fe^{3+} is a strong oxidizer and can easily etch away electrodeposited copper through the reaction 8.1 shown below.

$$\boldsymbol{2Fe^{3+} + Cu \leftrightarrow Cu^{2+} + 2Fe^{2+}} \qquad \textbf{(8.1)}$$

Based on this reaction mechanism, it can be inferred that in the presence of an oxidizer in the system (Fe^{3+}), the grain size of electrodeposited copper is always adjusted real time as it nucleates. When the concentration of the oxidizer is increased further to 3g/l, it is natural that the grain sizes are reduced further due to the increased etching activity of the Fe^{3+} oxidizer. SEM micrograph images shown in Figure 8.11 confirm that with increase

in concentration of oxidizer in the electrolyte solution, the grain size is reduced further. No further analysis were conducted with these films.

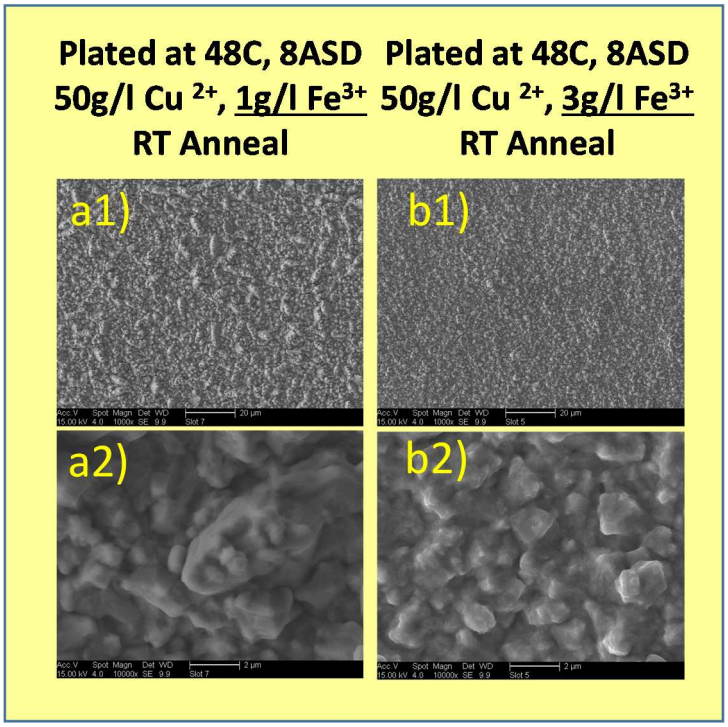

Figure 8.11: SEM micrograph of electrodeposited copper after RT anneal with 65g/l of bulk Cu^{2+} ion and 8ASD reverse current at a) 1g/l Fe^{3+} and b) 3g/l Fe^{3+}

Section 8.6 Summary

In summary microstructure analysis of electrodeposited copper reveal significant differences in film characteristics with modifications in deposit conditions. In this study, various electrodeposit parameters that affect flash deposited copper were studied. Key parameters that were adjusted include the bulk concentration of copper, bath temperature, annealing conditions and the concentration of Fe^{3+} oxidizer. An in-house SEM (Hitachi)

analysis was performed for all the measurements. Bath temperature shows significant change in grain size with increased temperature. It is hypothesized that at increased temperatures the energy barrier for reduction reaction is minimized compared to deposition reactions with similar conditions but at reduced temperatures. With the lowering of energy barrier, it is highly likely that there is a higher propensity of nucleation or an increased nucleation rate at the surface (easier facilitation of the deposition reaction). Such increased nucleation rate leads to frequent formation of fresh grains than the growth of existing nuclei. Therefore, with the incorporation of reverse pulse process, at elevated temperatures (48^0C in this case) smaller grain sizes are observed due to increased nucleation rate when compared to reduced temperatures of 36^0C. XRD, EBSD, AFM and nanoindentation tests show that 48°C temperature has compressive intrinsic stress and smaller grains compared to tensile stress and larger grain size at 36°C. It has been shown that when a fresh grain size is formed it tends to remain compressive and as grains grow they tend to be tensile[17]. The presence of compressive stress at 48^0C is thus consistent with our earlier hypothesis of higher nucleation rate and frequent formed fresh grains at 48^0C compared to 36^0C. At 36^0C, where larger grain sizes were observed, it is likely that the intrinsic stress changing from compressive to tensile stress during grain growth.

So far, we discussed the extension of reverse pulse methodology to Via0 and Via1 geometry and the ensuing microstructure for IC substrate applications. There is another unique class of via geometry termed V5 in IC substrates that has fiber protrusion inside the via. In Chapter IX we study the challenges associated with gap fill for such a

geometry and identify additional knobs for improving throwing power besides optimizing reverse pulse methodology to enable void-free fill.

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CHAPTER IX

GAP FILL METHODOLOGY FOR VIA'S WITH GLASS FIBER PROTRUSION

Section 9.0 Introduction

In chapter VI, we discussed the ability of reverse pulse methodology to enable void-free gap fill for via dimensions Via0 and Via1 that are used in IC substrate applications. Via0 has a geometry of ~25µm depth with a via bottom diameter of ~25µm, which leads to an aspect ratio of 1.0. Via1 has a depth of ~25µm but with much larger opening sizes (diameter of ~50um) which leads to an aspect ratio of 0.5. As discussed before, these via's (Via0 and Via1) are drilled through a dielectric film to enable I/O routing and ground plane connections between an active die and the mother board. IC substrates also include another class of via dimensions termed Via5 in this study. The uniqueness of the Via5 geometry is that it is generated using a LASER on a glass cloth reinforced dielectric film instead of a normal dielectric film. Typically, the depth of the via ranges on the order of ~65um and the via bottom diameter is on the order of ~55µm to ~60µm. Furthermore inside the via , there are always fiber protrusions extending inside the via, normally on the order of ~9µm to 10µm from the via side walls to the center. These fiber extensions protruding inside the via demand a unique challenge for bottom-up gap fill process. Copper electrodeposited at the fiber protrusions have the propensity to collude before any bottom fill can happen due to the small opening area present at those locations compared to the via bottom. Electrodeposit growth at the fiber protrusion region needs to be reduced compared to the growth rate via top and via bottom to avoid pinch-off.

Otherwise, the likelihood of void entrapment is highly likely. Unique approaches and innovations are needed to develop a methodology that shows bottom-up fill process without void entrapment for such via's with fiber protrusions and is the focus of the study below. Figure 9.1 shows the top down and cross-sectional view of a Via5 geometry generated on glass fiber reinforced dielectric film. In Figure 9.1b, the dielectric film is uniformly coated with a copper seed surface. Fiber's protrusions can be seen extending ~9um to ~10um from the sidewalls roughly at center region of the via. Given the limitations of the upstream processes, the location of fiber protrusion inside the via can vary widely. As shown in Figure 9.2 fiber protruding at ~10um from the sidewalls are seen at various locations such as top, middle and bottom location along the depth of the via.

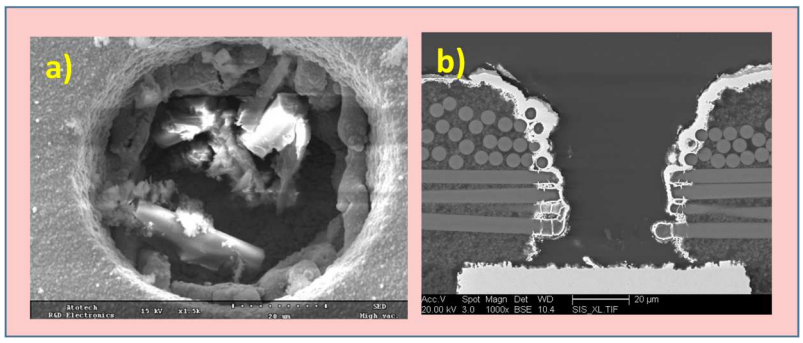

Figure 9.1: a) Top-view and b) cross-section view of a Via5 via prior to electrodeposition

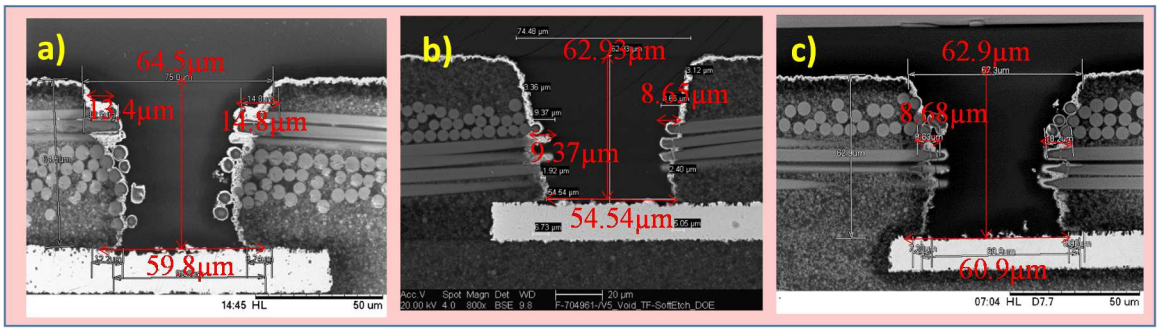

Figure 9.2: Cross-section view of a Via5 via prior to electrodeposition with copper seed surface and fiber protrusions extending at ~10um from the sidewalls along the various positions within the depth of via such as fiber protrusion at via top (a), fiber protrusion at via bottom (b) and fiber protrusion at via middle (c) In all cases, the coverage of the seed layer was found to be continuous and

uniform along the length of the via with the thickness of the copper seed to be measured around ~2um. Henceforth, the via of this geometry will be referred to as via5 and will be the focus for further discussion below.

Section 9.1 Design of experiments – experiments #A through #J

In chapter VI, we showcased a reverse pulse methodology to gap fill Via0 and Via1 dimensions. In this study, a similar attempt was made to generate void-free gap fill inside Via5 geometry. To begin with, 9 sets of experiments (Expt # A through J) in three set of batches (Batch 1 – Expt A,B,C; Batch 2- E,F; Batch 3- G, H, I, J) were performed with exactly similar parametric conditions to those attempted at enabling void-free free on Via0 and Via1 geometry. Experimental details are summarized in Table 9.1. The shape and amplitude of revere pulse waveforms #1, #2 and #3 that were utilized in these experiments are tabulated shown in Table 5.2 and Figure 5.5 (Chapter V).

Table 9.1: Experimental run card (Expt # A through J) for Via5 Gap fill evaluation

	Parameters	Expt A	Expt B	Expt C	Expt E	Expt F	Expt G	Expt H	Expt I	Expt J
Flash Cu	Cu2+ (g/l)	25	25	25	65	65	65	65	65	65
	Temp ©	36	36	36	36	36	36	36	36	36
	Pump Agitation (Hz)	15	15	15	30	30	30	30	30	30
	Reverse Pulse CD	10	10	10	10	10	10	5	10	5
	Reverse Pulse Duration (ms)	2	2	2	2	2	2	2	2	2
	Forward Pulse Duration (ms)	78	78	78	78	78	78	78	78	78
	Reverse Pulse Waveform ID	1	1	1	1	1	1	1b	1	1b
	Total Duration (s)	450	450	450	550	550	550	1100	550	1100
Via Fill	Cu2+ (g/l)		25	50	65	65	65	65	65	65
	Temp ©		36	48	36	36	36	36	36	36
	Pump Agitation (Hz)		15	13	13	13	30	30	13	13
	Reverse Pulse CD		10	40	40	24	10	5	40	20
	Reverse Pulse Duration (ms)		2	4	4	4	2	2	4	4
	Forward Pulse Duration (ms)		78	76	76	76	78	78	76	76
	Reverse Pulse Waveform ID		1	2	2	3	1	1b	2	2b
	Total Duration (s)		1250	900	900	600	950	2400	900	1800

Section 9.2 Results and discussion

Section 9.2.1 Results: via5 experiments #A through #C

Figure 9.3a shows the SEM cross-section of a Via5 after flash plating deposition (Expt #A). Flash plating is always performed because of concerns of seed dissolution during early part of the process. Flash plating of this layer was performed for a duration of 450s utilizing reverse pulse waveform #1 with the concentration of the Cu^{2+} ion maintained at 25g/l, 36°C. The pump agitation was controlled at 15Hz. As seen from Figure 9.3a, the thickness of the deposit looks continuous with the thickness of the deposit measured at the via top region at ~2X or larger than at the via bottom. In order to understand the true extent of the variation of the thickness of side walls at the top and bottom of the via, the plating process was further continued with the same parametric deposition conditions for

an additional 1250s as Expt #b. The SEM cross-section from Expt #b is shown in Figure 9.3b. The thickness of the sidewalls looks higher at the via top region than at the bottom leading to lower throwing power (Thickness $_{bottom}$ / Thickness $_{top}$) and more importantly, due to the inherent nature of glass fiber protrusion present inside Via5 geometry, the size of the via opening at those fiber locations looks much smaller than at the via bottom and has a high propensity to collude and trap a void underneath with any further extension in the deposition process with similar parametric conditions. In Expt # C, after flash deposition process, in order to generate improved bottom-up fill, reverse pulse methodology that was earlier attempted for Via0 and Via1 was tested for Via5 with revere pulse waveform #2 that has a high reverse current density of 40ASD for a pulse duration of 4ms. The concentration of the bulk Cu^{2+} concentration was doubled to 50g/l to mitigate any mass transfer limitations and the temperature of the bath was increased to 48°C from 36°C to improve the mobility of ions to the via bottom and the overall deposition rate along with faster nucleation.

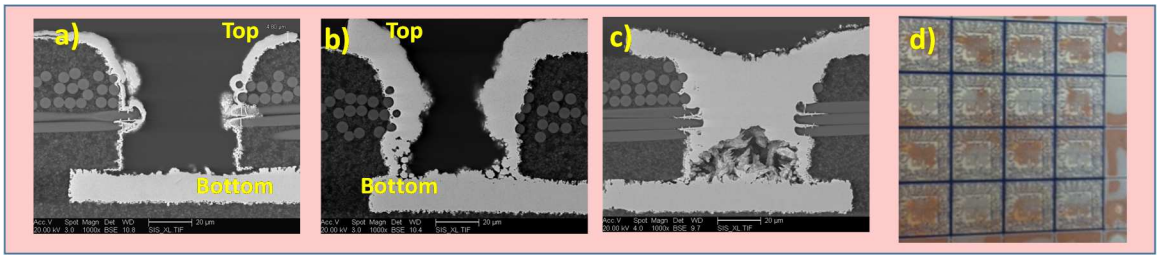

Figure 9.3: a) Flash deposited via with 25g/l of Cu^{2+} ions, b) Via fill with reverse pulse #1 post Flash Cu with 25g/l of Cu^{2+} ions, c) Via fill with reverse pulse #2, 50g/l of Cu^{2+}, 48°C post Flash Cu with 25g/l of Cu^{2+} ions, d) Non-uniform pattern observed with Expt # C

As shown in Figure 9.3c, even with the incorporation of all these capable knobs via void was entraped due to the impingement of copper plated on the fiber protrusions before any bottom-up fill process can happen. In expt # C, the surface of the coupon, post deposition is patchy and resembles a "honey comb" like pattern that corresponds to non-uniform thickness distribution. The surface of the copper is highly non-uniform due to the application of high reverse current repeatedly or a long duration of time. The applied high reverse current generates non-uniform surface thickness on the surface rather than a gap fill inside the via. The large pinch-off void observed inside the via region confirms this mechanism further and indicates that momentum plating was established after sidewall collusion happened leading to non-uniform copper on the ensuing top surface. Figure 9.3d shows a top view microscope image of the highly non-uniform patter observed on the surface post deposition.

Section 9.2.2 Results: via5 experiments #E through #F

In order to eliminate, pinch-off voids and regulate large scale non-uniformity observed on the surface, in the second batch of experiments, experiments E through F, the bulk concentration of the copper was increased to 65g/l for the entire deposition process to minimize any mass transfer limitation of Cu^{2+} ions at the via bottom sidewalls.

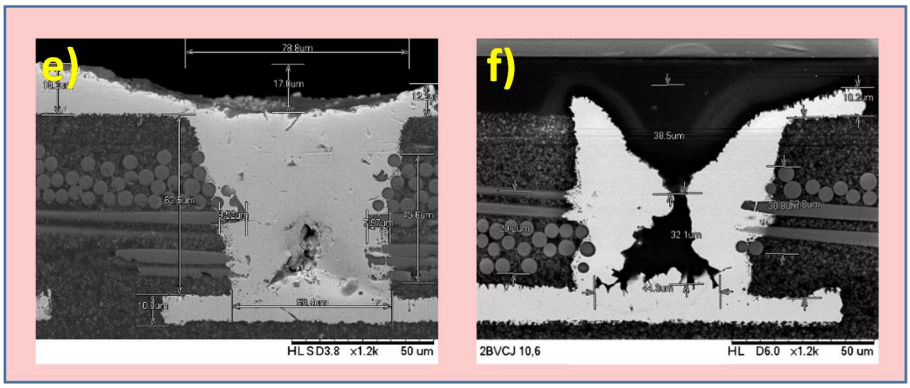

Figure 9.4: e) Via fill with reverse pulse #2 post Flash Cu with 65g/l of Cu^{2+} ions (Expt #E), f) Via fill with reverse pulse # 3 post Flash Cu with 65g/l of Cu^{2+} ions (Expt # F)

In experiment Expt # E, via fill was performed with a reverse current density of 40ASD for 4ms. In Expt #F, the reverse current density was reduced to 24ASD for 4ms. These waveforms at high bulk concentration of Cu^{2+} ions have previously resulted in void-free fill for Via0 and Via1 geometry. However, with Via5 geometry due to the presence of fiber protrusions, the throwing power generated with the reverse pulse methodology was not adequate to eliminate pinch-off at fiber protrusion regions leading to entrapment of voids as shown in Figure 9.4e and 9.4f. It is also important to note that there is no significant deposition seen from the bottom pad region of the via or on the via sidewalls corners.

Section 9.2.3 Results: via5 experiments #G through #J

Takahashi and Gross have previously outlined which phenomena dominate current distribution on ≤1micron feature scales.[1] Distribution of an electroplated deposit depends upon which transport phenomenon controls the plating rate, such as inadequate mixing, so that reactant concentrations are not uniform (convection effect), or by spatial

variations in the electrical-potential difference across the electrode/electrolyte interface or due to concentration gradient (diffusion). If diffusion limitation dominates the overall charge distribution at the bottom of the via, assuming the spatial variations in the electrode –potential difference across the electrode-electrolyte interface and inadequate mixing effects were assumed to be minimal and negligible then an increase in concentration of Cu^{2+} ions or reduction in the deposition current density should aid in attaining similar via bottom thickness as at the top. Diffusion time scale based on the initial depth of the feature can be easily estimated using equation 9.1 shown below

$$t_D = l^2/D \qquad (9.1)$$

where, l = 65µm (depth of the feature) and D =7.2E-06cm^2/s is the diffusion coefficient of Cu^{2+} in water: Based on equation (9.1), the diffusion time (t_D) approximates per equation 5.87s shown in Table 9.2.

Table 9.2: Estimation of diffusion time for Via5 feature geometry

Ion	D (cm^2/s)	h (cm) = depth	t_D (s)
Cu^{2+}	7.2E-06	0.0065	5.87

Therefore, in order to eliminate any diffusion limitation effects and prevent depletion of Cu^{2+} ions at the via bottom, the concentration of bulk was maintained at 65g/l of Cu^{2+}ions for all experiments going forward. For some of the experiments, reduced deposition rates was also explored. In order to understand the limitation of the current system and the throwing power obtained with the existing parameters, four set of experiments (Expt #G

through #J) were performed at 36°C with the bulk concentration of Cu^{2+} ions maintained at 65g/l utilizing reverse pulse waveform #1 and #2. Experiment # H and # J were performed with half the current density as that was utilized earlier for reverse pulse waveform #1 and # 2 as reverse pulse waveform #1b and #2b. The shape and current density of the waveforms that were utilized in the experiments are captured in Figure 9.5 below for reference.

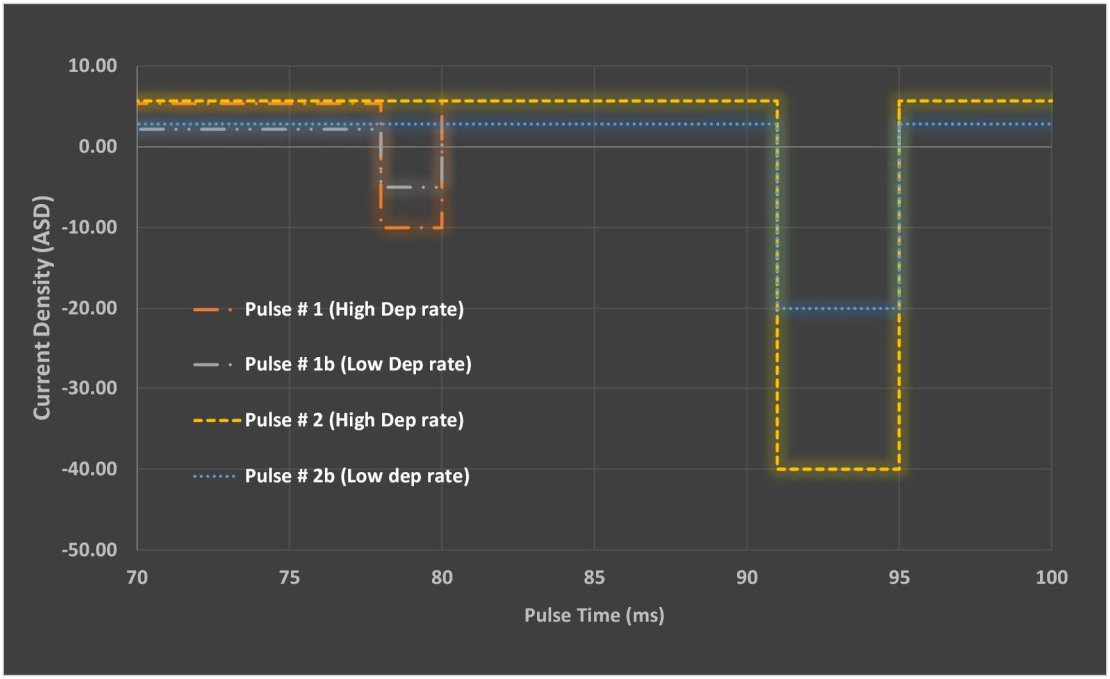

Figure 9.5: Reverse Pulse waveforms (#1, #1b, #2, #2b) utilized for expt #G (#1, high dep rate) , expt #H (#1b, low dep rate) , expt #I (#2, high dep rate) , expt #J (#2b, low dep rate)

In reverse pulse waveforms #1b and #2b, both the forward and reverse current density were reduced in half but the corresponding reverse time durations were kept the same. Table 9.3 shows the exact current density parameters that were utilized in these waveforms.

Table 9.3: Reverse Pulse waveforms parameters for #1, #1b, #2, #2b that were utilized for expt #G (#1, high dep rate) , expt #H (#1b, low dep rate) , expt #I (#2, high dep rate) , expt #J (#2b, low dep rate)

	Average Current density and Time period		Reverse Current density and Time period		Forward Current density and Time period	
	i_{total} (A/dm^2)	T_{total} (s)	i_2 (A/dm^2)	T_2 (s)	i_1 (A/dm^2)	T_1 (s)
Pulse Waveform # 1	5.0	0.08	10	0.002	5.38	0.078
Pulse Waveform # 1b	2	0.08	5	0.002	2.19	0.078
Pulse Waveform # 2	3.4	0.08	40	0.004	5.70	0.076
Pulse Waveform # 2b	1.7	0.08	20	0.004	2.84	0.076

Reducing the overall current density should assist in mitigating some of these mass transfer effects (if present) and aid to attain improved throwing power. The undesired consequence of reducing the current density is that it leads to increased process time to achieve the same specified target thickness. Therefore, in experiment # H and J the plating deposition time was extended 2X or longer (accounting for lower current efficiency at reduced current density) as summarized in Table 9.1. The results obtained with experiments #G through #J are shown as SEM cross-sections in Figure 9.5.

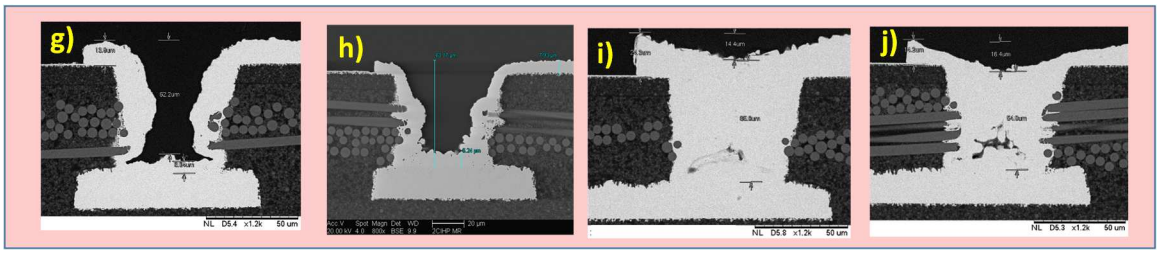

Figure 9.6: SEM micrograph of Expt #G through Expt #J
g) Via fill with reverse pulse #1 post Flash Cu at 65g/l of Cu^{2+} ions, 950s, h) Via fill with reverse pulse # 1b post Flash Cu at 65g/l of Cu^{2+} ions, 2400s, i) Via fill with reverse pulse #2 post Flash Cu at 65g/l of Cu^{2+} ions, 900s, 9.6 j) Via fill with reverse pulse # 2b post Flash Cu at 65g/l of Cu^{2+} ions, 1800s

In Expt # G, the via fill deposition process post flash Cu was performed with reverse pulse waveform #1 but the deposition process was extended to 950s. SEM micrograph of the sample post deposition is shown in Figure 9.6g. The thickness of the copper deposit at the via bottom (on the pad region) was measured to be 5.43µm. The via pad thickness on the top surface was measured from SEM cross-section to be 13.9µm. The throwing power ratio (Thickness $_{bottom}$ / Thickness $_{top}$) for this experiment #G can then be calculated to be 0.4. In Expt #H, both the flash deposition process and the via fill happened at half the forward and reverse current density with reverse pulse waveform # 1b but with the overall deposition time extended. SEM micrograph of the sample post deposition is shown in Figure 9.6h. The thickness of the pad was measured to be 7.1µm and the deposit thickness at the via bottom was measured to be 7.0. Thus, with the low deposition rate in Expt #H, the overall pad thickness is reduced to ~7µm compared to ~14um with the high deposition rate on Expt # G. However, the throwing power with Expt #H that computes to a value of 1 (Thickness $_{bottom}$ / Thickness $_{top}$) which is significantly higher than the 0.4 that was obtained on Expt # G. This indicates that

electrodeposition at reduced current density can significantly improve throwing power except that such reduced current density leads to significantly long plating durations. Similar set of experiments were then repeated with reverse pulse waveform #2 and with reduced current density #2b as experiment #I and #J. In Expt # I, the via fill deposition process post flash Cu was performed with reverse pulse waveform #2 but the deposited process was completed at 950s. SEM micrograph of the sample post deposition is shown in Figure 9.6I. The thickness of the copper deposit at the via bottom (on the pad region) is irrelevant due to the entrapment of voids that are seen. Via pad thickness on the top surface was measured from SEM cross-section to be ~7μm. In Expt #J, both the flash deposition process and the via fill happened at half the forward and reverse current density with reverse pulse waveform #2b but with the overall deposition time extended. Once again, as shown in Figure 9.6J, void entrapment is observed even at these low current densities. So far, incorporation of reverse pulse methodology alone has not yielded a void-free process for Via5 geometry that has glass cloth fiber protrusions inside the via region. Reduction in current density to mitigate the mass transfer effect and increase in bulk concentration of the electrolyte also shows void entrapment with poor bottom-up fill. Earlier with Via0 and Via1 geometry, improved throwing power leading to void-free fill were obtained with optimization of reverse pulse methodology alone, but Via5 poses a different set of challenge.

Section 9.3 Optimization of organic additive ratio and bath temperature with reverse pulse methodology

In order to identify additional knobs for improving throwing power, the ability of organic additives and bath temperature was investigated as independent knobs to improve throwing power for Via5 geometry.

It is well known that in the presence of Cl^- ion species in the electrolyte, organic additives such as accelerators enhance the corner growth rate at the via bottom and suppressors temporarily block adsorption of Cu^{1+} at the via top until displaced by the accelerator[2]. West et al studied the ratio of these additives to the ensuing throwing power for damascene applications. [3] A similar attempt was made for Via5 geometry, by performing a comparative study to generate the correlation of throwing power to various ratio of accelerator to suppressor molecules. Such a study could generate a good understanding of the ability of the organic additive to enable bottom-up fill for Via5 geometry.

Investigating the effect of Accelerator and Suppressor species independently significantly increases the number of experiments to be performed when coupled with other independent bath deposition variables such as bath temperature and reverse pulse waveforms that influence TP differently at different additive concentrations. Therefore, it was decided to consider the ratio of the additives as a single variable during the design of the experiments rather than independently varying the concentration of the two species. In the experiments conducted thus far (chapter VI - VIII), the organic ratio was maintained at 0.75 (ratio of measured accelerator to suppressor concentration). In our

testing so far, two proprietary additives namely “SBP2 Accelerator” and “SBP2 Leveler” purchased from Atotech Inc., were utilized for the experiments. The Accelerator concentration was targeted and maintained at 12ml/l while Leveler concentration was measured at 16ml/L. An analytical CV (Cyclic Voltammetry) method was utilized to measure and target the concentration of the bath periodically as needed. Overall, the concentrations were maintained within the range of ± 0.2ml/l from specified target. The exact molecular details of these species were unknown for this study and the functionality of these species were expected to behave primarily as accelerator and suppressor that are referenced in scientific literature studies. Henceforth, these species will be termed as accelerator and suppressor for rest of this study and their concentration would be varied to understand their impact on bottom-up fill for Via5 geometry.

Increased deposition temperature leads to increased mobility of the Cu^{2+} ion as well as the additive species to the via bottom. Previously, the temperature of the plating bath has been shown to affect bottom-up gap fill mechanism for Cu damascene applications[3]. In such studies lower operating temperatures (20°C) had been recommended due to the scale of the features that needs void-free fill. In the present application given the large size of the via with a critical need to enable the availability of Cu^{2+} ion and additive species to the via bottom much higher temperature such as 40°C and 48°C were studied.

Section 9.4 Design of Experiments with various organic additive ratio and bath temperature with reverse pulse waveform # 1 and # 1b

As explained earlier, the primary goal of the testing here was to identify an optimal concentration ratio of the additive at elevated bath temperature for gap fill with Via5 geometry. An experimental DOE run card was set up to investigate the effect of these variables with reverse pulse waveforms # 1. Reverse pulse waveform #1 accommodates a maximum reverse current density of 10ASD for 2ms duration. The average current density for deposition was set at 5.4ASD and plated for a duration of 950s post Flash Cu deposition. Reverse pulse #1b was performed for the same 2ms duration with the reverse current density reduced to 5ASD with the average current density for deposition reduced to 2.2ASD. Reverse pulse #1b was performed for an extended time (2400s) to accommodate for the reduced current density. For samples obtained with Low deposition rate (reverse pulse #1b), the flash Cu deposition was also performed at low current density for an extended duration (1100s). Six different accelerator to suppressor additive concentration ratio were studied with the ratio of the additives being varied from 0.26 to 1.75. Each additive ratio was first tested at bath temperature of 40°C (Experiment 1 through 6) with reverse pulse waveform #1. The exact set of experiments were then repeated with reduced current density (lower deposition rate) utilizing reverse waveform #1b (Experiment 7 through 12). Going forward, these conditions will be termed high and low dep rate for rest of this section.

Table 9.4: Experimental run card (Expt# 1 through 24) for Via5 Gap fill evaluation with various additive ratio for bath temperature 40°C and 48°C with reverse pulse waveform # 1 (high dep rate) and reverse pulse waveform # 1b (low dep rate)

(* experiment malfunction for those tests and data not presented further in the study)

Reverse Pulse	Accelerator Conc. (ml/L)	Suppressor Conc. (ml/L)	Ratio	Temperature	Current Density	Expt
Pulse Type # 1	5	19	0.26	40^0C , 48^0C	High	1, 13
Pulse Type # 1	12	28	0.43	40^0C , 48^0C	High	2, 14
Pulse Type # 1	16	28	0.57	40^0C , 48^0C	High	3, 15*
Pulse Type # 1	12	19	0.63	40^0C , 48^0C	High	4, 16
Pulse Type # 1	15	12	1.25	40^0C , 48^0C	High	5, 17
Pulse Type # 1	21	12	1.75	40^0C , 48^0C	High	6, 18
Pulse Type # 1b	5	19	0.26	40^0C , 48^0C	Low	7, 19
Pulse Type # 1b	12	28	0.43	40^0C , 48^0C	Low	8, 20
Pulse Type # 1b	16	28	0.57	40^0C , 48^0C	Low	9, 21*
Pulse Type # 1b	12	19	0.63	40^0C , 48^0C	Low	10, 22
Pulse Type # 1b	15	12	1.25	40^0C , 48^0C	Low	11, 23
Pulse Type # 1b	21	12	1.75	40^0C , 48^0C	Low	12, 24

Experiments 1 through 12 were then repeated with the exact parametric conditions at 48°C bath temperature and is identified in the DOE table as experimental splits 13 through 24 for high and low dep rates. The experimental run card tabulated in Table 9.4 shows the different parameters studied. The choice of the ratio of the additives selected to study between the ranges of 0.26 - 1.75 was random. During the execution of the experiments, Expt # 15 (high dep rate) and Expt # 21 (low rate) corresponding to additive ratio of 0.57 at 48°C bath temperatures had an experimental malfunction and the samples generated from those experiments are not measured. In summary, 24 different experiments were performed with various additive ratios at high and low deposition rate for bath temperature 40°C and 48°C utilizing reverse pulse waveform #1 and #1b. An SEM cross-section was performed for each of those 24 experiments.

Section 9.5 Results and discussion with various organic additive ratio and bath temperature with reverse pulse waveform # 1 and # 1b

Results obtained with cross sections for 40°C bath temperature samples are shown in Figure 9.7 (1-12) with the top row of images shown for high deposition rate and the bottom row with identical parametric conditions except for low deposition rates. SEM cross-sections for 48°C bath temperature experiment conditions are shown in Figure 9.8 (13 -24) with a similar set of image classification for top row and bottom row figures correspondingly for high and low deposition rates. Throwing power ratio was calculated for each of those experiments based on the measurements of the thickness of copper deposited at the via bottom and at the via top. A certain approximation had to be made in

determining the thickness values from the SEM graph as the via deposit is not completely flat. Therefore, the reported thickness values are subject to certain tolerance of variation. The measured values and the ratio are tabulated in Table 9.5. Figure 9.9 shows the plot of measured throwing power for each of those additive ratio conditions at different deposition rate and temperature. As shown in the bottom plot of Figure 9.9, for 40°C bath temperature at high dep rate (blue line in Figure 9.9), there is a gradual increase in throwing power as the additive ratio is decreased. A zoomed version of this plot is shown on the top plot. A linear Trendline fit shows reasonable match with the TP (throwing power) ratio increasing with reduced additive ratio. Reduced additive ratio directly correlates to increased suppression. This result indicates that as the overall suppression characteristic of the bath is increased, an improvement in throwing power can be obtained. Figure 9.9 also shows plot for 40°C bath temperature at low dep rate (Orange line in Figure 9.9). This condition did not show any significant as increase in throwing power. A maximum TP ratio of 1 or close to 1 was seen at all additive ratios. At high dep rate for 48°C (Grey line in Figure 9.9), an increase in throwing power is seen with reduced additive ratio similar to 40°C, but a Trendline did not have a clean linear fit likely due to noise present in the data. However, at low dep rate for 48°C, a drastic increase in TP is observed with reduced additive ratio. TP as high as 3.5 was achieved with an additive ratio of 0.3 at 48°C.

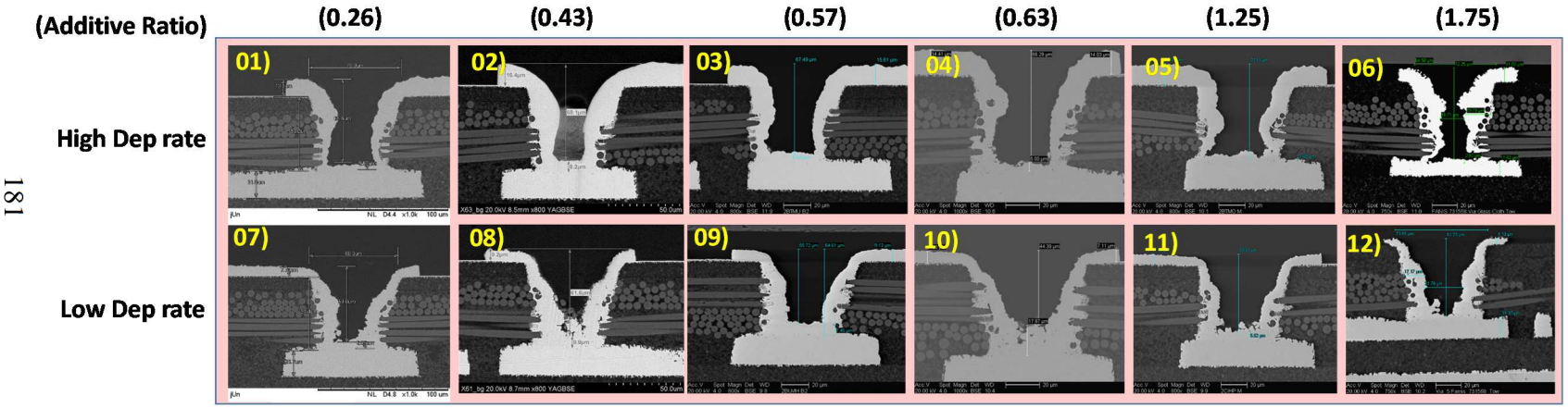

Figure 9.7: (Top row): Experiment 01 – 06 show via fill with various additive ratio for high deposition rate (reverse pulse # 1) utilizing 40°C bath temperature and 65g/l of bulk Cu^{2+} ions

Figure 9.7: (Bottom row): Experiment 07 – 12 show via fill with various additive ratio for low deposition rate (reverse pulse # 1b) utilizing 40°C bath temperature and 65g/l of bulk Cu^{2+} ions

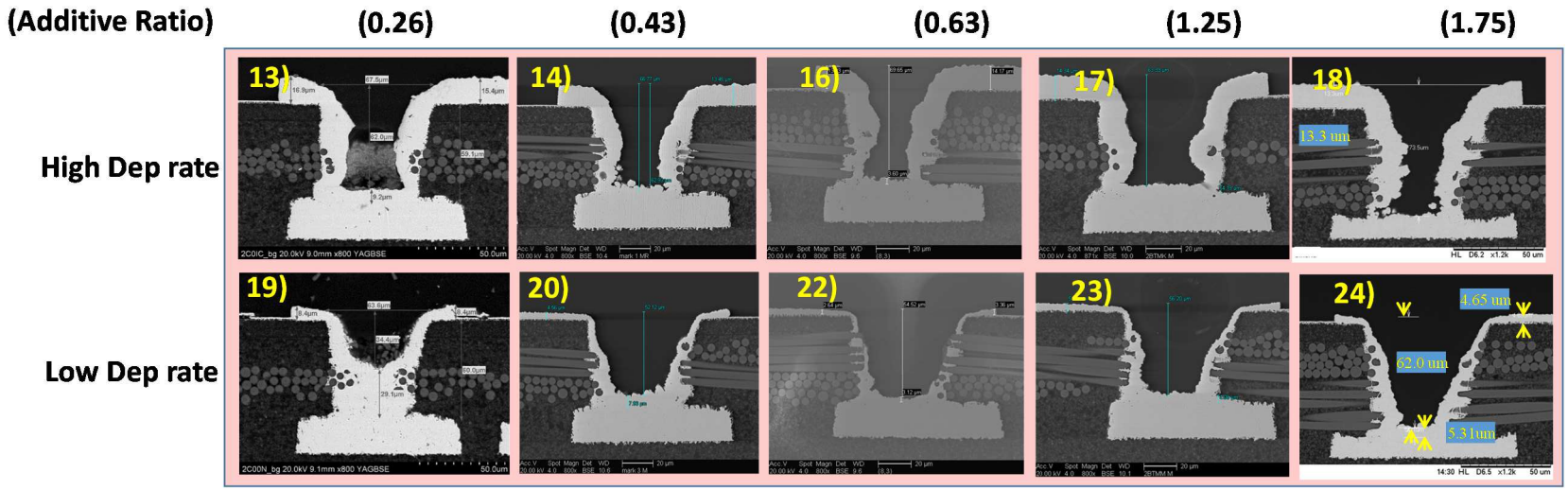

Figure 9.8: (Top row): Experiment 01 – 06 show via fill with various additive ratio for high deposition rate (reverse pulse # 1) utilizing 48°C bath temperature and 65g/l of bulk Cu^{2+} ions

Figure 9.8: (Bottom row): Experiment 07 – 12 show via fill with various additive ratio for low deposition rate (reverse pulse # 1b) utilizing 48°C bath temperature and 65g/l of bulk Cu^{2+} ions

(* experiment #15 and #21 had malfunction for those tests and data not presented)

Table 9.5: Electrodeposited Via5 top and bottom thickness and TP ratio measured for Expt# 1 through 24 with various additive ratio for bath temperature 40°C and 48°C with reverse pulse waveform # 1 (high dep rate) and reverse pulse waveform # 1b (low dep rate)

Expt #	Dep Rate	Bath Temp	Additive ratio	XSEM Bottom Thickness (µm)	XSEM Top Thickness (µm)	TP Ratio (Bottom thickness / Top Thickness)
Expt #1	High Dep rate	40^{0}C	0.3	5.6	13.8	0.4
Expt #2	High Dep rate	40^{0}C	0.4	8.2	16.4	0.5
Expt #3	High Dep rate	40^{0}C	0.6	5.0	15.6	0.3
Expt #4	High Dep rate	40^{0}C	0.6	5.3	14.5	0.4
Expt #5	High Dep rate	40^{0}C	1.3	3.9	16.1	0.2
Expt #6	High Dep rate	40^{0}C	1.8	2.8	11.3	0.2
Expt #7	Low Dep rate	40^{0}C	0.3	5.1	7.7	0.7
Expt #8	Low Dep rate	40^{0}C	0.4	8.8	9.2	1.0
Expt #9	Low Dep rate	40^{0}C	0.6	9.0	9.1	1.0
Expt #10	Low Dep rate	40^{0}C	0.6	7.0	7.1	1.0
Expt #11	Low Dep rate	40^{0}C	1.3	5.5	7.7	0.7
Expt #12	Low Dep rate	40^{0}C	1.8	3.0	4.1	0.7
Expt #13	High Dep rate	48^{0}C	0.3	9.2	16.9	0.5
Expt #14	High Dep rate	48^{0}C	0.4	3.0	13.9	0.2
Expt #15	High Dep rate	48^{0}C	0.6	0.0	0.0	
Expt #16	High Dep rate	48^{0}C	0.6	5.9	15.7	0.4
Expt #17	High Dep rate	48^{0}C	1.3	3.9	14.5	0.3
Expt #18	High Dep rate	48^{0}C	1.8	0.0	13.0	0.0
Expt #19	Low Dep rate	48^{0}C	0.3	29.1	8.3	3.5
Expt #20	Low Dep rate	48^{0}C	0.4	7.6	4.7	1.6
Expt #21	Low Dep rate	48^{0}C	0.6	0.0	0.0	
Expt #22	Low Dep rate	48^{0}C	0.6	3.5	3.0	1.2
Expt #23	Low Dep rate	48^{0}C	1.3	3.5	5.0	0.7
Expt #24	Low Dep rate	48^{0}C	1.8	5.5	4.4	1.3

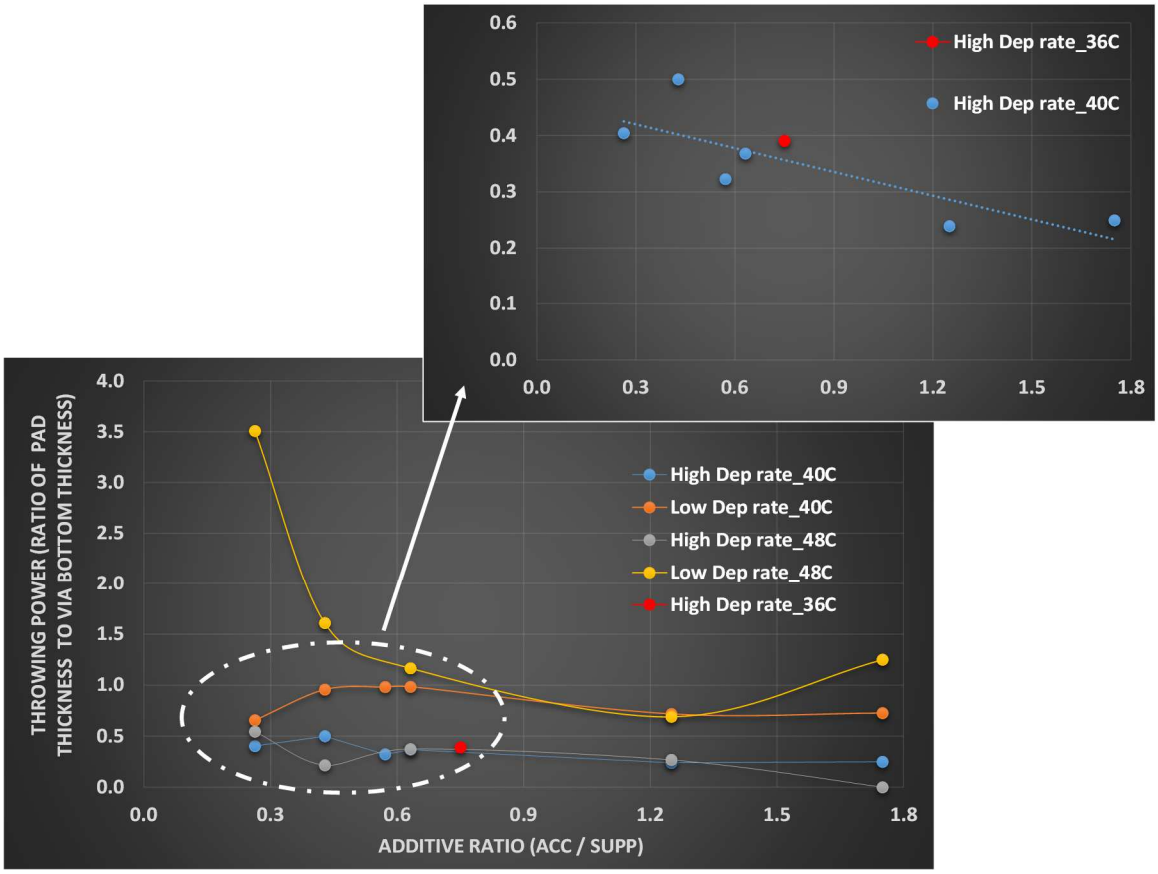

Figure 9.9: Plot of additive ratio Vs Throwing power for high and low deposition rate utilizing 40°C and 48°C bath temperature and 65g/l of bulk Cu^{2+} ions for via5

Section 9.6 Key learning's with various organic additive ratio and bath temperature with reverse pulse waveform # 1 and # 1b

To summarize, 24 different experiments were performed with various additive concentration ratios (termed as additive ratio going forward) at high and low deposition rate for bath temperature 40°C and 48°C utilizing reverse pulse waveform type #1 for high deposition rate and #1b for low deposition rate. An SEM cross-section was performed for each of those 24 experiments. The results obtained with such cross sections indicate a linear increase in throwing power for reduced additive ratio at all conditions.

The extent of improvement varies with bath temperature and deposition rate. With 48°C and low deposition rate, TP as high as 3.5 is achieved with an additive ratio of 0.3.

Section 9.7 Design of experiments with various organic additive ratio and bath temperature with reverse pulse waveform # 2 and # 2b

Reverse pulse waveform #1 accommodates a maximum reverse current density of 10ASD for 2ms duration. The average current density for deposition was set at 5.4ASD and plated for a duration of 950s post Flash Cu deposition. Reverse pulse #1b was performed for the same 2ms duration with the reverse current density reduced to 5ASD with the average current density for deposition reduced to 2.2ASD. In order to see the impact of reverse pulse current density and duration on Via5 fill, similar set of experiments performed earlier with reverse pulse #1 and #1b were repeated with reverse pulse waveform #2 and #2b. Reverse pulse waveform #2 accommodates a maximum reverse current density of 40ASD for 4ms duration. The average current density for deposition was set at 3.4ASD. Reverse pulse #2b was performed for the same 4ms duration with the reverse current density reduced to 20ASD with the average current density for deposition reduced to 1.7ASD. Reverse pulse #2b was performed for an extended time (1800s) to accommodate for the reduced current density. For samples obtained with low deposition rate (reverse pulse #2b), flash Cu deposition was also performed at low current density for an extended duration. Here again, six different ratio of the additives were studied with the ratio of the additives being varied from 0.26 to 1.75. Each additive ratio was first tested at bath temperature of 40°C (Experiment 25

through 30) with reverse pulse waveform # 2 (high dep rate). The exact set of experiments were then repeated with reduced current density (lower deposition rate) utilizing reverse waveform #2b (Experiment 31 through 36). Experiments 25 through 36 were then repeated with the exact parametric conditions as earlier but at 48°C bath temperature and is shown as experimental splits 37 through 48 for high and low dep rates. The experimental run card tabulated in Table 9.6 shows the different parameters studied with reverse pulse waveform type #2 and #2b. The choice of the ratio of the additives selected to study were kept identical to reverse pulse waveform #1. During the execution of the experiments, Expt # 39 (high dep rate) and Expt # 45 (low rate) corresponding to additive ratio of 0.57 at 48°C bath temperatures had an experimental malfunction and those data samples were not analyzed. To summarize, 24 different experiments were performed with various additive ratios at high and low deposition rate for bath temperature 40°C and 48°C utilizing reverse pulse waveform #2 and #2b. An SEM cross-section was performed for each of those 24 experiments.

Section 9.8 Results and discussion with various organic additive ratio and bath temperature with reverse pulse waveform # 2 and # 2b

Results obtained with such cross sections for 40°C bath temperature are shown in Figure 9.10 (25 - 36) and cross sections for 48°C bath temperature are shown in Figure 9.11 (37 - 48). A quick overview of the results published in Figure 9.10 and 9.11 show significantly improved gap fill with Via5 geometry on reverse pulse #2 and #2b compared to the fill results obtained with reverse pulse #1 and #1b.

Table 9.6: Experimental run card (Expt# 25 through 48) for Via5 Gap fill evaluation with various additive ratio for bath temperature 40°C and 48°C with reverse pulse waveform # 2 (high dep rate) and reverse pulse waveform # 2b (low dep rate)

(* experiment malfunction for those tests and data not presented further in the study)

Reverse Pulse	Accelerator Conc. (ml/L)	Suppressor Conc. (ml/L)	Ratio	Temperature	Current Density	Expt
Pulse Type # 2	5	19	0.26	40^0C , 48^0C	High	25, 37
Pulse Type # 2	12	28	0.43	40^0C , 48^0C	High	26, 38
Pulse Type # 2	16	28	0.57	40^0C , 48^0C	High	27, 39*
Pulse Type # 2	12	19	0.63	40^0C , 48^0C	High	28, 40
Pulse Type # 2	15	12	1.25	40^0C , 48^0C	High	29, 41
Pulse Type # 2	21	12	1.75	40^0C , 48^0C	High	30, 42
Pulse Type # 2b	5	19	0.26	40^0C , 48^0C	Low	31, 43
Pulse Type # 2b	12	28	0.43	40^0C , 48^0C	Low	32, 44
Pulse Type # 2b	16	28	0.57	40^0C , 48^0C	Low	33, 45*
Pulse Type # 2b	12	19	0.63	40^0C , 48^0C	Low	34, 46
Pulse Type # 2b	15	12	1.25	40^0C , 48^0C	Low	35, 47
Pulse Type # 2b	21	12	1.75	40^0C , 48^0C	Low	36, 48

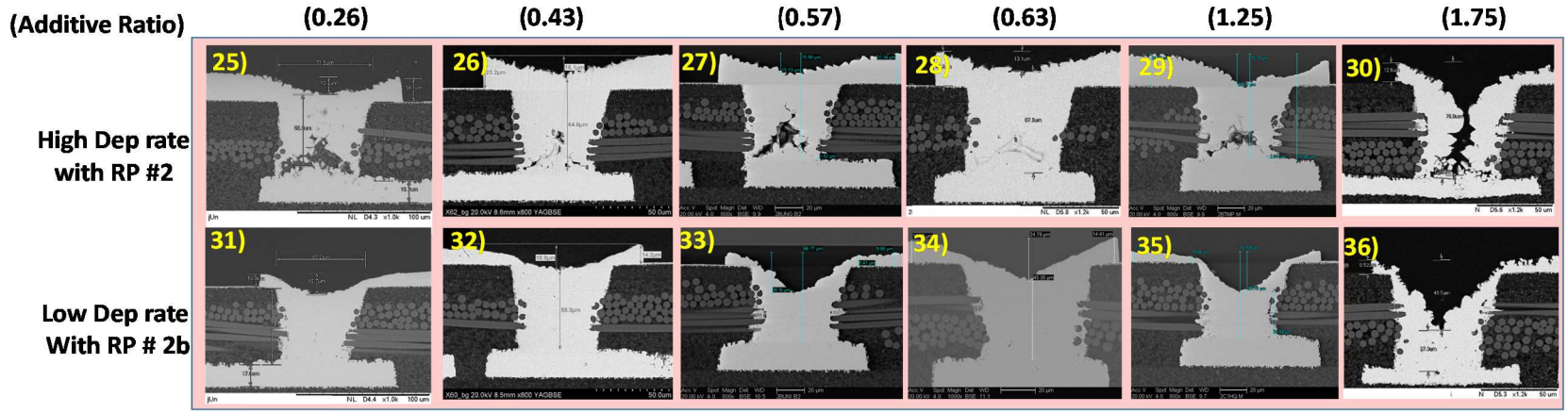

Figure 9.10: (Top row): Experiment 25 – 30 show via fill with various additive ratio for high deposition rate (reverse pulse # 2) utilizing 40°C bath temperature and 65g/l of bulk Cu^{2+} ions

Figure 9.10: (Bottom row): Experiment 31 – 36 show via fill with various additive ratio for low deposition rate (reverse pulse # 2b) utilizing 40°C bath temperature and 65g/l of bulk Cu^{2+} ions

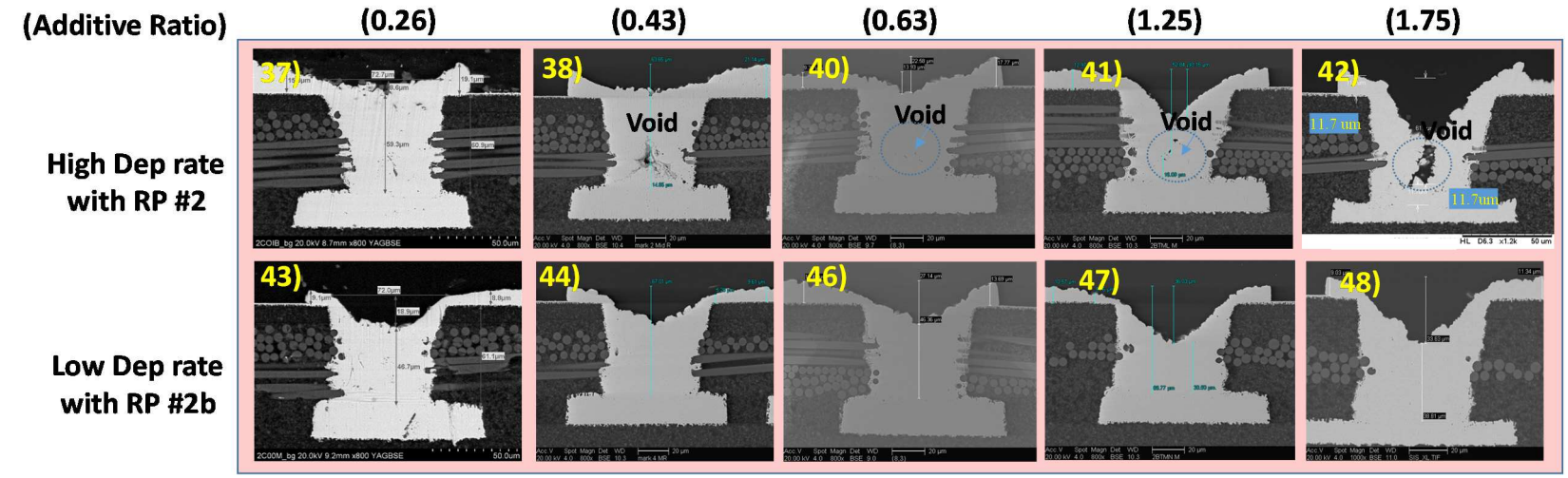

Figure 9.11: (Top row): Experiment 25 – 30 show via fill with various additive ratio for high deposition rate (reverse pulse # 2) utilizing 48°C bath temperature and 65g/l of bulk Cu^{2+} ions

Figure 9.11: (Bottom row): Experiment 31 – 36 show via fill with various additive ratio for low deposition rate (reverse pulse # 2b) utilizing 48°C bath temperature and 65g/l of bulk Cu^{2+} ions

Furthermore, for experimental results generated with utilizing reverse pulse waveform #2 and #2b, instead of reporting throwing power, a new parameter termed "via recess thickness" is measured and reported. Throwing power values with these results could be confounded by the fact that the via was already filled for most of the test conditions and it would be difficult to de-convolute the thickness contribution from the via sidewalls and via bottom in order to truly establish a throwing power that is consistent with the values reported earlier. The presence of glass fiber at different locations along the depth of the via further complicates the true sidewall contribution that needs to be offset to determine the via bottom thickness. Therefore, a new independent parameter called "Via recess" was defined to compare the performance for Expt #25 through 48. Figure 9.12 with a schematic cartoon shows the methodology for the measurement of the via recess thickness. Via recess in this study is defined as the amount of via region that is not completely filled. A profilometric measurement was utilized to obtain the via recess thickness by averaging the measurement point along the concentric circle points along on the outer via top region as well as the recessed location inside the gap filled via region. Differences between the measurements points along the outside concentric circle and the recess point enables the via recess thickness. Conversely, the via recess thickness can also be measured with a cross-section but the cross-section needs to happen on the center of the via and it is always difficult to land the polish at the exact center location and is more prone to error. For this reason, the data from profilometer was utilized to determine the via recess thickness measurements. In most cases, consistent results between the cross-section and profilometer was obtained but not this was not always the case.

Profilometer reported much higher recess values in some cases, indicating a worse fill condition than the results generated with SEM cross-section.

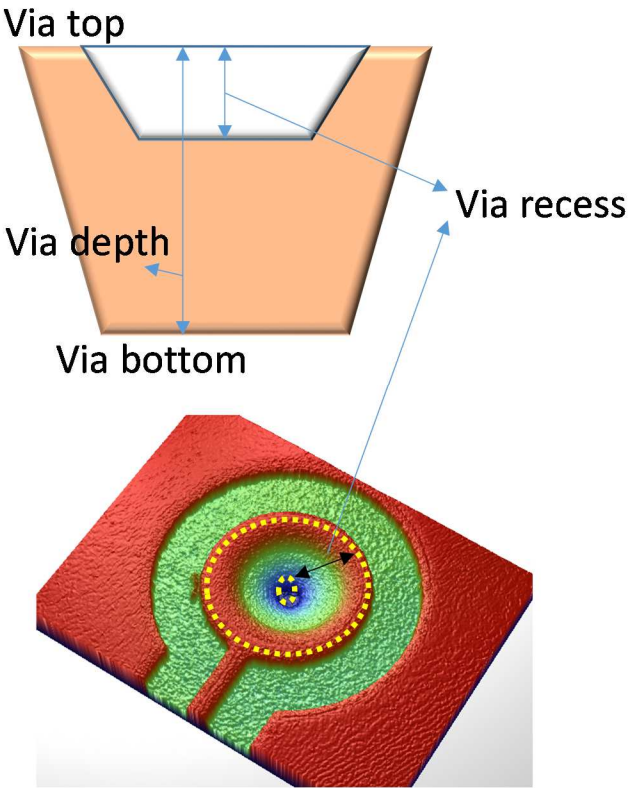

Figure 9.12: Schematic of Via recess measurement with a Cross-section (top picture) and a top view (bottom picture)

From the schematic above in Figure 9.12, it can be easily concluded that a sample that shows low via recess thickness would indicate a very good fill bottom-up and vice-verse for a sample that has a poor bottom-up or gap fill with high via recess. The profilometer measured via recess thickness values for Expt #25 through 48 are tabulated in Table 9.7. In each case the presence of via void was also verified and tabulated in Table 9.7. Figure 9.13 shows the plot of measured via recess for each of those additive ratio conditions at

different deposition rate and temperature. It is notable here that all high dep rate conditions at 40°C show via voids while the low deposition rate conditions do not show via voids. With 48°C condition, the low additive ratio of 0.26 do not show via voids at high deposition rate while the rest of the condition show some level of voiding. Low dep rate at 48°C do not show voiding.

Table 9.7: Electrodeposited Via5 via recess thickness and presence of void measured for Expt# 25 through 48 with various additive ratio for bath temperature 40^0C and 48^0C with reverse pulse waveform #2 (high dep rate) and reverse pulse waveform #2b (low dep rate)

Expt #	Dep Rate	Bath Temp	Additive ratio	Via Recess (µm)	Void Observation
Expt # 25	High Dep rate	40^0C	0.26	13.3	Y
Expt # 26	High Dep rate	40^0C	0.43	12.1	Y
Expt # 27	High Dep rate	40^0C	0.57	12.0	Y
Expt # 28	High Dep rate	40^0C	0.63	14.0	Y
Expt # 29	High Dep rate	40^0C	1.25	25.8	Y
Expt # 30	High Dep rate	40^0C	1.75	25.0	Y
Expt # 31	Low Dep rate	40^0C	0.26	13.3	N
Expt # 32	Low Dep rate	40^0C	0.43	12.0	N
Expt # 33	Low Dep rate	40^0C	0.57	26.2	N
Expt # 34	Low Dep rate	40^0C	0.63	16.2	N
Expt # 35	Low Dep rate	40^0C	1.25	36.5	N
Expt # 36	Low Dep rate	40^0C	1.75	35.0	N
Expt # 37	High Dep rate	48^0C	0.26	9.4	N
Expt # 38	High Dep rate	48^0C	0.43	13.8	Y
Expt # 39	High Dep rate	48^0C	0.57		
Expt # 40	High Dep rate	48^0C	0.63	20.9	Y
Expt # 41	High Dep rate	48^0C	1.25	41.8	Y
Expt # 42	High Dep rate	48^0C	1.75	27.0	Y
Expt # 43	Low Dep rate	48^0C	0.26	16.7	N
Expt # 44	Low Dep rate	48^0C	0.43	18.0	N
Expt # 45	Low Dep rate	48^0C	0.57		
Expt # 46	Low Dep rate	48^0C	0.63	18.9	N
Expt # 47	Low Dep rate	48^0C	1.25	31.1	N
Expt # 48	Low Dep rate	48^0C	1.75	24.0	N

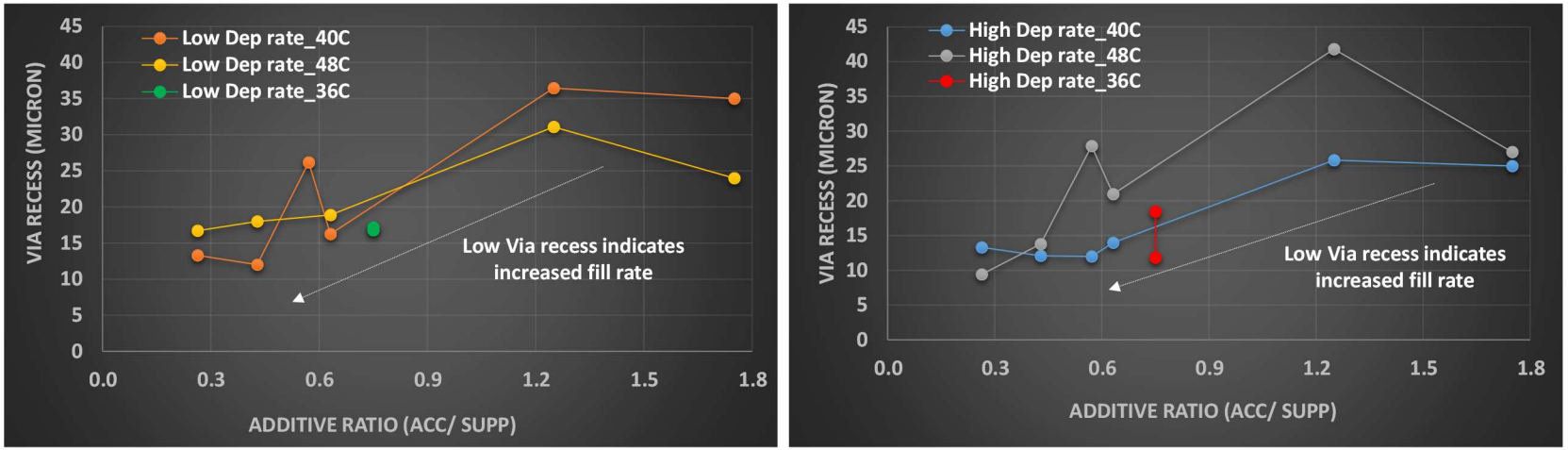

Figure 9.13: a) Plot of additive ratio Vs Via recess for low deposition rate utilizing 40°C and 48°C bath temperature and 65g/l of bulk Cu^{2+} ions, b) Plot of additive ratio Vs Via recess for high deposition rate utilizing 40°C and 48°C bath temperature and 65g/l of bulk Cu^{2+} ions

As shown in the right plot of Figure 9.13a, for 40°C bath temperature at high dep rate (blue line), there is a gradual decrease in via recess with the reduction in additive ratio. Reduced additive ratio directly correlates to increased suppression. This result indicates that as the overall suppression characteristic of the bath is increased, an improvement in fill rate can be obtained. Figure 9.13a also shows plot for 48°C bath temperature at high dep rate (Grey line) a decrease in via recess is seen with reduced additive ratio similar to 40°C condition. Similarly, as shown in the left plot of Figure 9.13b, for 40°C and 48°C bath temperature at low dep rate a decrease in via recess is observed with reduced additive ratio. These findings are consistent with the results on the left plot for high deposition rate. It is to be noted that via voids are observed for most high deposition rate conditions at 40°C and 48°C, except for additive ratio of 0.26 at 48°C. All low dep rate condition shows no voiding with the lowest recess value obtained at a low additive ratio of 0.26 at 40°C and 48°C.

Section 9.9 Key learning's with various organic additive ratio and bath temperature with reverse pulse waveform # 2 and # 2b

To summarize, 24 different experiments were performed with various additive ratios at high and low deposition rate for bath temperature 40°C and 48°C for reverse pulse waveform type #2 and #2b. An SEM cross-section was performed for each of those 24 experiments. The results obtained with such cross sections indicate a decrease in via recess for reduced additive ratio at all conditions. Via voiding is still observed at high

deposition rates but void-free via fill is obtained at low deposition rates with the optimized fill performance at low additive ratio conditions.

Section 9.10 Summary

Via5 geometry presents a unique challenge for void-free gap fill due to the presence of glass fiber protrusions inside the via region. Incorporation of reverse pulse methodology with reverse pulse waveforms #1 and #2 that improved fill performance and enabled void-free fill with Via0 and Via1 geometry did not show much success for via5 geometry. A "pinch-off" void was observed even with the incorporation of reverse pulse methodology. Additional process parameters that control the deposition process had to be identified to further improve the throwing power inside Via5 geometry. Six different combination ratio of organic additives such as accelerator and suppressor were then tested at two different bath temperatures of 40°C and 48°C. These sets of experiments were performed with reverse pulse #1 and reverse pulse #1b to ascertain the throwing power with different additive combinations. A low additive ratio of accelerator to suppressor shows improved fill performance at all conditions. Furthermore, when these sets of experiments were performed with reverse pulse #2 and #2b that incorporates larger reverse current density and duration, a complete gap fill process was obtained with no via voids at low depositions rates and via recess reduced at small additive ratio combinations. With increased reverse pulse duration, fill behavior (pertaining to throwing power) were similar at 48°C compared to 40°C. Thus, these efforts enable a capable reverse pulse deposition process with optimized additive concentration for Via5

geometry that shows void-free fill and improved overall fill performance. In Chapter X, we perform the same set of experiments for Via1 geometry to confirm whether the newly identified deposition regime with increased suppression present in the electrolyte enables improved gap fill not only for Via5 geometry but across all Via geometry.

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CHAPTER X

EXTENSION OF ADDITIVE RATIO OPTIMIZATION FOR VIA1 GEOMETRY

Section 10.0 Introduction

In chapter IX, we discussed the ability of reverse pulse methodology and additive ratio optimization to enable void-free gap fill for Via5 geometry that has a via depth on the order of ~65um and via bottom diameter is on the order of ~55µm to ~60µm. Besides the large sizes, these via geometry also had glass fiber protrusions extending inside the via that necessitated a very aggressive bottom-up fill condition to prevent a void-free fill. IC substrate applications have via bottom stack that has varying via geometry with Via0 that has a geometry of ~25µm depth along with a via bottom diameter of ~25µm and Via1 that has a depth of ~30µm but with via bottom diameter of ~50um. As discussed before, these via's (Via0 and Via1) are drilled through a dielectric film (with no glass fiber) to enable I/O routing and ground plane connections between an active die and the mother board. The characteristic of incoming via geometry and the ability to generate void-free fill with the incorporation of reverse pulse waveform was already discussed in Chapter VI. In this chapter, we would extend the learning's obtained from additive ratio optimization to the previously studied geometry of Via0 and Via1 and will confirm the learning's obtained from Chapter IX that a reduced additive ratio accommodates all via geometry for void-free gap fill besides the unique Via5 geometry. Such improvement in via fill can be obtained with the optimization of additive ratio along with the incorporation of reverse pulse waveform methodology.

Section 10.1 Results and discussions: Via1 gap fill – experiment# A

An incoming Via1 geometry with a uniformly coated copper seed surface is shown in Figure 10.1a1. Electrodeposition was performed with the bulk concentration of the copper targeted at 65g/l for the entire duration of the deposition process to eliminate any mass transfer limitation of Cu^{2+} ions at the via bottom sidewalls. In Expt # A via fill process was performed with a reverse current density of 24ASD for 4ms post flash Cu deposition. The parametric conditions utilized for this deposition are tabulated in Table 10.1. Flash Cu deposition was performed first to prevent seed dissolution during the initial stages of the deposition followed by via fill.

Table 10.1: Parameter Summary for Experiment #A utilized for gap fill on Via1 geometry

Steps	Parameters	Expt A
Flash Cu	Cu2+ (g/l)	65
	Temp ©	36
	Pump Agitation (Hz)	30
	Reverse Pulse CD	10
	Reverse Pulse Duration (ms)	2
	Forward Pulse Duration (ms)	78
	Reverse Pulse Waveform ID	1
	Total Duration (s)	700
Via Fill	Cu2+ (g/l)	65
	Temp ©	36
	Pump Agitation (Hz)	13
	Reverse Pulse CD	24
	Reverse Pulse Duration (ms)	4
	Forward Pulse Duration (ms)	76
	Reverse Pulse Waveform ID	3
	Total Duration (s)	700

As shown in Figure 10.1a2, a void-free fill is obtained with the incorporation of reverse pulse waveform # 3 with a reverse current density of 24ASD for 4ms duration.

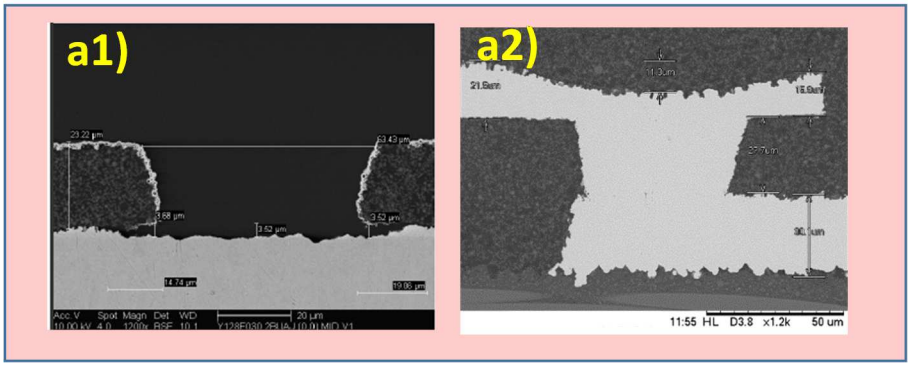

Figure 10.1a1) SEM Cross-section of Via1 with a copper seed layer, a2) SEM Cross-section of Via1 post Flash Cu plating with 65g/l of bulk Cu^{2+} ion and Via fill with 65g/l of bulk Cu^{2+} ions and 36°C bath temperature and reverse current density of 24ASD for 4ms

Via fill for IC substrate application require a void-free fill along with a completely filled via such that a dimple or via recess is minimized or completely eliminated. A schematic cartoon in Figure 10.2 shows the methodology for the measurement of the via recess thickness. Via recess in this study is defined as the amount of via region that is not completely filled. A profilometric measurement was utilized to obtain the via recess thickness by averaging the measurement point along the concentric circle points along on the outer via top region as well as the recessed location inside the gap filled via region. Differences between the measurements points along the outside concentric circle and the recess point enables the estimation of via recess thickness. Conversely, the via recess thickness can also be measured with a cross-section but the cross-section needs to happen on the center of the via and it is always difficult to land the polish at the exact center

location and such estimations are more prone to error. For this reason, the data from profilometer was utilized to determine the via recess thickness measurements. In most cases, consistent results between the cross-section and profilometer was obtained but not this was not always the case. Profilometer reported much higher recess values in some cases indicating a worse fill condition than the results generated with SEM cross-section.

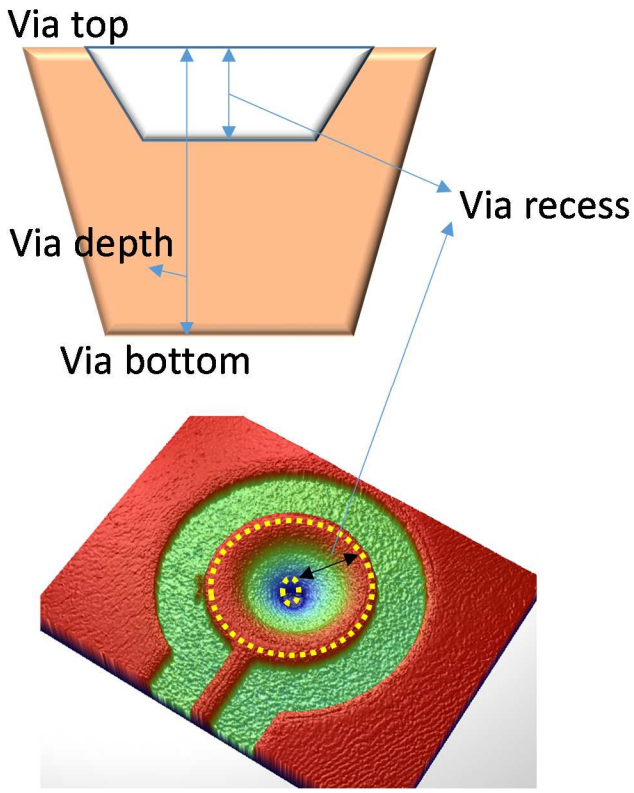

Figure 10.2: Schematic of Via recess measurement with a Cross-section (top picture) and a top view (bottom picture)

For example, for Expt #A with the application of reverse waveform #3 the via recess was measured to be on the order of ~10µm with an SEM cross-section as shown in Figure 10.1 a2. However, profilometer measurements indicated a maximum recess of ~20µm inside the via feature. Increase in deposition time shows an improvement in recess but

such activity could cause non-uniform copper surface. So far, incorporation of reverse pulse methodology alone has yielded a void-free process for Via1 geometry. However, further improvement in throwing power is needed to eliminate via recess and achieve a complete fill with a uniform copper surface without the addition of additional process time. Therefore, in order to identify additional knobs for improving throwing power, the ability of organic additives and bath temperature to influence throwing power was investigated as independent knobs to improve gap fill capability for Via1 geometry.

Section 10.2 Optimization of organic additive ratio and bath temperature with reverse pulse for via1

It is well known that in the presence of Cl^- ion species in the electrolyte, organic additives such as accelerators complex with the chloride ions and enhance the corner growth rate at the via bottom due to the presence of increased surface area at those regions and suppressors temporarily block adsorption of Cu^{1+} at the via top until displaced by the accelerator[1]. West et al studied the ratio of these additives to the ensuing throwing power for damascene applications[2]. A similar attempt was made for Via1 geometry, by performing a comparative study to generate the correlation of throwing power to various ratio of accelerator to suppressor molecules. Such a study should generate a good understanding of the ability of the organic additive to enable bottom-up fill for Via1 geometry.

In this study, the ratio of the concentration of the additives was considered as a single variable than the concentration of the two species independently. In the

experimental results shown in Chapter VI and in experiment #A earlier, the organic additive ratio was maintained at 0.75 (ratio of measured accelerator to suppressor concentration). In our testing so far, two proprietary additives namely "SBP2 Accelerator" and "SBP2 Leveler" purchased from Atotech Inc., were utilized for the experiments. The Accelerator concentration was targeted and maintained at 12ml/l while Leveler concentration was measured at 16ml/L. An analytical CV (Cyclic Voltammetry) method was utilized to measure and target the concentration of the bath periodically as needed. Overall, the concentrations were maintained within the range of ± 0.2ml/l from specified target. The exact molecular details of these species were unknown for this study and the functionality of these species were expected to behave primarily as accelerator and suppressor that are referenced in scientific literature studies. Henceforth, these species will be termed as accelerator and suppressor for rest of this study and their ratio would be varied to understand their impact on bottom-up fill for Via1 geometry.

Increased deposition temperature leads to increased mobility of the Cu^{2+} ion as well as the additive species to the via bottom. In the present application given the large size of the via with a critical need to enable the availability of Cu^{2+} ion and additive species to the via bottom much higher temperature such as 40°C and 48°C were studied.

Four set of waveforms were experimented for these various additive ratios at 40°C and 48°C with the bulk concentration of Cu^{2+} ions maintained at 65g/l utilizing reverse pulse waveform #1 and #3. These experiments were repeated with half the current density as that was utilized earlier for reverse pulse waveform #1 and # 3 as

reverse pulse waveform #1b and #3b. The shape and current density of the waveforms that were utilized in the experiments are captured in Figure 10.3 below for reference.

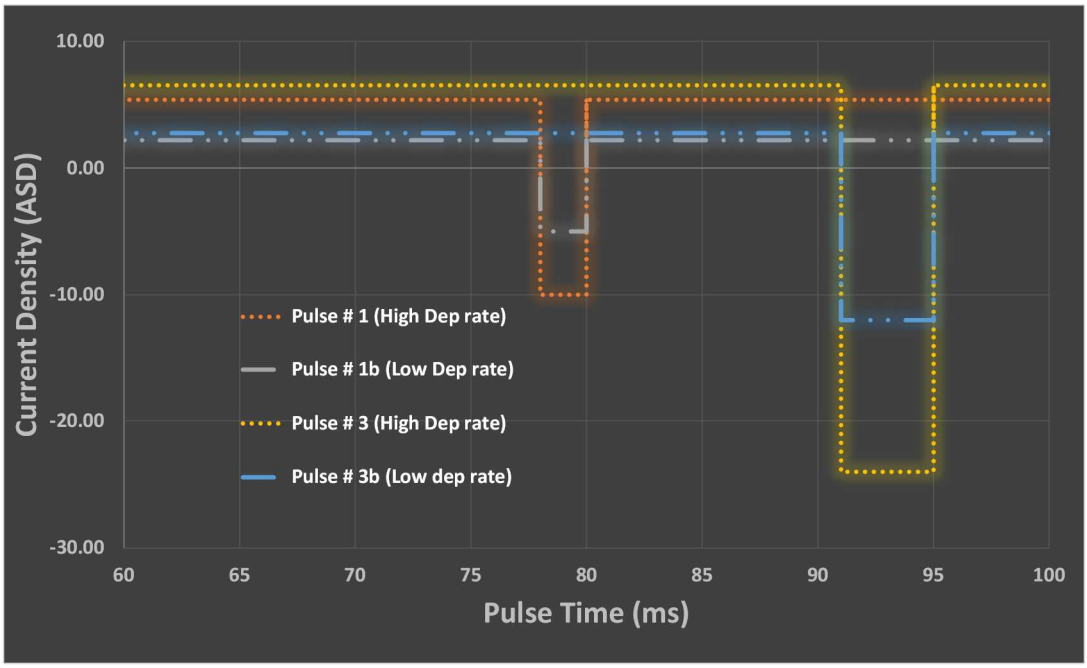

Figure 10.3: Reverse Pulse waveforms (#1, #1b, #3, #3b) utilized for additive ratio optimization

In reverse pulse waveforms #1b and #3b, both the forward and reverse current density were reduced to less than half but the corresponding reverse time durations were kept the same. Table 10.2 shows the exact current density parameters that were utilized in these waveforms.

Table 10.2: Reverse Pulse waveforms parameters for #1, #1b, #3, #3b that were utilized for additive ratio optimization

	Average Current density and Time period		Reverse Current density and Time period		Forward Current density and Time period	
	A0 (A/dm^2)	T0 (s)	A2 (A/dm^2)	T2 (s)	A1 (A/dm^2)	T1 (s)
Pulse Waveform # 1	5.0	0.08	10	0.002	5.38	0.078
Pulse Waveform # 1b	2	0.08	5	0.002	2.19	0.078
Pulse Waveform # 3	5	0.08	24	0.004	6.53	0.076
Pulse Waveform # 3b	2	0.08	12	0.004	2.75	0.076

Section 10.3 Design of experiments with various organic additive ratio and bath temperature with reverse pulse waveform # 1 and # 1b

As explained earlier, the primary goal of the testing here was to identify an optimal ratio of the additive at elevated bath temperature for gap fill with Via1 geometry. An experimental DOE run card was set up to investigate the effect of these variables with reverse pulse waveforms # 1. Six different accelerator to suppressor concentration ratio of the additives were studied with the ratio of the additives being varied from 0.26 to 1.75. Each additive ratio was first tested at bath temperature of 40°C (Experiment 1 through 6) with reverse pulse waveform #1. The exact set of experiments were then repeated with reduced current density (lower deposition rate) utilizing reverse waveform #1b (Experiment 7 through 12). Going forward, these conditions will be termed high and low dep rate for rest of this section.

Table 10.3: Experimental run card (Expt# 1 through 24) for Via1 Gap fill evaluation with various additive ratio for bath temperature 40°C and 48°C with reverse pulse waveform # 1 (high dep rate) and reverse pulse waveform # 1b (low dep rate)

(* experiment malfunction for those tests and data not presented further in the study)

Reverse Pulse	Accelerator Conc. (ml/L)	Suppressor Conc. (ml/L)	Ratio	Temperature	Current Density	Expt
Pulse Type # 1	5	19	0.26	40^0C , 48^0C	High	1, 13
Pulse Type # 1	12	28	0.43	40^0C , 48^0C	High	2, 14
Pulse Type # 1	16	28	0.57	40^0C , 48^0C	High	3, 15*
Pulse Type # 1	12	19	0.63	40^0C , 48^0C	High	4, 16
Pulse Type # 1	15	12	1.25	40^0C , 48^0C	High	5, 17
Pulse Type # 1	21	12	1.75	40^0C , 48^0C	High	6, 18
Pulse Type # 1b	5	19	0.26	40^0C , 48^0C	Low	7, 19
Pulse Type # 1b	12	28	0.43	40^0C , 48^0C	Low	8, 20
Pulse Type # 1b	16	28	0.57	40^0C , 48^0C	Low	9, 21*
Pulse Type # 1b	12	19	0.63	40^0C , 48^0C	Low	10, 22
Pulse Type # 1b	15	12	1.25	40^0C , 48^0C	Low	11, 23
Pulse Type # 1b	21	12	1.75	40^0C , 48^0C	Low	12, 24

Experiments 1 through 12 were then repeated with the same parametric conditions to what was experimented earlier but with the bath temperature at 48°C. These conditions are identified in the DOE table 10.3 as experimental splits 13 through 24 for high and low dep rates. The experimental run card tabulated in Table 10.3 shows the different parameters studied. The choice of the ratio of the additives selected to study between the ranges of 0.26 - 1.75 was random. During the execution of the experiments, Expt # 15 (high dep rate) and Expt # 21 (low rate) corresponding to additive ratio of 0.57 at 48°C bath temperatures had an experimental malfunction and those data samples were not analyzed. In summary, 24 different experiments were performed with various additive ratios at high and low deposition rate for bath temperature 40°C and 48°C utilizing reverse pulse waveform #1 and #1b. An SEM cross-section was performed for each of those 24 experiments.

Section 10.4 Results and discussion with various organic additive ratio and bath temperature with reverse pulse waveform # 1 and # 1b

Results obtained with such cross sections for 40°C bath temperature are shown in Figure 10.4 (1-12) with the top row of the images shown for high copper deposition rate and the bottom row with identical parametric conditions except for low copper deposition rates. SEM cross-sections for 48°C bath temperature experiments are shown in Figure 10.5 (13 -24) with a similar set of image classification for top row and bottom row figures correspondingly for high and low deposition rates. Throwing power ratio was calculated for each of those experiments based on the measurements of the thickness of copper

deposited at via bottom and at via top. A certain approximation had to be made in determining the thickness values from the SEM graph as the via deposit is not completely flat. Therefore, the reported thickness values are subject to certain tolerance of variation. The measured values and the ratio are tabulated in Table 10.4. Figure 10.6 shows the plot of measured throwing power for each of those additive ratio conditions at different deposition rate and temperature. As shown in the plot of Figure 10.6, for 40°C bath temperature at high dep rate (blue line from Figure 10.6), there is a gradual increase in throwing power with the reduction in additive ratio. Reduced additive ratio directly correlates to increased suppression. This result indicates that as the overall suppression characteristic of the bath is increased, an improvement in throwing power can be obtained consistent with the earlier findings on Via5 geometry. Figure 10.6 also shows plot for 40°C bath temperature at low dep rate (Orange line from Figure 10.6). This condition also shows an increase in throwing power with reduction of organic additive ratio. A maximum TP ratio of 1 to 1.5 was seen at low additive ratios for Via1 geometry. At high dep rate for 48°C (Grey line from Figure 10.6), an increase in throwing power is seen with reduced additive ratio but at a smaller rate. The TP values were lower at 48°C at low additive ratio. However, at low dep rate for 48°C (yellow line from Figure 10.6), an increase in TP is observed with reduced additive ratio with some tapering in TP at the lowest additive ratio. The reasons for this tapering for this bath temperature is not clear, other than to be classified with in the margin of the experimental error.

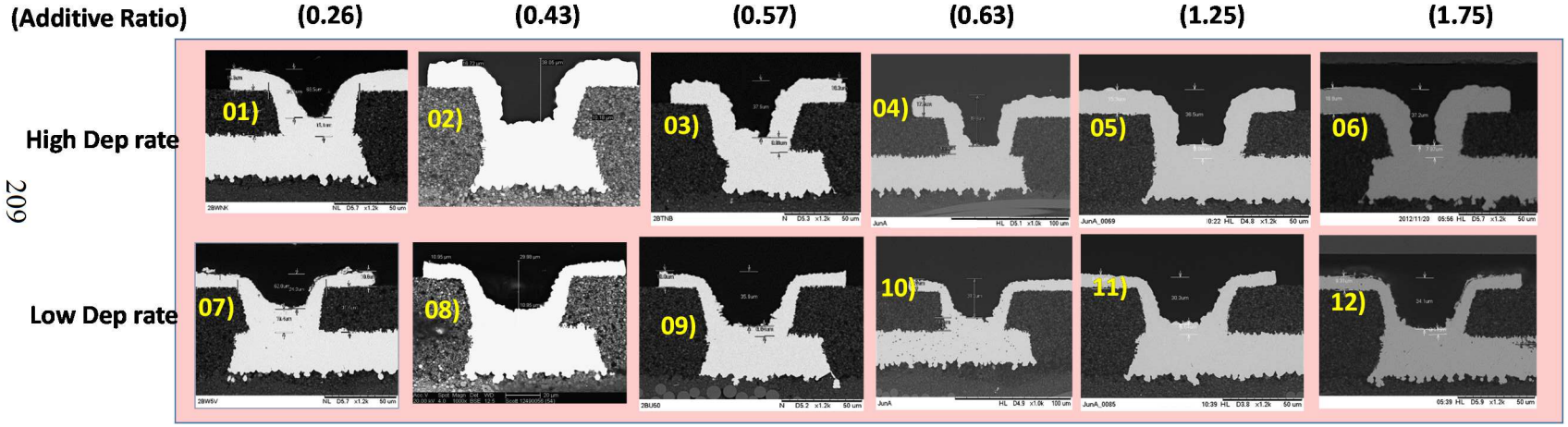

Figure 10.4: (Top row): Experiment 01 – 06 show via fill with various additive ratio for high deposition rate (reverse pulse # 1) utilizing 40°C bath temperature and 65g/l of bulk Cu^{2+} ions on via1 geometry

Figure 10.4: (Bottom row): Experiment 07 – 12 show via fill with various additive ratio for low deposition rate (reverse pulse # 1b) utilizing 40°C bath temperature and 65g/l of bulk Cu^{2+} ions on via1 geometry

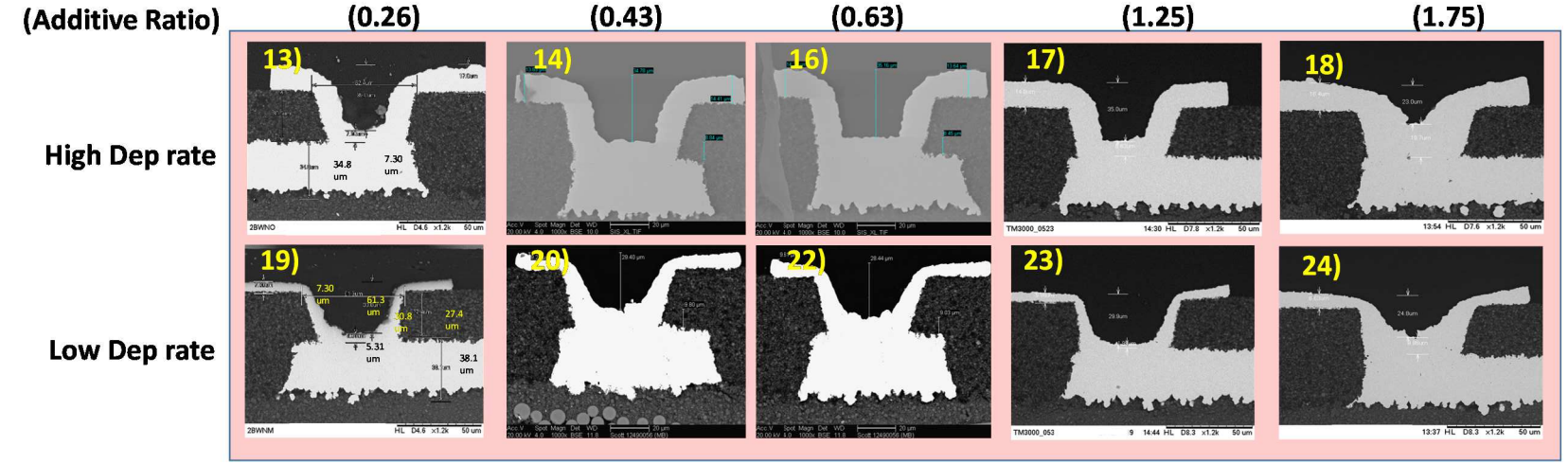

Figure 10.5: (Top row): Experiment 01 – 06 show via fill with various additive ratio for high deposition rate (reverse pulse # 1) utilizing 48°C bath temperature and 65g/l of bulk Cu^{2+} ions on via1 geometry

Figure 10.5: (Bottom row): Experiment 07 – 12 show via fill with various additive ratio for low deposition rate (reverse pulse # 1b) utilizing 48°C bath temperature and 65g/l of bulk Cu^{2+} ions on via1 geometry

(* experiment #15 and #21 had malfunction for those tests and data not presented)

Table 10.4: Electrodeposited Via1 top and bottom thickness and TP ratio measured for Expt# 1 through 24 with various additive ratio for bath temperature 40°C and 48°C with reverse pulse waveform # 1 (high dep rate) and reverse pulse waveform # 1b (low dep rate)

Expt #	Dep Rate	Bath Temp	Additive ratio	XSEM Bottom Thickness (µm)	XSEM Top Thickness (µm)	TP Ratio (Bottom thickness / Top Thickness)
Expt # 1	High Dep rate	40^0C	0.3	14.1	15.4	0.9
Expt # 2	High Dep rate	40^0C	0.4	9.5	16.7	0.6
Expt # 3	High Dep rate	40^0C	0.6	11.0	16.7	0.7
Expt # 4	High Dep rate	40^0C	0.6	7.3	16.9	0.4
Expt # 5	High Dep rate	40^0C	1.3	8.5	15.4	0.6
Expt # 6	High Dep rate	40^0C	1.8	7.5	16.8	0.4
Expt # 7	Low Dep rate	40^0C	0.3	17.9	10.7	1.7
Expt # 8	Low Dep rate	40^0C	0.4	10.3	10.8	1.0
Expt # 9	Low Dep rate	40^0C	0.6	6.6	10.8	0.6
Expt # 10	Low Dep rate	40^0C	0.6	10.3	9.8	1.0
Expt # 11	Low Dep rate	40^0C	1.3	5.8	8.7	0.7
Expt # 12	Low Dep rate	40^0C	1.8	5.8	8.6	0.7
Expt # 13	High Dep rate	48^0C	0.3	7.3	17.0	0.4
Expt # 14	High Dep rate	48^0C	0.4	6.8	14.4	0.5
Expt # 15	High Dep rate	48^0C	0.6			
Expt # 16	High Dep rate	48^0C	0.6	8.5	13.6	0.6
Expt # 17	High Dep rate	48^0C	1.3	8.7	15.1	0.6
Expt # 18	High Dep rate	48^0C	1.8	8.5	16.2	0.5
Expt # 19	Low Dep rate	48^0C	0.3	5.3	7.3	0.7
Expt # 20	Low Dep rate	48^0C	0.4	9.8	9.2	1.1
Expt # 21	Low Dep rate	48^0C	0.6			
Expt # 22	Low Dep rate	48^0C	0.6	9.5	9.3	1.0
Expt # 23	Low Dep rate	48^0C	1.3	4.9	5.6	0.9
Expt # 24	Low Dep rate	48^0C	1.8	3.2	5.4	0.6

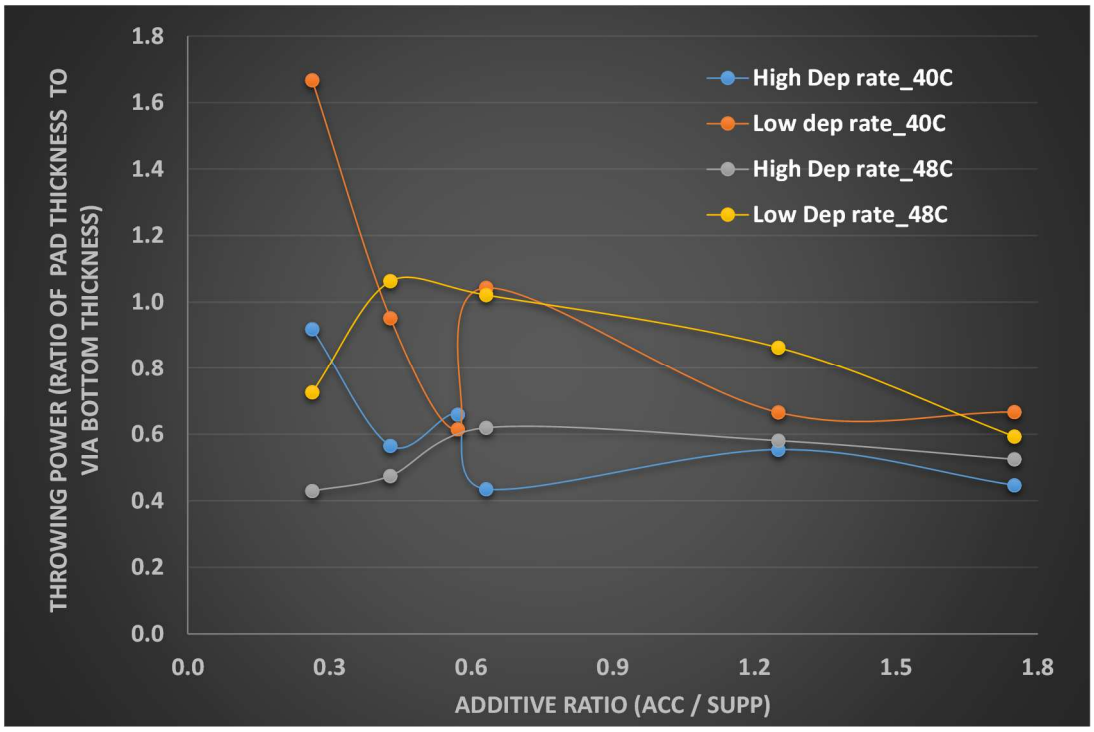

Figure 10.6: Plot of additive ratio Vs Throwing power for high and low deposition rate utilizing 40°C and 48°C bath temperature and 65g/l of bulk Cu^{2+} ions

Section 10.5 Key learning's with various organic additive ratio and bath temperature with reverse pulse waveform # 1 and # 1b

To summarize, 24 different experiments were performed with various additive ratios at high and low deposition rate for bath temperature 40°C and 48°C for reverse pulse waveform type #1 and #1b. Reverse pulse waveform #1 accommodates a maximum reverse current density of 10ASD for 2ms duration. The average current density for deposition was set at 5.4ASD and plated for a duration of 700s post Flash Cu deposition. Reverse pulse #1b was performed for the same 2ms duration with the reverse current density reduced to 5ASD with the average current density for deposition reduced to 2.2ASD. Reverse pulse #1b was performed for an extended time (2100s) to accommodate

for the reduced current density. For samples obtained with Low deposition rate (reverse pulse #1b), the flash Cu deposition was also performed at low current density for an extended duration (1400s). An SEM cross-section was performed for each of those 24 experiments. The results obtained with such cross sections indicate an increase in throwing power for reduced additive ratio at 40°C at high and low deposition rates. A similar characteristic is observed for high deposition rate at 48°C. At low deposition rate an increase in TP is observed until an additive ratio of 0.43 but the subsequent tapering down of the TP could not be explained clearly. Overall trend is still consistent in showing lower additive ratio improving the overall fill ratio. The extent of improvement varies with bath temperature and deposition rate. With 40°C and low deposition rate, TP as high as 1.7 is achieved with an additive ratio of 0.3.

Section 10.6 Design of experiments with various organic additive ratio and bath temperature with reverse pulse waveform # 3 and # 3b

Reverse pulse waveform #1 accommodates a maximum reverse current density of 10ASD for 2ms duration. The average current density for deposition was set at 5.4ASD and plated for a duration of 700s post Flash Cu deposition. Reverse pulse #1b was performed for the same 2ms duration with the reverse current density reduced to 5ASD with the average current density for deposition reduced to 2.2ASD. Reverse pulse #1b was performed for an extended time (2100s) to accommodate for the reduced current density. In order to see the impact of reverse pulse current density and duration on Via5 fill, similar set of experiments performed earlier with reverse pulse #1 and #1b were

repeated with reverse pulse waveform #3 and #3b. Reverse pulse waveform #3 accommodates a maximum reverse current density of 24ASD for 4ms duration. The average current density for deposition was set at 6.53SD. Reverse pulse #3b was performed for the same 4ms duration with the reverse current density reduced to 12ASD with the average current density for deposition reduced to 2.75ASD. Reverse pulse #3b was performed for an extended time (1400s) to accommodate for the reduced current density. For samples obtained with low deposition rate (reverse pulse #3b), the flash Cu deposition was also performed at low current density for an extended duration (1750s). The high deposition rate parameters were matched to Expt #A conditions summarized in Table 10.1. Here again, seven different accelerator to suppressor concentration ratio were studied with the ratio of the additives being varied from 0.26 to 1.75. Each additive ratio was first tested at bath temperature of 40°C (Experiment 25 through 30) with reverse pulse waveform # 3 (high dep rate). The exact set of experiments were then repeated with reduced current density (lower deposition rate) utilizing reverse waveform #3b (Experiment 31 through 36). Experiments 25 through 38 were then repeated with the exact parametric conditions, but the bath temperature increased to 48°C and shown in the DOE table as experimental splits 39 through 52 for high and low dep rates. The experimental run card tabulated in Table 10.5 shows the different parameters studied with reverse pulse waveform type #3 and #3b. The choice of the ratio of the additives selected for this study were kept identical to reverse pulse waveform #1 with an additional ratio at 1.58. During the execution of the experiments, Expt # 41 (high dep rate) and Expt # 48 (low rate) corresponding to additive ratio of 0.57 at 48°C bath temperatures had an

experimental malfunction and those data samples are not analyzed. Expt # 37 (low dep rate) and Expt # 51 (low dep rate) corresponding to additive ratio of 1.58 at 40°C and 48°C bath temperatures had an experimental malfunction and those data samples are not analyzed as well. To summarize, 28 different experiments were performed with various additive ratios at high and low deposition rate for bath temperature 40°C and 48°C utilizing reverse pulse waveform #3 and #3b. An SEM cross-section was performed for each of those 28 experiments.

Section 10.7 Results and discussion with various organic additive ratio and bath temperature with reverse pulse waveform # 3 and # 3b

Results obtained with such cross sections for 40°C bath temperature are shown in Figure 10.7 (25 - 38) and cross sections for 48°C bath temperature are shown in Figure 10.8 (39 - 52). A quick overview of the results published in Figure 10.7 and 10.8 show significantly improved gap fill with Via1 geometry on reverse pulse #3 and #3b compared to fill results obtained with reverse pulse #1 and #1b.

Table 10.5: Experimental run card (Expt# 25 through 52) for Via1 Gap fill evaluation with various additive ratio for bath temperature 40°C and 48°C with reverse pulse waveform # 3 (high dep rate) and reverse pulse waveform # 3b (low dep rate)

(* experiment malfunction for those tests and data not presented further in the study)

Reverse Pulse	Accelerator Conc. (ml/L)	Suppressor Conc. (ml/L)	Ratio	Temperature	Current Density	Expt
Pulse Type # 3	5	19	0.26	40^0C , 48^0C	High	25, 39
Pulse Type # 3	12	28	0.43	40^0C , 48^0C	High	26, 40
Pulse Type # 3	16	28	0.57	40^0C , 48^0C	High	27, 41*
Pulse Type # 3	12	19	0.63	40^0C , 48^0C	High	28, 42
Pulse Type # 3	15	12	1.25	40^0C , 48^0C	High	29, 43
Pulse Type # 3	19	12	1.58	40^0C , 48^0C	High	30, 44
Pulse Type # 3	21	12	1.75	40^0C , 48^0C	High	31, 45
Pulse Type # 3b	5	19	0.26	40^0C , 48^0C	Low	32, 46
Pulse Type # 3b	12	28	0.43	40^0C , 48^0C	Low	33, 47
Pulse Type # 3b	16	28	0.57	40^0C , 48^0C	Low	34, 48*
Pulse Type # 3b	12	19	0.63	40^0C , 48^0C	Low	35, 49
Pulse Type # 3b	15	12	1.25	40^0C , 48^0C	Low	36, 50
Pulse Type # 3b	19	12	1.58	40^0C , 48^0C	Low	37*, 51*
Pulse Type # 3b	21	12	1.75	40^0C , 48^0C	Low	38, 52

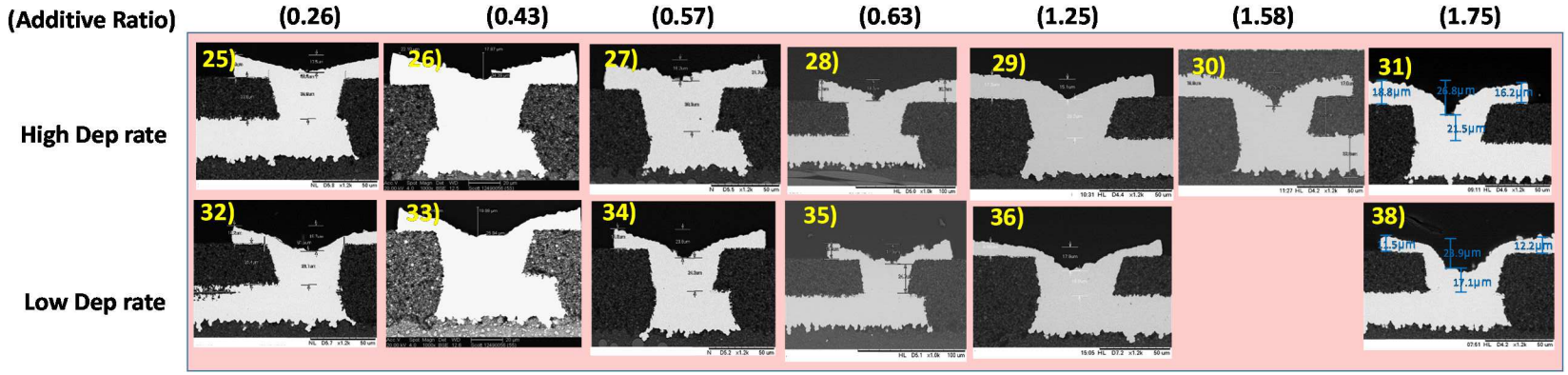

Figure 10.7: (Top row): Experiment 25 – 31 show via fill with various additive ratio for high deposition rate (reverse pulse # 3) utilizing 40°C bath temperature and 65g/l of bulk Cu^{2+} ions for Via1 geometry

Figure 10.7: (Bottom row): Experiment 32 – 38 show via fill with various additive ratio for low deposition rate (reverse pulse # 3b) utilizing 40°C bath temperature and 65g/l of bulk Cu^{2+} ions for Via1 geometry

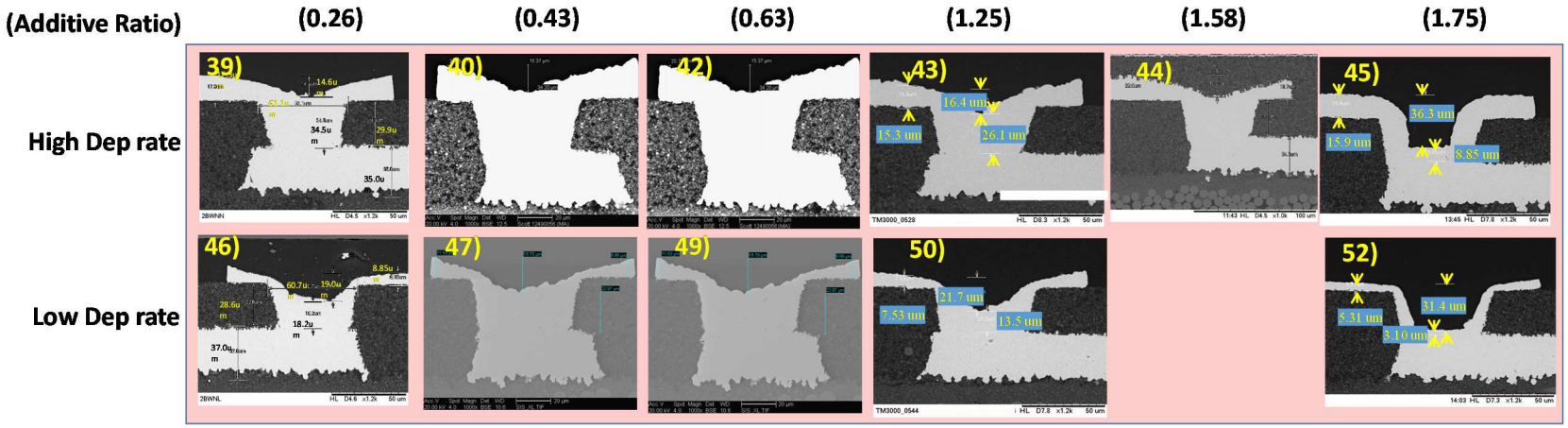

Figure 10.8: (Top row): Experiment 39 – 45 show via fill with various additive ratio for high deposition rate (reverse pulse # 3) utilizing 48°C bath temperature and 65g/l of bulk Cu^{2+} ions for Via1 geometry

Figure 10.8: (Bottom row): Experiment 46 – 52 show via fill with various additive ratio for low deposition rate (reverse pulse # 3b) utilizing 48°C bath temperature and 65g/l of bulk Cu^{2+} ions for Via1 geometry

Furthermore, for these set of tests with reverse pulse waveform #3 and #3b, instead of throwing power, "via recess thickness" was measured and reported. Throwing power values with these results could be confounded by the fact that the via was already filled for most of the conditions and it would be difficult to de-convolute the thickness contribution from the via sidewalls and via bottom in order to truly establish a throwing power that is consistent with the values reported earlier. A schematic cartoon in Figure 10.2 shows the methodology for the measurement of the via recess thickness. Via recess in this study is defined as the amount of via region that is not completely filled.

From the schematic in Figure 10.2, it can be easily ascertained that a sample that shows low via recess thickness would indicate a very good fill bottom-up and vice-verse for a sample that has a poor bottom-up or gap fill with high via recess. In each case the presence of via void was also verified and tabulated in Table 10.6. Profilometric measurement of via recess thickness is tabulated in Table 10.6. Figure 10.9 shows the plot of measured via recess for each of those additive ratio conditions at different deposition rate and temperature. It is notable here that none of the high and low dep rate conditions at 40°C and 48°C show any via voids.

Table 10.6: Electrodeposited Via1 via recess thickness and presence of void measured for Expt# 25 through 52 with various additive ratio for bath temperature 40°C and 48°C with reverse pulse waveform # 3 (high dep rate) and reverse pulse waveform # 3b (low dep rate)

Expt #	Dep Rate	Bath Temp	Additive ratio	Via Recess (µm)	Void Observation
Expt # 25	High Dep rate	40^{0}C	0.3	18.7	N
Expt # 26	High Dep rate	40^{0}C	0.4	22.5	N
Expt # 27	High Dep rate	40^{0}C	0.6	25.3	N
Expt # 28	High Dep rate	40^{0}C	0.6	27.3	N
Expt # 29	High Dep rate	40^{0}C	1.3	16.7	N
Expt # 30	High Dep rate	40^{0}C	1.6	18.5	N
Expt # 31	High Dep rate	40^{0}C	1.8	23.0	N
Expt # 32	Low Dep rate	40^{0}C	0.3	21.4	N
Expt # 33	Low Dep rate	40^{0}C	0.4	23.7	N
Expt # 34	Low Dep rate	40^{0}C	0.6		
Expt # 35	Low Dep rate	40^{0}C	0.6	31.1	N
Expt # 36	Low Dep rate	40^{0}C	1.3	14.6	N
Expt # 37	Low Dep rate	40^{0}C	1.6	20.4	N
Expt # 38	Low Dep rate	40^{0}C	1.8		
Expt # 39	High Dep rate	48^{0}C	0.3	19.5	N
Expt # 40	High Dep rate	48^{0}C	0.4	23.5	N
Expt # 41	High Dep rate	48^{0}C	0.6	16.7	N
Expt # 42	High Dep rate	48^{0}C	0.6	30.4	N
Expt # 43	High Dep rate	48^{0}C	1.3	19.0	N
Expt # 44	High Dep rate	48^{0}C	1.6	21.5	N
Expt # 45	High Dep rate	48^{0}C	1.8		
Expt # 46	Low Dep rate	48^{0}C	0.3	18.4	N
Expt # 47	Low Dep rate	48^{0}C	0.4	24.9	N
Expt # 48	Low Dep rate	48^{0}C	0.6		
Expt # 49	Low Dep rate	48^{0}C	0.6	28.8	N
Expt # 50	Low Dep rate	48^{0}C	1.3	18.7	N
Expt # 51	Low Dep rate	48^{0}C	1.6	22.5	N
Expt # 52	Low Dep rate	48^{0}C	1.8	25.3	N

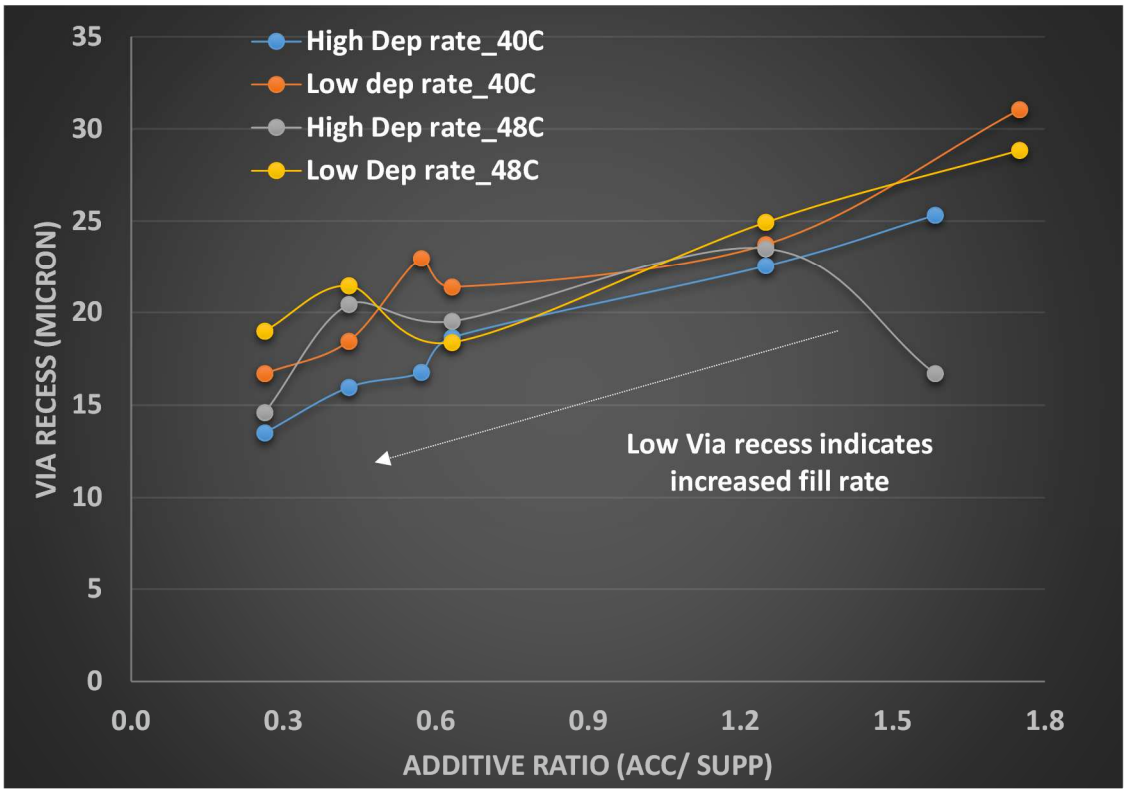

Figure 10.9: Plot of additive ratio Vs Via recess for high and low deposition rate utilizing 40°C and 48°C bath temperature and 65g/l of bulk Cu^{2+} ions

As shown in the plot of Figure 10.9, for 40°C bath temperature at high dep rate (blue line), there is a linear decrease in via recess with the reduction in additive ratio. Reduced additive ratio directly correlates to increased suppression. This result indicates that as the overall suppression characteristic of the bath is increased, an improvement in fill rate can be obtained. Figure 10.9 also shows plot for 48°C bath temperature at high dep rate (Grey line). Decrease in via recess is seen with reduced additive ratio similar to 40°C condition. Similarly for 40°C and 48°C bath temperature at low dep rates, a decrease in via recess is observed with reduced additive ratio. These findings are consistent with the earlier results obtained with those on the Via5 geometry. It is to be noted that no via voids are observed for most high deposition rate conditions.

Section 10.8 Key learning's with various organic additive ratio and bath temperature with reverse pulse waveform # 3 and # 3b

To summarize, 28 different experiments were performed with various additive ratios at high and low deposition rate for bath temperature 40°C and 48°C for reverse pulse waveform type #3 and #3b. An SEM cross-section was performed for each of those 28 experiments. The results obtained with such cross sections indicate a reduction in via recess for decreased additive ratio at all temperatures and reverse pulse durations. Via voiding is not observed at high deposition rates and void-free via fill is obtained at all deposition rates with the optimized fill performance at low additive ratio conditions.

Section 10.9 Summary of additive ratio optimization for via1 geometry

Incorporation of reverse pulse methodology with reverse pulse waveforms #1 and #3 shows void-free ill performance with Via1 geometry. However, a high via recess ~10um was observed. Additional process parameters that control the deposition process had to be identified to further improve the throwing power inside Via1 geometry. Six different combination ratio of additives such as accelerator and suppressor were then tested at two different bath temperatures of 40°C and 48°C. These sets of experiments were performed with reverse pulse #1 and reverse pulse #1b to ascertain the throwing power with different additive combinations. A low additive ratio of accelerator to suppressor shows improved fill performance at all conditions. Furthermore, when these sets of experiments were performed with reverse pulse #3 and #3b that incorporates larger reverse current density and duration, a complete void-free gap fill process was obtained at all deposition rates that were tested. Decreased via recess indicating better fill was observed at small additive ratio combinations of accelerator to suppressor. With increased reverse pulse duration, fill behavior (pertaining to throwing power) were similar at 48°C compared to 40°C. Thus, these efforts enable a capable reverse pulse deposition process with optimized additive concentration for Via1 geometry that shows void-free fill and improved overall fill performance. In chapter X1, a simulation effort is undertaken to understand the limitations of TP improvement with the present additive system and identify new capabilities to further improve TP. The simulation model is validated to experimental data collected thus far on Via1 and Via5 geometry.

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Chapter XI

SIMULATION OF ADDITIVE EFFECT FOR SUPER FILLING OF COPPER FOR IC SUBSTRATE APPLICATIONS

Section 11.0 Introduction

Early in 2001, West *et al*[1] developed a three additive model for super filling of copper for damascene applications. In his work he utilized molecules with different concentration ratios of SPS (bis (sodium sulfo propyl) disulfide) as an accelerator, JGB [Jannus Green B] as a leveler and PEG [Polyethylene Glycol] as suppressor to obtain throwing power and fill behavior for submicron feature scale applications. In their work, the activity of PEG and Cl^- were lumped together to explain the activity of suppressor. Furthermore, in their work, PEG was considered to be not consumed at surface or incorporated into growing Cu deposit. In such a scenario, there is no concentration gradient of PEG species in the electrolyte solution. The role of PEG was primarily defined as an adsorbate that physically adsorbs to the surface and blocks sites for Cu reduction reaction. The role of SPS (accelerator) was defined to remove the adsorbed PEG species from the surface and free up the surface sites for Cu reduction reaction. The role of JGB (leveler) was defined similar to PEG, wherein it blocks sites of Cu reduction but is not affected by SPS activity. In fact, JGB and PEG compete for surface sites. The kinetic parameters in this model were characterized based on flat or non-patterned RDE (Rotational Disc Electrode) experiments utilizing Linear Sweep Voltammetry (LSV). This potentiostatic 2D model was then used to map out gap fill results throwing power, (TP) for various

additive concentrations. Inclusion of shape evolution simulations (to capture feature gap-fill during metallization) for a subset of cases was used to demonstrate that short time (no appreciable feature deformation) throwing power results were sufficient to predict the relative robustness of a gap-fill for a given set of additives' concentrations. Model results were partially validated by experimental gap-fill data. However, it was later demonstrated, that this model would not predict "momentum plating" (or bump formation directly over features) in sub-micron features which for this additive mixture occurred as concentration of JGB was driven to 0. It needs to be noted here that surface reactions can be quite complex, and this three additive system was primarily developed to explain an overall trend in additive behavior for gap fill behavior than to accurately predict the throwing power for a given system.

Section 11.1 Simulation model

In the present study a simulation effort was undertaken by adapting the three additive model that West and Radek *et a l*[1] had developed for the existing two additive system that was experimentally studied thus far. In our experimental studies, two proprietary additives namely "SBP2 Accelerator" and "SBP2 Leveler" purchased from Atotech Inc., were utilized for the experiments. The exact molecular details of these species were unknown for this study and the functionality of these species were expected to behave primarily as accelerator and suppressor that are referenced in scientific literature studies. Therefore, the activity of these species were roughly approximated to be that of similar to SPS and PEG molecules. Reaction rate constants and equilibrium constant for adsorption

for these species were utilized from the work of West *et a l*[1] in the three additive system to develop the model. Kinetic constants adapted from those studies are tabulated in Table 11.1 Other electrodeposition parameters such as bulk concentration of Cu^{2+} ($C_{Cu^{2+},\infty} = 65g/l$) were matched to the experimental conditions tested earlier The purpose of this simulation effort was to predict the general trend in additive behavior as a function of accelerator to suppressor ratio for IC substrate application and establish a correlation to the experiment results obtained till now. Therefore, the contribution from reverse pulse for TP improvement was not accounted in the simulation study. Instead the deposition current density utilized in the study was averaged to the overall average current utilized with various reverse pulse waveforms studied so far that accounts for both the FWD and REV current density and duration. In order to have a meaningful correlation to the data, only the TP data obtained from reverse pulse waveform #1, which has the smallest reverse current amplitude of 10ASD for 2ms with the average current density at 5ASD was utilized for comparison. Reverse pulse waveform #1B with the net average current density as 2ASD was also utilized for additional data comparison. More aggressive reverse pulse waveforms were not utilized for comparison. Furthermore, this model does not show feature fill by fitting parameters but was only utilized to estimate throwing power as function of various additives concentrations ratios. Unlike the work of West *et al*[1] for sub-micron, Damascene plating, present application was operating closer to the mass transport limit (to enable higher fill rates of these larger features) of Cu^{2+} hence the effect of Cu^{2+} ion depletion during deposition could not be neglected. It has been incorporated into this study utilizing the same principles as those adapted in Chapter VII.

The model testing was applied to V1 and V5 geometries and to test whether model results contradict any available existing data trends.

Section 11.2 Model construction

The copper plating current density *i* depends on this interfacial overpotential according to generalized Butler Volmer kinetics

$$\boldsymbol{i} = \boldsymbol{i_0} \frac{\boldsymbol{C_{Cu^{2+},0}}}{\boldsymbol{C_{Cu^{2+},\infty}}} \boldsymbol{(1-\theta_{eff})} \left[\boldsymbol{exp}\left(\frac{\boldsymbol{(-\alpha)nF(E-E^0)}}{\boldsymbol{RT}} \right) \right] \qquad \textbf{(11.1)}$$

where α is the symmetry factor between cathodic and anodic reaction, i is the current density and i_0 is the exchange current density, n is the number of electrons, R is a gas constant, T is the temperature of the reaction and E and E^0 are the applied potential and standard reduction potential. $C_{Cu^{2+},0}$, $C_{Cu^{2+},\infty}$ is the concentration of Cu^{2+} at the surface and bulk of the solution. $\boldsymbol{\theta_{eff} = \theta_{PEG} + \theta_{JGB}}$ represents surface sites blocked for Cu^{2+} reduction. This effective surface blockage is a result of multiple additive species interacting with each other such as suppressor (PEG/Cl^-), Accelerator (SPS) and Leveler (JGB). For our two component study, the concentration of leveler (JGB) was equated to be negligible, therefore, $\boldsymbol{\theta_{eff} \approx \theta_{PEG}}$. Accounting only for the near surface effects on short length scale where diffusive transport and surface reaction kinetics dominate, the current density (i) simplifies to,

$$\boldsymbol{i = k \frac{C_{Cu}{}^{2+,0}}{C_{Cu^{2+},\infty}} (1-\theta_{PEG})} \qquad \textbf{(11.2)}$$

Where k is a kinetic constant for deposition that can vary in time with overpotential but not spatially and θ_{PEG} is the effective surface coverage obtained with the additives (suppressor). Therefore, $(1-\theta_{eff})$ is the net reduction due to surface blockage by additives. Deposition ratio TP (TP=throwing power) at early stages of plating is a very useful metric for determining feature-fill robustness of a process. Given the large feature size and sluggish mixing present in the current system, a steady state gradient concentration develops very early on in plating process because of consumption along vertical sidewall. Early in Chapter VII, based on Peclet number analysis we determined that the effect of convective solution mixing (relative to diffusion) present inside the via is negligible with PE<<1 for a via depth of 25μm. Increased via depth of ~53μm for the larger Via5 is likely to show even more sluggish mixing at the via bottom. Wagener number analysis indicated ohmic resistance contributions are also small inside via regions. Therefore, concentration gradients (driven by consumption at the interface and diffusive transport inside the via) dominate current distribution inside the via's. Unlike an RDE system, determination of an effective diffusion boundary layer thickness in an industrial electroplater is not straightforward. The adopted West et al model was run for a range of diffusion boundary layer thickness values until a match with throwing power results was obtained. A value of ~1000microns (corresponding to <5rpm on an RDE) yielded good agreement with data. This suggested a relatively sluggish mixing near the panel surfaces in our reactor. Therefore, at sufficiently high deposition rates (higher plating currents), most benefits of additives can be lost. Simulations were carried out using an in-house, 2D boundary element code to solve a steady state diffusion equation (from bottom of a via to

the edge of the diffusion boundary layer thickness) subject to boundary conditions defined in equations 11.2 to 11.9.

$$\nabla^2 c_{SPS} = 0 \tag{11.3}$$

$$\nabla^2 c_{JGB} = 0 \tag{11.4}$$

$$-D_{SPS}\frac{\partial c_{SPS}}{\partial n} = k_{r,SPS}\theta_{SPS} \tag{11.5}$$

$$-D_{JGB}\frac{\partial c_{JGB}}{\partial n} = k_{r,JGB}\theta_{JGB} \tag{11.6}$$

$$\theta_{SPS} = \frac{K_{SPS}c_{SPS,0}}{1+ K_{SPS}c_{SPS,0}} \tag{11.7}$$

$$\theta_{PEG} = \frac{K_{PEG}\ exp\left(-\alpha\theta_{SPS}^{0.5}\right) c_{PEG,\infty}}{1+ K_{PEG}\ exp\left(-\alpha\theta_{SPS}^{0.5}\right) c_{PEG,\infty}} \tag{11.8}$$

$$\theta_{JGB} = \frac{K_{JGB}c_{JGB,0}}{1+ K_{JGB}c_{JGB,0}}\ (1 - \theta_{PEG}) \tag{11.9}$$

The interaction between SPS and PEG was introduced using a Frumkin isotherm[1, 2]. Table 11.1 captures the various simulation parameters utilized for this simulation.

Table 11.1: Parameters used for the simulation study

Parameters	Values
$C_{Cu^{2+},\infty}$	1.01 X 10^{-3} mol cm^{-3} or (65g/l)
$C_{PEG,\infty}$	Vary assuming (Mw 3350)
C_{JGB}	~0 (0.01 PPM)
C_{SPS}	vary
$D_{Cu^{2+}}$	5 X 10^{-6} cm^{-2} s^{-1}
D_{JGB}	1 X 10^{-6} cm^{-2} s^{-1}
D_{SPS}	1 X 10^{-6} cm^{-2} s^{-1}
k_{SPS}	1 X 10^{-10} mol cm^{-2} s^{-1}
k_{JGB}	2 X 10^{-11} mol cm^{-2} s^{-1}
$\mathrm{K_{JGB}}$	5.11 X 10^{9} mol^{-1} cm^{-3}
K_{PEG}	3.61 X 10^{8} mol^{-1} cm^{-3}
K_{SPS}	3.08 X 10^{7} mol^{-1} cm^{-3}
α	7.0

Section 11.3 Simulation results

For the present simulation efforts two different via geometry Via5 and Via1 were chosen to study. Experimental data of the TP for various additive ratios obtained with these different geometries were summarized in Chapter IX and X. Simulation efforts were undertaken to compare the results with the recently exhibited experimental data and extrapolate the behavior to predict additional knobs for improved TP (throwing power). Key features of the simulation model can be summarized as,

A) Additive Effect → self-consistent kinetic model from West et al[1]

B) Solution Mixing → modeled as boundary layer thickness and optimized to fit with experiment data

C) Plating Rate → model is potentiostatic so Cu^{2+} depletion is changed by modifying its reduction reaction rate constant

Figure 11.1 shows a cartoon of the two different via geometry tested for this simulation effort along with their corresponding dimension. An example of SEM cross-section obtained with experimental studies obtained in Chapter IX and X for Via5 and Via1 are shown in Figure 11.1b to show how TP ratio were obtained experimentally.

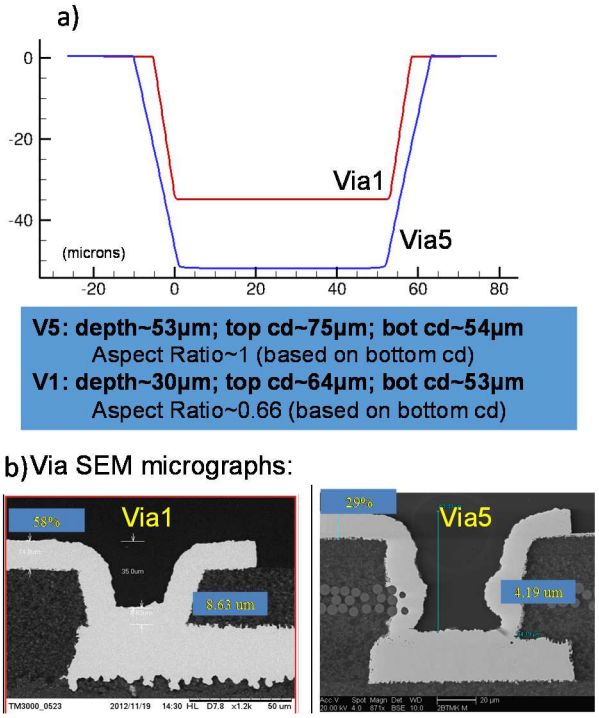

Figure 11.1: a) Schematic of Via5 and Via1 geometry and b) Sample SEM images utilized for TP calculation utilized in experimental studies for Via1 and Via5 geometry

To begin with, two initial simulation tests were run to check the validity of assumptions and the overall ability of model to predict throwing power. In the first simulation run, the distribution of Cu^{2+} at the via top and via bottom were generated assuming an electrodeposition system without the presence of additives. Figure 11.2a shows the Cu^{2+}

distribution in the absence of additives and Figure 11.2b shows the corresponding (i/i_{avg}) at the top and bottom position of the via. It can be easily inferred that in the absence of additives the throwing power (TP) is much less than 1 (~0.14). Simulation test 2 was repeated with the same parametric set up but accounting for the presence of additives. For this run, two different additive ratio were tested for both Via1 and Via5 geometry. C_{JGB} was set at 0.1PPM and 10PPM and the corresponding concentration for C_{SPS} was set at 9PPM and 0.1PPM. C_{PEG} was set at 300PPM. Figure 11.3a and 11.3b shows the corresponding Cu^{2+} ratio and i/i_{avg} along the via locations. Via top regions shows significantly reduced thickness for increased C_{JGB} concentration compared to the increase in concentration of SPS (C_{SPS}). This early simulation tests confirms that TP>1 can be obtained with the incorporation of additives and the concentration ratio of the additive is a key metric that needs to be optimized for these various via geometries. Figure 11.4 shows the comparison of simulation predicted TP at high and low reaction rates for via5 and via1 geometry with the corresponding experimental data obtained earlier at 40°C and 48°C bath temperature. The trend prediction with the model seems consistent with the experimental data obtained earlier in that a low accelerator and high suppressor concentration tends to increase the TP at high reaction rate. A maximum throwing power of 1 can be obtained at low reaction rates with no change in TP ratio as a function of additive ratio. Figure 11.5 has the simulation prediction of throwing power (TP) with various C_{SPS} (Accelerator) and C_{PEG} (Suppressor) ratio's at high reaction rate for Via 5 (Figure 11.5a) and for for Via1 (Figure 11.5b) geometry. In all cases the model prediction pertains to very high suppressor concentration and a lower accelerator concentration for

increased TP. Even at the highly reduced ratio, at high reaction rates the maximum TP that can be achieved for these geometries is on the order 0.6 -0.8. Previously in Figure 11.3b, we saw significantly higher TP with the addition of JGB leveler. It is likely that the present system operates with two additive components identified as SPS and PEG with a reasonably consistent match of the simulation data to experimental results.

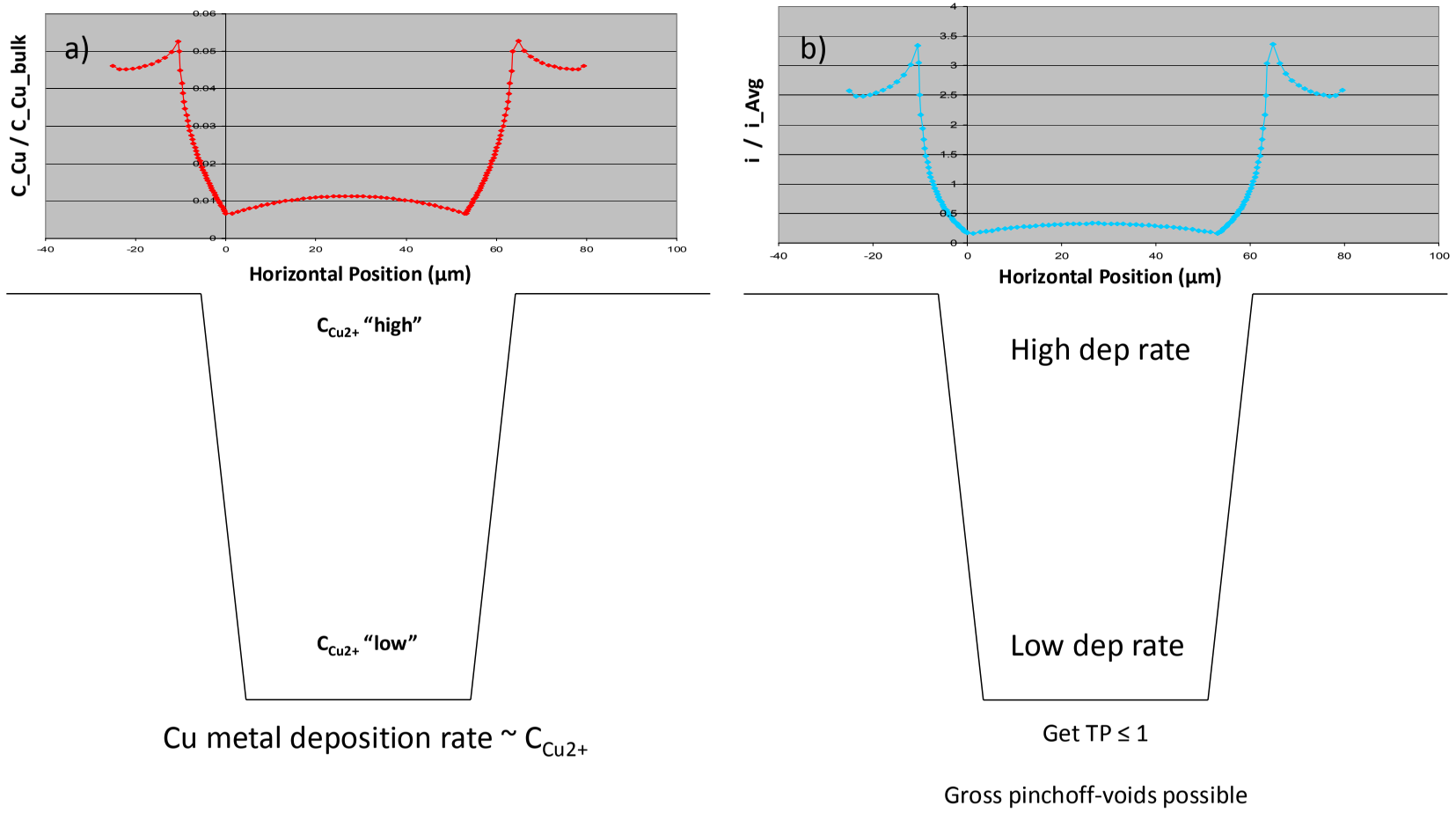

Figure 11.2: a) Simulation report of Cu^{2+} concentration distribution inside the via in the absence of additives b) Simulation report of current distribution inside the via in the absence of additives

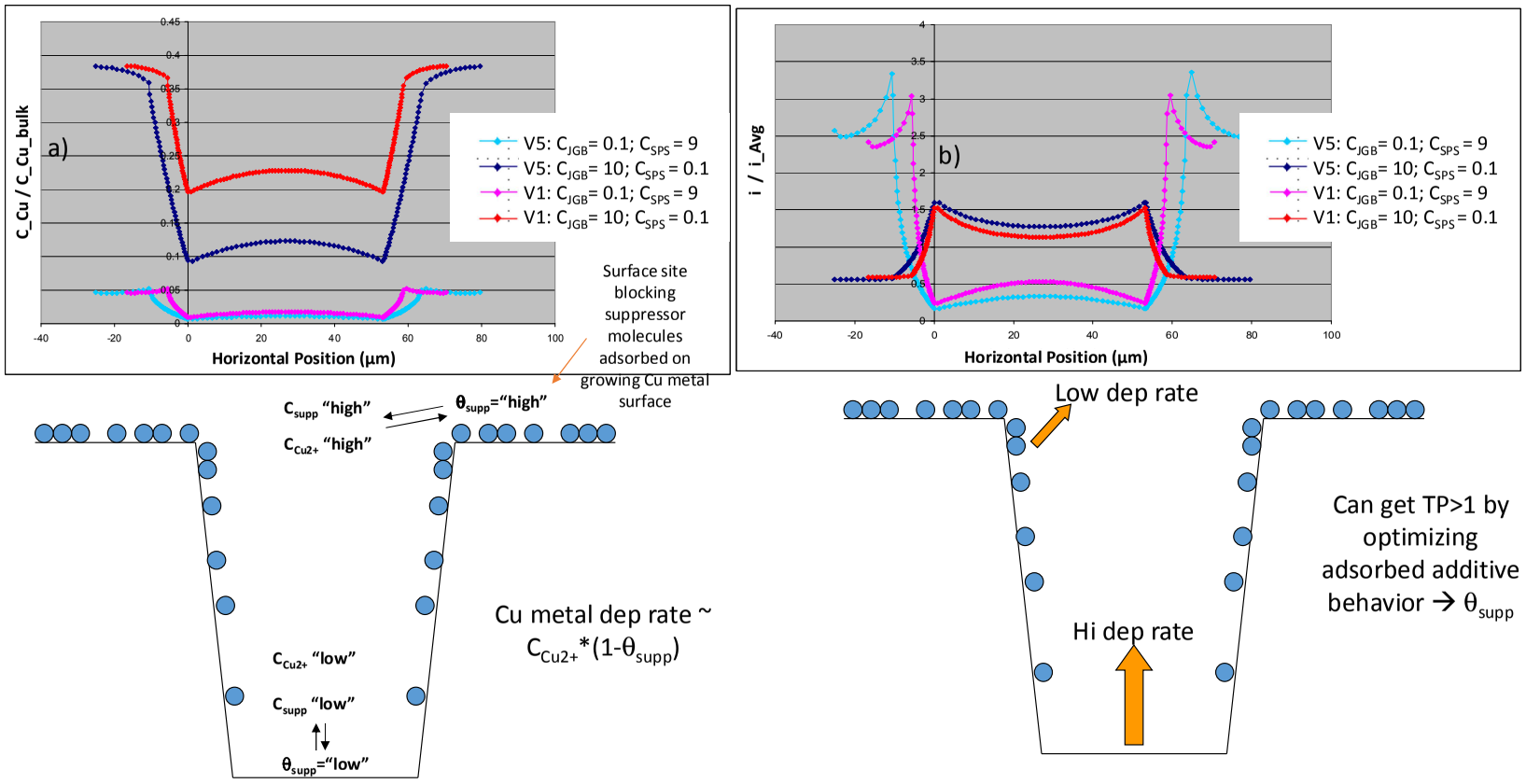

Figure 11.3: a) Simulation report of Cu^{2+} concentration distribution inside the via in the presence of additives b) Simulation report of current distribution inside the via in the presence of additives

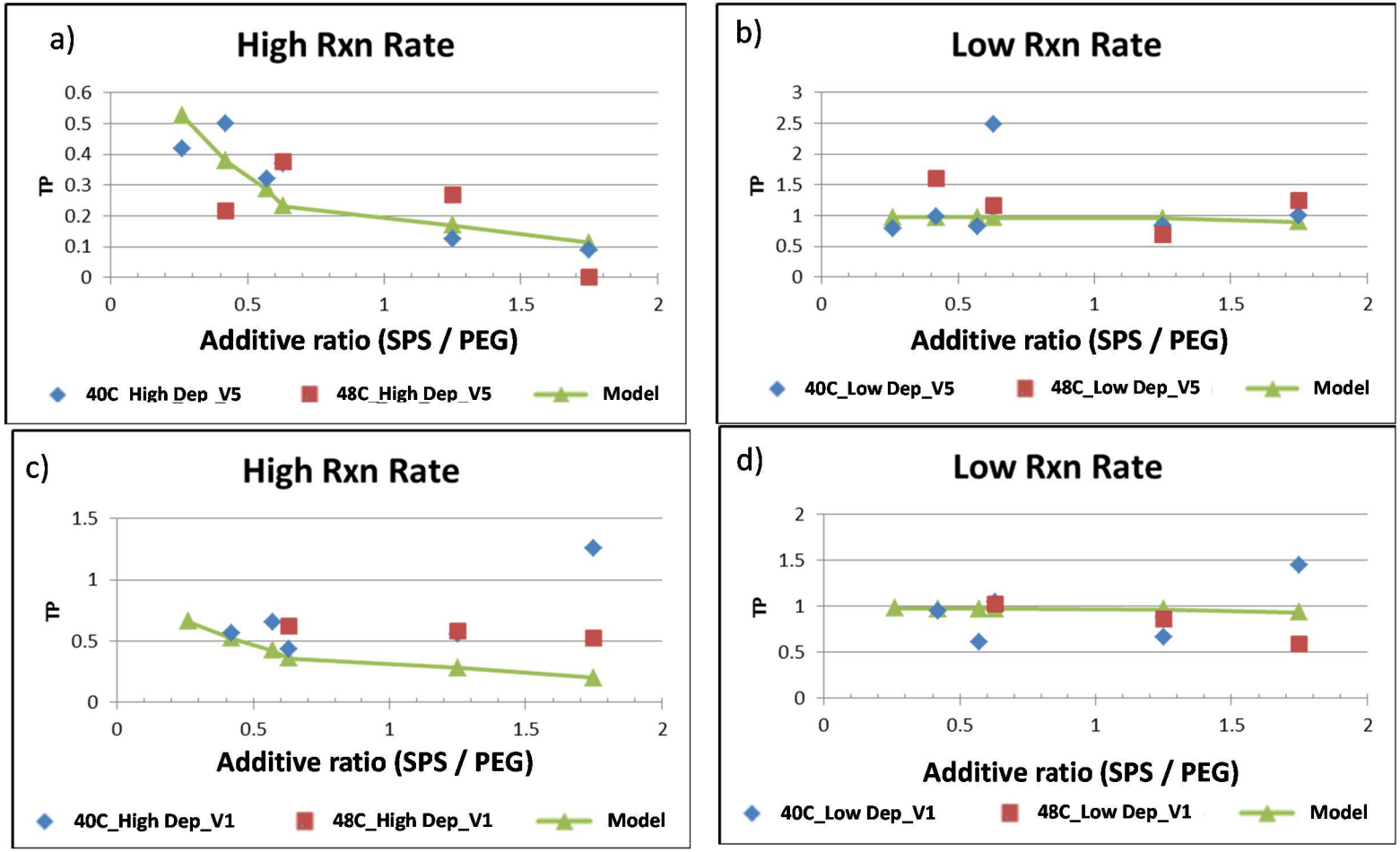

Figure 11.4: Comparison of experimental and simulation results for TP Vs Additive ratio for a) Via5 geometry_ high Reaction rate b) Via5 geometry_ low reaction rate a) Via1 geometry_ High Reaction rate b) Via1 geometry_ low reaction rate

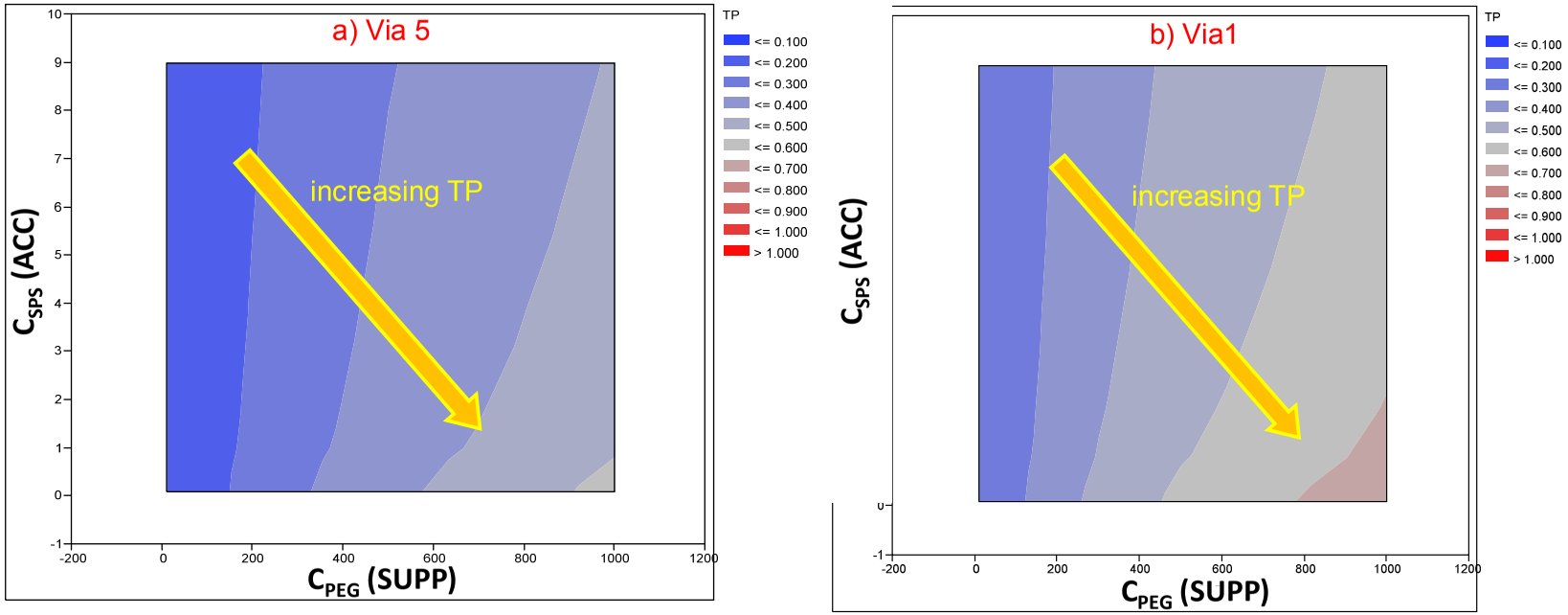

Figure 11.5: Simulation prediction of throwing power (TP) with variation in CSPS (Accelerator) and CPEG (Suppressor) at high reaction rate

Section 11.4 Summary

A diffusion-reaction solver for predicting the throwing power (TP or ratio of current densities) inside a feature as a function of additives' concentrations during electrodeposition was developed and results were compared to the experimentally obtained TP data. Model results correctly captured the trends seen in data as well as the magnitude of the TP ratio (for most of the available data). Model results suggest that the present set of additives can only enable a relatively weak TP with the prediction that the present system likely has SPS and PEG components and needs incorporation of a Leveler species for improved TP. In chapter XII, we showcase a void-free gap via fill process for all via geometry with single optimized bath composition that has high suppression along with the incorporation of reverse waveform methodology. Improved uniformity for pattern features is also shown and the study concludes with microstructure validation for the newly optimized bath composition to show a capable and reliable electrodeposition process for IC substrate applications.

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CHAPTER XII

CAPABLE ELECTRODEPOSITION METHODOLOGY FOR IC SUBSTRATE APPLICATION ACROSS ALL VIA GEOMETRIES

Section 12.0 Introduction

IC substrate applications are made up of stacks of various geometry. So far we discussed the fill characteristics and gap fill behavior of each of these via geometry independently. Early in the process, voids were observed across all geometry and optimization of the fill process was needed with the incorporation of reverse pulse methodology. Figure 12.1 shows the void observed across Via0, Via1 and Via5 geometry with 25g/l of bulk Cu^{2+} concentration with reverse pulse waveform #3 across via 0, via 1, via 5 and stacked via geometries. For optimization, in certain cases incorporation of reverse pulse waveform accounting for mass transfer limitation with increased bulk electrolyte concentration enabled void-free fill while in the case of Via5, optimization of additive ratio and increased bath temperature was needed to improve the mobility of the ions to the via bottom and obtain better throwing power. For IC substrates, besides achieving void-free fill, the electrodeposition process also needs to generate uniform film deposit across patterned FLS features utilizing the same process conditions. Table 12.1 summarizes the various via geometries and line space dimensions studied of each layer with the test coupon far. Each layer presents unique via geometries along with a need to deposit uniform copper thickness on finely patterned regions in each layer.

Table 12.1: Summary of via dimension and FLS structures with the test coupon

Plating Summary	Via bottom diameter	Via Depth	FLS widths studied
V0 / Layer 1	25µm	25 -30µm	9µm, 13µm, 77µm, Planes
V1 / Layer 2	50µm	25µm	9µm, 13µm, 77µm, Planes
V2 / Layer 3	50µm	25µm	9µm, 13µm, 77µm, Planes
V5 / Layer 4	75µm	65µm	13µm, 77µm, Planes

Section 12.1 Reverse pulse waveforms with optimized additive ratio for all via geometries

Experimental results so far (learning's from Chapter IX and X) with Via5 and Via1 geometry indicate that a low additive ratio of 0.26 continues to show improved gap fill performance. This low additive concentration ratio of accelerator to suppressor directly correlates to increased suppression needed early in the deposition process to generate differential fill across the top of via region and via bottom. In all these test cases, the concentration of the Cl^- ion species in the bulk electrolyte was maintained at 50PPM. We discussed in Chapter II that the formation of a film of CuCl very early in the deposition process on the cathodic Cu seed surface is key to the adsorption of the accelerators at the via bottom corners and suppressor additives at via top surface. This phenomenon eventually leads to differential fill. In the absence of Cl^- molecule no additive adsorption occurs[1]. Kondo *et al*[2] show increase in TP with increase in Cl^- concentration for via geometries of 30µm depth and via opening of 100µm and argue that the increased Cl^-

concentration enables generation of more Cu(I) thiolate species and improved TP. In order to validate the hypothesis that an increased suppression is needed to optimize void-free bottom-up fill, an additional experiment with an accelerator to suppressor additive ratio of 0.26 was tested across all via geometries such as Via0, Via1, Via2, Via5. This experiment was conducted with the concentration of the Cl- species increased from 50PPM to 80PPM. Bulk concentration of the copper was maintained at 65g/l. Figure 12.2 shows the 3D X-ray image of a stacked via with various via geometry with the bottom layer as Via0 and Via1, Via 2 and Via5 stacking on top in that order. Electrodeposition was performed with the electrolyte condition described above with the bath temperature set at 40°C. Flash Cu deposition was performed to prevent seed dissolution and via fill deposition was then performed with reverse pulse waveform #3 that was classified as high Cu deposition rate in chapter X for via geometry Via0, Via1 and Via2. It is to be noted here that Via1 and Via2 are identical geometries. For Via5 geometry, reverse pulse waveform #2b with low copper deposition rate was utilized. As shown with the 3D X-ray image in Figure 12.2, the via stack shows completely filled via's without any entrapped voids across all Via geometry.

Section 12.2 Results and discussion with non-uniform deposition across all via geometry

A high throwing power with the via bottom plating at an increased deposition rate than via top leads to void-free fill and this phenomenon can be established with the incorporation of reverse pulse methodology. IC substrates have large via sizes that

require a strong reverse pulse waveform with high reverse charge to enable bottom-up fill. In the absence of strong leveler or other additive species to arrest the accelerated growth of copper, bottom-up fill process is likely to continue uncontrollably leading to a phenomenon termed as “momentum plating”. Momentum plating causes non-uniform metal deposit across finely patterned regions. For IC substrates, there is a strong need to establish uniform deposit thickness in patterned FLS regions in conjunction with enabling gap fill of via’s. Optimization of reverse pulse waveform to arrest momentum plating and enabling uniform deposition is therefore critical to achieve a reliable IC substrate package.

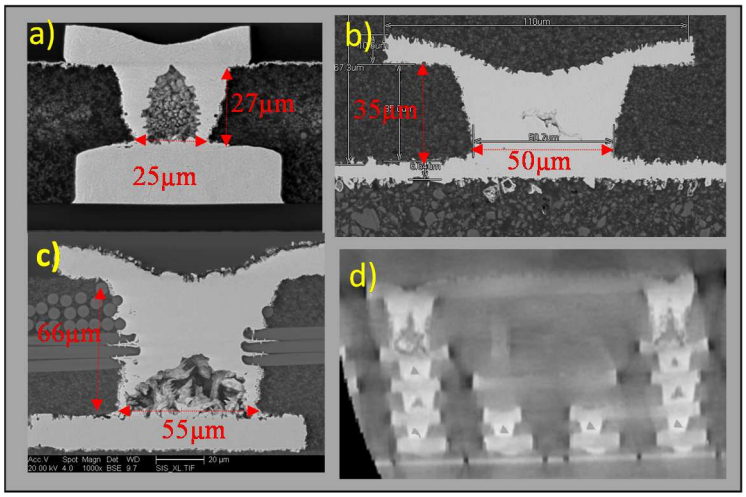

Figure 12.1: SEM Micrograph of various via geometry (a) Via 0, (b) Via 1 (c) Via 5 and (d) stacked via of the test coupon obtained after electrodeposition with reverse pulse methodology at 36°C bath temperature and 25g/l of bulk Cu^{2+} ions, with an additive ratio of 0.75 and Cl^- at 50PPM

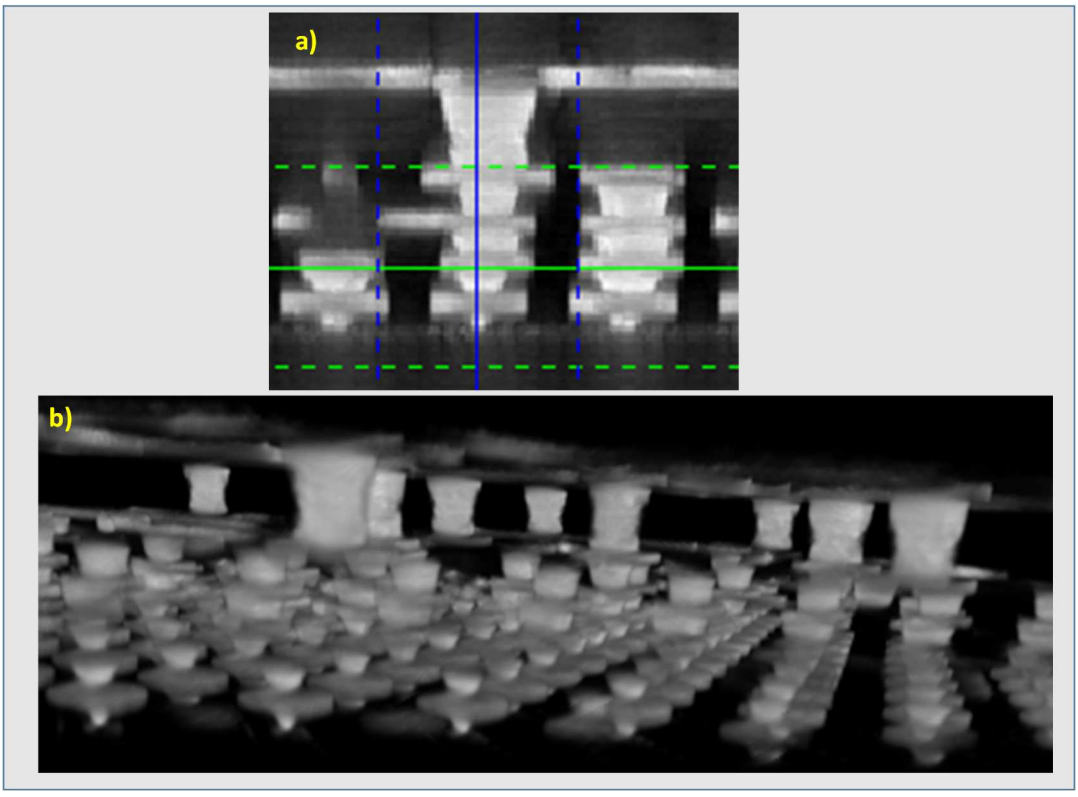

Figure 12.2: Three dimensional X-ray image of stacked via of the test coupon obtained after electrodeposition with reverse pulse methodology at 40°C bath temperature and 65g/l of bulk Cu^{2+} ions, with an additive ratio of 0.26 and Cl^- at 80PPM

For this reason, a balance needs to be reached with an optimization to reverse pulse current density and duration to obtain uniform copper deposit wherein the variation in thickness of the feature is minimized. This needs to happen while ensuring the void entrapment inside the via region is prevented. Recapturing the learning's from chapter IX, although void-free fill is attained with the incorporation of reverse pulse waveform #2 for via0 and via1 geometries, incorporation of a reverse pulse amplitude of 40ASD for 4ms duration with this waveform, provides highly non-uniform copper surface with "ski sloped" pads as shown in Figure 12.3a. Fine trace and large pad regions tend to plate at a different rate. Fine trace regions plate tend to plate thick while the surrounding large pad regions show significantly lower thickness. Non-uniform "ski slope" topography is also observed with the large pads. Figure 12.3a and 12.3b show a qualitative contour plot of the non-uniformity observed on the surface with the thickness of the finer 9μm trace regions being much higher than the surrounding. The shape of the surrounding pads is also not planar with the establishment of momentum plating with these large reverse pulse amplitudes as shown in Figure 12.3a for Via0, Layer 1 and Figure 12.3b for Via5, Layer 4. Figure 12.3c show the profilometer measured deposit thickness across different features for each via layer deposition with reverse pulse waveform #2.

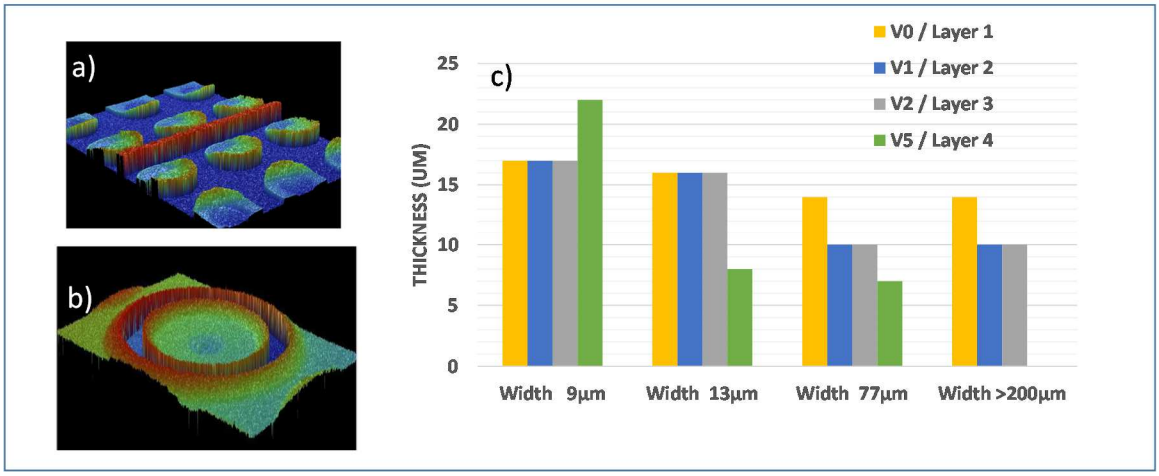

Figure 12.3: (a) Thickness contour map of Layer 1 with reverse pulse waveform # 2, additive ratio of 0.75, 36°C bath temperature and 65g/l bulk Cu^{2+} concentration (b) Thickness contour map of Layer 4 with reverse pulse waveform # 2, additive ratio of 0.75, 36°C bath temperature and 65g/l bulk Cu^{2+} concentration (c) Profilometer thickness measurement of all features at Layers 1,2,3,4 with additive ratio of 0.75, 36°C bath temperature and 65g/l bulk Cu^{2+} concentration

Section 12.3 Uniform FLS plating with void-free fill across all via geometry

In order to address the large ski slope and non-uniform deposit observed with reverse pulse waveform #2 and to preserve the void-free gap fill capability that was previously established, a milder reverse pulse waveform # 3 was tested for Via0 and Via1 geometry. The goal was to generate uniform FLS plating along with void-free fill. These reverse pulse waveforms were tested with an optimized additive ratio of 0.26 along with the bath temperature at 40°C and the bulk concentration of Cu^{2+} maintained at 65g/l. This condition provided void-free fill across via0 and via1 geometry as shown in Figure 12.2 earlier. As shown in Figure 12.4a, the contour maps of test coupons plated with the optimized additive ratio of 0.26 along with reverse pulse waveform #3 exhibits very uniform trace and pad regions with minimal variation in plating deposit thickness. Non-

uniform “ski slope” profile is also eliminated. Figure 12.4b shows the contour map of Layer 4, Via5 geometry. Via5 geometry was tested with reverse pulse waveform #2b that deposits at low deposition rate due to the presence of glass cloth fiber. It’s also notable that very fine feature of 9µm was not included in the coupon design for this layer. The rest of the parametric conditions such as electrolyte concentrations, additive ratios and bath temperature were kept identical to the earlier testing. As shown in Figure 12.4a and 12.4b, the shape of the surrounding pads looks planar and uniform.

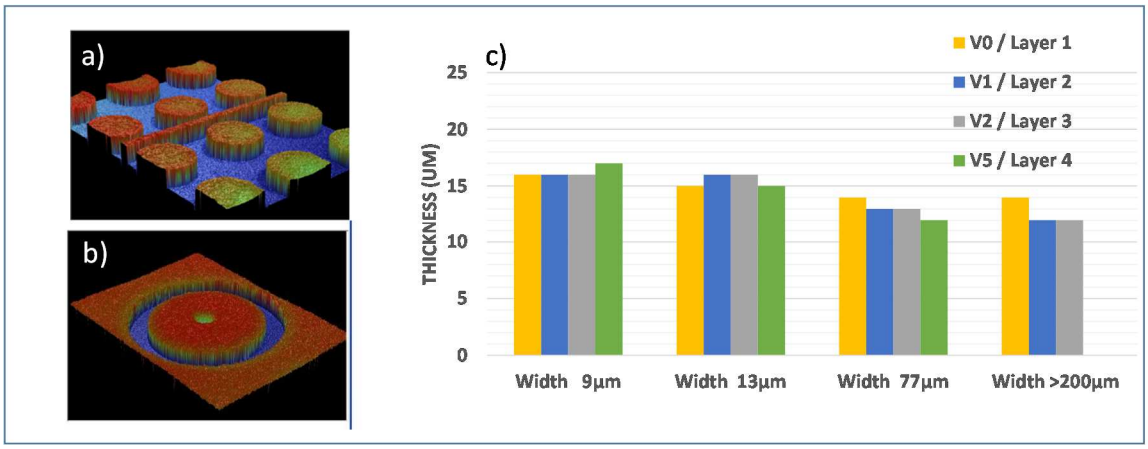

Figure 12.4: (a) Thickness contour map with reverse pulse waveform # 3 waveform at layer1 with optimized additive ratio of 0.26 at 40°C bath temperature and 65g/l bulk Cu^{2+} concentration (a) Thickness contour map with reverse pulse waveform # 2b waveform at layer4 with optimized additive ratio of 0.26 at 40°C bath temperature and 65g/l bulk Cu^{2+} concentration (c) Profilometer thickness measurement of all feature regions at different via layers with optimized additive ratio of 0.26 at 40°C bath temperature and 65g/l bulk Cu^{2+} concentration

Figure 12.3c show the profilometer measured deposit thickness across different features for each via layer deposition with reverse pulse waveform #2. The measured features were at the identical location as the data reported in in Figure 12.3 with reverse pulse waveform # 2. A quick comparison of thickness range as plotted in Figure 12.5 shows

that the non-uniformity in thickness (range) was reduced significantly with the introduction of a milder reverse pulse waveform and optimized additive ratio at a bath temperature of 40°C (orange line, Series #2) compared to a high amplitude reverse pulse waveform operating with a higher additive ratio and 36°C bath temperature (blue line, Series #1). By enabling an optimized reverse pulse plating methodology, low cost and high yield plating process is delivered for substrate plating industry.

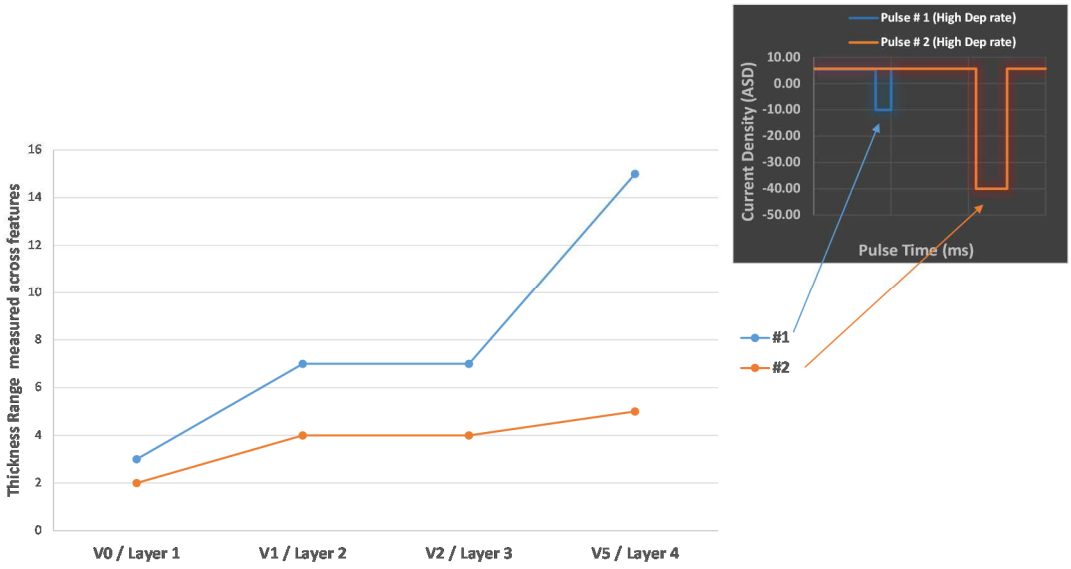

Figure 12.5: Profilometer thickness comparison of all feature regions at different via layers between (#1) and (#2) reverse pulse waveforms

Section 12.4 Microstructure characterization with optimized additive ratio

Microstructure characterization was previously performed (results shown in Chapter # VIII) for 36°C and 48°C bath temperatures with an additive ratio of 0.75 to show grain size morphology evolving with reduced bath temperature. A reverse current density of 10ASD for 2ms duration was utilized to generate the films for such analysis. To perform an identical comparison, the same reverse pulse waveform and magnitude was utilized

for the new parametric conditions that is identified. The additive ratio was modified to 0.26 and bath temperature increased to 40°C to generate the sample. Bulk concentration of the Cu^{2+} ions was maintained at 65g/l. An electro-less copper seed that has a preferred (220) orientation with the thickness measured at $1000A^0$ was utilized as the surface upon which electrodeposited Cu is built. EBSD (Electron back scatter diffraction) analysis was performed to ascertain the difference in grain sizes. The data obtained with EBSD measurements are shown in Figure 12.6. Earlier results obtained with 36°C and 48°C are added here for a comparison. Electron Back-scatter diffraction data confirms that samples electrodeposited with 40°C bath temperature with an additive ratio of 0.26 show intermediate grain sizes compared to those plated at 36°C and 48°C bath temperature with an additive ratio of 0.75. Pole diagrams are shown on the left side of the figure for all test cases. Mostly, the new sample (Leg #1) also shows no preferred orientation but random orientation.

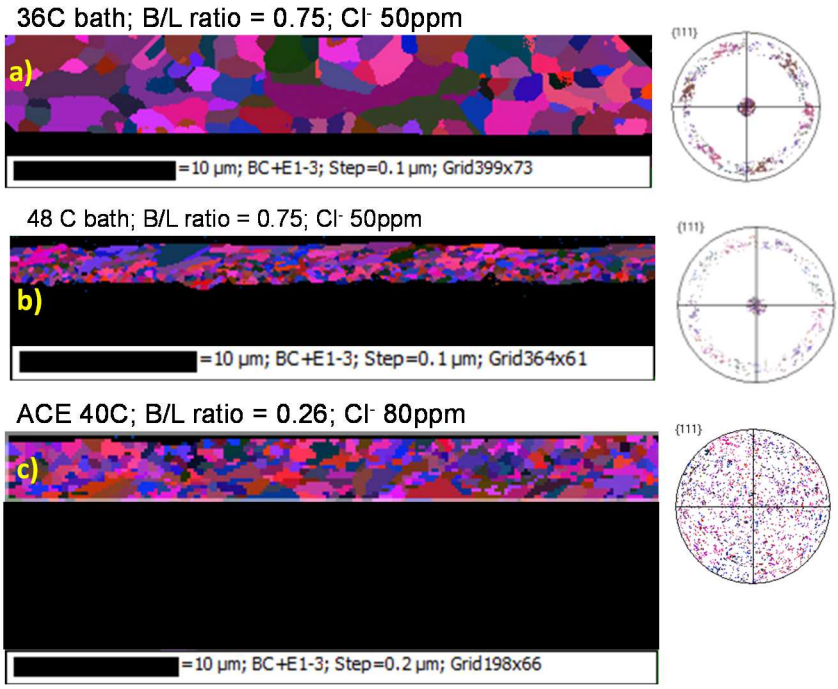

Figure 12.6: EBSD of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C with additive ratio of 0.75, b) 48°C with additive ratio of 0.75, c) Leg 1 with 40°C bath temperature and additive ratio of 0.26

XRD analysis was performed to compare texture and morphology differences for the latest sample generated at the new optimized additive ratio and 40°C bath temperatures, Figure 12.7 shows the summarized data obtained after XRD analysis. PANalytical XPert Pro MRD system with X-ray wavelength CuKα of 1.54nm operating at 45kV currently at LeRoy Eyring Center at Arizona State University was utilized for this measurement. . Earlier results obtained with 36°C and 48°C are added here for a comparison. As shown in Figure 12.7, a strong (111) preferential orientation is observed for 36°C (86%) and a slightly reduced (111) orientation (66%) was observed for 48°C. The leg #1 sample generated at 40°C with the optimized additive ratio of 0.26 shows roughly uniform

presence of all orientations including (111), (200) (220) and (311) with a minor texturing of (111).

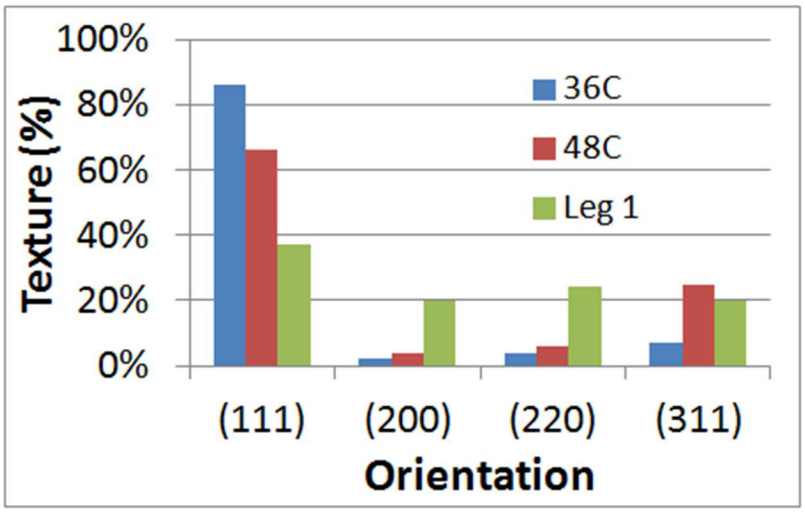

Figure 12.7: Texture of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C with additive ratio of 0.75, b) 48°C with additive ratio of 0.75, c) Leg 1 with 40°C bath temperature and additive ratio of 0.26

Lastly, intrinsic stress values were computed from XRD analysis using the conventional $\sin^2\Psi$ method. [3,4]. Earlier results obtained with 36°C and 48°C are added here for a comparison. The calculated stress numbers are plotted in Figure 12.8.

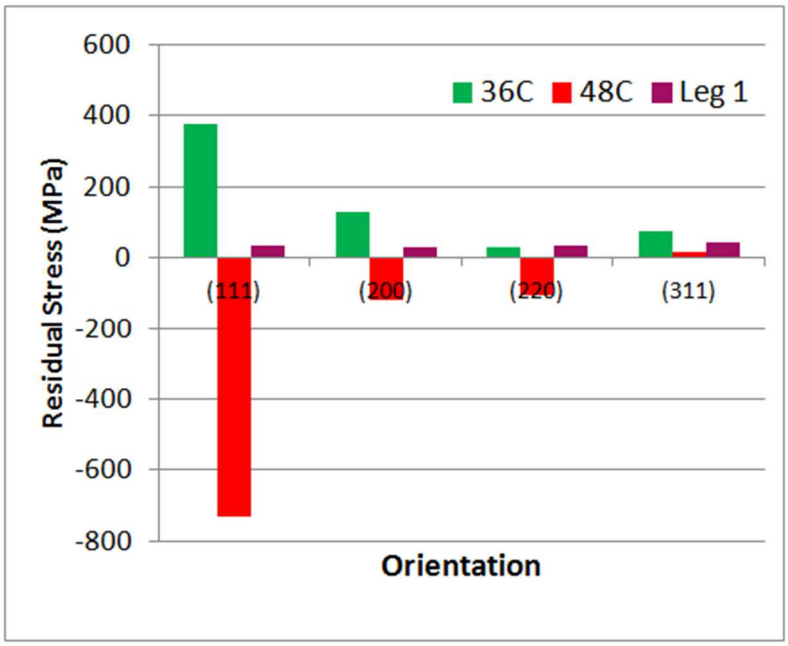

Figure 12.8: Residual stress chart of electrodeposited copper after 180°C bake with 65g/l of bulk Cu^{2+} ion and 10ASD reverse current at a) 36°C with additive ratio of 0.75, b) 48°C with additive ratio of 0.75, c) Leg 1 with 40°C bath temperature and additive ratio of 0.26

Figure 12.8 confirms that samples electrodeposited with 40°C bath temperature with an optimized additive ratio of 0.26, exhibit intermediate stress values compared to those plated at 36°C and 48°C bath temperature. A small tensile stress was observed for all orientation with the new leg 1 condition.

Section 12.5 Summary

Void-free fill across various all via geometries is demonstrated. A low additive ratio of 0.26 continues to show improved gap fill performance across all via geometry. This low additive ratio directly correlates to increased suppression needed in the deposition process to generate differential fill across via top and via bottom. Strong reverse pulse

waveform show momentum plating with fine traces plating thick and the deposit of pad and plane regions plating non-uniformly with a “ski slope” profile. A balanced approach with reduced reverse currents enables both super fill across all via geometries & prevents “pinch off” / key-hole void formation. With such waveforms, momentum plating is arrested and thickness of the multilayer deposit stack is kept uniform. Microstructure evaluation shows random crystal orientations observed with the electrodeposited film with nominal intermediate grain size to those generated at 36°C and 48°C. A low intrinsic stress is also observed at 40°C with the low additive ratio. In this study, a capable reverse pulse methodology is identified to establish uniform copper thickness on large pads (77µm - 200µm) and fine traces (9µm – 50µm). This concludes this dissertation study. In chapter XIII, we summarize all the learnings obtained from this study.

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CHAPTER XIII

CONCLUSION

In summary, manufacturing cost for reliable package continues to trend up. Such high package costs could be offset by focusing our research and development activities on developing critical manufacturing process steps in the make-up of the packages. Furthermore, today's market requirement is driving an increased desire to scale packaging technologies. To enable that, an increase in interconnect density needs to happen. Such capabilities needs to exist without significantly increasing the overall cost of the packages and improve yield. Thus, high density interconnects with IC substrates require development of advanced processing technologies to establish advanced capabilities and minimize the cost of manufacturing. The focus of this work is to reduce cycle time and enabling advanced fill performance and improved deposit quality for electrodeposition of Cu. Traditional approaches for gap fill involved additive based bottom-up fill with reduced deposition rates and long process time to avoid void entrapment and bottom-up fill. In this study, we have demonstrated a capable reverse pulse methodology along with the presence of additives to achieve void-free fill and uniform copper deposit in high density trace regions. Early into the study, significant challenges were encountered for all via geometry that was tested.

For Via0 and Via1 geometry with via depths on the order of ~25 μm, reverse pulse methodology was experimented at very high deposition rate to reduce the overall deposition time. A void-free gap fill process was also established at such high deposition rates. Limitations of diffusion transport process leading to poor throwing power with the

via bottom plating at much lower rate than via top region was identified. The bulk concentration of electrolyte was significantly increased to offset this limitation. With the dilution in concentration gradient minimized, incorporation of reverse pulse current density of 40ASD enabled void-free gap fill for both V0 and V1 geometry. Higher reverse pulse current processes exhibit non-uniform surface deposit. Finely patterned traces show higher thickness while the deposit on pad and plane regions show relatively lower thickness and deposit non-uniformly with a "ski slope" profile. Therefore, reverse pulse current density was optimized to 24ASD from 40ASD to attain void-free fill and enable reasonably uniform pattern plating of fine traces (9µm – 50µm) for such geometries.

2D simulation efforts was used to showcase the mass transfer limitation and the presence of large concentration gradient with Cu^{2+} ion depletion at the via bottom for Via0 geometry. Increase in bulk concentration of Cu^{2+} ion in the electrolyte minimizes the differential gradient seen in Cu^{2+} ion distribution inside the via. We have shown that incorporation of off-time with off time durations longer than the diffusion time are needed for the Cu^{2+} ion to reach the via bottom and enable improved TP and achieve void-free fill. More importantly, this study proves with experimental and simulation efforts that, with the incorporation of reverse pulse methodology, additional Cu^{2+} ions are generated through dissolution of some of the freshly deposited copper and helps to quickly offset for any depletion of the Cu^{2+} ion and enable a differential gradient for fill. The reverse pulse durations are on much smaller time scales than the required off-time to establish similar concentration gradient profile. Validation of the simulation effort with

the 1D simulation effort of West et al[1] exhibits a close match with the simulation predicting the critical TP needed for void-free behavior to be on the order of ~0.6 or higher for Via0 geometry.

Grain size, texture and intrinsic stress analysis of the electrodeposited copper films indicate significant reduction in grain size and variation in intrinsic stress direction from tensile to compressive at higher bath temperature. The copper films has a preferred (111) orientation and nano-indentation studies prove lower hardness at reduced temperature. Such capabilities allow us to tune the deposition flatness / warpage control on the substrate package layers and enable ease of assembly manufacturing and improved package reliability

Early in the study, we found that the application of reverse pulse methodology to enable void-free gap fill on Via0 and Via1 geometry was not adequate for large size via5 geometries due to the presence of fiber protrusions inside the via. Optimization of additive ratio with a 48 leg DOE with six different concentrations of additives with high and low reverse pulse magnitudes and different bath temperatures indicates strong correlation of improved throwing power with reduced concentration of accelerator and increased concentration of leveler species. It was noted that the additive ratio value needs to be small to attain increased throwing power. Void-free fill was generated for V5 with these optimized ratios. These learning's were then extended to Via0 and Via1 geometry to show case a capable gap fill methodology across all via geometries with a single bath composition.

Lastly, a simulation effort with extrapolation of three additive model to the present system indicates similar trend as those observed with experimental studies. Further optimization of the additive concentrations with the present system is unlikely to yield any further improvement in throwing power due to the limitations in surface coverage with PEG only suppression. The result of modeling effort enables us to recommend incorporation of leveling agents such as JGB to improve the TP>1 for these systems.

CHAPTER XIV

FUTURE WORK

Based on the various key learning's established from the study thus far and the fundamental limitation that existed in designing some of the experiment in the existing study we propose the following additional work scope to further optimize the gap fill process for IC substrate applications. We believe extrapolation of such efforts could lead to accommodate deposition process at higher current density and improved TP which in turn leads to shortened process time and increased factory output.

Section 14.0 Future work: Incorporation of leveler as a third additive component

In the present study, incorporation of large reverse pulse magnitudes (>24ASD) could not happen due to the establishment of momentum plating and generation of non-uniform copper deposit with the fine traces plating thicker than the surrounding plane regions. An attenuated reverse waveform was needed to balance the uniformity of the deposit and enable void-free gap fill inside via. We believe the presence of a strong leveling agent in the additive system is likely to offset this behavior. Reid *et al*[1] show that the activity of a charged leveler species can significantly attenuate the surface deposit and prevent a non-uniform deposit (ski sloped, non-uniform plating). Furthermore, his efforts for additive optimization to achieve improved bottom-up fill indicate that increased suppression is needed at via top regions to block the available surface sites for copper reduction reactions. PEG molecules act as surface blocking sites until displaced by the accelerator. In our simulation effort, the addition of a small amount of JGB (Leveler molecule) shows rapid increase in overall suppression and higher throwing power compared to suppression

with PEG molecules only. The role of JGB (leveler) is defined similar to PEG, wherein it blocks sites of Cu reduction but is not affected by SPS activity likely due to the design of the molecular species. Larger molecular weight species are likely to have diffusion limitation and enable differential surface blocking effect, with more coverage at the via top than at the bottom leading to significantly improved TP.

Thus, introduction of a well-designed leveler species for the present applications enables multiple advantages. Foremost, they acts as surface blocking sites similar to PEG and enable uniform pattern deposit. The increased suppression is also likely to enable better TP due to the increased suppression at the via top region. Presence of a strong leveler also enables incorporation of larger reverse pulse current density to establish momentum plating and improved throwing power with the known advantage that the presence of leveler species can attenuate the surface non-uniformity due to momentum plating.

Section 14.1 Future work: Identify the role of Cu^{+} species in IC substrates

Recently Hayashi *et al* [2,4,5] reported that reverse pulse enables differential distribution of Cu^{1+} at the top and bottom of via which in turn enables the via bottom region to plate at a much faster rate than the via top leading to very high throwing power. We had discussed earlier that Cu^{2+} reduction to Cu metal is a two-step process with the formation of Cu^{1+} intermediate. In order to establish a higher throwing power with reverse pulse deposition methodology, Hayashi argues that a differential distribution of Cu^{1+} inside the via region needs to be established. During the application of the reverse pulse waveform which immediately follows a forward pulse deposition step, dissolution of Cu from the metal

surface is likely to happen generating excess Cu^{1+} species rather than Cu^{2+} species. Hayashi *et al*[2,4,5] explains and validates that the concentration of this excess Cu^{1+} generated during reverse pulse is much more at the via bottom than via top. The underlying assumption being that Cu^{1+} generated at the via top has the propensity to easily diffuse away than at the via bottom. Furthermore Cu^{1+} generated at the via top can be easily oxidized with the addition of some oxidizers such as O_2 or by increasing the dissolved oxygen level in the electrolyte solution [2-5]. Cu^{1+} generated at the via top can be easily oxidized back to Cu^{2+} and gets consumed while the Cu^{1+} concentration in the via bottom remains unchanged. This excess generation of Cu^{1+} in the via bottom leads to increased deposition rate at the via bottom than at the via top and enables super fill. In his work, Hayashi's work was primarily focused on gap fill with high aspect ratio via's. We believe these mechanisms can also be extended for via geometries of IC substrate applications and needs to be studied to further improve TP at increased deposition rates.

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APPENDIX A

LIST OF SYMBOLS, ABBREVIATIONS AND ACRONYMS

MPS	3-mercapto-1-propanesulfonate
θ_PEG	Active surface coverage with PEG molecules
Al	Aluminum
m	Amount of mass deposited
ω	Angular rotation rate of the electrode
i_{app}	Applied current density
A_C	Arrhenius constants for the forward reaction
A_r	Arrhenius constants for the Reverse reaction
AFM	Atomic Force Microscopy
A_w	Atomic Weight
BGA	Ball Grid Array
SPS	Bis(sodium sulfopropyl) disulfide
BUF	Bottom-up fill
c_{bulk}	Bulk concentration of Cu_{2+} ions in the electrolyte
Zi	Charge number of the ionic species i
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
Cl^-	Chloride Ion
CTE	Coefficient of Thermal Expansion
$(\partial C_i)/\partial x$ (or) $\blacktriangledown C_i$	Concentration Gradient of species i along x direction
$\frac{\partial c}{\partial n}$	Concentration gradient with n represents the derivative taken normal to boundary
C	Concentration of a given species
c	Concentration of a given species
c_i	Concentration of species i
c_{bulk}	Concentration of species at the bulk
Cu	Copper
Cu_{ad}	Copper adsorbate
CuCl	Copper Chloride
CCL	Copper Clad Film
$CuSO_4.5H_2O$	Copper sulfate pentahydrate
CE	Counter electrode

Cu^{2+}	Cupric ion
Cu^{+}	Cuprous ion
I	Current
i	Current density
i_B (or) i_{bottom}	Current density at via bottom
i_T (or) i_{top}	Current density at via top
CEAC mechanism	Curvature enhanced accelerator coverage
CV	Cyclic Voltammetry
DI	Deionized Water
h	Depth of the via
D_i	Diffusion coefficient of species i
	Diffusion length
t_D	Diffusion time
DC	Direct Current
"d"	Double layer thickness
DFR	Dry Photoresist Film
θ_eff	Effective coverage with additives
EM	Electromigration
e^-	Electron
EBSD	Electron back scattered diffraction
Ø	Electrostatic potential
k^0	Equilibrium Reaction rate constant
E_{rest}	Equilibrium Rest Potential
I_0	Exchange current
i_0	Exchange current density
Expt #	Experiment #
exp	Exponential function
F	Faradays constant
Fe^{3+}	Ferric ion
FLS	Fine Lines and Spaces
ν	Fluid velocity
J_i	Flux of species i
i_{FWD} or i_{dep}	Forward current density during pulse
T_{FWD} or T_{dep}	Forward pulse time duration
FTIR	Fourier transform infrared spectroscopy

GC	Glass Cloth
HV	Hardness
HAST	Highly accelerated stress testing
HCl	Hydrochloric acid
R	Ideal Gas constant
IHP	Inner Helmholtz Plane
I/O Signals	Input / Output signals
IC	Integrated circuit
κ	Ionic conductivity, Solution conductivity
JGB	Janus Green B
JEDEC	Joint Electron Device Engineering Council
k	Kinetic constant for Cu deposition
LGA	Land Grid Array
l	Length of the non-planar surface or Via depth
LASER	Light Amplification by Stimulated Emission of Radiation
i_L	Limiting diffusion current density or Levich current density
LSV	Linear sweep voltammetry
LPM	Liters Per Minute
ln	Logarithmic factor
log	Logarithmic factor
$h_{avg}(t)$	Mean thickness deposited in the feature at given time t
N_i	Molar flux of the species i
n	No of electrons
OCP	Open Circuit Potential
OHP	Outer Helmholtz Plane
η	Overpotential
Z - Height	Package Height
PPM	Parts Per Million
Pe	Peclet Number
PVD	Physical vapor deposition
PGA	Pin Grid Array

PEG	Polyethylene glycol
PEI	Polyethyleneimine
PPG	Polypropylene glycol
PVP	Polyvinyl pyrrolidone
PCB	Printed Circuit Board
PWB	Printed wiring board
H^+	Protons
i_{AVG}	Pulse average current density accounting for the forward and reverse condition
i_{total}	Pulse deposition current density
T_{off}	Pulse deposition off time duration
k_c	Rate constant of the forward reaction (Cathodic)
k_r	Rate constant of the reverse reaction (Anodic)
RE	Reference electrode
RC Delay	Resistive Capacitive Delay
i_{REV} or i_{diss}	Reverse current density during pulse
RP	Reverse Pulse
T_{REV} or T_{diss}	Reverse pulse time duration
RDE	Rotating disc electrode
R_a	Roughness (average)
SEM	Scanning Electron Microscope
SAP	Semi-additive process
E^0	Standard electrode potential
ΔG^0	Standard free energy of reaction
SHE	Standard Hydrogen Electrode
R-SH	Sulfonate functional group
H_2SO_4	Sulfuric acid
SMT	Surface Mount Technology
α	Symmetry factor between cathodic and anodic reaction
T	Temperature
$R\text{-}SO_3$	Thiolate functional group
3D	Three dimensional

TSV	Through silicon via
TP	Throwing Power
t	Time
T_{total}	Total deposition time duration
t_i	Transference number
2D	Two dimensional
ASD	Units of Current density, Ampere per Square Decimeter
ϑ	Kinematic Viscosity
v_i	Velocity of species i
VCP	Vertical Continuous Plater
L	Via depth
VR	Via Recess
V0	Via0
V1	Via1
V2	Via2
V5	Via5
VMS	Virgin makeup solution
Wa	Wagner number
WE	Working electrode
XRD	X-ray Diffraction
XPS	X-ray photoelectron spectroscopy

APPENDIX B

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APPENDIX C

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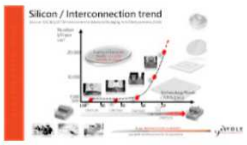

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