Small Form Factor Hybrid CMOS/GaN Buck Converters for 10W Point of Load Applications

by

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ABSTRACT

Point of Load (PoL) converters are important components to the power distribution system in computer power supplies as well as automotive, space, nuclear, and medical electronics. These converters often require high output current capability, low form factor, and high conversion ratios (step-down) without sacrificing converter efficiency. This work presents hybrid silicon/gallium nitride (CMOS/GaN) power converter architectures as a solution for high-current, small form-factor PoL converters. The presented topologies use discrete GaN power devices and CMOS integrated drivers and controller loop. The presented power converters operate in the tens of MHz range to reduce the form factor by reducing the size of the off-chip passive inductor and capacitor. Higher conversion ratio is achieved through a fast control loop and the use of GaN power devices that exhibit low parasitic gate capacitance and minimize pulse swallowing.

This work compares three discrete buck power converter architectures: single-stage, multi-phase with 2 phases, and stacked-interleaved, using components-off-the-shelf (COTS). Each of the implemented power converters achieves over 80% peak efficiency with switching speeds up-to 10MHz for high conversion ratio from 24V input to 5V output and maximum load current of 10A. The performance of the three architectures is compared in open loop and closed loop configurations with respect to efficiency, output voltage ripple, and power stage form factor.

Additionally, this work presents an integrated CMOS gate driver solution in CMOS 0.35um technology. The CMOS integrated circuit (IC) includes the gate driver and the closed loop controller for directly driving a single-stage GaN architecture. The designed

IC efficiently drives the GaN devices up to 20MHz switching speeds. The presented controller technique uses voltage mode control with an innovative cascode driver architecture to allow a 3.3V CMOS devices to effectively drive GaN devices that require 5V gate signal swing. Furthermore, the designed power converter is expected to operate under 400MRad of total dose, thus enabling its use in high-radiation environments for the large hadron collider at CERN and nuclear facilities.

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1 INTRODUCTION

1.1 Motivation

Recent advancements in power converter applications such as automotive point-of-load converters (PoL), space power management, and wireless and computational electronics demand buck converters with high load currents and large step-down conversion ratios. Unfortunately, integrated solutions do not exist to support the high load current, and these power converters have historically used high power silicon-based devices operating at ≤200 kHz switching frequencies [1], which have large physical output filters and exhibit low efficiencies. There is a need for low form factor and medium power (10 to 15W) converters for such applications.

There are many design challenges associated with developing PoL converters with large load current requirements and high conversion ratios in a small form-factor. Figure 1 indicate the studies from the IHS Markit Technology indicate that the GaN device has huge potential in various applications with the demand expected to increase US$1 billion mark in the next 5 years [2]. Figure 2 indicates the trade-off of several factors such as power dissipation losses, cost, weight, volume and Mean Time Between Failures (MTBF) in the design of state-of-art PoL converters [3]. A typical power management system utilizes a switched mode power supply (SMPS), which can be a buck, boost, buck-boost regulator or any other variant of a DC-DC converter. In the above applications, the commonly used SMPS is a step-down type converter [4], which converts a higher voltage to a lower regulated voltage. The buck consists of a high side transistor connected to either a low side transistor or free-wheeling diode. This work presents hybrid CMOS/GaN buck power

converter architectures as a solution for high current, small form-factor PoL converters. While the developed converters in this research target high radiation environments, the developed techniques could be used for other medium-power applications.

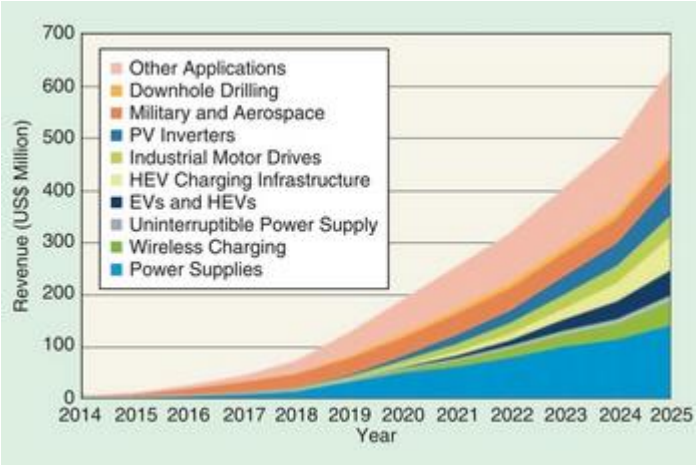

Figure 1: Market Study by Research Firm IHS Markit Technology for the GaN Sales Revenues [1]

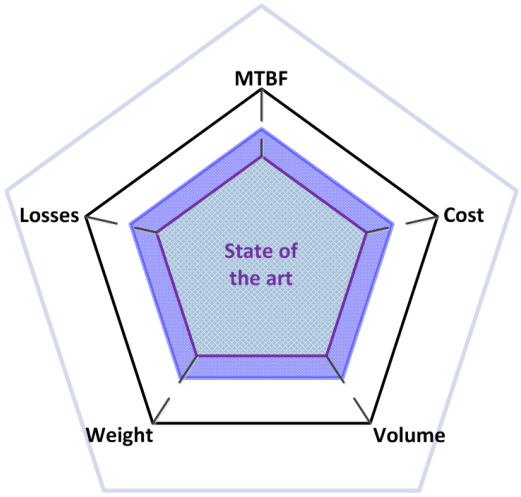

Figure 2: PoL Converters Design Trends Based on Contributing Factors

The enabling technology for realizing high-efficiency, high current density (>5A), power stages for supporting the proposed work is gallium nitride (GaN) [5]. The DC-DC converter architecture proposed in this research is implemented in GaN-on-silicon (GaN-on-Si) and paired with a high-voltage radiation-hardened CMOS chip packaged in a single unit. The intent of this work is to use an existing enhancement-mode eGaN-on-Si FET

process. The chosen EPC GaN process/devices are an established production process, with published total dose reliability numbers [6]. GaN material is most commonly used for fabrication of large power transistors for: 1) military communications requiring low-noise amplifiers and high-frequency linear power amplifiers, and 2) discrete devices for power management circuits in high-power electronic systems [6, 7] Presently, GaN is an expensive process, but with an increasing number of foundries entering the marketplace and the development of GaN-on-Silicon, industry sees an avenue towards decreasing costs. GaN technology offers high maximum current handling capability, high breakdown voltage devices, and high frequencies of operation (e.g. +1 GHz switching). These characteristics make GaN advantageous for power supply circuits. With respect to switching devices, GaN is the only technology offering both high power density and high switching speeds [5]. Compared to silicon substrates, GaN has factor of 2x lower on-resistance than silicon (Si)-devices for same device size and provides up to 100 times the power density [6]. Figure 3 and Figure 4 shows some of the major advantages of GaN devices compared to existing technology. This approach combines the compactness, high voltage capability, large output current capability, wide operation temperature, and high radiation hardness of the GaN material with the radiation hardness and medium voltage capability of CMOS based drivers to obtain a truly innovative converter that is optimal for high radiation environments. Additionally, these GaN devices offer advantages in terms of higher operating temperature range, increased current (power) capability per mm of device size, and low Ciss and Coss loss (input and output capacitance respectively, which restrict the usable frequency and switching speed when a FET is used for switching applications), thereby providing high switching frequency capability [5]. The comparison of different

devices of enhancement, depletion mode GaN with the Si Power MOSFET [8, 9, 10] indicates the advantage which GaN possess in terms of on resistance, input and output capacitance, thermal resistance and package size.

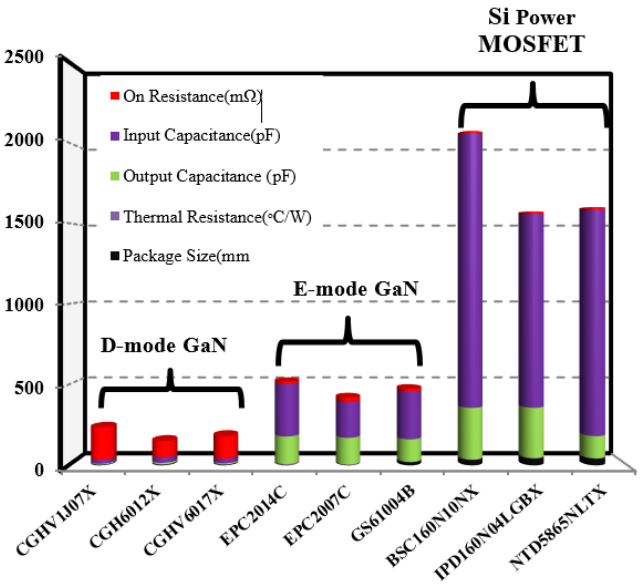

Figure 3: Comparison of Depletion Mode, Enhancement Mode GaN with Si Power MOSFET Devices

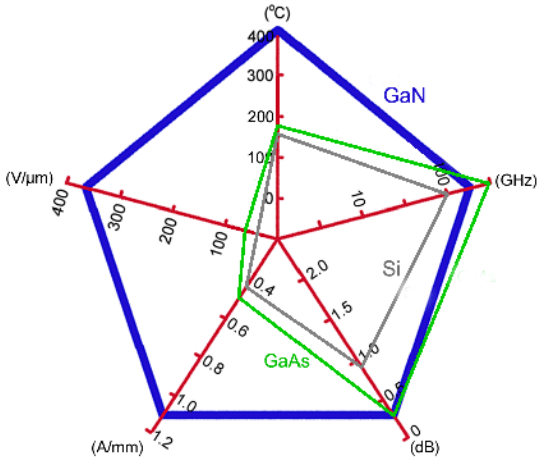

Figure 4: Key Characteristics of GaN Compared to GaAs and SiC [11]

1.2 Objectives and Challenges

The presented topologies use discrete GaN power devices and CMOS integrated drivers and controller loop. The presented power converters operate in the tens of MHz range to

reduce the form factor by reducing the size of the passive inductor and capacitor. Higher conversion ratio is achieved through design of a fast control loop, and the use of GaN power devices that exhibit low parasitic gate capacitance and minimize pulse swallowing.

This research addresses key challenges with designing radiation-hardened, small form-factor power converters, including: performance variation with radiation, maintinaing high efficiency at high switching speeds, minimization of ringing at critical nodes with high switching frequency to improve electromagnetic compatibility, design innovation to use low voltage-rated devices to drive the high voltage GaN, high gate drive current capability, design for high-radiation environments, efficient PCB design for high frequency applications, and thermal management of power dissipation at heavy loading conditions. This work has application in the field of voltage trackers and calorimeters for the large hadron collider. The objectives for this research are summarized as:

1. Design and test discrete power converter architectures using (COTS).
2. Develop a radiation robust CMOS gate driver and controller integrated circuit (IC) to drive and regulate a single stage buck converter.

Table 1 summarizes the key converter design specifications for the discrete and radiation-robust integrated converter module. This table acts as the requirements for the design and simulation of the DC-DC converter for this research.

Table 1: DC-DC Converter Design Specifications

Parameter	Design Target (Discrete)	Design Target (Hybrid)	Unit
Input voltage	24	18	V
Output voltage	5.0	5.0	V
Output voltage ripple	10	10	%
Typical load current	5	5	A
Maximum load Current	7	10	A
Converter efficiency	~80	>80	%

Converter frequency	2-10	10-20	MHz
Ambient temperature range	-40 to 125	-55 to 125	ºC
TID tolerance	N/A	400M	rad
Mean Time to Failure	N/A	4e7 @ 125 ºC	hours
Physical dimensions	4 x 4 x 1	2 x 2 x 1	mm

1.3 Prior Work

Prior work in this field has primarily focused on: high switching frequency using depletion mode GaN in open-loop converter operation, high frequency but low current monolithic converters [13], multi-phase integrated approaches to increase the load current capability [14], lower conversion ratio converters with the input and output voltage close to each other [14, 15], and lower output current capability [16]. The other commonly used approach for such power converter applications is to use a transformer solution, which increases the form factor of the converter and is not generally desirable for PoL applications. Table 2 compares one state of the art power converter that is most closely related to the proposed design solution. The proposed power converter has significant advantages when compared with current state-of-the-art DC-DC converters.

Table 2: Comparison of the Proposed Work with the State-of-art Power Converter

Parameters	**FEAST_MP[12]**	**This Work**
Input voltage	5-12V	18-24V
Switching frequency	2 – 4 MHz	~20MHz
Typical load current	<4A	~10A
Converter efficiency	~70 %	~80%
Physical dimensions	38mm x 17mm x 8mm	20mm x 15mm x 4mm

State of the art design and performance trends for discretely implemented buck converters follows the performance trends shown in Figure 5. The higher switching frequency provides smaller discrete device sizes. The general trend is reduced load current capability and reduced efficiency for increases in switching frequency.

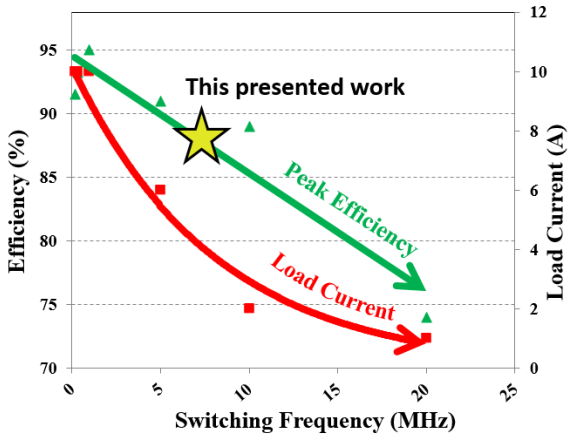

Figure 5: Design Trends for the Discrete Implementation of Buck Converters

The design trend for the fully-integrated buck converters shows that the load current is limited for high switching frequency applications, as illustrated in Figure 6. The fully integrated buck converters include the power FETs within the IC, which has increased power dissipation and size limitations at high load currents. This is the limiting factor for the load current (<1A). The switching frequency for the converter can achieve higher (100's of MHz) speeds than discrete solutions because there is low parasitic inductance between the inter-connections within the IC. This work employs a hybrid CMOS/GaN architecture to increase the load current to 10A at 20MHz switching frequency.

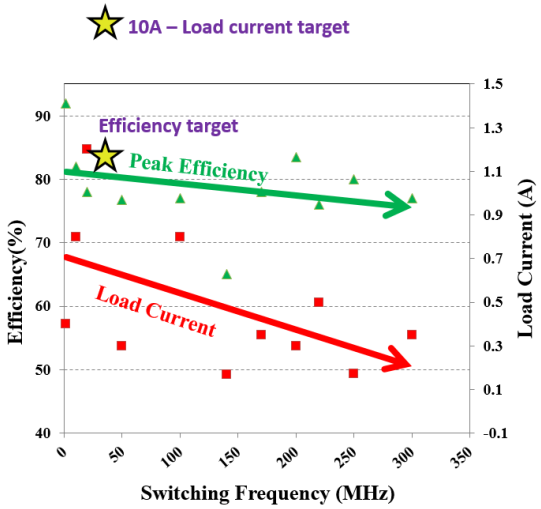

Figure 6: Design Trends for the Integrated Buck Converters

Furthermore, the conversion ratios in prior work indicates that the efficiency is low at reduced duty cycle operation [19]. Moreover, fully-integrated silicon solutions have conversion ratios higher than 30% and typically operate for sub-5V input and output voltages [16]. A goal of this work is to maintain high efficiency at low duty cycle operation (~20%) and allow for high conversion ratios.

1.4 Proposed Solution

This work compares three discrete buck power converter architectures: single-stage [12], multi-phase with 2 phases [17], and stacked-interleaved [16], using components-off-the-shelf (COTS). Each of the implemented power converters achieves over 80% peak efficiency, and switching speeds up-to 10MHz for high conversion ratio from 24V input to 5V output and maximum load current of 10A. The performance of the three architectures is compared in open loop [20] and closed loop configurations with respect to efficiency, output voltage ripple, and power stage form factor.

Additionally, this work presents an integrated CMOS gate driver solution in CMOS 0.35um technology. The CMOS integrated circuit (IC) includes the gate driver and the closed loop controller for directly driving a single-stage GaN architecture. The designed IC is expected to efficiently drive the GaN devices up to 20MHz switching speeds. The presented controller technique uses voltage mode control with an innovative cascode driver architecture to allow a 3.3V CMOS device to effectively drive GaN devices that require 5V gate signal swing. Furthermore, the designed power converter is expected to operate under 400MRad of total dose, thus enabling its use in high-radiation environments.

1.5 Thesis Organization

This thesis details the design and implementation of both discrete and integrated solutions for buck converters. The thesis is organized in 5 chapters. Chapter 1 gives a brief introduction of the motivation and the proposed solution. Chapter 2 details the overview of three power converter architectures as discrete solutions. Chapter 3 discusses the implementation of the board-level power converters. Chapter 4 presents the integrated power converter solution using a CMOS controller and driver. Chapter 5 summarizes the measurement characterization of the system as a whole, various circuit blocks within the system, and the fabricated CMOS IC results. Finally, the conclusion and the future scope of this work is highlighted in Chapter 6.

2 BUCK CONVERTER ARCHITECTURES

2.1 Overview

This section presents three discrete high efficiency power converter architectures, as shown in Figure 7, operating at high switching frequency (1MHz – 10MHz) with high step-down conversion ratio (24V to 1.5V/5V). The three architectures include: a single-stage buck, a multi-phase buck with 2 phases, and a stacked interleaved configuration, which are compared in open loop and closed loop configurations.

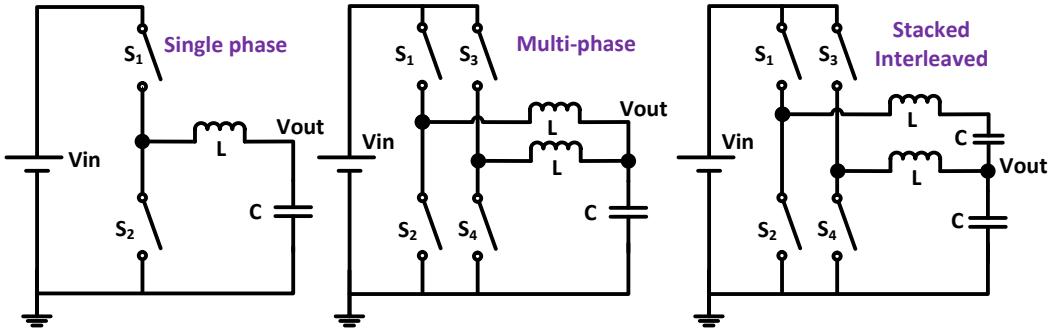

Figure 7: Overview of Discrete Converter Architectures

2.2 Single Stage Architecture

The implemented single-stage synchronous buck converter architecture is illustrated in Figure 8 [14]. Within the single stage architecture, the two GaN devices operate complementary to each other, with some dead time between their on and off cycles to prevent shoot-through. The dead time control is provided by the non-overlapping dead time circuit. The switching waveform's duty-ratio ("on" time within a switching period) is used to regulate the output voltage. A single channel of the multi-phase CMOS controller (ISL6558) [19] is used to control the power stage for this architecture. This controller regulates the converter's output voltage by providing a pulse width modulated (PWM) control signal with duty cycle of D. This signal is generated by comparing the feedback

voltage with the converter's reference voltage. The PWM signal is converted to two complementary signals with duty cycle D and (1-D) and fed to the silicon gate driver (LM5113) [20]. The external bootstrap circuit provides flexibility for high frequency operation of the silicon gate driver by minimizing the bootstrap power loss. A Type-3 [23]external compensation circuit is used for the closed loop stability. The converter's time domain characteristics are shown in Figure 9 [4]. The gate signals S_1 and S_2 are complementary to each other with some dead time (3-5ns) between them. This dead time (t_{dead_time}) between each device's on and off cycle prevents shoot-through current. The controller is designed for continuous conduction mode (CCM), as constant switching frequency is required for good EMI performance. The limitations of this architecture are limited output current handling capability, thermal management, and low duty cycle operation that may lead to pulse swallowing.

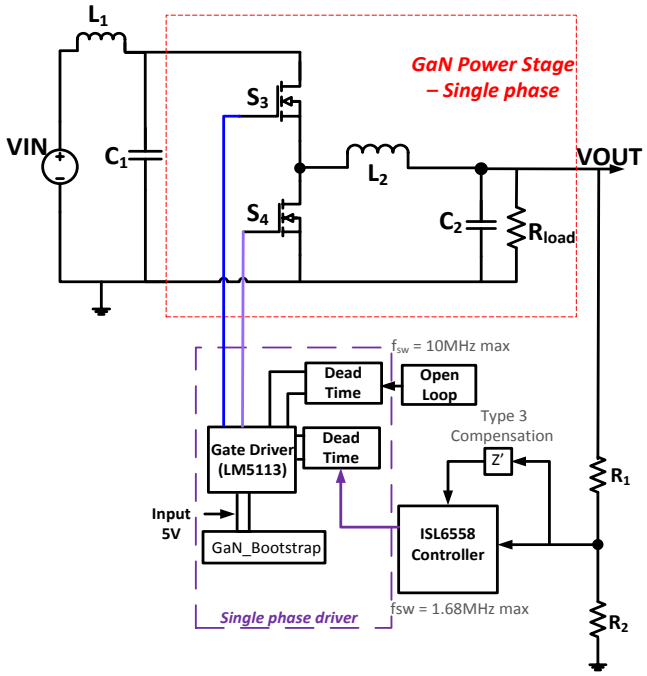

Figure 8: Schematic Diagram Illustrating the Single Stage Prototype Power Converter using COTS

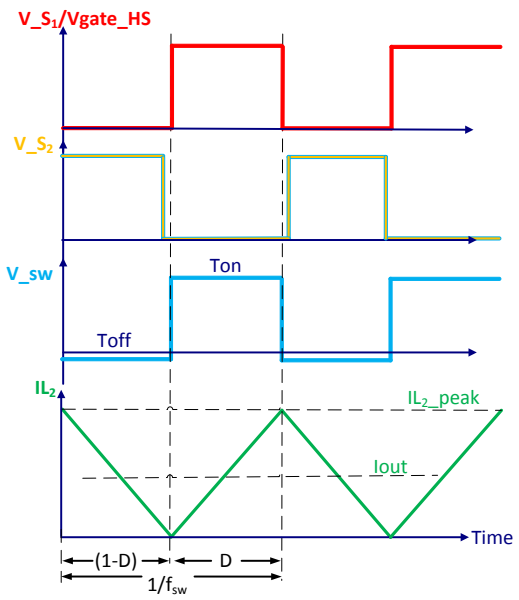

Figure 9: Timing Diagram of the Single Stage Buck Architecture

For the single-phase converter, the conduction loss is directly proportional to duty cycle of operation (D), drain to source resistance (R_{DSon}), and square of the load current (I_{Load}). This indicates that higher R_{DSon} and heavy loading conditions increase conduction loss [4] [27].

$$P_{cond} = D \times R_{DSon} \times I_{Load}^2 \quad (1)$$

The GaN device switching losses with the inductive or resistive load are a function of the output parameters of the device, the rise (t_{rise}) and fall (t_{fall}) time of the gate signals, and the device's switching frequency (f_{sw}). These losses have been derived as follows:

$$P_{sw\_L} = (V_{out} \times I_{LOAD} \times (t_{rise}+t_{fall}) \times f_{sw}) + (V_{out}^2 \times C_{oss} \times f_{sw})/2 \quad (2)$$

$$P_{sw\_R} = (V_{out} \times I_{LOAD} \times (t_{rise}+t_{fall}) \times f_{sw}) + (V_{out}^2 \times C_{oss} \times f_{sw})/6 \quad (3)$$

Switching losses are decreased with smaller device capacitance (C_{oss}), lower f_{sw}, and faster gate signal rise/fall times. The freewheeling diode loss (PFWD) is directly proportional to the forward voltage drop of the freewheeling diode (V_D), which occurs

during the dead time operation (t_{dead_time}) in a synchronous converter and is therefore small [4].

$$P_{FWD} = t_{dead\_time} \times V_D \times I_{LOAD} \quad (4)$$

The inductor's conduction loss is a function of DC resistance of inductor, R_{L_DCR}, and I_{LOAD}. This can be minimized by choosing an inductor with low DC resistance [4].

$$P_{ind} = R_{L\_DCR} \times I_{LOAD}^2 \quad (5)$$

The total power dissipation is the summation of the above values and is given as [4]:

$$P_{Total} = P_{cond} + P_{sw\_R/L} + P_{FWD} + P_{ind} \quad (6)$$

As the converter's switching speed increases, the device's switching loss increases, but since GaN has substantially lower C_{OSS} than silicon, power dissipation still remains low compared to conduction loss for frequencies below ~10 MHz. Additionally, high switching speed reduces the output filter size requirements, thereby reducing the R_{L_DCR} and decreasing inductor power loss. This analysis supports the use of GaN for high-speed medium-power converters.

The bootstrap technique employed in the single-phase converter architecture uses a GaN device instead of the traditional bootstrap diode to minimize the reverse recovery loss [28]. The additional Zener diode provides voltage clamping within the absolute maximum ratings for the gate to source voltage of the GaN power device. The bootstrap GaN turns on the instant the low side power GaN device is on to enable the bootstrap voltage, V_{boot}, to charge to the supply (V_{cc}) level, as illustrated in Figure 10. The GaN (EPC8004) [30] being a low reverse recovery device has advantages for reduced losses at high frequency operation and ringing at the V_{boot} node. When the low side is off, the body diode of EPC8004 acts as a blocking diode with V_{boot} voltage going up-to VIN+V_{cc} level.

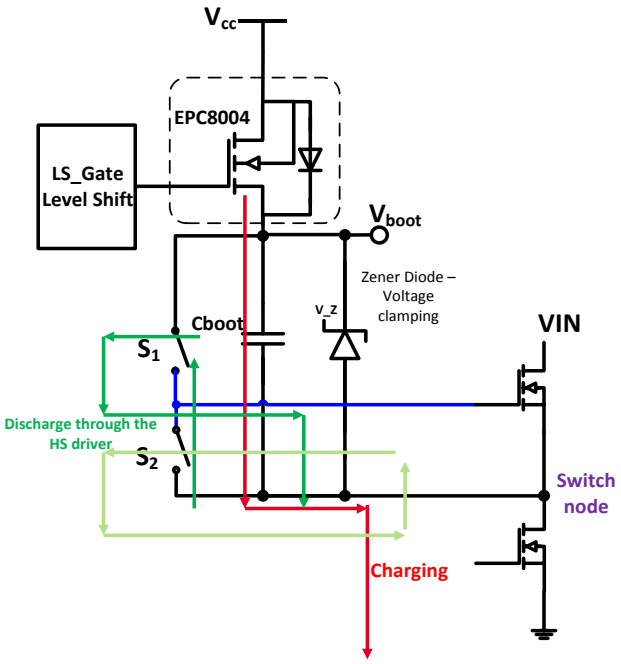

Figure 10: GaN Bootstrap Architecture

2.3 Multi-phase Architecture

The presented multi-phase power stage configuration with a two-phase implementation is given in Figure. 11. It has the advantage of current sharing between multiple phases [9], where each phase is realized using a separate switching branch. The current sharing allows for increased output current handling capability for the same active device size when compared to the single-stage architecture [18, 27, 43]. Reduction in current through each phase reduces the power dissipation in the devices based on equations (1) through (6). The multiphase converter consists of multiple buck stages connected in parallel with out-phased input switching signals. The gate synchronization, results in partial cancellation of ripple at 50% duty cycle for 2-phase architecture; 25%, 50% and 75% duty cycles for a 4- phase; and increasing number of duty cycles for higher number of phases [18]. The gate drive controller must provide accurate load balancing between the multiple phases [15].

At 50% duty cycle, the two inductor currents, IL_2 and IL_3, are complimentary in nature, as shown in the time domain waveforms of Figure 12, and ripple cancellation occurs at the output to provide accurate regulation of the output voltage [18]. Since the ripple is close to zero, the system power loss due to ripple is also minimized.

In the implemented design, the two phases are synchronized with the multi-phase CMOS controller (ISL6558), and the output with 180º phase shift is fed to two separate channels, each with an individual dead time circuit and gate driver to control the high-side and low-side GaN transistors of the multi-phase power stage. The bootstrap diode loss is minimized to increase the power stage efficiency by bypassing the internal bootstrap diode of the CMOS driver with an external low reverse recovery Schottky diode (D_Boot_EXT of Figure 11).

The main disadvantage of multi-phase converters has traditionally been the high component count and area requirements when using silicon-based MOSFETs [18]. The multi-phase solution is more amenable when using GaN devices, as the effective form factor of multiple GaN devices is lower than a single power MOSFET. However, multiple output inductors still consume significant area, even though the required size of each inductor is lower due to the high effective switching frequency of the multi-phase when compared with the single-stage topology. It is therefore advantageous to use a multi-phase power stage in high current applications [7]. For applications with widely varying duty cycles (e.g. large changes in input voltage), the multi-phase architecture is not the best approach due to its lack of ability to cancel output voltage (V_{out}) ripple at all duty cycles. For these applications, a stacked interleaved architecture is a better suited topology.

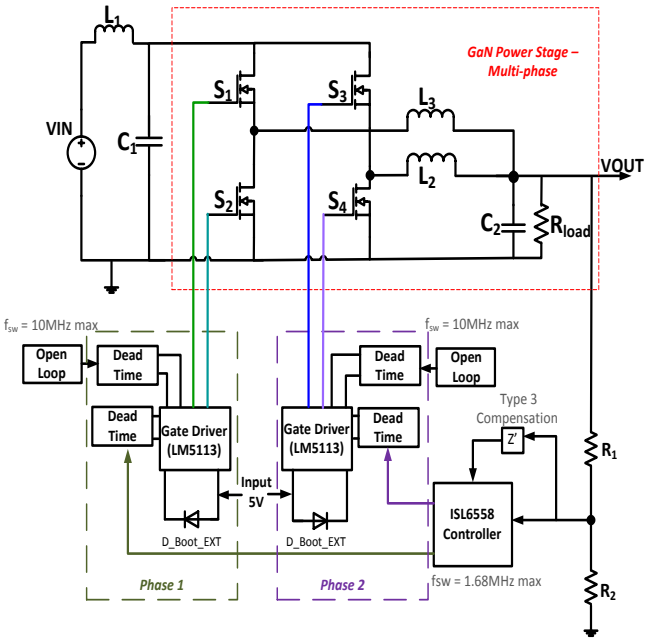

Figure 11: Schematic Diagram Illustrating the Multi-phase Prototype Power Converter

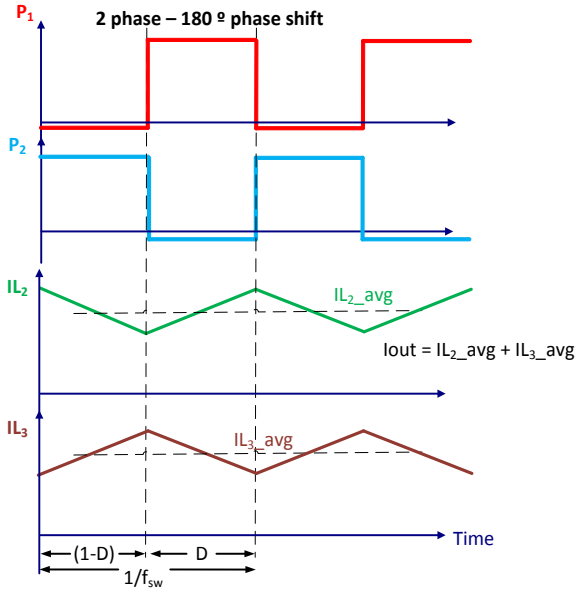

Figure 12: Timing Diagram of the Multi-phase Power Stage

2.4 Stacked Interleaved Architecture

The stacked interleaved power stage architecture is illustrated in Figure 13. The converter has two phases, which are out-of-phase in operation (e.g. phase 2 operates with

duty cycle D and phase 1 operates with duty cycle of (1-D)). The result is that the secondary phase (Phase 2) current ripple is out of phase with the primary phase (Phase 1) current ripple, as shown in the timing diagram of Figure 14. The inductor current ripple (ΔI_L) is therefore canceled at the output voltage node. The capacitor C_2' (10µF) acts as blocking capacitor for the current ripple, and it is connected between the output inductors (L_2 and L_3) of the two phases for ripple cancellation [16]. Unlike the multi-phase architecture, the primary phase provides the majority of the load current to the output load, and the secondary phase is only used to cancel current ripple. Therefore, the primary phase path handles the high current requirements, whereas the secondary phase has much lower current handling requirements because the current ripple is normally a small percentage of the average load current.

The stacked interleaved structure has the advantage of duty cycle independent ripple cancellation, unlike the multi-phase configuration [15]. Cancellation of the output ripple provides faster transient response and lower undershoot/overshoot of the output voltage, which enables reduction in output inductor size.

Lower inductance value typically correlates to lower inductor resistance (R_{L_DCR}), thereby allowing for higher output load currents for the same output inductor conduction losses (P_{ind}) compared to the multi-phase configuration. This architecture is therefore advantageous in applications requiring stringent load regulation. But, the stacked interleaved architecture has the following disadvantages compared to a single-stage: 1) the size of the power stage is larger with two inductors and four GaN devices, and 2) the

switching signals must be synchronized with multiple gate drivers, hence increasing controller complexity.

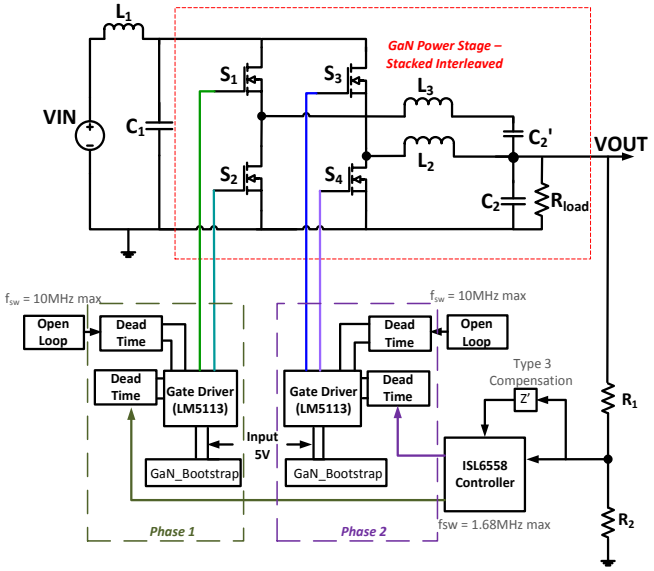

Figure 13: Schematic Diagram Illustrating the Stacked Interleaved Prototype Power Converter using COTS

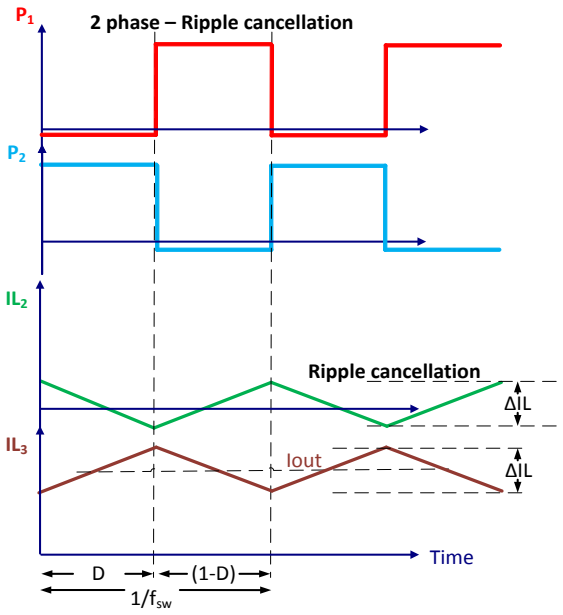

Figure 14: Timing Diagram of the Stacked Interleaved Power Stage

Table 3 provides the qualitative comparison of the different power converter architectures. This table acts as a comparative tool to enable easy selection of a power converter architecture based on a specific application's requirements.

Table 3: Qualitative Comparison of Power Converter Architectures

Parameter	Stacked Interleaved	Single-phase	Multi-phase
Switching frequency	Medium	Low	High
Load current	Low	Low	High
Efficiency at high load current	Low	Low	High
Output voltage ripple	Low	High	Medium
Design Complexity	High	Medium	High

3 DESIGN IMPLEMENTATION OF BUCK CONVERTER ARCHITECTURES

3.1 Overview

The three designed buck converters are compared with respect to efficiency, output voltage ripple, and power stage form factor. The presented designs use external bootstraps, board layout optimization, and efficient architectural techniques to push the driver and power stage performance beyond the manufacturer specified limits and meet performance requirements using COTS. The intent for implementing three power converter architectures is to provide various options for different applications. This study also provides a performance comparison among the architectures for high switching frequency GaN implementations. The challenges [5] in the design of high frequency and high efficiency discrete implementation of the 10W output power converters are: 1) Bootstrap losses of the high-side driver, 2) Low on-resistance of the gate driver, 3) Low duty cycle of operation with fast rise and fall time 4) Low propagation delay of the controller loop, and 5) Design and layout of the board with consideration to routing parasitics.

3.2 Architecture Implementations on Board

The discrete power converter board dimension that includes the three architectures is 140mm x 100mm x 5mm. The GaN-based power stage (S_1 and S_2) is implemented as one of three architectures using Efficient Power Conversion (EPC2014C) devices. This device was chosen for its optimized on-resistance versus capacitance to allow for up to 50MHz switching frequency (f_{sw}) with 7.3A output current and 40V drain-to-source voltage limit. The crossover frequency for which this device has equal switching and conduction loss at a 7.3A converter output current is around 20-30MHz. The maximum switching frequency on

the power converter board is limited by the bootstrap circuit losses and the driver push-pull stage. An air core inductor of 500nH with capacitor of 110µF (ceramic) are used for the input filter, and air core inductor of 111nH with capacitor of 22µF (ceramic) are used for the output filter. In order to suppress transient ringing at the converter's output switching node and ensure that it does not exceed 40V, an RC snubber is used with 2Ω resistance value and fine-tuned capacitance from 100pF to 1nF. Capacitors of around 100pF are also connected from the switching node to GND to reduce switch node ringing. Figure 15 highlights the circuit diagram of the power stage for each of the architectures with the GaN FET and the snubber configuration. This is a general schematic for the power stage [39], which is employed in each of the converter architectures.

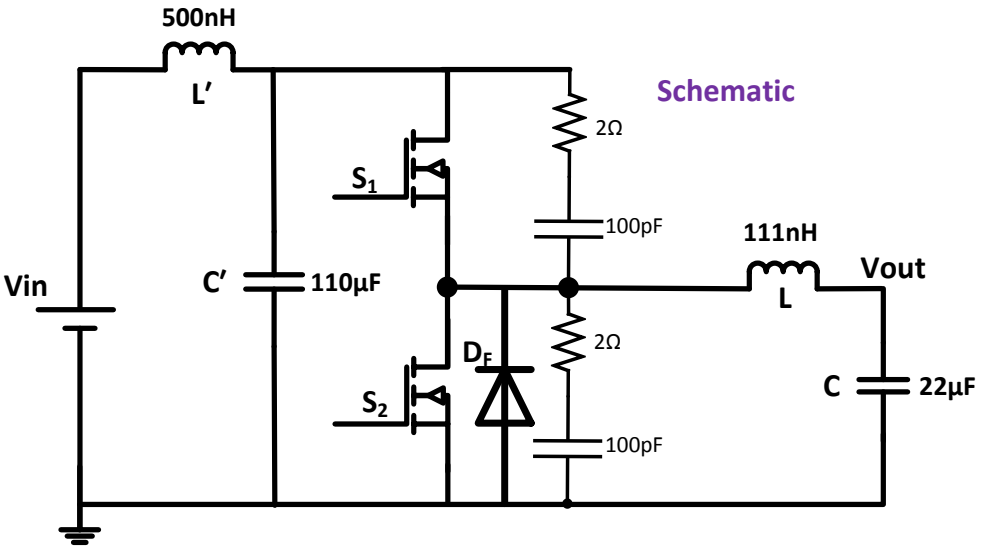

Figure 15: General Schematic of the Power Stage Showing the Configuration and Snubber

The duty cycle control and the output voltage regulation is performed using a fast accurate controller COTS product with differential output sensing, which is designated by the "ISL6558CBZA Controller" block in the feedback loop. The developed power converter system requires a fast load transient response with a precision internal reference to offer

±0.67% output regulation and the ability to correct for up to ±500mV variations in the output terminals due to line losses. Additionally, the controller must support the 10MHz switching frequency range. The COTS part ISL6558CBZA is chosen for the presented proof-of-concept, with the limitation of this controller being that the maximum operating frequency is 1.70MHz [12]. On-board Type-3 compensation is used for the error amplifier within the controller. A simple RC dead-time circuit is used to provide the minimum dead time required for switching operation at 1.70MHz. Two improved dead-time circuits discrete implementation are used, one with an integrated circuit approach, i.e. discrete non-overlapping clock generator with the feedback loop and the other as series cascaded delay elements as shown in Figure 16. The dead time circuit from Figure 16 a) is used for multi-phase architecture and the circuit from Figure 16 b) is used for the evaluation of the single phase and stacked interleaved architecture. Different dead time circuits are explored to provide flexibility in design and evaluation of power converters.

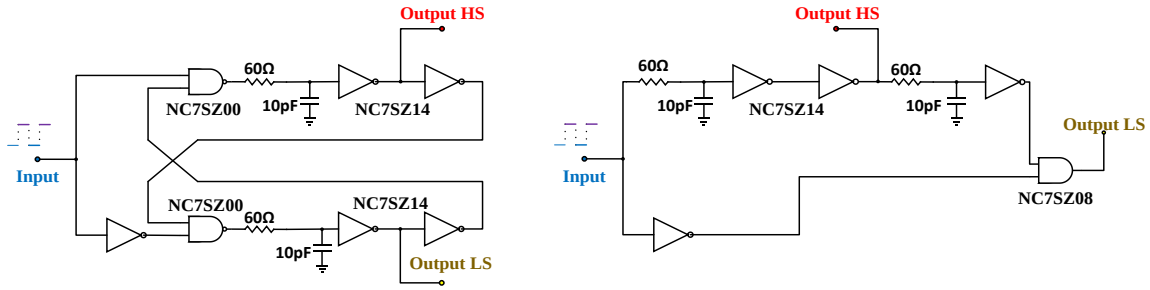

Figure 16: a) Discrete Non-Overlapping Clock Generator Circuit, b) Series Cascaded Dead Time Circuit

The controller is followed by a gate driver to drive the enhancement mode GaN (e-GaN) FET devices [21]. The chosen COTS part for this function is LM5113, which is a 1.2A/5A half bridge driver for power FETs. Its advantages lie in the fast propagation times (28ns typical) and low pull-up or pull-down resistance. It can support operating frequency up to 1MHz [20]. Unfortunately, the internal gate voltage clamp and the bootstrap circuits within

the LM5113 limit the maximum frequency of operation to well below 10MHz. Therefore, these circuits are bypassed, and an external clamp is employed with an EPC8004 GaN FET, as illustrated in Figure 10, for the stacked interleaved and the single phase converter architectures. For the multi-phase architecture, a low reverse recovery Schottky diode for is used on board in lieu of the internal LM5113 bootstrap circuits. The losses from the bypass circuit are lower than the LM5113 internal bootstrap solution, and the external bypass helps the driver operate at 10 times higher f_{sw} than the absolute maximum ratings.

The gate resistors within the driver control the gate charge and discharge current by forming a first order RC filter network [38, 40, 41]. They can be empirically tuned to increase the rise and fall time of the gate signals and suppress the high frequency ringing of the gate signals. There are provisions provided to reduce the internal body diode drop of GaN with the parallel diode across the drain and source of GaN. This acts as a bypass path for the internal body diode, which is fabricated in the GaN device. These diodes have high forward voltage drop in the range of 1-2V. A Schottky diode (D_F as shown in Figure 15) with ultra-fast reverse recovery is used in parallel with the low-side GaN device for free-wheeling operation during the dead time period. This has a lower forward voltage drop compared to the GaN body diode, thus bypassing the body diode during freewheeling. The Schottky diode also provides additional robustness in a way that the switching node is never at voltages less than -1V as discussed before.

Efficient Power Conversion Corporation (EPC) devices were chosen for the presented converter implementations because EPC devices offer e-GaN (nominally off) functionality, small form factor parts, and good performance at the 20MHz switching frequencies [41]. The specific EPC power device was chosen based on the performance review of Figure 17.

The EPC2014C GaN power device is chosen as a trade-off between $R_{DS,on}$ and efficiency [30].

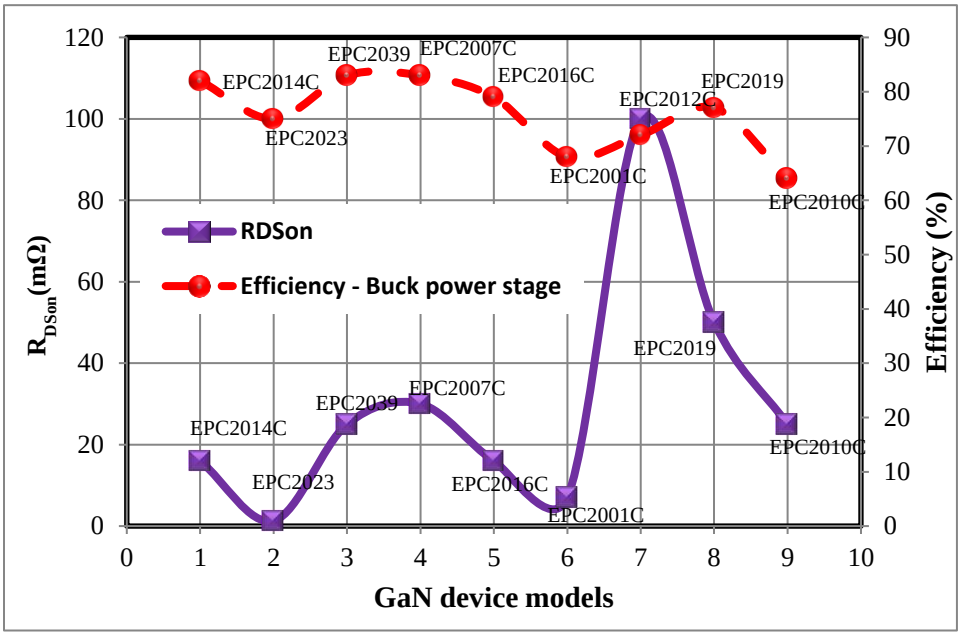

Figure 17: Device Selection Method for the GaN Power Device

3.3 Board Layout

The prototype board is implemented as a 4-layer FR4 integrated printed circuit board (PCB) design. The converter design uses the top layer for mounting components and providing the critical signal routing, including switching signals, the second layer as a continuous ground (GND) plane, the third layer is used as the power plane, and the bottom layer used as a GND plane except when a routing trace is required [5]. The board layout including the single-phase, multi-phase, and stacked interleaved converters is shown in Figure 18. The top half of the board houses the stacked-interleaved architecture, and a zoomed view has also been provided in Figure 18. The photo shows only the top layer of the board, which includes the main signal and power routing and all surface mount devices, with the exception of the bootstrap device that is located on the bottom side of the PCB [21].

All converter layouts use common layout techniques, including short traces in the driver path, wide signal lines for the switching nodes, and a second layer power plane for the driver and controller power routing. Additionally, all critical signal lines in the gate drive were modeled and scattering parameters (s-parameters) were simulated to ensure that parasitics associated with the board routing do not affect power converter performance.

The active area for each the multi-phase and stacked interleaved architecture is 4" x 2.3", and the single-phase converter is roughly half of this area (Figure 18). In order to optimize EMI performance, the converters use device placement and routing as illustrated in the diagram of Figure 19. The main intent of the power converter high current loop is to minimize the parasitic inductance and resistance. This is done to keep the undershoot or overshoot in the switching waveforms within the absolute maximum ratings of the GaN FET and to increase the efficiency of the converter. Figure 19(a) indicates the position of the discrete components of the power stage with C_1 as the input capacitor connected to Vin and C_2 as the output capacitor connected to Vout. The star connection GND between C_1 and C_2 has to be of minimum length and continuous. This is performed by the inner GND plane (2 layer), which acts as continuous GND for the star connection. The other components for the high current path are on the top PCB layer. The inner layer 2 is the power plane and the bottom layer has additional GND area for power dissipation.

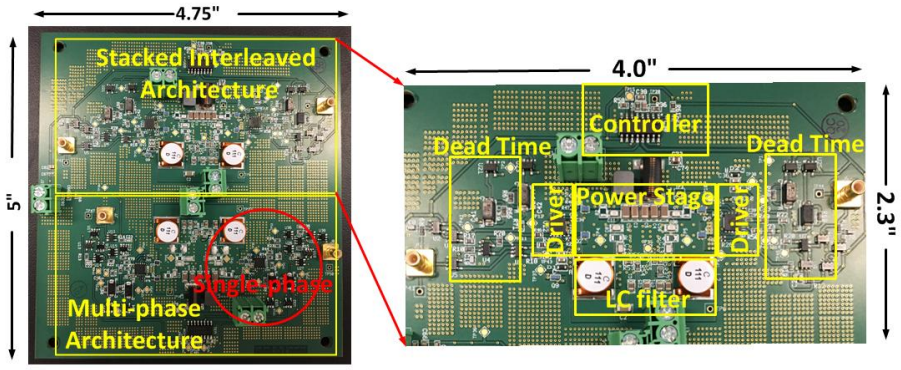

Figure 18: The Populated DC-DC Converter Board Top Side

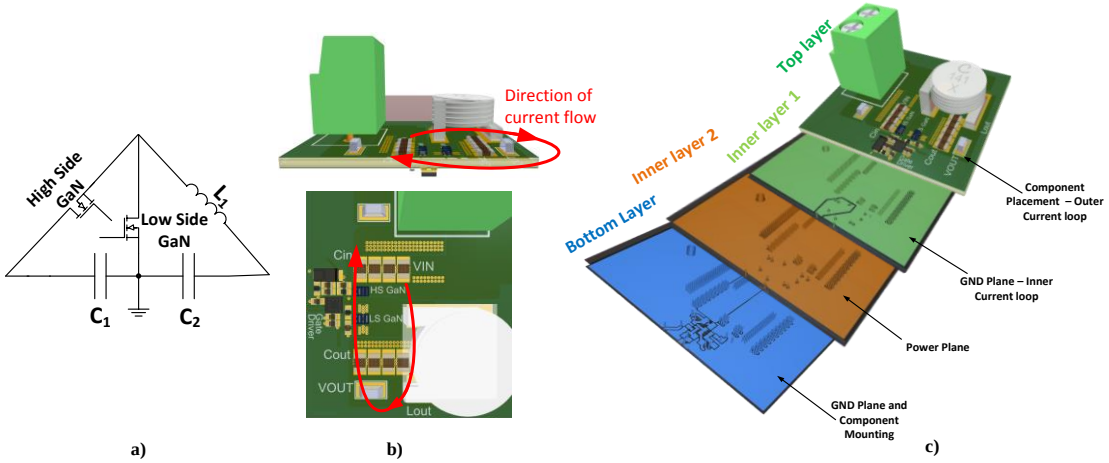

Figure 19: Power Device Converter Layout Configuration for Optimum EMI Performance. a) The Power Loop used in the Layout for GaN Power Stage, b) The Top and Side View of the Single-stage Power Converter, c) PCB Stack-Up of the Internal Layers for Single-Stage Power Converter

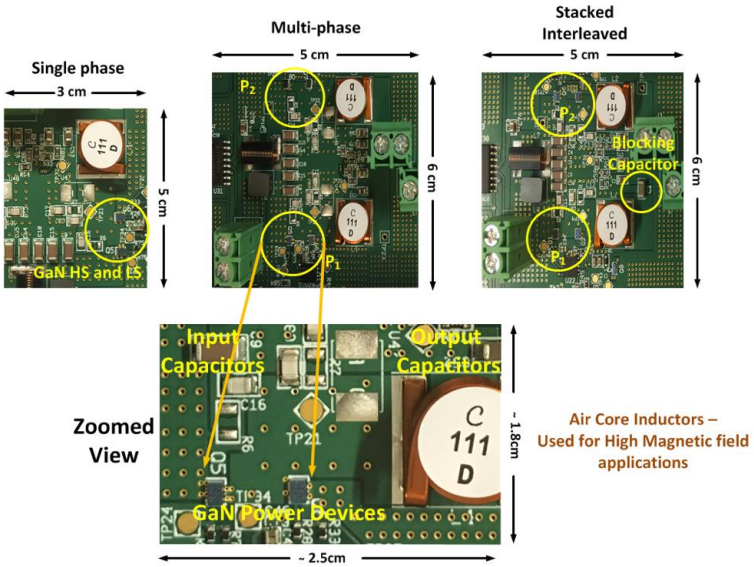

Figure 20: Overview of the Board Layout Indicating the Dimensions of the Power Converter Architectures

3.4 Measurement Results

The measured results are as shown in Figure 21-23. The three stages are designed for an input voltage of 24V to an output voltage of 5V with 22.8% duty cycle in open loop at different switching frequency and 7V to 1.6V in closed loop at maximum 1.6MHz switching frequency. The converters are configured in CCM (Continuous Conduction Mode) for high load current (5A to 15A) applications and Forced CCM/PWM (FPWM) for light load conditions to avoid EMI issues. The stacked interleaved architecture provides current ripple cancellation. The ripple in the output voltage is measured to be 0.4V (8%) for stacked interleaved, 0.45V (9%) for single stage, and 1.0V (20%) for the multi-phase architecture at non-50% duty cycles [27]. The results indicate that switching losses are dominant at low current condition due to high switching frequency operation. At high load current condition, conduction losses are dominant. Additionally, multi-phase architecture exhibits high efficiency at high current condition. The efficiencies of stacked and single phase architecture are similar in values.

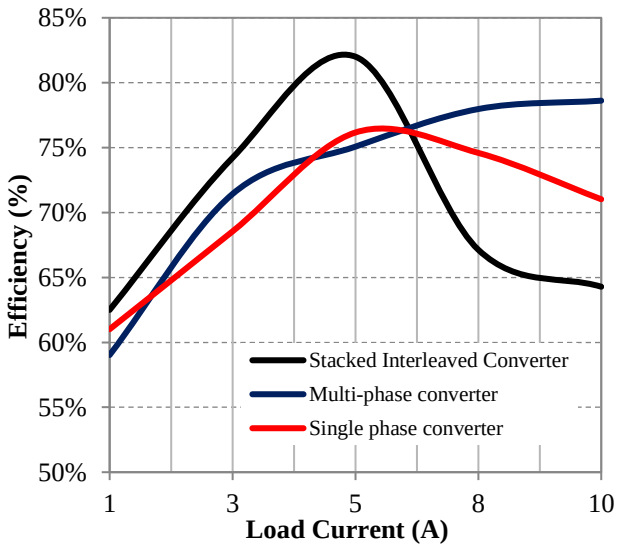

Figure 21: Efficiency for Various Load Current for Different Power Converter Architecture in Open Loop at 10MHz Frequency

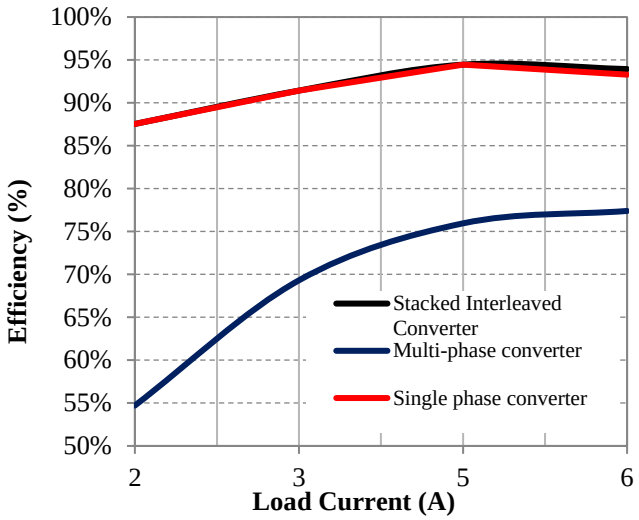

Figure 22: Efficiency for Various Power Levels for Stacked Interleaved Architecture in Closed Loop

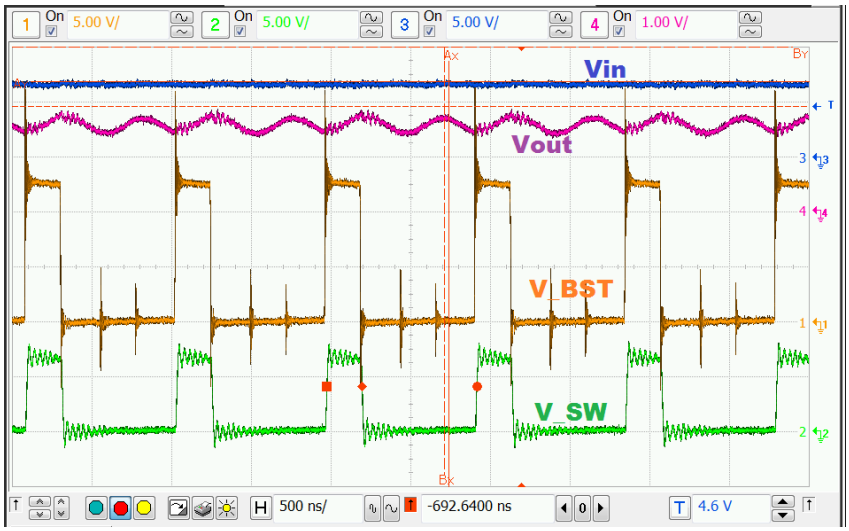

Figure 23: Measured Waveforms of: Vin (blue), Vout (red), Vgate_HS (yellow), and V_switching node (green) at 1.6MHz Switching Frequency in Closed Loop

The measurement test set-up is shown in Figure 24. The prototype measurement results verify that the switching converter power stage exceeds 80% efficiency at 10MHz switching in open loop and 1.5MHz in closed loop configuration. The results in the preceding section are validated under different loading conditions and operating frequency. The small form factor is achieved with the use of low value of output LC filter. The different power converter architectures are successfully compared using GaN. Table 4 compares measured

performance of the proposed work with existing state-of-the-art DC-DC converters. The board parasitics and the components in this discrete implementation design limits the performance of the buck converter at high frequency. The controller and the driver speeds are also limited to maximum 10MHz switching frequency in the discrete implementation. Since the discrete designs have limited speeds, the integrated circuit implementation detailed in the subsequent sections is created to achieve the final system specifications of Table 1.

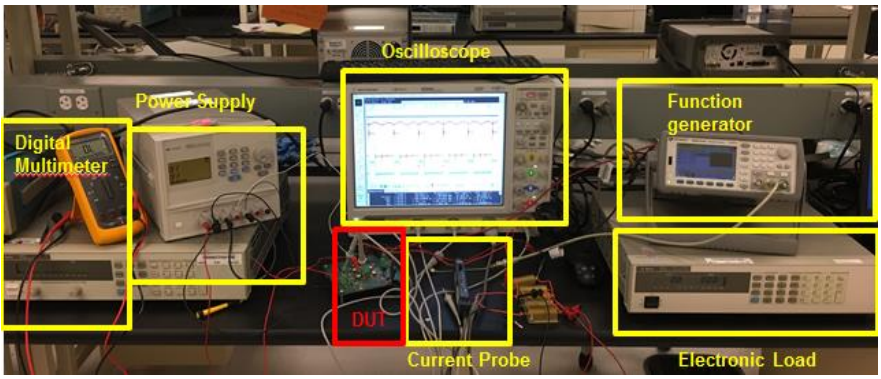

Figure 24: Measurement Test Bench Set-Up

Table 4: Performance Comparison with State-Of-The-Art DC/DC Buck Converters

Parameters	**[21]**	**[12]**	**[14]**	**[13]**	**[22]**	**This work**	**This work**	**This work**
V_{in} (V)	12 (9-28)	12 (5-12)	3.3	8	12 (4-15)	24	24	24
V_{out} (V)	3.3	5 (0.6-5)	2.4	1.0	3.3 (0.9-6)	5	5	5
Architecture	Single-phase	Single-phase	Single-phase	Multi-phase (3)	Multi-phase (2)	Single-phase	Multi-phase (2)	Stacked interleaved
Power-stage switching devices	GaN EPC2015	Si Process 0.35µm LDMOS	Si Process 40nm CMOS	Si Process 180nm CMOS	Si Process	GaN EPC2014C	GaN EPC2014C	GaN EPC2014C
Max. f_{sw} (MHz)	1	3	100	40	2	10	10	10
I_{max} (A)	15	4	0.3	0.198	6	10	10	10
Peak η (%)	93.5% @ 15A, 1 MHz	88% @ 2A, 1.8MHz	91.5% @ 0.15A, 100MHz	76% @ 0.051A, 40MHz	92% @ 4A, 1.6MHz	88.3% @ 5A, 2 MHz	83% @10A, 2 MHz	88.3% @ 5A, 2 MHz
ΔV_{out} (%)	N/A	<6.5%	<2%	N/A	<2%	20%	9%	8%

4 SYSTEM OVERVIEW OF INTEGRATED CIRCUIT IMPLEMENTATION

4.1 Top Level Architecture

The main challenge for the proposed converter is sustaining fast and stable loop response with high overall converter efficiency over radiation that causes parameter drifts in potentially every component. The switched-mode buck configuration is designed to provide a minimum of 5A of current at an output voltage of 5V, with state-of-the-art power efficiency. Additionally, the proposed design shall employ switching (clocking) speeds over 10MHz in an effort to reduce passive device sizing and decrease physical area for module-level integration [38]. The converter uses a GaN-based power stage together with radiation-hardened CMOS-based drivers, feedback, and compensator. The CMOS integrated circuit (IC) is divided into two voltage domains: a high voltage (18V) domain and a low-voltage (3.3V/5.0V) domain. The logic and controller circuitry are performed at 3.3V, with an on-chip radhard linear regulator providing the 3.3V supply from a 5V internally generated supply. With the radiation hardening strategy highlighted in this thesis, the low voltage devices have shown to be immune to total dose effects at 400 megarad (Mrad) levels. The low-side gate driver circuitry is implemented at 5V. The components in the high voltage domain (18V) for the high-side gate drive are subject to degradation in harsh environments, but these devices have also been radiation hardened using radhard layout techniques, as described in this thesis. Both industry and research have explored fabrication processes and circuit topologies to reduce power losses due to switching in converters.

The following design innovations are targeted from the integrated implementation of this work with the system overview shown in Figure 25. There is an optimal division of functionality present between GaN and silicon CMOS [13]. The system is designed to improve the efficiency at large conversion ratio with the CMOS gate driver architectures to control the GaN power devices. The design challenges and proposed solutions of this work are summarized in Table 5.

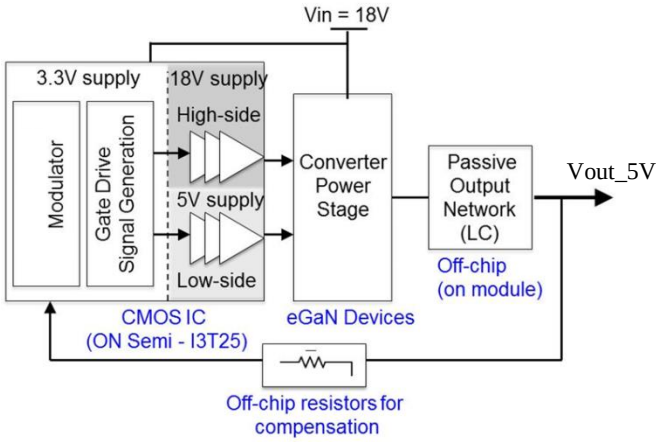

Figure 25: System Overview of the Work

Table 5: Overview of design problems and solutions

Design Problem	Solution
V_{GS} 5V swing for GaN	Cascode transistor architecture
High switching frequency/High Gate drive transient current	Driver stage sized appropriately, & Layout techniques
Efficiency	Device choice, Soft switching on board, and External bootstrap
Transient response	High switching frequency and Increase of loop bandwidth
Low duty cycle operation	Fast loop bandwidth
Single 18V Supply solution	Two integrated linear regulators to support three voltage domains

Based upon the selection of EPC power devices as well as the CMOS process technology of ON Semiconductor's I3T25 (350nm) process, Figure 24 shows the overall diagram of the final DC-DC power converter. The converter consists of a CMOS integrated circuit (IC) that includes all controller and driver circuitry. The feedback compensation requires a couple of off-chip resistors. The output filter is also implemented off-chip. The final DC-DC converter will use a single-stage synchronous buck converter. This power stage architecture was chosen based upon the measurement results from the prototype design discussed in Chapter 3. The single-stage power architecture consumes the smallest area because it requires only one output inductor and two power devices.

The designed IC employs voltage mode control architecture [32] due to its following advantages: it has single feedback loop (easy design), constant switching frequency to eliminate frequency hopping for EMI, good noise margin due to large amplitude ramp waveform, and low impedance power output, which provides better cross regulation when using multiple output supplies. The limitations of this control method are slow response to load transient and loop gain variation with change of input voltage.

In summary, the IC shall provide sufficient drive requirements to control the GaN power stage for a minimum switching frequency of 20MHz. Furthermore, the IC utilizes one supply voltage of 18V and internally converts to 5V and 3.3V [33] to provide voltage to the controller and low-side driver circuits. The chip includes two driver architectures, an on-chip bandgap reference circuit [35], ramp generator for 20MHz switching frequency (with tune-ability for lower frequency switching), and adjustable dead time control, as

detailed in Figure 26 [31]. The power converter, including the CMOS chip, is radiation hardened.

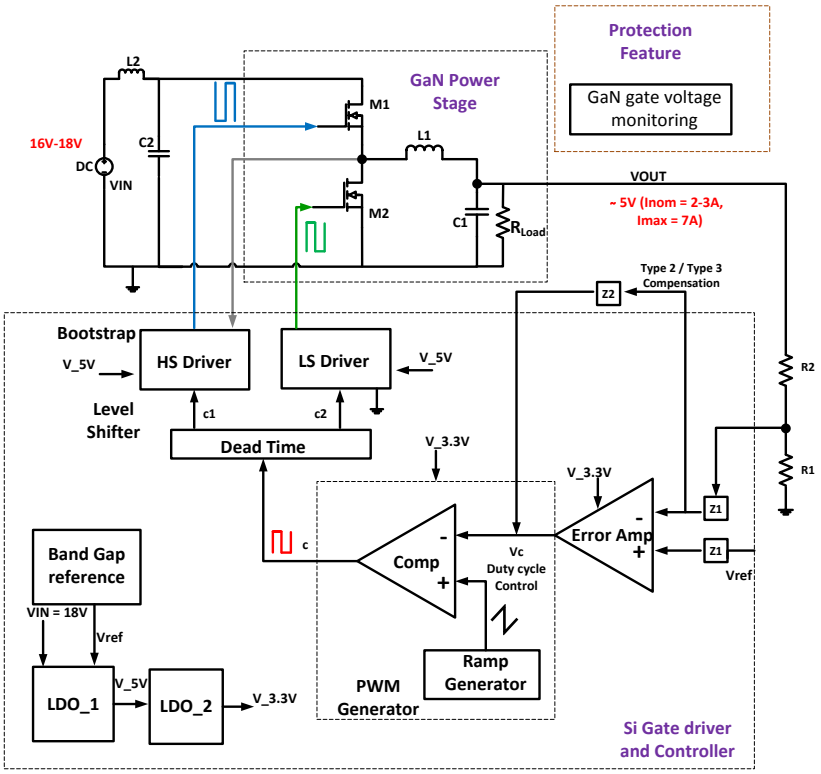

Figure 26: Power Converter System-Level Block Diagram

4.2 CMOS Driver and Controller design

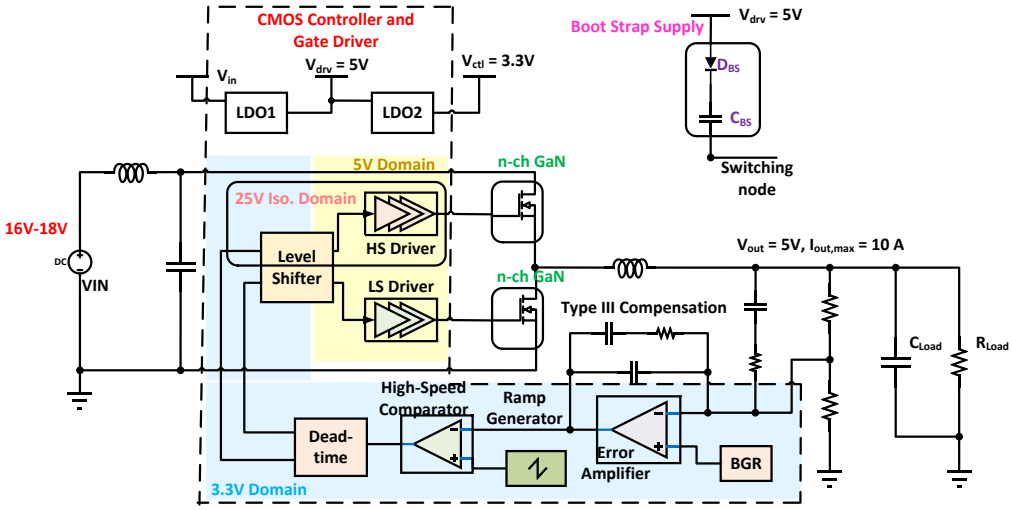

Figure 27: Schematic of the CMOS Driver and Controller on a Single IC

The CMOS driver and controller are integrated on a single IC capable of switching a GaN gate capacitance (200-300pF) load at a switching frequency of 20 MHz. The CMOS system-level block diagram is given in Figure 27. The details for each circuit are given in the following sub-sections with their associated simulation results. The PVT and Monte-Carlo is performed for the majority of the individual blocks. The closed loop stability analysis is performed across PVT and Monte-Carlo to ensure correct operation of all blocks within the controller and gate driver. The CMOS driver and controller use voltage mode control with external Type-3 compensation [32]. The BGR generates the reference voltage with the internal supply generated with two-step voltage conversion: LDO (linear regulator) One has Vin (~18V) to 5V for the driver supply, and LDO two has 5V to 3.3V conversion to generate the 3.3V control voltages. The error amplifier uses a folded-cascode topology [33, 35] with its output fed to a high-speed comparator. The other input of the comparator is connected to the ramp generator output with the option to bypass the internal ramp generator. The output of the comparator is the input to the dead time circuit, which generates two non-overlapping pulse-width modulation) signals. The discrete GaN power device is similar to an N-channel FET. Hence, the driver signal swing needs to be higher than the input voltage, and a bootstrap circuit is used to provide this higher voltage. The level shifter performs the function of the level shifting to the PWM high side output from the dead time to turn on/off the high side driver. The driver is the cascaded version [25] of the standard output driver stage, which consists of the use of low voltage rated transistors to driver the high voltage GaN. The design innovations are summarized as follows:

1. Highly integrated, high switching speed buck converter topology to achieve small physical form-factor.

2. Optimal division of functionality between Silicon and GaN to take advantage of inherent high current density and high switching speed of GaN devices for the crucial power stage and the versatility of CMOS to implement the bulk of the controller functionality.
3. An enclosed layout transistor (ELT) technique and design flow to reduce the total ionized dose (TID) induced leakage [24, 26].
4. Innovative CMOS-based gate driver architectures that directly control the converter's high voltage GaN power stage by employing only thin gate-oxide low-voltage devices to maintain highest radiation hardening [25].
5. On-chip high-efficiency voltage regulation and distribution schemes.
6. Accurate Bandgap Reference (BGR) employing CMOS devices without radiation-prone bipolar devices [17].

The subsequent section provides details of the schematic designs and the simulation results for the CMOS gate driver and controller circuits.

4.3 "House of Cards" Circuit Driver Stage

"House of cards" (HoC) is the driver architecture used for high switching frequency RF applications [25]. The implementation of this circuit to drive power devices is a novel method for using silicon to directly drive GaN. The advantage of this circuit is that lower break-down voltage transistors can be used to achieve higher output voltages as the voltage levels in the transistors never exceed the absolute maximum ratings of the MOSFET. For the presented system, a 5V driving voltage must be generated using the 3.3V silicon

transistors (which have thin oxides and are thus inherently tolerant to radiation-induced V_T-shift, as discussed later in this report). The intermediate node capacitors are used to provide the transient current requirements for the gate of the GaN. The switching is controlled by the level shifter circuit detailed in next section. The capacitor divider needs accurate inter-digitization layout technique for better matching. In this circuit the input and output bond wire inductances are modelled and tested. The schematic and the simulation results with 20MHz switching frequencies are shown in Figure 28 and Figure 29. The post extraction simulation results show the rise/fall time of the PWM signals to be ~3ns with the voltage level of the output to be ~5.5V. The drive strength of the PWM signal is 350mA average with 1A peak current capability. The layout of this block with the approximate size of 880 um x 440 um is shown in Figure 30, which shows the input inverter stage with the input capacitors, output inverter stage and the intermediate capacitors.

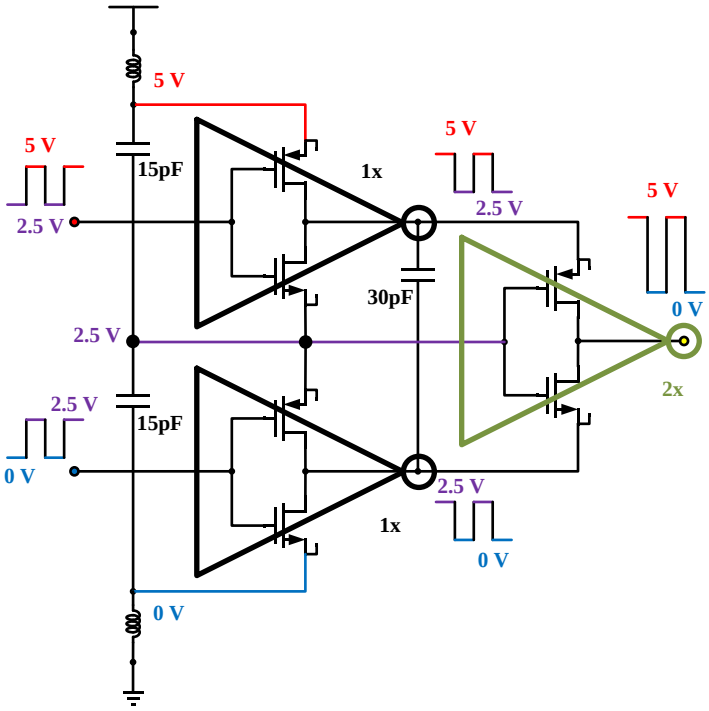

Figure 28: Schematic of HoC using 3.3V Transistors for Driver Stage and the Simulation Output

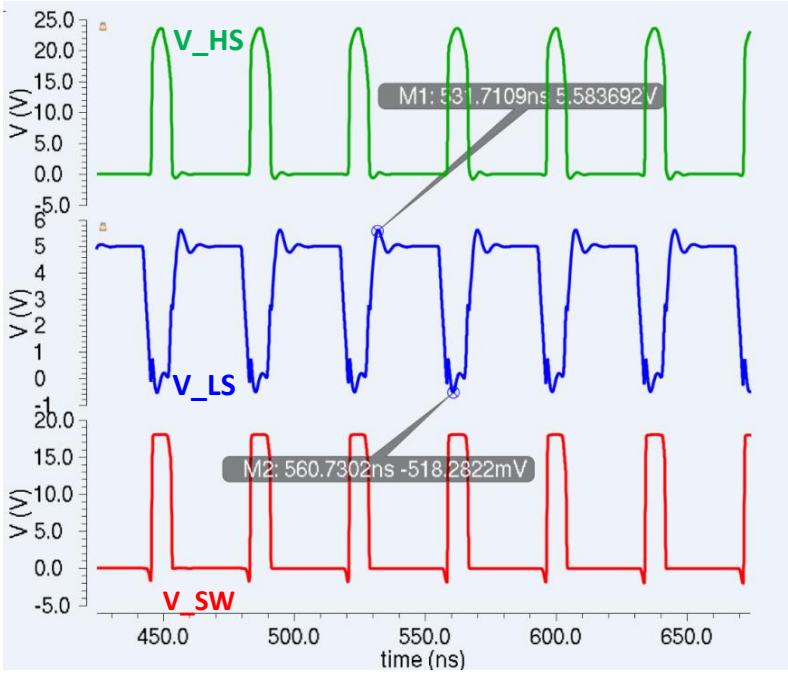

Figure 29: PEX Simulation Results of the HoC Driver Stage

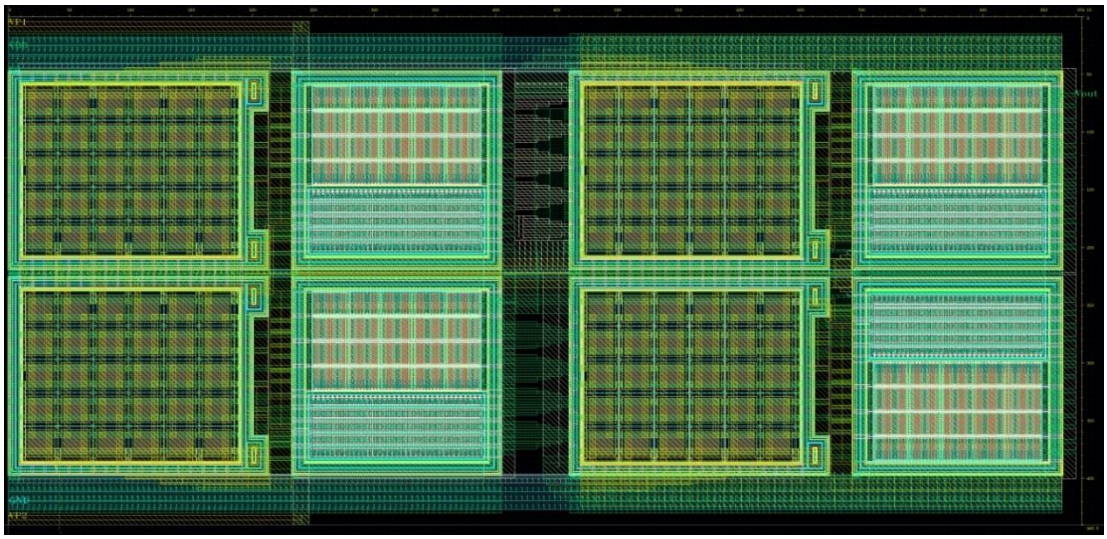
Figure 30: Layout of the Driver Stage (HS/LS)

4.4 Dead Time Circuit

The basic dead time circuit (aka non-overlapping clock generator) was designed using a standard cross coupled circuit [31]. The dead time can be configured by varying the analog voltage delay control – External analog pin 'Control' as shown in Figure 31. It is

configurable and the simulation result is for 1ns dead time between the HS and LS signals as shown in Figure 32 at 20MHz.

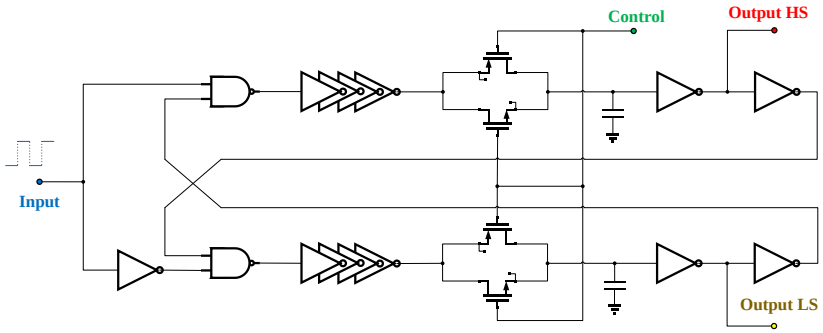

Figure 31: Simulation Schematic of the Designed Dead Time Circuit

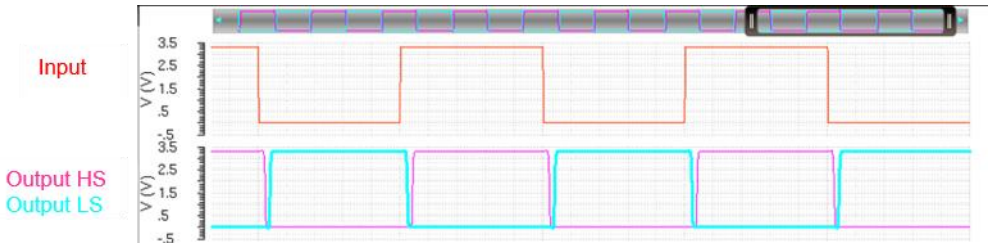

Figure 32: Simulation Results of the Designed Dead Time Circuit. OUT_HS and OUT_LS are the 0 to 3.3V Outputs and clk_in is the Input

4.5 Level Shifter

The level shifter is designed using the cross coupled inverter stage, as shown in Figure 33 [29]. This block is required to provide the desired signal swing for the cascade of the driver stage (high side/low side). The presence of HV – bootstrap voltage demands the need for 25V HV transistors as GaN gate needs 5V V_{GS} swing. This adds additional challenges for the high side level shifter stage with its low level being the switching node of the power converter. To drive the cascaded output driver, a complementary signal pair with one swing range of at 2.5-5V and the other one at 0-2.5V is needed as shown in Figure 34. Level shifter also used the radiation tolerant thin gate-oxide low-voltage LDMOS

provided in the 0.35um CMOS process. Simulation shows the simulation waveforms with 2-3ns dead-time at 20 MHz with 20% duty cycle. The layout of this block with the effective area of 420um x 500um is shown in Figure 35.

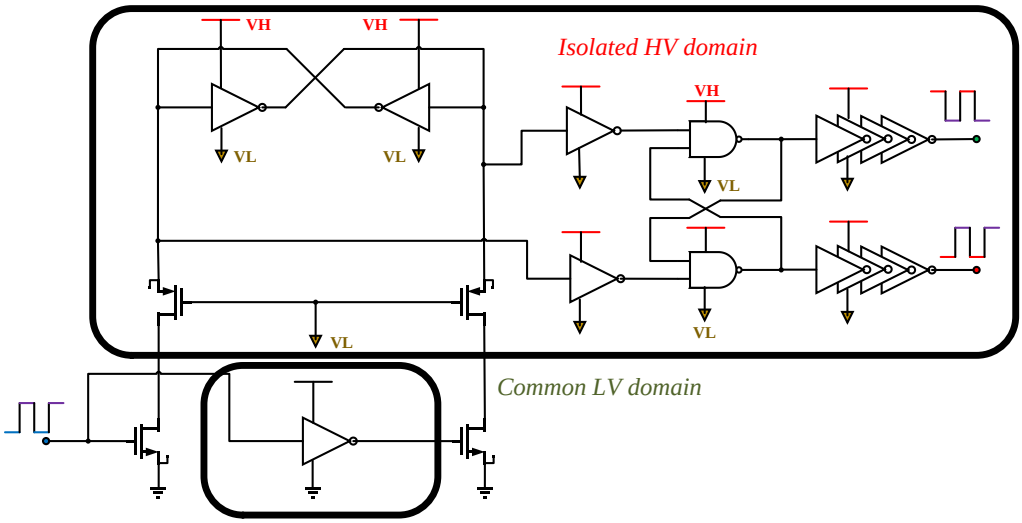

Figure 33: Schematic of the Level Shifter Block

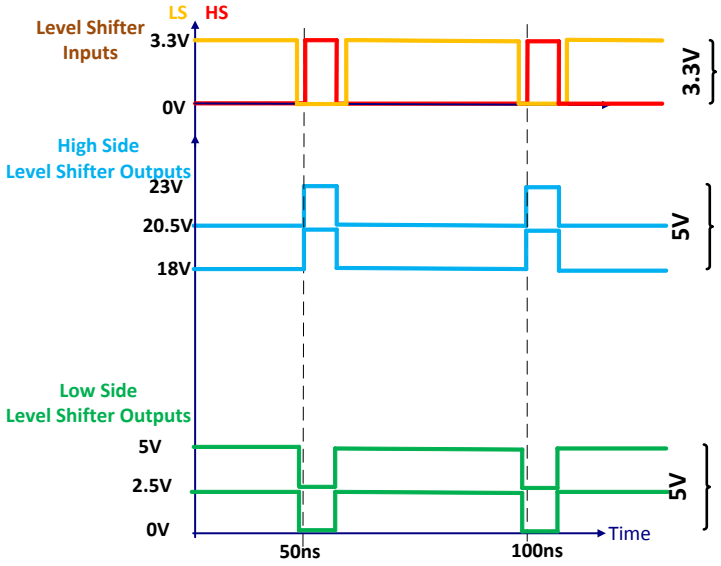

Figure 34: Simulation of the Level Shifter Block

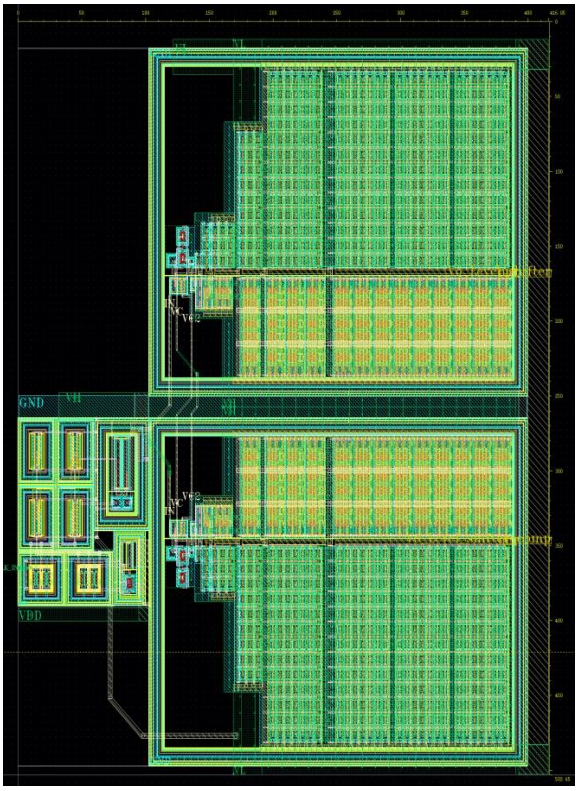

Figure 35: Layout of the Level Shifter Block

4.6 Error Amplifier Topology

This block is used as the first stage of the controller [35], which senses the output feedback voltage and thereby controlling the PWM pulse width. The schematic is shown in Figure 36 with the frequency response in Figure 37 exhibiting gain of ~75dB and 62MHz unity gain cross-over frequency. With the switching frequency being approximately 20MHz, the control loop bandwidth is selected to be 1MHz. External Type 3 compensation is used for error amplifier to provide the flexibility in design. The cascode stage at the output is used to boost the low frequency gain of the circuit. The criteria for the design was high bandwidth and hence the gain was compromised with low frequency gain across

corners being approximately 70 dB. The phase margin is approximately 80º to ensure the stability of the operational amplifier.

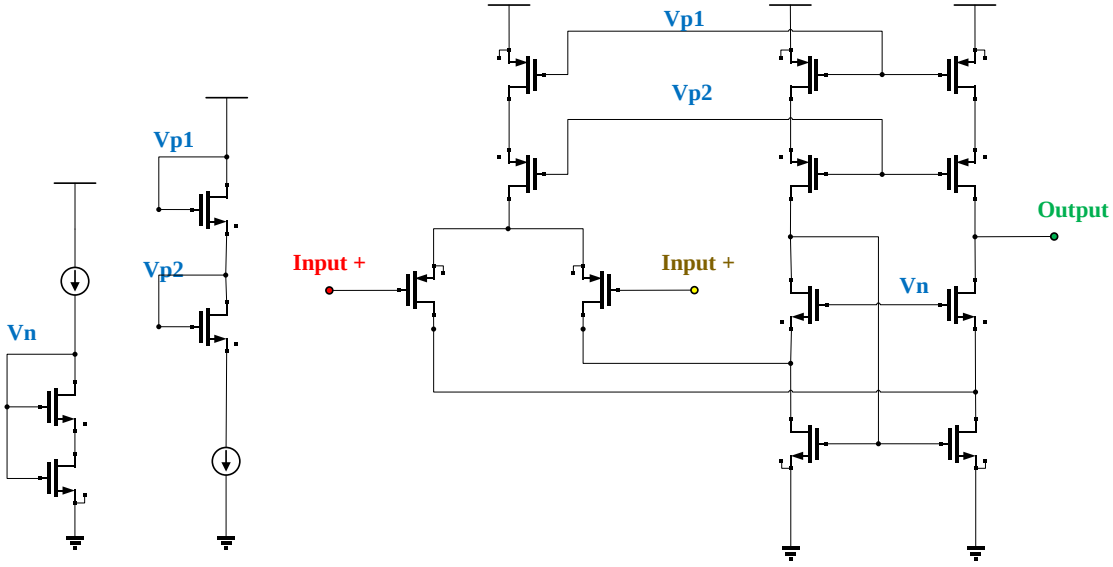

Figure 36: Schematic of the Error Amplifier Circuit with Telescopic Cascode Architecture

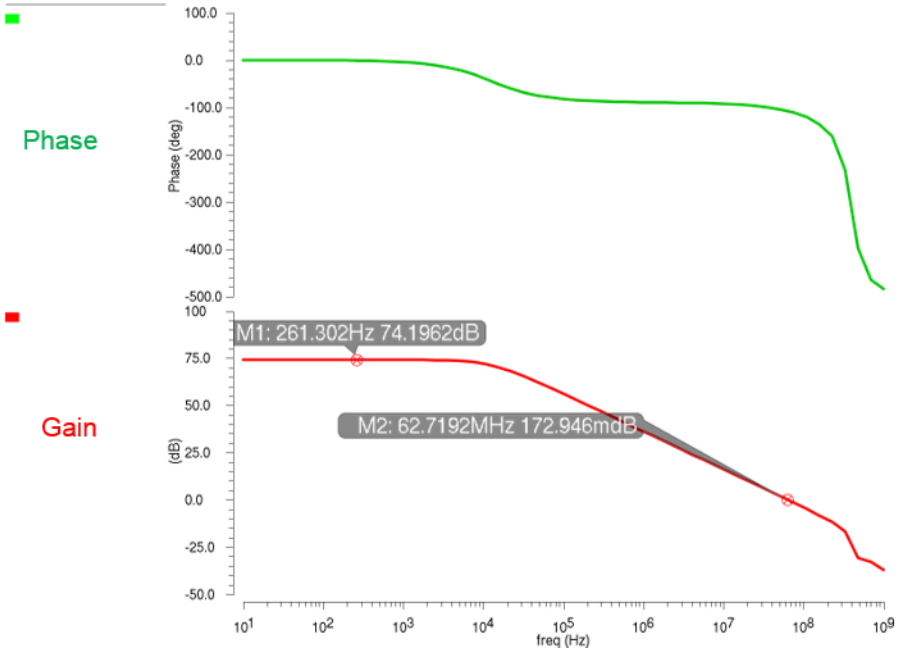

Figure 37: AC Response of the Error Amplifier in Open loop Configuration and Stability is also Ensured with Appropriate Type 2 or 3 Compensation

4.7 High-Speed Comparator

The high performance comparator consists of 3 stages: Pre-amplification, Decision feedback, and Post amplification (output buffer). The comparator is designed to operate up to 20MHz of switching frequency, as shown in Figure 38 [35]. It is current controlled with the decision feedback stage using the cross coupled stage. The level shift is provided by the diode connected transistor in the 2 stage. There are no high impedance nodes in the circuit other than input and output, thus enabling high speed operation. The decision circuit is designed such that the precision of mV signal level is present. The positive feedback approach is used and the circuit operation is ensured for low duty cycle operation which is required for this application. The output buffer converts the decision feedback output to appropriate logic signal (0 to 3.3V in this case). Figure 39 shows the inverting and non-inverting input and the output signals with the complementary output signal verifying the operation of the comparator.

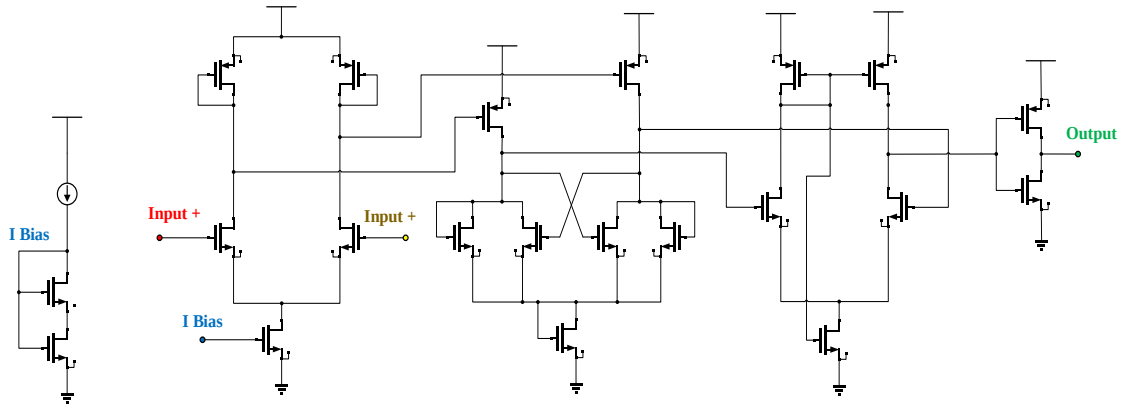

Figure 38: High Speed Comparator Circuit Design and Simulation Schematic

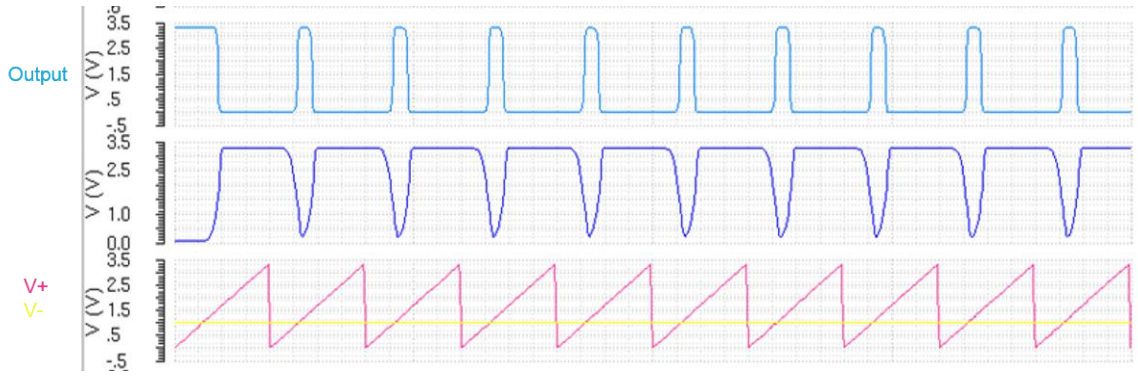

Figure 39: Comparator Simulation Results. The Test Signal Nodes (1,2 and 3) are Intermediate Signals

4.8 Linear Regulator

The pmos based LDO is used for 5V to 3.3V to provide power for the 3.3V transistors used in most of the circuit blocks on the chip (the driver output stage requiring 5V) as shown in Figure 40. The opamp used has 2 stages with appropriate compensation to ensure closed loop stability [32, 33]. The output pole is the dominant one in this circuit. The opamp reference is from the band-gap supply and the opamp supply through a Zener regulator (low current consumption). PMOS differential input stage is used in the opamp. The 2 stage opamp open loop gain is around 70dB. The LDO is designed with average current output being 100-200mA. Figure 41 shows the output voltage regulation of LDO at 200mA.

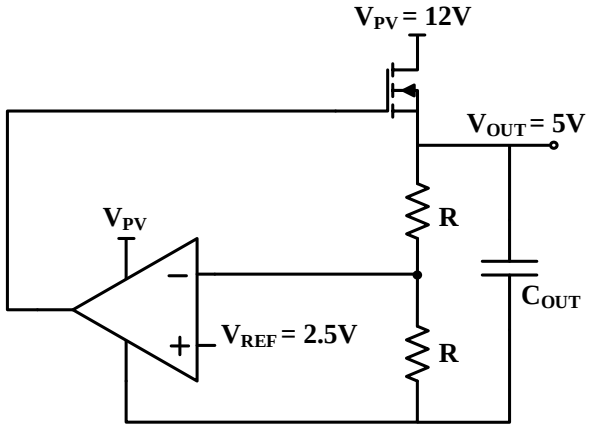

Figure 40: Schematic of the LDO Architecture

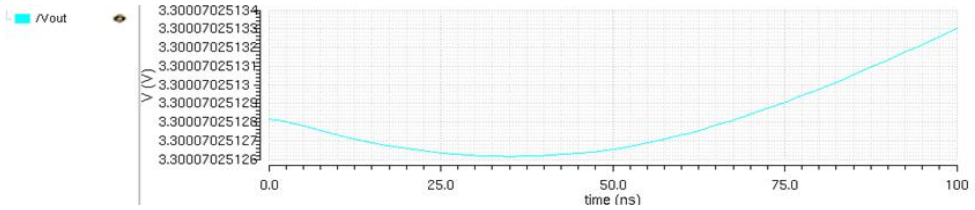

Figure 41: Simulated Regulation of the Output Voltage of the LDO

4.9 Ramp Generator

The ramp generator is implemented by a negative feedback loop with a desired voltage hysteresis controlled by the high and low switching voltage levels [35]. Ramp waveform generator is implemented with the Schmitt trigger, NAND gate and inverter in feedback loop. The NAND gate has the trigger input for the start-up of the circuit. It's output is fed to the inverter forming an oscillator circuit. The capacitor charge and discharge paths with different resistance (pull-up or pull-down) provides the ramp output. This controls the charge and discharge slope of the ramp waveform. The control of frequency for the ramp is done by setting different values of bias currents or using switch based method for pull-down path with different resistances. The former approach is used in this design. The desired transient hysteresis is controlled by the number of current sinking transistors (multipliers) and the capacitive charging loads. By using a 3-to-8 decoder, we will be able to select the number of current sinking transistors and load capacitive units. Figure 42 shows the schematic of the designed ramp generator and Figure 43 shows the schematic simulation results at highest desired frequency of 20 MHz, i.e. ramp output. The 3.3V trigger signal is provided externally (on-board) to start-up the ramp generator circuit. This ramp generator is simulated with a maximum frequency capability of 20MHz.

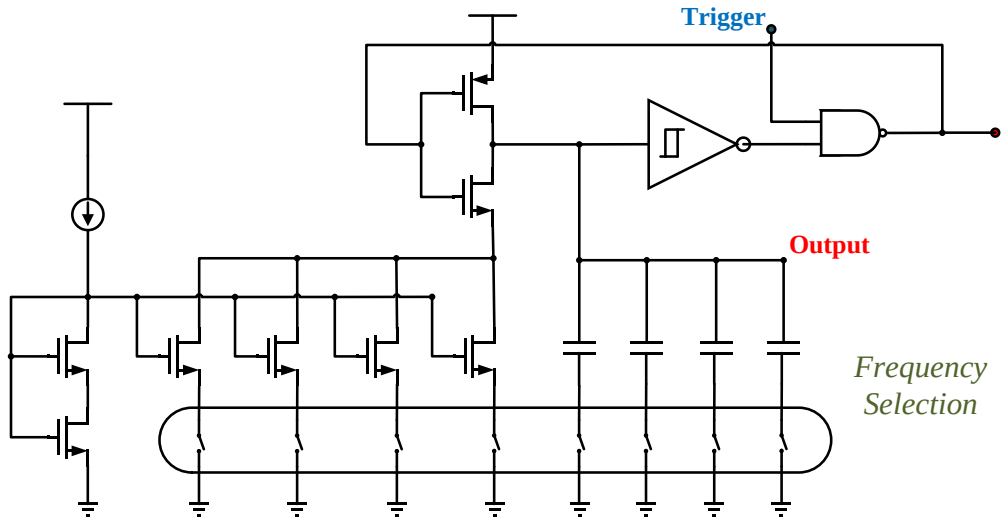

Figure 42: Schematic of Ramp Generator

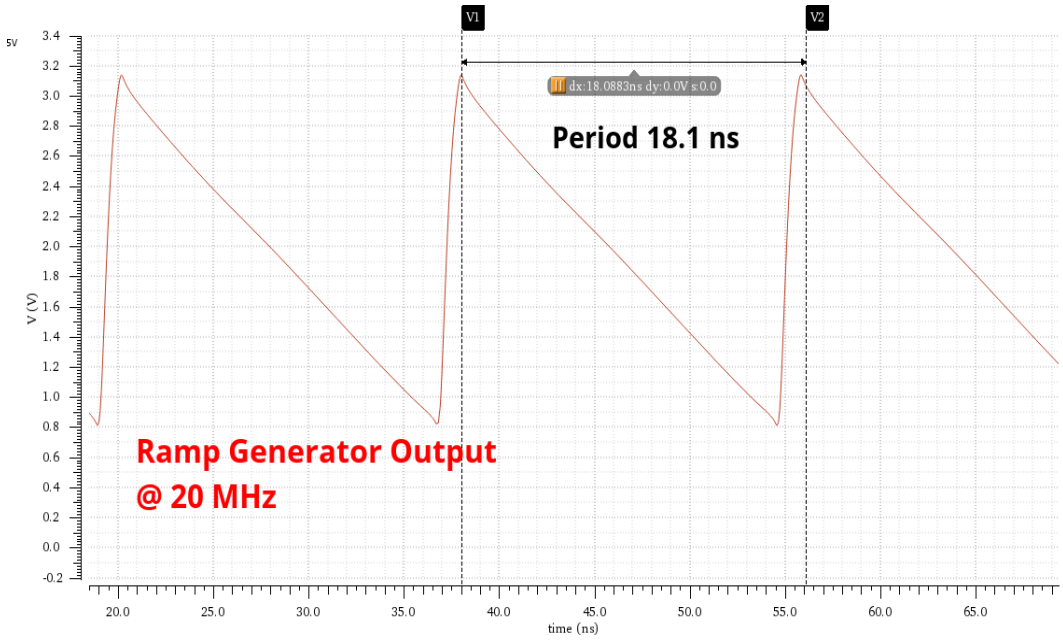

Figure 43: Schematic Simulation of the Ramp Generator at 20 MHz

4.10 GaN Power Stage Simulations

The single phase power stage is simulated and verified with EPC device models [30] as shown in Figure 44. The discrete component values are the same as the one designed for this application. The simulation results show the set output voltage at 1.76V with the

settling time as 2.5us as shown in Figure 45. The zoomed view of the switching signals for HS, LS and switch node is shown in Figure 46.

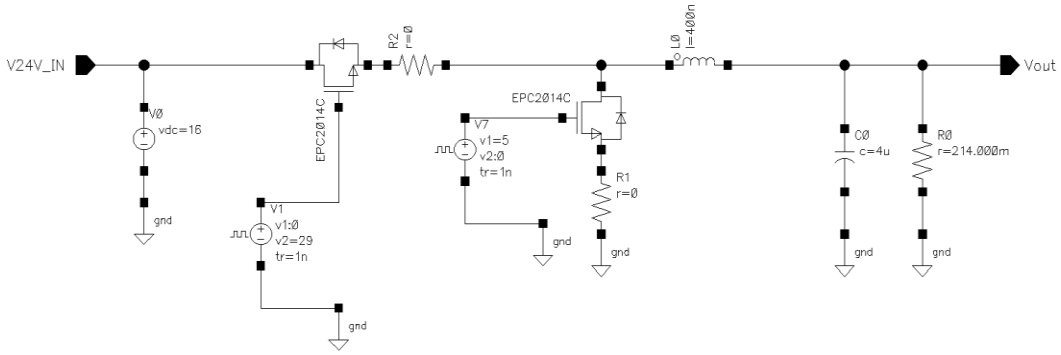

Figure 44: Power Stage Simulation with the EPC models

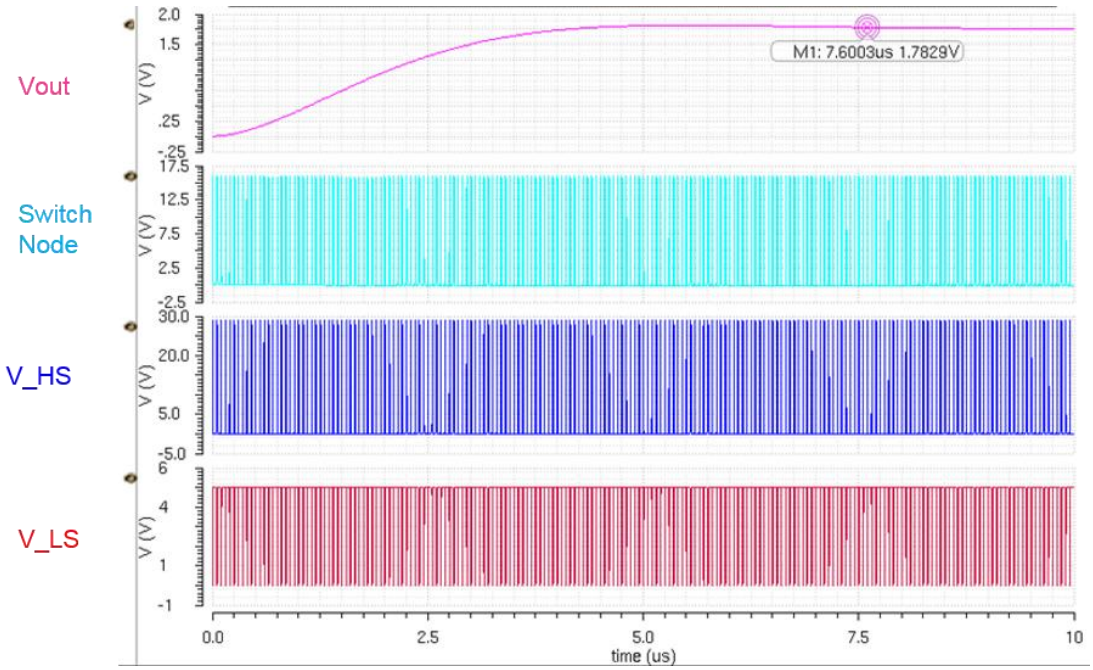

Figure 45: Transient Response of the Output Voltage

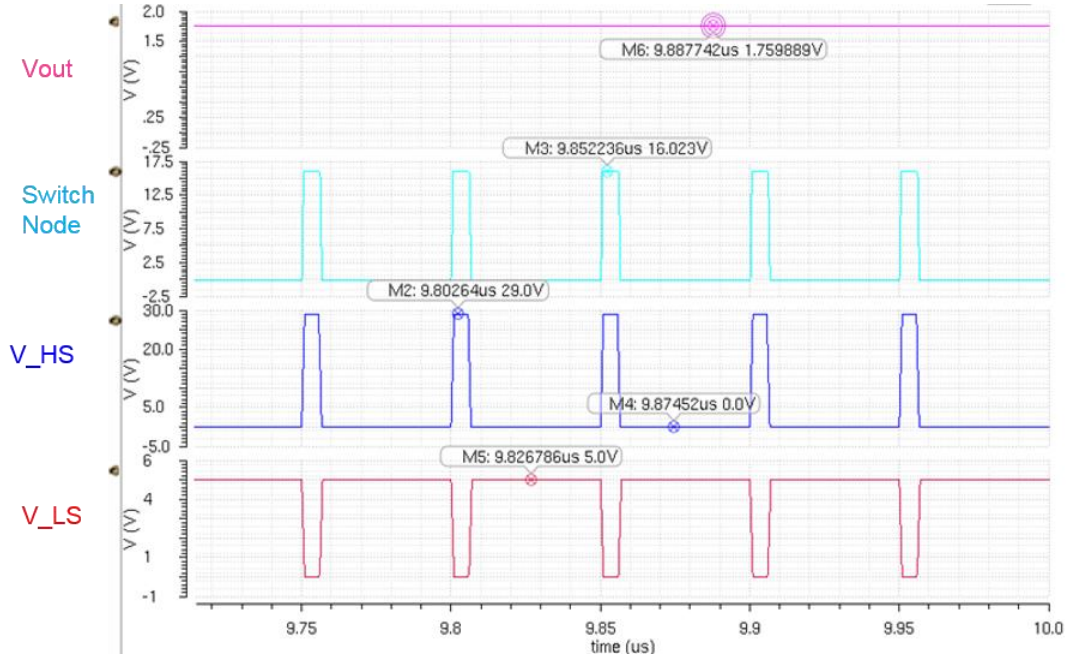

Figure 46: Zoomed View of the Output Voltage with the PWM Control Signal (HS and LS : net 28 and net 21 respectively) and Switching Node Signal for 10% Duty Cycle

4.11 Custom IC Layout

Angular gate (edgeless transistor) configuration is widely used in the design of IC's for radiation hardening applications. Based on the selected 0.35um process (ON-Semi I3T25) I3T25, customized rad-hard p-cell component libraries is developed to start the chip layout design process. Figure 47 shows the current snapshot of the customized I3T25_radhard library. The initial layout can be done by generating the corresponding layout views from the schematic views with all connections bindings. Based on above isolation requirements, further development of customized multi-parts path templates in Cadence were done for different kinds of isolation rings or wells without knowing the details of the process and rad-hard layout techniques, which will significantly reduce the coming tremendous layout work load for future designs in this PDK. A fully customized ELT-type NMOS low-voltage core transistor library cells including different sizes of primitive cells (p-cell) based on the

selected 0.35um CMOS process is developed to assist EDA design flow such as DRC, VLS and PEX process [24, 26, 43]. The procedures can be divided into four steps.

1. Approximate a standard NMOS W, L and W/L with a calibre extracted layout view.
2. Create a complete DRC and LVS clean cell with all isolation ring, body contact and parasitic diodes added, run PEX simulation if necessary.
3. Create a core device cell views with only gate, source and drain connection kept the last step.
4. Create/Update Cadence component description format (CDF) parameters for the core cells created above.

For example, in order to design a 20µ/0.7µ ratio angular gate NMOS, we first estimate the angular layout shape and sizes, then we make sure everything is DRC clean. By running Calibre LVS and find out what the exact Calibre extraction W/L values, we then change our corresponding schematic to these extracted values and run LVS again to ensure it is LVS clean again. In this case, the exact extracted W and L values for the layout are 20.3695 um for W 0.719138 um for L. In the schematic, the pin "B" is the NMOS body, which is an isolated p-well. "NPKT" means n-pocket, which is a concept we borrowed from I3T25 manual where HV or LV isolated e-epitaxy wells are called LV or HV pocket. "PSUB" is the connection to the p-substrate nested in the deep p-well. The final outer rings are called "NEPI" since it is common to the non-isolated n-epitaxy layer.

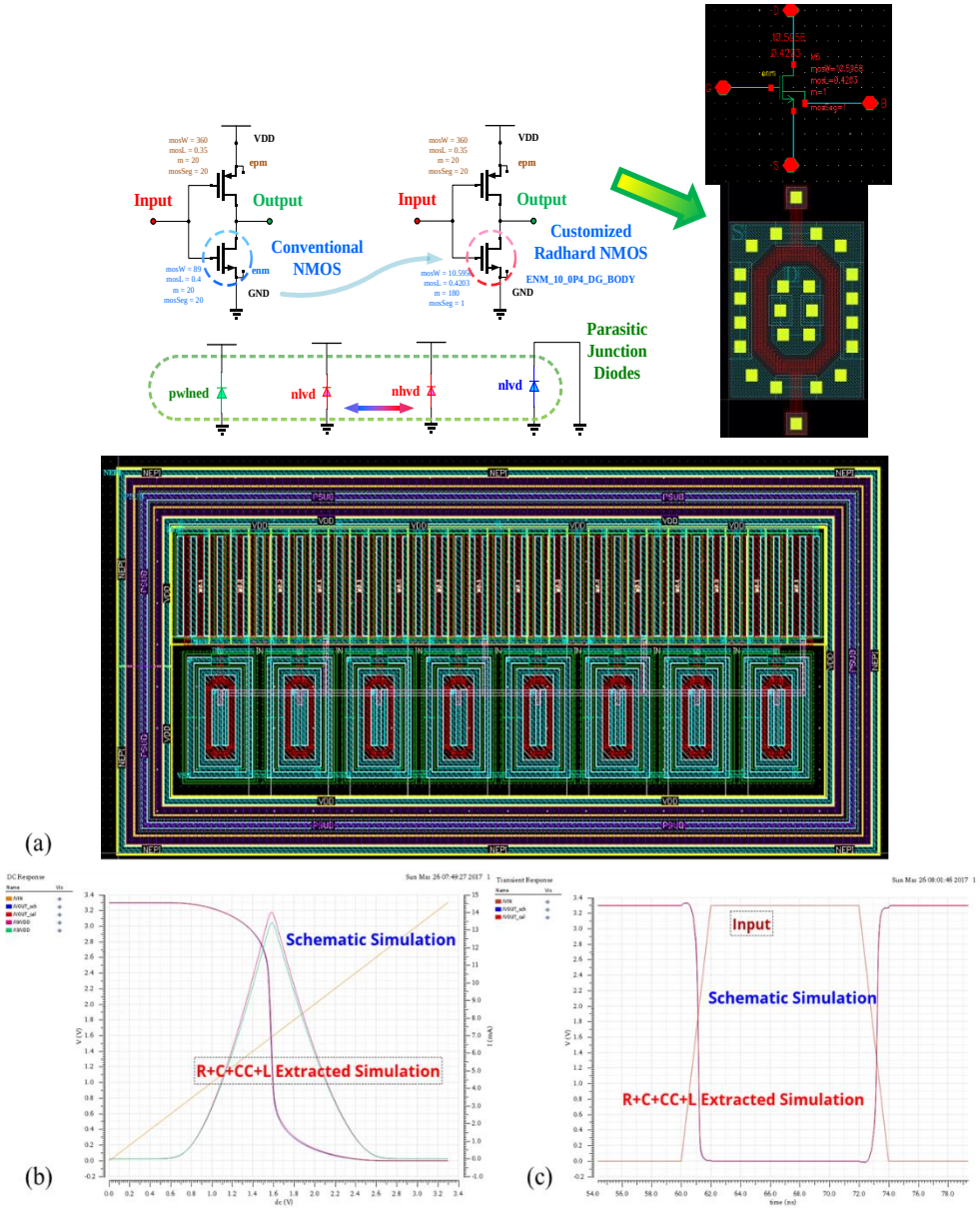

Figure 47: : An Inverter Schematic and Layout with m=8 Instantiated from the I3T25_radhard library, (a) Layout, (b) DC-sweep simulation, (c) Transient Simulation with 100 fF load

In the I3T25 process, there are only two types of on-chip isolation, called LV (3.3V) or HV (< 25V). The only difference in schematic is the parasitic diode from “NPKT” to “PSUB”, either “nlvd” or “nhvd”. In layout, however, it means wider deep p-well region

and several HV identification layers. Our customized HV isolation multi-path templates developed from the one in original I3T25 process will automatic generate isolation types for different NMOS and PMOS core transistors layouts.

A Schmitt trigger is used in most digital inputs pins to mitigate signal noise and buffer a clean digital signals into the chip. Figure 48 shows a Schmitt trigger design [35] using our customized rad-hard library. Notice here the PMOS and NMOS FET's do not share the same body connection. Two PMOS and NMOS have their own source –body connections. A separate "pwlned" parasitic diode, which indicates the NMOS p-well to isolated n-epitaxy pocket, from the floating NMOS body (label "A" in schematic), and another separated "nlvd" parasitic diode, which indicates the PMOS body to p-substrate connection through deep p-well, are added in the schematic and generated correspondingly in layout in Cadence automatically by the "Connection" option.

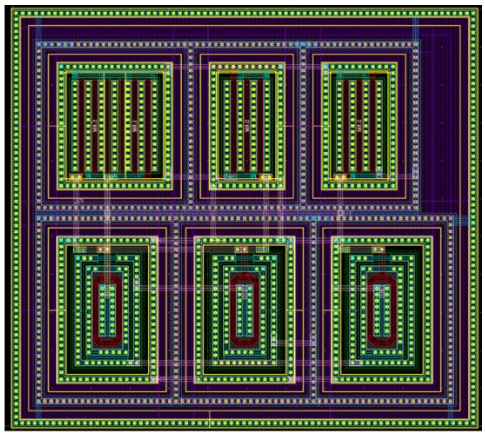

Figure 48: Schmitt Trigger Design from the I3T25_rad-hard Library - Layout.

The schematic and layout extracted simulation results for the designed Schmitt trigger are shown in Figure 49. We initially designed our Schmitt trigger to switch high at 2 V and switch low at 1 V. The extracted simulation in Figure 49 shows the expected switching

points. Due to the well-connected body to source terminal, simulation shows that the final layout results can even switch faster than the schematic specification.

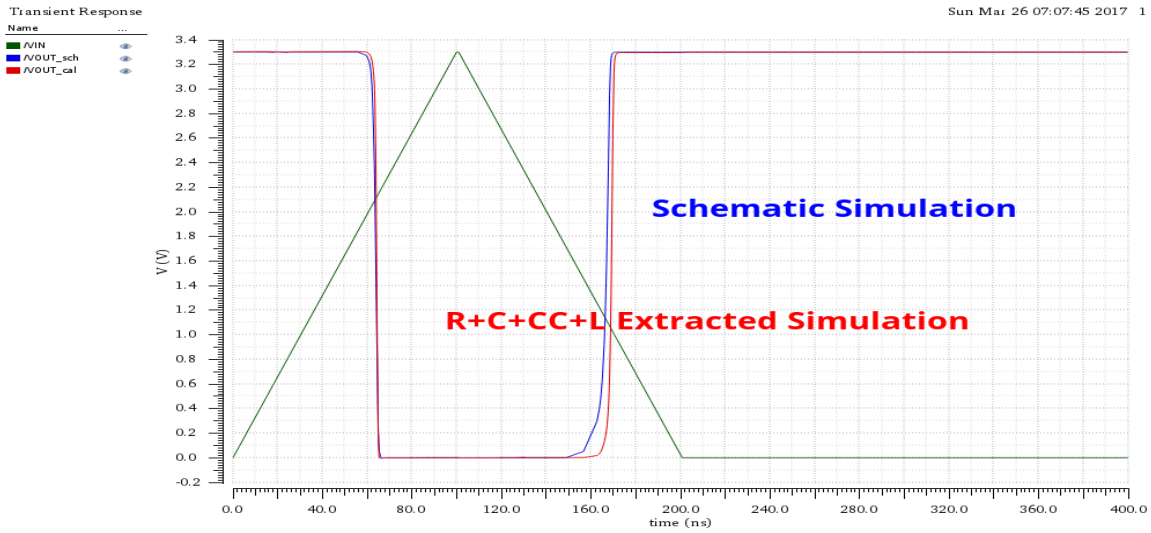

Figure 49: Schematic and Layout Extracted Transient Simulation of Schmitt Trigger

The layout of the fabricated integrated circuit is as shown in Figure 50. The process technology uses 5 metal layers [43]. Figure 51 shows the pinout of the fabricated die in the QFN 56 package with the pin names. The top level placement and routing for this IC is done with the intent of efficient operation at 20MHz switching frequency. Hence, the HS and LS driver blocks are placed close to the package pin and the die is placed longitudinally close to package pin. This is done to reduce the bondwire inductance (~3nH per bondwire) at the supply and PWM output. Each of the PWM output, driver supply, V_{SS} or GND path has four bondwires or die pads connecting to the corresponding two package pins. The HS and LS driver are vertical mirror image of each other to ensure symmetry in the HS and LS switching. Each block is isolated with the high voltage isolation guard ring up-to 25V in an n-epi process to ensure functionality at high supply voltage. Each HS and LS driver has two level shifter which are symmetrically placed as shown in Figure 50. All the analog

blocks for feedback control is placed towards the left of the IC with the 3.3V supply around the periphery of the die. The two LDO's (high voltage 18V to 5V for the driver supply and the low voltage 5V to 3.3V) are placed at the lower right area of the die. These are standalone blocks which have the provision to supply the driver or control blocks of the IC through the on-board connection. To reduce the ringing at the VDD nodes for the driver and controller, sufficient decoupling capacitors (~10pF) are placed closed to supply pins in the die area. The MIM capacitor are used for low voltage supply (3.3V) and the parasitic "nhvd" diode capacitor are used for high voltage driver blocks (5V). The bootstrap supply does not have any decoupling capacitor on die as it is very high voltage node (up-to 23V).

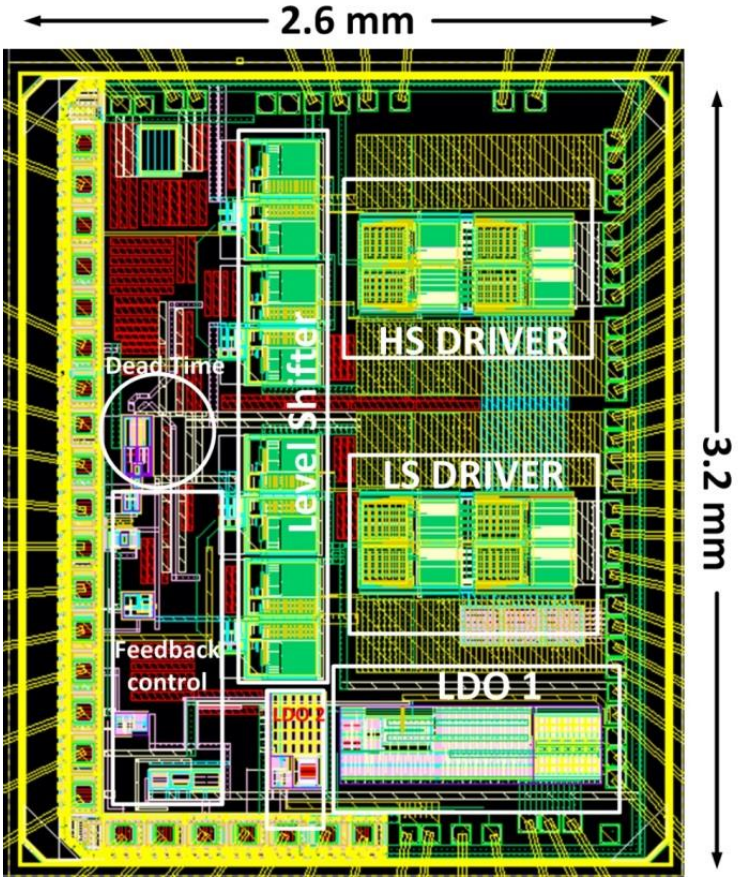

Figure 50: Layout of the Fabricated CMOS Gate Driver and Controller IC

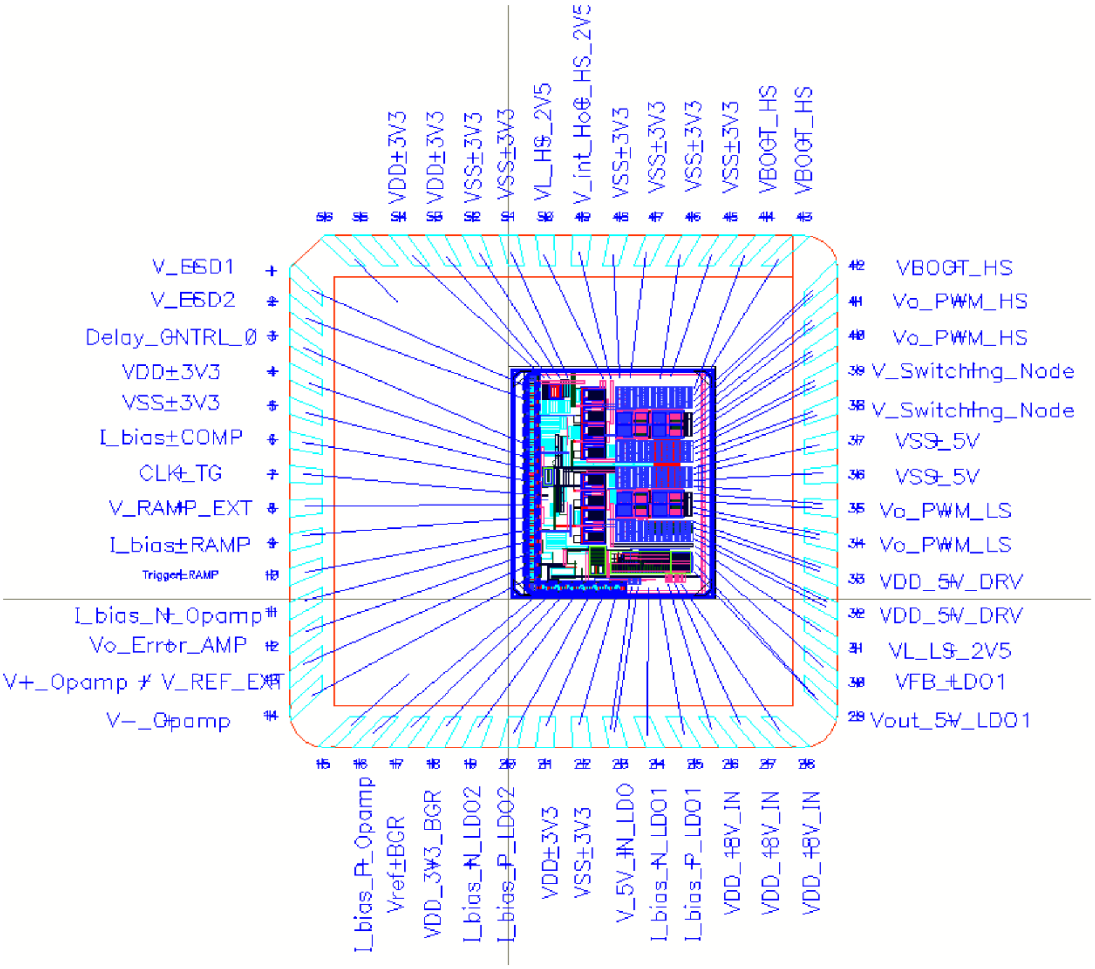

Figure 51: Pin Description of the QFN 56 Package of the Fabricated IC

5 FABRICATED IC AND MEASUREMENT RESULTS

5.1 Die Photograph and Test Prototype Board

The die photo of the fabricated IC is given in Figure 52 highlighting the different designed blocks that form the driver and controller blocks. Figure 53 shows the fabricated prototype converter board with different sections used for debugging the fabricated IC. The effective board size of the prototype board is 8.7cm × 9.2cm. The IC was measured for different test cases to validate the power converter's performance.

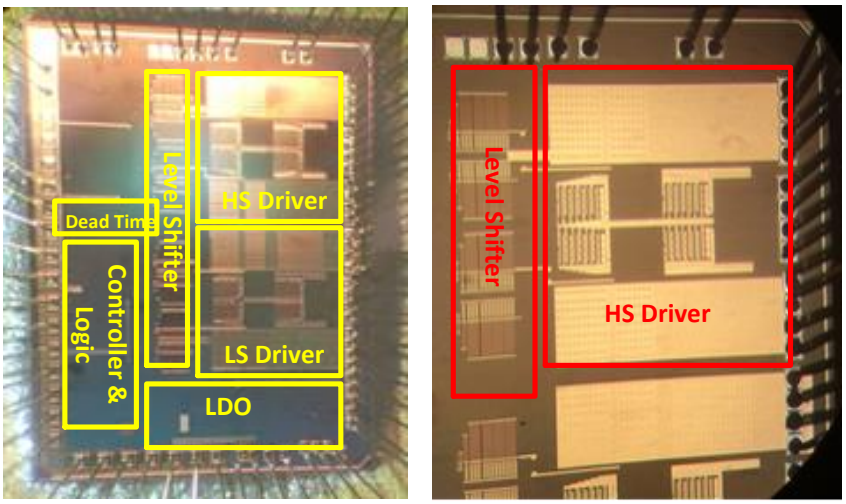

Figure 52: Die Micrograph of the Fabricated Die and the Zoomed View of Die

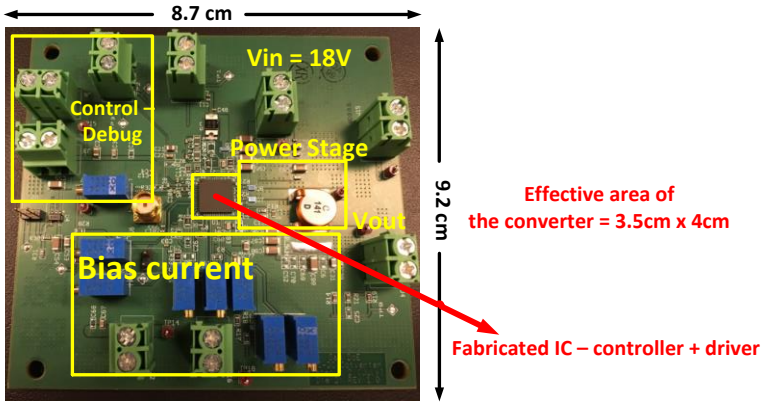

Figure 53: Zoomed View of the Prototype Board used for Die Measurement

5.2 Measurement of Switching Signals in Open Loop

The first measurement of the fabricated IC is the DC voltage measurement and power on test. This is followed by setting the exact values of the potentiometers for fixing bias currents of the various circuit blocks. Upon successful evaluation of the DC voltages and current, the internal ramp generator and external ramp (through external function generator) is validated successfully. Then, the analog delay control for the dead time is verified at different switching frequency from 5MHz to 20MHz. This is followed by switching signal output validation with 100pF as the capacitive load on the driver output. The open loop test with capacitive load validates the successful operation of the individual blocks in the driver and controller IC from the error amplifier to the HoC driver. The error amplifier is configured in the voltage follower mode and the DC input (error voltage) is fed to the inverting input of the amplifier. This error voltage modulates the duty cycle of the PWM output signal.

Figure 54 shows the high-side and low-side gate signals when the GaN power stage is off (no supply voltage to the GaN power stage) at 13.8MHz with capacitive load. The setting of frequency for measurement is tuning the bias current for ramp generator on-board. This led to varying the switching frequency in discrete intervals such as 13.8MHz, 15.8MHz and maximum of 20MHz. This test is used to verify the correct dead time between the two complementary control signals and the control signals' voltage levels. The glitch during the rising edge of the waveform is due to analog control of the dead time circuit through the pass transistor. The measured dead time between the high side and low side output is 2ns - 6ns. Figure 55 shows the switch node signal with the snubber design for the GaN power stage. The snubber is designed optimally through measurement and the

value of the snubber for optimum control of the switch node ringing is 6.5Ω and 300pF. This snubber suppresses the peak amplitude of the switching node to 3.58V at 15V input supply.

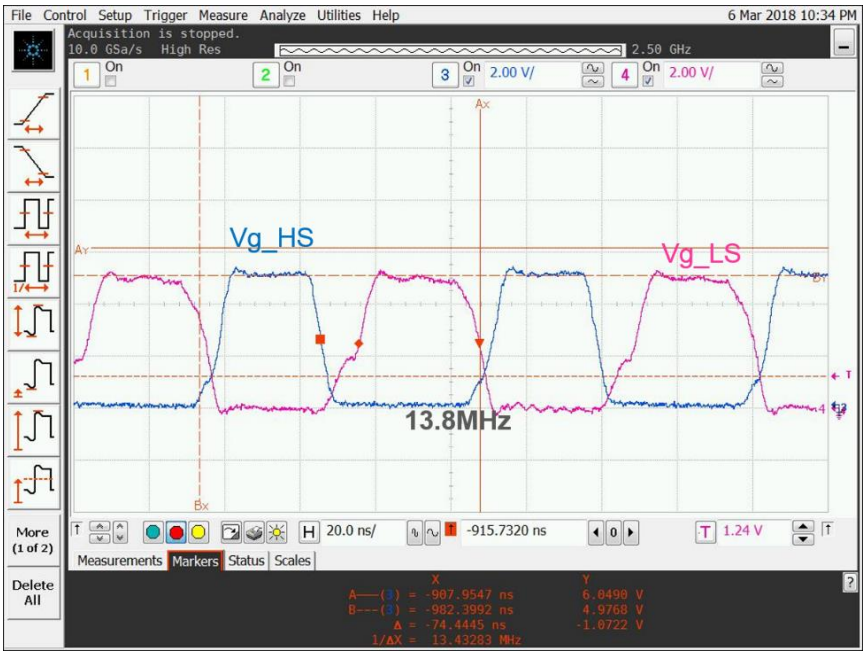

Figure 54: High side and Low side Switching Signals at 13.8MHz

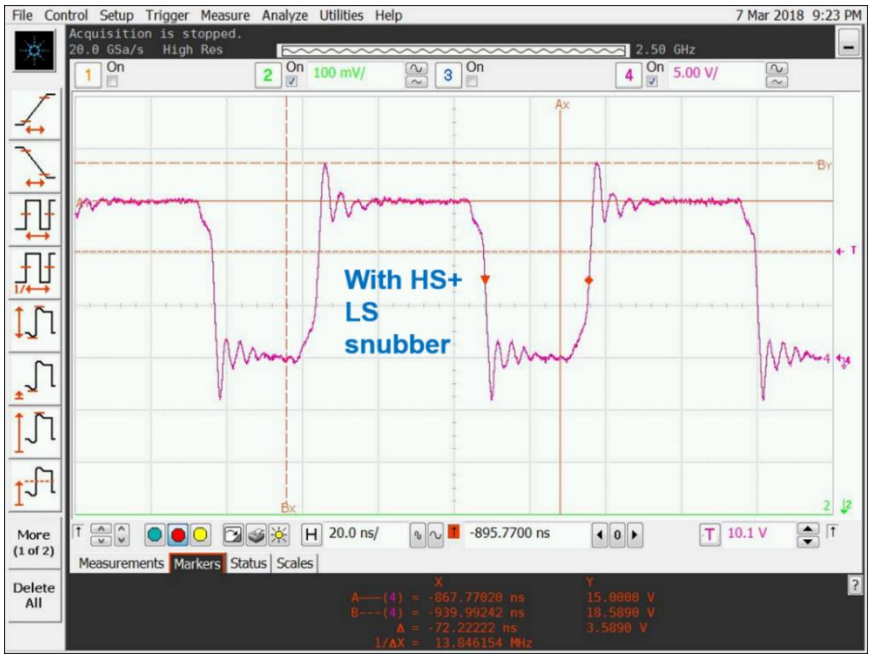

Figure 55: Effect of Snubber on the Switch Node for Ringing upto 3.58V at 15V Input Supply

Figure 56 shows the gate and switch node signals at 20MHz switching frequency. The ringing is significant due to high frequency operation. The HS and LS gate signals were captured with the GND spring probe to minimize the ESL of the GND probe of the oscilloscope. The switch node is captured with the large GND probe connection and hence the ringing is observed for this captured waveform. The high frequency ringing at the gate signals could be minimized by reducing the switching frequency (as shown in Figure 57), or by using reducing dv/dt of the signals by increasing the gate resistor, or by introducing large decoupling capacitor at the V_{DD} of the driver supply [34, 40]. The below measurement results indicates the approximate limit of the fabricated IC in terms of the maximum achievable switching frequency. The glitch in the high side gate waveforms at 20MHz is due to the Forced Continuous Conduction Mode (FCCM) in light load condition. The high side gate signal is switching between 0V and 13V (5V + 8V Vin signal) due to bootstrap, and the low side gate signal is switching between 0V and 5V with the switch node signal swing from 0V to 8V (Vin) average value.

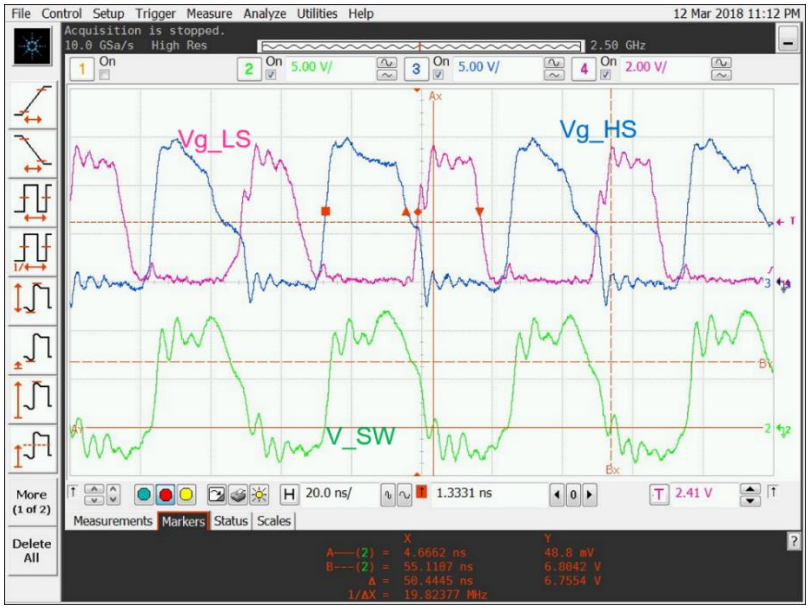

Figure 56: HS, LS Gate Signal and Switch Node Waveforms at 20MHz Switching Frequency

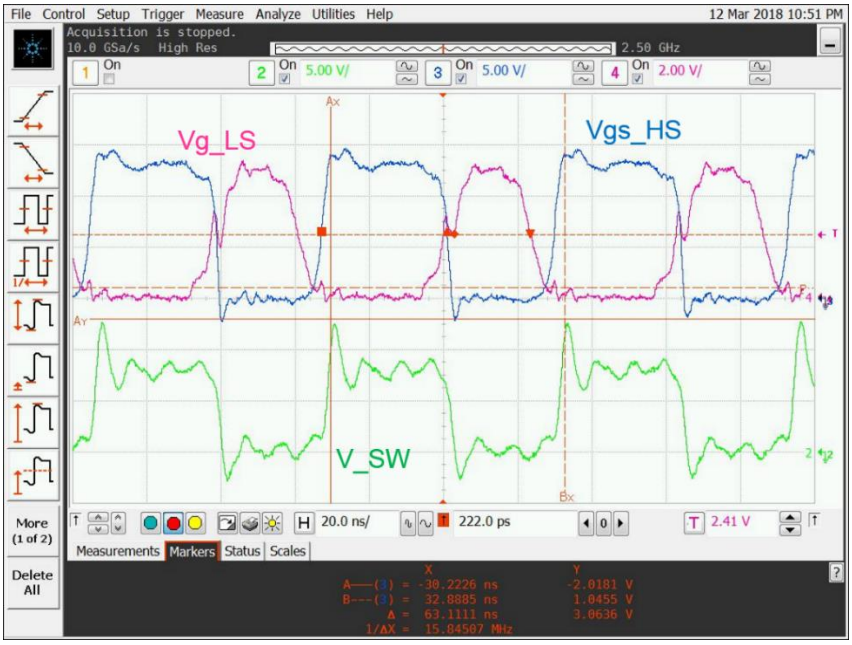

Figure 57:HS, LS Gate Signal and Switch Node Waveforms at 15.8MHz Switching Frequency

Figure 58 shows the Vout ripple in AC coupling mode to be at 93.5mV at 20MHz switching frequency with the boundary condition of the inductor current average at 335mA (output load). Figure 59 shows the inductor current in boundary conduction mode and the Vout ripple in AC coupling mode for 15.8MHz switching frequency. The observed ripple is periodic with peak to peak amplitude at 200mV. Figure 60 shows the behavior of Vout overshoot with the step load of 2A. The measured dip is high at 450mV due to the converter operating in open loop condition. Figure 61 shows the Vout settling time at power-on which is 21.2ms. This is due to 176µF of output capacitor. Figure 62 shows the switch node waveform at 15V input voltage of the converter. This condition is under light load of 350mA load current which shows the Forced Continuous Conduction Mode (FCCM) of operation. This is due to the drain to source voltage of the LS GaN, which is positive under FCCM mode.

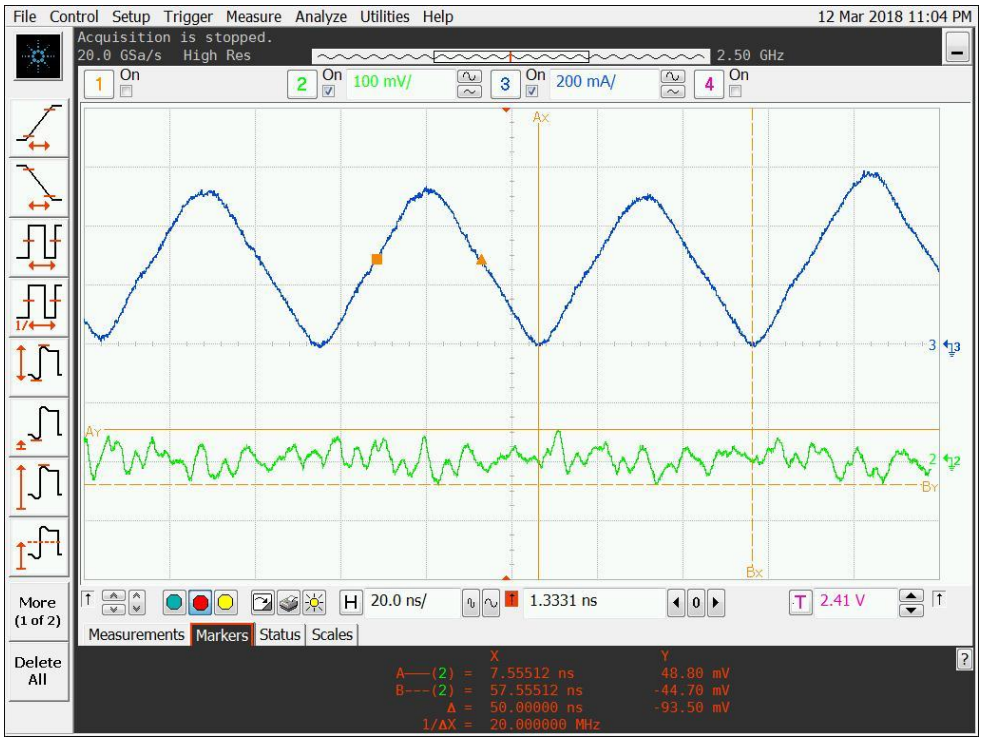

Figure 58: Inductor Current and Vout Ripple in AC Coupling Mode at 20MHz

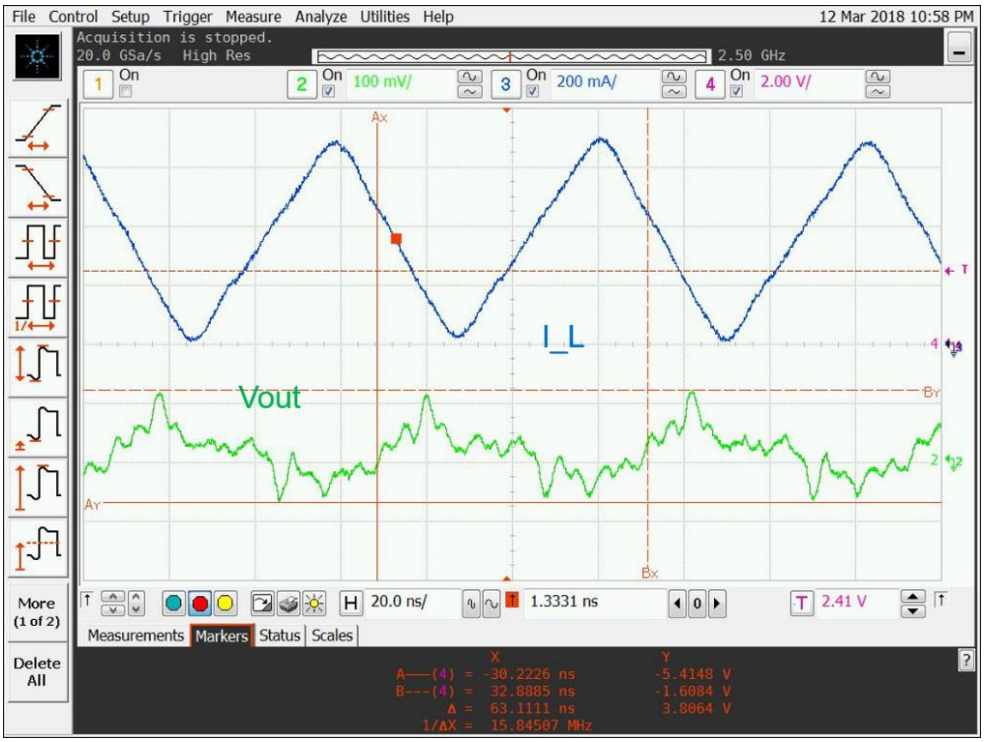

Figure 59: Inductor Current and Vout Ripple at 15.8MHz Switching Frequency

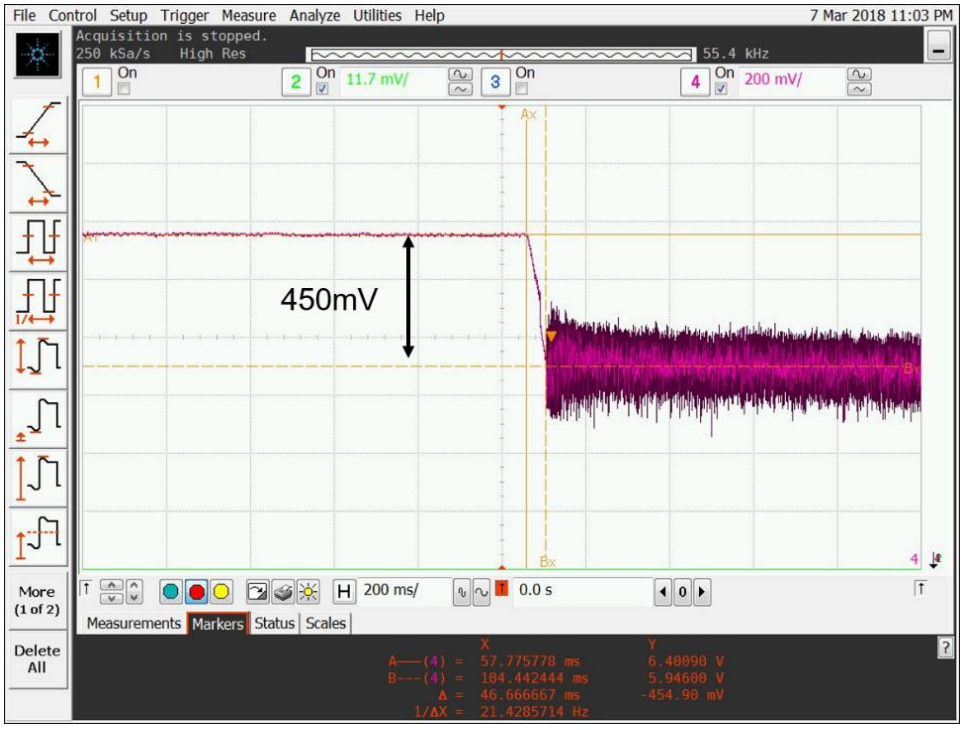

Figure 60: Vout Behavior for 2A Step Load at the Output

Figure 61: Vout Settling Time as 21.2ms During Start-Up in Open Loop

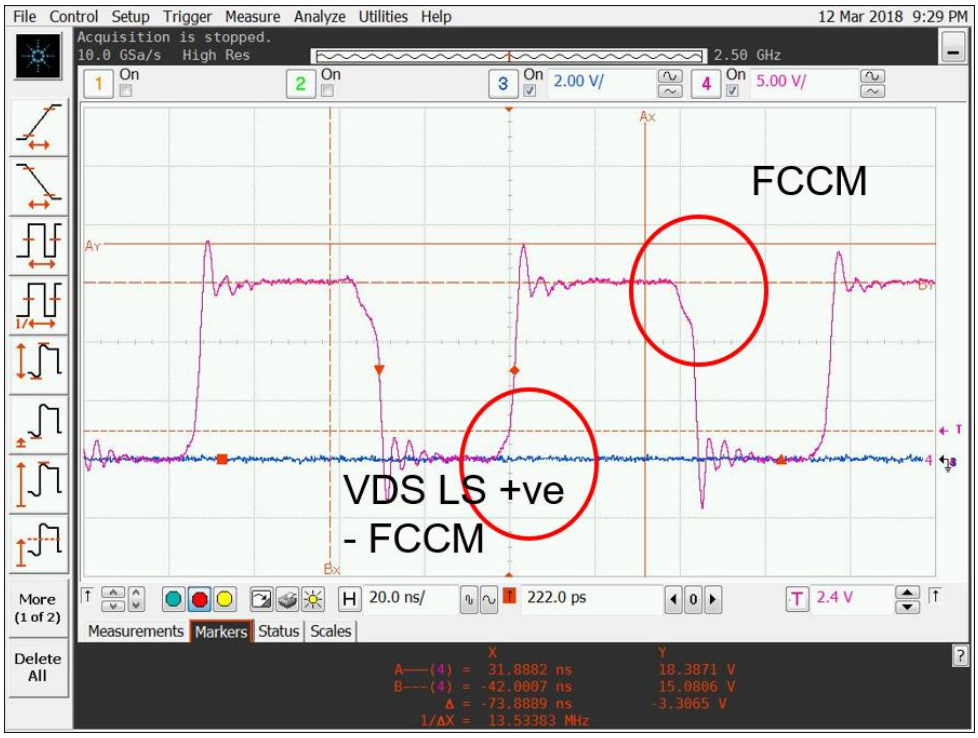

Figure 62: Switch Node Waveform Indicating the FCCM Mode of Operation at Light Load Conditions

5.3 18V to 5V Linear Regulator Measurement

The 18V to 5V LDO is the high voltage linear regulator used for driver supply to drive the gate of the GaN power stage. Figure 63 shows the load transient on the 18V to 5V LDO which is required as the input to the driver supply for switching signals. This LDO is capable of ~400mA average current for the driver required for switching the gate signals at 20MHz of switching frequency. The load transient to 400mA shows undershoot/overshoot up-to 161mV. The line transient test was performed for this LDO by varying the input voltage from 10V to 18V and measuring the output of the LDO through a high precision digital multimeter. The line and load transient measurement results shows the regulation to be at 3% for this LDO, which is acceptable for the driver supply. Figure 64 shows the line regulation for 18V to 5V LDO with the variation in the input supply from

10V to 18V. The measurements verify that the LDO accurately regulates the output voltage to 5V with 3% error.

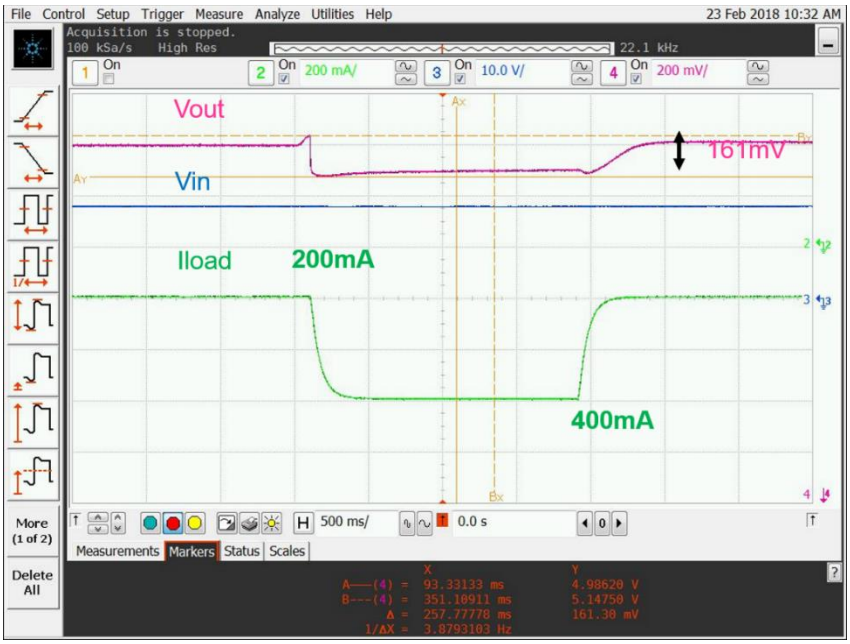

Figure 63: Load Transient for 18V to 5V LDO

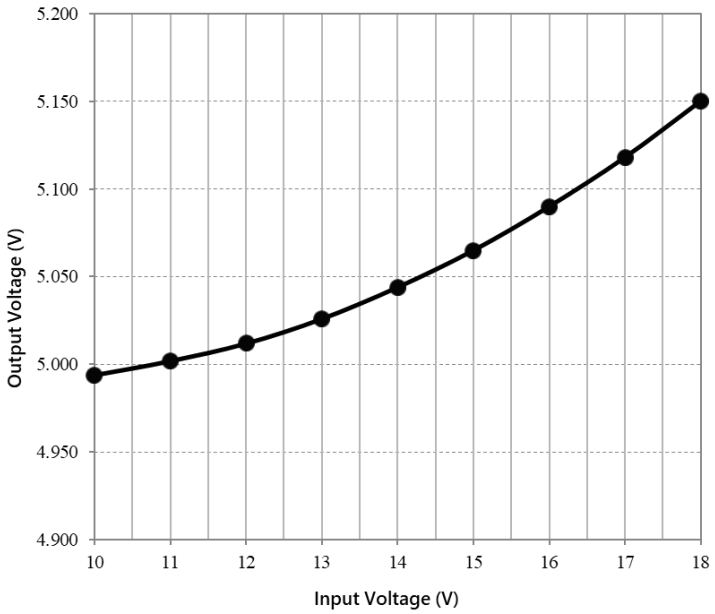

Figure 64: Line Regulation of the HV LDO

Table 6 highlights the performance comparison of the measured and fabricated controller and driver with the existing best-in-class works [12, 13, 14, 44]. The presented solution demonstrates highest reported conversion ratio for 20MHz switching speeds and highest load current of 10A.

Table 6: Performance Summary of the Fabricated IC with the Existing Work

Parameters	**ISSCC -15 (Min Kyu Song et.all)**	**CERN's work (F. Faccio et.all)**	**Trans. on Power Elec.-16(F. Neveu et. all)**	**JSSC-17 (E. Alkimi et. all)**	**This work**
V_{in} (V)	15	12 (5-12)	3.3	8	18
V_{out} (V)	6	5 (0.6-5)	2.4	1.0	5
Architecture	Multi-phase (4)	Single-phase	Single-phase	Multi-phase (3)	Single-phase
Power-stage switching devices	Si Process 0.35µm BCD	Si Process 0.35µm LDMOS	Si Process 40nm CMOS	Si Process 180nm CMOS	Si Process 0.35µm CMOS
Max. f_{sw} (MHz)	20	3	100	40	20
I_{max} (A)	1.2	4	0.3	0.198	7
Peak η (%)	78% @1.2A, 20MHz	88% @ 2A, 1.8MHz	91.5% @ 0.15A, 100MHz	76% @ 0.051A, 40MHz	81% @ 7A, 15 MHz
ΔV_{out}(%)	N/A	6.5	N/A	N/A	2
Die Area (mm^2)	6	25	0.048	8	8.32

6 CONCLUSION AND FUTURE WORK

Three power converter board implementations and an integrated circuit controller with driver solution were presented and the performance was verified through hardware measurements to meet the >80% efficiency specification at high (20MHz) switching frequency and worst case loading conditions. The layout area of the entire chip including the drivers and regulators is ~3mm x 3mm, where the driver occupies ~30% of the total area. Therefore, it has been demonstrated that the presented solution significantly reduces physical form factor (size) from state-of-the-art solutions by providing an integrated solution for high frequency power converters. The following points can be concluded based on this research:

1. Design and measurement of three discrete power converter architectures.
2. Power stage architectures compared with respect to efficiency, size and load current.
3. GaN implementation exhibits high efficiency compared to state-of-art silicon integrated solutions.
4. Demonstrated solutions with 24V input to 5V output conversion at 10A load current capability.
5. Integrated high current buck converter at 20 MHz switching frequency was designed, fabricated and measured. The controller and drivers are implemented in a 0.35um CMOS process.

The future work related to this research can be summarized as follows:

1. Develop reconfigurable capabilities: frequency selection, dead-time, soft-start adjustment. Upgrade to a customized output air-core inductor to achieve optimal converter efficiency and reduced volume requirements.
2. Add radhard redundancy at system and circuit levels with techniques such as triplication and voting for both analog and digital blocks.
3. Update the off-chip passive components for control-loop compensation to a fully on-chip compensation. Improve performance of non-BJT bandgap reference, and on-chip voltage regulation options for a stable multiple voltage supply.
4. Add protection schemes such as under-voltage lockout (UVLO), over-current protection (OCP), over-temperature protection (OTP), output voltage protection, adaptive dead-time control, etc to the next prototype IC tape-out.
5. Improve circuit performance, such as sink/source current capability and driving transition for output driver, closed-loop response stability and control band-width.

Additionally, the most common architectures for DC-DC converters implement hard-switching, where the operation relies on the assumption that voltage and current are never simultaneously passing through the active device(s). With increased switching speeds, more effort has been placed into dead-time control algorithms and resonant converters, which force zero-voltage or zero-current switching (ZVS/ZCS), to notably increase the converter's power stage efficiency. These methodologies can be employed in any of the switching converter architectures to further increase the converter's efficiency.

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