Monitor-Based In-Field Wearout Mitigation for CMOS RF Integrated Circuits

by

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ABSTRACT

Performance failure due to aging is an increasing concern for RF circuits. While most aging studies are focused on the concept of mean-time-to-failure, for analog circuits, aging results in continuous degradation in performance before it causes catastrophic failures. In this regard, the lifetime of RF/analog circuits, which is defined as the point where at least one specification fails, is not just determined by aging at the device level, but also by the slack in the specifications, process variations, and the stress conditions on the devices. In this dissertation, firstly, a methodology for analyzing the performance degradation of RF circuits caused by aging mechanisms in MOSFET devices at design-time (pre-silicon) is presented. An algorithm to determine reliability hotspots in the circuit is proposed and design-time optimization methods to enhance the lifetime by making the most likely to fail circuit components more reliable is performed. RF circuits are used as test cases to demonstrate that the lifetime can be enhanced using the proposed design-time technique with low area and no performance impact. Secondly, in-field monitoring and recovering technique for the performance of aged RF circuits is discussed. The proposed in-field technique is based on two phases: During the design time, degradation profiles of the aged circuit are obtained through simulations. From these profiles, hotspot identification of aged RF circuits are conducted and the circuit variable that is easy to measure but highly correlated to the performance of the primary circuit is determined for a monitoring purpose. After deployment, an on-chip DC monitor is periodically activated and its results are used to monitor, and if necessary, recover the circuit performances degraded by aging mechanisms. It is also necessary to co-design the monitoring and recovery mechanism along with the primary circuit for minimal

performance impact. A low noise amplifier (LNA) and LC-tank oscillators are fabricated for case studies to demonstrate that the lifetime can be enhanced using the proposed monitoring and recovery techniques in the field. Experimental results with fabricated LNA/oscillator chips show the performance degradation from the accelerated stress conditions and this loss can be recovered by the proposed mitigation scheme.

Dedicated to my beloved parents and family

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CHAPTER 1

INTRODUCTION

1.1. Background

Integration of RF/analog and digital subsystems is considered as the way to meet stringent specifications in terms of performance, power consumption, and form factor. These integrated systems consist of high performance mixed-signal designs with analog/digital blocks and sensitive RF frontends. In order to meet the ever increasing performance demands, digital circuits necessitate the use of advanced digitally-tuned processes. However, these processes are inherently less stable in terms of variations and are subject to wearout mechanisms in transistor parameters, which can cause malfunction in analog circuits long before the underlying devices are deemed to catastrophically fail [1, 2]. Hence, it is essential to ensure that a circuit operates with respect to all specifications to meet lifetime requirements at specified use conditions.

While in-field degradation due to aging for digital circuit is a continuing challenge, concerns for analog/RF circuits have scarcely been researched. In the context of analog and RF circuits, reliability is defined as the ability of a circuit to conform to its specifications over a specified period of time under specified conditions [3]. Several researchers have focused on analysis of aging degradation in various analog/RF circuits. These mechanisms include hot carrier injection (HCI) [3-5], time dependent dielectric breakdown (TDDB) [6-8], negative bias temperature instability (NBTI) [9-11], and electromigration (EM) [12], [13]. Of these mechanisms, HCI and NBTI are determined to

be the most critical for deep submicron designs [2][10]. As CMOS technology scales to the nano-meter range, the threshold voltage shift due to increased internal electric fields becomes more prominent on transistor. Major mechanisms of the circuit aging as HCI and NBTI eventually result in an increase in the absolute threshold voltage and reduction in device current, thereby degrading circuit performance such as speed, gain, and data stability. An analysis of the performance of CMOS LC-tank oscillators under HCI stress is presented in [5], [14]. The authors conclude that HCI causes increased phase noise because of the decrease in the oscillation amplitude due to the degraded NMOS transistors. In [11], various analog circuits are simulated for NBTI reliability and their degradation is analyzed. The authors conclude that when these circuits are implemented using fine-geometry digital processes, performance degradation starts within the first few months of device use and gradually accelerates. In [15], the authors develop a time scaling model to relate experimental data from accelerated aging studies to nominal operational use.

In order to assess the reliability risk on silicon for RF circuits experimentally, aging studies have conducted on a commercial RF amplifier (MAX1472). This amplifier was subjected to a temperature of 120°C and 10% supply voltage overdrive to enhance the effects of aging degradation. Fig. 1.1 shows the degradation in the amplifier gain with respect to stress time. After about 60 hours of continuous stress, the gain of the amplifier has dropped by 0.5dB, which is a significant loss. Under nominal supply voltage, 60 hours of stress time is projected to 5400 hours of continuous operation, which may make the device parametrically fail within the first 7 months of deployment. This experiment

demonstrates that analog/RF circuits are just as susceptible to aging related failures as digital circuits.

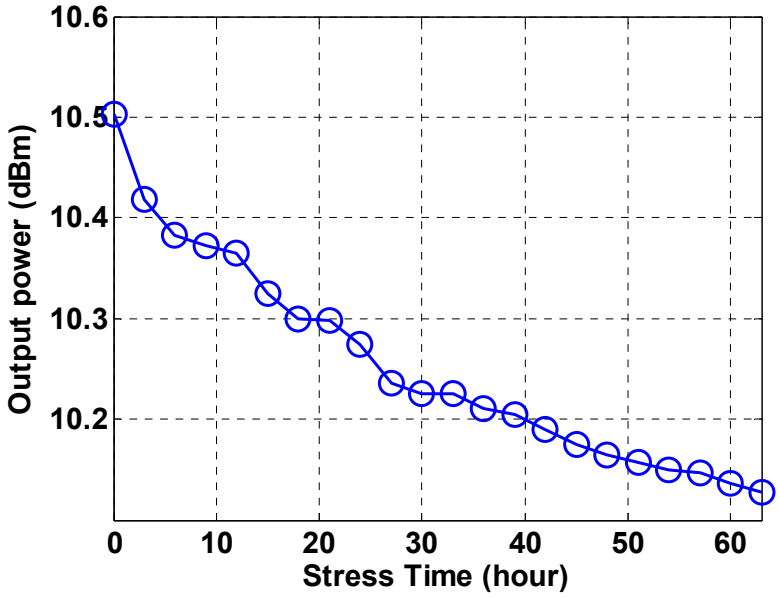

Figure 1.1. Performance Degradation of RF Amplifier for Reliability Study.

With mounting evidence on the impact of device aging for analog circuits, many techniques have been developed to analyze circuit reliability at design time [14], [16-18]. Design-time improvements at the circuit-level and at the layout level, such as using higher than minimum length, can ensure that statistically, most manufactured devices will not experience significant degradation in their parameters. For example, NBTI and process variations are exacerbated with technology scaling based on Pelgrom's law [19], [20]. In digital circuits such as SRAM, by using larger devices, the delay spread due to process variations can be reduced as a function of device dimension ($\propto 1/\sqrt{LW}$, where L is gate length and W is the gate width), and the impact of NBTI on circuit reliability also can be reduced. However, aging is a random process and cannot be ruled out even with

design-time adjustments. More importantly, there are no known techniques to identify devices that will experience faster aging during operation time. Wholesale use of reliability enhancement techniques at the device level is also counterproductive in terms of performance and area [21]. Hence, an in-field mechanism to monitor and mitigate the effects of device aging is needed.

While prior work in RF reliability addresses the analysis of aging phenomena on RF circuits, there has been little to no work to make use of this knowledge in the field as the device ages. Since aging results in continuous degradation after the device is deployed, it can be detected by monitoring the circuit performance. Once it is known that aging mechanisms have started causing noticeable degradation, remedial action can be taken by introducing compensation circuits. As a result, it is necessary to monitor the degradation of the circuit while the circuit is in the field.

Unfortunately, direct monitoring of RF/analog circuit performance is often not feasible since many specifications, such as noise, third order input intercept, or S-parameters, cannot be measured in the field. Therefore, alternative measurement mechanisms need to be developed for in-field monitoring that relies on information from easy-to-design circuits. This monitoring strategy requires establishing a strong correlation between the current and future status of the circuit and the monitor response. Existing work for design-for-reliability focuses on compensating for PVT variations [22]-[24]. However, they require significant increase in design area and time to incorporate for self-compensation.

1.2. Reliability Models for CMOS Transistors and Analog/RF Circuits

Of the various mechanisms of degradation, HCI and NBTI have been identified as the most detrimental to the device operation for deep sub-micron technologies. In this section, the aging mechanisms are reviewed, and a simulation and analysis method for these aging mechanisms under process variations and mismatch is presented.

1.2.1. Hot Carrier Injection (HCI)

Time-dependent aging effects will cause a shift of transistor parameters as a function of time. Hot-Carrier injection (HCI) is one such degradation mechanism mainly affecting N-type MOSFETs. During hot carrier stress caused by high electric field near the drain region, either an electron or a hole at the end of the drain junction gains sufficient kinetic energy to overcome the potential barrier, and then migrates toward the oxide silicon surface. These hot-carriers can cause both interface state generation and charge traps which increase the leakage substrate current and decrease drain current. After hot carrier stress, the transistor characteristics, such as threshold voltage and channel mobility, may shift, changing the characteristics of the device.

The impact of HCI effect is more pronounced for RF/analog circuits due to the strong dependency of performance parameters on the threshold voltage of critical transistors. Effects of HCI on the RF characteristics of single N-type MOSFET and RF circuits have been studied [8].

HCI can be physically shown as the generation of charges in the region close to the Si/SiO2 interface. Charge generation is localized to drain region making HCI to be a

strong function of drain-source (lateral field) voltage, V_{ds}. For a given stress time and assuming interface trap generation for HCI occurs at drain end, it is possible to derive the closed form equation for threshold voltage V_{th} shift of a device under HCI stress [10][26]. For example, for a constant gate voltage increasing drain voltage results in higher V_{th} shift. At higher gate-source voltage V_{gs} for thin oxide devices, the electric field across oxide increases which causes higher scattering of electrons for the same drain voltage. Thus, HCI depends both on V_{ds} and V_{gs}.

The set of analytical models governing the HCI effect with respect to the stress time, t, is given in Table 1.1. E_{OX} is the vertical electric field (due to V_{gs}), E_m is the lateral electric field, φ_{it} is the minimum energy in eV required by hot electron to create impact ionization, λ is the mean free path, E_0 is the activation energy, K is the fitting parameter and n is the time exponent. The model parameters can be characterized for a given technology node and implemented in a circuit simulation environment. This model has been experimentally verified for a multitude of bias conditions [10][27].

$$\Delta V_{th\_HCI} = \frac{q}{C_{ox}} K \sqrt{Q_i} \exp(\frac{E_{ox}}{E_0}) \exp(-\frac{\varphi_{it}}{q\lambda E_m}) t^n$$

SUMMARY OF PARAMETERS IN AGING MODELS

E_m	$(V_{ds} - V_{dsat}) / l$	E_{ox}	$(V_{gs} - V_{th}) / t_{ox}$
E_0 (V/nm)	0.8	Q_i	$C_{ox}(V_{gs} - V_{th})$
λ (nm)	7.8	K ($nm \cdot C^{-0.5}$)	1.7×10^8
δ	0.5	φ_{it}	3.7

Table 1.1. Summary of HCI Aging Model.

1.2.2. Negative Bias Temperature Instability (NBTI)

The negative bias temperature instability (NBTI) occurs in PMOS devices when a negative bias is applied to the gate or equivalently, when the gate is grounded and a positive bias is applied to the source/drain. NBTI is caused by the interface traps and fixed charge under negative gate voltage bias and accelerates when the operation temperature increases. In other words, NBTI is caused by the reaction-diffusion (R-D) mechanism, where holes initiate the breaking of Si–H bonds (reaction phase) at the silicon substrate/oxide interface by a combination of electric field and temperature. The broken hydrogen species diffuse away from the interface into gate oxide and the polysilicon gate (diffusion phase) and thus, interface charges are generated [28]. Therefore, NBTI leads to a shift in the threshold voltage, which is proportional to the interface trap generation. This threshold voltage shift decreases the drain current under

constant voltage bias. For current bias, the threshold voltage shift will result in increased gate-to-source bias voltage. Hence, if a transistor is biased through a current mirror, the mismatch between the mirror transistor parameters is the major source of degradation.

NBTI effects can be categorized by two models depending on the stress conditions, namely, static NBTI and dynamic NBTI. Static NBTI is experienced under constant stress, as in the case of DC bias. This form of NBTI degradation cannot be recovered. For dynamic NBTI, the device undergoes AC operation and experiences positive and negative stresses, which generates a cycle of degradation/recovery. Finally, the threshold voltage degradation due to NBTI at a time t can be obtained by $\Delta V_{th\_NBTI} = C_{NBTI} \cdot t^{n'}$ where C_{NBTI} is a parameter depends on process variations, voltage, and temperature. n' is the time exponent [10], [26].

Based on this stress/recovery cycle, one might conclude that NBTI is not a big issue for oscillators where voltage swing is comparable to DC bias. However, the large swing is only experienced by the coupled transistors, and is not symmetric.

1.2.3. Electromigration (EM)

Shrinking metal thickness leads to higher current density flowing through interconnects, exacerbating electromigration (EM) effects on circuit performance and reliability. Even though some new materials with better immunity to EM failures have been used as on-chip interconnects to replace Aluminum (Al), EM is still a reliability concern. EM is the process of mass transport caused by momentum transfer between conducting electrons and metal atoms. During electromigration, the metal atoms move in the direction of electron flow along the grain boundaries. Over time, enough material

may move resulting in significant change in the metal resistance. As in the case of HCI and NBTI, research has focused mostly on catastrophic failure, and the well-established Black's model is used for calculating MTTF [29]:

$$MTTF = \frac{A}{J^n} \exp(\frac{E_a}{kT}) \tag{1.1}$$

where A is a material parameter dependent on structure and geometric properties of the conductor, n is the current exponent factor, J is the current density, E_a is the activation energy, k is the Boltzmann constant, and T is the temperature. While most EM research has focused on digital circuits and catastrophic failure modes [30][31], studies show that EM results in continuous increase of trace resistances as soon as current starts flowing through the metal [32][33].

1.2.4. Process Variation

Parametric variations present one of the toughest challenges in reliability analysis and modeling for RF/analog circuits [17], [18], [21]. Variations exist both in physical process parameters, such as threshold voltage, and in degradation model parameters, such as the trap generation energy. Hence, it is imperative to take process variations into account. Process variations are classified as die-to-die variations and within-die (mismatch) variations [34][35]. Die-to-die variations, which shift parameters of all devices on the same die in the same fashion, are larger compared to mismatch variations, which affect each device randomly. Traditionally, die-to-die variations have been the main concern in CMOS digital circuit designs. However, as CMOS technology scales down, within-die variations are a growing concern for maintaining the specified

performance [36]. Since analog/RF circuits are very sensitive to mismatch, both die-to-die and mismatch variations need to be taken into account. There have been literature works in the past which considered process variations and the aging in RF/analog circuit simultaneously at the simulation level [1], [18], [37]. However, mismatch in degradation parameters is typically considered negligible. In this dissertation, a hybrid simulator/model based technique is used to evaluate random circuit instances and a mismatch in both process and degradation parameters is included in the analysis.

1.3. Reliability Simulation at Circuit Level

In order to analyze the effect of the failure mechanisms on circuit reliability, a simulator is needed. However, most reliability simulators that are commercially available are not amenable to analog operation where devices undergo different bias/swing conditions. In order to identify the reliability hotspots, it is required to be able to turn the degradation on or off for each transistor or transistor pair. In [37], a reliability simulation framework is presented that integrates variability with reliability by employing transistor drain current surrogate models. A transistor-level circuit simulator is employed to measure the degradation of performance parameters of fresh and aged circuits [38-40]. The proposed method uses a similar hybrid methodology by adapting a sub-circuit model of the threshold voltage shift of the aged transistors [41]. The analytical model of each aging effect (HCI of NMOS and NBTI of PMOS) is implemented to a Verilog-A simulator and modeled as a voltage-controlled voltage source (VCVS) in series to the gate of the aged transistor as illustrated in Fig. 1.2. In each time step during a transient circuit simulation, the threshold voltage shift is determined based on the current bias

conditions of a transistor and degradation parameters of the aging effect. Finally, this VCVS-based aging model is inserted into SPICE environment for each NMOS/PMOS transistor. Since the model is calibrated for various bias conditions during the operation, the sub-circuit model accurately captures the aging degradation. The complete sets of analytical models of aging effects are summarized in [10], [42]. These model coefficient can be easily characterized for a given technology and implemented in the circuit simulation environment. The major difference in this work is that a mismatch between aging parameters of various transistors is taken into account during circuit simulation environment.

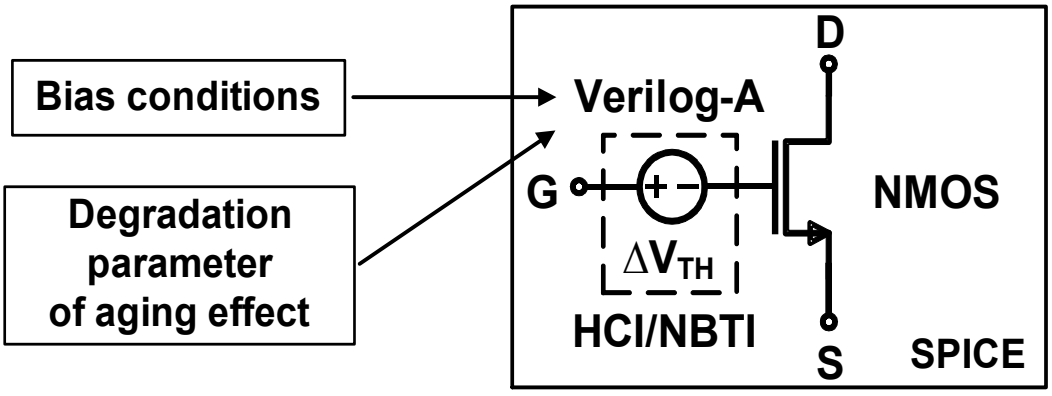

Figure 1.2. Sub-circuit Implementation of Aging Effect Model Using Verilog-A.

1.4. Outline of Dissertation

In this dissertation, RF BIST methods for advanced RF transceiver such as RF polar transceiver and RF phased array are proposed. In addition, robust amplitude and gain measurement for RF BIST application are proposed and discussed.

In chapter 2, a systematic approach to design on RF circuit with expected lifetime as a specification parameter is proposed. In the proposed framework, parametric aging effects for RF circuits are analyzed and the overall lifetime is determined. An algorithm to determine reliability hotspots in the circuit and design-time optimization methods to enhance the lifetime by making the most likely to fail circuit components more reliable are presented. Based on the information that has been collected from simulations, it is possible to enhance the lifetime of the circuit without changing its performance if reliability is taken into consideration at design time.

In chapter 3, a comprehensive systemic methodology for co-designing CMOS LC oscillators together with in-field monitoring and recovery mechanisms to enable aging mitigation with minimal performance and area overheads. The proposed technique includes hotspot identification to determine the weakest component, monitor/reconfiguration network design, and an algorithm to automatically swap the aged transistor with a new one to enhance the lifetime. In order to demonstrate the proposed technique, cross-coupled LC oscillator circuits are used for simulations and a CMOS class-C LC oscillator is fabricated in 180nm IBM process for experimental results.

In chapter 4, a methodology for enhancing the lifetime of RF circuits in the field using low-impact circuit level monitor and recovery techniques. The particular aging mechanism focusing on is hot carrier injection (HCI) although the proposed method

would work with any aging mechanism that can be modeled to enable simulations. Since the monitoring circuit is also prone to process variations, the monitoring mechanism is designed as a relative measurement, based on the amount of change in the monitor circuit output, rather than the absolute value. In order to demonstrate the concepts of reliability analysis and monitor and recovery circuit design, a generic LNA architecture is implemented as a case study.

CHAPTER 2

DESIGN-TIME RELIABILITY ENHANCEMENT USING HOTSPOT IDENTIFICATION FOR RF CIRCUITS

2.1. Simulation Framework for Aging Mechanisms

To develop a design-for-reliability approach for RF circuits, a framework for simulating aging effects is necessary. While commercial tools exist to simulate for digital circuits, they typically report an overall lifetime in terms of a catastrophic failure, mean-time-to failure (MTTF). Therefore, an aging simulation method that is based on SPICE is developed to:

1) Analyze each circuit component and each aging mechanism independently and

2) Evaluate parametric degradation in specifications and determine lifetime.

To enable these simulations using existing tools (e.g., SPICE), each circuit component model is modified with an equivalent that changes circuit parameters with respect to the amount of degradation. The degradation amount with stress time for pre-silicon simulation is determined based on well-established reliability models [10], [27] and the current state of the circuit performance. In this proposed simulation framework, the aging effects of HCI, NBTI, and EM are included.

Similar to [40], the proposed simulation framework uses improved circuit components to model the degradation effects. However, [40] aims to analyze the effect of degradation on the circuit when all circuit components are under stress. This approach does not provide the necessary information for hotspots identification. Moreover, device-to-device mismatch for process or degradation parameters has not been previously

considered. Mismatch results in unequal degradation in different transistors and has a profound effect on analog circuit performance. In the proposed framework, it is necessary to pay particular attention to the following issues:

1) Circuit components are subject to both die-to-die and within-die (mismatch) variations.

2) Degradation model parameters are also subject to mismatch variations among circuit components.

3) Each circuit component is subject to differing levels of stress due to bias conditions and dynamic signal behavior.

4) Circuit bias conditions change over time; simulations based on an initial bias point are unreliable.

Fig. 2.1 shows the flow of the reliability simulation approach. Initial bias voltages and currents are determined via simulations. For small-signal operation, degradation parameters (e.g., threshold voltage) can be determined using dc bias. For large-signal operation, dynamic signals also need to be considered. An initial time step (e.g., N months) is used to calculate degradations in circuit component parameters. The circuit is simulated again to determine the change in dc operating point. If the shift in dc point is above a tolerable threshold (e.g., $> \alpha$ mV), the time step is reduced and the prediction is repeated. Otherwise, the circuit is simulated for performance evaluation (e.g., gain and phase noise). With this simulation framework, it is possible to simulate the aging effect for a single or multiple components.

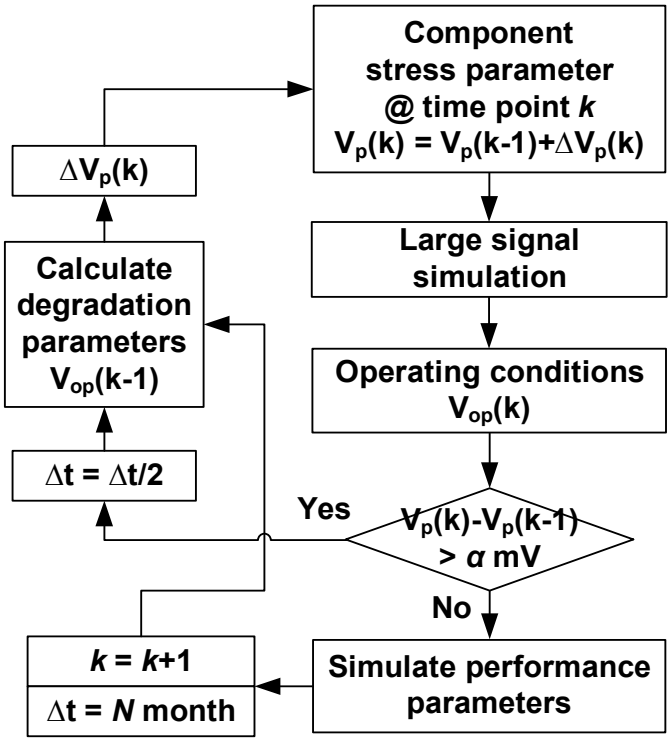

Figure 2.1. Flow of the Reliability Simulation Approach.

2.2. Design-Time Optimization Methodology

After analyzing the reliability impact of aging mechanisms on the circuits in several steps, the reliability simulation can concentrate on each circuit component and determine at what point it will cause a specification failure, assuming that it is the only contributor to degradation. This proposed method can determine the reliability hotspots and concentrate design optimization efforts on these circuit components. If the projected lifetime is not satisfactory, the most dominant lifetime-limiting component is modified so as to increase its reliability.

Fig. 2.2 shows an overview of the proposed methodology. The first step in the process is to analyze the aging effects on circuit performances using the analytical models of each aging effect. One aging effect for one device is activated at a time to isolate the hotspot device and the cause of the degradation. The stress time is gradually increased with an adaptive time interval and the aging impact on circuit specifications is analyzed. This information combined with the circuit specifications yields a certain time point at which the specification will fail. The sensitivity of circuit specifications with respect to each circuit component degraded by aging effects differs. Due to different sizes and operating points, this profile will be different for each circuit component. Therefore, each circuit component will cause a distinct failure time for each specification.

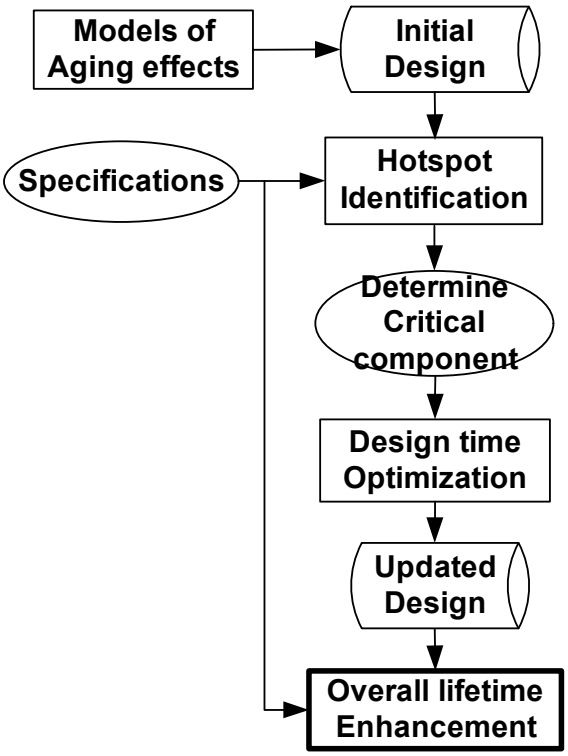

Figure 2.2. Flow of the Proposed Design-time Optimization Method.

Note that at this point, the method focuses on one circuit component at a time to determine the lifetime-limiting factors. The actual failure point of the circuit will differ from this first-level sensitivity study, since all circuit components simultaneously age, albeit at a differing rate. This process iteratively go through each circuit component and track the failure time of the each circuit specification. Once all the failure times are collected, it is possible to decide the most vulnerable component to aging effects. Component-centric lifetime enhancement can be done using established techniques by adjusting the component parameters. Clearly, once one component is modified, circuit specifications shift, thus requiring modifications on other components. Hence, circuit modifications need to be done incrementally to avoid ping-pong behavior of the optimization process. Moreover, a circuit component is not modified to enhance the lifetime to beyond what is limited by another circuit component.

2.3. Case Studies

2.3.1. Low Noise Amplifier with HCI and EM Analysis

A cascode low noise amplifier (LNA) is used as an example to demonstrate the RF performance degradation due to HCI and EM effects. Fig. 2.3 (a) shows a narrow-band LNA where the transistors are enhanced to account for degradation effects [43]. The circuit is designed with the following specifications:

[S21 > 17 dB, S11 < -10 dB, S22 < -10 dB and NF < 1.5 dB] @ 1.5 GHz.

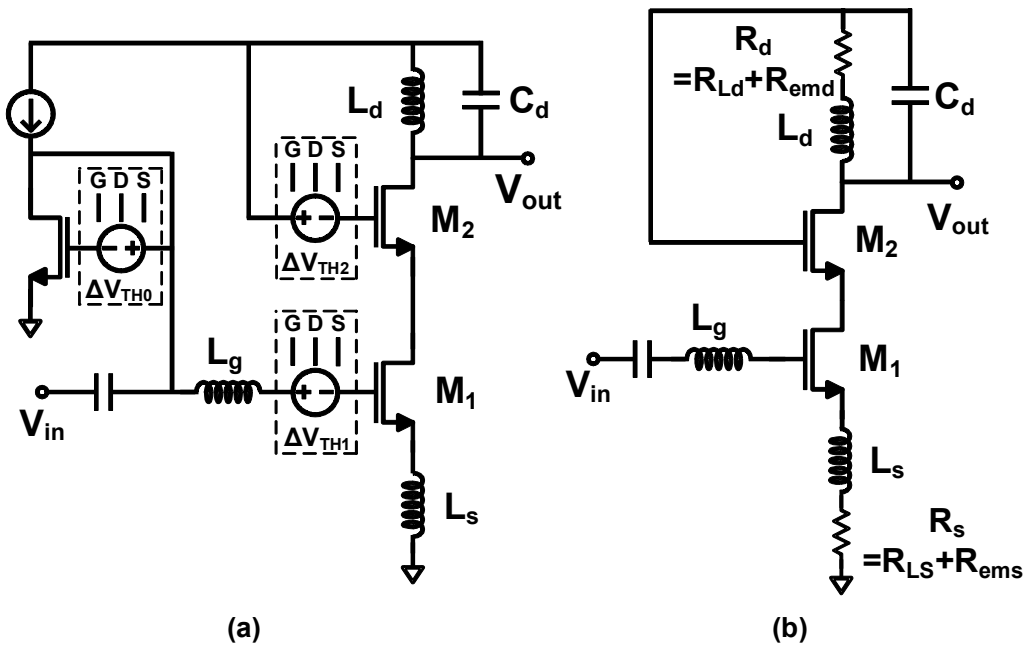

Figure 2.3. (a) HCI Analysis and (b) EM Analysis of Cascode LNA.

Reliability simulations of the LNA due to HCI effects are performed using the framework outlined previously over three years of stress time. Time-varying threshold voltage shift of HCI is modeled as a dependent voltage source with input node voltages. These node voltages are connected to gate, drain, or source of the device and updated after each time step to obtain more accurate actual simulation responses. In this design example, there are three voltage sources $\Delta V_{TH0,1,2}$ at the gate of each nMOSFET to consider the effects of threshold voltage shift. Degradation profiles of the LNA specifications, such as S-parameters and noise figure (NF) are shown in Fig. 2.4. Due to the degradation of threshold voltage, it reduces the drain-source current of transistor and hence its transconductance g_m, thus resulting in degradation in specifications [43]. From the simulations, it is observed that the circuit is likely to fail input return loss (S11), gain (S21) and NF between 1 and 3 years of lifetime, which is generally not acceptable.

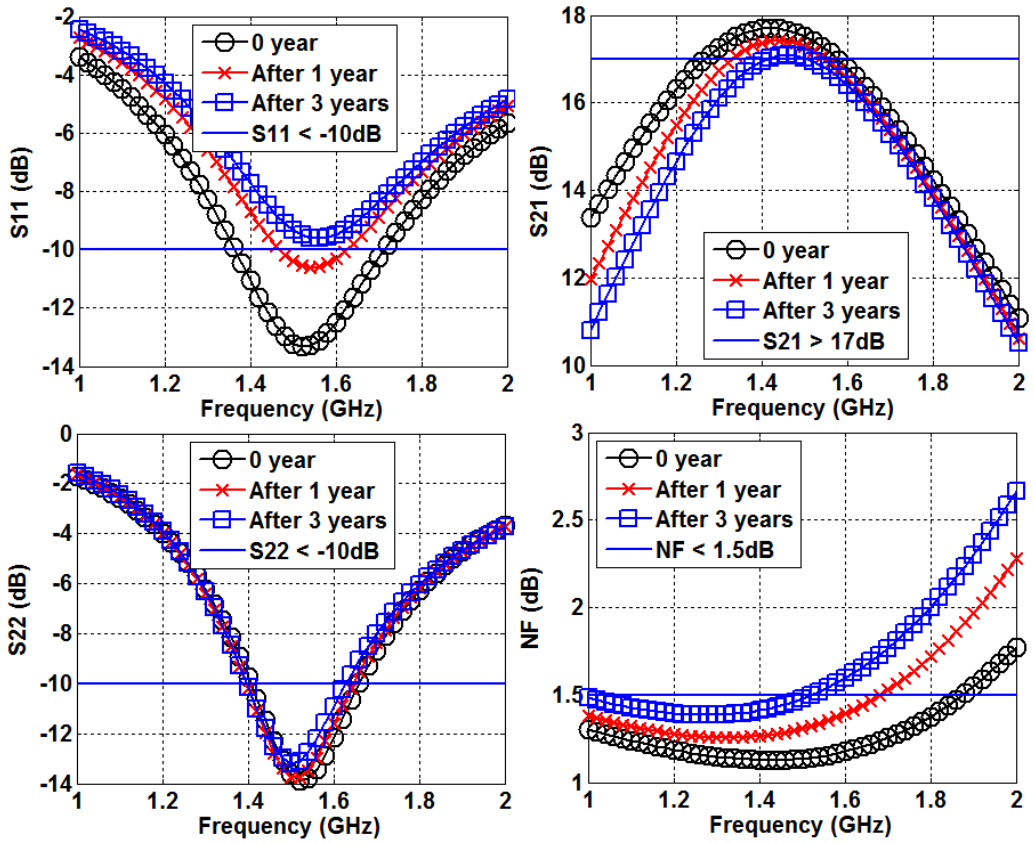

Figure 2.4. Performance Degradation Due to HCI Effect in Cascode LNA During One and Three Years of Operation at Room Temperature.

To analyze the reliability impact of EM on the LNA, it is important to concentrate on conductors (via and inductor) as shown in Fig. 2.3 (b). Both on-chip inductors, L_d and L_s are implemented using metals. The inductor Q is modeled using the resistors R_{Ld} and R_{Ls}, in series with ideal inductors, L_d and L_s, respectively. The inductor EM model R_{emd} and R_{ems} are additional resistances in series with R_{Ld} and R_{Ls}. Since there is no dc current into the gate of the input transistor, there is no EM effect on L_g. EM results in a slow linear change in the resistance of the metal line [33]. LNA S-parameter degradation due to increasing line resistances within three years is shown in Fig. 2.5. This result shows

that the circuit is projected to fail the gain specification within eight months (~20×10^6 s) of its deployment.

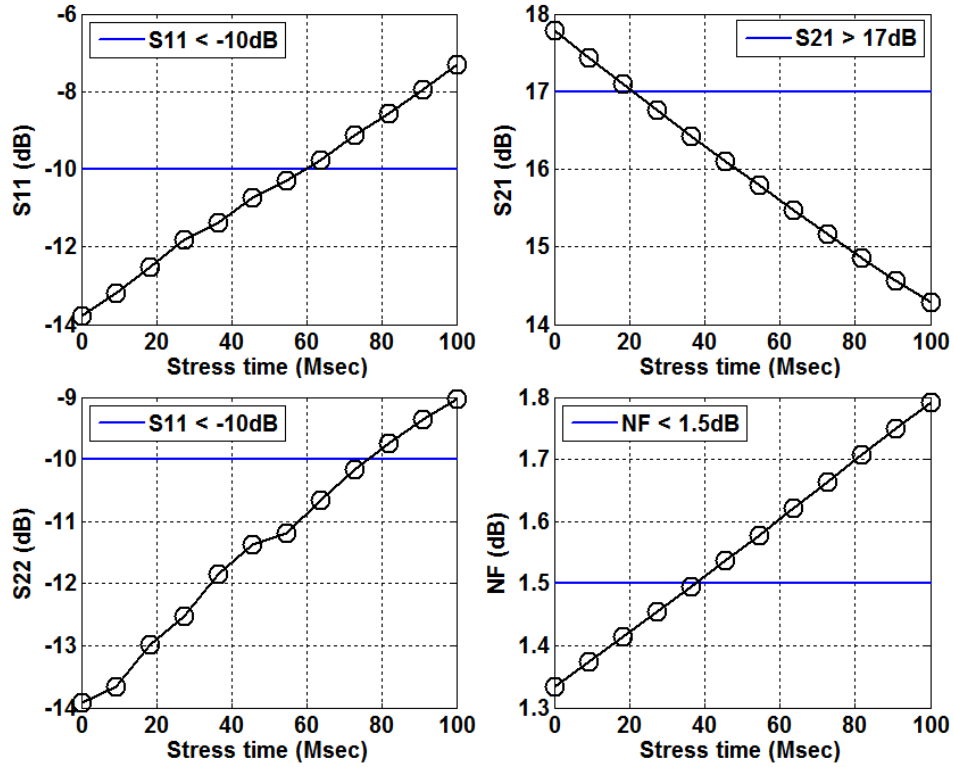

Figure 2.5. EM Simulation Results.

2.3.2. CMOS LC Oscillator with HCI and NBTI Analysis

Fig. 2.6 (a) and (b) shows the two types of CMOS LC-tank oscillators used in the circuit experiments. Important performance parameters of the LC oscillator are phase noise and output amplitude [44]. The N-type oscillator is designed to yield a phase noise better than -114 dB/Hz at 1-MHz offset and an output amplitude higher than $2V_{pp}$ at 5-GHz center frequency.

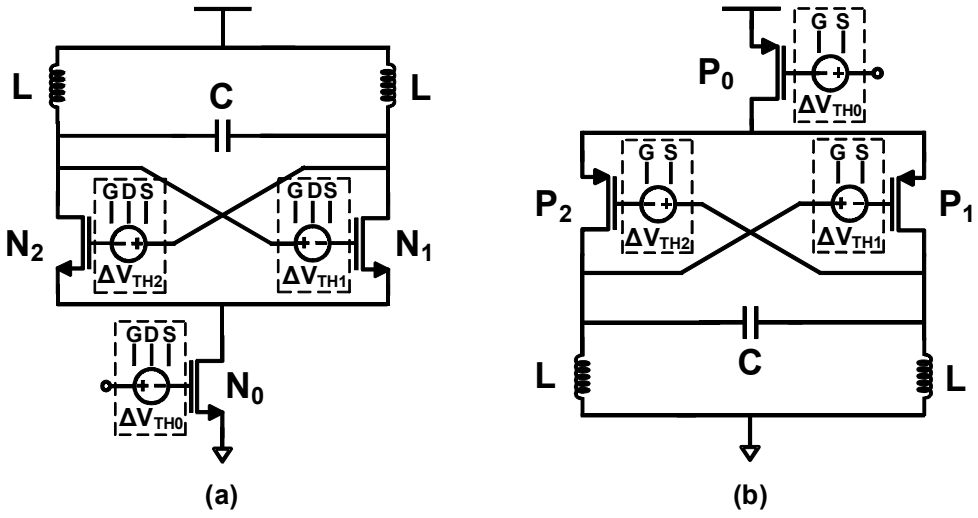

Figure 2.6. (a) HCI Analysis of N-type and (b) NBTI Analysis of P-type LC Oscillators.

Fig. 2.7 (a) shows the performance degradations in N-type LC oscillator over stress time. Note that the cross-coupled transistors degrade faster due to higher voltage stress. Therefore, a lifetime of $< 60\times10^6$ seconds is predicted when output amplitude is higher than $2V_{pp}$.

The performance degradation for the P-type oscillator is similar to the N-type. However, NBTI has unique characteristics due to stress recovery [10]. In a P-type oscillator circuit, the cross-coupled transistors are exposed to ac stress, while the tail transistor is under dc stress. Due to the recovery phase of the NBTI, the parameter degradations on cross-coupled transistors are less compared with the tail transistor, although the stress conditions for cross-coupled transistors are greater than the tail transistor in the P-type LC oscillator. Fig. 2.7 (b) also represents the simulation results for the P-type oscillator after NBTI effect.

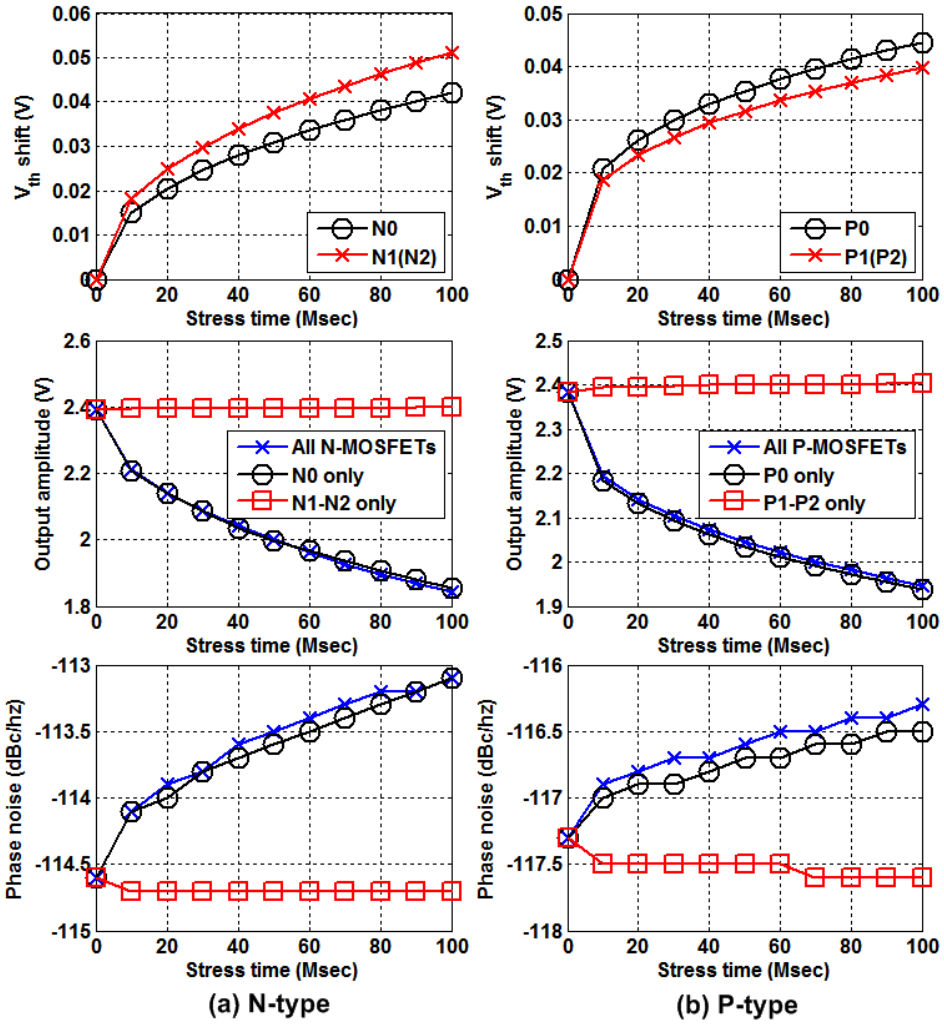

Figure 2.7. Performance Degradations of (a) N-type and (b) P-type LC Oscillators versus Stress Time.

Fig. 2.7 also shows the reliability simulation results of cross-coupled transistors with ±5% mismatch in process parameters and aging parameters. While these transistors undergo similar stress patterns, in both dc and ac domains, there is still some mismatch in their parameters. This is due to the mismatch in process and degradation patterns. It is observed that the degradation in cross-coupled transistors does not cause a significant degradation in the overall performance. This result may be at first counterintuitive.

However it can be explained with the phase noise model [44]. The g_m of the cross-coupled transistors plays a role in determining the equivalent resistance, hence the phase noise. However, it is primary determined by the tail transistor, since the transistor size does not change. Hence, a change in the threshold voltage of cross-coupled transistors does not cause significant degradation in the phase noise, unless it alters the bias so significantly that the circuit diverts from the desired operating point.

2.4. Hotspot Identification

The degradation of threshold voltage and LNA performances due to the HCI effect during three years of stress time are shown in Fig. 2.8. This analysis indicates that the $S11$ will fail earliest due to the degradation in transistor M_1. Hence, for the first iteration, M_1 is determined as the reliability hotspot due to HCI.

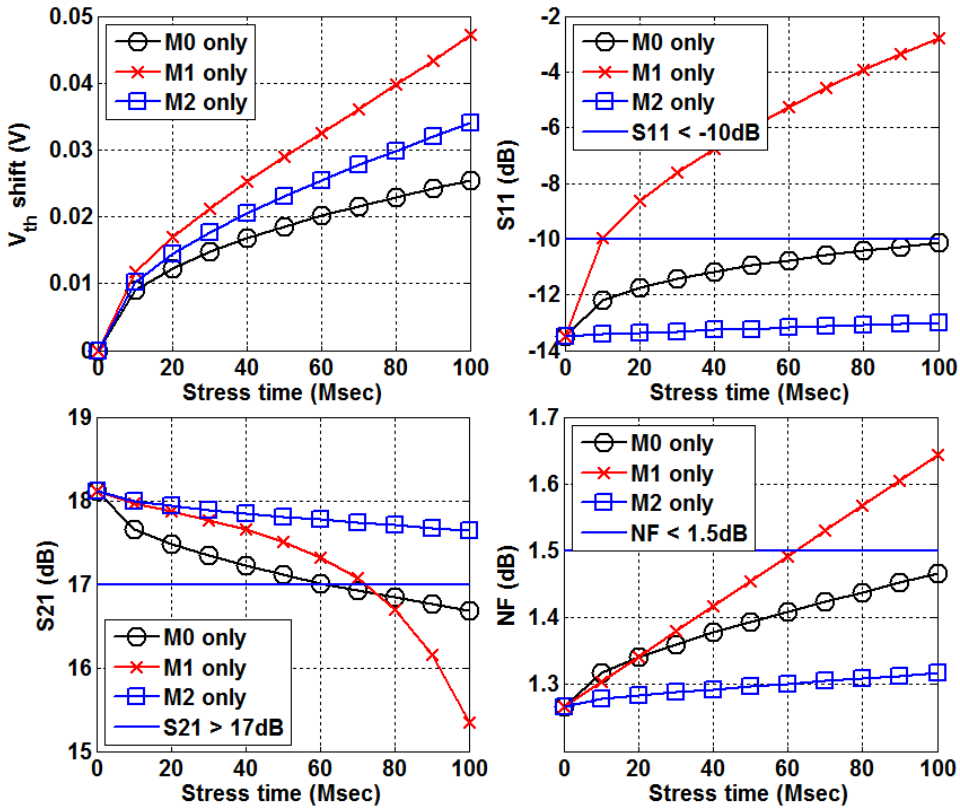

Figure 2.8. Hotspot Identifications of LNA Due to HCI Effects.

To identify the critical component of EM resistances on LNA lifetime, the functions relating the resistance of R_s (= R_{Ls}+R_{ems}) and R_d (= R_{Ld}+R_{emd}) to stress time are shown in Fig. 2.9 (a) by scaling the slope for the design's current density. EM results in a linear increase in resistances R_{emd} and R_{ems} with stress time. The variations in LNA performance parameters due to EM are shown in Fig. 2.10. Based on these simulations, it is concluded that the R_{emd} resistance is the critical component for $S21$. For specifications ($S21$ > 17 dB and $S11$ < -10 dB), the lifetime of this device is estimated as 50×10^6 seconds (~20 months). Thus, the reliability of this design is limited by the current path through L_d.

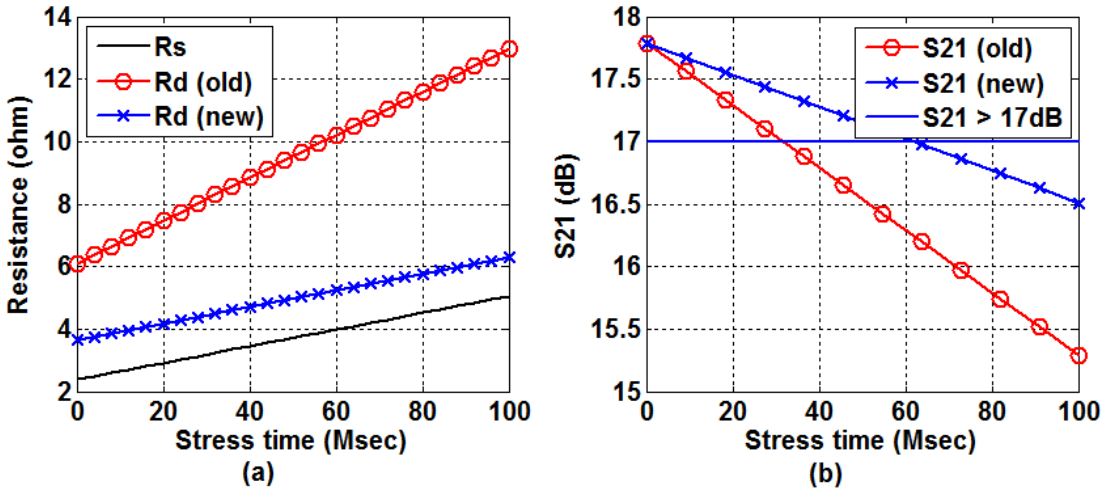

Figure 2.9. (a) R_s and R_d Variations Due to EM Effects over Stress Time and (b) Lifetime Enhancement of LNA Due to EM Effects.

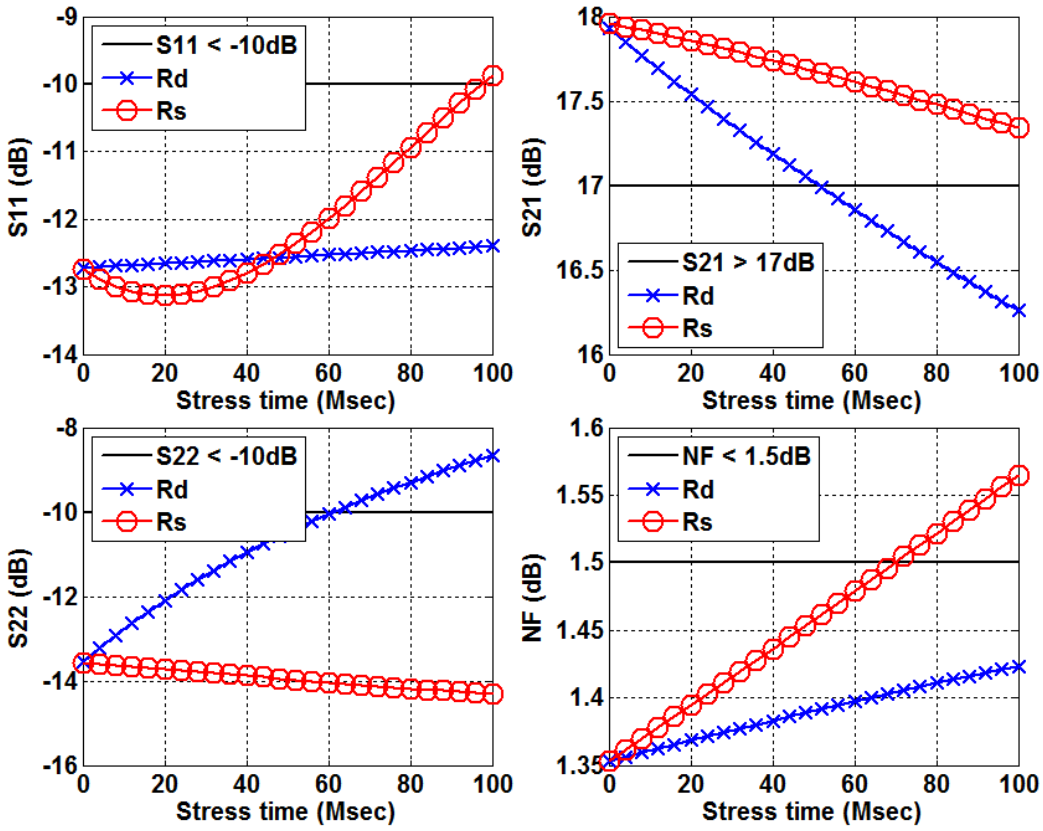

Figure 2.10. Impacts of Each EM Resistor on Circuit Performances.

For the N-type LC oscillator shown in Fig. 2.6 (a), the degradation model of each transistor is adjusted by HCI effect. First, the threshold voltage shift model of tail transistor is adopted to analyze the performance with gradually increased stress time. Because both tail transistor and cross-coupled transistor are biased with different dc bias conditions, different amounts of degradation in threshold voltage shift are determined and applied to the circuit. The overdrive voltage at the tail transistor is usually kept low to allow a higher output swing. Thus, the transistor at the cross-coupled pair experience a dc bias voltage of $V_{ds} = V_{gs} \approx V_{dd}$. From the degradation results, shown in Fig. 2.7 (a), although the degradation of threshold voltage in cross-coupled transistor is higher than tail transistor, the degradation performances, such as phase noise and output amplitude, for tail transistor N_0 only aged are more significant than those of cross-coupled only aged during three years. It is concluded that the tail transistor of N-type LC oscillator is a critical device due to HCI.

The same simulation process is implemented for the P-type LC oscillator. The degradation model of NBTI effect is used to demonstrate the threshold voltage shift under the stress condition. Fig. 2.7 (b) represents the reliability simulation results for a P-type oscillator considering NBTI. As predicted earlier, the cross-coupled transistors will introduce less degradation effects on the performance than the tail transistor because of the recovery phase in the cross-coupled transistors. Therefore, the tail transistor P_0 of the P-type LC oscillator is the critical device causing degradations due to NBTI.

2.5. Design-Time Optimization in RF Circuits

To reduce or eliminate the HCI and NBTI effects, the circuits are redesigned with adjusted bias to relieve the stress on the hotspot. After identifying the critical transistor(s) with HCI or NBTI effects, it is possible to minimize the performance degradation by changing the size of this critical transistor(s). HCI effect has a strong dependence on the channel length of the nMOS device. For the cascode LNA and N-type LC oscillator with the HCI effect, as the length of the nMOSFET device is reduced, the lateral channel electric field increases, and the HCI effect becomes more significant [10]. Therefore, redesigned LNA and N-type LC oscillator have increased critical transistor length from 65 to 130 nm, thus reducing the lateral electric field through the channel, and reducing threshold voltage degradation. The critical transistor's bias conditions and the RF performance of the original and redesigned circuits should be the same at initial stress time. To achieve comparable performance to the original design, it is required to co-design the circuits by adjusting circuit parameters, such as transistor dimensions and passive component values, in the redesigned circuits. The reliability simulation results shown in Fig. 2.11 confirm that the redesigned LNA with 130-nm critical transistor length has less performance degradations than the original LNA with 65-nm transistor length. Furthermore, lifetime has been increased significantly. For instance, the lifetime of original cascode LNA, which is estimated as 15×10^6 seconds due to a failure in $S11$ ($S11 < -10$ dB), has increased to 35×10^6 seconds after the redesign technique is applied. The simulation results illustrating the enhanced performance in the N-type and P-type

oscillators are shown in Fig. 2.12. For specifications (output amplitude > 2V), the original N-type oscillator's lifetime is estimated

as 50×10^6 seconds. However, it is possible to achieve longer lifetime ($>100\times10^6$ seconds) by adopting the longer channel length for the tail transistor. Therefore, the proposed design technique mitigates the degraded performance and increases both the LNA and N-type LC oscillator's lifetimes.

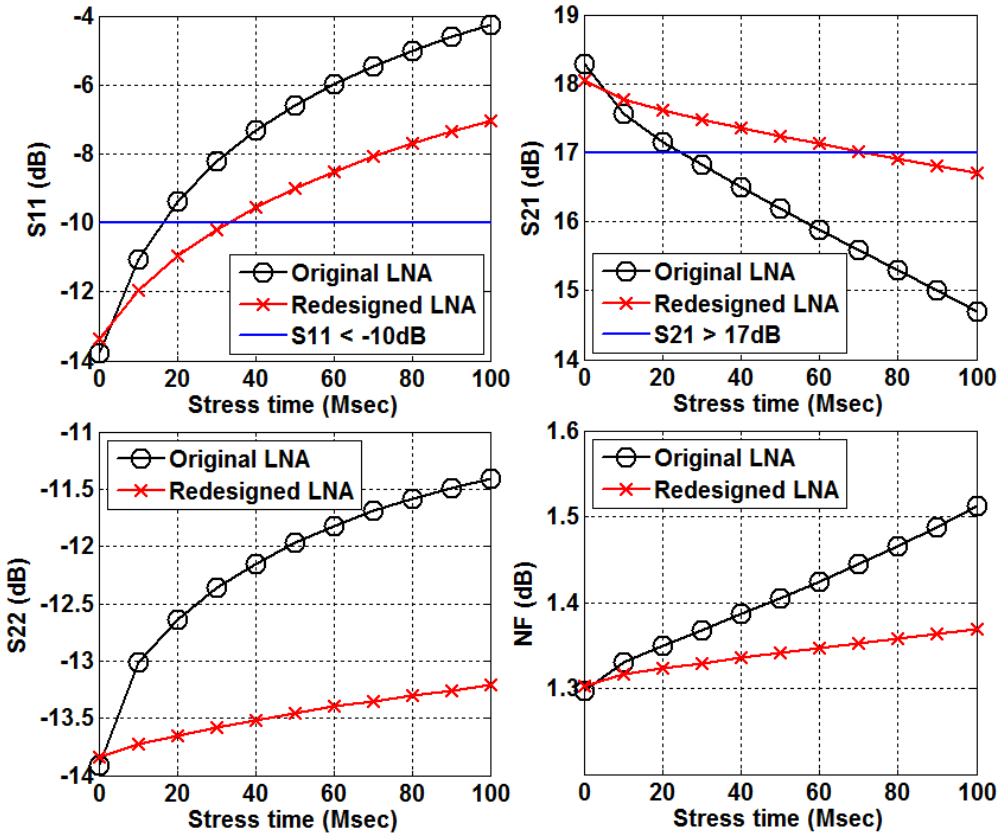

Figure 2.11. Lifetime Enhancement of LNA Due to HCI Effects.

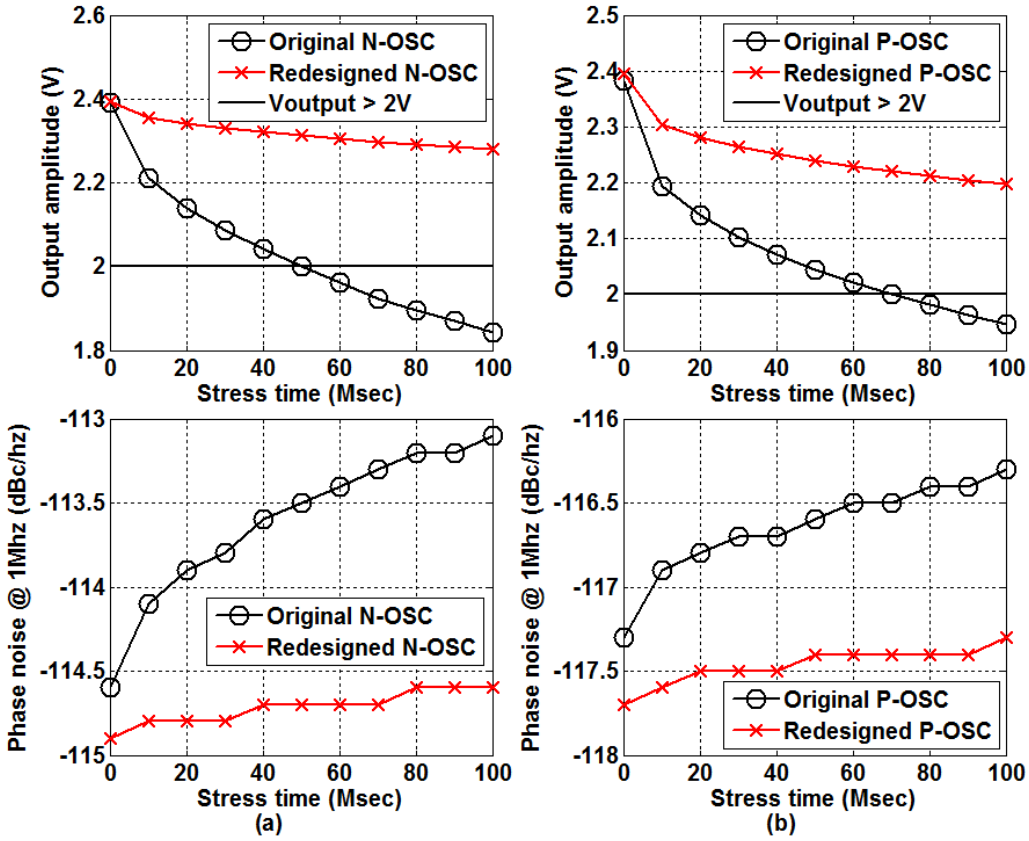

Figure 2.12. Lifetime Enhancement of (a) N-type and (b) P-type LC Oscillators.

While designing a P-type LC oscillator to reduce the NBTI effect, it is required to consider the bias condition of critical device which is a tail transistor in the P-type LC oscillator. Contrary to HCI, NBTI is relatively independent of the channel length of device. Because the higher vertical electric field across the gate oxide results in the NBTI effect of the pMOSFET, one can select a lower tail transistor gate bias voltage to reduce the degradation in threshold voltage shift. By decreasing the gate bias voltage and increasing the tail transistor's device width, the RF performance remains the same as the original circuit. The source-drain voltage and transconductance of the pMOS tail

transistor are chosen to have similar values to the original circuit so that the phase noise and output amplitude of the redesigned circuit are comparable with the original circuit.

The performance degradation and lifetime limitation of RF circuits due to EM are mainly due to current stress. To increase the lifetime of degraded circuits, the current density through the critical component should be decreased. Decreasing actual current would affect other circuit performance parameters. Therefore, a layout improvement technique that increases the metal line width(s) to decrease current density is proposed for mitigation of the EM effect. As presented in previous section, the critical EM components in the cascode LNA are the drain inductors L_d. For inductors, increasing the line width has two effects. First, it decreases the initial baseline resistance, making the initial point lower. Second, it decreases the rate of the resistance degradation. By increasing the width of L_d, lifetime can be increased. The total resistance R_d at the drain side with a wider width of L_d will have less series resistance compared with the original design at a certain stress time. Although a decrease in resistance is achieved by the increase in total area, a decreased resistance of the inductor can improve RF performance and extend the LNA lifetime. An area penalty exists, but this technique is better than blindly resizing all components. From Fig. 2.9 (b), modifying the critical device within layout increases the circuit lifetime by 100%, from 30×10^6 to 60×10^6 s. Table 2.1 shows circuit specifications such as power, area, and lifetime when redesign technique is used. Compared with the results of redesign layout technique without hotspot identification, which means all circuit components are resized blindly, it should be noted that focusing the layout technique on the critical device identified through hotspot analysis enhances lifetime without a large area penalty.

Aging effects	HCI in n-type OSC			NBTI in p-type OSC		
Redesign technique	Initial Design	w/ hotspot	w/o hotspot	Initial design	w/ hotspot	w/o hotspot
Power (mW)	4.89	**5.08**	5.13	5.07	**5.23**	5.3
Area ($\times\mu m^2$)	112500	**113600**	114000	111500	**113300**	113800
Lifetime ($\times 10^6$s)	50	**>100**	>100	70	**>100**	>100

Aging effects	HCI in LNA			EM in LNA		
Redesign technique	Initial design	w/ hotspot	w/o hotspot	Initial design	w/ hotspot	w/o hotspot
Power (mW)	8.50	**8.81**	8.9	8.48	**8.51**	8.53
Area ($\times\mu m^2$)	216400	**218100**	218800	216500	**233000**	242000
Lifetime ($\times 10^6$s)	15	**35**	35	30	**60**	60

Table 2.1. Comparison of Circuit Specifications for Aging Effects.

2.6. Conclusion

In this chapter, a methodology to analyze the performance of RF circuits degraded by aging mechanisms, such as HCI, NBTI and EM is presented. The proposed method is focused on finding the device that is most critical for circuit performance degradation. Once the critical device of RF circuits is determined, remedial action can be taken to mitigate the circuit performance degradations. It shows the demonstration of the proposed technique on an LNA and two LC oscillators as case studies. Experimental results show that the degradation performance and the lifetime were enhanced by increasing the critical transistor size or widening the inductor line. The methodology should be applied to the particular design at hand to fully gauge the impact of aging effects.

CHAPTER 3

MONITOR-BASE IN-FIELD WEAROUT MITIGATION FOR CMOS LC OSCILLATOR

In this chapter, a comprehensive systemic methodology for co-designing CMOS LC oscillators together with monitoring and reconfiguration mechanisms is proposed to enable aging mitigation with minimal performance and area overheads. Specifically, the contributions in this work are as follows:

(1) Analysis of hotspot identification in CMOS LC oscillator

(2) Analysis of a method for determining low impact reconfiguration mechanism

(3) An algorithm for determining recovery trigger conditions in the field

(4) Low cost on-chip measurement of monitoring voltage

(5) Detailed analysis of area overhead of the entire monitoring / recovery circuits

(6) Manufactured CMOS LC oscillator in 180nm IBM process with monitoring mechanism, accelerated aging experiments, and results on aging and recovery.

3.1. In-field Detection and Recovery Scheme

Fig. 3.1 shows the overview of the proposed methodology. At design time, given the DUT (Design under Test) architecture and initial design point, reliability simulations are conducted to obtain circuit performance profiles over time by aging one device at a time. While the predicted lifetime will not be accurate, this analysis will help to identify reliability hotspots to effectively monitor device performance. Appropriate monitor

location as well as the reconfiguration mechanisms are included in the design and the DUT is co-optimized with these monitoring and recalibration hooks.

Fabricated devices will be characterized during production test along with the monitor output. Specification margin of each manufactured circuit will be different due to process variations. This margin is used to determine the allowable degradation and thus the threshold to initiate reconfiguration.

Once the device is deployed in the field, the monitor response will be periodically evaluated and circuit will be reconfigured if necessary.

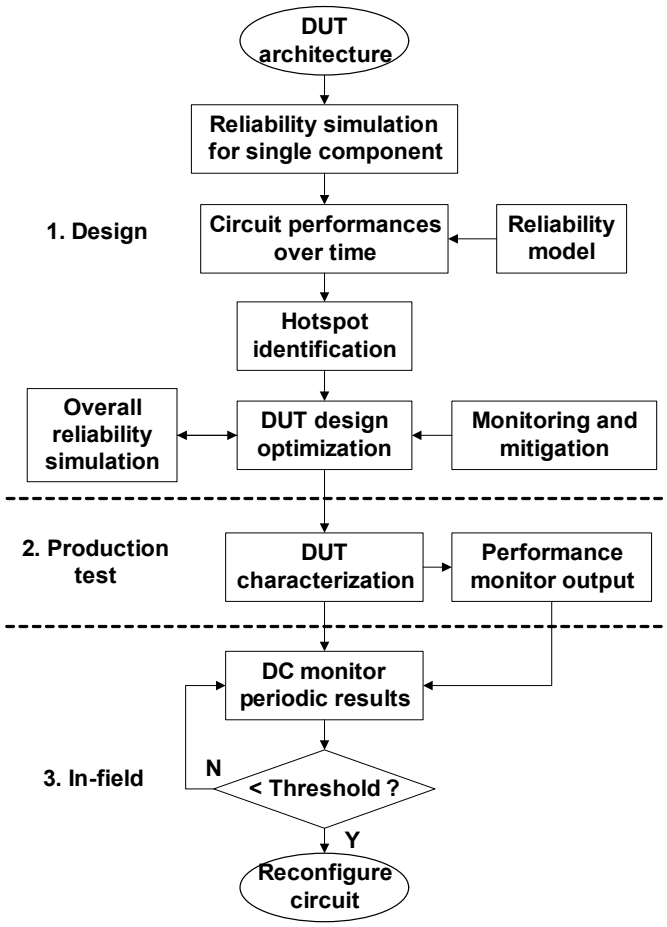

Figure 3.1. Flow Diagram for the Proposed Methodology.

3.1.1. Hotspot Identification

The first step is to analyze the reliability of the circuit and determine the hotspots, such as the transistors or components that are predicted to cause parametric failures.

The analytical degradation model of each MOSFET is used to extrapolate the degradation of its parameters (e.g. threshold voltage) during operation time (e.g. years) based on nominal stress conditions that is obtained from the circuit simulator. Circuit performance is re-evaluated at each time point. The extrapolated device parameters are used to modify the parameters in the degradation model and the circuit is re-simulated to obtain the updated stress conditions. Hence, the performance of the circuit gradually shifts in time. This information combined with the circuit specifications yields a certain time point at which the specification will fail. This time point is chosen as the failure time of the circuit. Due to different sizes and operating points, the degradation patterns will be different for each circuit component. Thus, each circuit component will cause a distinct failure time for each circuit performance over stress time. The process iteratively go through each circuit component and track the degradation profile of the each circuit parameter. Once all the degradation patterns are analyzed, it is possible to determine the most vulnerable component to aging effects. This process called hotspot identification, concentrates on each circuit component and identifies the circuit component that causes a specification failure at the earliest time [45]. Note that this is not necessarily the lifetime of the circuit. The actual failure time (lifetime) of the circuit will differ from the failure time determined by hotspot identification since all circuit components age at the same time, albeit at a differing rate.

3.1.2. Monitoring Scheme

A second step in the proposed method is to add a simple monitoring circuit to detect performance degradation. In order to enable the proposed recovery, a monitoring mechanism is required to detect performance degradation. For LC oscillators, phase noise is the most stringent performance parameter and it is the one that fails first under stress [14]. However, direct on-chip measurement of phase noise is not feasible. Hence, it is necessary to identify a circuit parameter, preferably in the low frequency domain, that is most correlated to phase noise. In the next section, the proposed methodology is applied to two designed LC oscillators and determine how this monitoring can be enabled with low impact and high accuracy.

3.1.3. Reconfiguration Scheme

A third step is to improve the predicted circuit lifetime (for most devices) by re-designing the circuit. In other words, if the projected lifetime is not satisfactory, the lifetime-limiting component is adjusted by changing the transistor sizes and re-designing the entire circuit around the new sizes. It should be noted that this enhancement strategy is not always feasible, especially when frequency domain operation is taken into account. This design-time reliability enhancement strategy is common to most procedures in the literature [26], [34]. It is observed that even when design-time enhancements are employed, degradation is unavoidable and cannot be easily predicted at production time. In order to mitigate the effects of aging, additional circuit components are included. Finally, a recovery strategy that includes spare transistors is employed to replace the transistor that is identified as the hotspot.

3.2. Case Study of PMOS and NMOS Oscillator

CMOS LC oscillators are widely used in high performance PLLs and frequency synthesizers due to their relatively good phase noise and ease of design. As shown in Fig. 3.2, there are two kinds of oscillators (N-type and P-type) for case studies. The fundamental of tail current due to filtering in LC tank creates differential output voltage of across the tank as in Eqn. (3.1) [46].

$$V_{out} = \frac{4}{\pi} I_{tail} R_{eq} \tag{3.1}$$

where R_{eq} is the equivalent resistance of the tank. The phase noise of an LC oscillator at an offset frequency ω_m from the frequency of oscillation ω_0 normalized with respect to the carrier is given by Eqn. (3.2) and (3.3) [46], [47].

$$L(\omega_m) = 10\log\left[\frac{4kTFR_{eq}}{V_{out}^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2\right] \tag{3.2}$$

$$F = 2 + \frac{8\gamma R_{eq} I_{tail}}{\pi V_{out}} + \frac{8}{9}\gamma g_{m\_tail} R_{eq} \tag{3.3}$$

where F denotes the noise factor, γ is the noise factor of a single transistor. The value of γ is 2/3 for long-channel transistors and may rise to between 2 and 3 in short-channel devices. V_{out} is the output amplitude of the differential oscillator output, and g_{m_tail} is the transconductance of the tail transistor, and Q is the quality factor of the tank inductor and capacitors.

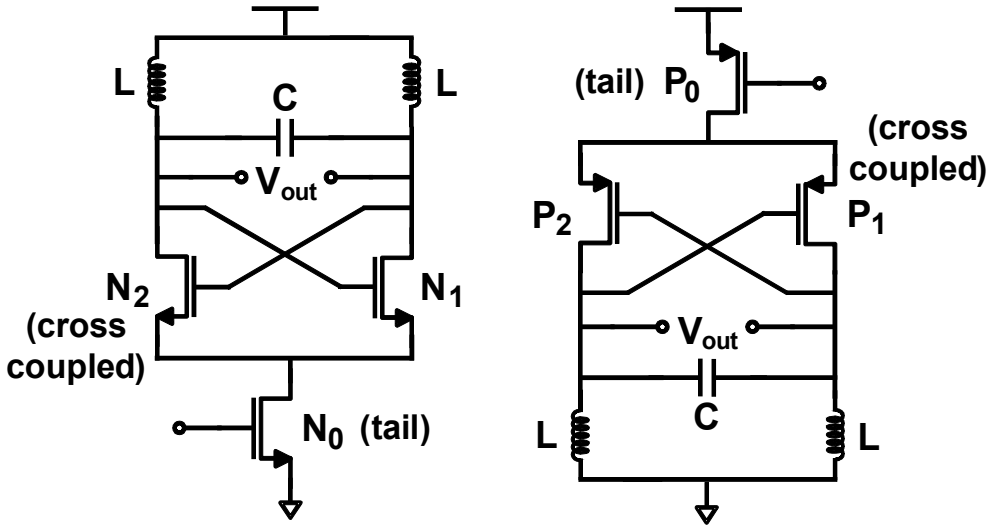

Figure 3.2. N-type and P-type LC oscillator.

3.2.1. Reliability Analysis and Hotspot Identification of LC Oscillator

Fig. 3.3 shows the proposed method for reliability analysis of the LC oscillator. The most common reliability issues of HCI and NBTI are analyzed for the effects on CMOS LC oscillators.

HCI and NBTI cause degradation in the threshold voltage for N- and P-type devices, respectively. Considering these effects, threshold voltage shifts are modeled according to [10]. Since these shifts are dependent on operating conditions, they are changed at each time step for the simulation. As shown in Eqn. (3.3), there are three terms in the noise factor F. The first term which ends up being a constant, shows the noise generated in the resonator, which has insignificant impact on the reliability analysis since it is composed of passive devices. The second and third terms are from the noise generated by the cross-coupled transistors and the noise generated by the tail transistors, respectively. Therefore,

in order to perform the reliability analysis with respect to the phase noise of LC oscillator, it is imperative to focus on those transistors, which may degrade due to aging.

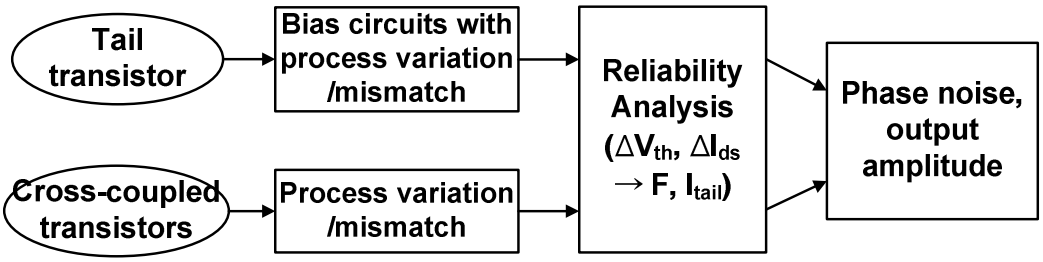

Figure 3.3. Reliability Analysis of LC Oscillator.

3.2.1.1. Reliability Analysis of Cross-coupled Transistors of LC Oscillator

Fig. 3.4 shows reliability simulation results in terms of phase noise and output amplitude of one random N-type and P-type LC oscillator instance from Monte Carlo simulations. Statistical simulations within 10% variation from nominal values are used to explore not only the effects of process variation and mismatch, but the aging parameters between cross-coupled transistors.

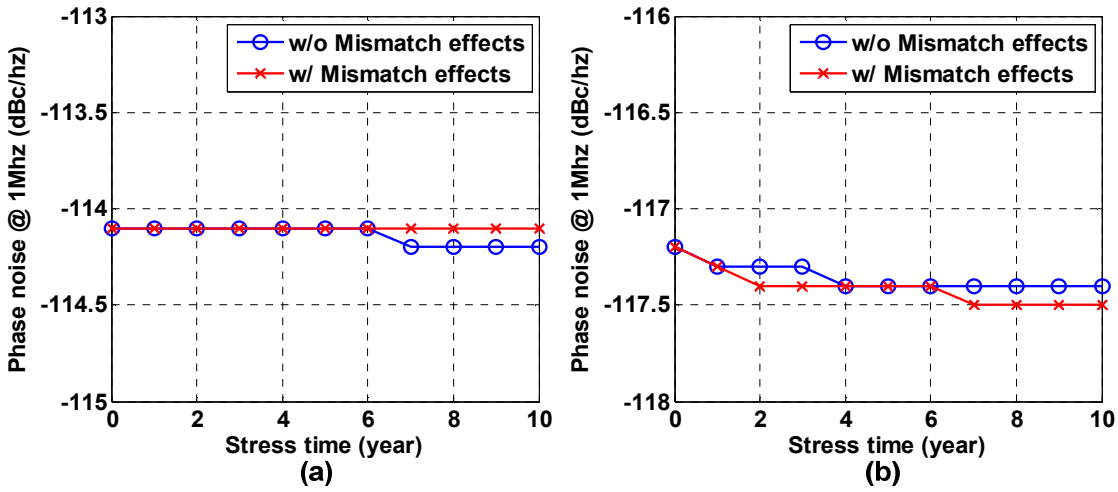

Figure 3.4. Simulation of Phase Noise Degradation Due to Cross-coupled Transistors of (a) N-type and (b) P-type Oscillator under Nominal Stress Conditions.

In both LC oscillator circuits, cross-coupled transistors experience AC stress while the tail transistor is under DC stress. Because of the large voltage swing up to $2V_{dd}$ across the cross-coupled transistors, the total stress on these transistors will be higher than the tail transistor and they will experience faster degradation compared to the tail transistor. While the cross-coupled transistors undergo high stress conditions, it is observed that the degradation in cross-coupled transistors with the mismatch effects does not cause a significant degradation in the overall phase noise performance. This result may be at first counter-intuitive. However, it can be explained with the phase noise model by substituting Eqn. (3.1) in Eqn. (3.2) and (3.3).

$$L(\omega_m) = 10\log\left[\frac{4kTR_{eq}(2+2\gamma+\frac{8}{9}\gamma D_n\sqrt{I_{tail}R_{eq}})}{(\frac{4}{\pi}I_{tail}R_{eq})^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2\right] \tag{3.4}$$

$$F = 2+2\gamma+\frac{8}{9}\gamma D_n\sqrt{I_{tail}R_{eq}} \tag{3.5}$$

where D_n is $\sqrt{2\mu_n C_{ox}(W/L)}$. From Eqn. (3.4), $L(\omega_m)$ can be written to display dependence on I_{tail} and R_{eq}, which are separately affected by the tail transistor, and by the cross-coupled transistors. It is shown that the phase noise is primary determined by the tail current I_{tail}. The g_m of the cross-coupled transistors plays a role in determining the equivalent resistance, hence only the oscillation condition ($R_{eq} \geq 1/g_{m\_cross}$). Therefore, a change in the threshold voltage of cross-coupled transistors does not cause significant degradation in the phase noise of the oscillator, unless it alters the bias conditions so significantly that the circuit diverts from the desired oscillation condition. It is shown later with simulation results that phase noise is insensitive even to large degradations of cross-coupled transistors. Moreover, thanks to the recovery phase of the NBTI which is a unique feature for PMOS aging effect, the degradations on cross-coupled transistors in the P-type oscillator are less compared to those in the N-type oscillator.

3.2.1.2. Reliability Analysis of Tail Transistor of LC Oscillator

Degradation of the tail transistor due to the increase in threshold voltage causes a decrease in both the tail current and the transconductance, which are dominant parameters in the phase noise model. Moreover, Eqn. (3.1) indicates that the output amplitude of the differential oscillator is directly proportional to the tail current. Hence, the performance of the tail transistor significantly affects the overall performance. This analysis assumes that the tail current is voltage biased such that a shift in the transistor threshold voltage results in a shift in the tail current. However, most design techniques use a separate bias block and mirror the current to various locations in the circuit. Hence, it is required to take this current mirror into account. If the bias circuit transistors and the

tail transistor undergo identical stress conditions, and possess identical process and degradation parameters, the tail current will not be changed, hence there will be no degradation. However, this is typically not the case, since the bias block is designed with many circuit blocks in mind and generally uses larger transistors. Large transistors are not preferable for oscillators since they degrade circuit performance and cause increased thermal noise. Moreover, mismatch between the bias circuit transistors and the tail transistor will still cause significant change in the threshold voltage. This intuitive analysis is confirmed with reliability simulations under various biasing design conditions.

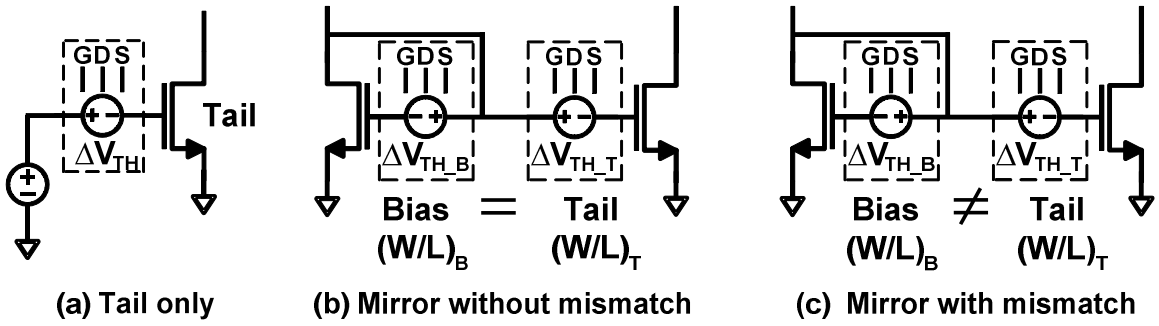

Figure 3.5. Reliability Analysis of a Tail Transistor with Different Bias Designs.

The different biasing designs are shown given in Fig. 3.5, where a) tail only refers to voltage biasing technique, b) mirror without mismatch refers to current mirror biasing where bias transistors and the tail transistor are assumed identical in every respect (which is not realistic but is included as a point of comparison), and c) mirror with mismatch refers to current mirror biasing where transistors have mismatch effects in terms of their design, process, and degradation parameters. In general, because these transistors undergo similar stress patterns in DC domain, and due to the layout proximity, it is hard to expect big variations in circuit performances. However, there is still some mismatch in

aging parameters. In Fig. 3.6, one N- and P- type LC oscillator instance with different biasing designs is selected from Monte Carlo samples and simulated for phase noise performance. Especially, in the design c), 10% variation from nominal values are used for process variation and mismatch effects in Monte Carlo simulation. Fig. 3.6 shows the simulation results for the worst case of corner when matched transistors are at opposing mismatch corners. The simulation results show that unless a precise matching in the bias conditions is assured, degradation in the tail transistor will cause a significant degradation in the overall performance within the first few years of the operation under nominal stress conditions. Fig. 3.6 also shows that N-type and P-type oscillators have a similar degradation pattern even if the aging mechanisms and degradation profiles are different. Therefore, it is certain that phase noise degradation is primarily due to the aging of the tail transistor for both N-type and P-type oscillators.

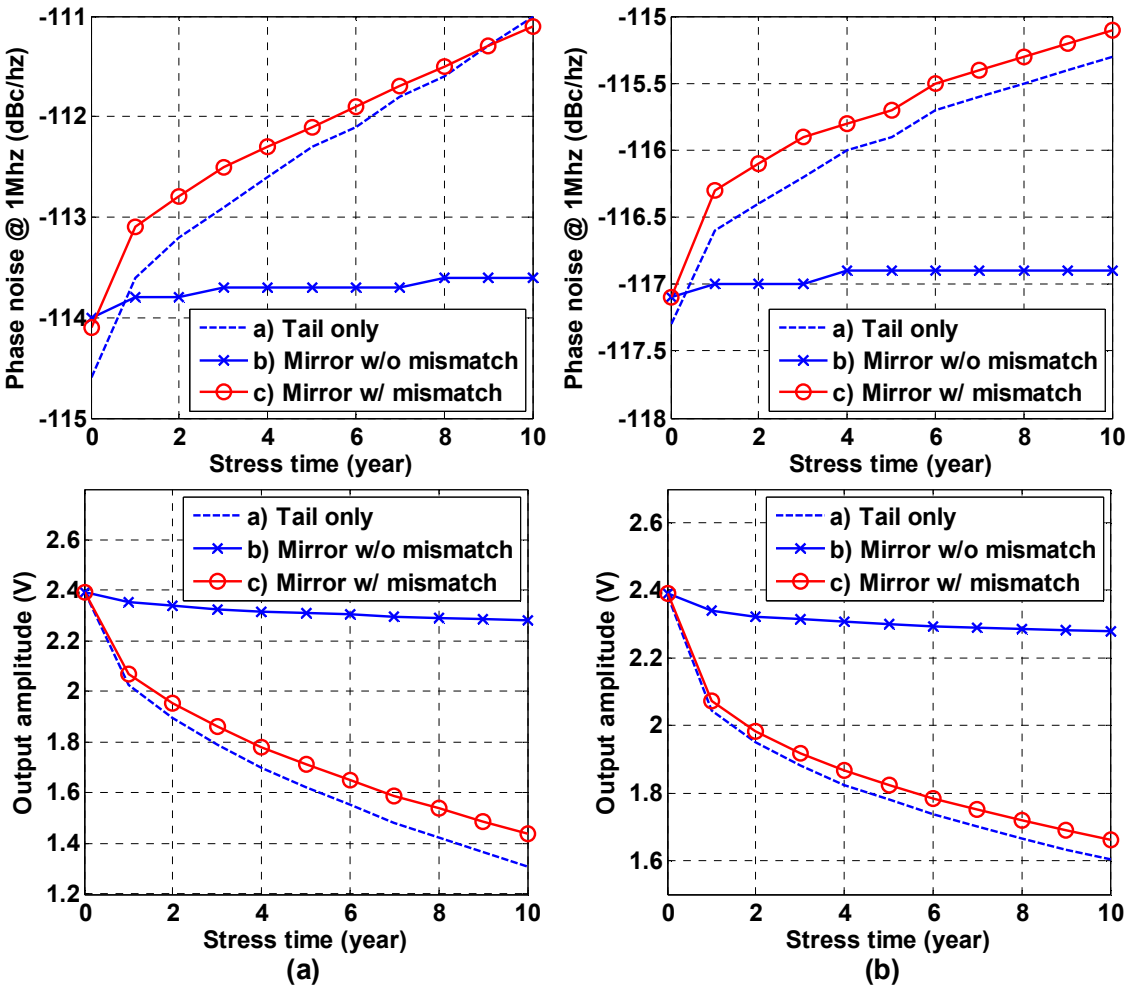

Figure 3.6. Phase Noise Degradation Due to Tail Transistors with Different Biasing Techniques in (a) N-type and (b) P-type Oscillator.

3.2.1.3. Hotspot Identification of LC Oscillator

For hotspot identification, each transistor is aged separately, and monitor the circuit response, both in terms of performance and in terms of additional parameters that can be monitored. First, the threshold voltage shift model of the tail transistor is adopted to analyze the performance with gradually increased stress time. Since tail transistor and cross-coupled transistors are biased with different DC bias conditions, they experience different amounts of degradation in threshold voltage, which are identified and applied to

the circuit. The overdrive voltage at the tail transistor is usually kept low to allow a higher output swing. Thus, the transistors at the cross-coupled pair experience a DC bias voltage of $V_{ds} = V_{gs} \approx V_{dd}$.

The results of this analysis for the N-type oscillator are given in Fig. 3.7 (a). Although the degradation in cross-coupled transistors is higher than the degradation in the tail transistor, the degradation of the overall performance in terms of phase noise is significantly higher for the tail transistor, N_0. Hotspot identification process shows similar results from reliability analysis mentioned in previous section. In other words, it is clearly noted that the aging of cross-coupled pair has no visible effect on the phase noise of oscillator even if there are process variation or mismatch effects in these transistors. Contrary to cross-coupled transistors, aging of tail transistor causes an increase in phase noise and decrease in oscillation amplitude.

The same simulation process is examined for a P-type LC oscillator. The degradation model of NBTI effect is used to demonstrate the threshold voltage shift under the nominal stress conditions (10 years stress time). The results are similar to the N-type LC oscillator. Fig. 3.7 (b) represents the hotspot identification results for a P-type oscillator. As mentioned earlier, the cross-coupled transistors will introduce less degradation effects on the performance than the tail transistor because of the recovery phase in the cross-coupled transistors. Therefore, it is clear that the tail transistor of the P-type LC oscillator is determined as a critical device which causes significant degradation due to NBTI.

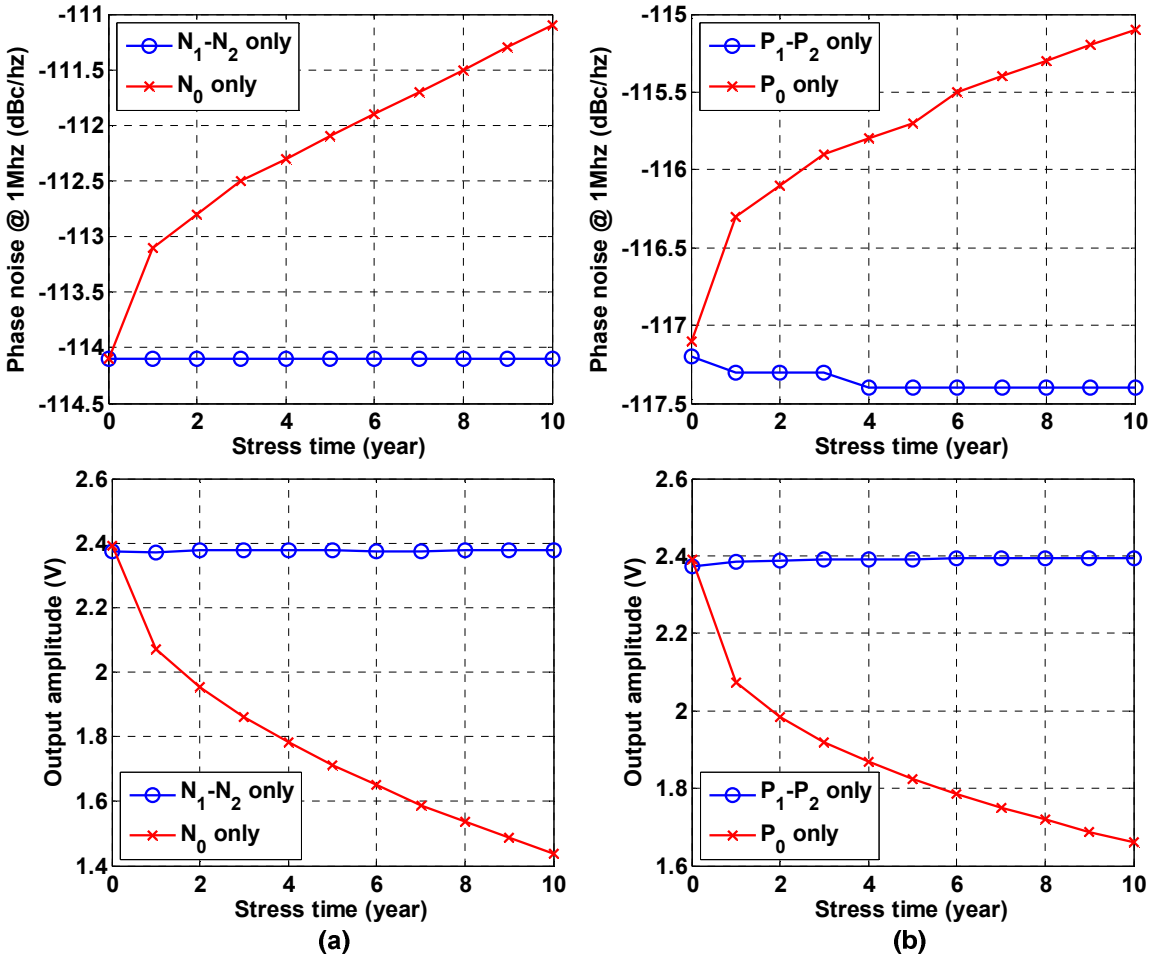

Figure 3.7. Hotspot Identification for (a) N-type and (b) P-type Oscillators.

3.2.2. Performance Monitoring

Since it is impossible to directly measure a phase noise on-chip with reasonable overhead, an alternative parameter that is easy to measure needs to be determined. Reliability analysis of LC oscillator has identified that the reduction in oscillation amplitude is primarily due to aging and is strongly correlated to aging based degradation. For the monitoring purpose, a peak detector circuit can be employed to measure the output amplitude for this purpose. Another alternative is to attempt to measure the tail current directly. A mirror-based approach cannot be used since the mismatch in the

mirror will eventually lead to inaccurate results. However, a sense resistor can be inserted into the current path for the monitoring purpose. Both options are implemented and shows that using the sense resistor leads to more reliable results and low impact in terms of performance. Since the tail current has a strong correlation with output amplitude and phase noise of the oscillators shown in Eqn. (3.1) and (3.2), it can be used as a low frequency alternative to monitor the degradation.

There are two possible locations for inserting the resistor, at the tail transistor side and at the LC tank side. For the N-type LC oscillator, inserting the sense resistor at the tail end will increase the source voltage of the tail transistor, causing a small difference between the source and the body voltage. Thus, this will cause inaccuracy in the measurement of the tail current. The second location of inserting the resistor is between the LC tank and the supply voltage/gnd. This location has a very small effect on the performance of the oscillator. The presence of the resistor connected with LC tank can cause a shift in the oscillation frequency. Moreover, adding sense resistor in series with the spiral inductor L can increase inductor loss. However, it is possible to reduce or completely eliminate these effects by taking this resistor into account at design time and co-designing the primary circuit with the monitoring circuit. If the value of the resistor is kept much smaller than the inverse of the transconductance, the noise from the sense resistor is negligible compared to the noise generated by the transistor. Therefore, it shows that the sense resistor has negligible effect on the overall performance at design time. The phase noise simulation in the presence and absence of the resistor is presented in Fig. 3.8.

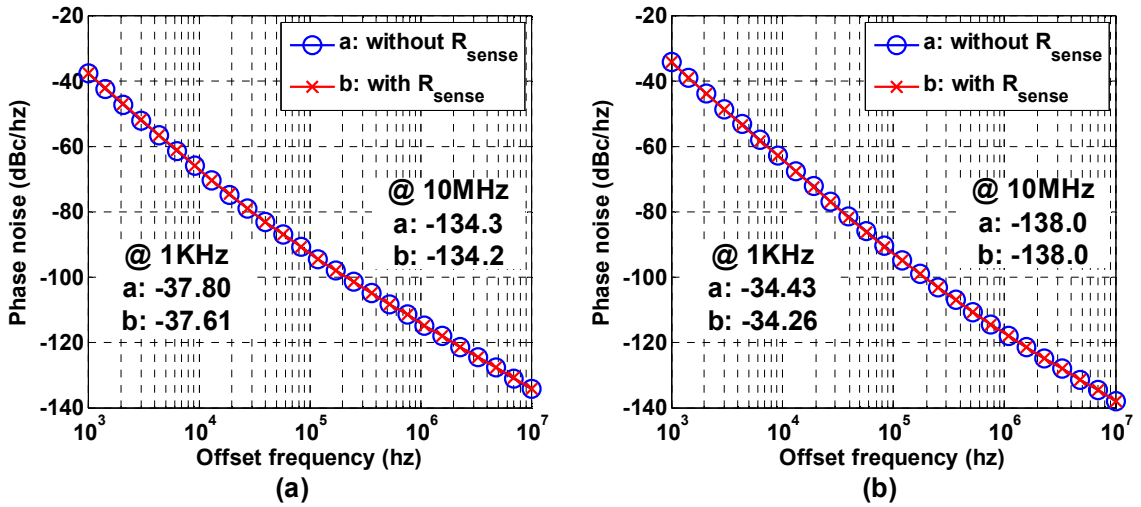

Figure 3.8. Phase Noise Degradation of (a) N-type and (b) P-type Oscillator with and without the Sensing Resistor.

On-chip sense resistor must be kept small to avoid significant voltage drop. Measuring a small deviation around a large DC value using traditional ADC architecture is challenging. However, a VCO-based ADC is suitable for the monitoring the small voltage from the sense resistor since it provides adequate resolution around a fixed point at very compact area [48]. A VCO-based ADC with 7 inverter stages is used for the measurement of the voltage across the sense resistor. This ADC has been shown to provide 50μV resolution for a 200 mV range [48].

3.2.3. Reconfiguration Hardware

In order to recover the degraded performance of aged oscillator, mitigation circuit consists of fresh transistors and digitally controlled MOS switches which can replace the aged transistor. Since the tail transistor is identified as the reliability hotspot, this aged tail device will be substituted with the fresh devices when the voltage across the sense

resistor degrades by a pre-determined fraction. Fresh transistors with same dimension to the tail transistor are connected in parallel to the tail transistor. There is another possible solution by adding extra small devices in parallel to the aged tail device to compensate the tail current of aged oscillator. However, this enhancement technique results in higher noise. Fig. 3.9 shows the three options for inserting MOS switches with tail (T_0) and fresh (T_1) transistors of N-type oscillator.

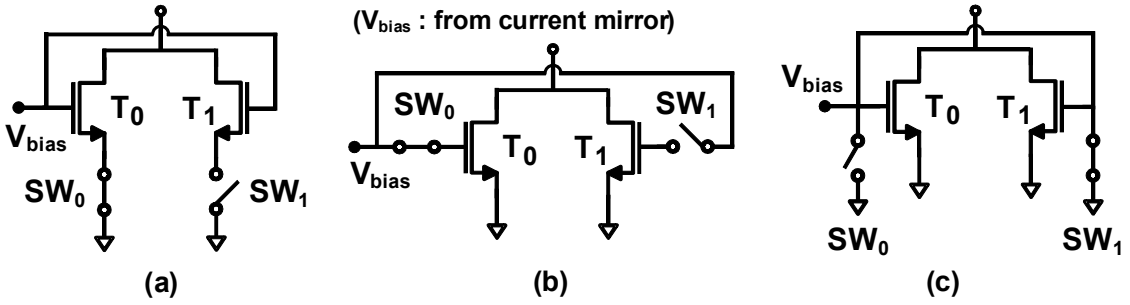

Figure 3.9. Possible Insertion Points for Digitally Controlled MOS Switches.

In the option shown in Fig. 3.9 (a), the MOS switches are in series with the transistor. There will be a slight increase in the source voltage of the tail transistor. Fig. 3.9 (b) shows an option where the unused transistor's gate is left floating and in Fig. 3.9 (c), the unused transistor is turned off by shorting gate and ground. For the architecture in Fig. 3.9 (a), the noise generated by the switch is not amplified by the tail transistor. However, for the architectures in Fig. 3.9 (b) and (c), the noise generated by the switch is indeed amplified by the tail transistor. Consequently, the architecture in Fig. 3.9 (a) has better noise performance than the other two options (Fig. 3.9 (b) and Fig. 3.9 (c)). Fig. 3.10 shows that having the reconfiguration switches at the source of the tail transistor, there is no noticeable degradation in the phase noise or output amplitude compared with

the baseline design. With co-design of reconfiguration switches and primary circuit, it is possible to avoid any performance degradation.

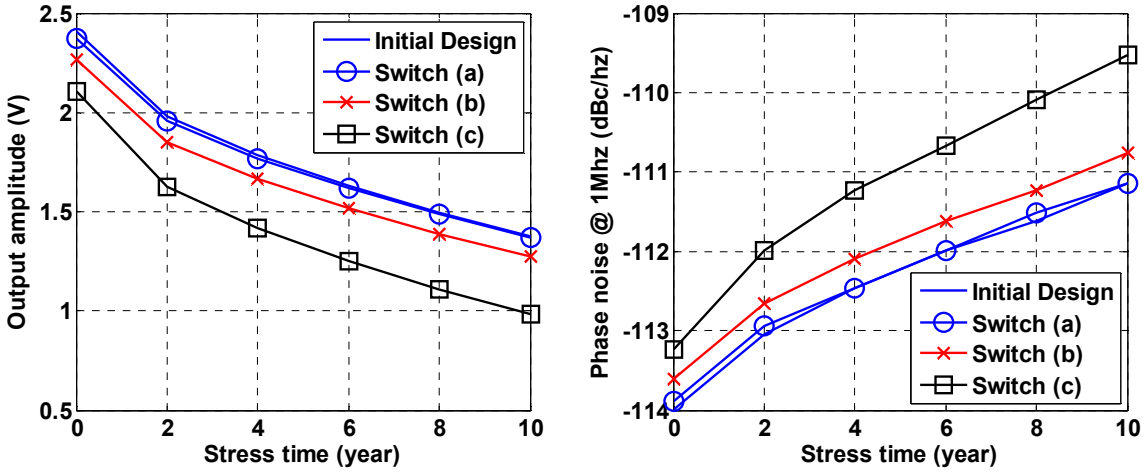

Figure 3.10. Performance Comparison with Different Locations of MOS Switches in N-type Oscillator.

3.2.4. Lifetime Enhancement

Fig. 3.11 shows the schematic and mechanism of the proposed monitoring and recovery circuits for N-type oscillator. The tail current of this N-type oscillator is monitored using the sense resistor (4 Ω) as discussed in the earlier section.

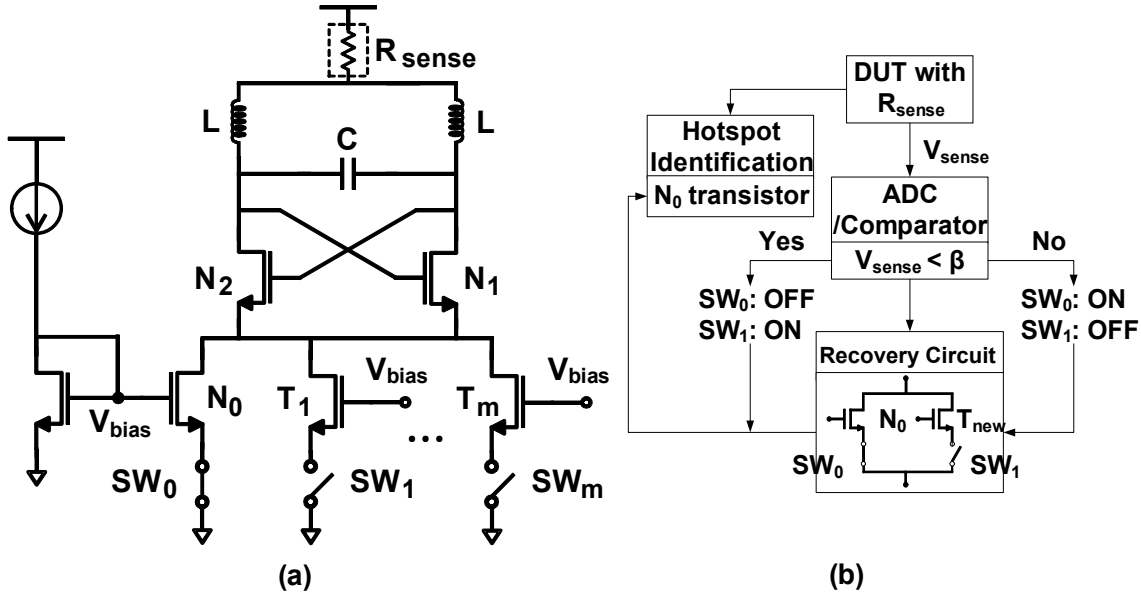

Figure 3.11. (a) N-type Oscillator with Proposed Monitoring and Mitigating Circuits and (b) the Overall Flow Chart of the Proposed Mechanism.

At production time, the oscillator is characterized in terms of phase noise and output power along with the monitor voltage. In order to verify the correlation between the monitor voltage and circuit performances of LC oscillator, Monte Carlo simulations are conducted with 100 circuit instances including process variations. Fig. 3.12 shows the correlation between the simulated performances for the tail current, the sense voltage, and phase noise of the proposed LC oscillator circuit under nominal conditions for 10 years operation time. It is observed that the sense voltage ($=V_{dd}–I_{tail}\times R_{sense}$) is proportional to the tail current. Furthermore, it is confirmed that the degradation in the phase noise is correlated with the deviation in the sense resistor voltage. For small changes, the correlation can be modeled as a linear relation even though the overall relation is non-linear. Since the monitor voltage (tail current) and phase noise are correlated, the same percentage degradation of the monitor voltage is used as a trigger mechanism for

reconfiguration. This comparative trigger mechanism eliminates reliance on the absolute value of the sense resistor as well as the performance of the ADC. Hence the reconfiguration mechanism is tailored with respect to characteristics of each manufactured device while being robust to the process variations.

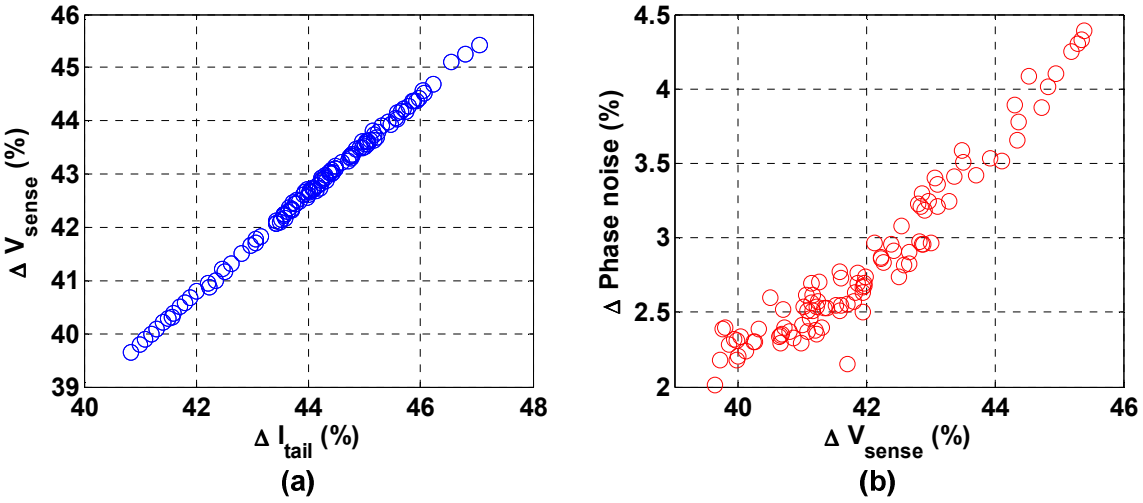

Figure 3.12. Correlation Between Circuit Performances from Monte Carlo Simulation of 100 LC Oscillators after 10 Years under Nominal Stress Conditions.

In the field, the monitor voltage is measured periodically (in a matter of weeks or months). This voltage is compared with the threshold determined during production test so that a replacement transistor can be used. Once the voltage on the sense resistor drops by a certain percentage (e.g. 20%), the existing tail transistor is swapped with a fresh one using the switch network. It should be noted that since each MOS switch changes a position only once (ON ↔ OFF), the impact of the switches on the RF performance is negligible.

Fig. 3.13 confirms that there is only 0.1 ~ 0.2dB difference in phase noise performance between initial design (no sense resistor and no switches) and the design including proposed sensing and mitigation circuits.

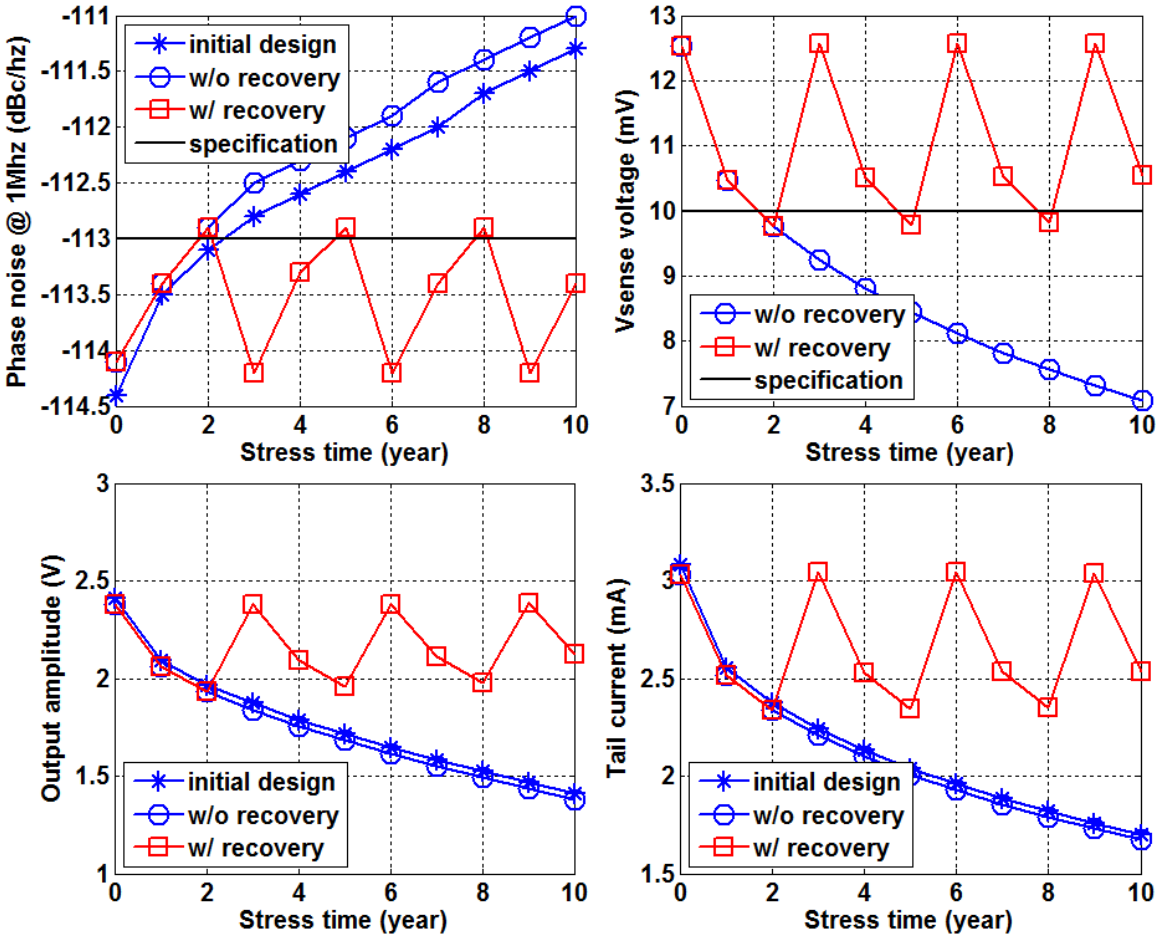

Figure 3.13. Simulation Results of Enhanced Lifetime Using the Proposed Method.

For the circuit in the example given in Fig. 3.13, the phase noise limit is –113dBc/Hz and the corresponding limit for the sense resistor voltage is chosen as 10 mV, which represents a 20% reduction in the tail current. Lifetime of the oscillator circuit

can be estimated as the time point where at least one parameter fails its specification. Therefore, the lifetime of this oscillator can be estimated as 2 years. The output amplitude and tail current can be recovered by substituting the aged tail transistor with a fresh one. With respect to this analysis, the lifetime of the device can be enhanced from 2 years to 5 years if there is only one spare tail transistor. If additional lifetime is desired, higher redundancy can be used. Fig. 3.13 shows that the degradation can be periodically recovered by using additional transistors.

It should be noted that since the enhancement circuit is designed in conjunction with the oscillator, the potentially diverse effects on performance can be eliminated by design time optimization. Fig. 3.13 also shows that for this particular circuit instance, there is virtually no performance difference between the baseline design and the reliable design.

3.2.5. Area Impact

The proposed technique requires additional circuit components in terms of a sense resistor, spare tail transistors and an ADC. Tail transistors are generally smaller compared to the LC tank and the sense resistor is quite small. Control is achieved digitally via MOSFET switches, which are very small transistors. The major component that is required is the ADC to convert the sense voltage into digital form. Due to the comparative measurements, a very small VCO-based ADC can be used to conduct the measurements. The resolution of the ADC needs to be 0.5 mV~1 mV with a 200 mV range to cover process variations as well as degradation. This ADC has been previously

designed and shown with hardware measurements to provide 0.05 mV resolution for the 200 mV range with less than 0.03 mm^2 area using 0.5μm technology [48].

3.3. Experimental Results of Class-C Oscillator

The efficacy of the proposed method is evaluated using 5 Ghz CMOS class-C LC oscillator shown in Fig. 3.14 (a), designed using IBM 180nm process technology. Fig. 3.14 (b) shows a photograph of the proposed class-C oscillator with chip area of 450 μm $\times$ 250 μm. Class-C configuration is the one biased so that the output current is zero for more than half of the input cycle, thereby yielding high efficiency at around 80% [49]. Class-C configuration is commonly used in high frequency sine wave oscillators. Class-C LC oscillator has been recently reported in literature [50-53]. The main advantage of this configuration is that class-C mode can achieve the phase noise improvement compared to the standard differential-pair LC oscillator for the same current consumption. The key features in the design are: 1) a large tail capacitance at the common source node of the differential pair filtering the high frequency noise from the tail current; 2) cross-coupled transistors working in a class-C configuration, enhancing efficiency; and 3) a minimum generation of noise for the cross-coupled pair [50].

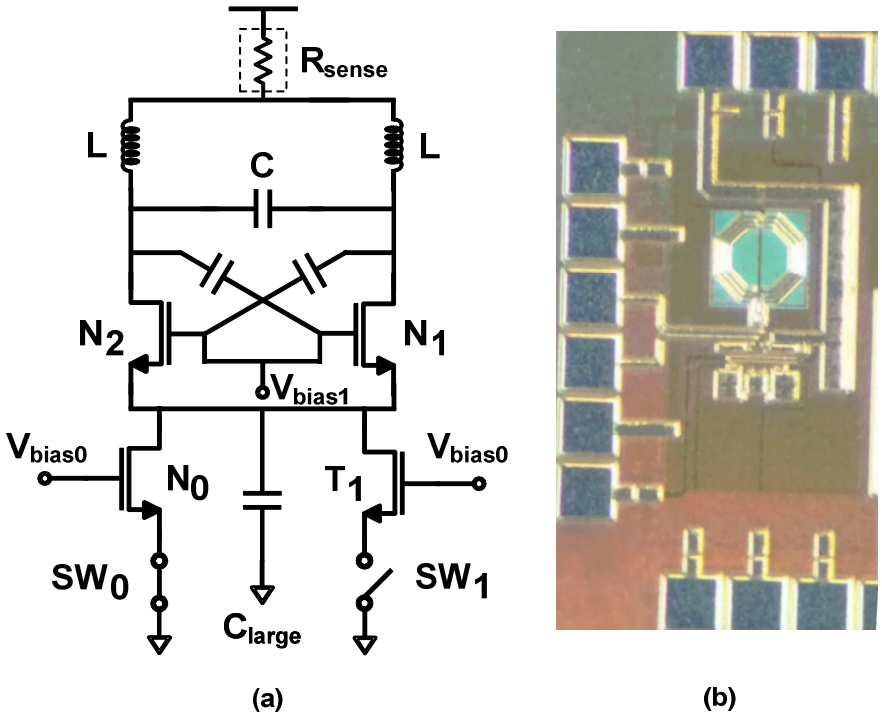

Figure 3.14. (a) Schematic of the Proposed Class-C Oscillator and (b) Die Photograph of the Proposed Design.

The specifications of interest are phase noise, output amplitude and DC voltage from the sense resistor. In the initial measurement shown in Fig. 3.15, the oscillator is operating with 1.35 mA tail current from a 1.8 V power supply. The oscillation frequency and the output power of class-C oscillator are measured using an Agilent N9020A spectrum analyzer. The phase noise measurement is conducted using an Agilent E5052A signal source analyzer. For reliability studies, accelerated aging approach have used under high temperature and voltage overstress [54], [55]. By using Arrhenius model, the test results generated at these stressed conditions are then extrapolated to nominal operation conditions. The fabricated chips are placed in stressed conditions with a temperature of 120°C and 20% of supply voltage overstress for total 300 hours, which

corresponds to approximately 3 years in normal operation conditions. The measurement results for the fabricated chip are summarized in Table 3.1.

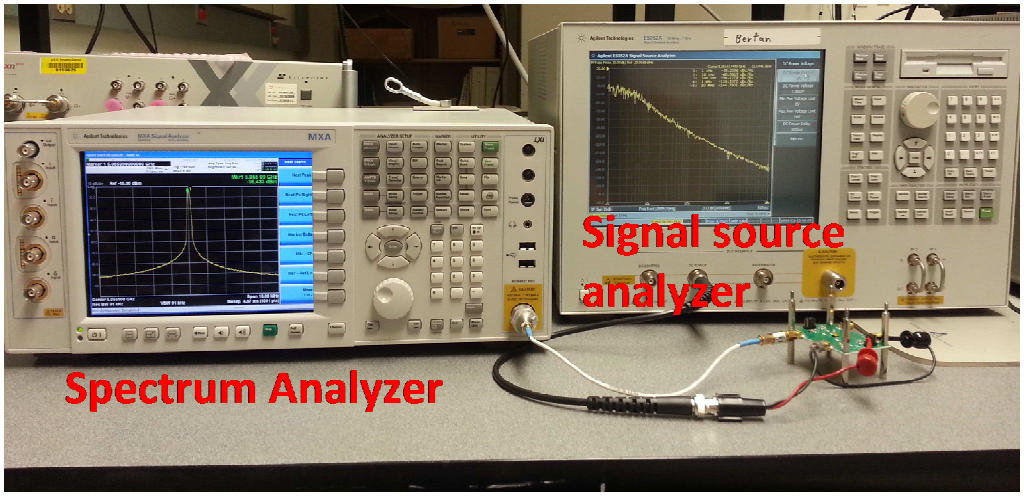

Figure 3.15. Initial Measurement Set-up.

Technology	IBM 7RF 180nm CMOS
Power Supply (nominal / stressed)	1.8 V / 2.2 V
Temperature (nominal / stressed)	55 °C / 120 °C
On-chip R_{sense} / power	9 Ω / 2.25µW
Oscillation frequency	5.054 GHz
Phase noise @ 1Mhz	–119.5 dBc/hz
Power consumption	2.7 mW
Chip area	0.11 mm^2

Table 3.1. Summary of Chip Measurements.

Initial performance measurements of the device consistently show –119.5 dBc/hz phase noise at 1 Mhz offset and about -13 dBm of output power. After 240 hours of stress which corresponds to about 2.5 years in nominal operation conditions, phase noise degrades by 1.5 dB and the output power degrades by 1.2 dB as shown in Fig 3.16. One of the manufactured boards is periodically monitored with a target of sustaining phase noise below –118 dBc/hz at 1 Mhz offset. It is determined that the monitor voltage needs to remain over 12.5 mV to sustain this phase noise performance. At 240 hours of stress, reconfiguration mechanism is activated when the monitor voltage falls below this point. It is observed that the oscillator performance is fully recovered after reconfiguration and follows the same degradation pattern up to 300 hours. Therefore, the lifetime of this device is enhanced from 240 hours to about 480 hours with extrapolation.

These measurement results are in full agreement with the simulations in terms of initial performance, degradation patterns, monitor voltage correlation to phase noise and output power, and the effectiveness of the recovery mechanism. In terms of area impact of the fabricated chip, the class-C oscillator occupies 0.11 mm^2 area and two switches, a sense resistor, and a spare transistor occupy 0.003 mm^2 area. Although an on-chip ADC is not implemented, it is necessary that the DC voltage from the sense resistor has to be measured by the ADC. The VCO-based ADC is fabricated separately and performances of this ADC are presented in [48]. For the area overhead analysis, the 180nm implementation of the ADC occupies 0.011 mm^2 area. Therefore, the overall area impact of the full monitoring and reconfiguration scheme is therefore estimated as 11% for this design.

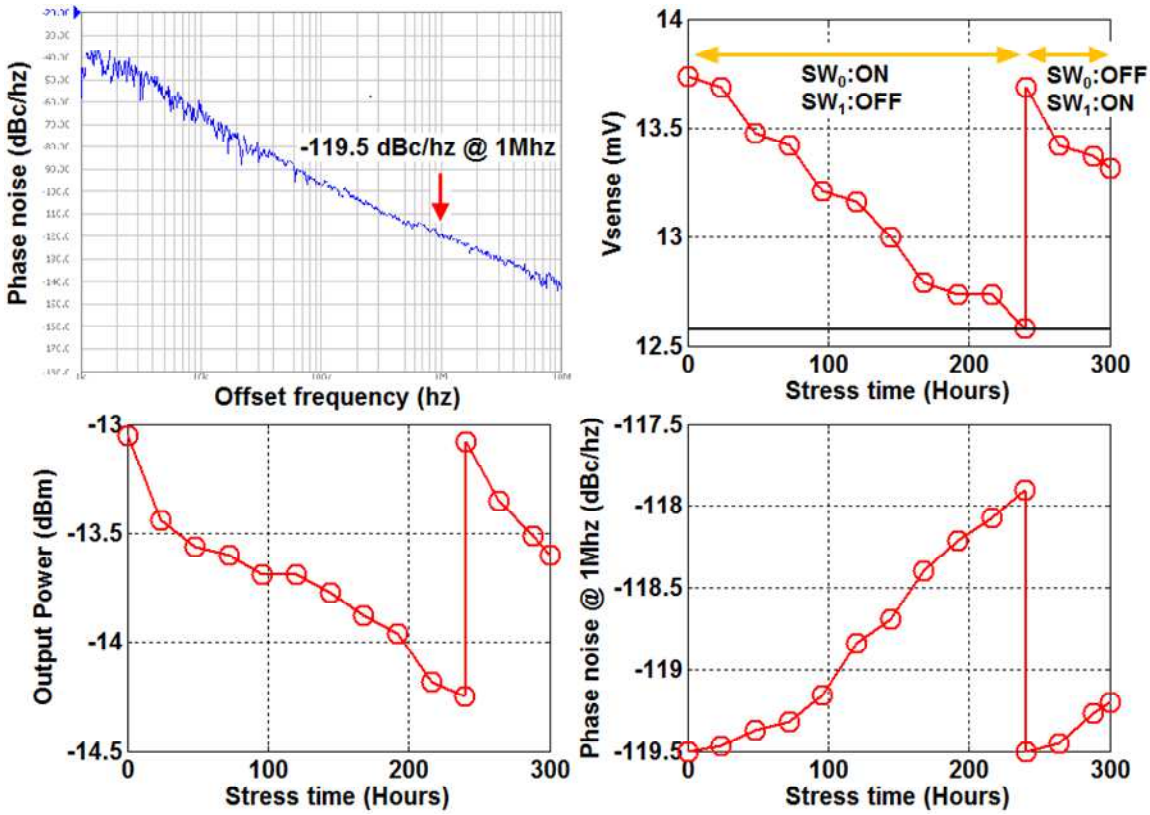

Figure 3.16. Measurement Results of Enhanced Lifetime Using the Proposed Method.

3.4. Conclusion

In this chapter, a method to enhance the lifetime of RF LC oscillators using in-field sensing and mitigation circuits is presented. This method includes hotspot identification to determine the weakest component, monitor/reconfiguration network design, and an algorithm to automatically swap the aged transistor with a new one. In the case study, the weakest component is identified as the tail transistor and this conclusion is explained through extensive analysis. A simple current-based monitor circuit is used to monitor performance degradation and activate the recovery process. The proposed technique is demonstrated on both N-type and P-type LC oscillators based on simulation.

Experimental results on a fabricated class-C oscillator show that if the circuits are designed with reliability as a part of the specification, lifetime can be enhanced with less than 11% area overhead.

CHAPTER 4

IN-FIELD RECOVERY OF RF CIRCUITS FROM WEAROUT BASED PERFORMANCE DEGRADATION

In this chapter, a methodology for enhancing the lifetime of RF circuits in the field using low-impact circuit level monitor and recovery techniques. The particular aging mechanism focusing on is hot-carrier injection (HCI) although the proposed method would work with any aging mechanism that can be modeled to enable simulations. Since the monitoring circuit is also prone to process variations, the monitoring mechanism is designed as a relative measurement, based on the amount of change in the monitor circuit output, rather than the absolute value. In order to demonstrate the concepts of reliability analysis and monitor and recovery circuit design, a generic LNA architecture is used as a case study.

4.1. Reliability Analysis and Hotspot Identification of Low Noise Amplifier

In order to demonstrate the in-field monitoring and recovery method, the low-noise amplifier (LNA) is chosen as a case study for RF circuits. LNAs are designed to provide sufficient amplification in the band of interest while maintaining a low noise figure. Aging will result in degradation of LNA performance in all aspects of its operation, ranging from DC bias to its noise figure. The goal is to monitor this degradation through simple means and take remedial action to recover the lost performance at a low hardware and almost no performance overhead.

4.1.1. Reliability Analysis of Low Noise Amplifier

In this section, the effect of aging is evaluated on critical LNA performance parameters including noise figure (NF), S-parameters (S11, S12, S21 and S22). The parameters S11, S22 are input and output reflection coefficients, and S21, S12, are forward and backward transmission coefficients. The common approach for designing a narrowband LNA is to use a common source topology with a cascode transistor, as shown in Fig. 4.1. For this LNA, the input impedance is approximately calculated by Eqn. (4.1) [56].

$$Z_{in} = j\omega(L_G + L_S) + \frac{1}{j\omega C_{GS}} + \frac{g_m}{C_{GS}} L_S \tag{4.1}$$

where ω is the frequency of operation, g_m is the transconductance of the input transistor M_1, and C_{GS} is the gate-source capacitance of the input transistor M_1. The real part of the LNA input impedance Z_{in} is adjusted using g_m and the source inductor L_S, while the imaginary part is removed at the resonant frequency using the gate inductor L_G.

The noise figure and the gain at the resonance frequency ω_o are obtained by Eqn. (4.2) and Eqn. (4.3) [56].

$$NF = 1 + \gamma g_m R_S \left(\frac{\omega_o}{\omega_T} \right)^2, \qquad \omega_T = \frac{g_m}{C_{GS}} \tag{4.2}$$

$$Gain(S21) = \frac{\omega_T}{2\omega_o} \cdot \frac{R_D}{R_S} = \frac{R_D}{2L_S\omega_o} \tag{4.3}$$

where γ is the noise coefficient, R_S is the source resistance, and R_D is the load resistance.

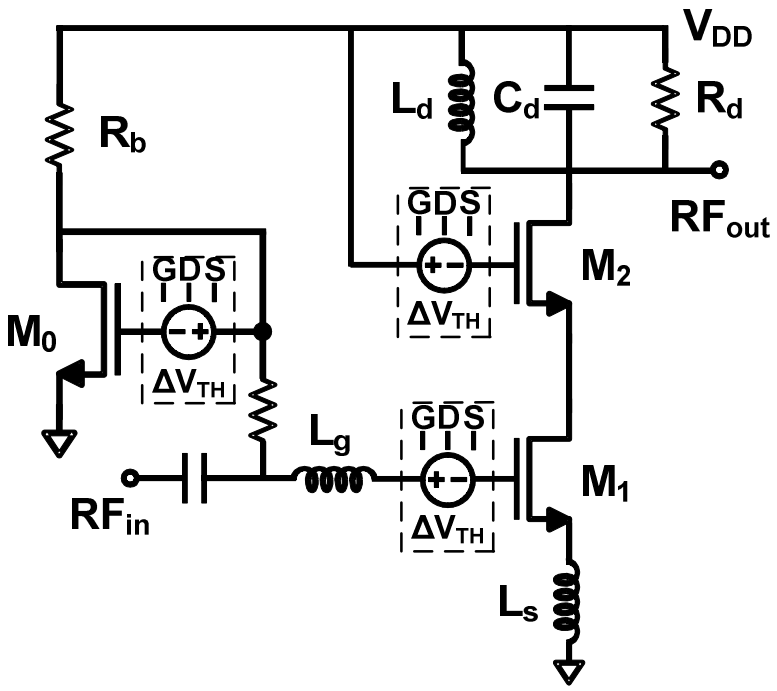

Figure 4.1. Schematic of Low Noise Amplifier with HCI Aging Models.

The performance of the LNA depends heavily on the transconductance of the input transistor M_1, which is determined by its threshold voltage and mobility, two parameters that degrade with HCI.

Threshold voltage shift is the main result of HCI effect. According to $g_m = 2\beta(V_{GS}\text{-}V_{th})$, the increase in threshold voltage due to HCI aging causes a decrease in g_m of the input transistor, which in turn also affects the real part of the LNA input impedance, Z_{in}. Therefore, the input matching (S11) varies after aging, which will change the gain and noise figure further. Fig. 4.2 shows the simulation results of a 2.4 GHz LNA for each specification before and after stress of 1 and 3 years. It is observed that a decrease in the gain (S21), an increase in the noise figure (NF), the input reflection coefficient (S11) and the output reflection coefficient (S22) between from 2.3 to 2.5 GHz frequency range.

Overall, the most significant degradation was observed in S11 and S21 at a single frequency 2.4 GHz used for Wi-Fi or Bluetooth applications.

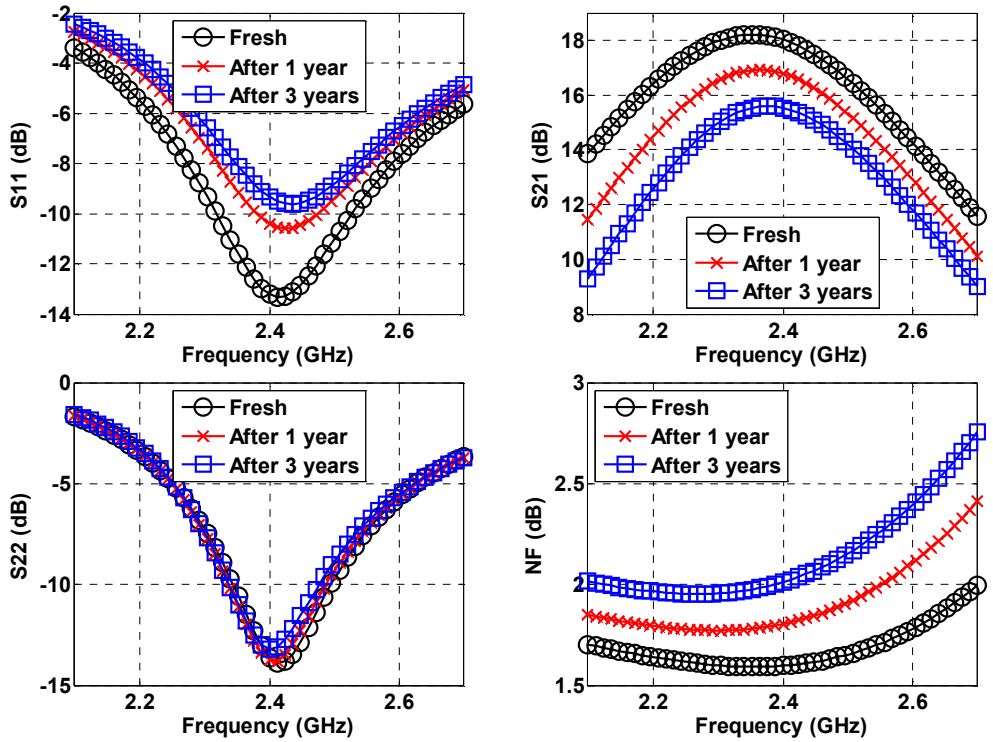

Figure 4.2. Performance Degradation Due to HCI Effect in Cascode LNA after 1 and 3 Years of Operation at the Room Temperature.

4.1.2. Hotspot Identification of Low Noise Amplifier

Reliability hotspot identification is performed to analyze the reliability impact of aging mechanisms on each individual component of the LNA. During reliability hotspot identification, one component is set to age over time, while others are kept at their initial state and performance degradation profiles are obtained. Comparing these degradation profiles, the circuit component that would result in the earliest failure time is identified as

the reliability hotspot. Note that the estimated lifetime in this step is not meaningful since in reality all devices age at the same time. However, reliability hotspot identification helps comparatively to analyze aging profiles to determine the lifetime limiting component [45]. Fig. 4.3 shows an overview of the hotspot identification method. The first step in the process is to conduct the reliability simulation on transistor-level circuit performances using the analytical aging model. The analytical aging model of each component is used to extrapolate the degradation of its parameters (e.g. threshold voltage) during operation time (e.g. years) based on nominal stress conditions. The extrapolated device parameters are used in the aging model in order to re-simulate the circuit and obtain the updated stress conditions. Hence, the performance of the circuit gradually shifts in time. Due to different sizes and operating points, the degradation patterns will be different for each circuit component. Thus, each circuit component will cause a distinct degradation profile for each circuit performance. This process iteratively goes through each circuit component and track the degradation profiles. Once all the degradation patterns are analyzed, it is possible to determine the most vulnerable component to aging effects.

For the hotspot identification of LNA shown in Fig. 4.1, there are three voltage sources $\Delta V_{TH0,1,2}$ at the gate of each n-type transistor to be considered as HCI effect. The results of degradation in threshold voltage and LNA performances during three years of stress time are shown in Fig. 4.4. This analysis indicates that the S11 will fail earliest due to the degradation in the input transistor M_1 based on the design specifications. This figure also shows that the other specifications (S21 and NF) are degraded much faster for the case of M_1 only. Hence, the input transistor M_1 is determined as the reliability hotspot.

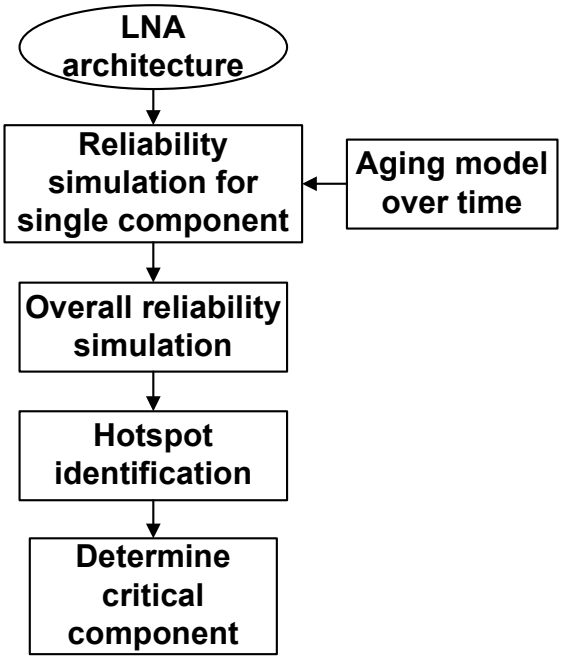

Figure 4.3. Flow of the Proposed Methodology for Hotspot Identification of LNA.

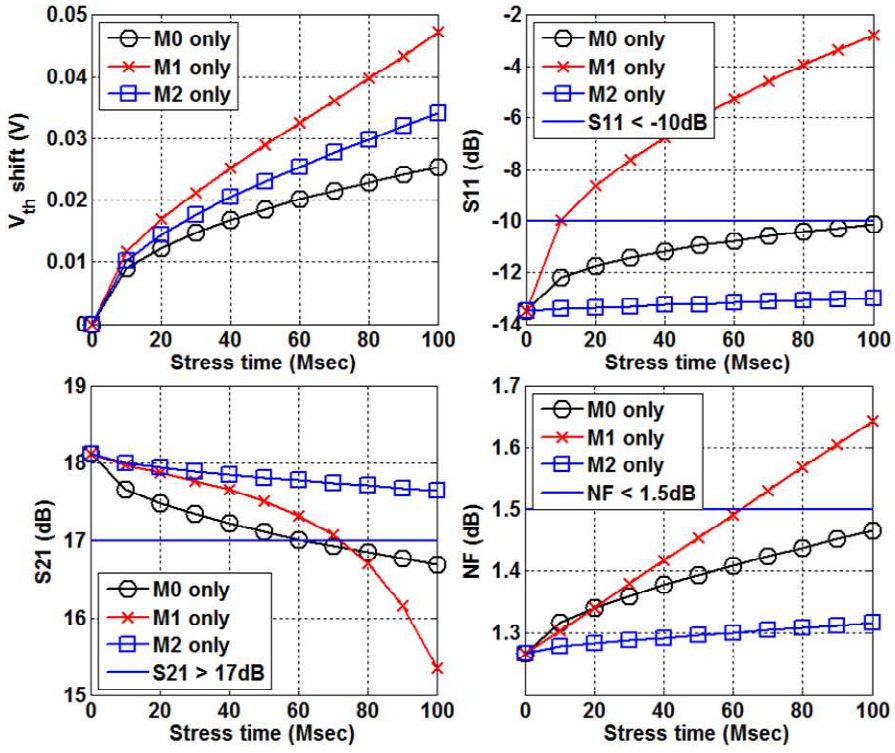

Figure 4.4. Hotspot Identification Results of LNA Due to HCI Effects.

4.2. In-field Lifetime Enhancement Method

In this section, the in-field lifetime recovery mechanism is presented to mitigate the degradation in circuit performance. Hotspot identification provides a way to determine critical components that need to be monitored for reliability. Noting that aging results in degradation of both mobility and threshold voltage, the most common symptom of aging is a reduced current (for voltage biased transistors) or an increased gate voltage (for current biased transistors). For DC monitoring, these two circuit variables can be used. In the LNA circuit, transistor M_1 is voltage biased; hence aging will result in degradation of the bias current.

On-chip monitors are subject to the same process variations as the primary circuit. Hence, the monitoring mechanism needs to be made relative with respect to a reference point. This can be achieved by measuring the monitor output once during production test and utilizing this value as a point of comparison for in-field measurements. Thus, instead of monitoring the absolute DC variables, the changes in these variables are monitored and those values are used to trigger recovery once significant change in the monitor variable is observed.

The recovery mechanism needs to restore the critical parameter that affects the performance of the device. This can be done in several ways: (a) swapping the degraded transistor with a fresh alternative, (b) enhancing the degraded transistor with smaller parallel transistors to recover drive capability, and (c) changing bias to recover the drive capability. Each solution presents with performance impact and the solution with the smallest performance impact should be selected. This can be achieved by using circuit simulation. As an example, for the LNA, option (a) significantly degrades noise figure

due to switches in the critical path, and option (b) shifts noise matching, again degrading noise figure. Option (c) can be enabled by changing bias voltage and does not have a significant impact on the LNA performance.

The proposed in-field reliability enhancement technique is shown in Fig. 4.5. The self-recovery procedure works as follows:

1) At design time, an in-field monitoring circuit is designed to generate a DC voltage correlated to the degradation in the performance of the device. A low speed analog-to-digital converter (ADC) converts this DC voltage to a digital code.
2) At production time, the monitor output as well as performance parameters are measured. The slack in the performance parameters are determined. A threshold for the monitor voltage is determined based on this slack.
3) In the field, the monitor circuit output is periodically measured (in a matter of weeks or months) and compared with the threshold to trigger the recovery mechanism.

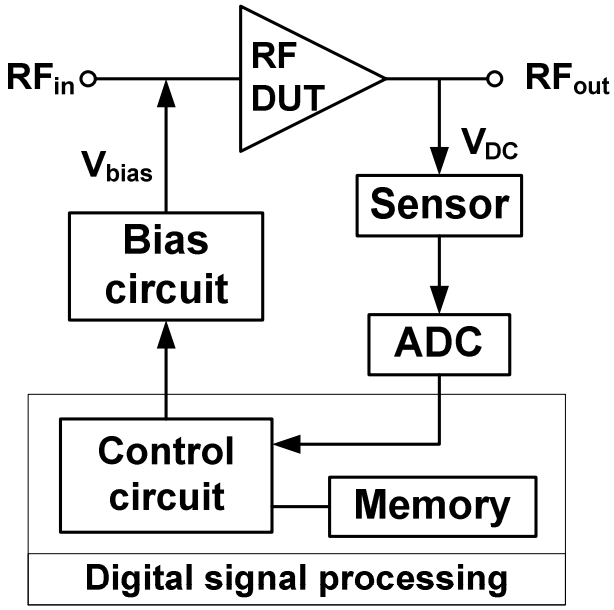

Figure 4.5. Proposed In-field Monitoring and Recovery Mechanism.

4.2.1. DC Monitor for In-field Monitoring

There are four important requirements for in-field monitoring circuitry. First, the monitor circuit should be non-invasive. Second, it should present with a small form factor. Third, the monitoring circuit should produce DC or low frequency response to enable low-cost measurements. Finally, the monitoring circuit should not significantly degrade due to aging itself.

At first sight, this problem resembles the built-in-self test (BIST) problem that has attracted a lot of attention recently. For instance, in [57][58], DC monitoring of the primary output is suggested to calculate specification parameters based on monitor response. However, there is an important distinction for the proposed method. In BIST, the goal is to replace production test with BIST measurements. This requires a monitoring circuit that has a response which is highly correlated to all the measurements.

Moreover, it requires an additional input source as a test stimulus to monitor the response for BIST measurements. The proposed method is different than BIST since it can make the monitoring mechanism relative to an initial point and does not require an input stimulus.

In order to satisfy the above-mentioned criteria, the proposed method provides a design of a simple voltage monitor that will provide an output that is correlated to the bias current/voltage of the most stressed transistor. This proposed in-field monitoring circuit is shown in Fig. 4.6 (a). This DC-based voltage sensor is composed of a source follower which can be operated as a voltage shifter with n-type MOSFET. The n-type MOSFETs are designed at a much lower width to limit the current that flow through it. The length of the monitor device is also much greater than minimum length as it is not concerned with high frequency operation. Hence, the monitor device experiences much slower aging compared to the hotspot transistor [10]. Fig. 4.6 (b) shows degradation in the monitor output voltage, V_{output}, due to HCI at several different lengths for the monitor devices. It is observed that at minimum length, the device experiences significant degradation. However, at L=325nm, the change in the monitor voltage due to the aging of the monitor device is negligible. Thus, the length of monitor devices are choose to L=325nm as a stable operation for the monitoring circuit. Note that there is no option to arbitrarily increase the length of the hotspot transistor, M_1, since it needs to be optimized for RF operation.

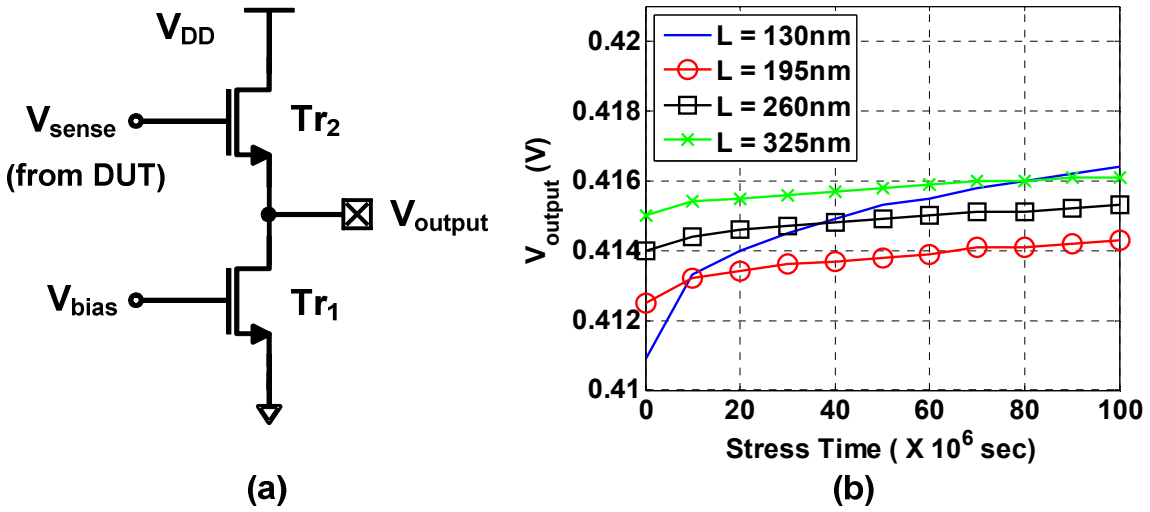

Figure 4.6. Proposed DC-based In-field (a) Monitoring Circuit and (b) DC V_{output} Voltage Variances under Various *L*.

4.2.2. Low-cost ADC and Bias Tuning Architecture for In-field Recovery

Another required component for in-field monitoring and recovery is the ADC to convert the output voltage of monitoring circuit into digital form. For this purpose, an open-loop Voltage Controlled Oscillator (VCO) architecture can be used [59]. The VCO is designed by adopting *N*-stage current starved inverters shown in Fig. 4.7 (a). The top and bottom transistors in each inverter stage make a current bottleneck during the transition. By controlling the bias voltage V_{VCO}, it is possible to adjust the current through each inverter stage, hence change the frequency. The equation used for determining the oscillation frequency is

$$f_{VCO} = \frac{I_D}{N \cdot C_{tot} \cdot V_{DD}} \tag{4.4}$$

where f_{VCO} is the VCO frequency at a given drain current I_D, N is the number of inverter stages and C_{tot} is the input and output capacitances of the inverter. In other words, the low cost VCO will convert an analog voltage signal to frequency domain by producing a continuous output signal whose frequency is proportional to the input voltage. Fig. 4.7 (b) shows the edge detector circuit for frequency to digital conversion (FDC). This operation can also be enabled by counting the VCO transitions within a given time window. The number of ones during a given measurement window in Fig. 4.7 (b) is proportional to the V_{VCO} voltage [60].

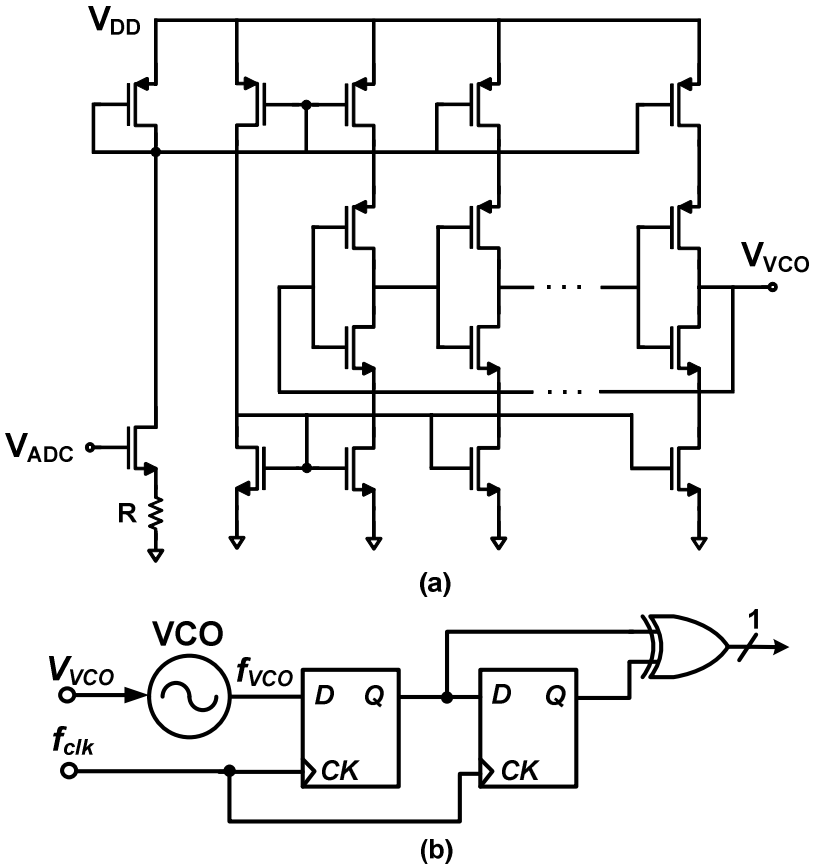

Figure 4.7. (a) Baseline VCO Architecture and (b) Block Diagram of Frequency-to-digital Converter (FDC) for 1-bit Quantization.

While the DC bias voltage is correlated to the performance of the LNA, the relation is non-linear. However, for small changes in the LNA performance, the change in the DC output is can be linearly correlated to changes in the LNA performance. Hence, the monitor output can be measured at production time and set a limit on it based on how much slack there is in the performance parameters of the LNA.

In order to set the threshold for triggering recovery, the VCO frequency as well as the slack in performance parameters are recorded at production time. Based on the allowable degradation in the bias current, the minimum VCO frequency and the corresponding counter value are determined. In the field, the counter result is directly compared with this threshold to trigger the recovery circuit. Since the input transistor is identified as the aging hotspot, the circuit parameters of this input transistor will be enhanced by the DC bias current. Fig. 4.8 shows the schematic of a tunable recovery circuit with an *N*-bit digital input signal. Resistors R_{b1} through R_{b3} are set to provide incrementally higher bias current. For each bias current level that is desired, the bias voltage is changed using the switch network. With digitally controlled signals, total bias current can also be determined by the binary weighted current source.

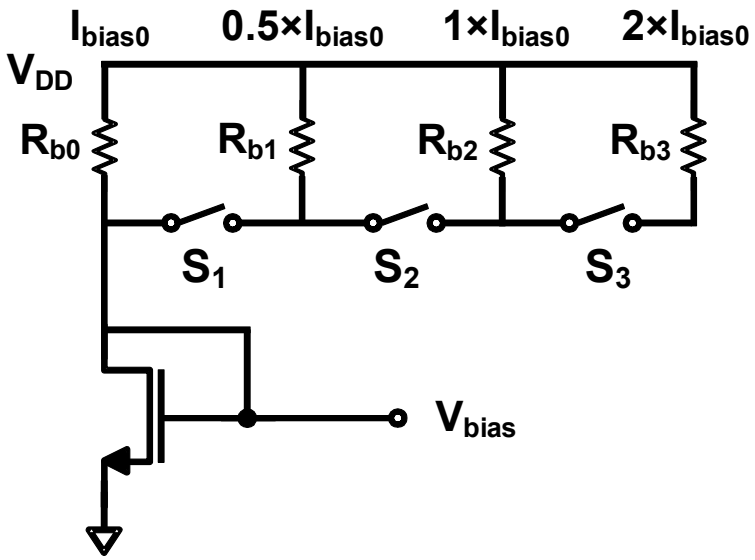

Figure 4.8. Proposed Tunable Recovery Circuit

4.3. LNA Case Study

The specifications for the LNA including gain, impedance matching, and noise figure, are shown in Table 4.1.

Specifications	S11	S21	S22	NF
Targets	< -10 dB	> 15 dB	< -10 dB	< 2 dB
Results @ 2.4GHz	-13.7 dB	18.2 dB	-14 dB	1.6 dB

Table 4.1. Specifications of Low Noise Amplifier.

4.3.1. In-field Monitoring

Using the hotspot identification method, it is determined that the highest performance degradation is due to transistor M_1. Also, it is identified that the degradation in LNA performances is primarily correlated to the bias condition of the input transistor

M_1. A sense resistor (R_{sense}) can be inserted into the current path of the input transistor M_1 for the monitoring purpose. It shows that the voltage across the sense resistor V_R is proportional to the drain current of the input transistor M_1.

The sense resistor need to be small enough to limit the performance impact and large enough to provide a measurable voltage. Since the degradation in performance can be alleviated to a large degree by co-design, the sense resistor value is set based on the resolution of the ADC. The compact VCO-based ADC provides 1mV of resolution. If a minimum of 0.3dB slack in the specification (e.g. the lowest acceptable initial gain is 15.3dB, while the absolute specification limit is 15dB) is allowed, the change in the voltage on the sense resistor due to 0.3dB degradation needs to be above the resolution of the ADC. Using this approach, it is determined that a sense resistor value of 13Ω is necessary for a drain current of 5mA.

Since the voltage on R_{sense} is small compared to V_{DD}, it is beneficial to shift this voltage down for measurement purposes. Fig. 4.9 also shows the monitoring circuit. Transistor M_4 is in common-drain configuration that essentially works as a level shifter to bring the baseline DC bias of the monitor voltage to a range that can be easily converted to the digital domain by a simple ADC. Fig. 4.10 shows the corresponding change in both sense voltage V_{sense} ($=V_{DD}–I_{DS}\times R_{sense}$) and the V_{output} voltage of the monitoring circuit through the same stress period.

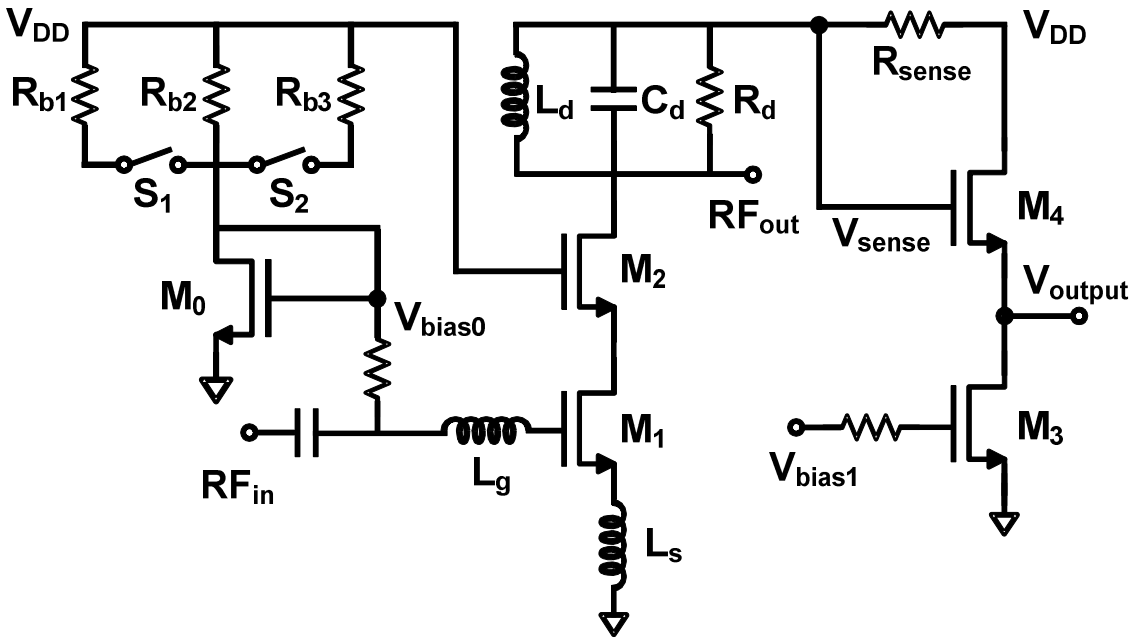

Figure 4.9. Cascode LNA Schematic with Monitoring and Tunable Bias Circuits for Recovery Process.

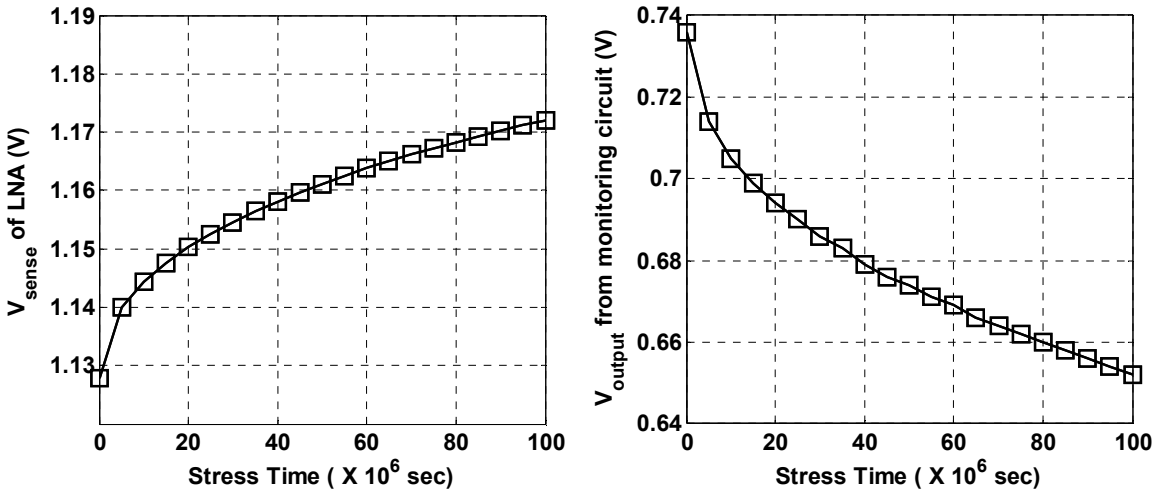

Figure 4.10. DC Voltage (V_{sense} and V_{output}) Changes versus Stress Time.

Fig. 4.11 shows the degradation in S-parameters (S11, S21 and NF) at 2.4 GHz and the bias current of LNA through approximately 3 years of stress time. It can be observed that there is a strong correlation between the degradation profiles of specifications (S-parameters and current/voltage) and DC voltage from the sensor. Fig. 4.12 shows Monte Carlo simulation results for the degradation in critical performance parameters and the monitor voltage. N_{one} represents the number of ones from the FDC. Although there are slight deviations, the monitor voltage tracks performance parameters closely. Once the initial values of the monitor voltage and performance parameters are determined, the relative slack in circuit performances can be reflected on the monitor voltage to determine the threshold for triggering the recovery circuit. For instance, if the gain specification has 15% slack (i.e. the measured gain is 15% above the specification limit), a 15% slack on the monitor voltage can be imposed as well. By using the measured specifications as reference, the recovery mechanism is tailored with respect to the characteristics of each manufactured device. Hence, this simple monitoring circuit can be used for detecting degradation in a process-robust manner.

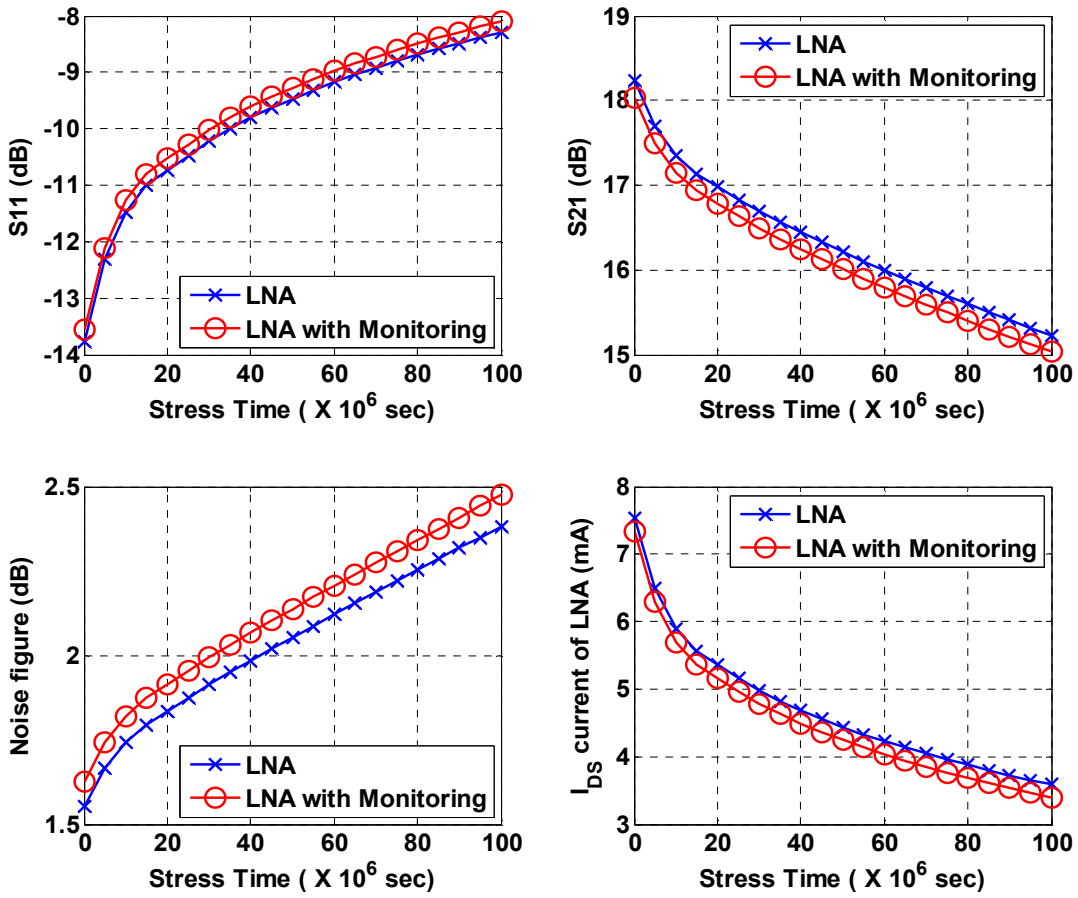

Figure 4.11. S-parameters and Bias Current Degradations versus Stress Time.

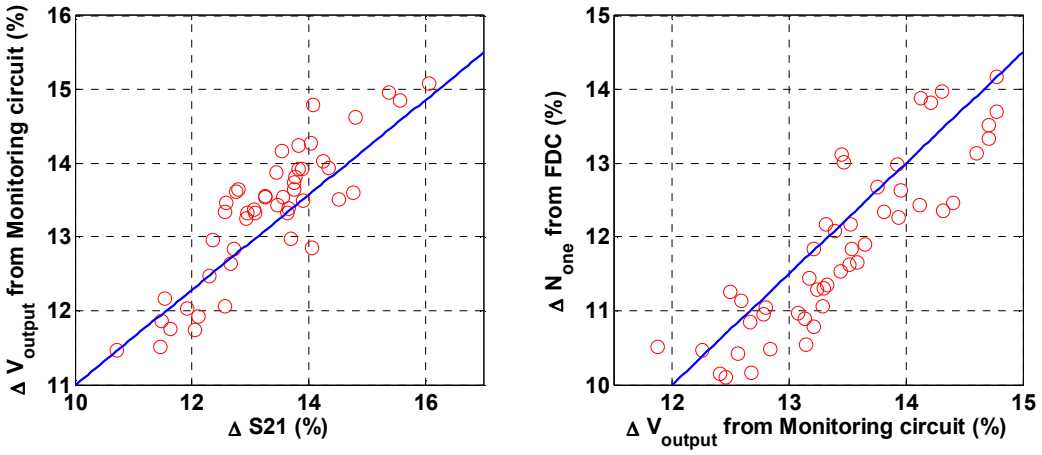

Figure 4.12. Correlation Between Circuit Performances from Monte Carlo Simulation of 50 LNAs after 3 Years under Nominal Stress Conditions.

It is also necessary to confirm that the monitoring circuit does not cause significant performance degradation. In the Fig. 4.9, the sense resistor is in series with the LC tank, degrading its Q. Therefore, the gain of the LNA (S21) will be degraded. The noise figure is also degraded slightly due to the presence of the resistor. However, there is no significant change in S11 as expected from Eqn. (4.1). Therefore, in this configuration, it is possible to co-design the LNA with the resistor using the Eqn. (4.3) for gain (S21). When the LNA is redesigned, by adjusting the values of drain inductor and capacitor by less than 15%, it is possible to achieve gain almost identical to the one in the absence of the resistor. Fig. 4.11 also shows circuit performance parameters with and without the sense resistance. The sense resistor can be determined by the value of few tens of ohm to reduce the impact on noise figure. It can be observed that the degradation due to the sense resistor is negligible and well within process variations.

To convert the sense voltage to the digital domain, a simple VCO-based FDC is used with a dynamic range that covers the monitored output voltage range, including process variations and expected degradation amount. The measured tuning characteristics of the VCO are shown in Fig. 4.13. In order to use the linear range of the tuning curve, the full-scale analog input voltage from monitoring circuit is set to 0.5~0.8V, which is corresponds to 5~35 MHz of output frequency. Fig. 4.13 also shows the number of digital bits from the counter. The counted values provide the mapping information between the V_{sense} voltage of LNA and output frequency of the VCO.

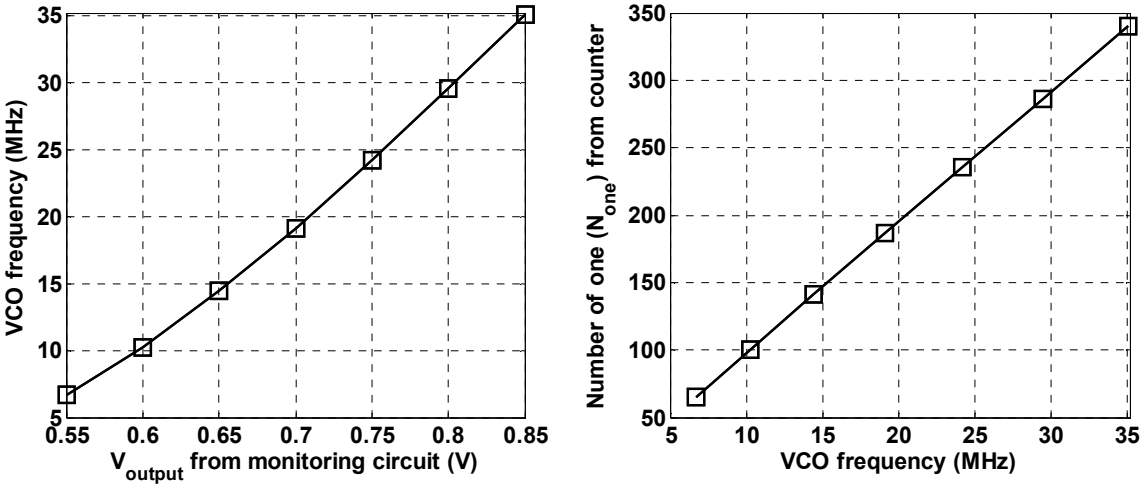

Figure 4.13. Characteristics of a VCO-based FDC.

4.3.2. In-field Recovery

Once the LNA is characterized in terms of S11, S21, and NF, and the monitor voltage, during the production time, the proposed recovery circuit can prolong the lifetime of LNA. The threshold for triggering the recovery mechanism is determined at production time based on the available slack. In the field, the proposed monitor circuit is activated periodically (via V_{bias1}) and the VCO frequency is measured by the counter. If the counter falls below the determined threshold, the bias current is enhanced by activating switches (S_1 or S_2). The entire monitoring and recovery mechanism is simulated for in-field wearout. The results of these simulations are shown in Fig. 4.14. For the initial circuit, it is determined that minimum slack is in S21, corresponding to 15% slack in the monitor voltage and set this counter value to 144. It can be observed that at about 20×10^6 seconds, the recovery circuit is triggered. At that point, both S21 and S11 parameters are slightly below their specified values (less than 0.1dB below). With the activation of the recovery circuit, all parameters recover to their initial states. At 82×10^6

seconds, the recovery mechanism is activated again, where S21 and S11 are right at specified limits and they recover again to the initial states. Hence, the lifetime of the LNA is enhanced from 20×10^6 seconds to at least 82×10^6 seconds using two switches in the recovery circuit.

Because of the increase in V_{bias0} voltage applied at gate of aged input transistor after the failure, the degraded parameters can be compensated and will mitigate the performance degradation. In other words, increase of the bias current of stressed transistor will recover the degraded performances, such as gain and input matching because transconductance can be compensated to the initial value.

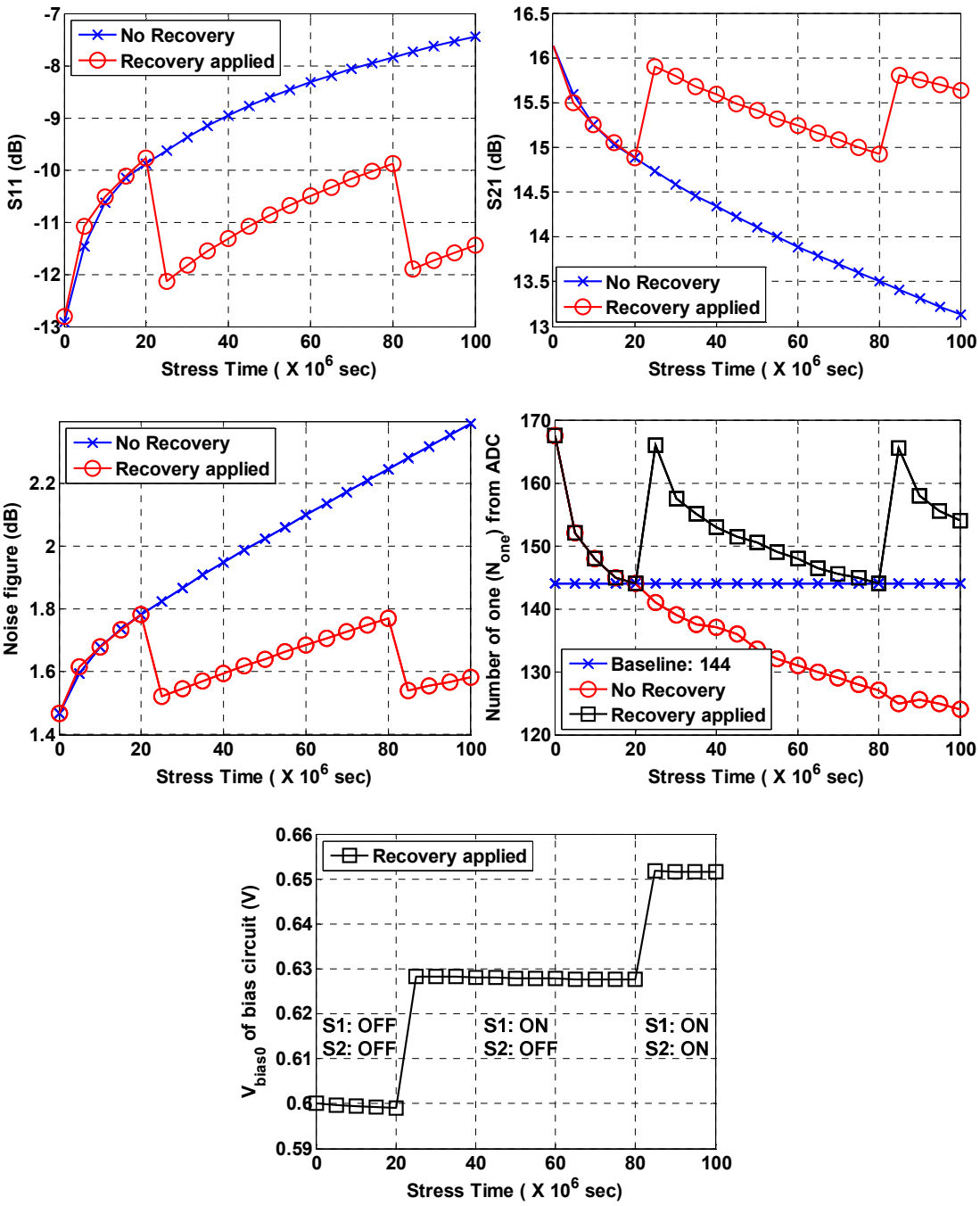

Figure 4.14. Simulation Results of Enhanced Lifetime Using the Proposed Recovery Technique.

Area overhead is usually a concern in in-field recovery mechanisms. In the proposed technique, the monitor transistors are very small compared to the LNA. The VCO-based FDC is composed of 7 inverter stages and digital blocks, and a small bias stage and digital control is achieved by CMOS switches and a small comparator circuitry. The area overhead is estimated including all of the necessary components to be below 15% of the area of the LNA.

4.4. Experiment Results

The efficacy of the proposed lifetime enhancement method is evaluated using 2.4 GHz CMOS cascode LNA. This LNA is manufactured using IBM 180nm process technology. Fig. 4.15 shows a photograph of the LNA and in-field monitoring/recovery circuits with a chip area of 1mm × 1mm. A VCO-based FDC with 7 inverter stages is also implemented for the measurement of the voltage from the monitoring circuit. The oscillation frequency can be measured with the range of 10 ~ 40 MHz. The measured transfer characteristics of the FDC are shown in Fig. 4.16. The average number of ones (N_{one}) is compared to the target value (S21 specification) predetermined through simulation data. Therefore, by adjusting the digital control bits in the tunable bias circuit connected to the LNA, the bias voltage of input transistor of LNA is increased to the optimized value satisfying S21 specification.

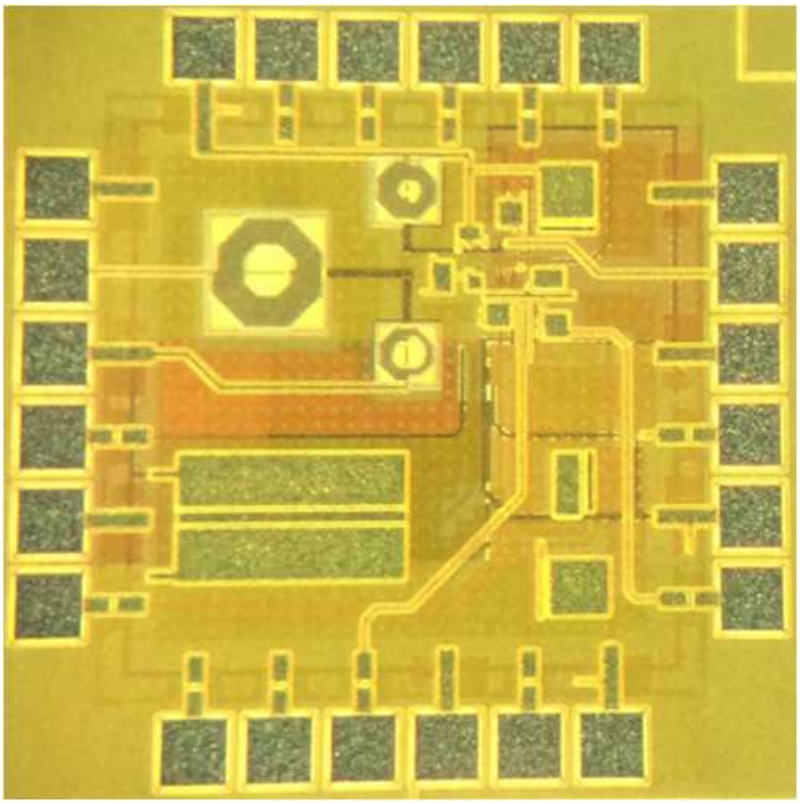

Figure 4.15. Die Photograph of the Proposed Design.

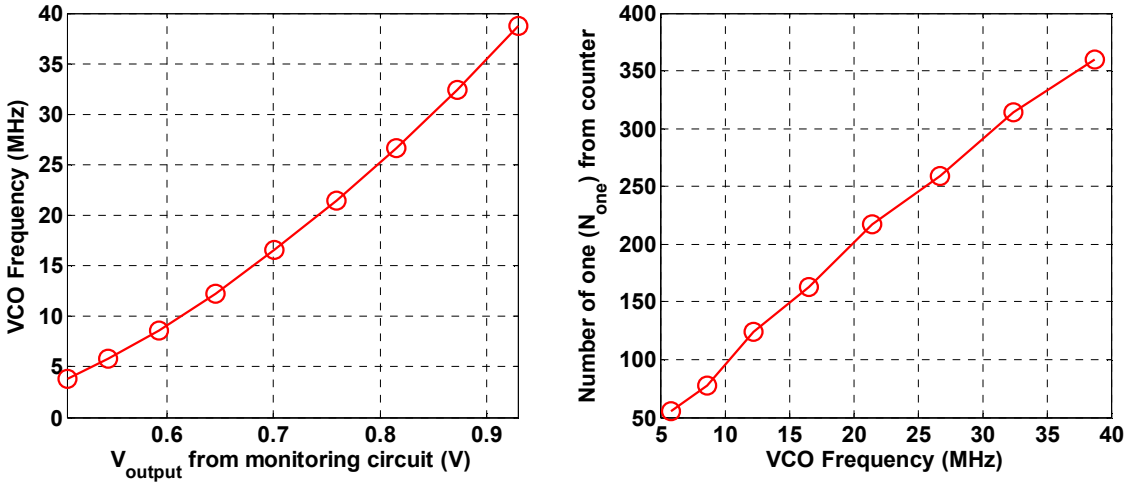

Figure 4.16. Measured Characteristics of a VCO-based FDC.

For reliability studies, accelerated aging approach under high temperature and voltage overstress is conducted [54], [55]. By using Arrhenius model, the test results measured at these stressed conditions are then extrapolated to nominal operation conditions. The fabricated chips are placed in stressed conditions with a temperature of 120°C and 20% of supply voltage overstress for a total of 400 hours, which corresponds to approximately 4 years in normal operation conditions. The measurement results for the fabricated chip are summarized in Table 4.2.

Technology	IBM 7RF 180nm CMOS
Power Supply (nominal / stressed)	1.8 V / 2.2 V
Temperature (nominal / stressed)	55 °C / 120 °C
On-chip R_{sense}	13 Ω
Power consumption	14.7 mW
Chip area	1mm × 1mm

Table 4.2. Summary of Chip Measurements.

Initially, the gain of the LNA is measured as 16.5dB at 2.4 GHz. After 200 hours of stress, which corresponds to about 2 years in nominal operation conditions, gain degrades by 1.5dB as shown in Fig 4.17. One of the manufactured boards is periodically monitored with a target of sustaining gain above 15 dB. From the measurement, it is chosen that the voltage V_R needs to remain over 60 mV which corresponds to 15% reduction from the initial value. At 220 hours of stress, the recovery mechanism is

activated. At this point, it is also observed that the gain of the LNA has fallen to 14.8dB (0.2dB below spec). Once the recovery mechanism is activated, the gain of the LNA is restored back to 16.3dB. Same pattern repeats with another recovery trigger at 400 hours. Again, the gain is recovered to near its initial value. While the experiment is stopped at this point, it shows a similar degradation pattern and estimates that the final failure will occur at 600 hours. This corresponds to a 3-fold increase in the lifetime of the LNA by using two supplemental bias transistors.

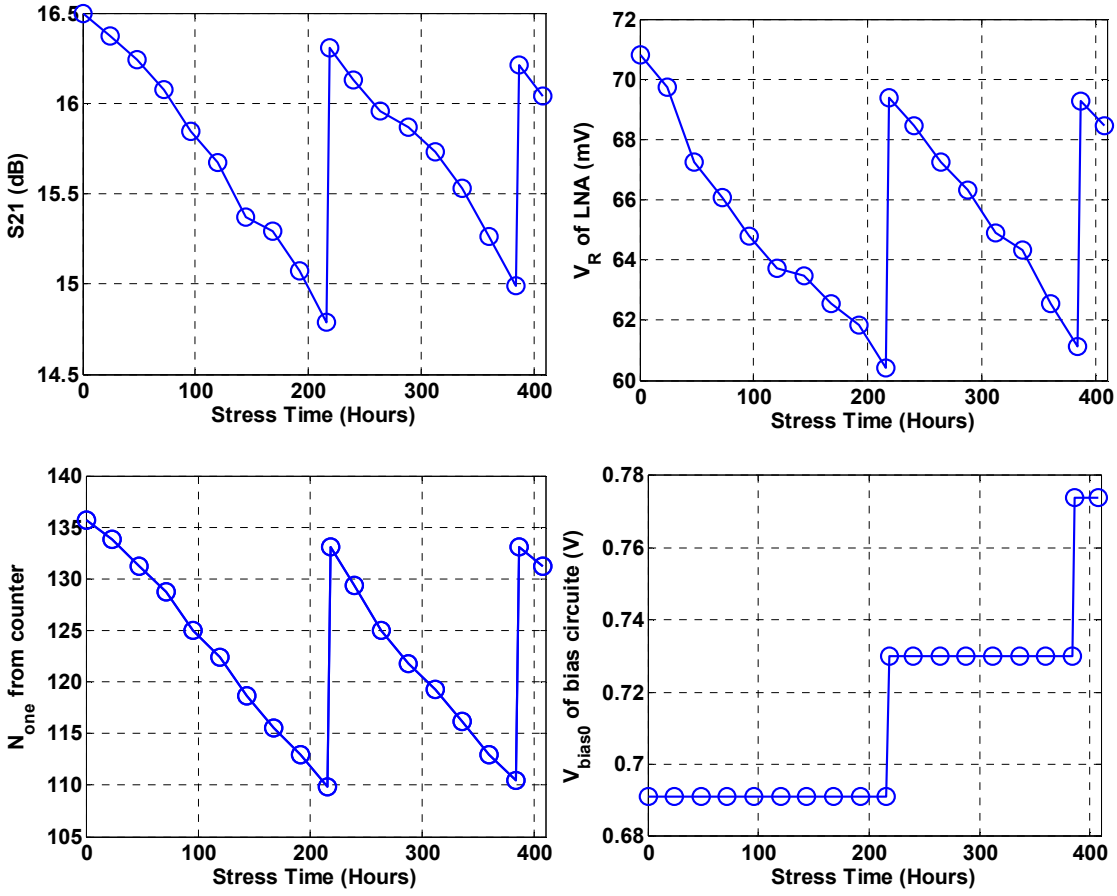

Figure 4.17. Measured Results of Enhanced Lifetime Using the Proposed Recovery Technique.

4.5. Conclusion

In this chapter, a method to enhance the lifetime of RF circuits in the field using simple on-chip monitor and recovery circuits is presented. While the HCI effect is focused on aging analysis, the proposed method is generally applicable to other degradation mechanisms. During the method, a simple monitor circuit is designed based on the principles of observing the important bias conditions so that similar degradation effects can be observed while keeping the current consumption as small as possible. The monitor circuit generates a DC output voltage, the degradation in which has a very strong correlation to the degradation of performance specifications. Finally, the technique is demonstrated on an LNA as a case study. Experimental results on a fabricated CMOS cascode LNA show that the proposed method can enhance the lifetime of the LNA 3-fold with less than 15% area overhead.

CHAPTER 5

SUMMARY AND CONCLUSION

In this dissertation, in-field monitoring and recovery technique for enhancing the lifetime of RF circuits which performances are degraded due to aging effects.

Firstly, a methodology to analyze the performance of RF circuits degraded by aging mechanisms, such as HCI, NBTI and EM is proposed to identify the device that is most critical for circuit performance degradation. Once the critical device of RF circuits is determined from hotspot identification, design-time optimization method can be taken to mitigate the circuit performance degradations. Hence, component-centric lifetime enhancement can be done using established techniques by adjusting the component design parameters. It shows the demonstration of the proposed technique on an LNA and two LC oscillators as case studies. Experimental results show that the degradation performance and the lifetime were enhanced by increasing the critical transistor size or widening the inductor line. The methodology should be applied to the particular design at hand to fully gauge the impact of aging effects.

After the hotspot identification is conducted in aged RF circuits, a method to enhance the lifetime of RF LC oscillators using in-field sensing and mitigation circuits is presented. This method includes hotspot identification to determine the weakest component, monitor/reconfiguration network design, and an algorithm to automatically swap the aged transistor with a new one. In the case study of LC oscillator, the weakest component is identified as the tail transistor and this result is explained through extensive analysis. A simple current-based monitor circuit is used to monitor performance

degradation and activate the recovery process. The proposed technique is demonstrated on both N-type and P-type LC oscillators based on simulation. Experimental results on a fabricated class-C oscillator using IBM 7RF 180nm technology show that if the circuits are designed with reliability as a part of the specification, lifetime can be enhanced with less than 11% area overhead.

Finally, another method to enhance the lifetime of RF circuits in the field using simple on-chip monitor and recovery circuits is presented. While the HCI effect is focused on aging analysis of MOSFET, the proposed method is generally applicable to other degradation mechanisms. During the method, a simple monitor circuit is designed based on observing the bias conditions of hotspot device so that similar degradation effects can be observed from the monitored output parameters while keeping the current consumption as small as possible. The monitor circuit generates a DC output voltage, the degradation in which has a very strong correlation to the degradation of performance specifications. The recovery circuit adjusts the bias current of the hotspot device in RF circuits in order to mitigate the performance degradation. The proposed technique is demonstrated on an LNA using IBM 7RF 180nm technology as a case study. Experimental results on a fabricated CMOS cascode LNA show that the proposed method can enhance the lifetime of the LNA 3-fold with less than 15% area overhead.

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