Load Sharing Low Dropout Regulators Using Accurate Current Sensing

by

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ABSTRACT

The growing demand for high performance and power hungry portable electronic devices has resulted in alarmingly serious thermal concerns in recent times. The power management system of such devices has thus become increasingly more vital. An integral component of this system is a Low-Dropout Regulator (LDO) which inherently generates a low-noise power supply. Such power supplies are crucial for noise sensitive analog blocks like analog-to-digital converters, phase locked loops, radio-frequency circuits, etc. At higher output power however, a single LDO suffers from increased heat dissipation leading to thermal issues.

This research presents a novel approach to equally and accurately share a large output load current across multiple parallel LDOs to spread the dissipated heat uniformly. The proposed techniques to achieve a high load sharing accuracy of 1% include an innovative fully-integrated accurate current sensing technique based on Dynamic Element Matching and an integrator based servo loop with a low offset feedback amplifier. A novel compensation scheme based on a switched capacitor resistor is referenced to address the high 2A output current specification per LDO across an output voltage range of 1V to 3V. The presented scheme also reduces stringent requirements on off-chip board traces and number of off-chip components thereby making it suitable for portable hand-held systems. The proposed approach can theoretically be extended to any number of parallel LDOs increasing the output current range extensively. The designed load sharing LDO features fast transient response for a low quiescent current consumption of 300μA with a power-supply rejection of 60.7dB at DC. The proposed load sharing technique is verified through extensive simulations for various sources and ranges of mismatch across process, voltage and temperature.

DEDICATION

To my inspiring parents, my amazing brother,

and my dear friends,

without whom none of my success would be possible!

ACKNOWLEDGMENTS

First of all, I want to sincerely thank to my advisor and chair, Prof. Bertan Bakkaloglu for granting me an opportunity to work on this challenging research project. His guidance and encouragement throughout my journey here both technically and emotionally has been invaluable. His constant motivation and humble attitude has been a key driving factor for me to pursue research.

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My special thanks to Sanjeev, Keith, Chizim and the entire group of Texas Instruments for this amazing opportunity to work on this innovative project for state of the art power management circuits. Their experienced inputs through technical discussions and reviews have been very helpful in shaping this project.

I would like to convey my heartfelt gratitude to Raveesh for all his technical support and guidance. The countless number of technical discussions which I have had with him over the course of this project have been invaluable. I also like to thank all my research colleagues Dr. Debashis, Shrikant, Kishan, Navankur, Ming, Venkatesh, Ashwath, Prasanna and Parisa for their constant encouragement and friendship. I would also like to extend warm thanks to my roommates Abhinav, Kartik, Ritwik and Loy for their constant support and affection.

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CHAPTER 1

INTRODUCTION

A fundamental demand of all integrated circuits (ICs) is to ensure high quality power to support power efficient systems. The exploding number of features on ICs especially employed in high performance portable electronic devices is rapidly adding to the amount of processing power. As a result, devices are getting more power thirsty to an extent that power consumption and thermal issues become major limiting factors. The power management of such handheld battery-powered devices is thus becoming increasingly vital.

One of the key components of such a power-management system is a Low-Dropout Regulator (LDO). LDOs suitable for on-chip integration have recently been proposed [1][2][3], and inherently generate a low-noise & virtually zero ripple power supply exhibiting fast load regulation over a wide range of current loads and process, voltage, and temperature (PVT) variations. LDOs are thus the preferred choice of regulators for noise sensitive applications such as analog-to-digital converters, phase locked loops, etc. and precise medical instruments.

1.1 Motivation

The motivation for this research project stems from the fact as the load current increases, the heat dissipation of LDO increases significantly. It is absolutely vital to spread this heat to avoid thermal breakdown. Also considering an application in a portable battery-powered device application, a large heat sink is virtually impossible to realize.

Parallelizing multiple LDOs can alleviate this thermal concern by spreading the heat across the board. This technique is highly useful in a portable system where high output power supply with low noise is desired.

1.2 Challenges

The most compelling challenge associated with any parallel operation is ensuring balance of each individual operation. Similarly, the challenge associated with multiple LDO operation is to equate the output current of each individual LDO. Due to on-chip and off-chip mismatch [4], there will be a certain degree of mismatch in the performance of each individual LDO. The target is to ensure that the load currents are accurate within 1% of each other at full load. Avoiding thermal runaway wherein a single LDO hogs the entire load current is the crux of this research.

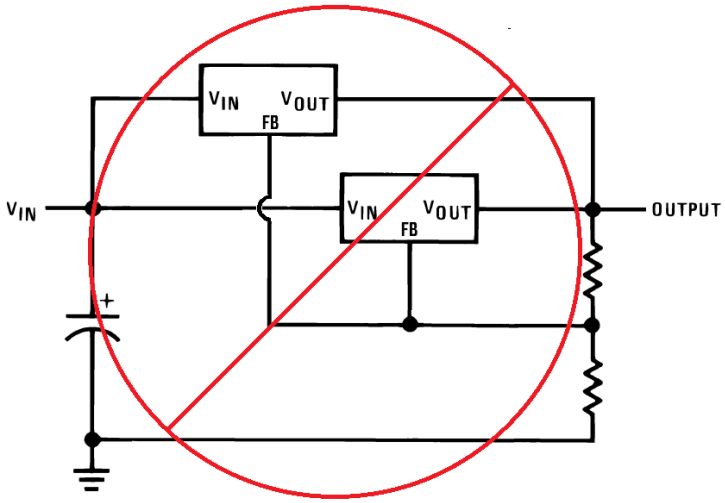


Fig 1.1 Simple Parallelizing of LDOs – A flawed approach [5]

1.3 Previous Work

There are a few industry solutions by Texas Instruments [5] and Linear Technology [6][7] for parallel LDO operation.

The Texas Instruments solution [5] employs the use of two TPS74401 LDOs each capable of supplying 3A for a total of 6A. It also requires the usage of many other components such as an external high precision amplifier (OPA333) and sense resistors to solve the problem of load sharing as shown in Fig. 1.2.

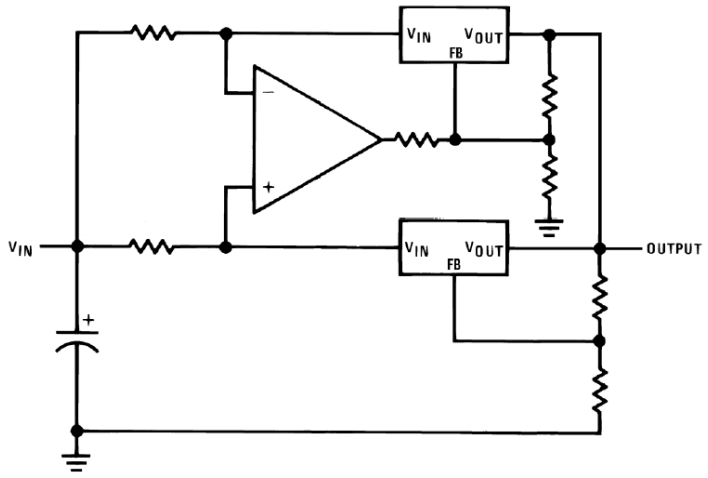


Figure 1.2 Control sharing solution by Texas Instruments [5]

In [6] as well, two LT3056 voltage based LDOs are paralleled albeit with an additional overhead of an amplifier and matched copper traces on PCB as shown in Fig. 1.3. It also shows 2 LT3081 current based LDOs with an additional requirement of matched copper PCB traces.

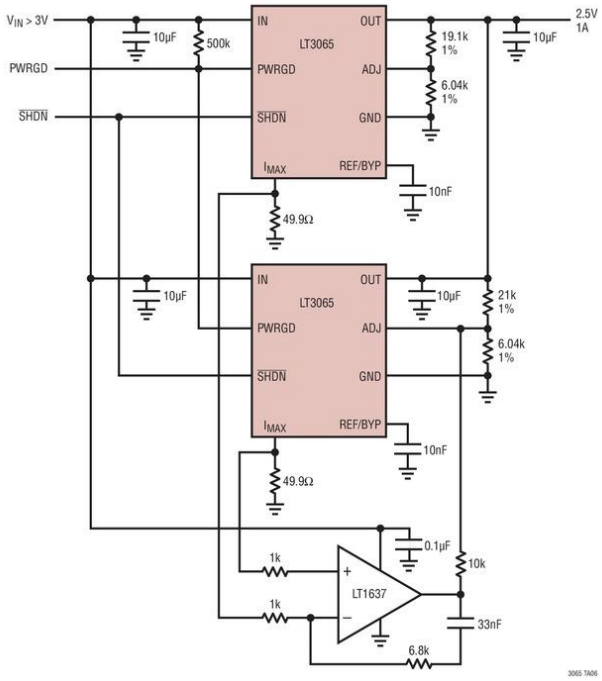


Figure 1.3 Using LDO Current Limit to Balance Shared Current by Linear Technology [6]

All the above techniques require either additional components or have stringent restrictions on their PCB layout. They are also based on a master-slave approach which has the potential to break down.

The focus of this research is to ensure simple PCB level connectivity for the end user and a scheme that can be extended to theoretically any number of parallel LDOs.

1.4 Thesis Outline and Organization

This research thesis report is organized into 5 chapters.

Chapter 1 establishes the need for load sharing LDOs, the challenges associated with it and summarizes some previous work.

Chapter 2 presents an overview of the load sharing system to be developed. It introduces the novel techniques employed to achieve the target set of specifications.

Chapter 3 gives the detailed description of all the novel techniques introduced in the earlier chapter and forms the core of this report. It gives the details of the circuit level implementation of each block within the LDO.

Chapter 4 captures all the simulation results of the developed load sharing scheme under various test cases and scenarios.

Chapter 5 concludes the report and reflects on future areas of improvement to the proposed scheme.

CHAPTER 2

SYSTEM OVERVIEW OF LOAD SHARING LDO

2.1 Overview

The major challenge associated with a parallel system of LDOs is equating the output current of each individual LDO. The primary idea is to generate an error proportional to the difference of the output current of each LDO and then correct for this error by modulating the feedback voltage of each individual LDO.

To enable generation of this error, 2 extra pins for current sensing and monitoring (ISENS & IMON) are required in addition to the conventional pins of a LDO (VIN, VOUT VSS and VREF). A top-level view of the proposed scheme of 'n' parallel LDOs connected in a daisy-chain is shown below in Fig. 2.1.

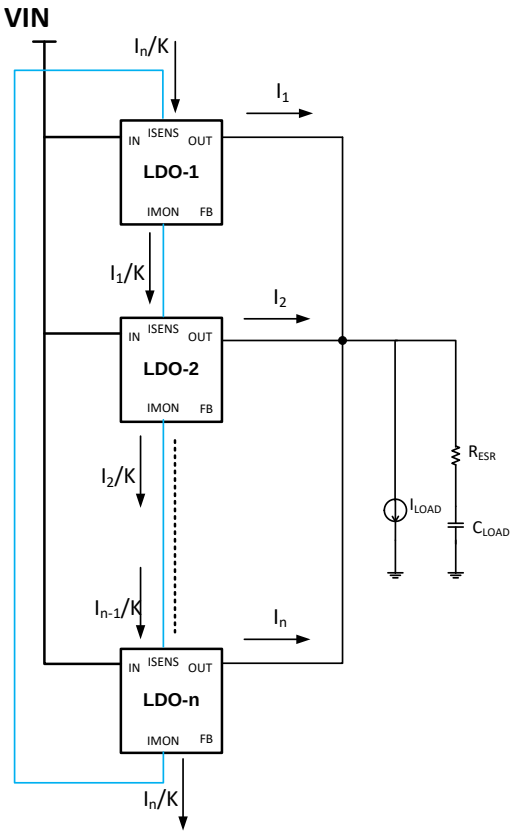


Figure 2.1 Top Level View of 'n' parallel LDOs

2.2 Proposed Solution

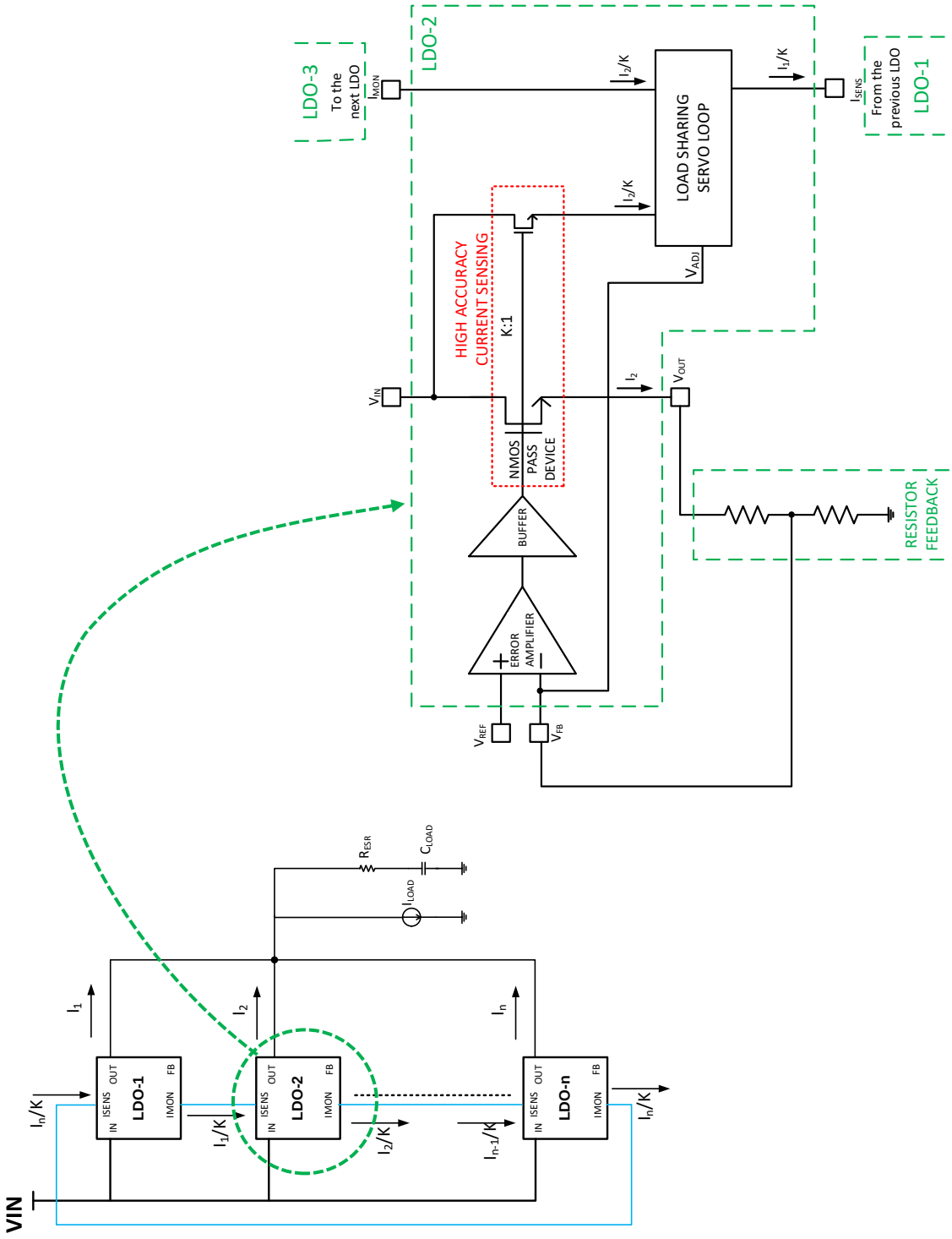


Figure 2.2 Block level implementation of each LDO

2.2.1 LDO Core Loop

The LDO core loop refers to the negative feedback loop that regulates the output voltage of the LDO. The major blocks of this LDO core loop are the error amplifier, buffer, a NMOS pass device, feedback series resistors, and a bandgap voltage reference (externally placed).

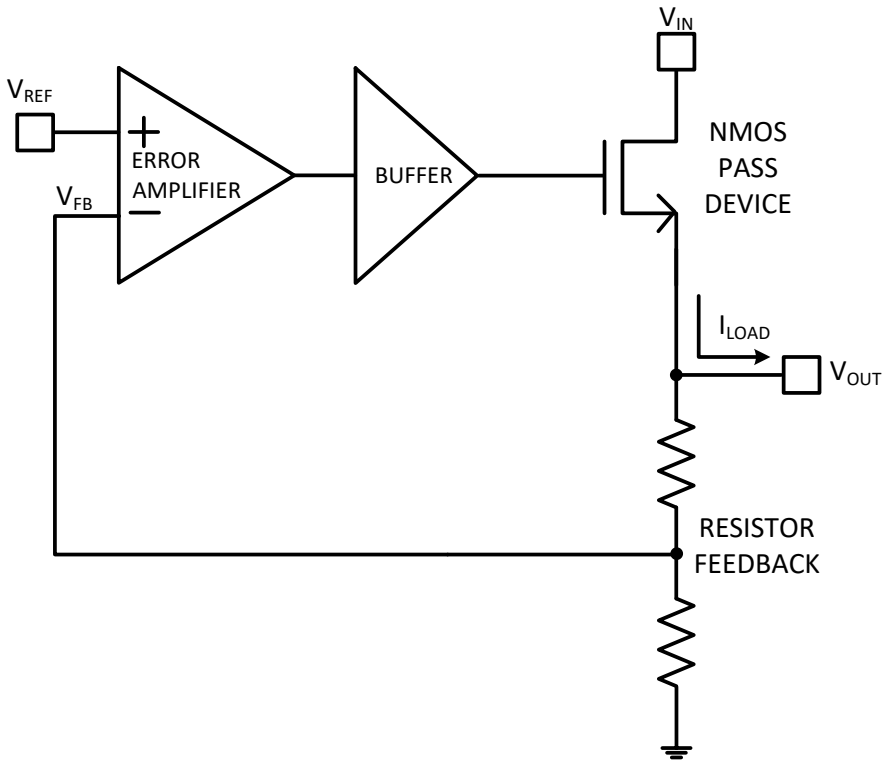


Figure 2.3 Basic Structure of LDO

The basic working of the LDO core loop can be understood by referring to Fig. 2.3. Consider that the output load current (I_{LOAD}) increases; this results in a drop in the output voltage (V_{OUT}). Due to this, the difference between V_{FB} & V_{REF} reduces and the error amplifier's output voltage increases increasing the NMOS pass device's gate voltage.

2.2.2 High Accuracy Current Sensing

The sensed current is a scaled value of the output load current for each LDO. A novel implementation of current sensing based on dynamic element matching (DEM) ensures the high accuracy of the sensed current. DEM is a technique employed in DACs to improve capacitor matching.

Current is sensed using devices added in the pass device (or power/pass FET). These additional devices called as sense devices (or sense FETs) are placed uniformly throughout the pass device to account for its thermal gradient. A sense device is chosen one at a time randomly and this helps in reducing the mismatch.

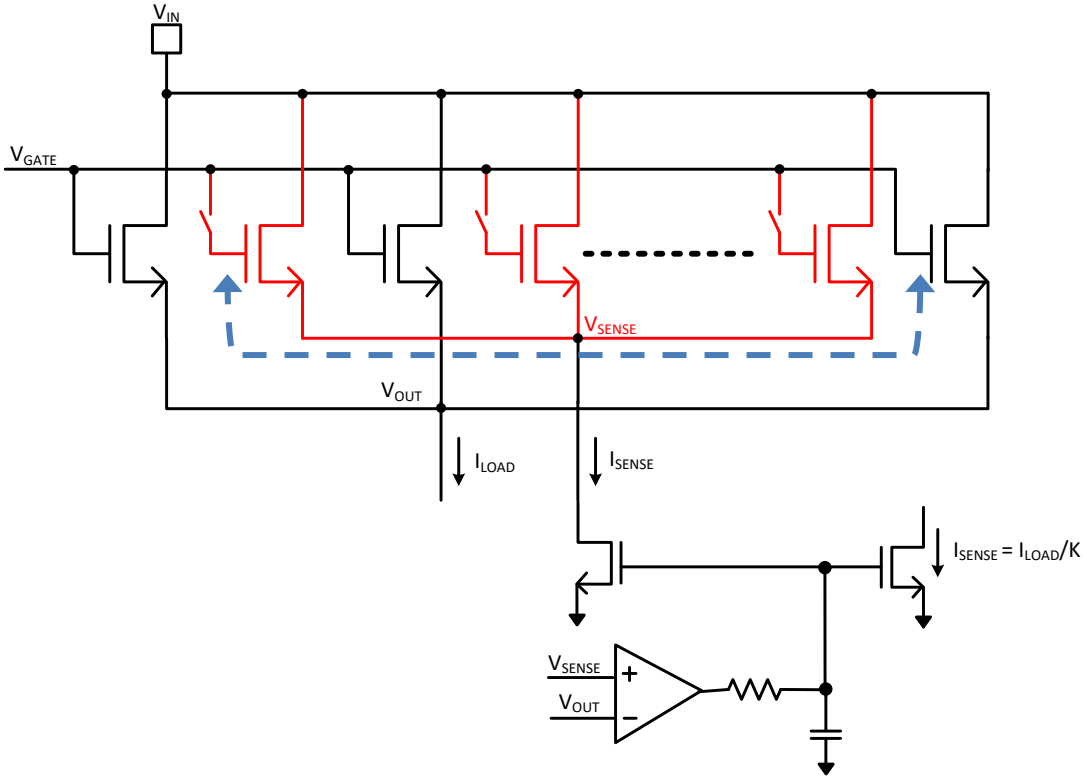


Figure 2.4 Uniform placement of sense devices in pass device and their random cycling for accurate current sensing

2.2.3 Load Sharing Servo Loop

The load balancing technique of a parallel LDO is based on an integrating servo loop. The major components of this loop are a lossless active-RC based servo integrator and a set of current mirrors used to sense & monitor output load currents and an amplifier to maintain the bias voltage of the current mirror system.

The proposed solution to implement the load-sharing logic is to use an integrating servo loop and use its output to modulate the feedback voltage negatively.

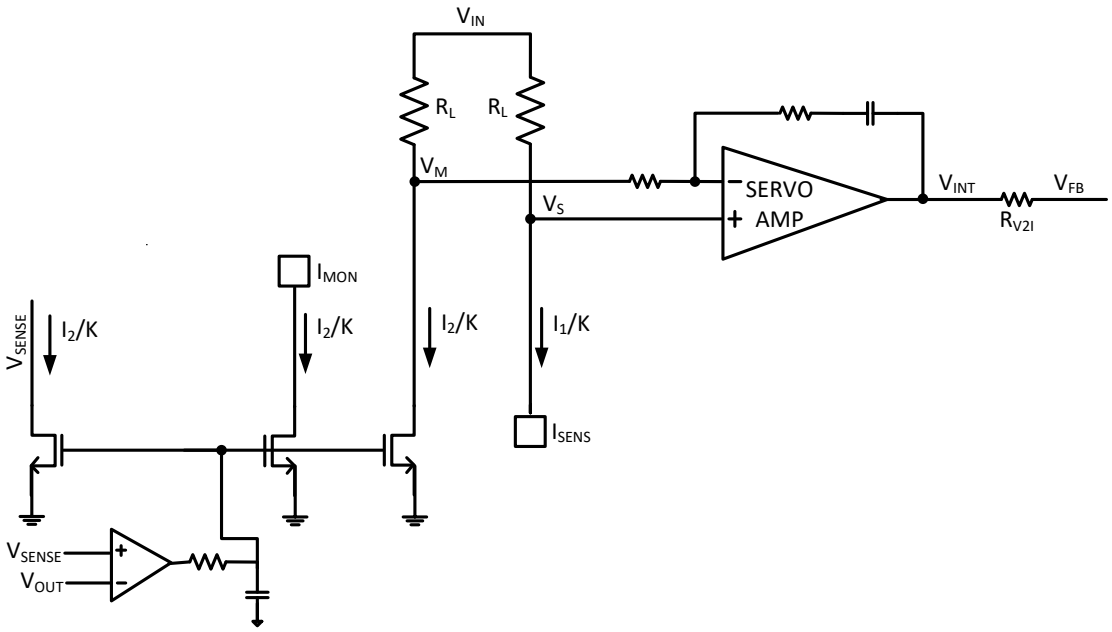


Figure 2.5 Implementation of Servo Loop for LDO-2 from Fig. 2.2

2.3 Operation

Consider the operation of LDO-2 in Fig. 2.1 and Fig. 2.2. The overall LDO implementation for LDO-2 can be shown in Fig. 2.6

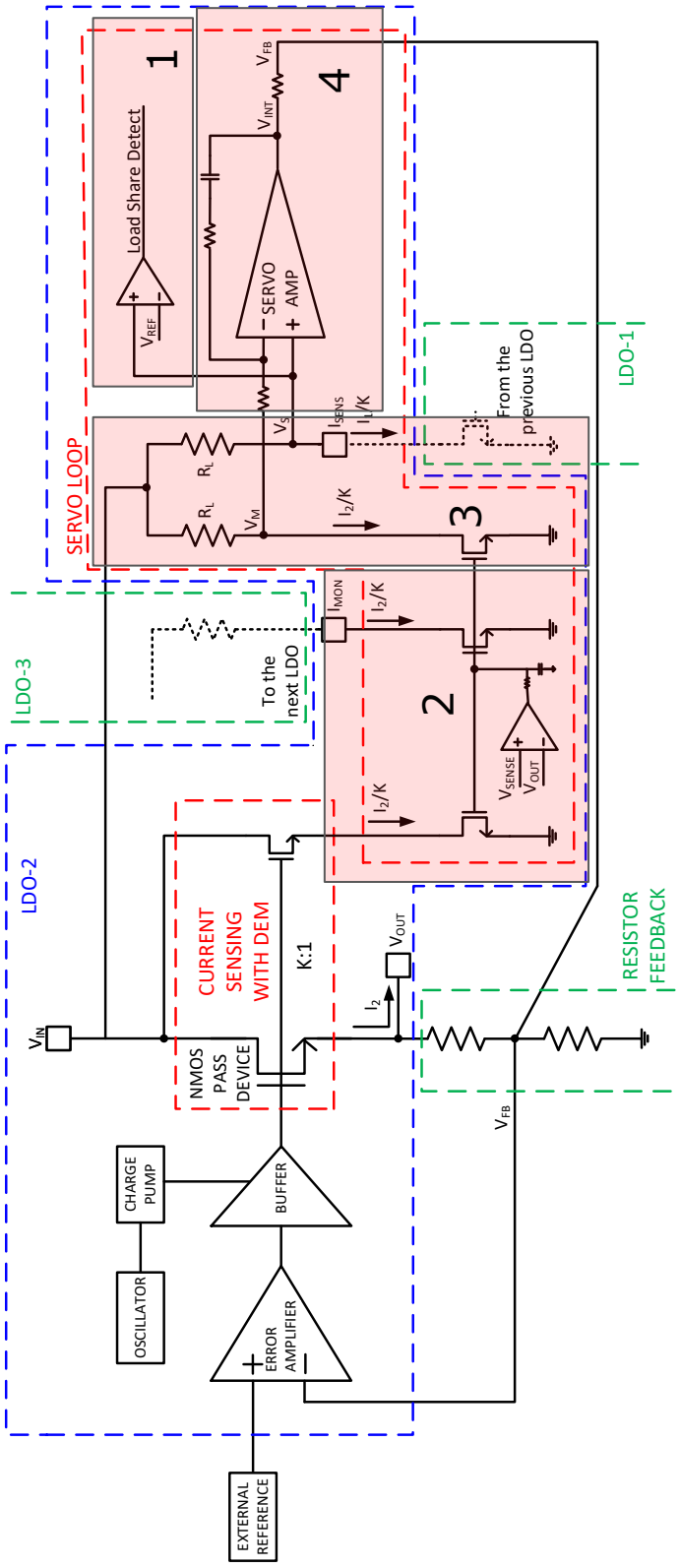


Figure 2.6 Operation of the LDO-2 in a load sharing scenario

The operation of the load sharing loop can be summarized as follows,

1. Determine if LDO is load sharing → Load share detect block and enable the servo loop

2. $I_{MON} = I_2/K$ is sent out from current LDO-2 and is received by I_{SENS} of the next LDO-3

3. $I_{MON} = I_1/K$ sent out from previous LDO-1 is received by I_{SENS} of the current LDO-2

4. Servo loop integrates the error between the sensed current (I_1/K) to the LDO-2's own load scaled current (I_2/K) and gives an error current output to the feedback node

5. Closed loop ensures that $I_1 = I_2 = I_3 = \ldots\ldots\ldots\ldots = I_N = I_{LOAD}/N$

2.4 Sources of Mismatch

Mismatch directly affects the accuracy of load sharing. Hence it is vital to understand the sources of mismatch and target the load sharing accuracy specification.

With the proposed approach, the major sources of mismatch that can be visualized are shown in Fig. 2.7

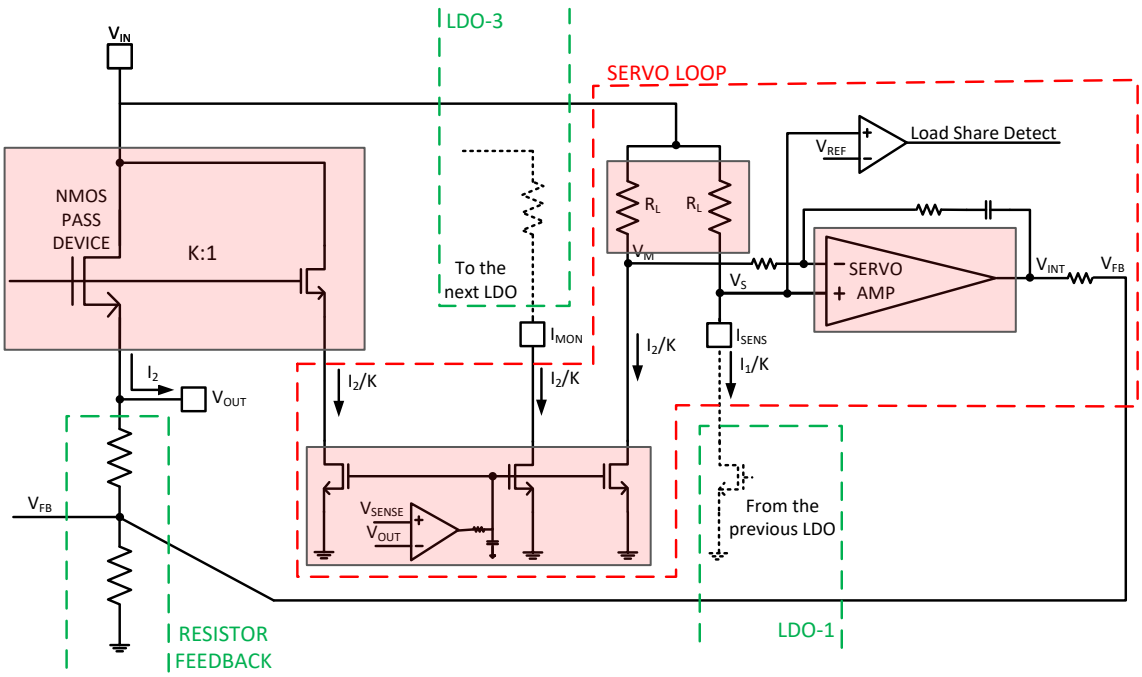
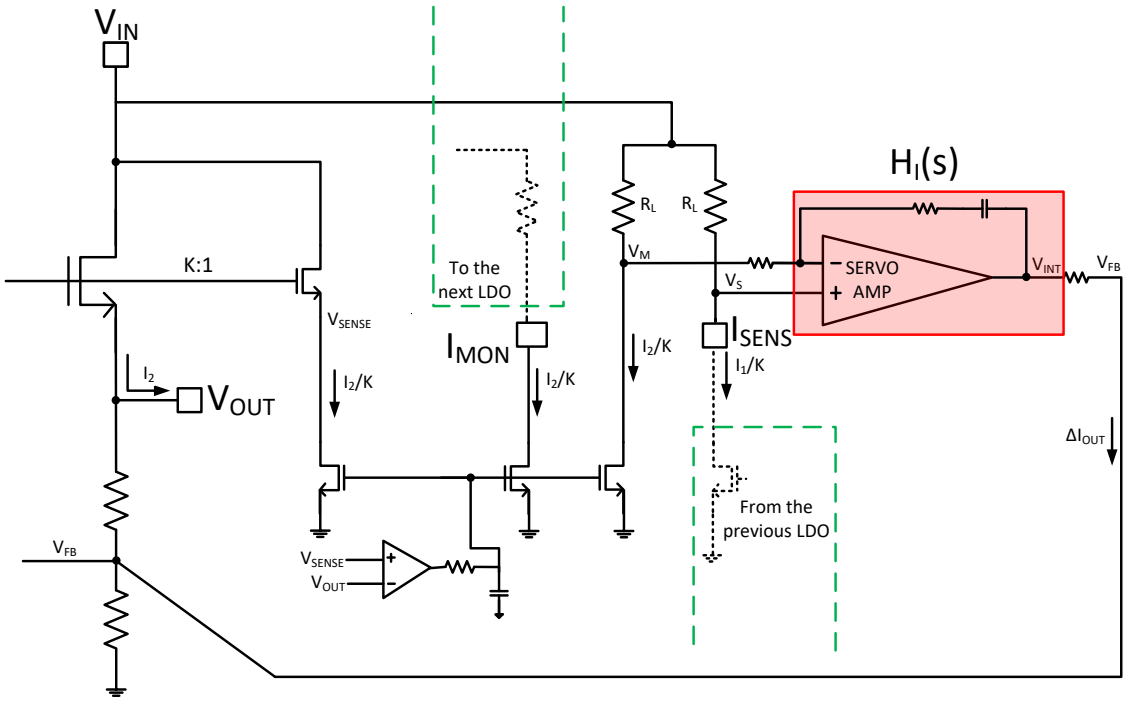


Figure 2.7 Load Sharing Sources of Mismatch

Source	**Mismatch (σ)**
NMOS power FET current sensing (with DEM)	~ 1.3%
Current sensing mirrors	< 0.2%
Load resistors (R_L)	< 0.2%
Servo loop amplifier gain	< 0.5%

Table 2.1 Load Sharing Sources of Mismatch

2.5 Load Sharing Analysis



The overall loop transfer function can be written as,

$$H_{loop} = \frac{I_{MON}}{I_{SENS}}$$

Assuming linear region for pass device,

$$I_{MON} \propto \Delta Vgs\ (\text{pass FET})$$

$$\therefore I_{MON} = H_{LDO} * \Delta V_{err}$$

where, ΔV_{err} is the error signal at the LDO error amplifier input due to error current ΔI_{out} dropping across $(R_1||R_2)$

$$\therefore \Delta V_{err} = \Delta I_{out} * R_1||R_2$$

However, from the servo loop integrator transfer function.

$$\Delta I_{out} = H_I(s)\Delta I_{in}$$

where,

$$\Delta I_{in} = I_{SENS} - I_{MON}$$

$$H_I(s) = G_{amp}\frac{(s + z_1)}{s}$$

Simplifying for I_{MON},

$$I_{MON} = H_{LDO}(s) * H_I(s) * (I_{SENS} - I_{MON})$$

Thus,

$$\therefore H_{loop}(s) = \frac{I_{MON}}{I_{SENS}} = \frac{H_{LDO}(s) * H_I(s) * R_1||R_2}{1 + H_{LDO}(s) * H_I(s) * R_1||R_2}$$

2.6 Target Specifications

Parameter	**Specification**
I_{LOAD} (each LDO)	0 - 2A
Input Voltage	1.5V – 3.3V
Output Voltage	1.0V – 3.0V
Load sharing accuracy	1%
I_Q (each LDO)	~ 300µA
Dropout Voltage	300mV
C_{LOAD}	22µF
C_{IN}	10µF

Table 2.2 Target Specifications

CHAPTER 3

DESIGN METHODOLGY AND IMPLEMENTATION DETAILS

Each individual LDO within the parallel LDO system can be divided into four major components as shown in Fig. 3.1. The implementation of each block within these components is discussed in this chapter.

1. LDO Core Loop
2. LDO Compensation Scheme
3. High Accuracy Current Sensing
4. Load Sharing Servo Loop

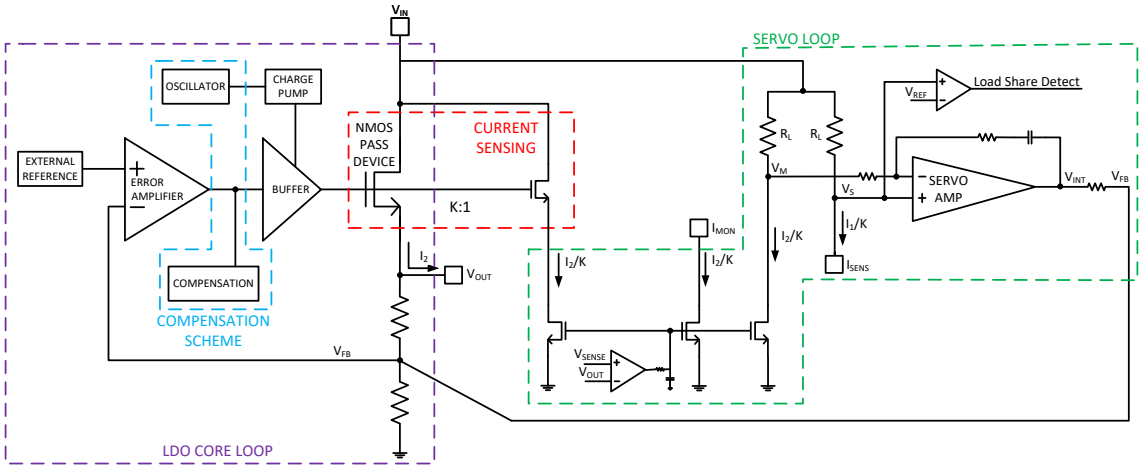


Figure 3.1 Major components of the LDO

3.1 LDO Core Loop

Within the context of an individual LDO, the LDO core loop refers to the feedback loop that ensures output voltage regulation in presence of load and line transients. The major blocks in this loop are the error amplifier, buffer, pass device and feedback resistors.

An external off-chip bandgap reference is chosen as the reference for all the LDOs. The reference voltage is set to 800mV for 1V operation and 1.2V for 3V operation.

3.1.1 Pass Device

The design of any LDO starts with the design of the pass device. The pass device is sized for the specifications of maximum output current and the dropout voltage. The pass device was chosen to be NMOS as they offer significant area advantages over PMOS pass devices. NMOS pass devices however offer no additional loop gain and suffer from body effect if the bulk is not tied to the source.

The NMOS pass device was sized to maintain a dropout voltage of 300mV at 2A of output current typically. The number of

3.1.2 Feedback Resistors

The feedback resistors shown in Fig. 3.2 are designed so as to compare the output voltage ranging from 1V to 3V to be compared with 800mV and 1.2V respectively. Considering a quiescent current of 5µA through the resistors, the resistor values can be calculated.

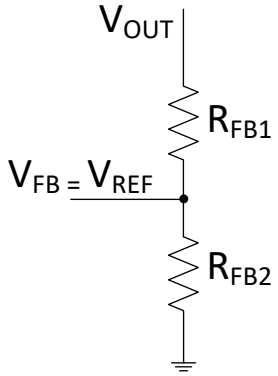


Figure 3.2 Feedback Resistors

$$R_{FB1} = \frac{V_{OUT} - V_{REF}}{I_{FB}}$$

$$R_{FB1} = \frac{V_{REF}}{I_{FB}}$$

V_{IN}	3.3V	1.5V
V_{OUT}	3V	1V
V_{REF}	1.2V	800mV
$V_{DD,INT}$	5V	3V
R_{FB1}	360KΩ	40KΩ
R_{FB2}	240KΩ	160KΩ
I_{FB}	5μA	5μA

Table 3.1 Feedback Resistors Mapping

3.1.3 Error Amplifier

The open loop gain of the LDO core loop can be defined as follows,

$$H_{openloop,LDO}(s) = H_{error\_amplifier}(s) * H_{buffer}(s) * H_{passdevice}(s) * \frac{R_{FB2}}{(R_{FB1} + R_{FB2})}$$

To ensure load regulation across all PVT conditions, the open loop gain of the LDO core loop needs to be high across corners. The buffer being in a source follower configuration gain ($H_{buffer}(s)$) is approximately 1, and owing to the NMOS pass device, the pass device gain ($H_{passdevice}(s)$) is also approximately 1. Thus, the open loop gain of the LDO core loop is provided in entirety by the error amplifier ($H_{error\_amplifier}(s)$).

A folded cascode amplifier topology is chosen for the error amplifier. Folded cascode amplifiers offer the benefit of high AC gain, good output swings for a pretty low current consumption. Considering the range of reference voltage of 800mV to 1.2V, a PMOS input pair is mandated. An AC gain of 60dB across PVT corners is achieved with minimal current consumption. A typical implementation of such an error amplifier is shown in Fig. 3.3.

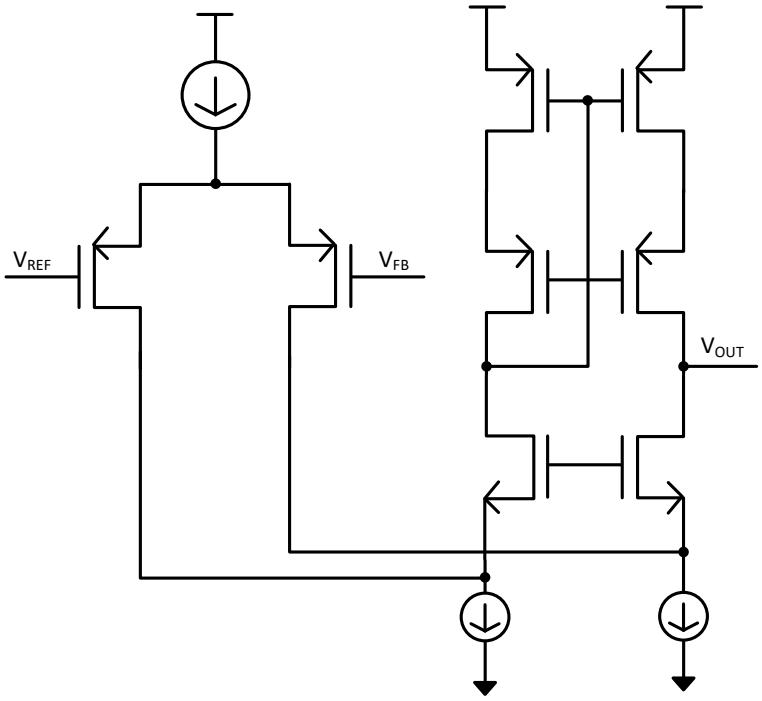


Figure 3.3 Topology of Error Amplifier

$$A_{V,\text{error amplifier}} \approx g_{m,\text{input}} * \frac{(g_{m,\text{pcasbias}} * r_{o,\text{pcasbias}} * r_{o,\text{pbias}})}{2}$$

$$\omega_{\text{dominant, output\_pole}} \approx \frac{1}{(g_{m,\text{pcasbias}} * r_{o,\text{pcasbias}} * r_{o,\text{pbias}}) * C_{\text{in,buffer}}}$$

3.1.4 Buffer

The role of the buffer is to take in the high impedance seen at the output of the error amplifier and present a low impedance output at the gate of the pass device. The low output impedance is necessitated to counteract the large capacitance seen at the gate of the pass device thereby generating a comparatively high frequency output pole [16][17].

A super-source follower topology is employed to realize the buffer. The super source follower presents very low output impedance for reasonable quiescent current consumption. It employs positive feedback loop to lower the output impedance by a factor of the loop's gain. The power supply of the buffer is derived from a charge

pump that generates a pseudo power rail at a maximum voltage of 5V. A conventional implementation of such a buffer is shown in Fig. 3.4.

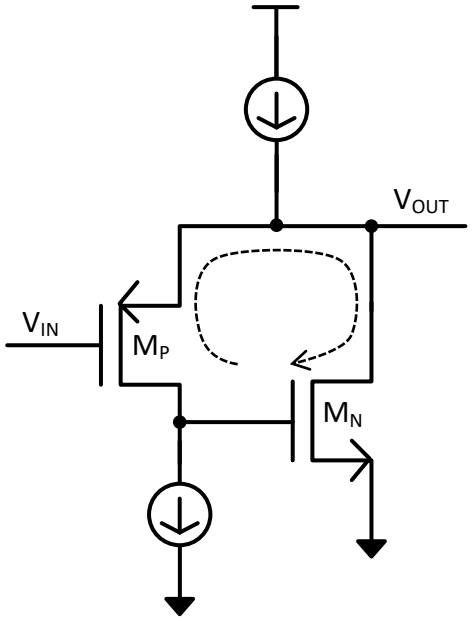


Figure 3.4 Topology of Buffer

$$\omega_{\text{dominant, output\_pole}} \approx \frac{(g_{m,M_P} * r_{o,M_N} * g_{m,M_N})}{C_{\text{gate,passdevice}}}$$

3.1.5 Charge Pump

As the LDO developed has a NMOS pass device, sufficient gate-to-source voltage needs to be maintained at all load currents to ensure output load regulation. This mandates the gate of the pass device or the output of the buffer to be at a voltage higher than the input voltage of the LDO. Thus, a charge pump is required to generate a pseudo VDD rail to power the buffer and error amplifier.

The charge pump designed is based on a single stage of a basic cross-coupled charge pump topology [20]. An on-chip current controlled relaxation oscillator generates a set of non-overlapping clocks that drives this charge pump. The pseudo VDD rail generated by the charge pump is regulated at 2 times V_{IN}. A Clamps are

also added to ensure that the maximum V_{OUT} to 5V. A low-pass RC filter is added to reduce the output ripple.

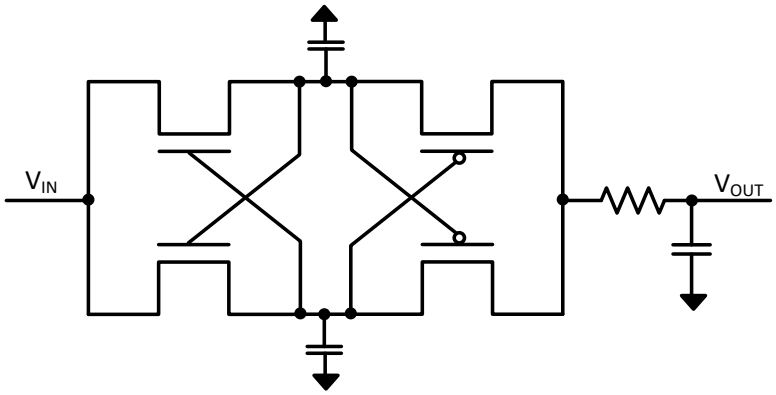


Figure 3.5 Topology of the Charge Pump

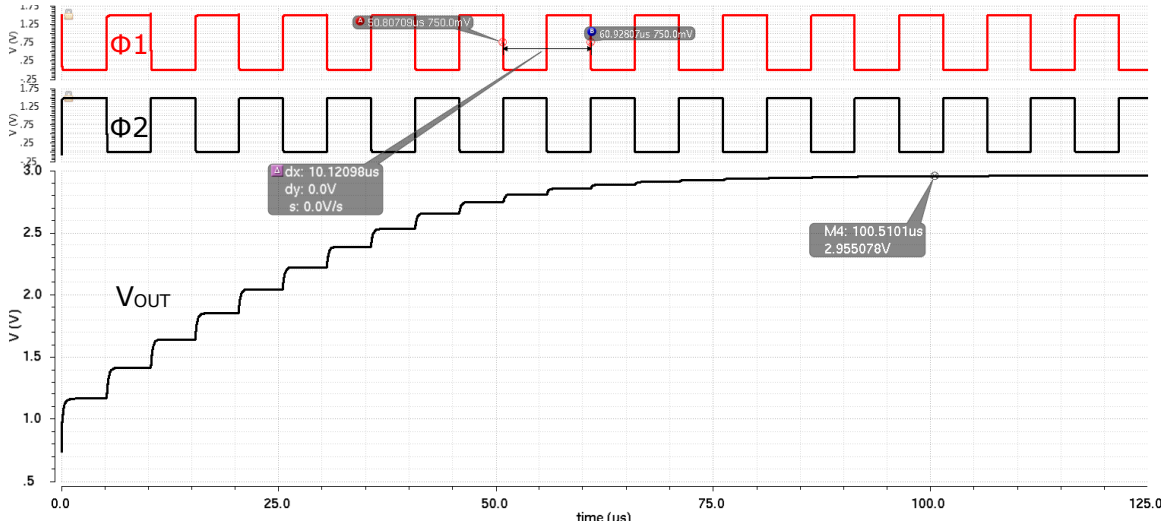


Figure 3.6 Transient response of charge pump for V_{IN} = 1.5V

3.2 LDO Compensation Scheme

The LDO core loop is a negative feedback loop that maintains constant output voltage. As with any feedback loop there is phase shift around the loop and the amount of phase shift determines stability. To have a stable loop the phase shift around the open loop must always be less than 180° at unity gain frequency. A phase margin of 60^0 is targeted for the system across all load conditions.

3.2.1 Pole-Zero Analysis of a Typical LDO

In a typical LDO implementation, 3 poles and 1 zero can be identified [14][19]. The 3 poles are at the output of the error amplifier, output of the buffer and output of the LDO [14][19]. The 1 zero is due to ESR of the ceramic output capacitor. The 3 poles and zero can be shown at the LDO core loop level in Fig. 3.7.

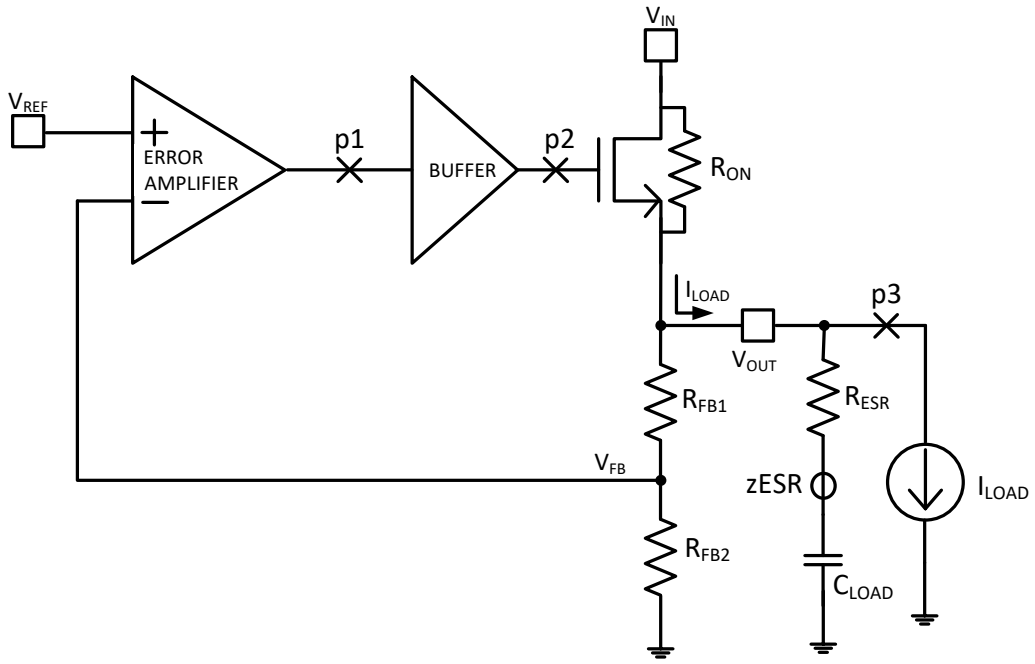


Figure 3.7 Locations of the 3 poles and a zero in a typical LDO [14][19]

The approximate expressions for these poles and zero are as follows,

$$\omega_{p1} \approx \frac{1}{R_{out,error\ amplifier} * C_{in,buffer}}$$

$$\omega_{p2} \approx \frac{1}{R_{out,buffer} * C_{gate,passdevice}}$$

$$\omega_{p3} \approx \frac{1}{R_{ON,passdevice} * C_{LOAD}}$$

$$\omega_{zESR} = \frac{1}{R_{ESR} * C_{LOAD}}$$

3.2.2 Pole Tracking Zero Addition

The typical implementation of the LDO is however unstable as the phase shift around the loop is 180^0 owing to the 2 poles within the open loop UGB. There is thus a need to develop a compensation scheme to ensure stability of the LDO core loop across PVT corners and range of load currents.

The proposed compensation scheme is to introduce an intentional variable zero within the loop UGB at the output of the error amplifier as shown in Fig. 3.8. This is done by adding a fixed large capacitor (C_1) and a variable resistor (R_1) dependent on the load current. The goal of this intentional zero (z1) is to track the output pole (p3) as the load current changes.

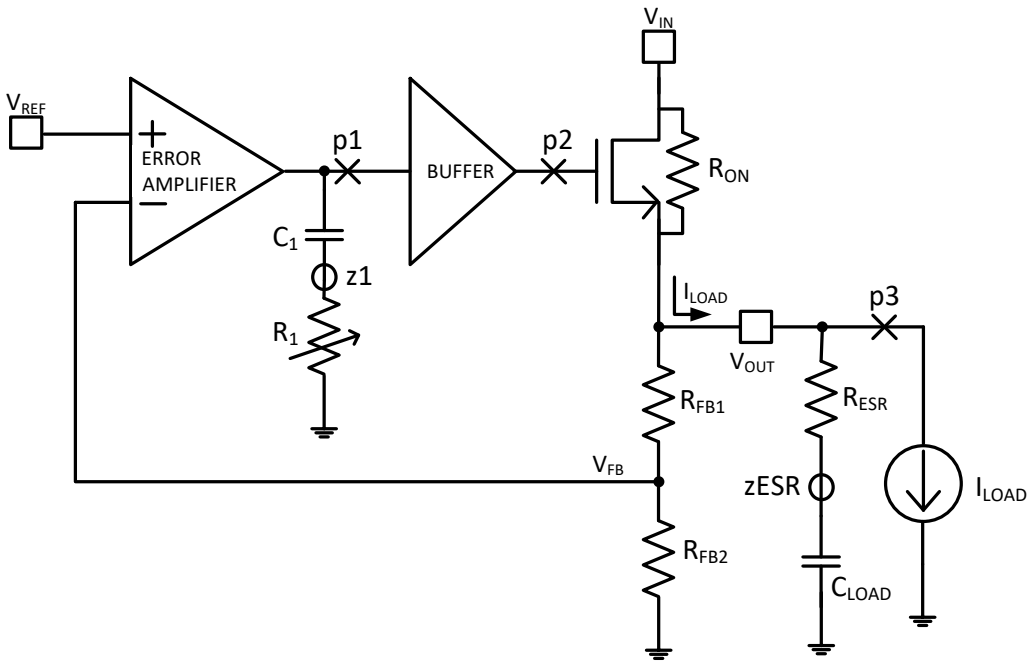


Figure 3.8 Locations of the 3 poles and 2 zeros after addition of pole tracking zero addition

The value of the fixed large capacitor (C_1) is decided to be at least 10x the input capacitance of the buffer ($C_{in,buffer}$). This fixes the value of pole (p1) at the output of the error amplifier irrespective of load current. The expression for the new pole (p1) and variable intentional zero (z1) can be shown to be,

$$\omega_{p1} \approx \frac{1}{R_{out,error\ amplifier} * C_1}$$

$$\omega_{z1} = \frac{1}{R_1 * C_1}$$

We now have a system with 3 poles and 2 zeros in the open loop gain expression of the LDO. p2 and zESR are ensured to be outside the open loop UGB. p1 and p3 and z1 are ensured to be inside the open loop UGB at all loads thereby realizing a stable system.

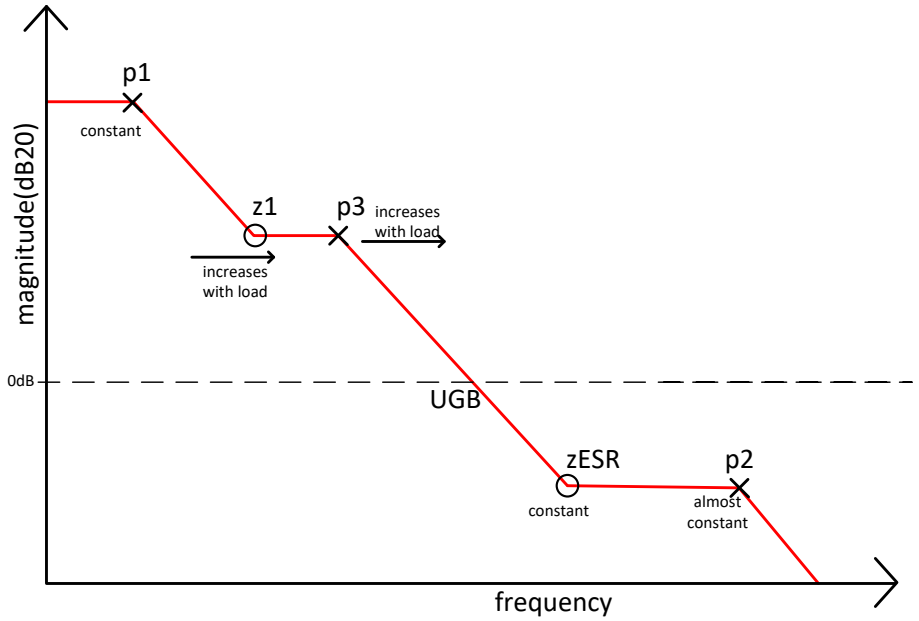


Figure 3.9 8 Pole and zero locations on the frequency scale

The output pole (p3) and variable zero (z1) varies as per the load current.

$$\omega_{p3} \approx \frac{1}{R_{ON,passdevice} * C_{LOAD}} = \frac{\lambda . I_{LOAD}}{C_{LOAD}}$$

$$\therefore \omega_{z1} = \frac{1}{R_1 * C_1} \propto I_{LOAD}$$

$$\therefore R_1 \propto \frac{1}{I_{LOAD}}$$

As output load current increases, p3 shifts to a higher frequency. As z1 is to track p3, z1 needs to shift to a higher frequency. z1 can be shifted to higher frequency by reducing the value of R_1.

Thus, R_1 needs to be varied inversely with respect to load current to ensure stable operation of the LDO core loop.

3.2.3 Variable Resistor Implementation

In the last section, we concluded that the variable resistor R_1 needs to be placed at the output of the error amplifier to ensure stability of the LDO core loop. The variable resistor is realized as a switched capacitor resistor with variable clock frequency. The variable clock frequency is generated by a current controlled relaxation oscillator described in section 3.2.4.

A switched capacitor resistor is the realization of resistor operation by switching the charge across a capacitor. Implementations of a switched capacitor based resistor independent of device & routing parasitics are shown in Fig. 3.10. A positive or negative resistor implementation can be realized based on the position of the clocking signals [12][15].

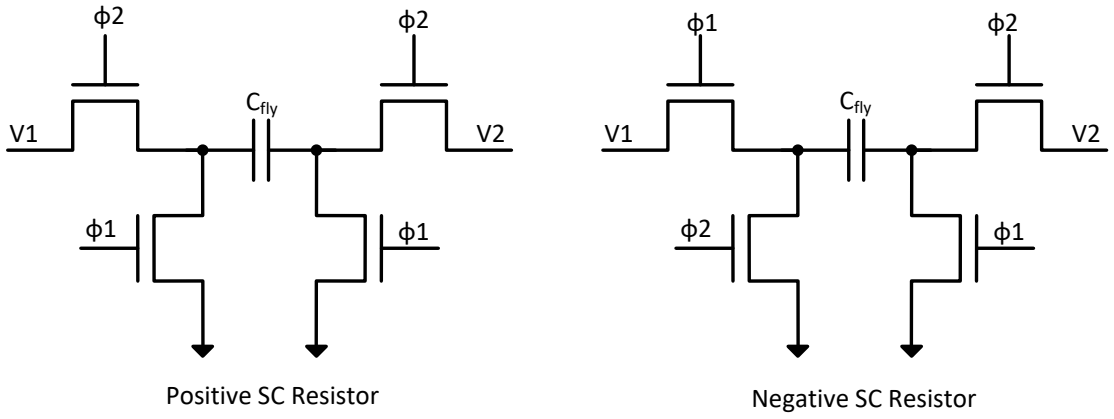


Figure 3.10 Parasitic independent switched capacitor resistor implementation [12][15]

The clocks (φ1, φ2) utilized to generate this need to be non-overlapping in nature, to allow for charge transfer. It can be shown that the equivalent resistance,

$$R_{eq} = \frac{V1 - V2}{I_{avg}} = \frac{T_{clk}}{C_{fly}} = \frac{1}{f_{clk} C_{fly}}$$

The switched capacitor based variable resistor R_1 is implemented by varying switching clock frequency. From the above expression, it can be clearly seen that the clock frequency (f_{clk}) is inversely proportional to the realized resistor value (R_1). As concluded in the previous section, R_1 needs to be inversely varied with the load current. Thus, the clock frequency (f_{clk}) needs to be directly proportional to the load current to realize the requisite R_1.

$$\therefore R_1 = \frac{1}{f_{clk} C_{fly}} \propto \frac{1}{I_{LOAD}}$$

$$\therefore f_{clk} \propto I_{LOAD}$$

3.2.4 Current Controlled Relaxation Oscillator

The input current of this oscillator needs to be directly proportional to the load current. The highly accurate sense current derived from the load current is employed as an input to this oscillator. The relaxation oscillator is based on a Schmitt trigger. A cross-coupled inverter chain and a non-overlapping clock generator circuit are also added. An implementation of the same is shown in Fig. 3.11.

Consider VIN to be at VDD initially with a zero input current (I_{SENSE}). Thus, CLK_INT is at 0 due to the inverting nature of the Schmitt trigger. This ensures that the gate of the holding PMOS is at VDD thus turning it OFF. Thus, VIN is held at VDD.

Now, a non-zero input current (I_{SENSE}) for a given I_{LOAD} and K is applied. This causes the capacitor to discharge and VIN drops linearly. Once VIN reaches the lower trip point of the Schmitt trigger, CLK_INT rises to VDD. This causes the PMOS to turn ON, VIN is again pulled to VDD and CLK_INT falls back to 0.

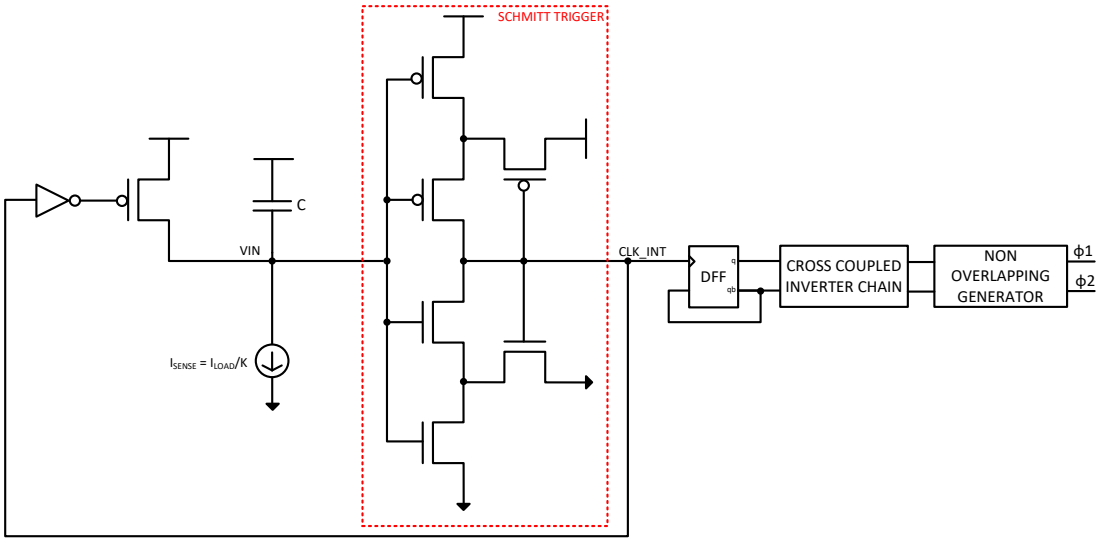


Figure 3.11 Current Controlled Relaxation Oscillator

This short pulse on CLK_INT can be processed through a D flip-flop and a clock with approximately 50% duty cycle can be obtained. This is then passed on through the cross coupled inverter chain to better the duty cycle and a non-overlapping clock generator generates φ1 and φ2.

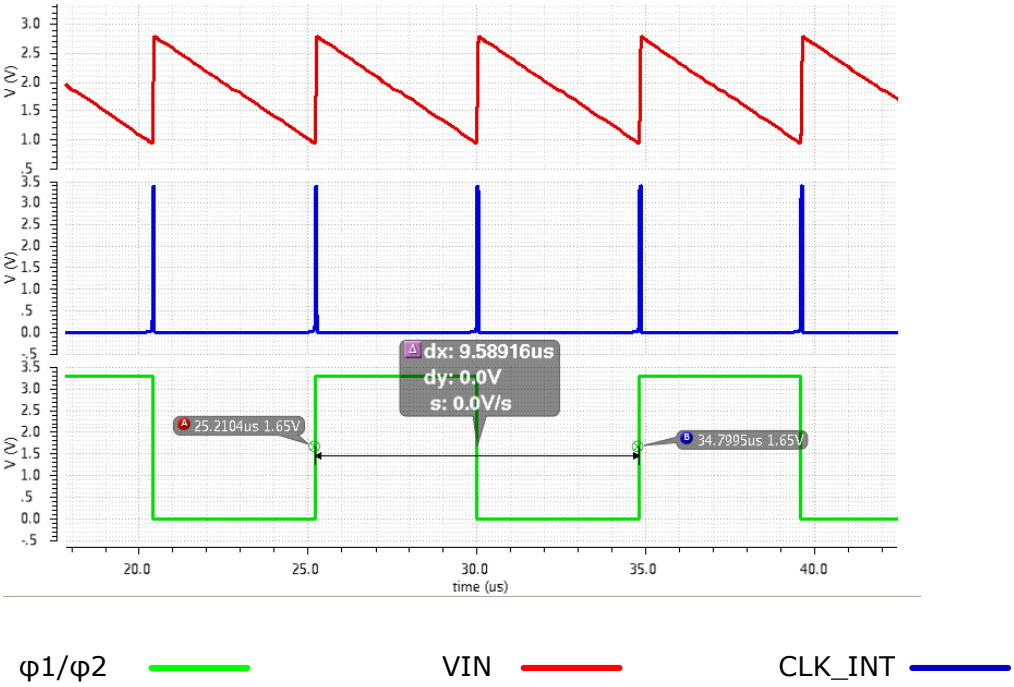


Figure 3.12 Current controlled relaxation oscillator waveforms

3.2.5 Quantitative Analysis

Based on all the qualitative analysis shown above and the given set of specifications, a mapping table can be devised to correlate the variable clock frequency and load current. The dependence equation for the switched capacitor resistor based implementation is,

$$f_{clk} \propto I_{SENSE} \propto I_{LOAD}$$

The value of added C1 is 30pF. This is added to ensure that p1 is always inside loop UGB at all load currents. The calculated approximate values of the poles and zeros are thus,

$C_1 = 30\text{pF}, R_{\text{out,error amplifier}} \approx 15\text{M}\Omega$ ➔ $f_{p1} \approx 77\text{Hz}$ ➔ constant

$f_{p2} \approx 903\text{KHz}$ to 978KHz ➔ almost constant across load

$C_{LOAD} = 22\mu\text{F}, R_{ESR} = 25\text{m}\Omega$ ➔ $f_{zESR} = 288\text{KHz}$ ➔ constant

$f_{p3} \approx 121\text{mHz}$ (no load)to 48.27KHz (full load $= 2\text{A}$) ➔ varies across load

f_{z1} ➔ needs to be varied across load

z1 is thus placed at exactly at p1 at no load output current and increases accordingly as load current increases. Also, from the dependence equation,

$$R_1 \propto \frac{1}{I_{LOAD}} \quad \therefore R_1 * I_{LOAD} = \text{constant} = \text{chosen to be } 20\text{K}\,\Omega\text{A}$$

This constant value ensures that the system is stable across loads. A linearized model of this switched capacitor resistor can thus be implemented by using an analogLib resistor whose value is set to ($20\text{K}/I_{LOAD}$) Ω.

$$\because R_1 = \frac{20000}{I_{LOAD}} = \frac{1}{f_{clk} * C_{fly}}$$

Considering a ratio of 'K' for the scaled sense current,

$$\therefore f_{clk} = \frac{I_{LOAD}}{C_{fly} * 20000} = \frac{K * I_{SENSE}}{C_{fly} * 20000}$$

A mapping table can thus be formed for the expected value of R_1 and f_{clk}. The value of C_{fly} used is 5pF. The scaling ratio of the sensed current is 20000. I_{SENSE} is important as it is used as an input to the current controlled oscillator.

$I_{LOAD}*R_1$	I_{LOAD}	R_1	I_{SENSE} (=$I_{OSCILLATOR}$)	f_{clk}
20K A-Ω	2A	10KΩ	100µA	20MHz
20K A-Ω	1A	20KΩ	50µA	10MHz
20K A-Ω	100mA	200KΩ	5µA	1MHz
20K A-Ω	10mA	2MΩ	500nA	100KHz
20K A-Ω	2mA	10MΩ	100nA	20KHz
20K A-Ω	1mA	10MΩ (fixed)	100nA (fixed)	20KHz (fixed)
20K A-Ω	0A	10MΩ (fixed)	100nA (fixed)	20KHz (fixed)

Table 3.2 Mapping f_{clk} to R_1 and $I_{OSCILLATOR}$

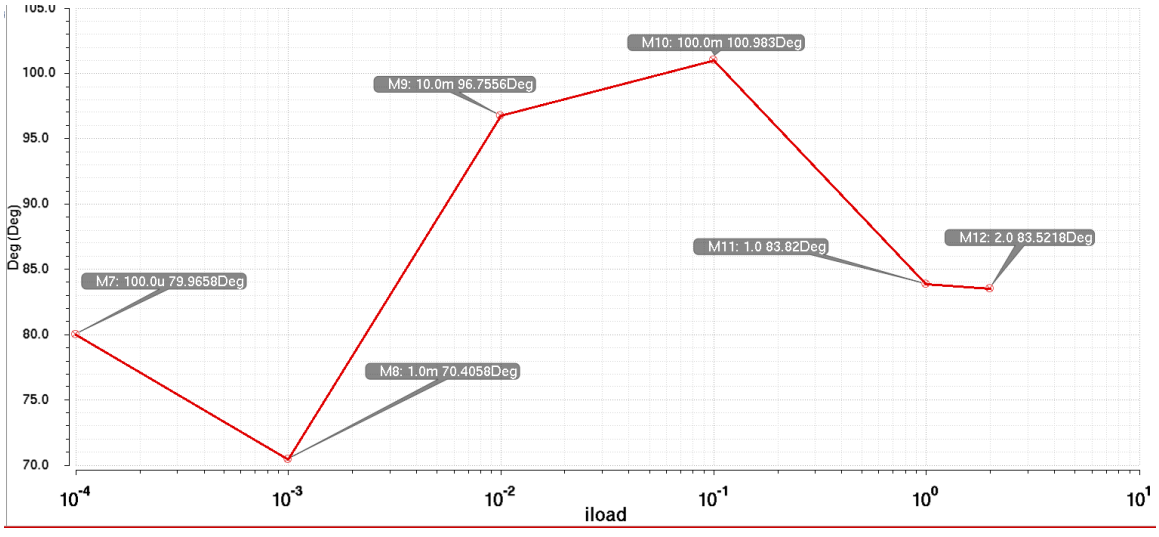


Figure 3.13 Phase Margin vs I_{LOAD}

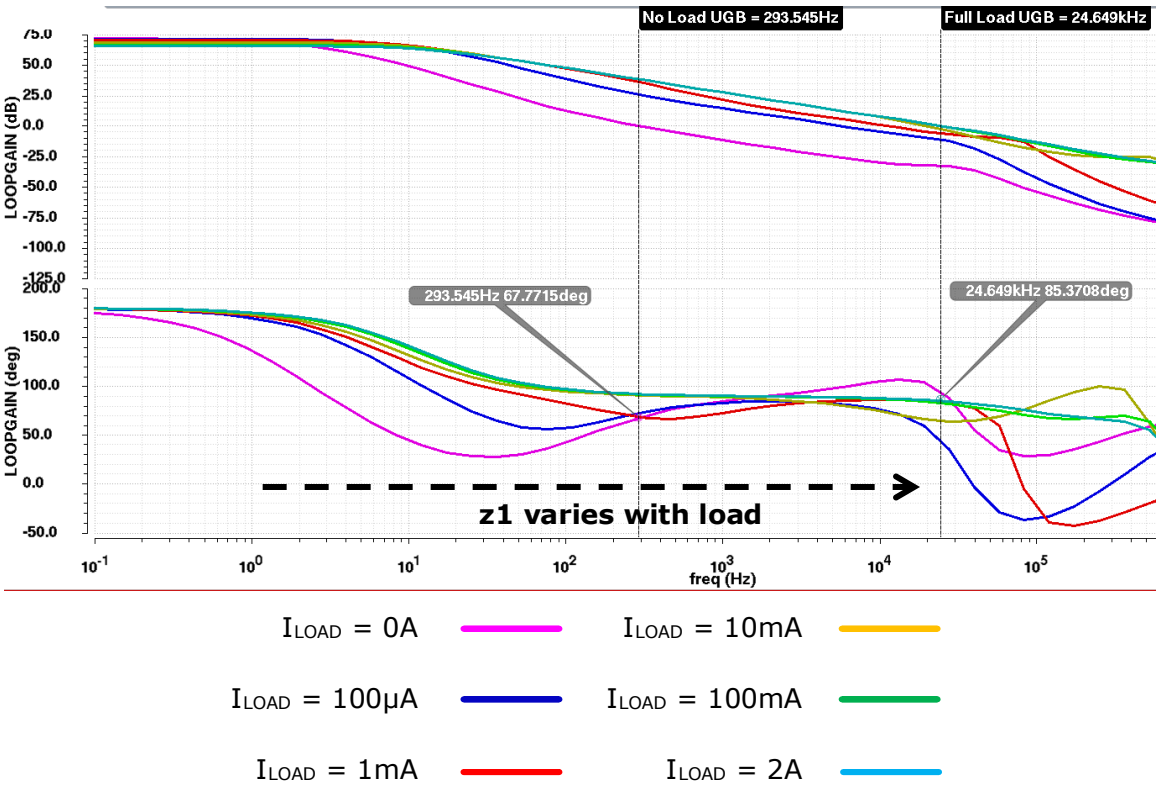


Figure 3.14 Open loop bode plot response of the LDO and variation of zero with load current

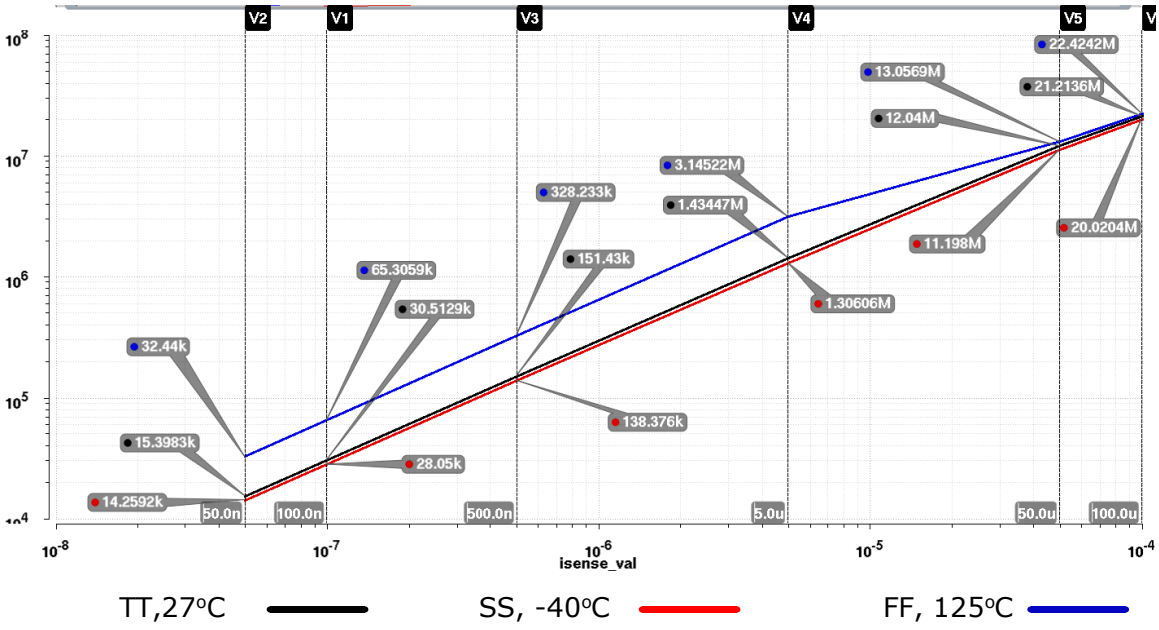


Figure 3.15 Oscillator frequency (f_{clk}) vs sense current (I_{SENSE})

3.3 High Accuracy Integrated Current Sensing

Conventional current sensing techniques involve the usage of a small value sense resistor in series with the load [8]. The accuracy of such a conventional approach is directly proportional to the variation of the sense resistance which can be integrated on the chip or placed off-chip.

Matched PCB traces may also be used instead of external sense resistors for sensing output current. This reduces the system cost however mismatch between PCB traces directly affects the current sensing accuracy.

3.3.1 Dynamic Element Matching

Dynamic Element Matching (DEM), a concept widely used in data converters is employed to achieve the intended high accuracy. DEM refers to a technique where a number of unit elements exhibiting a certain degree of mismatch in their absolute values are to be matched to a certain resolution finer than the mismatch tolerance [9][10][24]. It is commonly used in DAC architectures for capacitor ladder matching.

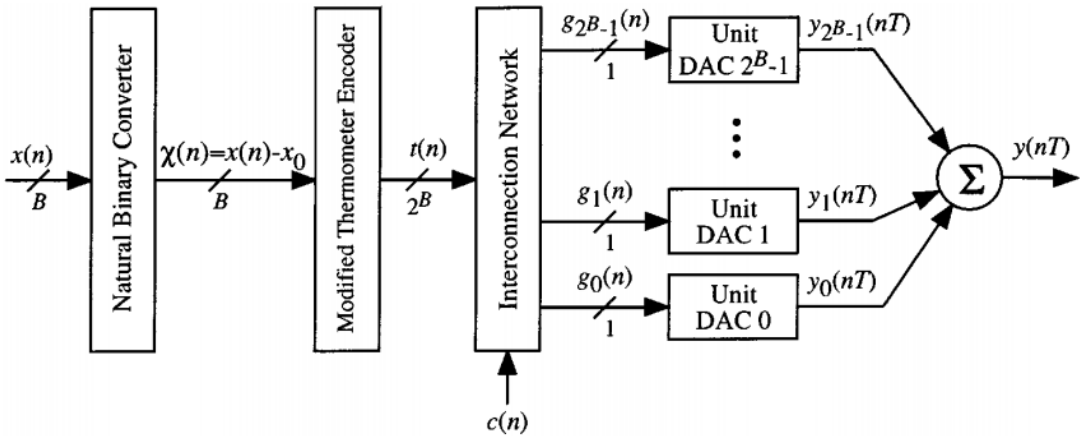


Figure 3.16 A block diagram of a B–bit dynamic element matching flash DAC [9]

3.3.2 Usage of DEM in LDO Current Sensing

In a typical LDO, the current is sensed using a single sense device (or sense FET) with the current scaling ratio of 'K'. To employ DEM in current sensing however, multiple sense devices (or sense FETs) each with the same current scaling ratio of 'K' are required. Each sense device is selected one at a time to ensure the sensed current is scaled down exactly 'K' times in both the approaches.

The DEM approach works best when this selection is random in nature. Various algorithms such as barrel shifting, data-weighted averaging, butterfly-shuffler, full randomization DEM, partial randomization DEM have been developed to implement DEM [22][23][24]. These techniques are quite complex, and are specifically targeted for use in DACs in delta-sigma (Δ-Σ) data converters.

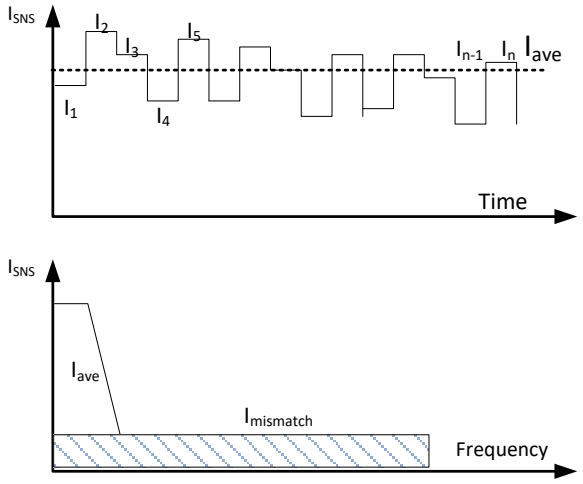


Figure 3.17 I_{SENSE} vs Time and Frequency

Within the framework of current sensing in LDOs and to keep the hardware complexity low, a simple pseudo-random binary sequence (PRBS) generator can also be used to generate the selection sequence of the sense devices. A PRBS although generated from a deterministic algorithm is difficult to predict.

The most generic implementation of a PRBS generator is based on linear-feedback shift register (LFSR). The PRBS sequence obtained is binary coded. A binary to thermometer decoder is used to obtain the thermometric code to be employed to select each sense device.

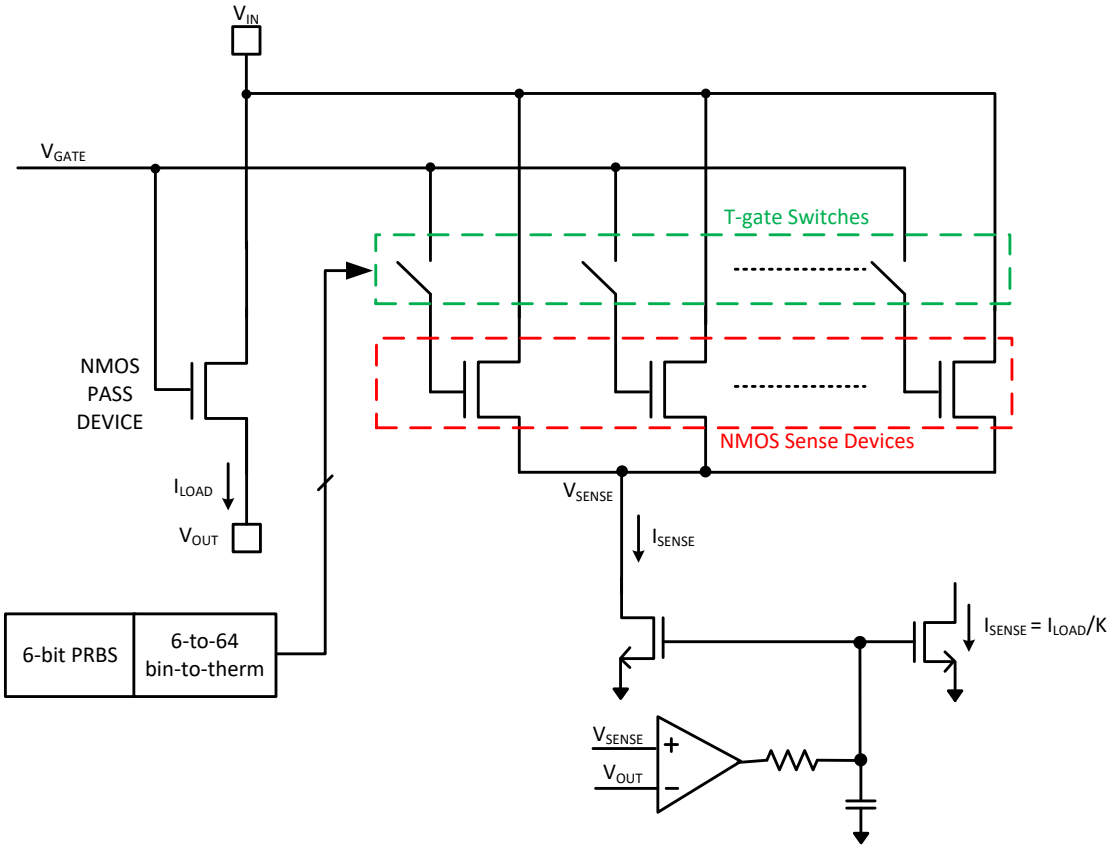


Figure 3.18 DEM based Current Sensing Scheme

3.3.3 Implementation of DEM in LDO Current Sensing

Consider a 3-bit LFSR to generate a 3-bit PRBS. This LFSR coupled with a 3-to-8 binary to thermometer decoder will give us 8 distinct outputs. These 8 distinct outputs can then be used to select 8 sense devices. With the designed pass device, appropriate scaling ratio and 8 sense devices, the accuracy of the sensed current is measured using Monte Carlo analysis for 300 runs.

The statistical variable used to quantify this accuracy is the mismatch between the simulated value and expected value of the sense current.

$$i_{mismatch} = i_{simulated} - i_{expected}$$

The scaling ratio employed is 20,000 and for a load current of 1A, the sense current should be exactly 50µA. The standard deviation of $i_{mismatch}$ divided by the expected value of sense current is used to calculate the accuracy.

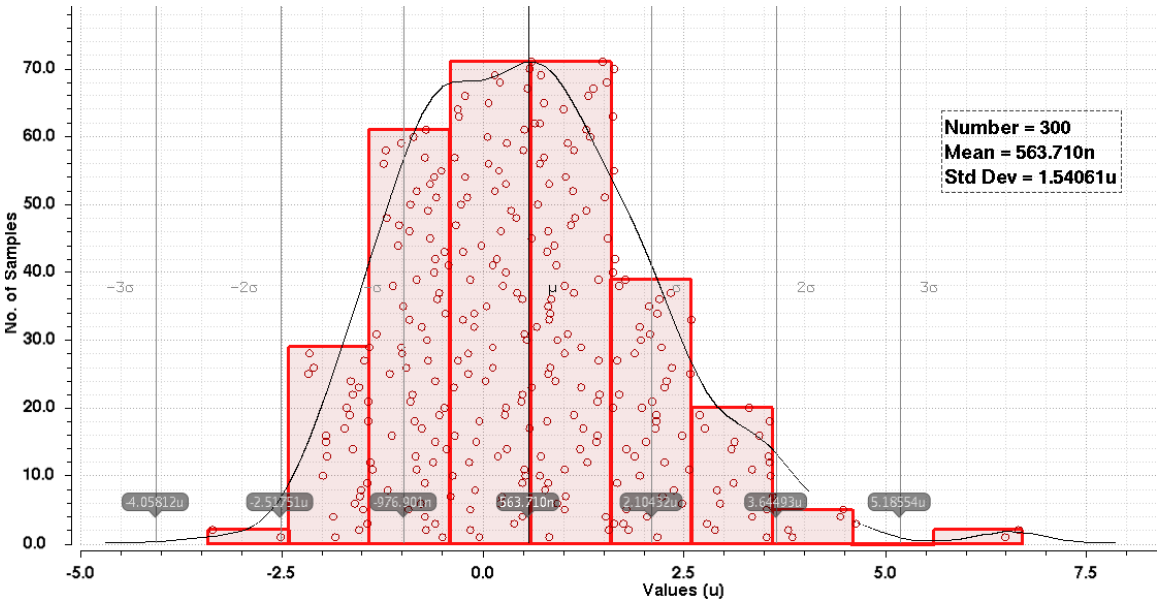


Figure 3.19 Current Sensing Mismatch for 8 sense devices

$$\therefore \sigma_I \text{ (8 sense devices)} = \frac{1.54061\mu A}{50\mu A} \sim 3\%$$

It is found that 8 sense devices are not sufficient to target the required accuracy of less than 1%. As shown in [9], the effective mismatch seen by the system is inversely dependent to the square root of the number of elements to be matched.

$$\sigma_{eff} = \frac{\sigma_{orig}}{\sqrt{N_{elements}}}$$

Hence to better the accuracy, the number of sense devices are increased from 8 to 64. The PRBS generation is now based on 6 bit LFSR and a 6-to-64 binary to thermometer decoder is also used to decode the binary code.

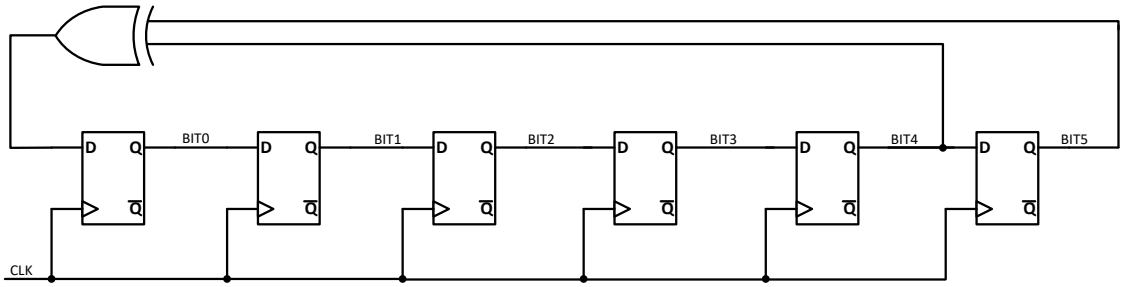


Figure 3.20 6-bit LFSR to generate PRBS

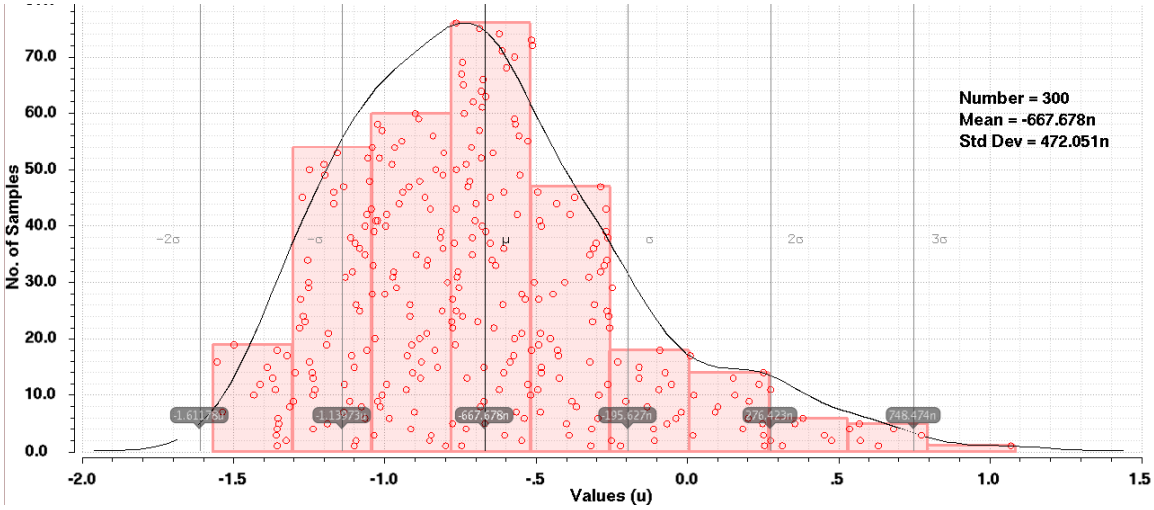


Figure 3.21 Current Sensing Mismatch for 64 sense devices

$$\therefore \sigma_I\ (64\ \text{sense devices}) = \frac{472.051\text{nA}}{50\mu\text{A}} \sim 1\%$$

The placement of the sense devices is also key to increasing the current sensing accuracy. Sections of the LDO pass FET with higher junction temperatures will tend to sense more current than sections with lower junction temperatures.

Uniformly placing the sense devices across the pass device as in Fig. 3.22 helps to sense the load current better. This will thus also account for the uneven thermal map of the pass FET.

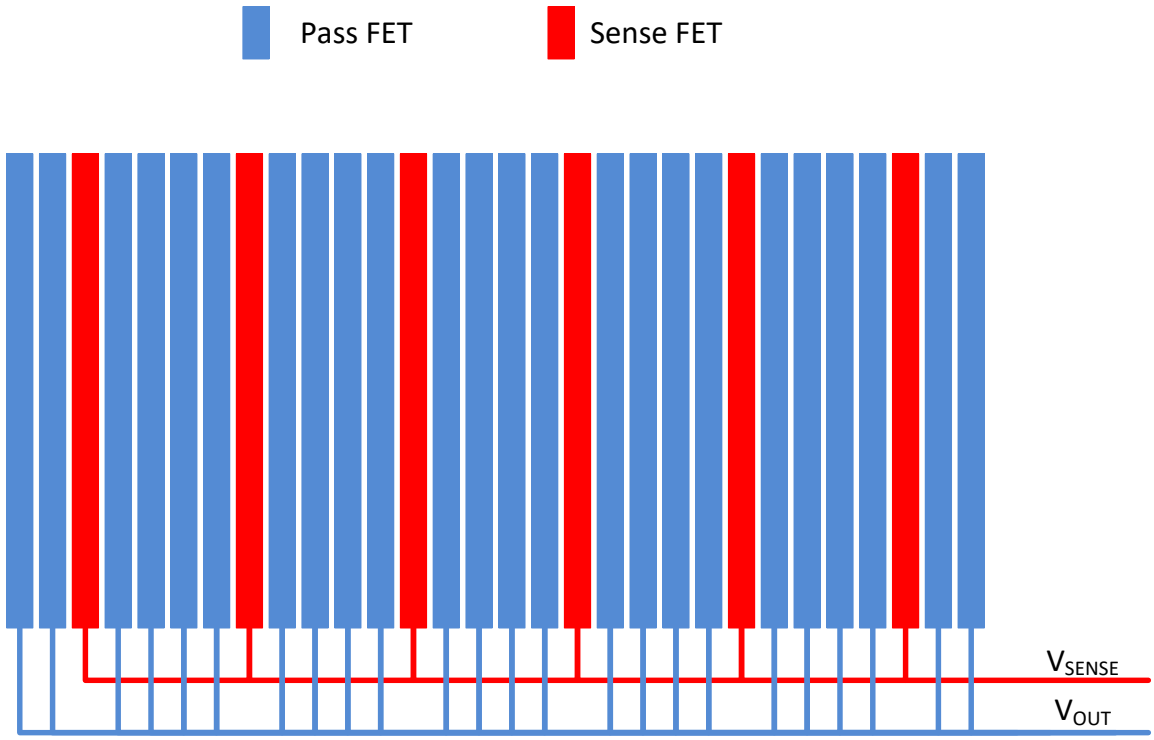


Figure 3.22 Placement of Sense FET across Pass FET

3.4 Load Sharing Servo Loop

The servo loop is an additional auxiliary loop present in every LDO that ensures load balancing between the parallel LDOs. This loop consists of the high precision current mirrors, the servo loop integrator and the load share detect block.

3.4.1 Operation

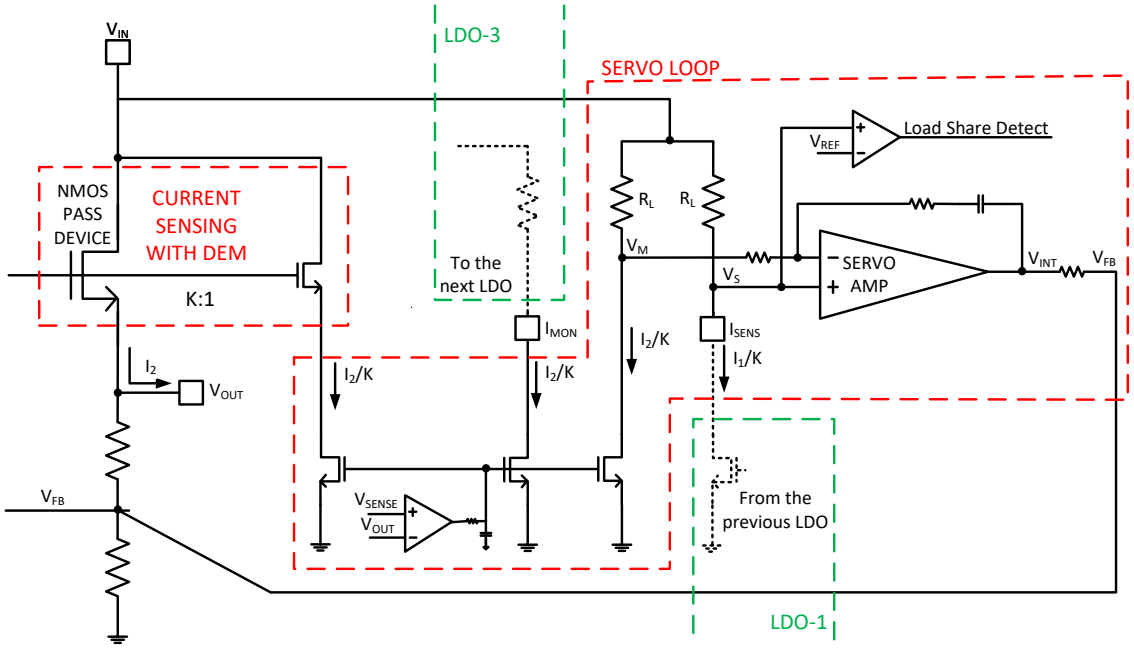


Figure 3.23 Servo Loop in LDO-2

Each servo loop within the LDO interacts with the adjacent LDO's servo loop in the daisy chain through the pins ISENS and IMON to achieve this current balance.

Consider the operation of the integrating servo loop in LDO-2 as in Fig 3.23. The sensed current of LDO-1 (I_1/K) is compared to the sensed current of LDO-2 (I2/K). This error is then integrated (V_{INT}) and converted to an error current. The error current modulates the current in the feedback resistors and thereby modulates V_{FB}. The modulation on V_{FB} cycles through the LDO core loop to adjust the output current of the LDO. The error current in steady state is 0.

3.4.2 Design Considerations and Analysis

From the load sharing analysis of section 2.5,

$$H_{loop}(s) = \frac{I_{MON}}{I_{SENS}} = \frac{H_{LDO}(s) * H_I(s) * R_1||R_2}{1 + H_{LDO}(s) * H_I(s) * R_1||R_2}$$

$|H_{LOOP}(s)|$ needs to be 1 to ensure current balance. If the value of $H_{LDO}(s)*H_I(s)*R_1||R_2$ is high, then $|H_{LOOP}(s)|$ is almost equal to 1. Thus, the servo loop integrator ($H_I(s)$) needs to have high gain.

To ensure load balance without disturbing load regulation, the servo loop needs to be slower than the LDO core loop. Thus, the servo loop integrator ($H_I(s)$) needs to have low bandwidth.

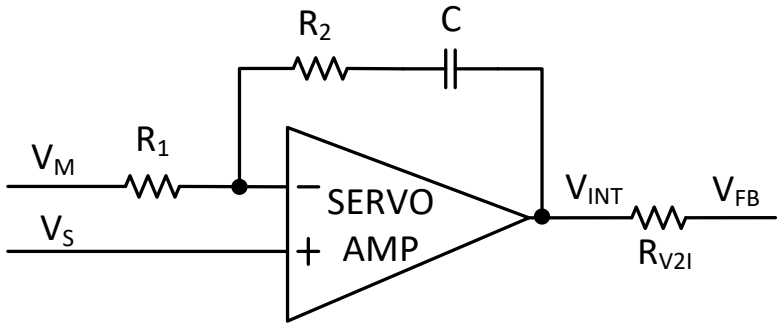


Fig 3.24 Servo Loop Integrator

The active-RC integrator in the servo loop integrates the differential input voltage generated due to the sense currents. The integrator transfer function and it's parameters are as follows,

$$\frac{V_{INT}}{V_M} = -\frac{R_2}{R_1}\left(\frac{s + \frac{1}{R_2 C}}{s}\right)$$

$$\omega_P = 0 \text{ Hz},\ \omega_z = \frac{1}{R_2 C}$$

$$\omega_{UGB} = \frac{1}{C\sqrt{(R_1^2 - R_2^2)}}$$

Considering the integrator UGB of 4KHz and C = 50pF, the values of R_1 = 800KΩ and R_2 = 200KΩ are calculated. The values of R1 and R2 are in hundreds of KΩs to safeguard the operation of the amplifier.

The amplifier's UGB is set to around 1MHz to ensure it provides flat constant gain without any poles at zeros at the lower operational frequency of the integrator. Considering the amplifier has to drive a large capacitance at the output, the amplifier topology employed is a folded cascode followed by a source follower. The amplifier input referred offset directly impacts the load sharing accuracy.

The load resistors R_L define the differential input and common mode voltage input to the integrator. Based on the sense currents of 100s of nAs to a few µAs, the values of these resistors can be limited to somewhere in the intermediate range of a few KΩs to tens of KΩs. Thermal noise being proportional to the resistance value is also of concern for high value resistors. Ensuring that these resistors are as matched as possible to reduce mismatch in the system.

3.4.3 Competing Loops – Servo Loop vs Core Loop

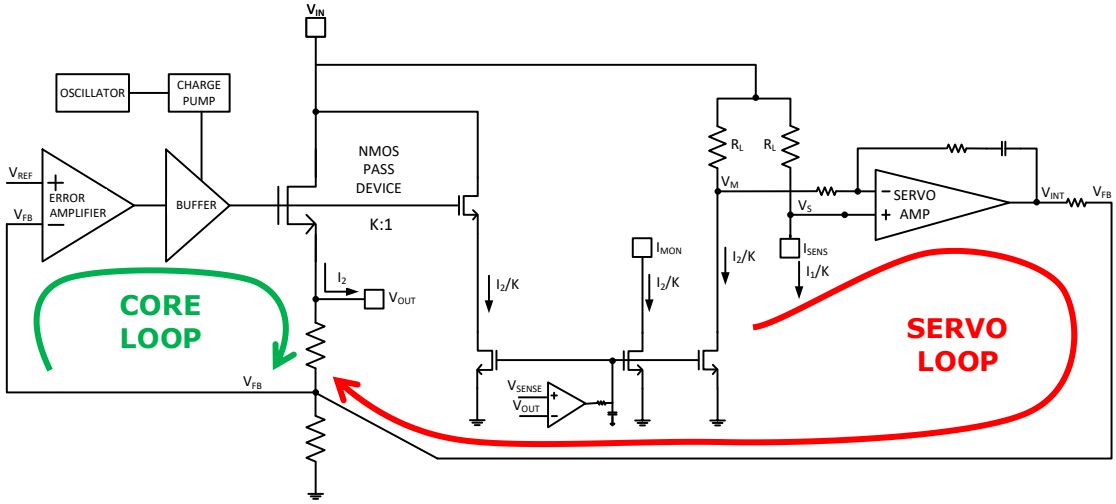


Figure 3.25 Competing loops in the proposed LDO

As both the servo loop and the core loop feed their error at the same point V_{FB}, it is crucial to understand the behavior of these loops working together. To ensure load regulation, the core loop needs to be dominant than the servo loop both in terms of gain and bandwidth! This nails down the load transient response as expected.

Whenever the output sees a load transient, output voltage is first stabilized. The load difference due to mismatch between multiple parallel LDOs is then corrected for only after attaining load regulation. To ensure that the servo loop is less dominant than the core loop, the design of the following devices is important.

1. Output Resistor (R_{V2I})

The output resistor (R_{V2I}) is extremely important to the operation of load sharing as it generates the modulating output current to balance the load.

$$I_{out,\ servo\ loop} = \left(\frac{V_{INT} - V_{FB}}{R_{V2I}}\right)$$

The ratio of this resistor with respect to feedback resistors and the ratio of $I_{out,\ servo\ loop}$ to I_{FBQ} (=5μA) is crucial. The value of R_{V2I} is currently kept to 2MΩ to ensure proper operation.

2. Load Resistor (R_L)

$$V_M = V_{IN} - \left(\frac{I_2}{K * R_L}\right)$$

R_L defines the differential input to the amplifier. A larger value of R_L leads to a larger differential input to the amplifier. The large differential input might cause the integrator will accumulate more error than it wants and saturate V_{INT}. So it is important to maintain the value of R_L to an optimum value. The value of RL is kept at 5KΩ to ensure proper operation.

CHAPTER 4

SIMULATION SETUP AND RESULTS

4.1 Mismatch Introduction Schemes

Intentional mismatch is introduced between the parallel LDOs to visualize the response of the system. This is a vital set of simulations as no 2 LDOs are exactly the same. The percentage of mismatch introduced directly affects the load sharing accuracy and hence a considerate value is chosen based on experience. The V_{TH} mismatch and the V_{REF} mismatch are the largest contributors to load sharing accuracy. These mismatches are introduced as follows

4.1.1 Threshold Voltage Mismatch (gate voltage mismatch)

To model the V_{TH} mismatch of the pass device, a DC voltage source is placed in series from the output of buffer to input of pass device. The value of this is defined for each LDO as a parameter which is then set in the testbench. Fig. 4.1 shows this mismatch modeling in a 2 parallel LDO setup.

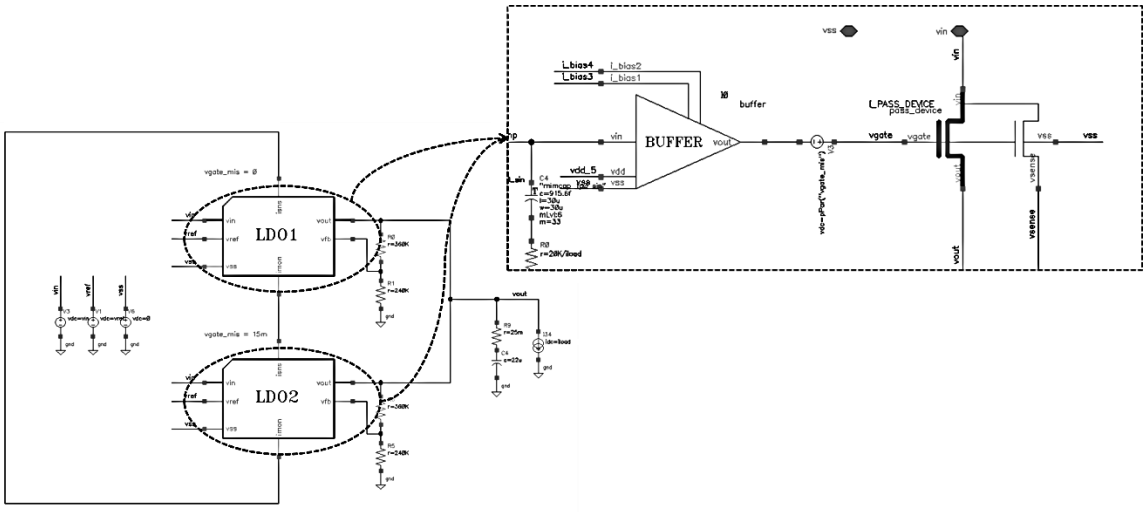


Figure 4.1 Threshold mismatch (gate mismatch) setup

4.1.2 Reference Voltage Mismatch

The reference voltage mismatch is another large contributor to load sharing accuracy and it can be modeled by individually changing the reference of each LDO. Fig. 4.2 shows this mismatch modeling in a 2 parallel LDO setup.

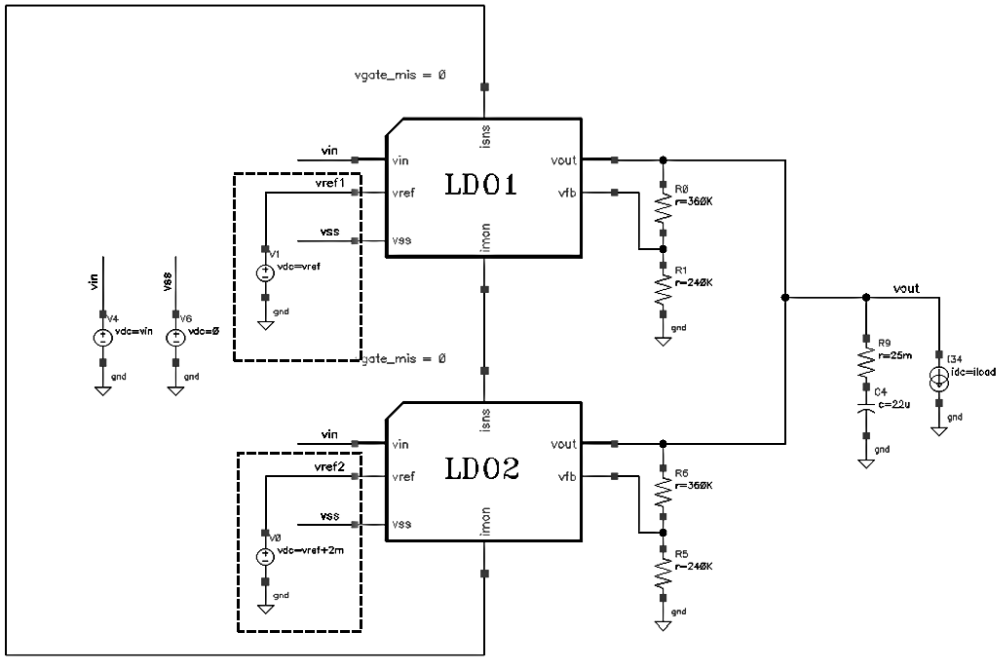


Figure 4.2 Reference mismatch setup

4.2 Simulation Results

4.2.1 Parallel LDOs – Transient Load Regulation

4.2.1.1 2 Parallel LDOs – V_{TH} Mismatch

A V_{TH} mismatch is introduced between the 2 LDOs with the following setup.

LDO1 → $V_{GATE} = V_{BUFFER\_OUT}$

LDO2 → $V_{GATE} = V_{BUFFER\_OUT} + 15mV$

V_{IN} = 1.5V, V_{OUT}=1V, I_{LOAD}=2*100µA → 2*2A → 2*100µA

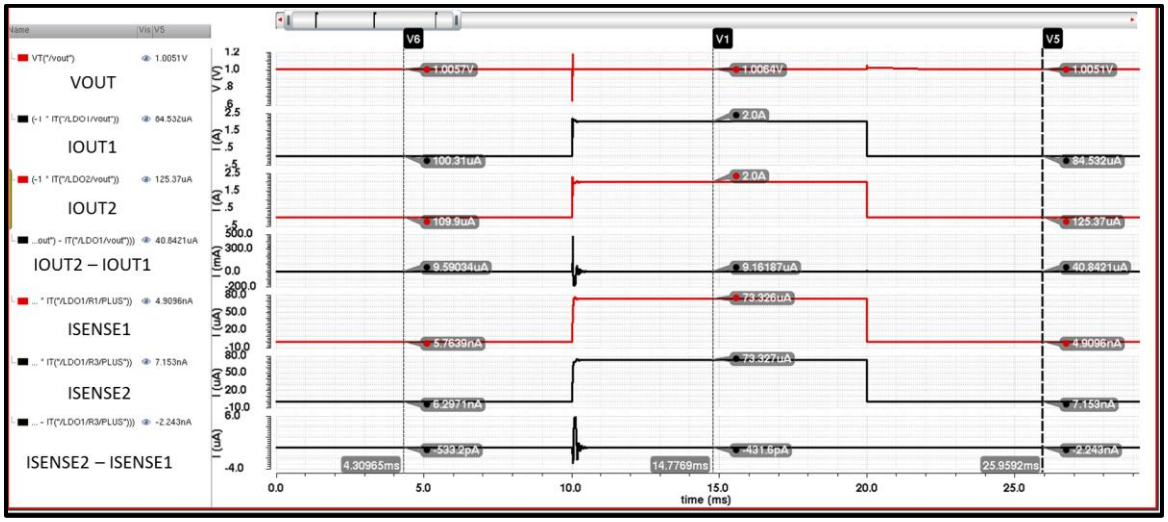


Figure 4.3 Load Regulation – 2 Parallel LDOs (V_{IN} = 1.5V, V_{OUT}=1V, TT, 27°C)

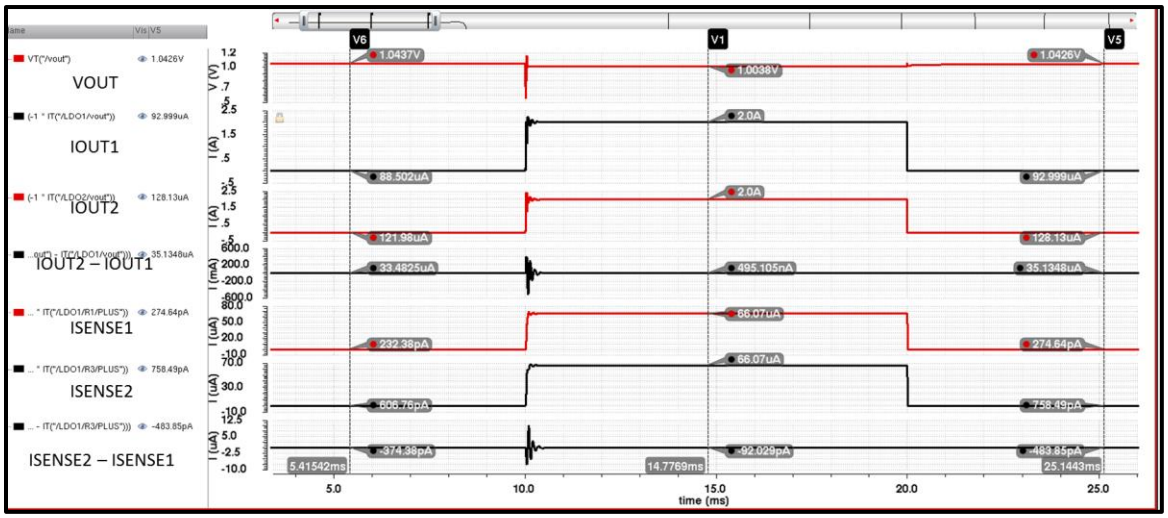


Figure 4.4 Load Regulation – 2 Parallel LDOs (V_{IN} = 1.5V, V_{OUT}=1V, FF, 125°C)

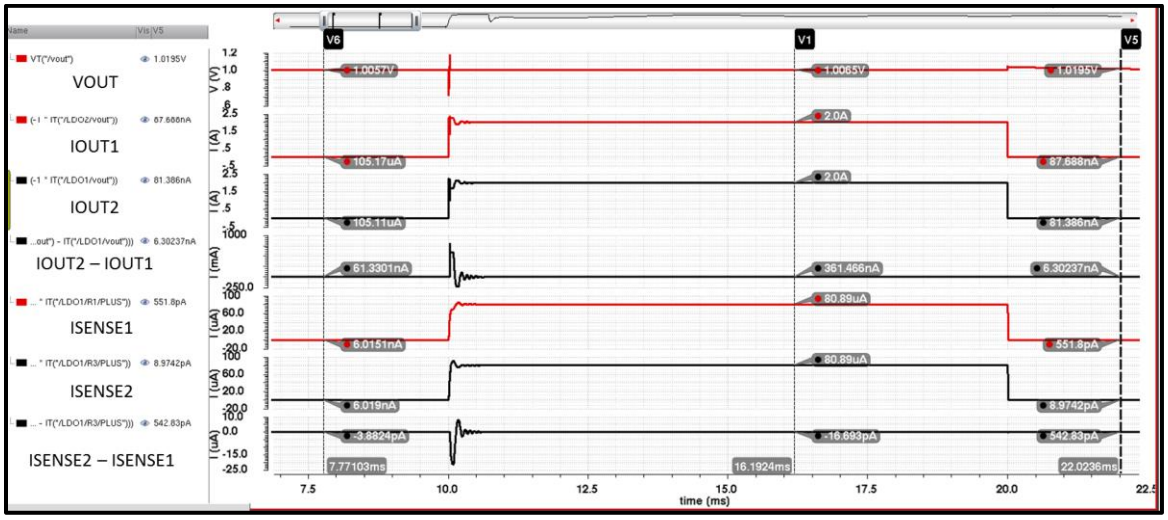


Figure 4.5 Load Regulation – 2 Parallel LDOs (V_{IN} = 1.5V, V_{OUT}=1V, SS, -40°C)

4.2.1.2 2 Parallel LDOs – V_{REF} Mismatch

A V_{REF} mismatch is introduced between the 2 LDOs with the following setup.

LDO1 → V_{REF} = 1.2V

LDO2 → V_{REF} = 1.2V + 2mV

V_{IN} = 3.3V, V_{OUT}=3V, I_{LOAD}=2*10mA → 2*2A → 2*10mA

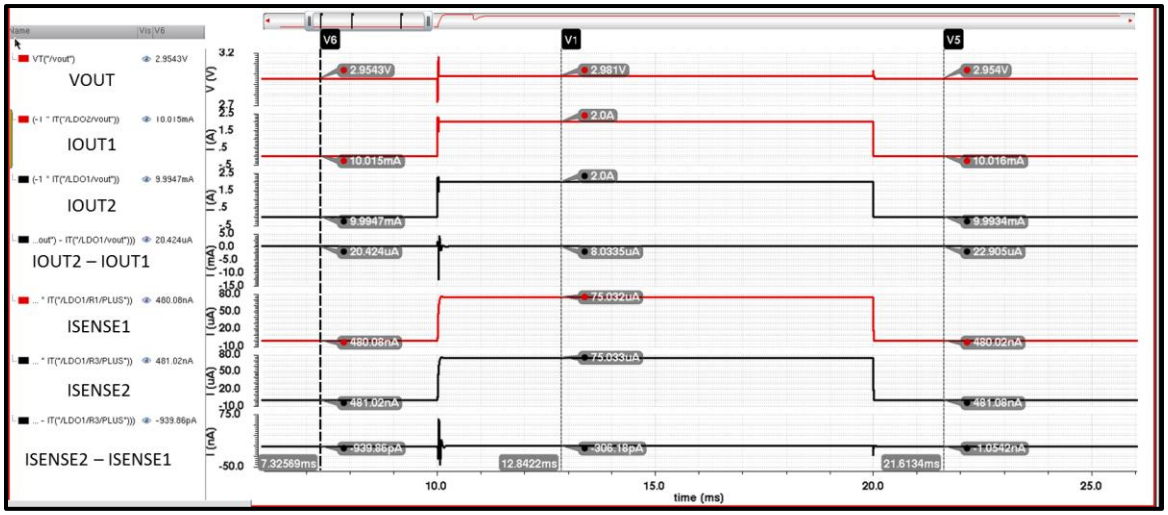


Figure 4.6 Load Regulation – 2 Parallel LDOs (V_{IN} = 3.3V, V_{OUT}=3V, TT, 27°C)

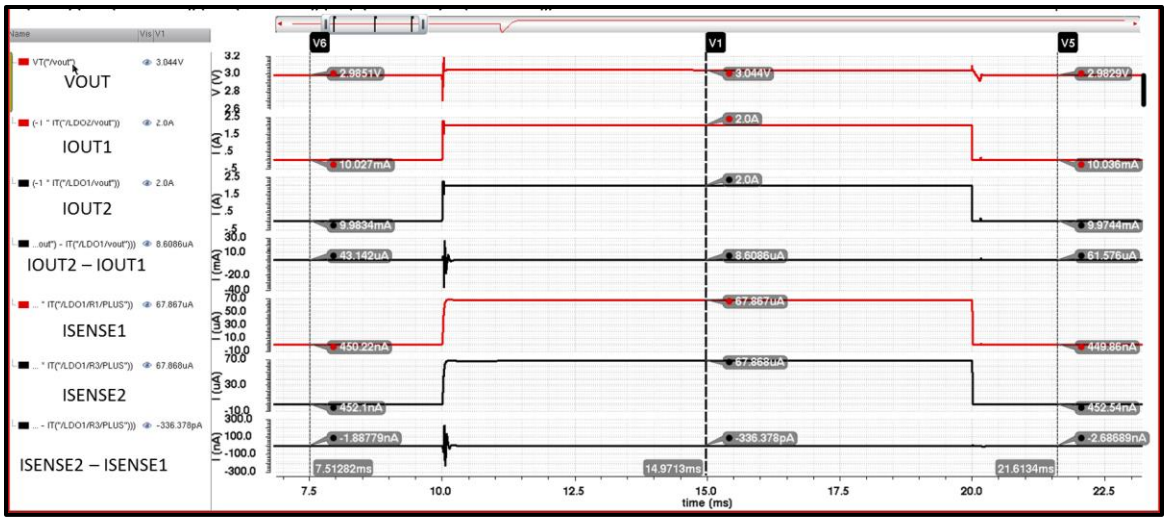


Figure 4.7 Load Regulation – 2 Parallel LDOs (V_{IN} = 3.3V, V_{OUT}=3V, FF, 125°C)

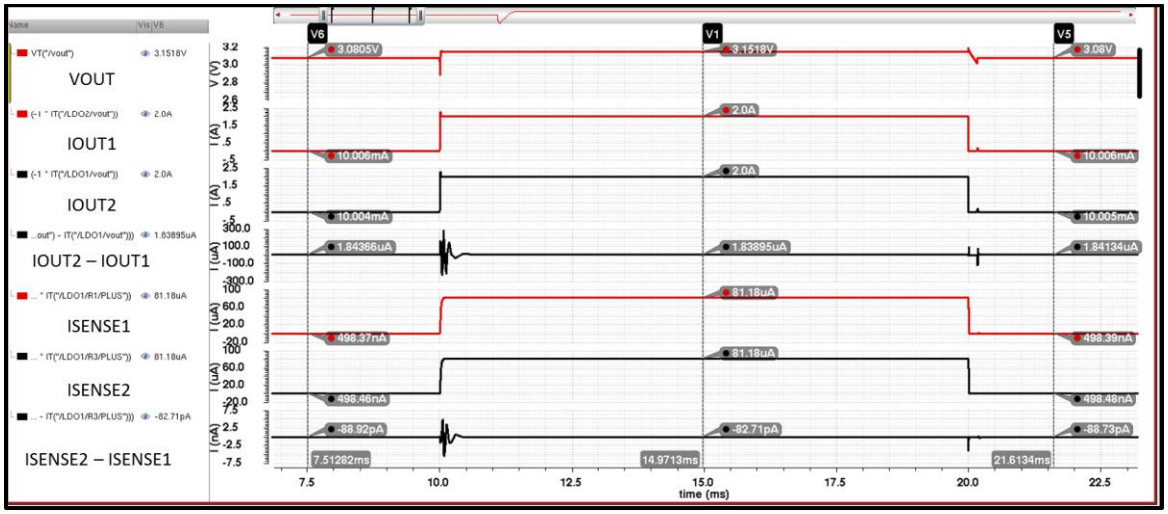


Figure 4.8 Load Regulation – 2 Parallel LDOs (V_{IN} = 3.3V, V_{OUT}=3V, SS, -40°C)

4.2.1.3 4 Parallel LDOs – V_{TH} mismatch

A V_{TH} mismatch is introduced between the 4 LDOs with the following setup.

LDO1 → V_{GATE} = V_{BUFFER_OUT}

LDO2 → V_{GATE} = V_{BUFFER_OUT} + 15mV

LDO3 → V_{GATE} = V_{BUFFER_OUT} + 5mV

LDO4 → V_{GATE} = V_{BUFFER_OUT} + 10mV

V_{IN} = 3.3V, V_{OUT}=3V, I_{LOAD}=4*100µA → 4*2A → 4*100µA

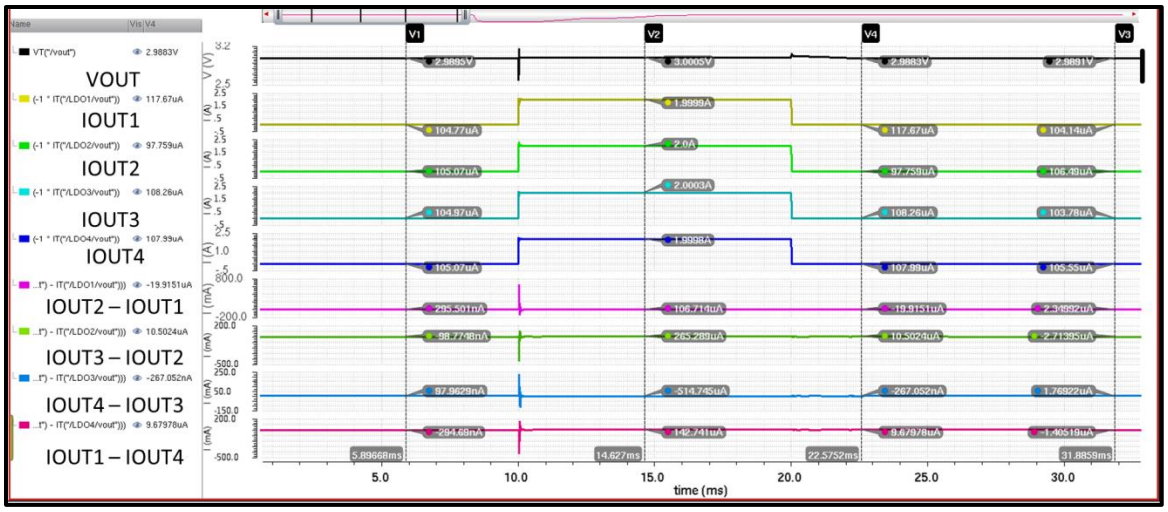


Figure 4.9 Load Regulation – 4 Parallel LDOs (V_{IN} = 3.3V, V_{OUT}=3V, TT, 27°C)

4.2.1.4 4 Parallel LDOs – V_{REF} mismatch

A V_{REF} mismatch is introduced between the 4 LDOs with the following setup.

LDO1 → V_{REF} = 1.2V

LDO2 → V_{REF} = 1.2V + 2mV

LDO3 → V_{REF} = 1.2V – 2mV

LDO4 → V_{REF} = 1.2V + 1mV

V_{IN} = 3.3V, V_{OUT}=3V, I_{LOAD}=4*10mA → 4*2A → 4*10mA

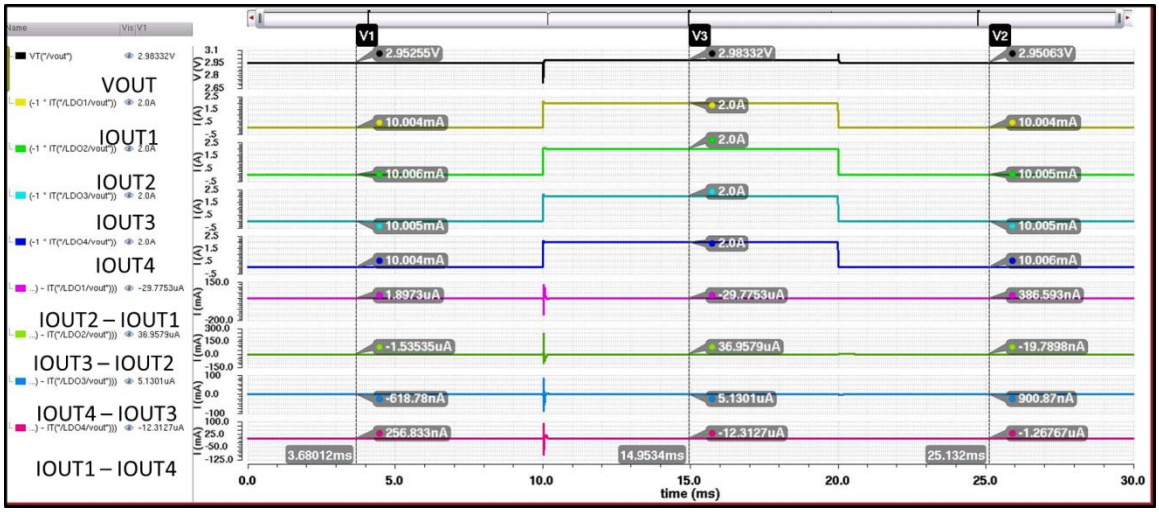


Figure 4.10 Load Regulation – 4 Parallel LDOs (V_{IN} = 3.3V, V_{OUT}=3V, TT, 27°C)

4.2.3 Parallel LDOs –Transient Line Regulation

4.2.3.1 2 Parallel LDOs – V_{TH} mismatch

A V_{TH} mismatch is introduced between the 2 LDOs with the following setup.

LDO1 → V_{GATE} = V_{BUFFER_OUT}

LDO2 → V_{GATE} = V_{BUFFER_OUT} + 15mV

V_{OUT}=3V, I_{LOAD} = 2A, TT, 27°C, V_{IN}= 3.3V → 5V → 3.3V

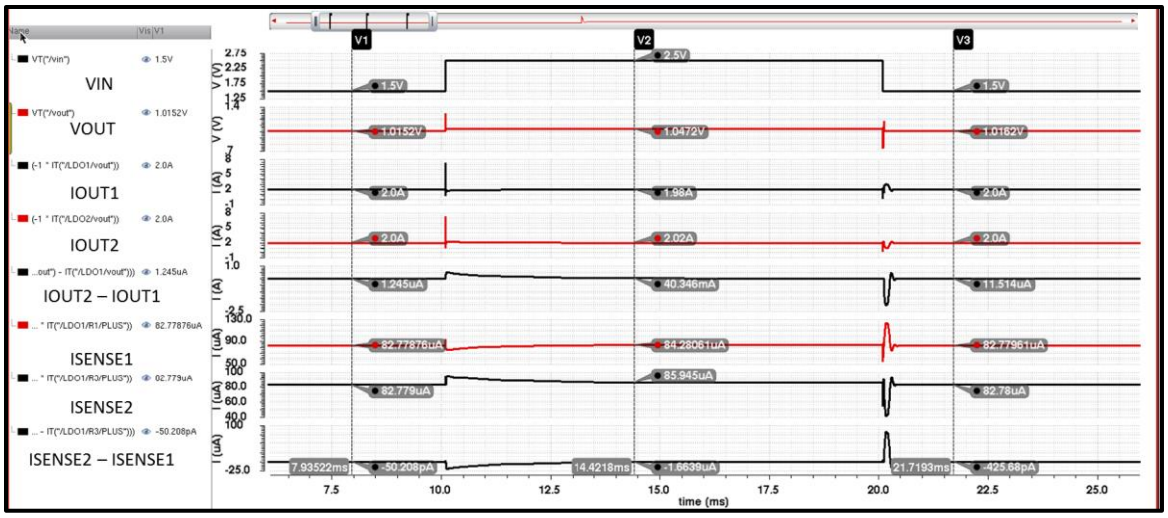


Figure 4.11 Line Regulation – 2 Parallel LDOs (I_{LOAD}= 2A, V_{OUT}=1V, TT, 27°C)

4.2.4 Power Supply Rejection

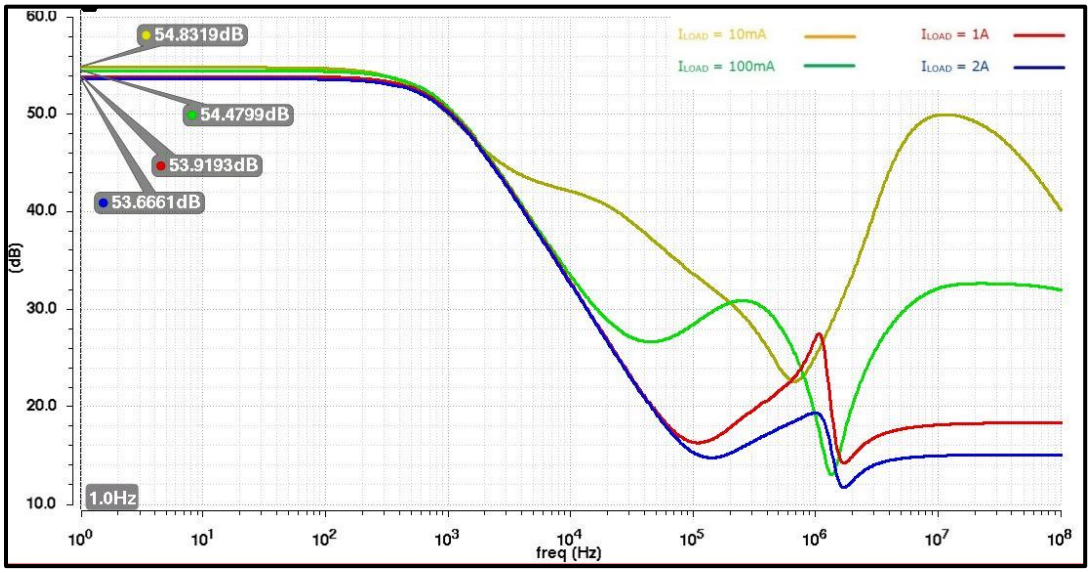
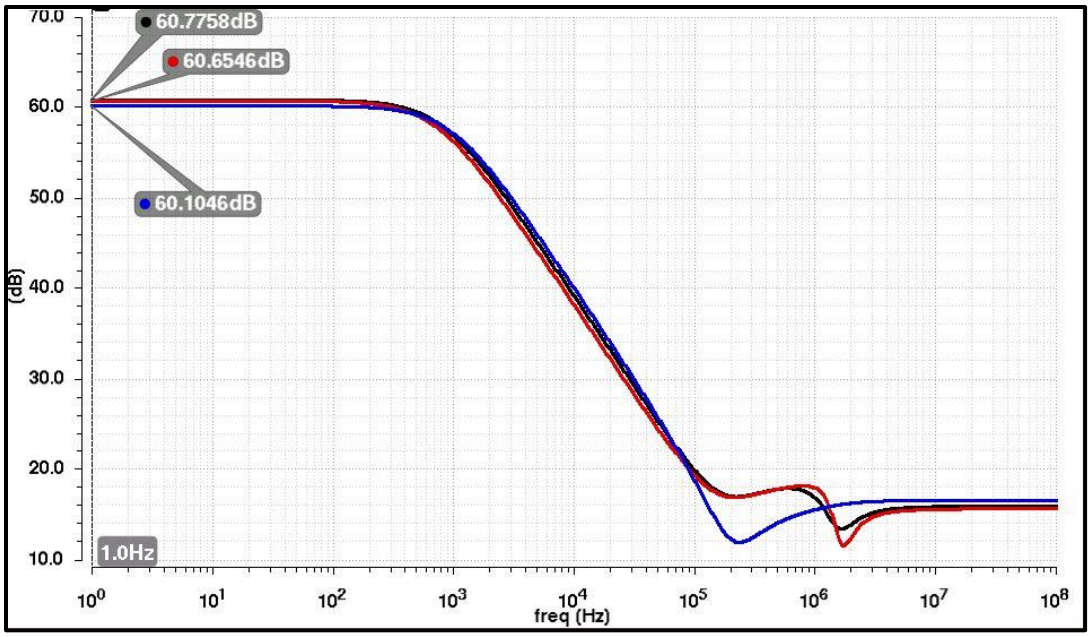


Figure 4.12 Power Supply Rejection for different I_{LOAD} (V_{IN} = 3.3V, V_{OUT}=3V)



TT,27°C SS, -40°C FF, 125°C

Figure 4.13 Power Supply Rejection across corners (V_{IN} = 3.3V, V_{OUT}=3V, I_{LOAD}=2A)

CHAPTER 5

THESIS SUMMARY AND FUTURE WORK

5.1 Summary

A daisy-chain approach to load current sharing for Low Dropout (LDO) Regulators is proposed as part of this research. Novel techniques like Dynamic Element Matching (DEM) based current sensing & Switched Capacitor based pole-zero tracking compensation are implemented to ensure the desired load sharing accuracy of 1% at high loads. The use of a servo loop based integrator approach ensures a fast and stable response to load balancing. The LDO is designed on the TSMC 180nm BCD Gen2 process for a range of output voltages (1V to 3V) and a high full-load current of 2A with the quiescent current consumption restricted to 300µA which are suitable for handheld battery-powered devices.

The proposed solution also reduces the cost of the entire system by eliminating the need for external sense resistors or components or matched PCB traces. The ease of use for the end user is vastly increased as the solution can theoretically be extended to support a large number of LDOs in parallel.

5.2 Future Work / Improvements

5.2.1 Error Feedback Point

Currently, the error current from the integrating servo loop is fed back to the LDO core loop's voltage feedback point. This has some limitations as a residual current from the integrator might cause an inadvertent static deterministic shift in regulated output voltage. Such an approach will also eliminate the need of R_{V2I} which is a large on-chip resistor.

To avoid this limitation, a better feedback point can be contemplated. One approach currently under consideration is to negatively feed the error at the input of

the buffer through the usage of a voltage subtractor. Another approach is to employ a differential difference amplifier topology for the error amplifier with the servo loop error acting as the rest of the input. The gain of the LDO core loop can be kept higher than that of the servo loop thereby ensuring output voltage regulation in presence of a load transient.

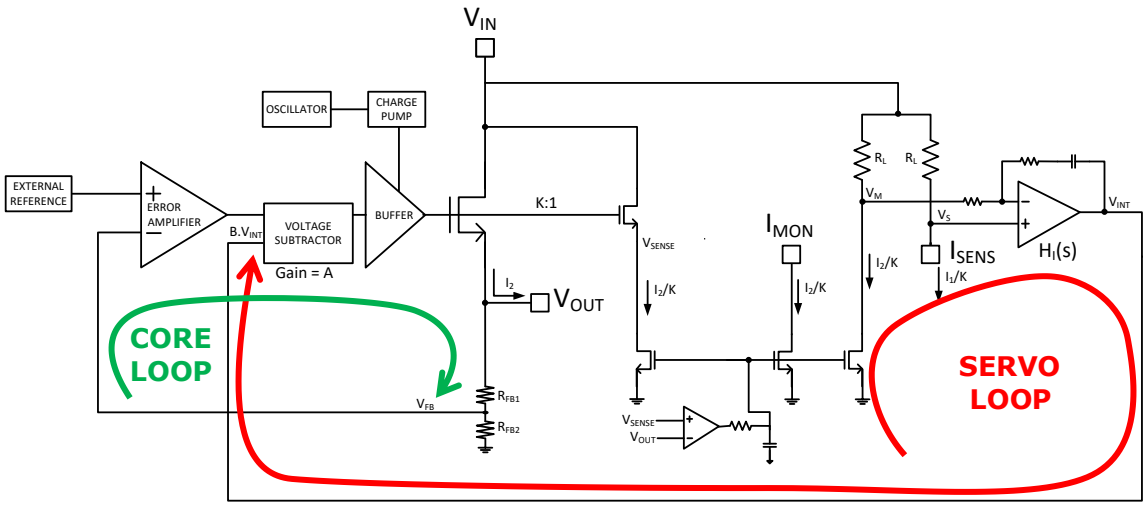


Figure 5.1 Better error feedback scheme

This approach also eliminates the use of the output resistor of the servo loop and may also eliminate individual feedback resistors for each LDO further reducing the size of the system.

5.2.2 Servo Amplifier Topology and Chopper Stabilization

A current input, voltage/current output topology for the servo amplifier can help to remove the need for R_L and possibly even R_{V2I}. The input-referred offset can further be reduced by introducing chopper stabilization in the servo amplifier. Both these techniques can further enhance the load sharing accuracy.

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