System Identification, Diagnosis, and Built-In Self-Test of High Switching Frequency DC-DC Converters

by

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ABSTRACT

Complex electronic systems include multiple power domains and drastically varying dynamic power consumption patterns, requiring the use of multiple power conversion and regulation units. High frequency switching converters have been gaining prominence in the DC-DC converter market due to smaller solution size (higher power density) and higher efficiency. As the filter components become smaller in value and size, they are unfortunately also subject to higher process variations and worse degradation profiles jeopardizing stable operation of the power supply.

This dissertation presents techniques to track changes in the dynamic loop characteristics of the DC-DC converters without disturbing the normal mode of operation. A digital pseudo-noise (PN) based stimulus is used to excite the DC-DC system at various circuit nodes to calculate the corresponding closed-loop impulse response. The test signal energy is spread over a wide bandwidth and the signal analysis is achieved by correlating the PN input sequence with the disturbed output generated, thereby accumulating the desired behavior over time. A mixed-signal cross-correlation circuit is used to derive on-chip impulse responses, with smaller memory and lower computational requirement in comparison to a digital correlator approach. Model reference based parametric and non-parametric techniques are discussed to analyze the impulse response results in both time and frequency domain.

The proposed techniques can extract open-loop phase margin and closed-loop unity-gain frequency within 5.2% and 4.1% error, respectively, for the load current range of 30-200mA. Converter parameters such as natural frequency (ω_n), quality factor (Q), and center frequency (ω_c) can be estimated within 3.6%, 4.7%, and 3.8% error respectively, over load inductance of 4.7-10.3µH, and filter capacitance of 200-400nF.

A 5-MHz switching frequency, 5-8.125V input voltage range, voltage-mode con-

trolled DC-DC buck converter is designed for the proposed built-in self-test (BIST) analysis. The converter output voltage range is 3.3-5V and the supported maximum load current is 450mA. The peak efficiency of the converter is 87.93%. The proposed converter is fabricated on a 0.6µm 6-layer-metal Silicon-On-Insulator (SOI) technology with a die area of $9mm^2$. The area impact due to the system identification blocks including related I/O structures is 3.8% and they consume 530µA quiescent current during operation.

To my parents and brother

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CHAPTER 1

INTRODUCTION

Power management circuits are undoubtedly one of the most ubiquitous circuits in the world of present day electronics. They can be found in applications requiring power ranging from several hundred milliwatts to hundreds of megawatts. They have helped in the move towards a more sustainable future by finding applications in wind-turbines, solar farms, and voltage/current scaling using solid-state transformers. They have also proved their utility in medium and low power application areas such as battery operated electric vehicles, spacecrafts and rovers, computers, smart-phones, and electronic lighting. In recent years, several new application areas encompassed under the umbrella of Internet of Things (IOT) have emerged. These systems are the backbone of the internet era infrastructure and are becoming increasingly complex requiring highly reliable operation and effectively zero downtime. Any downtime in these critical systems may result in disruption of daily life and loss of millions of dollars. The compound annual growth rate (CAGR) of power management integrated circuits (PMIC) market is estimated to be 6.15%, priced at $46 billion in 2019 [1]. This valuation is expected to grow due to PMICs increasingly being used in medical, industrial, and military sectors and in emerging novel applications such as autonomous self-driving cars and virtual/augmented reality.

Based on the type of input and output power, power management systems can be classified as DC-DC (switching converters and linear regulators), DC-AC (inverters), AC-DC (rectifiers), and AC-AC (cycloconverters). The work presented in this dissertation focuses specifically on the DC-DC switching converters.

1.1 Research Background

DC-DC converters have been widely used as an integral part of PMICs and power management units (PMUs) in computers, communications, and consumer electronics. They are commonly used as an interfacing stage between the energy source and the load. Usually, the load requires a constant supply voltage with minimal disturbance. DC-DC converters control the flow of energy from the source to the load and maintain the desired output voltage level amidst the disturbances such as variable input voltage and load current. Numerous such converters are used in present day PMICs and PMUs instead of using a central converter. This power delivery architecture is known as point-of-load (PoL) supply scheme. PoL schemes have several advantages. First, power is supplied at high voltage (low current) directly up to the load where it is converted to the desired voltage level by the PoL DC-DC converter. This results in reduced circuit area due to the decreased wiring required to achieve the same level of conduction losses. Second, each load can be supplied with an independent voltage at different voltage levels thus improving transient performance (tighter voltage regulation) by separating power domains with drastically varying dynamic power consumption patterns and at the same time reducing noise coupling between various circuits. Third, PoL scheme increases the reliability of these critical systems by avoiding a single central point of failure.

DC-DC converters can be categorized into two major categories, namely switching regulators and low dropout voltage regulator (LDO). LDOs, also known as linear regulators, are advantageous as they have relatively small size and provide low-noise output voltage but at the expense of reduced efficiency. Also, they can only provide an output voltage lower than the input voltage. They are mostly used to power noise sensitive analog and radio frequency (RF) circuits such as clock generators, envelope

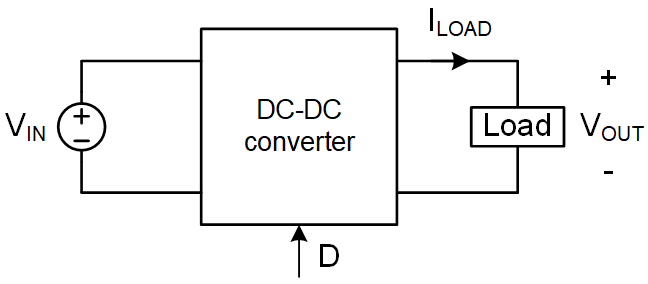


Figure 1.1: A DC-DC switching converter.

trackers, etc. On the other hand switching regulators are used in applications which require high efficiency. Additionally, they can both step-up and step-down the supply voltage and can provide negative (inverted) DC voltages. Even though the switching regulators have higher complexity, noise, and area, they are the preferred regulator of choice in battery based and high load current applications.

Figure 1.1 shows a basic diagram of a DC-DC switching converter [2]. It converts a DC input voltage, V_{IN}, to a DC output voltage, V_{OUT}, for a certain range of load current, I_{LOAD}. The switching converter includes one (or several) switches in order to control the output voltage. A constant output voltage is achieved by controlling the on/off time of the switches. The frequency at which these switches are operated is called the switching frequency (f_{SW}) of the converter. The turn on and turn off time of the switches is controlled by the signal D, the duty cycle. The duty cycle is defined as the percentage of time the signal is high to the total switching time period ($T_{SW} = 1/f_{SW}$). The controlled voltage passes through a junction of switches called the switching node. The voltage at the switching node is filtered by using inductor and capacitor based filters. Resistor based filters are avoided to obtain a higher efficiency converter.

Several different topologies can be obtained by connecting the switches and filter components in different ways. The most common method of classification of the

topologies is based on the input and output voltage of the converter. They are: buck (steps-down the input voltage), boost (steps-up the input voltage), and buck-boost (both steps-up and steps-down the input voltage). More advanced topologies which are widely used are Ćuk, SEPIC, forward, and flyback converters.

The converters can also be classified based on switch/diode use in power train (synchronous and asynchronous), control types (analog or digital control), controller type (voltage control, current control, hysteretic control, etc.), phase boost provided by the controller (Type I, Type II, or Type III), number of phases (single-phase or multi-phase) and if the topology is isolated or non-isolated. Detailed discussion of all of these classifications are out of the scope of this dissertation, but a brief introduction to a DC-DC buck converter is presented in the following section.

1.2 DC-DC Buck Converter

A DC-DC buck converter is used to convert a higher DC input voltage, V_{IN}, to a lower DC output voltage, V_{OUT}. Figure 1.2 shows a buck converter with switches Q_P and Q_N which are used to control the output voltage level. The junction node of Q_P and Q_N is called the switching node and the voltage at this node is a square waveform (V_{SW}). When Q_P is on (and thus Q_N is off), V_{SW} is equal to V_{IN}. Alternatively, when Q_N is on (Q_P is off), V_{SW} is equal to 0 (GND). The width of the pulse V_{SW} is

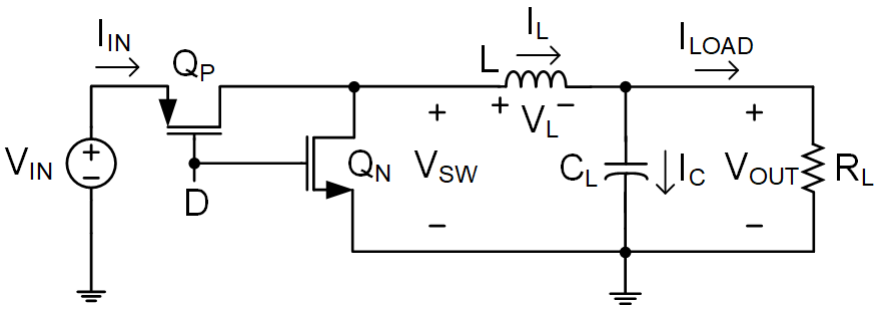


Figure 1.2: Buck converter power stage.

decided by the duty cycle, D. The switching voltage is filtered using a second order filter designed using an inductor (L) and a capacitor (C_L) to minimize the ripple and provide a DC voltage at the output node. This open loop circuit is part of a buck converter and is referred to as the power stage of the converter.

In the illustrated diagram, Q_P is a p-type power FET used at the high-side while Q_N is an n-type power FET used at low-side of the power train. The high-side p-type switch can be replaced with an n-type switch for better speed and area efficiency but at the cost of higher design complexity. The turn on/turn off of the switches then is controlled by the complimentary signals D and $\bar{D}$. Complimentary signals are used to avoid turning on both the switches at the same time causing a short between V_{IN} and GND resulting in high current flow and damage to the switches.

Assuming ideal components with zero losses, the average input power ($\bar{P}_{IN}$) is equal to the average output power ($\bar{P}_{OUT}$) and hence theoretically a DC-DC converter can achieve 100% efficiency. It is common for carefully designed practical switching converters to have efficiencies reaching around 96% under suitable operating conditions. Furthermore, a relationship between V_{IN} and V_{OUT} can be calculated by using volt-second balance across the filter inductor. This relationship is given by:

$$V_{OUT} = D \cdot V_{IN} \tag{1.1}$$

Consequentially, using the input/output power relationship and (1.1), during steady state (defined as when output current is constant and V_{OUT} has settled to its final value) the relationship between average input current ($\bar{I}_{IN}$) and the output current (I_{OUT}) of an ideal buck converter can be calculated as:

$$\bar{I}_{IN} = D \cdot I_{OUT} \tag{1.2}$$

The converter provides a constant output voltage across a range of load currents.

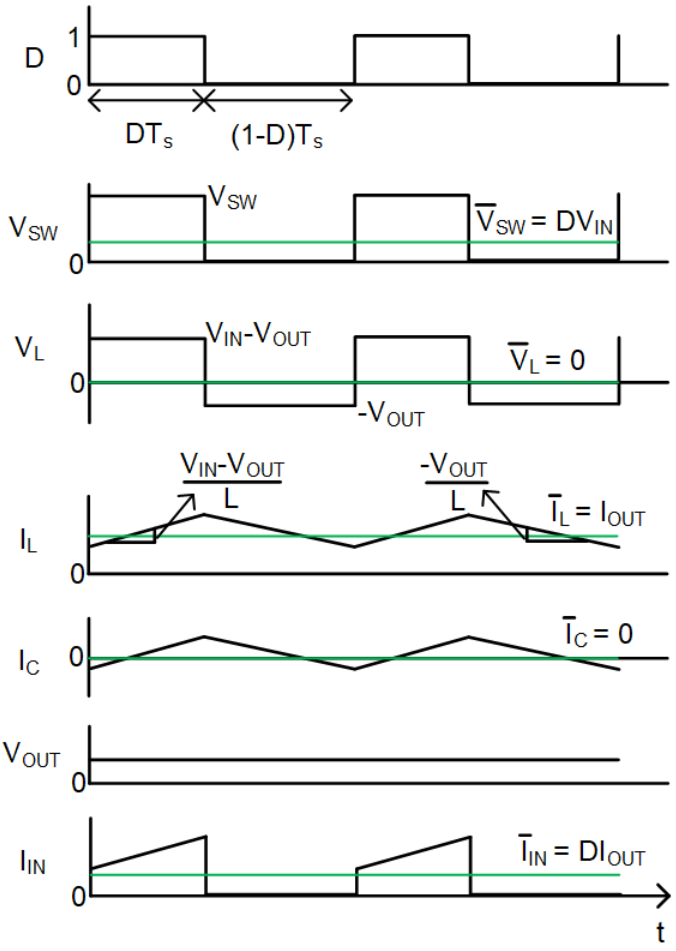


Figure 1.3: Buck converter waveforms during steady state operation.

The load is usually modeled as a DC load current sink or a resistor of value $R_L = V_{OUT}/I_{OUT}$ connected between V_{OUT} and GND.

The steady state waveforms related to important converter voltages and currents such as V_L (voltage across the inductor), I_L (current through the inductor), I_C (capacitor current), etc. are shown in Figure 1.3.

1.3 Motivation

Dynamic voltage scaling (DVS) DC-DC converters are an essential part of the PMUs used in the state-of-the-art system-on-chips (SOCs). DVS DC-DC converters

require fast transient response to reach the desired output voltage level quickly, to meet strict power-performance criteria [3]. DVS is used to save power and further increase the overall system efficiency. Also, these electronic systems use PoL supply scheme and contain multiple power domains. For example, Intels 6^{th} generation Core processor, Skylake, has 34 power domains supplied by several DC-DC switching converters [4]. To improve the settling time and power density, these converters are designed to operate at a high switching frequency, resulting in low inductor and capacitor values in their output filters [2]. However, small components suffer from larger manufacturing variations and increased degradation over their operational lifetime [3], [5], [6]. The component variations result in degradation of the dynamic performance and stability of the DC-DC converter [7]. Additionally, control loop characteristics are also affected by the variable load current, causing the loop dynamics to change, resulting in variation of open-loop phase margin (PM) [7].

Figure 1.4 shows a DC-DC converter with typical variations associated with its components. In [7], it has been shown that for a typical DC-DC converter, open loop frequency response PM drops 13° caused by ±25% variation in the output filter and load current. Variation in the power train and controller may reduce the PM even further. To compensate for these high variations and to maintain operation in worst case scenarios, the systems are often over-designed. Even then in many cases, the converter can become unstable over time and may also cause reliability issues in the systems powered by it.

As an example of typical variation, consider the output filter capacitor. In addition to manufacturing variations, the filter capacitor may degrade with respect to time (aging), temperature, and voltage [8], [9]. Voltage variation across the capacitor alone can cause a derating of up to 70% in capacitor value. Figure 1.5 shows capacitor variation for most used ceramic capacitors with respect to temperature, time,

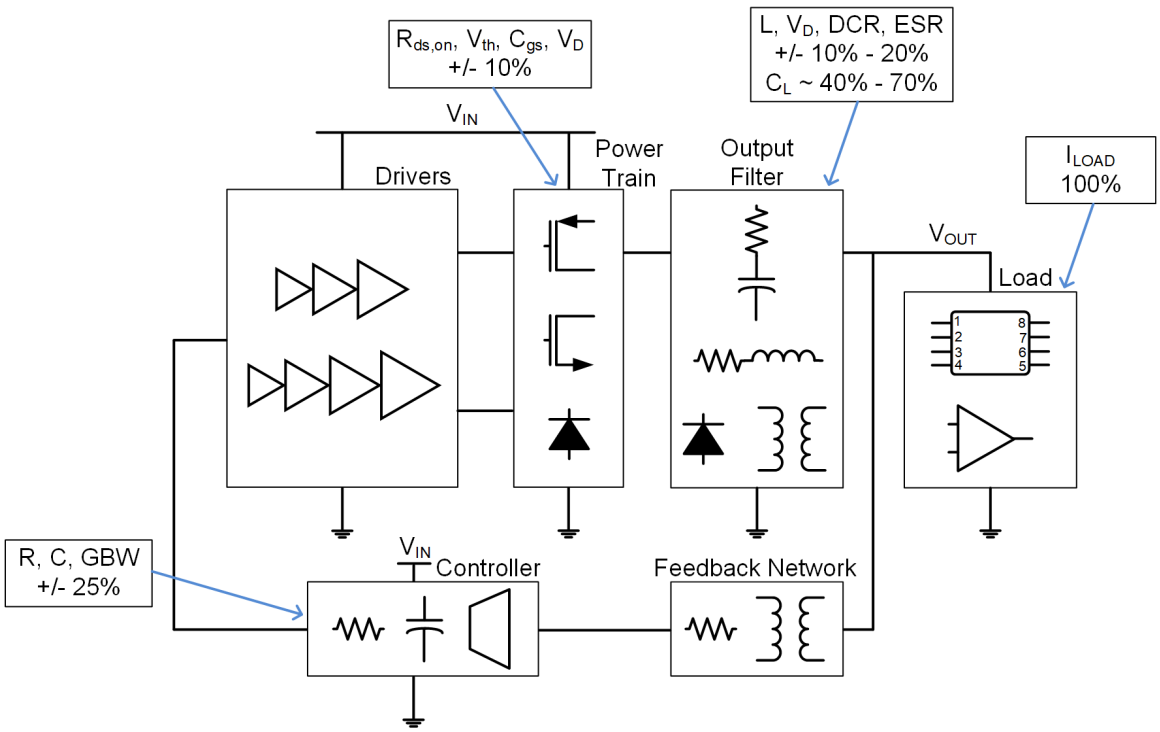


Figure 1.4: A DC-DC switching converter with typical variations associated with its components.

and voltage [10]. When the filter capacitor of the switching converter degrades, the transient performance of the converter is negatively affected. Figure 1.6 shows if the filter capacitor is highly derated, then a sudden increase in load current will result in a large undershoot which may result in memory reset in digital systems. Alternatively, a sudden decrease in load current will result in large overshoot which may result in electrical stresses in analog and digital circuits alike.

Hence, detecting the changes in loop dynamics and tracking performance degradation of the DC-DC converter filter components during closed-loop operation is a critical requirement for high reliability operation in automotive, aerospace, big-data and cloud computing applications.

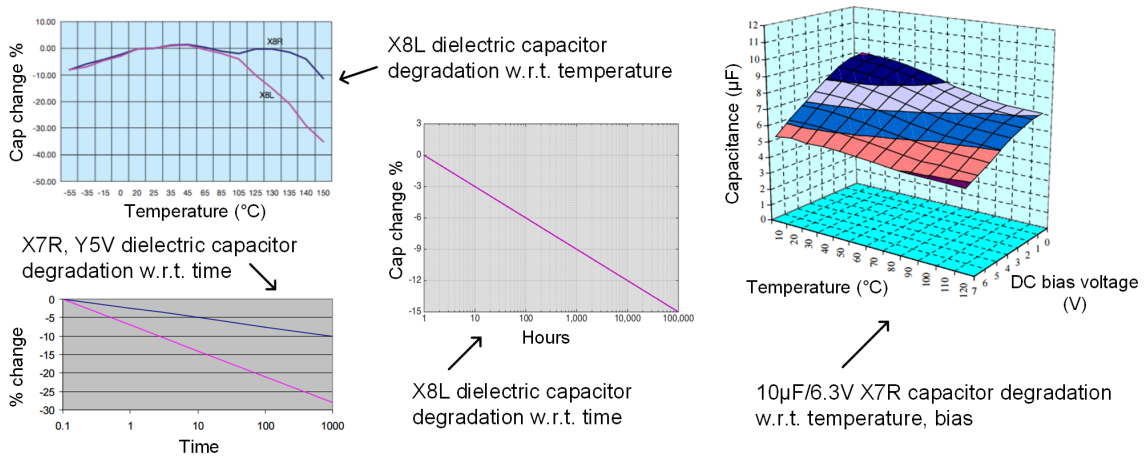


Figure 1.5: Typical variations associated with capacitors [8], [9].

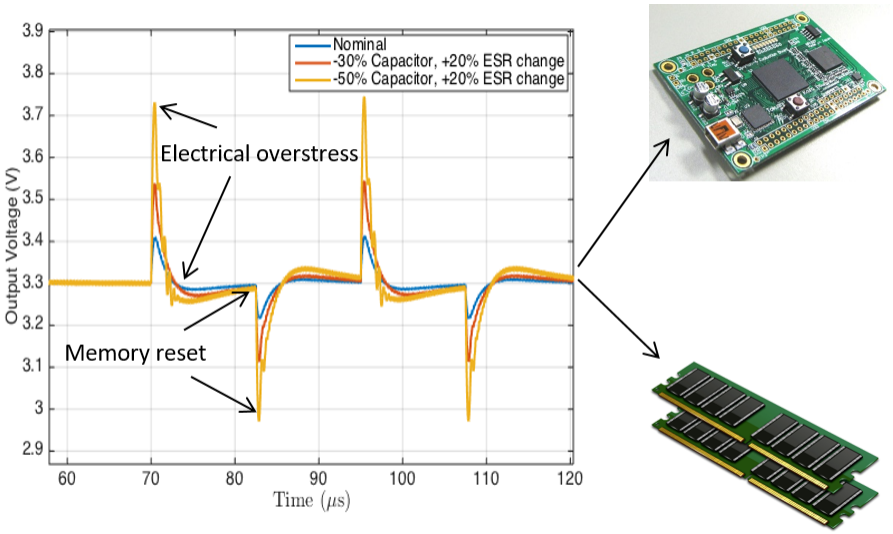


Figure 1.6: Transient performance degradation due to capacitor derating.

1.4 Dissertation Outline

This dissertation examines the techniques that can be used to diagnose and predict the degradation of switching converters filter components before a converters complete failure. Mathematical analysis and circuit implementation of such techniques are covered in this study. The techniques are applied on a voltage mode buck converter and experimentally verified. The document is organized as follows:

Chapter 1 provides a brief introduction to the DC-DC converters, explains their utility in modern day electronics, and the importance of reliable operation of these systems. This chapter thus introduces the research background and motivation behind the present work. Chapter 2 covers the survey of relevant literature. Existing techniques used for system identification of analog and digitally controlled converters are reviewed. A comparison of previous works based on their advantages and disadvantages is presented and the relevance of the work done in this study is also compared with them. Chapter 3 discusses the mathematical foundation of the suggested system identification techniques and the analysis methods. Chapter 4 presents the system architecture and the circuits used to implement the system identification method in the integrated circuit (IC) environment. Chapter 5 demonstrates the measurement results obtained using the designed IC. Chapter 6 summarizes the key findings of the dissertation and provides a discussion on possible future work.

CHAPTER 2

LITERATURE REVIEW AND PROPOSED APPROACH

This chapter provides a broader context of system identification and specific discussion on relevant prior work. Different techniques which have been used traditionally for system identification are discussed. They are evaluated based on their merits and ease of implementation and analysis. The signals which are used to perform the system identification are also analyzed and their effectiveness is compared. Various works have shown implementation of system identification techniques on DC-DC switching converters. These works are compared with the solution proposed in this dissertation.

2.1 System Identification

System identification techniques are classified as parametric and non-parametric [11], [12]. In parametric identification methods, the system to be identified is parameterized into a known system model structure and excited using a stimulus. The coefficients of this model are then estimated based on the observed response. On the other hand, non-parametric identification methods do not assume any particular structure. Instead, the system to be identified is excited using an appropriate stimulus and time-domain and/or frequency-domain response data are obtained directly from the observed response. In both cases, the results obtained can be compared to the similar results from a reference model calculated at nominal/ideal operating conditions using standardized testing methods [13]. This comparison indicates that the system has changed due to the change in operating conditions, component drift, and process-voltage-temperature (PVT) variation. When the observed response obtained using parametric techniques is compared with the reference response, it is referred

to as parametric model reference system identification method. Alternatively, when the observed response obtained using non-parametric techniques is compared with the reference response, it is referred to as non-parametric model reference system identification method.

This dissertation focuses on DC-DC power converters, hence system identification will be discussed from the perspective of application to electronic circuits.

2.1.1 Requirements for System Identification

System identification can be used to test a system or circuit during the product manufacturing process. Although it is not sufficient to monitor and qualify the system only during the manufacturing process as system performance and circuits can also be affected at the customers end during field operation. Hence, the utility of system identification will increase many-folds if it can be used during in-field operation. Additionally, it is advantageous if the process can be used without disrupting the normal operation of the systems and circuits. Here, *in-field* refers to the capability of system identification process and circuitry to operate at the customer end. A system being *on-line* means the system is operational and supplying the load without any disruption or loss of regulation when system identification is performed on it.

An in-field system identification technique for measurement of loop characteristics requires several qualities:

1. The system identification technique should have minimal effect on the output voltage of the converter,

2. Loop measurements need to be conducted during closed loop operation, at the operating point of the system,

3. System output response should have sufficient dynamic range,

4. The measurement needs to present little to no computational overhead and silicon die area.

2.2 Application of System Identification to DC-DC Switching Converters

System identification techniques have been applied to digitally controlled DC-DC converters in [14]-[27], and to analog converters in [28]-[39]. The techniques used in [14]-[19] and [28]-[33] qualify as parametric methods while [20]-[27] and [34]-[39] use non-parametric methods for system identification. Non-parametric system identification methods include transient response analyses such as impulse response [20], step response [15], [16], cross-correlation [20]-[25], [39], and frequency response using single tone sine-sweep [26], [36], [37] and multi-tone input [27], [35]. Limit-cycle oscillations (LCOs) based techniques can be used for both parametric system identification as in [17] and [32], or for non-parametric system identification as in [38]. In addition to non-parametric based identification, cross-correlation based techniques have also been used for parametric system identification [14], [18], [19], [28].

2.3 Discussion on Relevant Prior Works and Techniques

A number of methods have been proposed to self-test DC-DC converters using various test signals, as mentioned in section 2.2, to characterize the converters. Some techniques require the converter to be in open-loop and thus cannot reliably supply the connected load during testing, while others can be used in closed-loop, but are only applicable to digitally controlled systems. Many of these techniques have high hardware and computational requirements. The relevant techniques and architectures used previously to characterize the DC-DC converter systems are discussed in the following section.

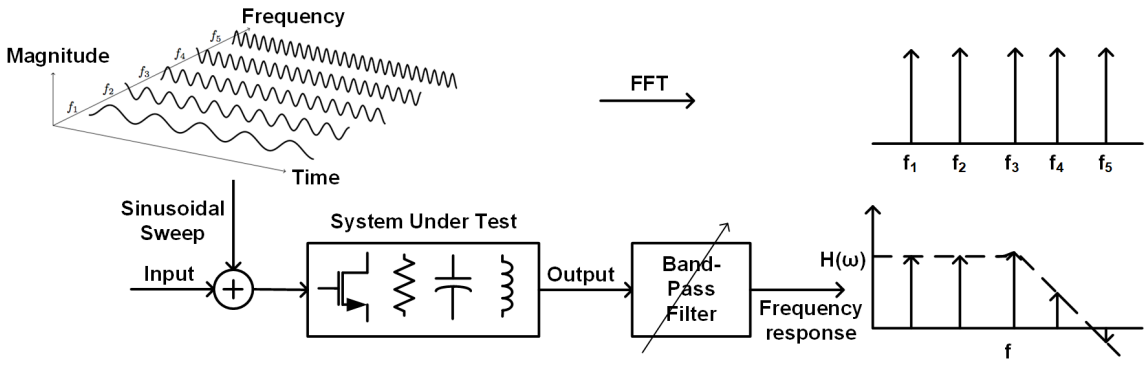


Figure 2.1: System characterization using frequency swept-sinusoidal method.

2.3.1 Frequency Swept-Sinusoidal Methods

The most basic method for system identification is to use a frequency-swept sinusoidal input to characterize the frequency response of the system [2]. Instruments such as spectrum analyzers use a sweep of a wide range of frequencies to characterize the input signal and produce a power spectral density analysis of the signal. Figure 2.1 shows the procedure to characterize the frequency response of the system-under-test (SUT) using frequency swept-sinusoidal method. The SUT is excited using a range of single or multi-tone sinusoidal signals. The output is passed through a band-pass filter and the amplitude and phase response information of the system output is obtained and thus the system behavior is characterized.

However, this approach is not suitable for on-line, closed-loop power system identification, and more so for an integrated circuit. To accurately obtain the frequency response of the system, very fine change in the step size of the frequency of input sinusoids is required. Thus, this method is hardware extensive and also requires computationally intensive post-processing. Most importantly swept-sinusoidal techniques result in significant tonal content concentrated at particular frequencies at the regulator output which may interfere in proper operation of the loads and also

result in electro-magnetic interference (EMI) problems. Even-though it is one of the most accurate methods for system characterization, it is not a preferred choice for an integrated built-in self-test (BIST) capable implementation of a DC-DC converter.

2.3.1.1 Single-Tone Excitation

A sweep of single-tone sinusoidal signals can be used to identify the frequency response of a converter system as presented in [26]. The method uses a software frequency response analyzer (SFRA). The software is loaded on the embedded digital processor which is used to control the DC-DC converter loop digitally. This implementation disposes of the need for an external FPGA/DSP. The proposed approach first measures the control-to-output transfer function to characterize the plant by injecting the sinusoidal perturbation at the control node in open-loop. Measurement of the loop transfer function can be subsequently done in closed-loop. As the plant transfer function is known from open loop measurements, the compensator transfer function can be extracted from the closed-loop measurements.

Although accurate, the single-tone sine sweep requires a long time for completion of the identification process. Additionally, it suffers from problems described in Section 2.3.1.

2.3.1.2 Multi-Tone Excitation

The detection of degradation using digitized multi-sine perturbations injected at the control node of the converter is demonstrated in [27]. A multi-tone signal has a faster sweep time in comparison to successive single-tone excitation methods as several frequencies are injected into the system at once. Figure 2.2 shows the system architecture of the multi-tone excitation based approach, which can be used in the closed-loop condition. In this approach, a weighted recursive least-square algo-

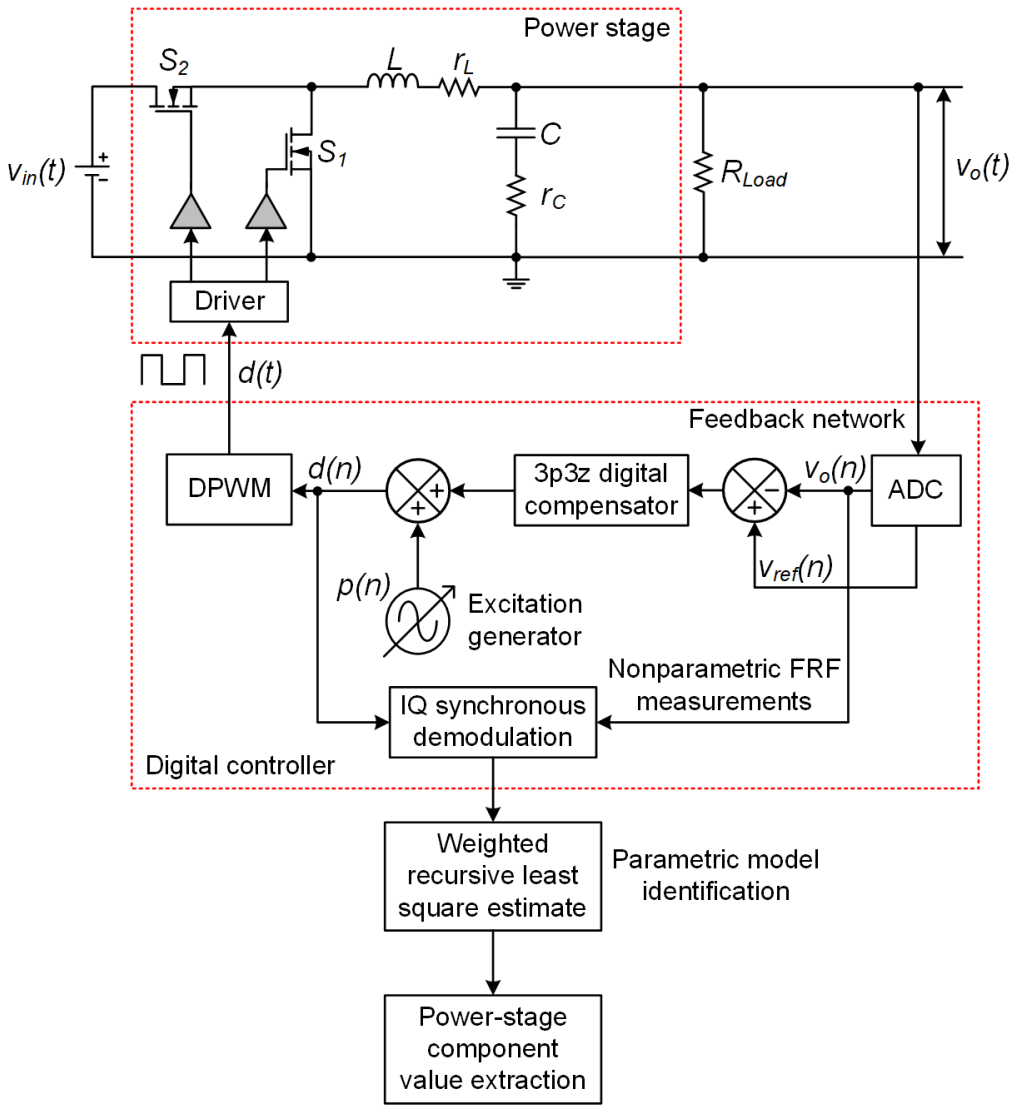


Figure 2.2: System characterization using multi-tone sinusoidal excitation [27].

rithm is used to minimize the relative error with respect to a parametric model and approximate the system model in frequency domain.

Usually, the amplitude response of the systems to be identified is not constant for the complete range of frequencies of the injected test signals. To maintain a constant signal-to-noise ratio (SNR) across the desired detection frequency range or to avoid saturation of internal nodes, degraded performance, and increased ripple at the output

of the converter, the amplitude of the test signal should be different at various frequencies. This requires some prior knowledge of the system to be identified, defeating the purpose of system identification. Multi-tone excitations also introduce multiple tones in the frequency response of the output, which is an undesirable attribute.

Additionally, averaging the output voltage to nullify the effect of noise and requirement of a high-speed, high resolution analog-to-digital converter (ADC) results in making this approach unsuitable for system identification of integrated DC-DC converters.

2.3.1.3 Limit Cycle Oscillation Based Excitation

Auto-tuning of a digitally controlled DC-DC power converter using LCOs is presented in [17]. The system is designed to intentionally introduce oscillations by reducing the digital pulse-width modulator (DPWM) resolution. When the identification/tuning mode is turned on, LCOs are introduced into the system, changing the digital code generated by the digital proportional-integral-derivative (PID) compensator. The steady state code just preceding the identification mode is captured by the steady state capture block as shown in Figure 2.3. The LCO is forced to be a symmetric signal by introducing an offset in the reference voltage to the converter. The change in duty cycle, as compared to the steady state duty cycle, is used for tuning the PID compensator. The approach uses a look-up table to update the programmable coefficients and the calibration works during closed-loop operation.

The approach provides a novel method of auto-tuning a digitally controlled DC-DC converter. The approach cannot be applied to analog controlled converters and requires high speed, high bandwidth ADC. Additionally, introducing LCO in a system is usually undesirable as it negatively affects both the voltage regulation and the frequency content of output voltage.

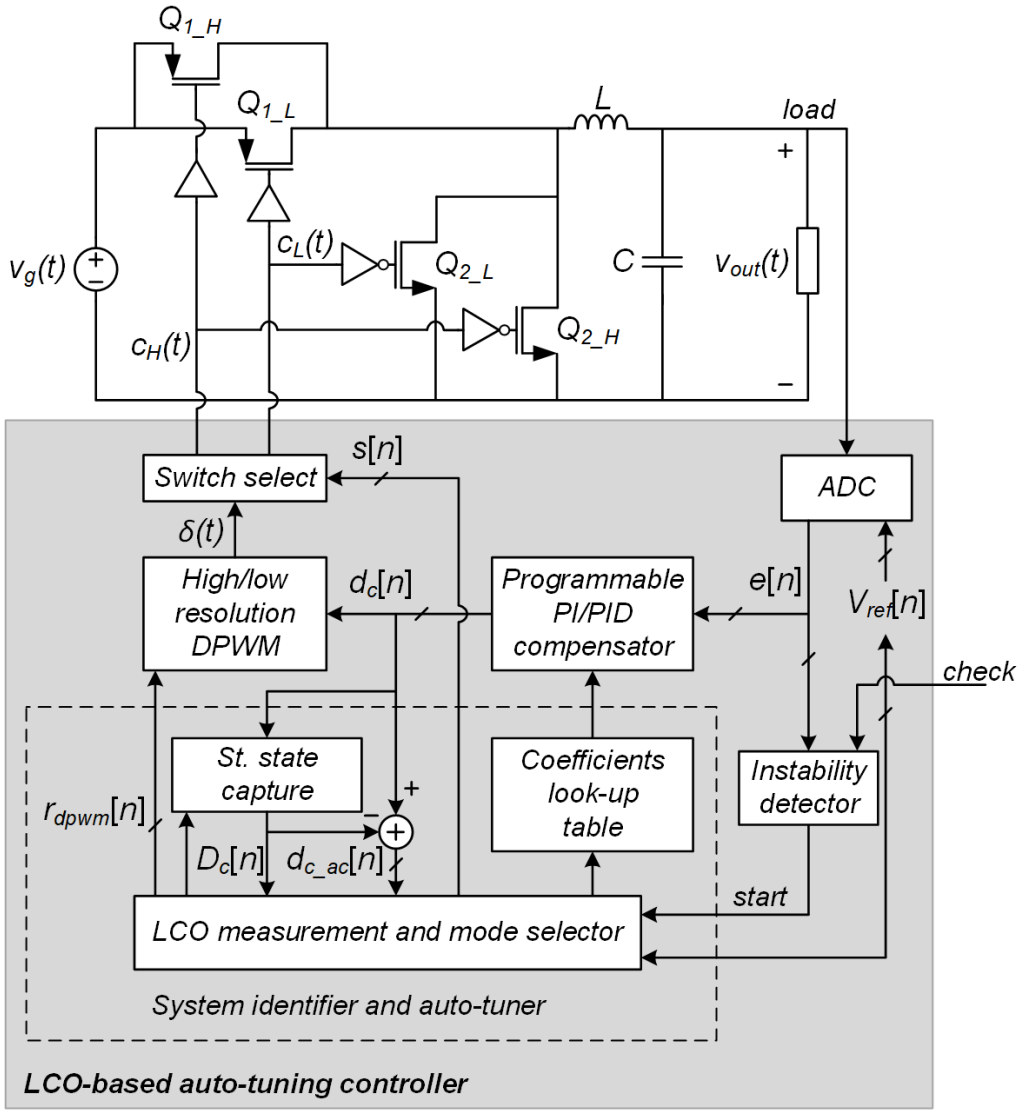


Figure 2.3: System characterization using limit cycle oscillation measurement [17].

2.3.2 Transient Signal Excitation Based Methods

Signals such as impulse and step can be used to excite and characterize an SUT. Important system parameters such as settling time, rise time, undershoot/overshoot, etc., can be calculated using these tests. The results obtained from the tests can also be converted from time-domain and analyzed in frequency-domain.

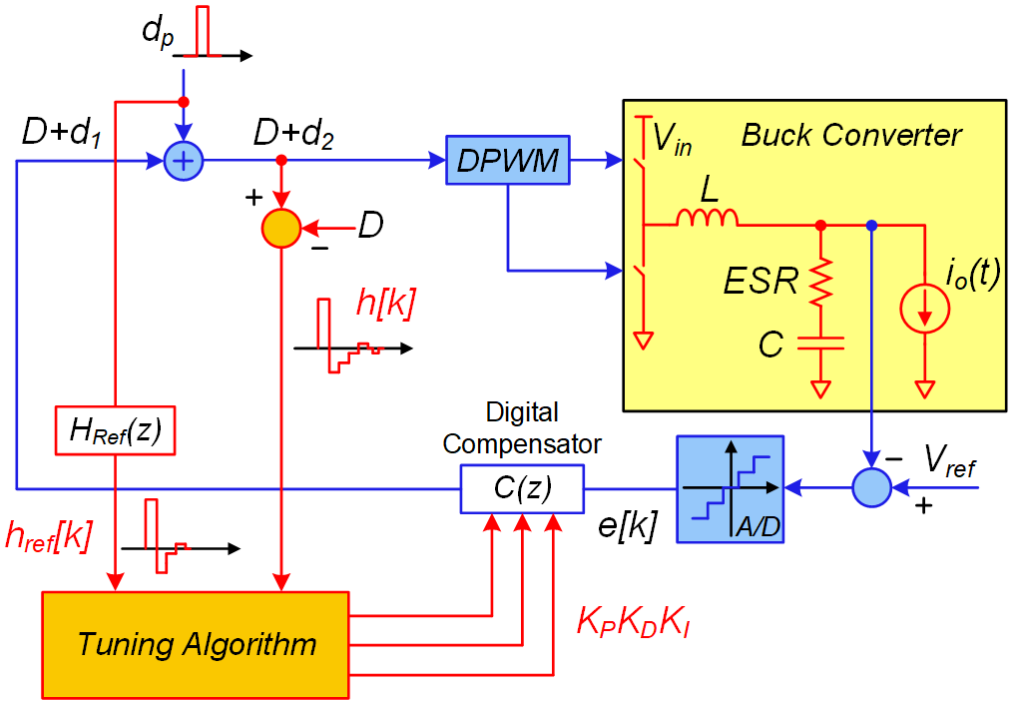


Figure 2.4: System characterization and tuning using impulse based excitation method [20].

2.3.2.1 Impulse Based Excitation

Use of impulse based excitation for system characterization is investigated in [20]. The technique is applied to a closed-loop digitally controlled system. The main goal of the proposed solution is to tune the digital controller coefficients to improve the transient response of the converter. The auto-tuning algorithm minimizes the difference in impulse response energy compared to a reference derived from the desired dynamic performance. The impulse is injected into the digital DC-DC converter system in the form of a narrow duty cycle pulse at the output of the PID controller as shown in Figure 2.4 . The response is observed and processed at the input of DPWM.

As an impulse by definition is a narrow signal (in time domain), the time required

to collect the relevant data to characterize and tune the system using this method is small. However, due to the requirement of obtaining an observable signal with high SNR, this technique produces non-negligible output voltage deviation. Additionally, digitally controlled systems are inherently limited by low transient response due to the delay in data conversion blocks in the feedback signal path and hence are not the most suited design choice for high speed DVS systems. Also, digital systems require high resolution, high bandwidth ADC to sample the output voltage and perform the cross-correlation in digital domain which results in high computational and storage requirements.

2.3.2.2 Step Based Excitation

In [15] and [16], a step based excitation is used to perform parametric system identification on the plant (FETs and filter stage) of a digitally controlled DC-DC converter in open-loop. The method identifies the control-to-output transfer function by injecting a step signal at the gate of the power FETs. The step input and the output of the converter is sampled using an ADC and the Steigliz and McBride algorithm proposed in [40] is used to fit the converter model in the digital equivalent of an analog 2 pole, 2 zero transfer function. Even though averaging is used to improve the SNR of the sampled data, it does not result in too high of an increase in computational workload due to the signal processing directly applied to the time-domain data.

The proposed technique can be applied to analog controlled DC-DC converters and can be modified to be used during closed-loop converter operation. The step applied at the gate should be much longer than the settling time of the system. However, it is not desirable to keep the power FETs in the system on for prolonged intervals. Additionally, the continuous change in output voltage level due to application of the

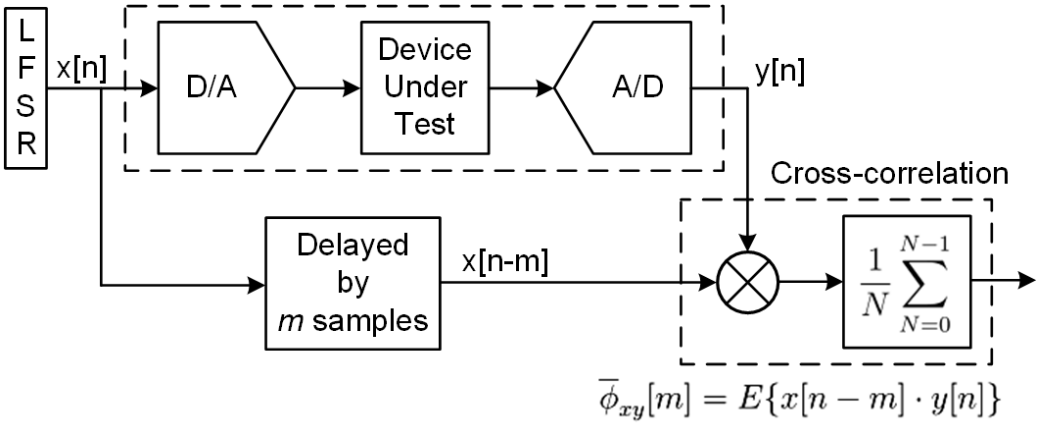


Figure 2.5: Mixed-signal implicit functional testing [41].

step test signal may result in reliability/degradation problems in the connected load.

2.3.3 Noise Based Excitation Techniques

In addition to sinusoidal signals and impulse/step based excitations, noise based signals also provide a way to perform identification on a system. Most commonly, white noise is used due to its several advantageous properties over other noise based signals. White noise is usually approximated using pseudo random binary sequence (PRBS). The mathematical aspects and justification of use of these signals is discussed in Chapter 3. The following section presents a summary of some relevant previous works which have used PRBS as an excitation signal for system identification.

2.3.3.1 Mixed-Signal BIST

A noise based BIST technique which can be applied to analog and mixed-signal systems is proposed in [41] based on the concepts presented in [42] and [43]. The technique is characterized as an *implicit* functional testing method, as it does not observe/measure the output response directly to determine the performance parameters are within the expected range, which is the case with *explicit* functional testing.

Instead, the performance of the system is estimated based on a signature set in a transformed performance space. When the calculated signature samples fall out of the boundaries of a predetermined constrained signature set, it can be inferred that the system has drifted from its optimal performance space.

Figure 2.5 shows the system architecture presented in [41] for mixed-signal implicit functional testing. Here, an analog test problem has been transformed into the digital domain. The method is primarily applied to low-pass (LP) and band-pass (BP) filters. The signature space is created using the amplitude of the cross-correlated samples of the impulse response.

This method ends up at a disadvantage as the transformation of an analog problem to digital domain results in the use of a digital-to-analog converter (DAC) and ADC pair which introduce additional hardware complexity. The performance of this technique will depend on the speed and resolution of the DAC and the ADC. Additionally, the calculation of cross-correlation in the digital domain will result in significant signal processing overhead.

2.3.3.2 PRBS Based Open-Loop Testing of DC-DC Converters

An open-loop, control-to-output system identification technique using pseudo-random input stimulus is proposed in [21] and further developed in [22]-[24]. Figure 2.6 shows the system architecture of this technique. The PRBS signal is used to modulate the control bits supplied to the DPWM which in turn modulates the duty-cycle pulse. The output of the converter is then sampled using an ADC and cross-correlated with the modulating PRBS to give the impulse response of the system. The frequency response of the system is obtained from the impulse response.

This technique uses a complex algorithm called Walsh-Hadamard, which is used to simplify more complex cross-correlation function calculations. The system archi-

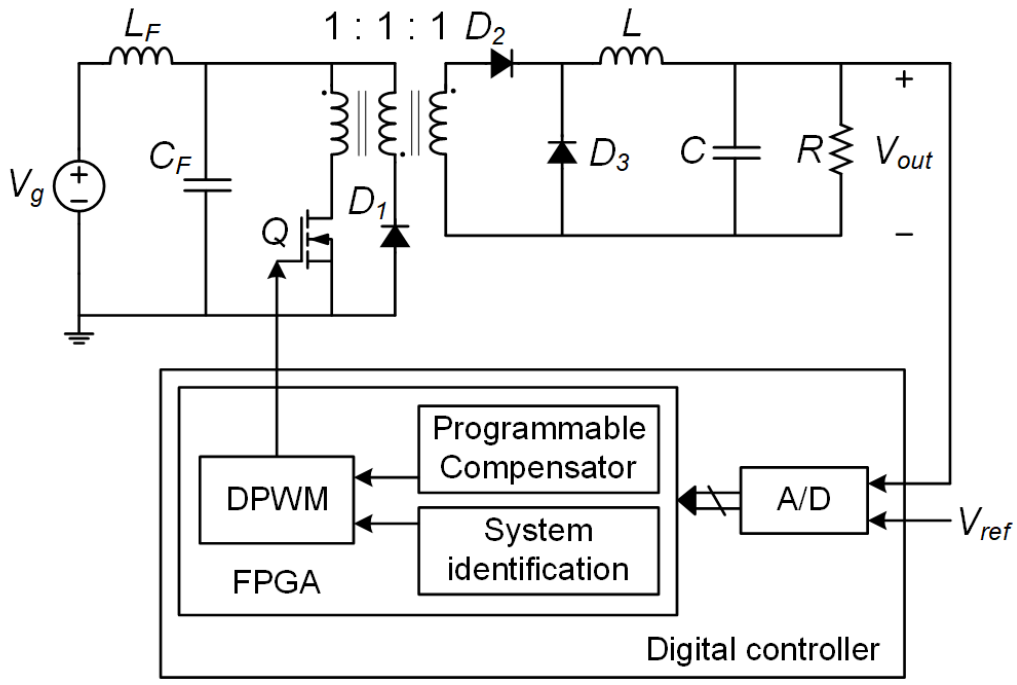


Figure 2.6: System characterization using PRBS method in open-loop [21].

tecture is designed primarily for application to digitally controlled converters. The cross-correlation calculation algorithm requires in the order of $O(N * 2^N)$ additions, which will impose a large hardware penalty if used in analog controlled systems. Here, N is the number of bits of PRBS. Additionally, a high speed, high resolution ADC will also be required to digitize the output voltage to calculate the cross-correlation in the digital domain. Also, due to its open loop mode requirement, this technique is not suitable for on-line characterization of DC-DC converters.

2.3.3.3 Closed-Loop BIST for Digital DC-DC Converters

This technique works on the same principles as discussed in Section 2.3.2.1. However, instead of using a duty cycle impulse at the output of the digital compensator, the modulation of the duty cycle is achieved using white noise approximated by PRBS as shown in Figure 2.7. The tuning of the digital compensator to optimize the loop

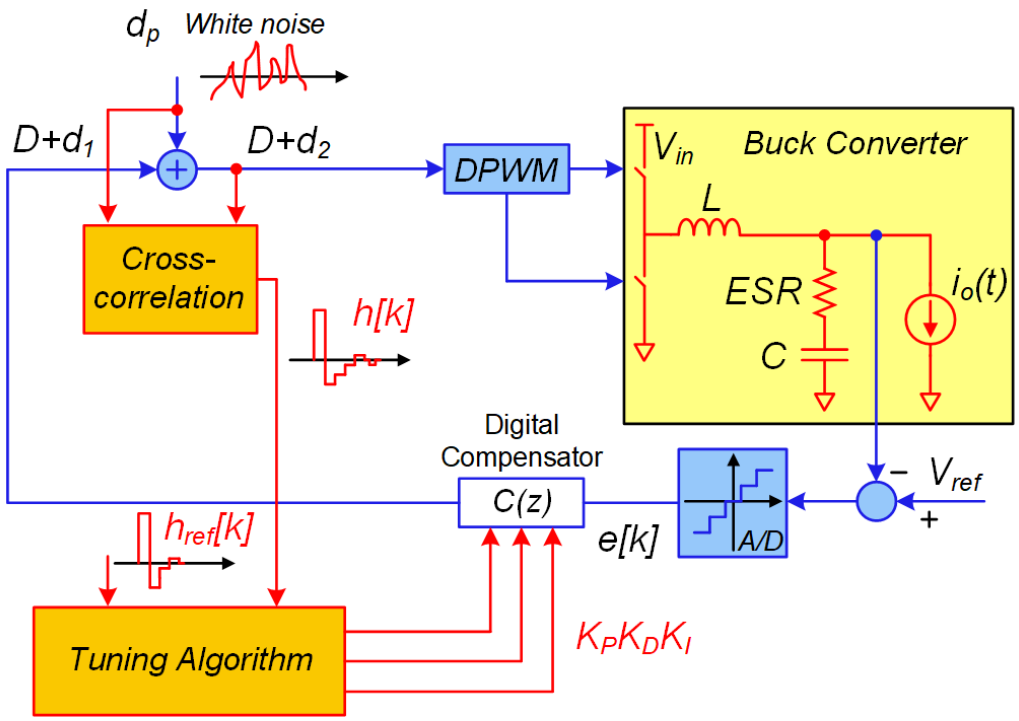


Figure 2.7: System characterization and tuning using PRBS based excitation method [20].

performance is done based on minimizing the difference in impulse response energy compared to a pre-calculated reference [20]. The technique operates in closed-loop but is designed primarily for digitally controlled systems, thus incurring usual complex hardware such as high speed, high resolution ADC, DPWM typical in digital DC-DC converters and high signal processing and memory overhead required for calculating cross-correlation in digital domain.

2.3.3.4 Multi-Level Multi-Period PRBS BIST

A multi-period maximum-length pseudo-random binary sequence (ML-PRBS) technique is used as the excitation signal in [39]. The transfer functions are identified from the measurement data using the circular cross-correlation method. The

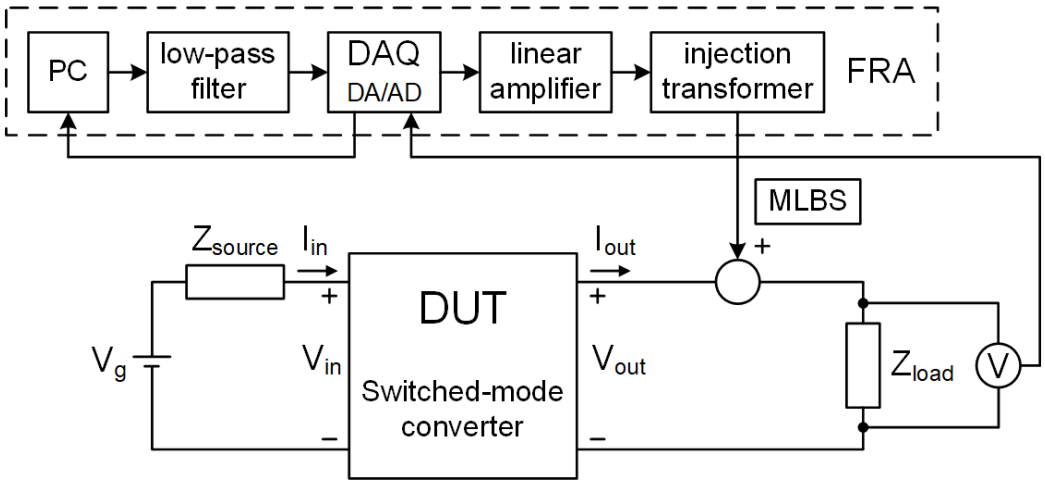


Figure 2.8: System characterization using circular PRBS and DAQ.

technique proves the effectiveness of using circular cross-correlation instead of linear cross-correlation as being more effective (less noisy). The technique also tries to address the effect of aliasing in the pulse-width modulation (PWM) converter due to PRBS injection in the system. However, to achieve reduced aliasing effects, this technique uses digital low pass filtered ML-PRBS, making it a multi-level analog excitation. Therefore, this technique requires a digital-to-analog converter (DAC) to generate the ML-PRBS and a transformer to couple the signal to the regulator output, making it unsuitable for fully integrated implementation due to the hardware complexity. Additionally, an increase in signal processing overhead is also incurred in this approach due to the use of multi-period ML-PRBS, which is used to reduce the effect of noise artifacts that occur in practical systems.

2.4 Proposed Integrated System Identification Approach

In view of the discussion on prior works in Section 2.3, no technique available in literature is suitable for integrated analog controlled DC-DC converters. Most of the techniques operate in open-loop during the identification phase, resulting in an

unregulated output voltage. As such, they cannot be used during in-field operation of the DVS systems. Additionally, most of the DVS systems are analog controlled due to their requirement of very fast transient response. These concerns and requirements are summarized here. Solutions to address them effectively in an integrated environment with reduced signal processing are proposed below and are further developed, implemented, and tested for their effectiveness in subsequent sections.

- In-field operational capability
  - A system identification technique is more useful if it not only has the capability to be used during the production and testing phase of product manufacturing, but also when the product is in-field and in use by the customer. Hence, it is of paramount importance that the diagnosis technique be able to operate without affecting the normal operation of the product. For a DC-DC converter this entitles that a regulated steady state voltage is always available to the load being supplied. Thus, the proposed solution operates during the closed-loop operation of the converter as against the open-loop testing techniques.
- Background operation
  - Even if the technique is capable of in-field operation, such that the DC-DC converter can be operated in closed-loop during the testing phase, the identification signals used should not affect the proper operation of the converter negatively. Additionally, the technique should not interfere with the proper operation of the load being supplied nor should it have EMI concerns. Hence, the test signal used should be such that the test signal energy is spread across the frequency spectrum and should not be

concentrated at one (or more) frequencies. Hence, PRBS is used as the test signal of choice as against using frequency-swept sinusoidal methods.

- Minimum effect on output noise and settling behavior of the system
  - In addition to minimizing the effect of system identification on the frequency spectrum, preserving the integrity of output voltage is also important. The technique should not introduce an unwanted ripple larger than that permitted during the identification phase. When impulse/step are used as test signals, they violate this requirement by introducing transient behavior at the converter output, which results in larger output voltage ripple, thus introducing stress on the connected load by supplying it with under/over voltage rather than a tightly regulated voltage. Hence, PRBS with a small amplitude is used as a test input signal in the proposed approach so that it only results in similar (or slightly larger) output deviation compared to its small steady state ripple.

- High accuracy system characterization and identification
  - Accuracy is another important characteristic required of a system identification process. The proposed approach uses PRBS to excite the system and cross-correlation to recover the information embedded in the output generated. The approach using which cross-correlation is calculated affects the accuracy of the overall results obtained. Either of linear cross-correlation or circular cross-correlation can be used. As shown in [39], circular cross-correlation provides more accurate results without relying on advanced post-processing techniques which require additional resources for signal processing. Hence, the proposed method in this dissertation uses

circular cross-correlation to extract the signal information.

- Suitability for IC level implementation
  - Due to the complexity of generating complex test signals on-chip, a simple stimulus which can be generated without complex implementation would be the most suitable for IC implementation. Thus, a single bit PRBS is used among other available options such as multi-bit or multi-level PRBS.

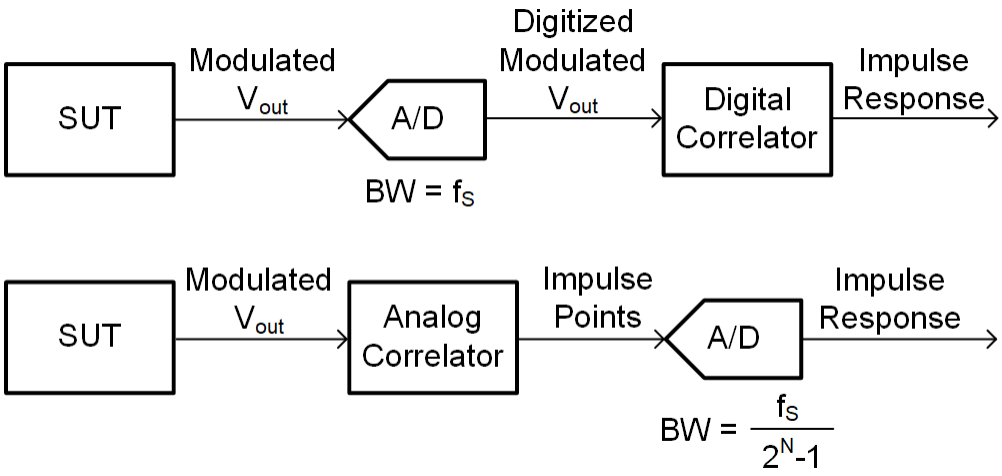


Figure 2.9: ADC bandwidth requirements for analog and digital correlation approach.

- Minimize associated hardware overhead
  - To reduce the complexity of processing the signals obtained from the system identification process, instead of first sampling the output voltage using a high-bandwidth, high-accuracy ADC and then cross-correlating, the signal will be cross-correlated first and then sampled. As shown in Figure 2.9, this approach relaxes the specifications of the required ADC. Here, f_S is the sampling frequency.

- To aid in relaxing the ADC specifications, for low storage and computational memory requirements, and suitability for an analog controlled DC-DC converter; the cross-correlation is performed using a proposed analog cross-correlator.
- Processing the correlation in the analog domain using an analog correlator instead of the digital domain, results in less ADCs than required in digitally controlled DC-DC converters.
- To reduce the post-processing required for curve fitting and calculation of FFT of the generated impulse samples, limited number of impulse response samples are used.
- Finally, the performance related parameters are identified such that only amplitude response monitoring is required to diagnose the degradation of the filter stage of the converter. This eliminates the signal processing required to calculate the phase response and further decreases the hardware overhead associated with post-processing.

As reasoned above, PRBS based techniques often satisfy the challenging requirements described in Section 2.1.1 [44], [45]. Hence, ML-PRBS is chosen as the signal of choice used for the implementation of system identification in this dissertation. Additional justification and clarification of choices made in the above discussion will be examined in more detail in subsequent sections.

CHAPTER 3

SYSTEM IDENTIFICATION AND MATHEMATICAL ANALYSIS

This chapter presents the mathematical analysis of impulse response calculation using white noise excitation of the SUT and the techniques which can be used to analyze the obtained impulse response. As mentioned in Section 2.3.3, PRBS is used to approximate white noise albeit band-limited and used as an excitation signal to perform system identification. Both parametric and non-parametric methods are discussed in the following sections.

3.1 Correlation

Correlation is the measure of similarity between two signals as a function of time lag between them. If both the signals are different, the correlation between them is called cross-correlation, while if both the signals are the same, it is called auto-correlation. The correlation operator is represented as $\odot$.

3.2 White Noise

White noise is a random signal which has equal intensity at all frequencies, thus having a constant power spectral density (PSD) throughout the frequency domain. White noise is non-deterministic and statistically uncorrelated in time. In discreet sense, white noise is a zero mean signal but has finite variance. In temporal domain, white noise is the differentiation of Brownian motion [46]. Mathematically, integral of white noise can be described by the Weiner process.

Having an equal PSD at all the frequencies implies that the power of such a signal is infinite. Hence, an infinite BW white noise signal is purely a theoretical concept. A white noise sample has a relation only with itself and does not statistically correlate

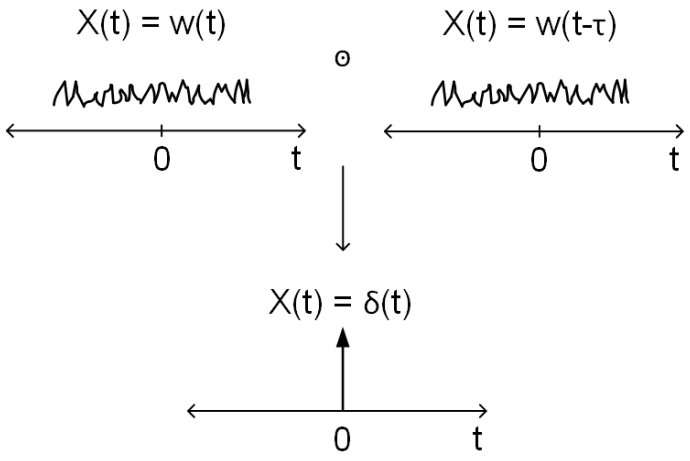


Figure 3.1: Relationship between Delta function and white noise.

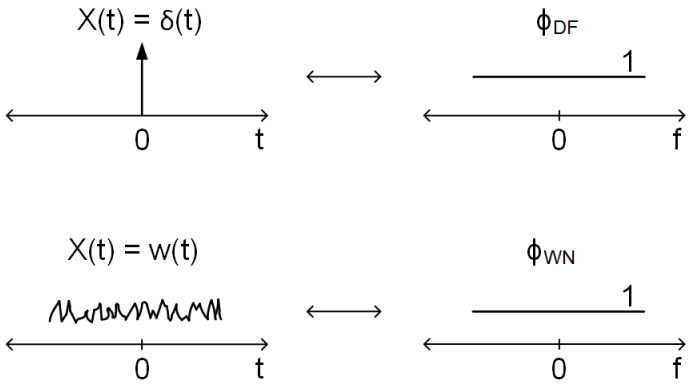


Figure 3.2: PSD of Delta function and white noise.

with other samples at any time. Thus, white noise is equal to itself only at that instant (at the moment of observation, say at $t = 0$). Hence, the correlation of white noise with itself is a Delta function at $t = 0$ (theoretically, infinite energy concentrated at a single instant of time), as shown in Figure 3.1. Since, the PSD of the Delta function consists of all the frequencies, similar to the PSD of white noise, both the Delta function and white noise are considered to be spectrally equal, as shown in Figure 3.2.

3.3 Impulse Response Calculation Using White Noise

A switching power converter can be approximated as a linear time-invariant discrete-time system for small-signal disturbances during the steady-state operation [2]. A linear time-invariant sampled system can be described by the following equation:

$$y[n] = \sum_{k=1}^{\infty} h[k]x[n-k] + v[n] \tag{3.1}$$

where $y[n]$ is the sampled output signal, $x[n]$ is the sampled input signal (PRBS injected at the reference or control node), $h[k]$ is the corresponding discrete-time system impulse response and $v[n]$ represents the unwanted disturbances in the system, such as switching noise, quantization noise, etc. The cross-correlation of $x[n]$ and $y[n]$ is given by:

$$R_{xy}[m] = \sum_{n=1}^{\infty} x[n]y[n+m] \tag{3.2}$$

$$= \sum_{n=1}^{\infty} x[n-m]y[n] \tag{3.3}$$

$$= \sum_{n=1}^{\infty} h[n]R_{xx}[m-n] + R_{xv}[m] \tag{3.4}$$

where $R_{xy}[m]$ is the cross-correlation of $x[n]$ and $y[n]$, $R_{xx}[m]$ is the auto-correlation of $x[n]$ and $R_{xv}[m]$ is the cross-correlation of $x[n]$ and $v[n]$ [11]. If $x[n]$ and $v[n]$ are independent, then $R_{xv}[m]$ is a constant [47]. Additionally, if $x[n]$, $v[n]$, or both are zero mean signals, then:

$$R_{xv}[m] = 0 \tag{3.5}$$

If $x[n]$ is white noise with variance σ^2, then:

$$R_{xx}[m] = \sigma^2 \delta[m] \tag{3.6}$$

and the cross-correlation gives the impulse response of the system,

$$R_{xy}[m] = \sigma^2 h[m] \tag{3.7}$$

where $\delta[m]$ is an ideal Delta function.

In practical systems, to satisfy the properties presented by equations 3.5 and 3.6, the most commonly used signal to approximate the white noise signal is a PRBS generated as a maximum-length sequence (MLS). The PRBS is periodic and deterministic, and the data length of the N-bit ML-PRBS is given by $M = 2^N - 1$. Auto-correlation of white noise is an ideal Delta function. However, for PRBS, an auto-correlation function is a mix of a Delta function at $m = 0$ and low amplitude components at $m \neq 0$ [39]. As seen in Figure 3.3, in case of normalized circular auto-correlation of PRBS, the amplitude of the Delta function at $m = 0$ is 1 and the amplitude of components at $m \neq 0$ is $-1/M$. In case the logic level 1 (HIGH) of PRBS has a voltage amplitude equal to $+e$ and the logic level 0 (LOW) has a voltage amplitude equal to $-e$, the amplitude of the Delta function at $m = 0$ is $+e^2$ and the amplitude of components at $m \neq 0$ are $-e^2/M$.

Similar to the components at $m \neq 0$ not being equal to zero, the cross-correlation of PRBS with system disturbances $v[n]$ is also not zero. Hence, the cross-correlation, R_{xy}, of the input PRBS with the output signal has undesired noise terms in addition to the system impulse response due to the non-ideality in R_{xx} and R_{xv}. The choice

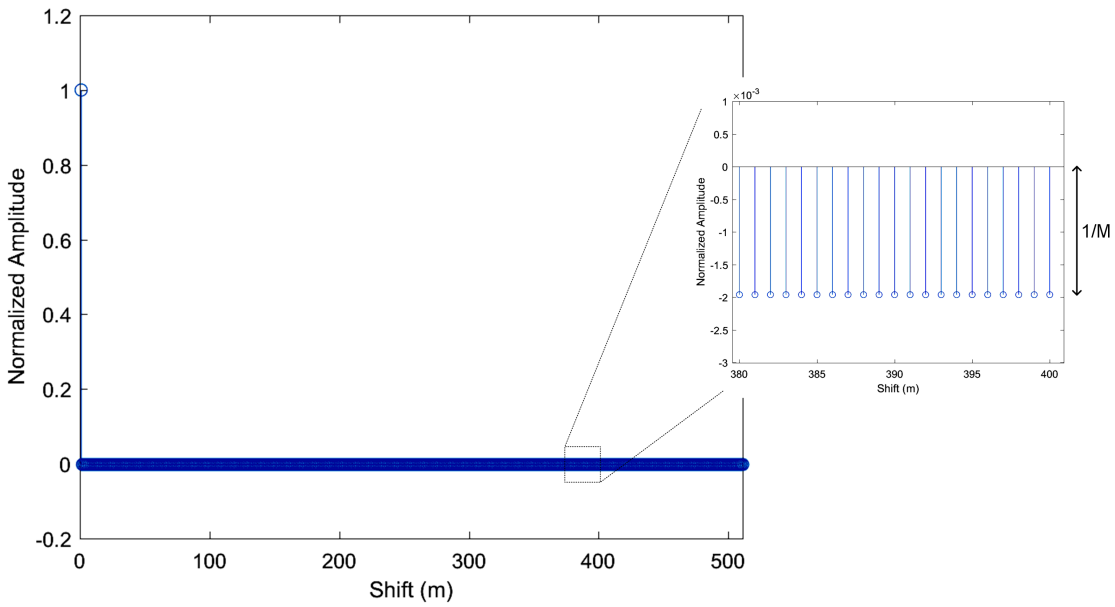


Figure 3.3: Normalized circular auto-correlation of 9-bit PRBS.

of the number of PRBS bits (N) and PRBS frequency (CLK_{PN}) affect these non-idealities and the accuracy of system identification. These considerations are further discussed in Section 3.6.

3.4 AC Small-Signal Model and Transfer Functions of Voltage Controlled Buck Converter

Figure 3.4 shows the small-signal model of the designed DC-DC buck converter. G_C is the transfer function of the loop controller, G_{PWM} is the PWM converter transfer function, G_{PS} is the duty cycle to output transfer function of the power stage, G_{XC} is the analog correlator transfer function, and H is the feedback gain factor. The signal $\hat{v}_{ref} = v_{ref} \pm e_{ref}$ is the reference voltage and $\hat{v}_c = v_c \pm e_c$ is the control voltage. e_{ref} and e_c are the amplitudes of the PRBS induced disturbances injected at the reference input node and the control voltage node, respectively. These disturbances are disabled during the normal mode of operation of the converter.

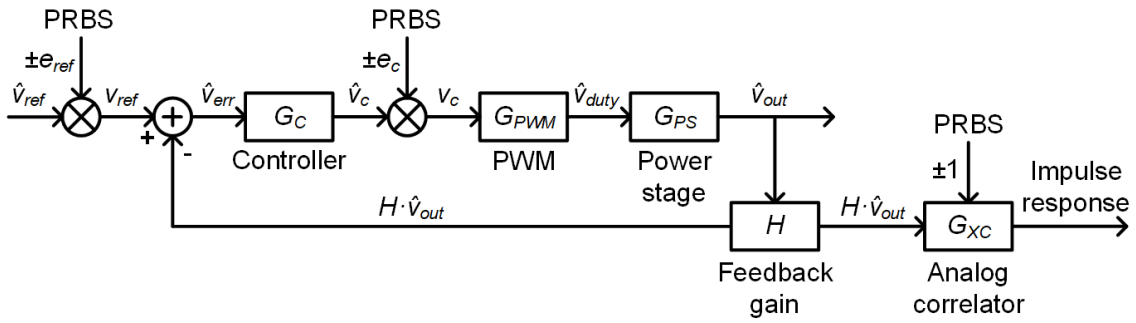


Figure 3.4: AC small-signal model of the proposed converter loop with online built-in self-test.

The loop gain in s-domain is given by [2],

$$L(s) = H \cdot G_C(s) \cdot G_{PWM}(s) \cdot G_{PS}(s) \tag{3.8}$$

To diagnose the changes in the system dynamics of the converter, the reference node and the control voltage node are chosen as the stimulus points and the output voltage node is chosen as the observation point for the respective loops. The closed-loop reference-to-output transfer function is given by:

$$T_{ro} = \frac{\hat{v}_{out}(s)}{\hat{v}_{ref}(s)}\Big|_{e_c=0} = \frac{1}{H}\frac{L(s)}{1+L(s)} \tag{3.9}$$

and the control node disturbance rejection transfer function is given by:

$$T_{eco} = \frac{\hat{v}_{out}(s)}{e_c(s)}\Big|_{e_{ref}=0} = \frac{G_{PWM}(s) \cdot G_{PS}(s)}{1+L(s)} \tag{3.10}$$

In the proposed system identification methodology, the loops under characterization are driven using a single-bit digital PRBS generator through corresponding nodes in the DC-DC converter (e.g., the reference input node and the control voltage node). The scaled down output of the loop filter (at the feedback node) is correlated

with the binary PRBS data using the circular cross-correlation technique. Cross-correlation of each MLS generates one corresponding point of the sampled impulse response. After calculating each impulse point, the MLS is circularly shifted and the process of cross-correlation of the complete sequence is repeated to calculate the next point of the sampled impulse response. The characterized loop responses are then analyzed to determine important system parameters. The parameters associated with the reference-to-output transfer function that can be tracked using this technique are the damping factor (ζ), PM, natural frequency (ω_n), CL-UGF, and quality factor (Q-factor). For the control node disturbance rejection transfer function the parameter that can be tracked is the peak gain frequency in bandpass shaped characteristics referred to as the center frequency (ω_c). The variation in these parameters can be observed over time for tracking the system characteristics and degradation, specifically due to the output filter derating and I_{load} change. The analysis of the generated impulse response can be performed in the time-domain or frequency domain, described as follows.

3.5 Impulse Response Analysis in Time-Domain

Although time-domain analysis of the dynamic loop characteristics of higher order systems (3^{rd} order or more) is a non-trivial problem, the theory for 1^{st} and 2^{nd} order systems is already developed [48]. In [14], the closed-loop DC-DC converter response is parametrically identified as a first-order system with time delay and unity gain. In the present work, the closed-loop system is parametrically equated to a second order system. If in a system, $||L(s)||$ approaches the unity gain with a -20 dB/decade slope, then the closed-loop reference-to-output transfer function can be approximated near the crossover frequency by the following function [2]:

$$\frac{L(s)}{1+L(s)} = \frac{\omega_n^2}{s^2 + \frac{\omega_n s}{Q} + \omega_n^2} \tag{3.11}$$

where Q is the quality factor given by,

$$Q = \frac{1}{2\zeta} \tag{3.12}$$

For a moderately damped system ($0.2 < \zeta < 1.2$), as is the case with most of the DC-DC converter loops, the time domain impulse response can be directly used to calculate ζ and in turn the open-loop PM. Furthermore, for smaller values of ζ, the resonant frequency, ω_r, is approximately equal to ω_n. For a constant ω_n, the change in Q-factor correlates with the changing stability conditions of the system. As ω_n is relatively constant with respect to the change in the load current I_{load} of the buck converter (for $R_{load} \gg \{DCR, ESR\}$), the change in the Q-factor can be used to diagnose the stability of the DC-DC converter for varying loading conditions. Here, R_{load} is the effective load resistance corresponding to the load current I_{load}, DCR is the DC resistance of the load inductance L, and ESR is the equivalent series resistance of the filter capacitor C_L.

Figure 3.5 shows the impulse response of a moderately damped second order system. The damping factor can be calculated from the impulse response as follows [49]:

$$R = \frac{h_I}{h_M} \tag{3.13}$$

where, h_M is the maximum height of the impulse and h_I is the height at the inflection point after point M.

The damping factor is given by:

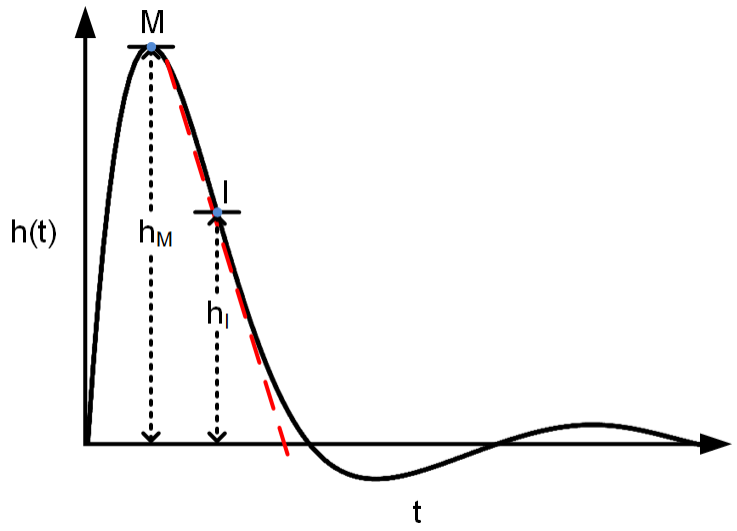


Figure 3.5: Impulse response of a moderately damped second order system.

$$\zeta = \frac{0.25}{1-R} + 0.50R - 0.32 \tag{3.14}$$

The phase margin can then be calculated using the following relation [2]:

$$PM = \tan^{-1}\sqrt{\frac{1+\sqrt{1+4Q^4}}{2Q^4}} \tag{3.15}$$

3.6 Impulse Response Analysis in Frequency-Domain

Frequency-domain analysis of the system-loop under test can be used to observe parameters such as ω_n and ω_c with respect to change in L and C_L. The frequency response can be calculated by taking the FFT of the discrete time impulse response generated using the cross-correlation method.

$$R_{xy}[m] \xrightarrow{FFT} H[j\omega] \tag{3.16}$$

As FFT is applied directly to the impulse points, the process is characterized as non-parametric system identification. Following the FFT, if the calculated frequency response is compared to a parametric model, the method will then be called parametric system identification. In either case, the calculated frequency response (non-parametric system identification) or frequency domain parameters corresponding to a parameterized model (parametric system identification) can be compared to a model response/parameters. The model response is calculated at nominal operating conditions, to diagnose any degradation or change in the response/parameters of the DC-DC converter with respect to aging or PVT variation.

3.7 Factors Affecting the Accuracy of System Identification Using PRBS Method

3.7.1 Resolution of the Generated Frequency Response

One of the factors affecting the accuracy of the frequency response obtained using the proposed system identification method is the selection of PRBS parameters such as M and CLK_{PN}. The frequency resolution (R_{FFT}) obtained using the PRBS method is given by:

$$R_{FFT} = \frac{CLK_{PN}}{M} \tag{3.17}$$

3.7.2 Accuracy of the Generated Frequency Response

For an accurate calculation of the impulse response the time-period of the PRBS should be much larger than the slowest time constant in the impulse response to be characterized [21]. This can be achieved by ensuring that the length M of the PRBS is sufficiently higher than the impulse response to be calculated, so that the complete impulse response is contained within the PRBS. In frequency domain, this

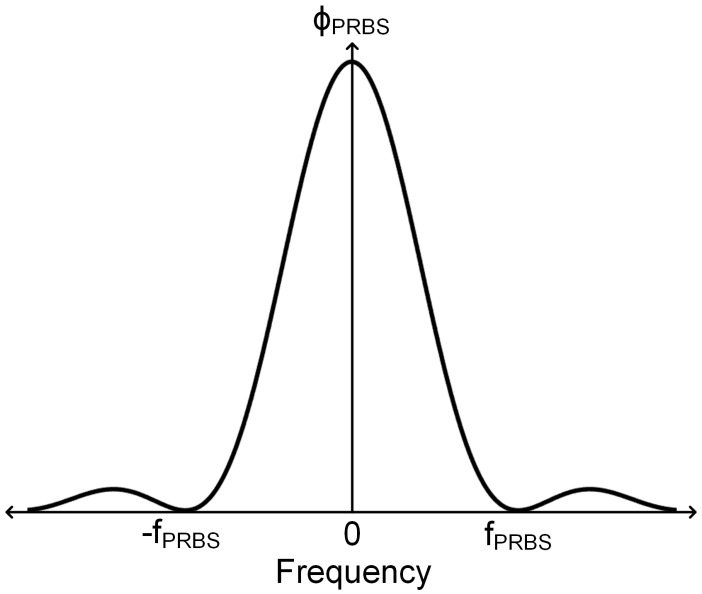


Figure 3.6: PSD of PRBS.

translates to the requirement of having a constant PSD throughout the frequency range of identification. PRBS approximates band limited white noise. The PSD of PRBS is given by:

$$\phi_{PRBS} = \frac{e^2(M+1)}{M^2} \frac{sin^2(\pi fT/M)}{(\pi fT/M)^2} \tag{3.18}$$

where, ϕ_{PRBS} is the PSD of PRBS, f is the frequency, and T is the total time period of the ML-PRBS.

In case PSD is not constant throughout the frequency range of identification as is the case with PSD of the PRBS as shown in Figure 3.6, the SNR will be different at different frequencies thus affecting the identification accuracy. Hence, a large enough N should be chosen such that the PSD is flat enough to obtain the required accuracy in the calculated results.

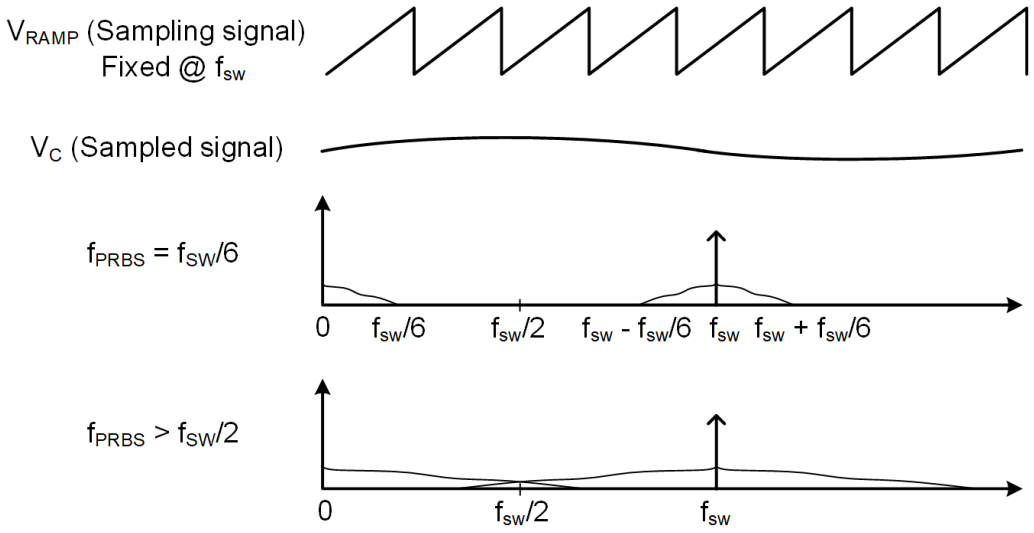


Figure 3.7: Aliasing in PWM converter.

3.7.3 Aliasing in PWM Due to PRBS

The PWM comparator acts as a sampling block in the feedback loop operating at a frequency f_{sw}, making the DC-DC converter a sampled-data system [50]. Thus, to prevent aliasing, CLK_{PN} should be higher than the frequency-band of interest, but low enough to avoid noise aliasing in the PWM converter [18], [39]. Figure 3.7 shows how choosing a PRBS frequency greater than the Nyquist frequency ($f_{sw}/2$) results in aliasing and thus causes degradation of the identification accuracy at the interfering frequencies. Although, in cases where identification of system response at greater than Nyquist frequency is required, techniques such as delayed output voltage sampling, windowing of measured cross-correlation, and correction for the non-ideal zero order hold (ZOH) and input PRBS spectrum can be used [25].

3.7.4 Linear vs Circular Correlation

For calculating the correlation between the signals, either linear or circular correlation can be used. During the calculation of correlation between finite length signals

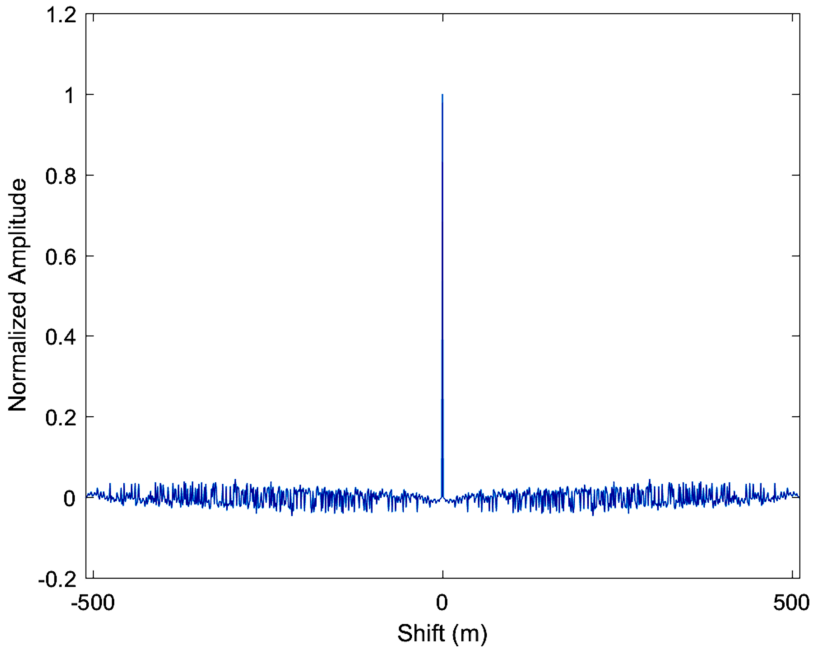


Figure 3.8: Normalized linear auto-correlation of 9-bit PRBS.

using the linear method, zeroes are padded at the beginning or the end (depending on the direction of the shift) of the signal after every shift operation to keep the signal lengths equal. Replacing the signal value with zero causes loss of information, resulting in additional noise in the calculated correlation [39]. This can be seen in Figure 3.8 for the auto-correlation of 9-bit PRBS sequence. The effect of this non-ideality can be reduced by using circular correlation where the effect of zero padded ends of the linear correlation procedure is reduced by circulating the two data sequences and multiplying the corresponding bits [39]. The improvement in the correlation function calculated using circular method can be seen in Figure 3.3.

3.7.5 Averaging vs Truncation of the Impulse Response

As discussed in Section 3.3, $R_{xv} \neq 0$ due to the PRBS not being completely uncorrelated with the noise in the system. To reduce the effect of this non-ideality, methods

such as averaging the sampled output multiple times, oversampling and performing running average, and using multi-period PRBS and averaging the sampled output are used. These methods result in an increase in post-processing requirements. In lieu of using these methods, impulse response truncation can be used to reduce the effect of measurement noise on the frequency response without the need for computationally extensive signal processing and large storage [51]-[53]. In fact, signal truncation results in even lesser storage and signal processing requirement than required to process one set of the sequence of the sampled signal. Further discussion on use of impulse response truncation can be found in Chapter 5.

CHAPTER 4

SYSTEM IDENTIFICATION OF VOLTAGE MODE DC-DC BUCK CONVERTER

System architecture and circuit implementation to provide an integrated solution for BIST of a voltage mode analog controlled DC-DC buck converter is presented in this chapter. Along with the circuit diagrams, operation of the circuits is discussed and related circuit waveforms are also provided.

4.1 System Architecture

Figure 4.1 shows the system architecture of the designed DC-DC buck converter with the proposed integrated system identification circuitry. The converter has two operating modes: the normal operating (regulation) mode and the system identification mode. When the converter is powered on, a resistor divider senses the output voltage (V_{OUT}) and generates the feedback voltage (V_{FB}). The reference voltage (V_{REF}), which is equal to $V_{REF,E}$ during the normal regulation mode, is compared with V_{FB} and a corresponding control voltage (V_C) is generated by the analog PID compensator. This V_C is compared with the saw-tooth waveform, of frequency f_{SW}, generated by the PWM converter and a corresponding duty cycle pulse signal (D) is generated. The duty cycle pulse is processed by the level-shifter and dead-time generator and then used to drive the power FETs to generate the switching-node voltage (V_{SW}). As both high-side and low-side FETs of the power train are NMOS for reduced die area and higher efficiency, a bootstrapping scheme is used to drive the high side power FET. The switching node voltage V_{SW} is filtered by the external LC filter to generate the regulated V_{OUT}.

The system identification mode can be turned on when the regulator is at its steady state. During this mode, the PRBS clock generator in the digital core divides the

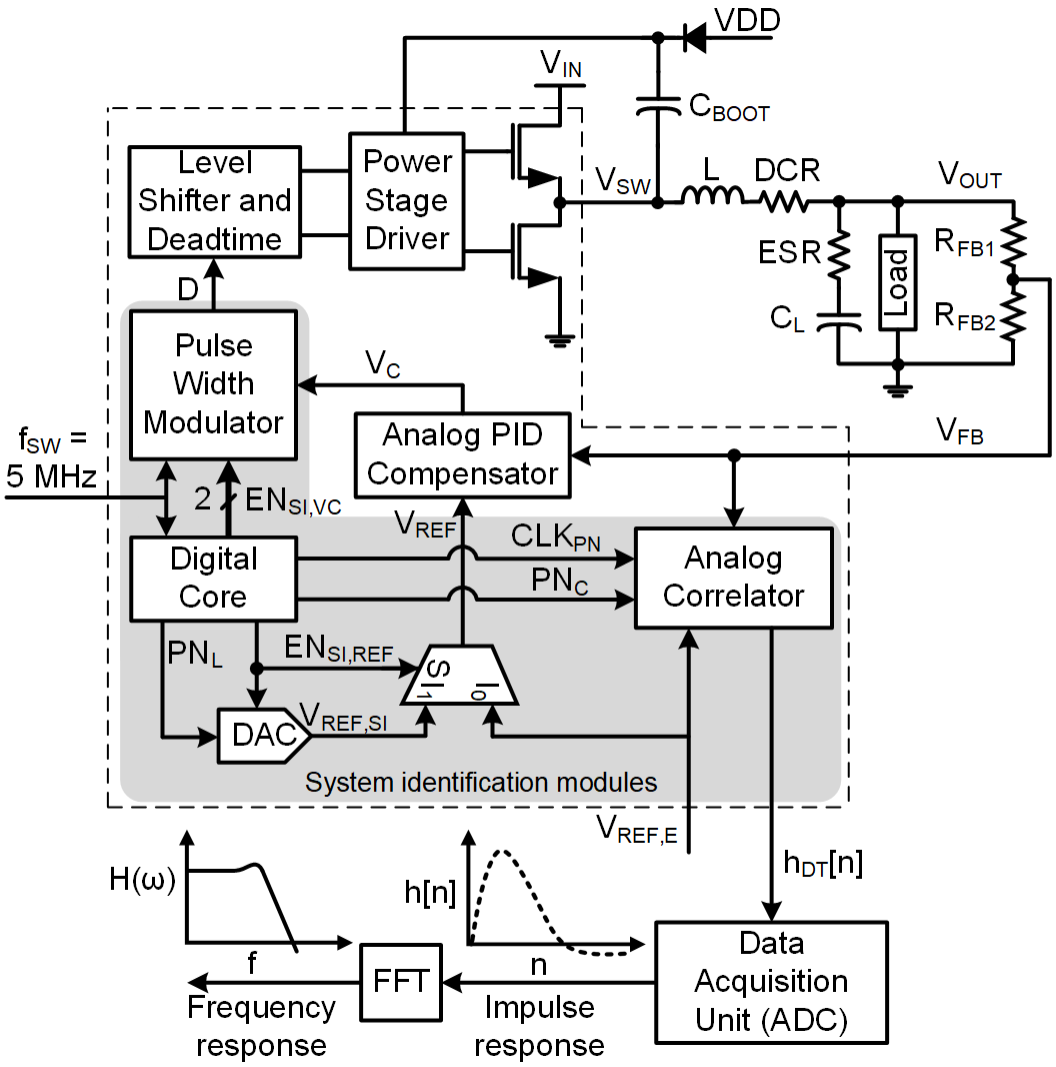


Figure 4.1: System level architecture of the proposed DC-DC buck converter IC with integrated system identification modules.

switching frequency f_{SW} by 6 to generate CLK_{PN} for the generation of linear (PN_L) and circular (PN_C) ML-PRBS. Frequency of CLK_{PN} is chosen to be $f_{SW}/6$ due to the aliasing concerns discussed in Section 3.7.5. The node selector block in the digital core is used to generate the enable signals to select the system-loop to be characterized i.e. either $EN_{SI,REF}$ to select V_{REF} node, for reference-to-output or $EN_{SI,VC}$ to select V_C node, for control node disturbance rejection loop characterization. Once the

PRBS starts to modulate the selected node, the feedback voltage V_{FB} of the converter is circularly cross-correlated with the excitation signal using the switched-capacitor analog integrator/correlator to generate discrete-time impulse response $h_{DT}[n]$ of the SUT. $h_{DT}[n]$ is sampled at the end of each accumulation cycle using an ADC to obtain the system impulse response $h[n]$. Impulse response $h[n]$ is then parametrically compared to a 2^{nd}-order moderately damped system response to estimate ζ and Q-factor. Finally, Q-factor is used to calculate the PM. Furthermore, FFT analysis is performed to estimate the frequency response H(ω) of the DC-DC converter and calculate CL-UGF, ω_n, and ω_c.

4.2 Circuit Implementation

4.2.1 Generation of Linear and Circular PRBS

The proposed approach uses circular cross-correlation to improve the accuracy of the calculated impulse and frequency response. Thus, the designed system uses both linear and circular PRBS. Linear PRBS is used to modulate the reference and control nodes while circular PRBS is used in the analog correlator to calculate circular cross-correlation. Linear PRBS is generated by using a linear feedback shift-register approach as shown in Figure 4.2(a). In the designed system, a 9-bit PRBS is used to generate a ML-PRBS of length M = 511. Thus, the output of the 9^{th} flip-flop is XORed with the output of the 4^{th} flip-flop to generate the MLS.

Delaying the complete PRBS after calculation of each sample point of impulse response or storing the sequence to achieve the effect of a circular shift will result in an inefficient and hardware intensive implementation. Hence, an efficient way to generate circularly shifted ML-PRBS is developed. Figure 4.2(b) shows the logic diagram of the proposed implementation. A 9-bit counter is used to gate the clock of

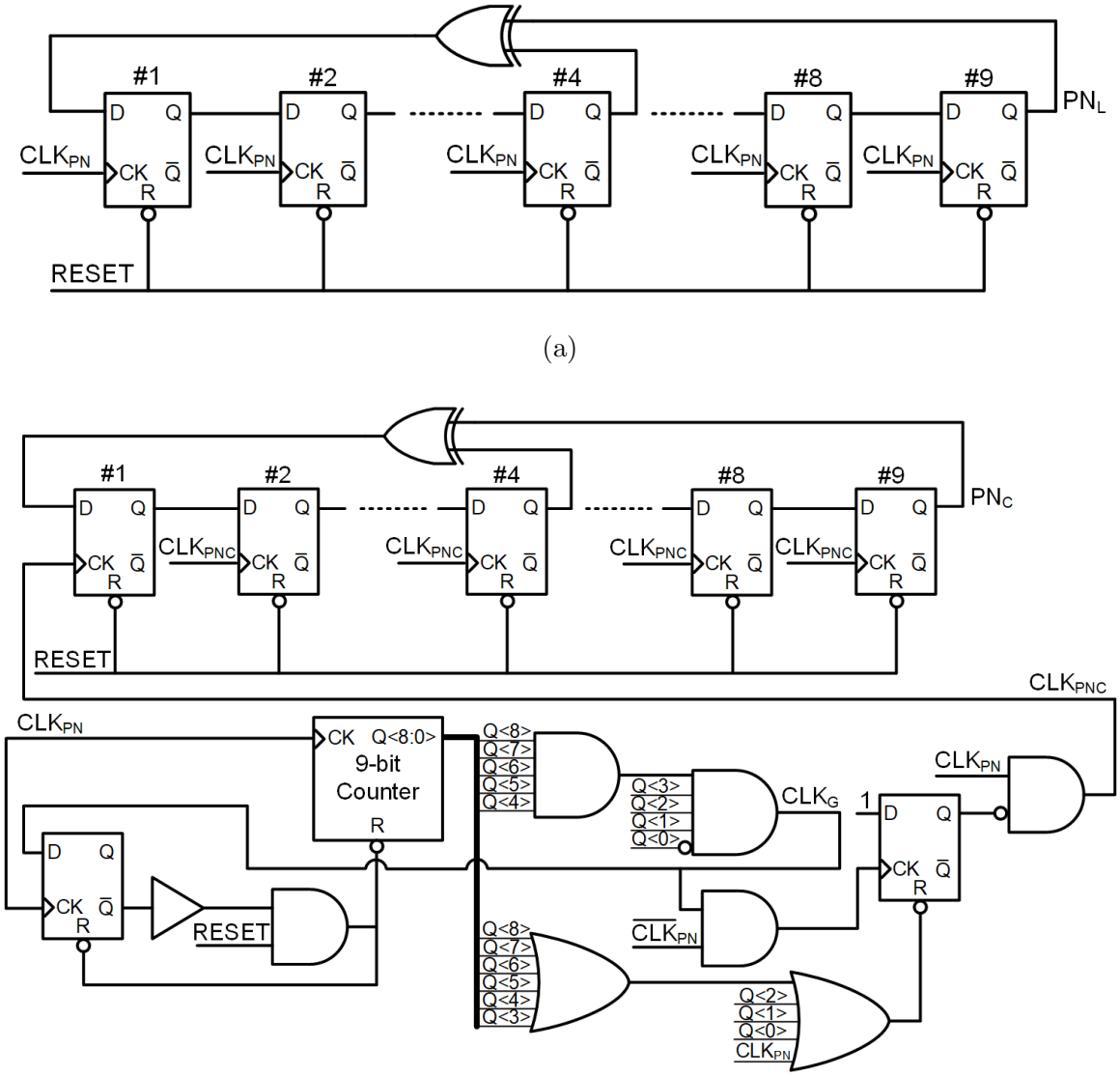


Figure 4.2: Linear and circular ML-PRBS generation. (a) Linear feedback shift register based generation of linear ML-PRBS. (b) Proposed logic scheme for generation of circular ML-PRBS.

the shift register at the end of generation of the ML-PRBS of length 511 for one clock cycle. This causes the last value of the shift register to be stored for an additional cycle, effectively causing a circular shift with respect to the linear PRBS generator.

The counter which is used to gate the clock signal is reset after the count reaches 510. Thus, at the next clock cycle it again starts to count starting from 0 and generates another shift with respect to the linear PRBS at the end of the count of 510. Thus, a circular shifted ML-PRBS can be generated with a very low hardware overhead and power penalty.

4.2.2 Reference Node Modulation

Figure 4.3(a) shows the unbuffered segmented resistive string DAC that is used to modulate the V_{REF} node to calculate the reference-to-output loop characteristics. It is a modified form of DAC presented in [54]. A string of resistors R_1, R, and R_2 provide the coarse resolution or the most significant bits (MSBs), while resistors R_3, R_4, and R_5 provide the fine resolution or the least significant bits (LSBs) of the DAC resolution. The proposed structure intentionally uses unequal resistors to center the $V_{REF,SI}$ node at 1.1 V and to achieve equal positive and negative modulation around this voltage.

Figure 4.3(b) shows the circuit waveforms during the identification mode. When PRBS is HIGH, switches S_1 and S_4 are on, while when PRBS is LOW, switches S_2 and S_3 are on. When S_1 and S_4 are turned on, the resistors in the LSB string appear in parallel to the resistor in the MSB string and loads it. This drops the voltage across the MSB resistor, increasing the voltage of $V_{REF,SI}$ by 11.8 mV. Similarly, when S_2 and S_3 are turned on, the voltage is decreased around $V_{REF,SI}$ by 11.8 mV. Thus, a modulation of 11.8 mV around 1.1 V reference voltage is achieved using this scheme.

4.2.3 Control Node Modulation

Control node modulation is achieved indirectly by modulating the slope of the ramp in the saw-tooth ramp generator. Figure 4.4(a) and (b) shows the circuit

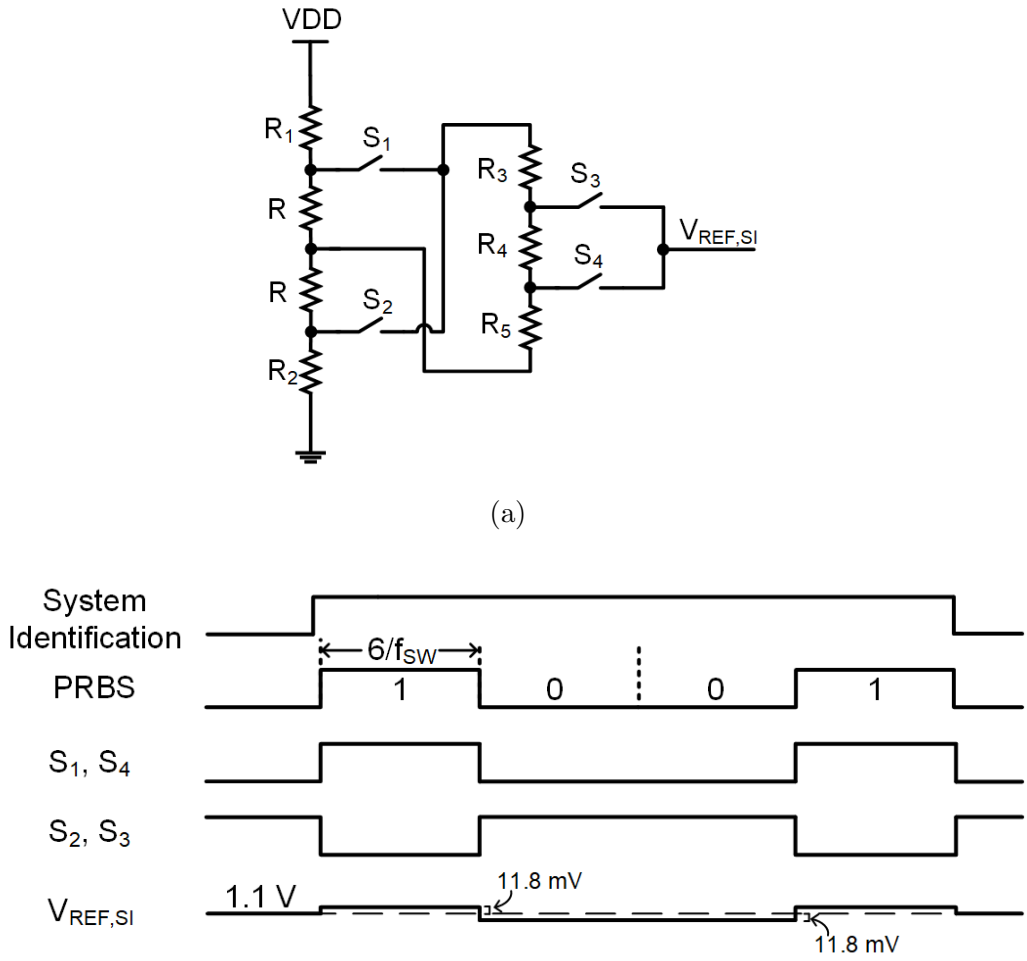
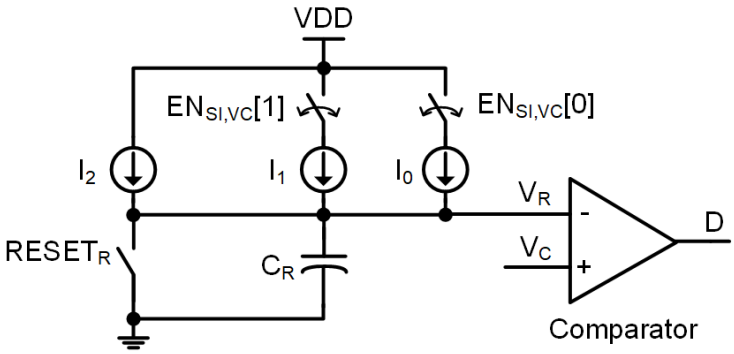


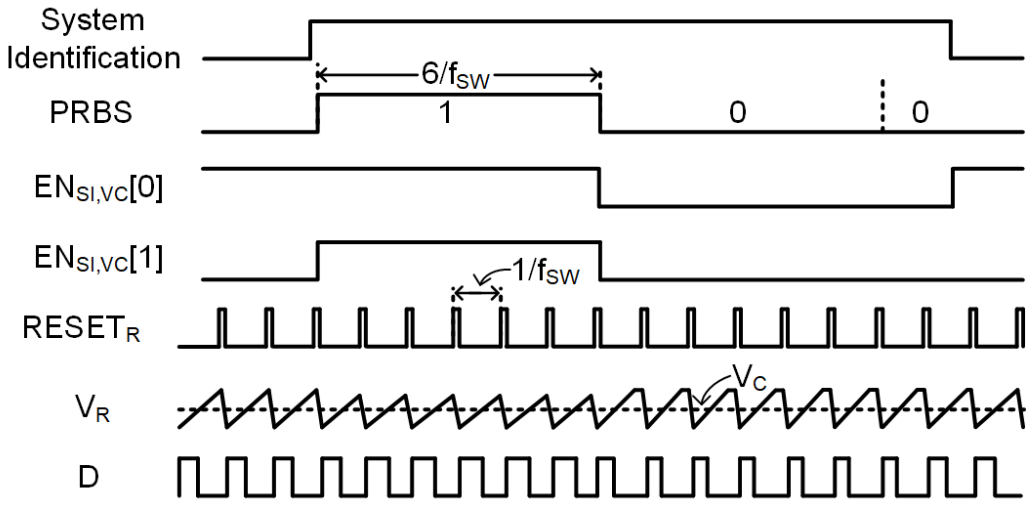
Figure 4.3: Unbuffered segmented resistive string DAC for reference node modulation. (a) Circuit implementation. (b) Modulation waveform around 1.1 V $V_{REF,SI}$.

implementation of the proposed saw-tooth ramp generator with the modulation circuitry and the circuit waveforms, respectively. The current sources and the switches are realized using pFETs. During normal operation, the switch controlled by signal $EN_{SI,VC}[0]$ is off while $EN_{SI,VC}[1]$ is on. Thus, two current sources I_1 and I_2 charge the ramp capacitor C_R. C_R is reset using switch $RESET_R$ after each switching clock

cycle to generate a saw-tooth of frequency f_{SW}.



(a)



(b)

Figure 4.4: Saw-tooth ramp generator with PRBS injector for control node pulse-width modulation. (a) Circuit implementation of the PWM converter. (b) Pulse-width modulation waveforms.

When system identification is turned on to characterize the loop T_{eco}, PRBS controls the charging/discharging of the ramp capacitor (C_R). When PRBS is HIGH, both the switches controlled by $EN_{SI,VC}[0]$ and $EN_{SI,VC}[1]$ are off, thus the current charging the capacitor is smaller than required to generate the nominal slope. This

causes the slope of the ramp to decrease and the comparison of V_C occurs with a slight delay, which corresponds to an increase in the duty cycle width, thus achieving the V_C node modulation. Similarly, when PRBS is LOW, both switches controlled by $EN_{SI,VC}[0]$ and $EN_{SI,VC}[1]$ are on, resulting in C_R being charged by a larger current and therefore, decreasing the effective width of the duty cycle. The ramp voltage when PRBS is LOW is limited to $V_G + |V_{thp}|$, where V_G is the gate bias voltage and V_{thp} is the threshold voltage of the pFET. I_0 and I_1 are sized relative to I_2 such that a modulation of 5% is generated.

It is important to note that this implementation of V_C node modulation does not take any extra power compared to the normal mode of operation. As, PRBS is a zero-mean signal, the average current consumed during the system identification mode is the same as the normal regulation mode when system identification is disabled.

4.2.4 Switched-Capacitor Analog Correlator*

To perform the circular cross-correlation in the analog domain, a switched capacitor integrator based correlator is proposed. In comparison to digital domain cross-correlation where complex algorithms (e.g., Walsh-Hadamard) are used, analog domain correlation offers significant savings in memory and processing requirements as correlation is performed in real-time. Additionally, it reduces the ADC bandwidth requirements. This is because as discussed in Section 2.4 and shown in Figure 2.9, instead of sampling the DC-DC converters output voltage at PN frequency CLK_{PN} before correlation, the ADC is used to sample the analog correlator output at frequency $CLK_{PN}/(2^N - 1)$.

Figures 4.5 and 4.6 show the flowchart and block diagram of the operation of

*This circuit was implemented by V. N. K. Malladi for this project. For more details, refer to [55].

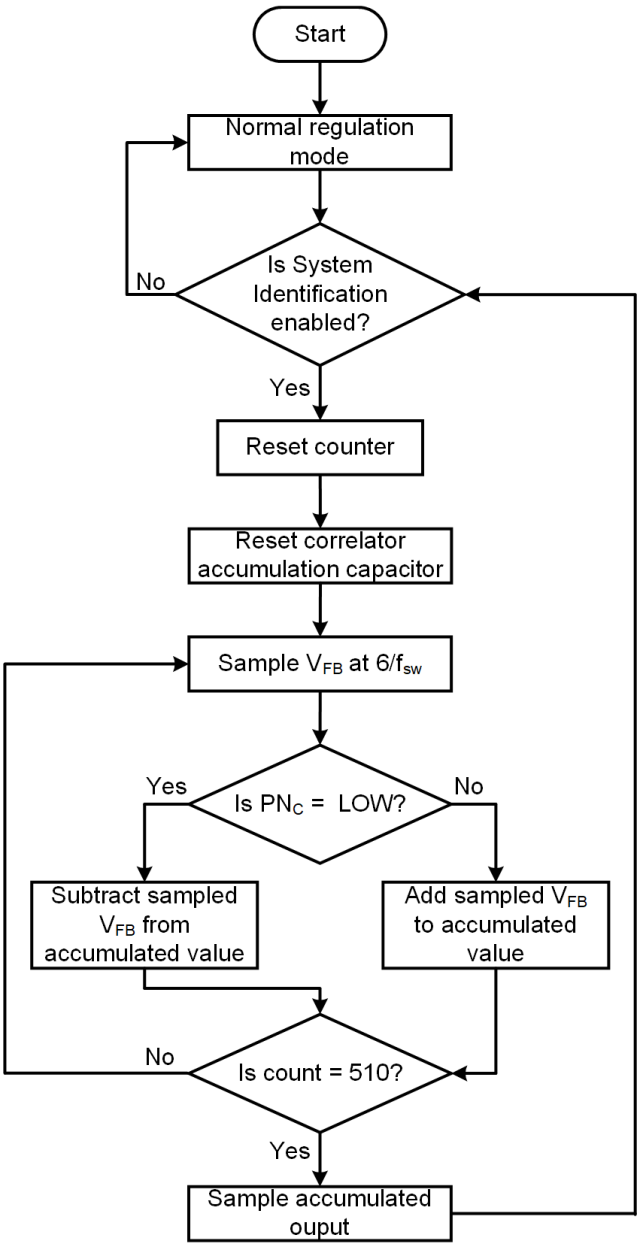


Figure 4.5: Flowchart of the operation of proposed switch capacitor based analog correlator.

the proposed switch capacitor based analog correlator, respectively. The correlator is a resettable integrator capable of performing both inverting and non-inverting integration. The decision to perform inverting or non-inverting integration during the

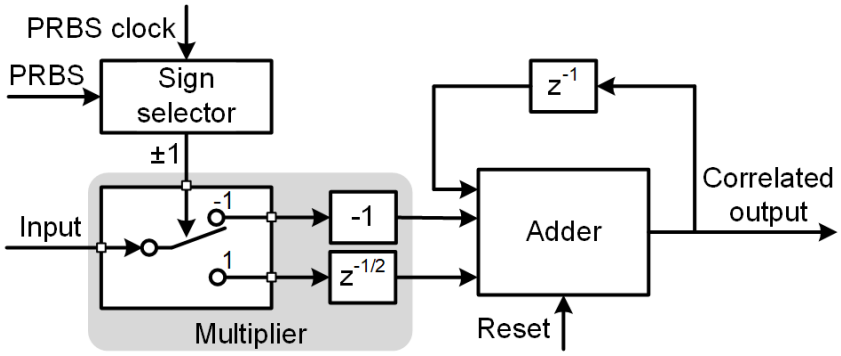


Figure 4.6: Block diagram of the operation of proposed switch capacitor based analog correlator.

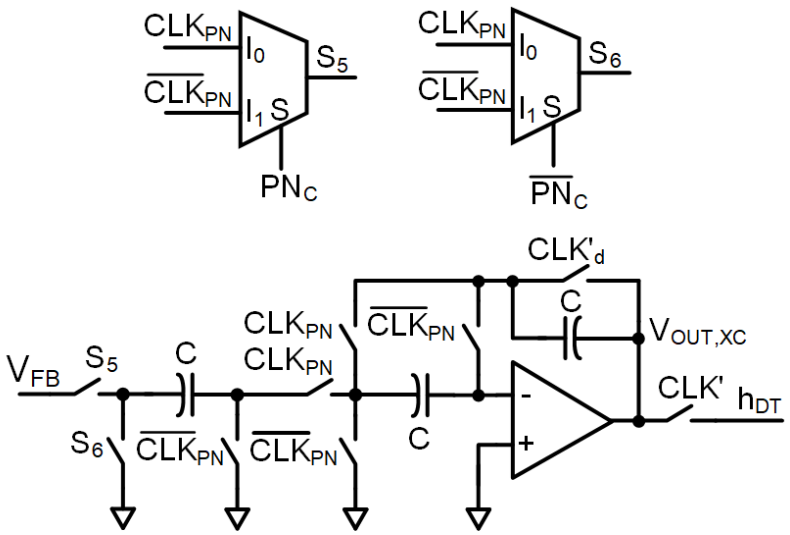
clock cycle is decided by the logic level of the PRBS. Figure 4.7(a) shows the circuit diagram of the designed analog correlator. PN_C is the circular version of the PRBS received by the correlator. The switched-capacitor correlator can be implemented by controlling the switches directly using PN_C, however, this increases the number of switches in the analog signal path, thereby increasing the noise in the output of the correlator. Instead, the overall number of switches are decreased by using PN_C and $\overline{PN_C}$ as select signals of the multiplexers, allowing them to control the switches.

When PN_C is logic low, the correlator acts as an inverting integrator (subtractor) while when PN_C is logic high, it acts as a non-inverting integrator (adder). Thus, the designed circuit implements signed multiplication and accumulation (MAC) operations required for correlation. The transfer function of the correlator during the inverting operation is given by,

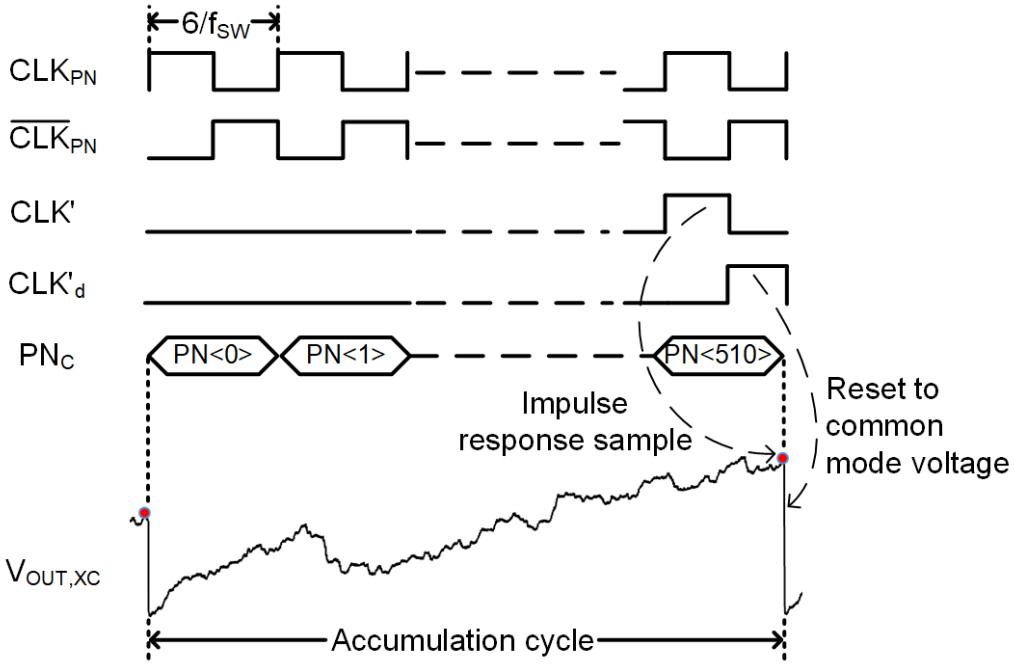
$$G_{XC,i}(z) = \frac{-1}{1 - z^{-1}} \tag{4.1}$$

and during the non-inverting operation is given by:

$$G_{XC,i}(z) = \frac{z^{-1/2}}{1 - z^{-1}} \tag{4.2}$$



(a)



(b)

Figure 4.7: Proposed switch capacitor based analog correlator. (a) Circuit implementation of the analog correlator. (b) Timing diagram and analog accumulation of impulse response sample.

Although the output in the case of $G_{C,i}(z)$ is available a half cycle before $G_{XC,ni}(z)$, the output in both cases is considered valid only at the end of each phase of PN_C for either of the logic levels, thereby making both the inverting and non-inverting transfer functions differ only in sign. The MAC operation finishes in the last phase of PN_C, PN<510>, during which the output of the correlator is sampled at the pulse CLK' and the integrator output is reset by the pulse CLK'_d. Each accumulation cycle results in one sample of the impulse response. Hence, after sampling and resetting, the integration process is again repeated with the circularly shifted PRBS to generate the next impulse response sample. Figure 4.7(b) shows the timing diagram and the generation of impulse samples using MAC operation at the correlator output.

To reduce the effect of non-idealities on the output of the correlator, bottom plate sampling is used. This reduces the effect of signal dependent charge injection. Additionally, to decrease the charge redistribution based charge injection during the transition of the switches between on and off states, half-size dummy switches are used in series with the actual switches. Although the offset of the operational amplifier does not affect the accuracy of the calculated impulse, it results in a DC shift at the output, thereby limiting the dynamic range of the integrated impulse response samples. To reduce this effect, correlated double sampling (CDS) is implemented in the designed correlator [56].

4.2.5 Level Shifted High-Side Driver

The designed DC-DC buck converter uses power NMOS for both high-side and low-side FETs of the power train. An inverted and level shifted duty cycle is therefore required to drive the high-side power switch. Due to the limitation of voltage levels available and lack of high voltage devices in the process, the high-side power FETs

cannot be driven directly using direct gate drive circuits. Thus, the drive of high-side FET is accomplished using a bootstrapping scheme [57], [58].

In the bootstrapping scheme, the driver of the high-side power FET is referred to the source of the FET, i.e. the switching node instead of GND. The power required to run the drive circuit is supplied by the bootstrap capacitor (C_{BOOT}) also referred to the switching node. The charge on C_{BOOT} is replenished by connecting it to the normal supply voltage (VDD) through a diode, as shown in Figure 4.1. This supply voltage is the same at which other circuit blocks are operating. The voltage at the supply of driver swings between the normal and level-shifted voltage together with the switching node. However, as the difference between the floating bias and the switching node is equal to VDD (minus the diode drop), high voltage devices are not required to implement the driver stage.

The Silicon-On-Insulator (SOI) process used for fabrication of the proposed IC has devices with a very strict safe operating voltage (SOV) range. Hence, a level shifter which provided reliable level shifting without violating the safe operating region (SOR) of the circuit components is designed to drive the high side power nFET using the bootstrapping scheme.

The signal propagation delay induced by the power stage driver at the rising and falling edge of the duty cycle causes high levels of voltage stress in the FET devices of the level-shifter during bootstrapping. The standard n-type and p-type FETs in the fabrication process used are rated for a maximum of 5.5 V. Laterally diffused MOS (LDMOS) are available in n-type with a higher voltage rating of $V_{DS} = 16$ V when $V_{GS} = 0$ V. All other voltage ratings of the LDMOS are the same as the standard FETs. Due to the unavailability of the p-type LDMOS, conventional cross-coupled level shifters in [59], [60] will encounter reliability concerns. The level shifter proposed in [61] is feasible for driving only very small capacitive loads. Hence, a high drive

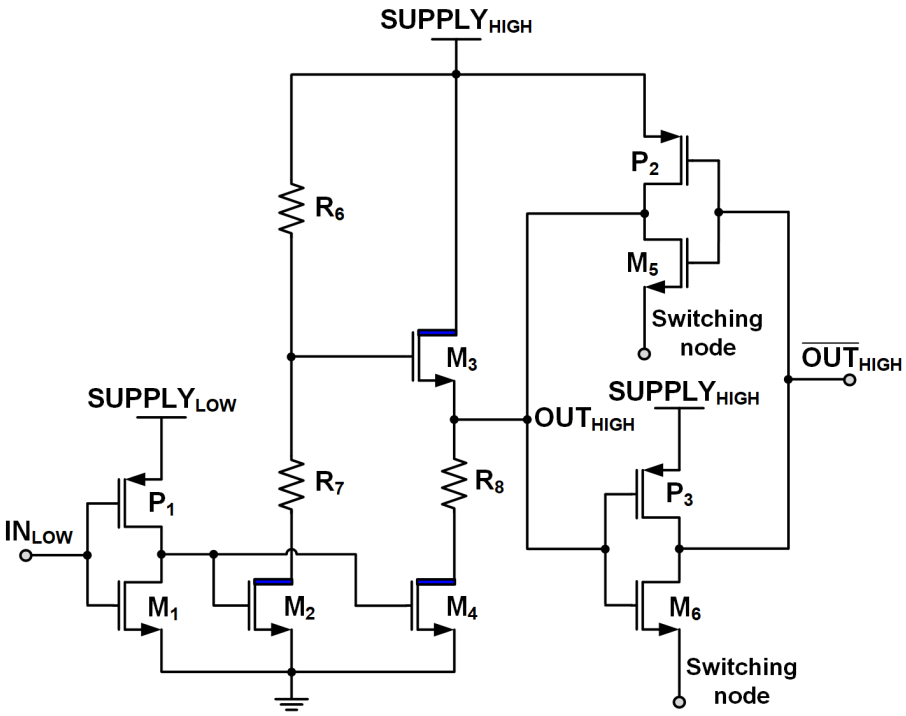


Figure 4.8: Proposed high reliability level shifter.

capability level shifter design using the available devices is proposed to alleviate these reliability concerns.

Figure 4.8 shows the proposed high reliability level shifter. IN_{LOW} receives the duty cycle D from the PWM converter. $SUPPLY_{HIGH}$ is the bootstrapping node and OUT_{HIGH} is the level shifter output. Except for M_2, M_3, and M_4, which are LDMOS devices, all other FET devices are standard FETs. When IN_{LOW} is logic high, M_2 and M_4 are turned off. The gate of the pass device, M_3, is charged through the resistor, R_6. When M_3 turns on, the voltage at OUT_{HIGH} becomes equal to $V_{SUPPLY,HIGH} - V_{TH,LDMOS}$ driving the first inverter (P_3 and M_6) of the power stage driver and producing the bootstrapping effect. Here, $V_{SUPPLY,HIGH}$ is the voltage at node $SUPPLY_{HIGH}$ and $V_{TH,LDMOS}$ is the threshold voltage of LDMOS M_3. The low strength keeper inverter (P_2 and M_5) then pulls the node voltage at OUT_{HIGH}

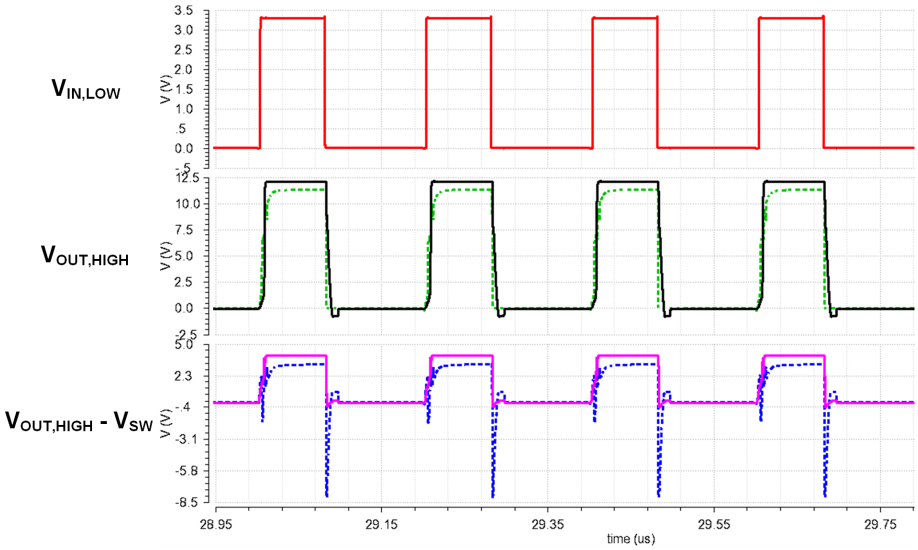


Figure 4.9: Comparison of simulated output waveforms of level shifters.

to $V_{SUPPLY,HIGH}$ thus increasing the drive strength. The keeper circuit also prevents the breakdown of the gate-oxide of M_6 due to a violation of SOV caused by the delay between OUT_{HIGH} turning logic high and the charging of the switching node to V_{IN}. The size of R_6 and M_3 also control the slew rate at OUT_{HIGH}. Resistance R_7, chosen such that the gate voltage of M_3 is smaller than $V_{TH,LDMOS}$ when M_2 is on, is used to decrease the leakage current through R_6. Resistance R_8 is used to avoid a direct path between the switching node and the ground node when M_4 is on, otherwise resulting in a short circuit when $V_{SW} = V_{IN}$. Figure 4.9 shows the simulated level-shifter output waveforms.

CHAPTER 5

VOLTAGE MODE BUCK CONVERTER MEASUREMENT RESULTS

To experimentally verify the proposed system identification techniques for detecting changes in the load current, output filter components, and overall DC-DC converter transfer functions, the converter is tested for various I_{LOAD}, L, and C_L values. Different I_{LOAD} values signify changing loading conditions while different L and C_L values signify the degradation in the filter components due to aging and PVT variation. To detect changes and degradation, the results calculated are compared to the similar results obtained for a nominal load and component values at nominal/ideal operating conditions using standardized testing methods. During testing, the closed-loop reference-to-output impulse function, control node disturbance rejection impulse function, and related frequency responses are generated. Then the parameters PM, CL-UGF, ω_n, Q-factor, and ω_c are calculated. The standard frequency-swept sinusoidal method is also used to calculate the same parameters and establish the accuracy of results calculated using the proposed identification method. To perform the sinusoidal sweep, multiple frequencies of single tone sinusoidal perturbation are applied at the reference node for reference-to-output transfer function generation and at the control node through capacitive coupling for control node disturbance rejection transfer function calculation.

The proposed converter is designed and fabricated with a 0.6 µm 6 layer-metal SOI technology with a die area of 9 mm^2. Figure 5.1 shows the die micrograph of the DC-DC buck converter with integrated system identification capabilities described in Section 4. Figure 5.2 and 5.3 demonstrates the test board and test setup used for testing the designed IC. The converter operates at $f_{SW} = 5$ MHz and supports an input voltage (V_{IN}) range of 5 V to 8.125 V and output voltage range of 3.3 V to 5

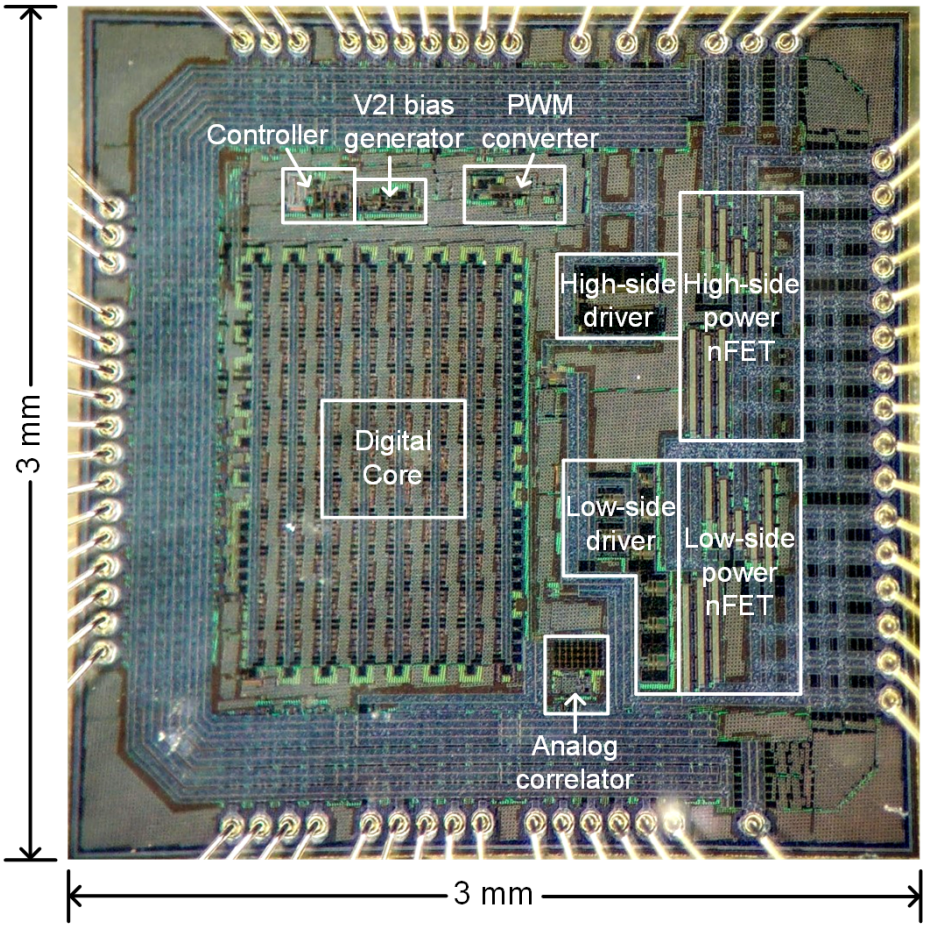


Figure 5.1: Die Micrograph.

V. Although the maximum load current supported by the converter is 450 mA, the nominal operating load current range at 3.3 V output is from 30 mA to 200 mA and at 5 V output is from 30 mA to 90 mA. A nominal V_{IN} = 6.5 V and V_{OUT} = 3.3 V has been used for testing purposes. The output filter inductor value used during the nominal operation of the converter is 10.3 µH. The inductor has a DCR of 60.8 mΩ. The nominal filter capacitor is 400 nF with an ESR of 50 mΩ. The PRBS noise frequency used is 833.33 kHz, providing an observable bandwidth (BW) of 416.65 kHz. The 9-bit MLS has a length of 511 codes which provides a frequency identification

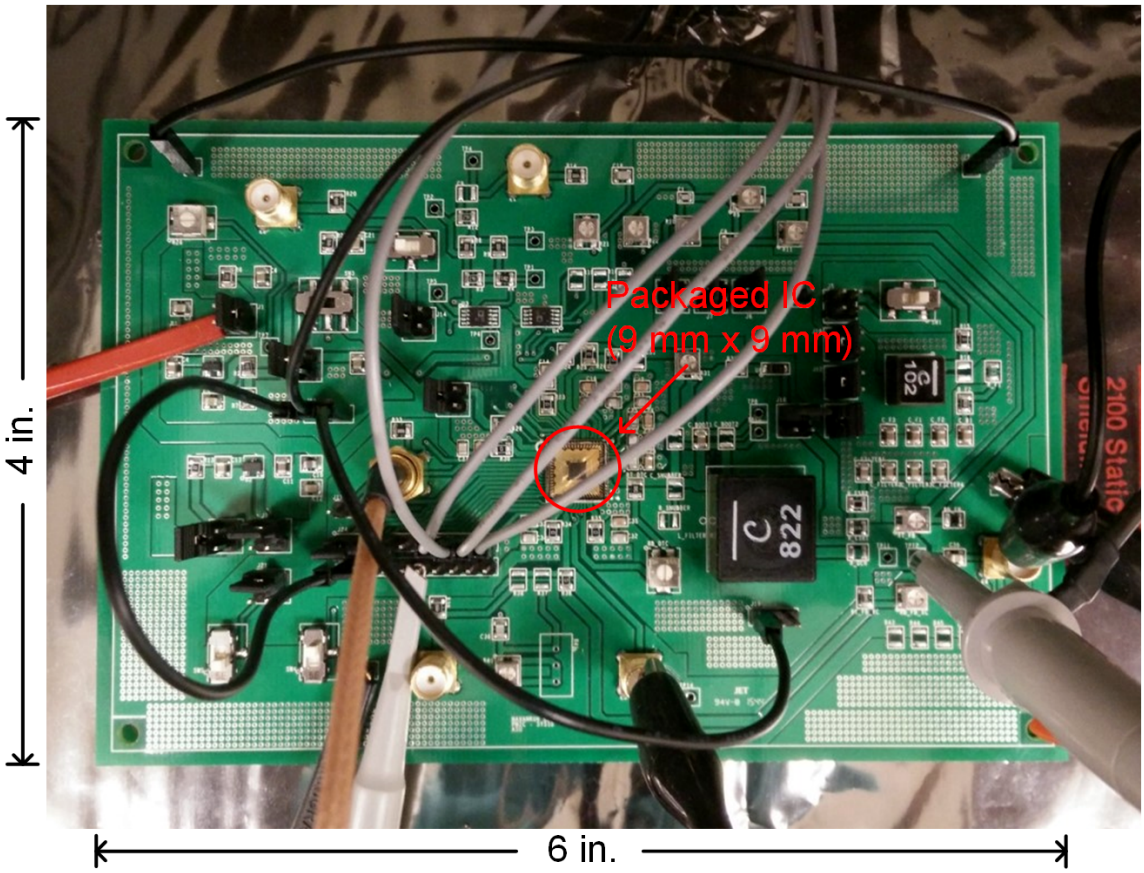


Figure 5.2: Test board used for testing the designed IC.

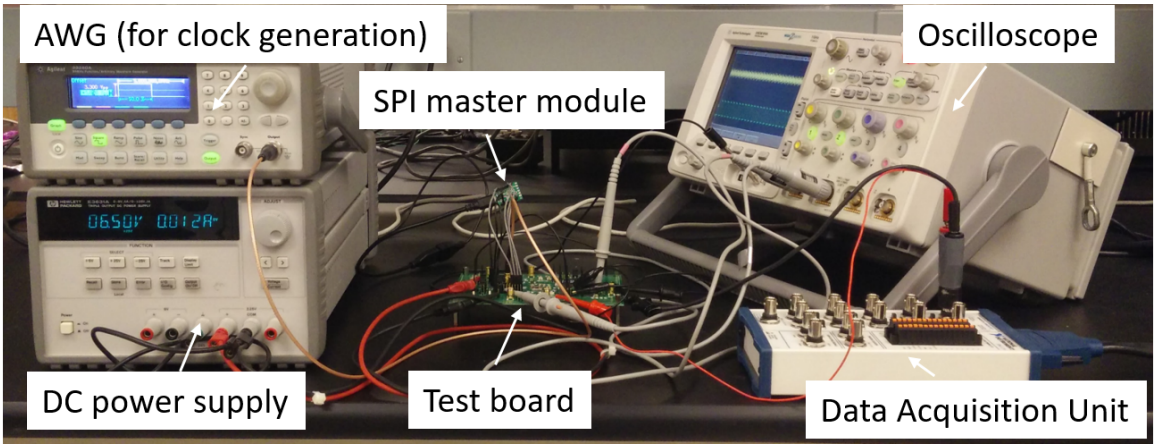
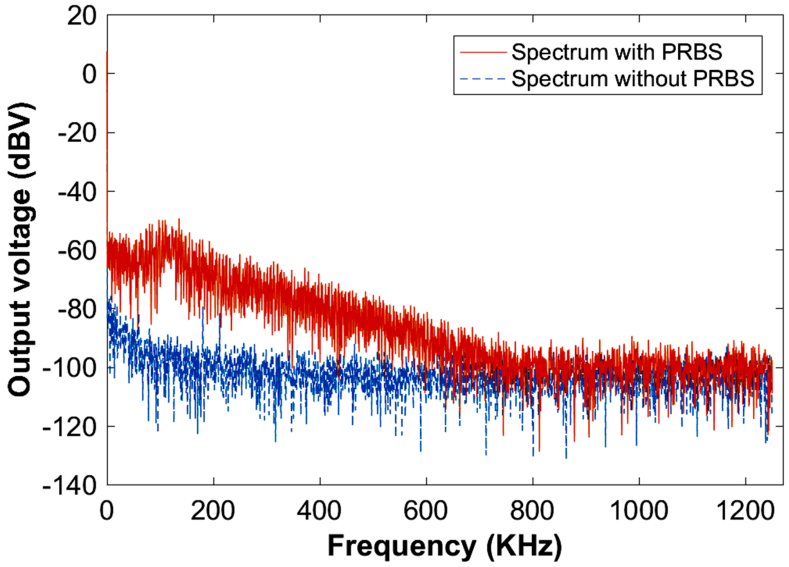
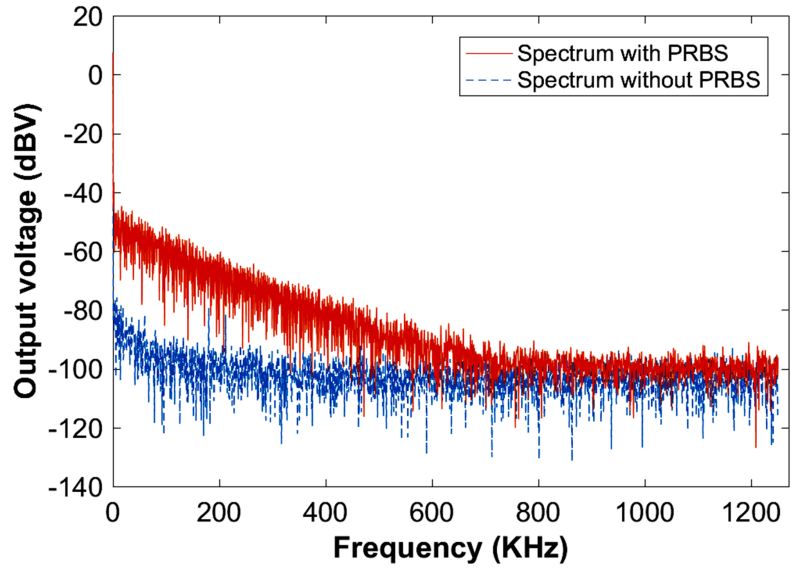


Figure 5.3: Test setup used for testing the designed IC.



(a)



(b)

Figure 5.4: Spectral density of V_{OUT} with and without PRBS noise injection. (a) Injection at the reference node. (b) Injection at the control node.

resolution of 1.63 kHz.

Figure 5.4 shows the spectral density plot of V_{OUT} of the designed buck converter

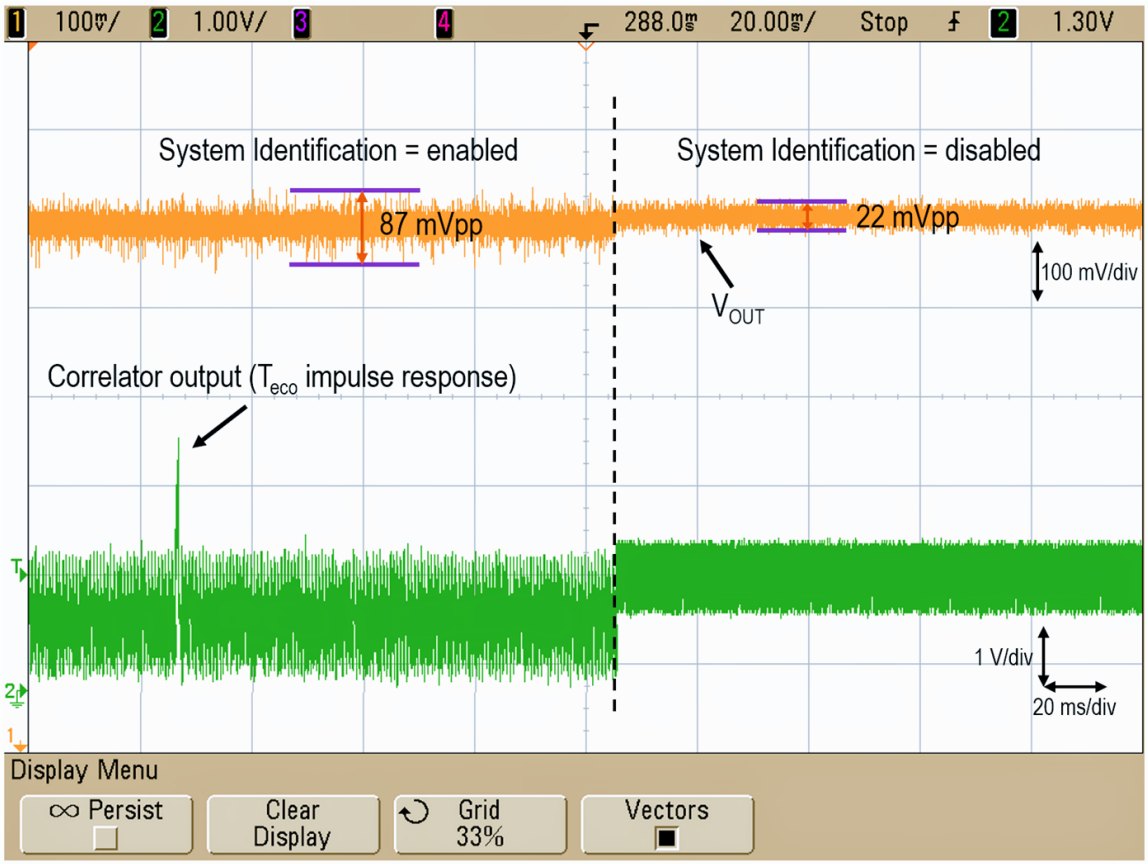
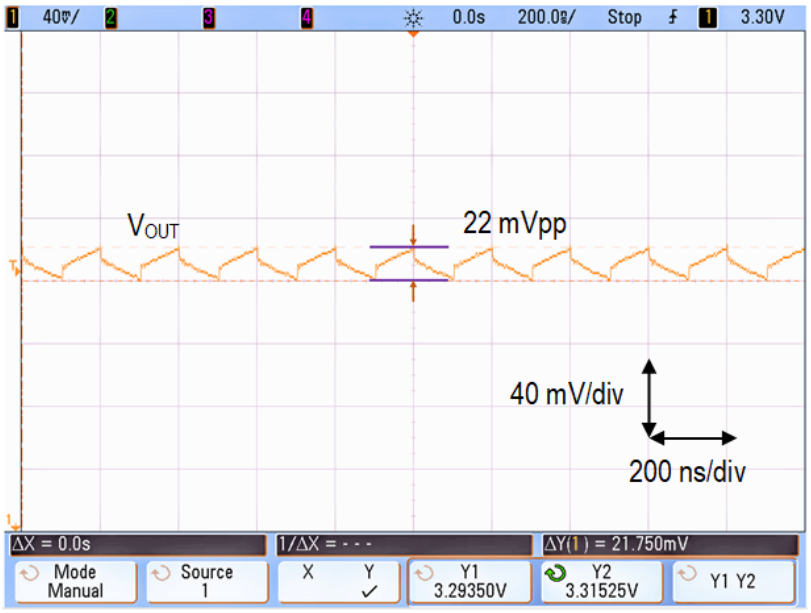


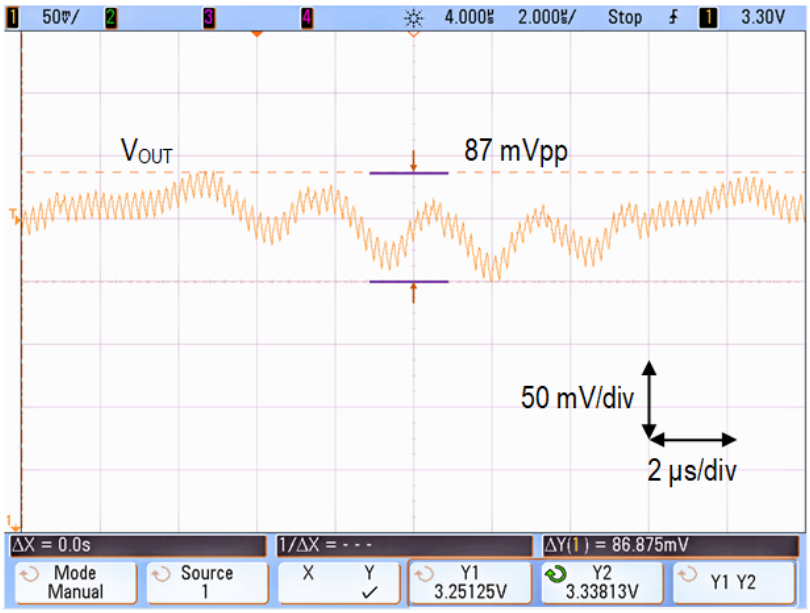
Figure 5.5: V_{OUT} and unsampled analog correlator output with and without PRBS injection at control node.

with and without PRBS noise injections at the reference and control nodes. Unlike frequency-swept sinusoidal or LCO based testing methods, PRBS is a spread spectrum signal, hence the test signal energy is spread across the spectrum without any tonal content concentrated at a single frequency. The comparison demonstrates that the PRBS signal energy almost completely dissipates above the PRBS frequency.

Figure 5.5 displays the V_{OUT} ripple performance and analog correlator output captured on an oscilloscope for PRBS disturbance injection at the control node. A $\pm 5\%$ change in the slope of the saw-tooth generator causes a V_{OUT} modulation ripple constrained to 87 mVpp during the identification process. The nominal V_{OUT} ripple,



(a)



(b)

Figure 5.6: Output voltage ripple. (a) During nominal operating conditions. (b) During control node modulation.

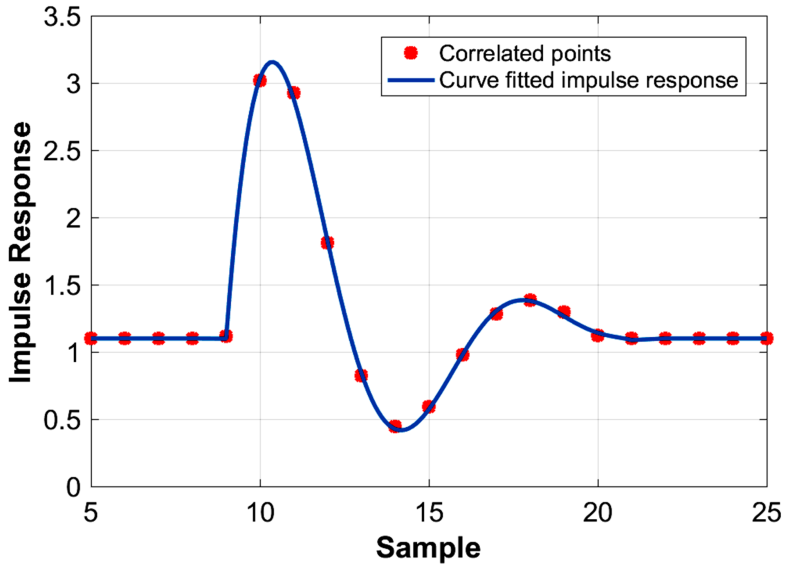


Figure 5.7: Sampled reference-to-output impulse response and curve fit.

when system identification is off, is 22 mVpp. Figure 5.6 shows the enlarged view of the V_{OUT} ripple during nominal and control node modulation operating conditions. During the modulation of the V_{REF} node, the V_{OUT} ripple generated is 71 mVpp.

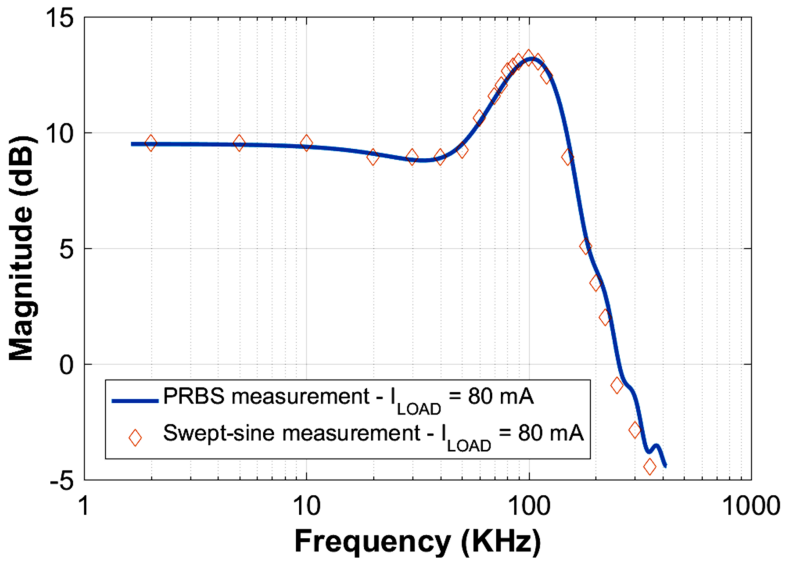
When system identification is on, the converter is required to be in a steady state condition at the same operating point. Many DVS systems have prolonged standby modes during which the load is constant. Also, in most high reliability applications, load conditions are relatively stable at steady state operation. Thus, system identification can be operated during these intervals. Additionally, the identification process is designed to operate in closed-loop, hence, in the event of a load transient during the identification process, the converter will supply the load without the loss of regulation. The impulse samples obtained during the event of a load transient can be discarded and the system identification process can be run again when the steady state is reached or the DVS system returns back to its sleep state. Next, for further processing, the impulse response generated by the analog correlator is sampled by a 10-bit ADC every 613.2 µs. The post-processing of the impulse response samples is

performed using MATLAB, although instead a DSP can also be used for complete embedded implementation.

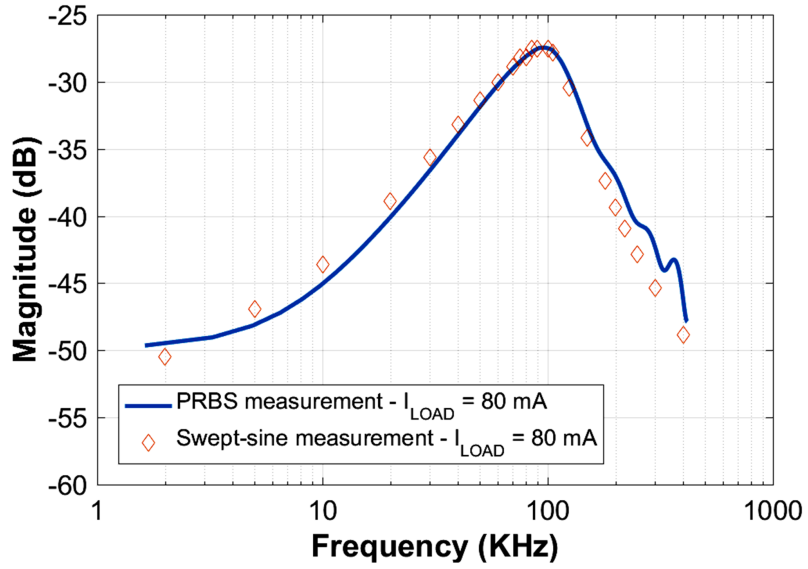
The sampled reference-to-output impulse response for nominal L and C_L values calculated for $I_{LOAD} = 80$ mA is shown in Figure 5.7. The correlator generates 511 samples for a full impulse response. However, for the designed system, significant impulse response information is contained within 20 samples starting at the peak of the response, which are sufficient for full characterization. Hence, impulse response truncation technique is applied and the rest of the samples are replaced with the DC voltage as they consist of noise around the DC level. This improves the noise and distortion immunity of the obtained results, thus reducing the computational resources required by averaging and for the calculation of FFT. The sampled response can be curve fitted to a 3rd order Fourier function so that the time domain analysis method explained in Section III can be used to directly calculate the relevant parameters. Additionally, FFT of the truncated impulse response samples collected directly from the analog correlator can be calculated for obtaining the frequency response of the characterized system loop for further analysis.

Figure 5.8(a) shows the comparison between the frequency response of reference-to-output transfer function calculated using PRBS and the frequency-swept sine wave method while Figure 5.8(b) shows the comparison for the frequency response of the control node disturbance rejection transfer function. The PRBS based measurement accurately tracks the sine-wave based measurement response.

The reference-to-output transfer function is used to detect the change in steady-state loading conditions of the converter. Figure 5.9 shows the measured transfer function for $I_{LOAD} = 50$ mA, 80 mA, and 150 mA. Both time domain and frequency domain analysis are used to diagnose the change in stability conditions of the converter due to loading effects. PM and CL-UGF are calculated and the results obtained are



(a)



(b)

Figure 5.8: Comparison of frequency responses obtained using the PRBS method with frequency-swept sine wave method. (a) Reference-to-output frequency response. (b) Control node disturbance rejection frequency response.

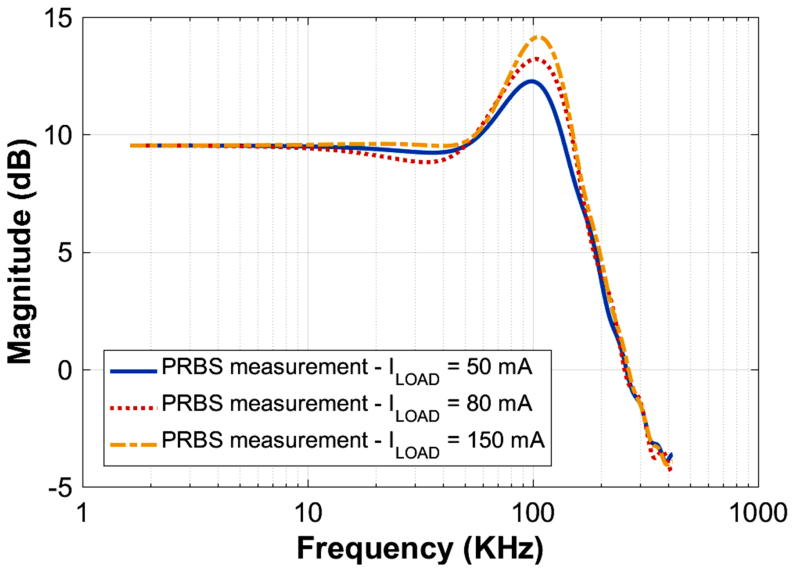
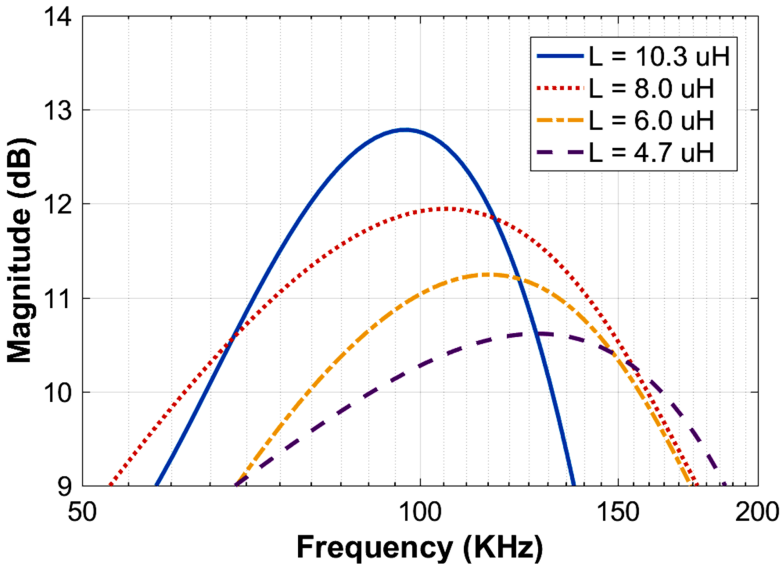


Figure 5.9: Reference-to-output transfer function frequency response measurements obtained for various I_{LOAD} using PRBS method.

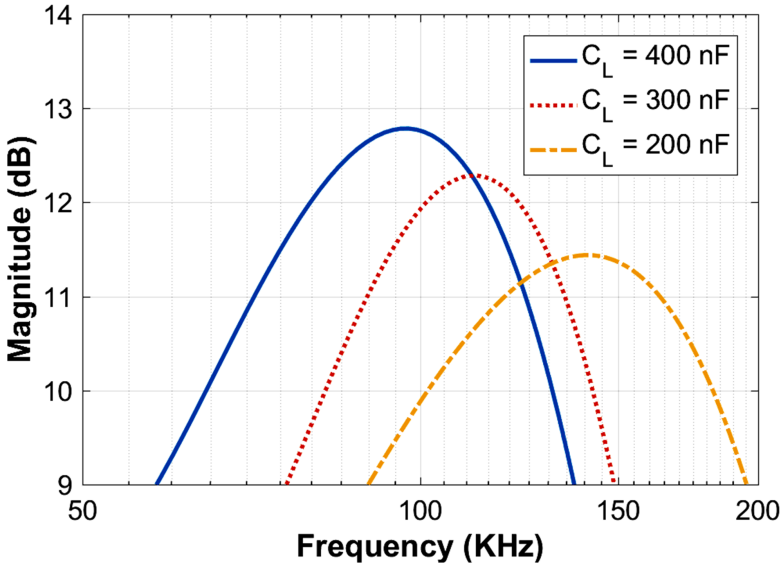
compared with those obtained using the frequency-swept sine wave method.

Figures 5.10 and 5.11 show the results close to the frequencies of interest (near ω_n and ω_c) obtained using the PRBS method for various L and C_L values for reference-to-output and control node disturbance rejection transfer function measurements, respectively. The values of L used are 4.7 µH, 6.0 µH, 8.0 µH, and 10.3 µH and C_L are 200 nF, 300 nF, and 400 nF. Using these transfer functions, parameters ω_n, Q-factor, and ω_c are calculated. The results obtained are compared to the model results calculated for nominal component values at ideal operating conditions, enabling diagnosis of the degradation/change in converter filter components.

The results in Figure 5.12 are calculated when both L and C_L values are changed simultaneously for identification purposes. This more accurately approximates the degradation of the converter filter components where more than one component experiences stress and derates during operation. Figure 5.12(a) shows the ω_n measured from the reference-to-output transfer function and Figure 5.12(b) shows ω_c measured

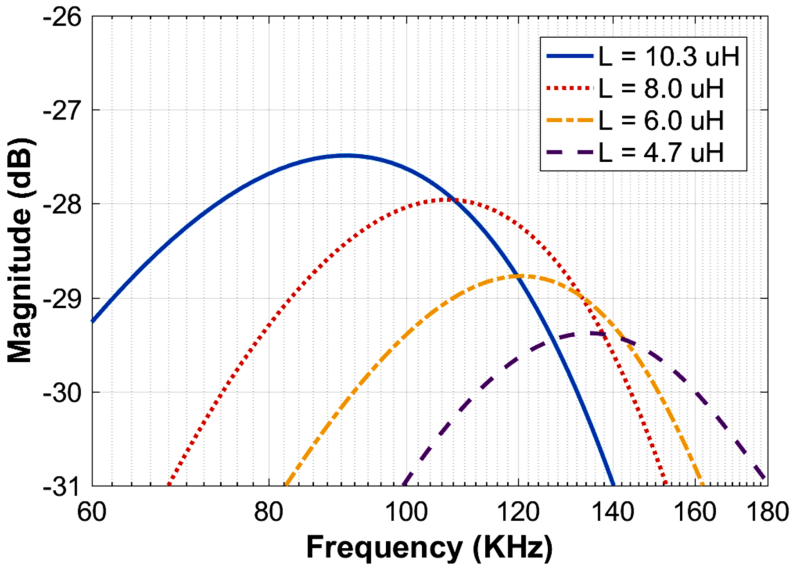


(a)

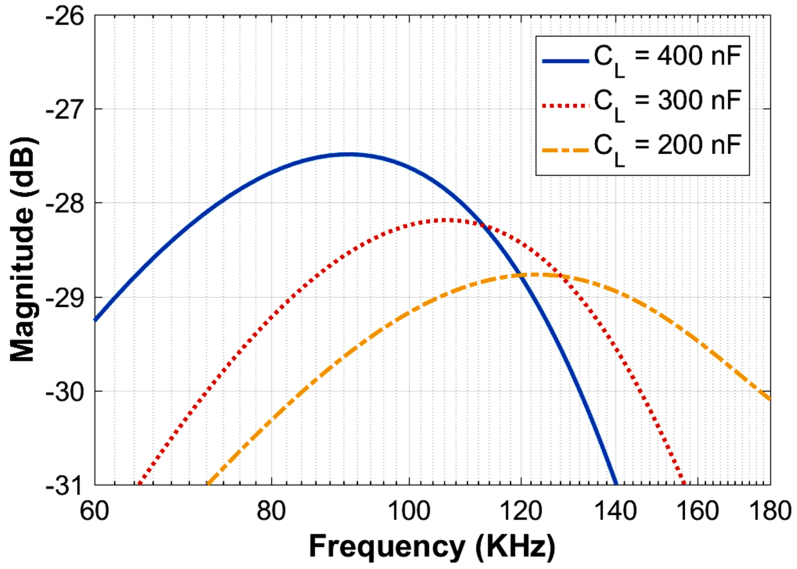


(b)

Figure 5.10: Reference-to-output transfer function frequency response measurements obtained using PRBS method. (a) Measurements for various L. (b) Measurements for various C_L

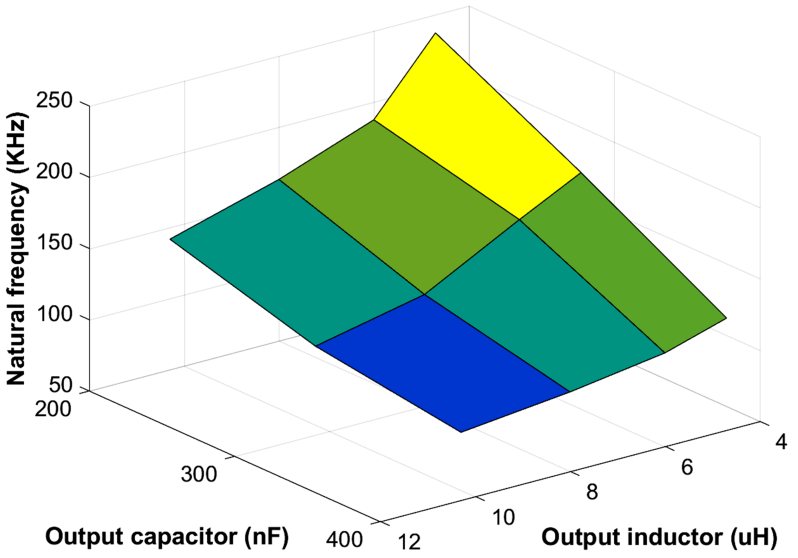


(a)

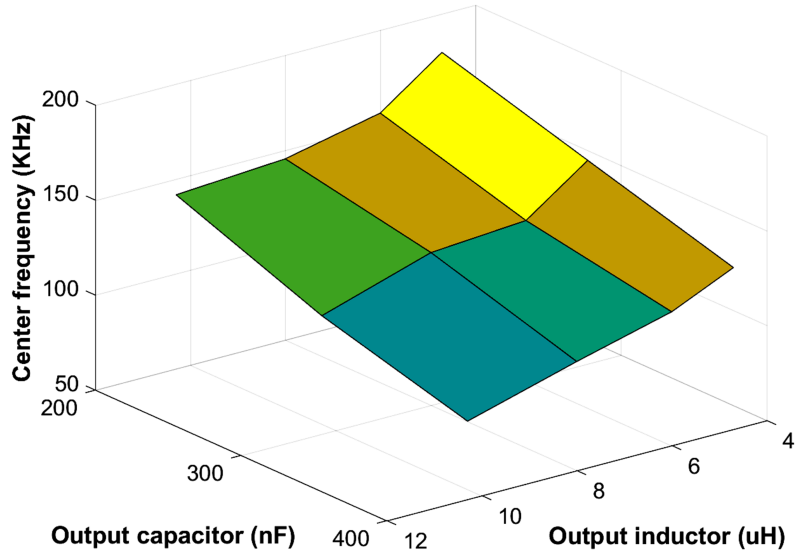


(b)

Figure 5.11: Control node disturbance rejection transfer function frequency response measurements obtained using PRBS method. (a) Measurements for various L. (b) Measurements for various C_L.

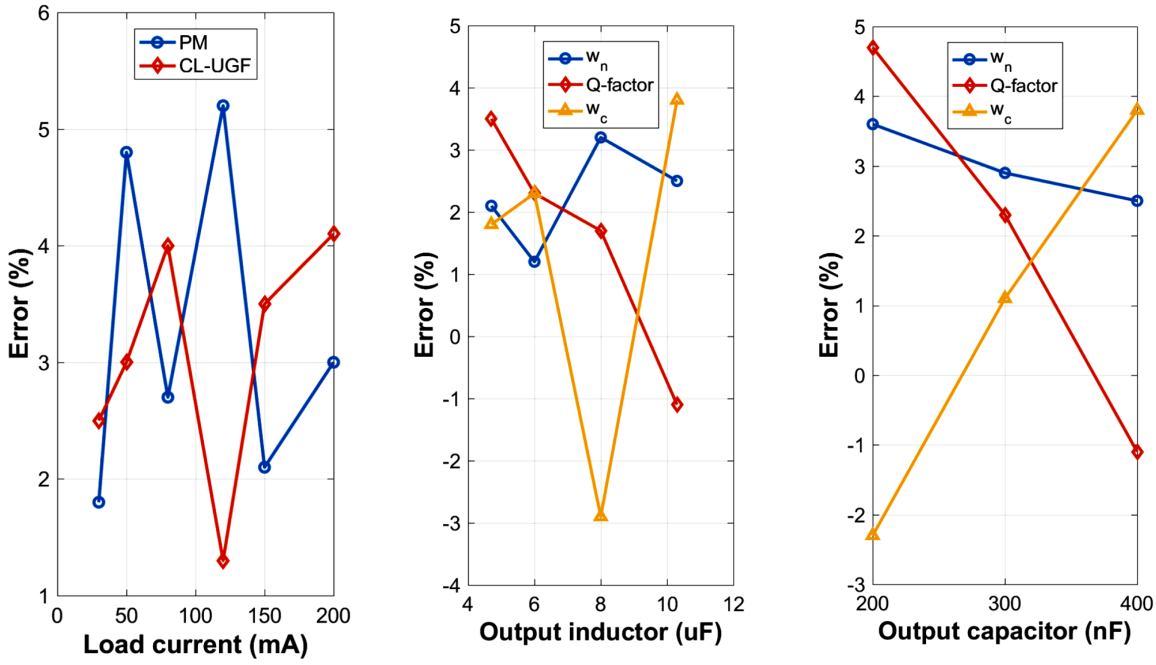


(a)



(b)

Figure 5.12: Results obtained using PRBS method for simultaneous change in L and C_L. (a) ω_n obtained from reference-to-output transfer function. (b) ω_c obtained from control node disturbance rejection transfer function.



(a) (b) (c)

Figure 5.13: Comparison of measurement errors of various parameters calculated using frequency-swept sine wave method and proposed PRBS method. Measurement errors against change in (a) I_{LOAD} (b) L (c) C_L.

from the control node disturbance rejection transfer function for various L and C_L values.

Figure 5.13 shows the errors in the calculation of the parameters calculated using the proposed PRBS method compared to the standard frequency-swept sine wave method, summarizing the results of Figure 5.9 - 5.11. The PM was calculated directly from the curve-fitted time domain impulse response while the parameters CL-UGF, ω_n, Q-factor, and ω_c were calculated from the frequency response obtained by taking the FFT of the truncated impulse response samples collected directly from the analog correlator. The proposed PRBS method can extract PM and CL-UGF within 5.2% and 4.1% error margin, respectively, over changes in I_{LOAD}. Additionally, converter

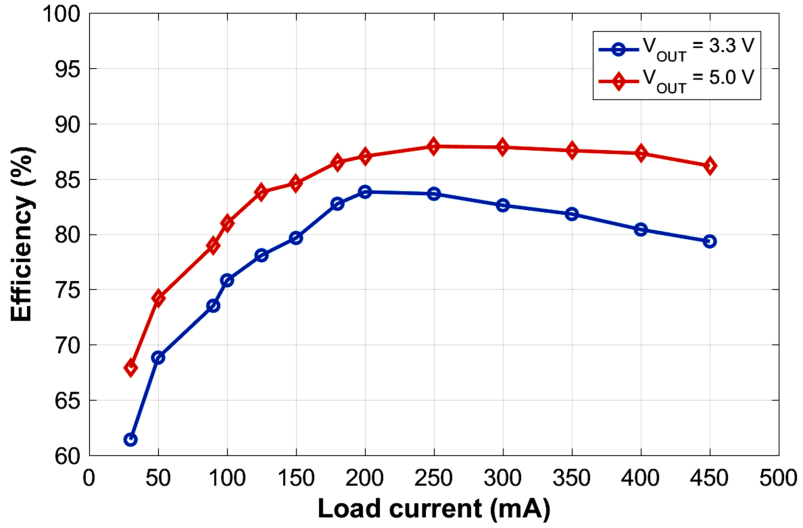


Figure 5.14: Measured efficiency of the DC-DC converter for different output voltages at nominal input voltage during normal regulation mode.

parameters such as ω_n, Q-factor, and ω_c can be estimated within 3.6%, 4.7%, and 3.8% error margin, respectively, over changes in L and C_L.

The current consumption of the regulation circuitry of the designed DC-DC buck converter during nominal operation conditions is 490 µA. The efficiency of the converter during normal mode of operation for V_{OUT} = 3.3 V and 5 V is shown in Figure 5.14. The system identification circuitry takes an additional 530 µA for 12.3 ms (typical, for 20 impulse samples) / 313.35 ms (max., for 511 impulse samples) when operated. As the system identification circuitry is turned on occasionally, the overall power impact on system efficiency is minimal. Also, the designed identification circuity has low hardware impact. The area impact due to the system identification blocks including related pads and ESD structures is 3.8%. TABLE 5.1 summarizes the IC specifications and performance.

Table 5.1: PERFORMANCE SUMMARY

DC-DC Converter Parameters	
Technology	JAZZ 0.6 µm SOI
V_{IN}	5 V - 8.125 V (6.5 V typical)
V_{OUT}	3.3 V - 5 V
Max. load current	450 mA
BIST @ I_{LOAD}	30 mA - 200 mA @ 3.3 V, 30 mA - 90 mA @ 5 V
Output voltage ripple	$\leq$ 25 mV
Switching frequency	5 MHz
Off-chip nominal filter capacitor (C_L)	400 nF
ESR of C_L	50 mΩ
Off-chip nominal filter inductor (L)	10 µH
DCR of L	60.8 mΩ
Efficiency	
I_{LOAD} [30 mA - 450 mA] @ V_{IN} = 6.5 V, V_{OUT} = 3.3 V	$61.41\% \leq \eta \leq 83.82\%$
I_{LOAD} [30 mA - 450 mA] @ V_{IN} = 6.5 V, V_{OUT} = 5 V	$67.91\% \leq \eta \leq 87.93\%$
BIST Performance	
Phase margin detection over I_{LOAD} change	5.2% max.
Unity gain frequency detection over I_{LOAD} change	4.1% max.
Natural frequency detection over L/C_L change	3.6% max.
Q-factor detection over L/C_L change	4.7% max.
Center frequency detection over L/C_L change	3.8% max.
Chip Area	
Die	3 mm x 3 mm
BIST Circuitry	3.8% of Die Area
Quiescent Current Consumption	
BIST circuitry	530 µA for 12.3 ms (typical) / 313.35 ms (max.)
Normal regulation circuitry	490 µA

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

A model reference based on-line BIST technique to track changes in the dynamic loop characteristics of analog-controlled DC-DC converters without affecting the normal mode of operation is presented. The proposed technique uses a digital PRBS based excitation and cross-correlation based measurement. The presented techniques are suitable for state-of-the-art high frequency DC-DC buck converters used in DVS applications, which have smaller footprint as they experience higher process/manufacturing variations jeopardizing their stable operation range. The presented techniques track dynamic parameters such as PM, CL-UGF, ω_n, Q-factor, and ω_c enabling diagnosis of degradation in advance and preventing system instability and failure. PRBS based white-noise disturbance is applied at the reference voltage and control input of the converter with test signal energy being spread across the spectrum. Circuit level implementation of circular PRBS, and reference and control node modulation are presented. The cross-correlation function to generate impulse response is also calculated on-chip using an analog correlator, which has lower computational complexity and storage requirements in comparison to digital correlation implementations.

A 5 V - 8.125 V input voltage range, 5 MHz switching frequency, analog-controlled voltage-mode DC-DC buck converter is designed for experimental verification of the proposed techniques. The results calculated using the PRBS based method are compared with a high accuracy frequency-swept sinusoidal method and are found to be in close agreement. The system identification circuitry has a small area impact with the designed circuitry consuming 3.8% die area (including related pads and ESD

structures) in a 0.6 µm 6 layer-metal SOI process. During operation, the system identification circuitry consumes 530 µA, thus having a minimal impact on the overall efficiency of the DC-DC converter.

6.2 Future Work

The presented work can be further refined and extensions to it can be made in the following areas:

- In the presented work, the data obtained by sampling the on-chip correlator output was transferred to a PC for further computation and post-processing in MATLAB. For a complete embedded implementation and online BIST; curve fitting, FFT, and diagnosis algorithms can be implemented in FPGA/DSP.

- The parameters such as PM, CL-UGF, ω_n, Q-factor, and ω_c give important information about the degradation of the converter circuit. Additional further work to extract individual parameters is performed in [62], where the output filter inductor identification is performed. Although a non-trivial task, similar identification techniques could be developed to individually identify other converter parameters, most notably the output filter capacitor.

- The information obtained by the proposed techniques could be used to improve the performance of the degrading circuits. Auto-tuning of the analog controller/filter could be implemented using field programmable analog arrays (FPAAs) proposed in [63] and [64].

- The presented technique for system identification is independent of the converter class. Hence, the technique can be modified and implemented for other DC-DC switching converters such as boost, buck-boost, forward, flyback, and

multiphase converters. The implementation of the technique has also been demonstrated by system level modeling in [55] for LDOs. The model can be further refined and a fully integrated implementation can be developed for BIST of LDOs.

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