Digital Controlled Multi-phase Buck Converter

with Accurate Voltage and Current Control

by

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ABSTRACT

With the rapidly growing functional capabilities of portable devices, the peak current of high current FPGAs and application processors (APs) becomes several amperes and higher. To prolonging battery life, switching regulators, such as the buck converter, are often used to provide power for such FPGAs and APs. However, power efficiency of single-phase DC-DC converters becomes problematic when the peak current reaches several amperes. Multi-phase operation has been proved to be one of the most effective ways to increase the power efficiency performance at heavy load conditions while providing faster transient response. Master-slave mode is often used to control the multi-phase operation of the buck converters.

To cope with the increasing speed of APs, the load transient performance is becoming more and more stringent for switching-regulators. Traditionally, the pulse width modulation (PWM) is used to control the buck converter and a large amount of by-pass capacitors are needed for improving the load transient performance. However, for portable and wearable applications, the PCB area is very limited and minimizing the required PCB area for the DC-DC converters is becoming more and more important. Hysteretic control mode is an attractive solution for such small portfolio applications, because hysteretic-controlled buck converter is inherently stable requiring on bulky compensation network and the load transient response is very fast.

In this paper, a 4-phase, quasi-current-mode hysteretic buck converter with digital frequency synchronization, online comparator offset-calibration and digital current sharing control is presented and fabricated by using a 5-level metal 0.18μm CMOS process with 5V thick gate oxide option. The switching frequency of the hysteretic

converter is digitally synchronized to the input clock reference by using a digital phase locked loop (DPLL). By using the online offset calibration techniques, the input-referred offset of the hysteretic comparator is canceled enabling accurate voltage regulation. Master-slave control mode is used to control the 4-phase operation for the buck converter. A digital-controlled delay line is designed to calibrate the duty cycle for slave phases to achieve equal current sharing among each phase. The buck converter is able to enter into the segmentation and burst-mode at the light load conditions to achieve high efficiency across all load conditions.

To My Wife, Zhining Qi, My Son, Mason Sun and Family

Thank you for all the love and support

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CHAPTER 1 INTRODUCTION

Power efficiency of single-phase DC-DC converters becomes problematic when the peak current demand of high performance FPGAs and application processors (APs) reach several amperes. Therefore, multi-phase operation is commonly used to increase settling speed and reduce the conduction loss for DC-DC converters in high current load applications [1]–[4]. In multi-stage parallel converters, the inductor current of each phase is interleaved and synchronized. As a result, the input RMS current and the output ripple current are both reduced. Because of the ripple cancellation effect, multi-phase operation is proved to be one of the most effective ways to reduce the decoupling capacitance for the stringent voltage tolerance requirements during the load transient [5], [6]. Another important benefit of multi-phase operation is better load transient response, due to the energy stored in each output inductor is reduced and the effective switching frequency is multiplied by the number of phases at the DC-DC converter's output [7], [8].

Traditionally, the pulse-width modulation (PWM) based DC-DC converters utilize voltage mode [9]–[11], peak current mode [12]–[14], valley-current mode [13] and the average current mode [15] controllers. Linearization is necessary when designing the compensation network required by the PWM closed-loop transfer function. The PWM controller is a sampled-data system, the bandwidth of which is limited by the switching frequency [16-17]. Beyond half of the switching frequency, the linearized model is not accurate. Therefore, the PWM controller's closed-loop bandwidth is usually designed to be at least 10 times less than the switching frequency. To cope with the stringent overshoot and undershoot voltage tolerance requirements, large decoupling capacitance is typically used for DC-DC converters utilizing PWM control to compensate the slow load

transient response performance. For instance, the decoupling capacitance for the Virtex-5QV FPGA include three 1μF, two 47μF and two 470μF ceramic capacitors when using a typical peak-current mode point of load regulator. Therefore, PWM control is not a suitable solution for mobile and wearable applications, where the PCB portfolio is limited.

Multi-phase current-mode hysteretic buck converter is a suitable candidate for point-of-load applications that require fast transient response and small PCB profile design. However, there are also some design problems for the DC-DC converters utilizing hysteretic control. First, the switching frequency of the DC-DC converter is highly impacted by external device parasitics, such as ESR of the decoupling capacitor, comparator delay, driver delay, and the hysteresis voltage. For example, for voltage-mode hysteretic controlled DC-DC converters, the switching frequency is low when the load current is small and that is why hysteretic control is widely used to decrease the switching loss and improve the power efficiency for light load conditions. To keep the voltage ripple same, the DC-DC converter will increase its switching frequency when the load current is large. Different input and output conditions also have a big impact on the switching frequency [21]. Therefore, it is very difficult to do the proper EMI shielding for hysteretic-controlled buck converter for the automotive and mobile applications. Second, there are several error sources that can cause a mismatch between the voltage reference input and the output voltage, which will degrade the voltage regulation accuracy, such as the inductor DC resistance (DCR) induced error and the comparator input-referred offset induced error. Third, the current sharing accuracy is highly dependent on the matching of the duty cycle, inductor DCR and the other resistance on the power path of each phase.

In [5], a master-slave control method is used to implement the multi-phase controller and the phase synchronization is achieved by the voltage ramp inside the PWM controller. An average-current-balancing (ACB) calibration loop is introduced to calibrate the duty cycle for the slave phases to obtain accurate current sharing. However, because of the voltage-mode operation, the transient response is not very fast. Another work on the multi-phase hysteretic buck converter is also reported in [22], which uses a delay locked loop (DLL) to implement the phase synchronization between the master and the slave phases. The phase synchronization is realized by the delay line which comprises of a series of current-starved inverters. The tail current of the current-starved inverters is calibrated by the delay line to provide accurate amount of delay required by the phase synchronization. However, it is lack of the current sharing scheme and purely depends on matching for current sharing among each phase. Also, the switching frequency of the hysteretic controlled buck converter is variable in [22], which will affect the automotive and mobile applications.

In this paper, a 4-phase quasi-current-mode hysteretic buck converter with digital frequency synchronization (DFS) and current sharing control is presented. Proposed approach can achieve constant switching frequency and accurate current sharing. An online auto-zeroing based hysteretic comparator offset calibration topology is also proposed achieving higher output voltage accuracy. In the proposed topology, master-slave control mode is used for multi-phase operation. In Chapter 2, the architecture of the current-mode hysteretic-controlled buck converter is discussed. This is followed by the description of the multi-phase operation and its benefits in Chapter 3. Chapter 4 introduces the system architecture and the operation principle of the multi-phase

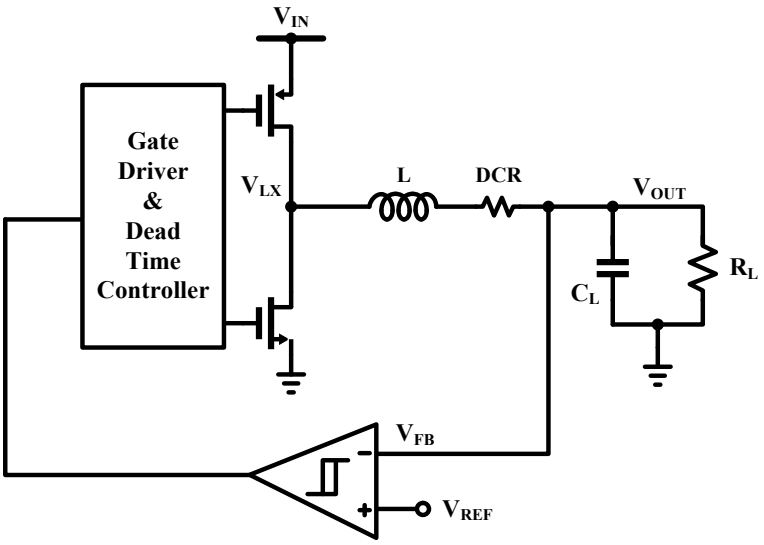
operation. And the proposed current sharing topology and power save mode are discussed in details in Chapter 5. The details of the master phase operation, such as frequency synchronization and online auto-zeroing offset calibration circuits are discussed in Chapter 6 and Chapter 7. Finally, the measured results and the conclusions are presented in Chapter 8 and Chapter 9.

CHAPTER 2 ARCHITECTURE OF THE CURRENT-MODE HYSTERETIC BUCK CONVERTER

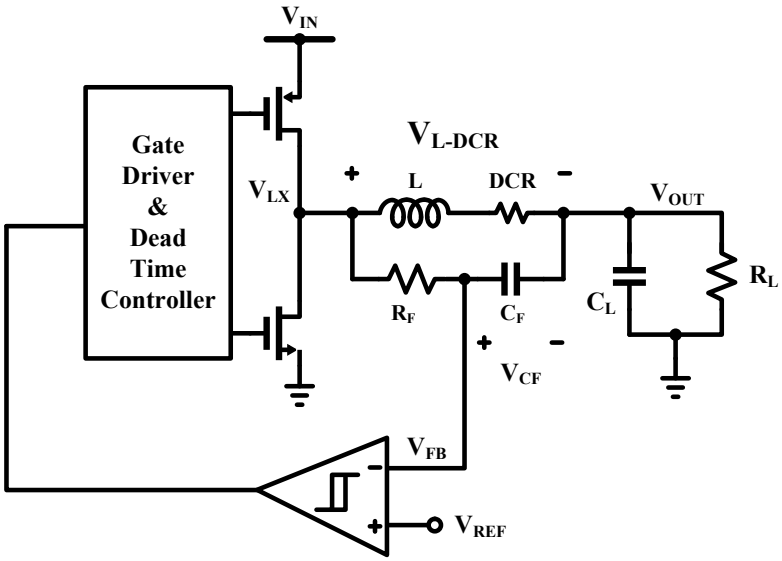
As discussed before, traditionally PWM control is utilized to control the buck converter and type II or type III compensator is commonly used to provide sufficient phase margin for the peak-current-mode or voltage-mode controller. When designing the PWM controller, linearization is required for the power stages because the small signal model is needed for deriving the transfer functions of the voltage loop or current loop.

Hysteretic control is totally different from the PWM control because it is inherently stable and does not need to design any compensation network as the PWM control. Indeed hysteretic control belongs to the so-called "ripple-based control", because it either regulates the output voltage ripple or the inductor current ripple. When the hysteretic controller is designed to control the buck converter, the buck converter itself can be considered as an oscillator.

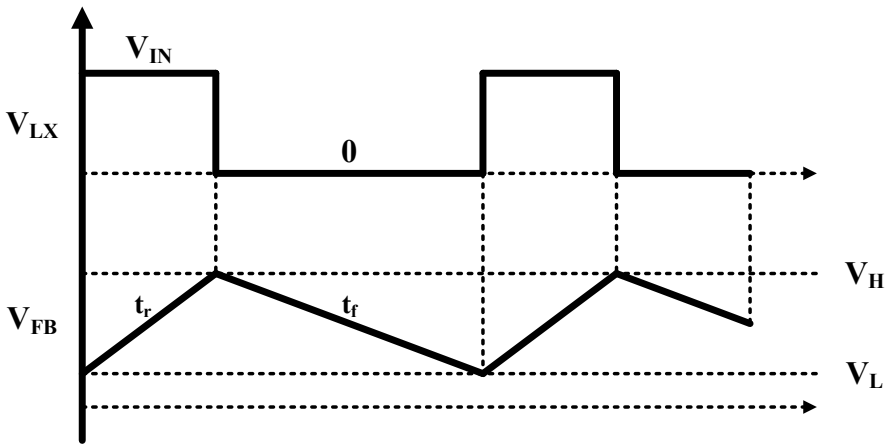
For the voltage-mode hysteretic buck converter as shown in Fig. 1 (a), the output voltage ripple is constant and for the current-mode hysteretic buck converter as shown in Fig. 1 (b), the inductor current ripple is constant, where V_H and V_L are the hysteresis voltage of the hysteretic comparator.



(a) Voltage-mode Hysteretic Buck Converter



(b) Current-mode Hysteretic Buck Converter



(c) Current-mode Hysteretic Buck Converter Operation Principle

Fig. 1 Structure of a Typical Current-mode Hysteretic Buck Converter [19].

Either for voltage-mode or current-mode hysteretic buck converter, the hysteretic comparator needs ripple to work. For multi-phase operation, the output voltage ripple might become zero at certain duty cycle conditions which will be discussed in details in Chapter 3. Therefore, voltage-mode hysteretic control is not a good candidate for multi-phase hysteretic buck converter and the current-mode control is adopted for our design.

To further explain the operation of the hysteretic control, when the high-side PMOS is turned on and the low-side NMOS is turned off, the voltage on the V_{LX} node is equal to V_{IN} by neglecting the on resistance of the PMOS. And V_{LX} node will charge the capacitor C_F through the resistor R_F as shown in Fig. 1 (c). When the high-side PMOS is turned off and the low-side NMOS is on, the V_{LX} node voltage becomes to zero by neglecting the on resistance of the NMOS. And the capacitor C_F will be discharged through the resistor R_F to ground. Therefore, the ripple necessary for the hysteretic comparator is generated by the R_F and C_F network.

A. Quasi Current Emulator

Traditionally, the R_F and C_F network is designed to emulate the inductor current as shown below:

$$I_L = \frac{V_{L-DCR}}{sL + DCR} = \frac{V_{CF} \cdot sC_F\left(R_F + \frac{1}{sC_F}\right)}{sL + DCR} = \frac{V_{CF}}{DCR} \cdot \frac{1 + sR_FC_F}{1 + s\frac{L}{DCR}} \quad (1)$$

where DCR is the DC resistance of the inductor. If $R_FC_F = L/DCR$, the voltage across the capacitor C_F is the same as the voltage across the DCR, which can be used to obtain the inductor current information [20]. To match the time constants, the inductor value and the DCR resistance value should be measured. In this application, the maximum load current is 6A. To reduce the conduction loss, a 330nH inductor with maximum 5mΩ DCR is used. Therefore, it is very difficult to accurately measure the exact value of the DCR.

In the quasi-current-mode hysteretic control, the time constants of R_F and C_F in Fig. 1 (b) is not necessary to match that of the L and DCR to get the current information flowing through the inductor. Instead, R_F and C_F form a quasi-current emulator of the inductor current. Considering in the multi-phase operation mode, the output voltage ripple might become to zero at certain duty cycle conditions, while the inductor current ripple is not. Therefore, by designing the quasi-current emulator, it will provide the ripple necessary for the hysteretic comparator to work in either single-phase or multi-phase operation mode.

B. Free-run Switching Frequency

Fig. 1 (c) shows the idealized voltage waveforms of the feedback node V_{FB} and the switching node voltage (V_{LX}). Because of the low-pass filter from V_{LX} to V_{FB} node and small ripple on the buck converter's output, the voltage waveform at the V_{FB} node can be assumed to be an ideal triangular wave with constant rising and falling slope. For capacitor C_F,

$$I_{CF} = C_F \frac{dv_{CF}}{dt} \tag{3}$$

Since the ripple on the capacitor C_F is designed to be very small, the charging current can be written as:

$$I_{Charging} = \frac{V_{IN} - V_{OUT}}{R_F} \tag{4}$$

Therefore, the rising slope is given by:

$$t_r = \frac{V_{IN} - V_{OUT}}{R_F C_F} \tag{5}$$

The same procedure can be applied when calculating the falling slope:

$$t_f = \frac{-V_{OUT}}{R_F C_F} \tag{6}$$

Therefore, the switching period can be written as:

$$T_S = t_1 + t_2 = \frac{V_H - V_L}{\frac{V_{IN} - V_{OUT}}{R_F C_F}} + \frac{V_H - V_L}{\frac{V_{OUT}}{R_F C_F}} = (V_H - V_L) \cdot R_F C_F \cdot \frac{1}{(V_{IN} - V_{OUT}) \cdot \frac{V_{OUT}}{V_{IN}}} \tag{7}$$

In this case, the switching frequency can be expressed as [22]:

$$f_{SW} = \frac{D \times (1 - D)}{\tau_{RC}(V_{hys} / V_{IN}) + \tau_D} \tag{8}$$

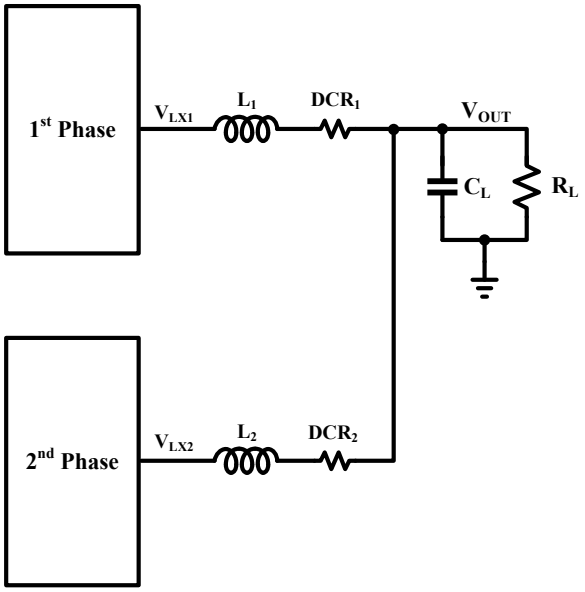
where D is the duty cycle, τ_{RC} equals to the time constant $R_F C_F$, τ_D is the propagation delay, V_{hys} is the hysteresis window voltage of the comparator and V_{IN} is the power supply of the buck converter. Notice when the load current changes, because of the internal on resistance of the power FETs, the duty cycle D also changes. Therefore, the load condition also has an impact on the switching frequency of the hysteretic buck converter.

From (8), duty cycle D is determined by the input and output voltage conditions. V_{IN} is the input power supply which is determined by the applications. Therefore, there are three parameters which can be tuned to ensure the switching frequency is fixed, which are the time constants τ_{RC}, the hysteresis window V_{hys} and the loop delay τ_D.

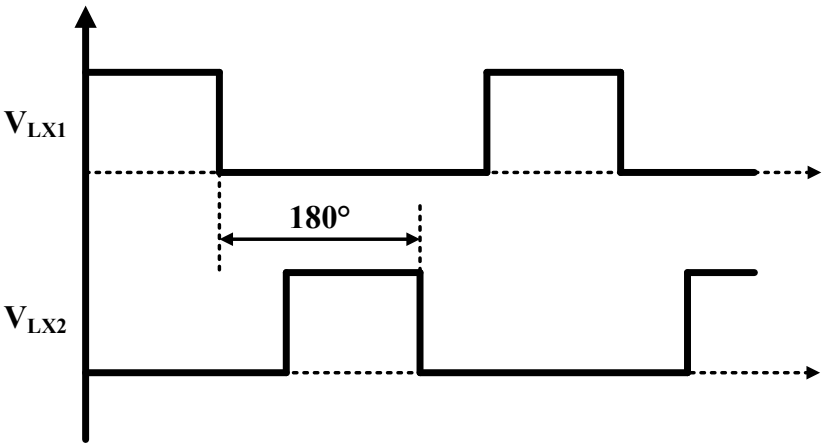
CHAPTER 3 OPERATION PRINCIPLE OF THE MULTI-PHASE BUCK CONVERTER

Multi-phase operation is widely used in research or industry to improve the power efficiency at heavy load conditions. As discussed before, the power loss of the DC-DC converters includes condition loss, switching loss, gate drive loss and etc. At heavy load conditions, the conduction loss dominates. To minimize the conduction loss, the most effect way is to minimize the on-resistance of the power FETs. By paralleling the buck converter, the effective internal on-resistance of the power FETs is divided by the number of the phases. Therefore, multi-phase operation is one of the most effective ways to improve the power efficiency performance at heavy load conditions.

However, multi-phase operation does not only require paralleling the buck converter. It also requires the phase synchronization among each phase. For example, for a 2-phase buck converter, the switching signal of the second phase should have a 180 degree phase shift compared with the first phase as shown in Fig. 2 (b). And for an N-phase buck converter, the phase shift between each phase should be equal to 360/N degree. One way to implement the phase synchronization function is to use a delay line which is comprised of a series of current-starved inverters and use a delay locked loop to calibrate the delay of the delay line [22].



(a) 2-phase Buck Converter



(b) Waveforms on the V_{LX} Node

Fig. 2 Operation Principle of 2-phase Buck Converter.

A. Benefit of Multi-phase Operation

By interleaving and phase shifting the switching waveforms, there are several benefits of the multi-phase operation. First, the output voltage ripple is reduced. For some radar applications, the ripple on the power supply is extremely important for the analog-to-

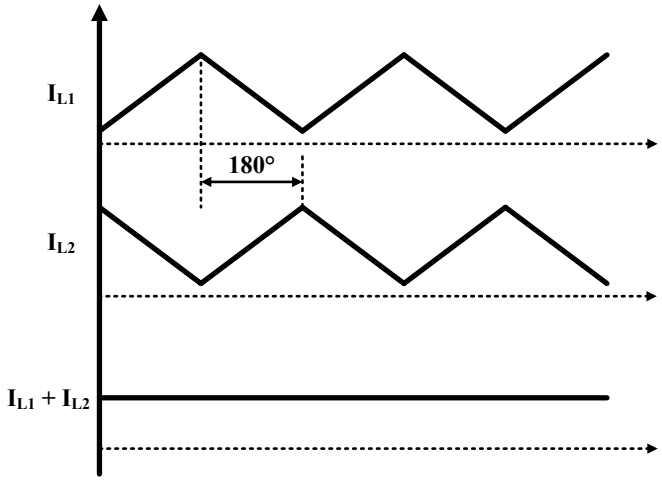
digital converter (ADC) performance. Therefore, customers have to pay very high price for the high PSR low-dropout voltage regulators (LDO). The buck converter is usually the power supply for such LDOs and if the output voltage ripple of the buck converter is reduced there is no need for purchasing a high PSR LDO. Therefore, the total cost will be greatly reduced. Considering the voltage ripple on the buck converter's output, it can be written as:

$$\Delta V = \Delta I_L \times ESR \tag{9}$$

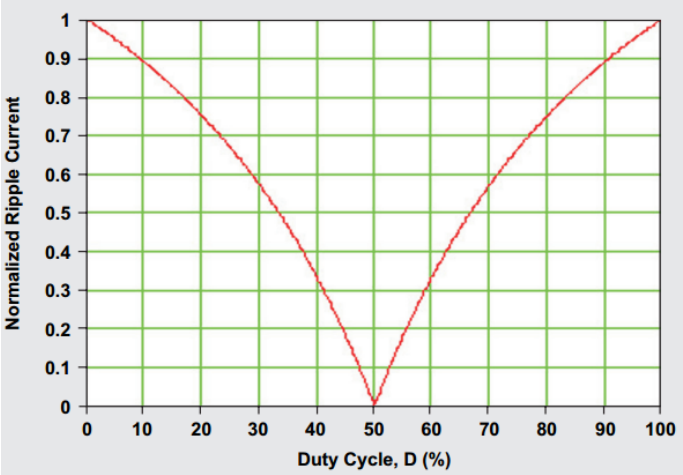
where ΔI_L is the inductor current ripple and ESR is the effective serial resistance of the load capacitor. One common way to reduce the voltage ripple is to use a large amount of load capacitor in parallel so that the effective ESR is reduced as seen in the single-phase operations of the DC-DC converters. And the other way is to reduce the inductor current ripple. Traditionally, large inductors are used to reduce the inductor current ripple because the ripple can be calculated as $D\times(V_{IN} - V_{OUT})/L\times T_S$, where D is the duty cycle, V_{IN} is the input power supply, V_{OUT} is the output voltage of the DC-DC converter and T_S is the switching period. However, large inductor will result in large PCB portfolio design and for mobile and wearable devices the PCB area and height is very limited.

Multi-phase operation will reduce the effective inductor current ripple since the inductor current is interleaved among each phase. Fig. 3 shows the inductor current for a 2-phase buck converter when duty cycle equals to 50% and the effective inductor current seen by the capacitor at the buck converter's output. By interleaving the switching signal, the effective inductor current becomes to zero and there is no ripple at the buck converter's output based on (9). Therefore, with the same output ripple specs, multi-

phase operation allows the DC-DC converters utilize small capacitance to achieve the same amount of output voltage ripple.



(a) Inductor Current of 2-phase Buck Converter When Duty Cycle = 50%



(b) Normalized Ripple Current vs. Duty Cycle [7]

Fig. 3 Inductor Current of 2-phase Buck Converter.

Fig. 3 (b) shows the normalized ripple current for a 2-phase buck converter to the single phase operation. It is easily to find out that multi-phase operation has less ripple current across the whole duty cycle range. Therefore, when DC-DC converter is working in the multi-phase mode, the amount of by-pass load capacitor can be reduced to get the

same output ripple. Not only the output voltage ripple gets reduced, the input current ripple also gets reduced by the multi-phase operation as shown in Fig. 4. As a result, the amount of by-pass capacitor for the DC-DC converter's input power supply can also be reduced.

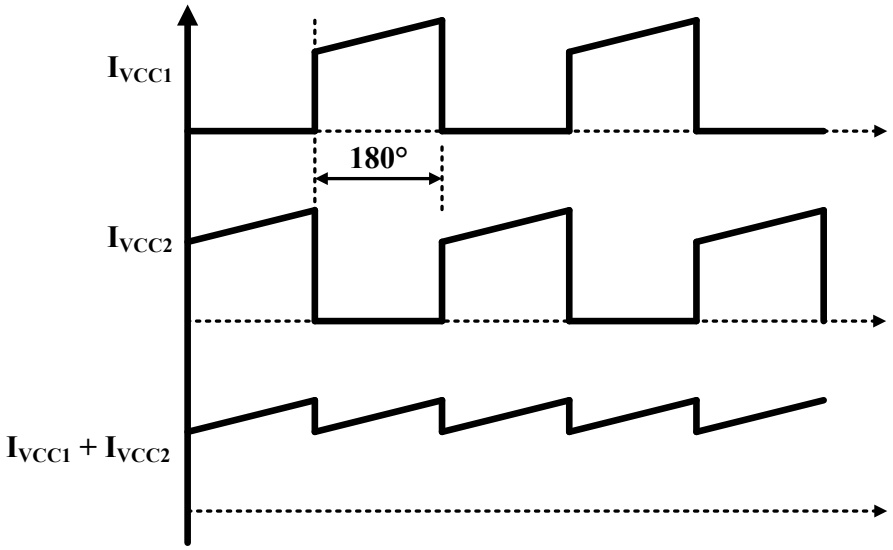


Fig. 4 Power Supply In-rush Current Simulation Results When Duty Cycle = 50% for a 2-phase Buck Converter.

Another important benefit for multi-phase operation is the faster load transient response compared with the single-phase operation. Assuming the switching frequency of each phase is f_{SW}, the effective switching frequency seen at the output for an N-phase DC-DC converter should be $N \times f_{SW}$. Therefore, the transient response is much faster for an N-phase DC-DC converter compared with the single-phase DC-DC converter with the same switching frequency. Thermal management is also better for multi-phase operation compared with the single phase because the inductor current is distributed across each phase. Therefore, the reliability is better for the multi-phase operation because even if

one of the phases is not working, there are other phases to provide the power for the DC-DC converter.

B. DC Current Sharing Model

The DC current sharing model of a multi-phase buck converter is shown in Fig. 5 (a) [22], where R_{loss-i} is the total resistance on the power path for each phase, including power train resistance of both the high-side and low-side power FETs, bond-wire resistance, package lead frame resistance, DCR, PCB trace resistance and other parasitic resistance. The total dc conduction loss equals to the sum of the dc conduction loss from each phase, which is given by:

$$P_{loss} = \sum_{i=1}^{N} \langle I_{L-i} \rangle^2 R_{loss-i} \tag{10}$$

where N is the number of phases and $\langle I_{L-i} \rangle$ is the average inductor current for the i^{th} phase. Considering the sum of the inductor current is constant:

$$I_O = \sum_{i=1}^{N} \langle I_{L-i} \rangle \tag{11}$$

Assuming $R_{loss-1} = R_{loss-2} = \cdots = R_{loss-N}$ to simplify the discussion,

$$P_{loss} = \sum_{i=1}^{N} \langle I_{L-i} \rangle^2 R_{loss-i} \geq \frac{I_O^2}{N} R_{loss-i} \tag{12}$$

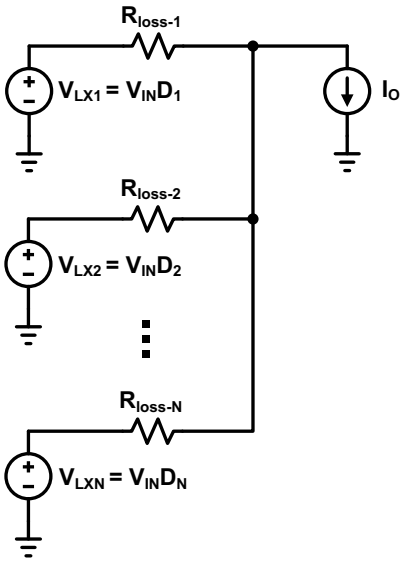
Only when $\langle I_{L-1} \rangle = \langle I_{L-2} \rangle = \cdots = \langle I_{L-N} \rangle$, the multi-phase converter is able to get the minimum conduction loss.

Both the duty cycle and the power-path resistance mismatch will result in mismatch between current stages and degrade the efficiency performance. For example, assume a two-phase buck converter with a 50mΩ resistance for R_{loss-1} and a 100mΩ for R_{loss-2}, which is quite possible considering the total resistance mismatch of the power train,

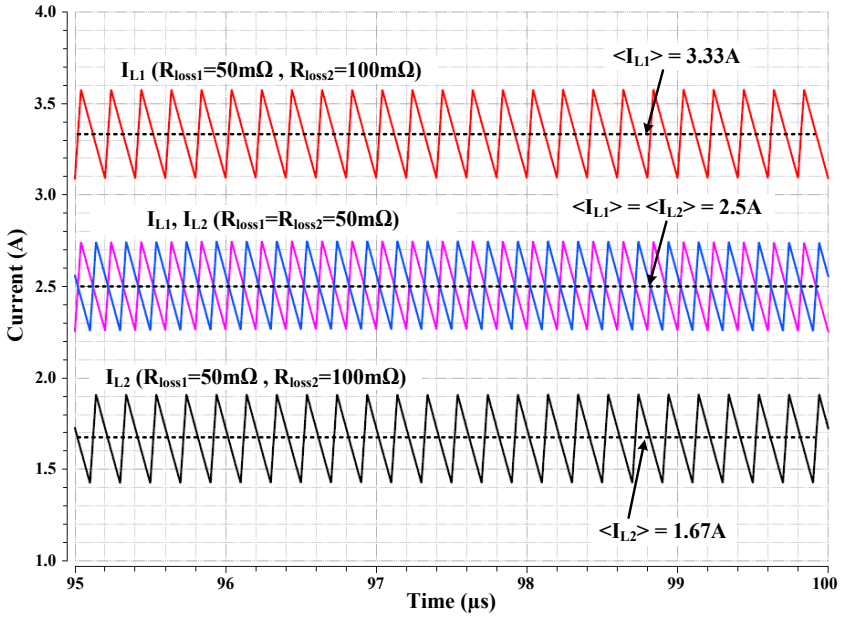
bonding wire, lead frame, IC layout structure and the PCB trace resistance. Fig. 5 (b) shows that even if with a 50mΩ R_{loss} resistance mismatch on the power path between two phases, it yields about 50% current mismatch between the two phases. Therefore an accurate method to control individual stage current and ensure current matching is a critical design problem.

The current flowing through each phase can be expressed as $(D_i V_{IN} - V_{OUT})/R_{loss-i}$. The V_{IN} and V_{OUT} are determined by the applications, which are out of the control of the designers. R_{loss} is determined by the on resistance of the high-side and low-side power FETs, the DCR of the inductor, the bonding wire resistance and the other parasitic resistance, which are all out of control of the designers. The only way which can be used to tune the current of each phase is the duty cycle.

In this work, the duty cycle of the slave phases is calibrated by a duty-cycle calibrated delay line through the digital duty cycle adder and the duty cycle substractor, which will be discussed in details in Chapter 5.



(a) DC Current Sharing Model of a Multi-phase Converter [22]



(b) Simulation Results of R_{loss} Mismatch Impact on Current Sharing for a Two-phase Buck Converter with 5A Load Current

Fig. 5 DC Current Sharing Model and 2-phase Buck Converter Inductor Current simulation result.

CHAPTER 4 SYSTEM ARCHITECTURE AND THE OPERATION PRINCIPLE OF THE PROPOSED MULTI-PHASE OPERATION

A 4-phase hysteretic-controlled current-mode buck converter is proposed and its diagram is shown in Fig. 6. Master-slave control method is used to control the multi-phase operation. The voltage regulation, switching frequency synchronization, burst mode and the load transient enhancement is implemented inside the master phase. The slave phases only contain the driver, power FETs and the current sensor.

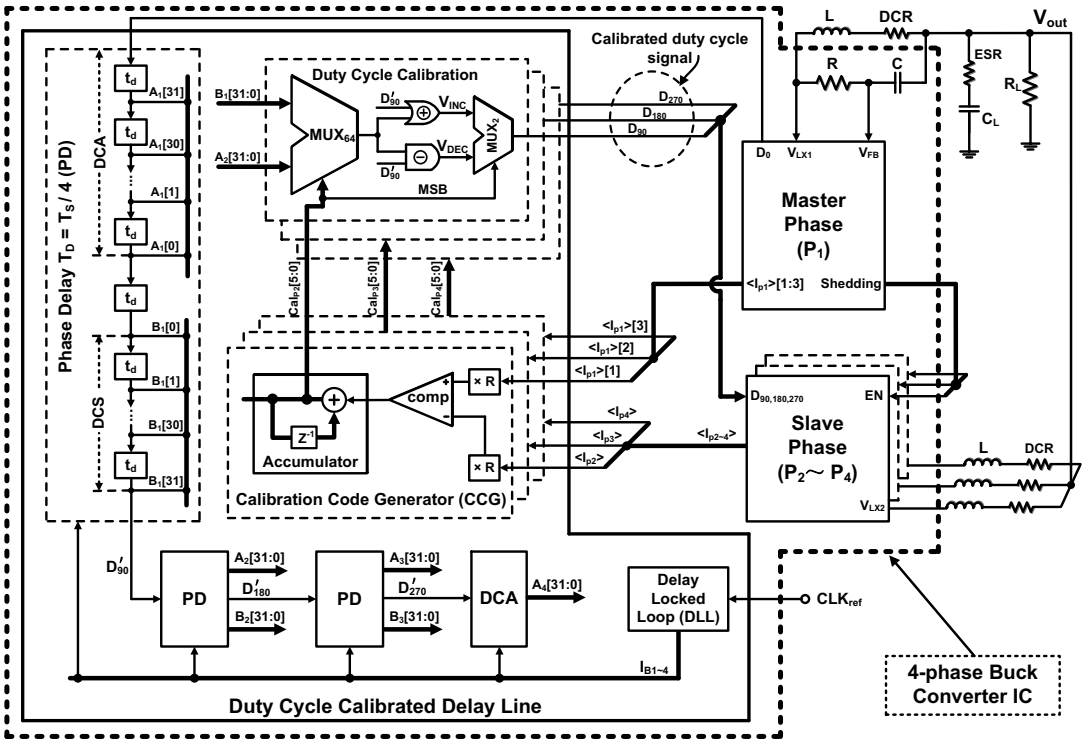


Fig. 6 Block Diagram of Proposed 4-phase Hysteretic-controlled Quasi-current-mode Buck Converter.

A. Phase Synchronization

Phase synchronization is required for multi-phase operation. For a 4-phase operation, each slave phase's switching signal should be 90° later than the previous phase as shown in Fig. 7.

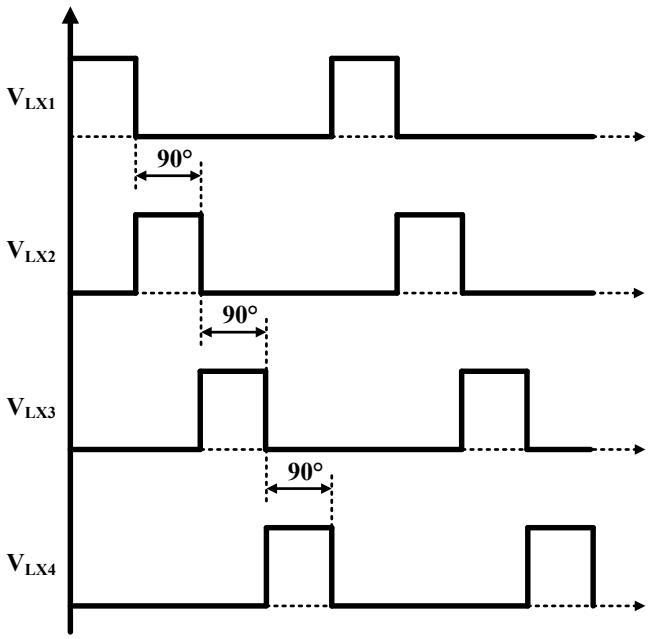
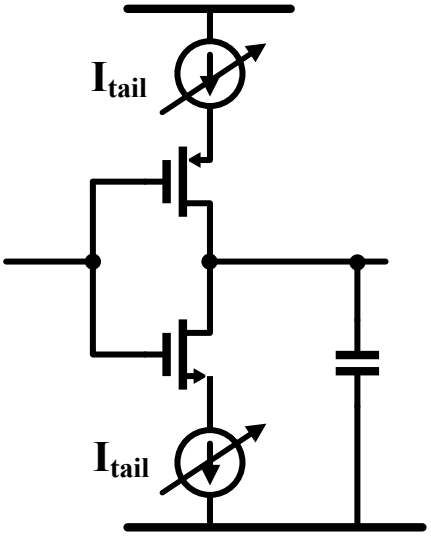


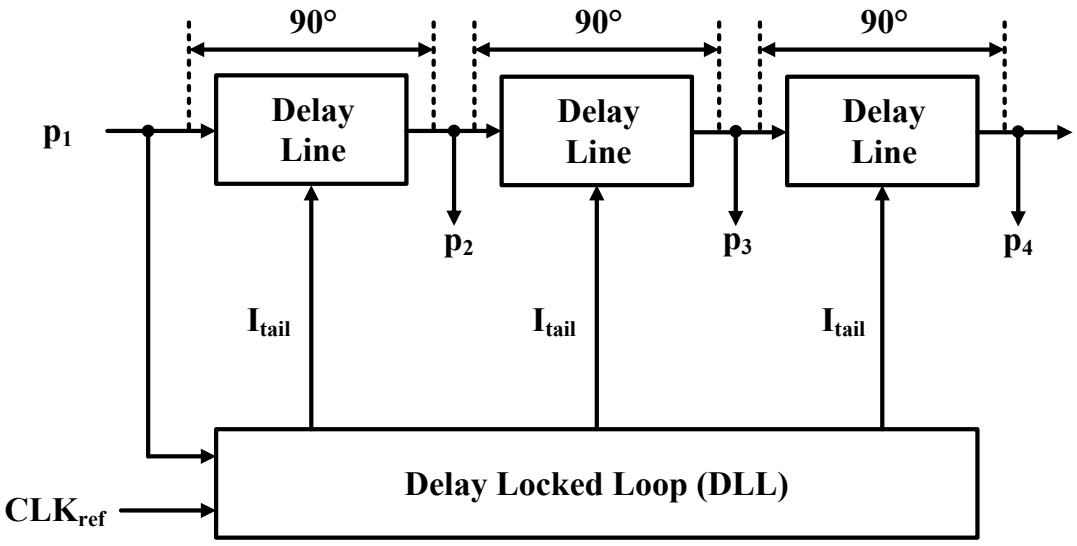
Fig. 7 Phase Synchronization Requirement for 4-phase Operation.

A delay line which is comprised of a series of current-starved inverters has been designed to delay the switching signal of the master phase (V_{LX1}) to achieve the desired phase delay for other three slave phases ($V_{LX2\sim4}$). The circuit for the current-starved inverter is shown in Fig. 8 (a). By controlling the current source and the current sink (I_{tail}), each current-starved inverter will implement a small amount of delay Δt. When a square-wave passes such current-starved inverters, there will be a slight duty cycle mismatch between the input and the output signal. Since a current sharing topology is designed, this

duty cycle mismatch will be corrected by the current sharing circuits and it does not affect the current sharing performance in this design.



(a) Current-starved Inverter



(b) Delay Line

Fig. 8 Current-starved Inverter and Delay Line.

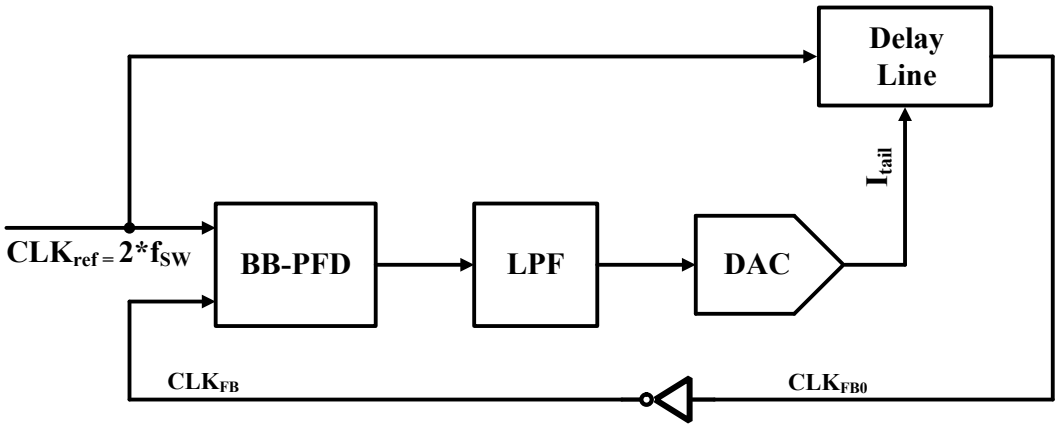
A delay locked loop is designed to calibrate the amount of delay needed for the current-starved inverter to obtain 90° phase shift and provide the proper current I_{tail} as

shown in Fig. 8 (b). The current sharing topology is also designed by reusing the delay line which will be discussed in details in Chapter 5.

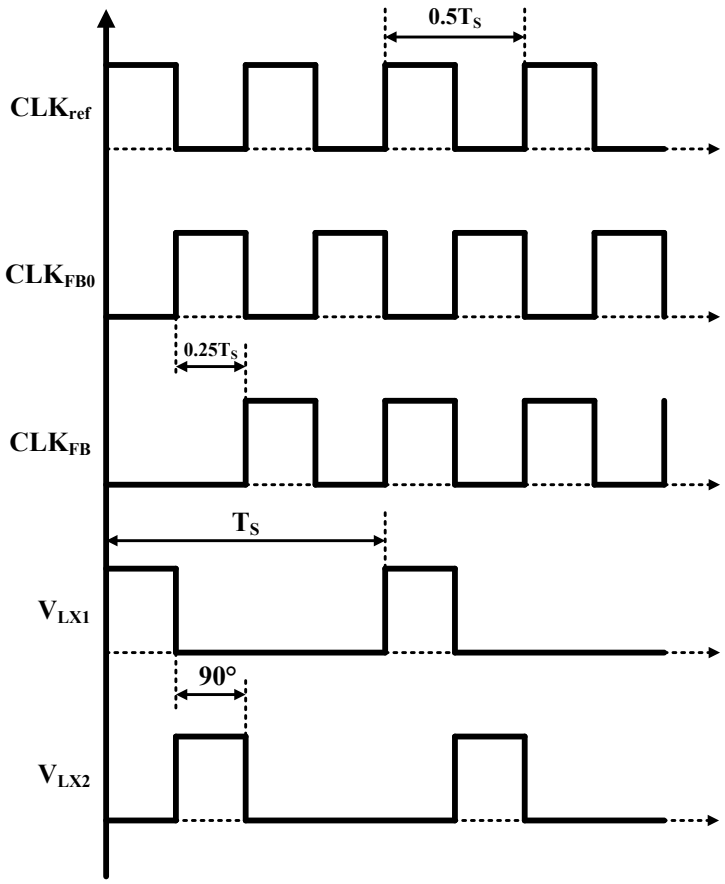
B. Delay Locked Loop (DLL)

The block diagram of the DLL is shown in Fig. 9, which comprises of bang-bang phase frequency detector (BB-PFD), low-pass filter (LPF), digital-to-analog converter (DAC) and delay line. The details of the BB-PFD and LPF will be discussed in details in Chapter 6. To illustrate the operation principle of the DLL, first assume there is zero delay generated by the delay line. Therefore, the CLK_{FB} will be simply the inverted signal of CLK_{ref} as shown by the waveform of CLK_{FB0} in Fig. 9 (b). In reality, because of the delay of the delay line, the rising edge of the CLK_{FB0} should be later than what it is shown in Fig. 9 (b).

The BB-PFD is not only able to detect the frequency difference, but it is also capable of detecting the phase difference. Therefore, the DAC will try to decrease its output current I_{tail} to bring the rising edge of CLK_{FB0} to the rising edge of CLK_{FB} as shown in Fig. 9 (b). When the DLL is in lock, the delay generated by the delay line is $0.25T_S$.



(a) Block Diagram of the DLL



(b) Operation Principle of the DLL

Fig. 9 DLL Block Diagram and Operational Principle.

For the multi-phase buck converter, the switching frequency for each phase is f_{SW}. Therefore, if the switching signal of V_{LX1} is the input of the delay line, the phase delay between the input and output signal of the delay line can be calculated as:

$$PhaseDelay = \frac{0.25 \times T_S}{T_S} \times 360° = 90° \tag{13}$$

Therefore, by feeding the DLL block with a $2*f_{SW}$ signal as its clock reference, it will generate the proper current for the delay line to provide a 90° phase shift for the requirement of the phase synchronization operation.

C. Phase Shedding

Multi-phase operation is one of the effective ways to improve the power efficiency performance at heavy load conditions. However, when the load becomes lighter and lighter the switching loss will become dominant. And if the buck converter is always working at the multi-phase operation mode, the power efficiency will be very bad at light load conditions. To achieve high power efficiency across all load conditions, the multi-phase buck converter will shut down all three slave phases and the duty cycle calibrated delay line to reduce the switching loss.

CHAPTER 5 OPERATION PRINCIPLE AND CIRCUITS OF CURRENT SHARING TOPOLOGY

To achieve highest power efficiency at multi-phase operation, accurate current sharing is required as shown by Eq. (12). Also from the reliability point of view, it is also not desired to assign the entire load current just to one phase. Instead, equally distributing the load current among each phase will prolong the life time of the DC-DC converter ICs. The proposed current sharing topology is shown in Fig. 6, where the duty cycle of the three slave phases are calibrated by the duty cycle calibrated delay line. The proposed current sharing topology is designed based on the delay line which has been discussed in details in Chapter 5.

As shown in Fig. 10, each sub delay line has been designed into two parts, the raw part and the fine part. The raw part is mainly designed to implement the dominant delay which is needed for the 90° phase synchronization requirement of each slave phase, while the fine part is designed for calibrating the duty cycle for the three slave phases. The raw part and the fine part are both comprised of a series of the current-starved inverters whose tail current is calibrated by the DLL as discussed in Chapter 5. The only difference between the raw part and the fine part is the capacitance inside the current starved inverter. The raw part has a much larger capacitor compared with the fine part so that most of the delay is implemented by the raw part. A small capacitor is chosen inside the fine part to improve the current sharing accuracy when the current sharing loop reaches to its steady state.

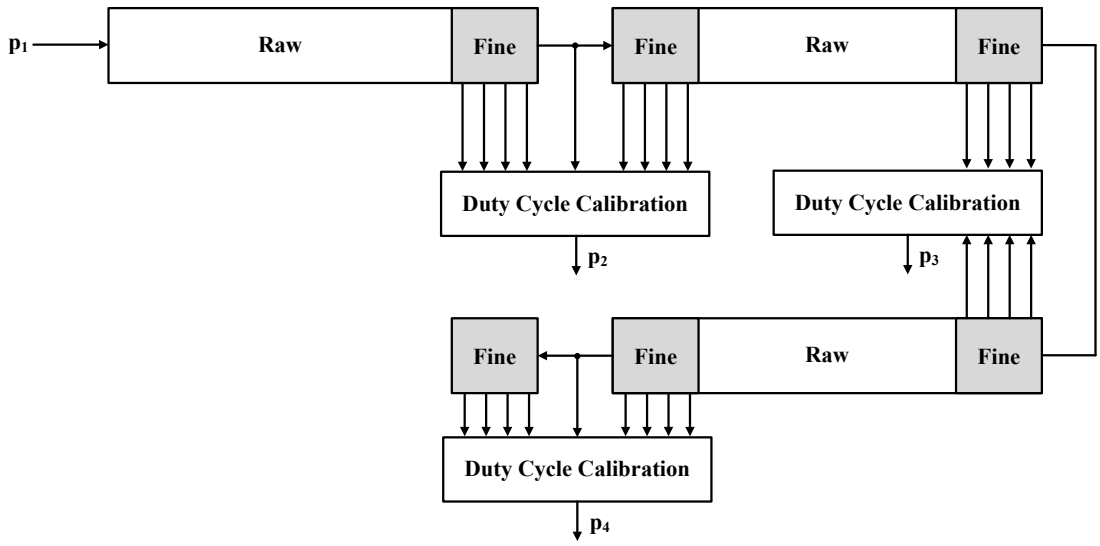
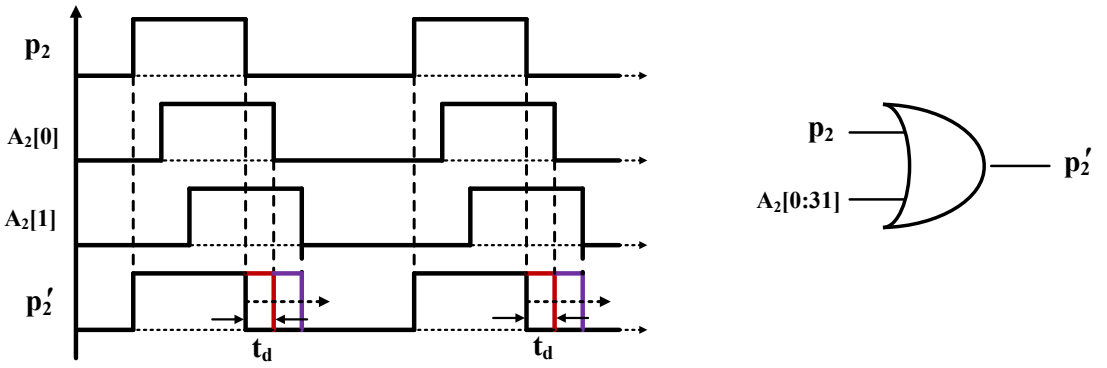
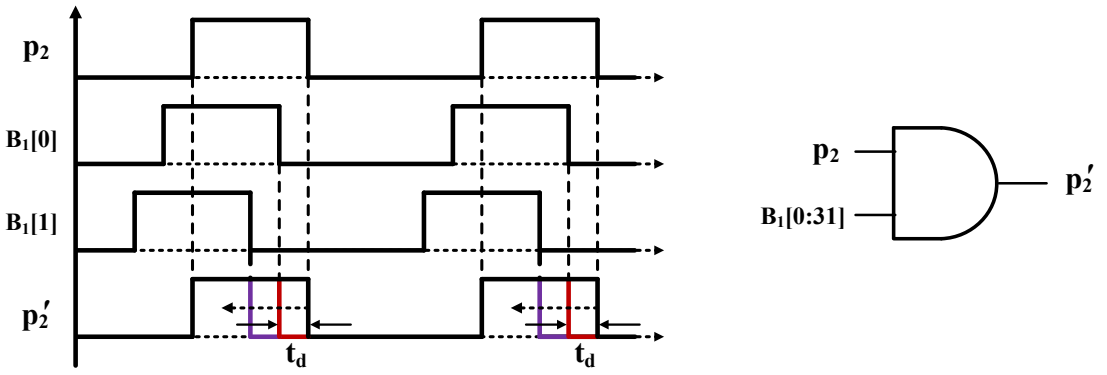


Fig. 10 Operation Principle of the Duty Cycle Calibrated Delay Line.

Fig. 11 shows the operation principle of the digital duty cycle calibration. An AND gate can be used as a duty cycle substractor as shown in Fig. 11 (a) and an OR gate can be designed to be a duty cycle adder as shown in Fig. 11 (b). For example, assuming the average inductor current of the second phase is lower than the master phase, the duty cycle of the second phase (p_2) should be reduced. To reduce the duty cycle of p_2, a group of delayed signals ($A_2[0:31]$) of p_2 is needed as shown in Fig. 11 (a). By passing one of the signals from $A_2[0:31]$ and p_2 through an OR gate, the duty cycle of p_2 is increased so that the average current of the second phase also gets increased. Notice that increasing the duty cycle of p_2 does not affect the phase synchronization because the rising edge of p_2 does not change after its duty cycle gets calibrated. Therefore, the current sharing topology is able to calibrate the duty cycle of the three slave phases without affecting the phase synchronization guaranteed by the DLL.



(a) Duty Cycle Addition



(b) Duty Cycle Subtraction

Fig. 11 Operation Principle of the Digital Duty Cycle Calibration.

The same also holds true for the duty cycle subtraction operation. A group of early signals of p_2 is needed for duty cycle addition. For example, if the average current of the second phase is higher than the master phase, the duty cycle of p_2 should be decreased. By passing one of the signals from $B_1[0:31]$ and p_2 through an OR gate, the duty cycle of the original p_2 is decreased so that the average current of the second phase also gets decreased. Notice that the phase subtraction operation does not affect the rising edge of the original p_2 signal. Therefore the phase synchronization still holds true while the duty cycle subtraction is performed.

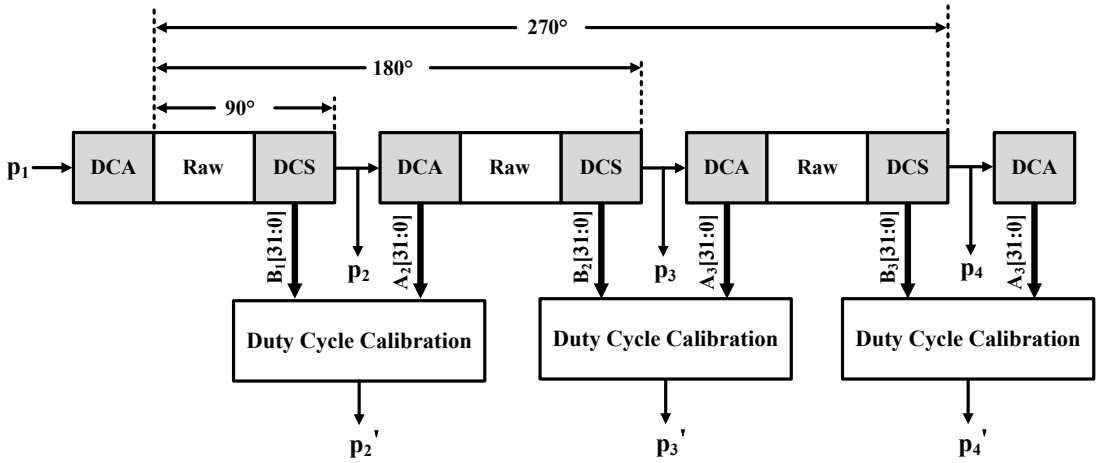
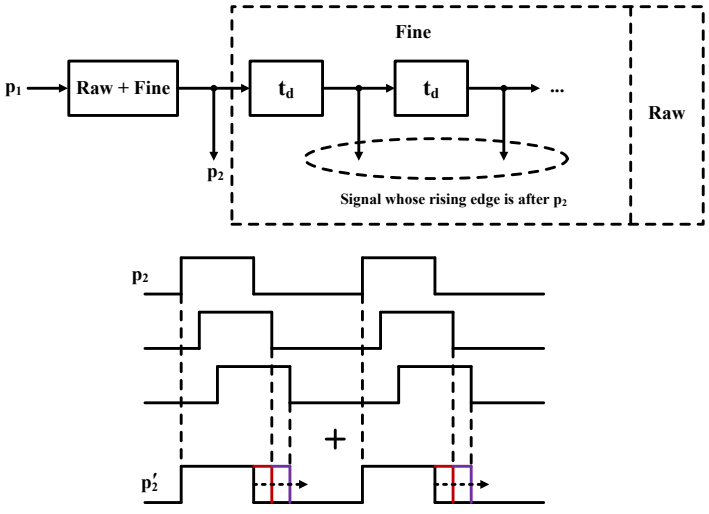
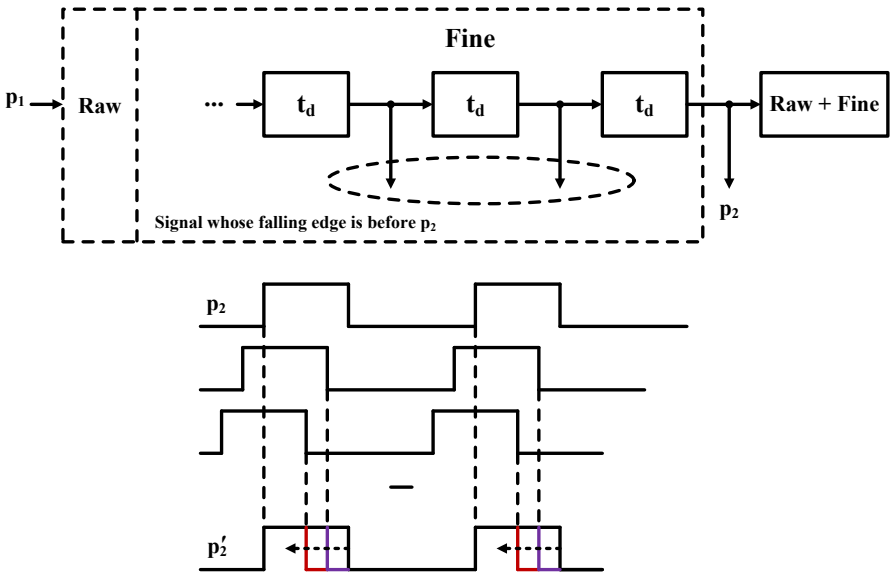


Fig. 12 A More Detailed Block Diagram of the Duty Cycle Calibrated Delay Line.

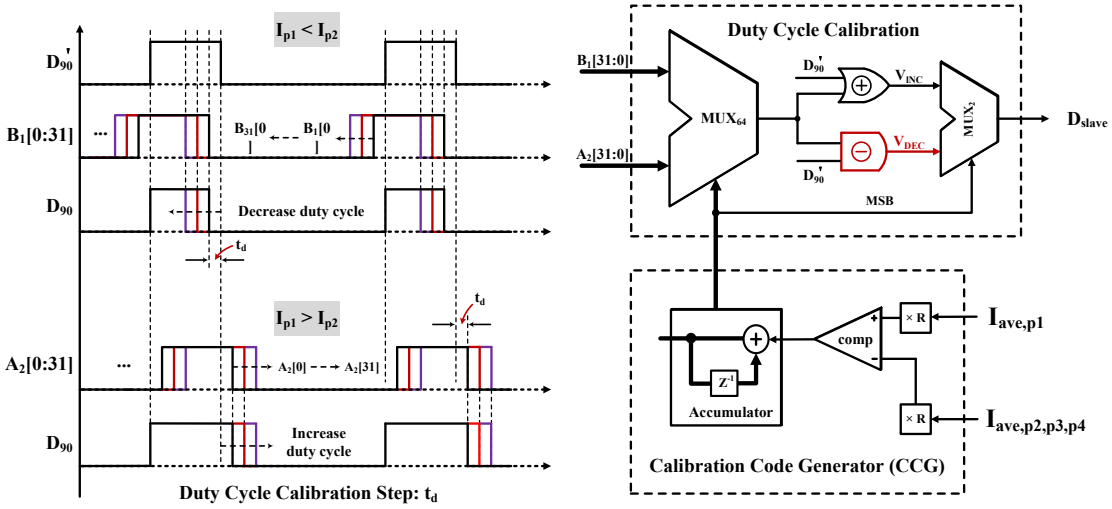
Based on the discussion above, a more detailed block diagram of the duty cycle calibrated delay line is shown in Fig. 12, where each sub delay line is comprised of a duty cycle addition (DCA) block for increasing the duty cycle, raw part for implementing most of the delay for the purpose of 90° phase synchronization and a duty cycle subtraction (DCS) block for decreasing the duty cycle. Each DCA and DCS block has a 5-bit output for either increasing the duty cycle or decreasing the duty cycle. The current sharing loop and its operational principle are shown in Fig. 13.



(a) Duty Cycle Addition for P2



(b) Duty Cycle Subtraction for P2

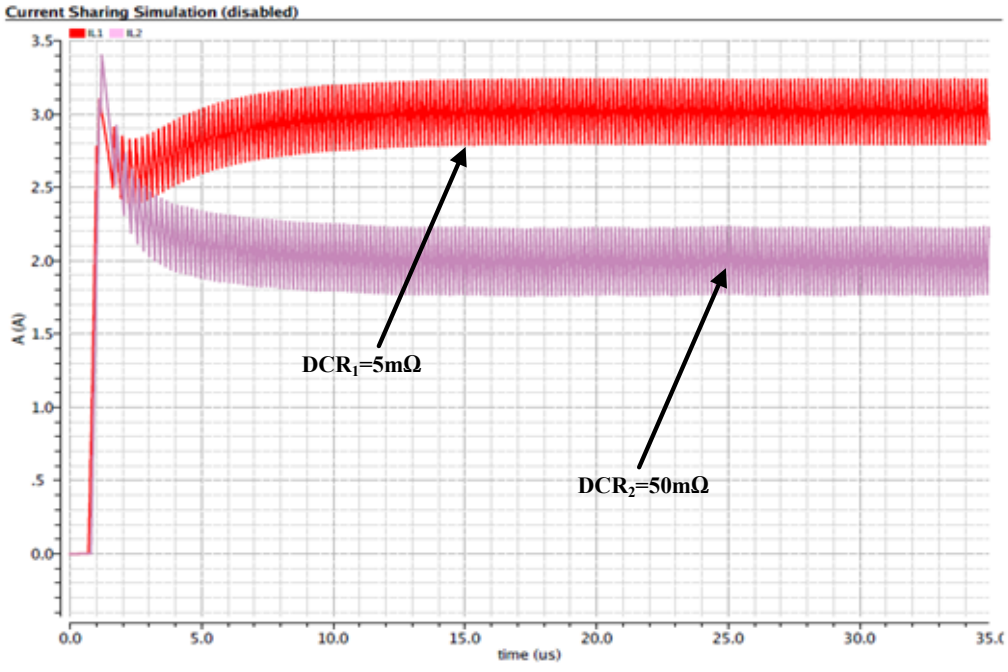


(c) Duty Cycle Calibration Operation Principle

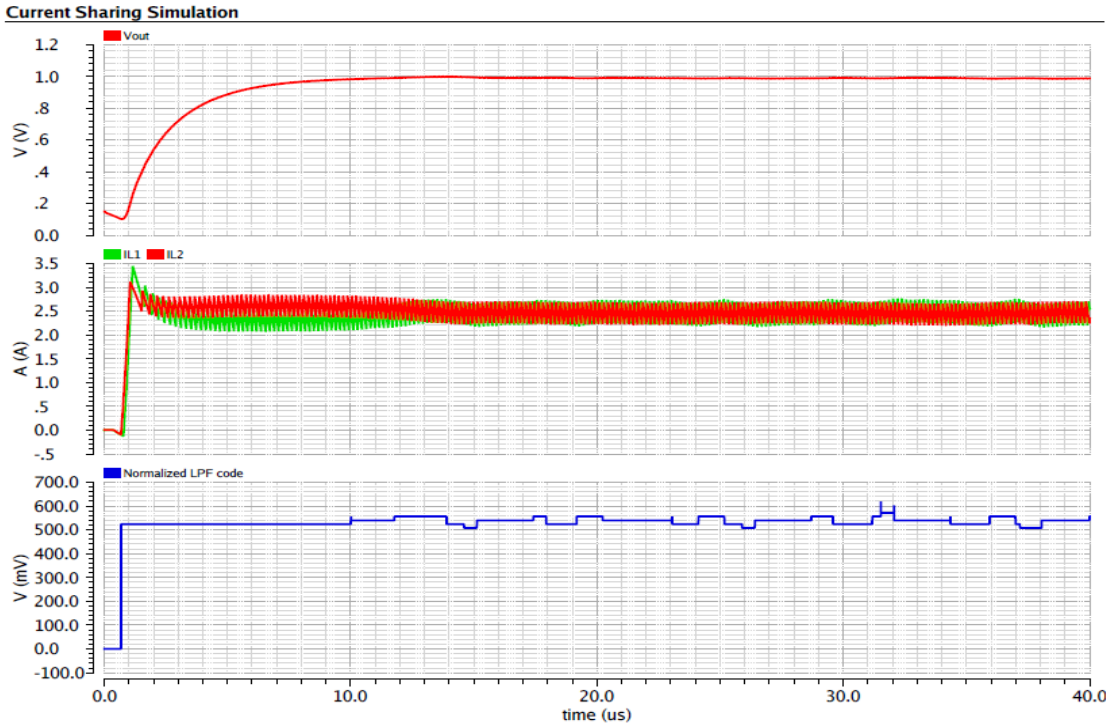
Fig. 13 Duty cycle Calibration Operation Principle.

Assuming second phase current I_{p2} is larger than first phase current I_{p1}, MUX_{64} in Fig. 13 (c) will choose $B_1[0]$ and MUX_2 will choose V_{DEC} as their outputs. Then, an AND gate is used to decrease the second stage duty cycle (phase-2) by the amount of t_d/T_S. After duty cycle signal is reduced for the second phase, if I_{p2} is still larger than I_{p1} for the

next several clock cycles, $B_1[1]$ is chosen to decrease the duty cycle further by the amount of t_d/T_S. This process will continue until I_{p1} is equal to I_{p2}. On the other hand, if I_{p2} is smaller than I_{p1}, MUX_{64} will select one of the signals from $A_2[31:0]$ and MUX_2 will select V_{INC} as its output. In this case, an OR gate is used to increase the phase-2 duty cycle by the amount determined by the CCG's output. Notice for both the duty cycle addition and subtraction operation, the rising edge of the original signal does not change while its duty cycle is being modulated. Therefore, the phase synchronization is not affected by the duty cycle calibration operation. The same procedure can be applied on the remaining slave phases to ensure the accurate current sharing among phases.



(a) Current Sharing Topology is Disabled



(b) Current Sharing Topology is Enabled

Fig. 14 Simulation Results of the Current Sharing Topology for DCR_1=5mΩ and DCR_2=50mΩ.

Fig. 14 shows the simulation results of the proposed current sharing topology, where V_{out} is the output voltage of the 4-phase hysteretic controlled buck converter, I_{L1} is the inductor current of the master phase, I_{L2} is the inductor current of the second phase and the blue curve is the normalized digital code of the accumulator inside the current sharing loop. The inductor DC resistance (DCR) for the master phase is 5mΩ and the DCR for the second phase is 50mΩ. From Fig. 14 (a), when the current sharing topology is disabled, there is about 50% mismatch between the average inductor current for master phase and the slave phase even if there is only 45mΩ resistance mismatch on the power path. When the current sharing topology is enabled, the average current of I_{L1} and I_{L2} is almost the same when the current sharing loop reaches to its steady state. When the

steady states reaches, the digital code of the accumulator will toggle by 1 LSB as shown in Fig. 14 (b).

CHAPTER 6 OPERATION PRINCIPLE AND CIRCUITS OF THE DIGITAL FREQUENCY SYNCHRONIZATION

Hysteretic control has already been widely used to improve the DC-DC converter's power efficiency at the light conditions in the industry. For example, when the hysteretic control is enabled at the light conditions, the switching frequency of the DC-DC converter may be as low as several hundreds of Hz. Since the switching loss is dominant at the light load conditions, hysteretic control will greatly increase the power efficiency and prolong the battery life.

Another benefit of the hysteretic control is the fast transient response compared with the traditional pulse width modulation (PWM). PWM control is linearized control and a PID compensator is usually needed. For example, voltage-mode PWM control usually requires a type III compensator and peak-current-mode PWM control usually requires a type II compensator. In either case, several bulky capacitors are needed to design the compensator network and provide sufficient phase margin to stabilize the control loop. Therefore, once a load transient happens, the error amplifier (EA) needs to provide a large amount of current to change the voltage value across the capacitors which takes very long response time. For the hysteretic control, there is no need for the compensation network because it is inherently stable. Therefore, the transient response is much faster for the hysteretic control compared with the PWM control topology.

One of the drawbacks of the hysteretic control is that the switching frequency of the hysteretic controlled DC-DC converters is highly dependent on the external device parasitics, such as ESR of the decoupling capacitor, comparator delay, driver delay, and the hysteresis voltage. Different input and output conditions also have a big impact on the

switching frequency [22]. In mobile and automotive applications, EMI protection is very important and the variable switching frequency is a design problem for the hysteretic control.

A. Operational Principle of the Master Phase for the Proposed 4-phase Buck Converter

The block diagram of the master phase for the proposed 4-phase buck converter is shown in Fig. 15.

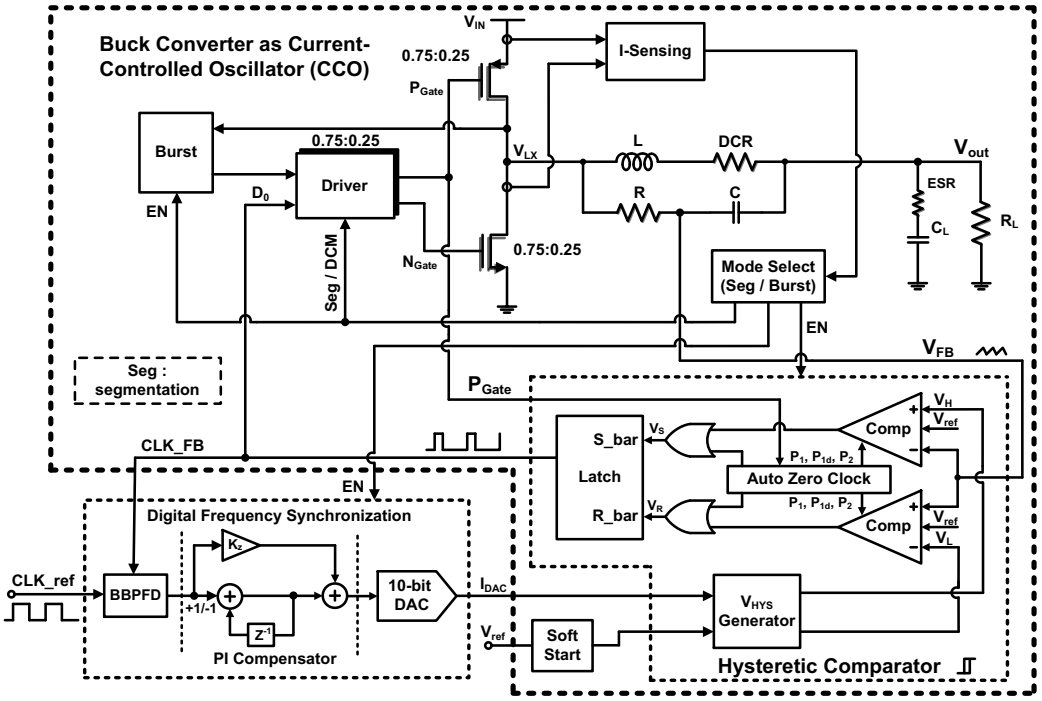


Fig. 15 Block Diagram of the Master Phase for the Proposed 4-phase Buck Converter.

High-side power FET is PMOS and low-side power FET is NMOS. To prevent the shoot-through current, a driver with the break-before-make (BBM) function is designed. Both the driver and the power FETs are segmented with the ratio of 3:1. When the load current is less than the pre-defined current threshold value, 75% of the driver and the power FETs will be turned off to decrease the gate drive loss and the switching loss. To

further boost the power efficiency performance in light load conditions, a burst mode is designed. During the burst mode, the voltage on the V_{LX} node is monitored. Once the V_{LX} node is higher than the zero voltage when the low-side NMOS is turned on, reverse inductor current will happen. At this moment, the low-side NMOS is turned off and let the out voltage droops by the load current.

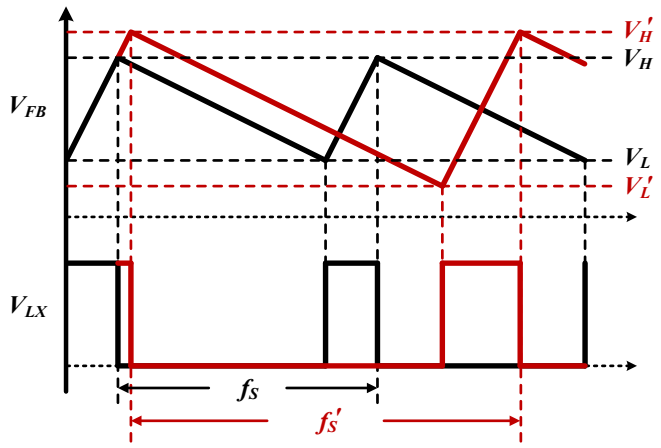
As mentioned in Chapter 2, the resistor and the capacitor in parallel with the inductor do not to need to match the time constants of L and its DCR. Instead the resistor and the capacitor network is only used to provide the voltage ripple necessary for the hysteretic comparator to work. To overcome the variable switching frequency of the hysteretic buck converter, a digital frequency synchronization loop is designed to stabilize the switching frequency, which be explained in details in section B.

As shown in Fig. 15, the hysteretic comparator comprises two sub comparators so that the hysteresis window is precisely defined. To remove the input referred offset of the hysteretic comparator, an online auto zero topology is designed which will be discussed in details in Chapter 7. A soft start function is also designed to prevent the inrush current during the startup of the buck converter.

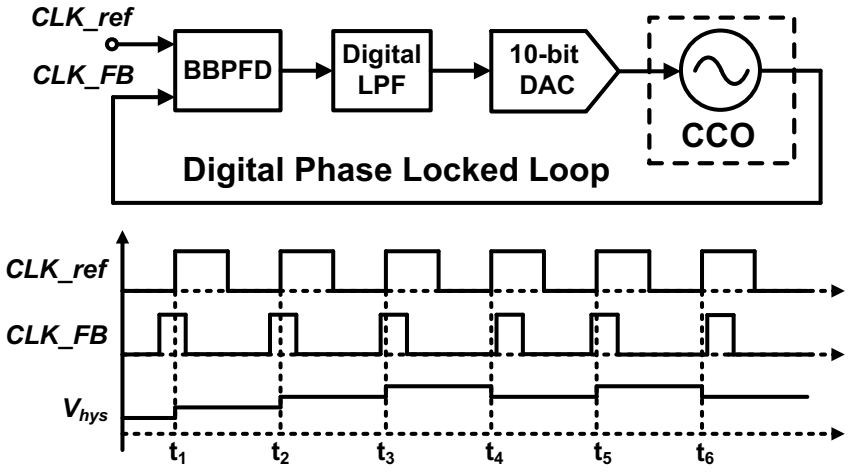
B. Operation Principle of the Digital Frequency Synchronization Scheme

From (8), To stabilize the switching frequency, one can use the digital-controlled delay line (DCDL) to adjust the propagation delay τ_D [23] or use a feedback resistor array in parallel with the inductor to tune the RC time constants τ_{RC} [19]. In this work, as a frequency control parameter, the hysteresis window V_{hys} of the comparator is tuned digitally by a 10-bit current-steering DAC. Wide hysteresis window will result in a slow

switching frequency, while a narrow hysteresis window will produce a fast switching frequency, as shown in Fig. 16 (a).



(a) Switching Frequency vs. Hysteresis Window



(b) Frequency Synchronization Loop and Operation Principle

Fig. 16 Frequency Synchronization Operation Principle.

By considering the buck converter as a current-controlled oscillator (CCO) as shown in Fig. 16 (b), the digital frequency synchronization (DFS) loop can be represented by a digital PLL (DPLL). The DPLL is comprised of a bang-bang PFD (BB-PFD) whose output is either logic high or logic low depending on the phase error, a digital PI

compensator as the low-pass filter to stabilize the DFS loop, a current-steering DAC and the CCO. The switching frequency (f_{SW}) will be locked to the desired input reference clock (f_{ref}) when the DPLL reaches steady state operation. Assuming f_{SW} is faster than f_{ref} as shown in Fig. 16 (b), the BB-PFD's output triggers a logic high, resulting in the digital code of the accumulator increment by one at each clock period. As a result, the DAC current increases and the hysteresis window is widened, slowing down f_{SW} during transitions [t_1-t_3] until it is locked to the desired f_{ref}, as shown in transitions [t_4-t_6].

C. DFS Loop Stability

The s-domain small signal model of the DFS loop is shown in Fig. 17, which can be used to derive the phase margin of the loop. By modeling the behavior of the BB-PFD and using the Markov chain theory, the gain of the BB-PFD can be expressed as [24], [25]:

$$K_{BB-PFD} \approx \frac{1}{\sqrt{2\pi}\sigma_j} \tag{14}$$

where σ_j is the rms jitter on the reference clock.

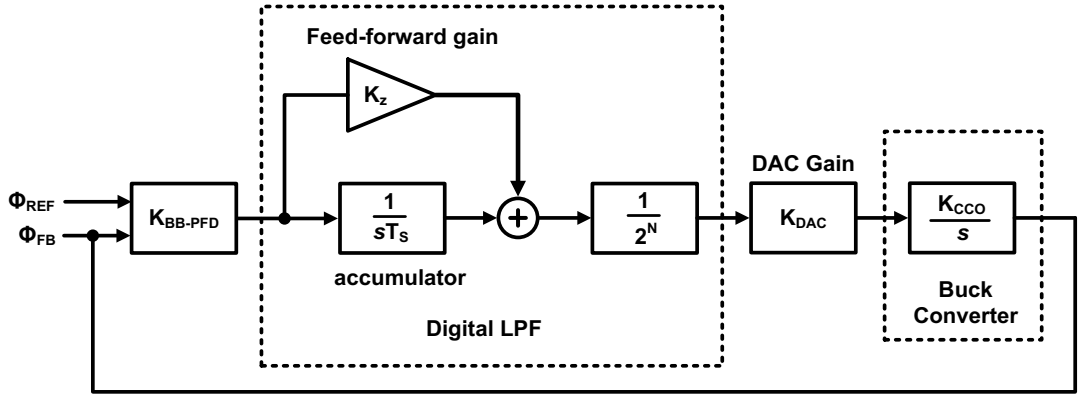


Fig. 17 S-domain Small-signal Model of the Digital Frequency Synchronization Loop.

The transfer function of the accumulator can be written as $1/sT_S$ and then normalized by 2^N, where N is the number of bits of the digital phase accumulator. The current-

steering DAC is following the digital low-pass filter which transforms the digital code into the current domain to tune the switching frequency of the buck converter. The gain of the DAC (K_{DAC}) is equal to its full-scale current output.

K_{CCO} represents the gain from the DAC's output current to f_{SW}, which can be expressed as:

$$K_{CCO} = \frac{\partial f_{SW}}{\partial I_{DAC}} = \frac{\partial f_{SW}}{\partial V_{hys}} \times \frac{\partial V_{hys}}{\partial I_{DAC}} \tag{15}$$

where I_{DAC} is DAC's output current. By using (8), small-signal gain from the hysteresis window to f_{SW} can be calculated as:

$$\frac{\partial V_{hys}}{\partial f_{SW}} = -\frac{D \times (1-D)}{\tau_{RC} f_{REF}^2} \cdot V_{IN} \tag{16}$$

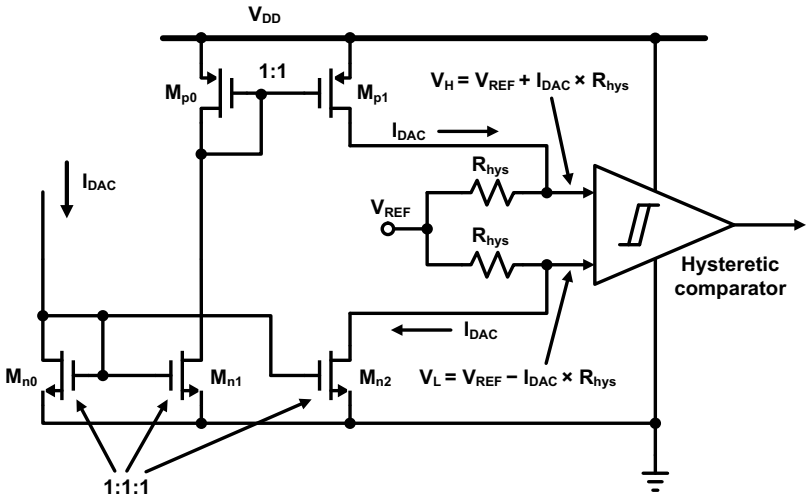


Fig. 18 Simplified Schematic of the Hysteresis Window Generator Block.

To analyze the gain from I_{DAC} to V_{hys}, a simplified schematic of the hysteresis window generator is shown in Fig. 18. The DAC's output current I_{DAC} has been mirrored to a current source which generates the upper hysteresis level V_H ($V_{REF} + I_{DAC} \times R_{hys}$) and a

current sink which produces the lower hysteresis level V_L ($V_{REF} - I_{DAC} \times R_{hys}$). Therefore, the hysteresis window V_{hys} can be calculated as:

$$V_{hys} = V_H - V_L = 2I_{DAC} \times R_{hys} \tag{17}$$

And the gain from the I_{DAC} to V_{hys} can be expressed as:

$$\frac{\partial V_{hys}}{\partial I_{DAC}} = 2R_{hys} \tag{18}$$

Substituting (16) and (18) into (15), K_{CCO} is given by:

$$K_{CCO} = \frac{\partial f_{SW}}{\partial V_{hys}} \times \frac{\partial V_{hys}}{\partial I_{DAC}} = -\frac{\tau_{RC} f_{REF}^2}{V_{IN} \times D \times (1-D)} \cdot 2R_{hys} \tag{19}$$

By breaking the DFS loop and inject a small signal perturbation, the open-loop transfer function TF_{DFS} is:

$$TF_{DFS} = \frac{K_{BB-PFD} \cdot \left(K_Z + \frac{1}{sT_S} \right)}{2^N} \cdot K_{DAC} \cdot \frac{K_{CCO}}{s} \tag{20}$$

A digital PI compensator is used to stabilize the DPLL loop and provide sufficient phase margin for the PLL. From phase margin and stability perspective, large K_z is preferred because it will generate a low frequency zero. However, large K_z will result in large cycle-to-cycle jitter and will degrade steady state frequency synchronization accuracy. For example, once the DPLL reaches to the steady state, the BB-PFD's output will toggle between logic high and logic low. The input code variation of the current steering DAC can be expressed as:

$$\Delta N = N[n+1] - N[n] = 2K_z + 2 \tag{21}$$

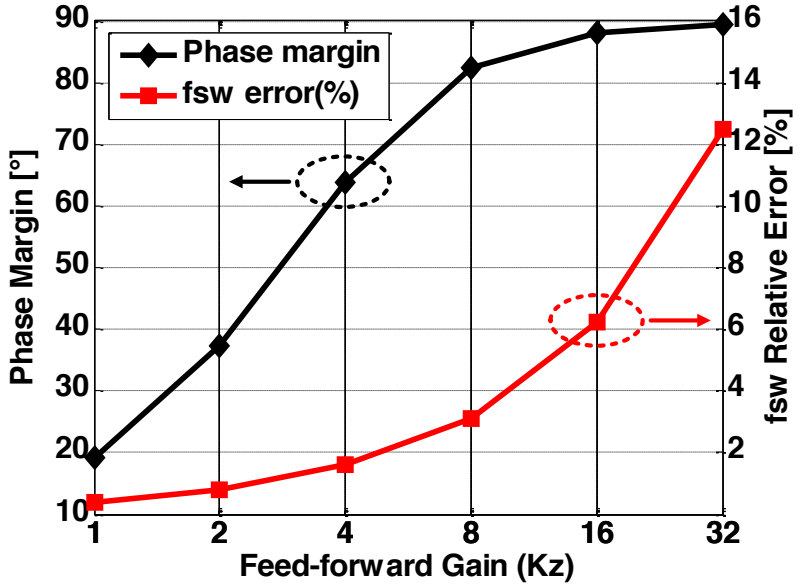


Fig. 19 Phase Margin of the Digital Frequency Synchronization Loop and Switching Frequency Relative Error Versus Feed-forward Gain Kz.

Assuming K_z equals to 4, the code variation among each cycle will be 10 which is 3.3 bits. Therefore the best switching frequency accuracy can be achieved is $1/2^{10-4} \approx 1.6\%$. Fig. 19 shows the simulation results of the phase margin and frequency relative error under different K_z conditions. $K_z = 4$ or $K_z = 8$ is a good candidate for the feed-forward gain to stabilize the DFS loop while providing accurate f_{sw}.

D. DFS Loop Dynamic Range

The dynamic range of the DFS loop is determined by the 10-bit current steering DAC and the loop delay. The maximum output current ability of the current-steering DAC determines how slow the buck converter can be synchronized to the input clock reference. Based on (8), large hysteresis window will result in a slow switching frequency and a small hysteresis window will result in a fast switching frequency. Therefore, to slow

down the buck converter, the lowest switching frequency can be achieved when the DAC's output current reaches to its full scale current.

On the other hand, the maximum switching frequency of the buck converter can be achieved when the DAC's output current is almost zero. Under this condition maximum switching frequency can be further increased by decreasing the time constants τ_{RC} in (8).

To make a conclusion, to achieve lower switching frequency which can be synchronized, one can increase the full scale current of the current-steering DAC. And to obtain higher switching frequency which can be synchronized, one can decrease the time constants of the resistor and the capacitor in parallel with the inductor.

CHAPTER 7 OPERATION PRINCIPLE AND CIRCUITS OF THE ONLINE AUTO ZERO CALIBRATION

One drawback of the quasi-current-mode control is that the feedback loop is closed from the feedback node, rather than the regulator output voltage V_{OUT}. Due to this, there is a DC voltage mismatch between V_{REF} and V_{OUT}, which can be represented by:

$$\Delta V = I_L \times DCR \tag{22}$$

where I_L is the DC current of the inductor. To remove DCR induced output voltage error (DCR-IE), one of the hysteretic comparator's inputs can be connected to buck converter's output during each switching period as proposed in [19]. However, while the DCR-IE reduces linearly with the load current, the hysteretic comparator offset-induced error remains constant. To avoid the conduction loss on the power path, an inductor with maximum 5mΩ DCR is used in this design. Fig. 20 shows relative output error comparison for DCR of 5mΩ and output voltage of 0.8V, with a hysteretic comparator input referred offset of 30mV. For load current less than 6A, dominant error source is offset-induced error. Considering that the maximum load current is 6A for this application, the offset-induced error should be removed.

Auto zero has been proved to be one of the most effective ways to remove the input-referred offset for both OTA and Op-Amp. Besides auto zero technique, correlated double sampling (CDS) and chopper are also able to remove the input-referred offset. Considering the minimum output voltage is 0.8V and 1% output voltage regulation error, the minimum offset needed to be removed is $0.8 \times 1\% = 8mV$. Therefore, auto zero is sufficient to remove the required offset specs without using the complicated CDS or chopper technique.

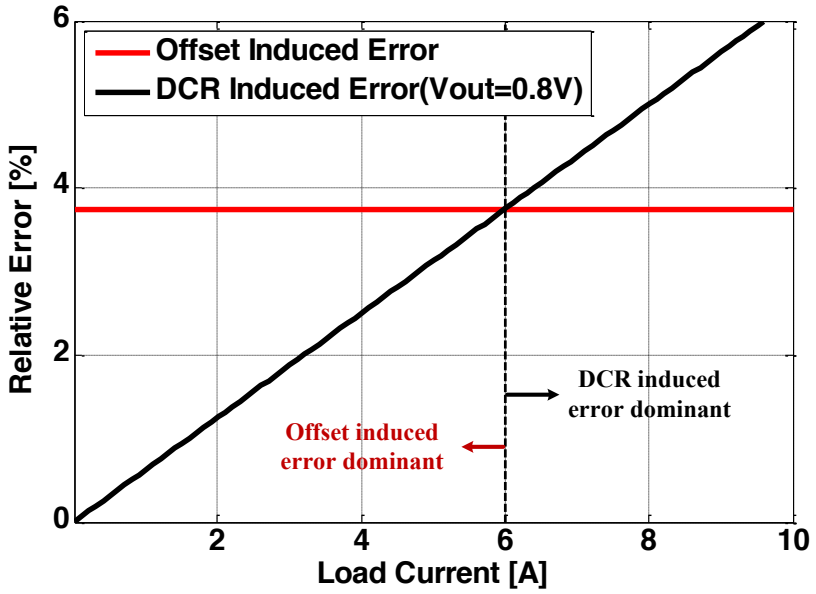
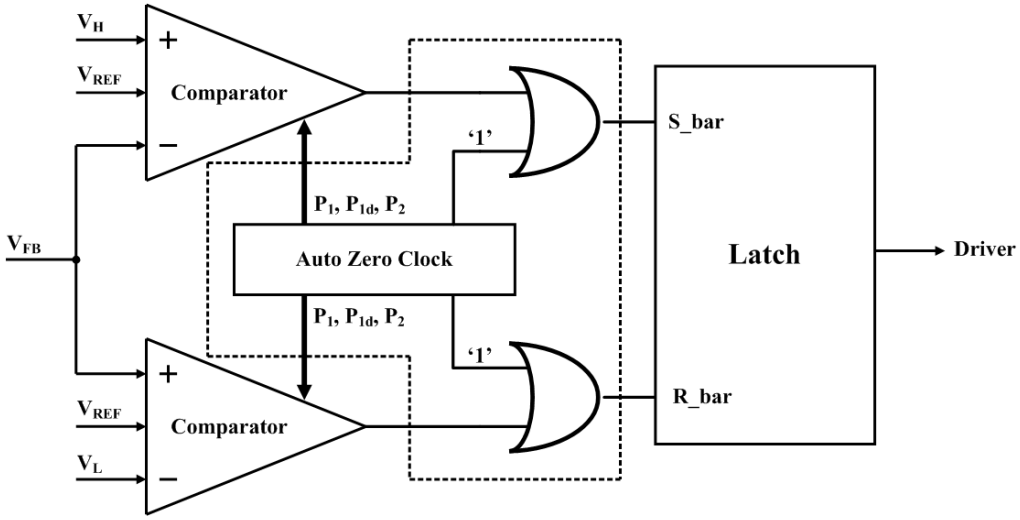


Fig. 20 Comparison of DCR Induced Error and Offset Induced Error for V_{OUT}=0.8V, DCR=5mΩ and V_{offset}=30mV.

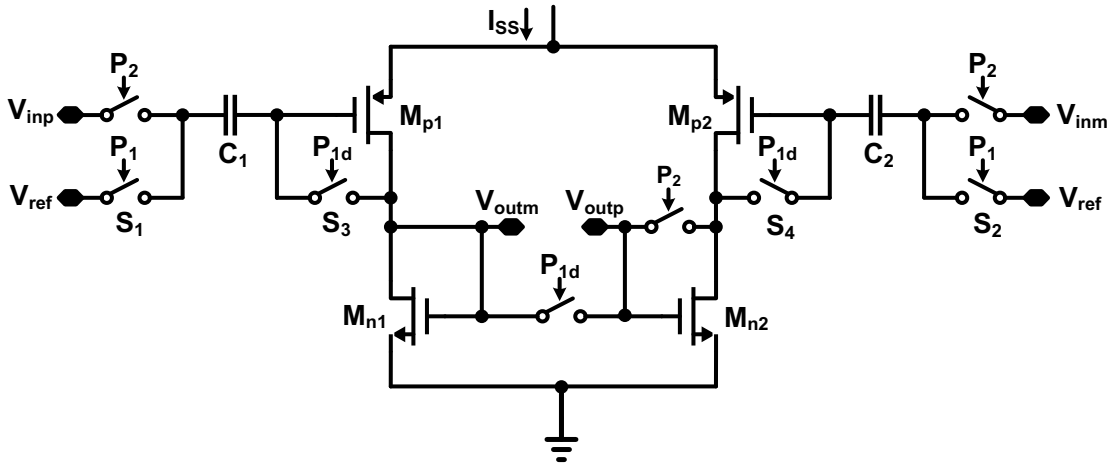
The hysteretic comparator consists of two sub comparators as shown in Fig. 15, each including a pre-amp and an OTA-based second stage. A RS latch follows the two sub comparators as shown in Fig. 21 (a). The hysteresis window is determined by the V_H and V_L, which are generated by the hysteresis window generator as shown in Fig. 18. The current information generated by the 10-bit current steering DAC is used to generate the hysteresis window. The current generated by the 10-bit DAC is mirrored into a current sink and a current source. The current sink is dedicated for producing the lower hysteresis window V_L and the current source is used for generating the upper hysteresis window V_H. The hysteresis window is then defined by the $V_H - V_L$.

Since the offset of the second stage will be suppressed by the gain of the pre-amp, the comparator pre-amp dominates the input-referred offset. Therefore, in this work, only the input referred offset of the pre-amp is removed by the online auto-zeroing topology.

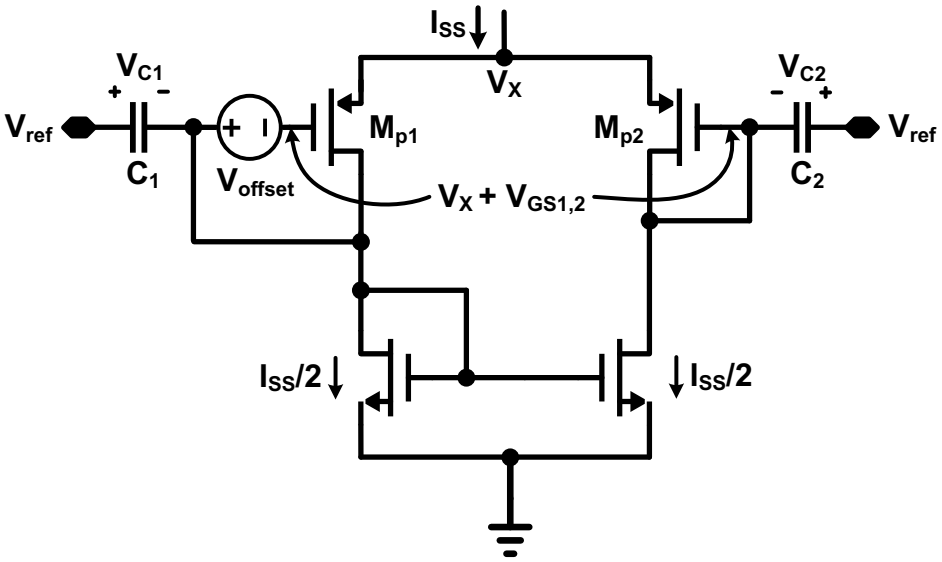
Fig. 21 (a) also shows the auto zero clock generator which is designed for generating the non-overlapping clock for the online auto zero topology to prevent shoot-through and charge leakage. Because of the nature of the RS-latch, the two sub comparators in Fig. 21 (a) are only used around the point where V_H and V_L is equal to V_{FB}. Therefore, the online auto zero topology can be implemented when the two sub comparators are not needed by the DC-DC converters. For POL applications, 1-D time period is larger than the D time period, where D is the duty cycle of the DC-DC converters, the online auto zero topology is chosen to be implemented during the 1-D time period.



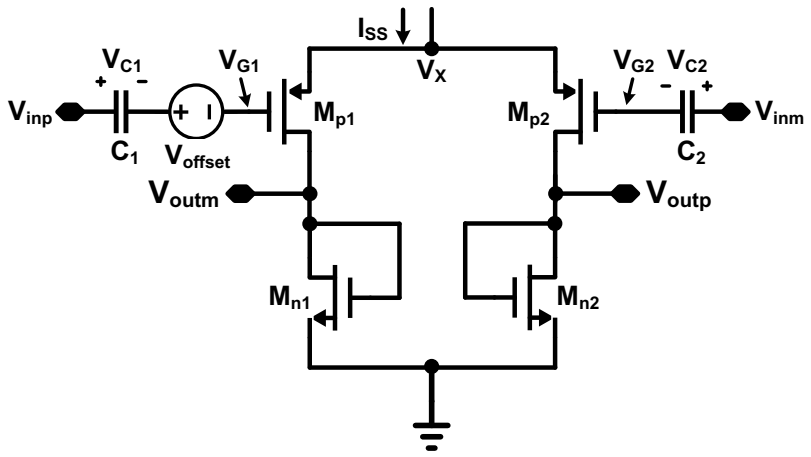
(a) Hysteresis Comparator of the Buck Converter



(b) Hysteretic Comparator Pre-amp



(c) Sampling Phase



(d) Settling Phase

Fig. 21 Pre-amp Circuits and Online Auto-zeroing Based Offset Calibration Principle.

Fig. 21 (b) shows the structure of the auto-zeroed pre-amp. The input referred offset will be sampled on capacitor C_1 and C_2 during the sampling phase by connecting V_{ref} to C_1 and C_2 respectively. As shown in Fig. 21 (c), during the sampling phase, M_{n1} and M_{n2} form a current mirror to ensure equal current flowing through M_{p1} and M_{p2}. The same gate-to-source voltage ($V_{GS1,2}$) is obtained and the voltage on C_1 and C_2, which can be expressed as:

$$\begin{cases} V_{C1} = V_{ref} - \left(V_X + V_{GS1,2} + V_{offset}\right) \\ V_{C2} = V_{ref} - V_X - V_{GS1,2} \end{cases} \tag{23}$$

The input-referred offset voltage will be stored on capacitor C_1 and C_2:

$$V_{C1} - V_{C2} = V_{ref} - \left(V_X + V_{GS1,2} + V_{offset}\right) - \left(V_{ref} - V_X - V_{GS1,2}\right) = -V_{offset} \tag{24}$$

During the settling phase, M_{n1} and M_{n2} form a diode-connected device instead of a current mirror to provide the gain for the pre-amp. The gate voltage difference of M_{p1} and M_{p2} is given by:

$$V_{G1} - V_{G2} = V_{inp} - V_{C1} - V_{offset} - \left(V_{inm} - V_{C2}\right) = V_{inp} - V_{inm} \tag{25}$$

Therefore, the input-referred offset is cancelled during the settling phase.

For applications where the input referred offset does not change, the offset can be measured during the startup and be held by a buffer afterwards. However, this project is targeted for the space applications, where the threshold voltage of the NMOS and PMOS will shift because of the impact of the particles in space. For example, the threshold of either NMOS or PMOS might be changed as much as 30% of its original value by the impact of the space particles. Therefore, the input referred offset of the hysteresis comparator also changes, which requires an online calibration method to remove the input referred offset cycle by cycle. In this design, since the two sub comparators are only needed to be online around the point where V_H or V_L is equal to VFB, the online auto zero topology is chosen to be implemented during the 1-D time period as shown in Fig. 22.

In Fig. 22, P_1 is the sampling phase during which the input referred offset of the pre-amp is sampled on the capacitor C_1 and C_2 as shown in Fig. 21 (b). P_2 is the settling phase during which the input referred offset of the pre-amp is canceled. The details about how the online auto zero operates are explained below.

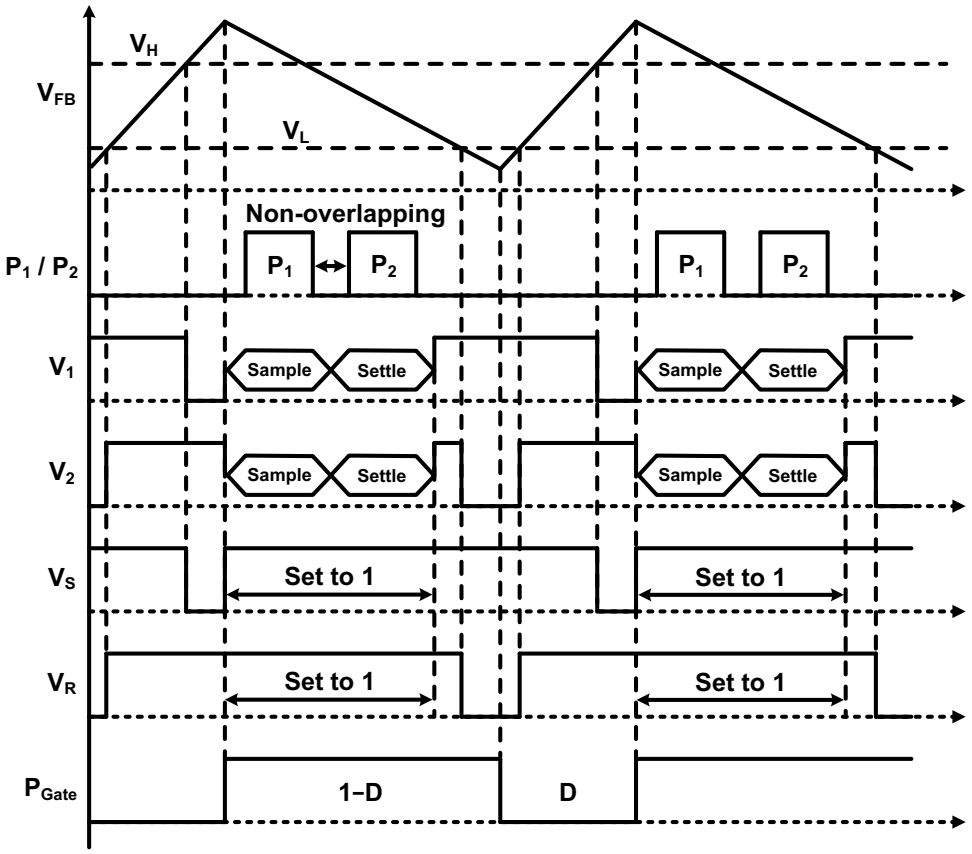


Fig. 22 Timing Sequence of the Online Auto-zeroing Based Offset Calibration.

Notice both sub comparators are only used around the time period when the feedback signal V_{FB} reaches V_H and V_L threshold point. The timing sequence of the sampling phase and the settling phase is shown in Fig. 22. A non-overlapping clock is designed for the auto-zeroing based offset calibration topology. Bottom-plate sampling is used to remove the charge injection errors when the switches S_1−S_4 are turned off. At the end of the sampling phase, S_1 and S_2 are turned off before S_3 and S_4 so that the charge injection caused by S_3 and S_4 cannot be injected to C_1 and C_2. Since the same voltage V_{ref} is connected to S_1 and S_2, an equal amount of charge will be injected on to capacitor C_1 and

C_2, which acts as a common-mode voltage and can be cancelled because of the differential operation of the pre-amp during the settling phase.

The two sub comparators of the hysteretic comparator are only used when V_{FB} triggers the hysteresis window V_H or V_L and their output state will be stored by the RS latch which follows the hysteretic comparator as shown in Fig. 6. For point-of-load applications, such as V_{IN}=5V and V_{OUT}=0.8V, the online offset cancellation is chosen to proceed during the 1-D time period as shown in Fig. 22. For applications where V_{OUT} is close to V_{IN} and time period D is longer than 1-D, the online offset cancellation can be implemented during the D time period instead.

Since V_{outp} and V_{outm} are shorted during the sampling phase, the input-referred offset of the comparator may trigger a logic low at the output. To avoid false triggering of the RS-Latch, two OR gates are used to set V_S and V_R to logic high respectively, during both the sampling and the settling phases as shown in Fig. 22.

CHAPTER 8 EXPERIMENTAL RESULTS

The proposed 4-phase hysteretic buck converter is designed and fabricated on a 5-level metal 0.18μm CMOS process with 5V thick gate oxide option for performance verifications. Fig. 23 shows the micrograph of the proposed 4-phase buck converter. The total effective area is about 12.5 mm^2 including all bonding pads. Over 70% of the total effective chip area is occupied by the power FETs and its driver to provide 80mΩ on-resistance of the high-side PMOS and 50mΩ on-resistance of the low-side NMOS for each phase. Over 60 pads are dedicated for the power supply, power ground and V_{LX} nodes for the purpose of high reliability and heavy load current conditions. Because of the large number of the bonding pads, LCC-84 with a 7.8mm by 7.8mm cavity is chosen as the 4-phase buck converter's package. Assuming a maximum 25% inductor current ripple, a 330nH Ferrite inductor is chosen to provide an exceptionally low DCR, which is less than 5mΩ.

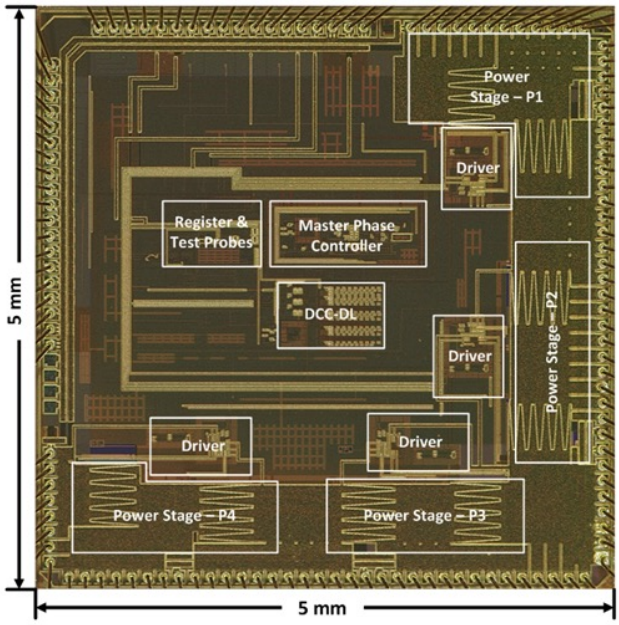
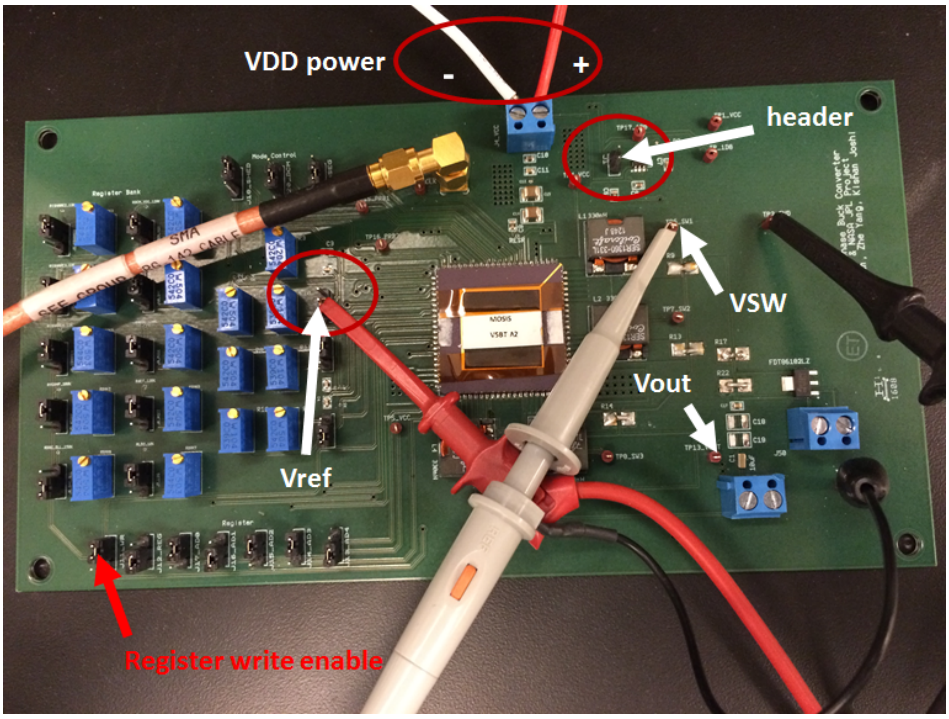


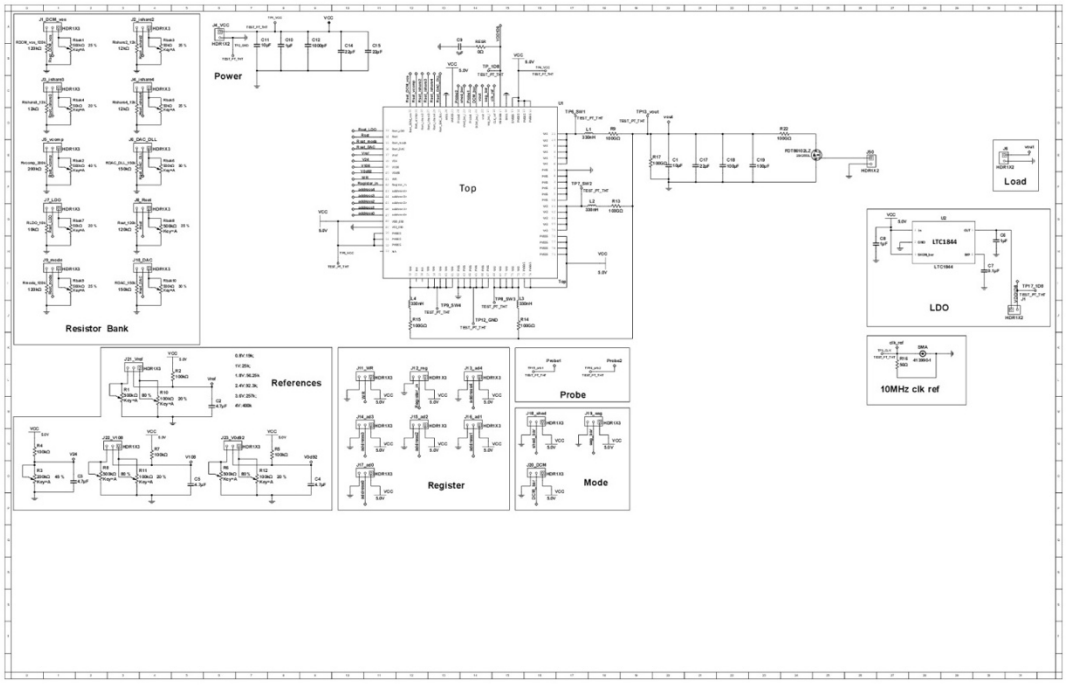
Fig. 23 Chip Micrograph of the Proposed 4-phase Buck Converter.

A. Test Bench

The fabricated chip was mounted to a double-sided FR4 PCB for characterization with ground as the top power plane and V_{CC} as the bottom power plane. The PCB specifications are listed in Table I and the board schematic is shown in Fig. 24 (b).



(a) PCB Test Bench for the 4-phase Buck Converter



(b) Schematic of the PCB

Fig. 24 PCB for the Testing of the Proposed 4-phase Hysteretic Buck Converter

Performance.

Table I

The PCB Specifications

Specs	Descriptions
Material type	FR4-Standard Tg 140C
Both sides	1.6mm
Minimum tracing/spacing	0.2mm
Copper weight	1oz
Layers	2 layer

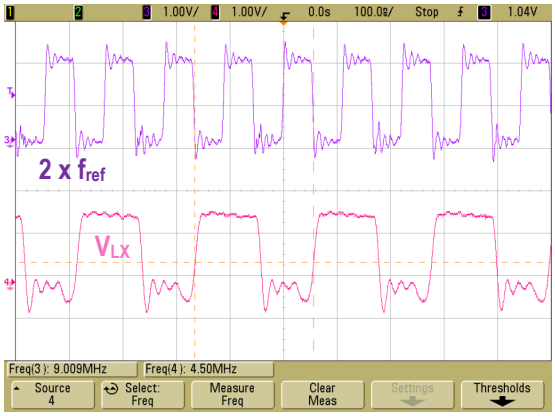
The maximum load current could be as high as 6A. Therefore, cautions are taken for the current density on the power bus and the ground bus. To avoid the interference between the power V_{CC} and the analog V_{CC}, Calvin connection is used to isolate the power V_{CC} and the analog V_{CC}. Also to avoid the switching noise from the power V_{CC} or the switching node V_{LX}, ground shielding is also used for the sensitive node, such as the feedback node V_{FB} as shown in Fig. 15.

An LDO is also designed on the board in case the internal LDO is not working. Also a lot of variable resistors are used to tune the current biasing in case the internal current bias is not accurate enough.

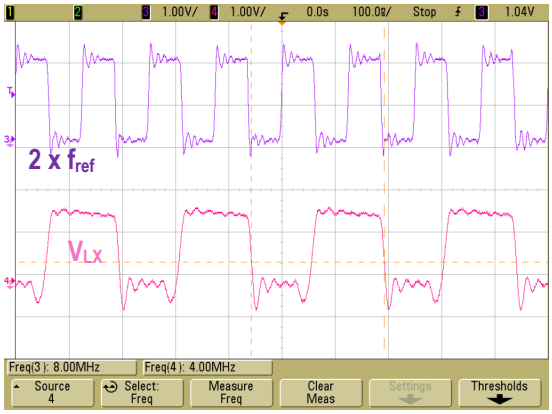
B. Measurement Results

Fig. 25 shows the waveform of the switching frequency under different input reference clock conditions for measuring the digital frequency synchronization (DFS) performance. The input reference clock is divided by two and fed to the BB-PFD for the purpose of comparing with f_{sw}. The dynamic range of the DFS is determined by the current-steering

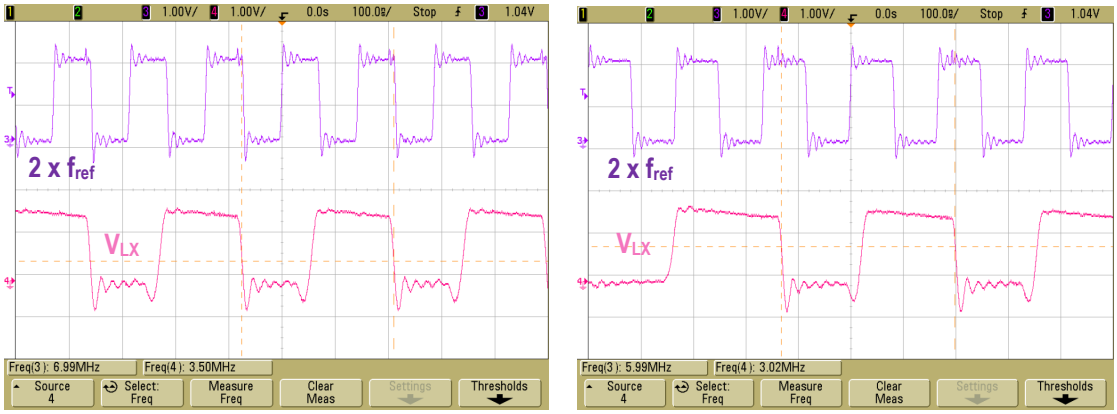
DAC and the loop delay. For example, if the input reference clock is very low, the DAC needs to provide sufficient current to produce a very wide hysteresis window to slow down f_{sw}, which may be higher than its maximum output current ability. On the other hand, if the input reference clock is very fast, a very narrow hysteresis window will be generated. However because of the size of the large power FETs, the driver is not able to drive the power FETs very fast which will limit the maximum switching frequency which can be synchronized from the input reference clock.



(a) f_{ref}=4.5MHz



(b) f_{ref}=4.0MHz



(c) f_{ref}=3.5MHz (d) f_{ref}=3.0MHz

Fig. 25 Measured Input Clock Reference and V_{LX} Waveforms for Digital Frequency Synchronization (DFS).

Fig. 26 shows that the dynamic range for the DFS scheme is roughly 3-9.5MHz and the switching frequency has a less than ±1.5% mismatch compared to the input reference clock within that range.

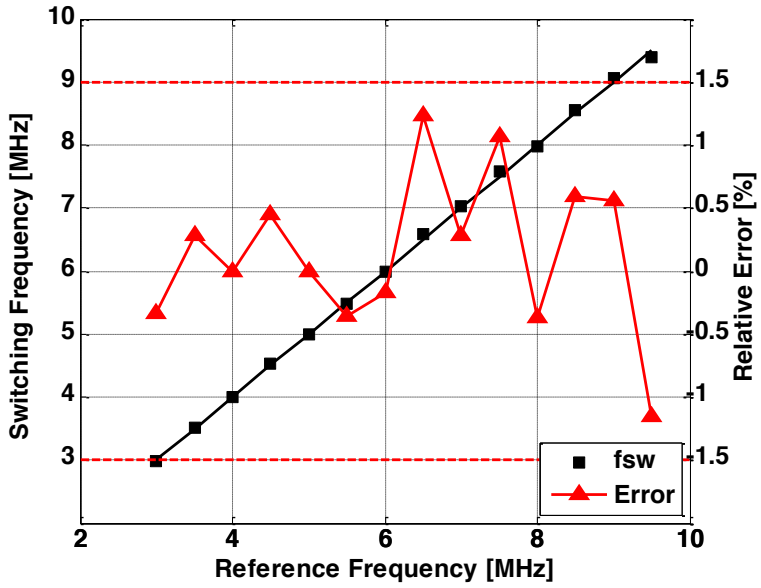


Fig. 26 Measured Digital Frequency Synchronization Performance and Switching Frequency Accuracy.

The voltage regulation accuracy is shown in Fig. 27 by comparing the performance with and without the online auto-zeroing based offset calibration topology. From the measured results, the auto zero scheme is able to cancel roughly 30mV input-referred offset for the hysteretic comparator. A 4X reduction of output voltage error is achieved when the output is 0.8V. The input-referred offset is relatively constant while increasing the output voltage from 0.8V to 1.8V. Therefore, the relative output voltage error caused by the input-referred offset of the hysteretic comparator gets reduced and the two curves in Fig. 27 start to merge.

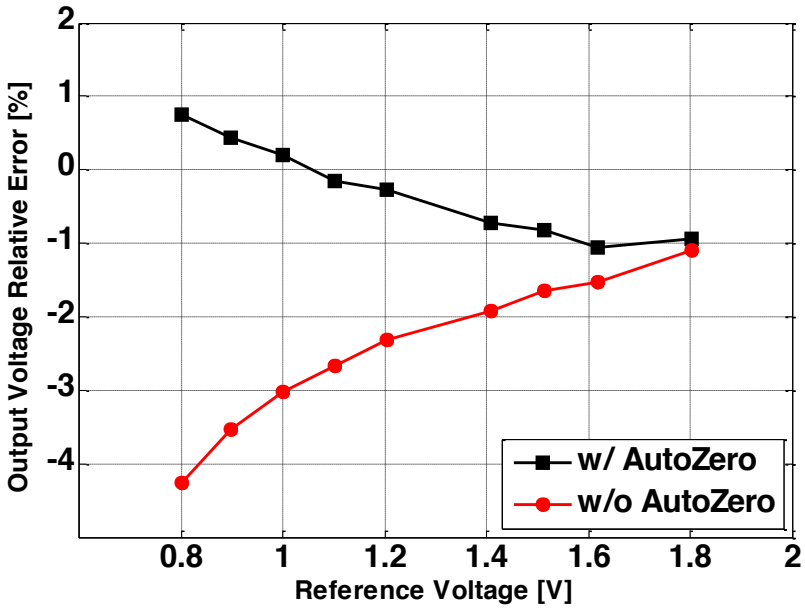


Fig. 27 Voltage Regulation Accuracy with and Without the Online Auto-zeroing Based Offset Calibration.

The measured switching node waveform of 4-phase operation is shown in Fig. 18. An equal 60ns delay between each phase is achieved through the delay line with DLL to calibrate its delay. With the current sharing topology, the duty cycle is calibrated for the

three slave phases and a 3.6% current mismatch is measured by using Keysight N2893A current probe.

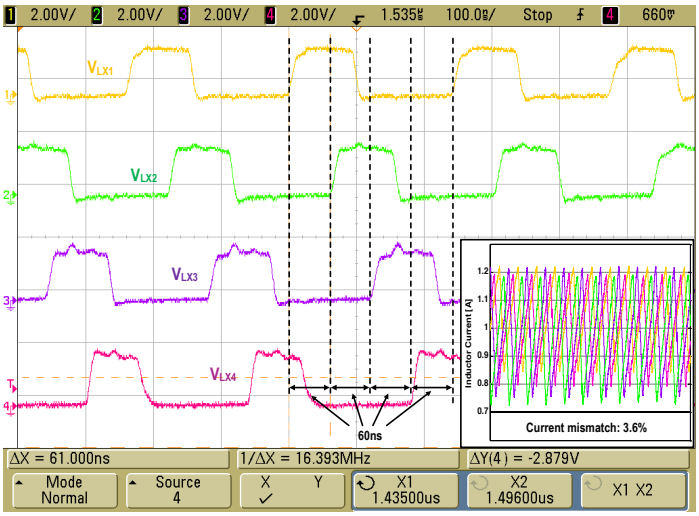


Fig. 28 Measurement of Switching Node (V_{LX}) and Inductor Current Waveforms During the 4-phase Operation Mode.

The measured efficiency performance is shown in Fig. 29. A peak 93% efficiency is achieved when V_{IN}=2V and V_{OUT}=1.6V. To enhance the efficiency performance, the proposed 4-phase buck converter will enter into the phase shedding mode [26] by comparing the inductor's average current with the pre-defined current threshold. Instead of matching the time constants of the feedback resistor and capacitor in parallel with the inductor [20], circuits are designed for sensing and averaging the current flowing from both the high-side and low-side power FETs [27], [28]. If the load current is less than the current threshold, the master phase will shut down the three slave phases and the buck converter will enter into the phase shedding mode [28].

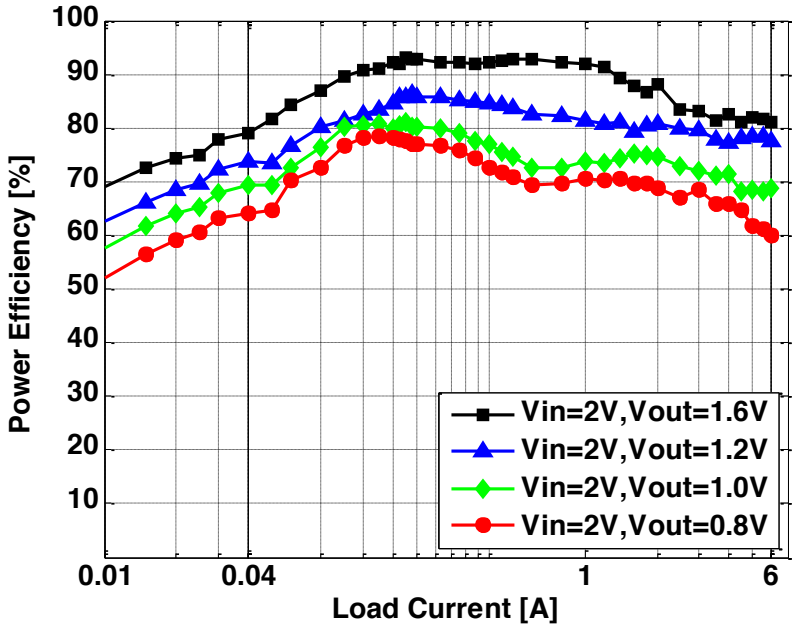
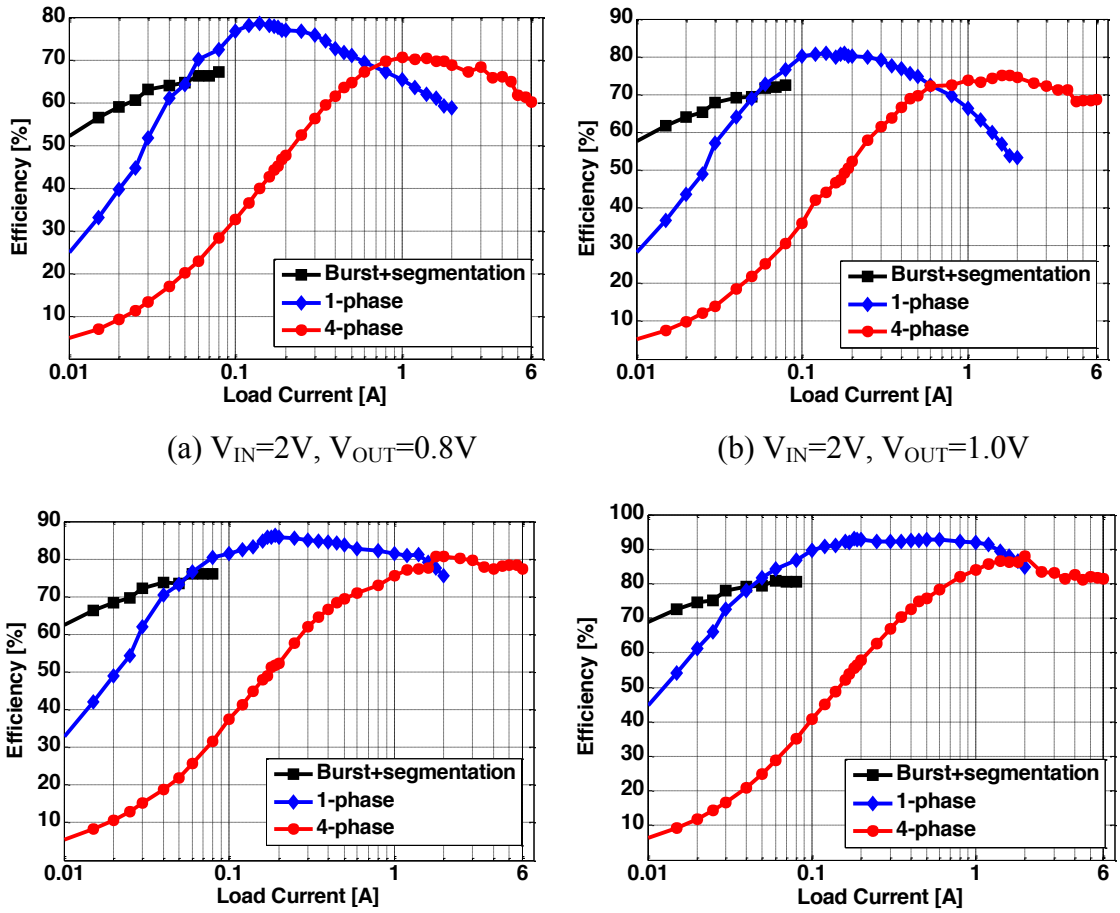


Fig. 29 Measured Efficiency Performance for the Proposed 4-phase Buck Converter.

If the load current is further reduced, the master phase will turn off 75% of both the power FETs and the driver, so that the converter can enter into the segmentation and burst mode. The efficiency performance under different operation mode is shown in Fig. 30. The efficiency performance is better for higher output voltages because the effective load resistance is higher when the output voltage is higher.



(a) V_{IN}=2V, V_{OUT}=0.8V

(b) V_{IN}=2V, V_{OUT}=1.0V

(c) V_{IN}=2V, V_{OUT}=1.2V

(d) V_{IN}=2V, V_{OUT}=1.6V

Fig. 30 Efficiency Performance Comparison for Different Operation Mode and Output Conditions.

Fig. 31 shows the load transient performance for the proposed 4-phase buck converter. To enhance the load transient performance, once the overshoot or undershoot is detected by the hysteretic comparator, it will turn off the high-side PMOS or the low-side NMOS and short one of the hysteretic comparator's output to V_{OUT} so that the hysteretic comparator is able to know the DC condition of the output voltage for the buck converter.

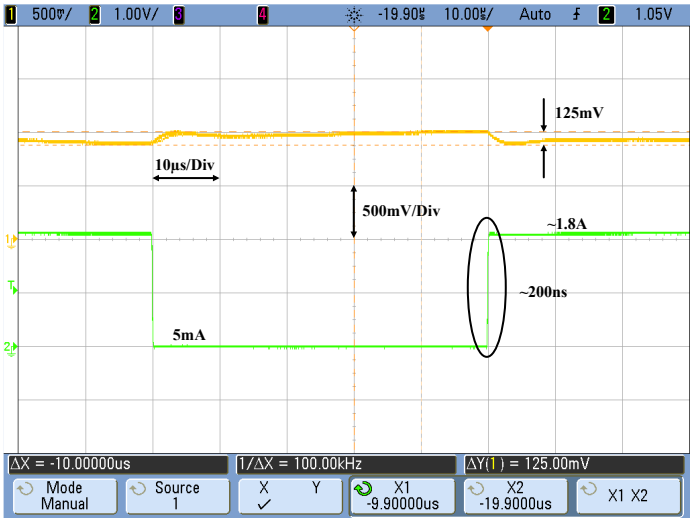


Fig. 31 Measured Load Transient Response for the Proposed 4-phase Buck Converter.

Table II provides the performance summary of the proposed 4-phase buck converter and the comparisons with the other state-of-the-art multi-phase buck converters. The reduction of the passive components for the state-of-the-art counterparts [5], [6], [8] and [22] comes with the price of the degradation of the efficiency. For this work, a 93% peak efficiency for V_{IN}=2V and V_{OUT}=1.6V is achieved when f_{sw} = 5MHz, which is the highest efficiency performance in the comparison table. Notice that prior work might have higher efficiency with the similar input and output conditions.

Table II

Performance Summary and Comparison with State-of-the-art Multi-phase DC-DC Regulators

	ISSCC ′13 [5]	ISSCC ′14 [6]	JSSC ′09 [22]	JSSC ′14 [26]	This Work
Control	Voltage Mode	Hysteretic	Hysteretic	Peak Current	Hysteretic
Technology	0.13μm CMOS	0.18μm CMOS	0.5μm CMOS	0.18μm BCD	0.18μm CMOS
V_{IN} (V)	1.2	3.3	4−5	2.7−5	2−3.3
V_{OUT}(V)	0.6−1.05	0.7−2.5	0.86−3.93	0.8−V_{IN}	0.8−1.6
I_{MAX}(A)	1.2	6	1	4.5	6
f_{sw}(MHz) (phases)	100 (×4)	40 (×4)	32−35 (×4)	2 (×4)	3−9.5 (×4)
Frequency Synchronization Error (%)	Fixed, PWM	N.A.	Variable	*Fixed, PWM*	±1.5%
Voltage Regulation (%)	N.A.	N.A.	N.A.	N.A.	±1.1%
Current Sharing	Master-slave	Cycle-by-cycle	None	Peak Current	Master-slave (DCC-DL)
Current Sharing Accuracy (%)	N.A.	N.A.	N.A.	N.A.	±3.6%
L(nH)	8	78	110	470	330
Inductor DCR (mΩ)	N.A.	42	N.A.	N.A.	5
C_L(μF)	0.00187	0.94	0.2	44	10
Load Regulation (%/mA)	0.0058	N.A.	0.0101*	0.0036*	0.0051
Line Regulation (mV/V)	N.A.	N.A.	N.A.	0.78	1.6
Load Step (mA/ns)	180/800*	5000/5	300/30*	3550/10000*	1800/200
1% t_{settle} (μs)	~2*	~0.23*	~0.35*	~36*	~6
Peak Efficiency (%)	82.4 @V_{IN}=1.2V, V_{OUT}=0.9V	86.1 @V_{IN}=3.3V, V_{OUT}=1.6V	83 @V_{IN}=4.8V, V_{OUT}=3.3V	91.6 @V_{IN}=2.7V, V_{OUT}=1.8V	93 @V_{IN}=2V, V_{OUT}=1.6V

*: Derived from paper

CHAPTER 9 CONCLUSION

The work in this dissertation focused on the design of a multi-phase buck converter. A 4-phase, current-mode hysteretic buck converter with digital frequency synchronization, online auto-zeroing based offset calibration and duty-cycle-calibrated delay line based current sharing control is designed and fabricated on a 5-level metal 0.18μm CMOS process with 5V thick gate oxide option for performance verifications.

The switching frequency of the hysteretic controlled buck converter is impacted by external device parasitics, such as ESR of the decoupling capacitor, comparator delay, driver delay, and the hysteresis voltage. To synchronize and stabilize the switching frequency, a digital frequency synchronization topology is proposed, which comprised of a bang-bang phase-frequency detector (BB-PFD), a digital low-pass filter with digital PI compensator, a 10-bit current-steering digital to analog converter (DAC) and a hysteresis window generator. By considering the buck converter as a current-controlled oscillator (CCO), the switching frequency can be synchronized with the input reference clock by using a DPLL with less than ±1.5% error in the range of 3-9.5MHz.

To achieve accurate voltage regulation accuracy, an online auto-zeroing based offset cancellation method is proposed to remove the input referred offset of the hysteresis comparator. During the sampling phase, the input referred offset is sampled on the two input capacitors and it is cancelled during the settling phase. To avoid the false triggering of the RS latch inside the hysteresis comparator, two OR gates are designed. The online auto-zeroing based offset calibration topology enables 4X reduction of output voltage error and ±1.1% voltage regulation accuracy.

The current sharing accuracy is highly dependent on the matching of the duty cycle, inductor DCR and the other resistance on the power path of each phase in the traditional design. To improve the power efficiency and the current sharing accuracy of the multi-phase buck converter, the duty cycle of the slave phases are calibrated to achieve accurate current sharing through a duty-cycle calibrated delay line (DCC-DL). By digitally calibrating the duty cycle of the slave phases, a current sharing mismatch of less than ±3.6% is achieved by a duty-cycle-calibrated delay line based PWM generator, without affecting the phase synchronization timing sequence.

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