Development of Novel Sensor Devices for Total Ionization Dose Detection

by

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ABSTRACT

Total dose sensing systems (or radiation detection systems) have many applications, ranging from survey monitors used to supervise the generated radioactive waste at nuclear power plants to personal dosimeters which measure the radiation dose accumulated in individuals. This dissertation work will present two different types of novel devices developed at Arizona State University for total dose sensing applications. The first detector technology is a mechanically flexible metal-chalcogenide glass (ChG) based system which is fabricated on low cost substrates and are intended as disposable total dose sensors. Compared to existing commercial technologies, these thin film radiation sensors are simpler in form and function, and cheaper to produce and operate. The sensors measure dose through resistance change and are suitable for applications such as reactor dosimetry, radiation chemistry, and clinical dosimetry. They are ideal for wearable devices due to the lightweight construction, inherent robustness to resist breaking when mechanically stressed, and ability to attach to non-flat objects. Moreover, their performance can be easily controlled by tuning design variables and changing incorporated materials. The second detector technology is a wireless dosimeter intended for remote total dose sensing. They are based on a capacitively loaded folded patch antenna resonating in the range of 3 GHz to 8 GHz for which the load capacitance varies as a function of total dose. The dosimeter does not need power to operate thus enabling its use and implementation in the field without requiring a battery for its read-out. As a result, the dosimeter is suitable for applications such as unattended detection systems destined for covert monitoring of merchandise crossing borders, where nuclear material

tracking is a concern. The sensitive element can be any device exhibiting a known variation of capacitance with total ionizing dose. The sensitivity of the dosimeter is related to the capacitance variation of the radiation sensitive device as well as the high frequency system used for reading. Both technologies come with the advantage that they are easy to manufacture with reasonably low cost and sensing can be readily read-out.

DEDICATION

To my loving parents

To my teachers and mentors

To my wonderful wife, precious daughter and family members

To my friends and peers

and

To all the wonderful and kindest people on earth!

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CHAPTER 1

INTRODUCTION

1.1. Importance of radiation detection systems:

In nuclear power generation stations or medical research facilities there are many workers who deal with radiation all the time. Several years ago, in Fukushima, Japan, a powerful earth quake and tsunami took down three of the four reactors at Daiichi nuclear power plant leading to explosion, core meltdown and significant releases of radioactive material into the local environment and atmosphere. This incident created an enormous impact socially, politically and economically in both local and global arena. The most important effect is probably the health impact due to radiation exposure.

Among the most dangerous sources of radiation originates from the atomic nucleus. Since atomic nuclei are strongly bound, the radiation emitted from them is very high in energy. Fig. 1.1 shows an electromagnetic spectrum presenting different types of waves that can be the source of radiation exposure either naturally or electively [1]. The left side of the spectrum indicates the radio waves with long wavelength where energy is lowest. Moving to the right as energy increases (and wavelength decreases) there is visual light that can be sensed very well. After visual light, there is infra-red that can also be sensed or felt mostly as heat. Further increasing the energy (reducing wavelength consequently), moves the spectrum into the X-ray and gamma ray domains. One of the challenges with the high energy radiation like X-rays or gamma rays is that they cannot be felt or sensed readily like visible light or infra-red. That makes it difficult to quickly detect and thus avoid an instant impact of radiation exposure. As Fig. 1.1 indicates, the higher energy radiation is ionizing which means it can generated electrons in materials. There is a demand for devices that can sense ionizing radiation [2], [3]. The good news is that, since the interaction between high energy radiation and materials is quite different than their lower energy counter-parts (e.g., radio waves, visible lights etc.), and these characteristics can be utilized to develop technologies for detecting ionizing radiation [4]-[7]. This dissertation presents two novel technologies developed by utilizing unique radiation-material interaction characteristics.

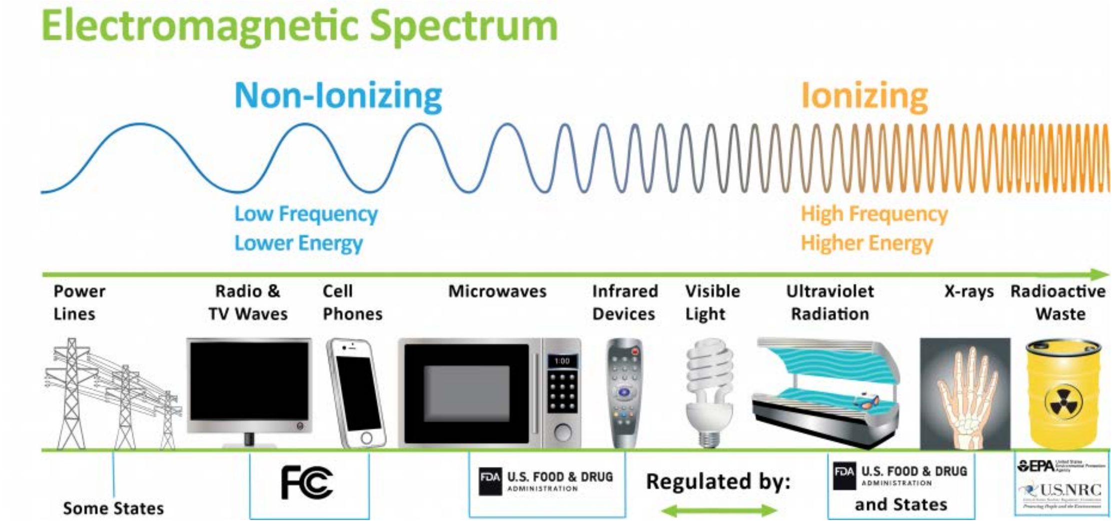


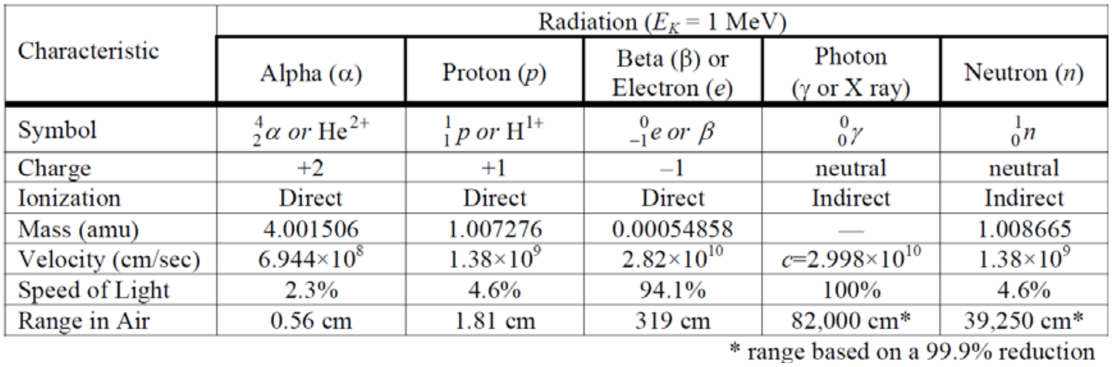
Fig 1.1: Electromagnetic spectrum showing sample sources of non-ionizing and ionizing radiation. [1]

1.2. Types of ionizing radiation:

Radioactivity fundamentally means the transformation of a nucleus from an unstable configuration to more stable configuration. While going from an unstable to a stable configuration, a material emits radiation. Different types of radiations can broadly be classified into two categories: (i) charge particle based radiation and (ii) charge neutral radiation [8]. When interacted with materials, charge particle based radiation can directly cause ionization by transferring charge. This category includes alpha, proton and beta radiation. Unlike charged particles, charge neutral radiations do not cause direct ionization. This category mainly includes gamma, x-ray and neutron radiation. Alpha particles (α) are positively charged and made up of two protons and two neutrons from the atom's nucleus. They are generated from the decay of the heaviest radioactive elements, such as uranium, radium and polonium. Since these elements are relatively heavy, they cannot travel very far from the source even with high energy. As a result, they are comparatively easy to stop (e.g., human skin is good enough to stop most of the alpha particles making them comparatively less harmful). Proton (*p*) particles are atoms that carry a positive charge. They are slightly lighter in mass compared to the alphas and therefore have a higher velocity and a bit larger travel range in the air. Beta particles (β) are small, fast-moving particles with a negative electrical charge that are emitted from an atom's nucleus during radioactive decay. These particles are emitted by certain unstable atoms such as hydrogen-3 (tritium), carbon-14 and strontium-90. Because they are much lighter in mass than the alpha particles and have only one unit of electric charge, it takes more material to stop them. But typically, a quarter inch of plastic is enough to stop most beta particles. Unlike alpha, beta or proton particles, gamma rays are photons with no electric charge and no mass. They are similar to visible light, but have much higher energy. In typical nuclear transitions, the wavelengths of photons are so short that human eyes cannot see them. Gamma rays are often emitted along with alpha or beta particles during radioactive decay. Due to their very high energy and larger range in air, gamma rays are much more difficult to stop compared to alpha or beta radiation. It takes dense materials like couple of inches of lead or several feet of concrete to stop them. If not blocked, they can completely pass through human body and ionize the tissue and DNA presenting a severe health hazard. X-rays are similar to gamma rays in that they are photons of pure energy and have the same basic properties. However, they are generated from a different part of the atom. While gamma rays originate inside the nucleus, X-rays are emitted from processes outside the nucleus. Also, they are generally lower in energy (compared to gamma), therefore less penetrating. Unlike gamma and X-ray, neutrons have mass. They mainly affect lattice atoms of a material through collision which can result in emission of gamma rays or charged particles. Neutron radiation is more penetrating than alpha or beta radiation and causes materials to degrade through crystal dislocations, swelling, and embrittlement of metals [9], [10]. Table 1.1 presents some key characteristics of these radiations, including charge, mass, and range in air. The passage of radiation through tissue is depicted in Fig. 1.2 [8].

TABLE 1.1

COMPARISON OF IONIZING RADIATION [8]



Characteristic	Radiation (E_K = 1 MeV)				
	Alpha (α)	Proton (p)	Beta (β) or Electron (e)	Photon (γ or X ray)	Neutron (n)
Symbol	${}^4_2\alpha$ or He^{2+}	${}^1_1p$ or H^{1+}	${}^{0}_{-1}e$ or β	${}^0_0\gamma$	${}^1_0n$
Charge	+2	+1	–1	neutral	neutral
Ionization	Direct	Direct	Direct	Indirect	Indirect
Mass (amu)	4.001506	1.007276	0.00054858	—	1.008665
Velocity (cm/sec)	6.944×10^{8}	1.38×10^{9}	2.82×10^{10}	$c=2.998\times10^{10}$	1.38×10^{9}
Speed of Light	2.3%	4.6%	94.1%	100%	4.6%
Range in Air	0.56 cm	1.81 cm	319 cm	82,000 cm*	39,250 cm*

* range based on a 99.9% reduction

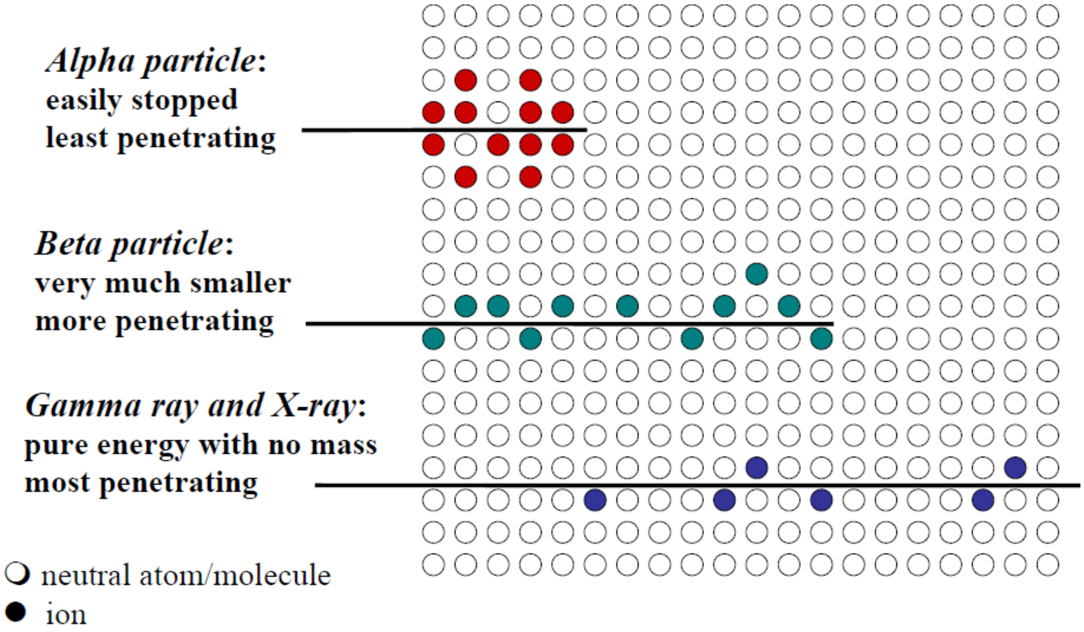


Fig. 1.2: Radiation path and range in tissues [8]

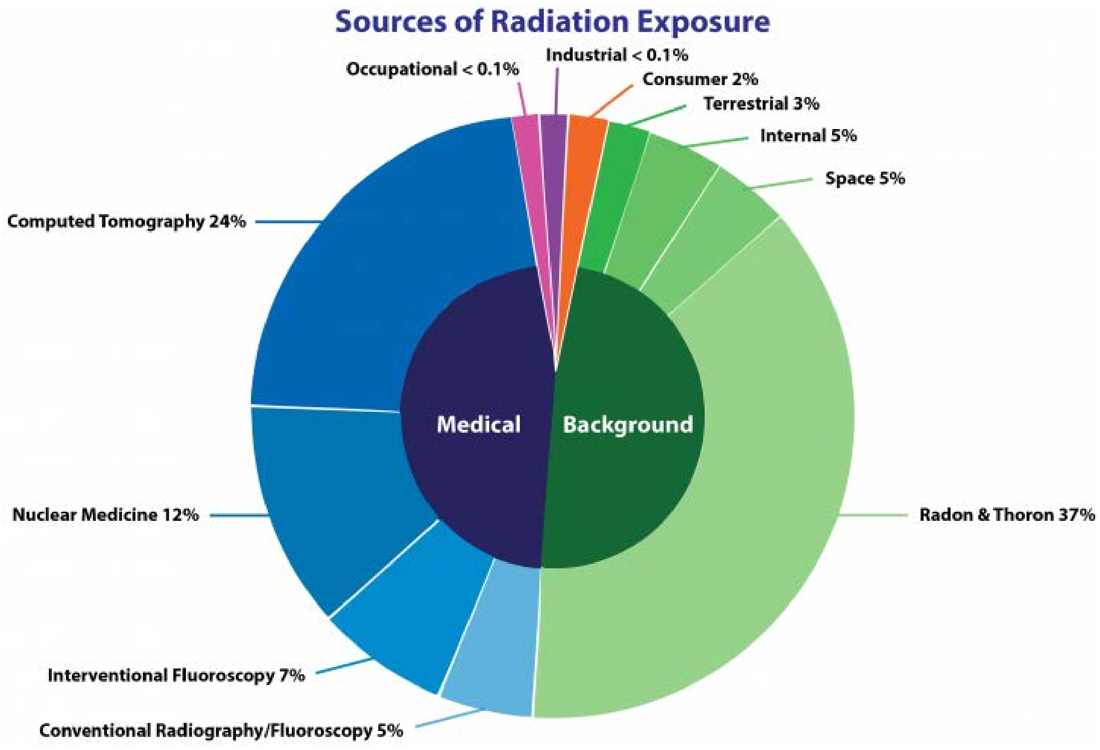
1.3. Common radiation sources and measurement units:

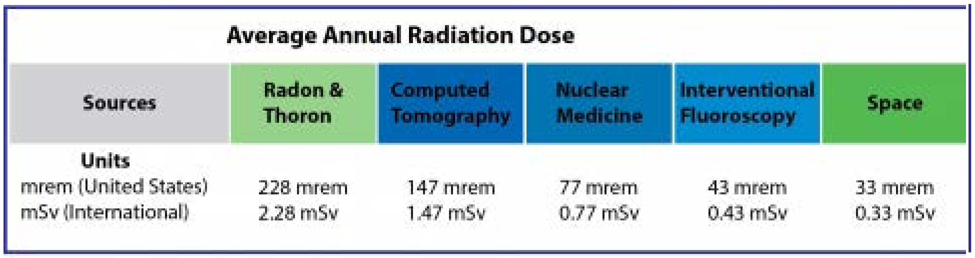
Radiation sources can be natural or man-made. The amount of radiation absorbed by a person is measured in dose. A dose is the amount of radiation energy absorbed by the body. According to the National Council on Radiation Protection and Measurements (NCRP), it has been found that on average a person in US is exposed to around 620 millirem or 6.2 millisieverts [11]. The millirem is the U.S. unit used to measure effective dose in tissue. One millirem equals 0.01 milliSievert which is the international unit. A detailed list of common radiation units and their equivalent conversion can be found in Table 1.2. The units becquerel and curie are used for describing radiation emitted from a radioactive material. Gray and rad are used to reflect the different amounts of radiation energy absorbed by a mass of material. The relative biological damage in the human body is measured using sieverts and rem, which depends on the type of radiation. Because x-rays and gamma rays are less damaging to tissue than neutrons or alpha particles (for a given deposited energy), a conversion factor is used to translate the rad or gray into rem or sieverts, which are used to express the biological impact [12], [13]. For example, if the radiation type is either x-rays or gamma rays, then 1 rad = 1 rem = 10 mSv. For neutrons it will be: 1 rad = 5 to 20 rem (depending on energy level) = 50 - 200 mSv and for alpha radiation (helium-4 nuclei): 1 rad = 20 rem = 200 mSv [13]. Finally, roentgen or (columb/kg) measures the ionization produced in air by X-rays or gamma radiation and it is used because air ionization can be measured directly [14]. Fig. 1.3 presents a pie chart that shows different sources of radiation that causes the average dose on a daily basis in United States. Fig. 1.4 compares radiation doses from common radiation sources, both natural and man-made.

TABLE 1.2

COMMON RADIATION UNITS AND EQUIVALENT CONVERSION [12]

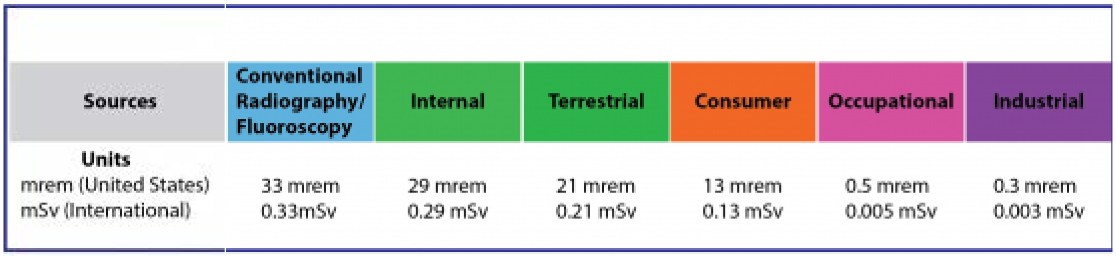
	SI Units	Common Units	Equivalent conversion
Radioactivity	becquerel (bq)	curie (Ci)	1 bq = 2.7×10^{-11} Ci
Absorbed dose	gray (Gy)	rad	1 Gy = 100 rad
Dose equivalent	sievert (Sv)	rem	1 Sv = 100 rem
Exposure	columb/kilogram (C/kg)	roentgen (R)	1 C/kg = 3880 R





Average Annual Radiation Dose

Sources	Radon & Thoron	Computed Tomography	Nuclear Medicine	Interventional Fluoroscopy	Space
Units mrem (United States) mSv (International)	228 mrem 2.28 mSv	147 mrem 1.47 mSv	77 mrem 0.77 mSv	43 mrem 0.43 mSv	33 mrem 0.33 mSv



Sources	Conventional Radiography/ Fluoroscopy	Internal	Terrestrial	Consumer	Occupational	Industrial
Units mrem (United States) mSv (International)	33 mrem 0.33mSv	29 mrem 0.29 mSv	21 mrem 0.21 mSv	13 mrem 0.13 mSv	0.5 mrem 0.005 mSv	0.3 mrem 0.003 mSv

(Source: National Council on Radiation Protection & Measurements, Report No. 160)

Fig. 1.3: Sources and amount of radiation absorbed by a person in US. [11]

As can be seen in Fig. 1.3, half of the exposure happens due to background radiation. Background radiation is present on Earth always and most of it occurs naturally from minerals in the ground, soil, water and even the human body. A notable portion comes from the outer space in the form of cosmic radiation. Another small fraction is generated from man-made elements. Natural sources include primordial radionuclides such as uranium, thorium which are naturally found in earth. These heaviest elements were created many billions of years ago in supernova events. The half-life of these elements is large; hence they live a long life until decay and act as the source of terrestrial radiation. Cosmic radiation consists of extremely energetic particles that strike the Earth's atmosphere from space. The annual exposure level depends on elevation, i.e., thehigher the altitude the higher the dose. Aside from these sources there can be exposures from other human beings since traces of radioactive materials (e.g., potassium-40, carbon-14) can be found in the body. This amount of exposure can be in the range of is 0.01 mSv/year. Nuclear weapon testing or power plant accidents like Fukushima Daiichi, Chernobyl or just simply operating a nuclear power station can also spread out traces of radioactive elements which can be a source of background radiation. It is noted here that natural background radiation levels can have large variances from place to place, as well as changes in the same location over time. Aside from background radiation, ~48% source of radiation exposure in the United States comes from medical procedures (not including dose from radiation therapy used in the treatment of cancer, which is typically many times larger).

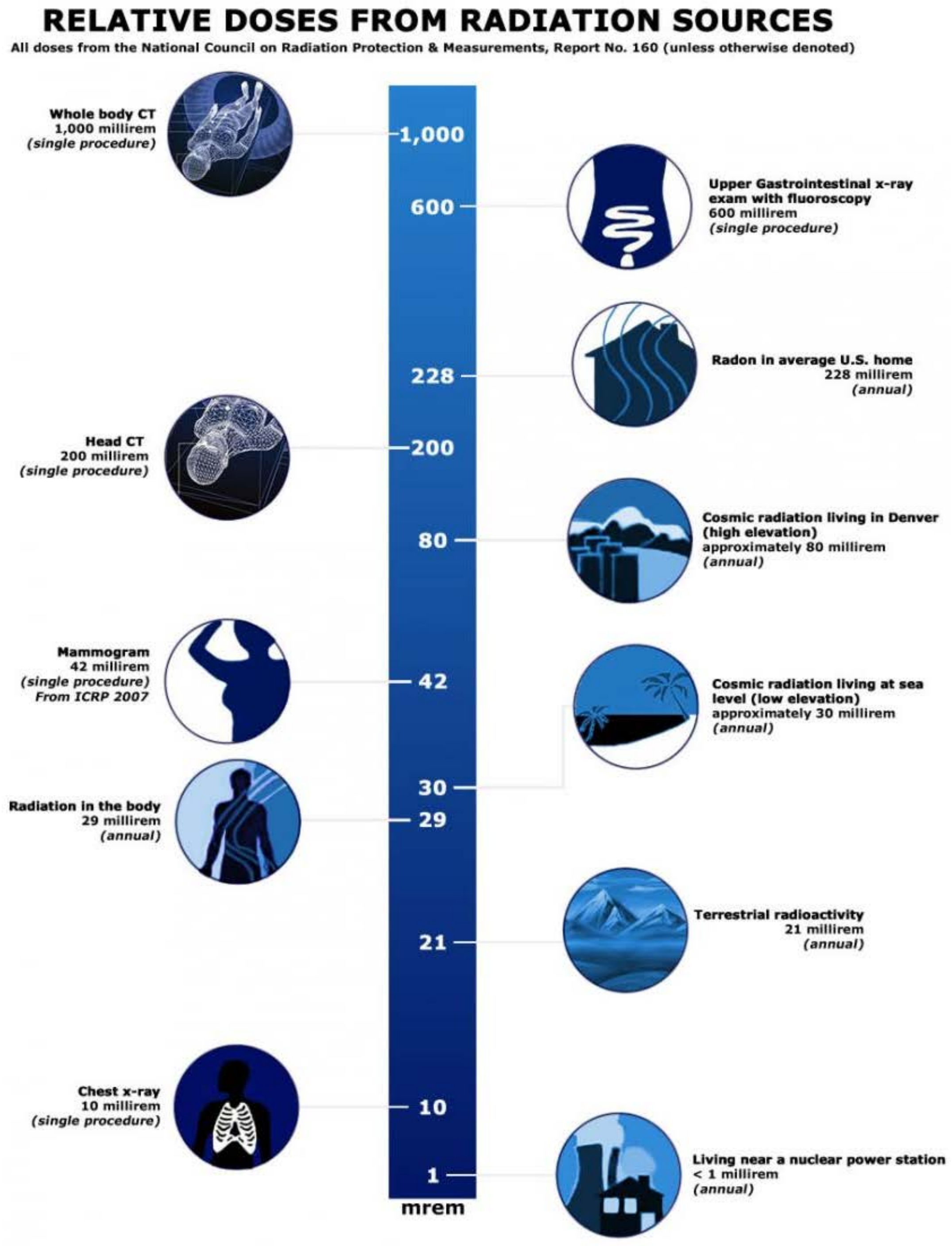


Fig. 1.4: Comparison of radiation doses from common radiation sources, both natural and man-made. [11]

Outside of US, there are other places in the world where the amount of average exposure can be higher. For instance, in Ramsar, Iran it can go up to 250 mSv/year [15]-[16]. It is important to note that, radiation that has biological effects does not depend on its source type (e.g., natural source/ non-natural source). For example, gamma ray emitting from bismuth-214 which is naturally occurring is very similar to gamma rays emitting from man-made source such as caesium-134 or caesium-137 (which is a signature for Fukushima). Because of this fact, the effects of radiation can be very similar regardless of the type of source.

1.4. Thesis outline:

Due to the health impact of high energy ionizing radiation, it is important to detect and measure it accurately. As previously mentioned, this dissertation presents two innovative radiation sensing approaches. The first technology is based on metal chalcogenide glass based systems. These sensors are developed on mechanically flexible polymer substrates and can withstand certain amount of mechanical strain. They are very lightweight and can be attached on non-flat objects. The low-cost manufacturing and simple operating process makes them attractive for a diverse range of market applications. The second technology is developed based on a radiation sensitive MOS capacitor that changes its device characteristics when irradiated. If the MOS capacitor can be manufactured with correct design parameters, this change in device characteristics can be tracked wirelessly when the MOS capacitor is loaded on a patch antenna and interrogated with a RF interrogator operating within a pre-determined frequency range. This technology has the potential to detect very low doses of radiation. Also, due to their small form factor and reasonably low manufacturing costs, they can be deployed as a wide network of sensors embedded in different media. This makes them very attractive for nuclear non-proliferation applications, nuclear forensics, and customs and border patrol agencies tasked with detecting, tracking and preventing the transport of unauthorized nuclear radioactive materials. Both technologies are in their early development stage which means that they are not free of limitations. But early test results suggest refinements that may make them ready for deployment. In the next chapter, a brief review of some of the technologies currently available in the market for radiation detection is provided. Chapter 3 will then introduce readers to the metal-chalcogenide glass based sensor technology and provide details on some performance optimization techniques. The MOS capacitor based wireless dosimeter technology will be presented in chapter 4. Chapter 5 will discuss potential research ideas to further improve the technologies by addressing some of the limitations. For the readers interested about the MOS capacitor based technology, Appendix A and B will present simulation work performed by an external collaborator (CFD Research Corporation, Huntsville, AL) based on the results presented in chapter 4.

CHAPTER 2

OVERVIEW OF COMMERCIAL DOSIMETER TECHNOLOGIES

There are various kinds of radiation detectors available in the market for commercial applications. This chapter will provide an overview of some of them (e.g., gas filled, scintillation and semiconductor detectors). They will be presented from the simplest to the most complex.

2.1. Gas filled radiation detectors:

Gas filled radiation detectors include ionization chamber, proportional and Geiger-Muller counters. All of them make use of the same general properties. If there is a container filled with sensitive volume of gas between two electrodes and ionizing radiation goes through it and interacts with the gas inside, it ionizes the gas by separating the negatively charged electrons and positively charged ions. Fig. 2.1(a) shows a conceptual diagram of a proportional counter detector. As can be seen, the structure looks like a cylinder which is full of gas and there is a thin wire which runs down the length of the cylinder that acts as the anode. The wall of the cylinder and the wire acts as two electrodes of the system (for the ionization chamber design, the second electrode can be another wire positioned inside the gas volume instead of the cylinder wall). On that thin wire, a positive high voltage is placed. The large potential difference between the anode and the cylinder wall creates a strong electric field in the contained gas volume. When ionizing radiation passes through the cylinder wall, it ionizes the contained gas atoms and generates electron-ion (partially ionized gas atoms) pairs. Due to the presence of the strong electric field, the negatively charged electrons are drifted toward the anode. As the kinetic energy of the electrons increases, they collide with other gas atoms on their way initiating further ionization (which produces more electrons). These secondary electrons themselves drift and acquire enough kinetic energy to cause further ionization (i.e., charge multiplication or avalanche process). As a result, a large cloud of electrons arrives at the anode. The quantity of charge collected in the anode is great enough to produce a large voltage pulse (which is the radiation signature and proportional to the energy deposited by the incident radiation) that can be detected by external electronics.

Unlike proportional counters, the potential difference between the two electrode wires are comparatively low in ionization chambers. Due to that, radiation generated electrons do not gain enough kinetic energy to participate in the charge multiplication process. Thus, the collected charge includes only the radiation generated electrons. Hence, the output pulses produced by the ionization chambers are smaller than those produced by proportional counters.

For the Geiger-Muller counter, the potential difference generally used is much larger than the proportional counters. As a result, charge multiplication process (like proportional counter) also increases, making the detector very sensitive. But eventually, the residual charge amount reaches such a high level that it prevents further charge multiplication events. Thus, the ionization process gets saturated and becomes independent of the initial deposited energy into the gas volume by the incident radiation. For this reason, Geiger-Muller counters do not differentiate among the kinds of particles or measure energy. It only counts the number of particles entering the detector by generating a same saturated high voltage pulse every single time an ionizing particle interacts. Also, it suffers from “dead time”, which is basically an insensitive period after each ionization of the gas during which any further incident radiation will not result in a count, and the indicated rate is therefore lower than the actual [17].

Unlike Geiger-Muller counters, the charge multiplication process does not reach saturation in proportional counters and ionization chamber detectors. Thus, they can provide an energy measurement of the detected particle. One of the limitations of these technologies is that it takes around 34 eV to generate a single electron-ion pair in a typical gas/air environment [18], [19]. If the energy deposited by an incident radiation is not big enough, there will be few electron-ion pairs created, which will be hard to detect.

Though the gas filled detectors are the simplest, their energy resolution is not great due to the broadening of the energy peaks caused by statistical distributions. They are widely used for neutron detection. Fig. 2.1(b) presents a plot showing how the amount of collected charge varies with applied voltage for different gas filled detectors. Conceptual 9diagrams of ionization chamber and Geiger-Muller counter are presented in Fig. 2.1(c) & (d). More information about the gas field detectors can be found in [17], [20]-[23].

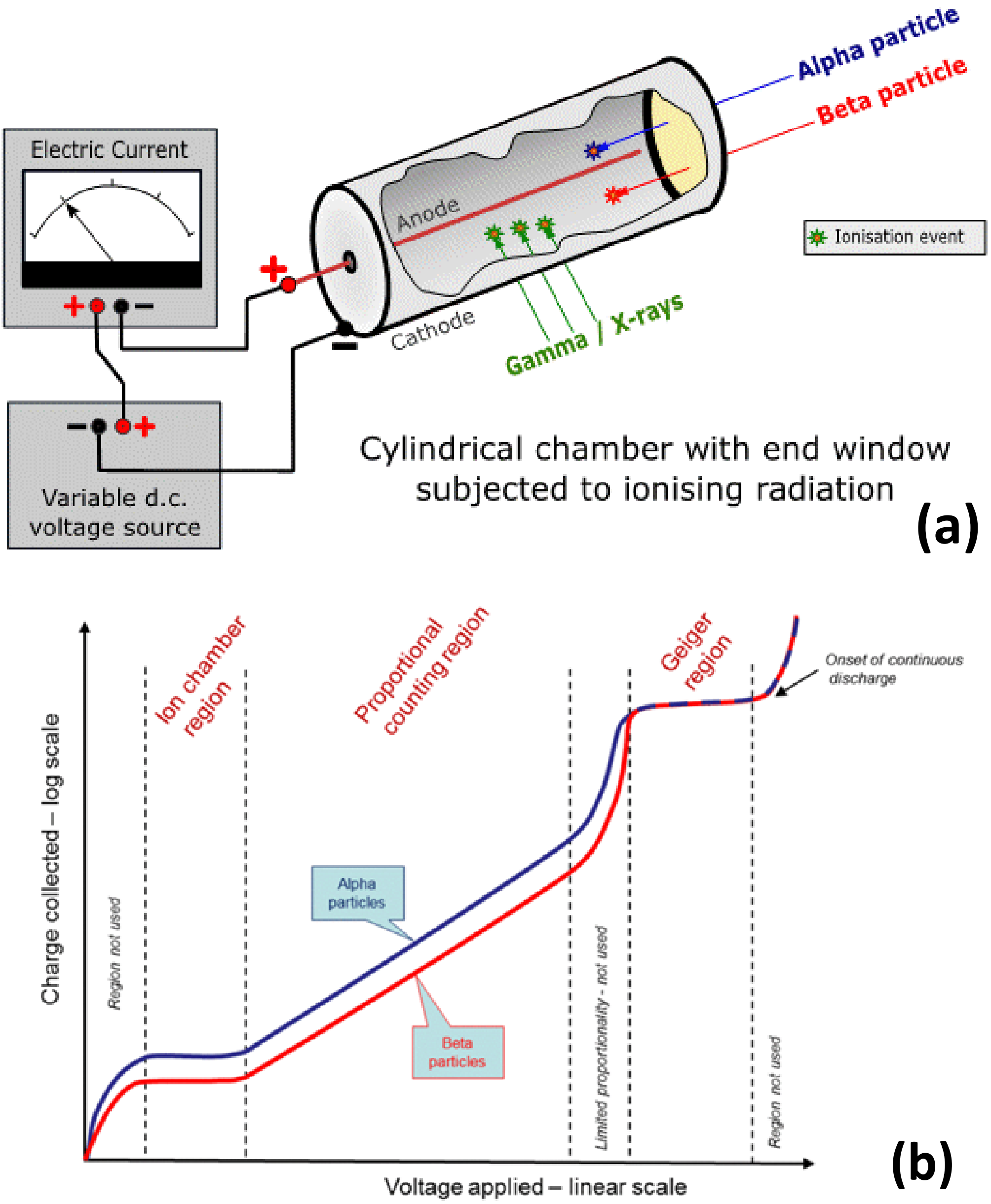


Fig 2.1 (part 1 of 2): Overview of gas filled radiation detectors: (a) The geometry of a proportional counter. The incoming low energy ionizing particle (alpha, beta) enters via an end widow, high energy photon (gamma, x-ray) can penetrate through sidewall. Both type creates many electron-ion pairs when interacts with the gas. The electron drift relatively slowly until they reach the neighborhood of the anode wire, where they are accelerated rapidly and create many secondary ionizations. (b) Variation of collected charge with applied voltage. Though alpha, beta plotted but similar event happens for any ionizing radiation. Figures taken from [23], [24].

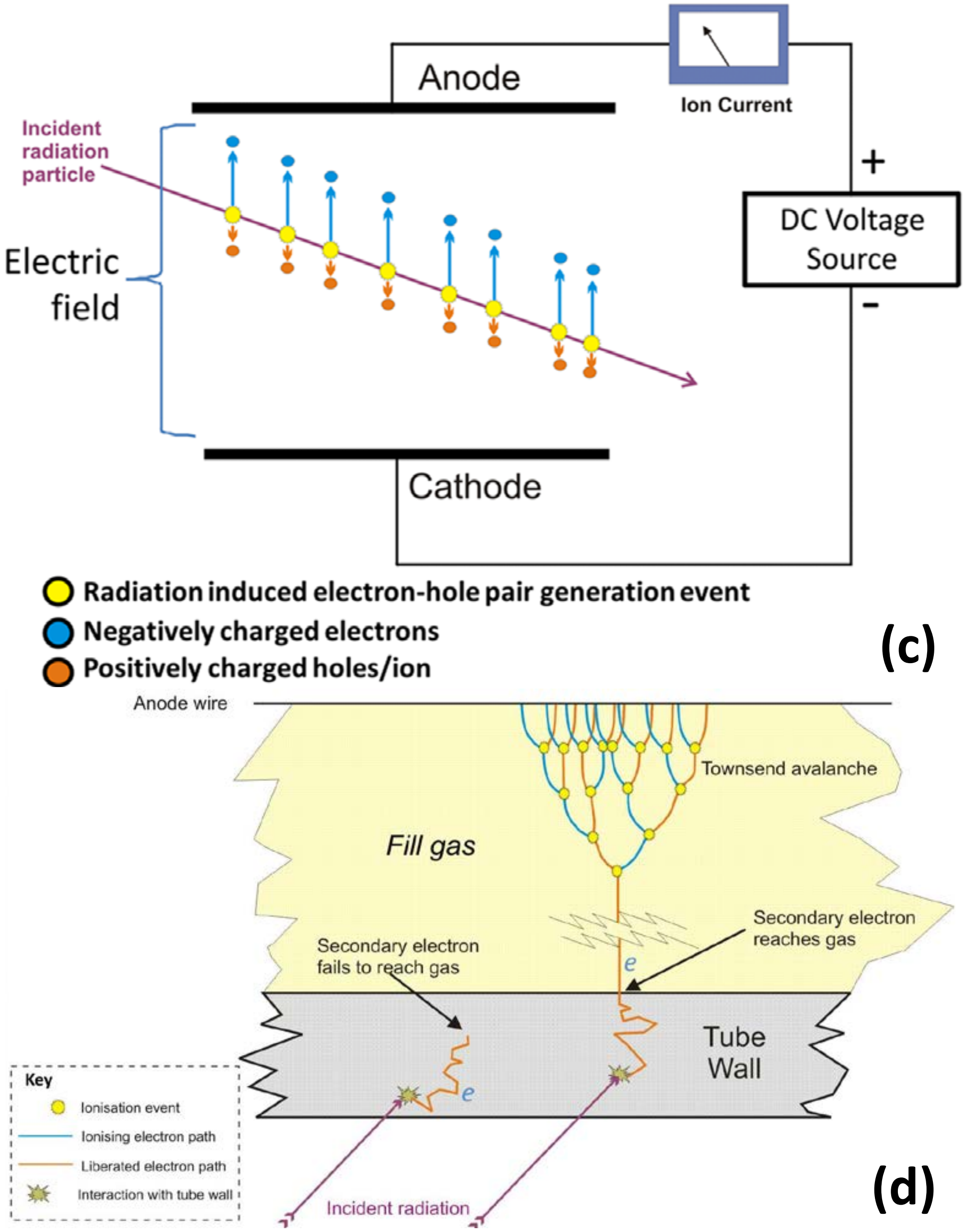


Fig 2.1 (part 2 of 2): (c) Visualization of ion chamber operation. Both electrodes are located inside the gas chamber unlike proportional counter. The applied voltage is low enough to avoid charge multiplication and collect only the primary charges generated through the ionization event. (d) Interaction of gamma ray inside a Geiger-Muller counter showing the interaction with the tube wall, generation of secondary electrons, ionization of the gas atoms and the increasing charge multiplication or the avalanche process. Figures taken from [25], [26].

2.2. Scintillation detectors:

Scintillation detectors are more complicated than the gas-filled detectors. The detectors utilize special types of luminescent materials (known as scintillators) which generate visible light when they interact with ionizing radiation. The materials can be an organic or inorganic solid (e.g., crystal or piece of plastic), liquid or gas. The most common scintillation materials are inorganic solids (e.g., NaI, CsI). They are developed to emit light when gamma rays, beta or alpha particles collide with material. In the detector system (Fig. 2.2), the scintillator is connected to a photo-cathode (typically metallic) that has a low ionizing potential. When incident ionizing radiation hits the scintillator, it can emit a valence electron into the conduction band (excitation state). After some time, the electron falls back into the valence band, losing energy in the form of a visible photon. This photon can be transmitted through the host scintillator material. Since the energy required to excite an electron from valence band to conduction band is equal to the energy of the emitted photon during the recombination process, it might cause the photon to get reabsorbed by the scintillator material instead of transmitting it to the photo-cathode, making the process inefficient. This can be resolved by doping the scintillator with activator impurities that creates intermediate energy levels near the scintillator's conduction and valence bands. During the recombination process, instead of falling back to the valence band, the electrons first fall into the energy levels added by the impurities. When further relaxation happens (i.e., recombination event from the activator energy level near the conduction band to another activator energy level near the valence band), it emits a photon that has too little energy to get absorbed by the scintillator material but has sufficient energy to activate the photo multiplier tube. An example of such an activator doped system is the NaI detector where a crystal NaI is doped with a small amount of thallium (Tl) to generate activator energy sites. This kind of detectors have much better energy resolution than the gas filled proportional counters discussed earlier. Fig. 2.2 illustrates the radiation-induced generation-recombination process of a pure crystal and activator doped scintillator material to show the role activator energy sites play to generate photons.

When photons of visible light are generated (direct or indirect photons), they transport strike the photocathode of the photomultiplier tube. As can be seen in Fig 2.3, the photons come from the scintillator material strikes the metal surface of the photocathode where

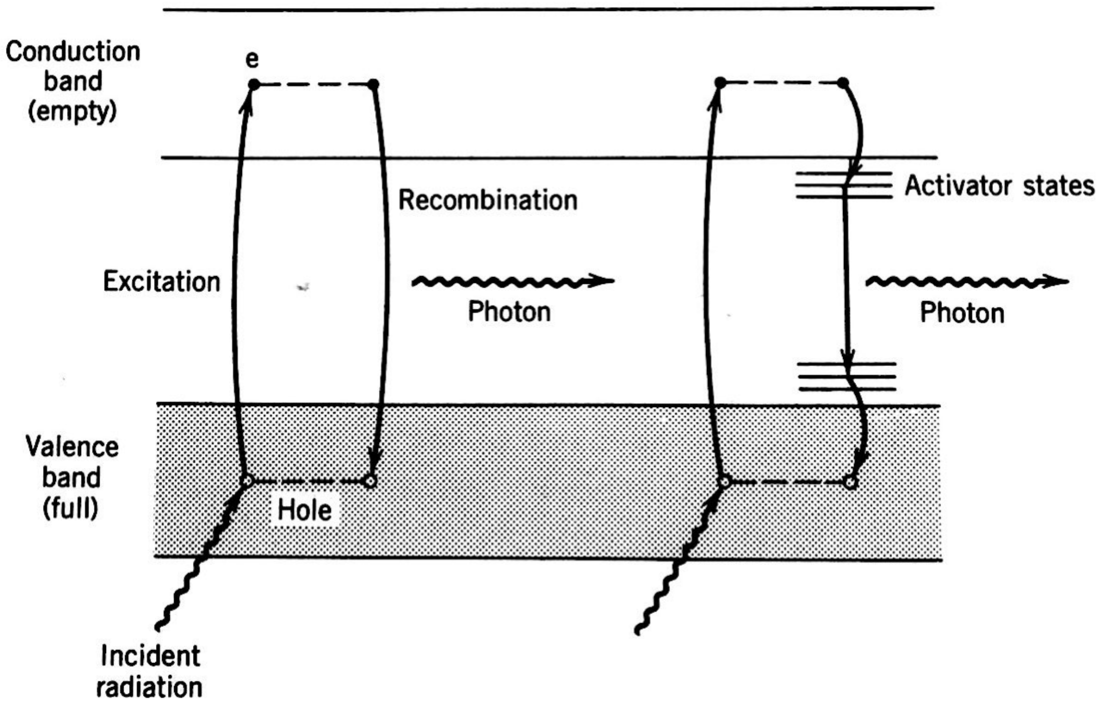


Fig. 2.2: Energy bands in a crystal. Radiation induced generation/ recombination process characteristic of a pure crystal such as NaI is shown at the left side. The right side shows the same processes in the presence of activator impurities, such as Tl in NaI(TI). Figure taken from [23].

energy of each single photon is transferred to a single photoelectron through the photoelectric effect. The photoelectrons than see a series of separately located electrodes (also known as dynodes) with successively higher potentials. A photoelectron generated at the photocathode drifts toward the closest electrode (that has the lowest potential) and knocks off multiple electrons upon strike by transferring its kinetic energy. These knocked off electrons then accelerate towards the second electrode which has comparatively higher potential. When the electrons from the first electrode strike the second one, they again knock off multiple electrons from the surface of the second electrode. Those knocked off electrons (from the second electrode) are then accelerated towards the third successive electrode that has a higher potential knocking off more electrons. This process of striking electrodes and generating more and more electrons continues until they reach the anode located at the opposite end of the photomultiplier tube (where all the charges are collected). By applying the right potential difference among the successive electrodes, it is possible to get a multiplication factor of 5 or 10 between adjacent electrodes.

In a typical photomultiplier tube, there can be 10 or 14 multiplication stages. Thus, a single photoelectron generated by a photon at the photocathode, can give rise to a large number of free electrons at the end of the multiplication process. This results in a current output that is big enough to be detected by external electronics. A schematic of the photomultiplier operation is presented in Fig. 2.4.

If the system is tuned to the right settings, the multiplication can be done in a linear way (i.e., the amplitude of the signal coming out at the end of the photo multiplication process, is proportional to the number of photons strike the photocathode). According to the photoelectric effect, the initial number of photoelectrons generated at the photocathode, is proportional to the number of photons incident on it (i.e., photo-cathode), which, in turn, is proportional to the amount of energy deposited in the scintillator material by the ionizing radiation (assuming no light loss from the scintillator volume which can be ensured by putting reflective material like MgO around it). Thus, an output signal is produced that is proportional to the energy deposited by the ionizing radiation in the scintillation medium and hence can provide energy measurement information [27].

A list of commonly used scintillators is presented in Table 2.1. Scintillator materials come with different densities, emit photons at different wavelengths and also, can produce different visible light output. Thus, for detecting a particular ionizing particle, one scintillator material can be better than the other. Moreover, photon emission wavelengths influence the choice of photomultiplier tube as well. In Table 2.1, the amount of light output that can be obtained from per unit energy deposition with NaI material is set as 1, since NaI has long been considered as the standard scintillator material. Compared to NaI, light generated by most other materials is somewhat less. For example, CsF has only 5% output compared to NaI. However, when compared to the the time constant point of view ("time constant" means the amount of time it takes for the light signal to come out of the scintillator material), NaI is not as good as CsF, which can generate an output signal much faster. Thus, for designing a faster detector, CsF might be scintillator material of choice instead of NaI. Aside from that, another scintillation material, bismuth germanate ($Bi_4Ge_3O_{12}$), commonly referred to as BGO, has also become popular in applications where its high gamma counting efficiency and its lower neutron sensitivity outweigh considerations of energy resolution [27]-[29]. A comprehensive discussion of scintillation detectors may be found in [17], [30], [31].

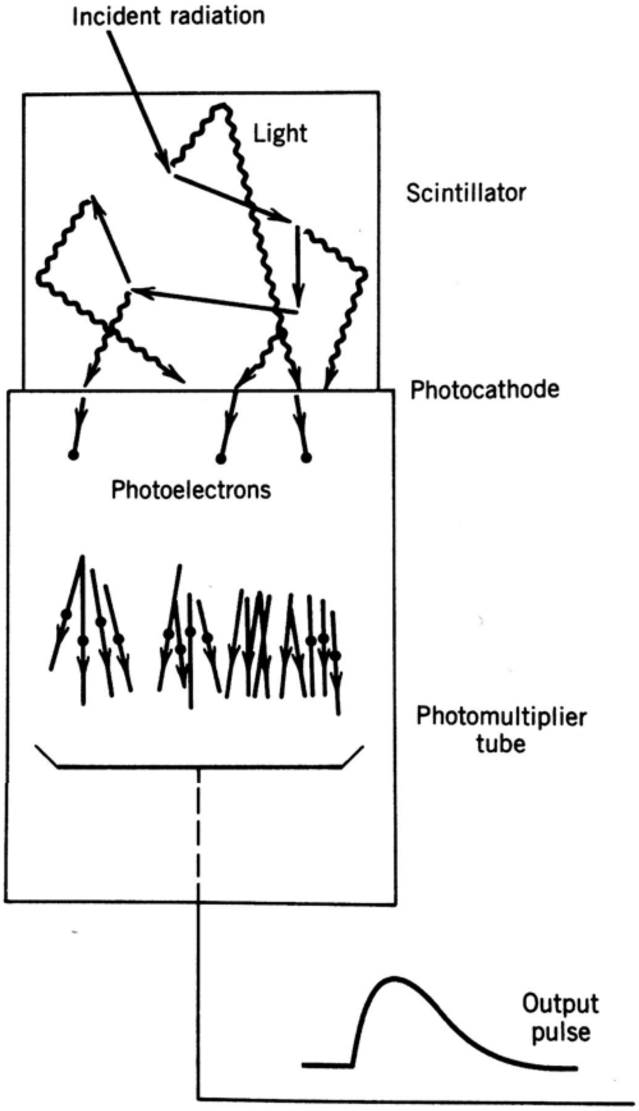


Fig. 2.3: The basic processes in scintillation detector. Figure taken from [23].

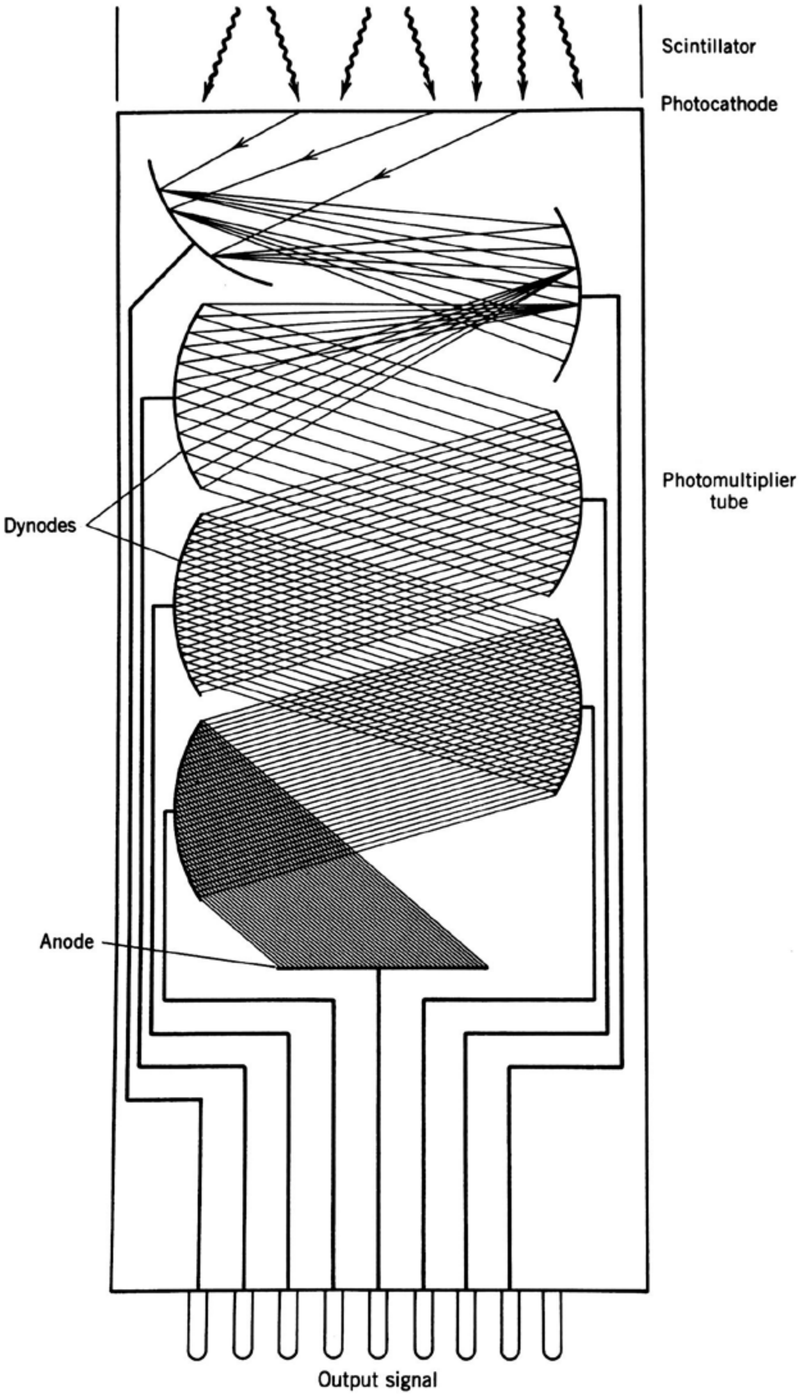


Fig. 2.4: Schematic of photomultiplier operation. Electrons released from the cathode are attracted to the first dynode and multiplied. Each successive dynode is at a higher potential than the previous one; a typical tube might have 10 or 14 dynodes. At each stage, the number of electrons increases by a factor of the order of 5. [23]

TABLE 2.1

PROPERTIES OF SOME COMMON SCINTILLATORS [23]

Name	Type	Density (g/cm^3)	Index of Refraction	Wavelength of Maximum Emission (nm)	Relative Output	Time Constant (ns)
Anthracene	Organic solid	1.25	1.62	447	0.43	30
Pilot B	Plastic (organic solid)	1.03	1.58	408	0.30	1.8
NE 213	Organic liquid	0.87	1.508	425	0.34	3.7
NaI(TI)	Inorganic solid	3.67	1.85	410	1.00	230
CsF	Inorganic solid	4.11	1.48	390	0.05	5

2.3. Semiconductor Detectors:

Semiconductor detectors offer better energy resolution compared to gas ionization chambers or scintillators. It is primarily because of the fact that the amount of ionization energy required to generate an electron-hole pair in a semiconductor is much less than the energy required to generate electron-ion pairs either in the gas or emit electrons in scintillators. Two of the semiconductor materials widely used in detectors are silicon or germanium, since both materials can be produced in high purity state which is very important for detector performance. Si detectors are primarily used for detecting charged particles like alpha, beta, and heavy ions. Ge detectors are widely used for high resolution gamma ray spectroscopy since Ge has several advantages over the Si. First, Ge has a smaller bandgap than silicon (0.7 eV vs. 1.1 eV for Si). This helps to generate more electron-hole pairs per unit of deposited energy when Ge is irradiated. Ge also has a higher density (5.32 gm/cm^{-3} vs. 2.33 gm/cm^{-3} for Si), and a higher atomic number, Z (32 for Ge and 14 for Si). Higher density and Z helps Ge detectors to obtain greater interaction rates and less Compton interference. Moreover, the lower impurity in Ge (i.e., 10^9 in Ge vs. 10^{12} cm^{-3} in Si) allows for much larger volumes to be depleted [32]. Besides Si and Ge, other materials can also be used as the detector depending on the application. Example of some of the widely used semiconductor detectors are given below:

- High-Purity Germanium (HPGe) detectors
- Germanium Lithium-drifted (GeLi) detectors
- Silicon Lithium-drifted (SiLi) detectors

- Cadmium Telluride (CdTe) detectors
- Cadmium Zinc Telluride (CdZnTe) detectors
- Mercury Iodide (HgI_2) detectors

Fig. 2.5 presents energy band diagrams of a p-n junction with zero bias and reverse bias conditions which can be used to explain the general operation of many semiconductor detectors. When a p-n junction is formed, electrons migrate from the n-type region to the p-type region and holes migrate from the p-type region to the n-type region. Migration of charges creates a region at the junction which is depleted of electric charge (known as depletion region). The depletion region can be extended to a bigger volume when an external reverse bias voltage is applied to the p-n junction. This will result in an electric field inside the depletion region that accelerates any excess electrons towards the n-type region and the positively charged excess holes towards the p-type region. When such a device is irradiated, the ionizing radiation generates electron hole pairs inside the depletion region. Due to the intrinsic and extrinsic (if the junction is reverse biased) fields, the excess carriers will transport to their respective regions and get collected. Collection of these generated charges will produce an electric current which is proportional to the energy deposited inside the detector by the ionizing particle. Semiconductor detectors thus have some similarity with the ionizing chamber detectors where two electrodes with opposite bias are used to collect the radiation generated charges. However, from performance point of view, semiconductor detectors are better than the ionization chamber (or any gas filled or scintillation detectors) since they can provide higher energy resolution. Fig. 2.6 illustrates such an example where energy spectra of ^{137}Cs radioactive source detected by both a NaI(Tl) scintillation detector and Ge(Li) semiconductor detector are superimposed together. The radioactive isotope ^{137}Cs emits gamma ray at 662 keV when it decays [33]. As can be seen in Fig. 2.6, the resolution (FWHM) of the NaI(Tl) is about 40 keV while that of the Ge is about 1 keV (FWHM or full width at half maximum means maximum width of the signal at half of the total height. The narrower the width, the better the resolution. The intensity (peak area) of the Ge is about 11% of that of NaI(Tl). This means that if a NaI detector detects two photon energies within 40 keV of each other and in the range of the ^{137}Cs 662 keV gamma ray, they may not be distinguishable as two separate photon energies. Since the Ge(Li) detector in this example has a FWHM of 1 keV, these two photons would be distinguishable, assuming they were more than 1 keV apart in energy [32].

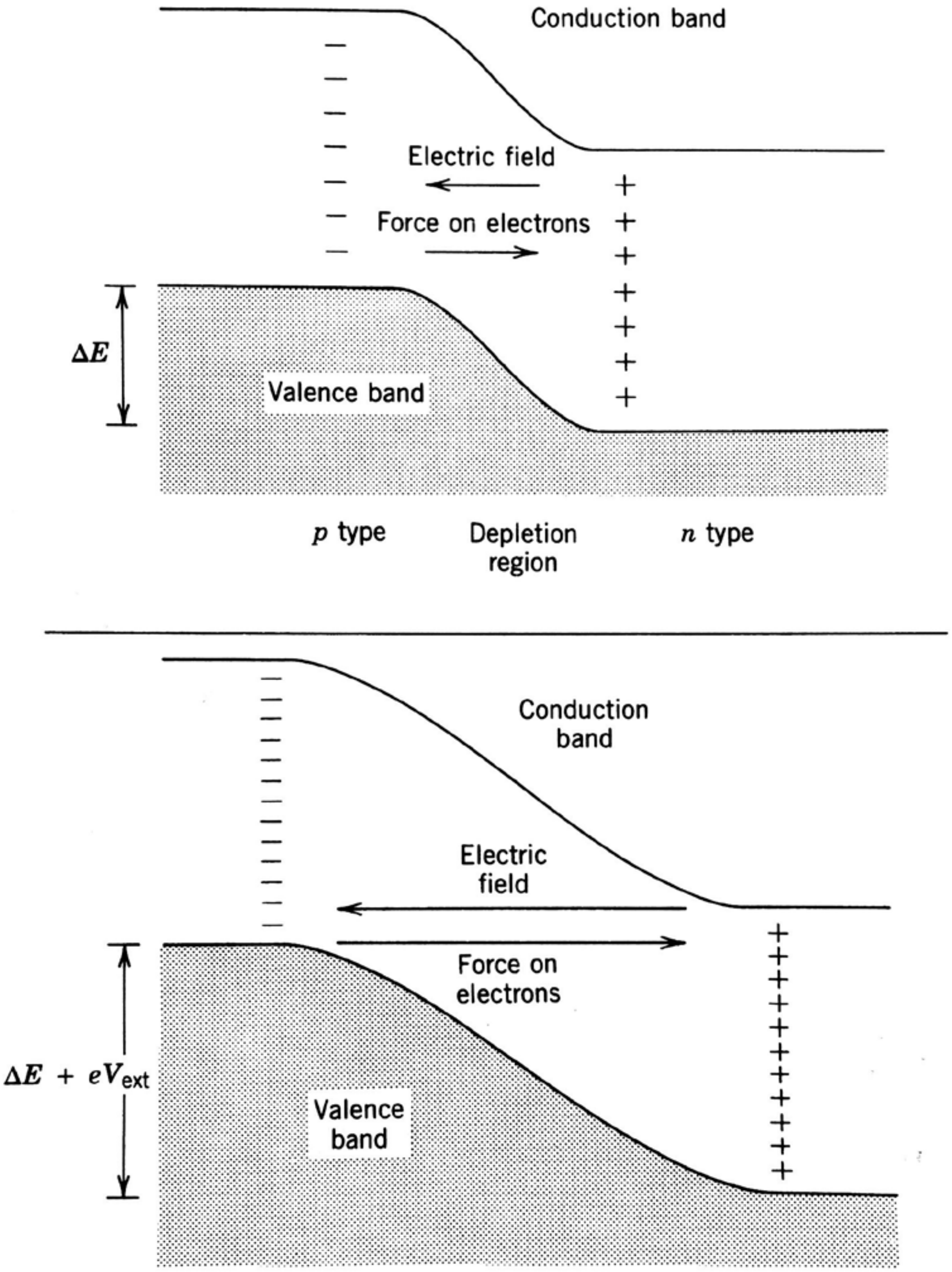


Fig. 2.5: Energy band diagram of a p-n junction used in semiconductor detectors: (top) When n-type ad p-type materials are brought into contact, electrons and holes near the junction can recombine to create a region that is depleted of charge carriers. (bottom) Under reverse bias (when the negative terminal of an external battery is connected to the p-type side), the depleted region becomes larger and the magnitude of the electric field increases. Figure taken from [23]

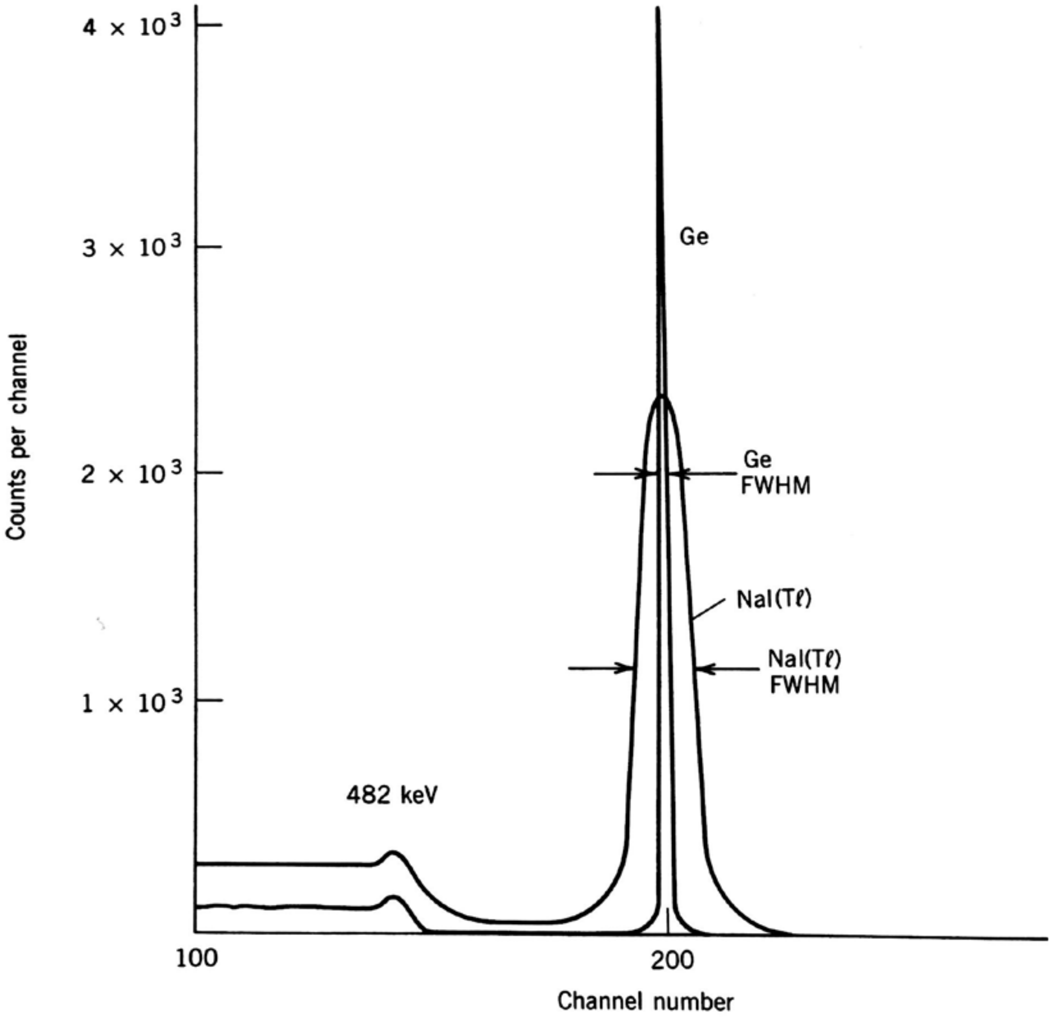


Fig. 2.6: Comparison of NaI(TI) and Ge(Li) spectra of ^{137}Cs. The energy of the photopeak is 662keV.The resolution (FWHM) of the NaI(TI) is about 40 keV, while that of the Ge is about 1 keV. The intensity (peak area) of the Ge is about 11% that of NaI(TI). Figure taken from [23].

2.4. Conclusion:

This chapter describes some of the most commonly known radiation detectors. Gas filled detectors are widely used since they are inexpensive. However, they are prone to damage if the contained gas leaks, which might result in inaccurate results. In comparison, scintillation counters are rugged, lightweight and more reliable. Their efficiencies and detection limits are also superior compared to the gas filled detectors. However, if energy resolution is a concern, performance of semiconductor detectors (specially HPGe detectors) exceeds both scintillation and gas filled detectors due to its capability to generate narrower FWHM. Interestingly, a recent technology known as bolometer detector is gaining attention since it can offer energy resolution even better than the semiconductor detectors with much higher efficiency [34], [35]. But unfortunately, the system is more complex compared to all the detector technologies discussed so far and difficult to operate as well. The good news is that there are many new technologies currently in research and development stage that have the potential to bring new capabilities in the radiation detection arena. The rest of the chapters will present two of such innovative technologies developed at Arizona State University that the scientific community might find interesting for radiation sensing applications.

CHAPTER 3

DEVELOPMENT OF METAL-CHALCOGENIDE GLASS BASED FLEXIBLE RADIATION DETECTORS

3.1. Background:

In this chapter, we present a novel metal-chalcogenide glass (ChG) based radiation detection sensors that can perform many of the functions of the commercial detectors while being far simpler in form, easy to operate and potentially cheaper to produce [36]. Chalcogenide glasses (ChG) are a recognized family of amorphous glass containing chalcogen atoms (sulfur (S), selenium (Se), Tellurium (Te)) in conjunction with more electropositive either group IV elements (i.e., Ge, Si) or group V elements (i.e., Sb, As) [37]. The properties of ChG are dependent on their composition. By changing the composition, these properties can be modified, which offers the opportunity to use them for various electronic, photonic and optoelectronic applications such as computer memory devices [38]-[40], flexible logic circuits [41], xerography [42], wave sensors [43], optical fibers [44], [45], solar cells, etc. [46], [47]. Our radiation detection system is basically a very easy to make laterally configured metal-ChG devices. They are fabricated on a mechanically flexible polymer substrate such as polyethylene naphthalate (PEN) by depositing a thin film of ChG followed by formation of metal electrodes on top of them [48]. Flexible sensors are potentially more useful than rigid variants as they can be readily (and conformally) attached to non-flat objects such as flasks, barrels, and pipes; and they are inherently more robust as they will resist breaking when mechanically stressed. They are also potentially lighter than rigid versions as they can be formed on thin plastic substrates, making them ideal candidates for wearable devices [48]. In addition, flexible substrates allow roll-to-roll processing and hence fabrication costs can be very low. When exposed to ionizing radiation, these lateral devices can sense radiation through migration of metal ions from the electrodes into intermediate ChG film regions. Before irradiation, they exhibit very high resistance state (~10^{11} **Ω**). The resistance between the electrodes drops to ~10^{3} **Ω** when they are radiated with either ^{60}Co gamma-ray or ultraviolet (UV) radiation. This significant reduction in resistance provides strong evidence for their use in radiation detection applications (although at the current stage of development the sensors are not reusable and exhibit saturation). They are suitable for applications in which absorbed dose ranges between 10^2 and 10^9 rad(GeSe) (e.g., reactor dosimetry, radiation chemistry, and clinical dosimetry) with fast readout [49].

The sensor development timeline can be broadly divided into three stages. First stage covers experiments carried out on the initial prototypes to demonstrate the radiation sensing concept. It also includes examination of the prototypes (irradiated samples) to observe their performance when exposed to mechanical stress (parallel and perpendicular stress, both tensile and compressive) and elevated operating temperature (Room temperature to 150^o C). Second stage primarily focused on studying the effect of physical design parameters (e.g., electrode spacings, electrode area, electrode thickness and ChG thickness) on the sensor operation. The main goal was to see if we can tune the sensor characteristic/ specification by changing the physical parameters to make them suitable for different range of applications. In the third stage, we extended our optimization study by concentrating on novel material systems beyond the default Ag-$Ge_{20}Se_{80}$ combination which was used in the previous phases. Here, he key purpose was to investigate the impact of varying (a) metals used to form contact electrodes and (b) chalcogenide glass atomic ratio/chemical composition on the performance of the sensors. For electrodes, three group 11 elements (i.e., copper, silver and gold) were used. For ChG film, either Ge_xS_{1-x} or Ge_xSe_{1-x} was used where the atomic ratio of the chalcogen atoms (i.e., sulfide, or selenide) was varied from device to device.

To help the readers to easily follow the discussion in the rest of chapter, we will name all the experiments performed under first stage (i.e., initial prototyping) as "Exp. A". Similarly, "Exp. B" will represent all the experiments performed under stage two (i.e., performance optimization study through physical design tuning) and "Exp. C" will stand for stage three investigations (i.e., performance optimization study exploiting novel material combinations).

In the next section (i.e., Section 3.2), we will start by presenting an overview of the sensor concept. Next, details of the sensor manufacturing process steps and device test protocol will be covered in Section 3.3. It will then be followed by experiment results and discussions obtained from all the three development stages in Section 3.4. Finally, Section 3.5 summarizes the conclusions drawn based on the experimental results.

3.2. Sensor Overview:

Since the mid-1960s, the special property of Ag dissolution into ChG has been studied [50]. When Ag migrates into ChG, it changes the electrical properties of the film by decreasing its resistivity [51]. The film resistivity depends on the atomic fraction of silver present in the Ag-ChG ternary compound. Compared to other pure metal films, the resistivity of the Ag-ChG film can be many orders of magnitude higher, even with a silver concentration as high as tens of atomic percent. This interesting property has made Ag-ChG based devices ideal for diverse applications. For instance, the effect of Ag photodoping in thin ChG films has led to development of high-resolution inorganic photoresists for optical lithography in semiconductor manufacturing [52], [53]. The addition of some metals into ChG can result in a significant increase in the electronic conductivity of the material [54], [55]. In case of cation (M+) migration, nano-scale group I elements (i.e., Ag or Cu) are dispersed into ChG to form binary and ternary solid electrolytes. These chalcogenide glass based solid electrolytes enable the essential resistance switching mechanism for Programmable Metallization Cells (PMC), a technology platform for Conductive Bridging Random-Access Memory (CBRAM) [56]-[59]. Lately, the impact of TID on the electrical characteristics of Ag-ChG devices has been investigated to understand their suitability for use in radiation environments [60]-[65]. The weak bonding that give ChG's their flexibility is also the source of their sensitivity to ionizing electromagnetic radiation, allowing some metals to be dissolved into their backbone structure when exposed [66]. The nature of the ChG allows for the generation of charges and defects as well as structural modifications upon exposure to high energy ionizing radiation. These radiation-induced processes facilitate the incorporation of Ag into ChG, thereby changing film conductivity which may be measured electrically [67]. The primary mechanism for the flexible sensors is radiation-induced diffusion of metal atoms, typically Ag, into the ChG (Ge_xSe_{1-x}, Ge_xS_{1-x} in our studies), which results in change in the resistivity of the glass. The more Ag dissolved in the ChG, the lower the resistance of the resulting Ag-Ge-Se ternary. In addition, sensor operation does not require an applied bias during exposure and can be related to the dose, via calibration and modeling, to provide an instantaneous readout at very low voltage. Fig. 3.1 shows the overview of the ChG sensor.

Undoped ChG films usually have very high resistance ($\sim 10^{11}\ \Omega$-m) [68], [69].

Fig. 3.1: ChG sensor overview: When the ChG sensors are exposed to ionizing radiation, the deposited energy causes Ag dissolution in ChG and the resulting resistivity change can be detected by the electrical resistance at the output.

However, after exposure to ionizing radiation (e.g., gamma rays), electron-hole pairs (ehp) are generated in the ChG. The increase in ehps in the films induces Ag transport into the ChG film. While the precise mechanisms are not fully understood, it is generally thought that radiation-induced "photodoping" is caused by both (either) Ag ionization through charge transfer with generated holes and (or) negative charge buildup from slow moving (or trapped) electrons in the glass. The combination of these two processes leads to the formation of an electrochemical potential between the positively charged Ag+ ions and negatively charged electrons. This causes Ag+ ions to drift into the undoped ChG region to form Ag-ChG ternaries [70]-[75].

During ionizing radiation exposure, incorporation of these Ag+ ions will continue until the ChG film becomes saturated with Ag or the source of surplus Ag+ ions is depleted [36]. The buildup of Ag in the glass results in a significant decrease in film resistivity, measured as resistance change between two surface electrodes [68], [76]. Radiation sensing can be quantitatively performed by measuring the substantial changes in the electrical resistance of the glass, especially when the doping fronts from two nearest electrodes make contact. Fig. 3.2 presents a typical “evolution of resistance” plot of the Ag-ChG flexible sensor devices in response to increasing ionizing dose level. The term limit of detection (LOD) indicates the dose level where the undoped/high resistance state (HRS) starts to decrease sharply in response to increased dose level and the dynamic range (DR) is the ratio between the undoped/HRS and doped/low resistance state (LRS).

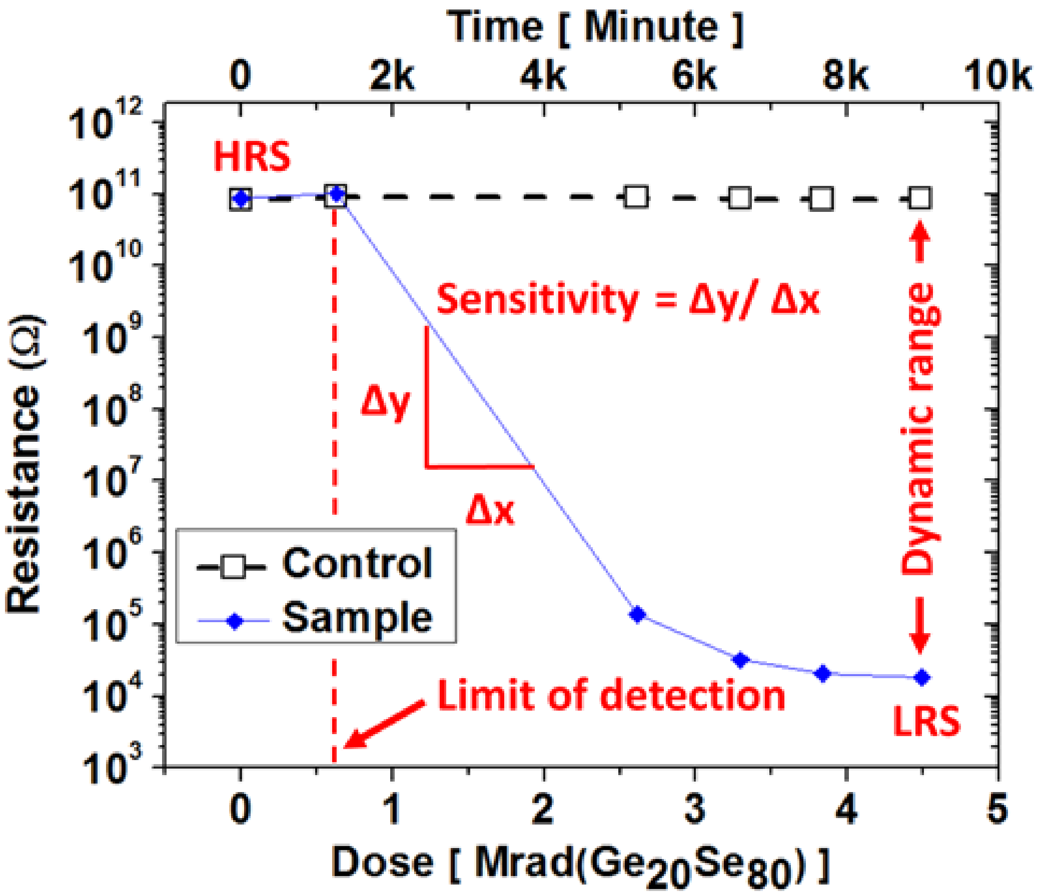


Fig. 3.2: Typical "evolution of resistance" plot of the Ag-ChG flexible sensor devices in response to increasing ionizing dose level. Geometry of these sensor devices such as electrode size and spacing shows significant influence on determining the dynamic range (DR) and the limit of detection (LOD).

3.3. Sensor Device Fabrication:

3.3.1. Exp. A sample fabrication (initial prototyping)

Out of many substrate choices, we choose one side pre-treated, heat stabilized flexible polyethylene-naphthalate (PEN) substrates manufactured by DuPont Teijin Films due to their smooth surface, low coefficient of thermal expansion, low shrinkage and rigidity. This lightweight and transparent substrate is ideal for fabricating metal-ChG based flexible radiation sensors due to their compatibility for use on non-flat objects. The manufacturing process of the radiation sensors discussed in this chapter is very simple and cost effective. For Exp. A., we manufactured samples with a simple shadow mask that has a single array of electrodes with constant spacings (i.e., 1 mm spacing between two adjacent electrodes) and fixed electrode area (i.e., 2 mm diameter). The basic sensor fabrication method involves: (1) deposition of a thin ChG film, in this case $Ge_{20}Se_{80}$, on a flexible substrate and (2) formation of soluble Ag electrodes. The Ag electrodes supply the metal into the underlying ChG during exposure as well as providing the electrical connection to the layer for resistance measurement [36]. The $Ge_{20}Se_{80}$ composition was chosen as Ag diffuses rapidly in this Se-rich material [77]. In addition, and just as importantly for this application, the low processing temperature (detailed below) and very high elastic modulus of the $Ge_{20}Se_{80}$ based glass makes this material an ideal choice for fabricating ChG on flexible substrates. Low processing temperature is necessary as most (low cost) polymer substrates cannot withstand high temperatures (e.g., over 180°C). It should be noted that the low hardness values, brittleness factor, hardness, and Young's modulus of the material are much lower than silicate glass [78]; and as a result, ChG films demonstrate more elastic deformation for the same amount of stress [79]. The fabrication sequence is depicted in Fig. 3.3.

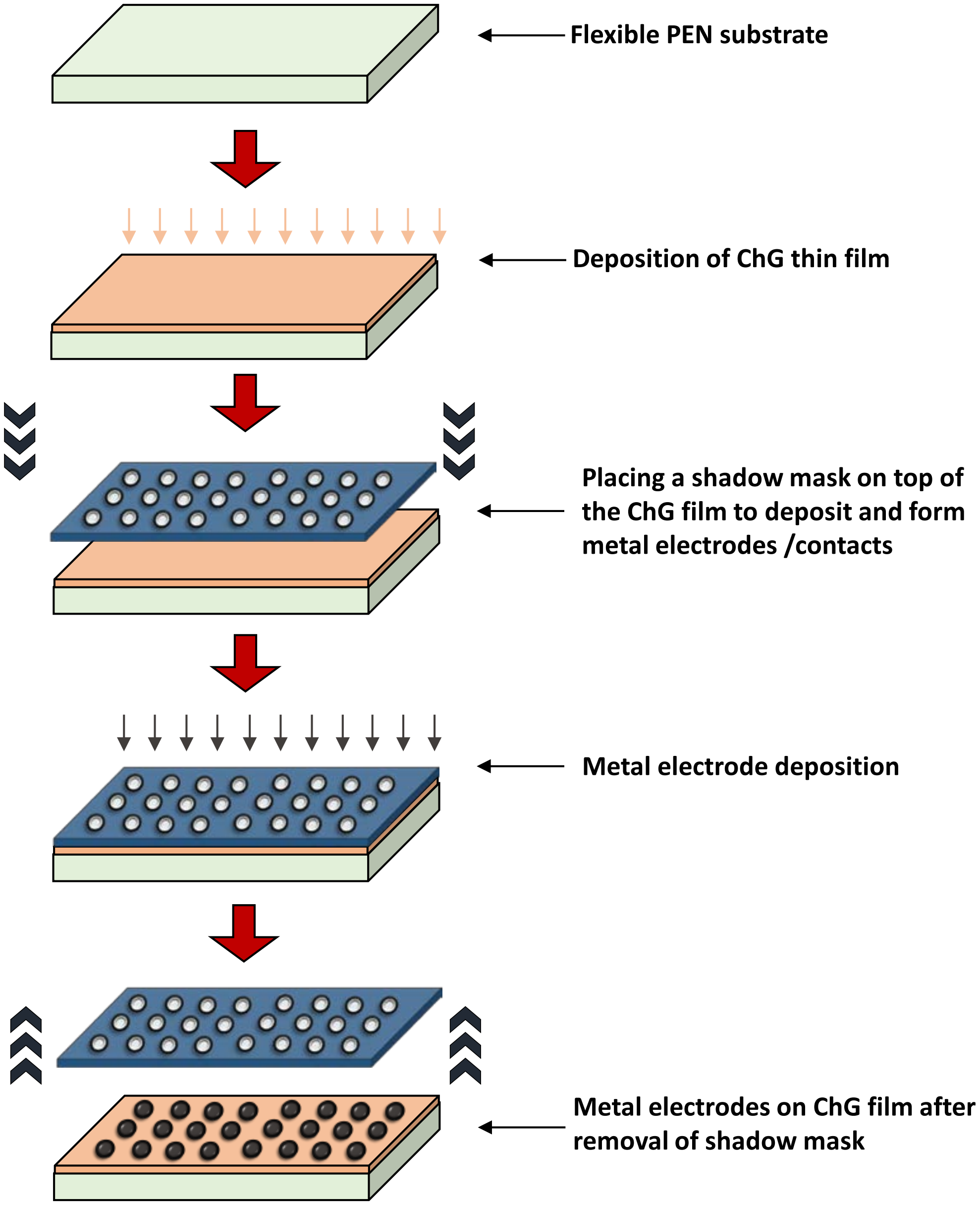
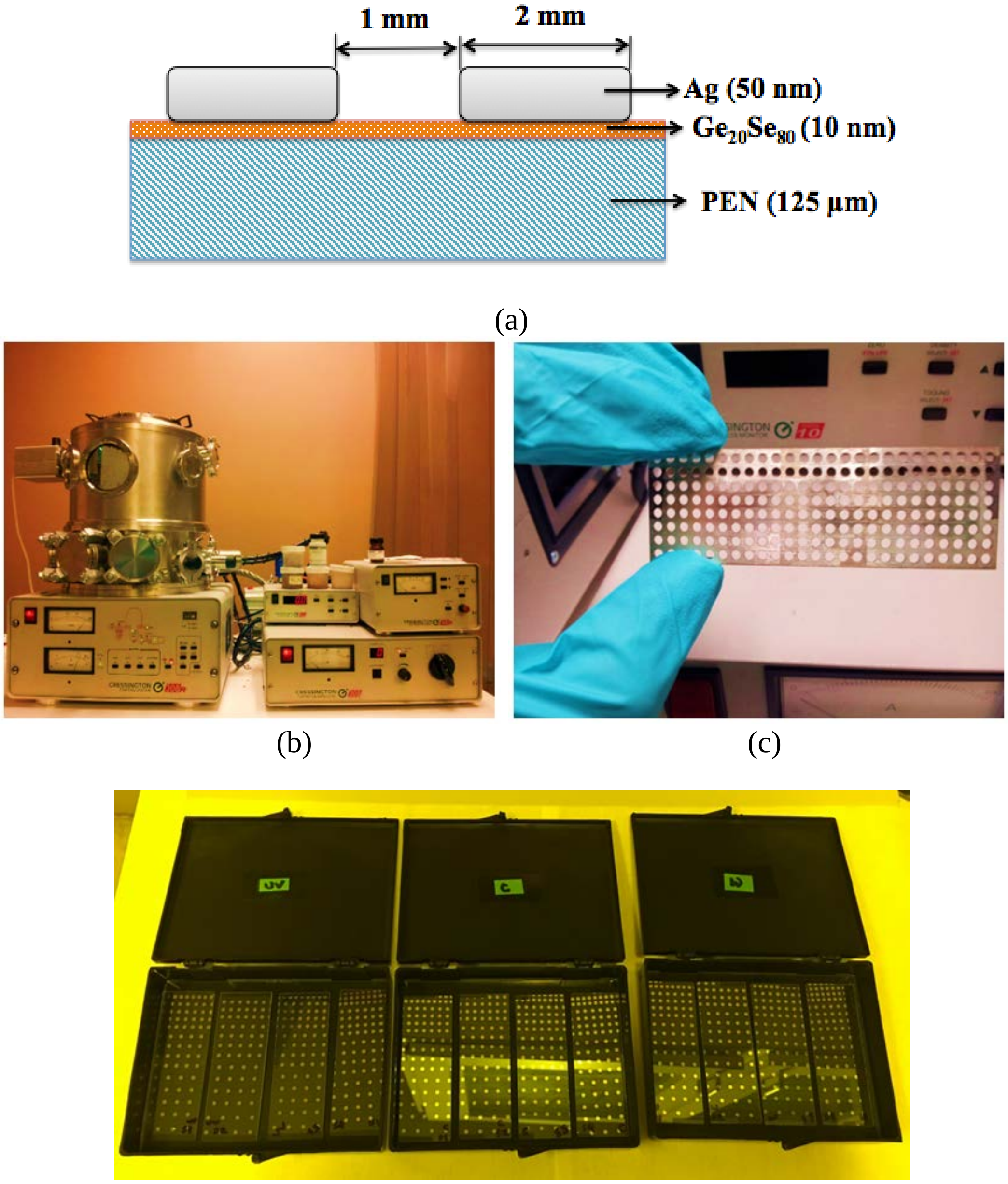


Fig. 3.3. The simple fabrication process flow that was closely followed to manufacture Exp. A, Exp. B and Exp. C samples. Though it should be mentioned that the film and electrode thickness, electrode placement and materials were different for different samples.

The manufacturing process begins with room temperature blanket deposition of 10 nm $Ge_{20}Se_{80}$ on a 125 µm thick polyethylene napthalate (PEN) flexible substrate at a rate of 0.01 nm/sec using a Cressington 308 evaporator. Next, a shadow mask with a specific pattern (i.e., arrays of circular shaped holes) is placed on top of the deposited film and 50 nm thick Ag electrodes are deposited using the same tool at 0.1 nm/sec at room temperature. While manufacturing, we put maximum effort to reduce the time between the above two deposition steps to minimize exposure of the ChG film to atmosphere. Extended exposure might grow unwanted oxides on ChG and deteriorate the Ag-ChG interface quality which might result in poor performance. The Ag electrodes are used as contact pads for the quasi static DC electrical measurement as well as the source of Ag^+ ions that transport into ChG when exposed to ionizing radiation. Both the control and exposed devices were manufactured at the same time to reduce variability. The sensor cross-section is shown in Fig. 3.4 (a). The thermal evaporator (i.e., Cressington 308) that was extensively used to manufacture the samples are shown in Fig. 3.4 (b) and Fig. 3.4 (c) shows the single array shadow mask that was used to manufacture Exp. A. and some Exp. B. samples. ‘

3.3.2. Exp. B sample fabrication (Performance optimization- Physical design tuning)

For Exp. B., three different sets of sensors were manufactured to study the effect of electrode spacings and area on the sensor performances. They are: (i) sensors with 2 mm fixed electrode diameter and variable intermediate spacing between nearest electrodes ranging from 1 to 5 mm, (ii) sensors with fixed 2 mm intermediate spacing and variable electrode diameter of 2 and 8 mm, and (iii) sensors with fixed 3 mm intermediate spacing and variable electrode diameter of 3 and 4 mm. All of them were manufactured on the 125 µm thick flexible polymer substrate using three different sets of shadow masks (Fig. 3.5).



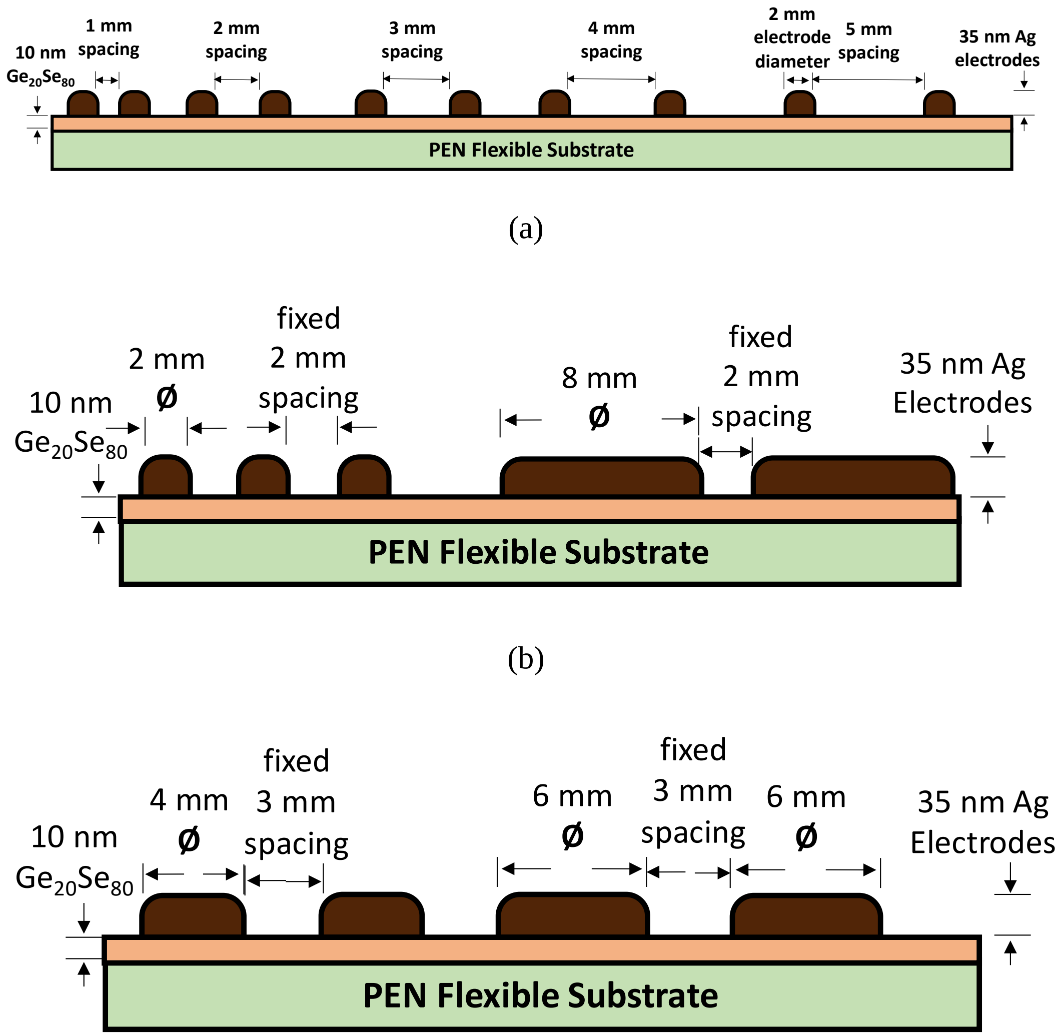
(a)

(b)

(c)

(d)

Fig. 3.4. (a) Cross-sectional schematic of the Exp. A. sensor layout. (b) The Cressington 308 thermal evaporator that was used to manufacture the samples. (c) The single array shadow mask that has electrodes of 2 mm diameter and spacings of 1mm. (d) Manufactured samples stored inside black boxes to reduce exposure to daylight.



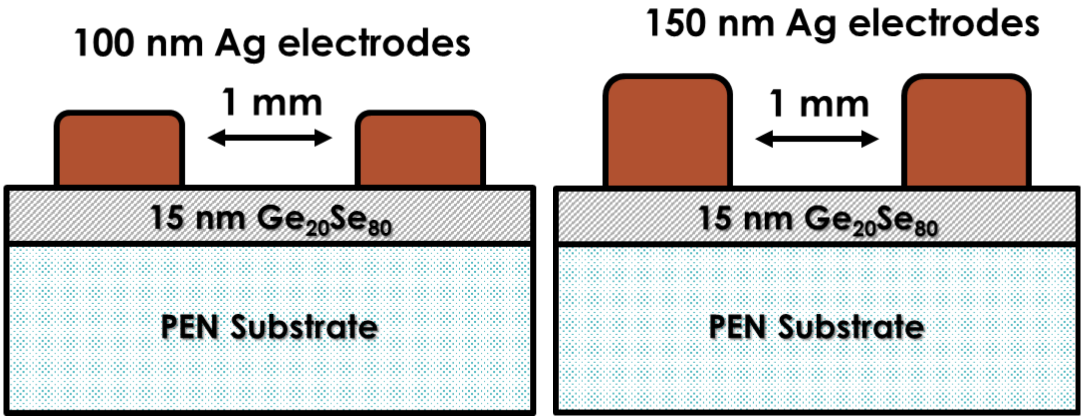
(a)

(b)

(c)

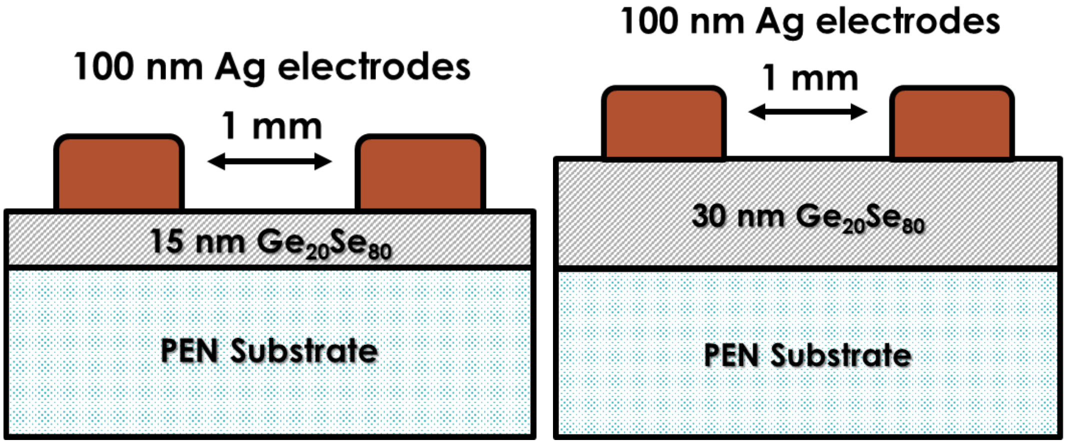
Fig. 3.5. Cross-section view of the Exp. B. manufactured samples with different electrode spacings and electrode area: (a) samples with fixed electrode diameter of 2 mm and variable spacing of 1, 2, 3, 4 and 5 mm. Photograph of the freshly manufactured samples with this geometry can be seen in Fig. 3.4-d. The bright circular dots on the samples represent silver electrodes. (b) samples with fixed spacing of 2 mm and variable electrode diameters of 2 and 8 mm (c) samples with fixed spacing of 3 mm and variable electrode diameters of 4 and 6 mm.

Similar to Exp. A. samples, the manufacturing process begins with room temperature blanket deposition of 10 nm $Ge_{20}Se_{80}$ on a flexible substrate at a rate of 0.01 nm/sec using a Cressington 308 thermal evaporator. Next, a shadow mask is placed on top of the deposited film and 35 nm thick Ag electrodes are deposited using the same tool at 0.1 nm/sec at room temperature. For samples with different metal electrode thickness, we first deposited 15 nm of $Ge_{20}Se_{80}$ film on the PEN substrate. Then we diced the substrate into two equal pieces. In one piece, we deposited 100 nm of Ag electrodes using the Exp. A. shadow mask (i.e., 2 mm electrode diameter, 1 mm spacings). On the other piece, we deposited 150 nm of Ag electrodes using the same mask. For both cases, Ag deposition was performed using the Cressington 308 evaporator. Fig. 3.6 shows the cross-section of Exp. B. samples with different electrode thickness.



(a) (b)

Fig. 3.6: Cross-section view of the Exp. B. samples with different electrode thickness: (a) devices with 100 nm of Ag electrodes. (b) devices with 150 nm of Ag electrodes.



(a) (b)

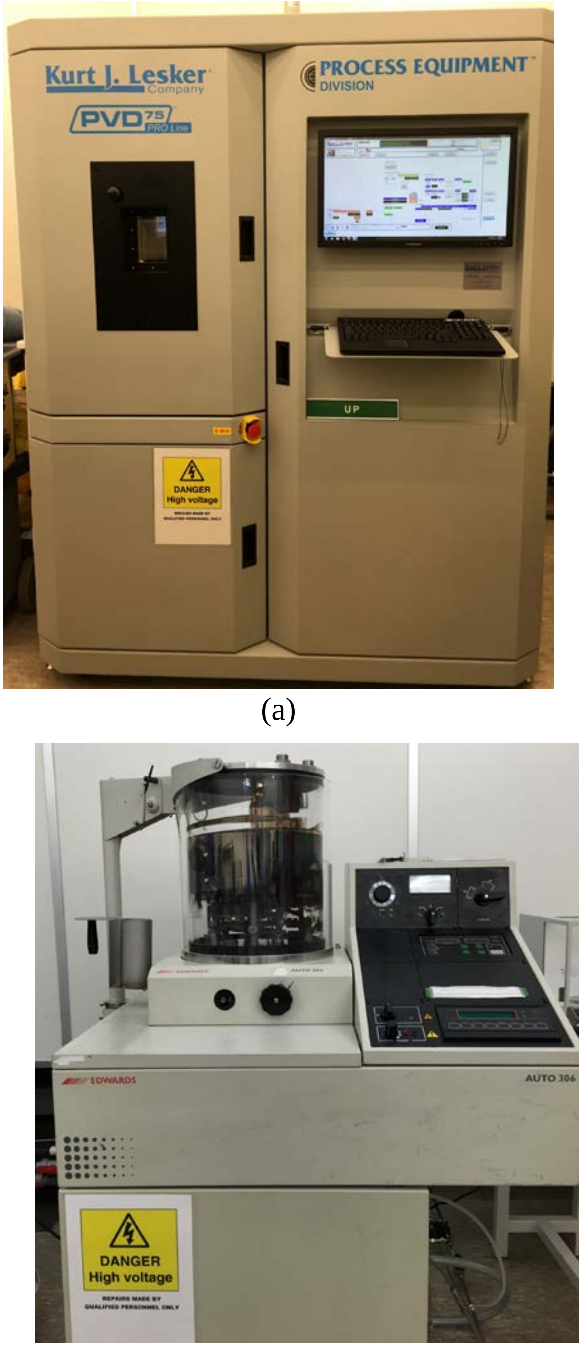
Fig. 3.7: Cross-section view of the Exp. B. samples with different ChG thickness: (a) devices with 15 nm of ChG film (b) devices with 30 nm of ChG film.

For samples with different ChG film thickness, we took two pieces of PEN substrate. On one of the pieces, we deposited 15 nm of $Ge_{20}Se_{80}$ and on the second substrate, we deposited 30 nm of $Ge_{20}Se_{80}$. Both substrates were then loaded inside the Cressington 308 using the same Exp. A. shadow mask to deposit 100 nm of Ag electrodes. Fig. 3.7 shows the cross-section of Exp. B. samples with different ChG thickness.

3.3.3. Exp. C sample fabrication (Performance optimization- New materials)

For Exp. C., we manufactured samples with different material combinations. Besides of using Ag, we made devices with Cu and Au electrodes. Our primary goal in this phase (i.e., Exp. C) was to check the viability of using these different combinations of group 11 metal-ChG systems, to manufacture the sensors and study their performance. The remaining group 11 metal, roentgenium, was not considered since it is an extremely radioactive synthetic element [80]. We also wanted to understand if ChG chemical composition and the ratio of the chalcogen atoms/Ge in combination with the different type of metals used for the electrodes can be exploited to regulate the performance characteristics of the sensors. An ultimate result of this study is finding the optimal materials' combinations suitable for further development of these types of radiation sensors. Thus, in addition to changing metal electrodes, we also used ChG films of different composition (i.e., selenides, sulfides) and atomic ratio (i.e. Ge_xSe_{1-x}, Ge_xS_{1-x}).

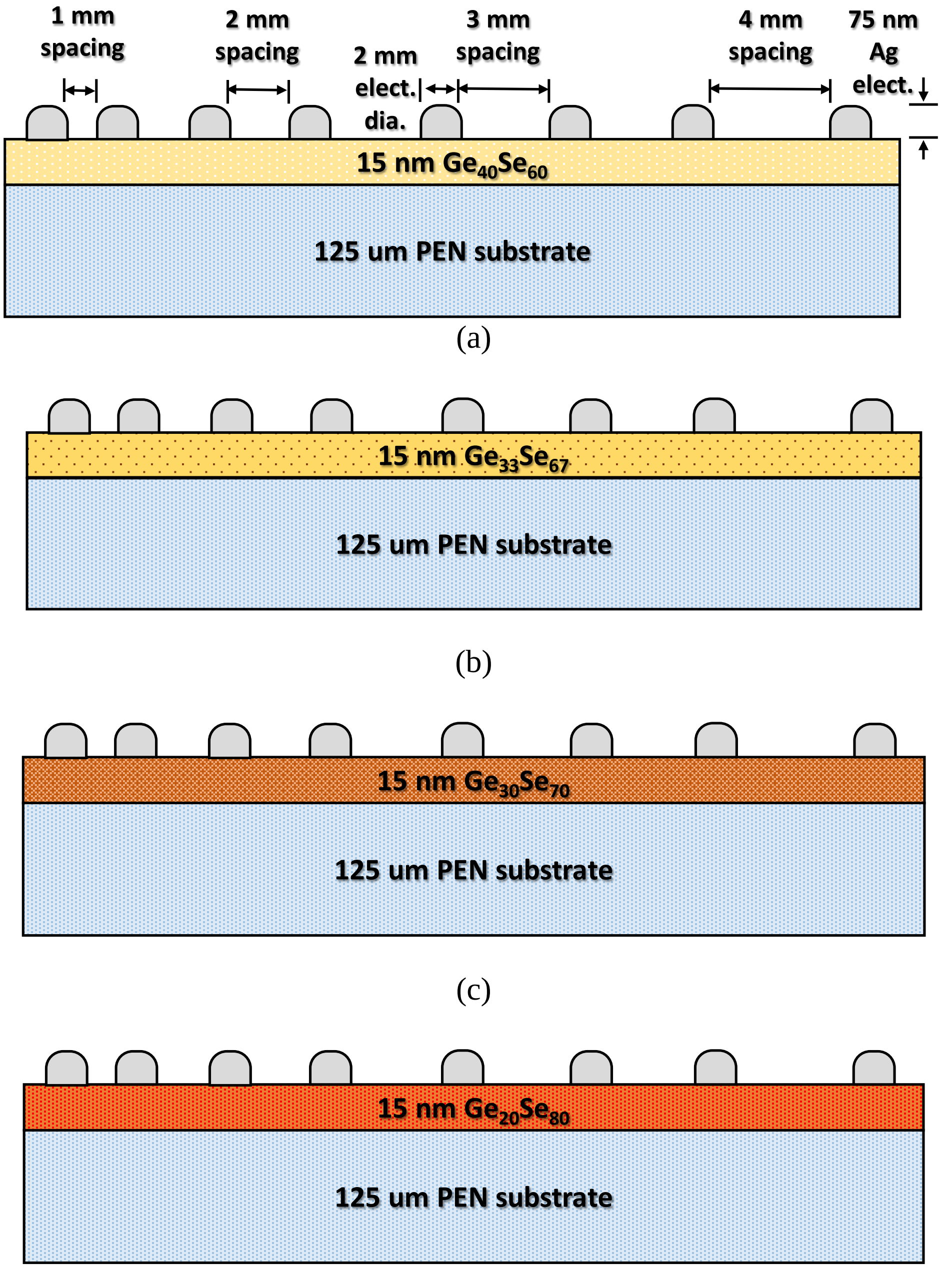
To help the readers to easily follow the experimental process of Exp. C., we again introduce a naming format that is used to denote different samples. For instance, samples with $Ge_{20}Se_{80}$ thin film and Au electrodes are named as Au_$Ge_{20}Se_{80}$. Similar naming formats are used for other Ag_Ge_xSe_{1-x}, Ag_Ge_xS_{1-x}, Cu_Ge_xSe_{1-x} and Cu_Ge_xS_{1-x} based systems. The manufacturing process of the sensors begins with the deposition of the thin ChG film. To fabricate samples with $Ge_{40}Se_{60}$ film (i.e., Ag_$Ge_{40}Se_{60}$ and Cu_$Ge_{40}Se_{60}$ samples), first a 100 mm by 100 mm square shaped PEN substrate was loaded inside a thermal evaporator (Cressington 308). Then, 15 nm of $Ge_{40}Se_{60}$ film was deposited at a rate of 0.1 nm/sec at room temperature. The substrate with ChG film was then diced into two equal sized 100 mm by 50 mm pieces. Each of these two pieces was used to manufacture samples with two different metal electrodes (i.e., Ag and Cu). To deposit the metal electrodes, a shadow mask was used that has several arrays of electrodes. For all the arrays, the diameter of the electrodes was fixed to 2 mm and spacing between nearest electrodes was varied from 1 mm to 4 mm. We opted for this particular square lattice type geometry in order to observe how the spacing between electrodes plays a role in the radiation induced diffusion process. Ag and Cu electrodes were deposited using an e-beam evaporator (PVD 75, Kurt J. Lesker Company®) shown in Fig 3.8 (a). For both cases, 75 nm thick metal films were deposited at a rate of 1 Å/s at room temperature to form the electrodes. Upon completion, the shadow mask was removed. Then, each of the 100 mm by 50 mm substrates were further diced into two equal sized 100 mm by 25 mm pieces to have both control and exposure samples from the same manufacturing batch in order to reduce the effects of process related variability. Since the devices are sensitive to the UV component of visible light, they were immediately stored inside dark boxes to minimize uncontrolled exposure. Similar processes were performed to manufacture other selenide (i.e., Ag_$Ge_{33}Se_{67}$, Cu_$Ge_{33}Se_{67}$, Ag_$Ge_{30}Se_{70}$, Cu_$Ge_{30}Se_{70}$, Ag_$Ge_{20}Se_{80}$, and Cu_$Ge_{20}Se_{80}$) and sulfide (i.e., Ag_$Ge_{40}S_{60}$, Cu_$Ge_{40}S_{60}$, Ag_$Ge_{33}S_{67}$, Cu_$Ge_{33}S_{67}$, Ag_$Ge_{30}S_{70}$, Cu_$Ge_{30}S_{70}$, Ag_$Ge_{20}S_{80}$, and Cu_$Ge_{20}S_{80}$) based control and exposure samples. A pictorial process flow has previously shown in Fig. 3.3. The cross sections of all the completed Exp. C samples is given on Fig. 3.9. Images of one of the completed samples bent around a circular pipe is shown in Fig. 3.10.



(a)

(b)

Fig. 3.8: Tools used for Exp. C sample manufacturing: (a) E-beam evaporator (PVD 75, Kurt J. Lesker Company®) used for Ag and Cu electrode deposition (b) Thermal evaporator (Edwards Auto 306) used for Au electrode deposition.



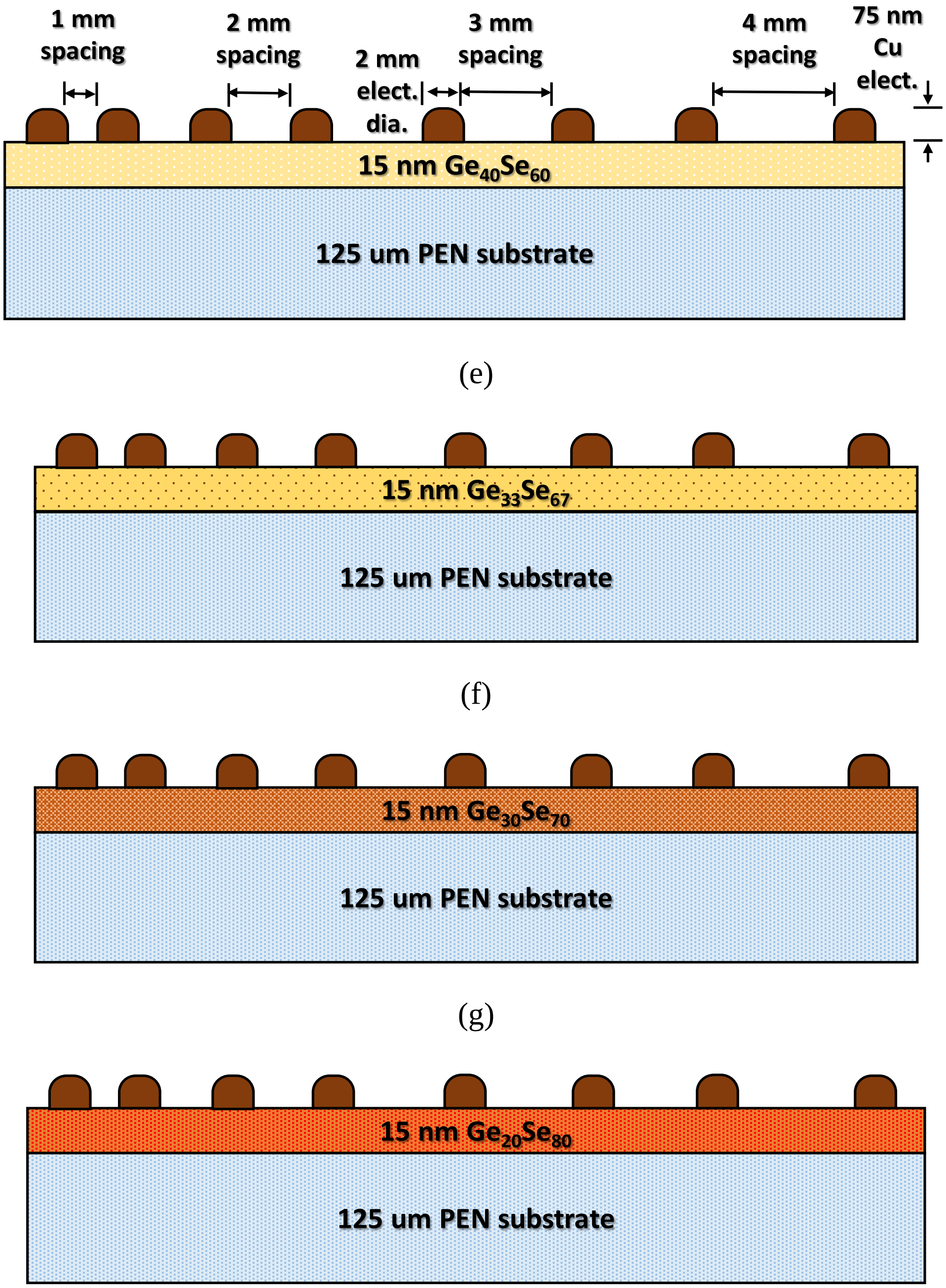
(a)

(b)

(c)

(d)

Fig. 3.9 (part 1 of 4): Cross-section of the Exp. C. samples those were made with Ag electrodes and selenide based ChG film of different atomic ratio: (a) Ag-$Ge_{40}Se_{60}$ (b) Ag-$Ge_{33}Se_{67}$ (c) Ag-$Ge_{30}Se_{70}$ and (d) Ag-$Ge_{20}Se_{80}$



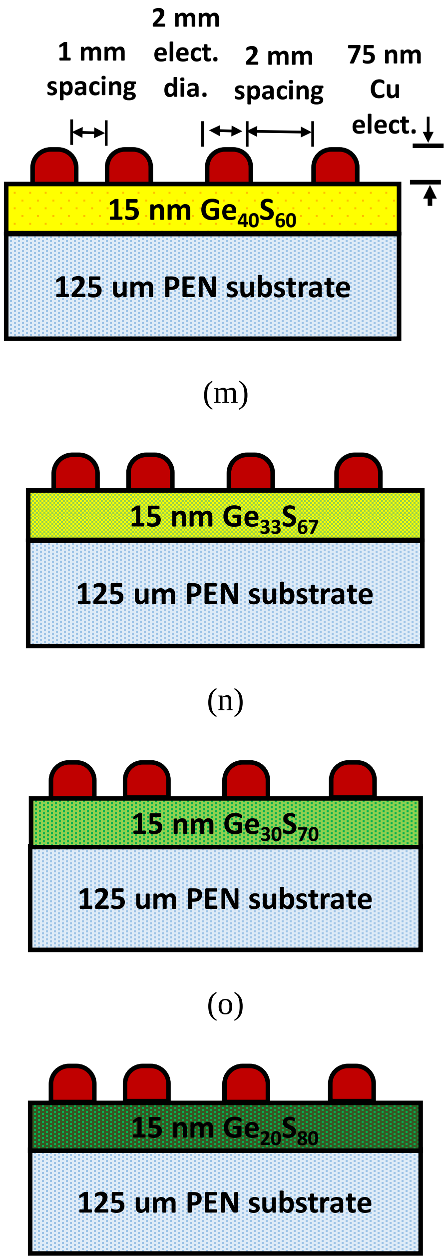
(e)

(f)

(g)

(h)

Fig. 3.9 (part 2 of 4): Cross-section of the Exp. C. samples those were made with Cu electrodes and selenide based ChG film of different atomic ratio: (e) Cu-$Ge_{40}Se_{60}$ (f) Cu-$Ge_{33}Se_{67}$ (g) Cu-$Ge_{30}Se_{70}$ and (h) Cu-$Ge_{20}Se_{80}$



(m)

(n)

(o)

(p)

Fig. 3.9 (part 4 of 4): Cross-section of the Exp. C. samples those were made with Cu electrodes and sulfide based ChG film of different atomic ratio: (m) Cu-$Ge_{40}S_{60}$ (n) Cu-$Ge_{33}S_{67}$ (o) Cu-$Ge_{30}S_{70}$ and (p) Cu-$Ge_{20}S_{80}$

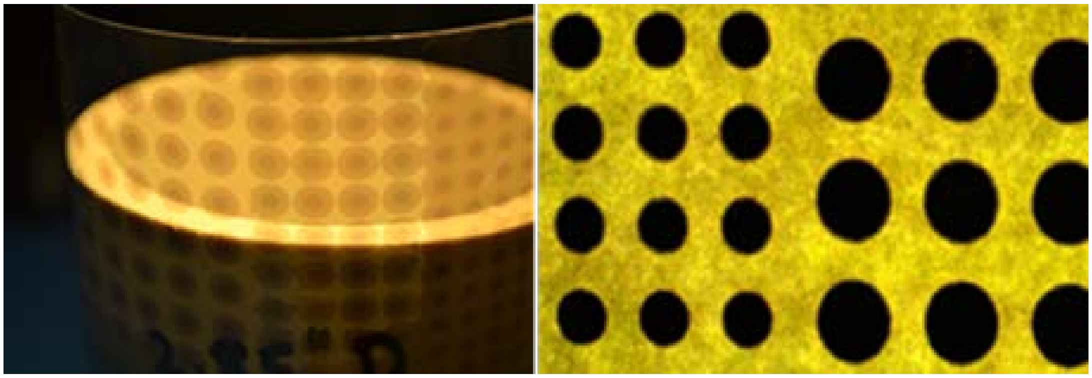


Fig. 3.10: Manufactured samples bent around a 2.58 inch diameter pipe.

For devices with Au electrodes, we only used $Ge_{20}Se_{80}$ for our preliminary study since they have a relatively low packing factor and the highest concentration of chalcogen atoms [81]. Both material packing and chalcogen concentration are potential triggers for radiation-induced doping processes. If transport of Au into $Ge_{20}Se_{80}$ is not observed in the exposed samples for TID > 3 Mrad(Ge_xSe_{1-x}), it is less likely to see the diffusion with other Ge_xSe_{1-x} and Ge_xS_{1-x} compositions. For Au_$Ge_{20}Se_{80}$ devices, a similar technique was used to deposit the 15 nm of $Ge_{20}Se_{80}$. A shadow mask with an array of 2 mm diameter of electrodes and 1 mm spacing was attached on top of the $Ge_{20}Se_{80}$ coated substrate and 75 nm of Au was deposited at 0.1 nm/s rate using a thermal evaporator (Edwards Auto 306) at room temperature. After removal of the shadow mask, the substrate was diced into two pieces to create the control and test samples and these were stored in a dark box as well. The cross section of Au-$Ge_{20}Se_{80}$ system is shown in Fig. 3.11. Since the thermal evaporator (i.e., Cressington) we have used has a substrate holder that can hold only one (100 mm) wafer sized sample, we needed to manufacture all the different sets of samples in separate batches. However, for all the Exp. A. to Exp. C. samples, we fabricated both the control and exposed devices of a particular set at the same time to reduce variability (i.e., both the control and exposed devices were part of the same batch).

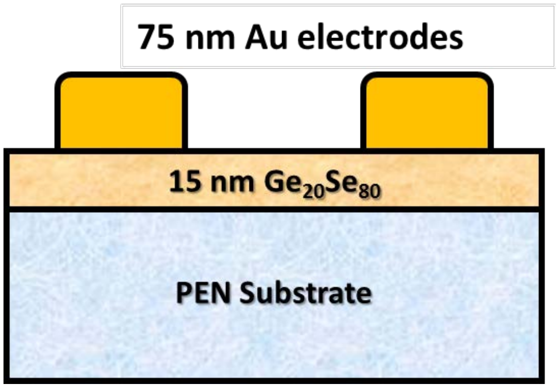


Fig. 3.11: Cross-section of Au-$Ge_{20}Se_{80}$ based system (Exp. C.)

3.4. Test Protocol:

3.4.1. Exp. A test protocol (initial prototyping)

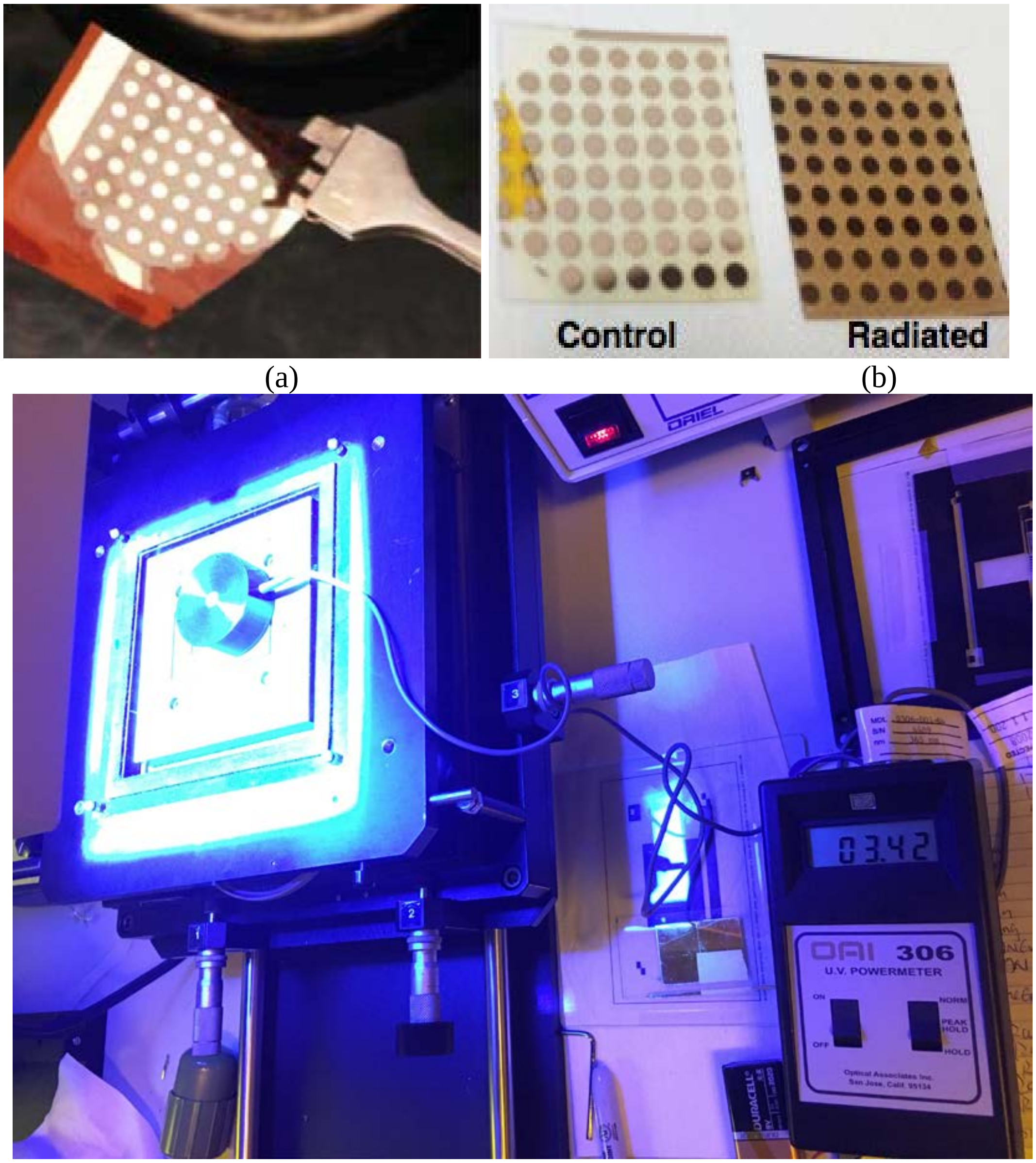
For Exp. A. samples, to assess device performance, the test samples were exposed to UV light at power density of 3.42 mW/cm^2 at a wavelength of 365 nm for a 1 h exposure (Fig. 3.12-c). This corresponds to a total energy absorption density of 12.31 J/cm^2. The use of UV light was shown in our previous studies [36] to be a simple and convenient substitute for ionizing radiation as both generate charged carriers and induce the dissolution of the metal into the ChG film. Samples, irradiated with UV doses up to 57.6 J/cm^2 (as shown in Fig. 3.12) and unexposed control samples, were monitored to detect Ag incorporation optically during the testing. For ^{60}Co gamma-ray exposure, the samples were placed in a Gammacell 220 irradiator with a dose rate of 477.5 rad($Ge_{20}Se_{80}$)/min. Increase of temperature over room temperature during the irradiation cannot be expected since the fluence is quite low and the films are very thin. The samples were periodically removed from the Gammacell to measure the change in electrical resistance with respect to increasing dose levels. Samples were exposed to a maximal total ionizing dose (TID) of 5.13 Mrad($Ge_{20}Se_{80}$) and the samples were left floating (electrodes unconnected) during the exposures. Resistance measurements were performed at room temperature using semiconductor parameter analyzers (SPA, Agilent 4155B for devices exposed to UV, and 4156C for devices exposed to ^{60}Co gamma-rays). The resistance between two adjacent Ag electrodes was monitored for 100s at 10 mV bias. The low measurement bias was necessary to minimize redox reactions at the electrodes but also demonstrate that these devices do not require high voltage for readout. For devices in the unexposed state, the range of current measured was around 1 pA. As a consequence, while characterizing these sensors in their high resistance state (HRS) using Agilent 4156C parameter analyzer (without kelvin connections), a small range of variation in resistance level can be considered as normal [82].

The sensor devices were bent around tubes of various radii for 96 hours. The resistance measurement of the sensors while subjected to mechanical stress is illustrated by the photographs in Fig. 3.13. While, this test plan was our initial choice, but connection issues with the measurement probes (due to non-flat object) made us unable to correctly perform the testing. Thus, we revised the test plan and took the resistance measurements before and after bending (by re-flattening the sensors after mechanical stress). The tensile stress was applied by bending the devices outward while compressive stress was applied with inward bending. All bending radii (R) are converted to percent strain (ε) by

$$\varepsilon = \frac{T_{PEN} + T_{Film}}{2 * R_c} * 100 \ , \qquad (3.1)$$

where T_{PEN} is the thickness of PEN substrate (125 µm), T_{Film} is thickness of the sensor film (~ 10 nm) and R_c is the bending curvature radius of the substrate [83]. A bending radius of 5 mm therefore corresponds to 1.25 % strain.

The effects of exposure to elevated temperatures on the performance of the sensors were investigated to assess how these devices would perform in high temperature environments. Devices exposed to UV light and control samples were heated on a hot plate to 75, 100, 125 and 150°C for 1 hour and resistance between adjacent electrodes was measured following the temperature stress.



(a) (b)

(c)

Fig. 3.12: (a) Array of Exp. A. ChG sensors on a flexible copper-polyimide substrate. (b) Unexposed and UV exposed sensor array on a flexible PEN substrate. The devices are 10 nm thick $Ge_{20}Se_{80}$ film and the devices were saturated after 57.6 J/cm^2 of UV dose. (c) Samples are shown irradiated with a 365 nm wavelength of UV source at power density of 3.42 mW/cm^2.

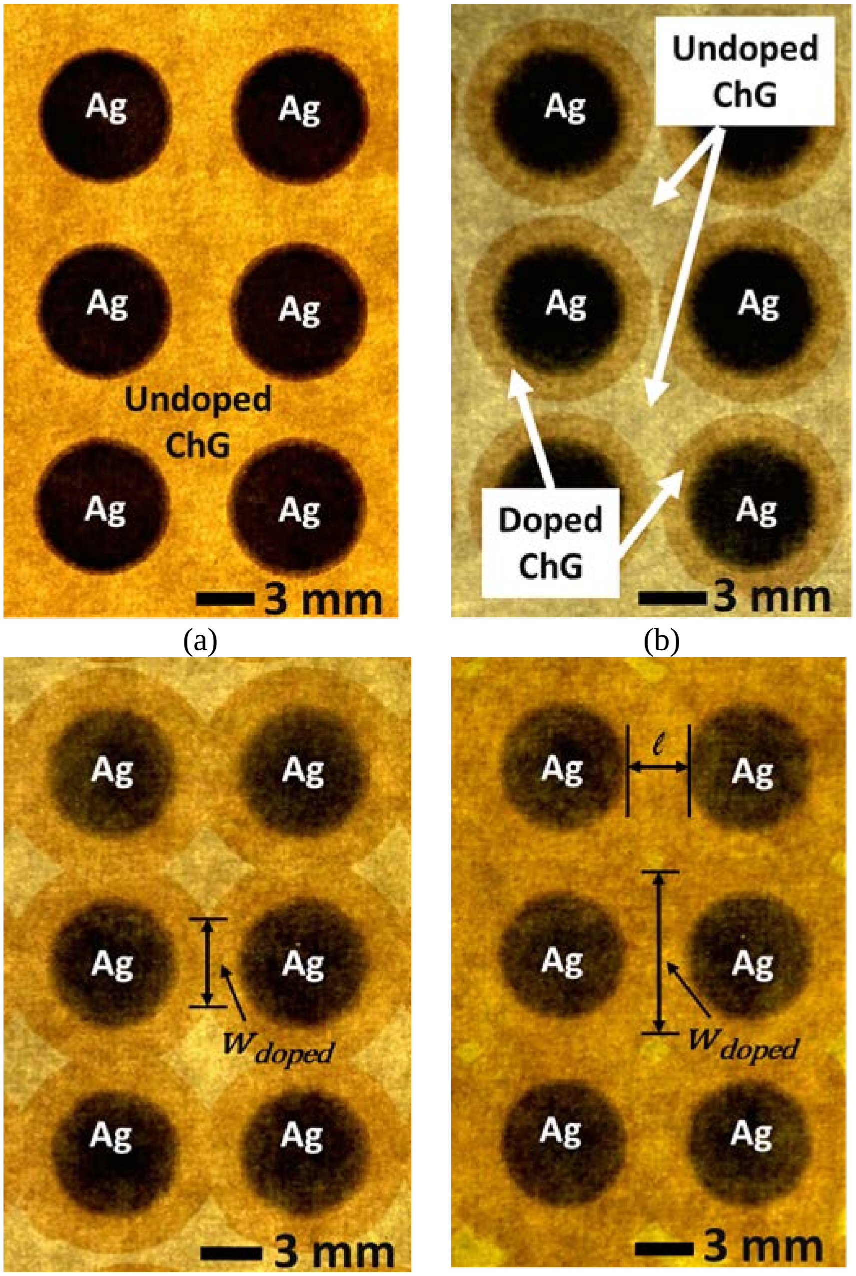
Fig. 3.13: Resistance measurement of Exp. A. sensor arrays while subjected to mechanical stress.

3.4.2. Exp. B test protocol (Performance optimization- Physical design tuning)

For Exp. B. samples, after completing fabrication, samples were placed into a Gammacell 220 for ^{60}Co gamma-ray exposure at a dose rate 477.5 rad($Ge_{20}Se_{80}$)/min. They were periodically unloaded from the Gammacell chamber for a short amount of time to measure the electrical resistance between nearest electrodes using a semiconductor parameter analyzer (Agilent 4156C). The same measurements were performed on unexposed control samples. To avoid oxidizing the silver electrodes, a small bias voltage (10 mV) was used when sampling the resistance. Optical images were taken after each measurement step to visually monitor the transport of Ag from the surface electrodes into $Ge_{20}Se_{80}$ film at increasing dose levels. Fig. 3.14 shows photographs of a test sample where the electrode diameter is 6 mm and spacing l is 3 mm. The images of the sensors were taken after each measurement step: (a) prior to irradiation and after (b) 1.31 Mrad($Ge_{20}Se_{80}$), (c) 2.55 Mrad($Ge_{20}Se_{80}$), and (d) 4.56 Mrad($Ge_{20}Se_{80}$). These figures reveal the radiation-induced transport of Ag from the surface electrodes into $Ge_{20}Se_{80}$ film. Figs. 3.14(c) and 3.14(d) also show how, once the Ag doping fronts from adjacent electrodes make contact, the width of the doped region, w_{doped}, will increase with dose level.

The ^{60}Co gamma ray exposures were continued up to a maximum dose level of 4.56 Mrad($Ge_{20}Se_{80}$) for the samples those were manufactured to study the effect of electrode spacings and area. On the other hand, the ^{60}Co gamma ray exposures were continued up to a maximum dose level of 3.45 Mrad($Ge_{33}Se_{67}$) for the samples those were manufactured to study the effect of electrode and ChG film thickness on the sensor performance. During exposure, all the test samples were left floating by keeping the electrodes unconnected. Fig. 3.15 shows optical images of the control and test samples after the 4.56 Mrad($Ge_{20}Se_{80}$) exposures. This particular set of samples has a 2 mm fixed electrode diameter and the spacing between two adjacent electrodes is varied from 1 to 5 mm.

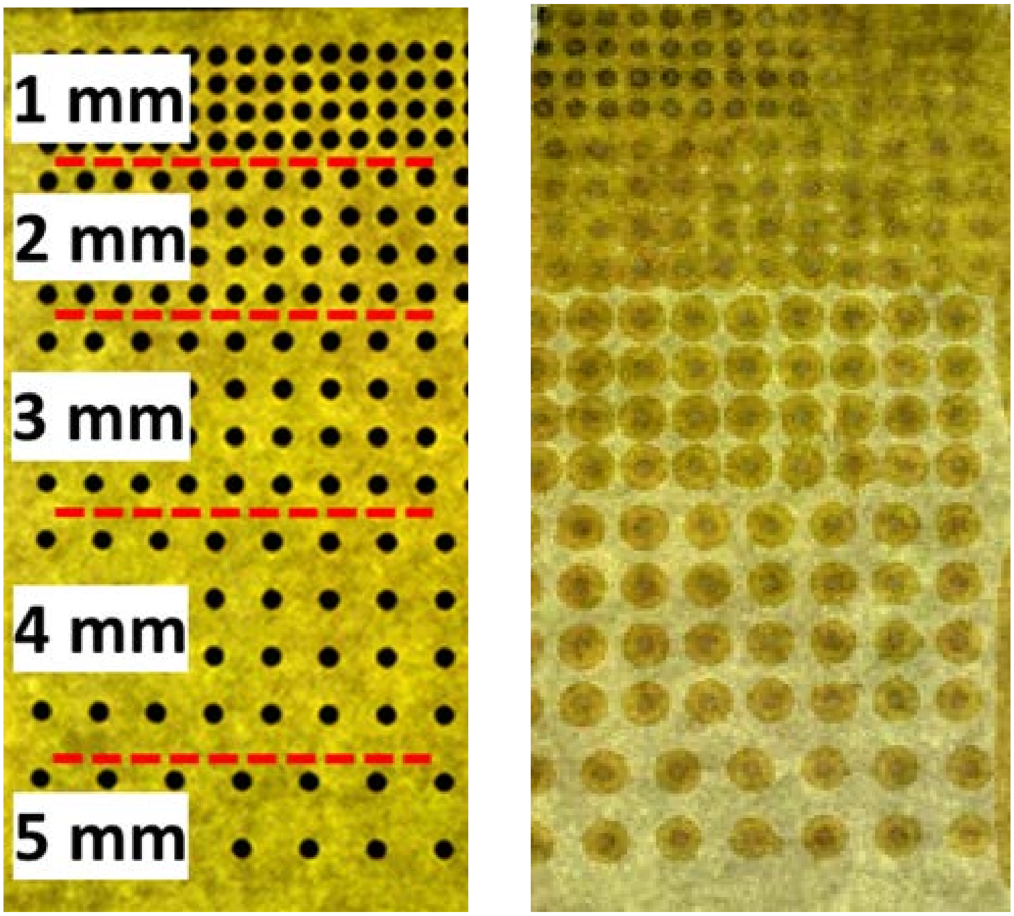
Fig. 3.16(a) shows the irradiation of the samples using gammacell 220 and Fig 3.16(b) shows the resistance level measurement between two adjacent electrodes using a probe station.



(a) (b)

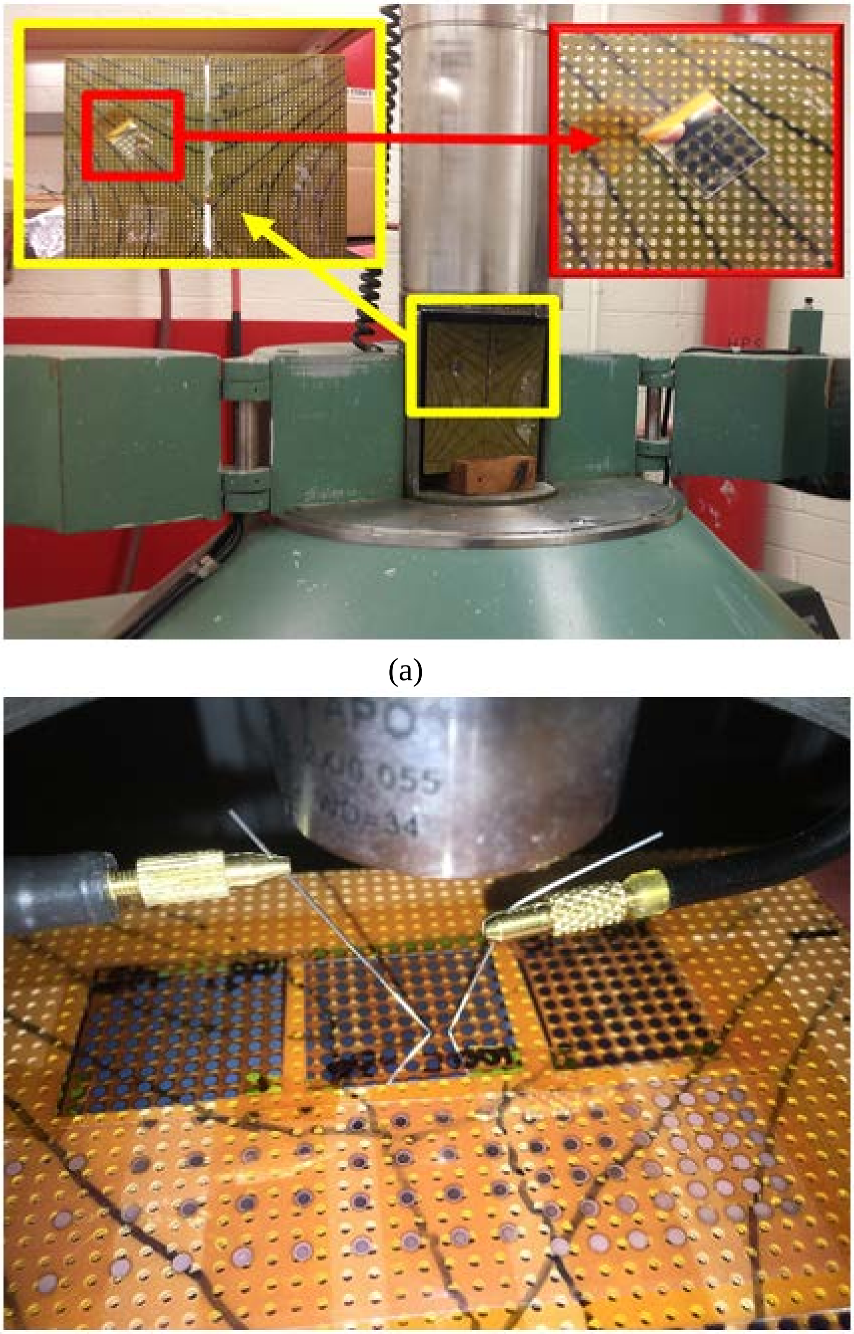
(c) (d)

Fig. 3.14: Optical illustration showing lateral dissolution of Ag into $Ge_{20}Se_{80}$ ChG films in response to increasing dose level. The electrode diameter of this particular test sample is 6 mm and the spacing (*l*) between them is 3 mm. (a) Shows the pre-exposure state of the samples. The remaining images show the radiation induced doping process of Ag: (b) after 1.31 Mrad($Ge_{20}Se_{80}$), (c) after 2.55 Mrad($Ge_{20}Se_{80}$), and (d) after 4.56 Mrad($Ge_{20}Se_{80}$). The parameter w_{doped} is the width of the doped region that increases with dose level.



(a) (b)

Fig. 3.15: Optical images of (a) control and (b) test samples after 4.56 Mrad($Ge_{20}Se_{80}$) dose level. The samples have arrays of electrodes of fixed 2 mm diameter and variable spacing of 1, 2, 3, 4 and 5 mm between the adjacent electrodes.



(a)

(b)

Fig. 3.16: (a) The samples were irradiated with ^{60}Co gamma ray using gammacell 220 irradiator. (b) Irradiated samples were periodically unloaded from the gammacell in order to probe the adjacent electrodes to measure their resistance level evolution using Agilent 4155C parameter analyzer.

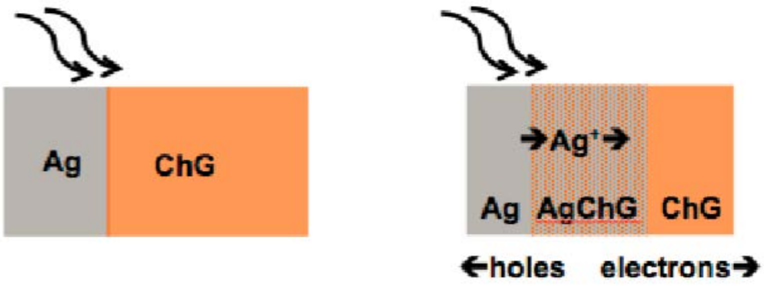
3.4.3. Exp. C test protocol (Performance optimization- New materials)

For Exp. C., all the exposure samples were irradiated at room temperature by a Gammacell 220 ^{60}Co irradiator. The selenide exposure samples were exposed at a dose-rate of 358 rad(Ge_xSe_{1-x})/min and the sulfide exposure samples were exposed at a dose-rate of 383 rad(Ge_xS_{1-x})/min. All the exposure samples were periodically unloaded from the Gammacell chamber for a brief period to measure the electrical resistance between adjacent electrodes within a particular array using a semiconductor parameter analyzer (Agilent 4156C). Similar measurements were performed on unexposed control samples within the same time [82]. The ^{60}Co gamma ray exposure continued up to a maximum dose level of 3.34 Mrad(Ge_xSe_{1-x}) for Au_$Ge_{20}Se_{80}$ samples, 3.45 Mrad(Ge_xSe_{1-x}) for the Ag_Ge_xSe_{1-x} and Cu_Ge_xSe_{1-x} selenide exposure samples and finally 3.68 Mrad(Ge_xS_{1-x}) for the Ag_Ge_xS_{1-x} and Cu_Ge_xS_{1-x} sulfide exposure samples. During exposure, all the test samples were left floating by keeping the electrodes unconnected. To avoid electrochemical oxidation of the metal electrodes, a very small bias voltage (10 mV) was used to measure the resistance level similar to previous Exp. A-B samples.

3.5. Results and Discussion:

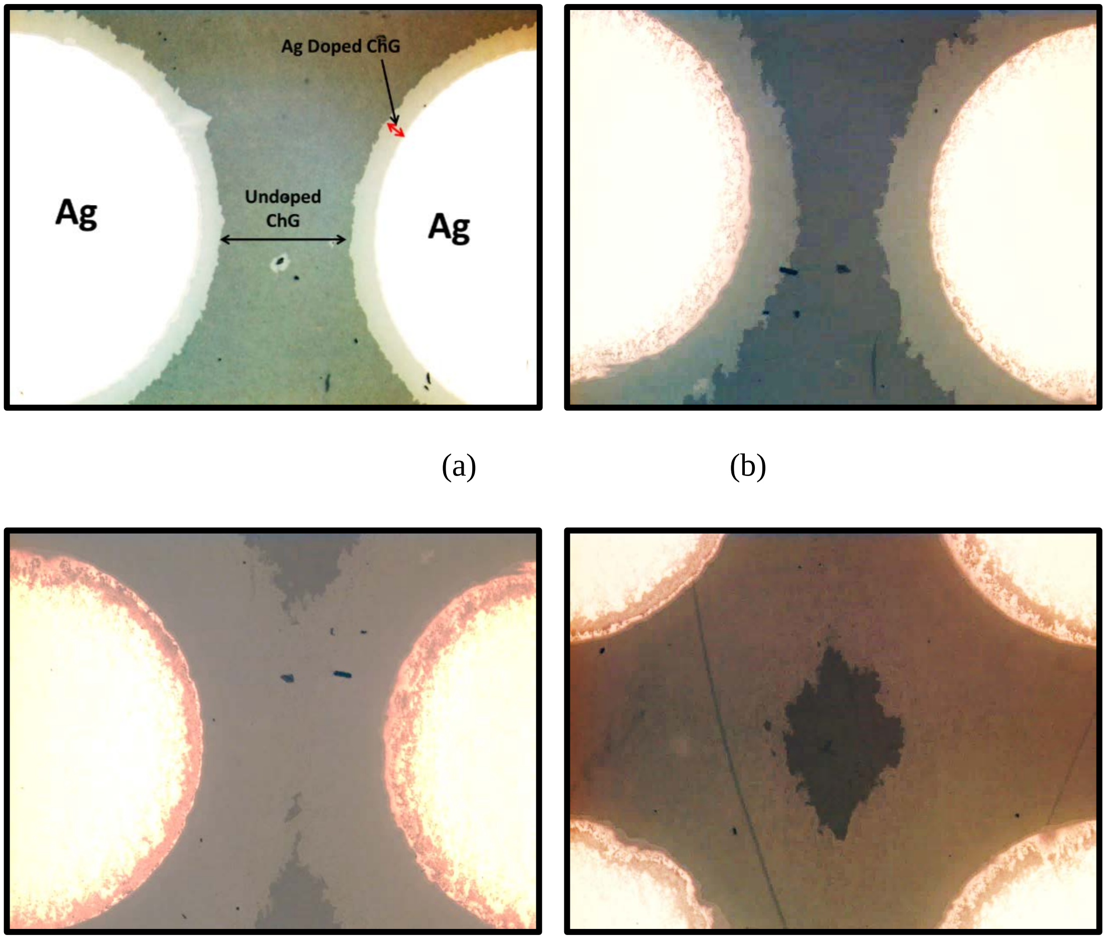
3.5.1. Exp. A Results (initial prototyping)

The metal photo-dissolution behavior observed in chalcogenide glasses has been extensively studied in recent years because of its potential application in producing high-resolution lithography, electrochemical resistive memory devices and optical components. Figs. 3.17(a) & 3.17(b) show the photo-doping process at Ag/ChG interface under irradiation. In the case of the photo-dissolution of Ag, light illumination creates charged defects in the ChG and the photocarriers absorbed at the Ag-ChG junction cause the diffusion of the Ag into the glass. The presumed mechanism [71] is that the Ag metal traps holes and the junction potential causes electrons to move deeper into the ChG film and become trapped there. Fig. 3.18(a) shows an optical micrograph of an unexposed 10 nm thick $Ge_{20}Se_{80}$ film with Ag electrodes formed on its surface. Prior to exposure to gamma-rays, the device is in its high resistance state(HRS) of around 10^{11} Ω (i.e., resistance between two nearest electrodes), since the undoped ChG (no Ag in film) acts primarily as a dielectric layer between the electrodes.



(a) (b)

Fig. 3.17: (a, b) illustration of the the photo-doping process at the Ag-ChG



(a) (b)

(c) (d)

Fig. 3.18: (a-d) Optical micrographs show evolution of ^{60}Co gamma irradiation induced Ag lateral diffusion in a 10 nm thick $Ge_{20}Se_{80}$ device on a flexible PEN substrate: (a) after 680krad ($Ge_{20}Se_{80}$) (b) after 1.22Mrad ($Ge_{20}Se_{80}$) (c) and (d) after 1.87Mrad ($Ge_{20}Se_{80}$).

The lateral progression of Ag (diffusion front) into the film is observed in Figs. 3.18(b) as a change in contrast of the ChG in the micrograph, but it is obvious that an undoped ChG layer still exists between the Ag diffusion fronts (Fig. 3.18-b). After 1.22 Mrad($Ge_{20}Se_{80}$), as shown in Fig. 3.18(b), the Ag has diffused laterally but an undoped ChG layer remains between the two electrodes. Hence, at this TID, the device remains in a high resistance state. Fig. 3.18(c) and 3.18(d) show a further diffusion of the Ag at TID close to 2 Mrad($Ge_{20}Se_{80}$). There are no longer undoped regions in the ChG layer and the resistance between adjacent electrodes drops to low-resistance state (LRS). HRS and LRS can interchangeably called as device OFF and ON state.

The evolution of resistance obtained after ^{60}Co gamma exposure is presented in Fig 3.19. It is important to note here that reduction of resistance (from $10^{11}\ \Omega$ to $10^{9}\ \Omega$) of some of the unexposed control samples were observed during our data collection. This reduction occurs due to the natural dissolution process of silver into the chalcogenide glass when exposed to daylight and background radiation. This unwanted silver transport in the controls can be minimized by storing the samples inside dark box and reducing visible light exposure.

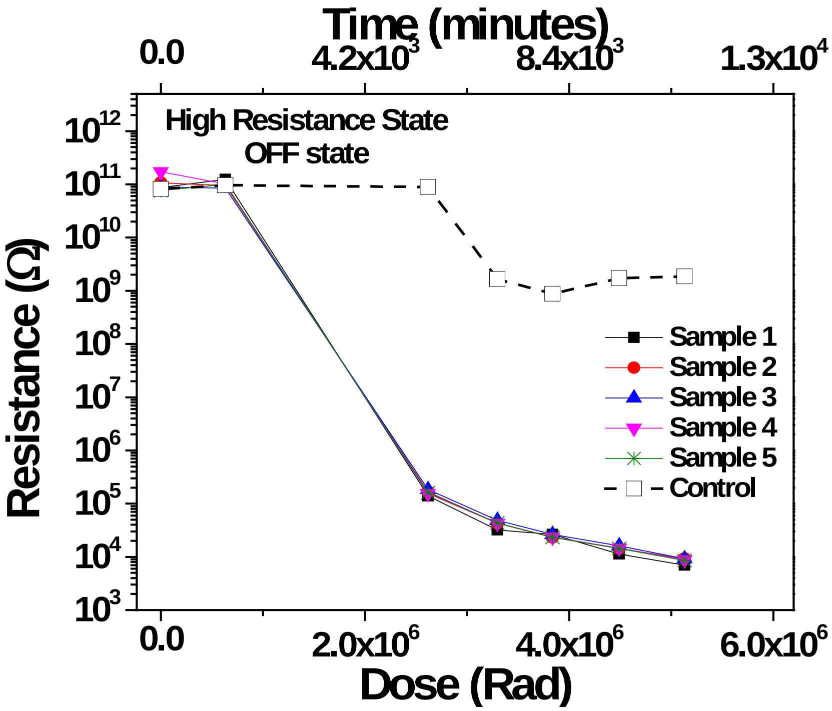


Fig. 3.19: Evolution of resistance prior to exposure, and after exposure to 630 krad($Ge_{20}Se_{80}$), 2.61 Mrad($Ge_{20}Se_{80}$), 3.29 Mrad($Ge_{20}Se_{80}$), 3.83 Mrad($Ge_{20}Se_{80}$), 4.49 Mrad($Ge_{20}Se_{80}$) and 5.21 Mrad($Ge_{20}Se_{80}$)

For samples irradiated with UV light, a similar decrease of the resistance has been observed as well. For those UV exposed devices, prior to exposure, the device is in a high resistance state of around 10^{12} Ω, since the undoped ChG (no Ag in film) acts as a dielectric layer between the electrodes. After 19.22 J/cm^2 of UV exposure, the Ag has diffused laterally by more than 0.5 mm between the electrodes. A complete "saturation" of the ChG film with Ag is observed at 43.25 J/cm^2 of UV exposure.

As mentioned previously, the simple room temperature fabrication method developed in this study and the flexibility of the $Ge_{20}Se_{80}$ based glass enables the manufacture of flexible sensor structures. However, the performance of the sensor under bending stresses should also be assessed to ensure that the materials do not undergo major electrical changes as a result of stress. Fig. 3.20 shows the change in ON-state resistance when the exposed device is subjected to parallel and perpendicular stress, both tensile and compressive.

For all measurements, several sensor samples were bent for 96 h on cylindrical surfaces of various radius and then probed on a flat surface to measure their resistance.

As shown in Fig. 3.20, the ON-state resistance of the device did not show significant degradation and falls within the range of resistance values of sensor devices measured before bending (in the order of 10 – 12 kΩ). Excessive bending strain, caused by bending with radius < 2 mm, induced cracks along the sensor electrodes and this increased the device resistance to around 10^6 Ω (this could be related to the cracks generated at the fringes of the substrate while the substrate was cut for mechanical strain). The unexposed samples did not show any Ag diffusion related to bending strain and retained their OFF-state resistance (around 10^{12} Ω).

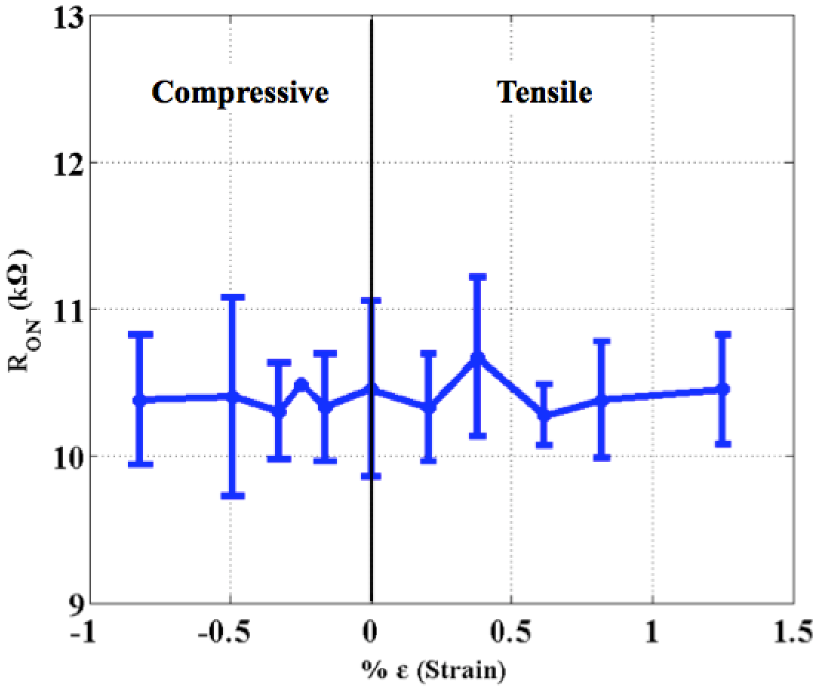


Fig. 3.20: ON-state resistance as a function of applied strain (ε). OFF-state resistance is ~ 10^{12} Ω.

Finally, the effect of elevated operating temperature on sensor characteristics was assessed. Fig. 3.21 shows the ON-state resistance as a function of temperatures between room temperature and 150 °C.

Once again, the ON-state resistance falls within the range of resistance values of the sensor devices measured before temperature stressing (10 – 12 kΩ). Although the OFF-state resistance shows no change with temperature, it is understood that prolonged high-temperature annealing could cause silver diffusion in the ChG [71].

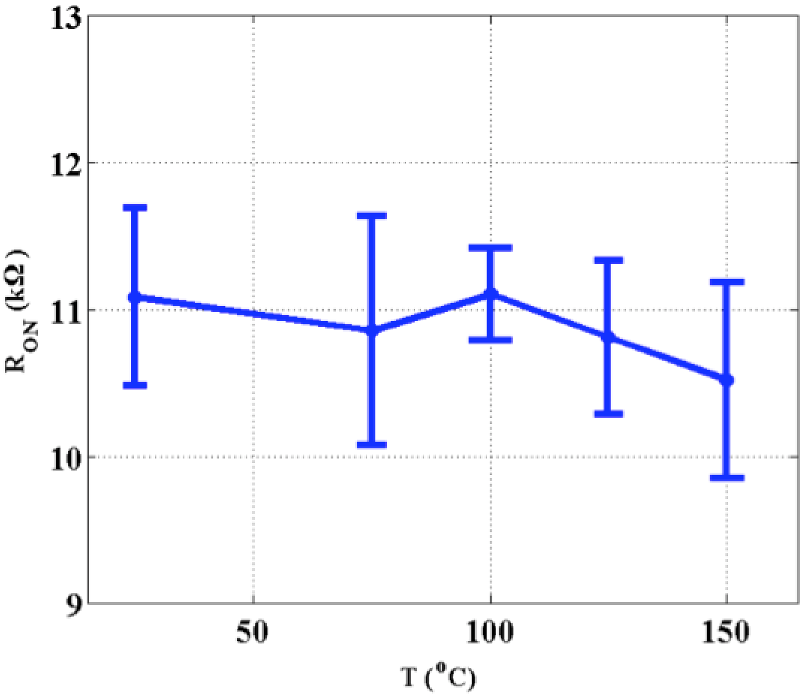


Fig. 3.21: ON-state resistance as a function of temperature annealing T (^OC). OFF-state resistance is ~ 10^{12} Ω

3.5.2. Exp. B results (Performance optimization- Physical design tuning)

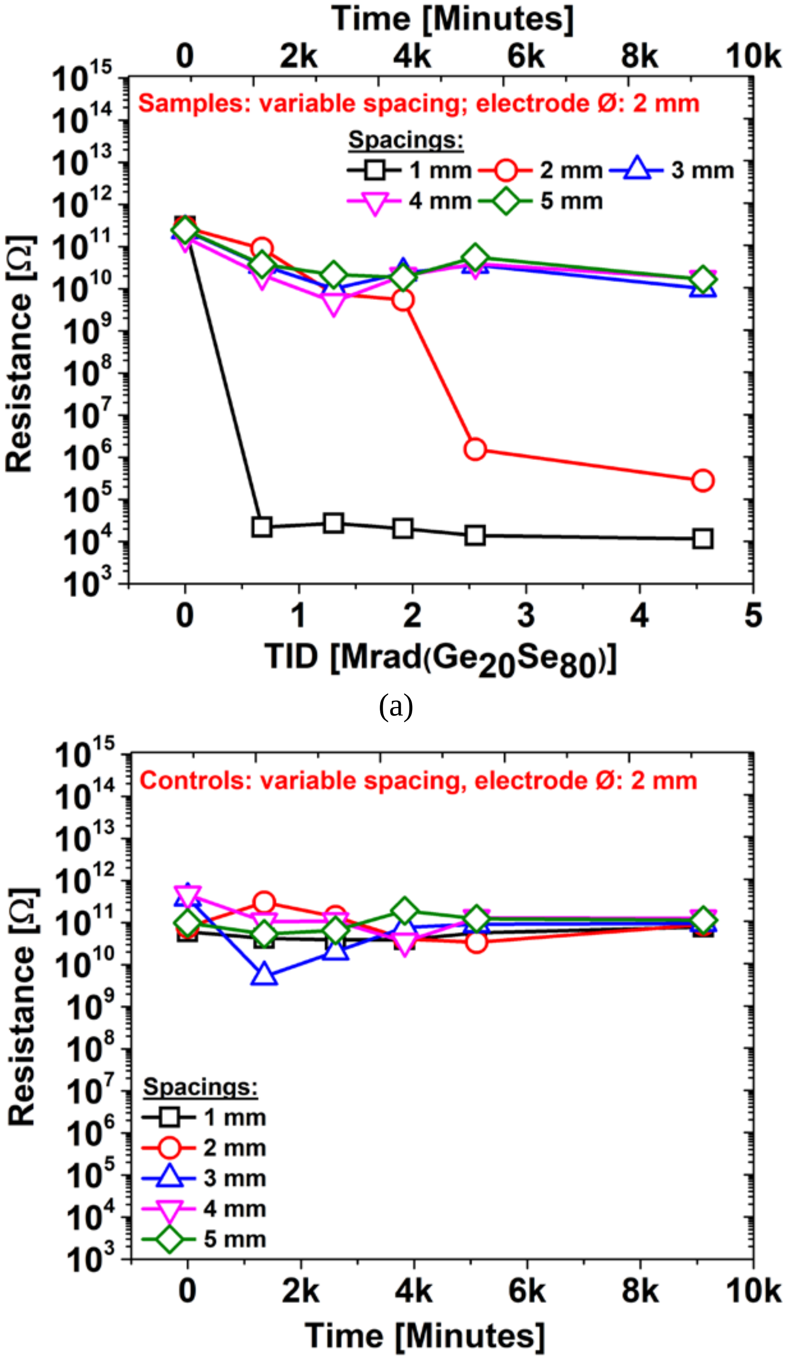
Exp. A results demonstrated the suitability of these mechanically flexible sensors for use in radiation environment where they can be attached on non-flat objects for measuring TID. Since structural features (or physical design parameters) are likely to control the radiation response characteristics of these sensors, identification of them would enable optimization of the sensor for specific uses. From our experiments, we have determined that some of these features include: 1) chalcogenide glass film composition and thickness; 2) electrode size, thickness and placement etc.. The impact of film processing on sensor performance has been investigated in previous works [70]-[72]. In this subsection, the impact of some of these physical design parameters (e.g., electrode area and spacing between electrodes, thickness of ChG film and electrodes) on sensor characteristics is investigated to understand the role they have on the limit of detection (LOD) and the dynamic range (DR) of the detector. Fig. 3.22(a) shows the evolution of resistance with increasing dose level (i.e., 675 krad ($Ge_{20}Se_{80}$), 1.31 Mrad ($Ge_{20}Se_{80}$), 1.92 Mrad ($Ge_{20}Se_{80}$), 2.55 Mrad ($Ge_{20}Se_{80}$), and 4.56 Mrad ($Ge_{20}Se_{80}$)) when the electrode diameter is fixed to 2 mm and the spacing between adjacent electrodes is varied from 1 to 5 mm. Fig. 3.23(a) shows the resistance evolution of the exposed samples with increasing dose when the electrode has either a 2 mm or 8 mm diameter and a fixed 2 mm spacing. Fig. 3.23(c) shows the resistance change with increasing dose when the electrode has either a 4 mm or 6 mm diameter and fixed 3 mm spacing. Figs. 3.22(b), 3.23(b), and 3.23(d) show the corresponding control samples which have been electrically characterized at the same time as the exposed parts.

Fig. 3.15(b) shows that after the maximum dose level of 4.56 Mrad($Ge_{20}Se_{80}$) Ag doping bridges the electrode gap for only the two arrays with smallest spacings (1 and 2 mm). From Fig. 3.22(a), we can see that the LOD for a 1 mm spaced array is much lower compared to the array with 2 mm spacing. Both Figs. 3.15(b) and 3.22(a) show that even after the maximum dose, the Ag doping fronts for arrays with larger spacings (3, 4 and 5 mm) do not make contact. This indicates that the LOD of this Ag-ChG sensor devices is a strong function of the spacing between nearest electrodes. Apart from that, spacing also plays critical role in controlling the dynamic range of the sensors. The minimum/doped resistance (R_{LRS}) between two nearest electrodes can be computed as

$$R_{LRS} = \frac{\rho_{\text{doped}} \cdot l}{w_{doped} \cdot t}, \qquad (3.2)$$

where ρ_{doped} is the resistivity of the Ag-Ge-Se ternary, which depends on the atomic fraction (x) of Ag present in $Ag_xGe_ySe_z$ and t is the thickness of ChG film [36]. Fig. 3.22 shows that by reducing spacing (l) between the nearest electrodes, the DR can be increased (as R_{LRS} reduces when l decreases).

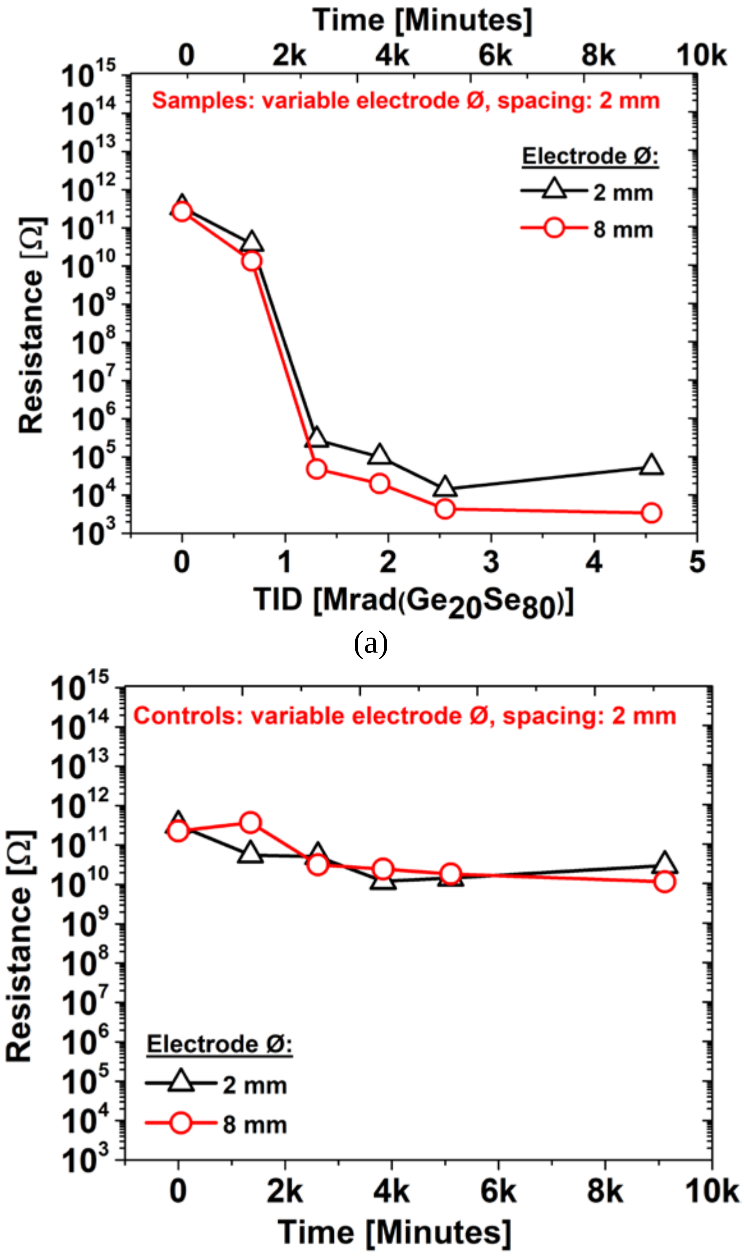
For devices with fixed spacing and variable electrode diameter (Fig. 3.23), a modest decrease in DR was observed with increased electrode diameter. Fig. 3.24 shows charts that compare the performance characteristics obtained from this experiment. The data show that the dynamic range can be tuned by varying both electrode area or intermediate spacing between the electrodes. However, the shift in DR in response to change in intermediate electrode spacing appears more prominent compared to devices where electrode area/diameter was changed. Finding the explicit explanation for this phenomenon is still an ongoing research topic. While LOD shows obvious shifts with spacing, no noticeable change was observed when electrode area was varied.



(a)

(b)

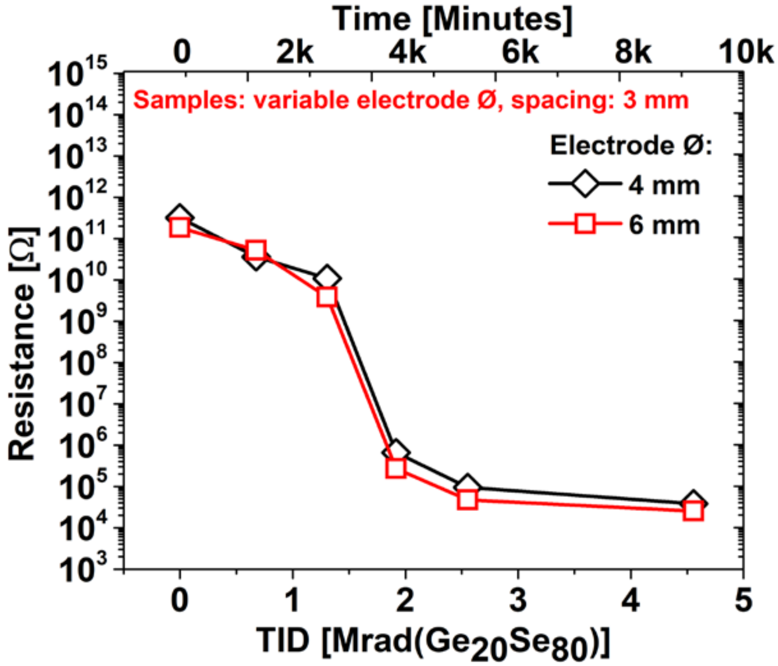
Fig. 3.22: Evolution of resistance of the (a) test and (b) control samples with fixed electrode diameter of 2 mm and variable spacing prior to exposure and after exposure to 675 krad ($Ge_{20}Se_{80}$), 1.31 Mrad ($Ge_{20}Se_{80}$), 1.92 Mrad ($Ge_{20}Se_{80}$), 2.55 Mrad ($Ge_{20}Se_{80}$), and 4.56 Mrad ($Ge_{20}Se_{80}$).



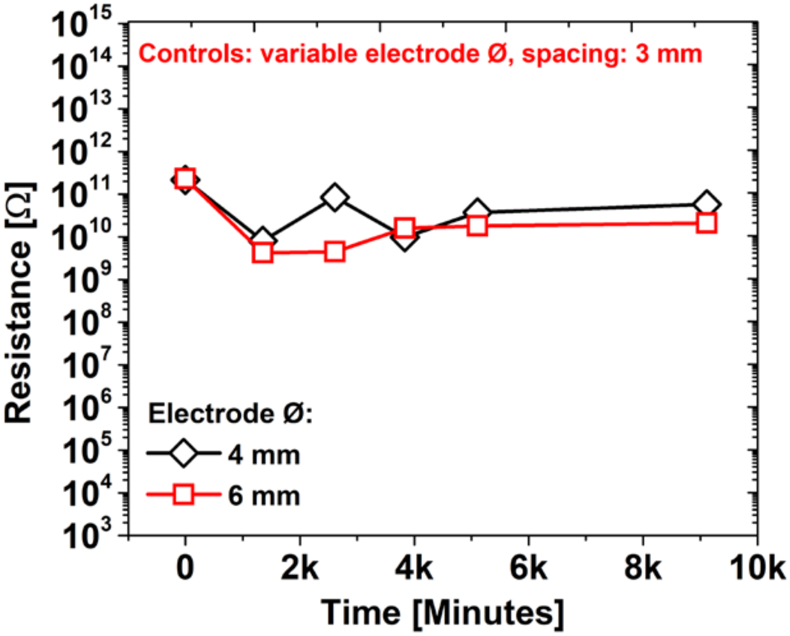
(a)

(b)

Fig. 3.23 (part 1 of 2): Evolution of resistance of the test and control samples prior to exposure and after exposure to 675 krad ($Ge_{20}Se_{80}$), 1.31 Mrad ($Ge_{20}Se_{80}$), 1.92 Mrad ($Ge_{20}Se_{80}$), 2.55 Mrad ($Ge_{20}Se_{80}$), and 4.56 Mrad ($Ge_{20}Se_{80}$). (a) Shows evolution of samples with fixed 2 mm spacing between adjacent electrodes, where variable electrode diameters are 2 and 8 mm. (b) Shows the control samples of the same batch.

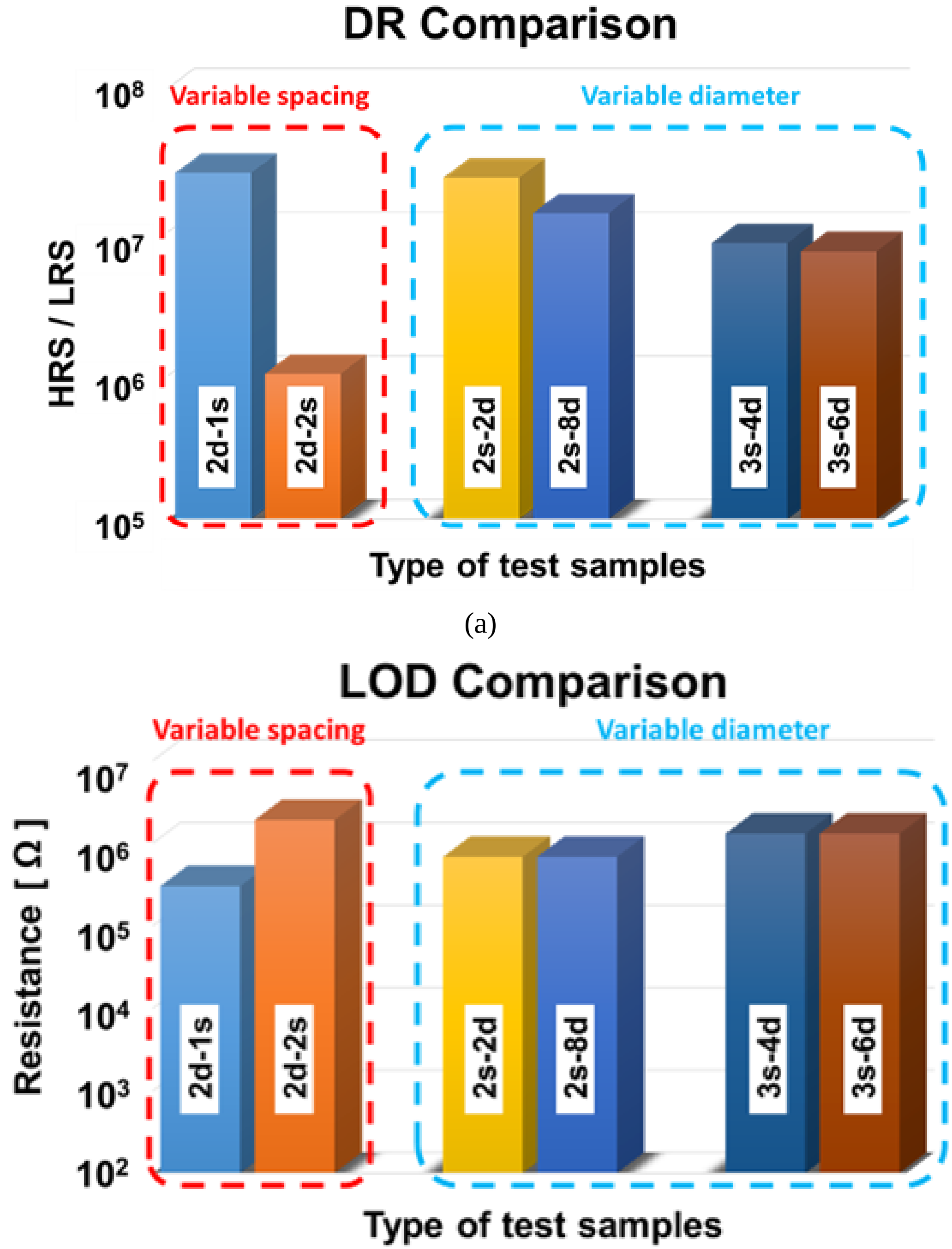


(c)



(d)

Fig. 3.23 (part 2 of 2): Evolution of resistance of the test and control samples prior to exposure and after exposure to 675 krad ($Ge_{20}Se_{80}$), 1.31 Mrad ($Ge_{20}Se_{80}$), 1.92 Mrad ($Ge_{20}Se_{80}$), 2.55 Mrad ($Ge_{20}Se_{80}$), and 4.56 Mrad ($Ge_{20}Se_{80}$). (c) Shows evolution of samples with fixed 3 mm spacing where variable electrode diameters are 4 and 6 mm and (d) Shows control samples of the same batch.



(a)

(b)

Fig. 3.24: Performance characteristics of Ag-ChG flexible sensors shown in comparative charts. “X*d*-Y*s*” or “Y*s*-X*d*” on the above charts interpret: diameter *d* of the electrode is ‘X’ mm and spacing *s* between the adjacent electrodes is ‘Y’ mm. (a) shows dynamic range and (b) shows limit of detection of the sensors.

TCAD simulation results for the samples with different electrode size and spacings (Exp. B):

In order to analyze the physical mechanisms governing the sensor radiation response, TCAD simulations were performed. Work functions for the Ag contacts were obtained from literature and set to 4.29 eV for the simulations [39]. Table I lists ChG film parameters. They include: bandgap (E_g), affinity (Φ), density of states in conduction band and valence band (N_C and N_V, respectively), electron and hole mobilities (μ_n and μ_p, respectively), and dielectric constant [39]. The chalcogenide glass is similar to p-doped materials where the hole concentration is dominant [76].

TABLE I

PARAMETERS OF THE GE_XSE_{1-X} AS CHG MATERIAL [39]

Bandgap at 300 K (E_g) [eV]	1.86
Affinity (Φ) [eV]	3.05
Density of states in conduction band (N_C) [per cm^3]	10^{19}
Density of states in valence band (N_V) [per cm^3]	10^{20}
Electron mobility (μ_n) [cm^2/Vs]	10^{-5}
Hole mobility (μ_p) [cm^2/Vs]	10
Dielectric constant	40.9

The Ag concentration in the contacts is assumed to be equal to the electron concentration and calculated based on [84], [85].

$$\left[n = \frac{8\sqrt{2}\,\pi\, m^{3/2}}{h^3} \left(\frac{2}{3} E_F^{3/2} \right) \right] \qquad (3)$$

In Eq. 3, h is the Planck constant, m is the electron mass, and E_F is the Fermi level which is equal to the metal work function (4.29 eV). By substituting values of parameters in Eq. 3, the Ag concentration is around 10^{23} cm^{-3}. The photodoping process, modeled with Silvaco's ATLAS device simulator [86], is based on the reaction, expressed in Eq. 4, which is the standard reduction-oxidation (RedOx) reaction for active metals in ChG films. Neutral Ag atoms have the tendency to lose one electron, because the highest energy of the atomic valence state is above the conduction band edge of the ChG material. Therefore, Ag atoms are readily ionized at the ChG/contacts interface and the forward reaction energy (0.5 eV) is assumed smaller than the reverse energy (0.7 eV). Due to the relatively high diffusivity of Ag^+ as well as its capacity to drift in the presence of a local electric field, silver ions transport into the films within several monolayers of the Ag-ChG interface. The diffusivity (D) of each species is calculated with Eq. 5, where a is the average hopping distance, v is the attempt to escape frequency, E_A is the activation energy for hopping, k is Boltzmann's constant, and T is material temperature. The diffusivity parameters for Ag and Ag^+ are listed in Table II. The relation of the mobility (μ) and D is based on the Einstein relation presented in Eq. 6. Based on the assumed values of for diffusivity, the neutral Ag species is essentially immobile in the glass film.

$$Ag \leftrightarrow Ag^{+} + e^{-} \qquad (4)$$

$$D = a^2 \nu \exp\left(\frac{-E_A}{kT}\right) \qquad (5)$$

$$D = \frac{kT}{q}\mu \qquad (6)$$

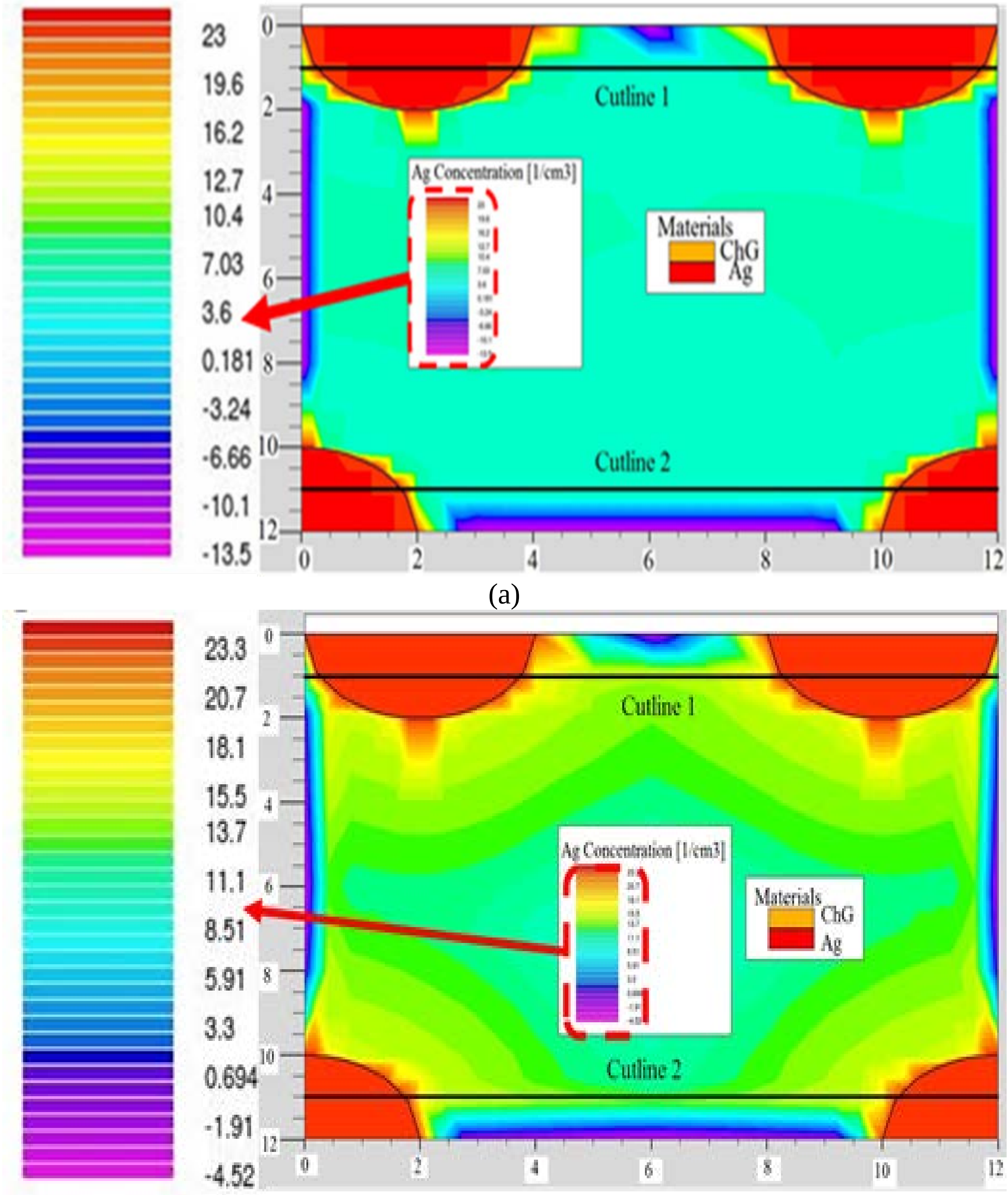
TABLE II

VALUES OF DIFFUSIVITY PARAMETERS FOR AG AND AG+ BASED ON EQ. (4)

	Ag	Ag+
E_A [eV]	1.5	0.5
ν [Hz]	10^4	10^{10}
a [cm]	10^{-10}	10^{-6}
D [cm^2/s]	6.31×10^{-42}	3.98×10^{-11}
Mobility [cm^2/V·s]	2.44×10^{-40}	1.54×10^{-9}

The finite element code used in this study simultaneously solves carrier statistics and transport equations for free carriers in the ChG material and also performs ion transport and reaction calculations on the device [76]. To simulate the photodoping process, the device is illuminated by UV light. The use of UV light was shown in our previous studies [36] to be a simple and convenient substitute for ionizing radiation as both generate charged carriers and induce the dissolution of the metal into the ChG film. For the UV exposure condition, the power density (P) of the light with generation rate (G) of 10^{20} ehp/cm^{3}s is 10 mW/cm^2.

With the simulation results, the effects of spacing between contacts and diameter of contacts are investigated. Fig. 3.25 plots the Ag distribution in the photodoped case of a structure in which semi-circles and quarter-circles are Ag contacts and the material between them is the ChG with the parameters presented in Table I. In order to obtain photodoped results, the structure is exposed to the UV light source for one half hour (simulation time) and then it is removed from the structure. After enough time has passed (~1 hour), the system settles to the equilibrium condition, the so called photodoped case. As shown in Fig. 3.25, all semi- and quarter-circles have the same diameter while the spacing between the two semi-circles at the top is less than that of the two quarter-circles at the bottom. Ag concentrations along the two cutlines drawn on Fig. 3.25 are shown in Fig. 3.26. The results verify that the Ag concentration for contacts with the same diameter should be higher if the spacing between contacts is shorter. Due to this higher Ag concentration between the electrodes with shorter spacing, doped resistance/LRS is reduced which results in an increase in DR. In addition, the simulation results (Figs. 3.25 and 3.26) suggest that the LOD for the electrodes with shorter spacing is lower compared to the case with larger spacing. This is consistent with experimental data and indicates that the LOD of this Ag-ChG sensor device can be optimized by adjusting the spacing between nearest electrodes.



(a)

(b)

Fig. 3.25: Ag distribution in (a) the unphotodoped case and (b) the photodoped case of a structure in which diameters of semi-circle and quarter-circle are the same while the spacing between two up contacts is smaller than that of two other contacts. The material between contacts is $Ge_{20}Se_{80}$ with the parameters presented in Table I.

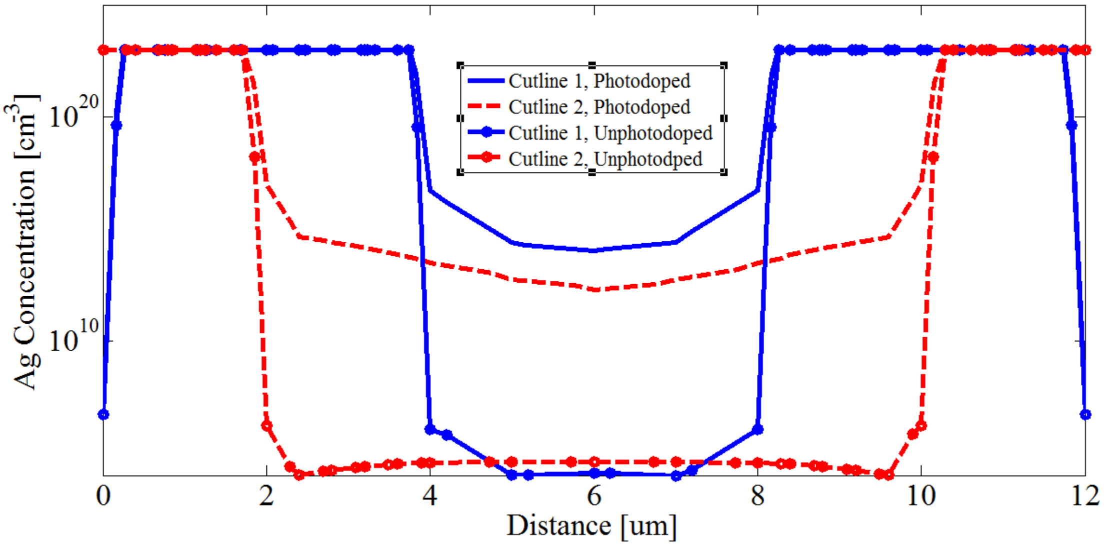
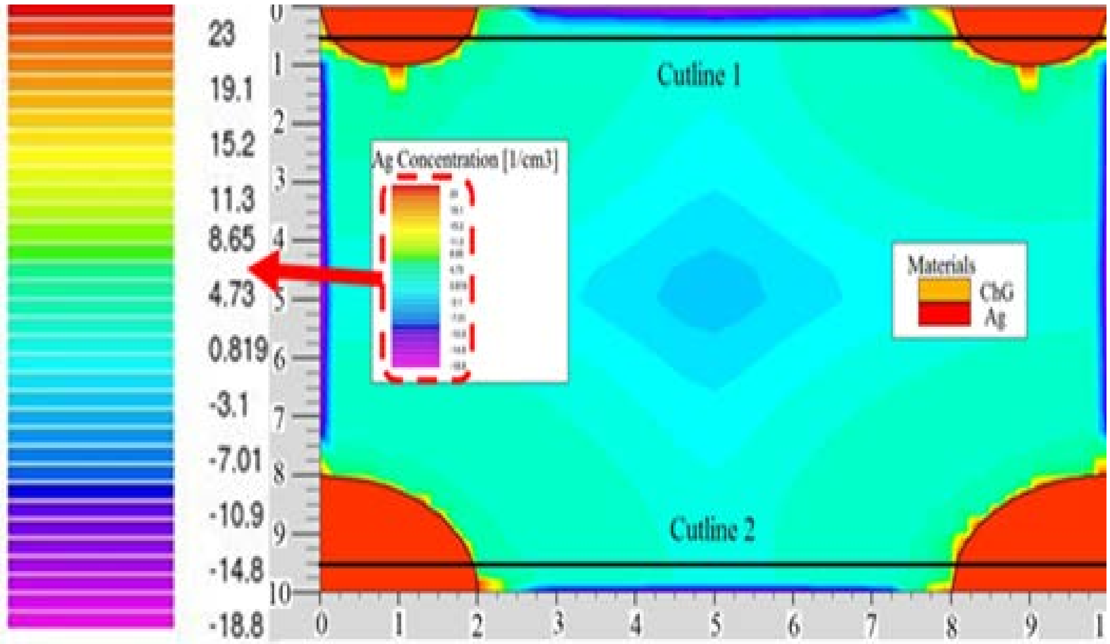
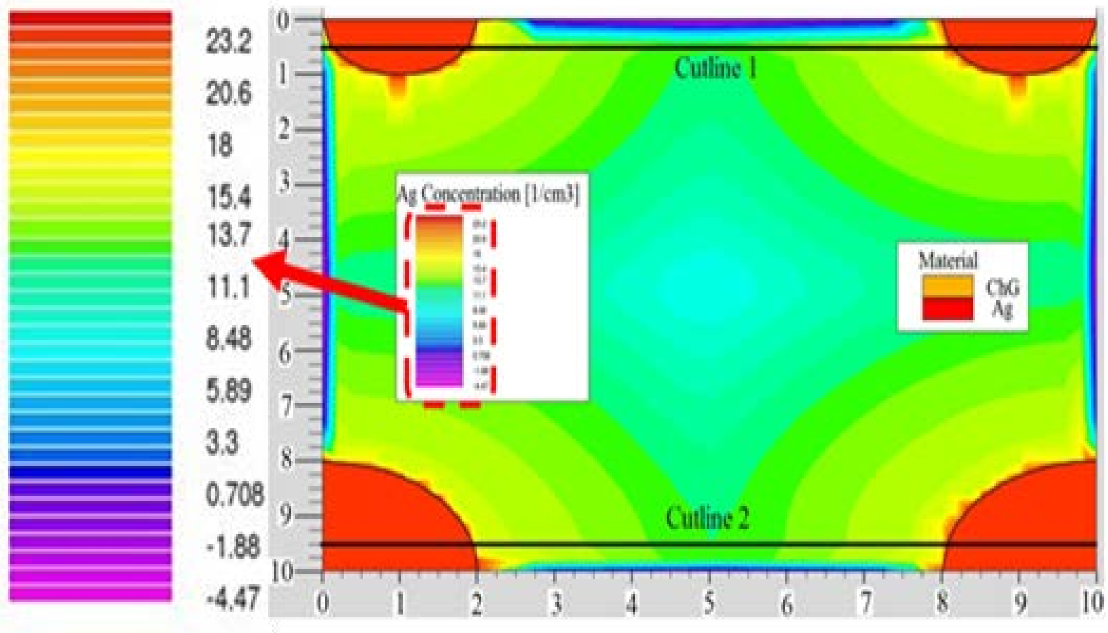


Fig. 3.26: Ag concentration across two cutlines shown in Fig. 3.25 for both unphotodoped and photodoped cases.

The effect of different diameters at the same spacing is considered in Figs. 3.27 and 3.28. In Fig. 3.27, the two upper semi-circle Ag contacts have a smaller diameter compared to the two lower Ag contacts with quarter-circle shapes. As shown in Fig. 3.28, the comparison of Ag concentration across the two cutlines (in Fig. 3.27) reveals that Ag concentrations for both cases with different diameters are approximately the same. Therefore, in spite of obvious change in Ag concentration with spacing, there is not any significant difference in Ag concentration when the contact radius varies at the same distance. Accordingly, the LOD is not significantly depending on the contact radius when contact distances are kept fixed. This behavior is also in the same path with experimental data.



(a)



(b)

Fig. 3.27: Ag distribution in (a) the unphotodoped case and (b) the photodoped case of a structure in which spacings of semi-circle and quarter-circle are the same while the diameters between two up contacts is smaller than that of two other contacts. The material between contacts is $Ge_{20}Se_{80}$ with the parameters presented in Table I.

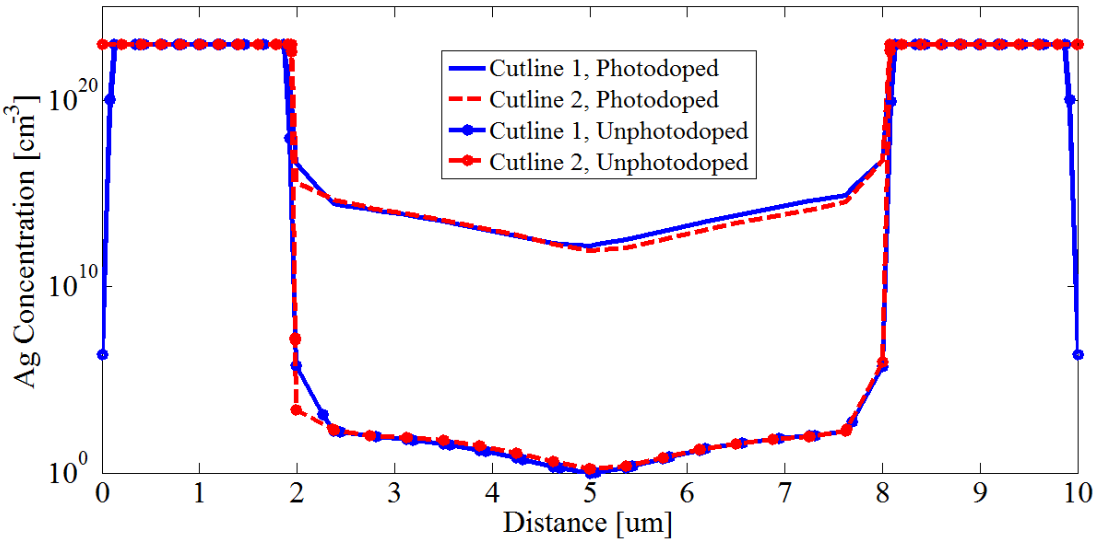
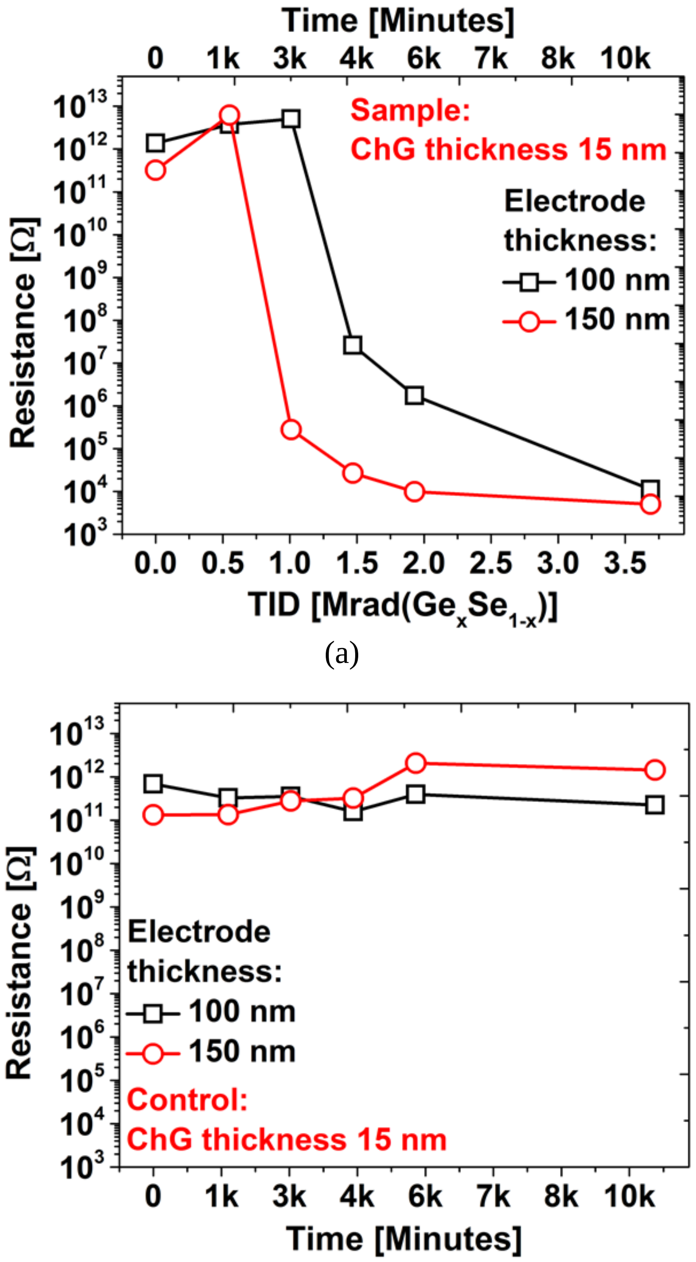


Fig. 3.28: Ag concentration across two cutlines shown in Fig. 3.27 for both unphotodoped and photodoped cases.

Aside from electrode spacing and area study, part of Exp. B. was to investigate the effect of electrode and ChG film thickness on the sensor performance characteristics such as limit of detection and dynamic range. Fig. 3.29 shows the results obtained from samples with different ChG film thickness. For this test, we have used two different exposure samples with 15 nm of $Ge_{20}Se_{80}$ and 30 nm of $Ge_{20}Se_{80}$. 100 nm of Ag was used to form the electrodes for both of the cases. The Exp. A single array shadow mask (i.e., that has fixed 1 mm spacings and 2 mm electrode diameter) has been used to manufacture the samples. The samples were exposed to a maximum TID level of 3.45 Mrad ($Ge_{20}Se_{80}$). They were periodically taken out after 515 krad ($Ge_{20}Se_{80}$), 945 krad ($Ge_{20}Se_{80}$), 1.37 Mrad ($Ge_{20}Se_{80}$), 1.8 Mrad ($Ge_{20}Se_{80}$) TID level to measure the resistance level between the adjacent electrodes. For each measurement cycle, three pairs of neighboring electrodes were tested and the average resistance value of these three measurements was taken.



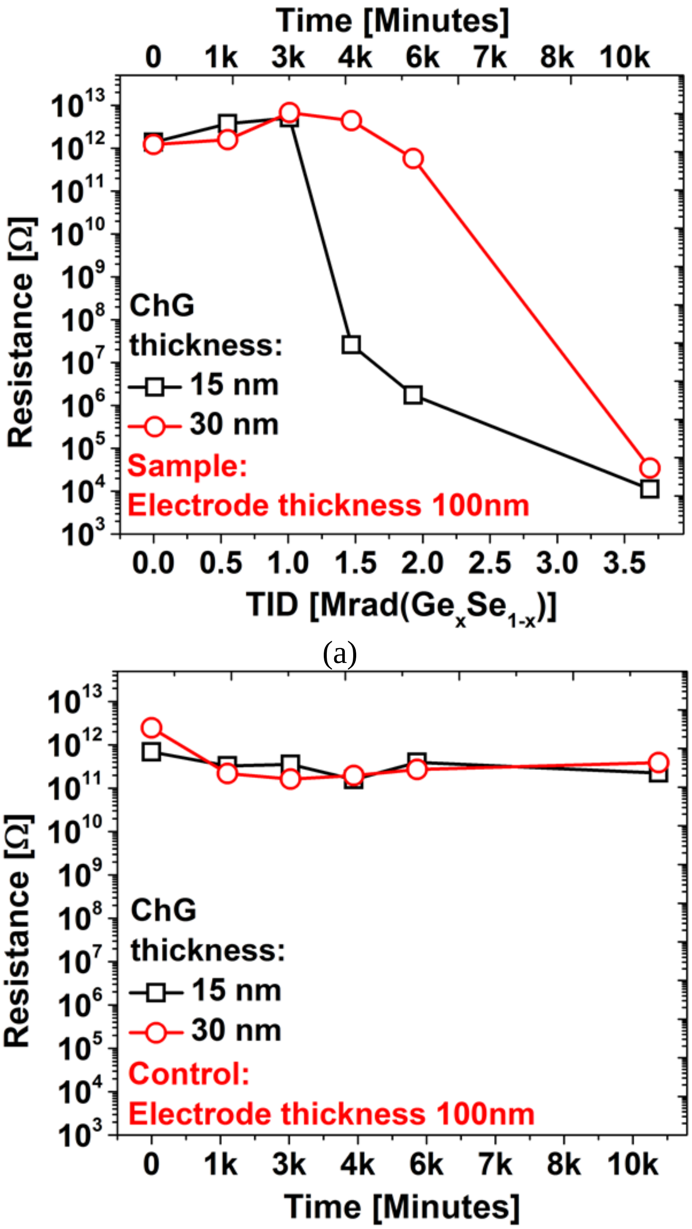
(a)

(b)

Fig. 3.29: Evolution of resistance of the test and control samples (with different electrode thickness) prior to exposure and after exposure to 515 krad ($Ge_{20}Se_{80}$), 945 krad ($Ge_{20}Se_{80}$), 1.37 Mrad ($Ge_{20}Se_{80}$), 1.8 Mrad ($Ge_{20}Se_{80}$), and 3.45 Mrad ($Ge_{20}Se_{80}$). (a) shows the exposure samples that clearly shows that samples with thinner electrode thickness (i.e., 100 nm of Ag) has larger LOD compare to sample with comparatively thicker electrode (i.e., 150 nm of Ag). (b) shows the control devices with 100 nm and 150 nm of Ag electrodes while the $Ge_{20}Se_{80}$ film thickness was kept constant to 15 nm.

Fig. 3.29 (a)-(b) show the results obtained from samples with different electrode thicknesses. It clearly reveals that the samples with 150 nm thick electrodes have a smaller LOD compared to the samples with 100 nm of electrode thickness. This happens since electrodes with larger thickness can supply more Ag+ ions into the ChG film when the electro-chemical potential is formed during ionizing radiation. The abundant supply of Ag+ ions can increase the lateral migration speed which eventually causes the doping fronts to come in contact for a smaller TID compared to the samples that have smaller electrode thickness. Thus, in order to reduce the LOD of a sample, increasing the electrode thickness can be a good option. However, no noticeable effect on the DR was observed due to the change in electrode thickness.

On the other hand, similar experiment was done where instead of changing the ChG film thickness, electrode thickness was increased. For this test, we made two samples where both of the cases the 15 nm of $Ge_{33}Se_{67}$ was deposited first. Then, on one sample, 100 nm of Ag electrodes were formed and on the other one, electrode thickness was increased to 150 nm of Ag. The samples were exposed to a maximum TID level of 3.45 Mrad ($Ge_{20}Se_{80}$). They were periodically taken out after 515 krad ($Ge_{20}Se_{80}$), 945 krad ($Ge_{20}Se_{80}$), 1.37 Mrad ($Ge_{20}Se_{80}$), 1.8 Mrad ($Ge_{20}Se_{80}$) TID level to measure the resistance level between the adjacent electrodes. The results are shown in Fig. 3.30. Fig. 3.31 shows the optical microscopic images those were taken after each measurement cycle to visually track the evolution of resistance level/ progression of doping fronts in response to corresponding TID exposure. For each measurement cycle, three pairs of neighboring electrodes were tested and the average resistance value of these three measurements was taken. Fig. 3.30 (a)-(b) show the results obtained from samples with different ChG film thicknesses.



(a)

(b)

Fig. 3.30: Evolution of resistance of the test and control samples (with different ChG thickness) prior to exposure and after exposure to 515 krad ($Ge_{20}Se_{80}$), 945 krad ($Ge_{20}Se_{80}$), 1.37 Mrad ($Ge_{20}Se_{80}$), 1.8 Mrad ($Ge_{20}Se_{80}$), and 3.45 Mrad ($Ge_{20}Se_{80}$). (a) shows the exposure samples that clearly shows that samples with thinner ChG film (i.e., 15 nm of $Ge_{20}Se_{80}$) has smaller LOD compare to sample with comparatively thicker ChG film (i.e., 30 nm of $Ge_{20}Se_{80}$) (b) shows the control devices with 15 nm of $Ge_{20}Se_{80}$ and 30 nm of $Ge_{20}Se_{80}$ while the Ag electrode thickness was kept constant to 100 nm.

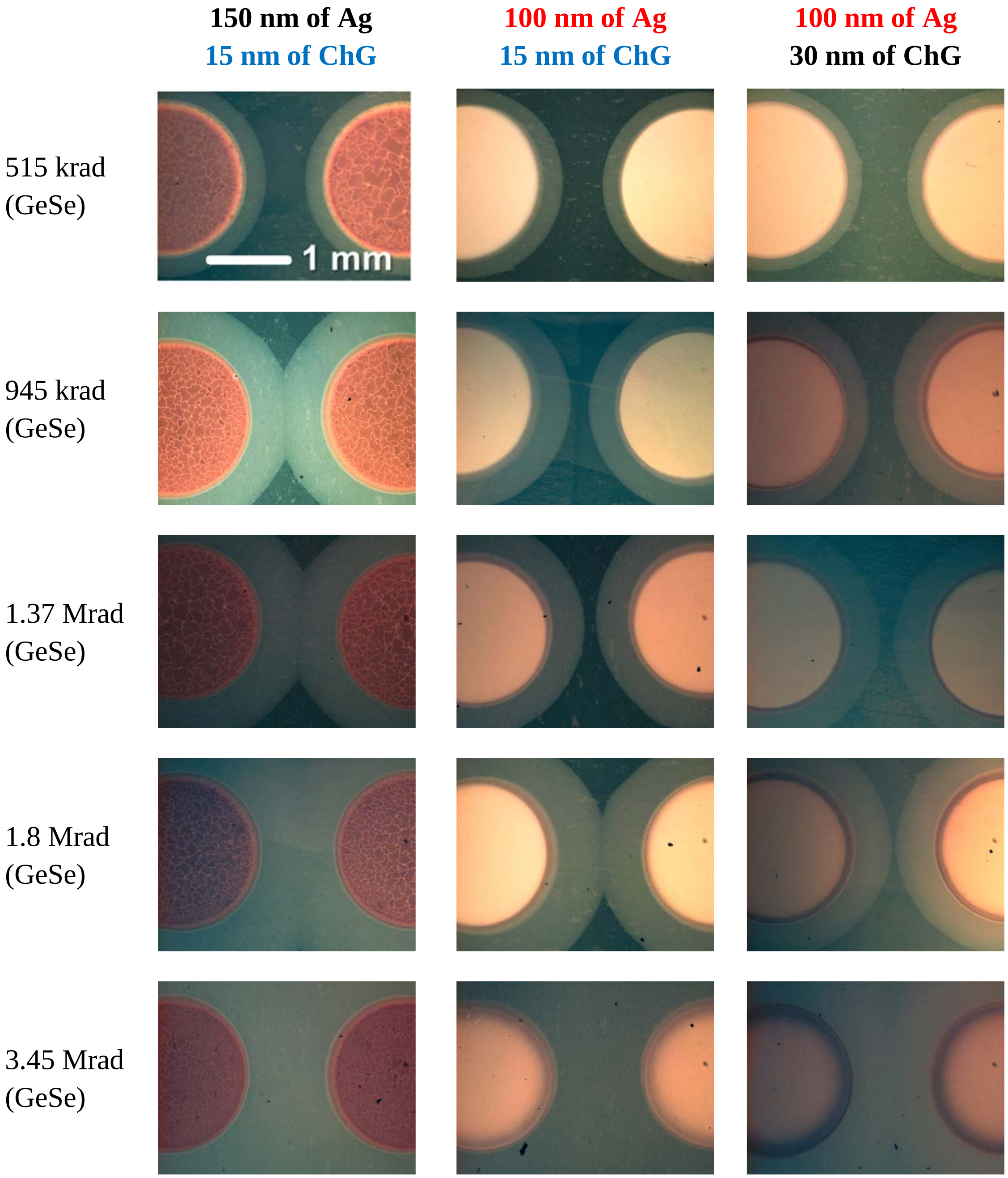


Fig. 3.31: Optical microscopic images those were taken after each measurement cycle to visually track the evolution or progression of doping fronts in response to corresponding TID exposure. Top left image indicates the scale which can be used for the other images as well.

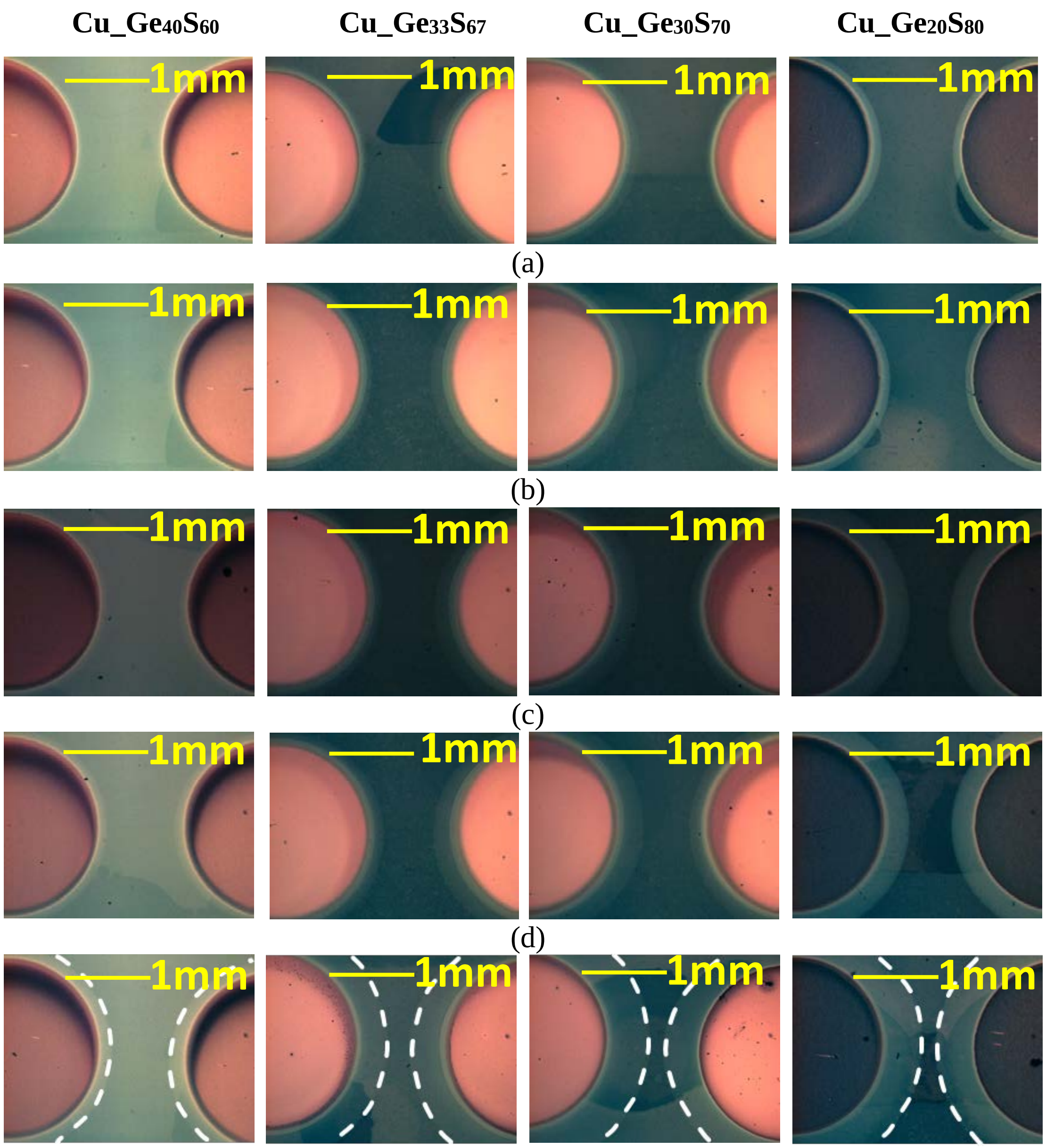
Apparently, they also demonstrate that the samples with 15 nm of ChG film have a smaller limit of detection compared to the sample with 30 nm of ChG. This is reasonable since it is understood that increasing the ChG film thickness causes Ag+ ions from electrodes to engage more on vertical migration to reach saturation. This effectively slows down the lateral migration speed of the Ag+ ions. Therefore, it takes a larger TID for the lateral doping fronts to contact compared to the samples with thinner ChG film. Similar to the different electrode thickness test, no noticeable effect on dynamic range has been observed due to change in ChG film thickness.

3.5.3. Exp. C results (Performance optimization- New materials)

In this particular set of experiment, we present results assessing the compatibility of other Selenide (i.e., Ge_xSe_{1-x}) and Sulfide (i.e., Ge_xS_{1-x}) based systems with different atomic ratio of the chalcogen, in order to investigate if ChG composition can be exploited to improve the control and performance of this metal-ChG based radiation sensors. We demonstrate that composition variation can be used to vary parameters such as the limit of detection or the dynamic range, as well as improve the shelf life of the samples. In addition, besides of using Ag, two other metals from column 11 (i.e., Cu and Au) are also used to investigate the impact of the diffusing atom on the sensor response (Cu and Ag are known to be highly diffusive atoms in dielectric films).

3.5.3.1. Sensor systems with sulfide based ChG

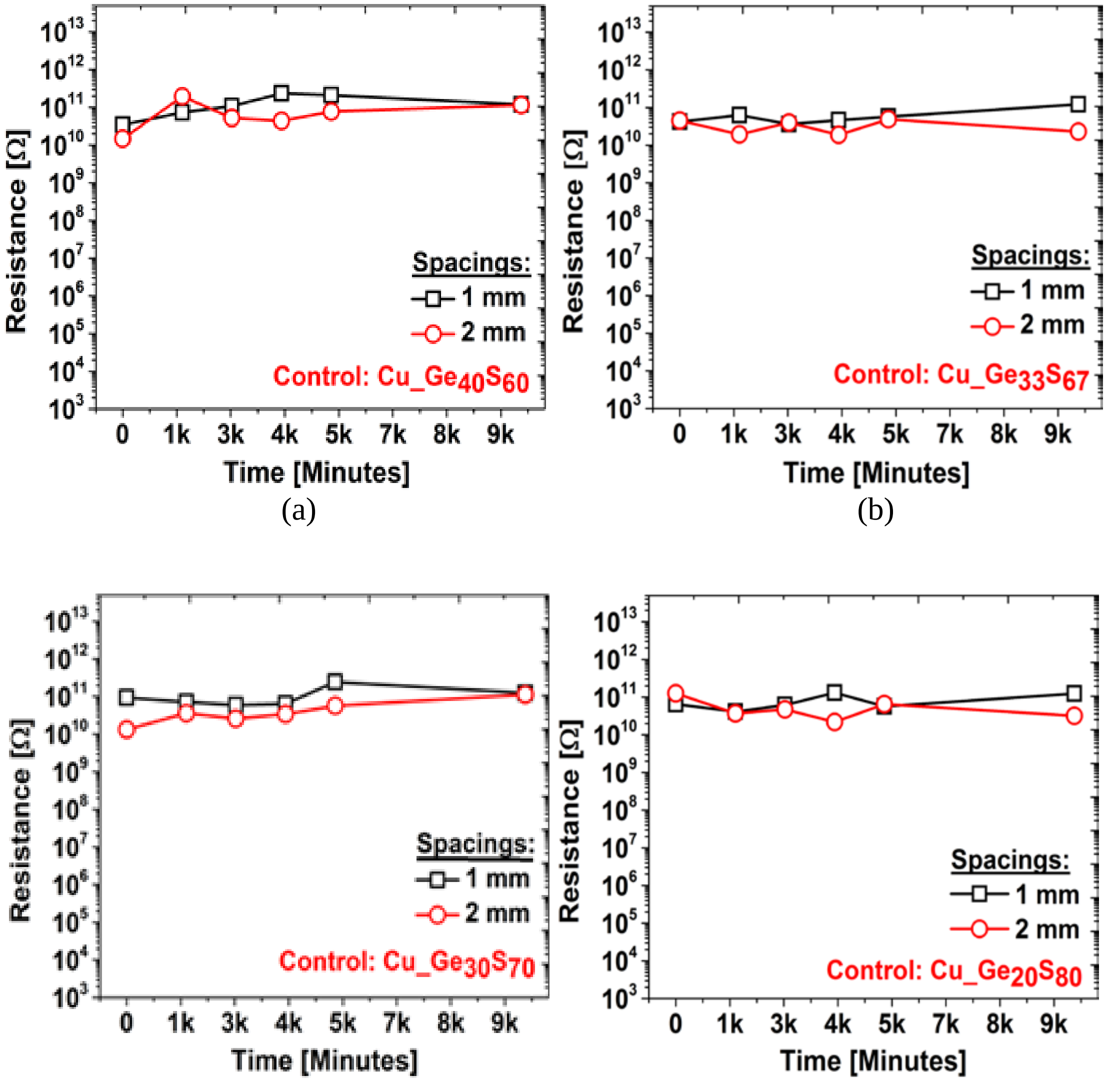
Fig. 3.32 shows the progression of the Cu doping fronts into the Ge_xS_{1-x} in response to increased dose level. These optical images were taken after each measurement cycle to visually track the lateral diffusion of Cu. From left to right (Fig. 3.32), the atomic percent of sulfide of the film increases (i.e., $Ge_{40}S_{60}$, $Ge_{33}S_{67}$, $Ge_{30}S_{70}$, $Ge_{20}S_{80}$). TID level increases from top to bottom: (a) after 551 krad(Ge_xS_{1-x}), (b) after 1 Mrad(Ge_xS_{1-x}), (c) after 1.47 Mrad(Ge_xS_{1-x}), (d) after 1.93 Mrad(Ge_xS_{1-x}) and finally (e) after 3.68 Mrad(Ge_xS_{1-x}). The white dashed lines in row (e) roughly show the boundary of Cu doping fronts after the maximum TID exposure. In Fig. 3.33, the evolution of resistance as a function of time for Cu_Ge_xS_{1-x} 'control' devices and resistance as a function of dose for 'exposed' devices are presented.



(e)

Fig. 3.32: Optical microscopic images taken after each measurement cycle to visually track the evolution or progression of Cu doping fronts into Ge_xS_{1-x} in response to corresponding TID exposure. From left to right, the atomic percent of sulfide of the film increases (i.e., $Ge_{40}S_{60}$, $Ge_{33}S_{67}$, $Ge_{30}S_{70}$, $Ge_{20}S_{80}$). TID level increases from top to bottom: (a) after 551 krad(GeS), (b) after 1 Mrad(GeS), (c) after 1.47 Mrad(GeS), (d) after 1.93 Mrad(GeS) and finally (e) after 3.68 Mrad(GeS). The white dash lines in row (e) roughly show the boundary of Cu doping fronts after the maximum TID exposure.

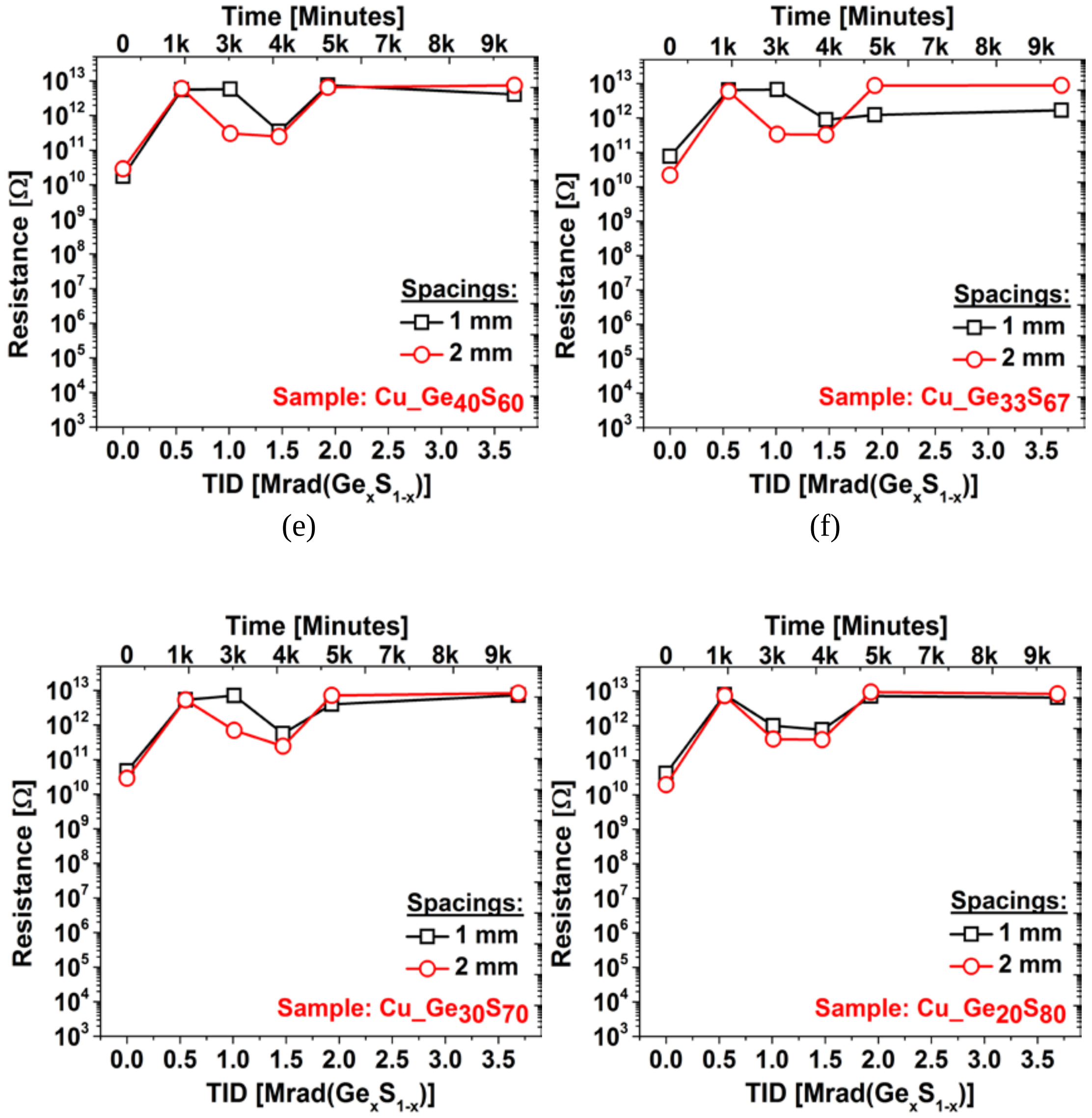
Cu_Ge$_x$S$_{1-x}$ Controls



(a) (b) (c) (d)

Fig. 3.33 (part 1 of 2): Resistance measured on control devices (a, b, c, d) of Cu_Ge$_x$S$_{1-x}$ based systems with different atomic ratio. From (a) to (d) the atomic percent of sulfide of the film increases (Ge$_{40}$S$_{60}$, Ge$_{33}$S$_{67}$, Ge$_{30}$S$_{70}$, Ge$_{20}$S$_{80}$). Results for devices with different spacing between electrodes (1 mm, 2 mm) are also presented.

Cu_Ge$_x$S$_{1-x}$ Test Samples



(e) (f)

(g) (h)

Fig. 3.33 (part 2 of 2): Resistance measured on ^{60}Co gamma ray exposed test sample devices (e, f, g, h) of Cu_Ge$_x$S$_{1-x}$ based systems with different atomic ratio. From (e) to (h) the atomic percent of sulfide of the film increases (Ge$_{40}$S$_{60}$, Ge$_{33}$S$_{67}$, Ge$_{30}$S$_{70}$, Ge$_{20}$S$_{80}$). Results for devices with different spacing between electrodes (1 mm, 2 mm) are also presented.

Fig. 3.33(a) shows resistance of Cu_$Ge_{40}S_{60}$ based control devices with two different spacings between electrodes (i.e., 1 mm and 2 mm), and similarly, Figs. 3.33(b)-(d) show evolution of resistance for Cu_$Ge_{33}S_{67}$, Cu_$Ge_{30}S_{70}$ and Cu_$Ge_{20}S_{80}$ systems. Figs. 3.33(e)-(h) show the resistance level of corresponding exposed samples which were measured within the same time frame.

For the Cu_Ge_xS_{1-x} systems, a very slow radiation-induced metal ion transport has been observed (in comparison to selenide systems). This might be due to sulfide based ChG glasses having a higher band gap compared to their selenide based ChG counterparts which would lead to smaller numbers of electron hole pairs generation during radiation exposure. From the optical images presented in Fig. 3.32 representing array with 1 mm spacing, one can notice that the Cu migration is relatively higher in chalcogen (or sulfur) rich devices compared to chalcogen poor devices. This demonstrates the impact of chalcogen/Ge atomic ratio on the TID influenced transport of metal into the ChG film and the influence of the chalcogen atom which generates higher amount of electron hole pairs to trigger the Cu diffusion. However, for none of the cases (even for the arrays with 1 mm spacings) were the doping fronts able to touch after the maximum TID level of 3.68 Mrad(GeS). Consequently, the resistance evolution plots (i.e., Fig. 3.33) for the control and exposure devices are generally similar. Like Fig. 3.32, Fig. 3.34 shows the progression of the Ag doping fronts into the Ge_xS_{1-x} in response to increased dose level. Figs. 3.35(a)-(d) demonstrate the evolution of resistance for Ag_$Ge_{40}S_{60}$, Ag_$Ge_{33}S_{67}$, Ag_$Ge_{30}S_{70}$ and Ag_$Ge_{20}S_{80}$ control samples. The corresponding resistance evolution plots of the exposed samples are shown in Figs. 3.35(e)-(h).

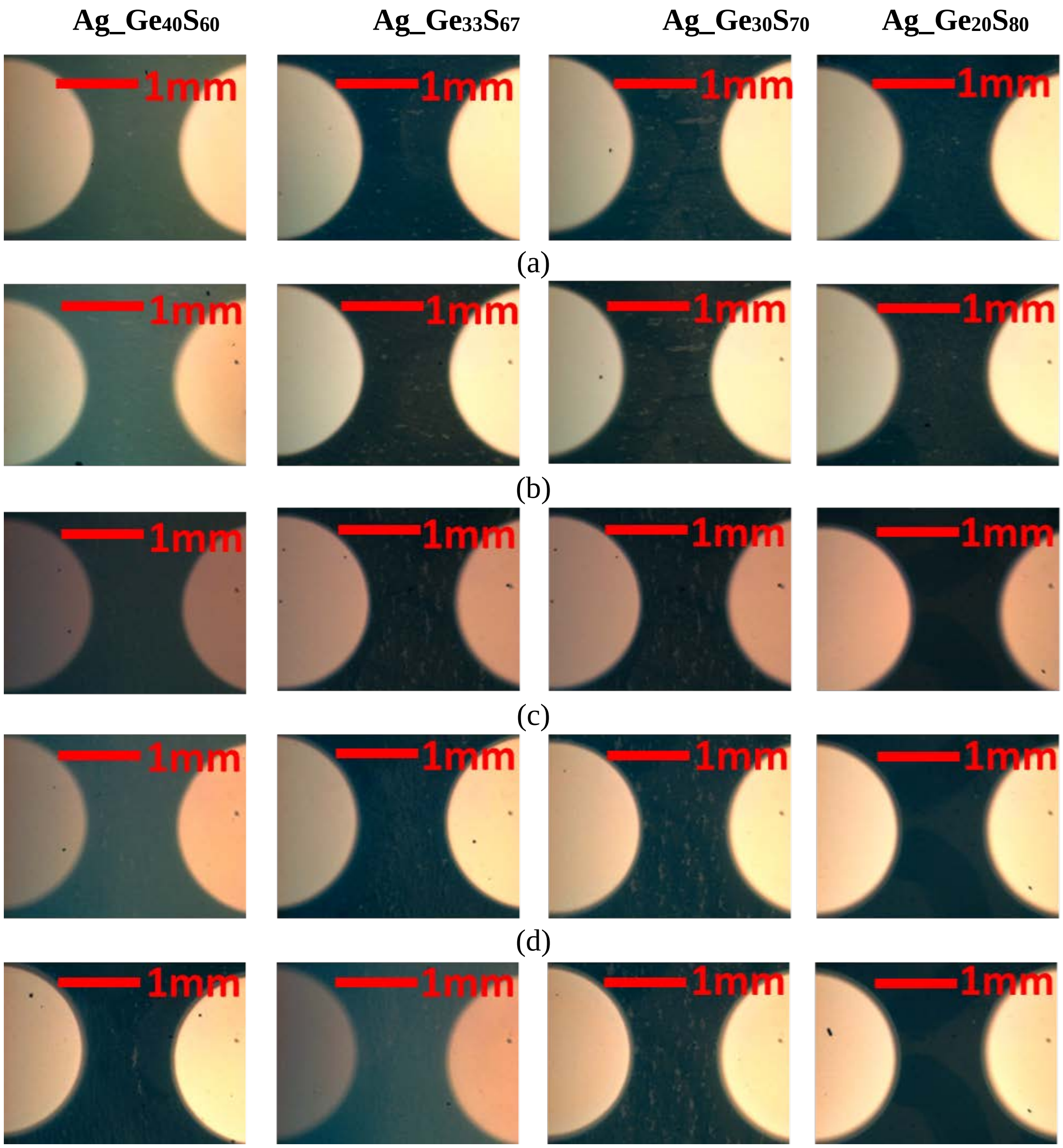
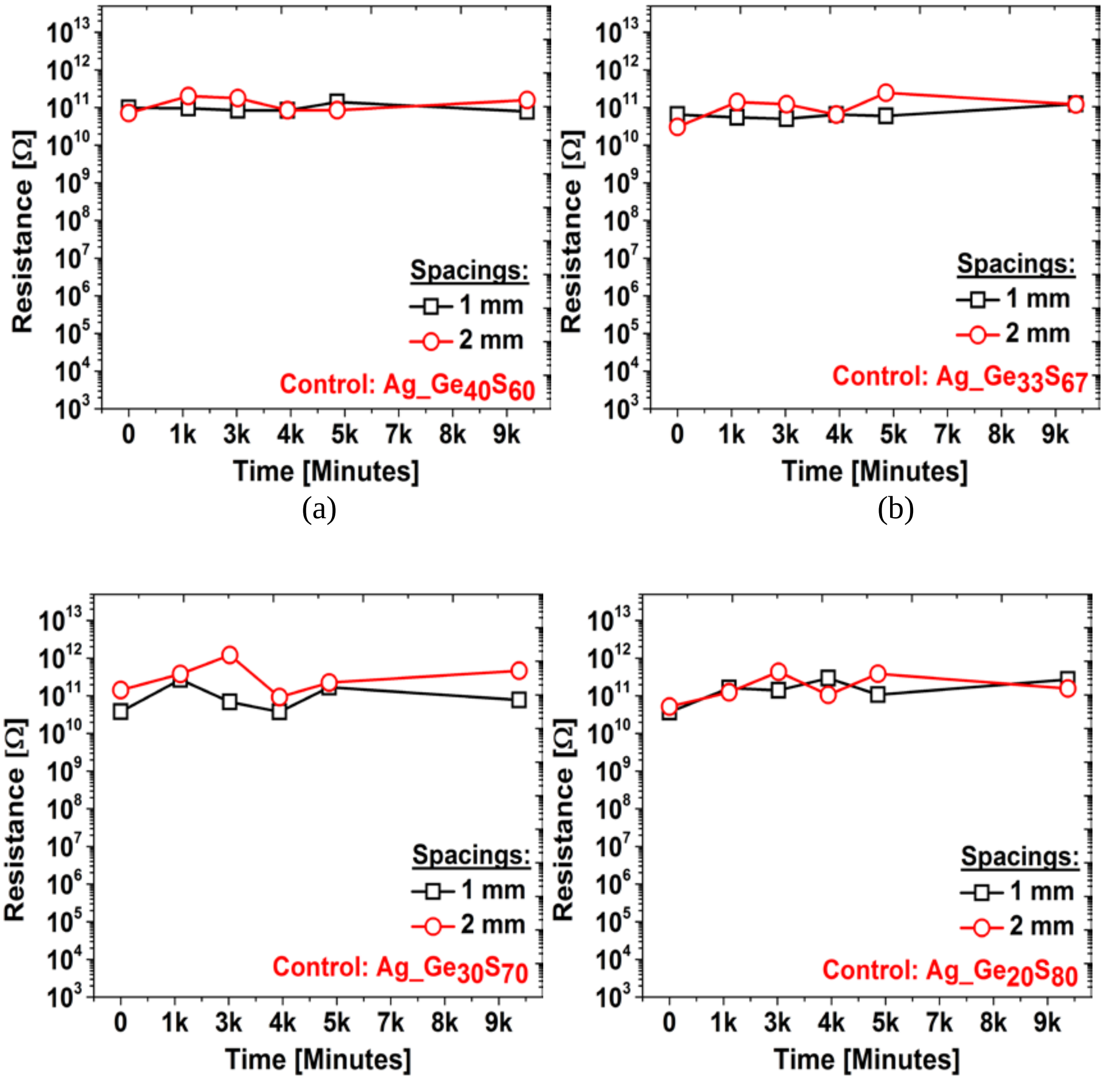


Fig. 3.34: Optical microscopic images taken after each measurement cycle to visually track the evolution or progression of Ag doping fronts into Ge_xS_{1-x} in response to corresponding TID exposure. From left to right, the atomic percent of sulfide of the film increases (i.e., $Ge_{40}S_{60}$, $Ge_{33}S_{67}$, $Ge_{30}S_{70}$, $Ge_{20}S_{80}$). TID level increases from top to bottom: (a) after 551 krad(GeS), (b) after 1 Mrad(GeS), (c) after 1.47 Mrad(GeS), (d) after 1.93 Mrad(GeS) and finally (e) after 3.68 Mrad(GeS). No significant lateral diffusion was observed after the maximum TID exposure.

Ag_Ge$_x$S$_{1-x}$ Controls

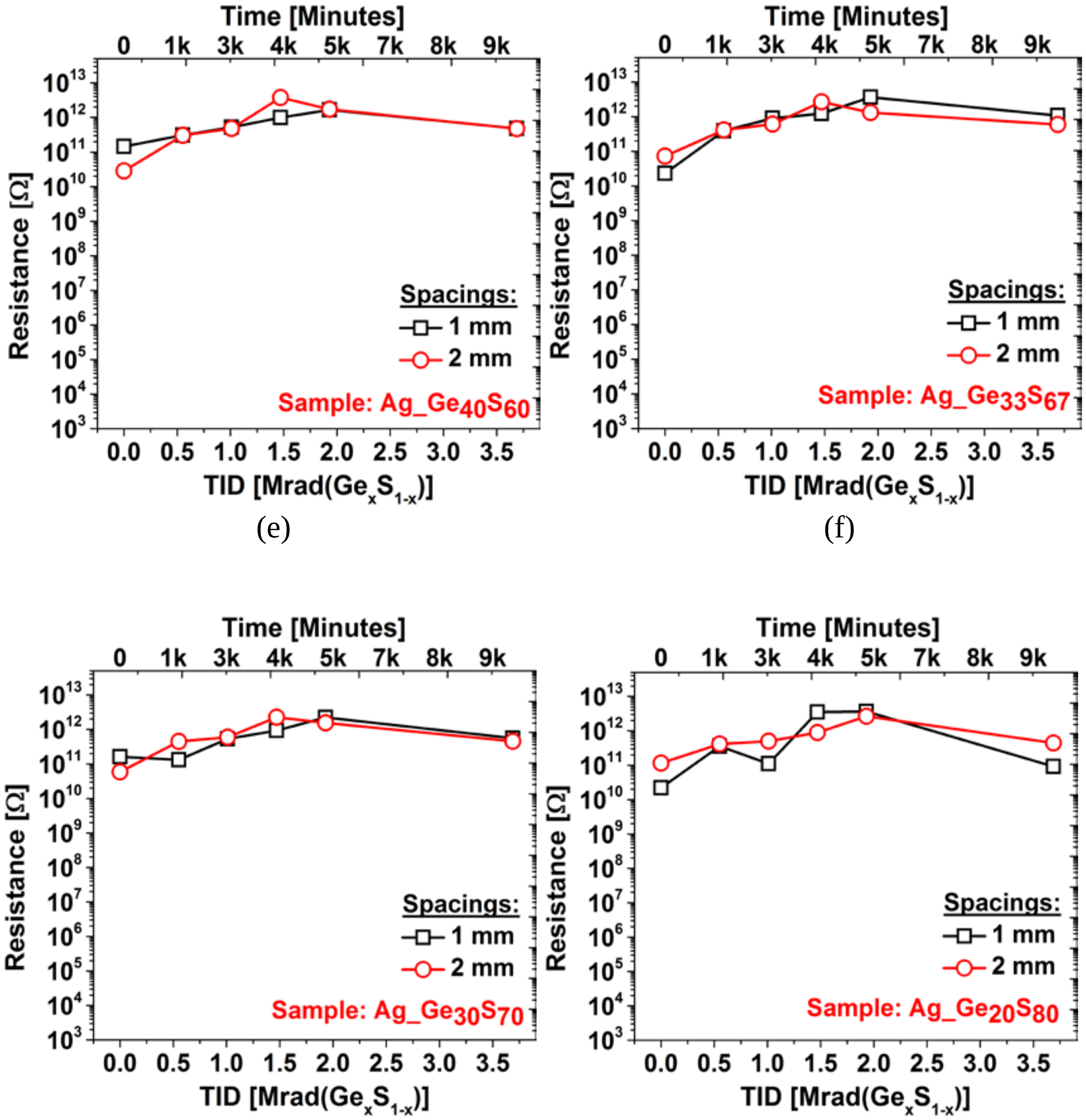


(a) (b)

(c) (d)

Fig. 3.35 (part 1 of 2): Resistance measured on control devices (a, b, c, d) of Ag_Ge$_x$S$_{1-x}$ based systems with different atomic ratio. From (a) to (d) the atomic percent of sulfide of the film increases (Ge$_{40}$S$_{60}$, Ge$_{33}$S$_{67}$, Ge$_{30}$S$_{70}$, Ge$_{20}$S$_{80}$). Results for devices with different spacing between electrodes (1 mm, 2 mm) are also presented.

Ag_Ge$_x$S$_{1-x}$ Test Samples



(e) (f)

(g) (h)

Fig. 3.35 (part 2 of 2): Resistance measured on ^{60}Co gamma ray exposed test sample devices (e, f, g, h) of Ag_Ge$_x$S$_{1-x}$ based systems with different atomic ratio. From (e) to (h) the atomic percent of sulfide of the film increases (Ge$_{40}$S$_{60}$, Ge$_{33}$S$_{67}$, Ge$_{30}$S$_{70}$, Ge$_{20}$S$_{80}$). Results for devices with different spacing between electrodes (1 mm, 2 mm) are also presented.

For the case of Ag-Ge_xS_{1-x} systems (Fig. 3.34), almost no visible lateral diffusion is observed even with the most sulfide rich samples after the maximum TID level of 3.68 Mrad(Ge_xS_{1-x}). The obtained data demonstrate that in Ge_xS_{1-x} systems, Ag migrates much slower compared to Cu; this is expected since Cu has smaller atomic radius and higher electronegativity compared to Ag and Ge_xS_{1-x} glass have smaller molar volume [87].

3.5.3.2. Sensor systems with selenide based ChG

Fig. 3.36 displays the evolution of resistance of Au_$Ge_{20}Se_{80}$ control and exposed devices with increasing dose level (i.e., 325.8 krad (Ge_xSe_{1-x}), 787.6 krad (Ge_xSe_{1-x}), 1.75 Mrad (Ge_xSe_{1-x}), and 3.34 Mrad (Ge_xSe_{1-x})). As can be observed, no radiation induced change of resistance and diffusion of Au has been noticed even after the maximum TID dose level, thus pointing to the unsuitability of this material system for the radiation detection application.

In Fig. 3.37, the evolution of resistance as a function of time for Cu_Ge_xSe_{1-x} 'control' devices and resistance as a function of dose for 'exposed' devices are presented. Fig. 3.37(a) demonstrates resistance of Cu_$Ge_{40}Se_{60}$ based control devices with four different spacings (i.e., 1 mm to 4 mm) between electrodes, and similarly, Figs. 3.37(b)-(d) show the evolution of resistance for Cu_$Ge_{33}Se_{67}$, Cu_$Ge_{30}Se_{70}$ and Cu_$Ge_{20}Se_{80}$ systems. Figs. 3.37(e)-(h) exhibit the resistance levels of corresponding exposed samples.

For Cu_Ge_xSe_{1-x} parts, we observed lateral diffusion of Cu into ChG film for both control and exposed samples. This is shown on control parts (Figs. 3.37(a)-(d)), where resistance variation is observed to occur faster on selenium rich parts. Previous work revealed that Cu can dissolve into $Ge_{30}Se_{70}$ systems without exposure to UV light [88]. It appears to us that this observation is true for other Ge_xSe_{1-x}compositions as well.

Therefore, we assume that exposure to visible light, which occurred during the film deposition processes and periodical resistance level testing, could not be solely responsible for Cu ionization at the electrode–ChG film interface, as that contribution was minimized by keeping the manufactured samples in the dark. Room temperature and background radiation might have provided adequate energy to Cu atoms to migrate into the Ge_xSe_{1-x} film.

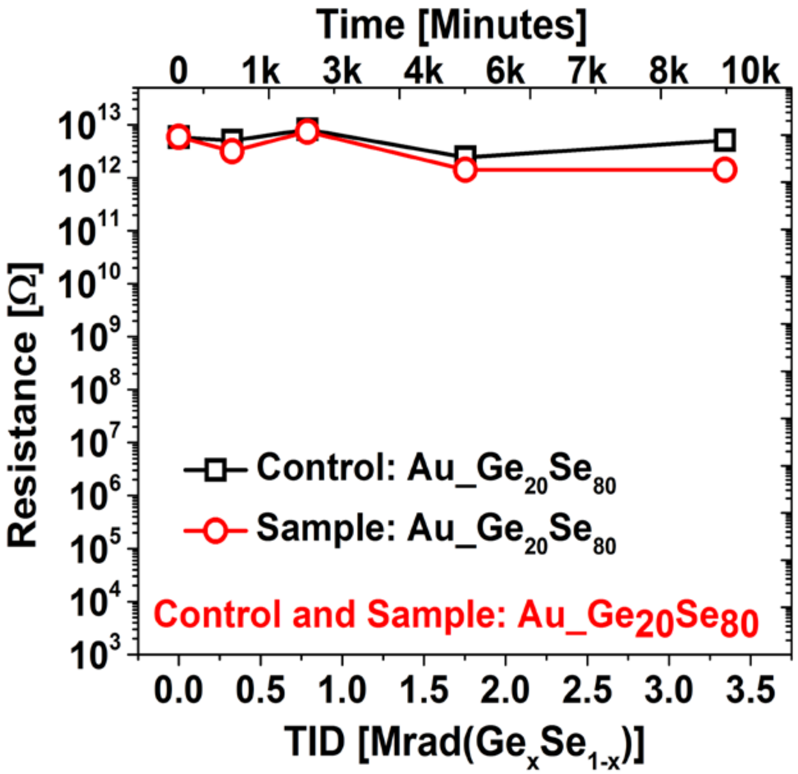
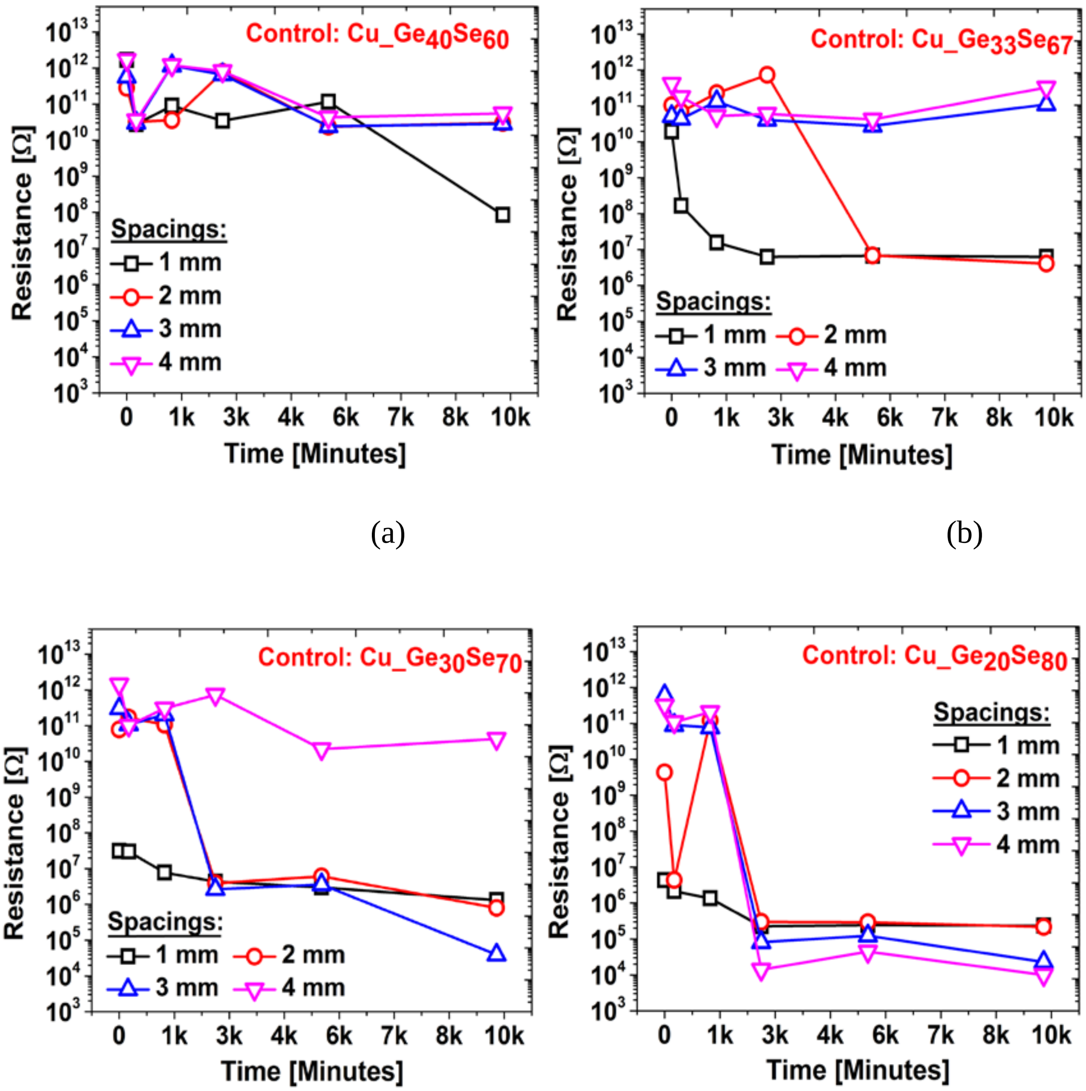


Fig. 3.36: Evolution of resistance of the control and exposed samples of $Au\_Ge_{20}Se_{80}$ system with increased dose level. The electrode diameter and spacing of the devices were respectively 2 mm and 1 mm.

Cu_Ge$_x$Se$_{1-x}$ Controls



(a)

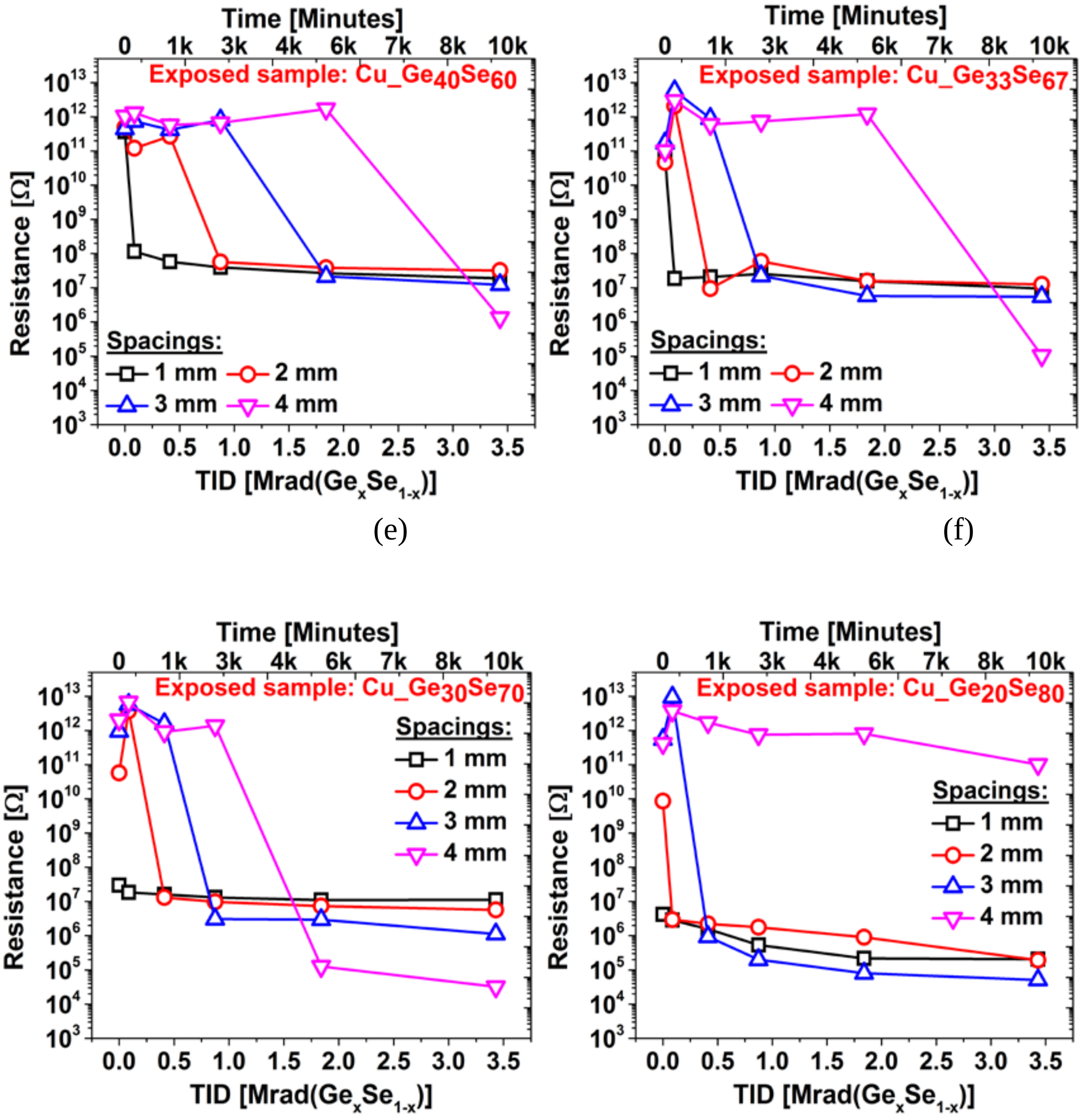
(b)

(c)

(d)

Fig. 3.37 (part 1 of 2): Resistance measured on control devices (a, b, c, d) of Cu_Ge$_x$Se$_{1-x}$ based systems with different atomic ratio. From (a) to (d) the atomic percent of sulfide of the film increases (Ge$_{40}$Se$_{60}$, Ge$_{33}$Se$_{67}$, Ge$_{30}$Se$_{70}$, Ge$_{20}$Se$_{80}$). Results for devices with different spacing between electrodes (1 mm, 2 mm) are also presented.

Cu_Ge$_x$Se$_{1-x}$ Test Samples



(e)

(f)

(g)

(h)

Fig. 3.37 (part 2 of 2): Resistance measured on ^{60}Co gamma ray exposed test sample devices (e, f, g, h) of Cu_Ge$_x$Se$_{1-x}$ based systems with different atomic ratio. From (e) to (h) the atomic percent of sulfide of the film increases (Ge$_{40}$Se$_{60}$, Ge$_{33}$Se$_{67}$, Ge$_{30}$Se$_{70}$, Ge$_{20}$Se$_{80}$). Results for devices with different spacing between electrodes (1 mm, 2 mm) are also presented.

On exposed samples, variation of resistance is observed but cannot be used effectively (or easily) for radiation sensing due to the transport occurring on the control samples. Copper migration/ thermal diffusion process was likely impacted by its smaller atomic radius (compared to Ag and Au, from group 11) which might be an important reason for the control devices to exhibit such a notable movement. Another important impact comes by the fact that Se has stronger affinity towards the group 11 metals due to its larger atomic radius which increases its ionization potential, giving rise to greater reactivity between Se and the metals and formation of metal-ChG compositions.

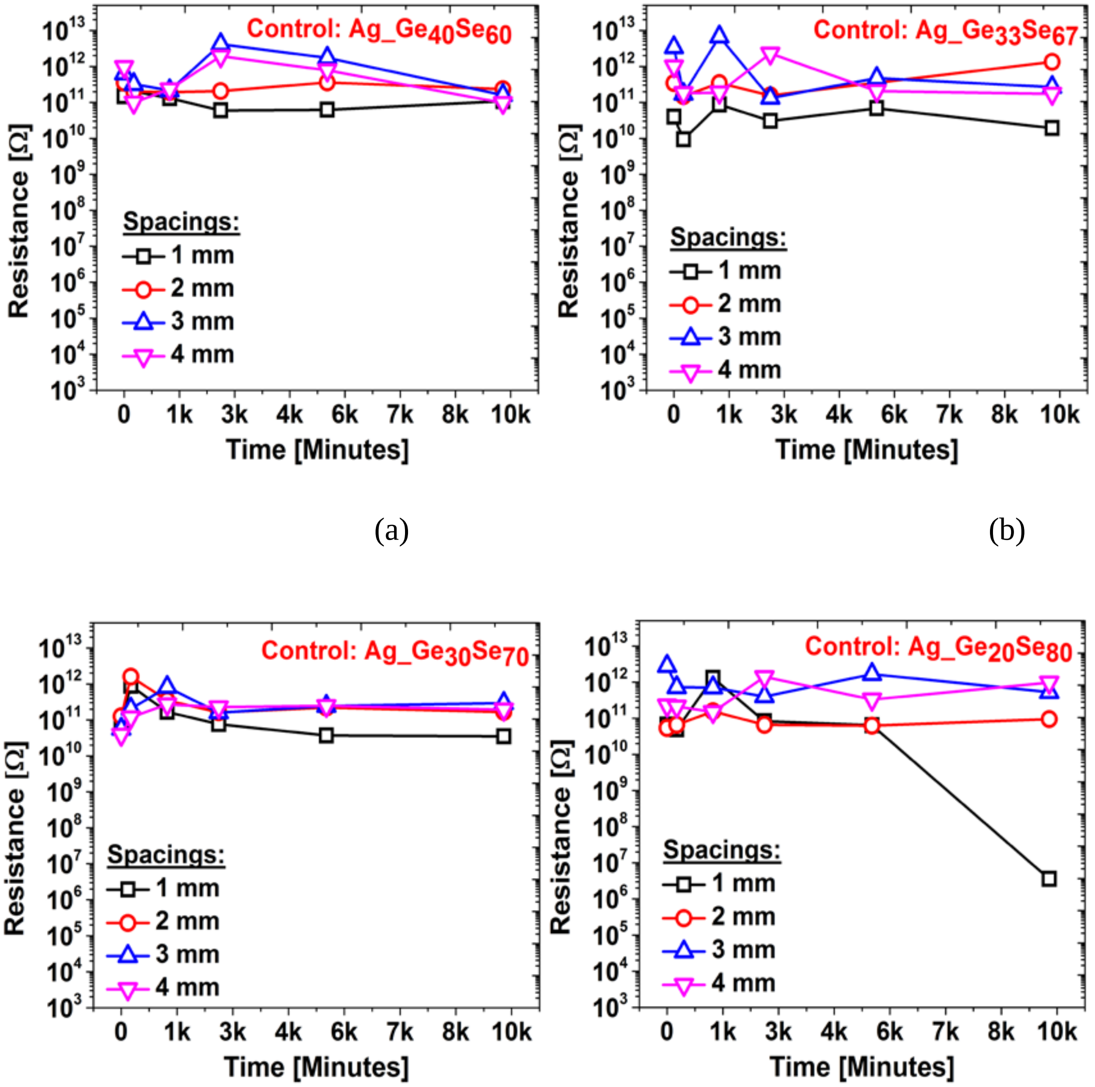
Similar to Fig. 3.37, Figs. 3.38(a)-(d) show the evolution of resistance for Ag_$Ge_{40}Se_{60}$, Ag_$Ge_{33}Se_{67}$, Ag_$Ge_{30}Se_{70}$ and Ag_$Ge_{20}Se_{80}$ control samples as a function of time. Corresponding resistance evolution plots of the exposed Ag_Ge_xSe_{1-x} samples are shown in Figs. 3.38(e)-(h) as a function of dose.

In Fig. 36 it can be observed that apart from the 1 mm spacing device on Ag-$Ge_{20}Se_{80}$ (Fig. 3.38(d)) all control samples stayed at HRS during the course of the experiment. In contrast, exposed devices exhibit varying behaviors with ChG composition. For Ag-$Ge_{40}Se_{60}$, only the 1 mm spacing device (Fig. 3.38(e)) undergoes a transition from HRS to LRS. Devices made with the ChG with the smallest selenium composition exhibit the lowest resistance variation trend with total dose. Figs. 3.38(e)-(h) show that the parts with higher selenium content experience the greatest sensitivity to TID [83].

The impact of the ChG film composition on the response of parts with a fixed spacing of (a) 1 mm and (b) 2 mm between electrodes is summarized in Fig. 3.39 (for Ag_Ge_xSe_{1-x} systems) and in Fig. 3.40 (for Cu_Ge_xSe_{1-x} systems), which shows the variation of response when selenium content is increased. The results presented in Figs. 3.38 and 3.39

have two important ramifications. First, they reveal a clear dependence of the observed resistance variation (i.e., radiation-induced diffusion process) on the atomic ratio of the Ge_xSe_{1-x} system. This dependence demonstrates the importance of chalcogen atom concentration on radiation-induced metal transport processes. The higher Se content makes the devices much more dynamically reactive to radiation. From the point of view of sensor characteristics, for the systems with Se-rich ChG films, the LOD is reached at smaller TID values (see Fig. 3.39). By changing the atomic ratio of the Ge_xSe_{1-x} film (i.e., selecting a Se poor or Se rich ChG), we can regulate the LOD of the sensor systems to a desired range. Second, both the LOD and DR of the Ag_Ge_xSe_{1-x} based devices display dependence on spacing regardless of the atomic ratio of the Ge_xSe_{1-x}. Exp. B experiments also demonstrated this effect on Ag_$Ge_{20}Se_{80}$ parts (i.e., with increase of spacing, LOD was found shifting to higher TIDs and DR decreasing to lower values) [89]. This study demonstrates that the above-mentioned trend is valid for other Ag_Ge_xSe_{1-x} systems as well. This happens due to the fact that when spacing is increased, the Ag doping fronts require higher levels of TID to transport additional amounts of Ag into the intermediate ChG film in order to make contact. This increases the LOD. On the contrary, a bigger spacing essentially increases the LRS or post-contact resistance level that ultimately reduces the dynamic range. Here the dynamic range is demonstrated to vary with the ChG composition [83]. Unlike Ag_Ge_xSe_{1-x} systems, no such effect of Ge_xSe_{1-x} atomic ratio has been observed on the Cu_Ge_xSe_{1-x} systems due to the instability of the Cu electrodes (Fig. 3.40).

Ag_Ge$_x$Se$_{1-x}$ Controls

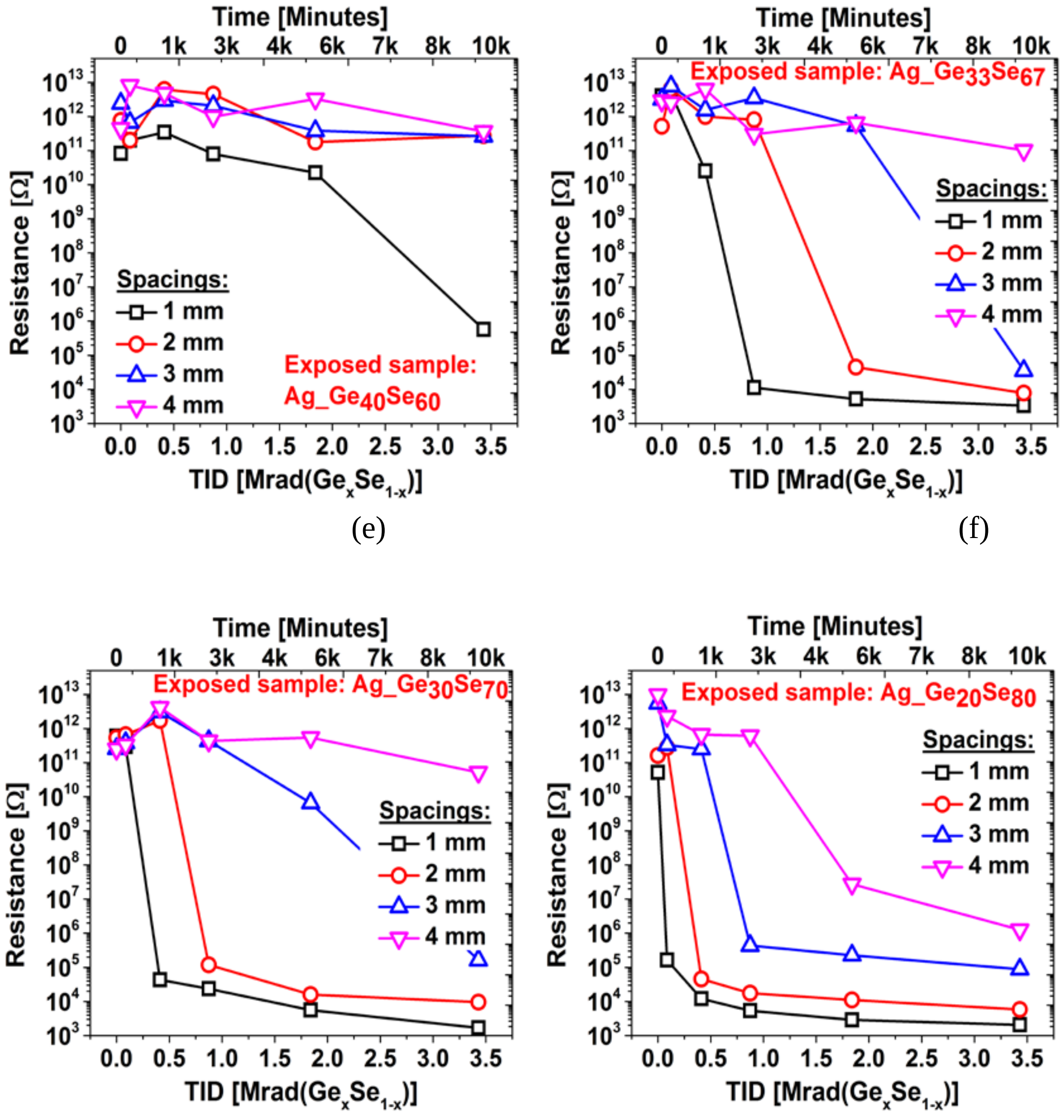


(a) (b)

(c) (d)

Fig. 3.38 (part 1 of 2): Resistance measured on control devices (a, b, c, d) of Ag_Ge$_x$Se$_{1-x}$ based systems with different atomic ratio. From (a) to (d) the atomic percent of sulfide of the film increases (Ge$_{40}$Se$_{60}$, Ge$_{33}$Se$_{67}$, Ge$_{30}$Se$_{70}$, Ge$_{20}$Se$_{80}$). Results for devices with different spacing between electrodes (1 mm, 2 mm) are also presented.

Ag_Ge$_x$Se$_{1-x}$ Test Samples

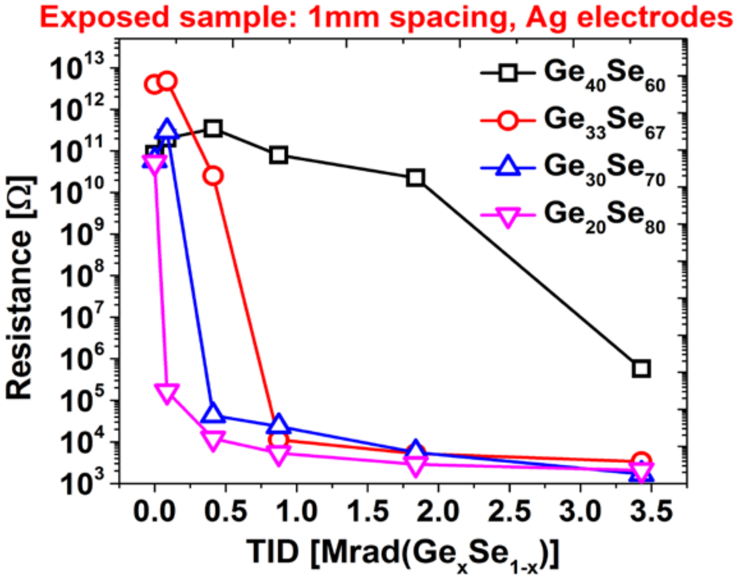


(e) (f)

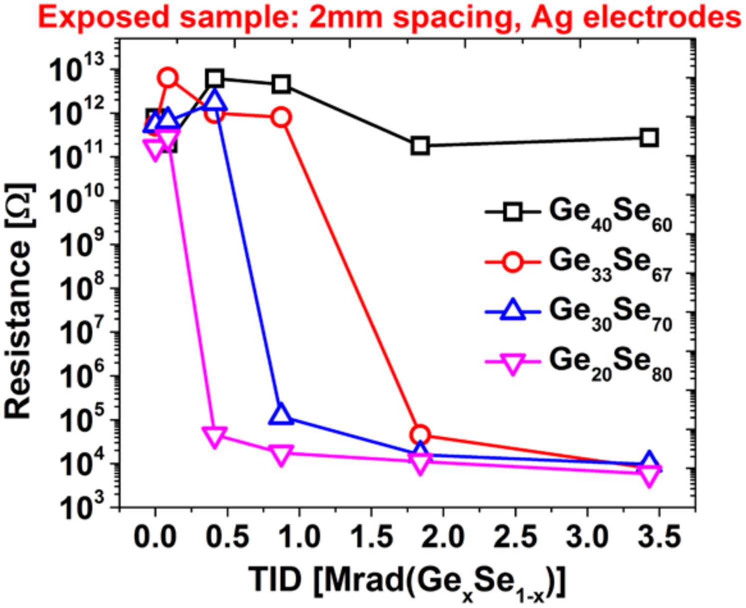
(g) (h)

Fig. 3.38 (part 2 of 2): Resistance measured on ^{60}Co gamma ray exposed test sample devices (e, f, g, h) of Ag_Ge$_x$Se$_{1-x}$ based systems with different atomic ratio. From (e) to (h) the atomic percent of sulfide of the film increases (Ge$_{40}$Se$_{60}$, Ge$_{33}$Se$_{67}$, Ge$_{30}$Se$_{70}$, Ge$_{20}$Se$_{80}$). Results for devices with different spacing between electrodes (1 mm, 2 mm) are also presented.

Effect of Ge_xSe_{1-x} atomic ratio (Ag electrodes)



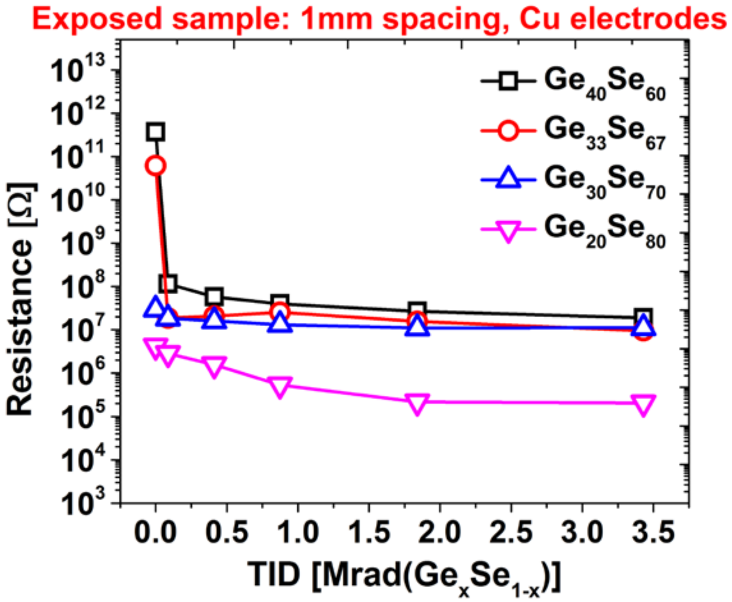
(a)



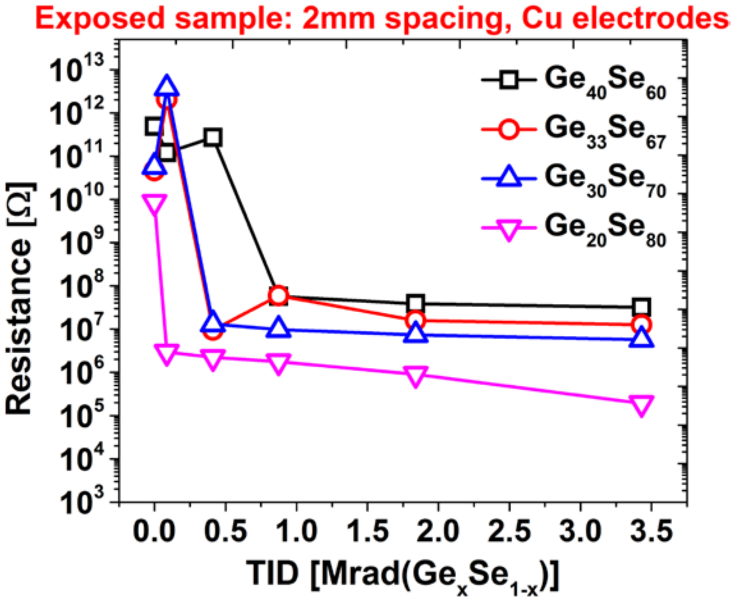
(b)

Fig. 3.39: Comparison among exposed samples with fixed (a) 1 mm spacing and (2) 2 mm spacings with Ag electrodes and with different atomic ratio of Ge_xSe_{1-x}. It's evident that atomic ratio plays a role on sensor performance when Ag is used as electrode. Higher selenium content in the ChG matrix results in lower LOD.

Effect of Ge_xSe_{1-x} atomic ratio (Cu electrodes)



(a)



(b)

Fig. 3.40: Comparison among exposed samples with fixed (a) 1 mm spacing and (2) 2 mm spacings with Cu electrodes and with different atomic ratio of Ge_xSe_{1-x}. Unlike Ag_Ge_xSe_{1-x} systems, no effect of Ge_xSe_{1-x} atomic ratio has been observed due to the instability of the Cu electrodes.

Though we observed that the choice of metals from group 11 in the periodic table can impact the sensor performance, it is not clear how the size of the metal atom plays role in the radiation induced diffusion processes. One can claim that, metals with smaller atoms can more easily move into the amorphous structure of the ChG films. In reality, this might not be accurate since in the case of radiation-induced metal doping, all metals transport as ions and even having a larger atomic radius, Ag ions diffuse more readily than Cu ions in the ChG [90]. This happens due to the unique electronic configuration of Ag which contributes to formation of ion with a very small radius, thus enabling a high mobility of the Ag ion. Our present work does not include any annealing study by irradiating the samples at elevated temperature. However, in Exp. A, we evaluated the effect of elevated operating temperature on the sensor characteristics (room temperature to 150° C). For the irradiated devices, the test data showed that the LRS falls within the range of resistance values of the sensor devices measured before temperature stressing. For non-irradiated or unexposed devices, the HRS showed no change with temperature. It is suggested that extended high-temperature annealing could cause silver diffusion in the chalcogenide glass [71], [83]. Table III summarizes the experimental results.

TABLE III

SUMMARY OF EXPERIMENTAL RESULTS AND OBSERVATION

Sensor System	Comments
Cu_Ge_xS_{1-x}	No clear radiation induced diffusion observed.
Ag_Ge_xS_{1-x}	No clear radiation induced diffusion observed.
Au_Ge_xSe_{1-x}	No clear radiation induced diffusion observed.
Cu_Ge_xSe_{1-x}	No clear radiation induced diffusion observed.
Ag_Ge_xSe_{1-x}	Clear radiation induced diffusion observed. Promising for radiation sensing application.

3.6. Conclusion:

In this report, we discussed the current development status of the flexible radiation-sensing devices which rely upon resistance change in flexible ChG films as a result of radiation-induced diffusion of some selected metals (e.g., Ag, Cu) into the chalcogenide glass. The sensors were stressed mechanically by bending them inward and outward to produce a range of compressive and tensile stresses and were also exposed to elevated temperatures to assess their stability. The HRS and LRS of the devices did not show significant degradation following mechanical or thermal stress although further research is needed to understand the limits of such operational trauma. We also presented test results on Ag-chalcogenide glass flexible radiation sensors with different electrode design parameters. Results show that by changing the different physical design parameters (e.g, electrode placement, size, ChG film thickness and electrode thickness etc.) it is possible to change the limit of detection and dynamic range to a desired dose level. In addition, test results were also reported on several metal-ChG based systems with Ag, Cu and Au electrodes along with different composition and atomic ratio of ChG films, in order to understand their suitability for radiation detection application. Ag_Ge_xSe_{1-x} based systems showed better response for lateral devices compare to Cu-Ge_xSe_{1-x} based systems. In fact, Cu-Ge_xSe_{1-x} based systems were basically found not suitable for radiation detection application due to their unstable controls and false positive responses. For the cases of sulfides, though some radiation induced metal transport has been observed for Cu- Ge_xSe_{1-x} based systems, but no visible or very negligible metal migration has been observed for Au- Ge_xSe_{1-x} and Ag-Ge_xS_{1-x} based systems. This shows that sulfide based systems might not be good fit for lateral based radiation detection sensors. However, they might be good candidate for vertical devices where the slower metal diffusion behavior can come as an advantage. For both selenide and sulfide cases, faster variation of resistance level (in other words, faster radiation induced metal transport) has been observed for the chalcogen rich samples. The sensors we developed are thin, lightweight, and capable of instantaneous readout with a low voltage. All of these positive factors make this technology a strong candidate in the field of electronic radiation dosimetry.

CHAPTER 4

WIRELESS TOTAL IONIZATION DOSE SENSOR BASED ON METAL OXIDE SEMICONDUCTOR LOADED PATCH ANTENNA

4.1. Background:

In previous chapter, a mechanically flexible metal-chalcogenide glass (ChG) based radiation detector systems intended as disposable total dose sensors was presented. In addition to that, another kind of novel, low cost, wireless dosimeter technology intended for remote total dose sensing was also developed. They are based on a capacitively loaded folded patch antenna (CLPA) resonating in the range of 3 GHz to 8 GHz for which the load comprises a device whose capacitance varies as a function of total dose. The dosimeter does not need power to operate thus enabling its use in the field without requiring a battery for its read-out. As a result, the dosimeter is suitable for applications such as unattended detection systems destined for monitoring of merchandise crossing borders, where nuclear material tracking is a concern [91].

Although the ‘detector in transit’ or ‘sensor network’ concept is not new, practical implementations have mostly been limited spatially to very few points of detection. There is a strong demand for an innovative highly sensitive TID detection technology that can detect very small amount of radiation emitting from common radioactive sources which can be shielded.

In addition, the nuclear non-proliferation and forensic entities might also prefer a cost effective reliable system that can enable deployment of sensor networks for efficient radiation detection across large storage facilities, transportation containers, and vehicles.

The MOS capacitor based novel, wireless, widely-distributed sensor technology (developed in collaboration with CFD Research Corporation, Huntsville, AL 35806) has the potential to greatly meet the above-mentioned challenges and reduce many of the vulnerabilities in some of the existing state-of-the-art technologies, by utilizing their sensitivity to low dose of ionizing radiation, small form factor and modest manufacturing cost.

They can blanket containers, walls, equipment panels, packages or cargo in transit, embedded in paint or fabric liners, etc. This vastly increases the solid angle (geometric efficiency) of detection. It also allows for prolonged exposure throughout the transit time between ports, enabling detection of even low amounts of radiation from cargo. If only one region of the blanketing sensors indicates a high dose reading, it would be indicative of the presence of radioactive material. Furthermore, the RF interrogation could be triggered to obtain an integrated dose reading at any time and transmitted to provide real-time data of cumulative dose at a stand-off range.

In addition to detecting transport of nuclear materials, other important civilian applications can be monitoring contamination and aiding cleanup in facilities that handle nuclear material such as nuclear power plants or decommissioning facilities, for instance, after disasters such as at Fukushima Daiichi in Japan in 2011. Application in the medical field could also be considered if dimension down-scaling of the system is done, which is possible and leads to the respective modifications of the operating frequency range. The sensitive element can be any device exhibiting a known variation of capacitance with total dose. In this chapter, preliminary results for a prototype device (i.e., wireless dosimeter) with a metal-oxide-semiconductor (MOS) capacitor will be presented. The sensitivity of the dosimeter will be related to the capacitance variation of the radiation sensitive device as well as the high frequency system used for reading. The next section (i.e., 4.2) discusses the concept of the sensors and some design guidelines for optimized performance. The manufacturing of the MOS capacitors and device characterization results are presented in section 4.3. Results obtained from the RCS testing of the MOS capacitor loaded patch antennas are explained in Section 4.4. Section 4.5 then gives an overview of the potentiality of the discussed system to be used for wireless dosimetry. Finally, Section 4.6 summarizes the chapter based on the experimental results. For interested readers, TCAD modeling to derive MOS capacitor design guidelines and electromagnetic modeling to obtain folded patch antenna design parameters are provided in Appendix A and B. The simulations were performed by CFD Research Corporation, Huntsville, AL (CFDRC) using NanoTCAD and ANSYS HFSS simulation software and were guided by the experimental data generated here at ASU and discussions with ASU researchers (i.e., author and his research advisers) [92].

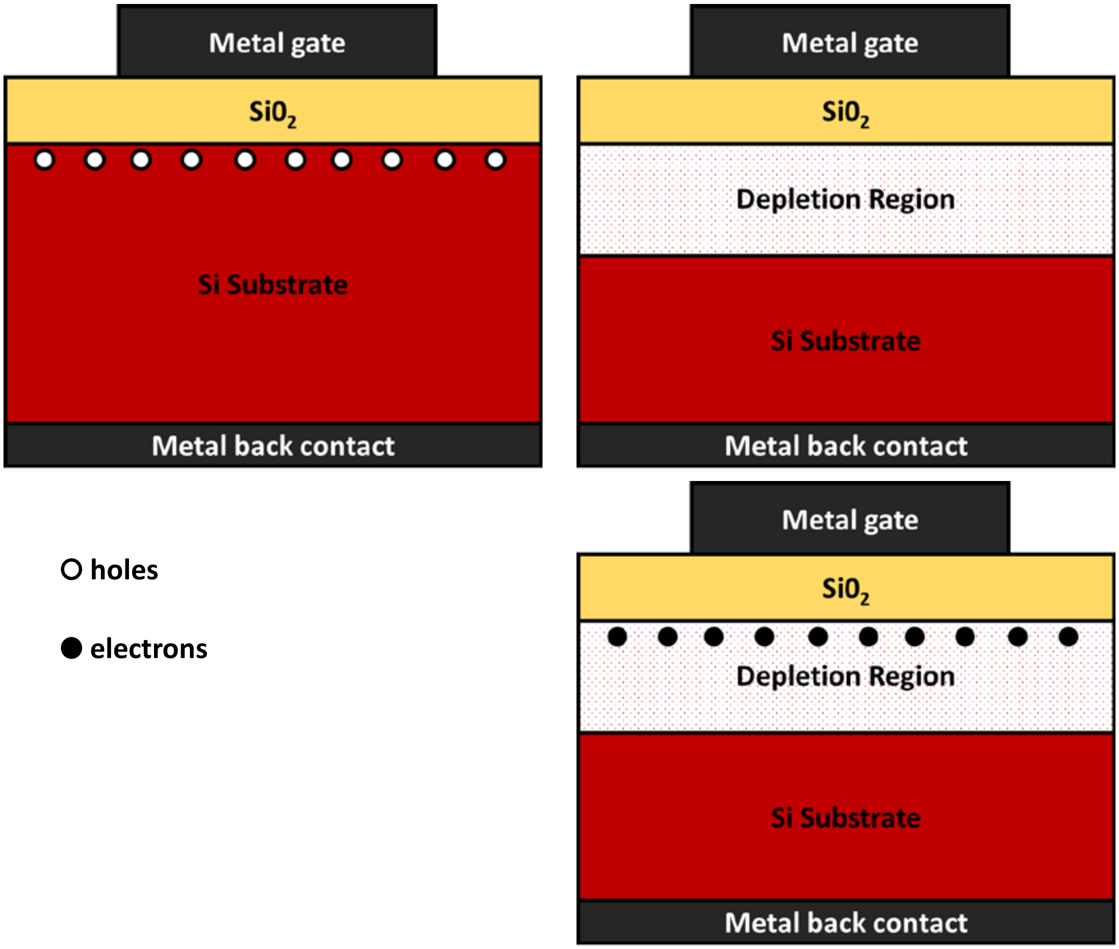
4.2. Sensor Concept:

4.2.1. MOS based core radiation sensor:

The wireless sensing system consists of two main components: (i) a sensor architecture, containing a combination of radiation-sensitive MOS capacitor and a folded patch antenna to yield a high-sensitivity device and (ii) an RF interrogator, that utilizes radio-frequency (RF) signals to probe the sensors, and calculates absorbed dose from modifications in the received signal. Here, the discussion will be limited to sensor architecture.

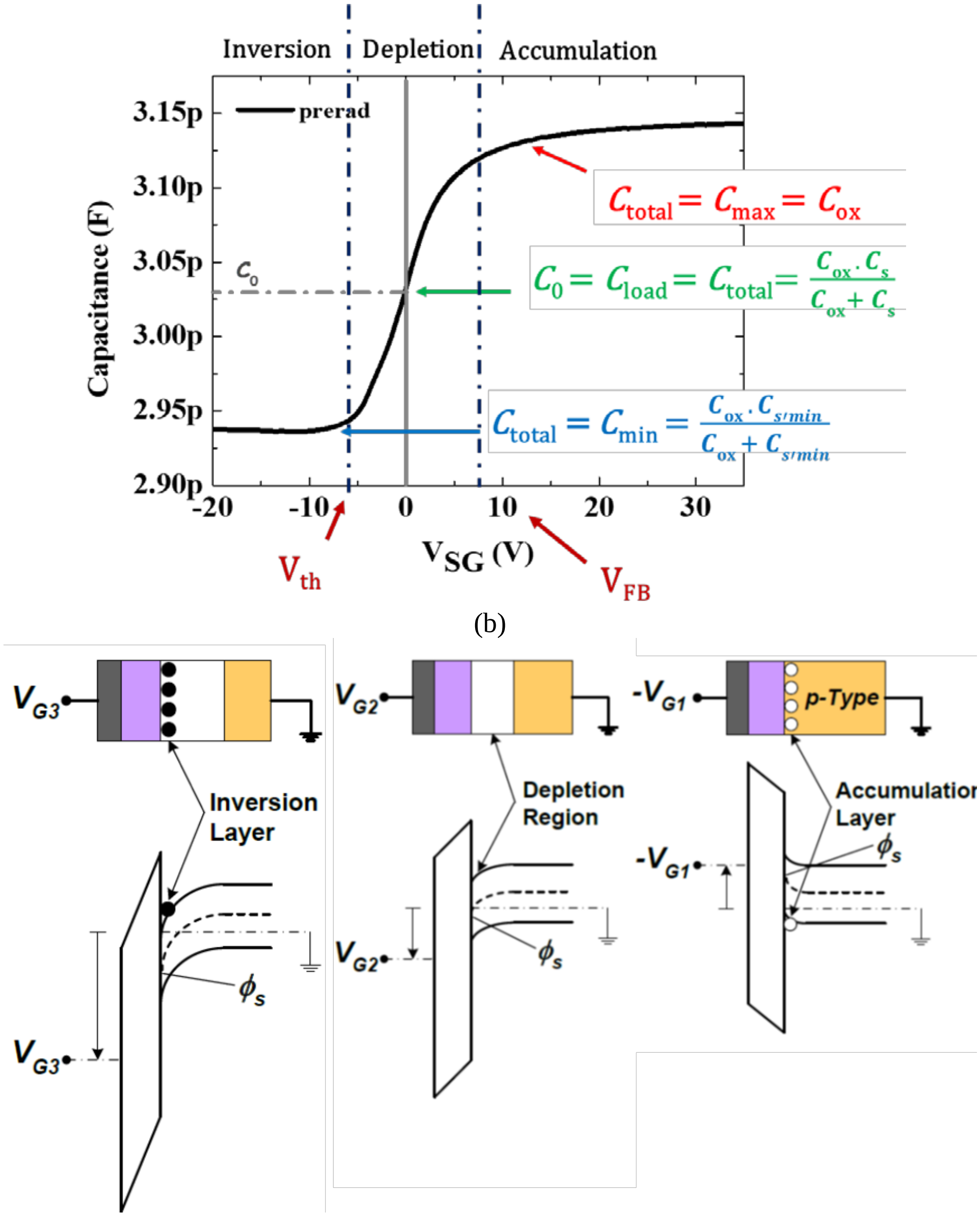
The MOS capacitor in the sensor structure loads an electrically small folded patch antenna and modifies its frequency response to an incident electromagnetic wave. The size of the MOS capacitor is very small and it contains engineered charge-trapping precursors at the oxide film. The semiconductor used for the proposed sensor system is silicon, thereby enabling low cost fabrication in standard CMOS processes. For the dielectric or oxide material, SiO_2 films were used. The manufacturing process is engineered in such a way so that the majority of the radiation-sensitive charge-trapping precursors are located near the semiconductor/SiO_2 interface (< 50 nm). These precursors are typically oxygen vacancies, but may also be specially engineered trapping sites such as nano-clusters. The density and distribution of these trapping sites can be controlled by varying fabrication conditions. For this discussion, a uniform doping condition in the silicon which is p-type is assumed.

Fig. 4.1(a) presents a cross-section of a MOS capacitor with a 500 µm x 500 µm metal gate. A corresponding capacitor-voltage (C-V) plot under high frequency operation mode is presented in Fig. 4.1(b) which covers different operating regimes (i.e., accumulation, flat band, depletion, inversion). Boundary lines and labels demarcate the different operating regimes on the plot along with the equations to calculate equivalent capacitance values. Fig. 4.1(c) exhibits relevant surface condition at different operating regimes and corresponding band diagrams.



(a)

Fig. 4.1 (part 1 of 2): (a) General cross section of SiO_2/Si (p-type) MOS capacitor with top metal gate area of 500 µm x 500 µm at different operation regime: accumulation (top left), depletion (top right) and inversion (bottom right).



(b)

(c)

Fig. 4.1 (part 2 of 2): (b) Corresponding C-V characteristics under high frequency conditions and (c) relevant surface conditions and band diagram for different operating regime [93]. Please note, the X-axis at (b) represents substrate to gate voltage.

Fig. 4.2 shows that the total areal capacitance of the MOS capacitor (F/cm^2), C_{tot}. This

C_{tot} can be considered as a series combination of two capacitors: capacitance due to the fixed dielectric (C_{ox}) and capacitance formed from the depletion layer in the silicon (C_{s}). As the substrate-to-gate voltage (V_{SG}) decreases, the depletion layer width (w_{d}) in the silicon increases. The depletion layer or space charge region width and the differential capacitance across this layer can be expressed as

$$w_d = \sqrt{\frac{2k_{si}\varepsilon_0\phi_s}{qN_A}} \dots\dots\dots\dots (1)$$

and

$$C_s(V_{GS}) = \frac{dQ}{d\phi_S} \approx \frac{k_{si}}{w_d V_{GS}}\ , \dots\dots\dots\dots (2)$$

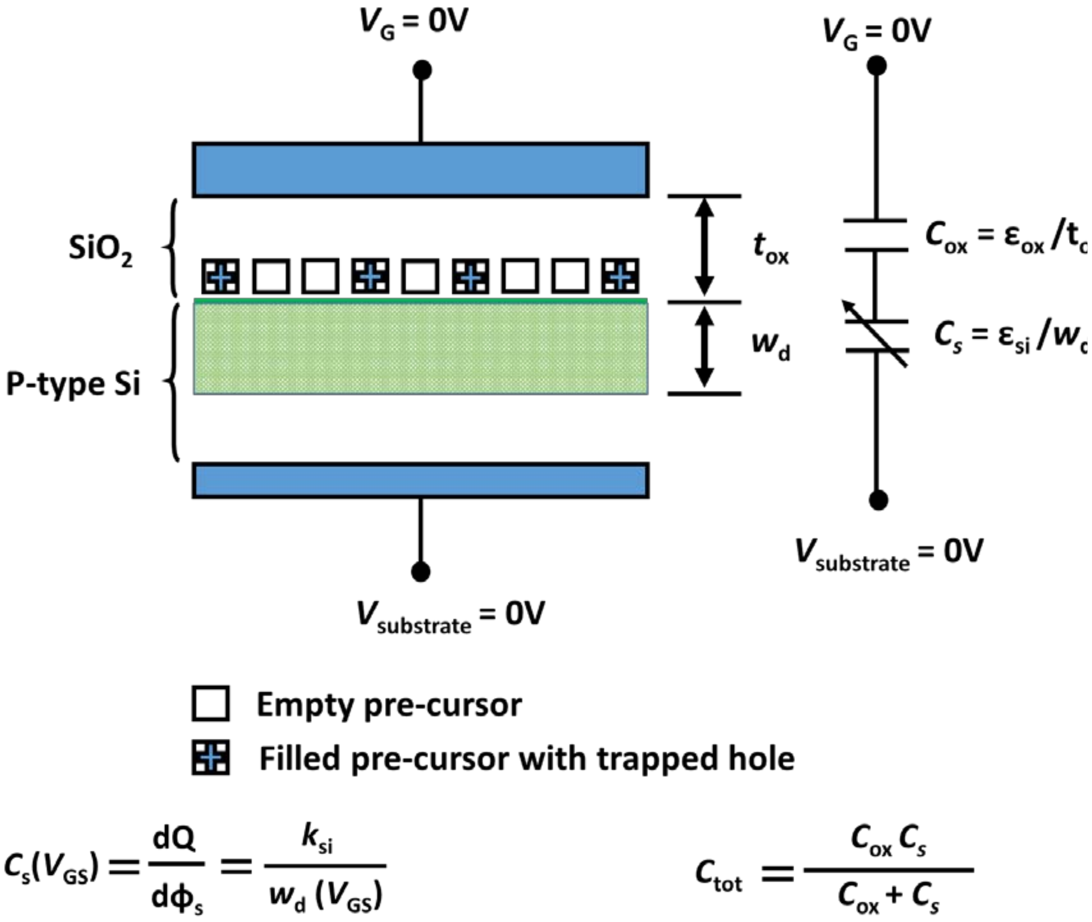
where, k_{si} is the relative permittivity of Si, ε_0 is vacuum permittivity, ϕ_{s} is surface potential, q is charge of electron, N_{A} is doping concentration in Si and dQ is the change in space-charge with a corresponding change in surface potential in the Si ($d\phi_{\text{s}}$). Also, the maximum and minimum equivalent capacitance can be expressed as

$$C_{max} = C_{ox} = \frac{k_{ox} \cdot \varepsilon_0}{t_{ox}} \dots\dots\dots\dots (3)$$

and

$$C_{\text{min}} = \frac{C_{ox} \cdot C_{s_{\text{min}}}}{C_{ox} + C_{s_{\text{min}}}}, \dots\dots\dots\dots (4)$$

where, k_{ox} is the relative permittivity of the oxide and $C_{\text{s-min}}$ is the minimum semiconductor capacitance when depletion layer width is maximum (i.e., $w_{\text{d-max}}$). The ratio between C_{max} and C_{min} determines the dynamic range of the sensors. Eqns. (1) to (4) show that both the doping concentration N_A and the oxide thickness ratio affect the dynamic range.



$$C_s(V_{GS}) = \frac{dQ}{d\phi_s} = \frac{k_{si}}{w_d\,(V_{GS})} \qquad C_{tot} = \frac{C_{ox}\,C_s}{C_{ox} + C_s}$$

Fig. 4.2: Illustration of the MOS capacitor. The total capacitance (C_{tot}) is determined by the fixed oxide capacitance (C_{ox}) in series with the variable semiconductor capacitance (C_s). In the equations shown in the figure, w_d is the semiconductor depletion layer width which depends on the gate-to substrate voltage V_{GS}; k_{si} is the relative permittivity of Si; ε_0 is vacuum permittivity; ϕ_s is surface potential; ε_{ox} and ε_{si} are the permittivity of oxide and silicon respectively.

Fig. 4.3 presents the effect of oxide thickness t_{ox} on the (C_{max}/ C_{min}) ratio. When the oxide thickness is increased, it reduces the capacitance across the oxide (C_{ox}). This

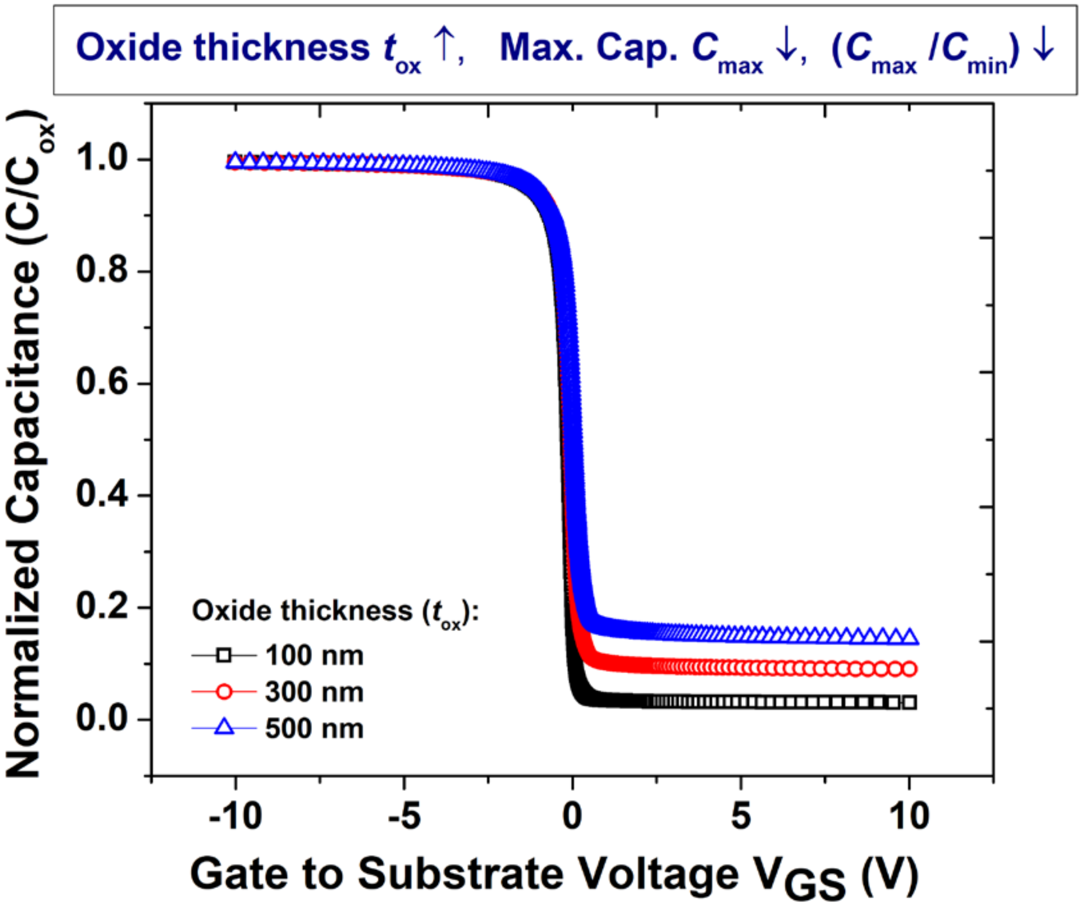


Fig. 4.3: Normalized capacitance-voltage (C-V) characteristics of a MOS capacitor under high frequency conditions with different oxide thickness, while all the other parameters are fixed (e.g., doping concentration, temperature, applied voltage etc.). Plot shows that increasing the oxide thickness reduces the oxide capacitance (C_{ox}). Since $C_{max} = C_{ox}$, this reduces the (C_{max} / C_{min}) ratio of the MOS capacitor. However, difference between V_{FB} and V_{th} remain unchanged for change in oxide thickness. [94]

results in a decrease in the (C_{max}/ C_{min}) ratio as well as a smaller dynamic range. Similarly, Fig. 4.4 exhibits the effect of doping concentration N_A on the (C_{max}/ C_{min}) ratio. Fig. 4.3 indicates that the MOS capacitor t_{ox} can play a role in setting C_{max}/ C_{min}. Fig. 4.4 shows that when N_A increases, it reduces $w_{d\text{-}max}$ (Eqn. 1).

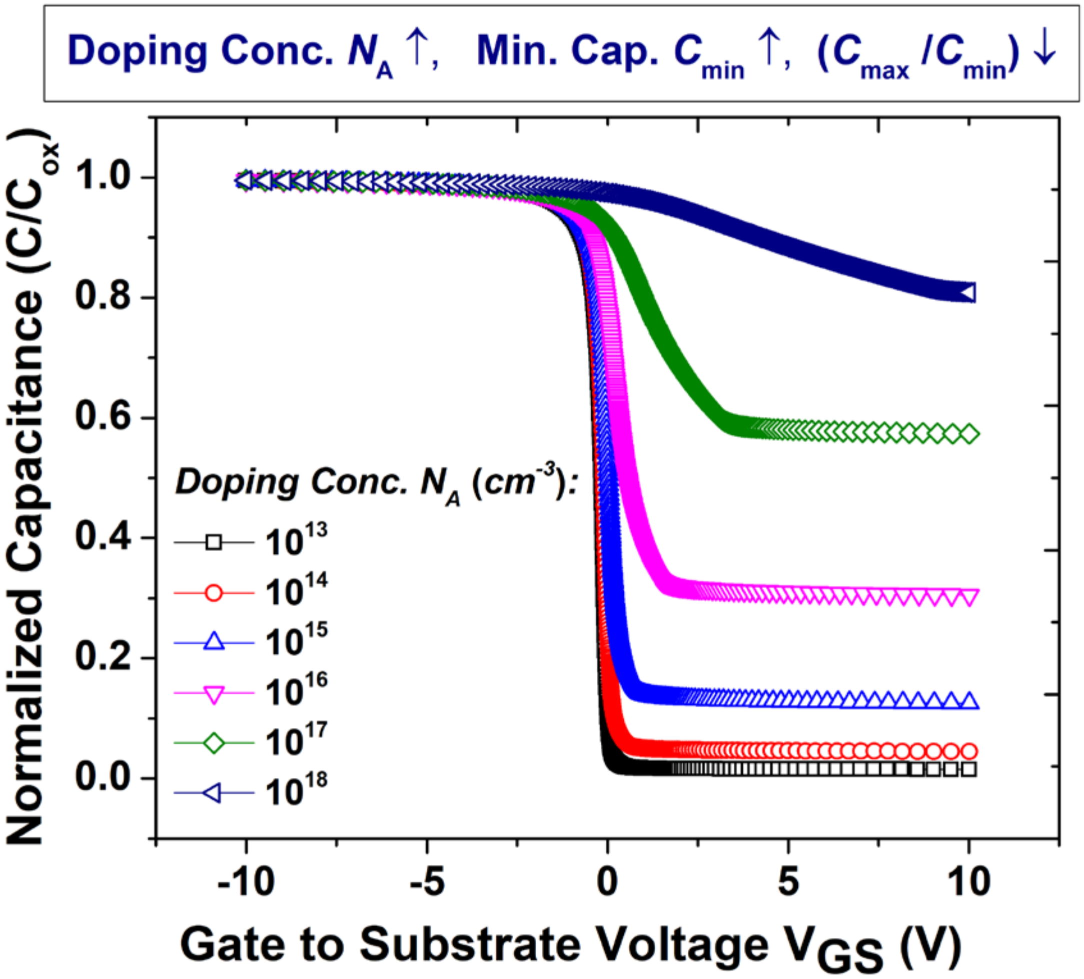


Fig. 4.4: Normalized capacitance-voltage (C-V) characteristics of a MOS capacitor under high frequency conditions with different doping concentration, while all the other parameters are fixed (e.g., oxide thickness, temperature, applied voltage etc.). Plot shows that increasing the doping concentration reduces depletion width (w_d) which consequently increases the C_{min} while C_{max} remains unchanged. As a result, (C_{max}/C_{min}) ratio of the MOS capacitor reduces as well. Also, difference between V_{FB} and V_{th} gradually increased while increasing the doping concentration. [94]

A smaller w_d increases the minimum capacitance across the space charge region, $C_{s\text{-min}}$ (Eqn. 2). This results in a larger minimum equivalent capacitance, C_{min} (Eqn. 4). Since, C_{max} or the capacitance across the oxide remains unchanged, a larger $C_{s\text{-min}}$ brings down the (C_{max}/ C_{min}) ratio, again resulting in a smaller dynamic range. Thus, from dynamic range point of view, lower doping concentration might be attractive. However, reducing the doping concentration (therefore increasing resistivity) increases the series resistance of the semiconductor which can detrimentally impact the resonant frequency response of the sensor structure (a discussion on this topic will be provided later in the chapter). Therefore, choosing the MOS capacitor design parameters (e.g., oxide thickness, substrate resistivity, metal type etc.) for optimum performance need careful consideration.

4.2.2. Radiation sensing mechanism using the MOS capacitor:

When the MOS capacitor is exposed to ionizing radiation (e.g., gamma radiation), the high energy photons interact with the valence band electrons in the dielectric (i.e., SiO_2). The incident photons can transfer enough energy to a valence band electron to jump the band gap of SiO_2 to reach into the conduction band. This process generates electron hole pairs (ehps) [95]. Fig. 4.5 shows the typical energy band diagram of a MOS capacitor that shows the physical processes that lead from the initial deposition of energy by the high energy photons to the creation of trapped charges [96]. The total amount of energy deposited by these high energy photons that generate electron hole pairs (ehps) in the targeted material is referred as total ionization dose (TID). The typical unit of TID is rad or Gray which indicates the energy absorbed per unit mass of a material. One rad(material) is equivalent to 0.01 J absorbed by one kilogram of the target material. Once generated, a fraction of the ehps will promptly recombine [97], [98].

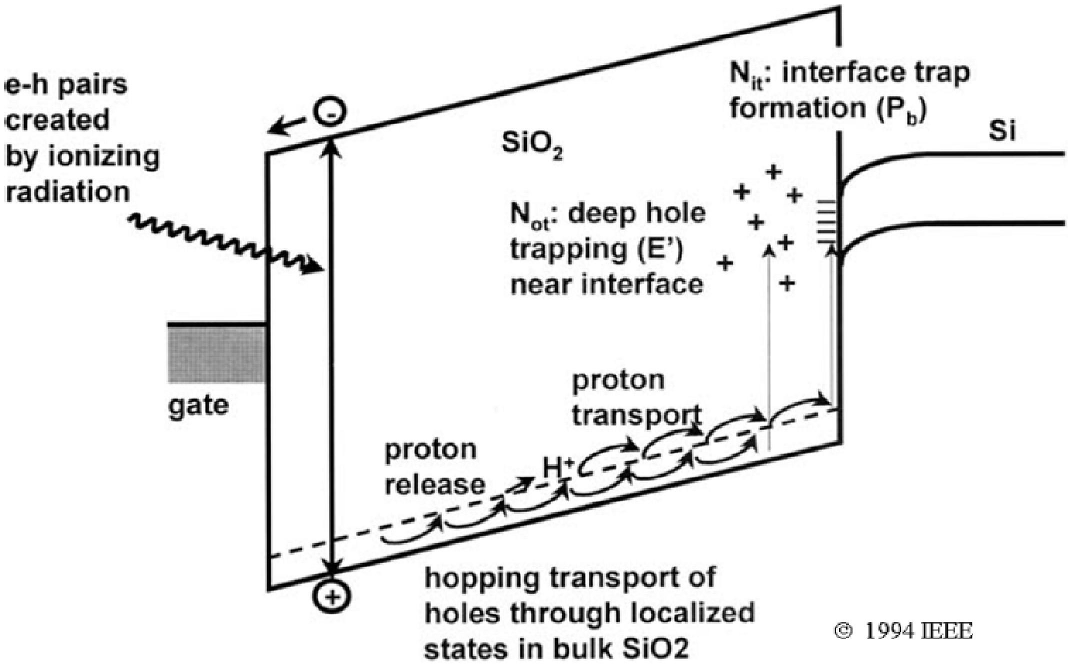


Fig. 4.5: Schematic of ionizing radiation-induced processes in an MOS capacitor. [96]

Now, for a MOS capacitor with p-type substrate, if the metal work function is slightly smaller than the work function of the semiconductor, it will generate a positive electric field in the SiO_2 without an external bias, since thermodynamics require the two fermi levels (i.e., metal and Si) to get aligned. This positive electric field aided by the comparative high mobility of the conduction band electrons in SiO_2 (i.e., ~20 cm^2/V-s) causes them to flow out to the metal gate terminal [95], [97]. On the other hand, the generated holes have an effective mobility in the range of 10^{-4} to 10^{-11} cm^2/V-s, which

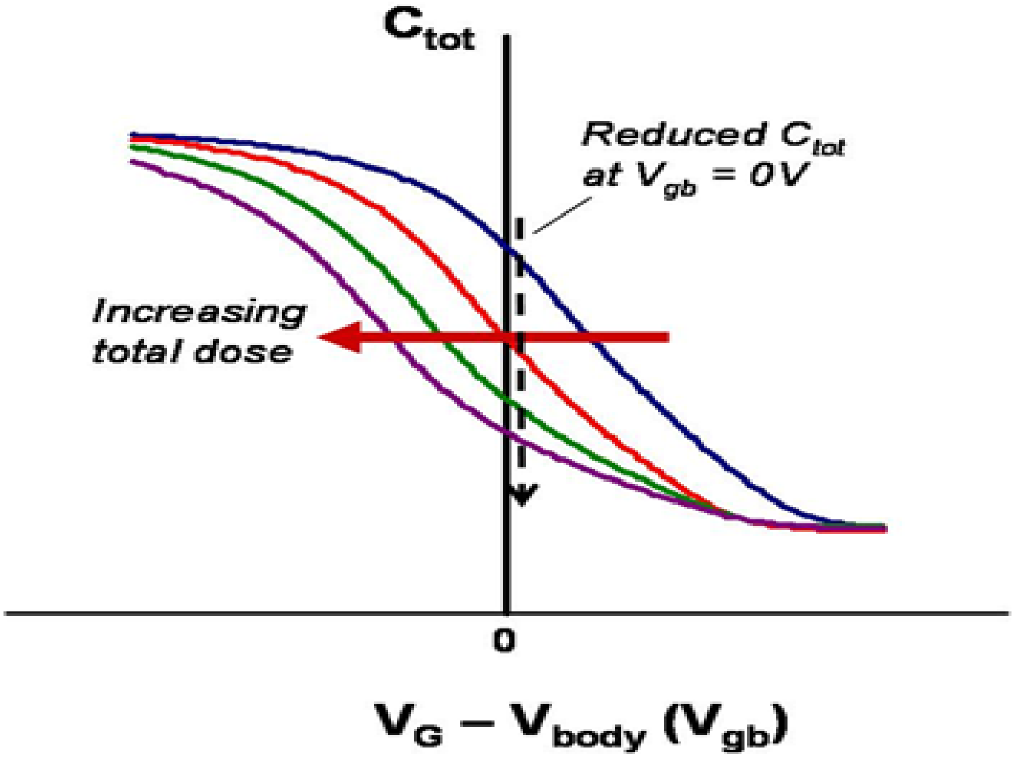


Fig. 4.6: Ionizing total dose causes the MOS capacitor C-V characteristics to shift to the left. No static dc gate-to-body bias is applied during exposure or during monitoring. It is the change in C_{tot} at $V_{GS} = 0V$ (dashed line above) which is the radiation signature.

make them relatively immobile in the oxide compare to electrons [95], [96]. These surviving holes will undergo a polaron hopping transport via the shallow traps in the SiO_2 (shown schematically in Fig. 4.5). A fraction of these transporting holes may fall into deep traps in the oxide bulk or near the oxide-semiconductor interface, thereby forming trapped positive charges [98]. These trapped positive charges near the interface increases the surface potential, ϕ_s (and as well as enlarges the depletion layer width, w_d in Eqn. 1) in the underlying silicon, thereby decreasing C_s, C_{tot} and causing a negative shift in the threshold voltage of the MOS capacitor C-V curve (Fig. 4.6). For the sensor implementation, no static dc gate-to-body bias is applied during exposure or monitoring. It is the change in C_{tot} at V_{GS} = 0V which is the radiation signature.

4.2.3. RF Interrogator:

The RF interrogator is a separate unit (e.g., hand-held wand) aside from the MOS capacitor loaded patch antenna, that transmits radio-frequency (RF) signals of a designed frequency and profile (e.g., chirp) and receives reflected signals from the network of patch antennas. The frequency response detected by RF interrogation is dependent on the capacitive load (C_{load}) of the sensors, and therefore, is a function of the total radiation dose incident on the device, enabling wireless, standoff detection of a radiation source. The readout of the passive sensors can be accomplished with a regularity that suits the monitoring requirements.

4.2.4. Basic operation of the proposed system:

The basic operation of the proposed system is illustrated in Fig. 4.7. The frequency response of a capacitively-loaded patch antenna (CLPA) can be modeled using an RLC equivalent circuit that resonates at a frequency f_{res}, dependent on the geometry/size of the patch antenna as well as on its capacitive load C_{load}. With a change of C_{load}, the patch equivalent circuit is modified, leading to a variation of its resonant frequency [99]. Considering that the antenna itself is not impacted by ionizing radiation, the variation of f_{res} is directly induced by a variation of the device capacitance used to load the patch antenna.

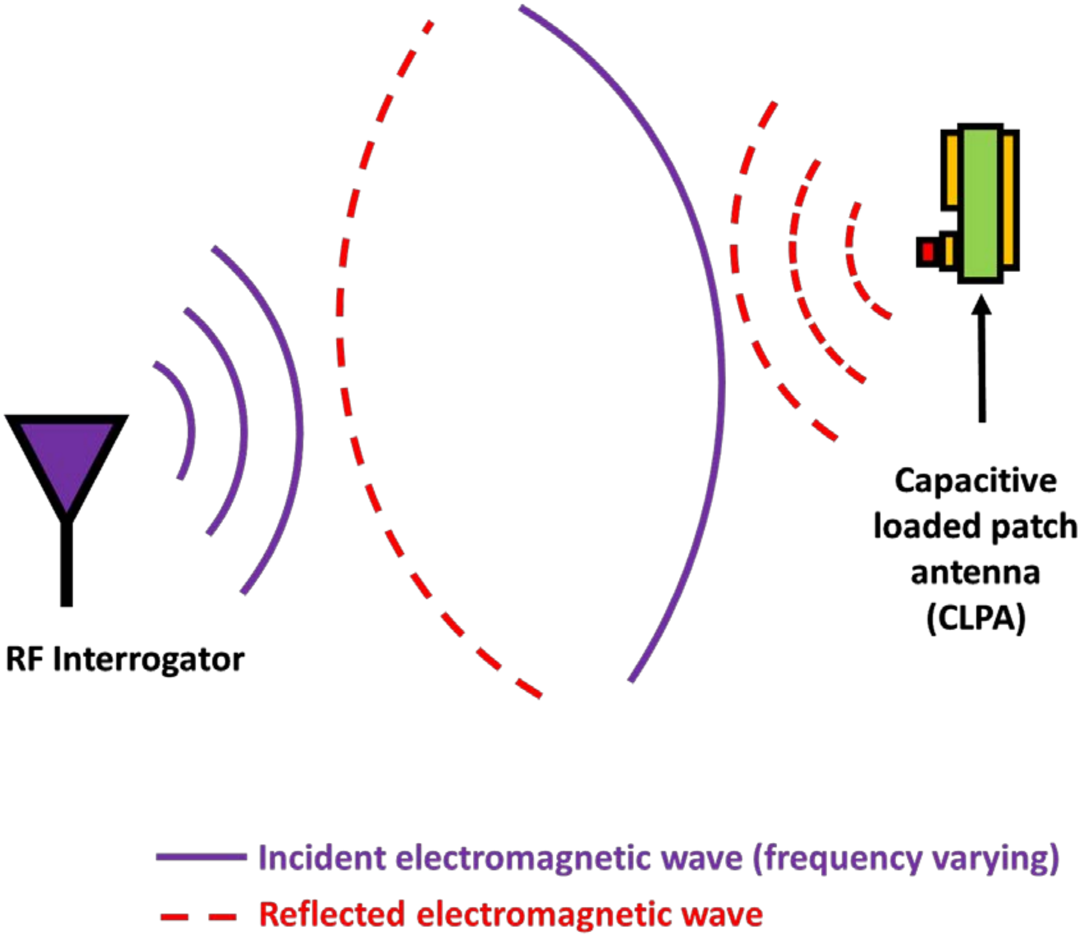
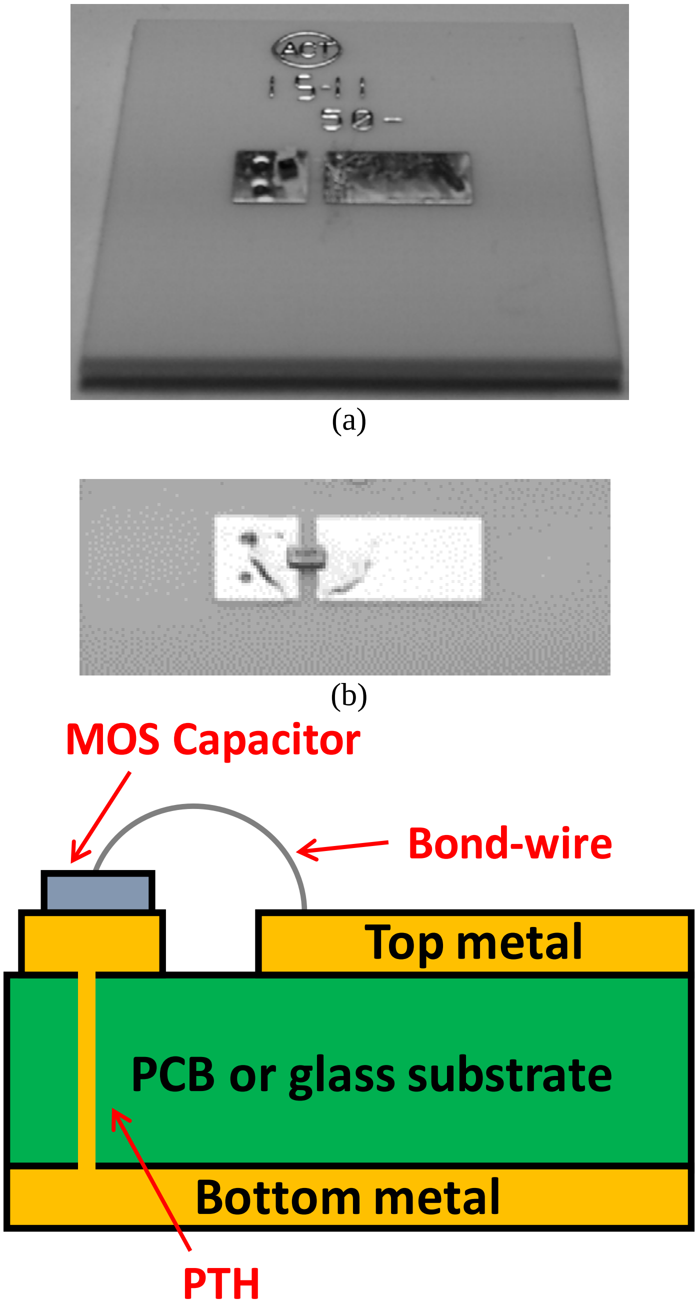


Fig. 4.7: Basic schematic of the operation of the system. An RF interrogator sends electromagnetic waves within the range of frequency of interest. When the electromagnetic waves with f_{res} encounter the resonating system (patch antenna), part of the electromagnetic wave energy is coupled in the resonator and can then be detected.

An implementation of a CLPA is presented in Fig. 4.8, showing micrographs of both MOS capacitor and “surface mount discrete (SMD) hyper-frequency capacitor” loaded patch antennas along with a cross section. As can be seen, the MOS capacitor is implemented on the top side of the patch antenna, with its gate terminal wire-bonded to the top metal plate of the folded patch antenna. The substrate of the antenna is connected to the bottom side of the patch antenna through a plated through-hole (PTH) implemented on the soldering pad of the loading element.



(c)

Fig. 4.8: (a) Microphotograph of one patch antenna capacitively loaded with a 0.5 pF MOS capacitor (b) capacitively loaded with a SMD hyper-frequency capacitor (c) schematic cross-section of the implementation of the CLPA.

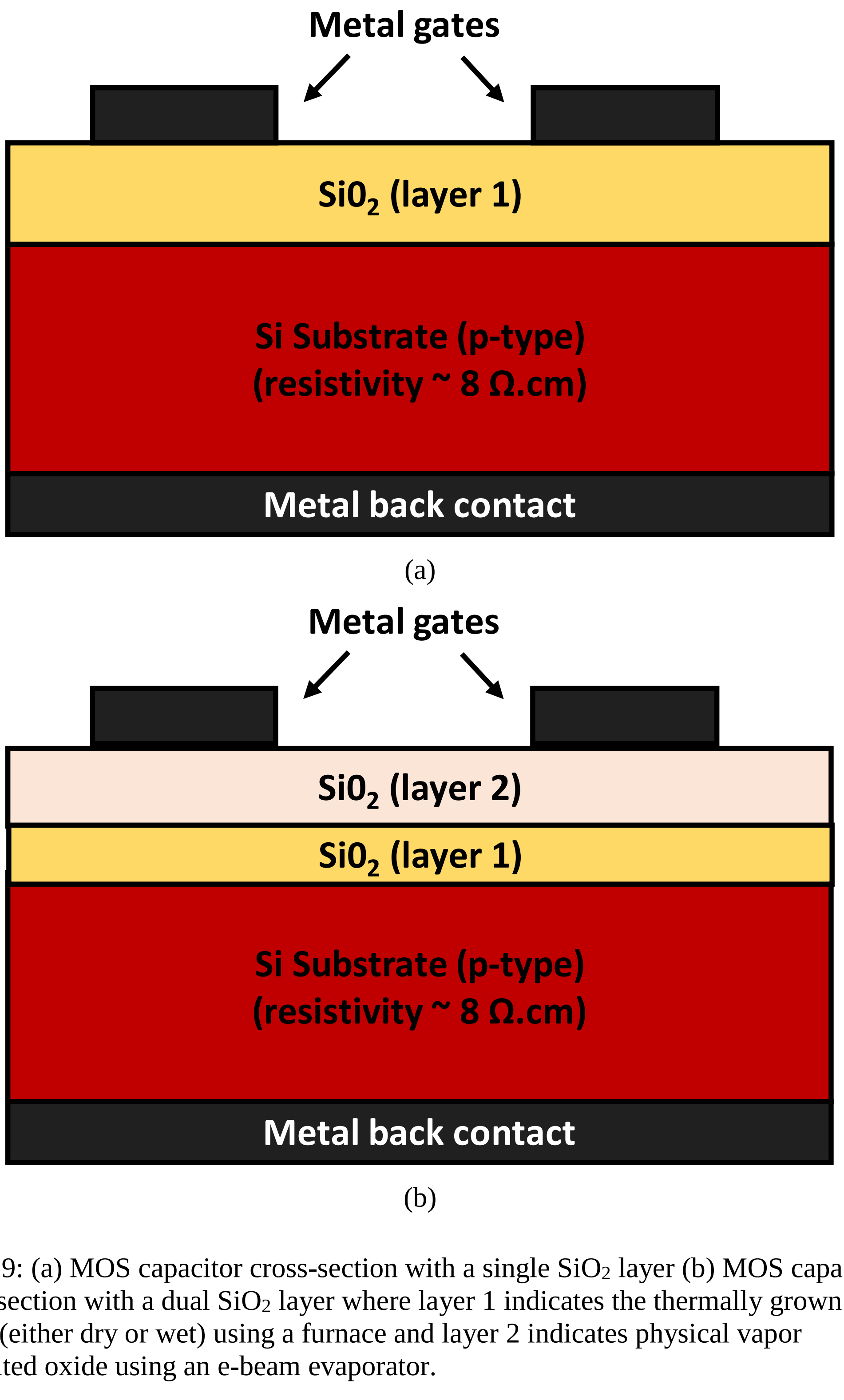
4.3. MOS Capacitor Loaded Patch Antenna Fabrication and Testing:

4.3.1. MOS Capacitor Structure:

At the initial stage of the project, two different MOS capacitor structures with different oxide stacks were considered. Fig. 4.9 provide a schematic representation of these MOS capacitors. Different batches of devices were manufactured to assess the manufacturing process, and to obtain the desired values of capacitance (around 0.5 pF – based on design value of resonance frequency of the patch antenna). This included:

- Wet oxide 80 nm + aluminum gate
- Dry oxide 90 nm + aluminum gate
- Wet oxide 80 nm + evaporated oxide 400 nm
- Dry oxide 90 nm + evaporated oxide 400 nm
- Wet oxide 470 nm-500 nm

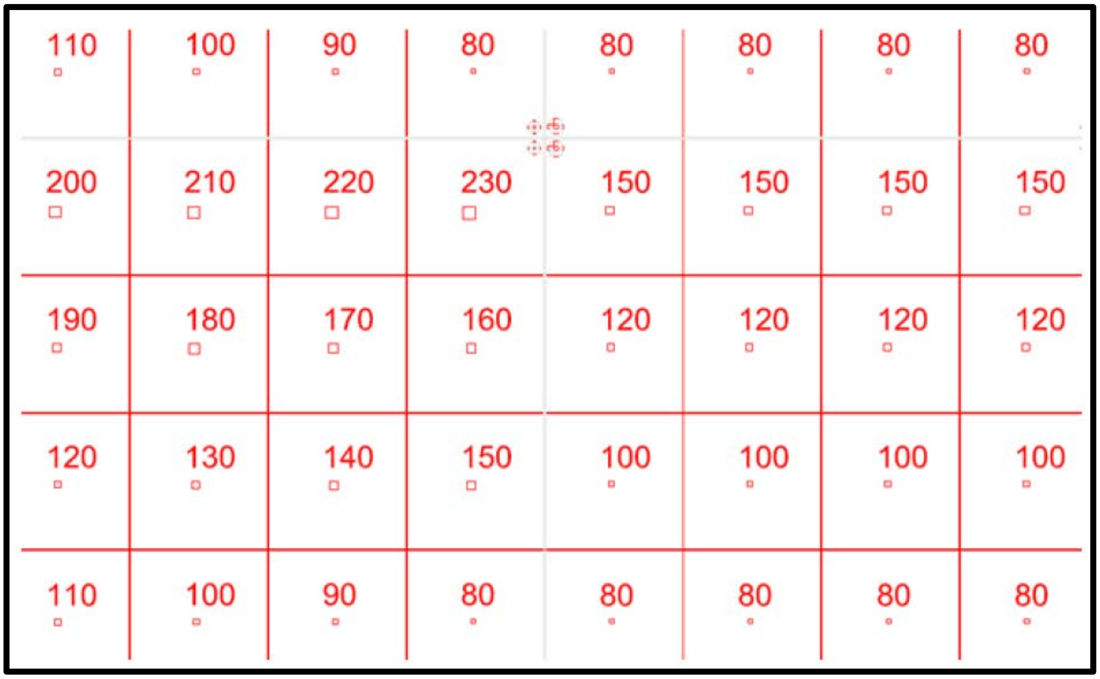
All these devices utilized an aluminum gate or a stack of “aluminum + chromium + gold” metal gate to ease the wire-bonding with gold wire. The backside substrate contact was formed by depositing 200 nm thick aluminum followed by forming gas annealing to form ohmic contact. Fig. 4.10 presents the design of the mask that has been used to obtain the broad range of capacitance values for a particular oxide thickness. The grid lines in the mask shows the dicing path. The squares of different sizes indicate the gate area and the numbers written on top of them tells the side length of the squares in µm.



(a)

(b)

Fig. 4.9: (a) MOS capacitor cross-section with a single SiO_2 layer (b) MOS capacitor cross-section with a dual SiO_2 layer where layer 1 indicates the thermally grown oxide (either dry or wet) using a furnace and layer 2 indicates physical vapor deposited oxide using an e-beam evaporator.



110	100	90	80	80	80	80	80
200	210	220	230	150	150	150	150
190	180	170	160	120	120	120	120
120	130	140	150	100	100	100	100
110	100	90	80	80	80	80	80

Fig. 4.10: The mask was designed with an objective to obtain several capacitance values from a single sample with a fixed oxide thickness. This enabled us to get MOS capacitors with capacitances (i.e., C_{max}) close to the desired value even when there was a process related variation in the oxide thickness. The grid lines in the mask shows the dicing path. The squares of different sizes indicate the gate area and the numbers written on top of them tells the side length of the squares in µm. After dicing, each die was ~ 2.5 mm x 2.5 mm size.

4.3.2. Effect of annealing on C-V characteristics:

The MOS capacitor with thin oxides (80 nm and 90 nm) were used to prepare the electrical characterization set-up. They were also utilized to check the effect of high temperature annealing and the quality of the interface obtained with such wet and dry oxides. The set-up is illustrated in Fig. 4.11, and several C-V characteristics obtained on different capacitors are presented in the subsequent figures.

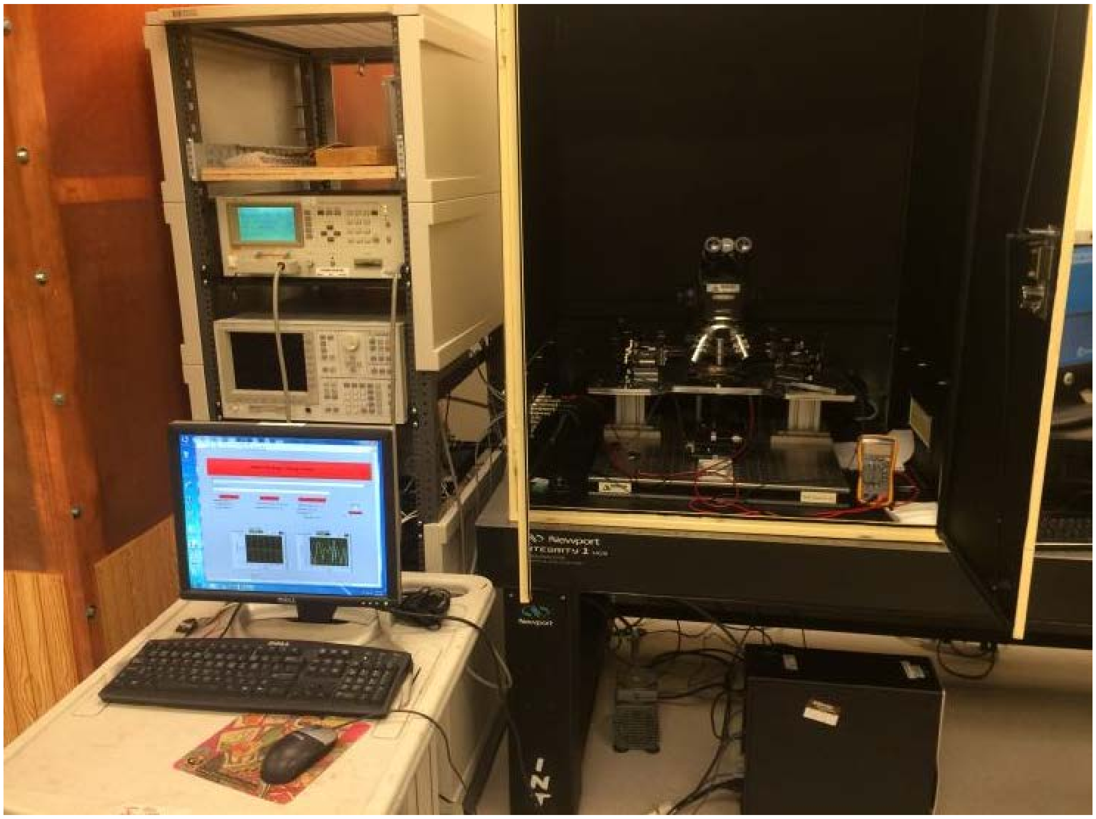


Fig. 4.11: Electrical set up with the probe station and the computer controlled LCR meter.

In Fig.4.12, the C-V characteristics obtained on 90 nm dry oxide devices are presented for freshly manufactured devices (black squares), relaxed devices (red squares) and for high temperature forming gas annealed parts (green squares). It is noticeable that the relaxed parts exhibit different $C_{\max}$ and $C_{\min}$ but are not shifted with respect to the freshly manufactured part. The annealed parts are shifted about 9 V with respect to the non-annealed parts, showing that trapped oxide charge was reduced by the annealing. The stretch out of the curves is also reduced after annealing indicating that the oxide interface charges are also reduced. Please note that the C-V shift can also be referred as shift in the device threshold voltage.

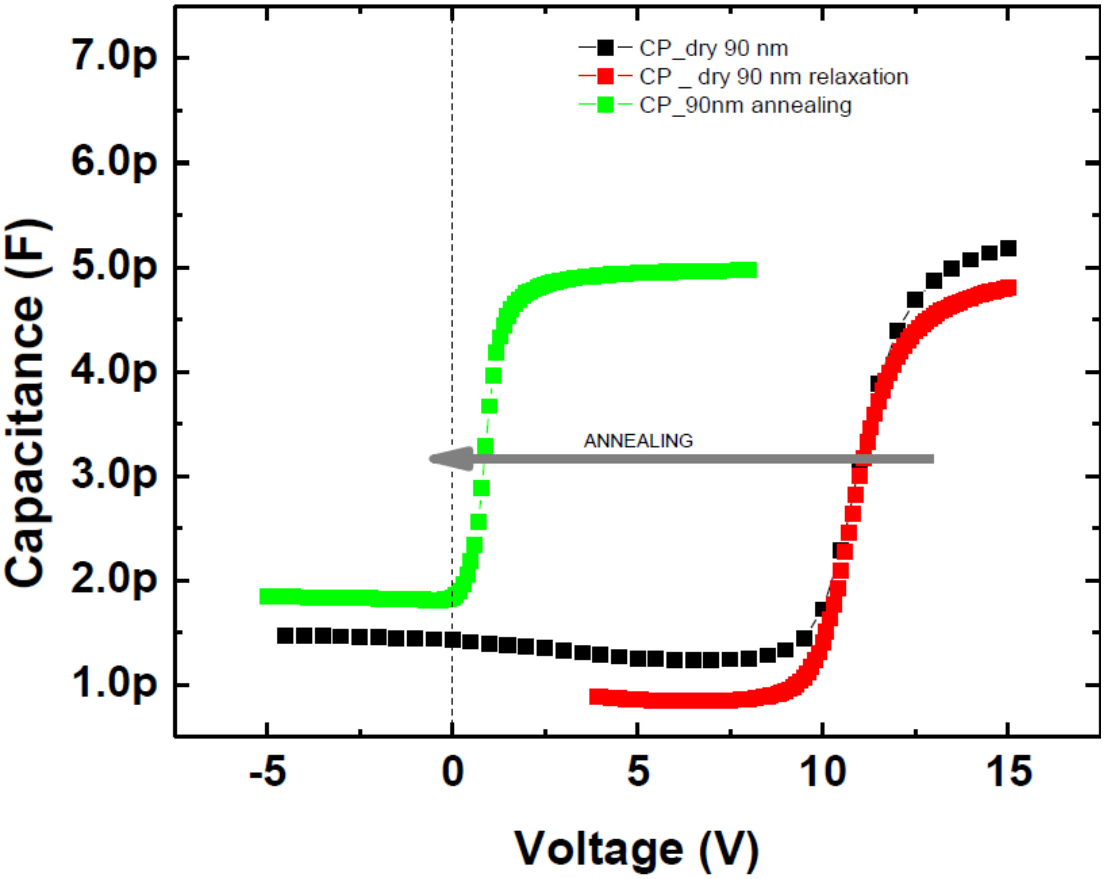


Fig. 4.12: C-V characteristics of (100 µm x 100 µm) MOS capacitors obtained on 90 nm dry SiO_2 devices. Capacitance is presented as a function of V_{SG} (substrate-gate potential). Black square represents freshly manufactured devices (testing was performed right after manufacturing), red squares represent relaxed devices (tested few days after manufacturing) and green squares indicates the annealed devices.

In Fig. 4.13, the C-V characteristics of 90 nm dry oxides that have been annealed at high temperature for different periods of time are presented. It can be seen that no matter what the duration of the high temperature forming gas anneal is, the final C-V characteristics are the same (different durations studied: 30 min, 60 min, 90 min and 120 min). As a consequence, for those samples a 30-minute annealing is enough to get the maximal shift on the C-V characteristics, i.e., to minimize most of the oxide trapped

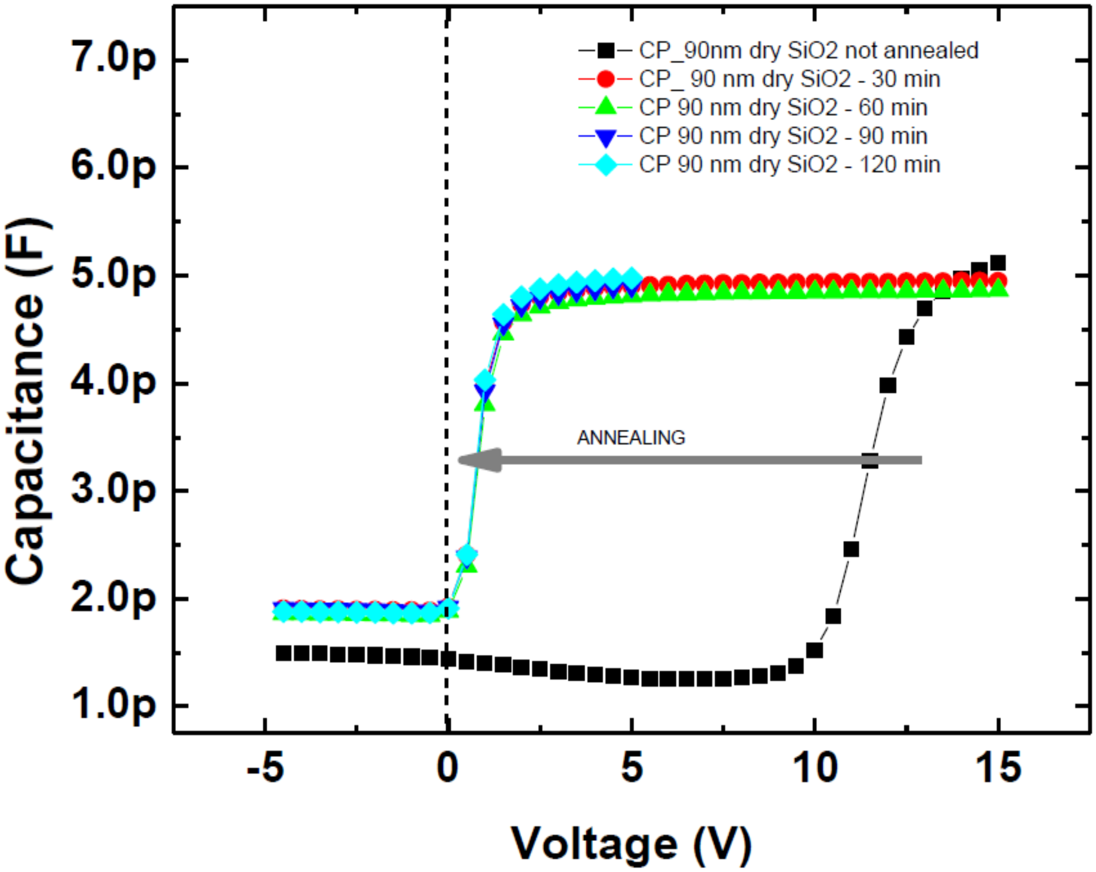


Fig. 4.13: C-V characteristics of (100 µm x 100 µm) MOS capacitors obtained on 90 nm dry SiO_2 devices. Capacitance is presented as a function of V_{SG} (substrate-gate potential) for different annealing times. Black square represents the C-V characteristic of a non-annealed part. The rest of the C-Vs were obtained from annealed devices. No effect of different annealing time on the C-V characteristics was observed.

charge in the oxide. Higher temperatures could be used but the use of aluminum prevents the use of temperatures higher than 450 °C due to aluminum spiking.

In Fig. 4.14, C-V characteristics obtained on wet oxides are presented. The thickness of the oxide is 80 nm, and the gates are made of aluminum. Similar to what was observed on the dry oxide parts, the freshly manufactured devices with wet oxide displays a high negative threshold voltage (please note, the X-axis represents substrate to gate voltage).

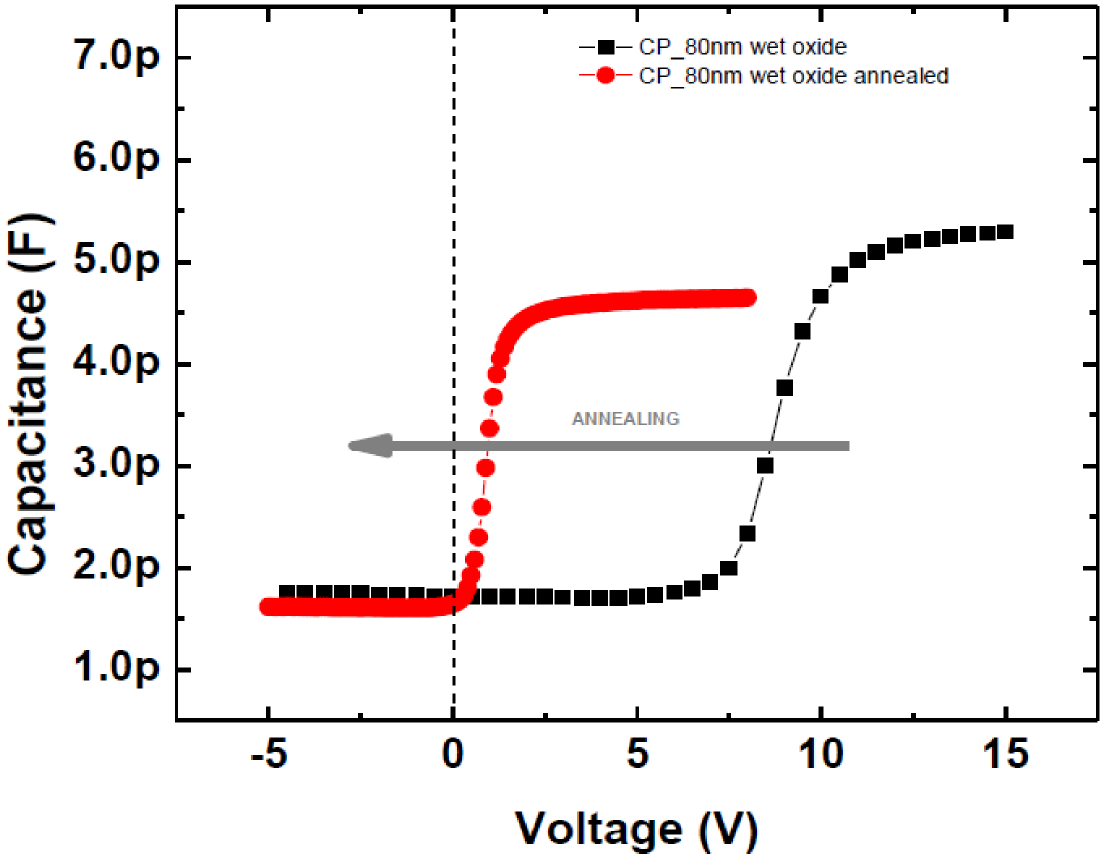


Fig. 4.14: C-V characteristics of (100 µm x100 µm) MOS capacitors obtained on 80 nm wet SiO_2 devices. Capacitance is presented as a function of V_{SG} (substrate-gate potential). Similar to MOS capacitors with dry oxide, these devices also displayed a significant shift in C-V or threshold voltage after performing the annealing.

But once they are annealed, there will be a significant positive threshold voltage shift as the oxide trapped charges get released due to annealing. Once again, a difference between the maximum and minimal capacitance values before and after annealing was observed.

In Fig. 4.15, the C-V characteristics of annealed wet and dry oxides are presented. It can be observed that the capacitance values of the thinner oxide (red squares) are actually lower than the capacitance obtained on devices with the thicker oxide (black squares), which may indicate a limitation in the optical measurement (e.g., film thickness

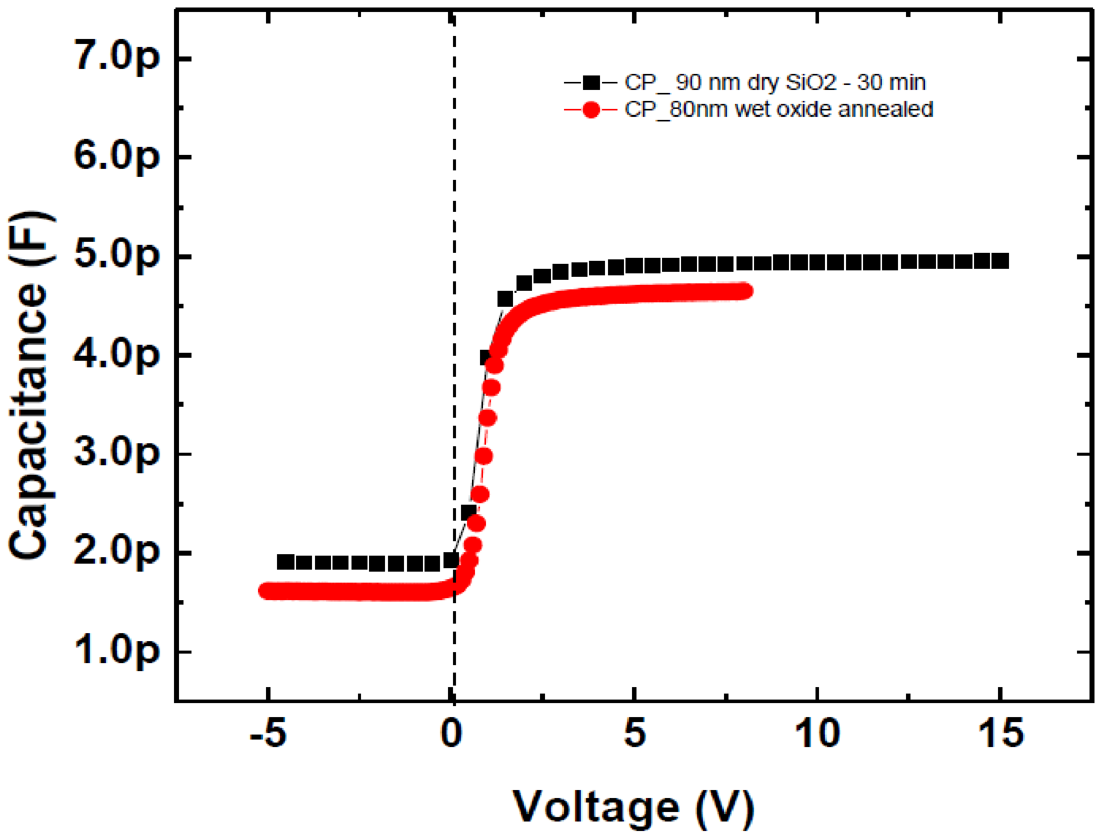


Fig. 4.15: C-V characteristics of (100 µm x100 µm) MOS capacitors obtained from devices with 90 nm dry SiO_2 and 80 nm wet SiO_2. Capacitance is presented as a function of V_{SG} (substrate-gate potential). Black squares show the devices with thicker oxide and red squares present the device with thinner oxide. It can be observed that (unexpectedly) the capacitance values of the thinner oxide are actually lower than the capacitance obtained on devices with the thicker oxide. This may indicate a limitation in the optical measurement systems (e.g., film thickness measurement tools) currently available at ASU's clean room for measuring oxide thicknesses below a certain range. It is also possible that there was a variation of the oxide thickness due to annealing.

measurement tools) at ASU's clean room for measuring thin oxides, or that there was a possible variation of the oxide thickness after annealing.

In addition to the above-mentioned observations, attention was given on another very important device parameter: the capacitance value that can be obtained at 0 Volts (i.e., the DC capacitance). Test results show that, all the MOS capacitors tested thus far, are giving DC capacitance values which is already equal to their $C_{\min}$. This means that if these capacitors are used to load the patch antenna, they would already be at the value for which the sensor would be saturated (because ionizing radiation causes a negative threshold voltage shift regardless of the substrate type in a MOS device up to certain limit of total dose exposure [100]-[102]) Thus, different manufacturing options were explored to obtain a DC capacitance value higher than the $C_{\min}$.

(i) One potential solution was to use a thicker oxide (due to stretching out of the C-V curve), as observed in the past (Fig. 4.4).

(ii) Another solution would be to use a metal gate with a different work-function. As a first order approximation, the flat-band voltage of a MOS capacitor primarily depends on the work function difference between the metal gate and the semiconductor. The work function of a metal is constant (i.e., a material property). However, the semiconductor work function can be varied by changing the doping concentration. Thus, by manipulating the MOS capacitor design with different metal gates or by using substrates with different resistivities, the C-V curve position (i.e., V_{FB}, V_{th}) and shifting can be enhanced.

4.3.3. Effect of SiO_2 stack thickness on C-V characteristics:

As mentioned earlier, different variations of MOS capacitors have been manufactured and electrically characterized. The devices manufactured include:

- 90 nm grown dry oxide + 400 nm deposited oxide with aluminum gates

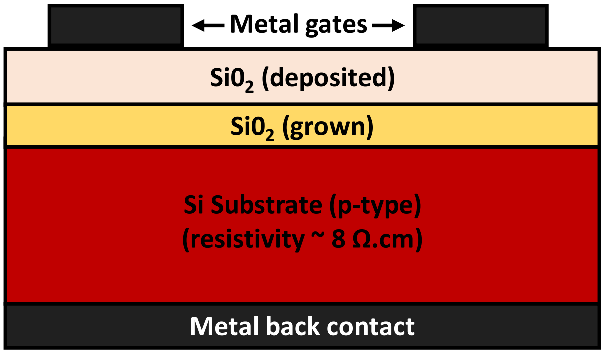


Fig. 4.16: MOS capacitors with grown and deposited oxide layers.

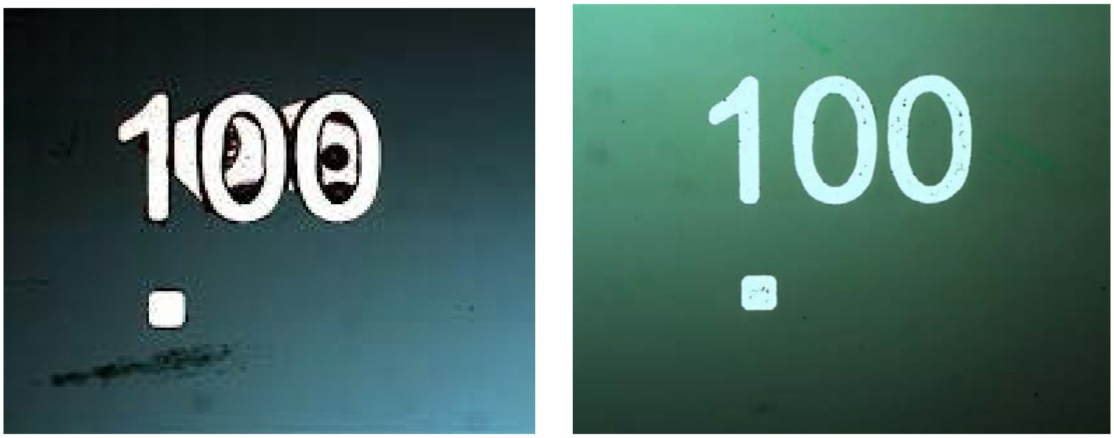


Fig. 4.17: Top view microphotographs of manufactured (100 µm x 100 µm) MOS capacitors on a ~500 µm thick p-type silicon substrate with ~ 8 Ω.cm resistivity: (left) MOS capacitor with 200 nm aluminum gate, 500 nm thermally grown wet SiO_2 (using Tystar Mini-Tytan 4600 furnace) and (right) MOS capacitor with 200 nm aluminum gate, 90 nm thermally grown dry SiO_2 (using Tystar Mini-Tytan 4600 furnace) + 400

- 80 nm grown wet oxide + 400 nm deposited oxide with aluminum gates
- 500 nm wet oxide with aluminum gate

A modified schematic representation of the two oxide layer devices is provided in Fig. 4.16 and microphotographs of the manufactured devices are provided in Fig. 4.17 below. C-V characteristics on these different batches of devices were obtained using the computer controlled test set-up at ASU, for devices as manufactured, and on devices annealed in a forming gas ambient. The results obtained on different devices are presented in the following figures.

4.3.3.1. 90 nm grown dry oxide + 400 nm deposited oxide with aluminum gates

In Fig. 4.18, the C-V characteristics obtained on a MOS capacitor with two layers dielectric made of 90 nm dry grown SiO_2 and 400 nm deposited SiO_2 are presented for three different gate areas (i.e., 100 µm, 200 µm and 240 µm side square). If scaling effectively occurs, the values of capacitance obtained are not the ones expected from

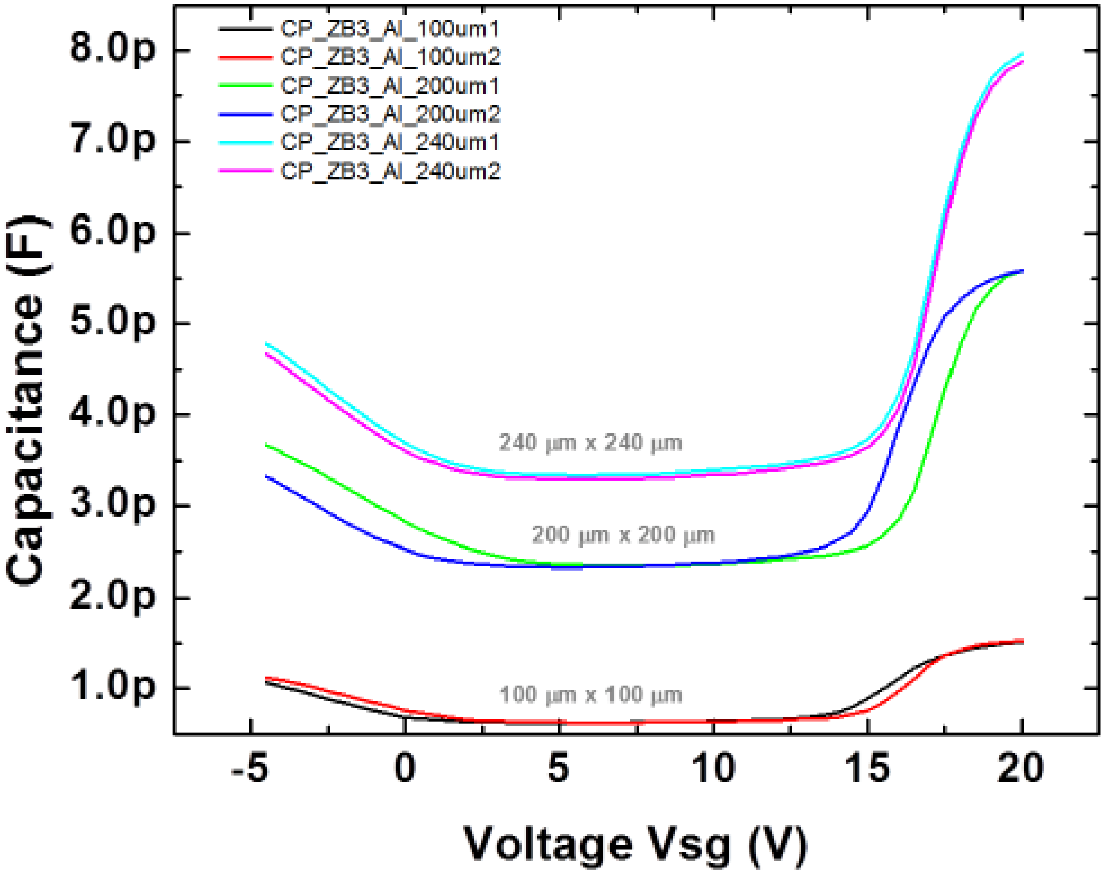


Fig. 4.18: C-V characteristics of 100 µm, 200 µm and 240 µm square side aluminum gate MOS capacitors with 90 nm dry grown SiO_2 and 400 nm physically vapor deposited SiO_2, as manufactured.

theoretical values using the simple calculation of oxide capacitance with a dielectric constant of 3.9. This is shown in Table 4.1, where the values of capacitance obtained after manufacturing and after annealing are compared to the values obtained theoretically for 90 nm dry oxide + 400 nm deposited oxide.

In Fig. 4.19, the C-V characteristics of devices are compared before and after standard forming gas annealing conducted for 30 minutes. As can be noticed, the capacitance values of annealed devices are lower than that of as-manufactured devices and are actually much closer to the theoretical values. In Table 4.1, the values of capacitance obtained on non-annealed and annealed parts are compared to the theoretical values. The results evidently show that the annealing step enables the shifting of C-V curve towards lower V_{SG} (substrate to gate potential, X-axis of the C-V plots) and capacitance values closer to the theoretical values. It can also be observed that the C-V characteristics are not ideal, with variation in slope in the transition from C_{max} to C_{min}, that could be due to a very poor Si/SiO$_2$ interface, or due to the bi-layer structure of the samples.

TABLE 4.1

MOS CAPACITANCE VALUES WITH DUAL LAYER (DRY + PHYSICAL VAPOR DEPOSITED) OXIDE

	As manufactured	After annealing	Theoretical
C_{max} (pF)	1.51447	$7.69849\ 10^{-1}$	$7.19\ 10^{-1}$
C_{min} (pF)	$0.974\ 10^{-12}$	$5.62922\ 10^{-1}$	$5.14\ 10^{-1}$

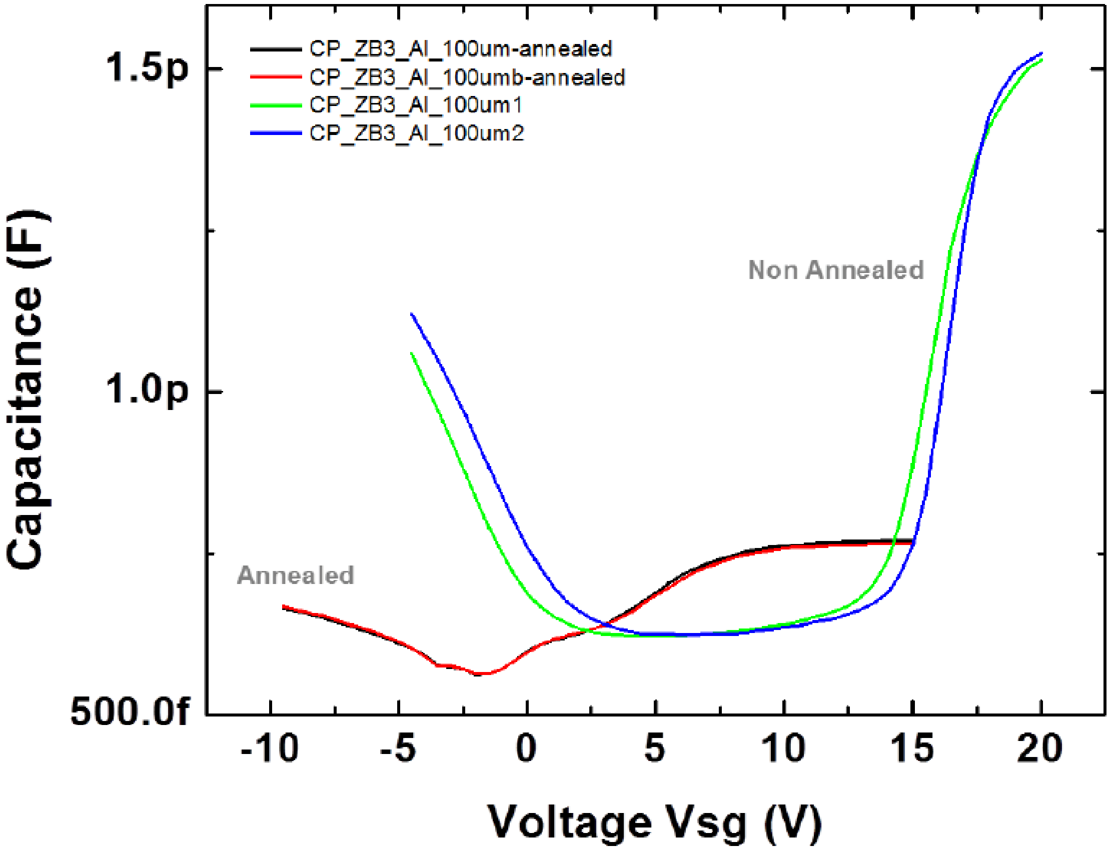


Fig. 4.19: Comparison of the C-V characteristics of 100 µm square side aluminum gate MOS capacitor with 90 nm dry grown SiO_2 and 400 nm deposited SiO_2 as manufactured and after standard forming gas annealing. As can be observed, the capacitance values of annealed devices are lower than that of as-manufactured devices and are actually much closer to the theoretical values. Also, a shift of the C-V was recorded due to annealing. The C-V characteristics do not look similar to the ideal cases probably due to a poor Si/SiO_2 interface or because of a bi-layer oxide structure with physically deposited oxide.

4.3.3.2. 80 nm grown wet oxide + 400 nm deposited oxide with aluminum gates

Similar to what has been done with the 90 nm grown dry oxide parts with 400 nm deposited SiO_2 on top, parts with 80 nm grown wet oxide with 400 nm deposited SiO_2 have also been manufactured and characterized. C-V characteristics and results obtained on such devices are presented in Fig. 4.20. As can be observed, the results obtained are similar to the ones found on the devices with a 90 nm grown dry oxide. Scaling occurs normally on those parts with increased area, and decrease of capacitance values occurs towards the ideal values after forming gas annealing is performed. Changes of slope in the C-V are observed and the capacitance at 0 V is close to C_{min}, but it is still a little bit higher. The annealing also enables a shift of the C-V characteristic towards lower V_{SG} levels.

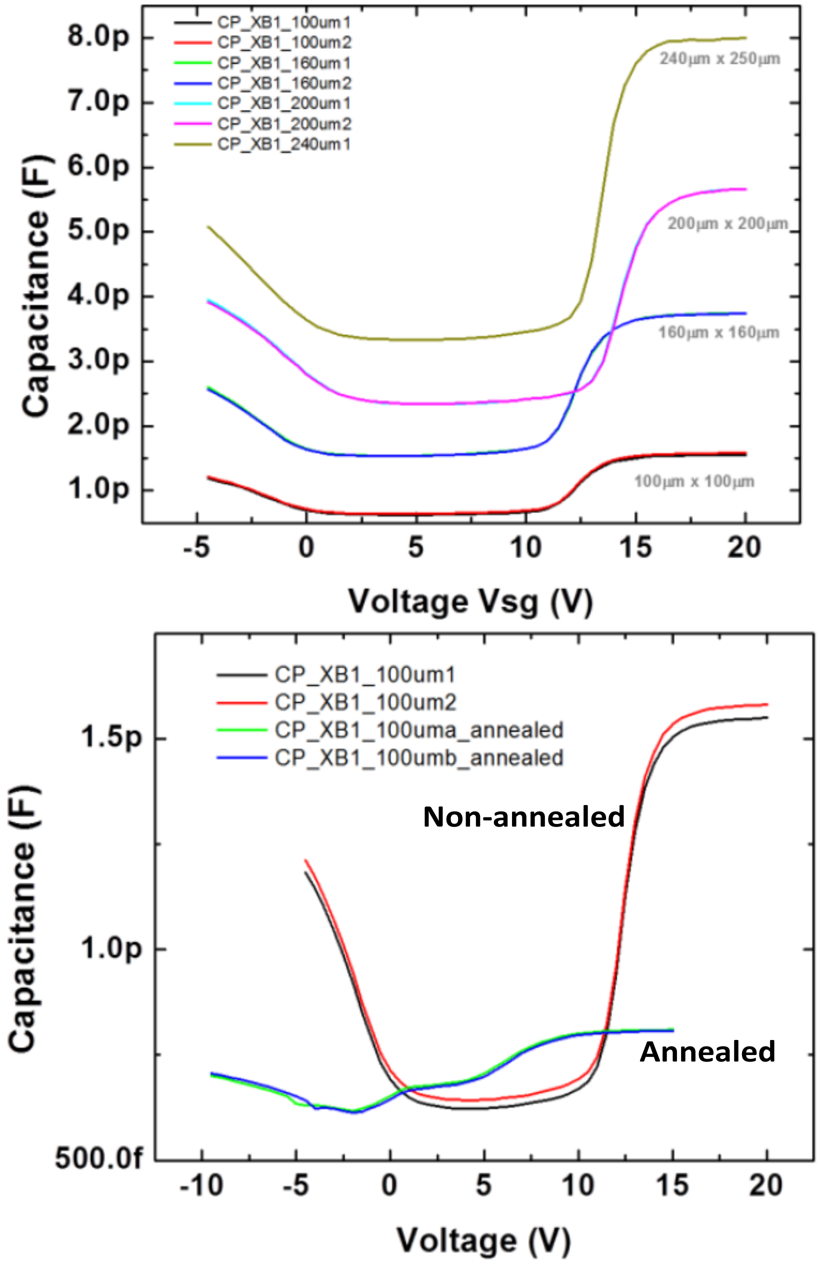


Fig. 4.20: Comparison of the C-V characteristics of 100 µm x 100 µm aluminum gate MOS capacitors with 80 nm wet grown SiO_2 and 400 nm deposited SiO_2: (top) As manufactured (i.e., non-annealed) MOS capacitors with increasing areas; (bottom) Comparison of the C-V of (100 µm x 100µm) MOS capacitors - annealed and non-annealed. Like Fig. 4.19, the capacitance values of annealed devices are lower than that of as-manufactured devices. Also, a shift of the C-V was observed due to annealing. The C-V characteristics do not look similar to the ideal cases probably due to a poor Si/SiO_2 interface or because of a bi-layer oxide structure with physically

4.3.3.3. C-V characteristics of MOS capacitors with 500 nm grown wet oxide:

The C-V characteristics obtained on 500 nm grown wet SiO_2 MOS capacitors with aluminum gate are presented in Fig. 4.21. Fig. 4.21(top) shows non-annealed devices C-V and annealed device C-Vs are given in Fig. 4.21 (bottom). These (100 µm x100 µm) devices with 500 nm wet SiO_2 have their capacitance in the range of 0.5 pF which is the range of capacitive load intended to load to the patch antenna to have a response in the 3 to 8 GHz frequency band. As previously observed, the aluminum gate does not allow us to obtain a capacitance at V_{SG} = 0 V close to C_{max} which is desired in order to detect the radiation induced C-V shift using a RF interrogator. Thus, the next step was to investigate this by changing the gate metal since the work function difference between the metal and semiconductor primarily establishes the flat-band voltage.

4.3.4. Effect of gate metal on MOS capacitor C-V characteristics:

4.3.4.1. Tungsten and nickel gates:

Using the same device structure showed in Fig. 4.16 earlier, additional MOS capacitors with 90 nm grown dry SiO_2 and 400 nm physical vapor deposited SiO_2 were manufactured with different metal gates: (a) tungsten and (b) nickel. The C-V characteristic of as manufactured devices are presented in Fig. 4.22, and compared in Fig. 4.23. For tungsten gate MOS capacitors, C-V characteristic plots of six devices with three different gate areas (i.e., 100 µm, 200 µm and 240 µm sides) were tested (Fig. 4.22-top). For nickel gate MOS capacitors, C-V characteristic plots of three devices with three different gate areas (i.e., 100 µm, 120 µm and 150 µm sides) were tested (Fig. 4.22-bottom).

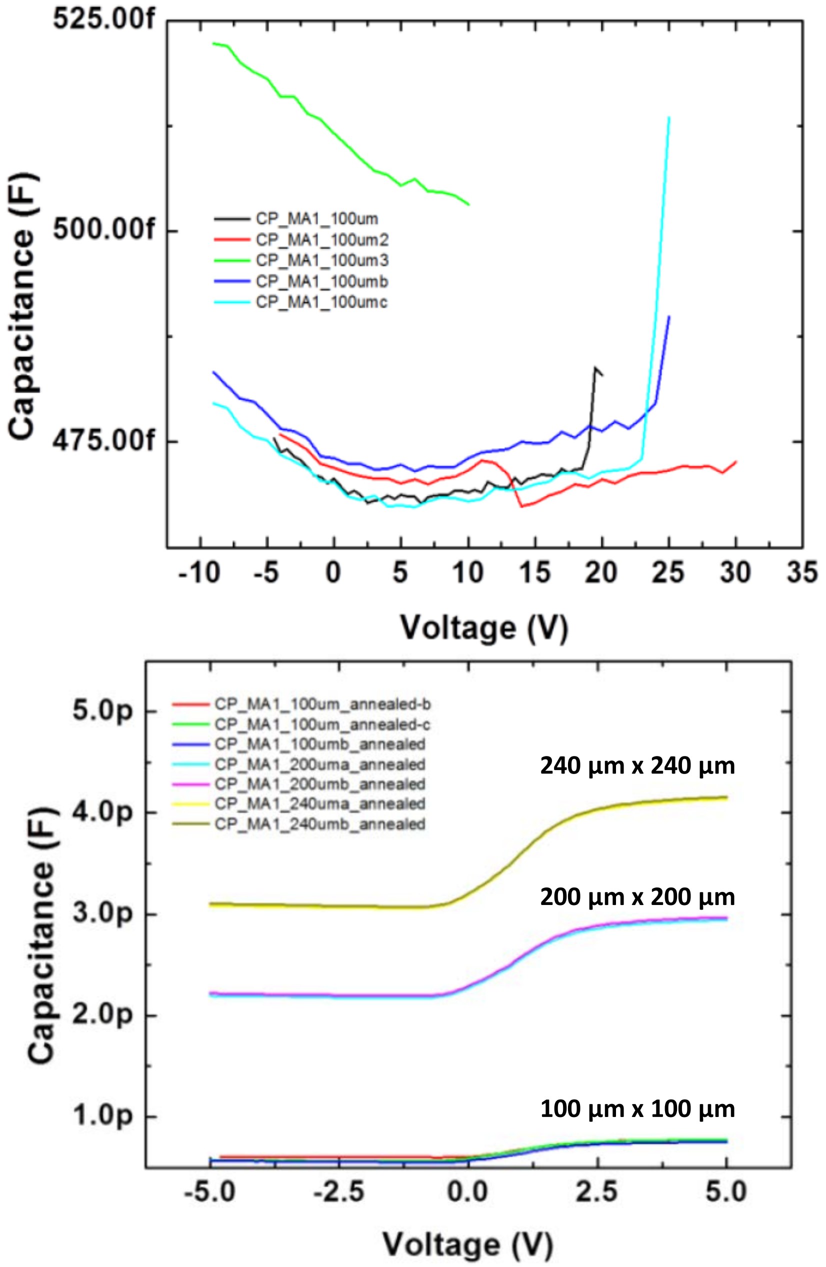


Fig. 4.21: C-V characteristics of 500 nm grown wet SiO_2. (top) MOS capacitors as manufactured (i.e., non-annealed); (bottom) MOS capacitors after annealing with three different gate areas. C_{max} of (100 µm x100 µm) devices are around 0.5 pF range which is the target value intended to load the patch antenna to get a response within 5 to 6 GHz frequency band. However, due to aluminum work function, the DC capacitance value is still not around the targeted C_{max} value which is necessary to detect the C-V shift through RF interrogation.

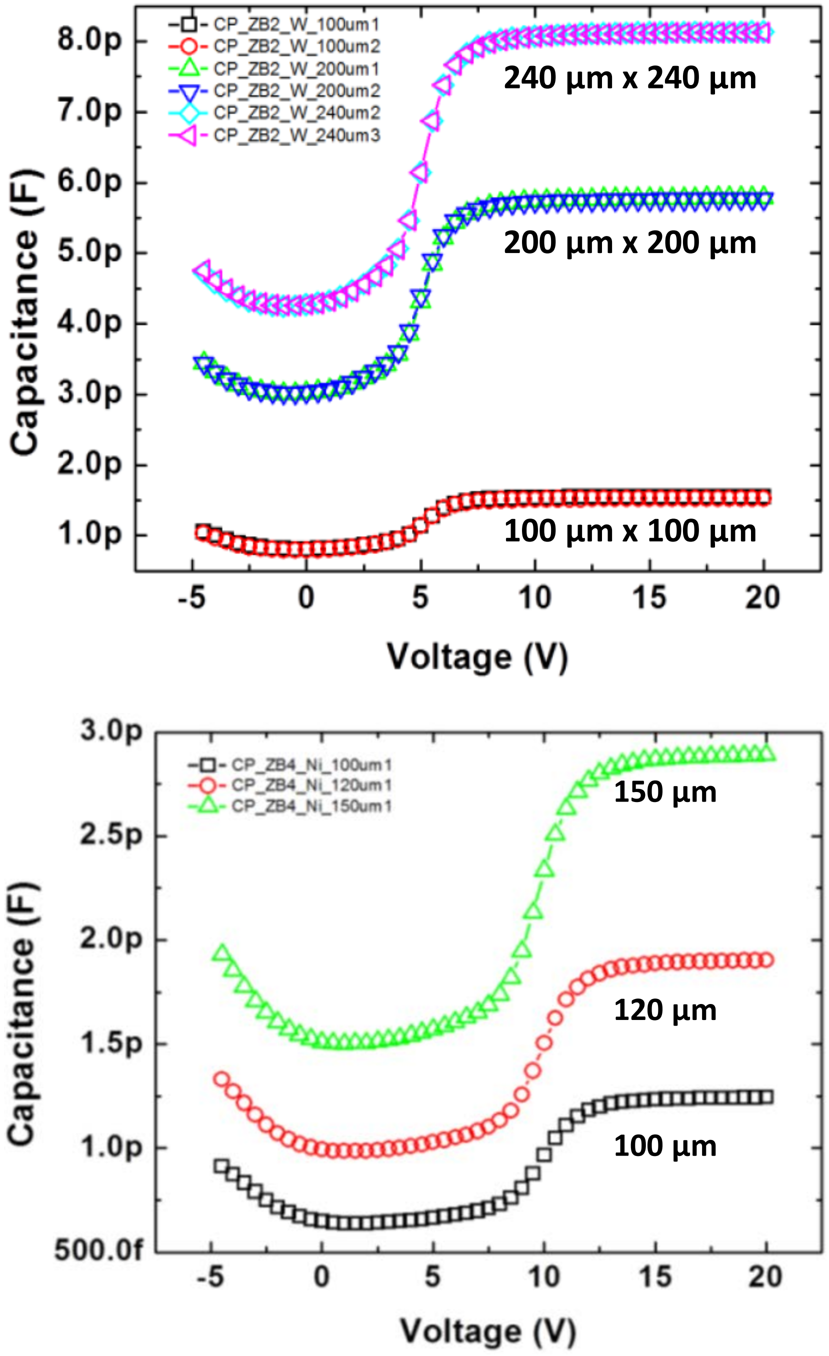


Fig. 4.22: C-V characteristics of square side MOS capacitor with 90 nm dry grown SiO_2 and 400 nm physical vapor deposited SiO_2 as-manufactured (i.e., before annealing): (top) with tungsten gate and three different areas; (bottom) with nickel gate and three different areas.

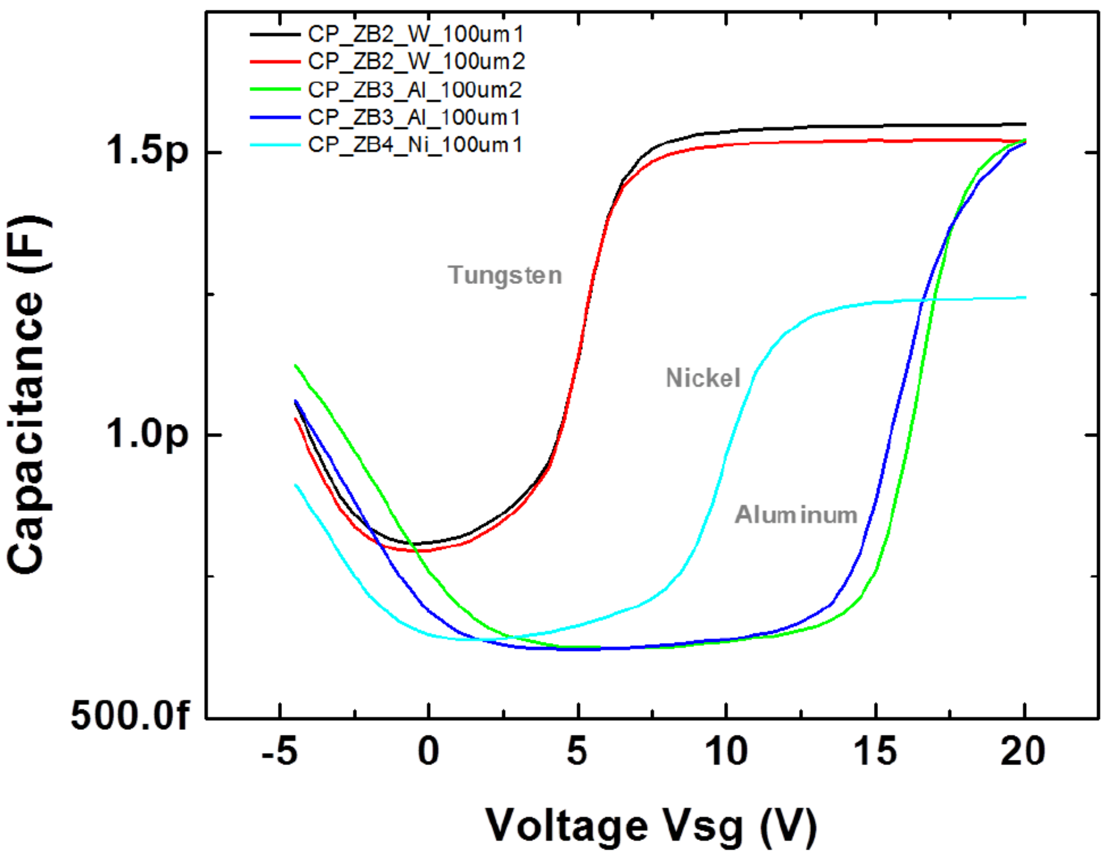


Fig. 4.23: Comparison of the C-V characteristics of 100 µm square side aluminum, tungsten and nickel gate MOS capacitor with 90 nm dry grown SiO_2 and 400 nm deposited SiO_2, as manufactured (i.e., before annealing). A shift in the C-V is observed due to the difference in work function of the metals. An unexpected smaller C_{max} was observed for the nickel gate MOS capacitors which might be due to process related variation during oxide deposition.

For these MOS capacitors, the results presented are without any annealing conducted on the devices. It can be observed that scaling occurs with areas for both parts. In Fig. 4.23, these C-V characteristics are compared to the ones obtained on similar devices with aluminum gate (i.e., without annealing). A shift in the C-V characteristics can be seen, which is due to the difference in work function of these metals. However, an unexpected smaller C_{max} was noticed for the Ni gate MOS capacitors. Since the oxide thickness was constant, C_{max} of all these MOS capacitors should have been very close to each other as they are determined solely by the oxide capacitance. Though there might be several explanations, but a process related variation (e.g., unwanted oxide thickness non-uniformity during the physical vapor deposition process) might be the most likely reason for this behavior. The C-V were obtained on MOS capacitors non-annealed, so the C-V characteristics of annealed parts should exhibit lower capacitance values for both C_{max} and C_{min}, as well as C-V shifted to lower V_{SG}, as it was shown in Fig. 4.20b. Annealing was conducted on the tungsten and the nickel parts, but unfortunately, this thermal treatment had a very significant (and unintended) effect of the top metal gates (i.e., the metal gate integrity was compromised leading to bubbling and flaking). This effect did not allow probing of the devices, nor did it allow them to be wire bonded. This is illustrated in Fig.4.24.

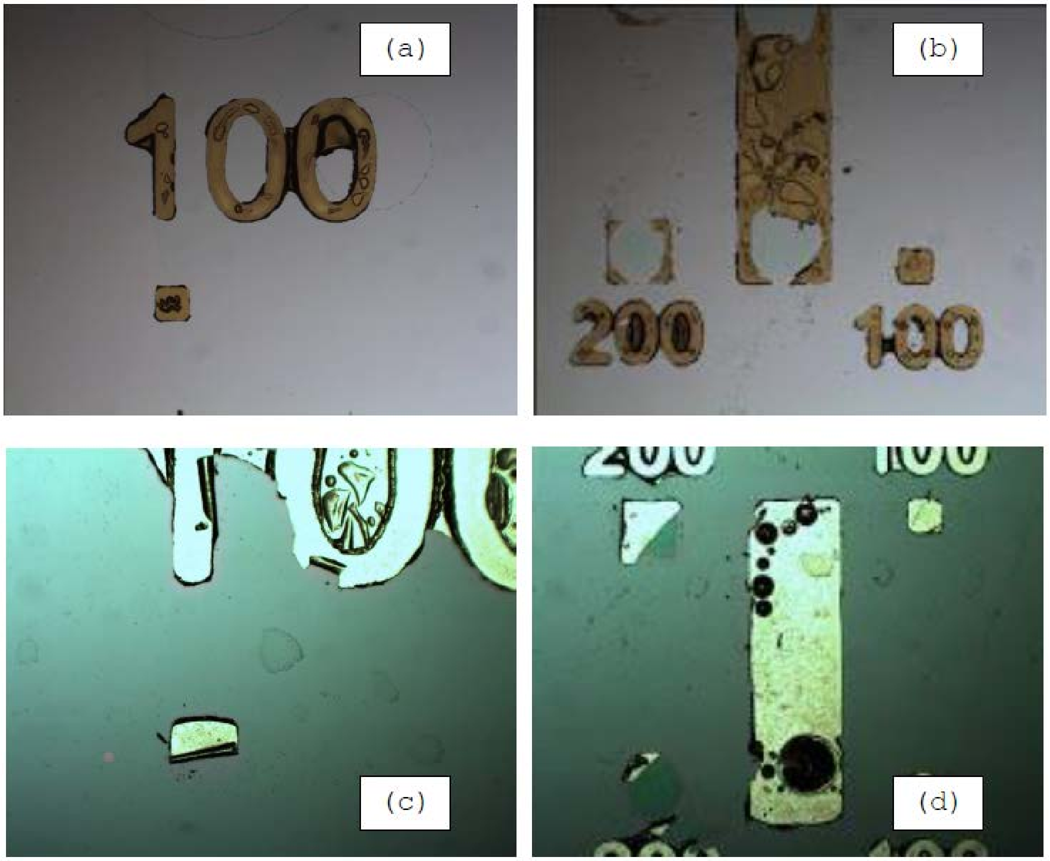


Fig. 4.24: Tungsten MOS capacitors (a, b) and Nickel MOS capacitors (c, d) after annealing.

4.3.4.2. Chromium, chromium/gold, titanium, and titanium/tungsten gates:

For investigating (a) chromium, (b) chromium/ gold, (c) titanium and (d) titanium/ tungsten gate MOS capacitors, the following devices were manufactured and electrically characterized:

- 500 nm wet oxide with 62 nm thick chromium gate (sample ID: MA2)
- 500 nm wet oxide with 100 nm titanium gate (sample ID: MB3)
- 500 nm wet oxide with 5 nm chromium + 76 nm gold gate (sample ID: MA3, MC1).
- 500 nm wet oxide with 20 nm titanium + 100 nm tungsten gate (sample ID: MA4, MC2)
- 2000 nm wet oxide with 25 nm chromium + 300 nm gold gate (sample ID: NA1)
- 2000 nm wet oxide with 200 nm aluminum gate (sample ID: NA2)

An illustration of the cross-section of those devices along with microphotographs of the manufactured samples is provided in Fig. 4.25 to Fig. 4.30. Fig. 4.31 presents the post annealed C-V characteristics of 100 µm x 100 µm devices with chromium, chromium + gold, titanium, and titanium + tungsten metal gates. Similar to Fig. 4.23, shift in C-V characteristics was observed due to variation in metal work function. However, same threshold and flat-band voltages was recorded for (i) chromium and chromium + gold and (ii) titanium, and titanium + tungsten metal gate devices. This indicates that the work function of the metal layer that forms the interface with the dielectric or SiO_2, plays the dominant role to establish the flat band and threshold voltages and metal layers stacked on top of them have minimal influence in this regard.

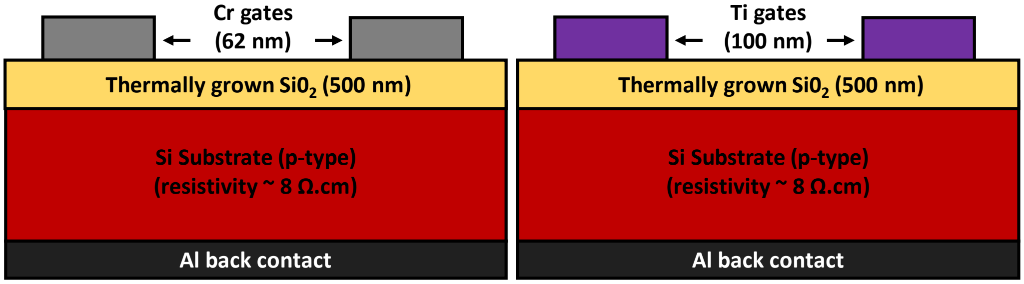
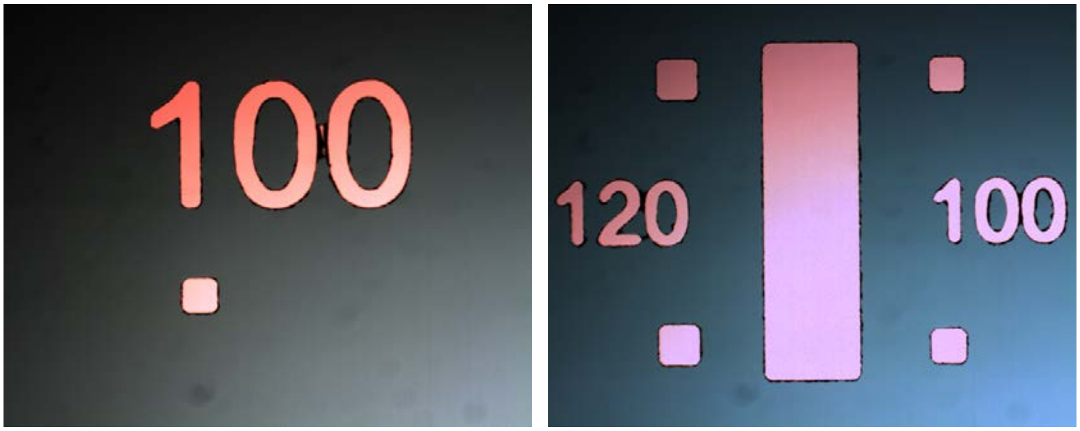
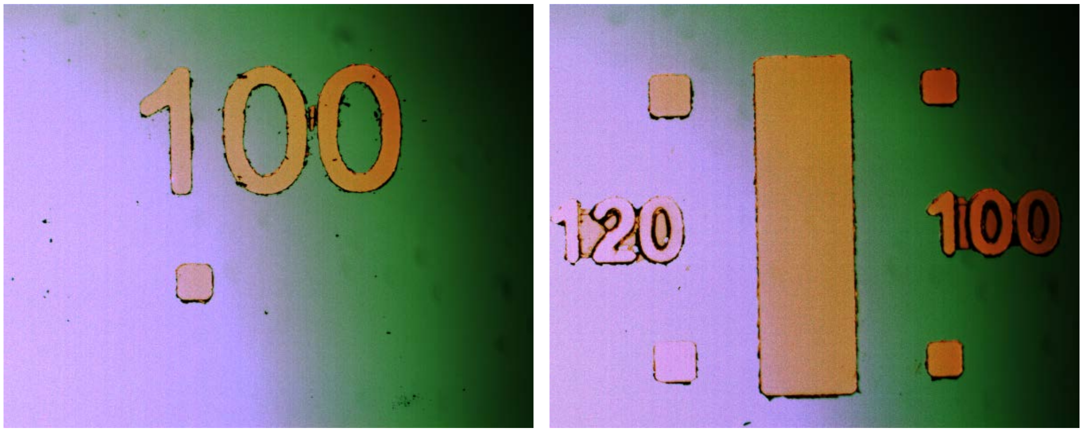


Fig. 4.25: (left) MOS capacitors with 62 nm thick chromium gates formed on 500 nm thick thermally grown wet oxide [MA1] and (right) MOS capacitors with 100 nm thick titanium gates formed on 500 nm thick thermally grown wet oxide [MB3].



(a)



(b)

Fig. 4.26: Different microphotographs of manufactured MA1 chromium gate MOS capacitors: (a) devices before 450 °C annealing; (b) devices after 450 °C annealing.

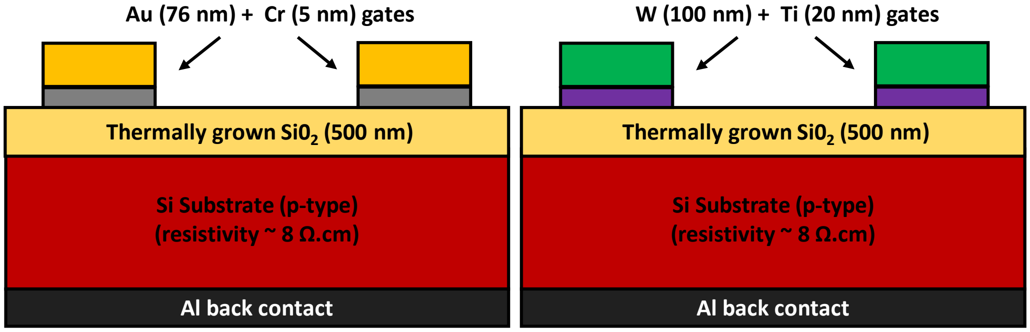
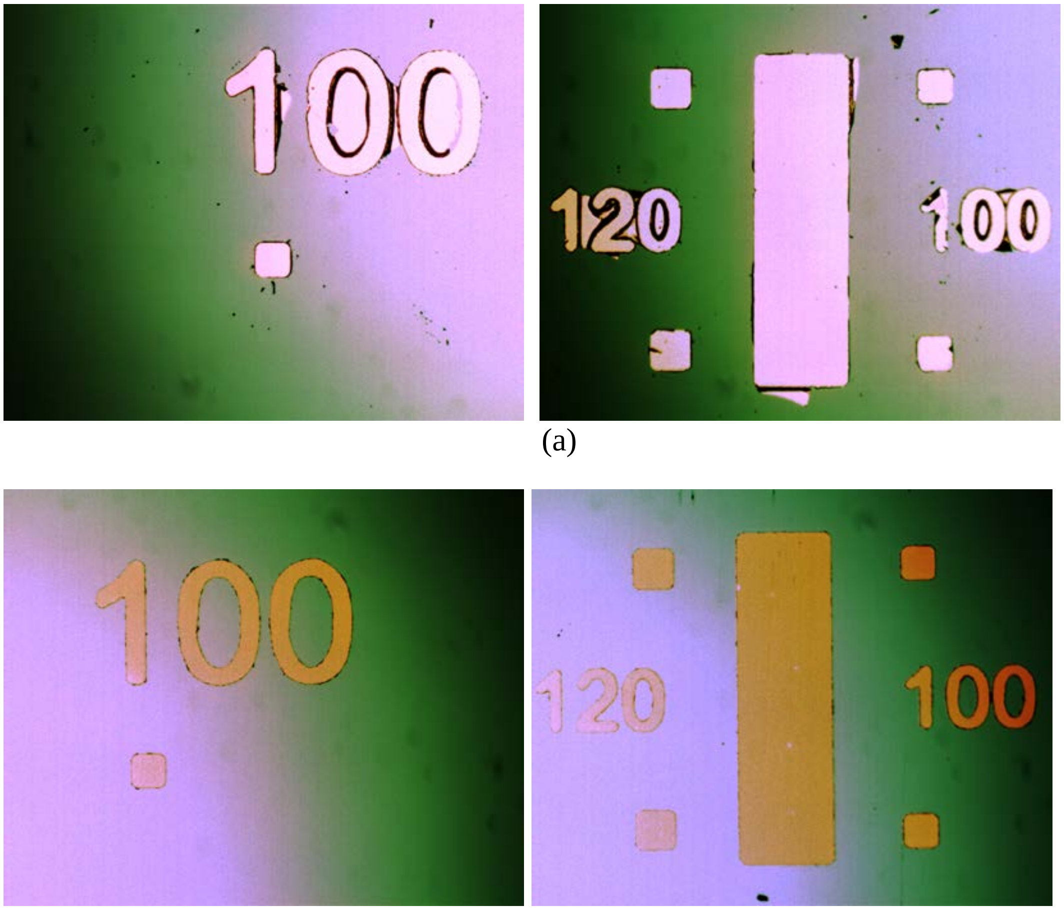


Fig. 4.27: (left) MOS capacitors with 5 nm chromium + 76 nm gold gates [MA3, MC1]; (right) with 20 nm titanium + 100 nm tungsten gates [MA4, MC2]



(a)

(b)

Fig. 4.28: Images of post 450°C annealed MOS capacitors: (a) chromium + gold gate devices [MA3, MC1]; (b) titanium + tungsten devices [MA4, MC2]

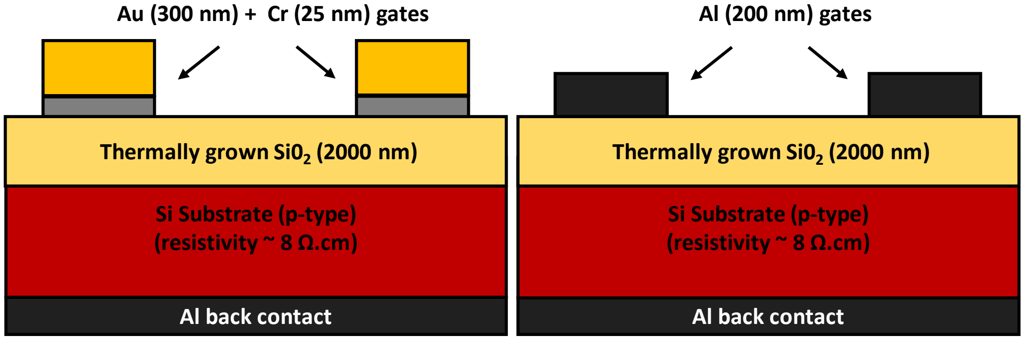
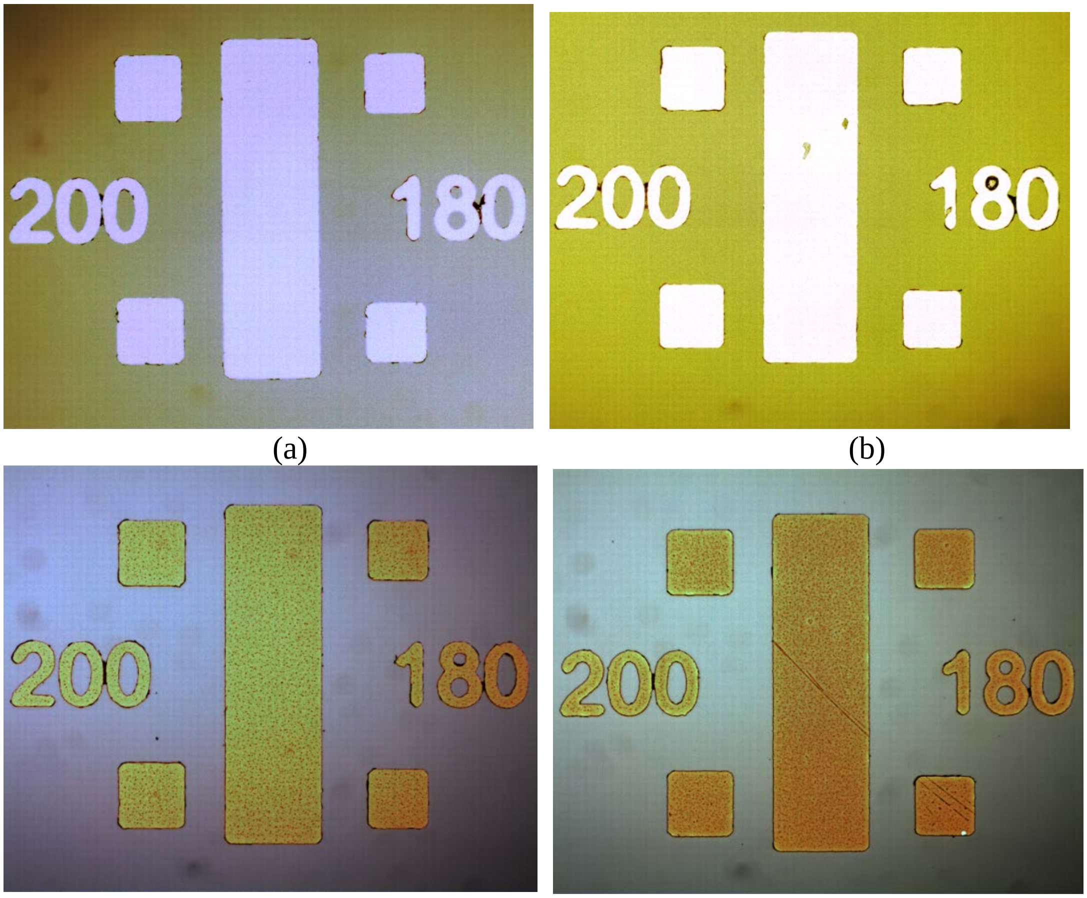


Fig. 4.29: (left) MOS capacitors with 2 μm thick thermally grown oxide: (a) 25 nm chromium + 300 nm thick gold gates [NA1]; (right) 200 nm aluminum gates [NA2]



(a) (b)

(c) (d)

Fig. 4.30: Microphotograph of NA1 devices after different anneal temperatures: (a) Non-annealed or virgin devices; (b) after 450°C anneal; (c) after 600 °C anneal; and (d) after 750 °C anneal

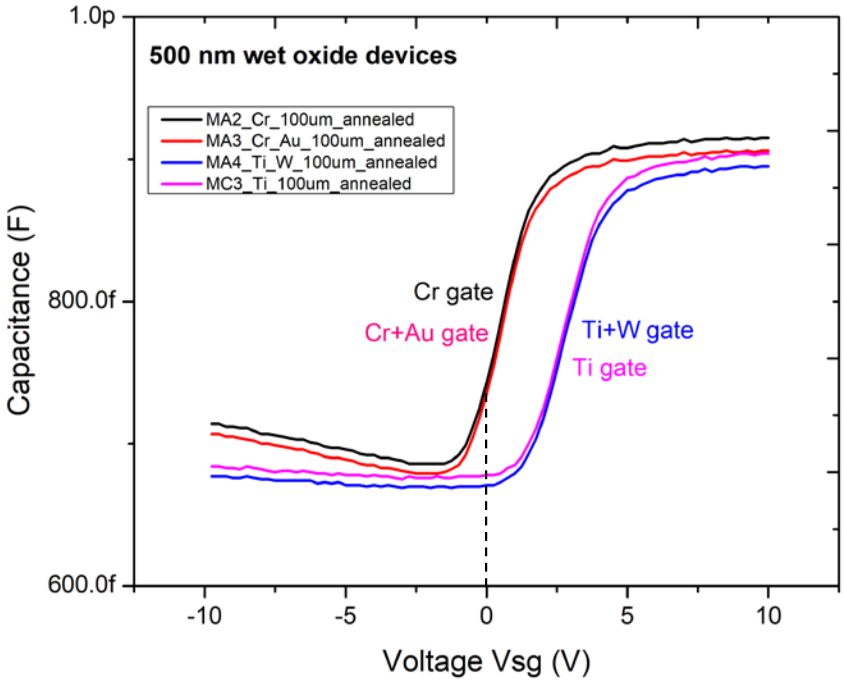


Fig. 4.31: Comparison between annealed (100 µm * 100 µm) devices with chromium, chromium + gold, titanium, and titanium + tungsten metal gates. Test results indicate that the work function of the metal layer that forms the interface with the dielectric or SiO_2, plays the dominant role to establish the flat band and threshold voltages and metal layers stacked on top of them have minimal influence in this regard.

4.3.5. Effect of pre-gate deposition anneal on the C-V curve:

The experimental results discussed so far has given the idea that annealing with forming gas plays critical role on the C-V response curves of the MOS capacitor devices. Normally, the annealing step is performed after completion of the manufacturing process. However, to further explore the effect of annealing, some devices were manufactured where the annealing was performed on the oxide before the gate metal deposition. After completion of the rest of the fabrication steps, they were tested to compare their C-V characteristics with non-annealed devices. The results (shown in Fig. 4.32) did not find any C-V characteristic differences between these two sets of devices indicating the that pre-metal gate deposition annealing step does not have significant impact on the device performance.

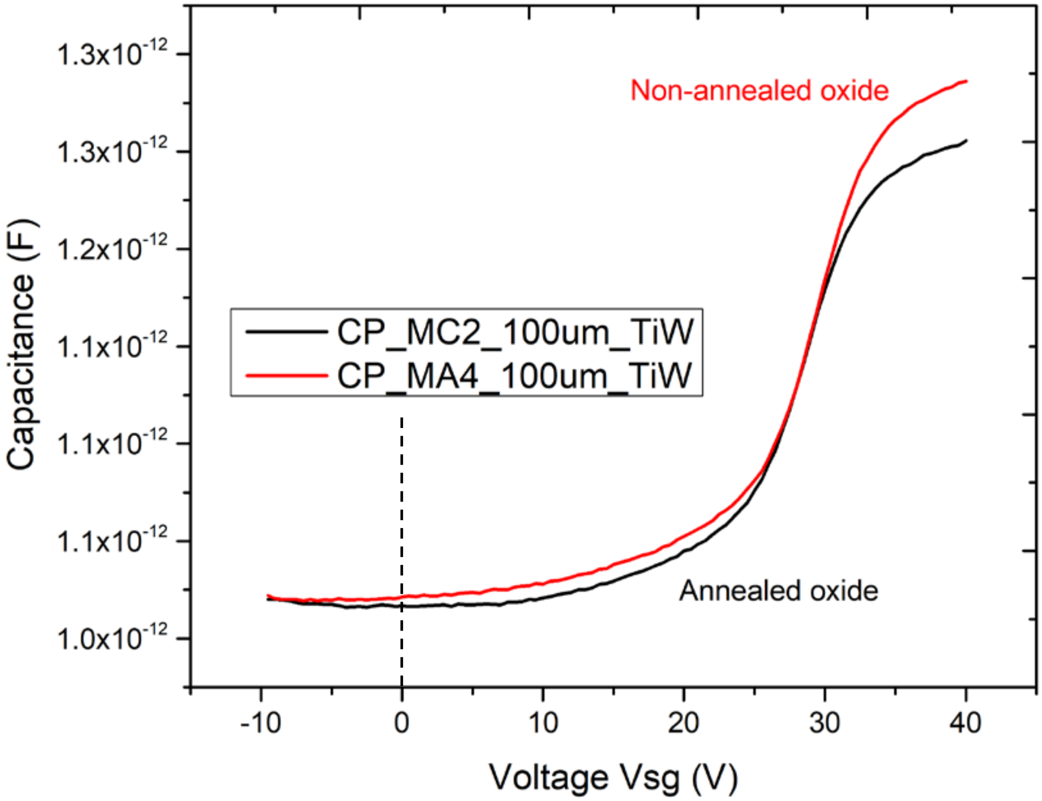


Fig. 4.32: Comparison between pre-gate annealed and pre-gate non-annealed oxide devices. No noticeable change in C-V characteristics was observed.

4.3.6. Effect of thermal deposition process on device scaling:

The photomask used to manufacture the MOS capacitors provided the option to test devices with different geometry from a single wafer. This was helpful to study the scaling effects without worrying about the batch to batch process variation. The test results show that the devices with 500 nm thermally grown wet oxide provides better scaling effect compared to the devices with 2000 nm thermally grown wet oxides. This happened due to the unusual thermal deposition process of the 2000 nm oxide. Normally, the thermal oxide growth step is performed in a single run. For this case, the furnace used for thermal growth was never tested before to grow oxide thicker than 500 nm. Due to lack of previous tool data, the entire thermal growth process could not be completed in a single run. Thus, the break of vacuum state during the growth process (to periodically check cumulative oxide thickness) might have introduced unwanted effects on the oxide quality. Fig. 4.33 shows the C-V characteristics of 500 nm oxide devices with different gate size. All of these 500 nm oxide devices showed scaling which is close to theoretical approximation. Fig. 4.34 shows the C-V characteristics of 2000 nm oxide devices with different gate sizes. None of them showed reasonable scaling effects and the obtained capacitance values are far off from the theoretical values. This indicates that break of vacuum during thermal growth process can introduce unwanted effect on the device performance.

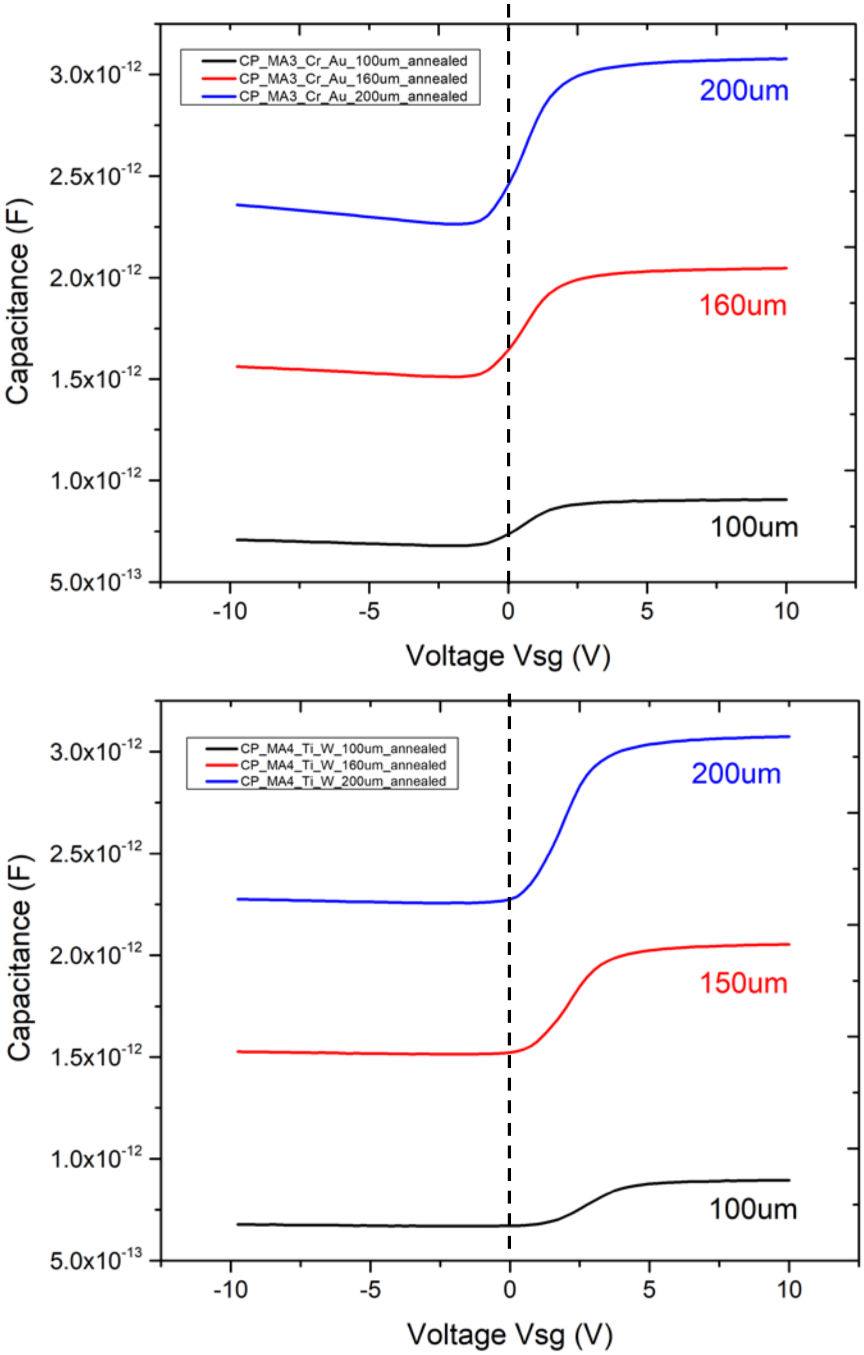


Fig. 4.33: Comparison between annealed devices with different gate sizes and 500 nm thick wet oxide. All of them showed scaling effects those are close to theoretical values. (top) 100 µm, 160 µm and 200 µm devices with chromium + gold gates [MA3] (bottom) 100 µm, 160 µm and 200 µm devices with titanium + tungsten gates [MA4]

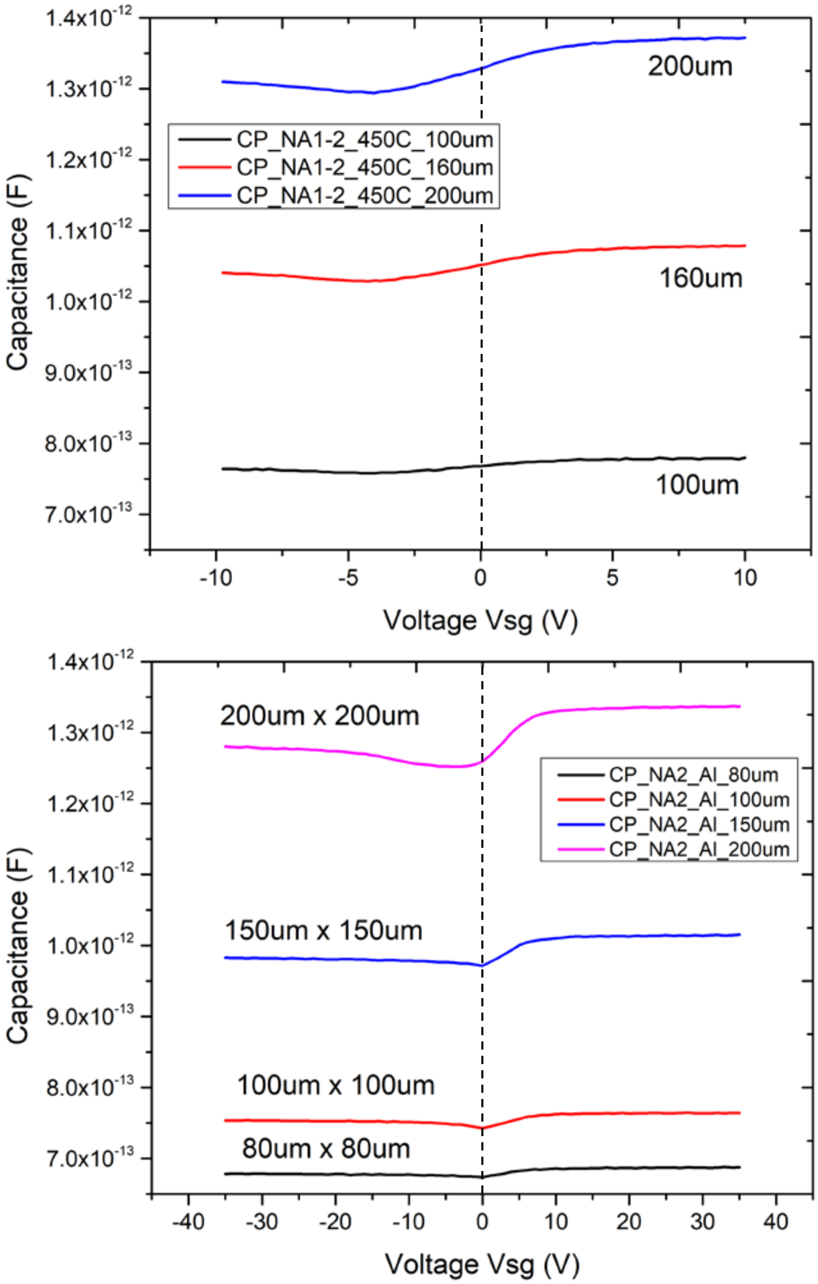


Fig. 4.34: Comparison among annealed devices with different gate sizes and 2000 nm thick thermally grown wet oxide. The oxide deposition was performed in multiple runs due to lack of previous tool data. These unwanted break of vacuum (to periodically check cumulative oxide thickness) possibly had an impact on the oxide quality. As a result, none of these devices showed scaling effects that are close to theoretical values. (top) 100 µm, 160 µm and 200 µm devices with thick chromium + gold gates [NA1] (bottom) 80 µm, 100 µm, 150 µm and 200 µm devices with aluminum gates [NA2].

4.3.7. Effects of higher anneal temperatures on the C-V characteristics:

For this experiment, some of the MOS capacitor devices with thick chromium + gold gates (25 nm Cr, 300 nm Au) were exposed to different anneal temperatures (450 °C for 30 mins, 600 °C for 30 mins, and 750 °C for 5 mins). Though both chromium and gold can withstand much higher temperatures, anneal temperature was not raised to more than 750 °C to ensure safe operation of the rapid thermal process (RTP) tool and, due to the aluminum back contact which has a melting point around ~660 °C. As expected, both 600 °C and 750 °C annealed samples showed some degree of melting of the back-side aluminum contact. However, this preliminary testing revealed that with an increase in anneal temperature, devices probably can shift their threshold voltage closer to 0 V and decrease their C_{max} as well (though further testing is required to check reproducibility). Fig. 4.35 shows the C-V characteristics of 100 µm x 100 µm devices with different anneal temperature.

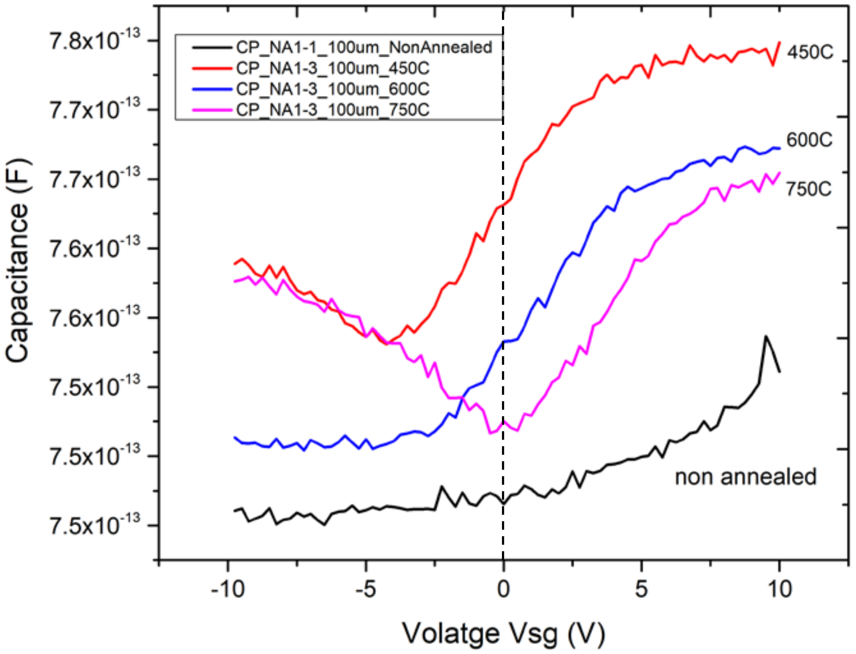


Fig. 4.35: Devices with thermally grown wet oxide and thick chromium + gold metal gates show a shift in threshold voltage towards 0 V and reduction in C_{max} with increasing anneal temperature. Further testing is required to confirm the reproducibility of this result.

4.3.8. Integrating the MOS capacitor with the folded patch antenna:

The folded patch antenna consists of three copper patches (width 0.035 mm) placed on top and bottom of a Rogers RO4003 substrate (relative permittivity of 3.55) of (25 mm x 25 mm) in size and 1.54 mm in height. The bottom (size: 7.75 mm x 16.75 mm) and the smaller of the top copper patches are linked to the bottom via copper through holes (i.e., plated through holes) of 0.25 mm in radius. The two top copper plates are joined via a capacitor (e.g., MOS capacitor) thus resulting in capacitive loading. The back-metal contact of the MOS capacitor is attached to the smaller top copper plate through conductive paste. The metal gate of the MOS capacitor is connected with the bigger top copper plate through wire bonding.

To wire-bond the MOS capacitor devices with the patch antenna, aluminum wire was used at the initial stage of the project. It was later realized that the series parasitic inductance added by the aluminum wire was shifting the resonance or dip frequency in the radar cross section (RCS) response curve beyond the test data observation range (i.e., 3 GHz to 8 GHz). Thus, to resolve that issue, aluminum wire was replaced by gold wire that has comparatively lower parasitic inductance [103]. Since a single wire-bond introduces additional parasitic inductance $Z_{\mathrm{Lparasitic}}$ in the total impedance of the system [104], it can be reduced to half by using two parallel wire-bonds in place of one [105]-[108]. As the resonant frequency of the system is inversely proportional to the amount of inductance, this need to be considered during design and manufacturing process in order to keep the pre-irradiated resonant frequency of the system within the 3 to 8 GHz detection window. For double wire-bonding purpose, the MOS capacitor need to have a bigger metal gate area to accommodate spaces for multiple wire bond pads without changing the capacitance value. This can be achieved by increasing the oxide thickness (which was one of the motivations to try making devices with 2000 nm thermally grown wet oxide). By testing different wire bonding schemes (i.e., gold or aluminum; single or double wire), it was realized that use of double gold wire bonding can help to set the resonant frequency within detection window thus improving the RCS response. However, gold wire is known to have some adhesion issue with aluminum and several other metals. This can be greatly resolved by depositing a stack of chromium and gold (alternatively titanium and gold) on top of the regular metal gate. Adding this additional metal stack will not impact the device C-V characteristics as previously seen in Fig. 4.31. The purpose of adding chromium or titanium is to improve the adhesion between the gold and the original metal gate layer and also, to prevent unwanted diffusion of gold. To test the gold wire-bonding scheme, initially, a MOS capacitor manufactured with 5 nm of chromium and 76 nm of gold gate [MA3, MC1] was used [Fig. 4.27a]. Unfortunately, the metal gate film thickness was inadequate to withstand the impact of pressure and ultrasonic energy during the thermosonic bonding [109]. Fig. 4.36 shows a micrograph of the devices after the wire-bonding attempt that shows peeling off of the gate metal stack due to impact. That issue was successfully resolved by manufacturing devices with thicker films (25 nm of chromium followed by 300 nm gold). Fig. 4.37 depicts micrographs of those devices with multiple gold bond wire parallel wedge bonded between two adjacent devices. Cross sections of the MOS capacitor loaded patch antennas with different wire bond scheme are presented in Fig. 4.38. Fig. 4.39 depicts the microphotographs of the wire-bonded regions of the MOS capacitor and the patch antenna showing the wedge type bonding.

Fig. 4.36: MOS capacitors with 5 nm of chromium and 76 nm of gold gates were used for the gold wire bonding experiment. The metal gate film thickness was inadequate as the impact of pressure and ultrasonic energy during the thermosonic wedge bonding process caused the gate to peel off (marked within the white circle).

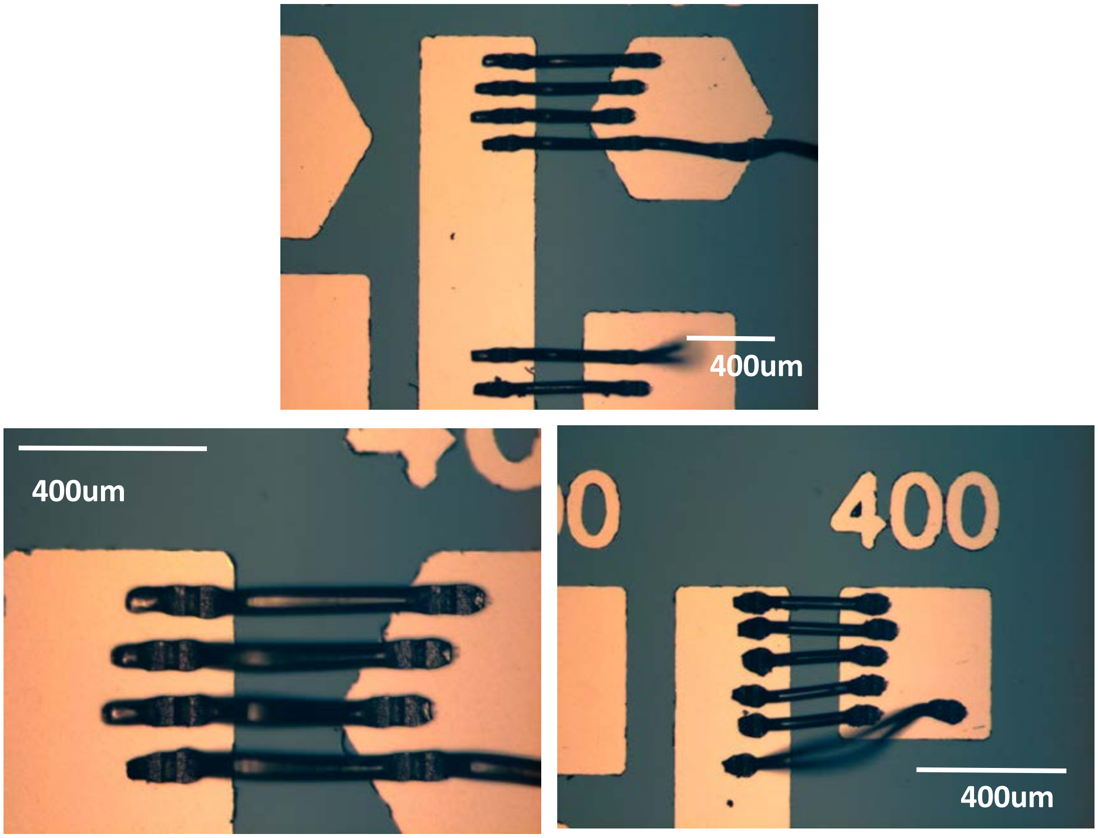


Fig. 4.37: Device with 2000 nm oxide and thicker chromium + gold metal gates are shown successfully wire-bonded with gold parallel wires without any peeling or damage to the metal gate.

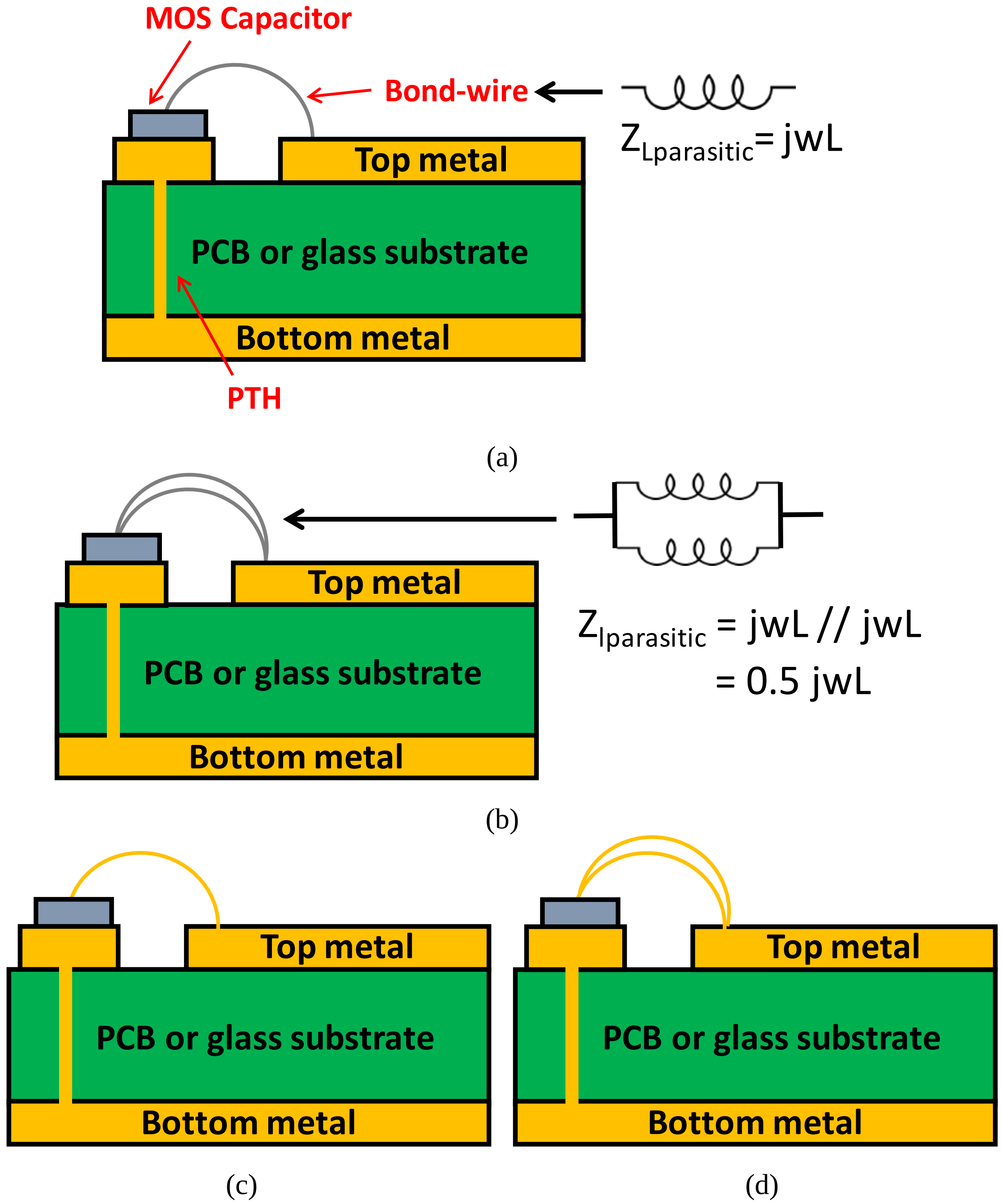
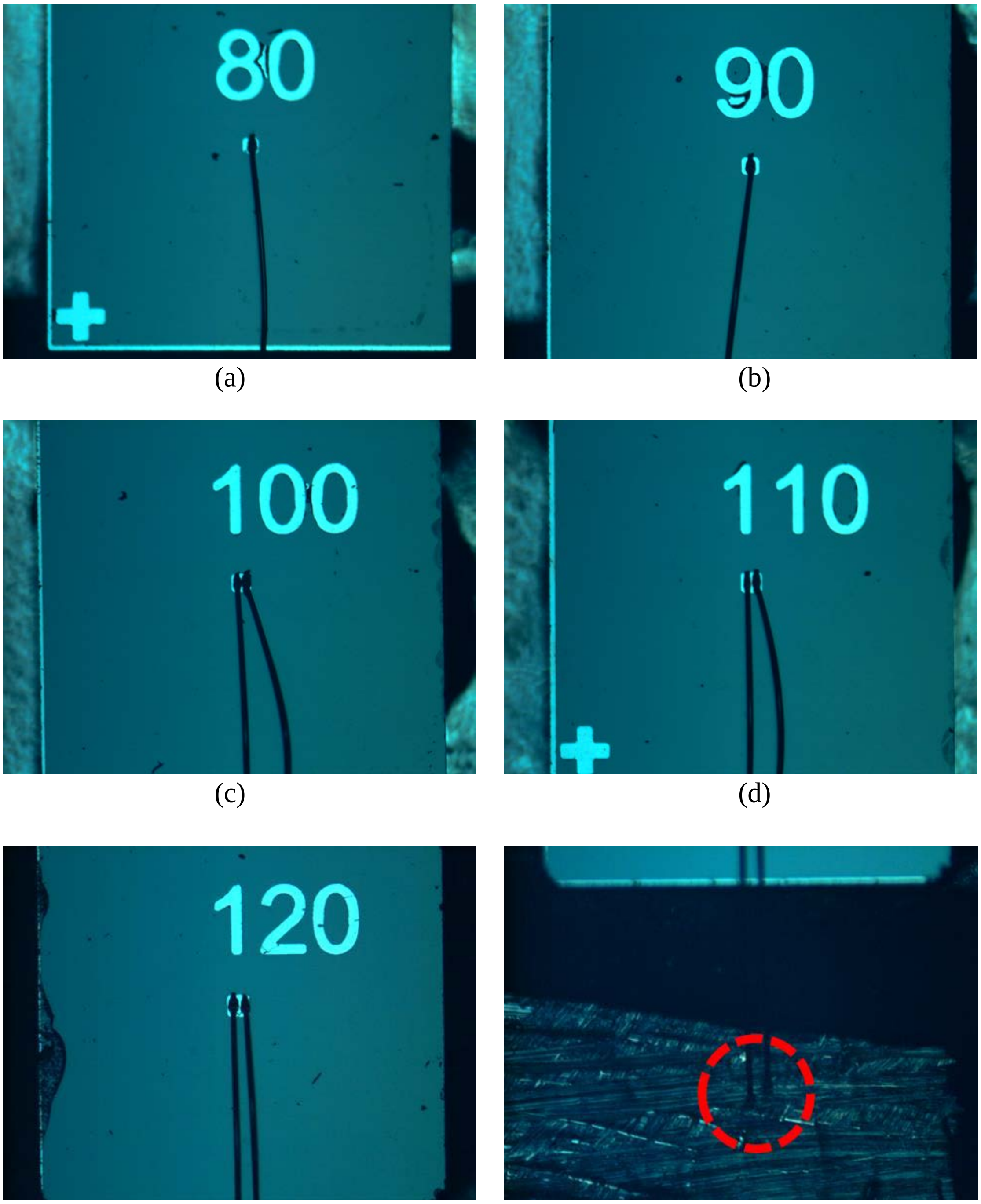


Fig. 4.38: Illustration of the stacked wire bond approach to integrate the MOS capacitors with the patch antenna: (a) with single aluminum wire bond introducing a parasitic inductance, $Z_{lparasitic}$ (b) with double aluminum wire bond the parasitic inductance can be reduced to half (c) with single gold wire bond and (d) with double gold wire bond.



(a) (b)

(c) (d)

(e) (f)

Fig. 4.39: <u>*Case 1:* </u>close view of MOS capacitor devices with single wire bonds: (a) 80 µm x 80 µm device (b) 90 µm x 90 µm device; <u>*Case 2*</u>: close view of MOS capacitor devices with double wire-bonds: (c) 100 µm x 100 µm device (d) 110 µm x 110 µm device (e) 120 µm x 120 µm devices; (f) shows double wire bond on folded patch antenna. It can be easily realized that bigger metal gate area is preferable for accommodating double wire-bonding (which is possible by using thicker gate oxide in order to keep the capacitance value unchanged).

Fig. 4.40 exhibits the top view of the patch antennas loaded with MOS capacitors of different capacitance values those were wire bonded using the double gold wire scheme.

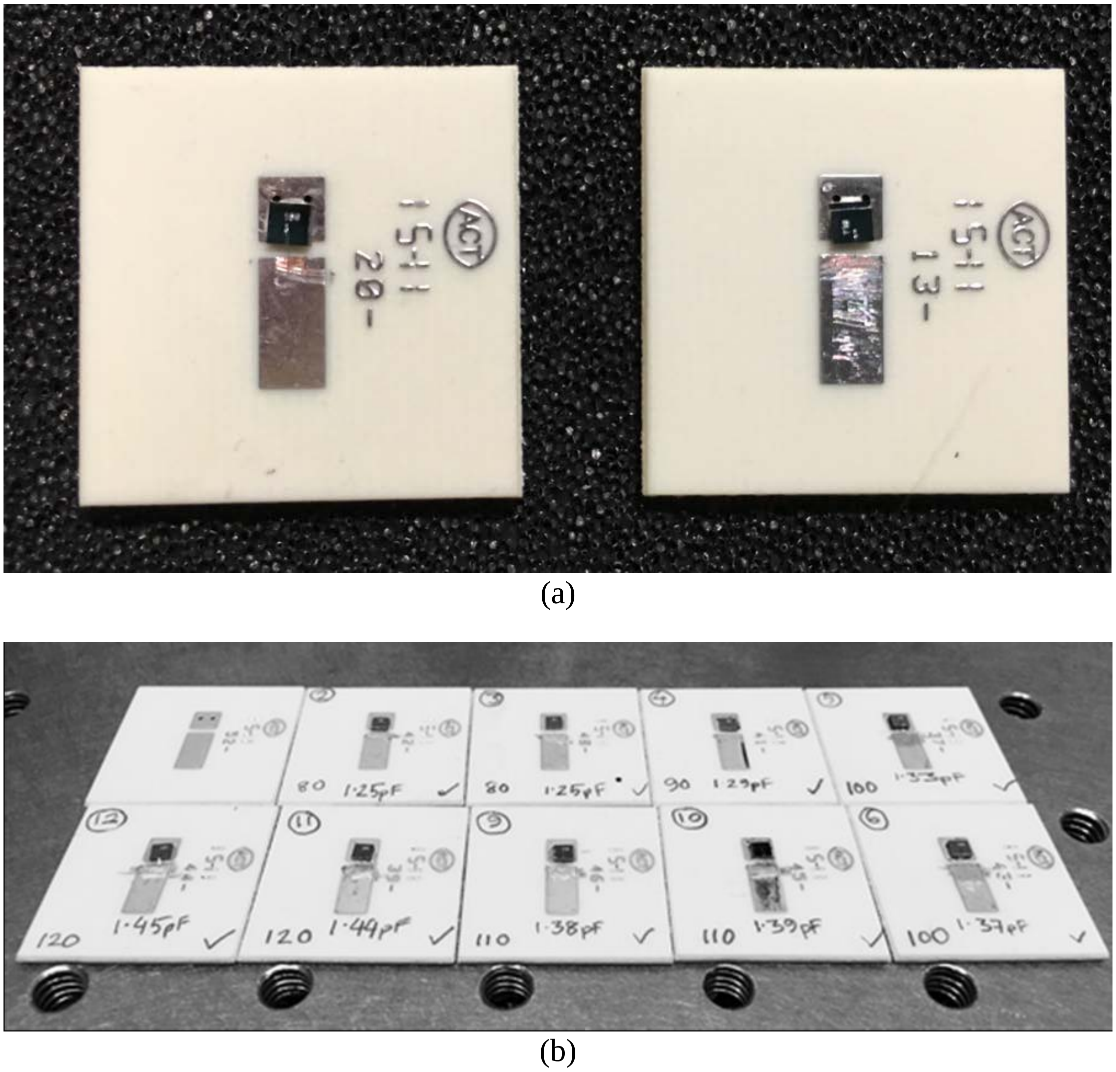


Fig. 4.40: (a) Patch antenna with wire bonded MOS capacitors. (b) Picture of all the loaded patch antennas that have been used for RCS measurement;

4.4. Radar Cross Section (RCS) measurement results:

The resonant frequency of the system varies with its load, which is capacitive. When such a system is interrogated with an incident electromagnetic wave, a sharp dip in backscatter will occur at the resonant frequency. This sort of response is typical of electrically small scatterers loaded with reactances that make them self-resonant. Such impact is illustrated in Fig. 4.41 where it is clearly observed that for increasing load capacitance (from different SMD capacitors) the radar cross section (RCS) characterized in an electromagnetic anechoic chamber [110] in the frequency range from 3 GHz to 8 GHz varies with C_{load}. Such characteristics have been obtained with SMD hyper-frequency capacitors, but similar behavior has been observed with integrated MOS capacitors, fabricated in the ASU Nanofab cleanroom (discussed in previous sections). However, before moving to the RCS results obtained from the MOS capacitor loaded patch antennas, an important observation related to the substrate resistivity needs to be discussed.

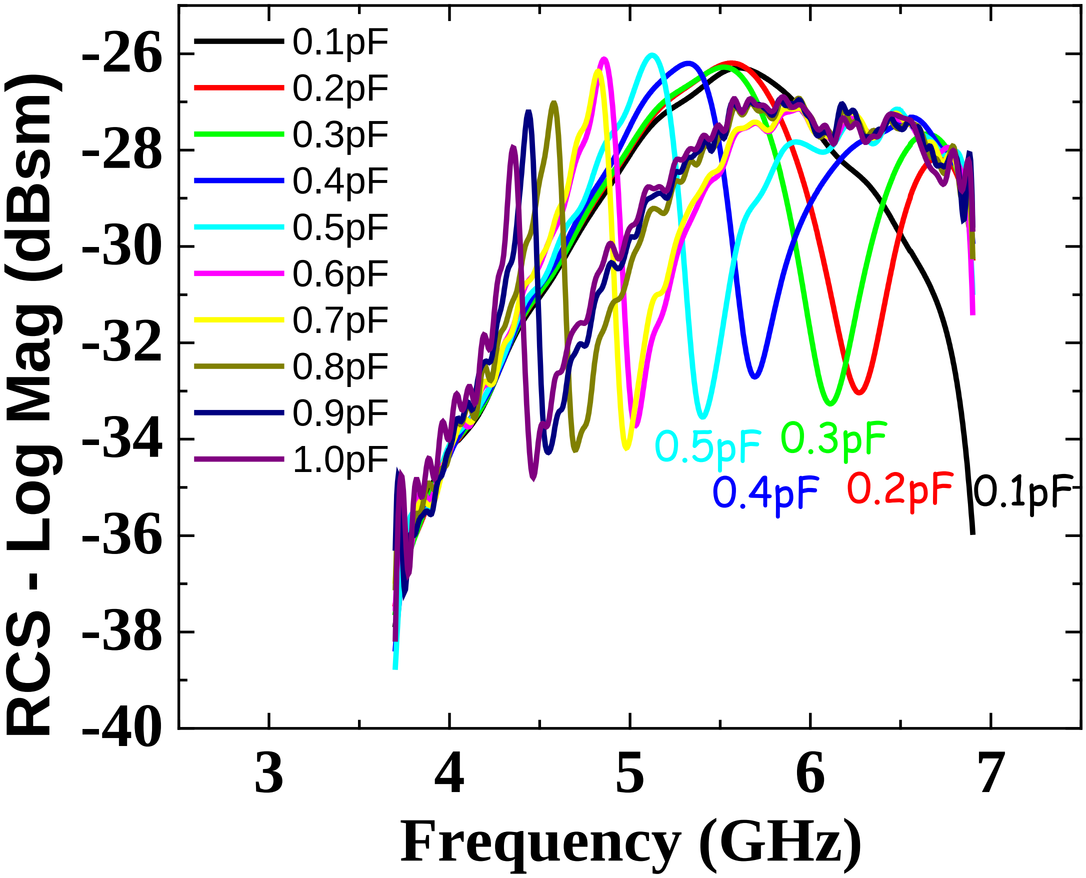


Fig. 4.41: Radar cross section of capacitively-loaded folded patch antenna, showing the variation and shift of the frequency dip occurring with the increase of C_{load}, each curve is obtained for a different C_{load} value.

4.4.1. Impact of substrate resistance on the resonance of the folded patch antenna:

Fig. 4.42 presents RCS characteristics of MOS capacitor loaded and non-loaded patch antennas measured at ASU anechoic chamber (photographs of ASU's anechoic chamber facility can be seen at. Fig. 4.43).

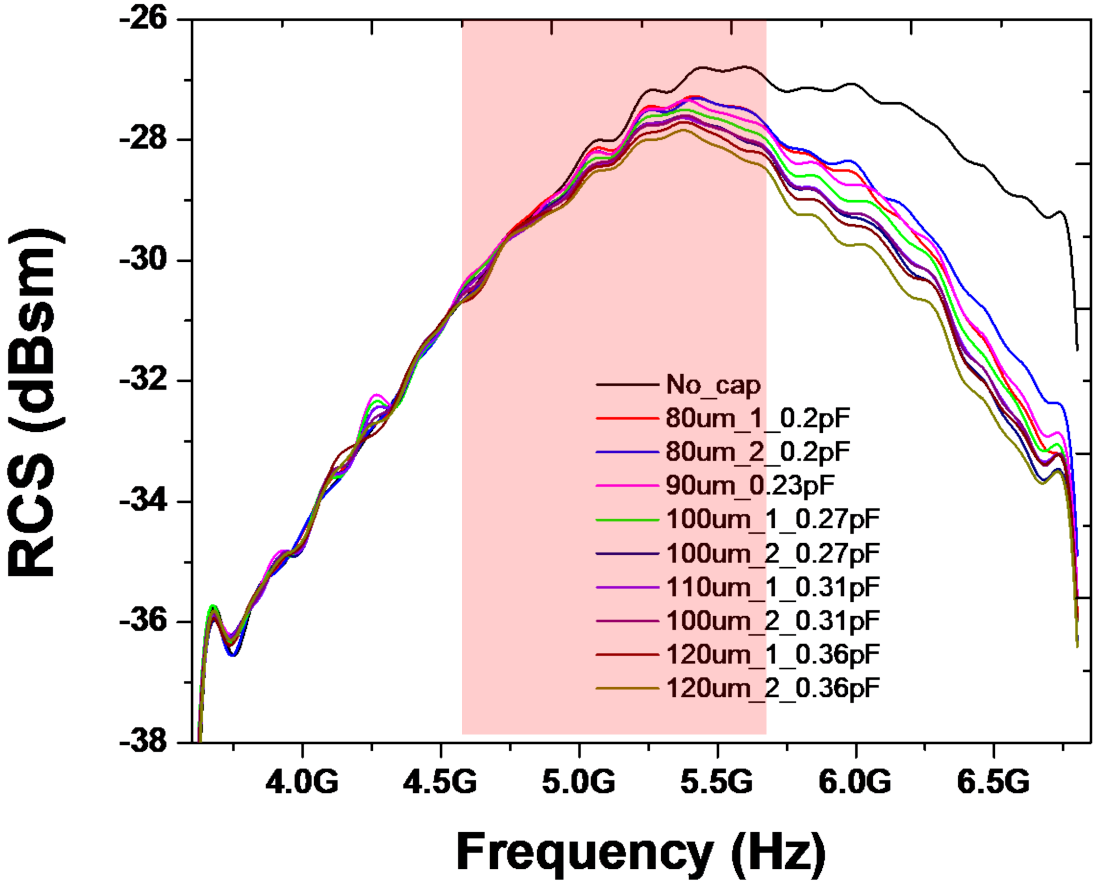


Fig. 4.42: Radar Cross Section measured on non-loaded and loaded patch antenna, with one or two wire-bonds attaching the MOS capacitors. In the legend, the size of the square-shaped metal gates is given that establishes the capacitance value when oxide thickness is constant. In addition, the number of wire-bonds used and the value of the capacitance are also provided. The shaded area indicates the frequency range where resonant dips were expected to occur.

RCS have been obtained with capacitive load in the range of 0.2 pF to 0.36 pF using MOS capacitors made using thicker oxides. It can be observed that there is no resonance observed on the RCS curves in the 3 to 8 GHz range frequency. After investigating this unexpected outcome, it was realized that the MOS capacitor structure that has been discussed thus far did not fully consider the effect of substrate thickness and resistivity on the resonance of the capacitor loaded patch antenna. The sensor system that has been designed and manufactured, was supposed to work as an LC resonator. However, there was some resistance added to the system due to the silicon substrate that makes it to be more like an RLC system which was not considered in the initial design. Fig. 4.44 shows the cross-section of the system indicating the series resistance due to substrate.

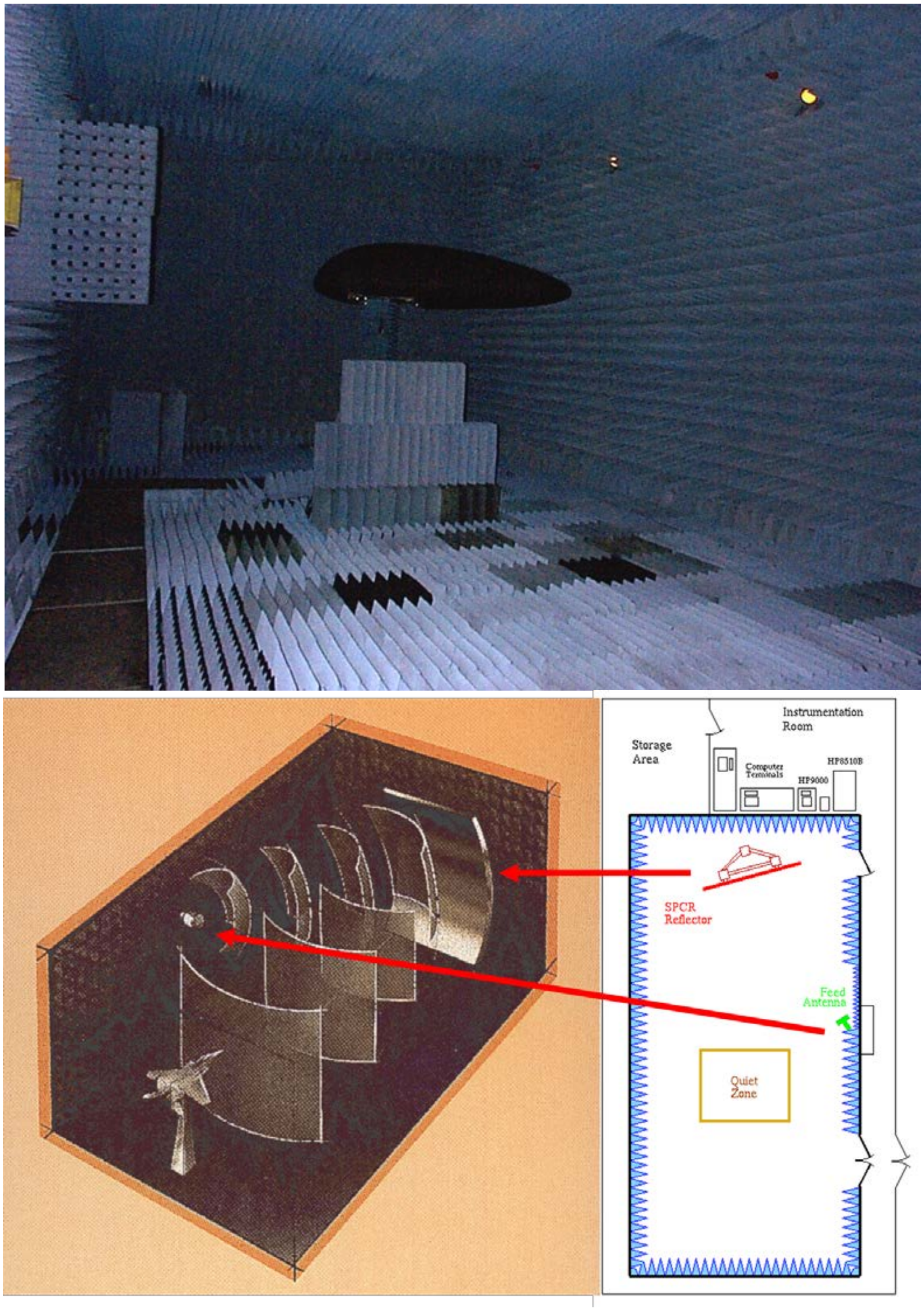
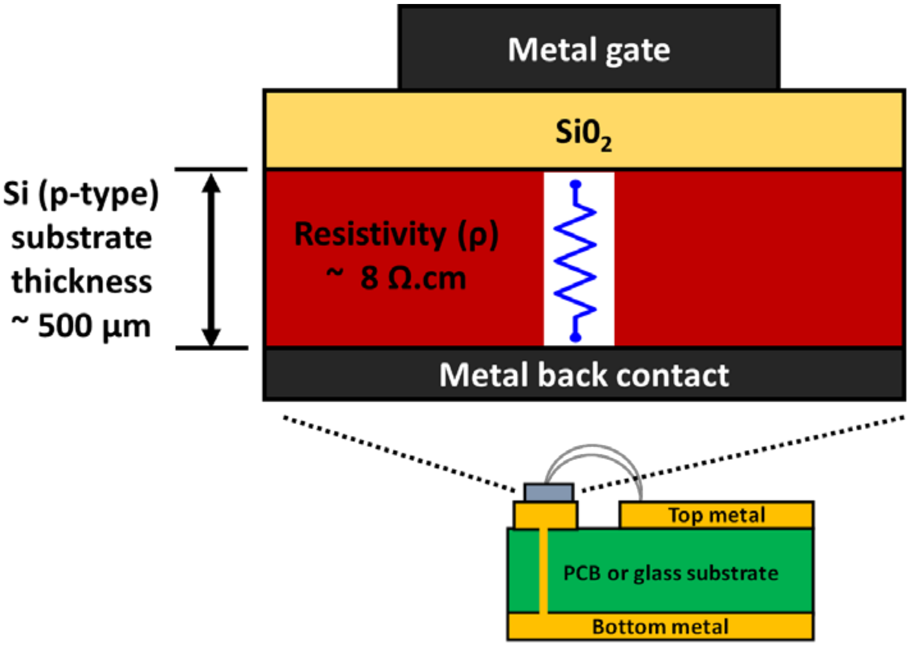


Fig. 4.43: Anechoic chamber at Arizona State University that was extensively used for radar cross section testing of the MOS capacitor loaded folded patch antennas [20].

As observed in Fig. 4.41, the patch antennas loaded with SMD capacitor of 0.5pF provided clear resonance signal on the RCS characteristic. These SMD capacitors have very low equivalent series resistance (ESR) as they are intended to be used at high frequencies (HF). When using the MOS capacitors on the patch antenna, a resistance (related to the substrate) present in series with the capacitance, should be taken into account. For manufacturing the MOS capacitors, 500 µm thick p-type substrate was used that has a resistivity around ~8 Ω.cm. For a capacitor with 100 µm x 100 µm metal gate area, this resulted in a $R_{\text{substrate}}$ or $R_{\text{parasitic}}$ of 4 kΩ as shown in Fig. 4.44.



$$R_{parasitic} = ESR = \rho \times \text{substrate thickness} / \text{cross sectional area}$$

For a 100µm x 100µm area gate:

$$R_{parasitic} = ESR = 8 \times 500\times10^{-4} / (100\times10^{-4})^2\,\Omega$$
$$= 4\times10^{3}\,\Omega$$

Fig. 4.44: Parasitic series resistance effect due to silicon substrate thickness and resistivity. A 500 µm thick Si substrate with 8 Ω.cm resistivity can result in 4 kΩ equivalent series resistance ($R_{\text{substrate}}$ or $R_{\text{parasitic}}$) when the gate size is (100x100) μm^2.

When compared to the typical values of ESR for HF SMD capacitor that are in the mΩ range, 4 kΩ is a pretty large number (almost a difference of 6 orders of magnitude). This leads to the fact that the resonance of the MOS capacitor loaded antenna will be damped by six orders of magnitude compared to the resonance observed with the SMD capacitor. This is something that can observed on Fig. 4.45 to Fig. 4.47, where the effect of $R_{\text{substrate}}$ is shown on the resonance of an ideal LC system with values close to the ones of the folded patch antenna system (please take into account the change of scale on the ordinate axis (y-axis) of the different graphs). The damping of the resonance increases dramatically for $R_{\text{substrate}}$ higher or equal than 50 mΩ. For the silicon wafer with 8 Ω.cm resistivity (that was used to manufacture the MOS capacitors), the damping on the resonance is extremely high, and gets wider. Due to that it was not possible to see the resonant peak with these MOS capacitors. To see the resonance of the patch antenna, the equivalent series resistance due to the substrate (i.e., $R_{\text{substrate}}$) should be brought in the range of a few mΩ which is possible by selecting a substrate with very low resistivity and reducing the thickness. These results were validated against HFSS simulations which is given at Appendix A.

4.4.2. RCS Measurements with MOS capacitors with low series resistance:

Based on the observations described in the previous section, several MOS capacitors were manufactured on different p-type silicon wafers that has a significantly lower resistivity of 0.001 Ω.cm and smaller thickness (i.e., ~250 µm), enabling a reduction of $R_{\text{substrate}}$ from 4 kΩ to 0.250 Ω.

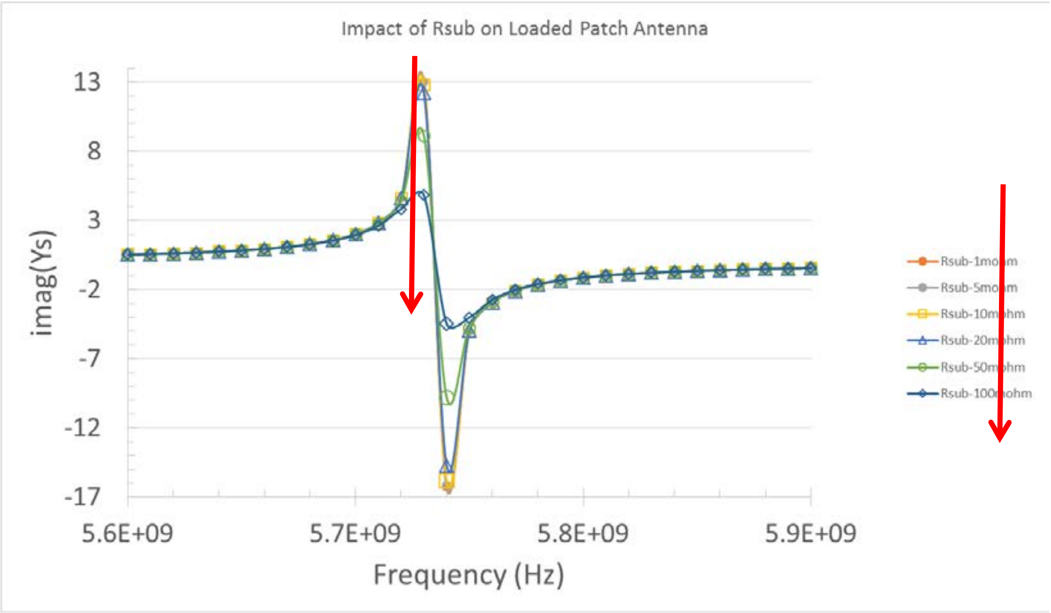


Fig. 4.45: Theoretical resonance with $R_{\text{substrate}}$ between 1 mΩ and 100 mΩ. The downward red arrows on the legend and the plot indicates that when $R_{\text{substrate}}$ increases, resonant peak dampens as a consequence.

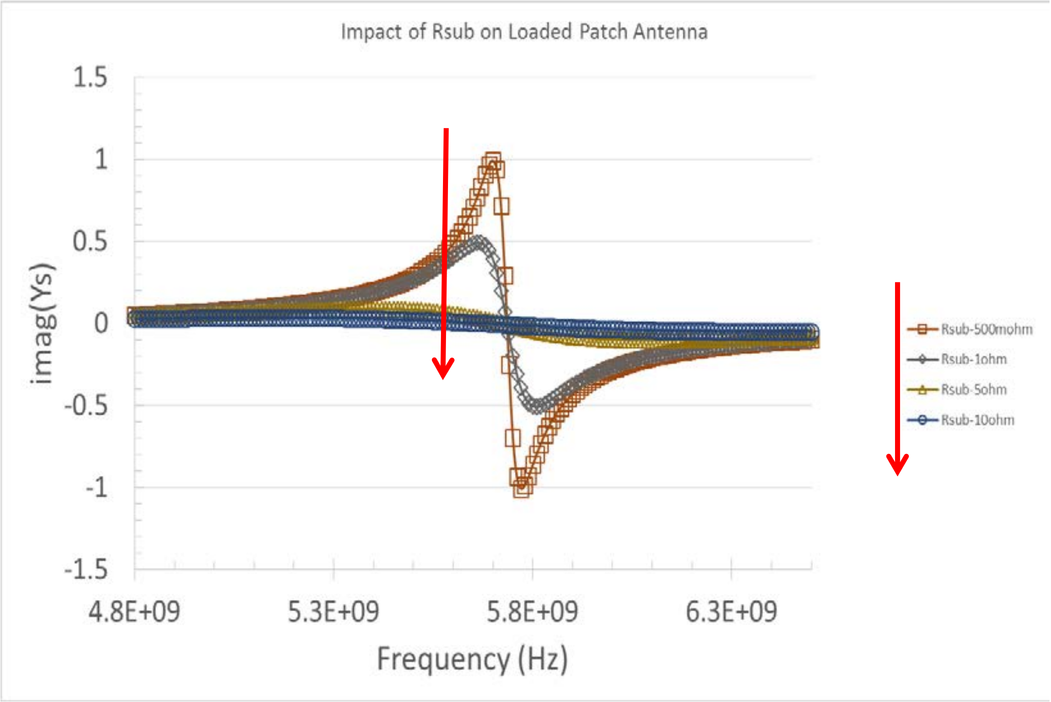


Fig. 4.46: Theoretical resonance with $R_{\text{substrate}}$ between 500 mΩ and 10 Ω. Like, Fig. 4.45, the downward red arrows on the legend and the plot indicates that when $R_{\text{substrate}}$ increases, resonant peak dampens as a consequence.

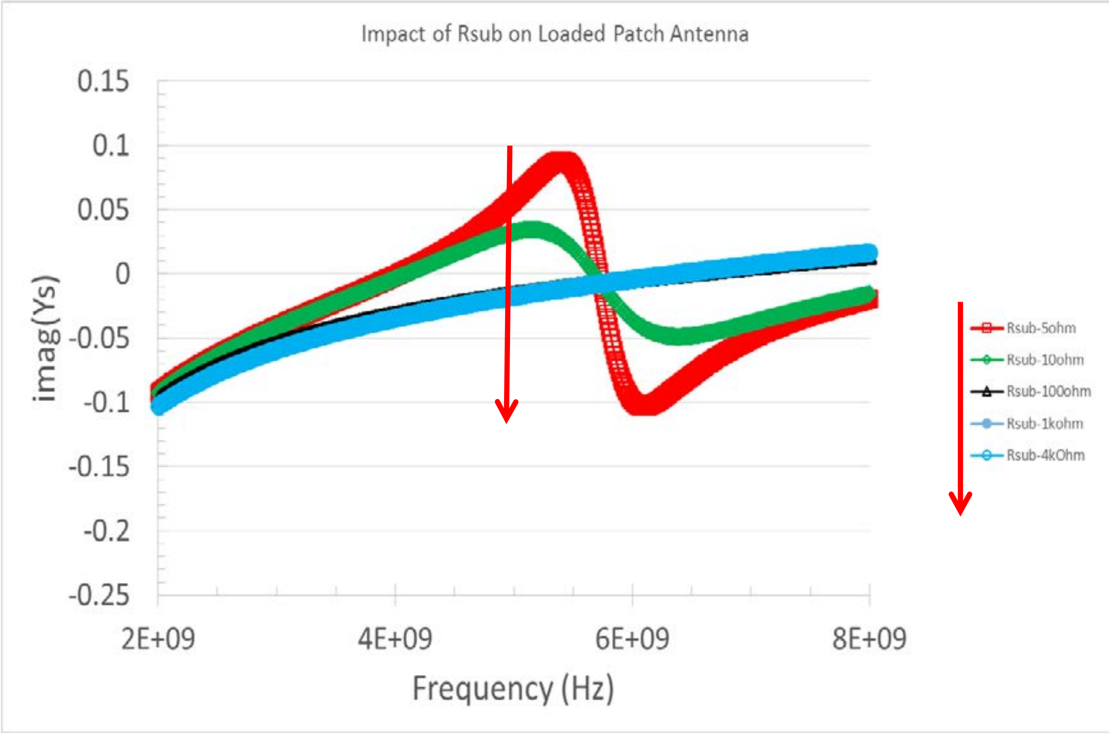


Fig. 4.47: Theoretical Resonance with $R_{\text{substrate}}$ between 5 Ω and 4 kΩ. Similar to previous two Figs., the downward red arrows on the legend and the plot indicates that when $R_{\text{substrate}}$ increases, resonant peak dampens as a consequence.

The RCS characteristic obtained from such MOS capacitor loaded patch antennas are presented in Fig. 4.48, where the MOS capacitors have different squared size gate areas (i.e., 80x80 μm^2, 90x90 μm^2, 100x100 μm^2, 110x110 μm^2 and 120x120 μm^2). First, with the reduced substrate resistivity, the resonance peak can be clearly observed in the frequency window of interest (3-8 GHz). This is true for all capacitor sizes that were tested. The legend shows the size of the various capacitors (i.e., length of each side). Secondly, it was observed that, similar to the case of the SMD capacitors, MOS capacitor loaded patch antennas exhibit an increase in the position of the frequency dip with decreasing area (i.e., with decreasing capacitance). This behavior is also replicated well by electromagnetic simulations, as shown later in Appendix A.

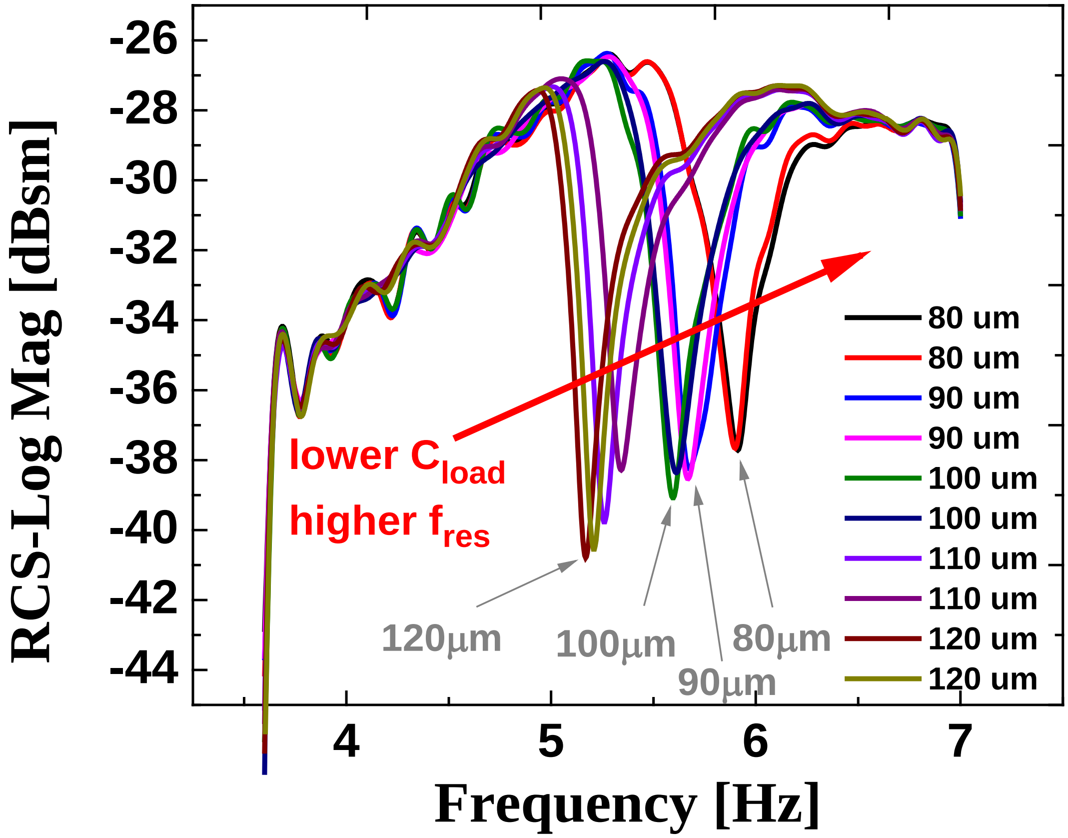


Fig. 4.48: Radar cross-sections of CLPA, showing the variation and shift of the frequency dip occurring for different MOS capacitors with varying area, i.e., 80 µm x 80 µm; 90 µm x 90 µm, 110 µm x 110 µm; 100 µm x 100 µm and 120 µm x 120 µm devices. The MOS capacitors were manufactured on a p-type silicon substrate that has a thickness of ~250 µm and resistivity of 0.001 Ω.cm. This resulted in a significant reduction of $R_{\text{substrate}}$ (equivalent series resistance of the MOS capacitors) from 4 kΩ (Figs. 4.42 and 4.44) to 0.25 Ω. As a consequence, sharp resonant dips were detected during the RCS testing.

4.5. Implementation of the wireless total dose detector:

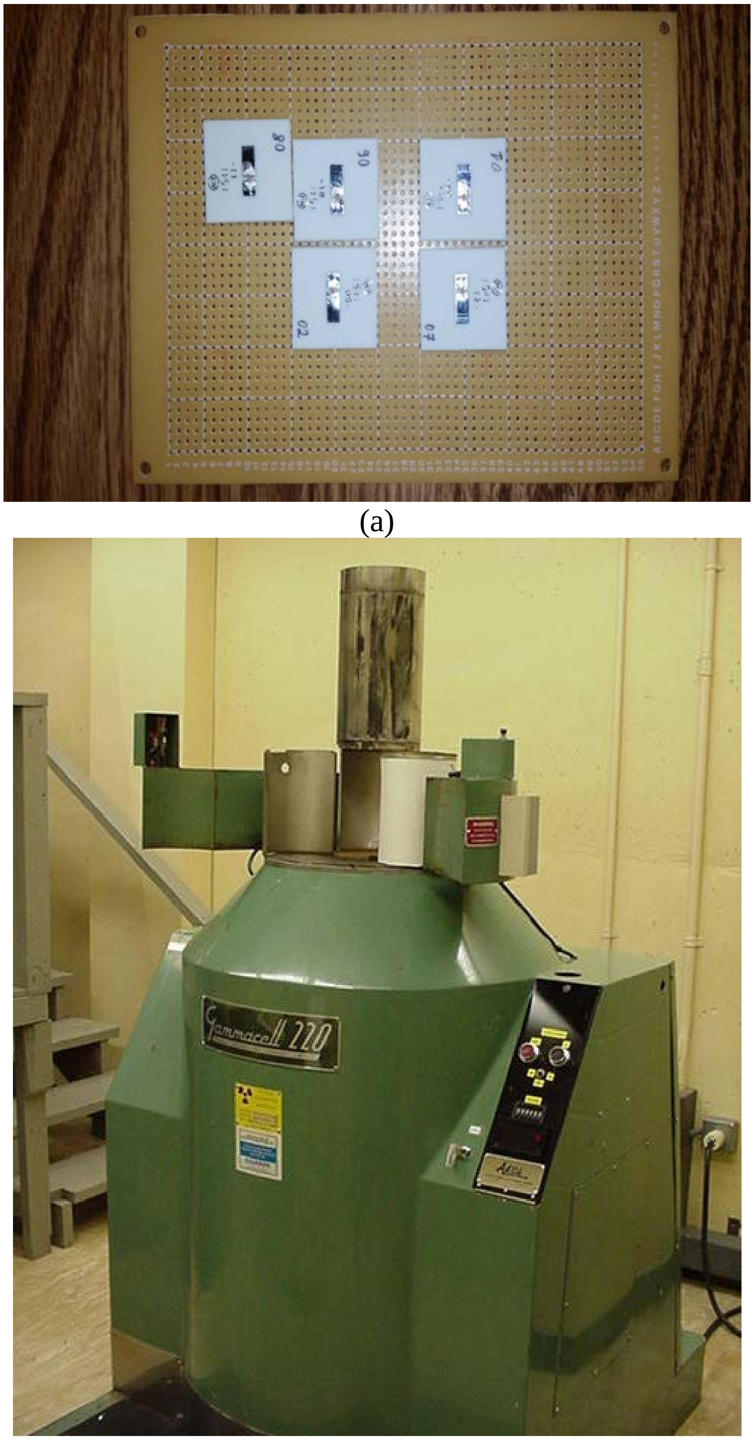
According to the principles described in the previous sections, it is possible to develop a wireless total dose sensor that is based on such devices (i.e., MOS capacitor loaded patch antennas). MOS capacitors are characterized by their C-V curve showing a variation of the capacitance of the structure, dependent on the mode of operation of the device (depletion, accumulation or inversion) [111]. An example of such characteristic measured on a 500 µm x 500 µm squared top electrode manufactured at ASU is previously presented in Fig. 4.1. where the capacitance measured using an Agilent 4284A LCR-meter is plotted as a function of substrate to gate voltage (V_{SG}) of the structure. At the point where $V_{\mathrm{SG}} = 0$ V (i.e., for DC conditions), the capacitance is designated as C_0 (also mentioned as DC capacitance earlier), which would be the capacitance loading the patch antenna (C_{load}), since it is a passive device (no biases applied on the patch antenna). As discussed earlier, the capacitance near $V_{\mathrm{SG}} = 0$ V varies as a function of TID due to radiation induced hole trapping and the subsequent change of surface potential. Such shifts in C_0 or C_{load} induces a shift of the resonance location in the RCS of the loaded antenna. The shift in frequency can be linked to the total dose absorbed by the capacitor, enabling the use of such system as a passive wireless dosimeter.

A series of MOS capacitors have been manufactured at the ASU Nanofab and characterized after exposure to ionizing radiation. Total dose exposure was conducted at the ASU radiation damage lab using a Gammacell 200 irradiator (Fig. 4.49) enabling Co-60 gamma-ray exposure at a dose rate of 10 mrad(air)/s. Exposure of the capacitors was conducted with all pins floating, as would be the case for patch antenna based sensors.

The C-V characteristic obtained for 500 µm x 500 µm and 400 µm x 400 µm MOS capacitors (dry SiO_2, LPCVD) exposed to gamma-rays are presented in Fig. 4.50. It was observed that the capacitors are soft to ionizing dose (i.e., a strong shift of the C-V occurs with TIDs as low as 540 rad(air)). From Fig. 4.50(a), it is evident that the capacitance measured at $V_{SG} = 0$ V varies with TID, leading to a variation of the DC capacitance of the MOS capacitor loaded patch antenna. For a MOS capacitor made with such a manufacturing process, and with capacitance values in the range of 0.3 pF to 1.0 pF (i.e., areas of 80 µm x 80 µm to up to 200 µm x 200 µm) the capacitance C_{load} would be in the range of capacitances exhibiting a dip in the RCS characteristic and the induced variation of capacitance and total dose could be measured through the variation of frequency values at which such dip occurs.

The behavior presented in Fig. 4.50 is measured on MOS devices whose areas lead to capacitances that are larger than the ones leading to RCS response. Nevertheless, for a given manufacturing process, the shifting of the C-V characteristic would be similar for devices with reduced areas as can be observed for the 500 µm and 400 µm side devices' C-V presented.

In Fig. 4.51, the frequency at which the resonance dip occurs is plotted as a function of the load capacitance (where the data are extracted from Fig. 4.41). A linear fit is used to obtain the relation between the dip frequency and the capacitance. The data are presented with a 0.1 pF abscissa error on the capacitances values as the RF/Microwave capacitors design kit used (Fig. 4.41) is an ATC Kit 15 – 500S, where devices have a 0.1 pF tolerance.



(a)

(b)

Fig. 4.49: MOS capacitor loaded patch antennas shown at (a) were loaded into Gammacell 220 irradiator shown at (b) for ^{60}Co irradiation

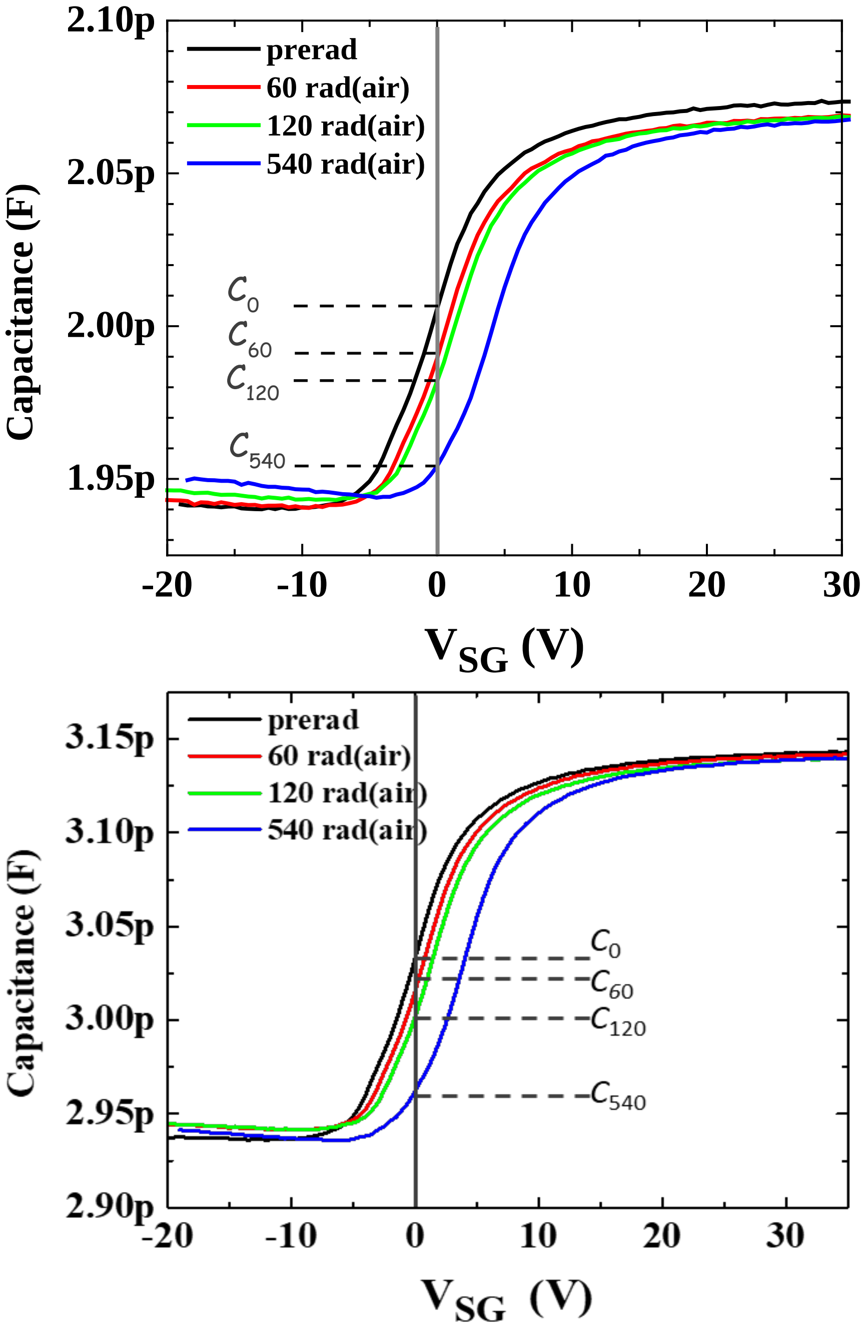


Fig. 4.50: C-V characteristics of MOS capacitors exposed to Co-60 gamma-rays. (top) 500 µm x 500 µm devices, (bottom) 400 µm x 400 µm devices. TID induced C-V shifts are clearly visible in both cases that results in change in the DC capacitance value. If such a device is loaded on a patch antenna (where C_{max} is around 1 pF and pre-irradiated C_0 is larger than C_{min}), the radiation induced change in the DC capacitance value will shift the resonant frequency dip of the system which can be tracked by using a RF interrogator.

The linear fit extracted from such data is characterized by the following equation:

$$y\ [\text{GHz}] = -2.3\cdot10^{21}\, x + 6.67844\cdot10^{9}\ ,\ x \text{ in [pF]} \ldots\ldots. (5)$$

Eqn. 5 allows one to obtain the expected variation of the dip frequency for MOS capacitors similar to the ones presented in Fig. 4.50. The capacitance variations observed in Fig. 4.50(a) are 0.81% at 60 rad, 1.18% at 120 rad and 2.57% at 540 rad (percentage variation of the initial DC capacitance) which for a normalized capacitance of 1 pF would incur variation as represented in Fig. 4.51, where the vertical lines represent the different $C_{0\text{rad}}$, $C_{60\text{rad}}$, $C_{120\text{rad}}$ and $C_{540\text{rad}}$ and their expected frequency dip location for a device with an initial capacitance of 1 pF. The variation of frequencies extracted are presented in Table 4.2, where the Δf/rad is also computed which depends on the linearity of the MOS cap TID response.

TABLE 4.2

VARIATION OF RESONANT FREQUENCY FOR DIFFERENT LOAD CAPACITANCE DUE TO INCREASING TID

TID (rad(air))	Load capacitance C_{load} (F)	Resonant frequency f_{res} (Hz)	Δf_{res} (Hz)	Δf_{res}/rad
0	10^{-12}	$4.29\ 10^{9}$	N.A	
60	$0.992\ 10^{-12}$	$4.30\ 10^{9}$	$1.42\ 10^{7}$	$3.07\ 10^{5}$
120	$0.9988\ 10^{-12}$	$4.31\ 10^{9}$	$8.74\ 10^{6}$	$1.53\ 10^{5}$
540	$0.974\ 10^{-12}$	$4.34\ 10^{9}$	$3.23\ 10^{7}$	$7.67\ 10^{4}$

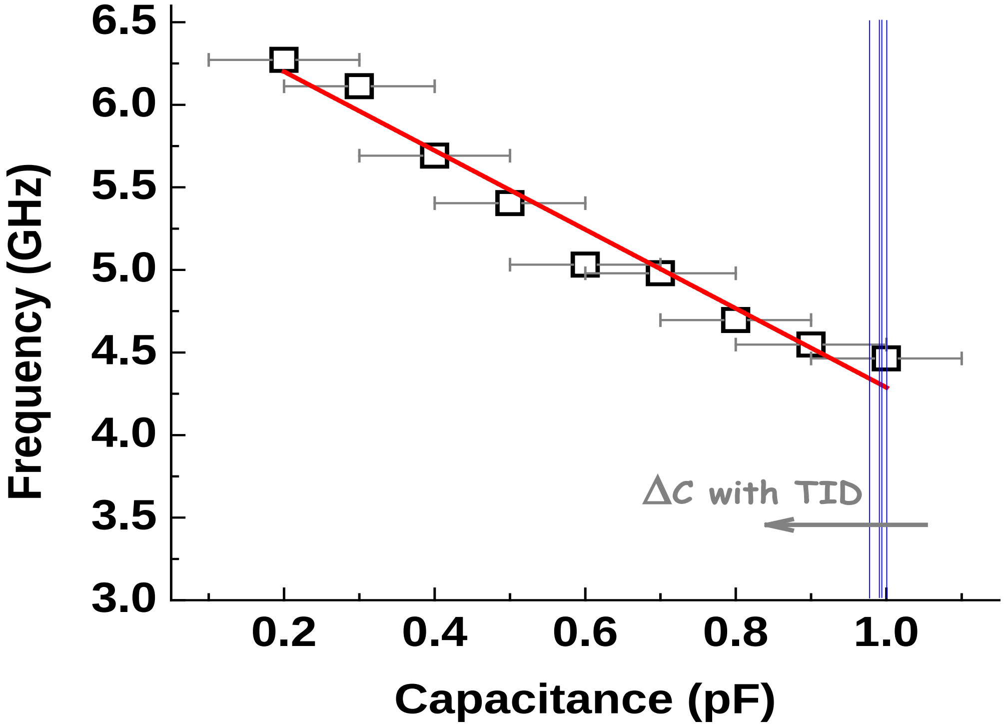
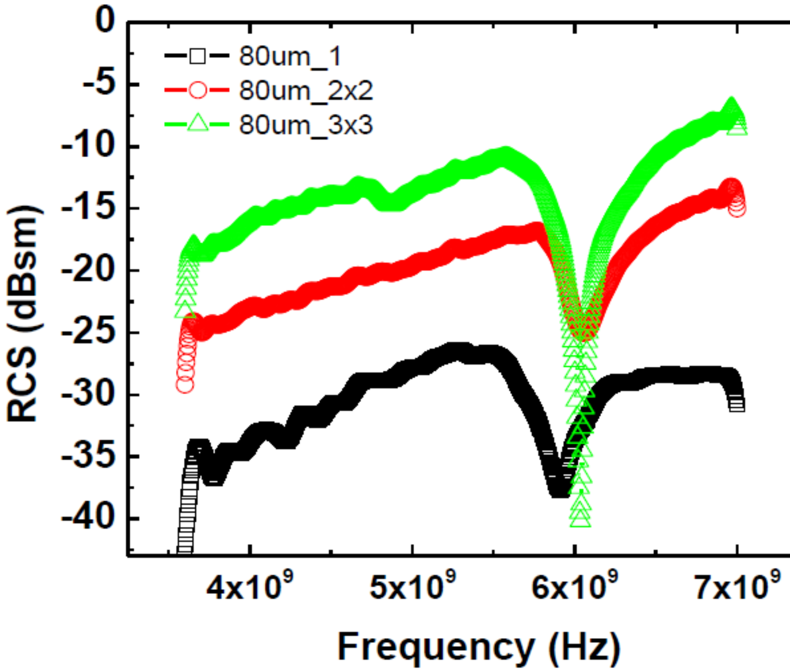


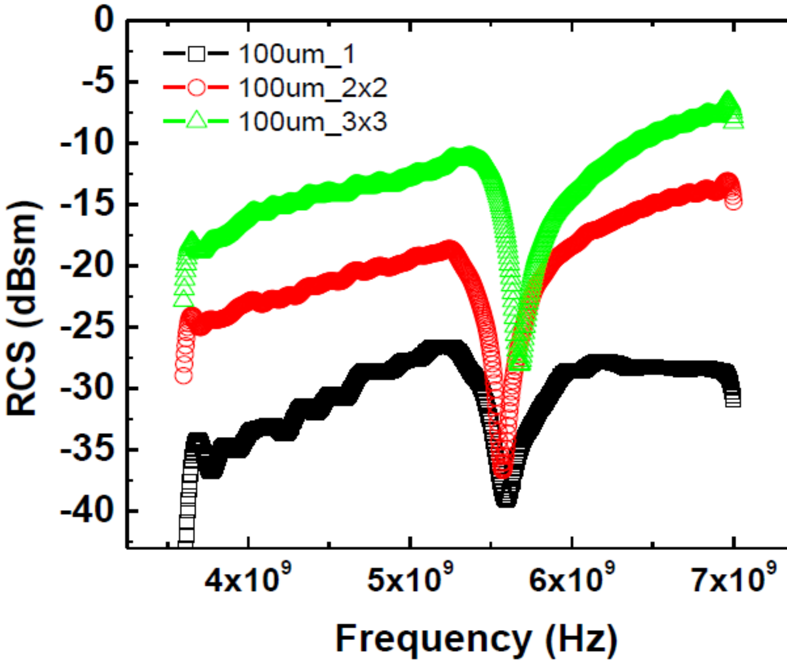
Fig. 4.51: Variation of the resonant frequency dip as a function of C_{load}, characterized with high frequency SMD capacitors loaded patch antennas.

Fig. 4.52: CLFPAs characterized in the ASU clean room. Set of 2 by 2 (on the left) and 3 by 3 (on the middle and on the right) antenna array used for RCS measurements.

RCS measurements have also been conducted on patch antenna arrays. The different arrays of CLFPA characterized are shown in Fig. 4.52. Each array is loaded with a single value capacitance. The RCS obtained on the different samples are presented in Fig. 4.53 and Fig. 4.54. In Fig. 4.53(a)-(c), the RCS of single patch antenna, and arrays of 2 by 2 and 3 by 3 patch antenna are compared, for different capacitance value in each figure. It can be observed that the RCS are shifted to higher return values (dBsm) and that the resonant frequency is only slightly modified. The modification of resonant frequency is due to the mismatch between capacitors and the total parasitic that exist between the different configurations. A higher return value means a higher electromagnetic power returned from the array than the single patch antenna making it easier to be detect by an RF interrogator. In Fig. 4.54(a)-(b), RCS measurements obtained on arrays loaded with different capacitances are presented. It can be observed that a shift of resonant frequency is clearly observed on the arrays, as was also observed on single patch antenna, when capacitance varies (Figs. 4.41, 4.48).

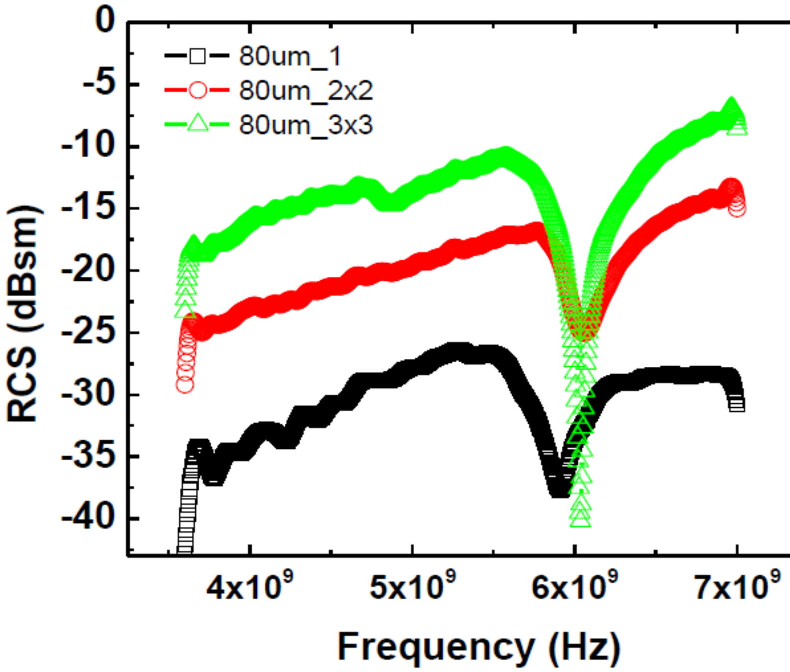


(a)



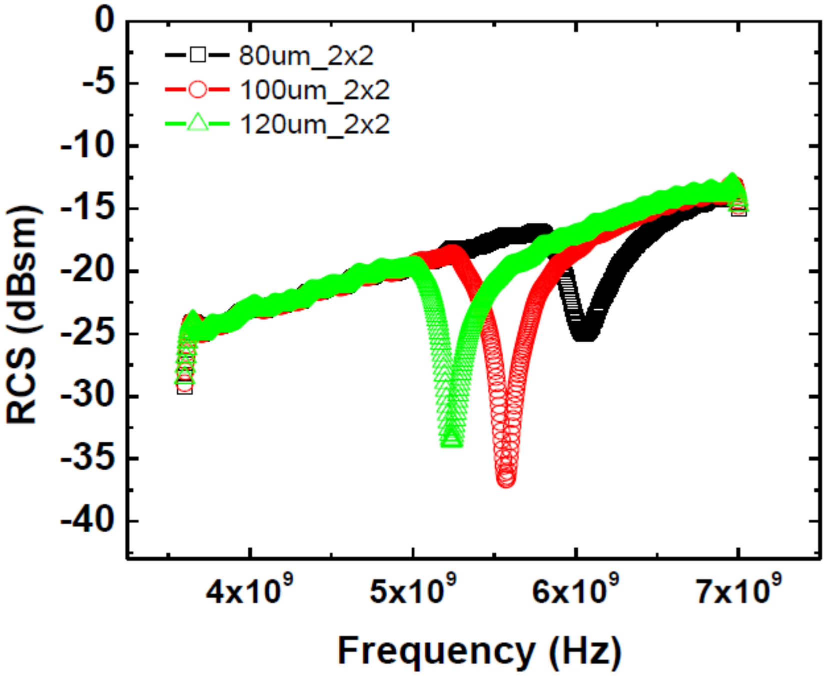
(b)

Fig. 4.53 (part 1 of 2): Radar Cross Section of antenna and array of antennas loaded with (a) 80 µm x 80 µm area capacitors (b) 100 µm x 100 µm area capacitors (c) 120 µm x 120 µm area capacitors

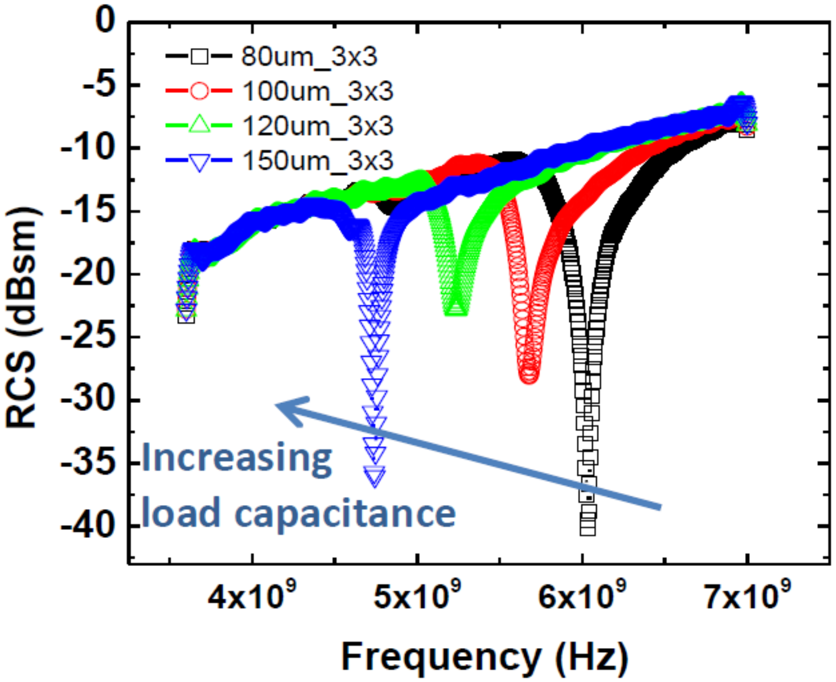


(c)

Fig. 4.53 (part 2 of 2): Radar Cross Section of antenna and array of antennas loaded with (c) 120 µm x 120 µm area capacitors



(a)



(b)

Fig. 4.54: RCS of (a) 2 by 2 arrays (b) 3 by 3 arrays. Both type of arrays are loaded with three increasing capacitance (80 µm, 100 µm and 120 µm side devices)

4.6. Conclusion:

In this chapter, we presented a novel wireless radiation detection system based on MOS capacitor loaded folded patch antenna. The system can be operated in the range of 3 to 8 GHz if the pre-irradiation load capacitance value can be tuned close to 1 pF. For a tuned system, the load capacitance decrease in response to TID can be sensed through an increase in resonant frequency since a variation of 0.1 pF can lead to clear shifts in the RCS characteristics, as presented in Fig. 4.51. Depending on the softness of the process used for the MOS capacitor manufacturing, the system sensitivity can be modified enabling use of the sensors for different applications and environments. To increase the antenna reflected power, arrays of patch antennas can be implemented. For array case, sensitivity studies need to be conducted to characterize the impact of capacitor mismatch on the TID response of the arrays. For interested readers, TCAD modeling of trap precursors and electromagnetic modeling of the folded patch antenna are provided in Appendix A. The simulations were performed by CFDRC using NanoTCAD and ANSYS HFSS simulation software and were guided by the experimental data generated here at ASU and discussions with ASU researchers (i.e. author and his research advisers) [92].

CHAPTER 5

FUTURE RESEARCH WORK

5.1. Metal-chalcogenide glass based sensors:

The smallest limit of detection (LOD) of the metal-chalcogenide glass based sensors at current development stage is around ~600 krad(GeSe). For personal dosimetry application, this is quite a large number. Thus, further research work needs to be done to bring down the LOD to make them suitable for applications that require low dose sensing. One possible way to do that might be the use of standard photolithography techniques to pattern the silver or metal electrodes. If this can be done successfully, it is possible to bring down the spacing between electrodes to couple of microns, thereby significantly reducing the LOD of the sensors (the relationship between LOD and spacing is presented in chapter 3). So far, the sensors manufactured using shadow masks have minimum spacing of 1 mm. Thus, scaling down the spacing to couple of microns can be considered a notable progress. However, introducing the photolithography step in the process flow can bring in new challenges. Recent experiments have shown that undoped chalcogenide glass films tend to react with some of the chemicals used for photolithography processes (e.g., developer, stripper). Therefore, a compatible chemistry needs to be explored that does not react with chalcogenide glasses during the photolithography processes. While this is done, a reasonably easy and cost-effective way to bring down the LOD can be slightly modifying the device structure. Fig. 5.1 presents such a cross-section. As can be seen, the device is quite similar to the samples presented in chapter 3. Only difference is that, a thin film of metal (preferably an inert metal that does not react with chalcogenide glass) is sandwiched between the PEN substrate and the chalcogenide glass film.

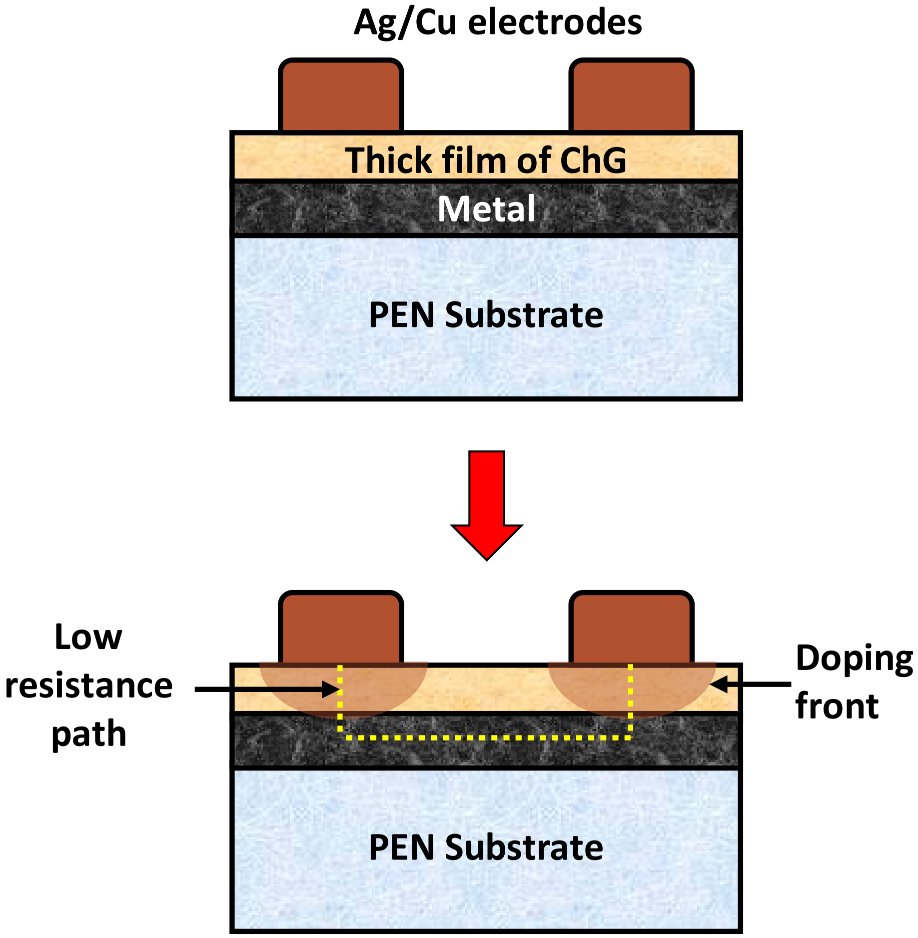


Fig. 5.1: An alternative structure to bring down the limit of detection of the metal-chalcogenide glass based sensors to a reasonable range for personal dosimetry application. The metal layer underneath the chalcogenide glass film and the assumed isotropic nature of the radiation induced Ag+ doping profile inside the ChG, helps bringing down the resistance level to "low resistance state" between two nearest electrodes even before the doping fronts laterally touch each other (resulting in lower LOD). This LOD reduction can be obtained without using an expensive photolithography step keeping the manufacturing cost low. However, future research works need to be done: (i) to validate this prototype concept and (ii) to explore the impact of ChG film thickness, composition and work function of the sandwiched metal film on the sensor performance characteristics.

As the proposed structure starts getting irradiated, the silver ion doping fronts begin to spread isotopically from the silver-chalcogenide glass interface into the undoped chalcogenide film region. When the doping front spreads enough and touches the sandwiched metal layer, the resistance level between two electrodes quickly goes down to the “low resistance state” due to creation of a low resistance path. The change of resistance state (or other words LOD) event happens way before the lateral doping fronts from nearest electrodes touch each other. This clearly demonstrates that the LOD can be tuned to a noticeably lower value without changing the electrode spacing parameter if an additional metal layer underneath the ChG film is added. For the proposed structure, the LOD will most likely depend on the chalcogenide film thickness and composition (selenium/ sulfide content). LOD is expected to go down as the ChG film thickness decreases. It is expected to further go down if the chalcogen content of the film (i.e., selenium, sulfide) is increased. However, use of too thin selenide rich ChG film might not be practical since devices made of such composition have shown getting impacted by background radiation and reaching saturation before irradiation. Regardless, the notable advantage of the proposed structure is that, the LOD reduction can be achieved with the same shadow masks used before, keeping the manufacturing cost considerably low (since the device operation takes advantage of vertical doping front progression instead of the lateral movement). Future research works on this topic can consider testing this possible prototype with different chalcogenide composition (to check the effect of chalcogen content), different metal films used as the sandwiched layer (to explore the effect of work function) and finally different thicknesses of the ChG film (to check scalability).

5.2. MOS capacitor based wireless total dose sensors:

As discussed in chapter 4, in order to achieve a high $C_{\max}/C_{\min}$ ratio, the resistivity of the silicon substrate needs to be higher. But selecting a high resistive substrate also increases the equivalent series resistance that eventually dampens/ widens the signal peak at the resonant frequency. A dampened resonant signal is quite difficult to detect during radar cross section testing. However, there is an alternative manufacturing technique using silicon-on-insulator (SOI) wafers that can enable use of silicon with high resistivity while keeping the equivalent series resistance low. The cross-section of a typical SOI wafer is given at Fig. 5.2 (a). SOI wafers can be manufactured with different dimensions (based on application) where the top silicon layer (also known as the device layer) can have a thickness starting from ~12 nm to couple of hundred microns. Similarly, the buried oxide thickness can be of diverse range. If the MOS capacitors are fabricated using a SOI wafer, the thin silicon device layer can be used as the semiconductor. Since the thickness of the device layer will be in the order of couple of microns, it’s resistivity can be set to a higher value. This will be helpful to obtain a reasonable high $C_{\max}/C_{\min}$ ratio while keeping the equivalent series resistance at a noticeably low value (therefore, less dampening effect on the resonant signal). The buried oxide underneath the device layer will act as the oxide layer of the MOS capacitor. By deep etching the handle layer (using KOH wet etching or DRIE dry process), squared areas of different sizes will be opened on top of the buried oxide layer. Directly on top of that, metal stacks of interest will be deposited to form the gates of the MOS capacitor. To etch the handle, DRIE etching process is preferable since it can provide steep sidewalls, thus reducing unwanted parasitic capacitance effects. However, DRIE process is expensive and time consuming since it needs sophisticated equipment. Also, dry etching is known for poor selectivity and the etch depth of DRIE process usually depends on the etch opening (e.g., for the same etch time, etch depth will be higher for larger etch openings [112]). Thus, caution should be exercised during manufacturing, specially at the final stage of the deep dry etch process. An alternative process flow can be the use of temperature controlled KOH wet chemistry to etch the handle layer (Fig. 5.3). This process is less expensive and faster compare to DRIE but care should be taken during the mask design process since KOH preferentially etches the <100> plane of silicon and produces a characteristic anisotropic V-etch profile with sidewalls that form a 54.7° angle with the surface [113]. Since geometry compensation is required for the KOH mask design process, the total number of devices per wafer would be noticeably low compare to the DRIE processed wafer (in other words, though expensive, DRIE processed wafers can yield more devices since they will need smaller foot print).

After the post handle etch process (either using DRIE or KOH), the diaphragm like structure (i.e., effective area of the MOS capacitor) can be very fragile depending on its area and the combined thickness of the "silicon device" and "buried oxide" layer. Thus, additional attention needs to be placed during the metallization process and further handling steps to avoid puncturing the samples. This might be one of the drawbacks of this SOI based process flow and will limit the use of a very thin silicon device layer to maintain the integrity of the structure. For metallization, a stack of layers can be used. The first layer that will be deposited directly on top of the buried oxide layer, will establish the flat-band voltage and the DC capacitance value of the pre-irradiated device, by employing its work function difference with the silicon device layer. A stack of chromium (alternatively titanium) and gold can be deposited on top of the first metal layer to improve the adhesion of the gold wire-bonds. For metal deposition, sputtering process would be preferable since it can maintain thickness uniformity and cover sidewalls better than some other deposition processes (e.g., e-beam, thermal evaporator etc.). Finally, the MOS capacitors can also be manufactured using epitaxial wafers to resolve the equivalent series resistance issue (can be an interesting future research work as well). A cross-section of such a device is presented in Fig. 5.4.

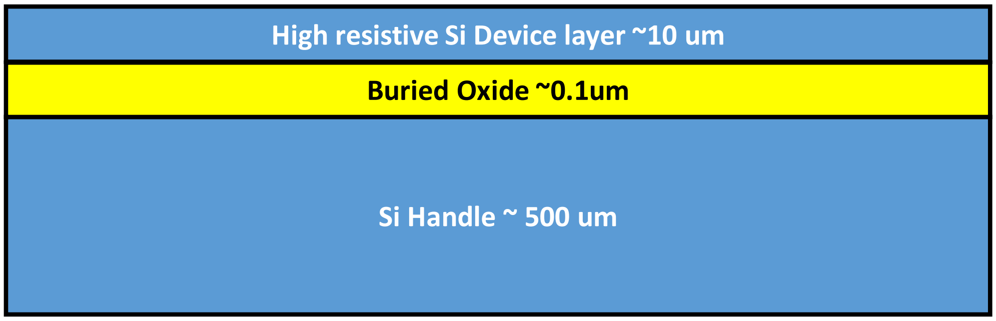


Fig. 5.2: General process flow of the MOS capacitor based radiation detection sensors using DRIE technique: (a) RCA cleaning of the SOI wafers

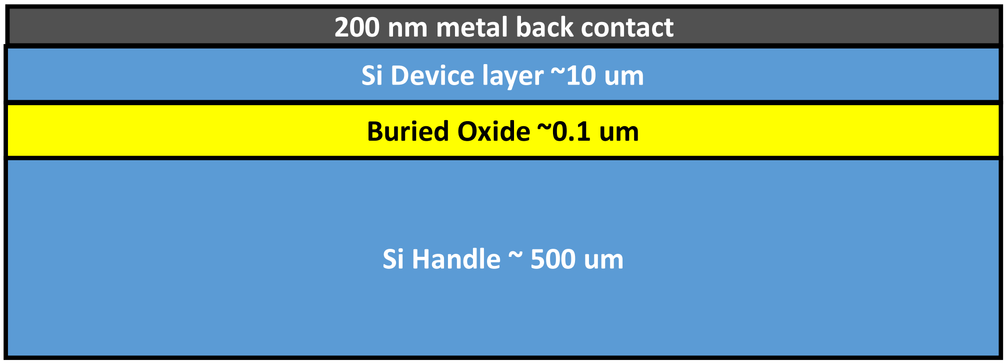


Fig. 5.2: (b) Deposition of the backside metal contact using e-beam/ sputterer.

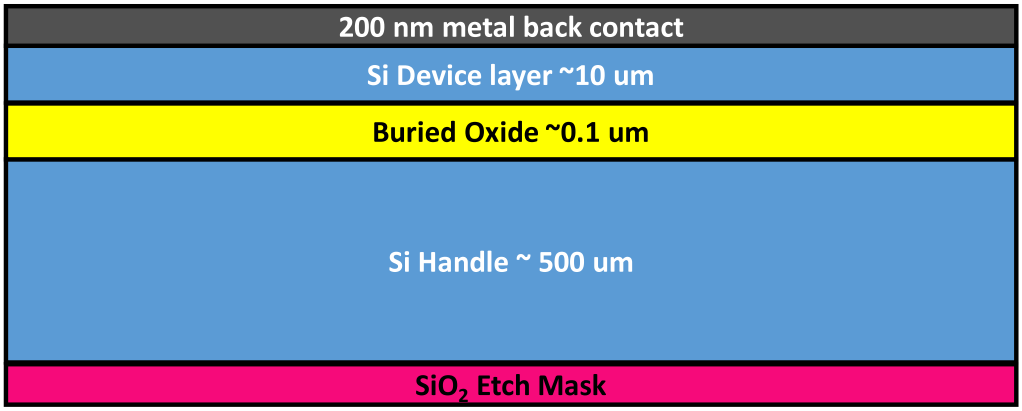


Fig. 5.2: (c) Deposition of oxide hard masking layer using PECVD process. (LPCVD process could provide better oxide quality but needs to be done before depositing the backside metal contact to avoid contaminating the furnace. Also, the oxide layer from the top device layer needs to be etched. Please note, silicon device layer thickness will be effected since portion of the silicon thickness will be converted to LPCVD oxide.)

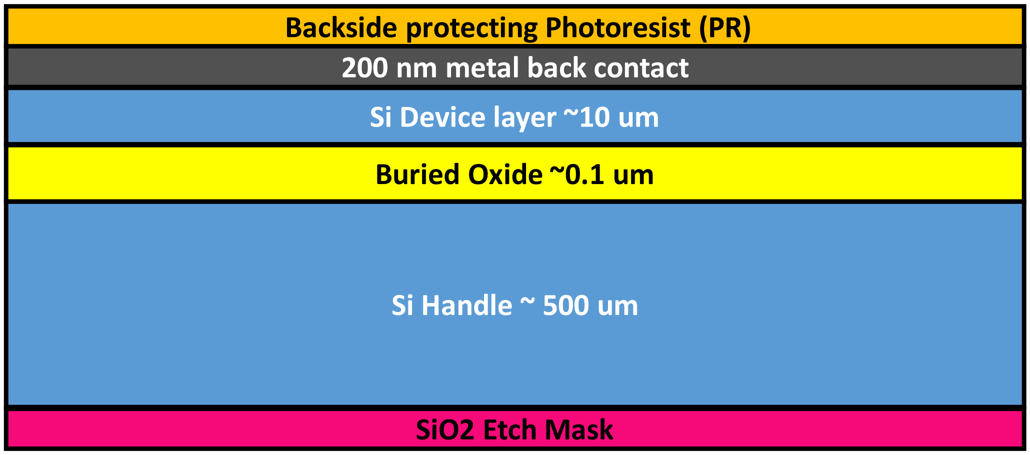


Fig. 5.2 (d): A layer of photoresist deposited on top of the backside metal contact to protect it from the subsequent process steps.

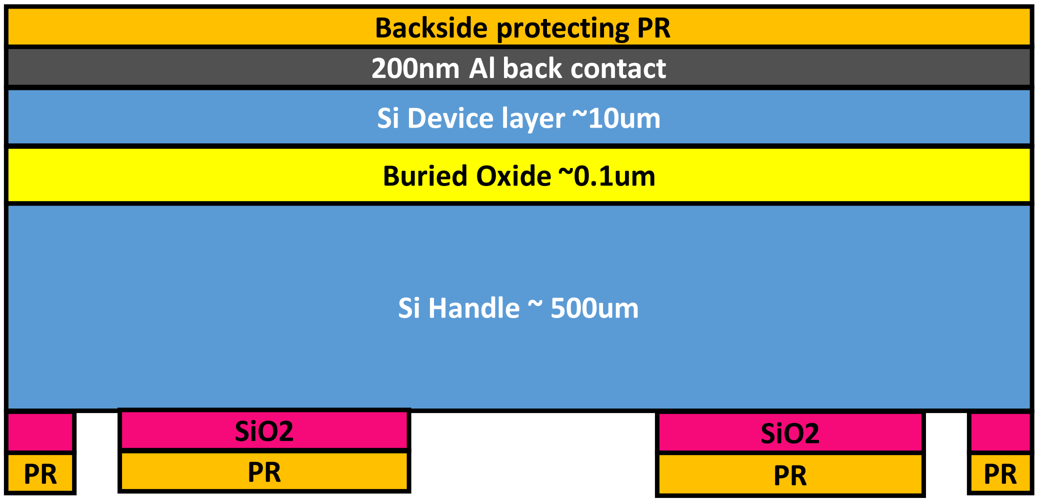


Fig. 5.2 (e): Photolithography step performed on the oxide hard masking layer to pattern it for the subsequent deep dry etching process. The mask used for this process to create the oxide opening (or MOS gate area) will eventually establish the MOS capacitance values. The oxide can be etched using dry etch processes.

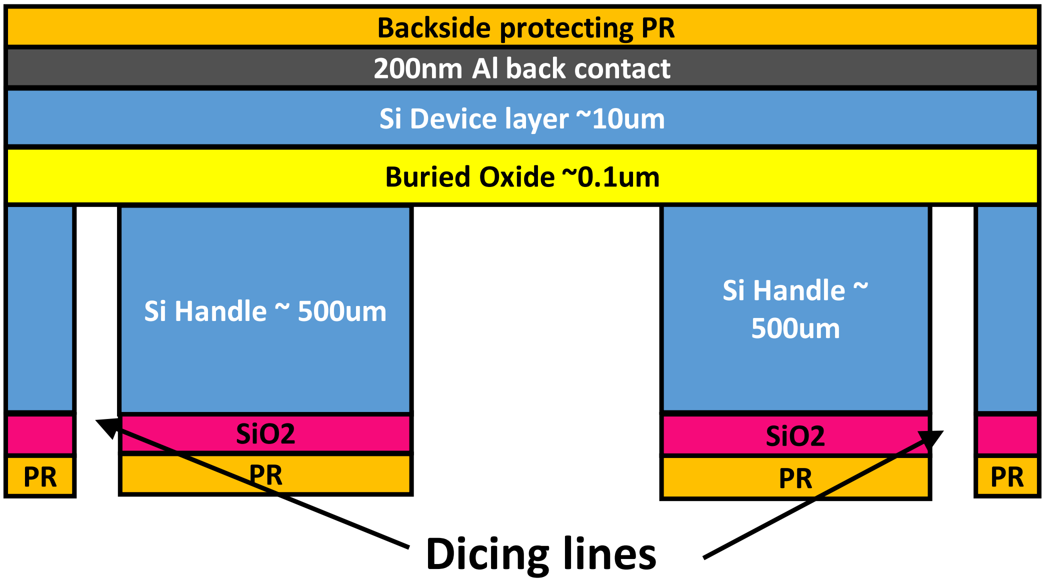


Fig. 5.2 (f): Deep reactive ion etching of the SOI handle layer all the way to the buried oxide. The process parameters need to be chosen carefully to improve selectivity and avoid etching the buried oxide layer which will establish the C_{max} value. The narrow openings on two side shows the possible dicing lines. The etch depth in these regions might not reach all the way to the oxide due to their small opening. But that should be fine since they will be used only for dicing.

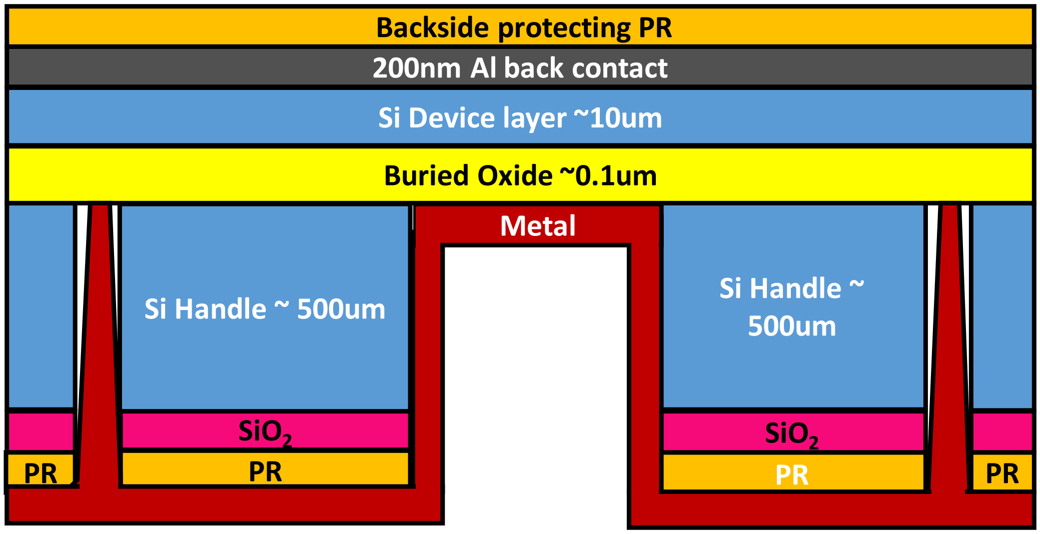


Fig. 5.2 (g): First layer of metallization on top of the buried oxide. Work function of this metal layer (along with the device layer work function) will establish the flat band voltage or pre-irradiated DC capacitance. Sputtering is recommended for better step coverage.

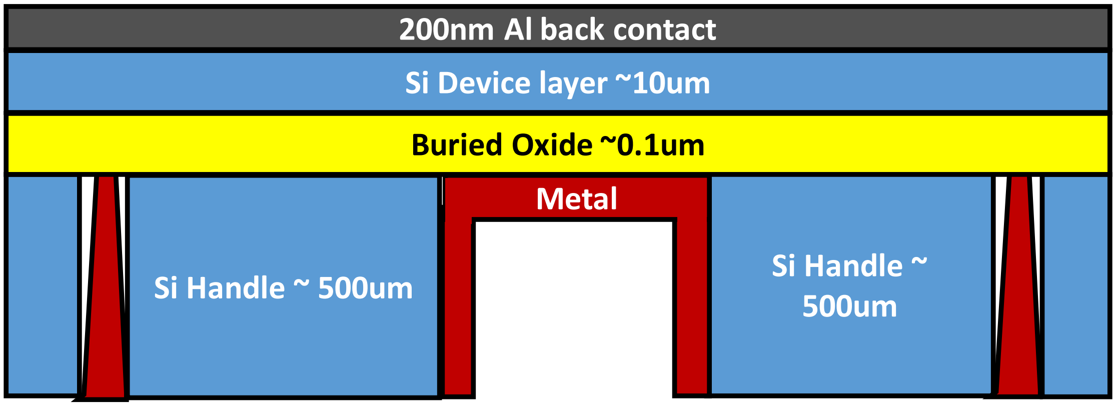


Fig. 5.2 (h): Removal of the photoresist protection layers (using stripper or acetone) and the oxide hard masking film (by dry etching).

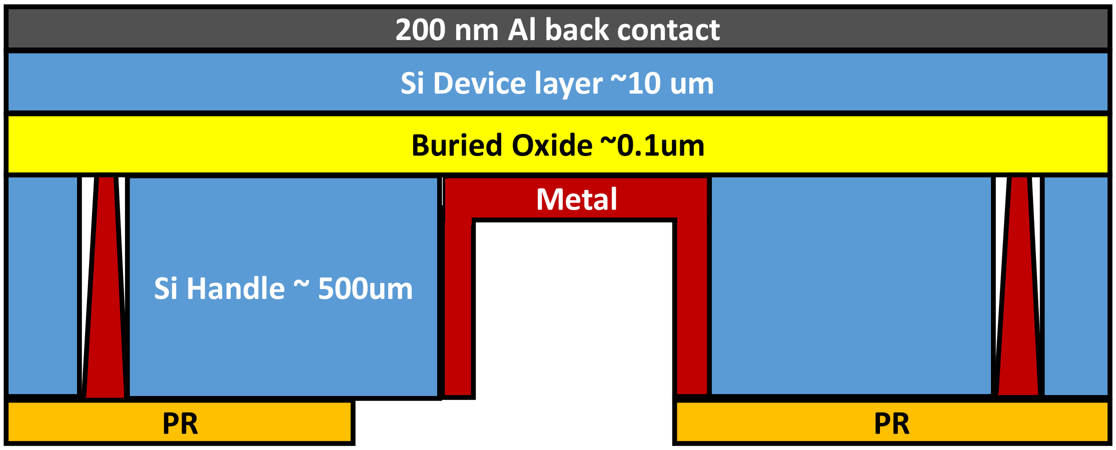


Fig. 5.2 (i): Photolithography performed for further metallization (i.e., deposition of chromium and gold).

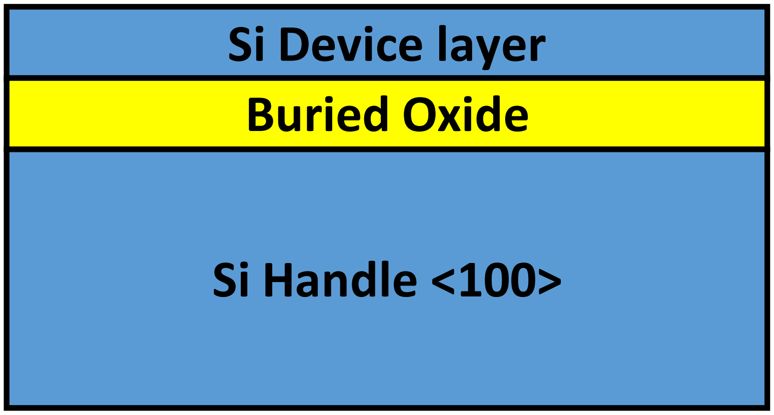


Fig. 5.3: General process flow of the MOS capacitor manufacturing using the KOH based wet chemistry. (a) Like DRIE, processing begins with RCA cleaning of the SOI wafers. The surface of the SOI handle should have <100> plane.

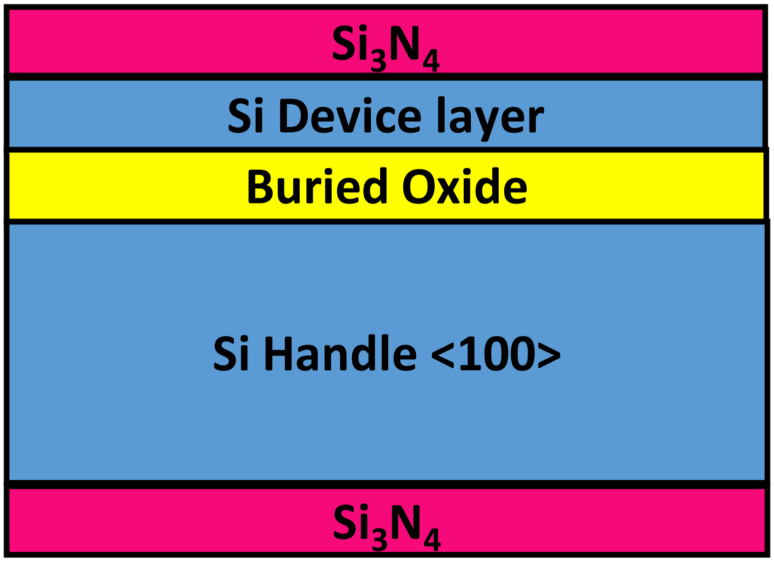


Fig. 5.3 (b): Deposition of LPCVD nitride which will act as the hard masking layer during the SOI handle KOH etch. It will also protect the top silicon device layer during the wet etching process.

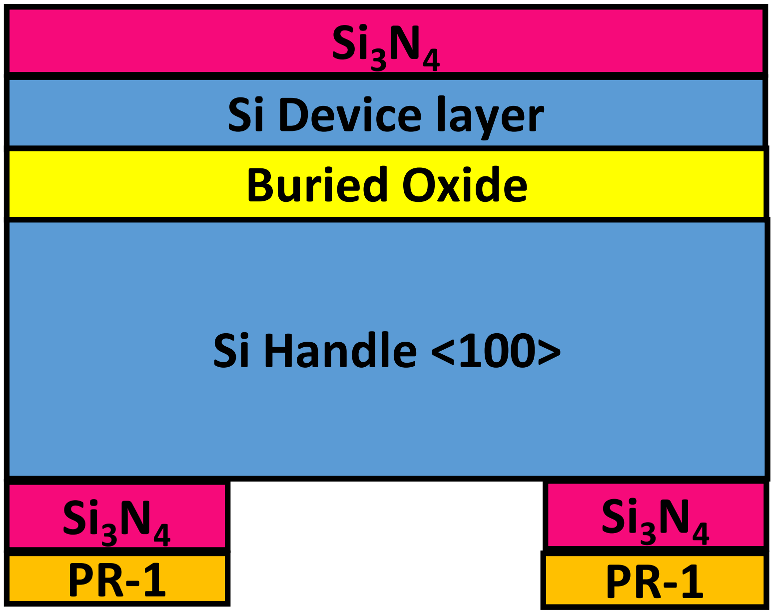


Fig. 5.3 (c): Photolithography to pattern the nitride hard masking layer. The mask used during the photolithography will eventually establish the MOS capacitors capacitance value.

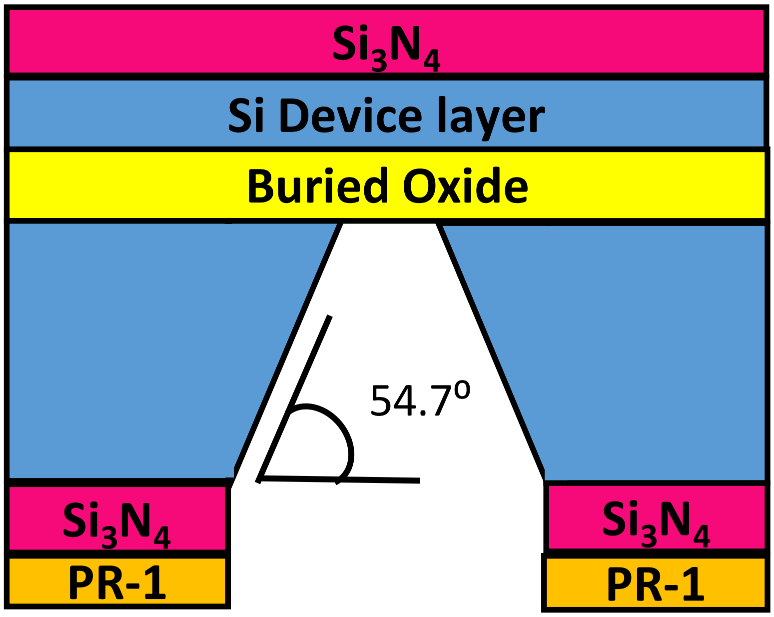


Fig. 5.3 (d): KOH etching of the handle layer to open the buried oxide layer. As previously mentioned, KOH preferentially etches the <100> plane of silicon and produces a characteristic anisotropic V-etch profile with sidewalls that form a 54.7 angle with the surface.

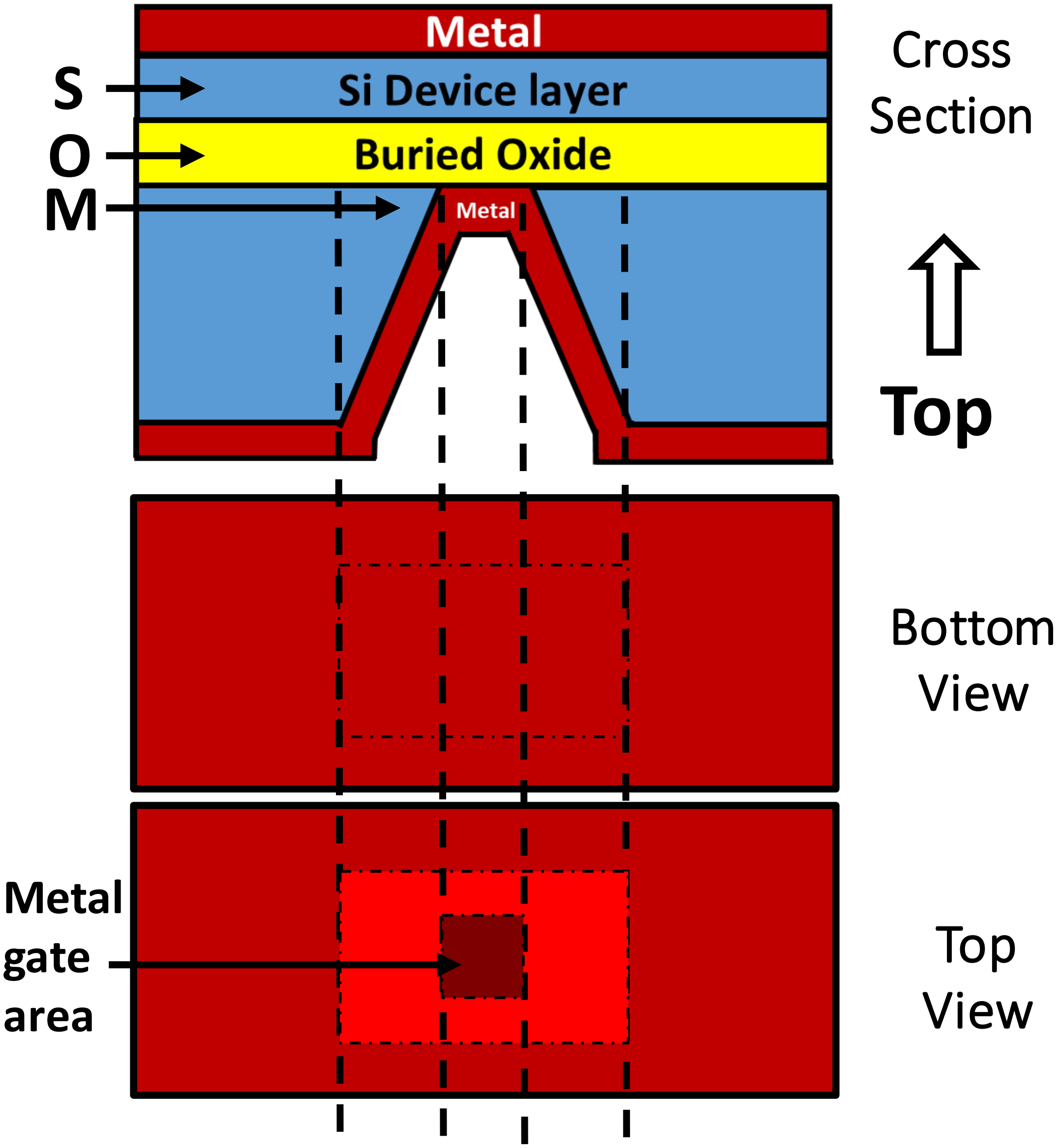


Fig. 5.3 (g): Side view/ cross-section (top), bottom (middle) and top view (bottom) of the completed device. Dark shaded region on the top view shows the actual metal gate area of the MOS capacitor.

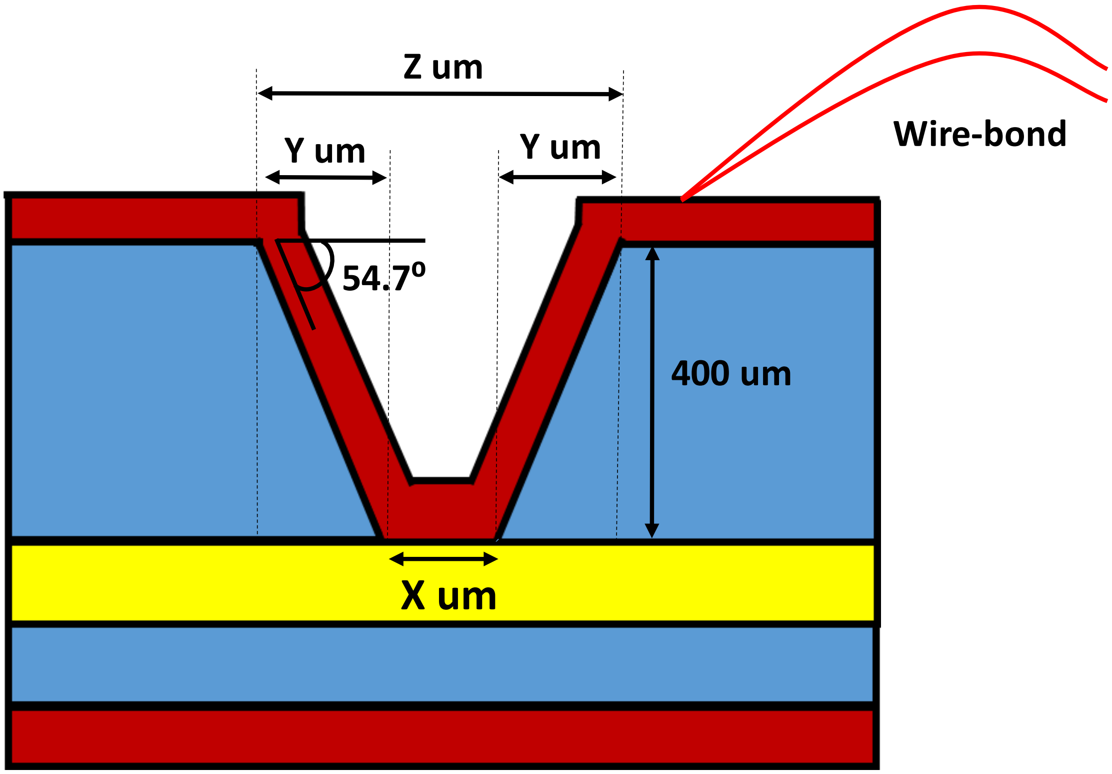


Fig. 5.3 (h): Geometric compensation needs to be considered during the mask design process. For instance, to make a MOS capacitor with a gate area of 100 µm x 100 µm using a SOI wafer that has 400 µm thick silicon handle layer, the actual mask gate area should be 666 µm x 666 µm. This clearly shows that the total number of devices per wafer would be far less compare to the DRIE processed wafers.

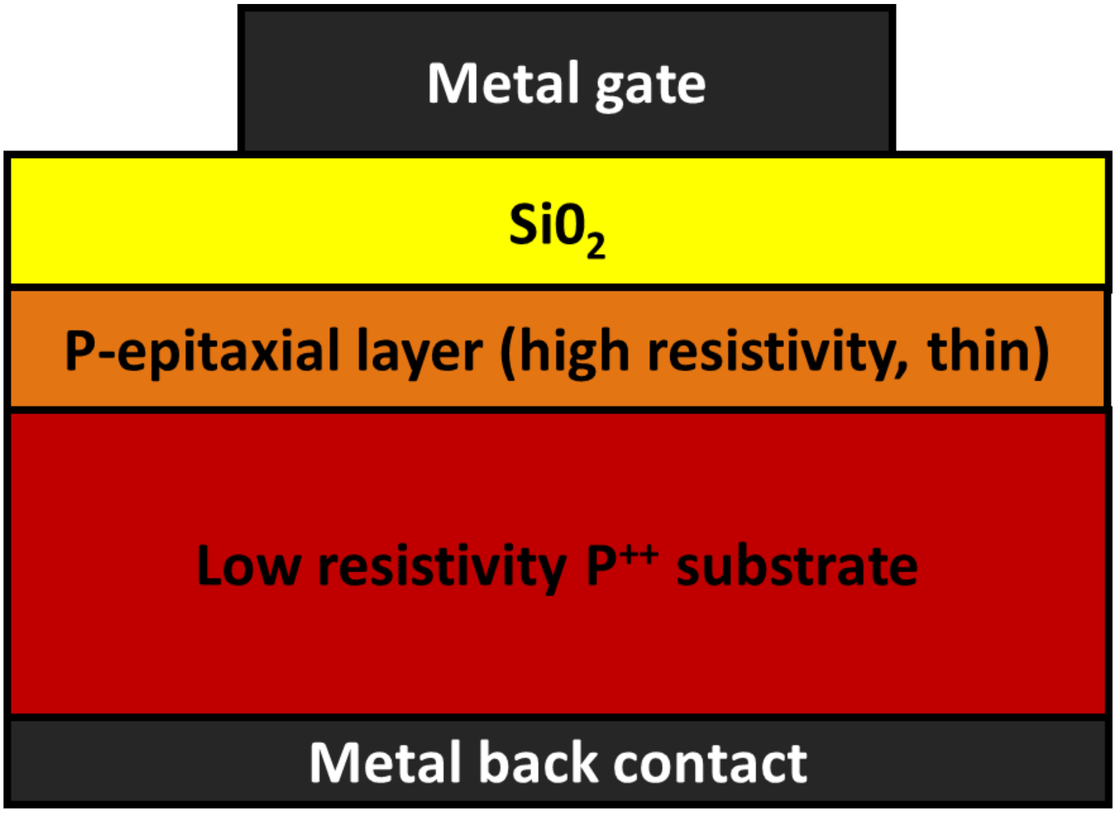


Fig. 5.4: Cross-section of MOS capacitor manufactured using a epitaxial wafer.

CHAPTER 6

SUMMARY

This dissertation work presents two innovative technologies for radiation sensing application. The metal-chalcogenide glass based sensor is manufactured on mechanically flexible polyethylene naphthalate substrate and can withstand reasonable amount of mechanical strain without degrading performance. This makes them ideal for applications that require installation of sensor devices on non-flat objects such as barrels or containers in nuclear decommissioning facilities or nuclear waste disposal stations where high radiation dose detection is normal. Since the sensor manufacturing process does not involve use of expensive photolithography or dry etch modules, the production cost is very low. In addition, this cost can be further reduced in commercial operations by utilizing roll-to-roll processing due to the use of flexible polymer or plastic substrate. Initial testing was performed on the prototype sensors to demonstrate the "radiation sensing" proof of concept using both UV light and gamma radiation. Next, mechanical and temperature stress testing was conducted to show the ability of these sensors withstanding certain amount of bending and elevated operating temperature without degrading performance. Then, focus was put on identifying design parameters that can be utilized to change the sensor performance characteristics such as limit of detection and dynamic range. Adjusting the limit of detection of the sensors is very important in order to make them suitable for a diverse range of applications from personal dosimetry to high dose monitoring systems in nuclear power generation stations or waste processing facilities. Therefore, optimization study was carried out to identify design criterions that can affect the total dose detection range. The parameters those were investigated include:

(i) electrode size (ii) electrode spacings (iii) ChG film thickness (iv) electrode film thicknesses and (v) novel material combinations (as electrode and ChG). Experimental results revealed that electrode spacing and film thicknesses of both electrode and ChG can greatly influence the limit of detection. By changing these parameters during design, the sensors performance can be tuned for diverse range of applications. Similarly, optimization study was performed for several group 11 metals (e.g., Cu, Ag and Au) and different ChG compositions (e.g., Ge_xS_{1-x} and Ge_xSe_{1-x}) as well. It turned out that Ag_Ge_xSe_{1-x} based systems are the best suitable material combinations to control sensor performance characteristics through changing the chalcogen content and are compatible to obtain scaling through changing physical parameters (i.e., spacings, film thickness etc.). An alternative novel structure is also presented in chapter 5 that can further reduce the limit of detection to significantly low TID levels without using any photolithography or etch modules, making them attractive for low dose sensing applications.

Aside from that, a proof-of-concept of MOS capacitor based wireless total dose sensing technology is also presented in chapter 4. Particularly, attention was given more on studying the impact of different design parameters related to the MOS capacitor structure and manufacturing process, that could affect their performance and radiation response. The parameters included: (i) oxide stack structure (ii) gate contact metal, (iii) annealing, (iv) substrate doping/ resistance, etc. For the gate metal, several options worked well such as (i) chromium (ii) chromium/ gold, (iii) titanium and (iv) titanium/ tungsten. To optimize bond wire inductances while connecting the MOS capacitor to the patch antenna, chromium/ gold gate contact was used as the material of choice and a thicker gate oxide structure was selected to allow use of larger metal gate for double gold wire bonding. Both the thickness and resistivity of substrate used to manufacture the MOS capacitor were realized to be the critical parameters to obtain an easily detectable resonant signature of the patch antenna within the desired frequency range. It was observed that a thick substrate with higher resistivity dampens the resonance of the loaded patch antenna (converted the LC oscillator into an LCR oscillator). Test results indicate that this issue can be greatly resolved by using an SOI wafer (alternatively epitaxial wafer) and a possible design of such a MOS capacitor structure is presented in chapter 5 which can be interesting future research work. Finally, arrays of loaded patch antennas were also measured for RCS response. As expected, higher return power levels were observed compared to individual antennas. Also, the resonant frequency was observed to be inversely proportional to the loading capacitance.

Both technologies presented here can be attractive for further research work and possible commercial applications due to their reasonable low manufacturing costs, small lightweight form-factor (to get dispersed in the field application as wide network of sensors) and instant easy readout operation.

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Appendix-A[1]

TCAD Modeling to Derive Design Guidelines for the MOS capacitors

(A) Small-signal model in NanoTCAD

As the first step, functionality of the small signal model was verified in CFDRC's NanoTCAD device simulation software [1]-[3]. These small signal calculations are based on the model proposed by Laux in [4], and essentially calculate the Y-parameter matrix for the device including the conductance and capacitance information for each electrode. In NanoTCAD, based on its architecture, a Fourier Decomposition (FD) based approach was employed to calculate the capacitance, which in turn relies on analysis of transient (step pulse) excitations of the contact voltage.

The test case used for initial evaluation was an oxide-only capacitor (thickness = 9.135 µm – due to mesh optimization, and area = 100 x 100 µm^2) for which simulation results could be verified against analytical calculations. In this test, both pulse and sinusoidal input signals were utilized to calculate the capacitance using NanoTCAD, and in both cases, the results matched analytical values very well.

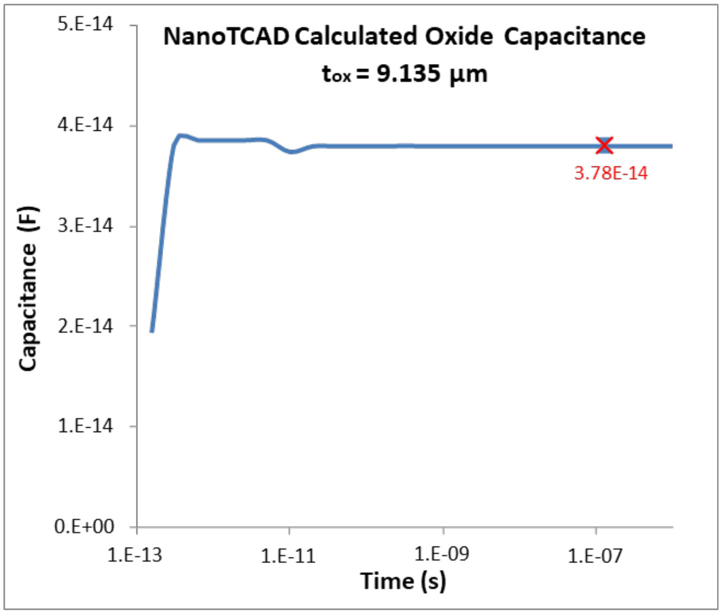

Fig. A.1: Test case: NanoTCAD calculated capacitance of an oxide-only capacitor with a thickness of 9.135 µm. The result matches the analytical value exactly.

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[1] The simulation results presented here were performed by CFD Research Corporation, Huntsville, AL (CFDRC) using the nanoTCAD simulation software and were guided by the experimental data generated at ASU and discussions with ASU researchers (i.e., author and his research advisers). The results are part of the jointly prepared DTRA STTR Phase I Final Report, Contract No. HDTRA1-15-P-0054. The author would like to sincerely thank Mr. Ashok Raman for his kind permission to use them.

The analytical value is calculated as: $C_{ox} = \varepsilon_0 \cdot \varepsilon_{SiO2} \cdot A_{ox}/t_{ox} = 3.78 \cdot 10^{-14}$ F, which matches the TCAD value exactly. This simple test helped to verify the procedure for subsequent use in calculating the capacitance of the MOSCAP.

(B) C-V Calculations for MOSCAPs with Single Oxide Layer

A TCAD model of the single oxide MOSCAP structure was developed which is based on representative (but close to actual) parameters. The corresponding schematic was shown earlier in Fig. 4.1(a).

The 3D TCAD model was generated for a single oxide layer with a thickness of 500 nm. The overall MOSCAP area was 100 μm x 100 μm, and for CV modeling purposes, the depth was assumed to be 9.135 μm (due to mesh optimization considerations). The substrate doping was p-type with a density of $2 \cdot 10^{15}$ cm^{-3} (corresponding to a resistivity of 8 Ω-cm). The gate and substrate contacts were assumed to extend over the entire top and bottom areas. Representative figures are shown in Fig. A.2, where a 3D model and the applied doping profile (color contours) can be observed.

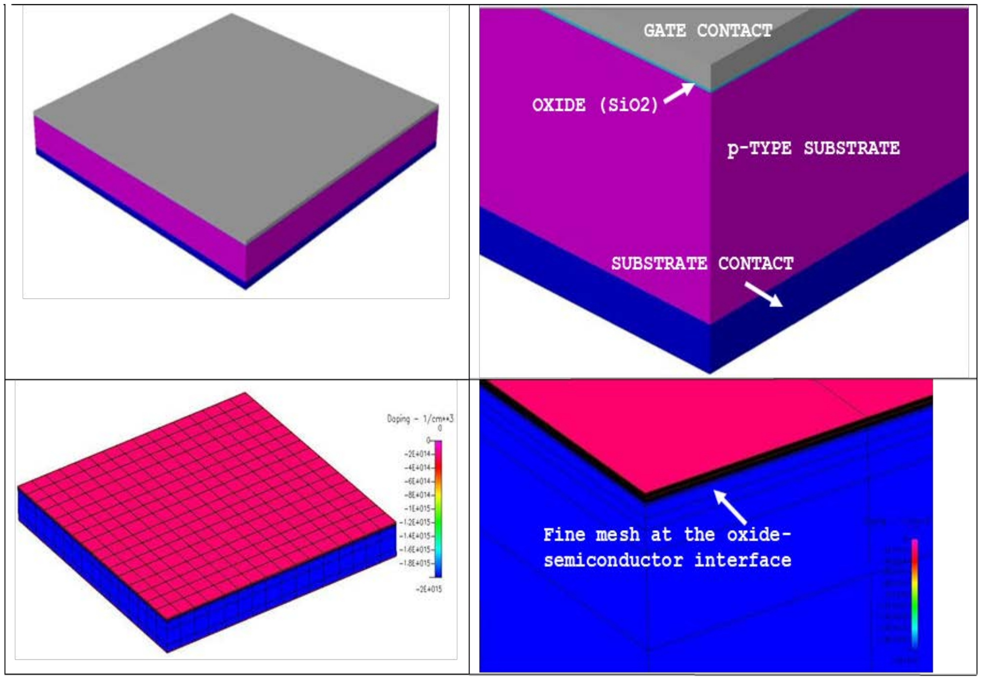


Fig. A.2: Selected details of the TCAD model developed using the NanoTCAD suite of tools for the single oxide layer MOSCAP structure (100 μm x 100 μm). The color contours represent net doping concentration (ND-NA). A p-substrate resistivity of 8 Ω.cm in Si translates into an acceptor doping density of ~ $2 \cdot 10^{15}$ cm^3.

The capacitance-voltage plot for the (pre-radiated) MOSCAP structure was computed using the small-signal model in NanoTCAD. The *CV plots were calculated at a frequency of 1 MHz* which is the high-frequency offered by the HP4284 LCR meter at ASU that has been used for MOS capacitor characterization.

The pre-radiation curve is shown in blue color in Fig. A.3, and it crosses the V_{sg}=0V line at $6.57 \cdot 10^{-13}$ F. The plot finally saturates at $6.9 \cdot 10^{-13}$ F at low V_{gs} values, thus matching the oxide capacitance as expected. Again, it need to be emphasized here that, *due to the early stage research in MOSCAP development, these calculations are not meant for comparison against a specific device, but rather to verify against analytical calculations when possible, and understand general trends and effects of parametric variations*.

As the next step, the impact of radiation on the C-V plot was analyzed via introduction of interface charges (positively trapped holes) at the oxide-Si interface. As clearly seen in the purple and green curves in Fig. A.3, a clear shift of the C-V plot is observed. A corresponding decrease of capacitance at Vsg=0V is also observed. This decrease in capacitance serves as the (passive) radiation signature. These simulation results demonstrate the same qualitative trends as prior measured MOSCAP results from 130-nm MOSCAPs [5].

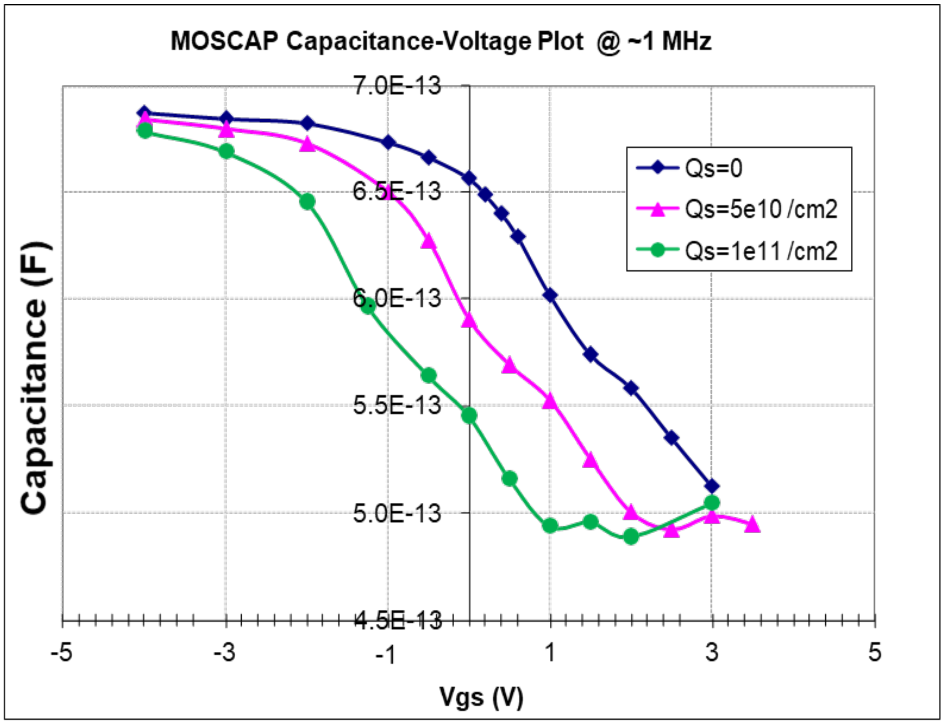


Fig. A.3: Capacitance-voltage plot at 1 MHz for the MOSCAP structure as calculated by NanoTCAD

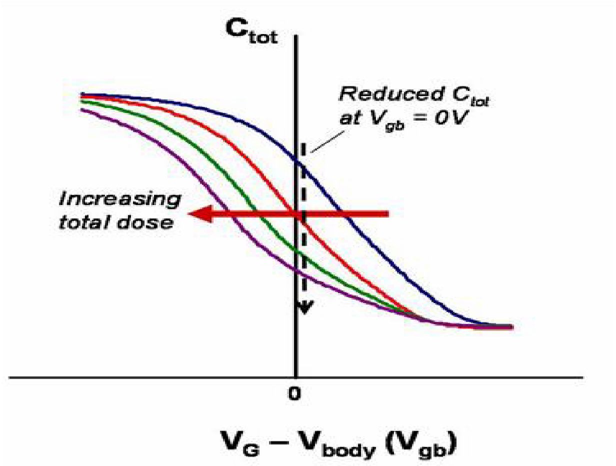


Fig. A.4: Prior measurements for total dose induced changes in the CV curve for a 130-nm MOSCAP showing expected trends for qualitative comparison [5]

The simulations performed here helped to verify the small signal modeling capability in NanoTCAD, and also test the basic performance of the representative MOSCAP, in terms of pre- radiation and post-radiation CV behavior (the latter using a simple interface sheet charge model). Next, a detailed oxide trapping model will be utilized to analyze the effect of different parameters on MOSCAP C-V behavior, with the aim of identifying representative parameter values (or trends) for higher sensitivity.

(C) Numerical Considerations in C-V Calculations

After the initial C-V calculations, the focus was put on further validation and improvement of the simulation procedure. In those simulations, some issues with consistency of the C-V plots at large gate voltages was observed. Also, simulations were noticed to be rather long for such a relatively simple device. Therefore, two strategies were pursued in order to validate the C-V computations and speed up the simulations: (i) study and refine the grid quality, and (ii) improvement and optimization of the time stepping procedure in the small signal model. Details are provided below.

(C-1) Simulation Grid Quality Studies

The grid quality near the interface between the oxide layer and the Si substrate is very important for MOSCAP simulations as carrier densities can vary strongly in the region adjacent to this interface especially at large (positive) gate voltages (inversion region for p-type substrate). Using CFDRC’s Micromesh software package several models were generated with different grid densities around the oxide-Si interface. Two representative examples are shown in Fig. A.5, with the first one being the base grid setup and the second one being the refined case. A series of simulations with different grids were then carried out. It was observed that using sufficiently small increments (~0.25–0.5 V) of the gate voltages to find DC solutions (which are then perturbed in the small signal model), well reproducible C-V plots could be obtained with good saturation properties for both fine and base grids, as shown in Fig. A.6. Thus, the grid convergence of the obtained results can be confirmed. Also, it can be realized that the base grid is sufficiently adequate to predict the MOSCAP device properties (such as capacitance) in the range of the conditions (gate voltages, doping profiles, etc.) of interest.

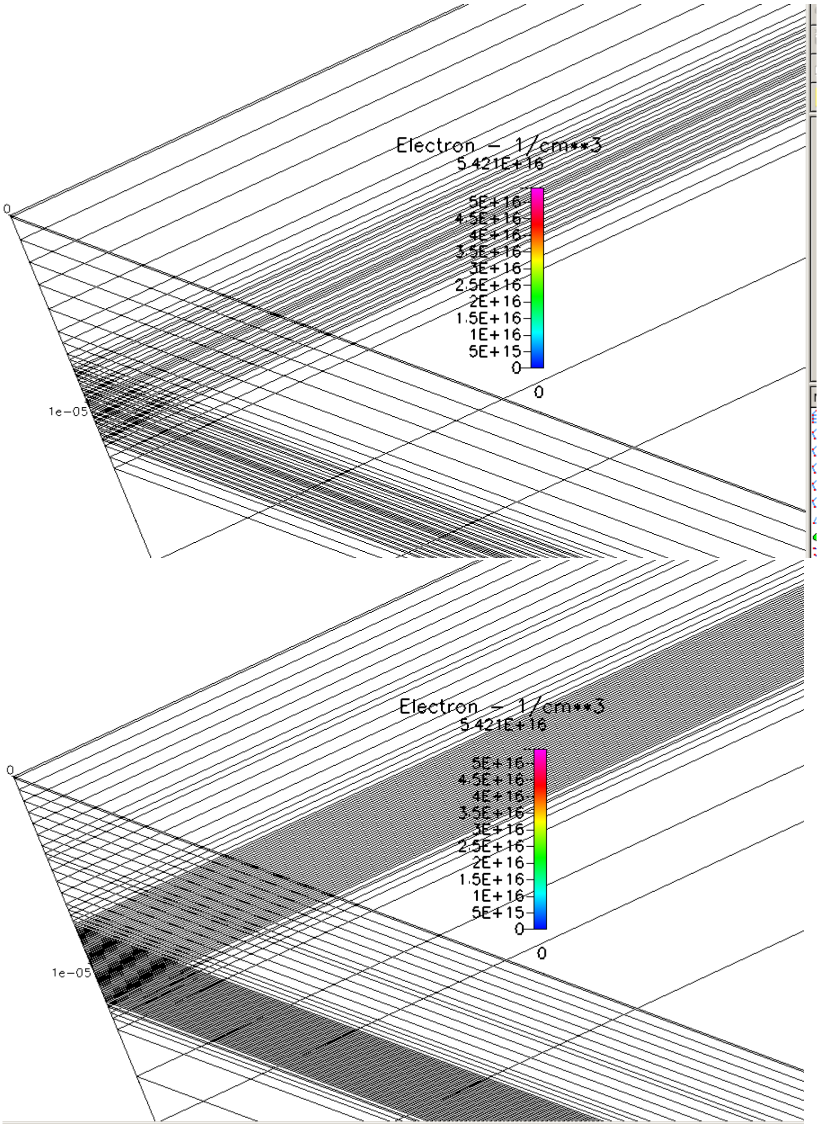


Fig. A.5: Comparison of the base (top) and fine (bottom) grids for MOSCAP simulations with NanoTCAD

(C-2) Time Step Refinement for CV Calculations

The second strategy was to study and fine tune the time stepping procedure. The small signal model implemented in NanoTCAD relies on the Fourier Decomposition (FD) analysis of a signal resulting from a step pulse excitation of the one of the terminal (contact) voltages (usually small amplitude step pulse excitation of 0.01 – 0.05 V are applied). *This small signal model allows the user to study both linear and non-linear*

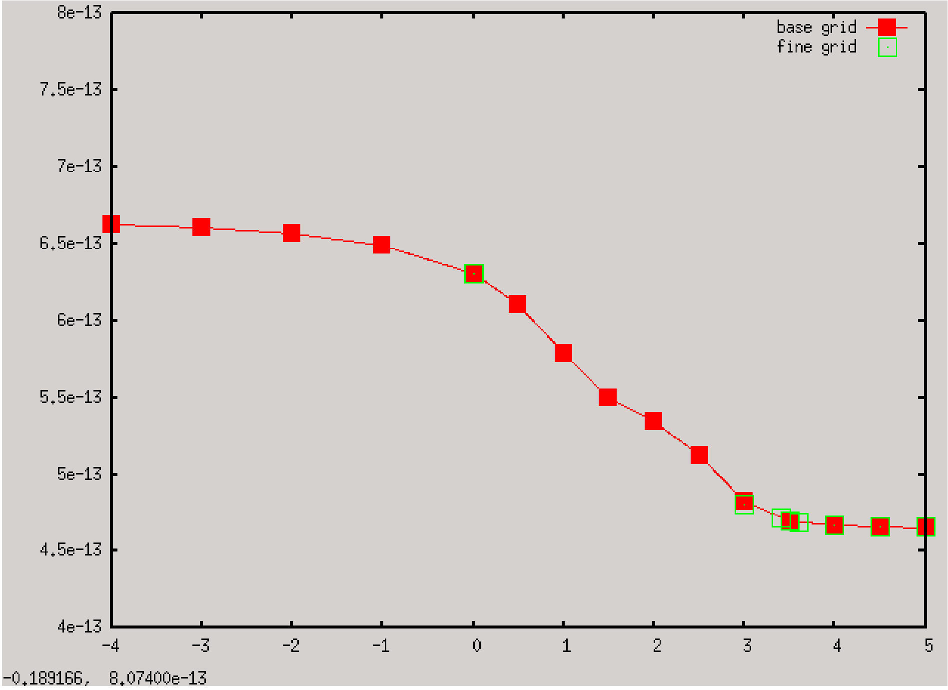


Fig. A.6: Capacitance-(gate) voltage plot at 1 MHz for the MOSCAP structure as calculated by NanoTCAD for base (filled red squares) and fine (open green squares) grids

system responses in a large range of frequencies (e.g., from 10^4 to 10^{14} Hz) at a time.

This is unlike the Laux small signal model [4] with system response linearization which allows the user to study only one frequency at a time. However, the NanoTCAD small signal model comes at an increased cost since it requires fully transient simulations to be performed until steady state is reached. As such, the time stepping algorithm is of primary importance for such simulations. The particularity of MOSCAP simulations is that the contact currents are zero at DC conditions. Only transient currents in such a device exist which comprise of the displacement current and carrier currents with the displacement current being dominant at large negative gate biases. Therefore, at larger negative biases when the p-type substrate is in accumulation, the MOSCAP capacitance is approximately equal to the oxide capacitance, and can be computed as $C = \varepsilon_0 \cdot \varepsilon_{SiO2} \cdot A_{ox}/d_{ox}$ which yields $C = 0.691 \cdot$pF. One can see in Fig. A.6 that the predicted saturated value of capacitance at negative Vg is lower than this theoretical value. Therefore, the attention was turned to the temporal dependence of the current signal after application of a step pulse (0.01 V amplitude). The time evolution using the base time marching scheme is shown in Fig. A.7 (top). The time dependence consists of the first strong current peak (time less than 0.1 ps) due to fast response to the applied step pulse, then a plateau (times less than 0.1 ns) and finally a quickly decreasing part which levels off at very small currents corresponding to DC conditions (times larger than 1 ns). It was observed that the initial current peak (time less than 0.1 ps) was not well described, and also too many unnecessary time steps were done at later times where much slower time evolution takes place. Thus, this time marching scheme was tuned by a) having smaller time steps at the initial phase of the current response to the step pulse (in order to resolve it better) and b) increasing the time step at a faster rate (in order to reduce the total number of time steps). This was done by using specialized scripts available in the NanoTCAD small signal model. The results of using such optimized time marching schemes are shown in Fig. A.7 (middle and bottom). One can see that the main current response peak is now well resolved. The base scheme (Fig. A.7, middle) allows much faster simulations (since it allows smaller number of time steps than the original scheme) with the refined scheme (Fig. A.7, bottom) being used for the final validation.

Using the optimized time marching scheme, well saturated C-V plots can be obtained (at both ends of the plot) with the saturation value at large negative gate biases, Vg, matching well the theoretical value, as can be seen in Fig. A.8. For these simulations, the base spatial grid was used which proved be adequate in earlier tests. One can also see in Fig. A.9 (open green squares) that the newly developed refined time marching scheme confirms the validity of the base time marching scheme (which in turn allows faster simulations).

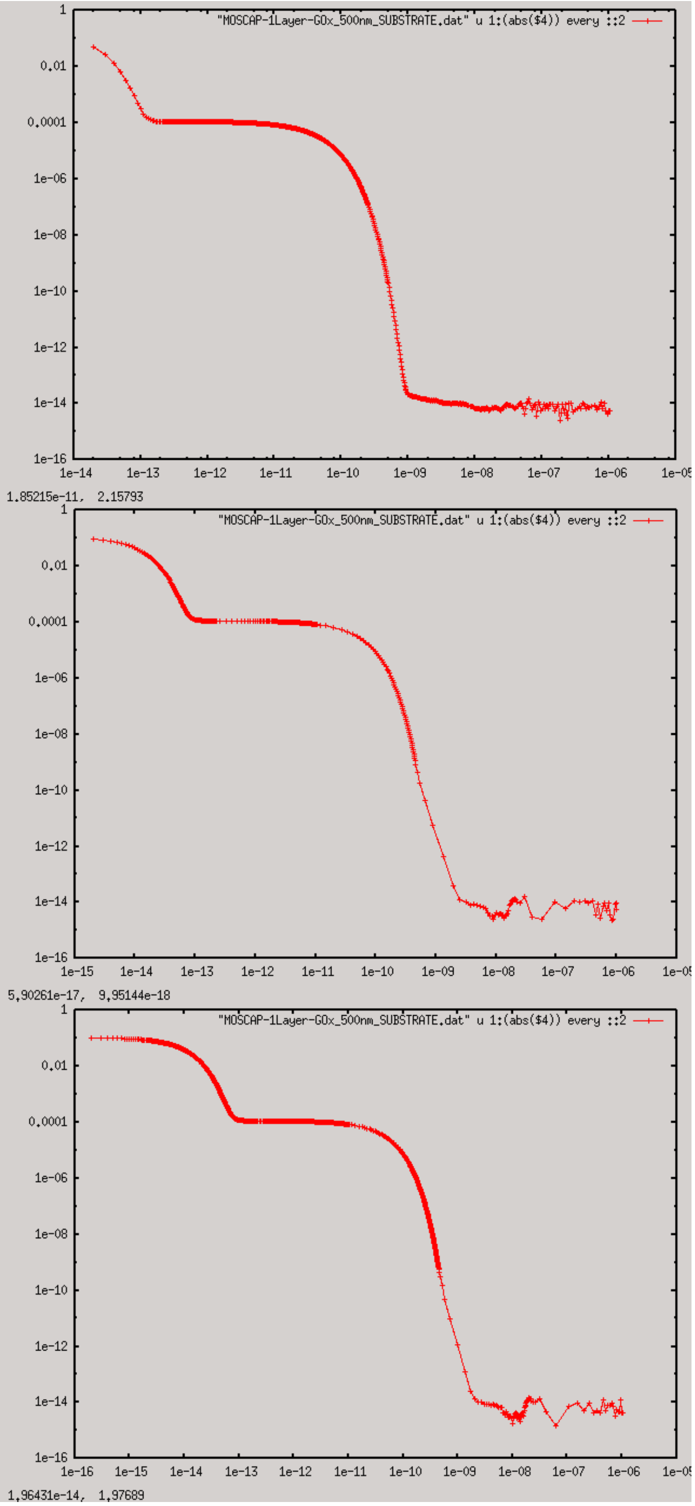


Fig. A.7: Substrate current vs time in log-log scale for 3 different time stepping methods: unoptimized (top); optimized base (middle); and optimized fine (bottom).

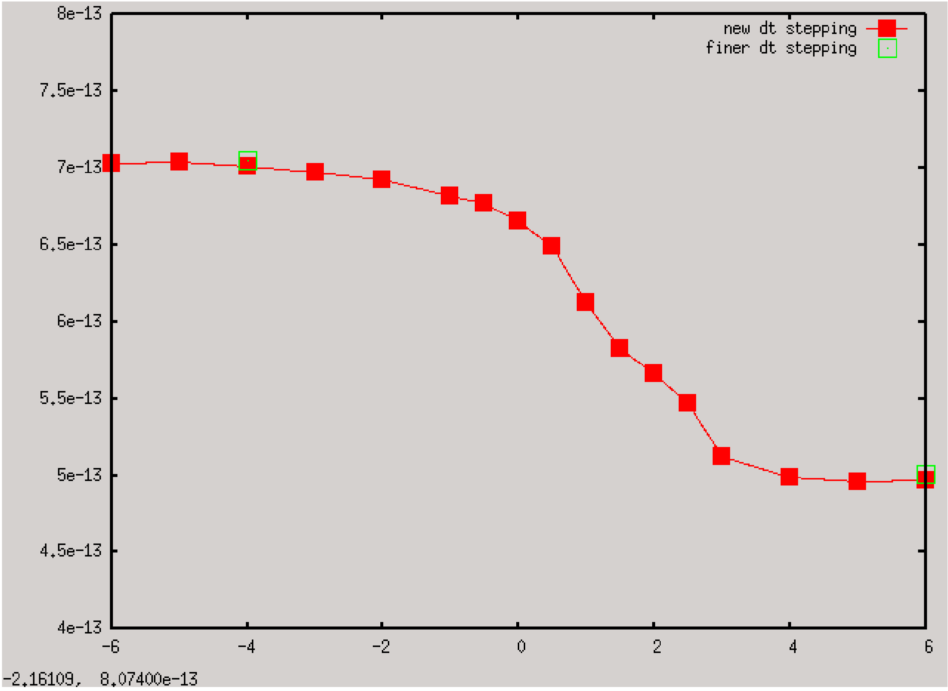


Fig. A.8: Capacitance-(gate) voltage plot at 1 MHz for the MOSCAP structure as calculated by NanoTCAD for base (filled red squares) and refine (open green squares) time marching schemes

Having obtained physically correct and numerically validated results, the newly developed schemes was applied to simulations with different values of the total dose represented in terms of a deposited surface charge (positively trapped holes) at the MOSCAP oxide-Si interface. These can be considered to be improved calculations over the results shown in Fig. A.3. The results using no surface charge and using two representative values of the surface charge of 5×10^{10} and 10^{11} cm^{-2} are shown in Fig. A.9. One can see a clear shift of the C-V plots for increasing surface charges, with the corresponding decrease of the capacitance at Vg=0V. One can also observe that well manifested saturations of the C-V plot at both large negative and positive Vg could be obtained for all values of the surface charge, with the saturated values at large negative values of Vg matching well the theoretical value.

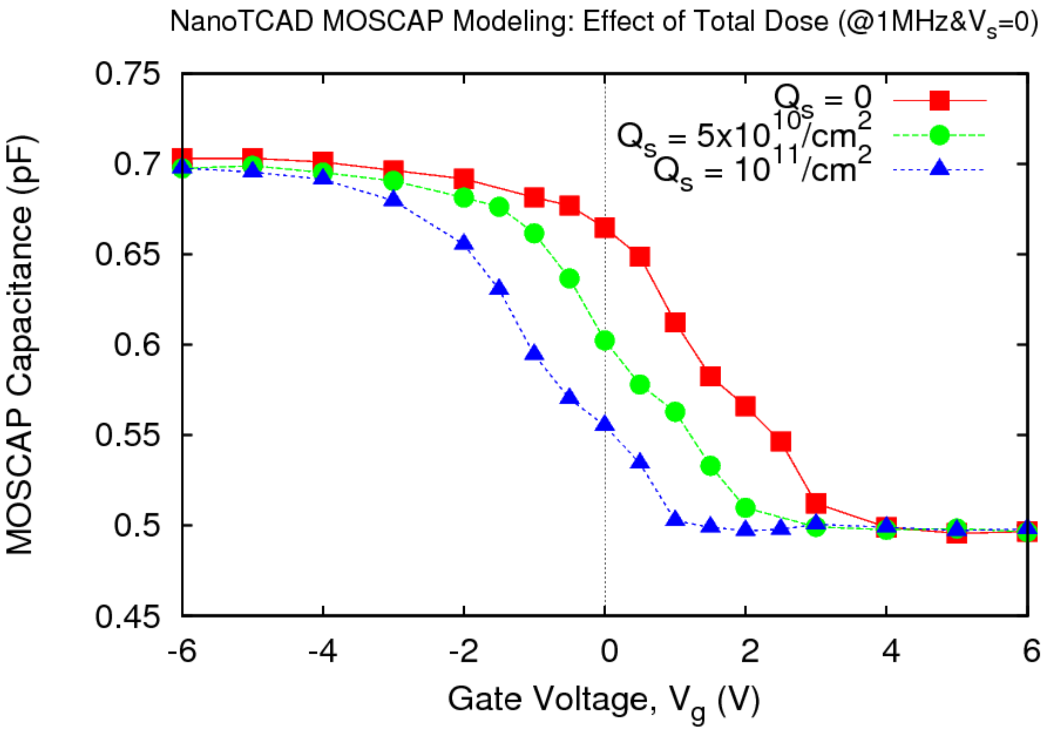


Fig. A.9: Capacitance-voltage plot at 1 MHz for the single-oxide MOSCAP structure as calculated by NanoTCAD for different values of total dose represented by the surface charge, Qs. Improved time stepping procedures were utilized to calculate the C-V curves

(D) Parametric Simulations of MOSCAP for Placement of Trap Precursors

The primary objective of this TCAD modeling task was to analyze parameters related to engineered trap precursors in the gate oxide stack for higher radiation sensitivity, and to derive initial design guidelines. The occupied trap precursors would be modeled as a sheet of positive charge in these calculations. The following modeling variations was considered as being of interest for the analyses at the current development stage of the project.

- Density of interface charge in 1-oxide layer (SiO_2 only)
- Density of interface charge in 2-oxide stack (high purity SiO_2 bottom layer and nitride top layer)
- Thickness of the high purity SiO_2 bottom layer in the 2-oxide stack, i.e., distance of the traps precursor layer from the Si interface

In order to observe clear variation of capacitance with radiation induced charge trapping in the engineered precursors (and not minimize trapping in processing induced trap locations), the two- layer stack has a high purity (“clean”) SiO_2 layer interfacing the p-Si substrate. This SiO_2/Si interface is assumed to have a constant, low sheet charge density of 1e10 cm^{-2}. On top of this pure oxide layer is a thicker silicon nitride layer, and the engineered trap precursors are preferentially located at the SiO_2/nitride interface. In the simulations, the density of the trap precursors was parametrically varied to determine their influence on MOSCAP response. These different models are schematically represented in Figs. A.10 and A.11.

(D-1) Effect of Trapped Charge Density in (Precursor Layer) in 1-Oxide Layer (SiO_2)

In this case, the SiO_2 layer thickness was 500 nm and three different charge densities were considered: Qs = 0, 5e10 cm^{-2}, and 1e11 cm^{-2}. The trapped precursor charge was applied directly at the SiO_2/Si interface (Fig. A.10-left). These calculations and results were presented earlier in Fig. A.9 and clearly show a stretching out of the CV curve (or a swing) with increasing trapped charge in the precursor location. These results agree qualitatively with prior findings in Fig. A.4 [5] and Martinez, et al. [6].

From these calculations, for this device structure, the following capacitance shifts at Vsg=0V (Table III) was observed. Recall that it is the capacitance shift at zero bias that makes this a passive sensor.

Table III. Effect of interface charge on zero bias capacitance in single-layer MOSCAP

	Capacitance at Vsg=0V	Δ Capacitance w.r.t Qs=0	Δ Capacitance (%)
Qs=0	6.647e-13 F	--	--
Qs=5e10 cm^{-2}	6.024e-13 F	6.23e-14 F	9.37 %
Qs=1e11 cm^{-2}	5.553e-13 F	1.094e-13 F	16.46 %

(D-2) Effect of Trapped Charge Density in (Precursor Layer) in 2-Oxide Stack (SiO_2_+ Nitride)

In this set of simulations, the MOSCAP had a thin (20-nm) clean SiO_2 layer with a low process induced charge of 1e10 cm^{-2} at the SiO_2/Si interface. On top of this was a thicker (480-nm) layer of silicon nitride with varying precursor densities at the SiO_2/nitride interface. This implies that the radiation induced chare trapping occurs at a distance of 20-nm from the Si interface, unlike the previous single-oxide layer.

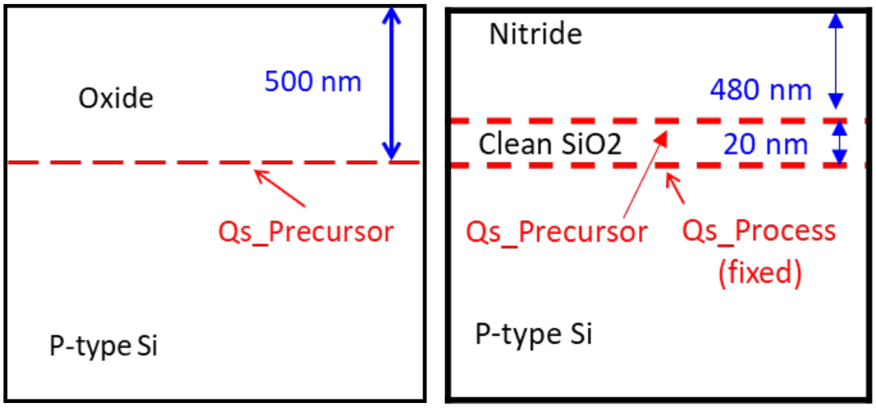


Fig. A.10: Schematic representation of trap precursor location in MOSCAPs with single-oxide layer (left) and two-oxide stack (right). In each case, the Qs_precursor value (i.e., interface sheet charge density) was parametrically varied in the simulations to calculate the effect on C-V response.

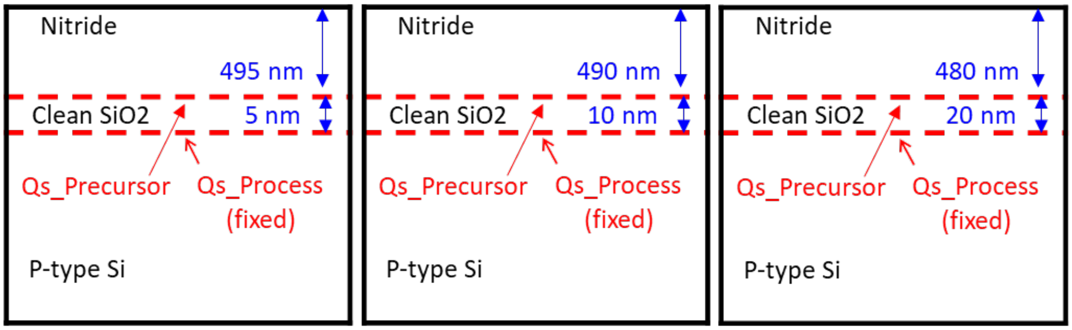


Fig. A11: Schematic representation of three different thicknesses for the high purity (clean) SiO_2 layer with the nitride layer on top. In each case, the total oxide stack thickness was 500 nm. The Qs_process value was fixed at 1e10 cm^{-2} in all cases, while the Qs_precursor was parametrically varied to determine effect on C-V response

For this device structure, the variation in C-V plots with interface charge is shown in Fig. A.12. A similar trend is observed as in the single-layer oxide device earlier, i.e., with increasing radiation (i.e., interface charge), the capacitance at Vsg=0V clearly decreases. The numbers for capacitance shifts at Vsg=0V are presented in Table IV.

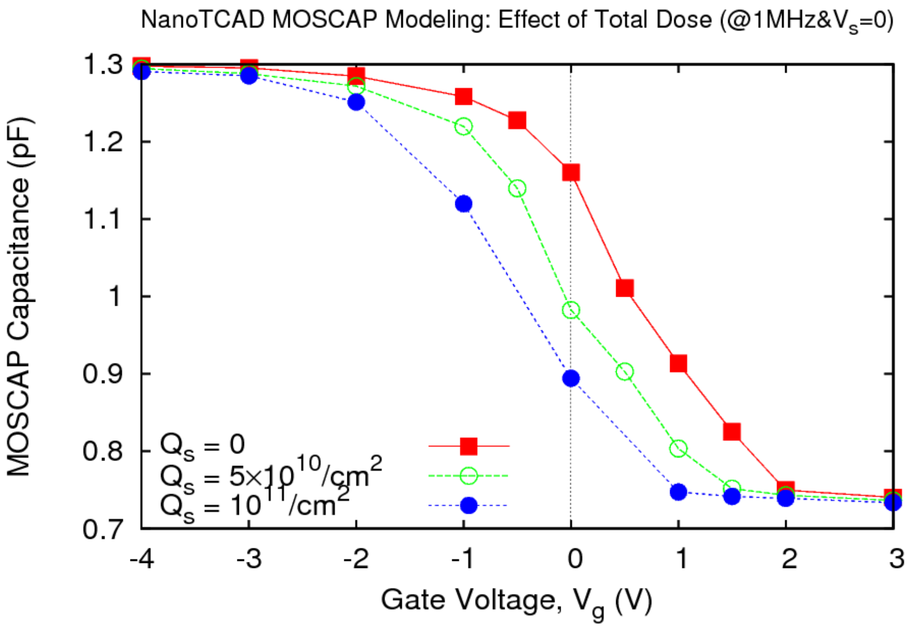


Fig. A.12: Capacitance-voltage plot at 1 MHz for the two-layer oxide MOSCAP structure as calculated by NanoTCAD for different values of total dose represented by the surface charge, Qs

Table IV. Effect of interface charge on zero bias capacitance in 2-oxide stack MOSCAP

	Capacitance at Vsg=0V	Δ Capacitance w.r.t Qs=0	Δ Capacitance (%)
Qs=0	1.16e-12 F	--	--
Qs=5e10 cm^{-2}	9.824e-13 F	1.776e-13 F	15.31 %
Qs=1e11 cm^{-2}	8.943e-13 F	2.657e-13 F	22.91 %

Additionally, at negative Vg, the p-type Si substrate is in accumulation, implying that the MOSCAP capacitance is equal to the oxide stack capacitance. Considering the oxide stack as two capacitances in series (SiO_2 of 20-nm thickness and nitride of 480-nm thickness), an analytical oxide stack capacitance of 1.28e-12 F is obtained. It can be seen from Fig. A.12 that *this value is well reproduced by the C-V calculations*.

(D-3) Effect of SiO2 Layer Thickness in 2-Oxide Stack (SiO$_2$ + Nitride)

The next set of simulations was to analyze the impact of distance of the trap precursor layer from the Si interface. Since the trap precursor layer was located on top of the clean SiO$_2$ layer (at the SiO$_2$/nitride interface), this impact of distance was modeled by simply varying the thickness of the clean SiO$_2$ layer, as shown in Fig. A.11. In all these simulations, the MOSCAP had a clean SiO$_2$ layer of three different thicknesses (5, 10, and 20-nm), all with a low process induced charge of 1e10 cm^{-2} at the SiO$_2$/Si interface. On top of this was a thicker layer of silicon nitride with a constant precursor density of 5e10 cm^{-2} at the SiO2/nitride interface. The CV curves for all three cases are shown in Fig. A.13 below.

At negative Vg values, the MOSCAP capacitance is expected to be equal to oxide stack capacitance. *It can be seen that the calculated capacitance matches theoretical values very well for the 2-oxide stack*: 1.28e-12 F (for 20-nm SiO$_2$ thickness), 1.304e-12 F for 10-nm SiO$_2$, and 1.315e-12 F for 5-nm SiO$_2$.

For this device structure, the following capacitance shifts at Vsg=0V (Table V) can be observed. As expected, thicker oxides are associated with lower capacitance. For the selected oxide layer thicknesses and interface charges, the change in capacitance is not observed to be significant.

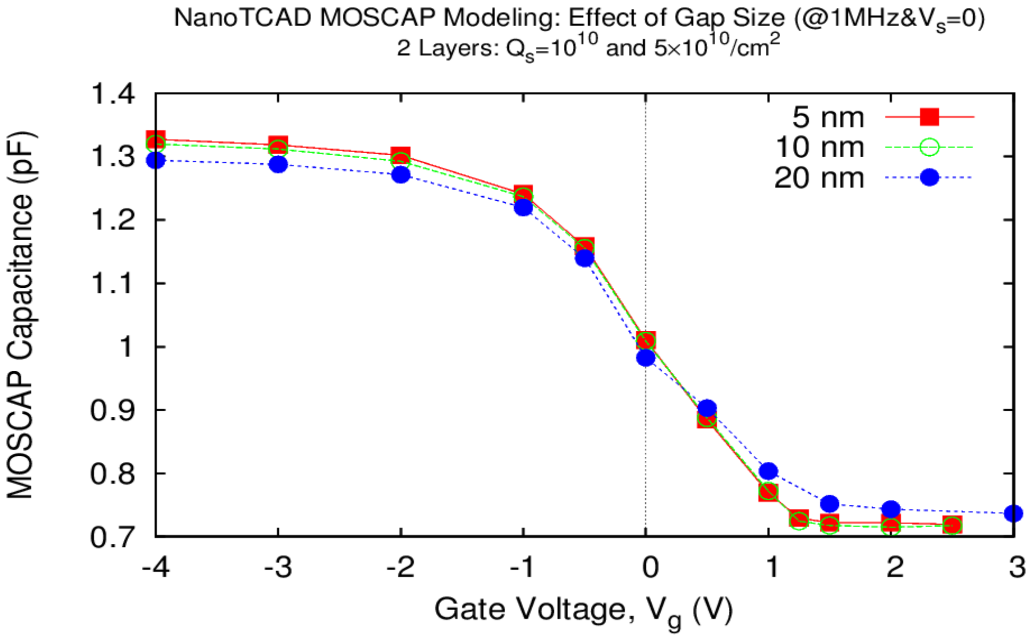


Fig. A.13: Variation of CV response of MOSCAPs with varying clean SiO$_2$ layer thickness. In all cases, the process-induced charge density at the SiO$_2$/Si interface was maintained at 1e10 cm^{-2}, and the trap precursor density at the SiO$_2$/nitride interface was maintained at 5e10 cm^{-2}

Table V. Effect of SiO_2 thickness (i.e., distance of precursor layer) on zero bias capacitance in 2-oxide stack MOSCAP. In all cases, Qs_process = 1e10 cm^{-2} and Qs_precursor = 5e10 cm^{-2}.

	Capacitance at Vsg=0V	Δ Capacitance w.r.t 20-nm thickness	Δ Capacitance (%)
SiO_2 = 20 nm	9.824e-13 F	--	- -
SiO_2 = 10 nm	1.009e-12 F	2.66e-14 F	2.71 %
SiO_2 = 5 nm	1.010e-12 F	2.76e-14 F	2.81 %

Appendix-B[2]

Electromagnetic modeling to derive design guidelines for a single MOSCAP loaded folded patch antenna structure

The objective of this effort is to capture the resonant frequency of the capacitively loaded patch antenna (LC oscillator) – close to the center of the target frequency window of 3-8 GHz. This is observed as a sharp peak in the RCS plot. Ionizing radiation changes the capacitance, and therefore, the resonant frequency, and this change can be used to back-calculate the received incident radiation. Based on experimental observations, several design parameters were identified that can affect the performance of the patch antenna. Numerical simulations were performed to understand their impact on the response curve (RCS). In addition, parameter ranges for optimal performance are also identified. These parameters included: (i) capacitance of the MOSCAP, (ii) MOSCAP size (iii) inductance of the bond wires connecting the MOSCAP to the patch antenna, (iv) resistance of the MOSCAP substrate, (v) number of bond wires, (vi) bond wire length, (vii) number of through hole vias, (viii) angle of reflected signal, (ix) array response vs. single patch antenna, and so on. For the patch antenna structure described in chapter 4, the parameter values to obtain a clear resonance in the 3-8 GHz frequency range (close to the center value of 5.5 GHz) were calculated as shown in Table B.1 below:

Table B.1. Parameter ranges calculated for components of the patch antenna structure used in the Phase I proof-of-concept demonstration, to obtain resonance in the target frequency window of 3-8 GHz

Parameter	Value
MOSCAP capacitance (without wirebonding)	0.2 - 0.7 pF
MOSCAP capacitance (with wirebonding, for bond wire inductance = 4.912 nH)	0.025 – 0.31 pF
MOSCAP substrate resistance (for MOSCAP ≤ 0.15 pF)	≤ 50 Ω
Bond wire inductance (for MOSCAP 0.7 pF)	0 – 1 nH
Number of bond wires	2

It can be observed that the optimal values of the components are interdependent. Therefore, the results can also be presented in the form of the following trends that serve

---

[2] The simulation results presented here were performed by CFD Research Corporation, Huntsville, AL (CFDRC) using the ANSYS HFSS simulation software and were guided by the experimental data generated at ASU and discussions with ASU researchers (i.e., author and his research advisers). The results are part of the jointly prepared DTRA STTR Phase I Final Report, Contract No. HDTRA1-15-P-0054s. The author would like to sincerely thank Mr. Ashok Raman for his kind permission to use them.

as design guidelines:

- → For a given bond wire inductance, higher MOSCAP capacitance moves the resonance to lower frequency values, and vice versa (ref. Fig. B. 17).
- → For a given MOSCAP capacitance, higher bond wire inductance moves the resonance to lower frequency values, and vice versa (ref. Fig. B. 26).
- → For a given MOSCAP capacitance and bond wire inductance, higher MOSCAP substrate resistance (which changes the LC to an LCR oscillator) leads to widening and decrease of the resonance peak. No frequency shift is observed though (ref. Fig. B. 36 and Fig. B. 37).

A detailed description of the electromagnetic modeling of the patch antenna and its components is provided in the following sections.

(A) CLFPA Design and Problem Settings

The geometry generated for the capacitively loaded folded patch antenna (CLFPA) consists of 3 copper patches (width 0.035 mm) placed on top and bottom of a Rogers RO4003 substrate (relative permittivity of 3.55) of 25×25 mm in size and 1.54 mm in height (Fig. B. 1). The bottom (size 7.75×16.75 mm) and the smaller of the top copper patches are connected via 5 copper through holes of 0.25 mm in radius. The two top copper plates are connected via a capacitor (e.g., MOSCAP) thus resulting in capacitive loading.

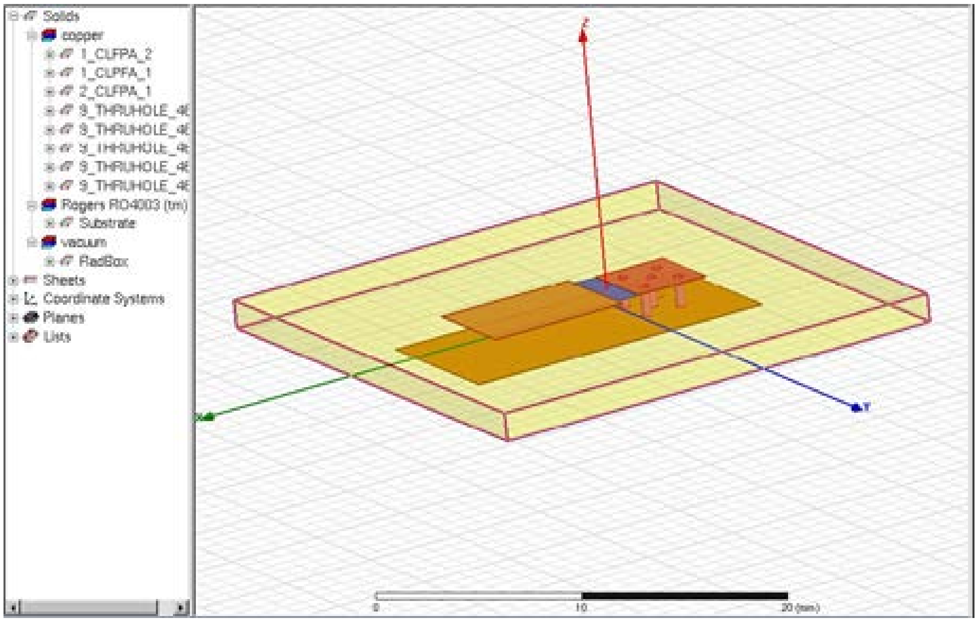


Fig. B. 1. General geometry overview of CLFPA setup with 5 through holes and Rogers RO4003 substrate. The two top copper patches are connected via a capacitor (gray surface).

Around the CLFPA a box of size 200×200×200 mm was created with “radiating only” boundary conditions, as shown in Fig. B. 2. The box is large enough to make sure, it does not affect the solution. The Radiation Boundary is used to create an open model in HFSS. According to the HFSS manuals, it should only be applied to outer faces of the solution space. If simulating an antenna, the radiation boundary should be placed at least a quarter wavelength away from any radiating surface.

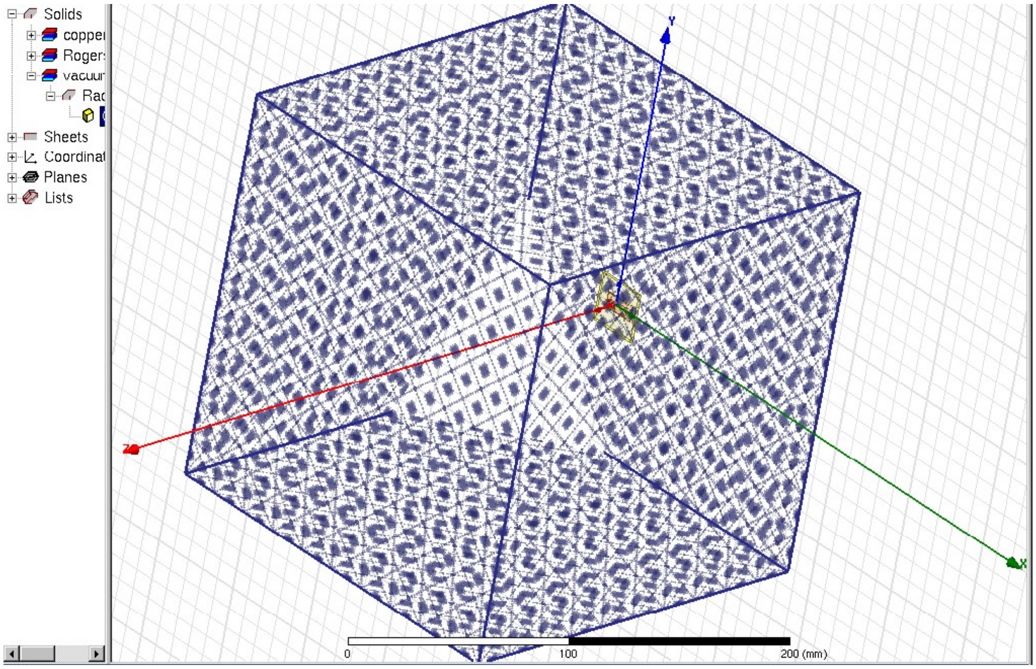
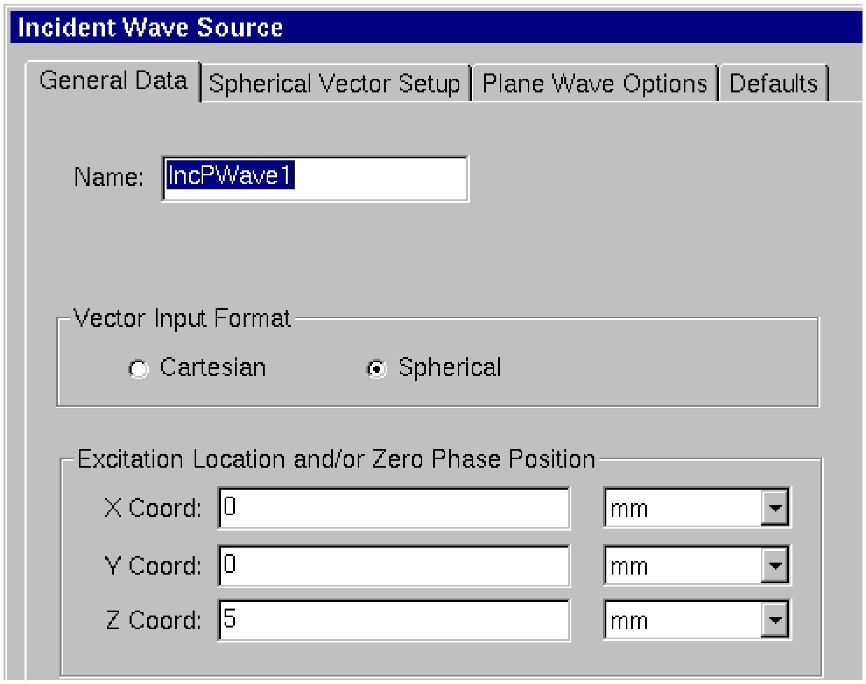


Fig. B. 2. Radiating only boundary box for modeling of CLFPA

The CLFPA antenna is irradiated by a spherical incident wave located 5 mm from the substrate, as seen in Fig. B. 3. The CLFPA is modeled as a driven solution with an 8 GHz solution frequency with lambda- refinement of the computational mesh, see Fig. B. 4. The mesh adaptation with 0.1 maximum delta-energy accuracy is used with a maximum number of passes of 12 and 30% maximum refinement per pass. The direct matrix solver is used, see Fig. B. 4.

Since the simulations can be long, specialized HPC settings were used by allowing the job to be run on 8 CPUs, as shown in Fig. B. 5. The list of the CLFPA design parameters is summarized in Fig. B. 6 and the frequency sweep is specified as shown in Fig. B. 7. Linear step frequency sweep setup from 3.5 to 8 GHz with step size of 0.1 GHz were used (sometimes step size is decreased in order to get better RCS resolution, but the value of 0.1 GHz was sufficient in most of the simulations). The choice of the studied frequency window is such that the RCS signal of a detectable level (> -40 dBsm) is predicted in that window.



Name: IncPWave1

Vector Input Format

○ Cartesian ● Spherical

Excitation Location and/or Zero Phase Position

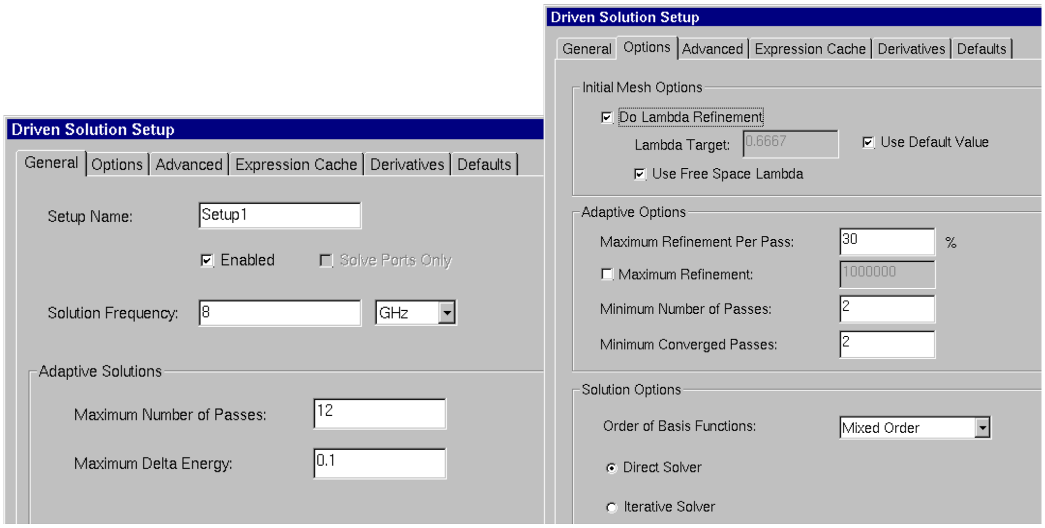
X Coord: 0 mm

Y Coord: 0 mm

Z Coord: 5 mm

Fig. B. 3. Incident wave source setup for CLFPA modeling

When setting up the CLFPA geometrical features special attention was paid to the design capabilities of the HFSS software. In particular, special variables were used to define the MOSCAP size and position on the antenna surface, as well as the antenna itself was setup using a dedicated set of design variables. This approach allows the antenna and MOSCAP geometry to be changed or adjusted easily without the need to rebuild entire 3D geometry. For example, for the MOSCAP of a shape of a rectangular parallel plate capacitor, DC, LC, and HC variables were used to set, respectively, the depth, length and height of the capacitor, see Fig. B. 8. Similarly, the location, radius, and height for a circular parallel plate capacitor were defined using variables X0CYL, Y0CYL, RCYL and HCYL, as shown in Fig. B. 9.



Setup Name: Setup1

☑ Enabled ☐ Solve Ports Only

Solution Frequency: 8 GHz

Adaptive Solutions

Maximum Number of Passes: 12

Maximum Delta Energy: 0.1

Initial Mesh Options

☑ Do Lambda Refinement

Lambda Target: 0.6667 ☑ Use Default Value

☑ Use Free Space Lambda

Adaptive Options

Maximum Refinement Per Pass: 30 %

☐ Maximum Refinement: 1000000

Minimum Number of Passes: 2

Minimum Converged Passes: 2

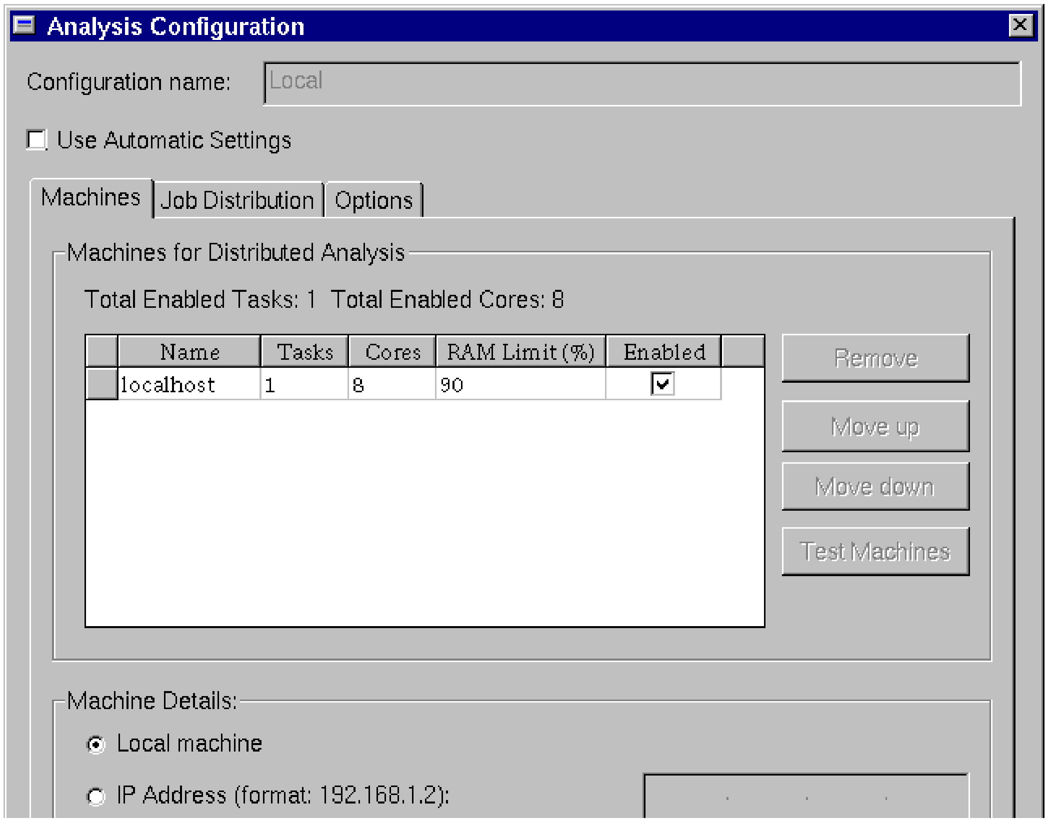
Solution Options

Order of Basis Functions: Mixed Order

● Direct Solver

○ Iterative Solver

Fig. B. 4. Driven Solution settings for CLFPA simulations



Configuration name: Local

☐ Use Automatic Settings

Machines for Distributed Analysis

Total Enabled Tasks: 1 Total Enabled Cores: 8

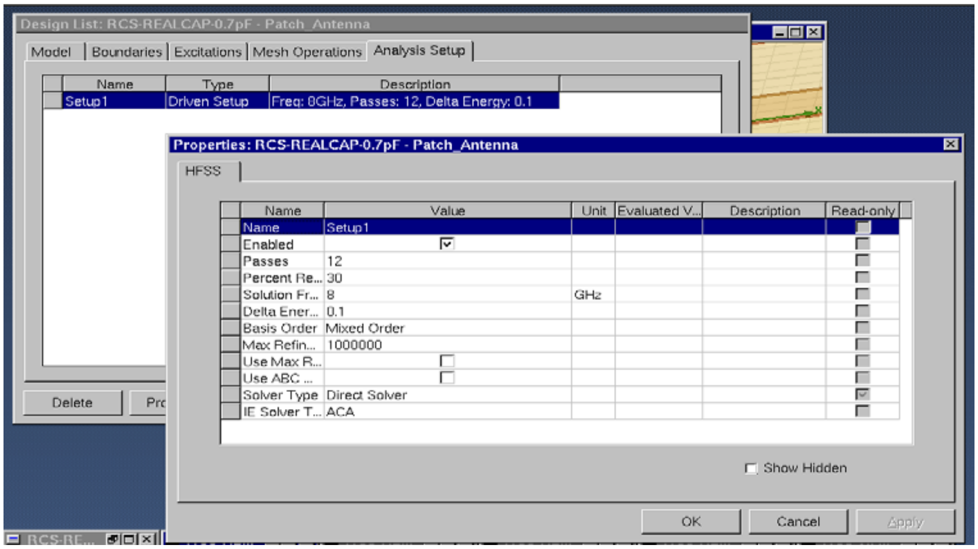
Name	Tasks	Cores	RAM Limit (%)	Enabled
localhost	1	8	90	☑

Machine Details:

● Local machine

○ IP Address (format: 192.168.1.2):

Fig. B. 5. HPC settings for CLFPA simulations

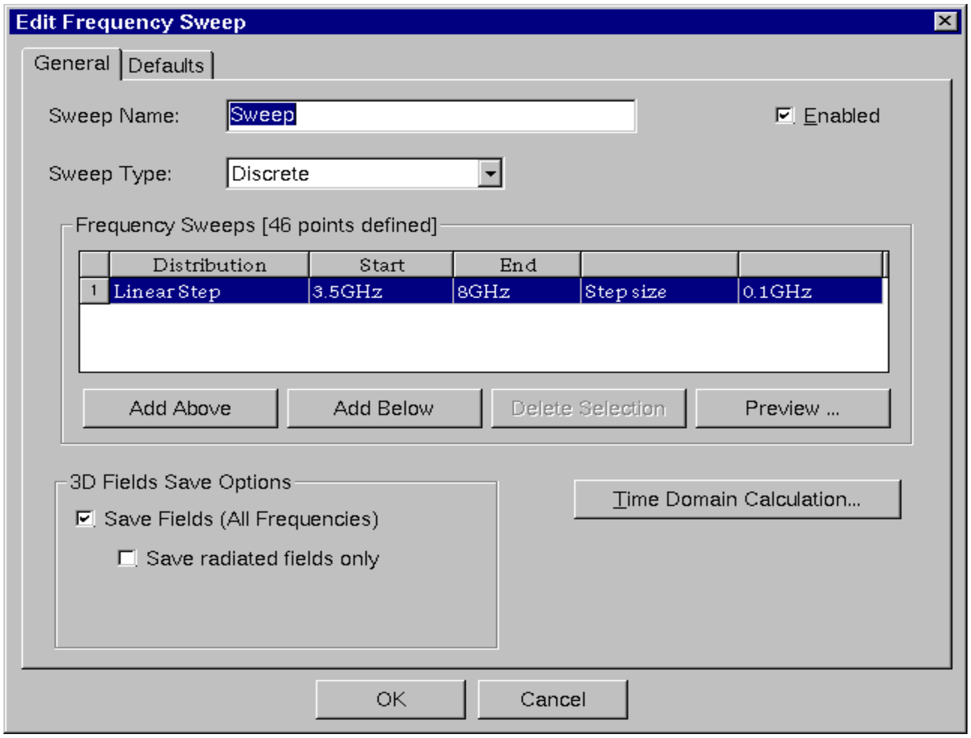


Name	Type	Description
Setup1	Driven Setup	Freq: 8GHz, Passes: 12, Delta Energy: 0.1

Name	Value	Unit	Evaluated V...	Description	Read-only
Name	Setup1				☐
Enabled	☑				☐
Passes	12				☐
Percent Re...	30				☐
Solution Fr...	8	GHz			☐
Delta Ener...	0.1				☐
Basis Order	Mixed Order				☐
Max Refin...	1000000				☐
Use Max R...	☐				☐
Use ABC ...	☐				☐
Solver Type	Direct Solver				☑
IE Solver T...	ACA				☐

☐ Show Hidden

Fig. B. 6. Folded patch antenna analysis setup around the solution frequency of 8 GHz



Sweep Name: Sweep

☑ Enabled

Sweep Type: Discrete

Frequency Sweeps [46 points defined]

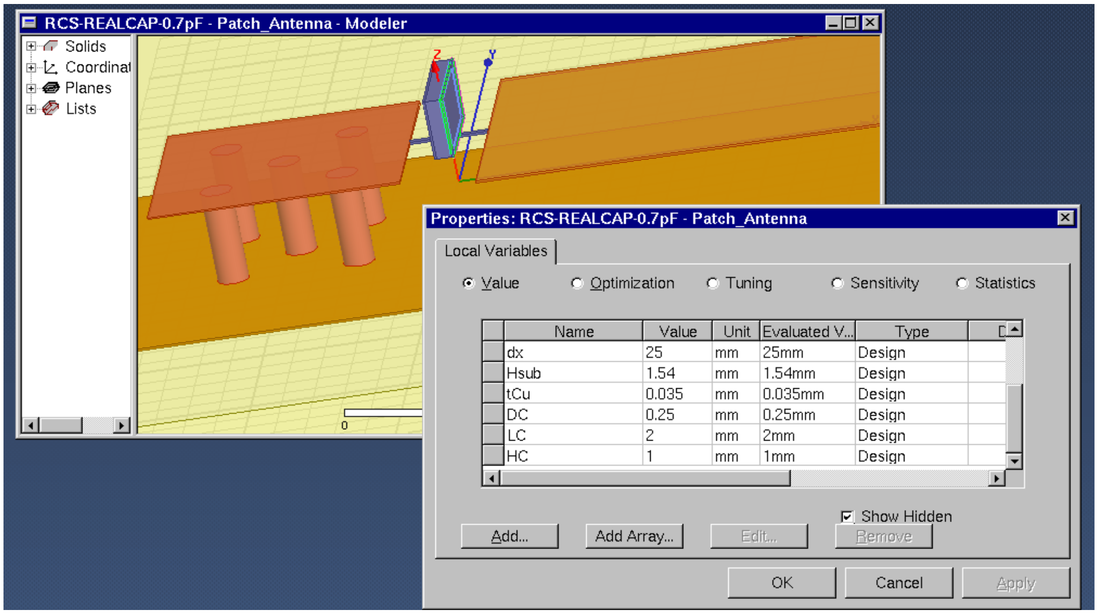
	Distribution	Start	End		
1	Linear Step	3.5GHz	8GHz	Step size	0.1GHz

3D Fields Save Options

☑ Save Fields (All Frequencies)

☐ Save radiated fields only

Fig. B. 7. Folded patch antenna linear step frequency sweep setup from 3.5 to 8 GHz with step size of 0.1 GHz



Properties: RCS-REALCAP-0.7pF - Patch_Antenna

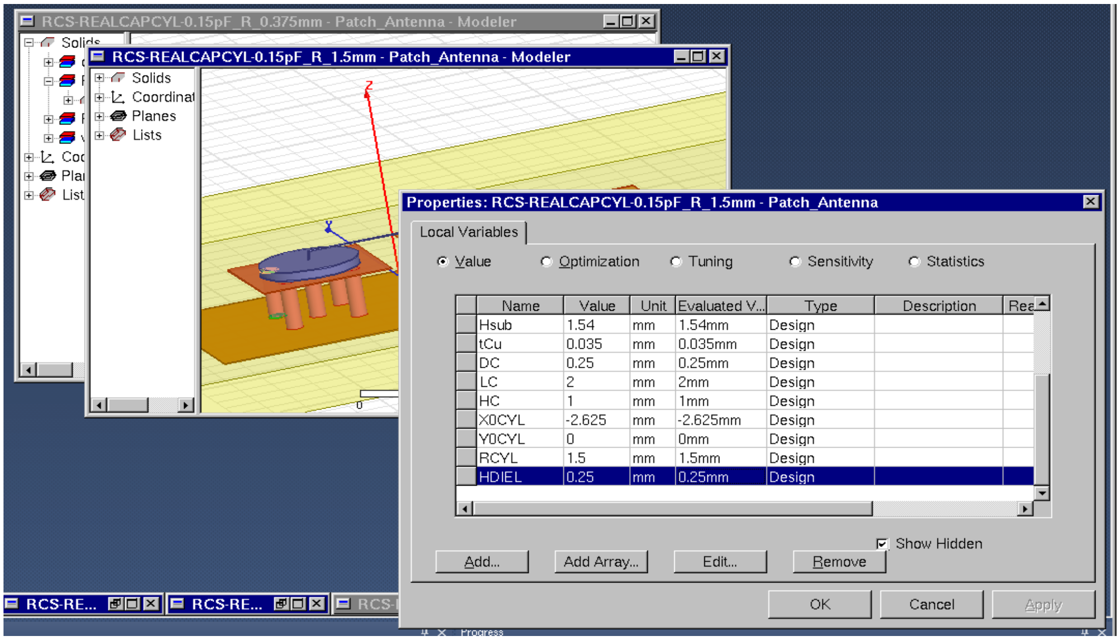
Local Variables

● Value ○ Optimization ○ Tuning ○ Sensitivity ○ Statistics

Name	Value	Unit	Evaluated V...	Type	D
dx	25	mm	25mm	Design	
Hsub	1.54	mm	1.54mm	Design	
tCu	0.035	mm	0.035mm	Design	
DC	0.25	mm	0.25mm	Design	
LC	2	mm	2mm	Design	
HC	1	mm	1mm	Design	

☑ Show Hidden

Fig. B. 8. Design settings for a real (rectangular parallel plate) capacitor. DC, LC, and HC variables are used to set, respectively, the depth, length and height of the capacitor object



Properties: RCS-REALCAPCYL-0.15pF_R_1.5mm - Patch_Antenna

Local Variables

● Value ○ Optimization ○ Tuning ○ Sensitivity ○ Statistics

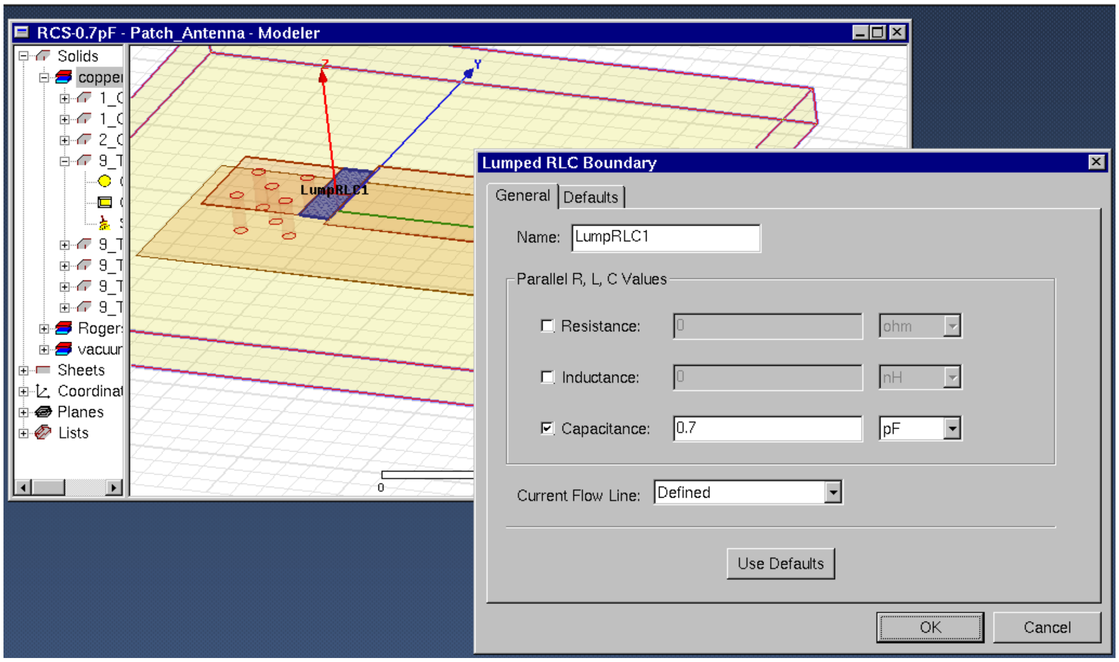
Name	Value	Unit	Evaluated V...	Type	Description	Rea
Hsub	1.54	mm	1.54mm	Design		
tCu	0.035	mm	0.035mm	Design		
DC	0.25	mm	0.25mm	Design		
LC	2	mm	2mm	Design		
HC	1	mm	1mm	Design		
X0CYL	-2.625	mm	-2.625mm	Design		
Y0CYL	0	mm	0mm	Design		
RCYL	1.5	mm	1.5mm	Design		
HDIEL	0.25	mm	0.25mm	Design		

☑ Show Hidden

Fig. B. 9. Design settings for a circular parallel plate capacitor

(B) Results with Lumped RLC Boundary

This section presents the results of simulations using the Lumped RLC boundary condition. Such boundary conditions are set via a planar sheet with a defined current flow line and values of R, and/ or L, and/ or C, as shown in Fig. B. 10, for a capacitively loaded patch antenna. The process was started by simulating pure capacitance boundary conditions by activating only C-values, thus neglecting inductance of the circuit (at the beginning). The results for a discrete capacitance value of 0.35 pF are shown in Fig. B. 11, which is a typical value used in the experimental studies.



Name: LumpRLC1

Parallel R, L, C Values

☐ Resistance: 0 ohm

☐ Inductance: 0 nH

☑ Capacitance: 0.7 pF

Current Flow Line: Defined

Fig. B. 10. Defining Lumped-RLC boundary conditions for modeling of CLFPA

The results for different values of capacitance are summarized in Fig. B. 12. One can clearly see that the range of capacitances at which strong resonance/dips takes place is between 0.2 and 0.7 pF. Also, for decreasing capacitance from 0.7 pF to 0.2 pF the positions of the dip shifts towards the higher frequencies. These predictions are in very good agreement with the experimental observations when discrete capacitors were used (which are directly mounted on the antenna without wirebonding).

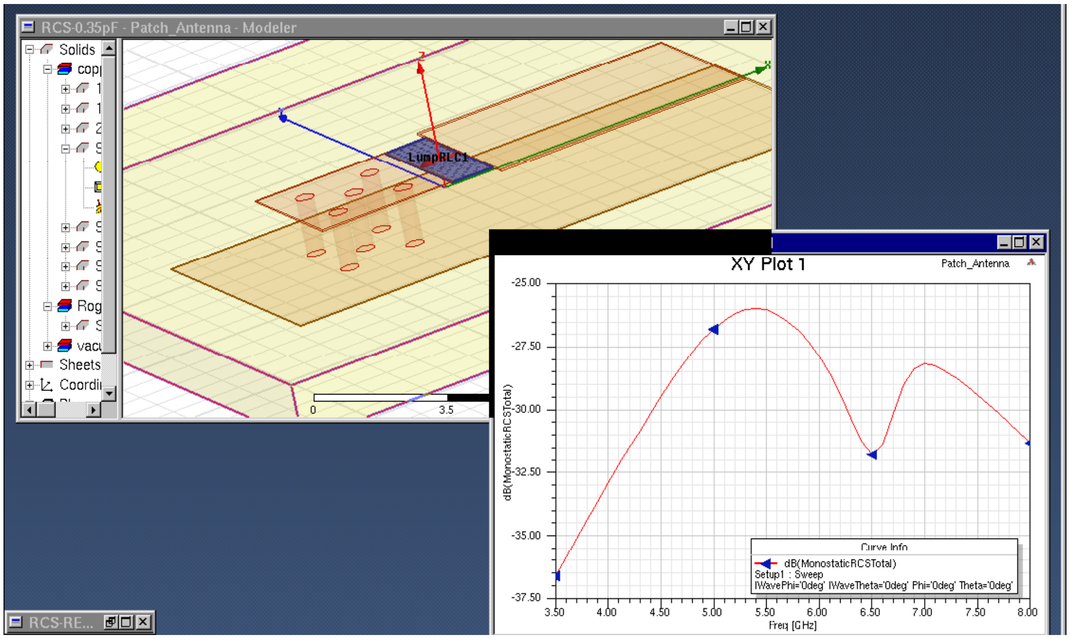


Fig. B. 11. Screenshot of folded patch antenna setup with lumped RLC boundary condition. The insert shows the total (monostatic) RCS signal as function of frequency for C = 0.35 pF.

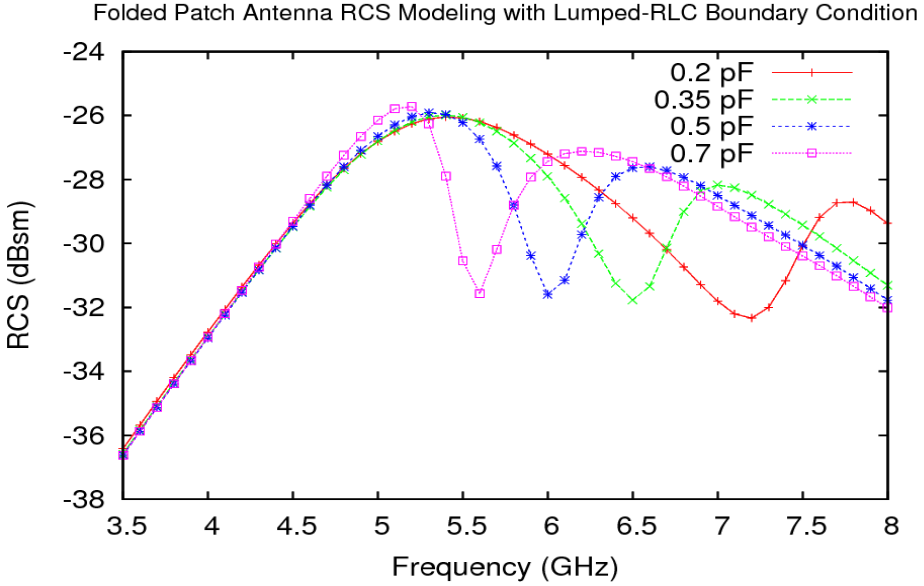


Fig. B. 12. Predicted (monostatic) RCS signals as functions of frequency with lumped RLC boundary for 4 different capacitance values

(C) Results with a Real Capacitor without Wirebonding

After testing the code on the simple case with a lumped RLC boundary condition, a more complex example was set up where the capacitor has a realistic shape. A rectangular parallel plate capacitor was generated with two metal electrodes of finite width which enclose a dielectric material of a prescribed relative permittivity, as shown in Fig. B. 13. Capacitance was adjusted by changing the value of the relative permittivity. The capacitor is connected to the top antenna patches via 2 short copper wires of rectangular shape, thus providing minimum amount of parasitic impedance.

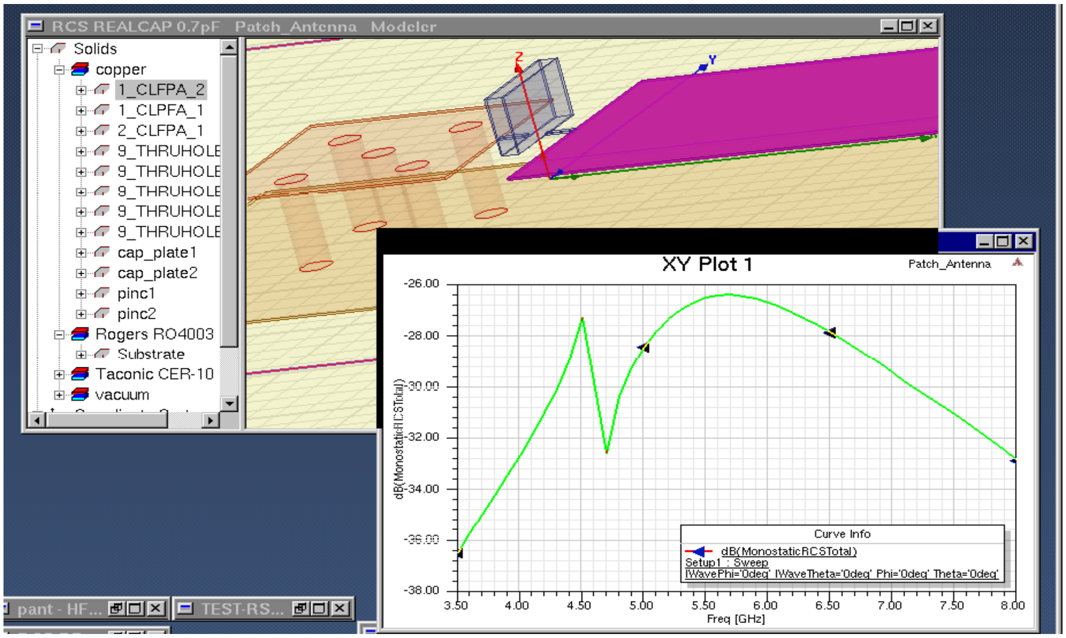


Fig. B. 13. Screenshot of folded patch antenna setup with a rectangular parallel shape capacitor. The inset shows the total (monostatic) RCS signal as function of frequency for C = 0.7 pF.

The results for the modeled patch antenna loaded with a rectangular parallel plate capacitor are summarized in Fig. B. 14. One can see that similar behavior is observed to that obtained when using the lumped RLC boundary. The values of the capacitance decreased but only by a small amount. These predictions again are in very good agreement with the experimental observations for discrete capacitors directly mounted on the antenna.

This successful modeling of a realistic capacitor within the HFSS framework helped to gain the necessary experience and confidence to proceed to a more complex case of MOSCAP + wirebonding configuration presented below.

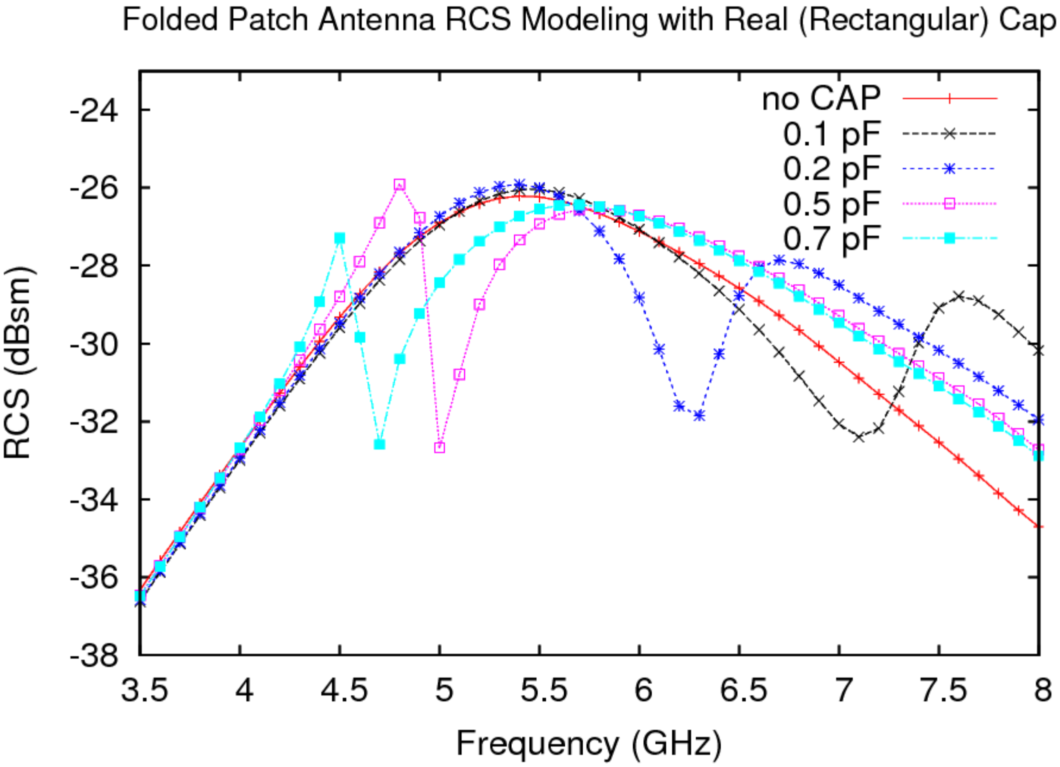
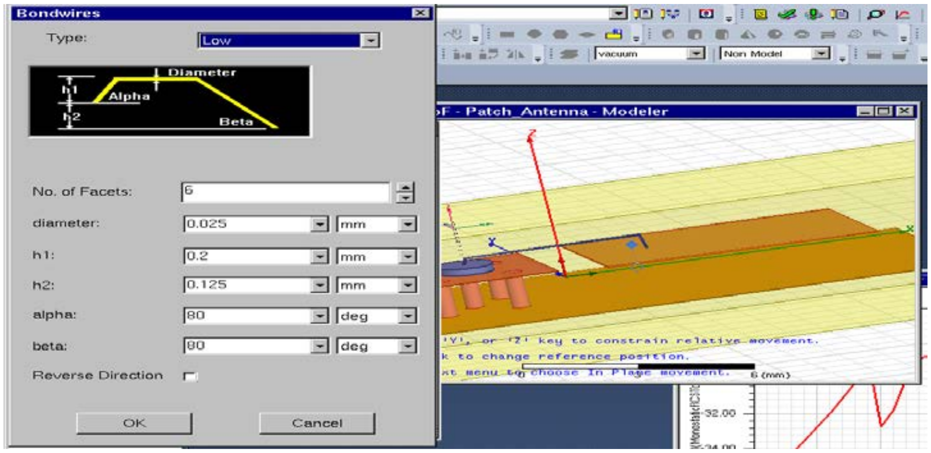


Fig. B. 14. Predicted (monostatic) RCS signals as functions of frequency with rectangular parallel plate capacitor for 5 different capacitance values

(D) Results with Circular Parallel Plate Capacitor with Wirebonding

Having validated the code for two types of capacitors, a more realistic case was set up where a circular parallel plate capacitor is used. Again, in order to enable easy modification of its geometry, a set of specialized variables were used to create the capacitor object (two metal plates of finite width and a dielectric material between them). This capacitor is connected to the antenna patch via a special bondwire object of “Low” type (total 3 types are available in HFSS), as shown in Fig. B. 15. The resulting capacitor object (0.75 mm in radius and 0.25 mm in height) and the bondwire object (length of 5 mm and diameter of 0.07 mm) are shown in Fig. B. 16 for conditions approximating those used in the experiments.



Bondwires

Type: Low

No. of Facets: 6

diameter: 0.025 mm

h1: 0.2 mm

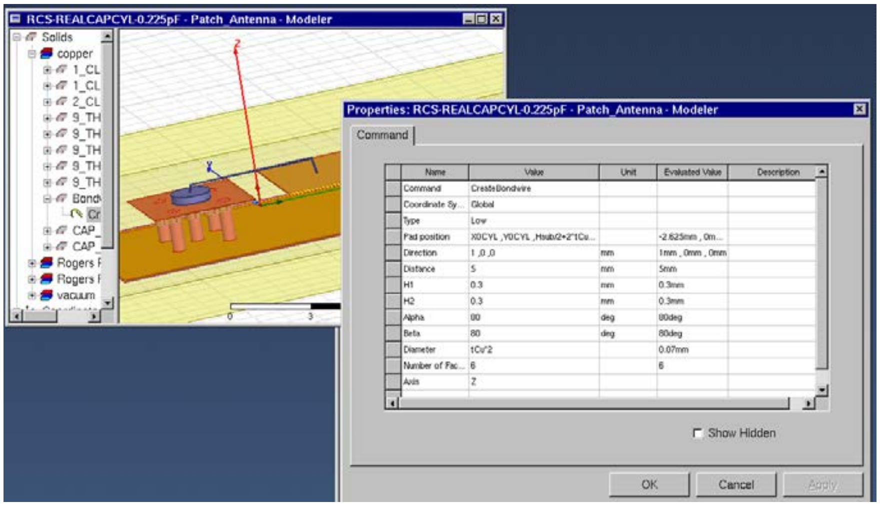
h2: 0.125 mm

alpha: 80 deg

beta: 80 deg

Reverse Direction ☐

Fig. B. 15. Bondwire type used in the modeling of CLFPA



RCS-REALCAPCYL-0.225pF - Patch_Antenna - Modeler

Properties: RCS-REALCAPCYL-0.225pF - Patch_Antenna - Modeler

Name	Value	Unit	Evaluated Value	Description
Command	CreateBondwire			
Coordinate Sy...	Global			
Type	Low			
Pad position	X0CYL ,Y0CYL ,Hsub/2+2*tCu...		-2.625mm , 0m...	
Direction	1 ,0 ,0	mm	1mm , 0mm , 0mm	
Distance	5	mm	5mm	
H1	0.3	mm	0.3mm	
H2	0.3	mm	0.3mm	
Alpha	80	deg	80deg	
Beta	80	deg	80deg	
Diameter	tCu*2		0.07mm	
Number of Fac...	6		6	
Axis	Z			

☐ Show Hidden

Fig. B. 16. Bondwire settings used in the modeling of CLFPA

The capacitance of the modeled MOSCAP object was changed by varying the relative permittivity of the capacitor dielectric material. The results for different capacitances are shown in Fig. B. 17. One can observe the same general trend with decreasing capacitance value. However, compared with the previous cases with no wirebonding, the striking result is that the resonance dips disappeared from the frequency window of interest for the capacitance values used previously (namely, between 0.2 and 0.7 pF). This agrees with the experimental results when MOSCAP with wirebonding were used. The conducted modeling shows that much lower values of capacitance are needed in order to have the resonance/dip to happen inside the frequency window. One can see that the values of C are lower by a factor of 5x–8x, compared to Fig. B. 12 and Fig. B. 14.

The results obtained for the 3 studied capacitor types are summarized in Fig. B. 18 in terms of the resonance/dip frequency as a function of the capacitance values. The dependence is super-linear for decreasing capacitance. One can also observe that the capacitance at which a particular dip takes place decreases significantly when more wirebonding is added. In other words, adding wirebonding (thus increasing parasitic inductance) decreases the extent of the useful capacitance range (going from 0.2-0.7 pF without wirebonding to 0.025-0.3 pF with wirebonding). To observe the resonance/dip, one has to decrease the value of MOSCAP (with wirebonding) capacitance by a factor of 5x-6x. This can be achieved by decreasing the radius of the MOSCAP device by a factor of 2x-2.5x or by other means (e.g. using other dielectric materials).

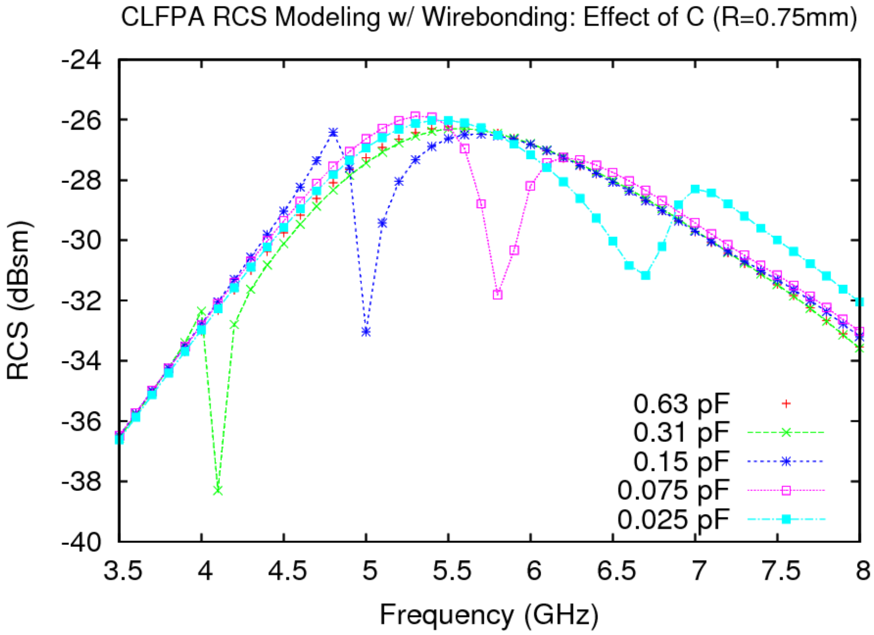


Fig. B. 17. Predicted (monostatic) RCS signals as functions of frequency for circular parallel plate capacitors with wirebonding for 5 different capacitance values

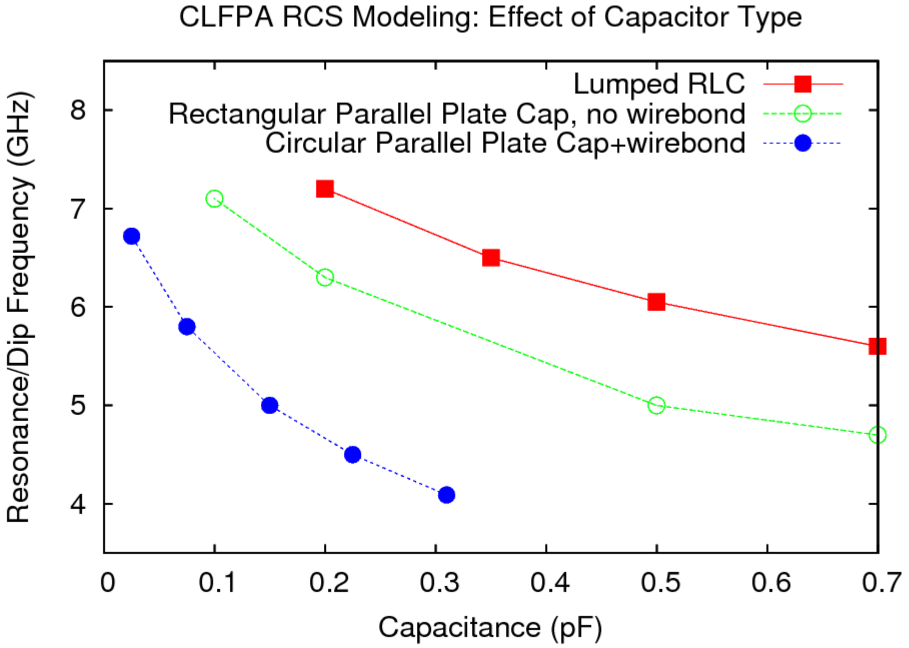


Fig. B. 18. Resonance/dip frequencies as functions of capacitance values for 3 types of studied capacitors

(E) Influence of Bond Wire Length and the MOSCAP Footprint on the RCS Signal

Having observed the crucial impact of wirebonding above, the effects of the wirebond size/length and of the MOSCAP footprint on the CLFPA (namely, its size or area) were studied. At first the influence of the wire bond size was studied. It is known from formulas shown in Fig. B. 23 that the inductance of a wire is proportional to its length. To achieve different lengths, 2 different CLFPA bondwire settings were used: height 1.5 mm (top) and distance 10 mm (bottom), as shown in Fig. B. 19. (Recall that the baseline bondwire is of 0.3 mm height and 5 mm distance). In first case, the length of the wire went from ~5 mm to ~8 mm and in the second case from ~5 mm to ~ 10 mm, thus increasing the inductance by a factor or 1.6 and 2, correspondingly. The simulation results for these two cases are shown in Fig. B. 20 together with the baseline case. One can see that increasing the length of the wire bond results in the dip moving towards low frequencies out of the usable frequency window. The dip completely disappears when using ~10 mm length wire.

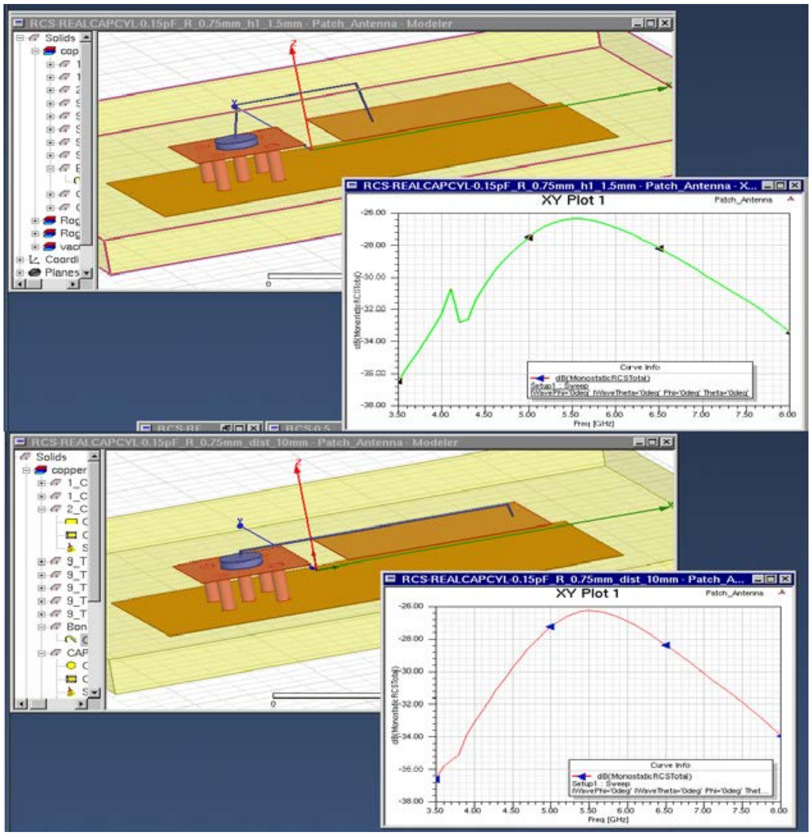


Fig. B. 19. Two different CLFPA bondwire settings: height 1.5 mm (top) and distance 10 mm (bottom). The baseline bondwire (Fig. B. 15) is 0.3 mm height and 5 mm distance.

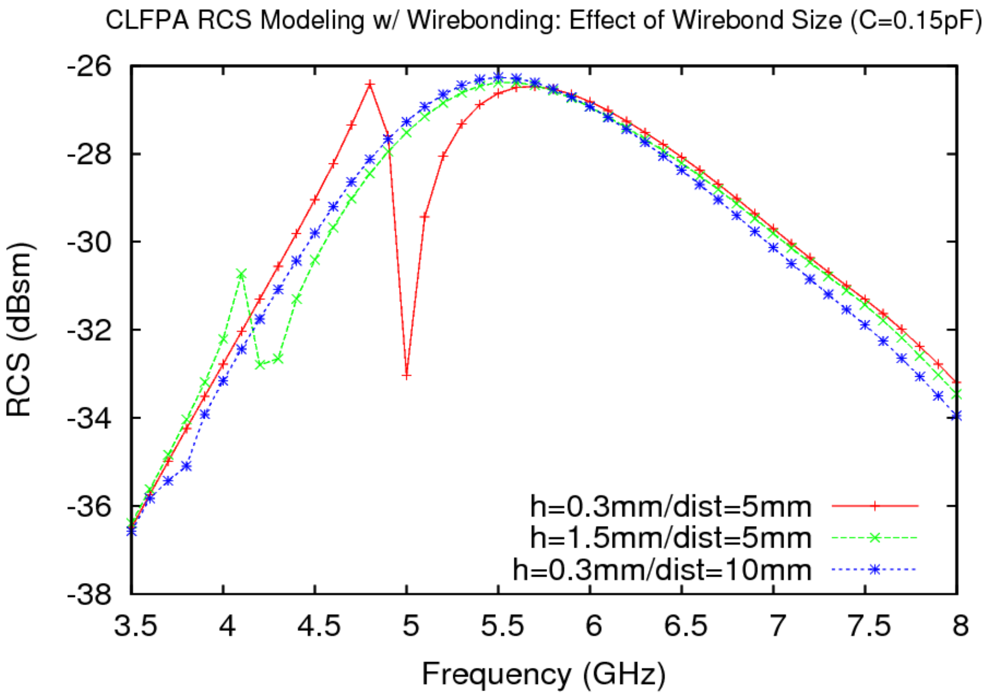


Fig. B. 20. Predicted (monostatic) RCS signals as functions of frequency for circular parallel plate capacitors with wirebonding of 3 different bond wire sizes (height and distance, see Fig. B. 19)

Finally, for this series of tests, studies were performed to figure out how the MOSCAP footprint on the antenna patch affects the results. To achieve this, capacitors of two different radii were used (0.375 mm and 1.5 mm), as shown in Fig. B. 21. Capacitance was kept to 0.15 pF to see the effect of MOSCAP size only. The results are summarized in Fig. B. 22. One can see that the baseline results are not affected when decreasing the capacitor size to 0.375 mm (halving the radius). Taking into account the previous results, this can be explained by decreasing parasitic inductance of the capacitance + bondwire setup. However, when increasing the cap size (doubling the radius), the dip shifts significantly towards low frequencies. This can be explained by increasing parasitic inductance of the capacitance + bondwire configuration.

The conclusion was drawn that adding more “wirebonding” (be it an increase in the physical size/diameter of the MOSCAP or in the wire length) and keeping the same MOSCAP capacitance shifts the resonance dip towards lower frequencies. To bring the dip back into frequency window of 4-7 GHz, one has to decrease the MOSCAP capacitance.

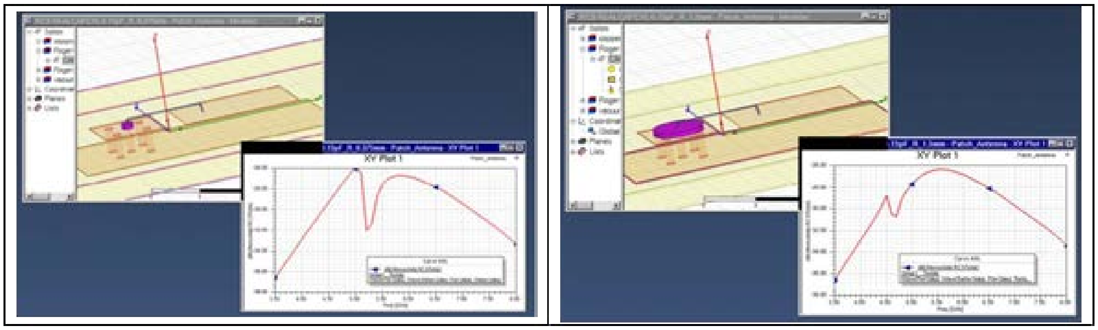


Fig. B. 21. Two different CLFPA cap settings: radius 0.375 mm (left) and 1.5 mm (right)

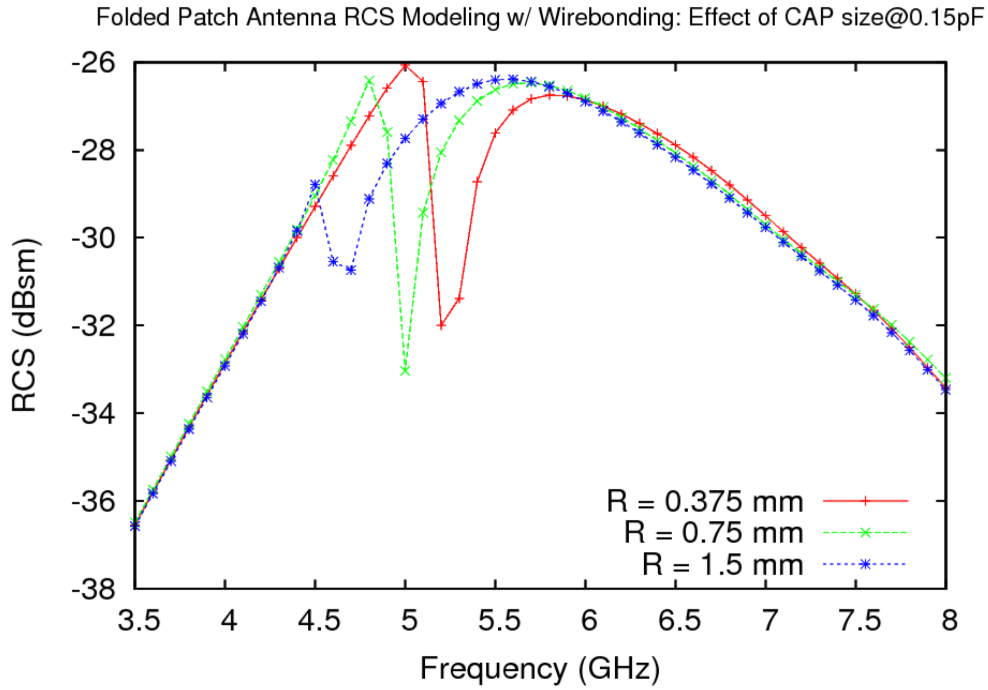
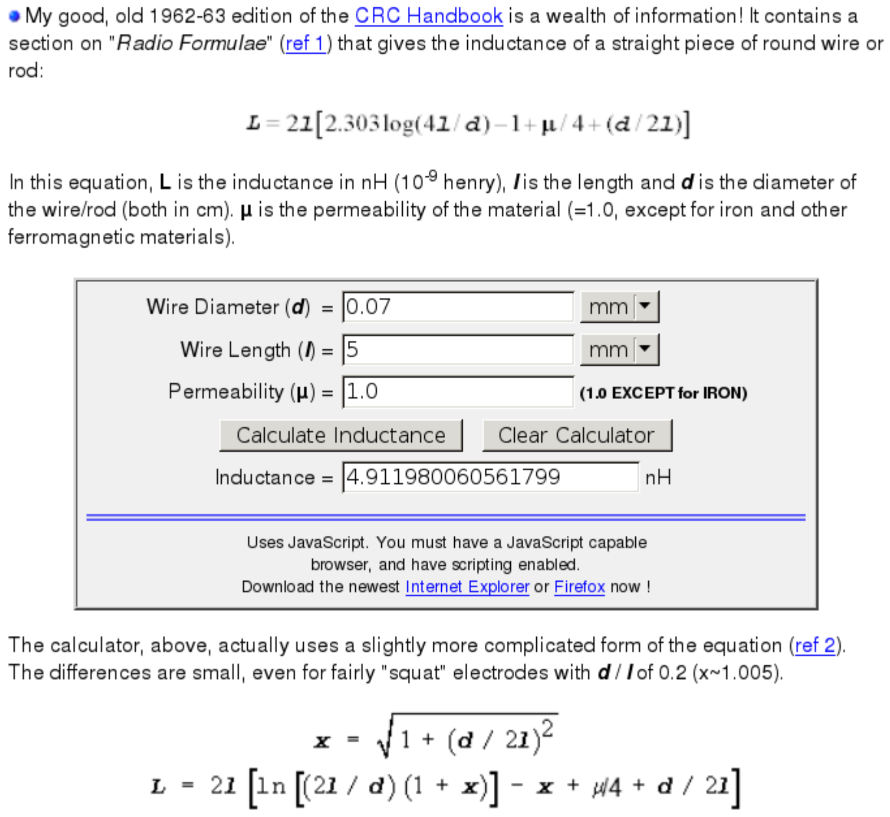


Fig. B. 22. Predicted (monostatic) RCS signals as functions of frequency for circular parallel plate capacitors with wirebonding of 3 different cap sizes (see Fig. B. 21)

(F) Influence of Bond Wire Inductance within the Lumped RLC Boundary Approach

An additional study of the possible effects of the parasitic inductance of the MOSCAP + wirebonding configuration were performed within the simplified lumped RLC boundary approach. For that the value of inductance of the wirebonding was estimated. Estimations of the inductance of a wire of 0.07 mm in diameter and 5 mm in length resulted in ~5 nH value. Corresponding formulas are shown in Fig. B. 23.



- My good, old 1962-63 edition of the CRC Handbook is a wealth of information! It contains a section on "*Radio Formulae*" (ref 1) that gives the inductance of a straight piece of round wire or rod:

$$L = 2l\left[2.303\log(4l/d) - 1 + \mu/4 + (d/2l)\right]$$

In this equation, **L** is the inductance in nH (10^{-9} henry), ***l*** is the length and ***d*** is the diameter of the wire/rod (both in cm). **μ** is the permeability of the material (=1.0, except for iron and other ferromagnetic materials).

Wire Diameter (***d***) = 0.07 mm

Wire Length (***l***) = 5 mm

Permeability (μ) = 1.0 **(1.0 EXCEPT for IRON)**

Inductance = 4.911980060561799 nH

Uses JavaScript. You must have a JavaScript capable browser, and have scripting enabled.
Download the newest Internet Explorer or Firefox now !

The calculator, above, actually uses a slightly more complicated form of the equation (ref 2). The differences are small, even for fairly "squat" electrodes with ***d*** / ***l*** of 0.2 (x~1.005).

$$x = \sqrt{1 + (d/2l)^2}$$

$$L = 2l\left[\ln\left[(2l/d)(1+x)\right] - x + \mu/4 + d/2l\right]$$

Fig. B. 23. Example of straight wire inductance calculator with the corresponding formulas, from http://www.consultrsr.net/resources/eis/induct5.htm

To create series circuits, two separate RLC boundaries must be applied to two separate 2D objects which are arranged in an end–to-end fashion. This is shown in Fig. B. 24. By following this example, an LC series circuit was created for the modeled CLFPA, as shown in Fig. B. 25.

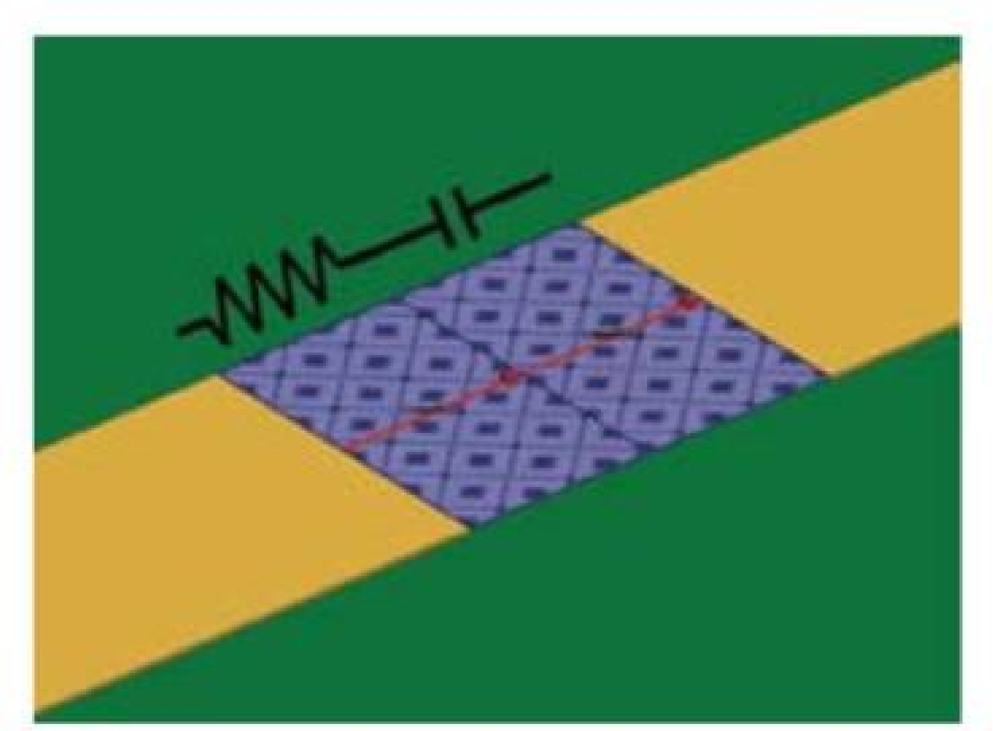
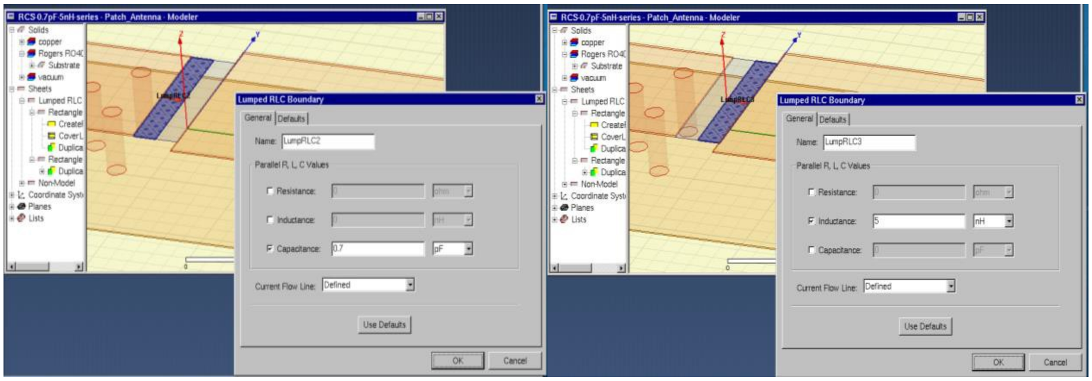


Fig. B. 24. From HFSS Manual: Microstrip model showing the RLC Boundary applied to two end-to-end 2D sheet objects in order to model a series combination of inline resistor and capacitor



RCS-0.7pF-5nH-series - Patch_Antenna - Modeler

Lumped RLC Boundary

Name: LumpRLC2

Parallel R, L, C Values

☐ Resistance: 0 ohm
☐ Inductance: 0 nH
☑ Capacitance: 0.7 pF

Current Flow Line: Defined

RCS-0.7pF-5nH-series - Patch_Antenna - Modeler

Lumped RLC Boundary

Name: LumpRLC3

Parallel R, L, C Values

☐ Resistance: 0 ohm
☑ Inductance: 5 nH
☐ Capacitance: 0 pF

Current Flow Line: Defined

Fig. B. 25. CLFPA modeling with LC boundary applied to two end-to-end 2D sheet objects to model a series combination of inline capacitor (left) and inductor (right)

By thus creating an LC-loaded FPA, the effect of the inductance was studied in series by varying its value at a fixed capacitance value. An example is shown in Fig. B. 26 for 4 different inductance values. One can see that when using 0.7 pF capacitance at 5 nH, the dip completely disappears from the frequency window. A weak signal/ dip appears only when the inductance is reduced to 1 nH and the full signal/ dip restoration takes place for inductances below 0.25 nH.

By thus creating an LC-loaded FPA, the effect of the inductance was studied in series by varying its value at a fixed capacitance value. An example is shown in Fig. B. 26 for 4 different inductance values. One can see that when using 0.7 pF capacitance at 5 nH, the dip completely disappears from the frequency window. A weak signal/ dip appears only when the inductance is reduced to 1 nH and the full signal/ dip restoration takes place for inductances below 0.25 nH.

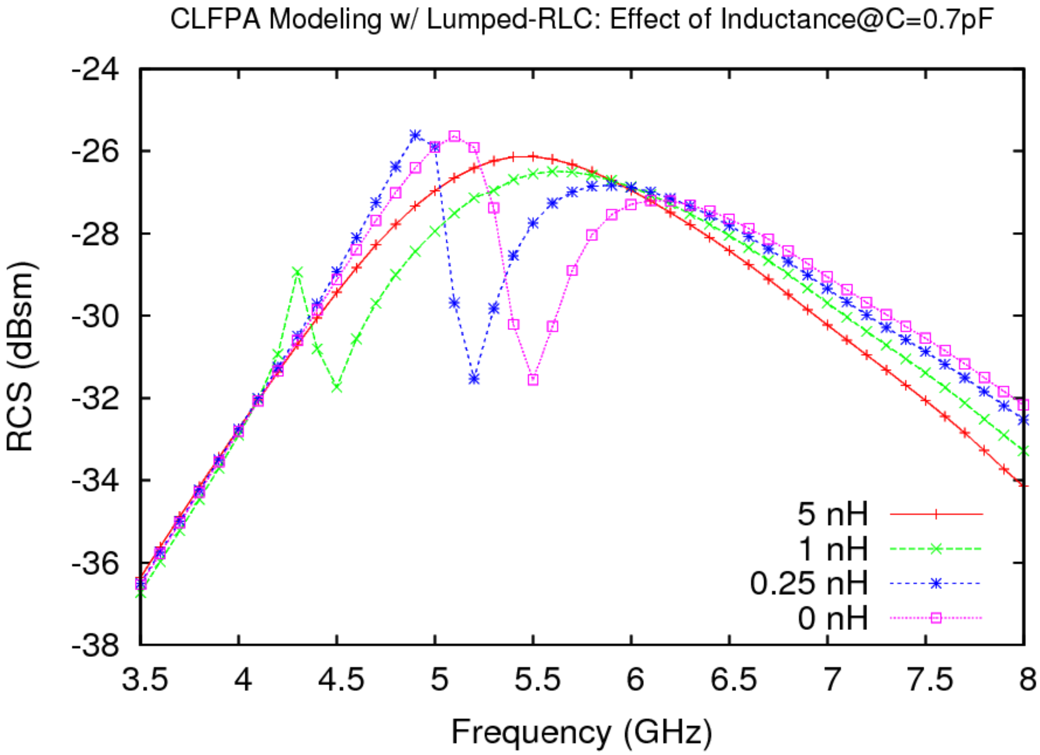


Fig. B. 26. Predicted (monostatic) RCS signals as functions of frequency with lumped RLC boundary for 4 different inductance values at fixed capacitance of 0.7 pF

Previous simulations of the full MOSCAP + wirebond configuration showed that, resonance dip can be brought back to the frequency window only by significantly decreasing the MOSCAP capacitance. This effect can be emulated within the LC boundary approach. Indeed, by decreasing the capacitance value from 0.7 pF to 0.1 pF, the resonance dip, being absent at 0.7 pF, comes back into the frequency window of interest, even at a high inductance of 3 nH, as is clearly seen in Fig. B. 27. There are multiple dip resonances (not observed in full simulations of the MOSCAP + wirebond configuration), which are most likely due to the oversimplified model of only LC-loaded FPA. Analysis of these results combined with previous results for the MOSCAP + wirebond setup provides an estimation that the parasitic inductance of the wire bonding element is of the order of 3-5 nH. It is only a crude estimate since the inductance is frequency dependent and is affected by many other parameters. This estimate is however very useful since it can help predict, how much the capacitance should be reduced to be able to observe a strong resonance dip in the frequency range of interest.

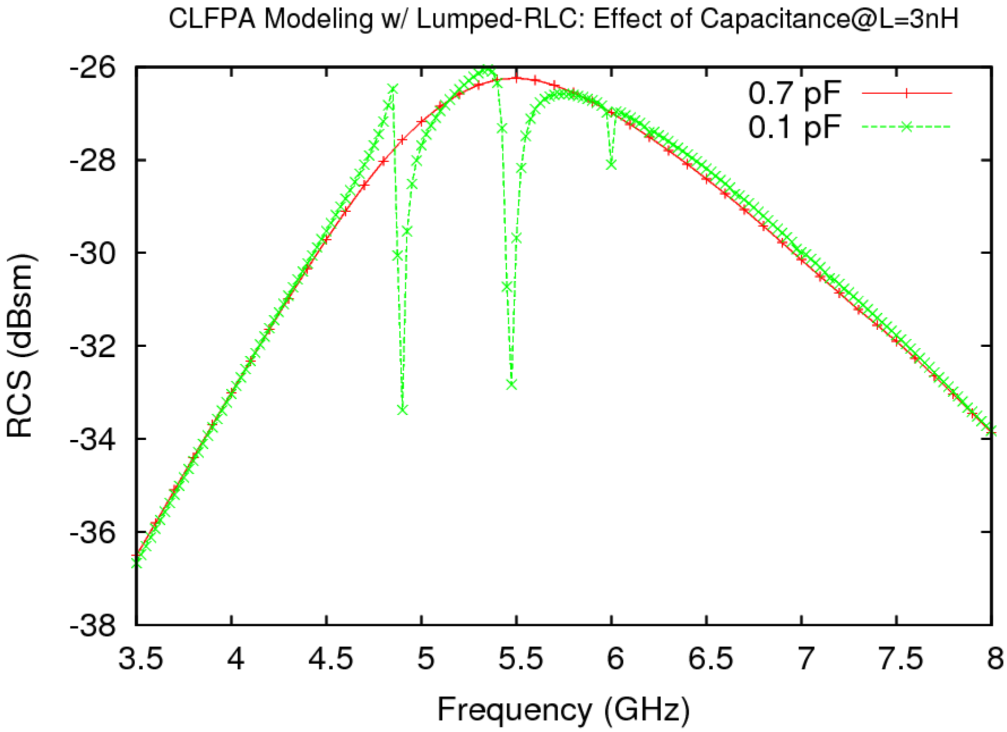
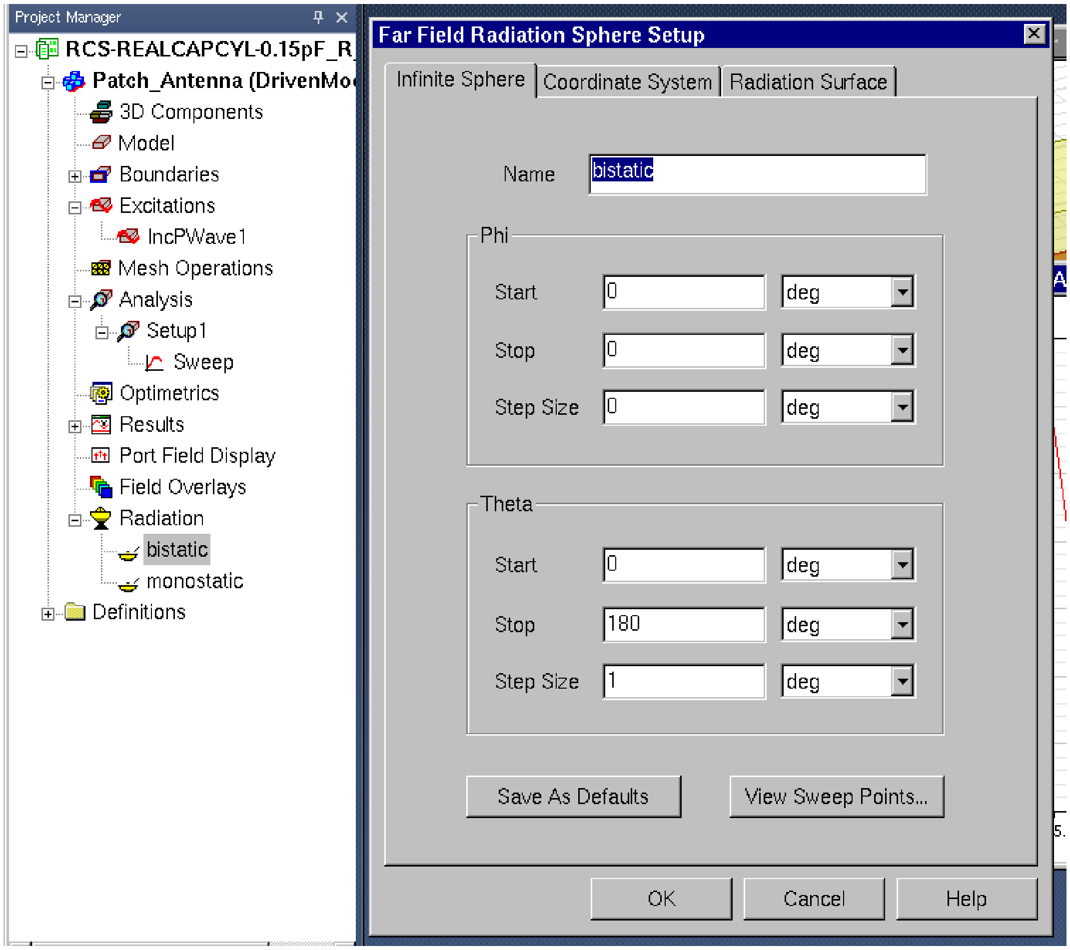


Fig. B. 27. Predicted (monostatic) RCS signals as functions of frequency with lumped RLC boundary for two different capacitance values at a fixed inductance of 3 nH

(G) Initial Study of the Angular Dependence of the RCS Signal

Initial analyses of the angular dependence of the RCS signal was performed. This is important to help assess the influence of transmitter and receiver placements with respect to a single CLFPA or an array of CFLPA devices. The bistatic RCS settings are shown in Fig. B. 28. Some initial results are shown in Fig. B. 29 (θ-angle is rotated away from the z-axis and φ-angle is rotated away from the x-axis). One can see that the reflected RCS signal drops by about 10 dBsm when the angle changes from 0 to 90 degrees. More detailed studies of the angular dependences of RCS are planned for later stages of the project.



Name: bistatic

Phi

Start: 0 deg
Stop: 0 deg
Step Size: 0 deg

Theta

Start: 0 deg
Stop: 180 deg
Step Size: 1 deg

Fig. B. 28. Radiation source bistatic settings with θ-angle variation from 0 to 180 degrees

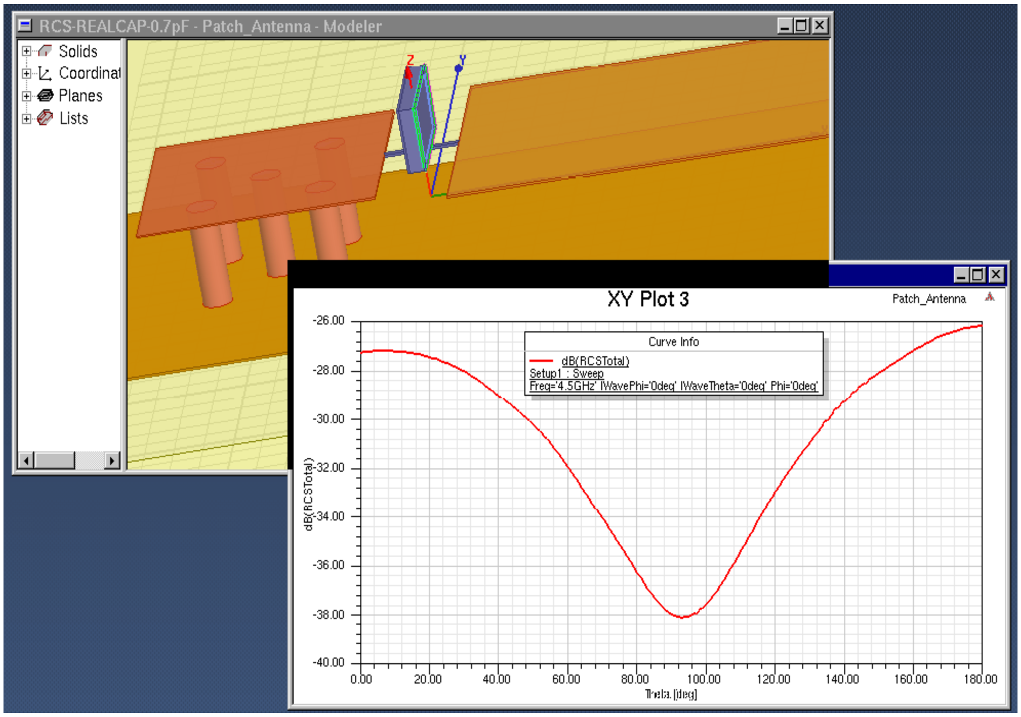


Fig. B. 29. Rectangular parallel plate capacitor without wire bonding. Angular dependence of bistatic RCS @ 4.5 GHz reflected signal frequency.

(H) Effect of the Number of Wire Bonds

The proposed idea to reduce the parasitic bond wire inductance was to use several wire bonds in parallel. Such a setup is demonstrated in Fig. B. 30.

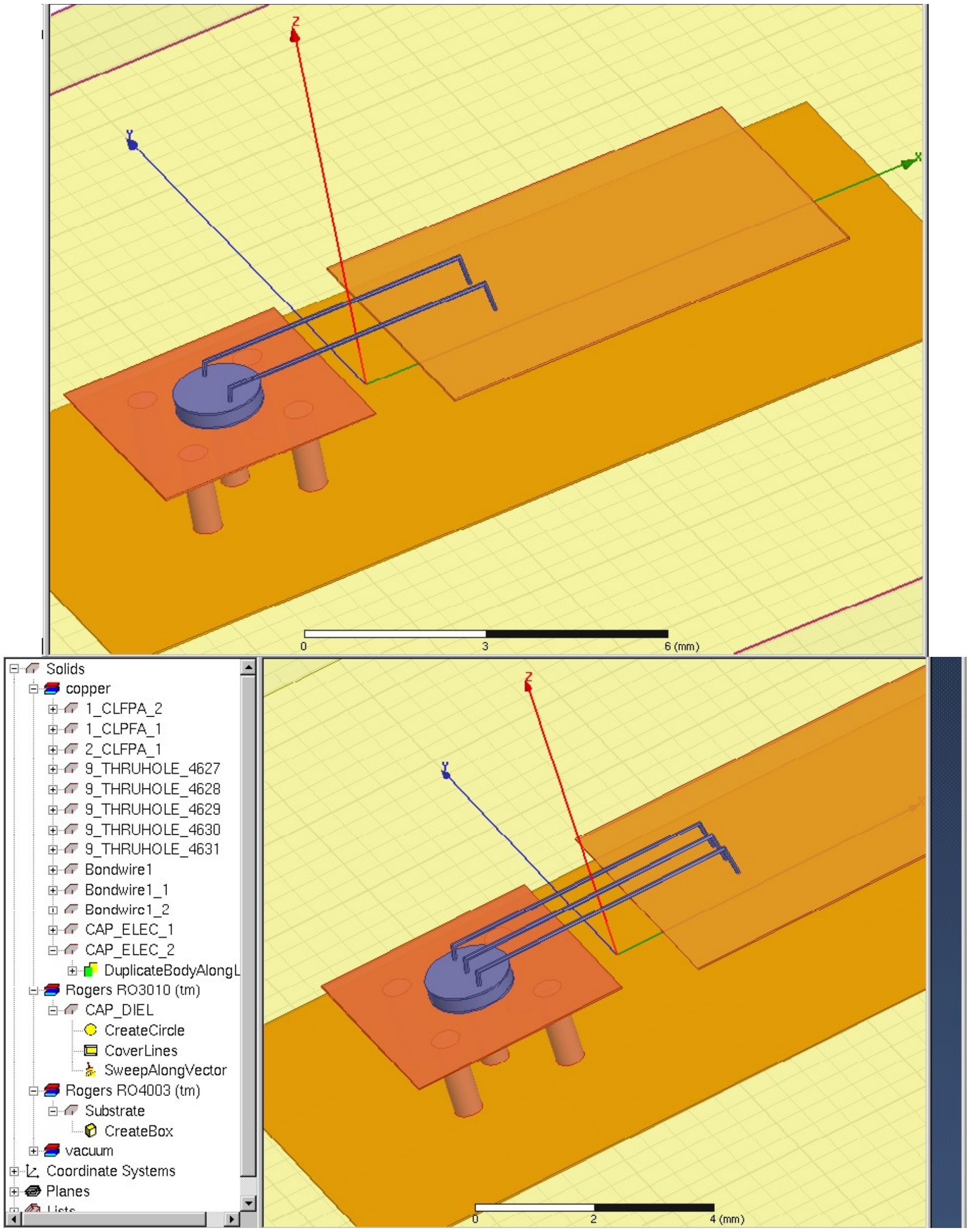


Fig. B. 30: Examples of antenna structures with 2 (top) and 3 (bottom) wire bonds

A series of simulations were performed using different number of wire bonds. The results are presented in Fig. B. 31. One can see that, as expected, the dip moves to the right end of the frequency window indicating a decrease of the wire inductance. When going from 2 to 3 wires the frequency shift is only small as expected from the inductance decrease of 2 to 3 parallel wires. This approach can be used to decrease the parasitic inductance in order to enable using larger MOSCAP capacitances

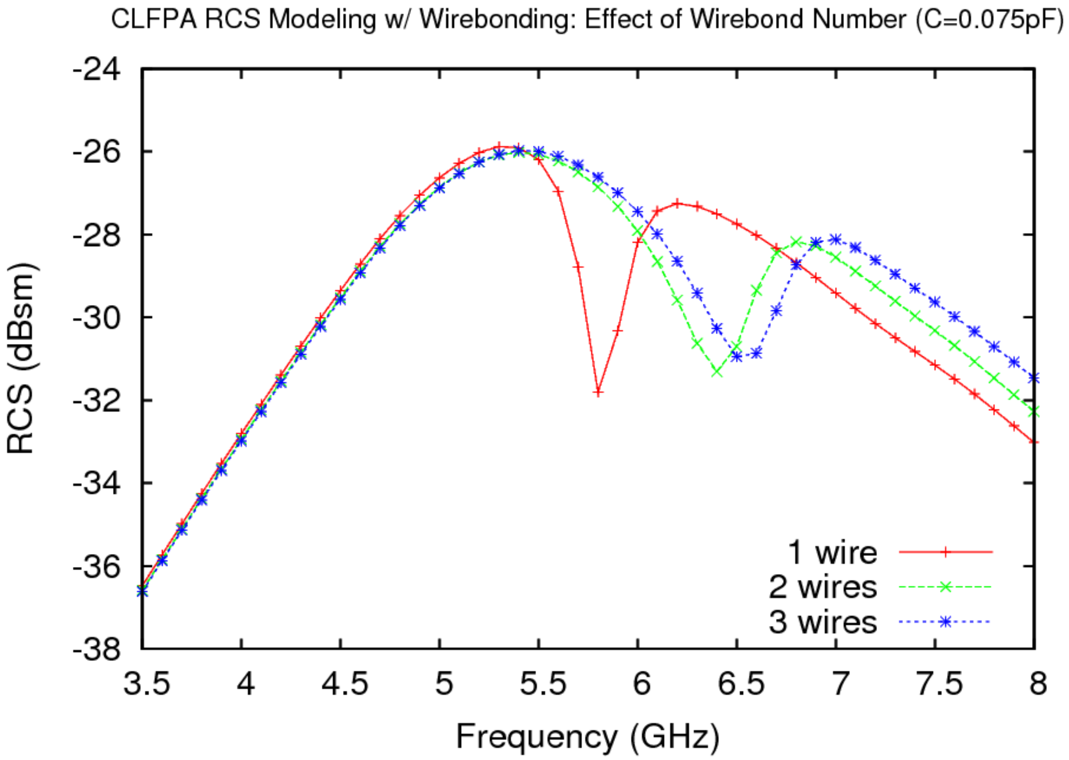


Fig. B. 31: Predicted (monostatic) RCS signals as functions of frequency with wirebonding for 1, 2 and 3 wires

(I) Effect of the Number of Through Hole Vias

A setup was prepared to conduct a series of tests using different numbers of through hole vias (Fig. B. 32). The results are presented in Fig. B. 33. One can see that the RCS signal is almost not affected by the number of through hole vias. Hence, subsequent simulations were continued using 5 through hole vias (as used originally).

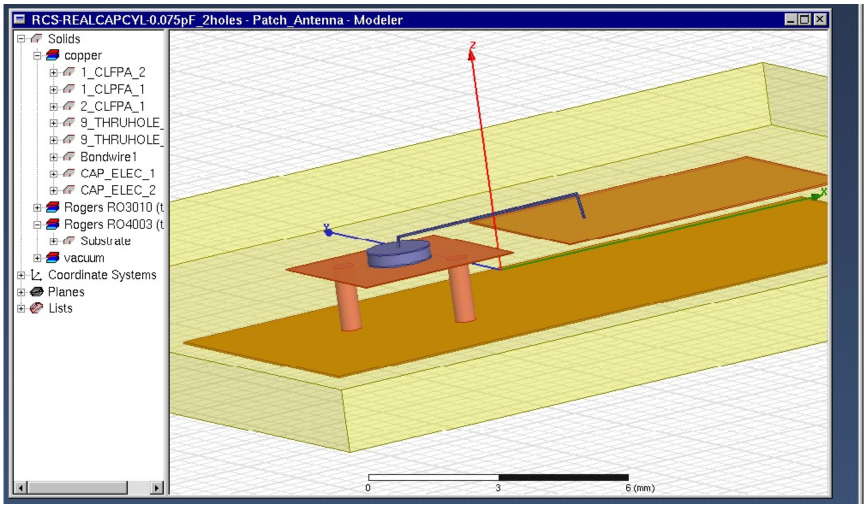


Fig. B. 32. Patch antenna setup with 2 through hole vias

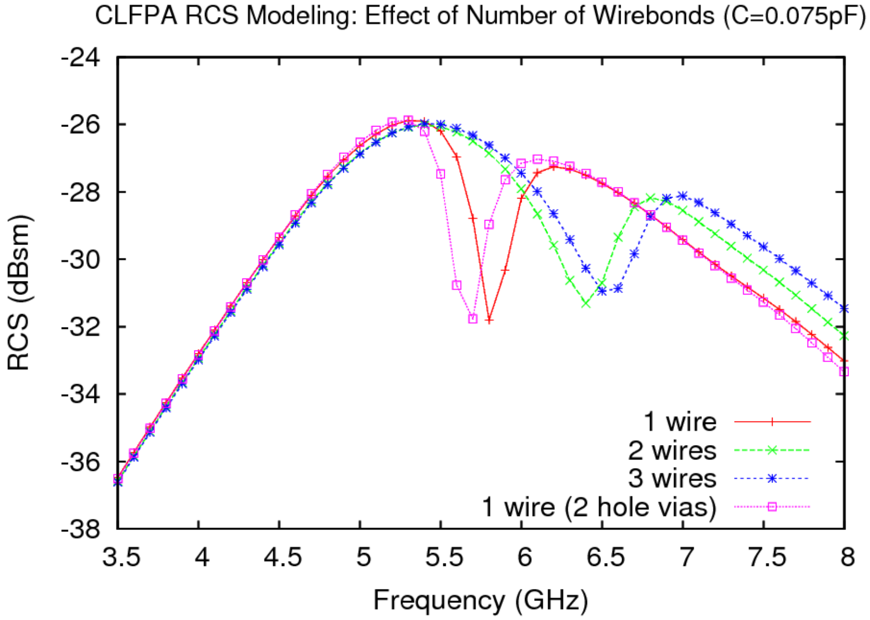


Fig. B. 33. Predicted (monostatic) RCS signals as functions of frequency with wirebonding for 1, 2 and 3 wires, as well as with 2 through hole vias

(J) Effect of the Substrate Resistance

To figure out the role of resistance on the RCS signal's dip/resonance, simulations of the folded patch antenna were carried out with a resistance (representative of the substrate resistance) connected in series with the capacitor. For that, lumped boundary conditions were implemented with some values of resistance. The resistor was placed at the tip of the bond wire in series with the loading capacitance. Since the choice of the size of a sheet used to apply the lumped boundary conditions is somewhat arbitrary, it was verified that the size of this sheet does not affect significantly the RCS signal. The settings of the two sheet geometries are shown in Fig. B. 34. The obtained RCS signals for these two sheets are shown in Fig. B. 35. One can see that the RCS signal is only little affected by the assumed size of the lumped boundary/ sheet size. Hence, subsequent simulations were proceeded with the smaller size sheet. Further, it was verified that when zero resistance is set, previously obtained results were fully recovered with no resistor in series (the bond wire connects directly to the MOSCAP metal electrode)

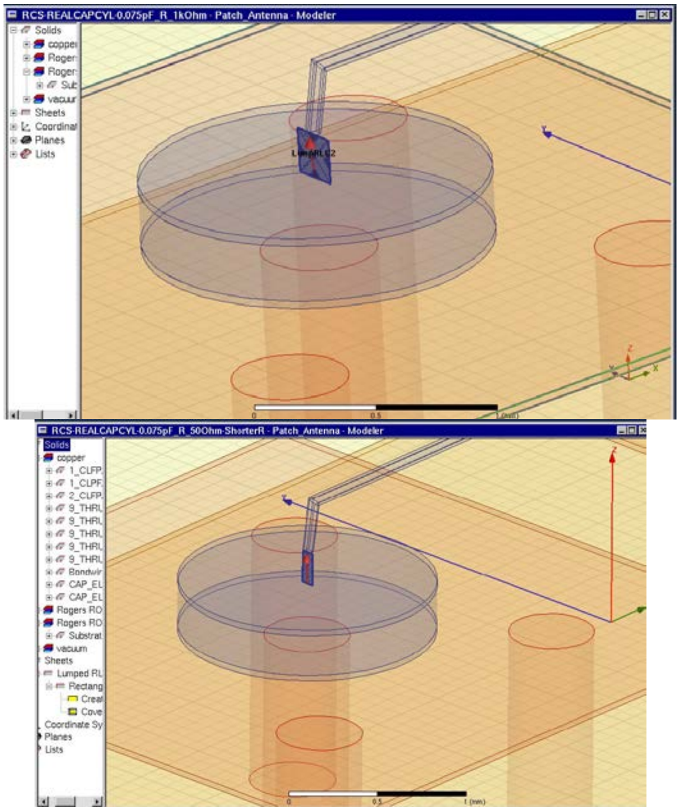


Fig. B. 34. Examples of lumped boundary conditions setups for the resistance computations with sheets of different size

.

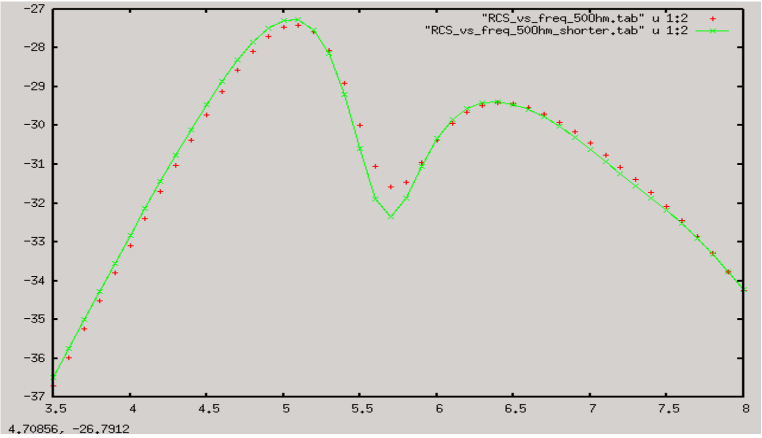


Fig. B. 35. Predicted (monostatic) RCS signals as functions of frequency with

Having verified the correct behavior when using a resistor in series (represented by a lumped boundary), a series of simulations were carried out with different values of the resistor. The results using different resistor values for 2 loading capacitance values are shown in Fig. B. 36 (C = 0.075 pF) and Fig. B. 37 (C = 0.15 pF). One can see that the zero-resistance data recovers those obtained previously with no resistor present. One can also see that increasing the resistor value results in the RCS dip gradually decreasing and eventually disappearing for R > 100 Ohm. This takes place at the same dip frequency, unlike the cases where using different wire inductances (or loading capacitances) resulted in the frequency shifts. The calculated dip disappearance and broadening of the resonance dip match the experiments (see Fig. B. 49 - Fig. B. 51). This provides another clear indication that these simulations can be used to provide guidance for future device designs.

Fig. B. 36 and Fig. B. 37 indicate that the variation of resonance peak with substrate resistance is not monotonic. Indeed, at low resistances of less than 10-20 Ohm, the dip becomes even more pronounced than in the case of no resistance (though the peak at lower frequencies does disappear). A complex RLC circuit (R - lumped resistivity, L - real wire inductance and C - real MOSCAP capacitance) can feature various resonances. Observation at low R (< 10 Ohm) can possibly be one of them. However, since resistivity is represented by a lumped (idealistic) boundary condition, the calculated behavior may not be fully realistic. Very sharp (and multiple) dips were observed a pure LC lumped boundary was used (see Fig. B. 27). Such sharp and multiple dips may not be fully realistic. In future efforts, instead of using a lumped R boundary, simulating the substrate resistance by adding a layer of finite (distributed) conductivity to the MOSCAP device may be considered. This way all three components (R, L, and C) will be modeled as real objects. However the expectation is that the trends obtained with the lumped R boundary will remain valid.

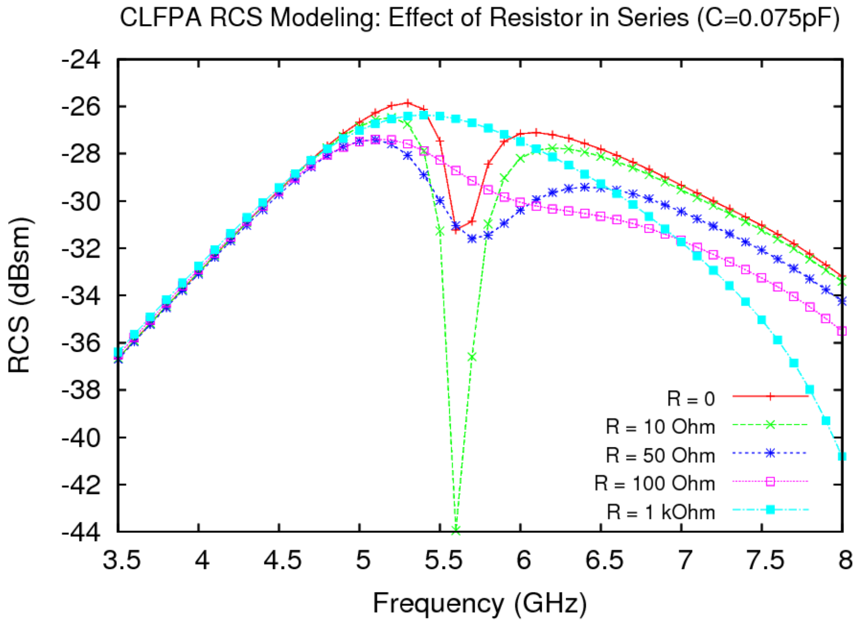


Fig. B. 36. Predicted (monostatic) RCS signals as functions of frequency for different values of the resistor in series. A loading capacitance of 0.075 pF is used.

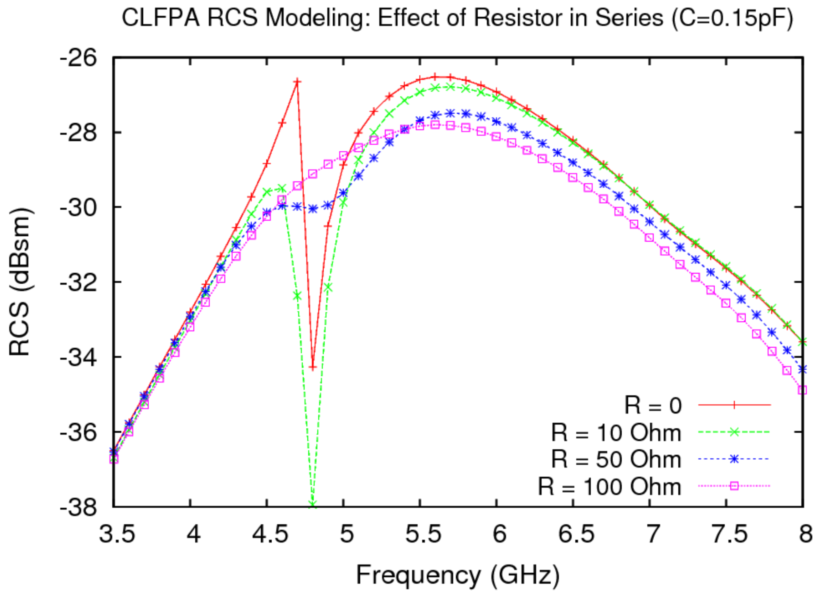
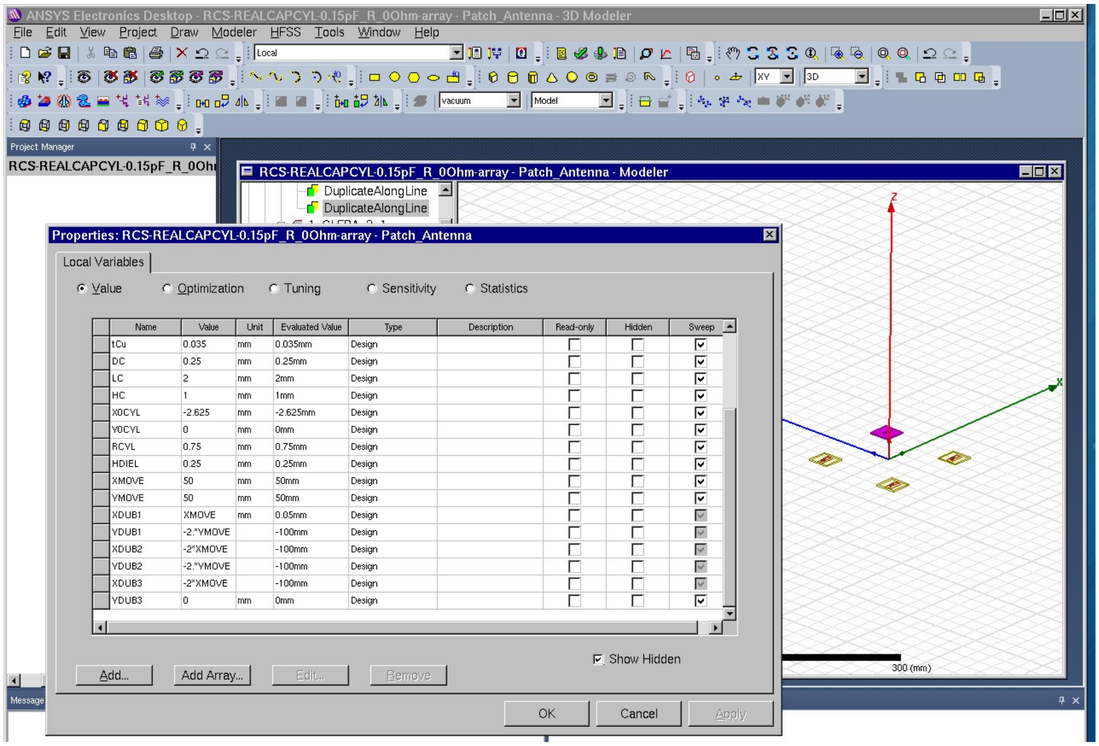


Fig. B. 37. Predicted (monostatic) RCS signals as functions of frequency for different values of the resistor in series. A loading capacitance of 0.15 pF is used.

Preliminary Antenna Array Simulations

Finally, preliminary studies of antenna arrays were performed, where instead of one patch antenna device, several devices were placed in an array. The main driving factor behind the use of such arrays is that the RCS signal can be increased by many orders of magnitude to make it more practical for reliable detection in noisy environments.

In order to setup an array of patch antennas, the design features of the HFSS software were used (as shown in Fig. B. 38 and Fig. B. 39) which allows convenient change of the geometry in a parametric manner (i.e., without manual repetition). Once such an antenna array is generated, one can set different boundary conditions on each element of the array if necessary (as shown in Fig. B. 40). An 2x2 antenna array was built as shown in Fig. B. 41 together with the radiation-only boundary box. (One should increase the outer box dimension to make sure that it can adequately represent the increased size of the antenna array).



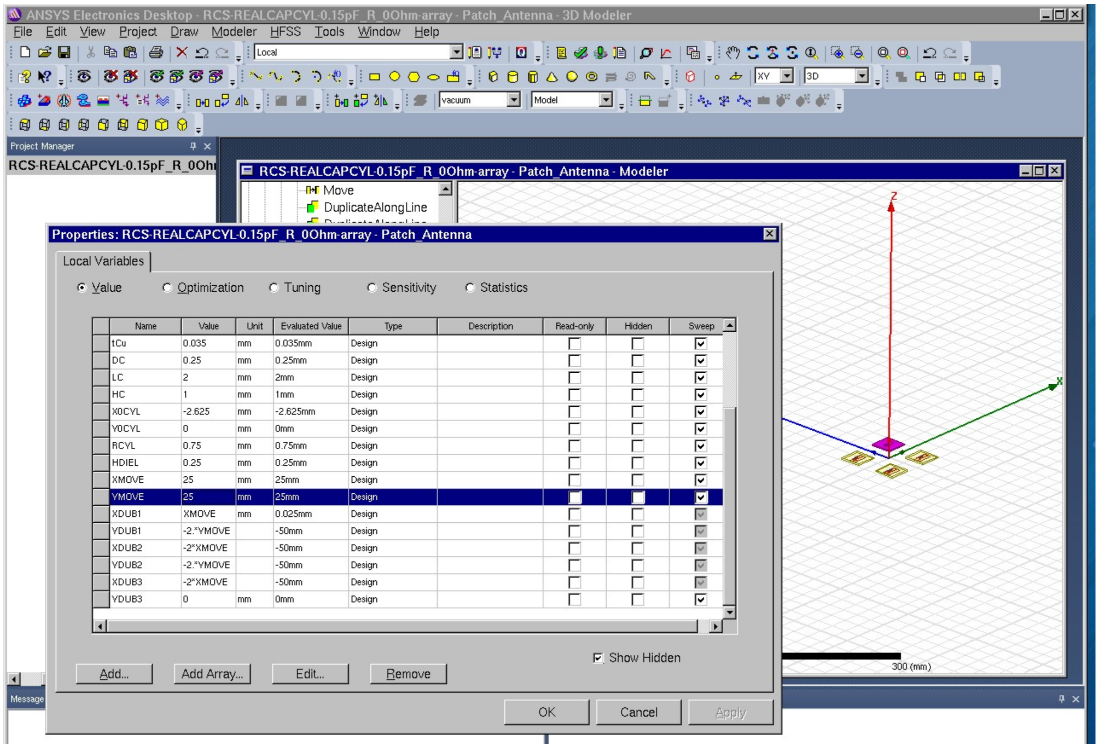
Properties: RCS-REALCAPCYL-0.15pF_R_0Ohm-array - Patch_Antenna

Local Variables

● Value ○ Optimization ○ Tuning ○ Sensitivity ○ Statistics

Name	Value	Unit	Evaluated Value	Type	Description	Read-only	Hidden	Sweep
tCu	0.035	mm	0.035mm	Design		☐	☐	☑
DC	0.25	mm	0.25mm	Design		☐	☐	☑
LC	2	mm	2mm	Design		☐	☐	☑
HC	1	mm	1mm	Design		☐	☐	☑
X0CYL	-2.625	mm	-2.625mm	Design		☐	☐	☑
Y0CYL	0	mm	0mm	Design		☐	☐	☑
RCYL	0.75	mm	0.75mm	Design		☐	☐	☑
HDIEL	0.25	mm	0.25mm	Design		☐	☐	☑
XMOVE	50	mm	50mm	Design		☐	☐	☑
YMOVE	50	mm	50mm	Design		☐	☐	☑
XDUB1	XMOVE	mm	0.05mm	Design		☐	☐	☑
YDUB1	-2.*YMOVE		-100mm	Design		☐	☐	☑
XDUB2	-2*XMOVE		-100mm	Design		☐	☐	☑
YDUB2	-2.*YMOVE		-100mm	Design		☐	☐	☑
XDUB3	-2*XMOVE		-100mm	Design		☐	☐	☑
YDUB3	0	mm	0mm	Design		☐	☐	☑

☑ Show Hidden



Properties: RCS-REALCAPCYL-0.15pF_R_0Ohm-array - Patch_Antenna

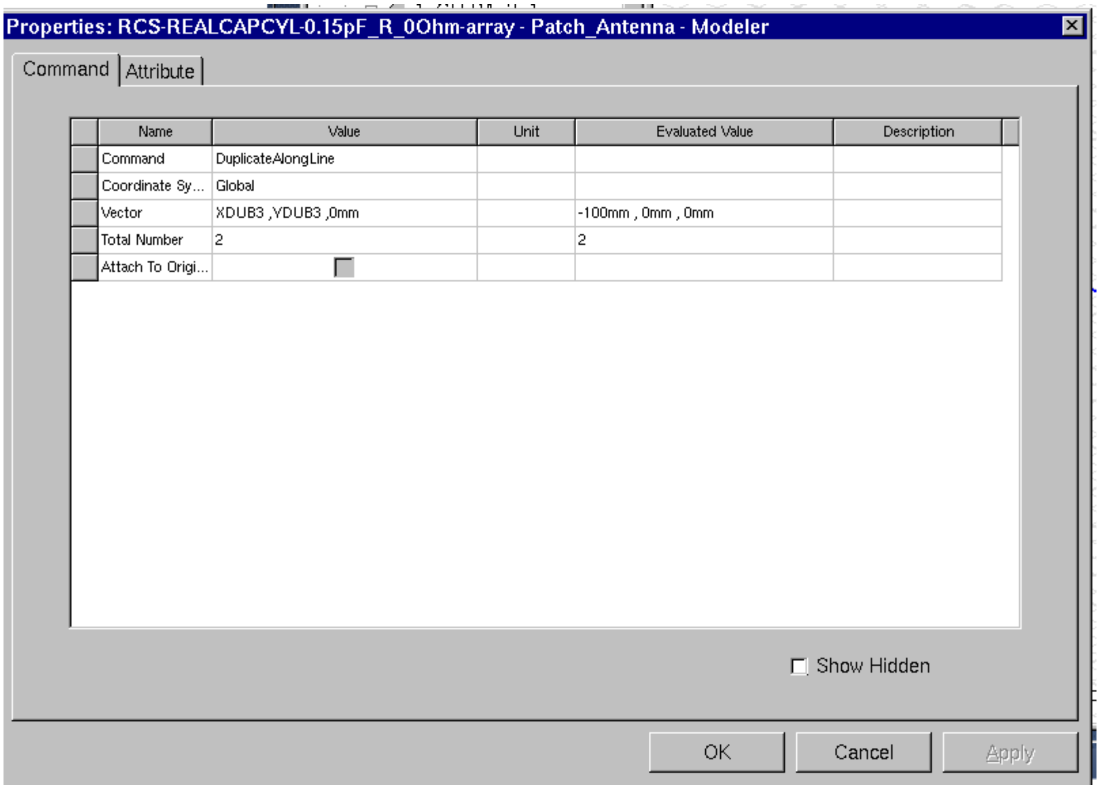
Local Variables

● Value ○ Optimization ○ Tuning ○ Sensitivity ○ Statistics

Name	Value	Unit	Evaluated Value	Type	Description	Read-only	Hidden	Sweep
tCu	0.035	mm	0.035mm	Design		☐	☐	☑
DC	0.25	mm	0.25mm	Design		☐	☐	☑
LC	2	mm	2mm	Design		☐	☐	☑
HC	1	mm	1mm	Design		☐	☐	☑
X0CYL	-2.625	mm	-2.625mm	Design		☐	☐	☑
Y0CYL	0	mm	0mm	Design		☐	☐	☑
RCYL	0.75	mm	0.75mm	Design		☐	☐	☑
HDIEL	0.25	mm	0.25mm	Design		☐	☐	☑
XMOVE	25	mm	25mm	Design		☐	☐	☑
YMOVE	25	mm	25mm	Design		☐	☐	☑
XDUB1	XMOVE	mm	0.025mm	Design		☐	☐	☑
YDUB1	-2.*YMOVE		-50mm	Design		☐	☐	☑
XDUB2	-2*XMOVE		-50mm	Design		☐	☐	☑
YDUB2	-2.*YMOVE		-50mm	Design		☐	☐	☑
XDUB3	-2*XMOVE		-50mm	Design		☐	☐	☑
YDUB3	0	mm	0mm	Design		☐	☐	☑

☑ Show Hidden

Fig. B. 38. (top and bottom). Array design settings defining the move and duplication parameters for two different distances between the array elements

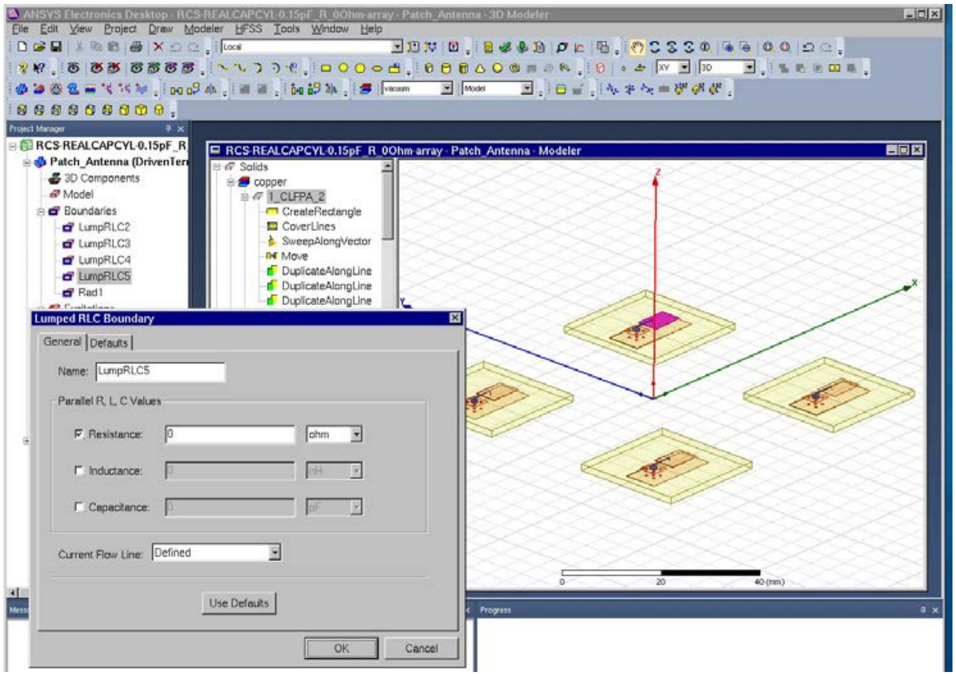


Properties: RCS-REALCAPCYL-0.15pF_R_0Ohm-array - Patch_Antenna - Modeler

Name	Value	Unit	Evaluated Value	Description
Command	DuplicateAlongLine			
Coordinate Sy...	Global			
Vector	XDUB3 ,YDUB3 ,0mm		-100mm , 0mm , 0mm	
Total Number	2		2	
Attach To Origi...	☐			

☐ Show Hidden

Fig. B. 39. Array design settings defining the move and duplication parameters



ANSYS Electronics Desktop - RCS-REALCAPCYL-0.15pF_R_0Ohm-array - Patch_Antenna - 3D Modeler

Lumped RLC Boundary

Name: LumpRLC5

Parallel R, L, C Values

☑ Resistance: 0 ohm

☐ Inductance: 0 nH

☐ Capacitance: 0 pF

Current Flow Line: Defined

Fig. B. 40. Lumped boundary conditions settings for antenna array

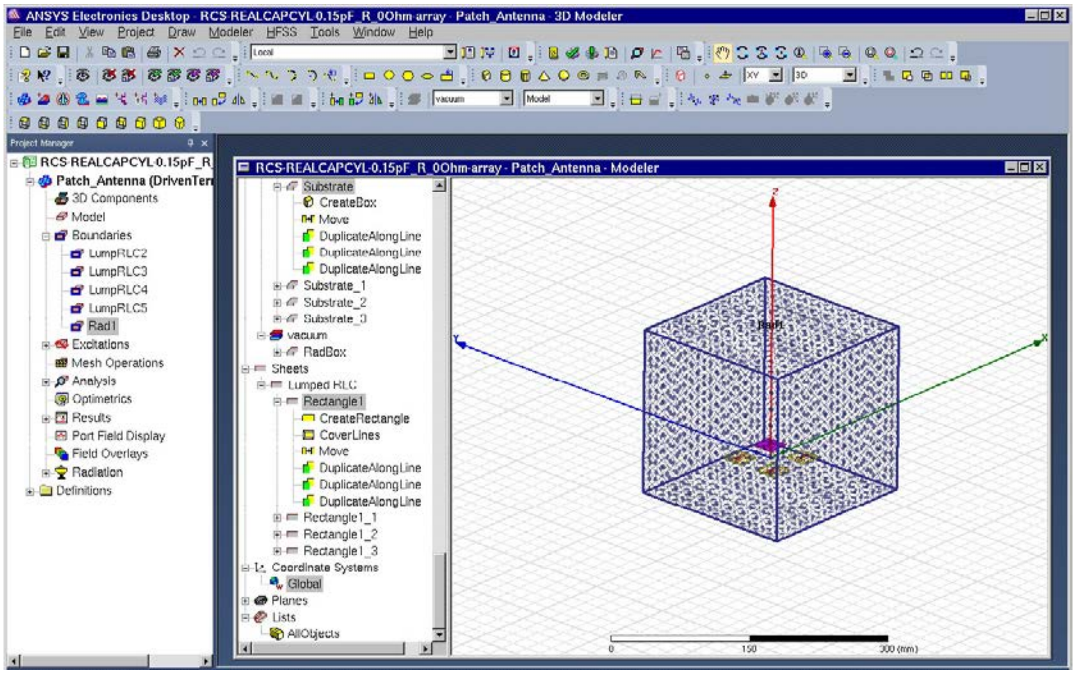


Fig. B. 41. 2x2 antenna array overview with the radiation-only box

Having built such an antenna array preliminary studies were conducted by changing the distance between the elements of the array. Studies were conducted for distances of 50 mm (see Fig. B. 40) and 25 mm (see Fig. B. 42)

The results of computations are shown in Fig. B. 43. One can see that the RCS signal for the 2x2 antenna array increases significantly (by about 12 dBsm). One can estimate such increase by recalling that

$$\text{dBsm} = 10\times\log_{10}(\text{RCS}/1\text{m}^2)$$

For an array of (independent) antennas a simple formulation would be:

$$\text{dBsm} = 10\times\log_{10}(\text{N}\times\text{RCS}/1\text{m}^2)$$

where N is the number of antennas in the array. For N = 4, RCS signal increases by a factor of $10\times\log_{10}(4) \sim 6$ dBsm. An increase of 12 was observed which can be explained by the fact that, the total cover area increases by more than a simple factor of 4. Another interesting fact is that, the RCS dip disappears when the devices are closely placed (25 mm distance). This might be due to the interference of the RCS signals when the distance becomes smaller or comparable to the EM wavelength (~37 mm at 8 GHz). These facts clearly indicate that one should carefully design the antenna array to get the optimum

RCS signal. This will be the subject of the future modeling and experimental efforts in Phase II.

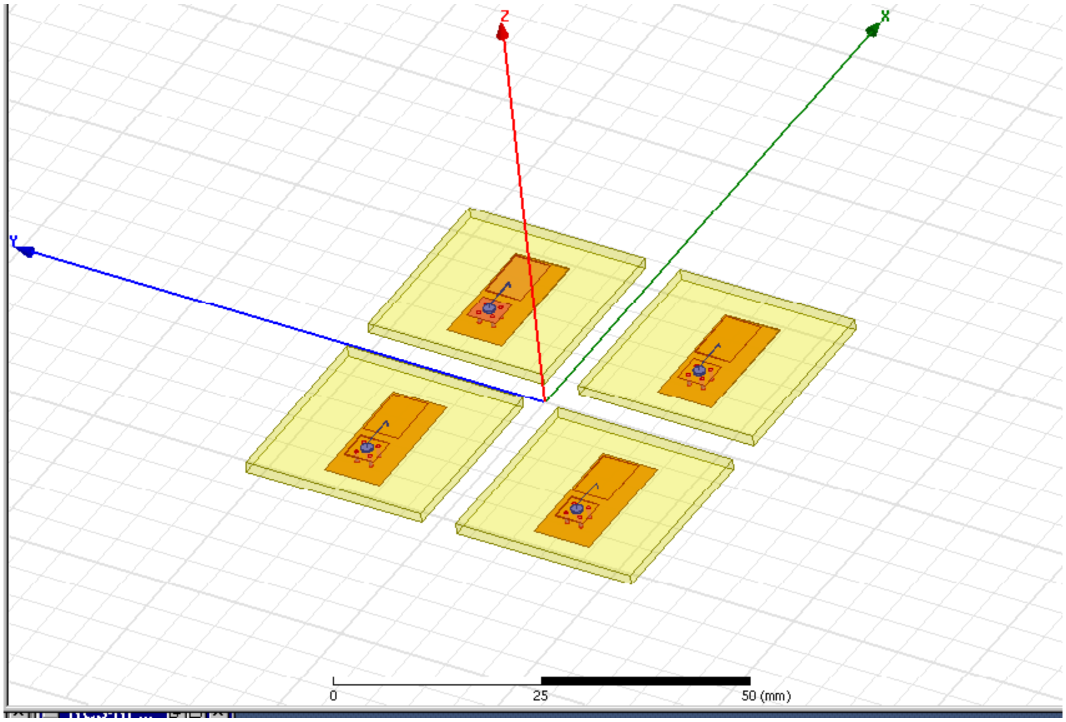


Fig. B. 42. Antenna array for distance between the elements of 25 mm

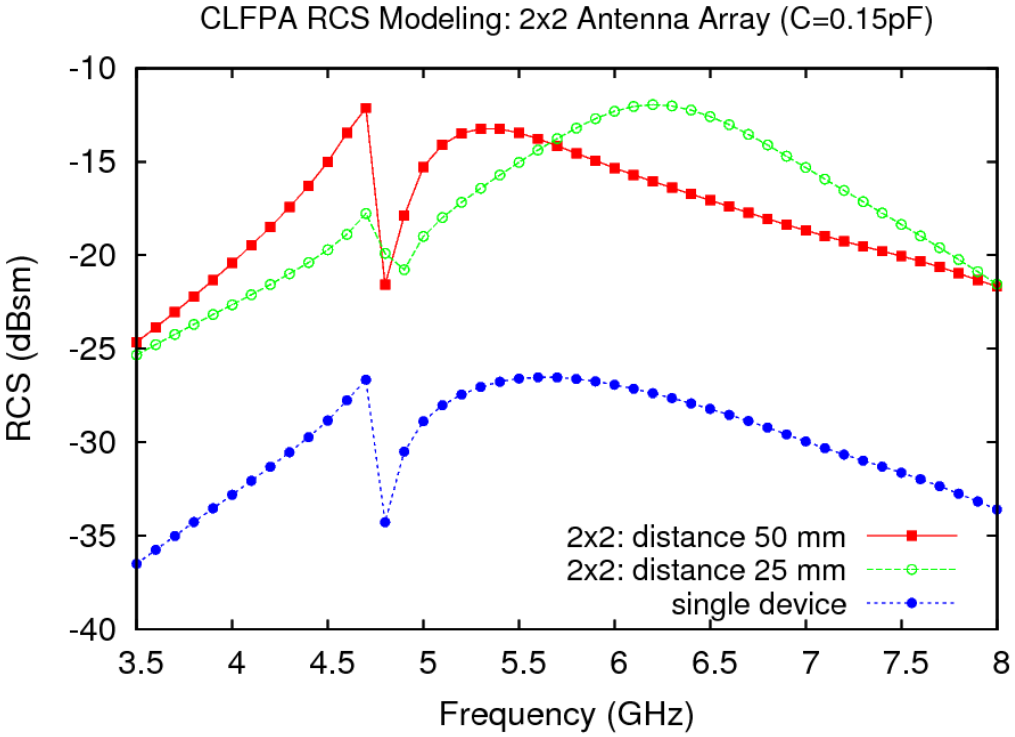


Fig. B. 43. Predicted (monostatic) 2x2 antenna array RCS signals as functions of frequency for different distances between elements. A loading capacitance of 0.15 pF is used with no resistance in series.