Gallium Phosphide Integrated with Silicon Heterojunction Solar Cells

by

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ABSTRACT

It has been a long-standing goal to epitaxially integrate III-V alloys with Si substrates which can enable low-cost microelectronic and optoelectronic systems. Among the III-V alloys, gallium phosphide (GaP) is a strong candidate, especially for solar cells applications. Gallium phosphide with small lattice mismatch (~0.4%) to Si enables coherent/pseudomorphic epitaxial growth with little crystalline defect creation. The band offset between Si and GaP suggests that GaP can function as an electron-selective contact, and it has been theoretically shown that GaP/Si integrated solar cells have the potential to overcome the limitations of common a-Si based heterojunction (SHJ) solar cells.

Despite the promising potential of GaP/Si heterojunction solar cells, there are two main obstacles to realize high performance photovoltaic devices from this structure. First, the growth of the polar material (GaP) on the non-polar material (Si) is a challenge in how to suppress the formation of structural defects, such as anti-phase domains (APD). Further, it is widely observed that the minority-carrier lifetime of the Si substrates is significantly decreased during epitaxially growth of GaP on Si.

In this dissertation, two different GaP growth methods were compared and analyzed, including migration-enhanced epitaxy (MEE) and traditional molecular beam epitaxy (MBE). High quality GaP can be realized on precisely oriented (001) Si substrates by MBE growth, and the investigation of structural defect creation in the GaP/Si epitaxial structures was conducted using high resolution X-ray diffraction (HRXRD) and high resolution transmission electron microscopy (HRTEM).

The mechanisms responsible for lifetime degradation were further investigated, and it was found that external fast diffusors are the origin for the degradation. Two practical

approaches including the use of both a SiN_x diffusion barrier layer and P-diffused layers, to suppress the Si minority-carrier lifetime degradation during GaP epitaxial growth on Si by MBE were proposed. To achieve high performance of GaP/Si solar cells, different GaP/Si structures were designed, fabricated and compared, including GaP as a hetero-emitter, GaP as a heterojunction on the rear side, inserting passivation membrane layers at the GaP/Si interface, and GaP/wet-oxide functioning as a passivation contact. A designed of a-Si free carrier-selective contact MoO_x/Si/GaP solar cells demonstrated 14.1% power conversion efficiency.

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Chapter 1

INTRODUCTION

1.1 Need for Solar Energy

The renewable energy is increasing rapidly as a result of the exhaustion of fossil fuels and environment pollution issues. Photovoltaics as one of the renewable energy has developed from a niche market into a significant energy source for the over three decades, which can realize the electricity generation allowing locally generated, high efficiency, scalable and environmentally benign energy systems.

The installed capacity of PV systems has increased dramatically over the last years. As reported by International Energy Agency (IEA) [1], 24 countries have passed the gigawatt (GW) PV installation mark and the 300 GW mark has been reached. In 2017, the solar ranked No. 2 source of new electric generating capacity with 30% in the U.S. [2]. However, the negative impact of high PV penetration is an obstacle for residential PV installation. Among the issues are the technical impacts of non-dispatchable generation on grid stability and a possible rapid increase in demand on conventional generators when photovoltaic power decreases (e.g. "duck curves"). These concerns, along with decreases in the price of PV systems, have led to reduced incentives or disincentives for customers to adopt PV, including reduced subsidies for PV systems purchase. To estimate the cost of electricity generated by photovoltaic (PV), a parameter called levelized cost of electricity (LCOE) can be used for analysis. It was analyzed the levelized price of electricity paid by owners of residential PV systems under various revised net metering policies and show that the price of electricity including battery systems can still achieve residential grid parity

[3]. The benefits of PV systems with storages could encourage the adoption of PV systems and the PV market will keep increase.

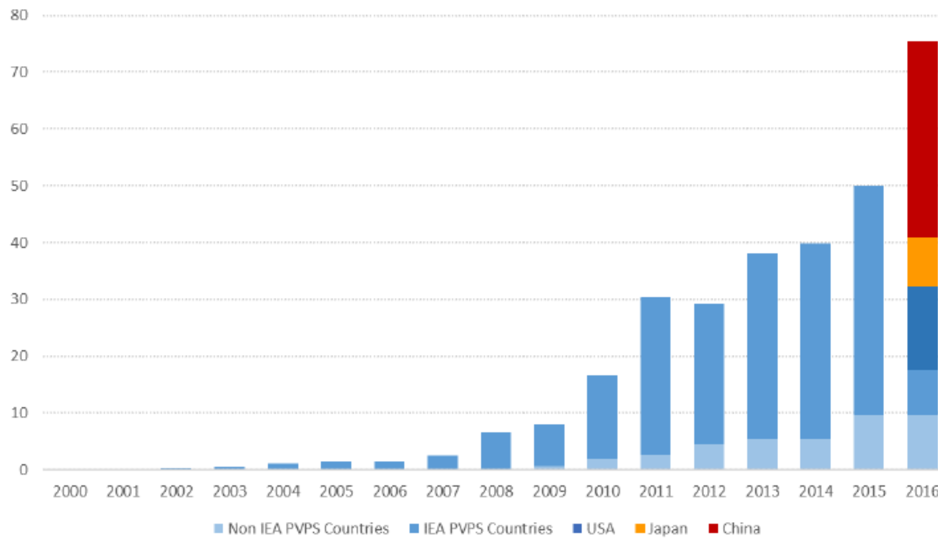

Figure 1-1 The evolution of annual PV installations [1].

1.2 The Potential of III-V/Si Solar Cells

Silicon solar cells are the most commercial due to their low cost comparing to other types of solar cells. Currently, solar cell technology based on silicon substrates is the dominant commercial photovoltaic technology, while the record Si solar cells have exceeded 26% conversion efficiency [4]. The properties of III-V solar cells, such as their direct energy bandgap and high absorption coefficient, make them become much potential to be widely used. In order to improve the efficient of light usage, multijunction solar cells and intermediate bands solar cells have attracted a lot of attention over the past two decades. Multijunction solar cells allow higher efficiency than single junction solar cells by enabling both high voltage and absorption of a large portion of the solar spectrum. "Champion" efficiency tandem solar cells have shown efficiency of 46% under

concentrated sunlight (508 suns) [5]. Despite these high efficiencies, wide spread commercial use of concentrating photovoltaics requires further cost reductions. Cost analysis [6] as shown in the Figure 1-2 of the lattice matched (LM) multijunction solar cells shows that the Ge or GaAs epi-wafer used as a substrate or bottom cell is the major cost of today's concentrated photovoltaics (CPV) technology. Replacement of the bottom Ge or GaAs substrates by Si can dramatically reduce cost and enable CPV technology for large-scale terrestrial applications.

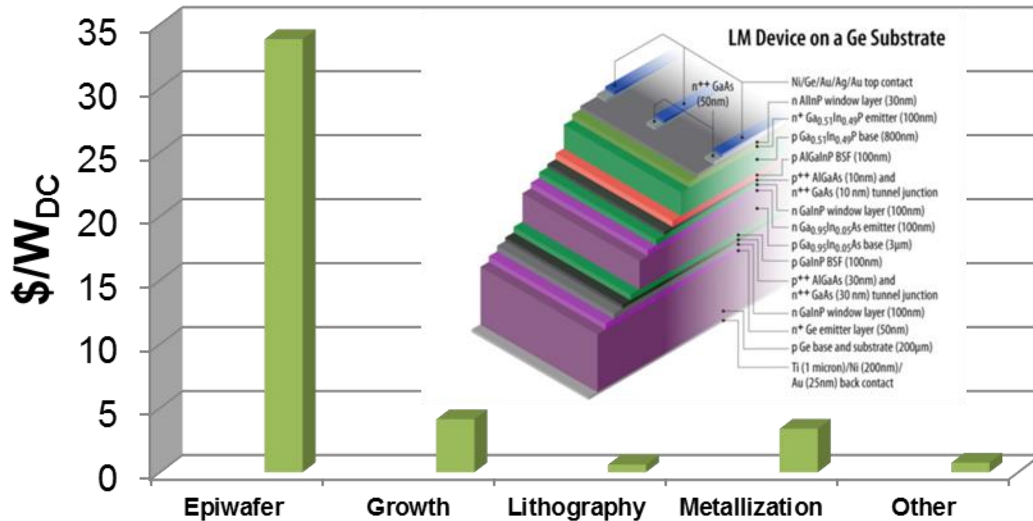

Figure 1-2 Cost analysis of a high concentration PV module and inserted figure is a typical structure of a lattice-match device on a Ge substrate [6].

High efficiency of Si-based solar cells, coupled with the steady increase efficiency of III-V compound semiconductor based solar cells enables high efficiency tandem solar cells. In addition, a tandem solar cell with Si as the active bottom layer integrated with III-V is promising for large scale production, allowing larger wafer sizes.

1.3 Epitaxial Challenges

Si with its small mass, good thermal conductivity, and low cost is a good candidate as the substrate of III-V compounds. However, the crystalline defects, such as anti-phase domains (APD) generated of these III-V on Si structures due to the lattice mismatch, difference in thermal expansion coefficients and polar-on-nonpolar interface.

In the heteroepitaxial growth, the relaxation is known to occur by the formation of misfit dislocations and/or stacking faults. The lattice mismatch strain is defined as $f \equiv \frac{a_{sub}-a_{epi}}{a_{epi}}$, where a_{sub} and a_{epi} are the relaxed lattice constant of the substrate and the epitaxial layer, respectively. For $a_{sub} < a_{epi}$, $f < 0$, it is called a compressive system, while it is a tensile system for $a_{sub} > a_{epi}$. In the low lattice mismatch heteroepitaxial growth ($|f| < 1\%$), the initial growth tends to be coherent/pseudomorphic and the epitaxial layer is fully stained on the substrate as shown in Figure 1-3(a). The stain energy increases as the epitaxial layer thickness increases. When it reaches to some thickness (critical thickness), it becomes energetically favorable for the introduction of misfit dislocations to release some strain. In the partially relaxed layer as schematic in Figure 1-3(b), the in-plane lattice constant of the epitaxial layer has not relaxed to fully relaxed value, but it is greater than the substrate lattice constant ($a_{sub} < a < a_{epi}$) and so some of the mismatch is still accommodated by the elastic strain. A portion of the mismatch is accommodated by misfit dislocations called plastic strain.

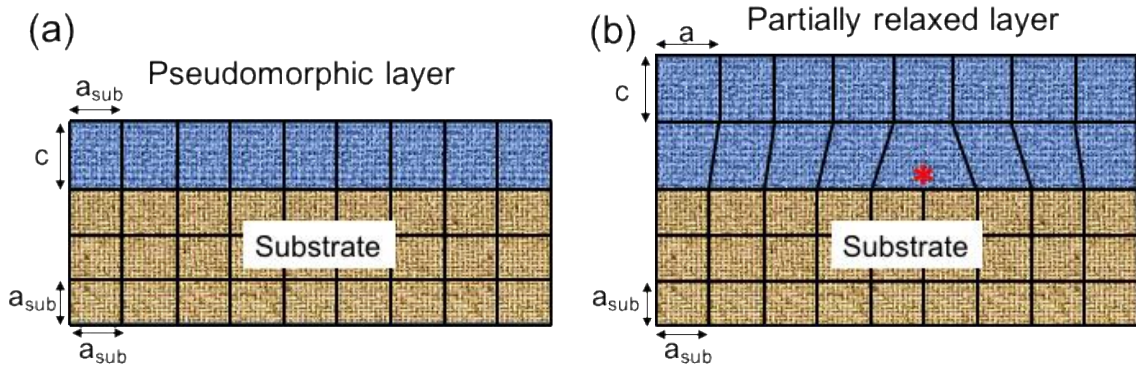

Figure 1-3 Growth of a heteroepitaxial layer on a mismatched substrate with two different cubic lattice constants: (a) pseudomorphic layer; (b) partially relaxed layer (star mark presents the misfit dislocations).

The lattice mismatch between GaAs and Si is about 4%, while GaP and Si has one order small lattice mismatch of 0.4%. Low-lattice-mismatched GaP epitaxially grown on Si substrates enables a pseudomorphic layer growth and provides a path for the high quality epitaxial growth of III-V materials for multijunction solar cells applications.

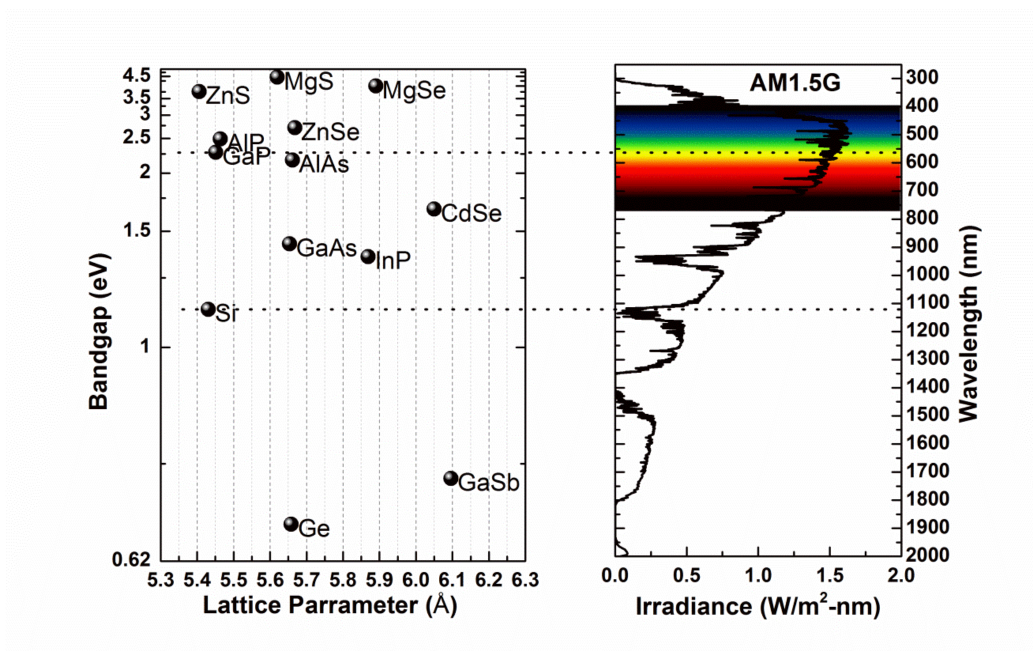

Figure 1-4 Lattice constants and bandgap of III–Vs, Si, and Ge at 300 K, and AM1.5G spectrum.

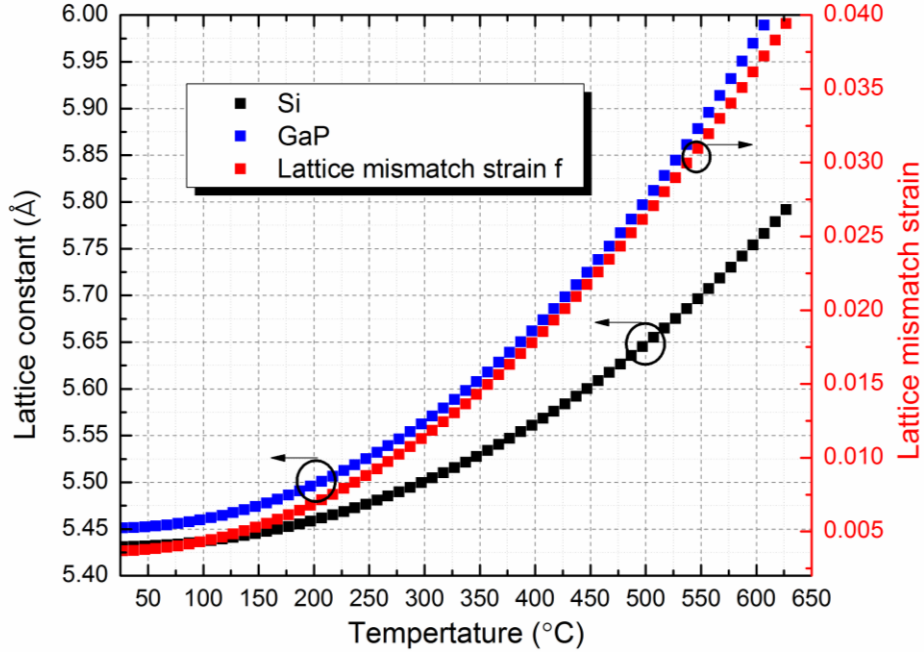

Figure 1-5 The lattice constant of GaP and Si at various temperatures, and also the corresponding lattice mismatch strain.

For different temperatures, the lattice constant of an epitaxial layer can be calculated: $a(T) = a(300K)[1 + \frac{A+BT+CT^2+DT^3}{100}]$, where the constants A, B, C, and D are thermal expansion coefficients. The thermal expansion coefficient of GaP is larger than those of Si, and so GaP should have a larger lattice constant than Si at the growth temperature. The lattice mismatch between GaP and Si increases as the temperature increases as shown in Figure 1-5. High quality thin GaP layers grown on Si using molecular beam epitaxy (MBE) have been recently reported by many researchers [7]–[10]. Compared to metalorganic chemical vapor deposition (MOCVD), the growth of GaP on Si via MBE is at much lower temperature and much lower V/III ratio, *i.e.* lower P flux. Growth parameters, such as substrate temperature, V/III flux ratio, growth rate and growth methods are affecting the quality of GaP on silicon substrate. During the GaP initial nucleation

stage, it is a common issue that the formation of separate large-sized islands that the coalescence contributes high density of defects and it shows the formation of point reflections characterizing as 3D growth observed from the *in-situ* reflection high-energy electron diffraction (RHEED). It was shown that GaP was nucleated on the Si by migration-enhanced epitaxy (MEE) and molecular beam epitaxy (MBE) methods at GaP/Si initial growth stages [11]. The clear isolated islanding growth was observed in the case of MBE growth, while the MEE growth, alternating Ga and P layers, formed wider lateral size and lower height which indicates that MEE growth enhances the two-dimensional (2D) growth. Therefore, it is critical to optimize the GaP growth conditions and growth methods to achieve high quality of GaP layers on Si substrates.

1.4 GaP/Si Heterojunction Solar Cells

As shown in Figure 1-6a, in a typical heterojunction (SHJ) solar cell, optimized intrinsic a-Si as passivation and p-type doped a-Si for forming a p-n junction with the substrate. The a-Si layers on the front have excellent passivation for the substrate, while a transparent conductive oxide (TCO) is required to provide lateral transport of the collected carriers to the metal electrode grid. However, most of the carriers generated in the front layers (a-Si:H, TCO) are lost due to recombination, parasitic absorption loss, which limits the ultimate performance of these SHJ solar cells. Potential gain in current density is up to 2.1 mA/cm^2 [12]. High bandgap, low optical absorption and high mobility should be integrated with silicon to minimize parasitic loss. GaP with high bandgap (2.26 eV) and indirect bandgap is promising for reducing parasitic loss at the front of silicon solar cells. In addition, a carrier-selective contact (CSC) (Figure 1-6b) on silicon substrates has been

scrutinized to develop high efficiency heterojunction silicon solar cells by effectively separating minority carriers. GaP, whose band offset with Si at the valence band ΔE_v=1.05 eV and at the conduction band ΔE_c=0.09 eV [13], is considered to be an excellent candidate as an electron selective contact for silicon.

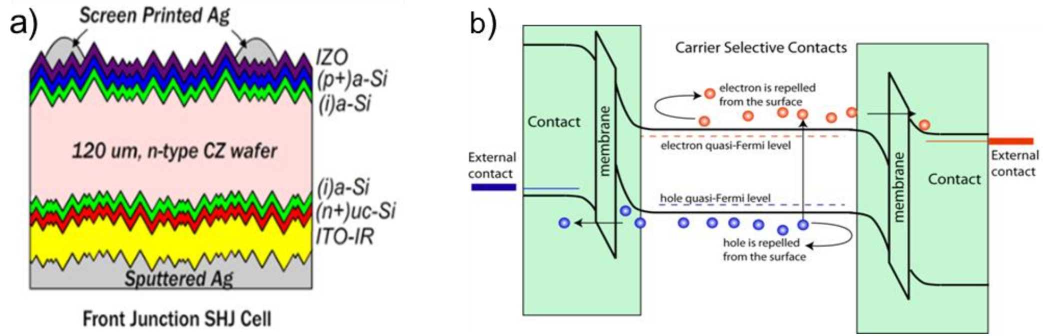

Figure 1-6 (a) Typical front junction silicon heterojunction (SHJ) cell. (b) Schematic of carrier-elective contacts (CSC).

1.5 Thesis Structure

In this manuscript, first the epitaxial growth of GaP by MEE and MBE methods is discussed, and the structural defects formation is investigated via high resolution X-ray diffraction (XRD) and transmission electron microscopy (TEM) in Chapter 2. Chapter 3 is devoted to reveal the Si minority-carrier lifetime degradation issues during GaP growth on Si in the MBE chamber and two approaches are proposed to suppress the lifetime degradation during III-V on Si integration. Chapter 4 describes GaP as a heteroemitter in GaP/Si solar cells and electrical properties are compared for different structures. Chapter 5 compares different heterojunction GaP/Si solar cells with GaP as an electron-carrier selective contact on the back and different approaches are analyzed to improve the device performances of GaP/Si solar cells. In Chapter 6, GaP was deposited on passivation membrane layers and the device performance is discussed. Chapter 7 is describing a novel

structure with GaP/wet-oxide functional as passivation layers for Si wafers and such solar cells are demonstrated. Chapter 8 is a summary of this dissertation and also an outlook for this work.

Chapter 2

GAP EPI-GROWTH ON SI VIA MBE

2.1 Introduction

It has been a long-lasting goal to epitaxially integrate III-V alloys with Si substrates [14], which can enable low-cost microelectronic and optoelectronic systems. Structural degradation during the growth of III-V compounds on Si due to the non-zero lattice mismatch is the main obstacle for developing high performance optoelectronic devices. It is a challenge to integrate polar III-V materials onto non-polar Si substrates. Among all the III-V alloys, GaPN can be lattice-matched to Si, however, the however, the direct growth of nitride alloy will generate other crystalline defects on the interface by the creation of silicon nitride on the Si surface [15]. Gallium phosphide (GaP), which has a relatively small lattice mismatch (0.37%) with Si, is a good candidate, such as serving as a buffer layer, for this III-V/Si integration, especially for multijunction solar cell applications [16], and many other solar applications [17], [18]. The almost pseudomorphic growth of GaP-based materials on Si can address this issue by delaying the onset of defect creation. However, symmetry change at the diamond-zinc blende interface additionally affects defect creation during epitaxial growth.

It was shown that degradation of crystal quality of GaP layers grown on Si substrate can be delayed by using the migration-enhanced epitaxy (MEE) technique and a post-growth annealing procedure [9], [10], [16], [19], [20]. Although the off-cut ($\geq 4^{\circ}$) Si wafers have been demonstrated reduced density of anti-phase domains (APD) [7], [20]–[23], precisely orientated Si(001) wafers are widely used in the standard complementary metal oxide semiconductor (CMOS) logic circuit fabrication [24] and solar cell structures.

Therefore it is important to investigate the defect formation for the GaP layers grown on the off-cut and exactly oriented Si(001) substrates under the same growth conditions. Due to the lattice mismatch pseudomorphic layers can be grown almost coherently strained, but beyond the specific layer thickness, depending on growth conditions, amount of already created misfit dislocations becomes sufficient to relieve relaxation some of the mismatch stress [24]. In the GaP/Si heteroepitaxial system initially by low lattice mismatch and symmetry change deteriorated it is critical to understand thickness related defect creation during the stress relaxation for comparison with low lattice mismatched III-V on III-V epitaxial structures [25].

In this chapter, a defect-free GaP layer on an off-cut Si substrate by MEE was grown, and the same growth condition was applied to a precisely oriented Si substrate. Later, GaP layers were grown by traditional MBE growth procedure with optimizing the V/III ratio and a series of GaP structures were grown for revealing the defects formation in the GaP/Si system. High-resolution X-ray diffraction (XRD) and transmission electron microscopy (TEM) structural investigations were conducted to reveal correlations between the growth conditions and the crystal perfection of the epitaxial structures.

2.2 Experimental Setup

2.2.1 Epitaxial Growth of GaP-Si(001) structures

The GaP epitaxial layers were grown on Si(001) substrates using a solid-source Veeco GEN III MBE system with a phosphorus valved cracker. The Si wafers were n-type float-zone material, precisely oriented (001) or with 4° offcut towards the [110] direction. This wafer misorientation should help to form double steps on the substrate surface during epitaxial growth and possibly minimize APD creation during GaP epitaxial growth [24].

Prior to deposition, Si wafers were chemically cleaned using the standard RCA solution, which was finally combined with 5% hydrogen fluoride (HF) for surface refresh. The GaP layers were grown on the Si substrates following preheating at 820℃ for 5 min to fully remove the residual native silicon oxide layer. Surface reconstructions during the preheating and deposition were monitored in situ by reflection-high-energy electron diffraction (RHEED). Initially, under the presence of the native oxide, (1×1) RHEED patterns were observed, while clear and streaky (2×1) patterns, indicative of native-oxide removal and perfect surface reconstruction, were observed after the substrate preheating. After annealing, the substrate temperature was then decreased to the growth temperature for epitaxial growth.

Two MEE-grown GaP-Si(001) heterostructures of 50-nm GaP layer thickness were deposited at 440℃ onto off-cut (MEE-I structure) and precisely oriented (MEE-II structure) Si wafers. The deposition loop consisted of a sequence of 5 second Ga deposition, 1 s pause with closed Ga and P sources, 8 s exposure under P flux, and 5 s pause, with the loop being repeated for a total of 184 cycles. Before commencing MEE growth, the P shutter was opened for 30 s and then closed for 12 s before the initial Ga deposition. The P and Ga flux ratio was about 5.

Together with the MEE growth process, a traditional MBE growth method for GaP layers was investigated. To optimize the growth conditions for GaP on precisely oriented (001) Si substrates, different V/III (P/Ga) ratios from 6.9 to 3.1 were conducted at 580°C at a growth rate of 0.52 μm/hr. A well below the critical thickness 37 nm GaP was epitaxially grown. At the initiation of growth, the P shutter was open for 20 s for P deposition, then 10 loops of (GaP-P) short-period quasi-super lattice with 5 s GaP

deposition and 5 s pause under P-flux were applied to improve the planarity of the growth front, and then the main growth process was started. Several GaP-Si(001) epitaxial structures with GaP layer thicknesses ranging from 37 nm up to 2 μm were epitaxially grown by MBE using a P/Ga ratio of ~ 4.5, which is the optimized growth condition for epitaxial growth at 580°C and precisely oriented wafers.

2.2.2 Characterization Methods

High-resolution XRD studies were performed using an X'Pert MRD diffractometer with a multilayer focusing mirror under double- and triple-axis alignment. Hybrid Ge(220) monochromator ensured 18 arc.sec collimated and monochromatic CuKα-1 incident radiation, while a Ge(220) analyzer with 12 arc.sec acceptance angle allows spatially separate coherent and diffuse-scattered radiation in the vicinity of the (004) and (224) reflections. Coherent double-crystal (DC) and triple-crystal (TC) ω-2θ and ω rocking curves (RCs) were used to determine layer composition and strain conditions to specify the type, spatial distribution, and density of crystal defects. Atomic force microscopy (AFM) was conducted by multimode scanning probe microscope (SPM) to study the surface morphology.

Specimens suitable for TEM observation were prepared using focused-ion-beam milling as well as additional argon-ion-milling to remove some surface milling artifacts. Observations were made with a FEI-Philips CM200 high-resolution electron microscope, operated at 200 keV, equipped with a double-tilt specimen holder, and an aberration-corrected ARM-200F microscope. Cross-section observations were made along {110}-type zone axes so that the surface normal would be perpendicular to the incident-beam direction.

2.3 Results and Discussion

2.3.1 Investigation of MEE-grown Structures

50-nm-thick GaP layers were epitaxially grown on two Si substrates, one 4º offcut (MEE-I structure) and one precisely oriented (001) Si wafers (MEE-II structure). Strong and extended interference pattern around GaP peak on DC ω-2θ RC and narrow coherent central peak without diffuse base on TC ω RC as shown in Figure 2-1a, b (black curves) confirm high crystal perfection of GaP layer grown on off-cut Si wafer. Based on the FWHM of the TC ω RC the bending of the structure is low, while volumetric density of crystal defects may be evaluated as $\sim 2\times10^{5}$ cm^{-2}.

On the other hand, noticeable diffusion of GaP related interference pattern for the DC ω-2θ RC of the MEE-II structure (Figure 2-1a, b red curves) means the deterioration of X-ray vertical scattering coherence of the GaP layer, which is caused by crystal defects with edge segment(s) in the volume of the epitaxial layer created during epitaxial growth. Most probably, these defects would be identified as stacking faults, created on the interface and intersected in the volume of the epitaxial layer, diminishing vertical coherence of the epitaxial layer. The diminished intensity of the central narrow peak and the wide diffuse base for the MEE-II TC ω RC confirms this suggestion. FWHM (≈ 600 arc.sec) of diffuse base allows evaluate the density of these defects as $\sim 1.3\times10^{9}$ cm^{-2}. Low intensity of diffused scattered radiation suggests that despite high density these defects occupy relatively small volume of the epitaxial layer, while narrow central coherent peak means that the elastic stress caused by these defects do not overlap in the layer and hence do not deteriorate entire volume of the epitaxial layer as well.

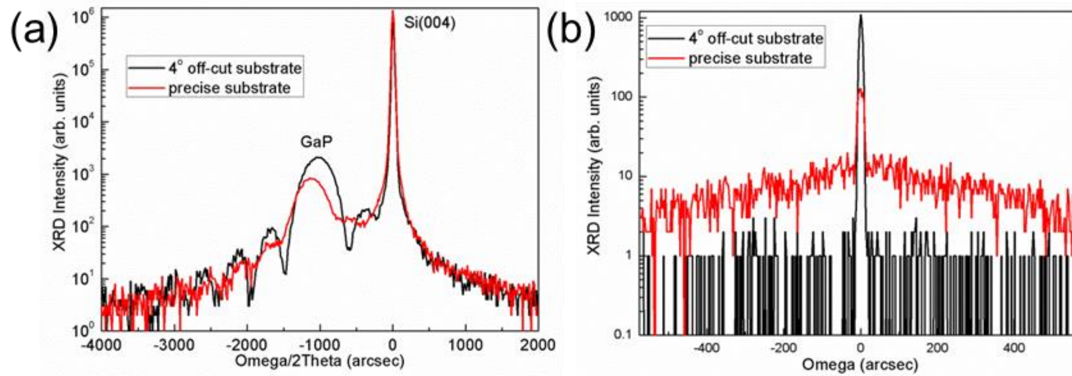

Figure 2-1 (a) DC coherent ω-2θ RCs measured in the vicinity of Si-GaP (004) reflections. (b) The corresponding GaP TC ω RCs.

TEM cross-section micrographs (Figure 2-2) visually confirm the trends of the XRD results. The MEE-I structure (Figure 2-2a) showed no extended crystal defects over large lateral distances. By comparison, the MEE-II GaP sample (Figure 2-2b) revealed many stacking faults and multiple twins in the volume of the GaP layer, some of them with stacked planes (red circles), others without. Therefore, defect-free GaP can be grown on the off-cut Si substrate at this MEE growth condition, however, it is not suitable for the precisely orientated Si substrate.

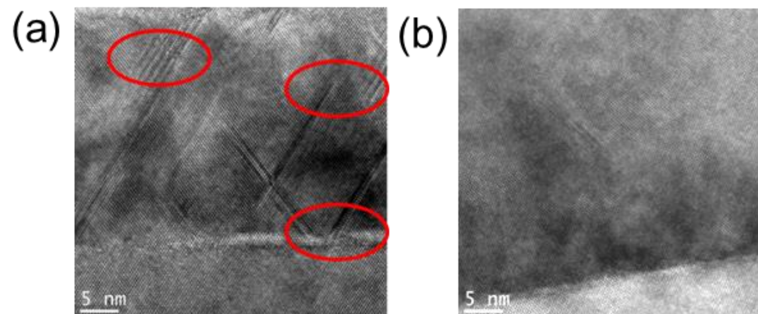

Figure 2-2 TEM cross-section micrographs of MEE grown structures: (a) GaP grown on precise Si wafer (MEE-II structure), (b) GaP grown on offcut Si wafer (MEE-I structure).

2.3.2 Investigation of MBE-grown Structures

A thickness of 37 nm GaP layer was grown by MBE procedure on Si substrates with different P/Ga ratio and the AFM measured surface morphology is shown in Figure 2-3. As the P flux reduced from P/Ga ratio of 6.9, the surface becomes smooth and the peak-to-valley distance is reduced to 4.3 nm at the P/Ga ratio of 4.5. If the flux ratio decreases below 4.3, the P flux is not sufficient to maintain P-stable surface and Ga droplets form and producing rough surface, which is consistent with [21]. From HR-XRD measurement to these samples (Figure 2-4), the sample grown at 580°C with 4.5 P/Ga flux ratio demonstrates the highest crystal perfection (ω-2θ and ω RCs look similar to 4° off-cut MEE structure RCs on Figure 2-1a, b) and lowest dislocation density, estimated as 2.6×10^5 cm^{-2}. The TEM (Figure 2-5) shows an abrupt and coherent GaP/Si interface and although the top surface is slightly uneven there are virtually no structural defects visible in the GaP layer across large lateral distances. However, antiphase boundaries can be observed from the TEM image in Figure 2-5b, which was formed during GaP epitaxially grown on the single step surface of precisely oriented Si substrate.

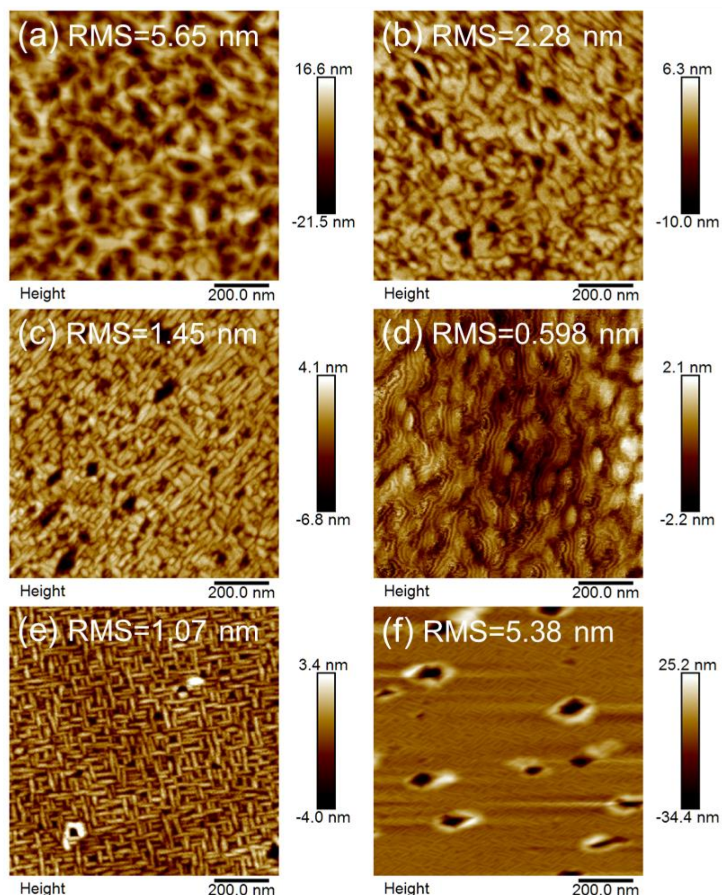

Figure 2-3 1μm×1μm AFM for different P/Ga flux ratio: (a) 6.9; (b) 5.9; (c) 4.8; (d) 4.5; (e) 4.3; (f) 3.1.

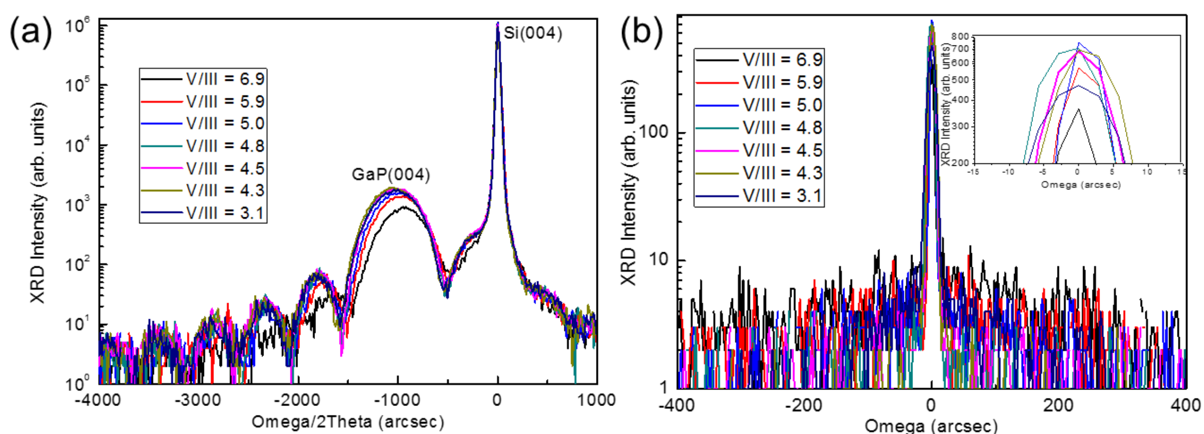

Figure 2-4 (a) DC coherent ω-2θ RCs measured in the vicinity of Si-GaP (004) reflections. (b) The corresponding GaP TC ω RCs

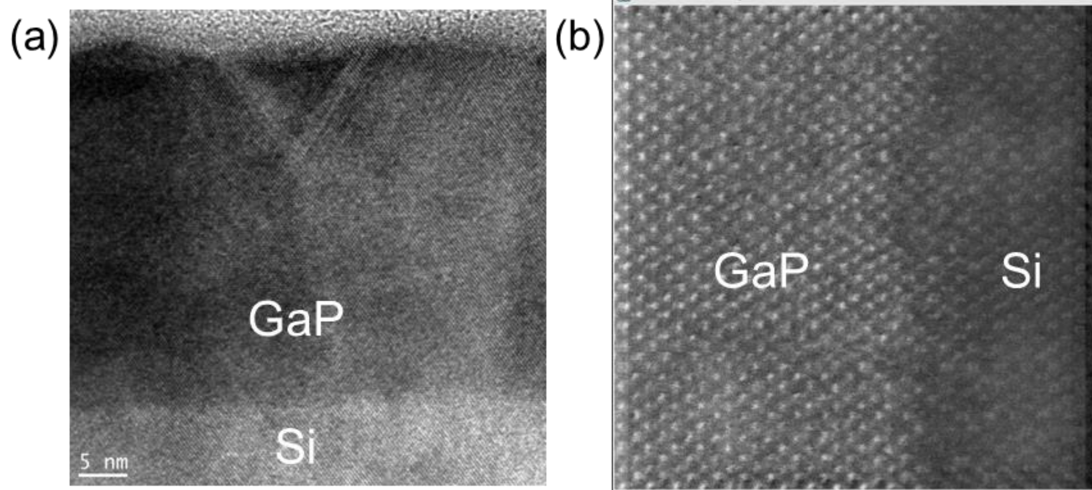

Figure 2-5 TEM images of 37 nm GaP sample with optimized MBE growth conditions.

To investigate defect formation for GaP/Si structures and their structural transformation during epitaxial growth, a set of thicker GaP layers were grown under established growth condition and investigated. The MBE-grown structures exhibited high crystal perfection for the thin (37 nm) GaP layer, while the thicker ~ 250 nm thick GaP layer structure clearly demonstrates beginning of defect creation on both, coherent DC ω-2θ and TC ω RCs (Figure 2-6). As the DC ω-2θ RCs plotted in Figure 2-6, the shift of GaP peak towards to Si peak indicates that the relaxation of the initial elastic stress gradually increasing for GaP layers thicker than 250 nm. Noticeable diffusion and angle shrinking of the entire interference pattern, and intensity diminution of the interference fringes on ω-2θ RC (Figure 2-7) confirm that. Despite that an angle position of GaP(004) peak on ω-2θ RC and position of the diffraction spots on asymmetrical (224) Reciprocal Space Map (RSM) (Figure 2-8 and Figure 2-9) reveal the lack of relaxation of the initial elastic stress in this structure .

TC ω RC of 250 nm GaP sample, shown in Figure 2-6b, also confirms the initial stage of defect creation: coexistence of strong and narrow (FWHM = 8.85 arc.sec) central coherent peak, corresponding to the main almost perfect crystalline matrix of GaP epitaxial layer, and low intensity diffuse base, caused by X-ray scattered on crystal defects, created during epitaxial growth. Based on the FWHM of the diffused pedestal (~ 85 arc.sec) the bending of the crystal planes of the epitaxial layer corresponds to ~ $2.6 – 2.7 \times 10^7$ cm^{-2} crystal defects in the epitaxial layer. Low intensity of the diffused base means that crystal defects, created during epitaxial growth and responsible for diffused scattering, occupy small, most probably, bottom part of the GaP layer, while the elastic strain, induced by these defects, still affects only a small part of the epitaxial layer.

The lack of interference fringes on the tails of the ω RCs, typical for the initial stage of relaxation at polar III-V low deteriorated epitaxial structures [26], means the lack of spatial ordering of crystal defects in low deteriorated III-V epitaxial layers deposited on non-polar substrates, while an entire coincidence of the shape of the ω RCs and diffused base, in particular, collected at two [110] and [1-10] azimuth directions suggests that GaP epitaxial layers grown on non-polar Si(001) substrate do not inherit structural anisotropy typical for Zinc-Blende (ZB) epitaxial layers grown on polar substrate.

Increase of the thickness of GaP layer to 500 nm totally diffused interference fringes on DC ω-2θ RC and also revealed onset of relaxation of the initial elastic stress in this structure (Figure 2-6b). Shape of the ω RCs for both <110> azimuth directions also noticeably transformed in comparison with 250 nm structure. Central narrow peak almost fully disappeared, overlapped by wide diffused peak induced by crystal defects. FWHM of this peak (~ 133 arc.sec) corresponds to ~ 6.5×10^7 cm^{-2} crystal defects in the epitaxial

layer. Dislocation density, increased in ~ 2.5 times in comparison with 250 nm layer, led to structural deterioration of the almost entire volume of the epitaxial layer, supposedly, caused by the lateral overlapping of the elastic stress induced by crystal defects (their dislocation cores) created on interface/in the volume of GaP layer. Well coincidence of the shape of the ω RCs measured for two azimuth directions shows the lack of azimuth <110> anisotropy of 500 nm thick GaP layer.

Thicker (~ 1 and 2 μm thick) GaP epitaxial layers demonstrate gradual structural transformation of crystal perfection: further increase of the bending of the layer and increase of the extent of relaxation up to 75%, extracted from (004) and (224) RSMs (Figure 2-8 and Figure 2-9). Significant difference between these trends for non-polar Si-GaP and low deteriorated III-V polar epitaxial structures [25] suggests that crystal defects, created in GaP layers have different nature in comparison with crystal defects created in polar epitaxial structures. Noticeable diminution of the layer bending demonstrated by low deteriorated polar epitaxial layers most probably is related to volumetric intersection of 60° dislocations in the volume of the epitaxial layer and final compensation of dislocation screw components.

Bending evolution of the epitaxial structures, correlated with the type and density of extended defects, is different in comparison with other low deteriorated and partially relaxed epitaxial structures [10]. Density of these defects, as evaluated by the FWHM of the ω RCs (as listed in Table 2-1), is steadily increasing (~6.5×10^7 cm^{-2} in 500 nm, ~7.3×10^8 cm^{-2} in 1 μm, and ~1.1×10^9 cm^{-2} in 2 μm GaP layer), as well as the bending elastic stress that is induced by them. Such behavior suggests the possibility of other types of crystal defects being created in the volume of thicker GaP epitaxial layers.

The electron microscopy observations (see Figure 2-10) confirm the trends in defect development that are predicted from the X-ray data. The thick (~ 2 μm) GaP layer contains a high density of threading dislocations, as well as considerable {111}-type inclined stacking faults.

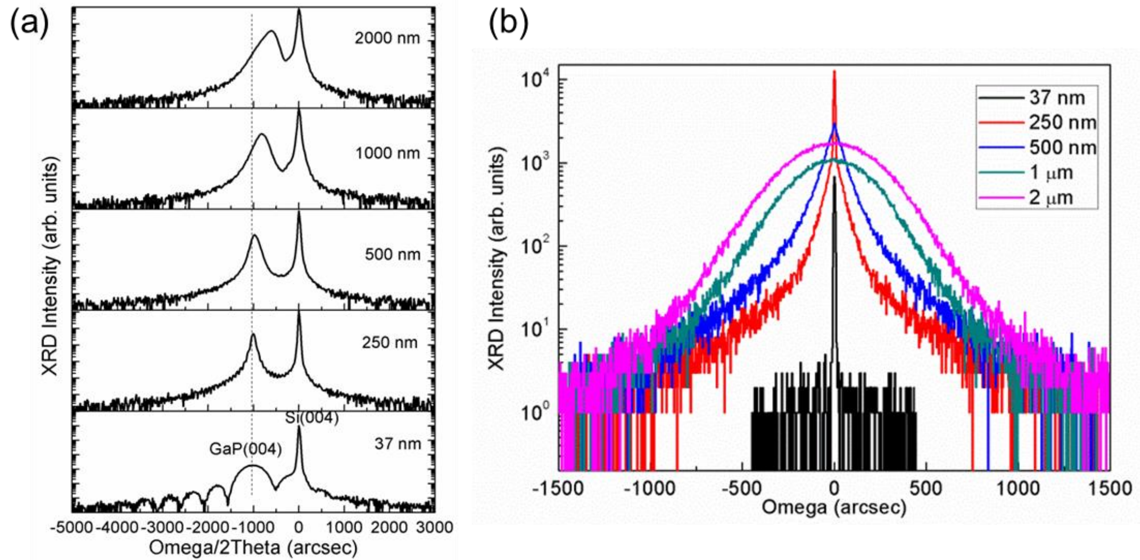

Figure 2-6 DC coherent ω-2θ RCs measured in the of vicinity of Si-GaP (004) reflections. Black and red bars specify the angle position of fully elastically stressed GaP layer and Si(004) substrate peaks. TC ω RCs shown insert.

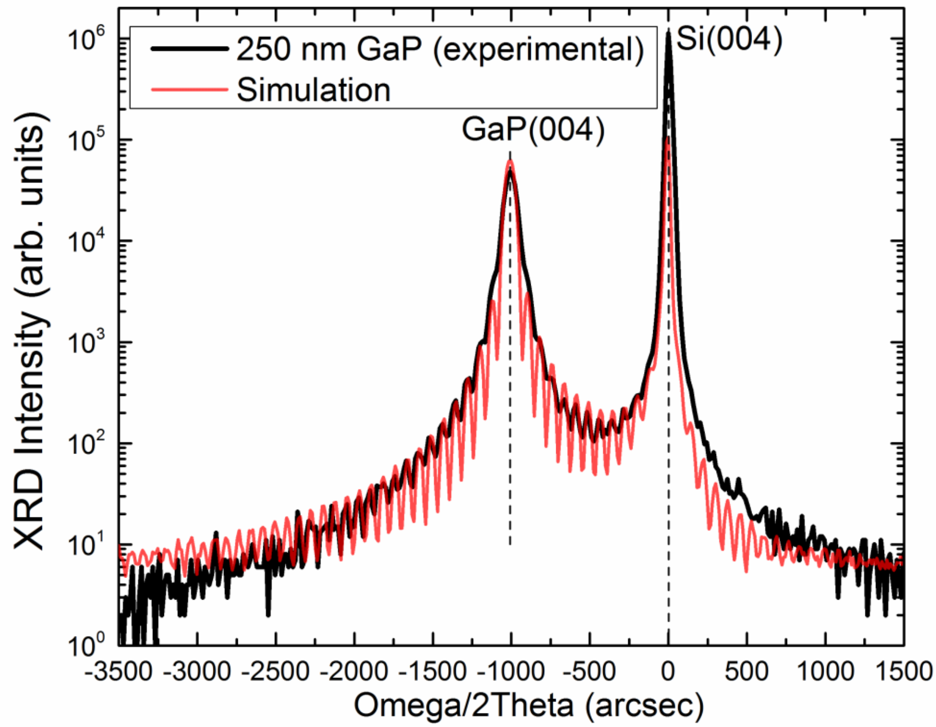

Figure 2-7 Experimental DC coherent ω-2θ rocking curve of 250 nm GaP compared to simulation curve.

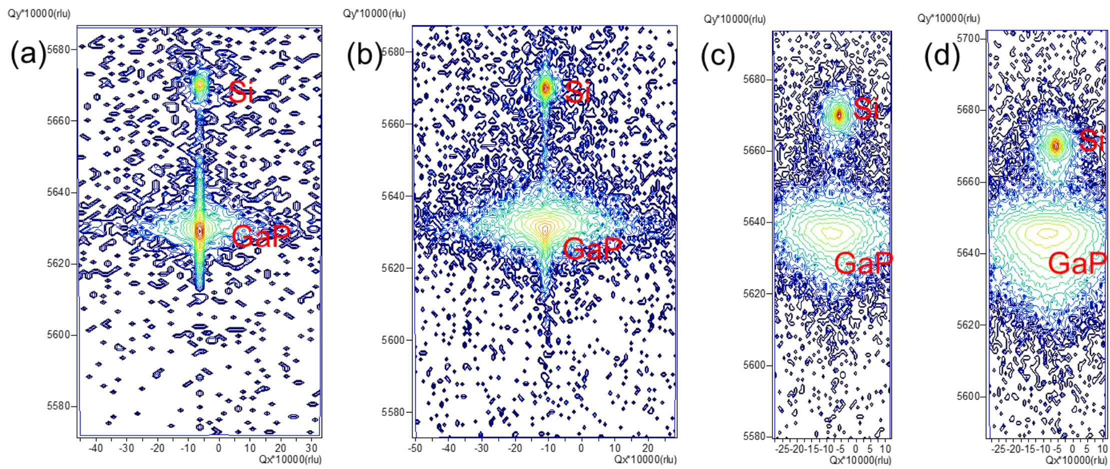

Figure 2-8 RSM(004) of different GaP layers thickness: (a) 250 nm, (b) 500 nm, (c) 1000 nm and (d) 2000 nm.

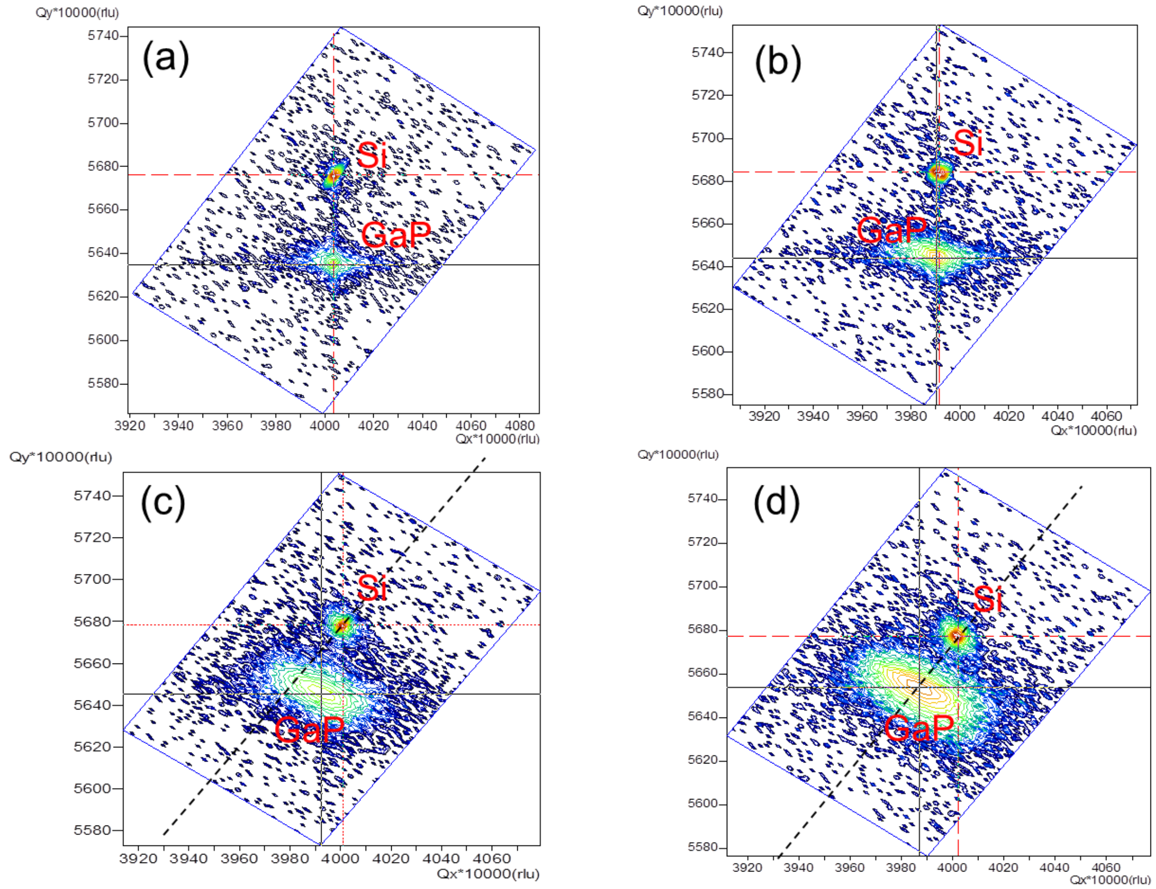

Figure 2-9 RSM(224) of different GaP layers thickness: (a) 250 nm, (b) 500 nm, (c) 1000 nm and (d) 2000 nm.

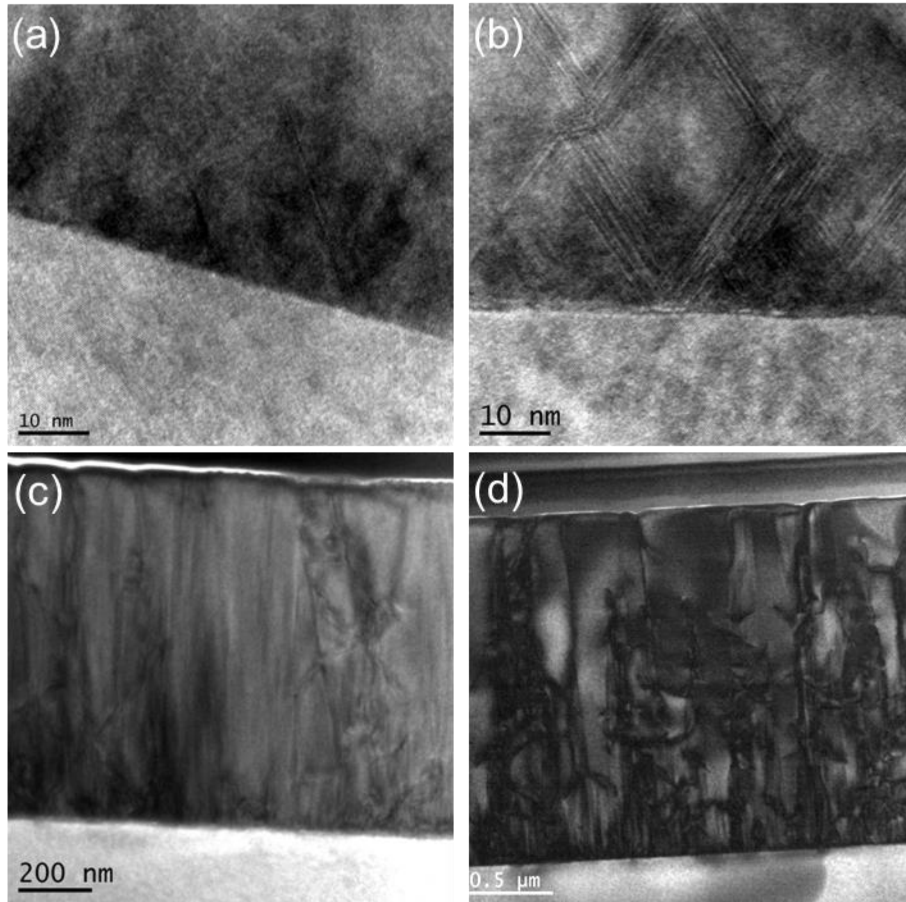

Figure 2-10 TEM of different GaP layers thickness: (a) 250 nm, (b) 500 nm, (c) 1000 nm and (d) 2000 nm.

Table 2-1 XRD results of various thicknesses MBE-grown GaP/Si samples

t_{GaP} (nm)	DC ω-2θ RC GaP peak FWHM (arc.sec)	GaP Layer Vertical Coherence (nm)	TC ω RC GaP peak FWHM (arc.sec)	Dislocation Density (cm^{-2})
37 nm	482	~36.5	11.0	2.6×10^{5}
250 nm	85	246	11.2 / 86	2.7×10^{7}
500 nm	133	143	133	6.5×10^{7}
1.0 µm	216	89	455	7.3×10^{8}

2.0 μm	237	80	545	1.05×10^{9}

Table 2-2 RSM results of various thicknesses MBE-grown GaP/Si samples

t_{GaP} (nm)	Sym (004) RSM q_x/q_y (rlu)	Asym (224) RSM q_x/q_y (rlu)	Relaxation (%)
250 nm	0 / 0.004067	0.000028 / 0.004041	0
500 nm	0 / 0.003983	0.000093 / 0.003899	9
1.0 μm	0.000231/ 0.003328	0.000813 / 0.003164	40
2.0 μm	0.000286/ 0.002405	0.001510 / 0.002273	50 => 76

2.4 Conclusions

Crystal perfection of MEE and MBE grown Si(001)-GaP structures were investigated by high-resolution XRD and TEM. MEE structures grown under the same growth conditions revealed that 4 degrees offcut angle significantly affects crystal perfection of GaP. Higher perfection of offcut structure most probably related to atomic migration and atomic incorporation on the growth front. The growth conditions of MBE growth structures on precisely orientated substrates allowed significantly postponed defects creation and hence beginning of relaxation in elastically stressed epitaxial structure. Crystal perfection of MBE grown structures revealed high crystal perfection of the thin GaP layer, then gradual relaxation of the initial elastic stress by 60° and Lomer dislocations in thicker GaP layers. Different bending of the thick GaP structures caused by threading dislocations, created in these layers.

Chapter 3

SI MINORITY-CARRIER LIFETIME CHALLENGES AND APPROACHES

3.1 Introduction

In order to develop high performance GaP/Si solar cells, the silicon must have a high minority-carrier lifetime in the millisecond range, which is required to obtain more than 725 mV open-circuit voltage for wafers with thickness of 100-160 µm. The growth of high quality GaP on precisely oriented (001) silicon has been demonstrated in Chapter 2. And to get high performance, more attention needs to be focused on conserving a high minority-carrier lifetime in silicon. Recent results reported by multiple research groups, looking at developing of both MJ and carrier selective contact, such as GaP, solar cells, have shown a dramatic deterioration in the silicon minority-carrier lifetime during the growth of III-V layers, both by molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD) [9], [27]–[32]. The degradation is attributed to forming recombination centers from the fast diffusing species or intrinsic defects. The most prevalent approach thus far to recover the degraded lifetime is by phosphorus gettering or hydrogen passivation. For example, gettering has been demonstrated either by phosphoryl chloride ($POCl_3$) diffusion [28], [29], [33], or by phosphine (PH_3) diffusion [31], or by hydrogen defect passivation [31]. While gettering or hydrogen passivation enable at least partial recovery of the minority-carrier lifetime in the silicon, the optimum approach is to understand and effectively prevent the lifetime degradation. High temperature post-growth gettering processes, such as phosphorus diffusion, can be detrimental to the properties of III-V epitaxial films and may be difficult to incorporate into a full solar cell process. Similarly, hydrogen passivation of defects makes the device highly dependent on

subsequent temperature processing, as hydrogen may out diffuse at temperatures below 400°C. Moreover, Varache *et al.* reported that a 500-nm-thick SiN_x coating on both sides of a p-type Cz wafers preserved the bulk lifetime in the hundreds of microseconds range after annealing in their MOCVD reactor [27]. Recently, SiO_2/SiN_x diffusion barriers were applied to prevent the iron contamination and minimize Si lifetime degradation in the MOCVD reactor [18].

In this chapter, we systematically investigate the effect of GaP growth conditions on GaP crystal quality as well as the effect of annealing conditions for Si wafer on Si bulk lifetime. Significant lifetime degradation of Si wafers is observed when annealed at high temperatures (> 700°C). This lifetime reduction is prevented by depositing SiN_x film, acting as a diffusion barrier and/or getter, on the backside of Si wafer. The SiN_x also enables the epitaxial growth of high-quality GaP layers on Si wafer. We investigate the Si minority-carrier lifetime after GaP epitaxial growth in an MBE system and approaches to mitigate lifetime degradation. By subsequently thinning down annealed samples with acids, the different lifetime profiles for different annealing temperatures reveal the signature of extrinsic impurity diffusion. Furthermore, we evaluate the impact of gettering via $POCl_3$ diffusion on MBE thermally treated Si wafers. Finally, we investigate two effective methods to mitigate the lifetime degradation during the MBE growth, which offers a path for higher quality III-V growth on active Si substrate and the development of high performance III-V/Si solar cells.

3.2 Experimental Details

In order to investigate the lifetime evolution during GaP grown on Si in the MBE system, four different types of (100)-oriented Si substrates with thicknesses between

180 μm and 380 μm were used in this work. These wafers are: (i) high resistivity intrinsic float-zone (FZ) wafers (>400 Ωcm), (ii) n-type P-doped FZ wafers, 1−5 Ωcm, (iii) p-type B-doped FZ wafers, 1−5 Ωcm, and (iv) n-type P-doped Czochralski (Cz) wafers, 1−3 Ωcm. All Si wafers were chemically cleaned in an RCA (Radio Corporation of America) solution and etched in a diluted hydrofluoric acid (HF) (10%) for 30 s before loading in the MBE pre-chamber which was pumped down to a pressure of about 1×10^{-8} Torr. After baking, the wafers were transferred to the growth chamber which was maintained at a pressure below 2×10^{-10} Torr. We used a solid-source Veeco GEN-III MBE system, equipped with a phosphorus valved cracker cell and Ga source. A temperature ranges from 700°C to 850°C was used in the processes for the decomposition of the native oxide on the Si substrate, which was monitored via changes in the *in-situ* reflection high-energy electron diffraction (RHEED) patterns. The surface reconstruction that the transition from (1×1) spotty RHEED patterns to (2×1) streaky patterns indicates the Si surface is clean and ready for epitaxial growth.

Unless otherwise indicated, all samples for the lifetime measurement were passivated on both sides after removal from the MBE chamber with 50-nm-thick intrinsic hydrogenated amorphous silicon (a-Si:H) films prepared by plasma-enhanced chemical vapor deposition (PECVD) at 250°C. The a-Si:H passivation enables a surface recombination velocity as low as 1 cm/s [34], which is low enough to estimate the Si bulk lifetime directly from measured effective minority-carrier lifetimes of the passivated silicon wafers. The Si effective minority-carrier lifetimes were measured by quasi steady state photoconductance decay (QSSPC) using a Sinton Lifetime Tester.

The samples were divided into two general groups. In one set, 15 nm thick GaP was grown on a polished high resistivity FZ Si substrate at 380 °C via migration enhanced epitaxial (MEE) method and post-growth annealed in the MBE chamber under a P flux at 580°C for 8 min. After measurement of the Si minority-carrier lifetime with GaP on the front and a-Si:H on the rear, a mixture of hydrofluoric, nitric and acetic acids (HNA) with a volume ratio of 10:73:17 at room temperature was used to isotropically etch the GaP layer and Si (c-Si or a-Si). The sample is then passivated with the a-Si:H process described above, and remeasured.

The second set of samples was used to investigate the influence of temperature on Si degradation. They were prepared by heating n-type FZ 280-μm-thick wafers in the MBE chamber between 350°C and 800°C for 30 min. There was no growth of GaP or other materials. To obtain the lifetime profile for the thinned-down wafers, we repeated the following sequence until the preferred depth was achieved: (1) etching in HNA solution, (2) PECVD surface passivation and (3) effective lifetime measurement. The amount of Si successively removed from each side was estimated by weighing the wafer.

For the gettering process, degraded n-type FZ samples were examined the lifetime with a-Si:H passivation and then the passivation layers were removed by HNA. And wafers were exposed to a flow of oxygen and $POCl_3$, at 850°C in a diffusion furnace, with a 25 min drive in step.

In the samples with a SiN_x diffusion barrier, all the amorphous SiN_x films were 150-nm-thick and deposited at 350°C by PECVD on the surface of cleaned Si wafers. After thermal treatment in the MBE, the SiN_x layer was removed by etching in a concentrated HF solution.

Also, we investigated the effect of such a SiN_x protection on the performance of an a-Si:H/c-Si heterojunction solar cell. We compared three p-type Si FZ wafer: a reference not annealed in the MBE, a bare Si wafer and a wafer coated with a SiN_x film at the back, both annealed at 820°C for 5 minutes in the MBE. and a third sample with a SiN_x film on the back After removing the SiN_x film from the third sample, a 6-nm-thick intrinsic a-Si:H layer was deposited on both sides of all three samples, including the reference cell, followed by a 10 nm (n) a-Si on the front side and a 10 nm (p) a-Si on the back side by PECVD. Indium-tin-oxide (ITO) with a thickness of ~75 nm was then deposited on top and also back as a current spreading layer. Finally, a 200 nm Ag was deposited on the front as fingers and on the back as a back contact. ITO and Ag were deposited by RF sputtering. External quantum efficiency (EQE) of the fabricated cells was measured by the solar cell spectral response measurement system (QEX10), manufactured by PV Measurements. The I-V characteristics were measured with a continuous Oriel class A solar simulator equipped with a Xenon ARC lamp (AM1.5G), which was calibrated with an original equipment manufacturer Si reference cell.

3.3 Si Lifetime Degradation

Figure 3-1 shows the effective minority-carrier lifetime of a high resistivity silicon wafer having a grown GaP layer on one side and a-Si:H on the other (red markers). Lifetime for this sample is two orders of magnitudes lower than that of a reference FZ Si wafer passivated on both sides with a-Si:H. By comparing these different lifetimes, the low lifetime of the GaP/Si/a-Si:H sample can originate from two factors: (i) the surface recombination at the GaP/Si interface before the GaP is etched; (ii) a strong increase in recombination in the Si wafer triggered by the growth process in the MBE system. The

effective minority-carrier lifetime depends on both surface and bulk recombination; therefore, to decouple which is impacted by the growth process, we removed the GaP layer and about 3 µm of Si from each side by etching in an HNA solution. After appropriate cleaning and repassivation with a-Si:H on both sides, the measured minority-carrier lifetime (blue markers) was higher than that of the GaP/Si/a-Si:H sample, but still significantly lower than the reference sample. During GaP growth, the phosphorous and the gallium diffusion if any are estimated in the first 3 µm of the Si on the surface. By etching the first 3 µm of the Si, the phosphorous and the gallium diffusion are not playing significant roles any more in the lifetime degradation process. The low lifetime (blue markers) of the sample after etching compared to the reference sample indicates that the degradation happened in the Si bulk.

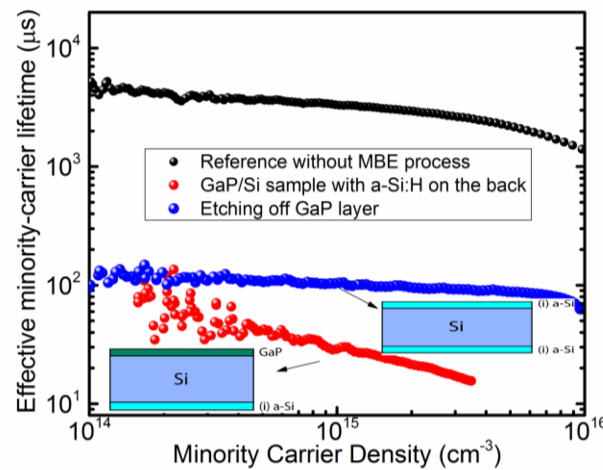

Figure 3-1 Injection-dependent effective minority-carrier lifetimes of different FZ-Si wafers: a reference that was not processed in the MBE, a sample with GaP grown on one side, and the same sample after etching the GaP layer and ~3 µm of silicon from each surface.

The second set of samples was used to investigate the influence of temperature on Si degradation. They were prepared by heating n-type FZ 280-µm-thick wafers in the MBE

chamber between 350°C and 800°C for 30 min. There was no growth of GaP or other materials. We measured the lifetime as a function of Si etched, so as to separate the surface and bulk contamination. To obtain the lifetime profile for the thinned-down wafers, we repeated the following sequence until the preferred depth was achieved: (1) etching in HNA solution, (2) PECVD surface passivation and (3) effective lifetime measurement. The amount of Si successively removed from each side was estimated by weighing the wafer.

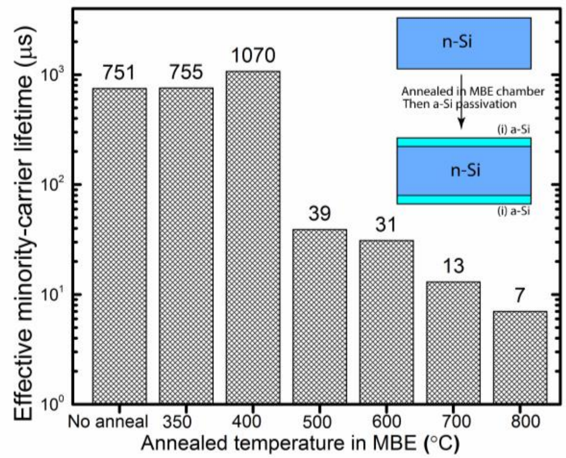

Figure 3-2 Effective minority-carrier lifetime (at the injection level of 1×10^{15} cm^{-3}) of Si wafers annealed in the MBE chamber for 30 min at different temperatures.

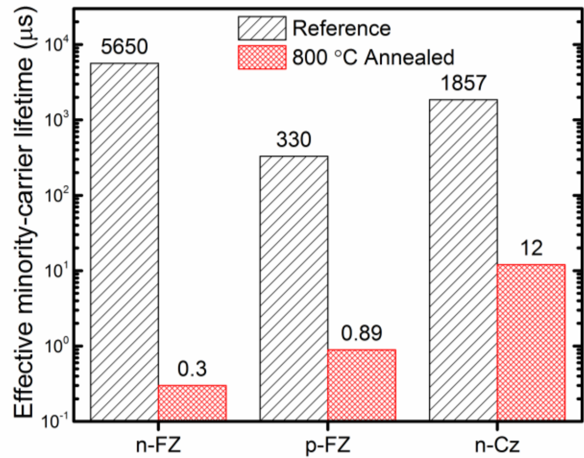

Figure 3-3 Effective minority-carrier lifetime (at an injection level of 1×10^{15} cm^{-3}) of different types of Si wafers (n-FZ, p-FZ, and n-Cz) before and after 800°C annealing in the MBE chamber for 30 min.

To further identify the cause of the reduced bulk minority-carrier lifetime, we performed a series of isochronal annealings of bare n-type FZ Si wafers in the MBE chamber at different temperatures for 30 min. The as-received wafers used were single side polished and required additionally chemically polished by HNA and appropriate clean before the processing.

After removal from the chamber, wafers were passivated with 50 nm a-Si:H. As shown in Figure 3-2, the effective minority-carrier lifetime increases slightly after annealing at 400°C, which may be related to the deactivation of intrinsic defects after low-temperature annealing [35]. However, the effective minority-carrier lifetime drops significantly for annealing at 500°C, and as the temperature further increases, the lifetime decreases to less than 10 μs at 800°C. As there was no growth for these samples, the Si-bulk degradation mechanism is not due to the growth of the III-Vs on the Si but caused by the temperature treatment, with a low threshold temperature of 500°C.

While there have been previous reports of thermal activation of grown-in defects, such as the lattice-impurity or impurity-impurity metastable defects, in FZ wafers as described in [28], there are several arguments that suggest that the lifetime degradation is rather originating from thermally activated diffusion of extrinsic impurities [36]: (i) There is a significantly stronger lifetime degradation in this work than in [28], with no sign of lifetime recovery at temperatures above 800°C (not shown). Similar thermal annealing was conducted to p-type FZ wafers and no significant degradation was observed in a high-purity furnace [32]; and (ii) We observed similar lifetime degradation occurs for Cz and FZ wafers (Figure 3-3), whereas Cz wafers should, according to [35], not accommodate the type of intrinsic defect causing the thermally activated degradation. This additionally implies that

the impurities responsible for the lifetime degradation are not associated with defect complexes related to O or C contaminants present in high concentrations in Cz but not in FZ. Furthermore, we investigated the impact of high temperature treatment in the MBE chamber on both p-type and n-type FZ wafers. After annealing at 800°C for 30 min, the Si-bulk minority-carrier lifetime degradation is seen for both types (Figure 3-3). This suggests that the impurities responsible for the lifetime degradation do not form defect complexes with a specific dopant like, for example, iron, chromium, and manganese that are well-known to form complexes with ionized boron but are insensitive to phosphorous.

To analyze the possibility of thermally-activated diffusion of extrinsic impurities, we evaluate lifetime depth profiles by progressively thinning down in HNA solution samples previously annealed at 500°C, 700°C, and 800°C. As seen in Figure 3-4, the lifetime of the sample annealed at 500°C gradually increases by about a factor five (from about 40 µs to 200 µs) after removing the first 10 µm from both Si sides, and reaches a plateau at 300 µs after a 40-µm-deep etching. On the contrary, the lifetime of the samples annealed at 700°C and 800°C stay at the same values after chemical thinning. These lifetime depth profiles thus suggest a temperature-activated diffusion of recombination-active impurities such as metals, penetrating very deep (>50 µm) into the silicon bulk during the high temperature steps, and not being restrained to the surface.

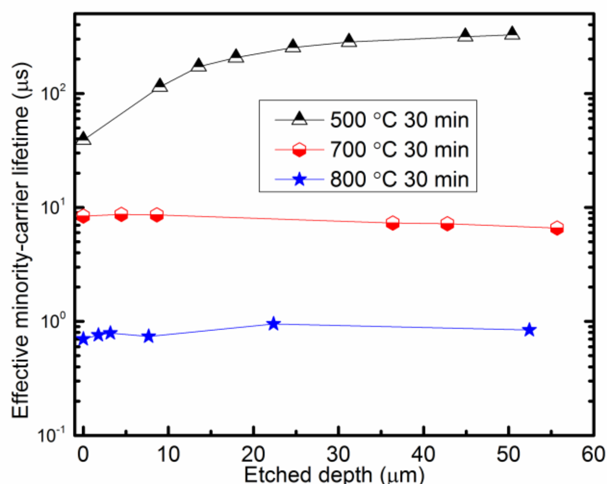

Figure 3-4 Depth-profile of the effective minority-carrier lifetime (at the injection level of $1\times10^{15}cm^{-3}$) for n-FZ Si samples annealed at different temperatures (500°C, 700°C, 800°C).

Finally, we examine the effect of the duration of the high temperature step in the MBE chamber on the Si lifetime. We determine the minimal thermal budget necessary to start observing surface reconstruction (but not the full de-oxidation) by ramping the temperature of an n-type FZ silicon wafer in the growth chamber until appearance of the well-defined (2×1) RHEED patterns, which corresponds to a temperature of about 700°C. We then immediately ramp the temperature down and unloaded the sample. After cleaning and surface passivation, the Si minority-carrier lifetime is less than 10 μs. Although the heating plateau is minimized, the wafer is still exposed to temperatures above 500°C for more than 30 min during temperature ramp up and down. This indicates that minority-carrier lifetime degradation seems almost unavoidable for processes including a thermal surface preparation step for epitaxial growth. Consequently, it is necessary to investigate approaches to recover from or prevent the Si degradation.

3.4 Approaches to Recover Lifetime

3.4.1 Impact of Gettering on the Degraded Wafers

For the gettering process, degraded n-type FZ samples were examined the lifetime with a-Si:H passivation and then the passivation layers were removed by HNA. And wafers were exposed to a flow of oxygen and $POCl_3$, at 850°C in a diffusion furnace, with a 25 min drive in step. Gettering is a method conventionally used to clean the bulk of silicon wafers and relies on the different partition coefficient of metallic impurities such as Cu, Au, Fe, Cr, Mn and Ni between the phosphorous glass and the Si bulk [27]. The symmetric heavily phosphorus doped layers introduced by $POCl_3$ diffusion has been reported to successfully lead to a recovery in the Si lifetime of more than 100 μs [18]. We investigate the impact of gettering from a phosphorus diffusion on the contaminated n-type FZ wafers. The samples were first annealed in the MBE chamber (without growth) at temperatures between 450°C and 800°C for 30 min leading to a degradation of the Si-bulk lifetime to the low μs-range for temperatures above 500°C as shown in Figure 3-5. After etching the (i)a-Si:H passivation layers and a few microns of Si on each side, these samples were exposed to phosphorous diffusion from a $POCl_3$ source at 850°C. The minority-carrier lifetime of all samples was recovered to the millisecond range (Figure 3-5), after etching the phosphorous glass and ~5 μm of Si from both sides to remove the P-rich region, followed by (i)a-Si:H passivation on both sides. The lifetimes were measured at an injection level of 1×10^{15} cm^{-3}, except for the 800°C-annealed samples which is measured at 1×10^{14} cm^{-3} because of its low lifetime. Gettering thus provides a solution to recover a Si-bulk lifetime suitable for the Si wafer to act as an active part of a high-quality photovoltaic device. The effectiveness of the gettering further strengthens the hypothesis

that the lifetime degradation originates from highly mobile impurities diffusing from the MBE environment. However, this *ex-situ* gettering process is not ideal for III-V/Si integration structures, since the long procedure at a temperature superior to the growth temperature and under such an atmosphere might degrade the quality of the III-V material; GaP films have been noteworthy shown to completely decompose if annealed above 800°C [10].

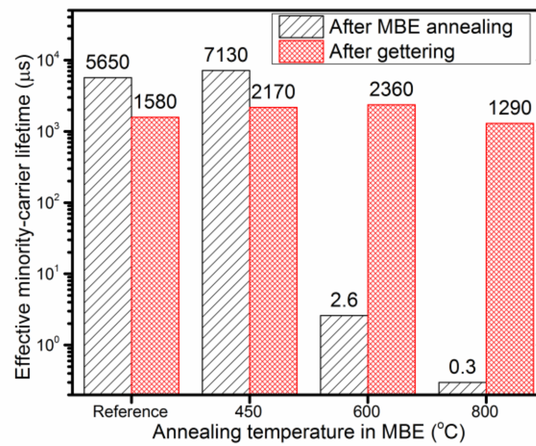

Figure 3-5 Effective minority-carrier lifetime of n-Fz Si samples annealed in the MBE chamber at different temperatures before and after gettering by $POCl_3$ diffusion (at an injection level of 1×10^{15} cm^{-3}, except for the 800°C-annealed samples at 1×10^{14} cm^{-3}). The "Reference" wafer was not MBE-annealed.

3.4.2 SiN_x Protective Coating

In the samples with a SiN_x diffusion barrier, all the amorphous SiN_x films were 150-nm-thick and deposited at 350°C by PECVD on the surface of cleaned Si wafers. After thermal treatment in the MBE, the SiN_x layer was removed by etching in a concentrated HF solution.

To avoid the necessity of a gettering step, we investigate a solution to prevent the detrimental diffusion of impurities in the Si wafer by using a sacrificial 150-nm-thick SiN_x coating deposited by PECVD prior to the MBE process to protect the Si wafer. The SiN_x layer is commonly used as a diffusion barrier against potential metal diffusion in semiconductor technology [37]. We annealed an n-type FZ wafer coated on both sides with a SiN_x layer at 800°C in the MBE chamber. After removal of the SiN_x layer and passivation with i-a-Si, the sample shows an effective lifetime of 850 μs, whereas the lifetime of a similar wafer treated in the same condition but without SiN_x coating (shown in Figure 3-6) is below 1 μs. The SiN_x coating thus effectively mitigates the lifetime degradation.

Since a double-side SiN_x coating prevents any epitaxial growth on the Si wafer, we investigate the influence of a back-side-only SiN_x coating. We annealed in the MBE at 800°C a FZ n-type wafer with a SiN_x coating only on the back side (facing the heater). After removal of the SiN_x with HF and passivation with a-Si:H, the silicon has an effective minority-carrier lifetime of over 700 μs (Figure 3-6C). To further confirm SiN_x on the backside could effectively maintain good lifetime, another three FZ n-Si wafers with SiN_x on back were annealed in the MBE chamber at 750°C, 800°C and 850°C, respectively. The lifetimes of these three wafers are more than 1.5 ms at an injection level of $1x10^{15}$ cm^{-3} with SiN_x removal and a-Si:H passivation, which is comparable to the lifetime of as-received wafers. Furthermore, the thickness of the SiN_x does not seem to be an important parameter since thinner (75 nm) and thicker (450 nm) coatings result in a similar lifetime protection as the 150-nm-thick film. Finally, we notice that when the bare Si faced the heater (SiN_x coating on the front) during annealing in the MBE (Figure 3-6D), the Si lifetime degrades to less than 1 μs, which is similar to the value for the case annealing

without SiN_x film (Figure 3-6A). This strongly suggests that the contaminants enter the wafer from the back side, which is in contact with the sample holder and in vicinity of the tantalum wires heater covered with a pyrolytic boron nitride plate.

The physical barrier provided by such dielectric SiN_x layer may not be the only effect contributing to the bulk Si protection. To further understand the physical mechanisms associated with coating preventing degradation the SiN_x, we examined the impact of the SiN_x coating to the lifetime degraded wafers. Previously degraded Si wafers (prepared by annealing without SiN_x on the rear) had SiN_x deposited on the rear, and then were annealed. Figure 3-7 shows that the degraded lifetimes can be partially recovered by reannealing them with a SiN_x coating. A high resistivity bare FZ wafer with effective lifetime below 10 μs (after annealing at 800°C in the MBE chamber) was coated with a SiN_x film on the back side and then loaded in the MBE chamber again and annealed at 850°C. As a result, its effective lifetime is increased to above 200 μs. Similarly, a SiN_x film was deposited on the back side of a similar wafer degraded at 580°C (as applied during the GaP growth process) had a lifetime of 238 μs, which improved to over 1 ms after re-annealed in the MBE at 850ºC. This suggests that the SiN_x coating provides internal gettering of the impurities to the SiN_x/Si interface, preventing distribution of most of the impurities to the bulk of the wafer. Additionally, the SiN_x layer is rich in hydrogen from the precursors used in the PECVD process and therefore may also provide hydrogen diffusing into wafers and passivating bulk defects during the annealing, as has been proposed by Grant *et al.* [38] and Hallam *et al.* [39].

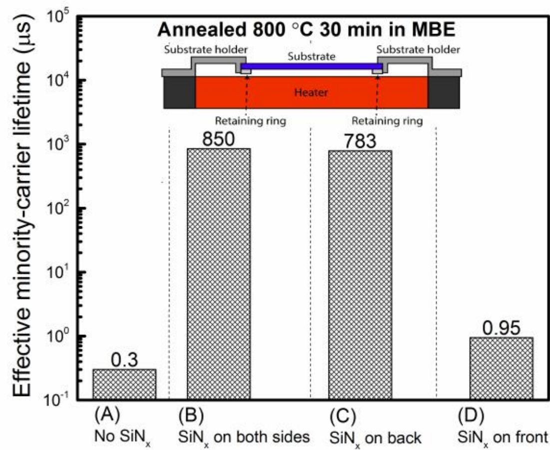

Figure 3-6 Effective minority-carrier lifetime of Fz (n) Si wafers with a SiN_x coating deposited on (A) no SiN_x, (B) both sides, (C) back side, and (D) front side, after the indicated treatment (at an injection level of $1x10^{15}$ cm^{-3}**,** except for the annealed sample in (A) and (C) at $1x10^{14}$ cm^{-3}). The SiN_x films were removed by etching and the wafers surface re-passivated before lifetime measurement.

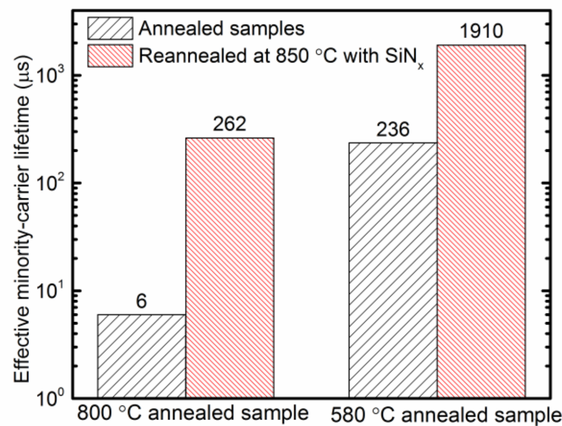

Figure 3-7 Change in the effective minority-carrier lifetime (at an injection level of 1×10^{15} cm^{-3}) of high resistivity FZ silicon samples annealed initially without SiN_x protective coating and re-annealed with SiN_x coated on the back in MBE chamber at 850°C for 8 min.

Finally, the external quantum efficiency (EQE) curves of the solar cells, including the wafers annealed with and without the SiN_x layer in the MBE chamber, are shown in Figure 3-8. It is clearly shown that the cell with no diffusion barrier has a lower EQE than

the cell protected with the diffusion barrier (protected sample), which is related to the significantly degraded bulk lifetime of the unprotected sample. By integrating the EQE curves (under AM1.5G spectrum) from 300 nm to 1200 nm, the short-circuit current J_{sc} can be estimated to be 28.4 mA/cm^2 for the Si cell annealed at 820°C, and approximately 34.7 mA/cm^2 for both the protected sample and the reference sample. The EQE difference between the reference cell and the protected cell is very small. From current density versus voltage (J-V) characteristics (not shown) under AM1.5G spectrum, the open circuit voltage is about 640 mV for both the protected cell and reference cell, while it is 535 mV for the unprotected cell. Therefore, it reveals that the SiN_x layer can perfectly maintain the Si wafer lifetime during the thermal treatment in the MBE.

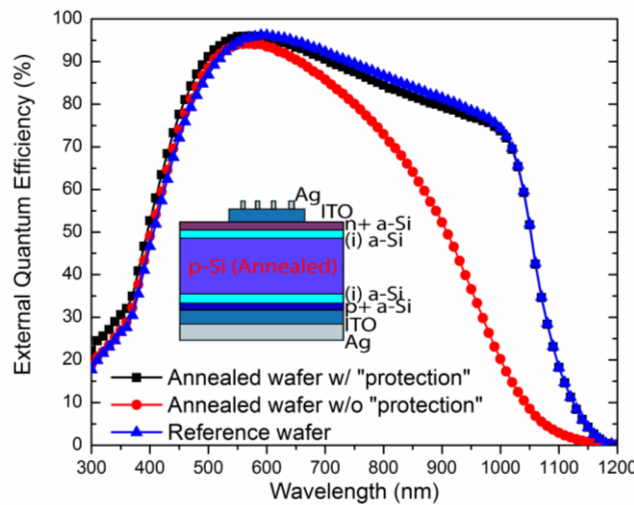

Figure 3-8 External quantum efficiency of the solar cells processed from the thermally treated p-type FZ Si wafers T.

To examine the SiN_x coating on Si substrate affects GaP quality, a 150 nm-thick SiN_x film is deposited on the backside of on (001)-oriented FZ n-type Si wafer, followed by epitaxial GaP layers growth with a nominal thickness of 15 nm. Before the thermal deoxidation at 850ºC, the RHEED shows (1×1) surface reconstruction of Si (Figure 3-9a).

The RHEED pattern changes to (2×2) streaks after the thermal deoxidation (Figure 3-9b). The substrate temperature is then ramped down to the growth temperature of 380°C for GaP growth. During the MEE growth of a 15 nm-thick GaP layer, the RHEED exhibits (2×2) diffuse patterns (Figure 3-9c), indicating that the GaP surface is rough. However, a post-growth annealing of the GaP layer under P flux at 580°C for 8 mins leads to (2×4) streaky RHEED patterns (Figure 3-9d), which is indicative of smoothly reconstructed GaP surfaces. Moreover, high-resolution transmission electron microscopy reveals that the GaP layer has a low density of anti-phase domains, which may be due to their self-annihilation caused by enhanced Ga-adatom diffusion on the GaP surface during the MEE growth [40].

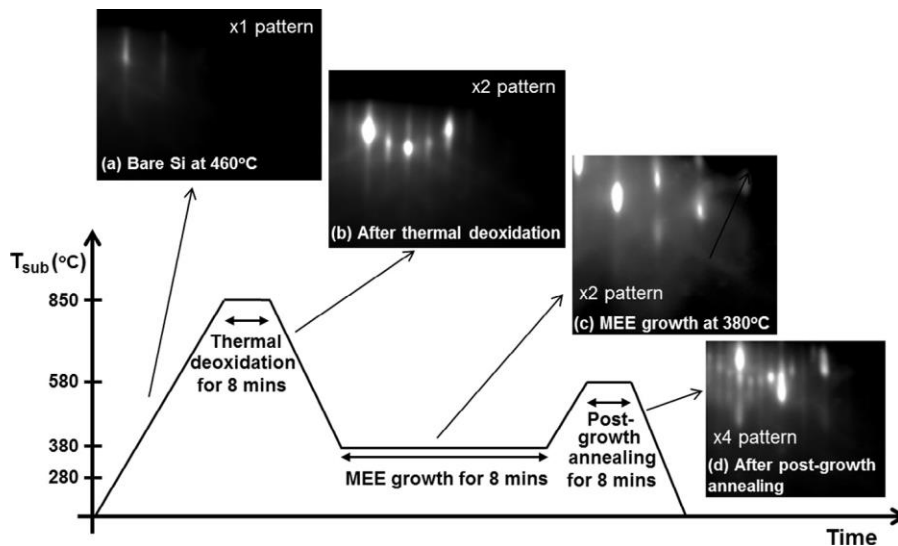

Figure 3-9 Schematic of the growth sequence of GaP and the RHEED patterns observed during the growth.

TC ω RC of the GaP layer is measured to investigate the crystal quality, as seen in Figure 3-10a. The RC exhibits a narrow coherent central peak with FWHM of 8.6 arcsec and the lack of diffuse interference fringes on the tails. From the ω RC, the density of 60° closed dislocation loops in the volume of the GaP layer is roughly evaluated to be 1.1×10^5

cm^{-2}, which is comparable to that of GaP layer grown on Si wafers without the SiN_x layers. The asymmetric reciprocal space map around the Si and GaP (224) diffraction spots, as shown in Figure 3-10b, reveals that the relaxation of the initial elastic stress in the GaP is almost zero, *i.e.* the GaP layer is almost elastically strained to the Si wafer. Therefore, the crystal quality of the GaP is not affected by the SiN_x film.

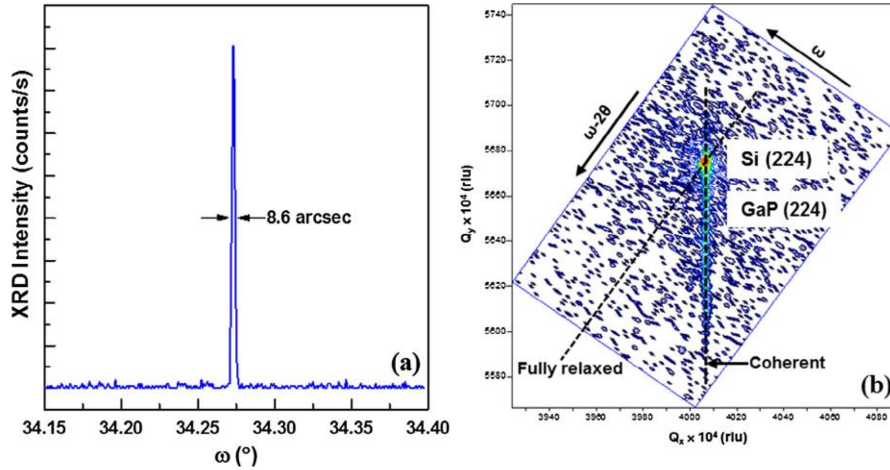

Figure 3-10 (a) XRD ω rocking curve of the GaP layer and (b) reciprocal space map around the asymmetric Si/GaP (224) diffraction spots. The same Q_x position of the both Si and GaP diffraction spots, elongated along the Q_y direction, demonstrates the lack of relaxation of the initial elastic stress in GaP layer during epitaxial growth.

To examine the Si bulk lifetime, GaP and SiN_x are removed from the GaP/Si/SiN_x structure and the wafer is passivated with the a-Si:H layers. As shown in Figure 3-11, the Si bulk lifetime (denoted by as-deposited) is found to be 1.83 ms at an MCD = 1×10^{15} cm^{-3}. The lifetime is increased up to 2.65 ms at the same injection level by performing a rapid thermal annealing (RTA) at 320°C for 20 sec in a nitrogen environment. This lifetime improvement is attributable to improved surface passivation by enhancing a hydrogen-rich interface between Si and SiN_x layers [30]. Therefore, it is demonstrated that the

introduction of SiN_x layers enables achieving both high bulk lifetime of Si wafer annealed at high temperatures and epitaxial growth of high quality GaP layers on Si wafer.

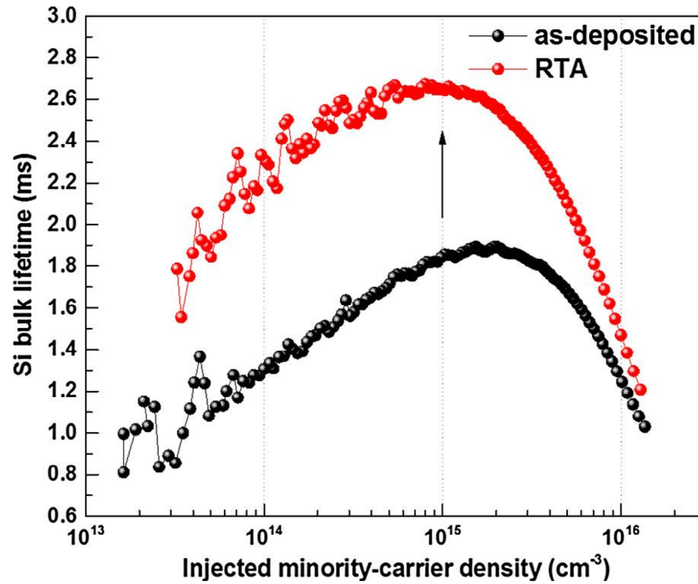

Figure 3-11 Si bulk lifetime as a function of injected minority-carrier density for the a-Si:H passivated GaP/Si sample before (as-deposited) and after the RTA.

3.4.3 Phosphorus Diffusion Layers

This method involves the formation of n+ regions on both sides of n-Si wafer by the phosphorus diffusion process. Prior to fabrication of GaP/Si solar cells, the effect of forming the n+ regions, as diffusion barriers and gettering agents, on the τ_{eff} was briefly investigated. The inset of Figure 3-12 shows the schematic diagram of the studied samples for the lifetime measurement. The Si wafers with n+ layers were annealed in the MBE chamber at different temperatures, 450, 600, and 800°C for 30 minutes. A reference Si wafer was also prepared with the same structure and no thermal treatment was applied. A detailed description of the fabrication methods and processes is discussed in an earlier publication [33]. The τ_{eff} of these samples at the injection-level of 10^{15} cm^{-3} is plotted in

the Figure 3-12. It is evident that the τ_{eff} of all samples, heated at different temperatures, are following the same trend as that of the reference cell. To give a comparison, the τ_{eff} of an unprotected Si wafer (bare Si wafer), τ_{eff}<1 µs, annealed at 800°C for 30 minutes in the MBE is dramatically lower than the protected wafers. These results clearly show that introducing the n+ layers can maintain the Si bulk lifetime during the annealing steps in the MBE chamber, which will lead to higher GaP/Si solar cell efficiencies (solar cells results are presented in the following sections). García-Tabarés *et al.* reported the similar lifetime recovery process in the MOCVD chamber [31] using PH_3 before the growth. The contaminants that reduce the lifetime during the high temperature annealing in the MBE originate from the back of the substrates [28], [41]. Khedher *et al.* shows that a phosphorus-based gettering agent, deposited using phosphoryl chloride ($POCl_3$) source, can getter impurities from Si wafer after undergoing a heat treatment in an infrared furnace [42]. The external or internal contaminants that potentially kill the lifetime can be collected in the n+ layers and kept away from the bulk of Si.

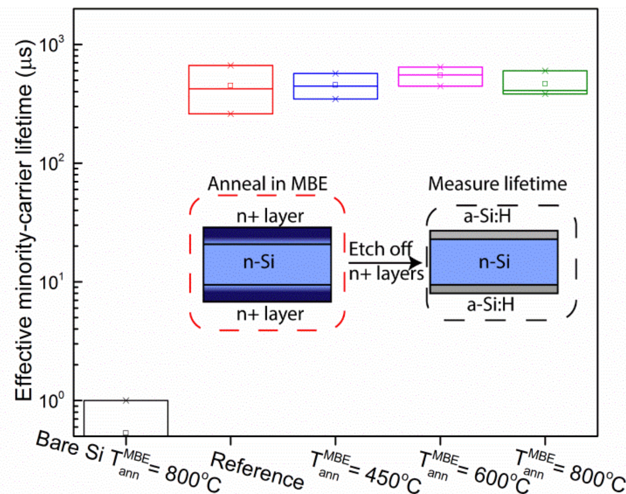

Figure 3-12 The effective minority-carrier lifetime of Si wafers annealed in the MBE chamber at different temperatures for 30 minues at the injection level of 10^{15} cm^{-3} (error bars are also indicated).

3.5 Conclusions

The severe Si-bulk lifetime degradation during MBE heteroepitaxial growth of III-V on Si is an obstacle to achieve high performance of Si-based multi-junction solar cells. We have shown that lifetime degradation is a thermally-activated process, independent of the doping types and silicon quality (Cz vs. FZ), and that the lifetime can be recovered via phosphorous diffusion gettering, which suggests that fast diffusing extrinsic contaminants originating from the MBE is responsible for this degradation. Coating the rear side of the silicon wafers with a sacrificial silicon nitride layer largely prevents the Si bulk lifetime degradation by providing both a diffusion barrier and a gettering interface and/or hydrogenation effect. The use of a SiN_x sacrificial layer successfully allows a Si minority-carrier lifetime at the millisecond level after various thermal treatments in the MBE growth chamber. Furthermore, a high-quality GaP layer is grown on SiN_x deposited Si wafer, which enables thermal deoxidation at a high temperature of 850ºC without degradation of Si bulk lifetime. Therefore, the experimental results presented here demonstrate that both high crystal quality of GaP and sufficiently high Si bulk lifetime can be achieved by applying SiN_x layers to GaP/Si heterostructures. It was also shown that by introducing P-diffusion layers, the Si bulk lifetime degradation can be suppressed. These approaches provide a technologically-relevant path to achieve high performance devices with III-V/Si integrated structures.

Chapter 4

GAP AS A HETEROEMITTER FOR SI SOLAR CELLLS

4.1 Introduction

The performance of conventional solar cell with phosphorus-diffused emitter is often limited by the surface recombination velocity, S_{eff}, and Shockley-Read-Hall, SRH, recombination centers, mainly due to the phosphorous diffusion process ($POCl_3$). These recombination mechanisms can impede the carrier collection of solar cell. In order to reduce the total recombination rate in the emitter, different methods have been suggested such as: thermal oxidation, ion implantation, deposition of dielectric film, and using p-n junction. One of the approaches related to the p-n junction method is based on deposition of hetero-emitter on a doped crystalline silicon substrate. It was shown by Sawada *et al.,* that good performance of solar cell can be achieved by incorporating an intrinsic amorphous Si (a-Si) as a passivation layer between a p-doped amorphous Si (a-Si) layer and an n-type c-Si layer. This hetero-junction solar cell with intrinsic thin layer, HIT, has demonstrated efficiencies more than 26% [4]. However, a-Si layer has low thermal stability and low free-carrier mobility. These can reduce the carrier collection through reducing the short circuit current of solar cell.

In order to further enhance the heterojunction solar cell performance, GaP, as a heteroemitter, has been theoretically shown to enable higher open-circuit voltages (V_{OC}) and higher conversion efficiencies [43]. GaP has significantly larger band gap (2.26 eV) and lower minority carrier concentration than that of a-Si (1.7 eV). GaP can provide multiple advantages over a-Si such as low recombination at Si interface, higher carrier mobility and formation of carrier selective interface due to its higher valance band offset

[13]. In addition, a high quality epitaxial growth of GaP on Si, with a small lattice mismatch (*f=0.4%*), can improve the solar cell performance through creation of low threading dislocation density in the volume and misfit dislocations at the interface.

In this chapter, we have demonstrated a method in which we were able to maintain the high Si carrier lifetime after the high temperature treatments by using SiN_x, grown by PECVD, at 350°C. SiN_x has been shown to be able to masks many diffusants and fast-diffusing recombination species during the thermal treatment due to its amorphous and tight structure in the previous chapter. This approach allows high quality GaP/Si hetero-junction solar cell through improving the carrier collection efficiency. In order to evaluate the effect of this method on the overall GaP/Si heterojunction solar cell performance, it was analyzed the electrical characteristics of different GaP/Si solar cells with different emitter thicknesses, doping levels, and configurations. These results represent the groundwork for further development and optimization of GaP/Si solar cells.

4.2 Experimental Details

In this chapter, prior to the loading of a Float Zone (FZ) Si wafer in the MBE vacuum chamber, the wafer was chemically cleaned by Radio Corporation of America (RCA) solution combined with hydrogen fluoride (HF). SiN_x with a nominal thickness of 150 nm was then deposited by plasma enhanced chemical vapor deposition (PECVD) on the backside of Si wafer at 350°C. Sample was grown on double-polished, float-zone (FZ), and p-type (001) Si substrate using a Veeco GEN III MBE system. This MBE is equipped with P valved cracker and Ga effusion cell. SiN_x/Si substrate is preheated in the MBE chamber to remove the residuary native oxide and reconstruct the surface. The growth

temperature was monitored using an *in-situ* thermocouple. After desorption of the surface oxide from the Si substrate, the growth temperature was reduced to 440°C to grow GaP layers. The GaP film was then epitaxially grown by migration enhanced epitaxy (MEE) method, which switching the Ga and P shutters to enhance atomic diffusing length.

To investigate the crystal quality and the degree of relaxation, asymmetric reciprocal space map (RSM) was performed around (224) diffraction spots of GaP and Si by XRD. The GaP epitaxial layer is elastically strained to the underlying Si layer. Hence, the threading dislocation density, as the major SRH recombination centers in the volume of GaP, was low.

To investigate the performance of solar cells based on the aforementioned growth method, two samples (A and B) with different emitter schematics were grown, fabricated as shown in Figure 4-1, and characterized. The dopant used for n-type doping of GaP layer is Si. Device A has a 50 nm GaP layer with the n-type doping level of 4×10^{18} cm^{-3}, while device B has a 10 nm unintentional doping (UID) GaP and 40 nm of n-type GaP with the doping concentration of 10^{19} cm^{-3}. Intrinsic a-Si (10 nm) and heavily boron-doped a-Si (10 nm) were then deposited with PECVD on the back side of the samples. To further investigate the structure of GaP as a heteroemitter, different thicknesses with unintentionally doped of GaP were grown on p-type Si wafers.

ITO (75 nm) and Ag (200 nm) were deposited using RF sputtering as contacts to n-type GaP and p-type a-Si. The thickness of ITO is selected to enhance the electrical conductance, form a constructive interference on GaP, and reduce the reflectivity of light. The samples were then annealed at 200°C for 20 minutes under atmospheric pressure. Both

contacts demonstrated ohmic behavior, measured by transmission line measurement (TLM) patterns.

The J–V characteristics of the devices were measured using a continuous Oriel class A solar simulator equipped with a Xenon ARC lamp (AM1.5G) (100 mW/cm^2). The spectral intensity was calibrated using a Si control cell to obtain the desired power. In addition, the external quantum efficiency (QEX10) was measured by a PV Measurements equipped with a dual grating monochromator, monochromatic probe light with long wavelength detection capability, and SRS lock-in amplifier.

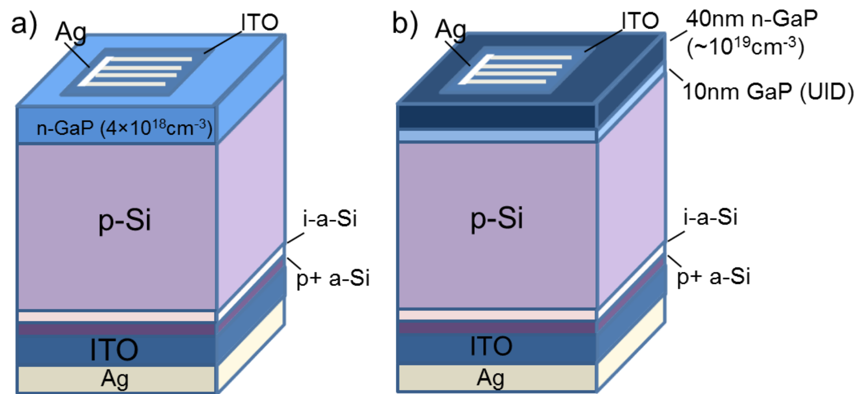

Figure 4-1 The schematic structures of GaP/Si solar cell devices: (a) Device A and (b) Device B.

4.3 Results and Analysis

4.3.1 Device A and Device B

All GaP/Si heterojunction solar cells demonstrate photovoltaic response. More than 80% EQE (Figure 4-2) is obtained at around 500 nm wavelength, which is at the range of GaP direct bandgap ~446 nm and indirect bandgap ~553 nm. The device performances were characterized by a solar simulator under one-sun illumination (100 mW/cm^2) at AM 1.5G. Table 4-1 shows the electrical characteristics of the solar cells. The J-V

characteristics of the solar cells (device A and device B) under dark and 1 sun conditions are shown in Figure 4. Device A exhibits an open circuit voltage (V_{OC}) of 0.516 V, a short circuit current density (J_{SC}) of 31.1 mA/cm^2, and a fill factor (FF) of 45.6%. In comparison, the same size sample with a UID GaP layer shows a V_{OC} of 0.512 V, a J_{SC} of 32.1 mA/cm^2, and a FF of 38.2%. It is evident that J_{SC} increases by introducing the UID layer in the emitter layer. The V_{OC} of both devices are strongly affected by SRH recombination centers, primary as a result of defect creation at the GaP/Si interface. Although the SRH recombination centers limit the performance of the solar cells, both devices show promising photovoltaic responses.

Diode fitting model was performed to understand the difference in performance between the samples

$$I = I_L - I_{01} \exp\left(\frac{e(V + IR_S)}{k_B T} - 1\right) - I_{02} \exp\left(\frac{e(V + IR_S)}{k_B T} - 1\right) - \frac{V + IR_S}{R_{SH}}$$

where T is the temperature, R_S is the series resistance, k_B is the Boltzmann constant, R_{SH} is the shunt resistance, I_L is the photo-current, and I_{01} and I_{02} are the first and second saturation currents, respectively. The results are presented in the Table 4-1. R_S were calculated from the linear portion of measured dark I-V characteristics and R_{SH} were determined from the slope of light I-V curve near the I_{SC}. The shunt resistance of sample A is 167 Ω, while it is 189 Ω in the sample B. Both devices are suffering from the leakage-current issues due to formation of defects in the GaP layer as confirmed by the low R_{SH} values, which negatively affect the V_{OC}. It was shown by both x-ray diffraction and transmission electron microscopy that UID GaP grown has a lower defect density compared to the n-doped GaP grown on Si substrate. The effect can be explained by

Shockley-Read-Hall (SRH) recombination process in the emitter region and shunt paths through the mesa sidewalls, mesa side walls were not passivated. The slight improvement in R_{SH} in sample B is mainly related to the less defect density originated from the dopants.

The low growth temperature (440°C) of GaP limits the phosphorus diffusion into the Si wafer and makes GaP a functional emitter. This will cause further increase in SRH centers in c-Si by introducing electrically inactive phosphorous precipitates. However, the device performance is still limited by the high surface recombination at the GaP/Si interface. The UID-GaP layer was initially introduced as a possible passivation layer but there is no evidence to support the role of this layer in reducing the surface recombination velocity (SRV) at the UID-GaP/n-Si interface. The band bending at the interface is caused by the band offset effects. The high doping of n-GaP (10^{19} cm^{-3}) causes the tunneling distance to be reduced, enhancing the tunneling probability. This can eventually increase the J_{SC} though improving the carrier collection efficiency. The UID-GaP/n-GaP can act as an electron selective contact due to its low conduction band offset and high valance band offset. Sample B has degraded series resistance and fill factor mainly due to the lack of contact optimization including current spreading layer (ITO) and metal contacts.

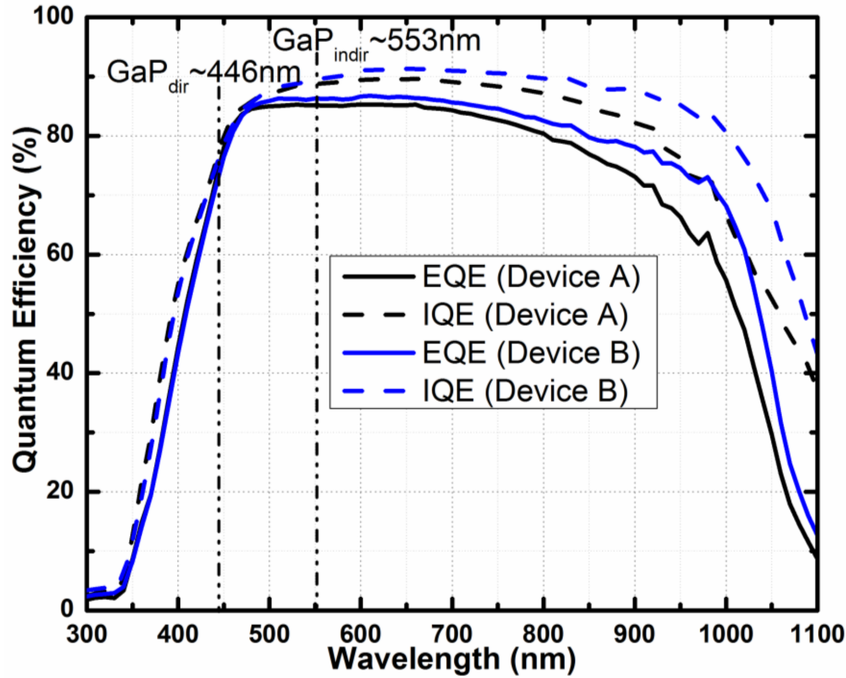

Figure 4-2 The EQE spectra and surface reflection of the fabricated GaP/Si solar cells.

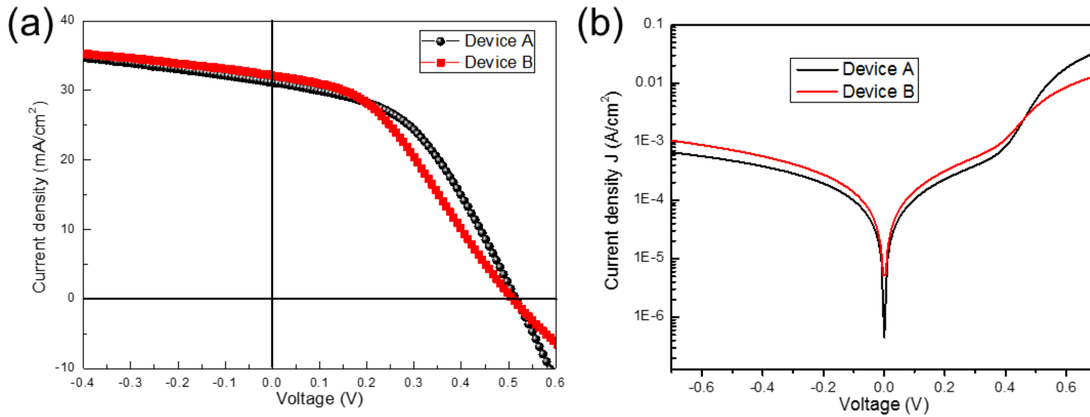

Figure 4-3 (a) AM1.5G illuminated current-voltage; (b) dark current-voltage of device A and device B

Table 4-1 Electrical characteristics of GaP/Si solar cells under 1 sun illumination

	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	R_S (Ω)	R_{SH} (Ω)
Device A	31.1	0.51	45.6	6.2	167
Device B	32.1	0.51	38.2	25.9	189

4.3.2 Unintentionally Doped GaP Layers

The p-Si/GaP cells with different GaP thicknesses were characterized. Figure 4-4 shows the EQE characteristics of the GaP/p-Si samples. The spectral responses of the p-Si/GaP cells at 300 nm are clearly lower than that of the p-Si reference cell and decrease as the GaP thickness increases, which indicates that the incident photons are lost by a high carrier recombination and parasitic absorption in the GaP layer. For wavelengths in the range of 370 to 600 nm, a significant increase in the EQE is observed. This mainly originates from a better front carrier collection of the GaP emitter. At 450 nm, it is observed more than 16% EQE enhancement for the 15 nm GaP/Si sample. Moreover, more than 96% of the EQE has obtained ~500 nm wavelength for the 15 nm GaP/Si sample, which is in the range of GaP direct (~446 nm) and indirect (~553 nm) bandgaps. At the long wavelengths (900 - 1200 nm), the EQE values of the GaP/Si samples are comparable to that of the reference cell, which indicates that they have similar rear passivation qualities and Si bulk lifetimes. Although the blue response enhancement was observed in the GaP/Si samples, the low open-circuit voltages can be due to the recombination loss at the frontsides of the cells, most probably from the GaP/Si interface and the GaP bulk. As listed in Table 4-2, the lifetime of GaP/Si structure is ~4 μs measured right after epitaxial growth and the back side of wafer is passivated by annealed SiN_x. Although the passivation of annealed SiN_x is degraded, the primary reason for low lifetime is the recombination at the interface of GaP and Si. And the implied-V_{oc} (iV_{oc}) value obtained from the photoconductance decay measurement indicates the theoretical open-circuit voltage of the sample and it is determined by the separation of the quasi-Fermi levels. Clearly, the low V_{OC} is due to the high surface recombination at the GaP/Si interface. 15 nm undoped GaP sample has a

higher short-circuit current than the 30 nm sample and it is consistent with the EQE spectra. The doping GaP sample has lower J_{SC}, which may due to the higher recombination in GaP layers introduced by the doping. All GaP/Si samples has higher J_{SC} than the reference wafer, which benefits from the higher bandgap of GaP layers than a-Si and so the less absorption loss in the front layers. It shows "S" shape in the I-V curve of reference wafer, which is due to the thick p-a-Si on the back of the wafer and forming a barrier for carriers transport.

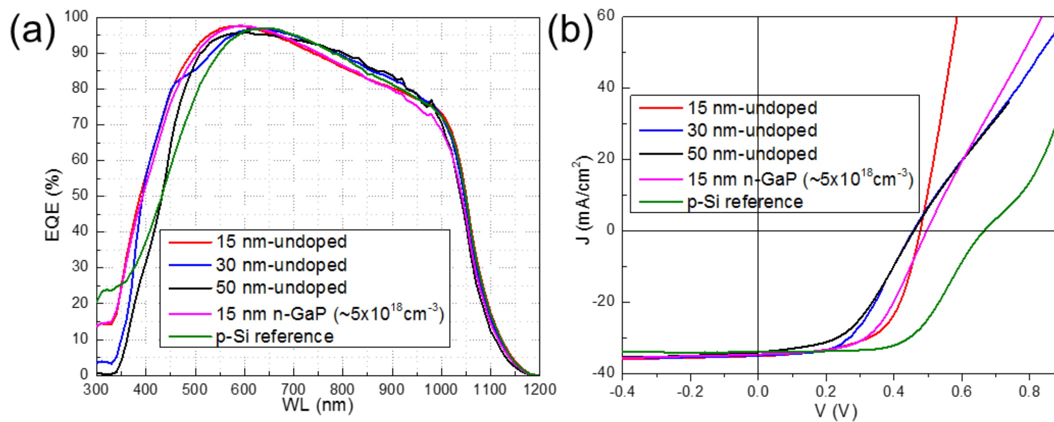

Figure 4-4 (a) External quantum efficiency (EQE) and (b) Light J-V curves of GaP/p-Si solar cells with various GaP thickness compared to the reference Si cell.

Table 4-2 Parameters of GaP/p-Si solar cells with various GaP thickness compared to the reference Si cell.

	15nm-undoped	30nm-undoped	50 nm undoped	15nm-Si (~5x10^{18} cm^{-3})	p-Si reference
Lifetime (μs)	4	4	4	4	266
iV_{OC} (mV)	536	534	526	529	651
J_{SC} (mA/cm^2)	35.1	34.9	34	34.6	33.9
V_{OC} (mV)	475	456	458	496	665

FF	0.604	0.507	0.478	0.557	0.59
η	10.10%	8.10%	7.50%	9.50%	13.30%

4.4 Conclusions

The performance of GaP/Si devices with different emitter structures were compared to give insight into the effect of GaP emitter design on the electrical properties. It is clear that GaP as a herteroemitter in GaP/Si solar cells could have a higher short-circuit current than the a-Si based Si heterojunction solar cells. However, low open-circuit voltage and low FF were obtained due the recombination at the GaP/Si interface. In order to achieve high performance of GaP/Si solar cells, the recombination loss at GaP/Si interface needs to be eliminated.

Chapter 5

GAP AS A BACK ELECTRON-SELECTIVE CONTACT

5.1 Introduction

Besides the crystal quality issues, arising from the lattice mismatch (*f*) between most of III-V materials and Si, achieving a high performance III-V/Si solar cell requires improving the carrier transport through the device by implementing novel contact architectures [44]. Among III-V material systems, gallium phosphide (GaP) is a good candidate for this integration. The lattice mismatch between GaP and Si is ~0.4%, smallest among all the III-V binary materials with respect to Si, and its indirect bandgap (E_G~2.26 eV) make GaP a suitable candidate to be used in Si heterojunction solar cells. Amorphous Si (a-Si) is widely being used as a passivation and a contact layer in Si heterojunction solar cells, enabling to achieve efficiencies of more than 25% [4]. However, GaP offers more advantages over a-Si, such as high carrier mobility, high valance band-offset (ΔE_V=1.05 eV), and low conduction bad-offset with Si (ΔE_C=0.09 eV) [13]. The last two features enable GaP to form a minority-carrier (electron) selective interface with Si and acts as a layer to suppress the thermionic emission and tunneling of photo-generated holes into other layers where they can be non-radiatively recombined [45].

GaP layer has been successfully used in Si solar cells with different architectures to improve the overall carrier collection efficiency [16], [18], [46], [47]. GaP was successfully demonstrated in a homojunction Si solar cell, as a window layer, with an open-circuit voltage of (V_{OC}) of 632 mV and efficiency (η) of 12.4% [18]. In addition, a GaP/Si heterojunction solar cell with an n-type GaP emitter has been theoretically shown to produce higher V_{OC} and η compared to the passivated emitter and rear solar cell (PERC)

[43]. It was experimentally shown a heteroemitter n-GaP/p-Si solar cell for the first time, however, the overall performance of this device is low [17]. Feifel *et al.* have shown higher quantum efficiency in the short wavelength regime (~ 350 - 700 nm) by using this heterojunction compared to the n-GaP/n-Si/p-Si homojunction cell [46]. Nevertheless, the reported V_{OC} and η show low values of 561 mV and 12.4%, respectively, which is still not comparable with PERC cell performance [48]. So far, a high efficiency GaP/Si solar cell (above 20%) has not been demonstrated yet. In order to do so, having a high Si bulk lifetime along with a high quality electron-selective GaP contact layer – with low interface recombination velocity and low contact resistance simultaneously - are crucial.

After establishing the effectiveness of these Si lifetime saving methods on the performance of GaP/Si solar cells, carrier collection efficiency can be further improved by implementing a novel p-emitter design to serve as a hole selective contact through reduction of parasitic absorption loss at low wavelength regimes, mostly due to (p+)a-Si/(i)a-Si stacks. In particular, it was shown that by using a molybdenum oxide layer (MoO_x) that has a higher band gap (~3 eV) than a-Si, as a hole selective contact, a higher optical gain at short wavelength regime can be achieved. In the present work, four heterojunction GaP/Si solar cells with different architectures of electron and hole selective contacts are grown, fabricated, and tested to give an insight into the carrier transport of GaP/Si solar cells.

5.2 Experimental Details

All the n-Si wafers used in this study were 4" Float-zone (FZ) (001), n-type, and double-side-polished with a thickness and a resistivity of 270 µm and 3 Ω.cm, respectively. The wafers were chemically cleaned with an RCA (Radio Corporation of America)

solution followed by a diluted hydrofluoric acid (5% HF) solution for 30 seconds and then rinsed with deionized (DI) water immediately prior to loading into the MBE chamber to remove the native oxide. All the epitaxially grown samples were grown using a Veeco GEN III MBE system equipped with P valved cracker operated at 960 °C and Ga and Si effusion cells. The surface reconstruction of the samples during the MBE growth was monitored via *in-situ* reflection high energy electron diffraction (RHEED) patterns.

To avoid introducing contaminants into the Si substrate, the first GaP/Si solar cell (structure I) was grown at 440°C, well below the critical temperature (T<500°C), where Si minority-carrier lifetime (τ_{eff}) starts to degrade significantly. It is shown in the earlier work that by avoiding the high temperature surface treatment (T<500°C), the Si lifetime of τ_{eff}>1 ms is achievable, which is comparable to that of unannealed Si wafer [33]. The growth of structure I was initiated without high temperature pre-heating for the purpose of surface reconstruction. The Si surface prior to the GaP growth showed a dim (1×1) RHEED pattern, whereas a clear and sharp (2×1) reconstruction RHEED pattern is expected during the Si deoxidation process at higher temperatures [49]. Without the surface reconstruction, a poor crystal quality of GaP was expected to form on the Si surface. During the GaP:Si growth a dim spotty RHEED pattern (not shown here) were observed which indicates that the GaP was formed from the coalescence of the island. The nominal Si doping level of the GaP for all samples were ~10^{18} cm^{-3}. After ~20 nm thick GaP deposition, the sample was taken out of the MBE vacuum environment and the subsequent a-Si layers (p+)a-Si/(i)a-Si were deposited on the other side of Si wafer by plasma-enhanced chemical vapor deposition (PECVD). Finally, indium-tin-oxide (ITO) (75 nm) and silver (Ag) (200 nm) layers were formed on both sides of the sample by RF sputtering

as a contact layer and a current spreading layer, respectively, as illustrated in Figure 5-1(a). The ITO film, as a transparent conductive oxide (TCO), was deposited on top of the (p+)a-Si film to attain a good lateral conductivity with a low ohmic contact to the Ag electrodes. The front ITO also acts as an antireflection layer to maximize the light coupling into the device. However, the rear ITO layer with Ag layer serve as a current spreading layer and an infrared reflector. Finally, all the cells capped with ITO layers were annealed in a muffle furnace at 220°C for 20 minutes in the atmospheric pressure to recover the a-Si interface passivation, which was degraded during the sputtering process. All the fabricated solar cells in this work are 1×1 cm^2.

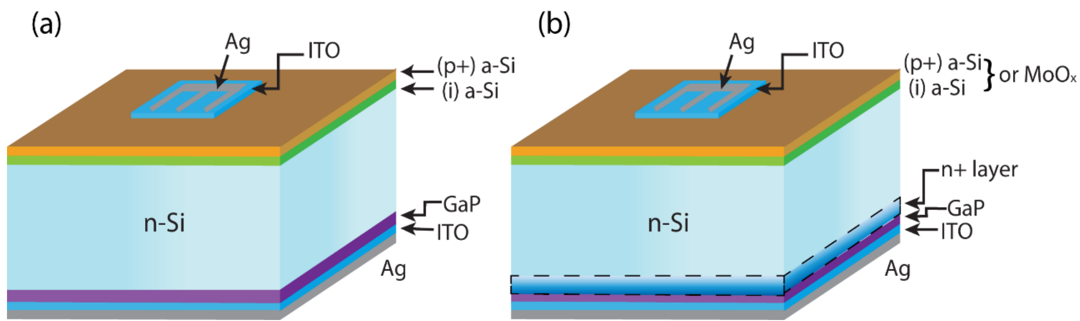

Figure 5-1 (a) Schematic of structure I, structure II and structure IV. (b) Schematic structure IIIA with a-Si-based layers on top. Structure IIIB has MoO_X layer instead of a-Si as a hole selective contact. The active area of the solar cells is defined as the area within the aperture (1×1 cm^2) that is not shaded by metal.

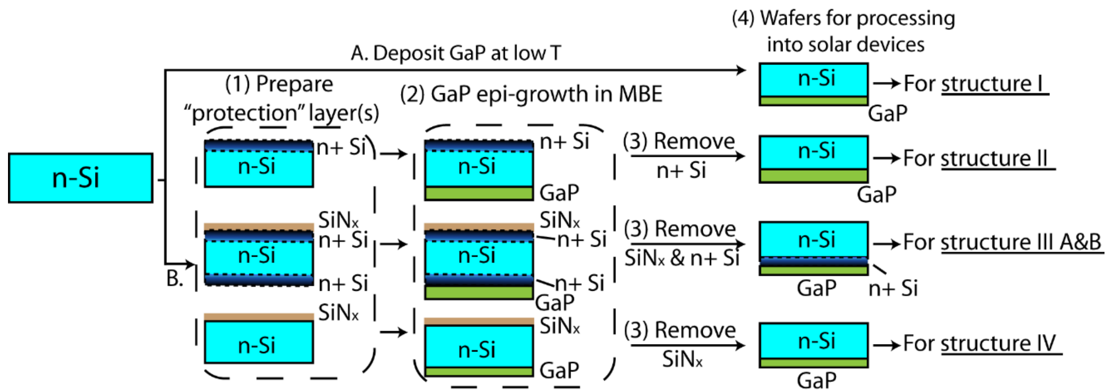

Figure 5-2 Simplified schematic diagram of preparing GaP/Si structures for structure I, II, IIIA, IIIB and IV.

In the second GaP/Si solar cell (structure II), an n+ layer was deposited on the backside of the Si wafer to act as a gettering agent. To form this n+ layer, a 200 nm thick SiO_2 layer was initially deposited at 200°C by PECVD on the frontside of the wafer. The SiO_2/Si wafer was then loaded in the diffusion furnace and exposed to O_2 and $POCl_3$ flows at 830°C to form a diffused phosphorus (P) layer on the backside. After the P-diffusion, the SiO_2 layer was etched by the buffered oxide etch (BOE) solution for 10 minutes and then rinsed with DI water. The simplified process is depicted in Figure 5-2. After SiO_2 removal, the Si wafer was loaded into the MBE chamber for the GaP deposition on the frontside of n-Si wafer. The growth was initiated with preheating at 800°C for 10 minutes to achieve high surface quality. A nominal 100 nm thick GaP:Si layer was then deposited at 540 °C by migration enhanced epitaxy (MEE) technique [11]. After the MEE GaP growth, ~30 μm of Si layer including the n+ region was isotropically etched by a mixture of hydrofluoric, nitric, and acetic acids (HNA) (10:73:17) at room temperature. This was followed by deposition of an (i)a-Si (8 nm) and (p+)a-Si (12 nm) on the etched side of the Si. Finally, Ag/ITO were deposited on the both sides, using RF sputtering, as shown in Figure 5-1a.

In the structure III, n+ layers were first formed on the both sides of the Si wafer by the P-diffusion in the furnace as explained earlier. Afterwards, a 150 nm thick SiN_x, as a diffusion barrier, was deposited on the backside of the sample by PECVD. The sample was then loaded in the MBE chamber and after the high temperature preheating process, a 25 nm thick GaP:Si layer was deposited at 580°C. As shown in Figure 5-2, the SiN_x layer and ~30 μm of the Si wafer including the n+ layer was etched by a concentrated HF solution to ensure a complete removal of the n+ layer from the backside of the structure (the GaP

layer was protected during the etching process). The GaP/Si sample was cleaved into two separate wafers, to deposit p-a-Si and MoO_X layers. In the first sample (structure IIIA), (p+)a-Si (16 nm)/(i)a-Si (9 nm) layers were deposited on top of the bare side of n-Si for the purpose of passivation and forming a p-emitter. In the second sample (structure IIIB), a 9 nm thick MoO_x were deposited by the thermal evaporation from a MoO_3 (99.99%) source at a base pressure of 5×10^{-7} Torr and a deposition rate of 0.5 Å/s on the bare side of n-Si. To fabricate these structures into the solar cells (Figure 5-1b), Ag/ITO layers were sputtered on both sides of the samples, using RF sputtering.

Two samples were prepared for structure IV, one was deposited with 15 nm unintentionally doped (UID) GaP layer, and the other one was deposited with 25 nm nominally 10^{18} cm^{-3} doping GaP. The Si substrates were coated by 150 nm SiN_x for preventing the lifetime degradation as described in Chapter 3. After GaP deposition and SiN_x removal, a-Si layers were deposited and ITO and Ag were sputtered as illustrated in Figure *5-1*a.

External quantum efficiency (EQE) was measured by the solar cell spectral response measurement system (QEX10), manufactured by PV Measurements. The IQE curves were obtained by correcting the EQE for the reflection. Light J-V characteristics of the solar cells were measured using the class A Newport solar simulator (one-sun AM1.5G), no shading correction factor was considered. Suns-V_{OC} (illumination-dependent or pseudo light J-V) characteristics of the samples were measured by a flash tester provided by Sinton Instruments. The pseudo light J-V shows the effect of series resistance on the carrier collection of the solar cell. All the measurements are in-house from the best cells across the wafers. The effective minority-carrier lifetime (τ_{eff}) was measured by quasi-

steady state photoconductance decay (QSSPC) using a Sinton lifetime tester. Unless otherwise stated, to acquire τ_{eff}, the samples were passivated by deposition of 50 nm thick (i)a-Si: H films, deposited by PECVD at 250°C.

5.3 Results and Analysis

5.3.1 GaP/Si Solar Cell Grown at Low Temperature (structure I)

As explained in the previous section, the first GaP/Si solar cell was grown at a low temperature regime (T_{Growth}<500°C), without Si surface reconstruction process which requires high temperature (over 700°C). The EQE and reflection corrected IQE curves of structure I are shown in Figure 5-3a. Figure 5-3b illustrates the light J-V and Suns-V_{OC} curves. The IQE curve shows the values of more than 90% at the wavelength range of ~550 to ~880 nm. The J_{SC} and V_{OC} have the values of 31.0 mA/cm^2 and 475 mV, respectively. The electrical characteristics of all the GaP/Si solar cells, presented in this work, including structure I, are shown in Table 5-1. The light J-V curve has a kink shape around the V_{OC}, which can be an indicative of an extreme form of a voltage-dependent photo current. This can be ascribed to a carrier collection issue or formation of a barrier along the structure. In particular, this probably indicates a band alignment issue at the GaP/Si interface impeding the extraction of electrons. In addition, this could be related to a poor quality of GaP:Si layer grown on Si and the presents of the interface states. Further investigation is necessary to understand the origin of this "S" shape in the J-V curve. The pseudo-fill factor (FF_0) and the pseudo-efficiency (η_0) show the values of 93% and 13.3%, respectively. However, the actual fill factor (FF) and the efficiency (η) have lower values, ~54% and ~8%, respectively. The as-grown bulk lifetime of structure I is ~1 ms, which indicates that the contaminants are not contributing to the low conversion efficiency and the low temperature growth mode

is effective to preserve the Si lifetime. The high FF offset ($\Delta FF = FF - FF_0 \sim 39\%$) and the high Si lifetime suggest that the device performance is significantly impacted by series resistance losses and carrier transport issues. These two loss mechanisms can be related to the GaP crystal quality and/or a poor interface passivation. The low quality of GaP layer and its interface with the Si are related to the oxygen and carbon surface contaminations (due to lack of Si surface deoxidation at the low growth temperature these contaminants were no removed from the surface) [50]. Thus, developing another practical method in which both a high Si lifetime and a high quality GaP can be achieved, which leads to a better GaP/Si interface quality, are crucial to achieve higher efficiency solar cells.

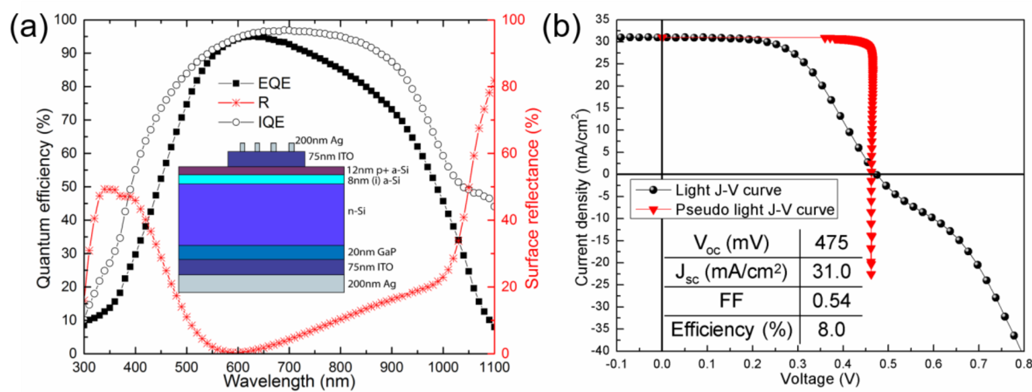

Figure 5-3 (a) EQE, IQE, and surface reflectance of structure I. (b) Light and pseudo J-V curves of structure I (under AM1.5G spectrum with irradiation intensity of 1000 $W.m^{-2}$). IQE is generated from the EQE data and the absorption data according to IQE = EQE/(1 – R).

Table 5-1 Light and pseudo J-V values for GaP/Si Heterojunction solar cells of structure I, II, IIIA and B

	Sample ID	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	FF_0 (%)	W_{OC} (mV)	η (~%)	η_0 (~%)
Structure I	G15-167	475	31.0	54	93	665	8.0	13.3
Structure II	G16-033	608	33.1	58	80	532	11.5	16.0
Structure IIIA	G16-115	618	33.1	64	80	522	13.1	16.5
Structure IIIB	G16-115	598	34.3	69	80	542	14.1	16.9

5.3.2 GaP/Si Solar Cell with “n+ layer” as a Gettering Agent (structure II)

Structure II was grown at elevated temperature of 540°C with the inclusion of the n+ layer as a gettering agent (complete description of sample preparation was elucidated in the experimental details section). Structure II demonstrates a PV response with higher electrical characteristics compared to the sample I, as shown in Figure 5-4. The measured main spectral response of structure II occurs in the range of ~350 to ~1100 nm. The EQE and IQE show the values of ~93% and ~97%, respectively. The top surface reflection (R) makes up the majority of the optical losses. This reduces J_{SC} and η of the device. The optical loss is more dominant at long (λ>1000 nm) and short wavelength (λ <350 nm) regimes. V_{OC} and J_{SC} show the values of ~608 mV and ~33.1 mA/cm^2, respectively, which are remarkably improved compared to the structure I. In addition, FF and η show high values of 57% and 11.3%, respectively, which are still lower than FF_0=80% and η_0=16%. The Si bulk lifetime of this sample was measured to be ~950 μs at the injection level of 10^{15} cm^{-3}, indicating that getterable diffusing impurities, do not have a significant impact on the carrier collection efficiency.

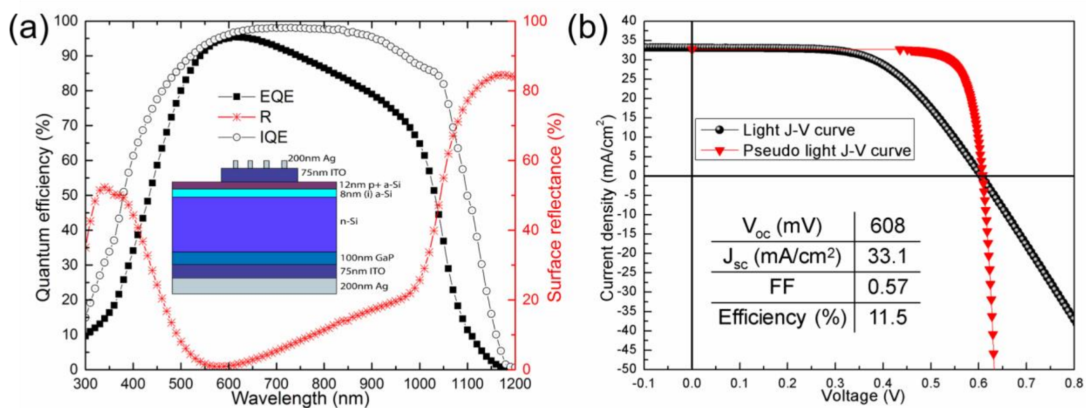

Figure 5-4 (a) EQE, IQE, and surface reflectance of structure II. (b) Light and pseudo J-V curves of structure II (under AM1.5G condition with irradiation intensity of 1000 W/m^2).

The improved solar cell performance (V_{OC} and FF) of structure II compared to the structure I indicates that the GaP crystal quality is improved (verified by XRD analysis, not shown here) since the GaP was epitaxially grown on a thermally cleaned Si surface, which led to a lower defect density in the volume and higher surface diffusion mobility on the surface of GaP layer. The superior cell performance of structure II can be also ascribed to a high Si effective minority-carrier lifetime, measured after the 560°C thermal treatment. Although the GaP layer partially passivated the Si rear surface and successfully acts as an electron selective contact, the defect at the GaP/Si interface and the GaP bulk are still the main limiting factors in achieving higher V_{OC}. These results imply that use of a diffusion barrier to maintain the Si bulk lifetime is crucial to achieve higher cell performances. However, both samples show poor EQE behaviors at the short wavelength regime (~300 to ~500 nm), which is mostly related to the recombination in the front layers. This suggests that the surface reflection and/or some carrier transport issues at the front side limit the cell performance. By adding an antireflection coating layer (such as SiO_X) on the ITO top layer [51] or texturing the front surface, the carrier collection efficiency can be significantly improved.

5.3.3 a-Si/n-Si/n+Si/GaP Solar Cell (structure IIIA)

All the GaP/Si samples discussed earlier in this chapter are suffering from the recombination at the GaP/Si interfaces. One approach to eliminate this recombination loss is using a n+ layer between n-GaP and n-Si layers, as briefly explained previously. To investigate the impact of the P-rich region (n+ layer) on the quality of the MBE grown GaP layer, the XRD measurements were performed. The double-crystal ω-2θ rocking curves are shown in Figure 5-5), including before and after the GaP growth (GaP/P-rich) and after

etching off the GaP and n+ layers (including the P-rich region). As observed in Figure 5-5a, a shoulder appears on the right side of the Si substrate peak for the GaP/n+Si/Si and n+Si/Si samples, which is due to the lattice strain induced by the P-rich region [52]. Furthermore, reciprocal space map (RSM) at the vicinity of the (224) diffraction spots of Gap and So was measured and plotted in Figure 5-5b, which reveals that the GaP is fully strained to the Si. The triple crystal (TC) ω full width at half maximum (FWHM) of the GaP peak is ~14 arcsec, and the threading dislocation density is calculated to be ~2×10^6 cm^{-2}. The RMS of the surface roughness was measured to be ~0.49 nm. As a result, a high quality of the GaP layer was achieved on the P-rich surface.

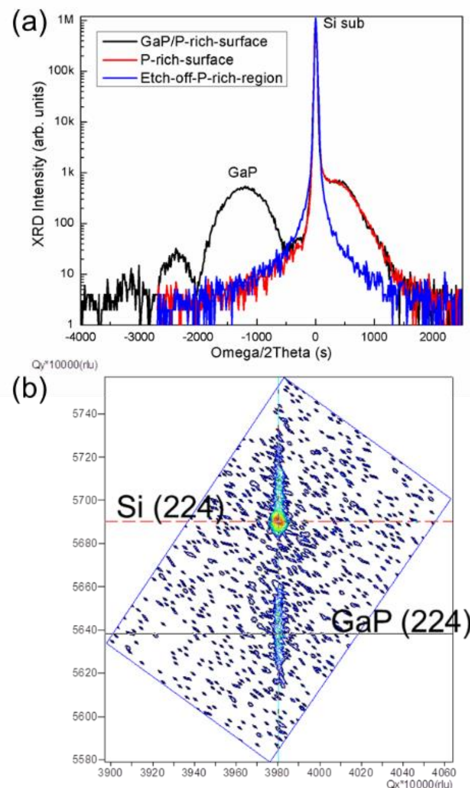

Figure 5-5 (a) Double crystal ω-2θ rocking curves scanned in the vicinity of (004) reflection (under symmetric geometry). (b) Reciprocal space map of the GaP/n+/Si sample at (224) reflection.

After the removal of SiN_x and n+ layer on the back, the minority carrier lifetimes of ~113 μs and ~2.2 ms at the injection level of 10^{15} cm^{-3} were measured from the GaP/Si sample and the bulk Si wafer, respectively. From these two measurements, high carrier collection efficiency through increased minority carrier diffusion length is expected. The IQE of structure IIIA, plotted in Figure 5-6, was compared to the counterpart sample with no n+ layer. It clearly shows that the IQE of structure IIIA is significantly higher, from ~900 to ~1150 nm. This suggests that the carrier collection efficiency at the n-emitter side is improved through the band bending at the interface of n+Si/GaP, caused by n+Si layer, and accumulation of electrons (n_e) at this interface.

The dark J–V curve (Figure 5-8b) of the structure IIIA was fitted with a double-diode model. The fitting parameters are listed in Table 5-2. The small slope at J_{SC} was fitted with a shunt resistance (R_{SH}) of ~1.26×10^3 kΩ·cm^2, indicative of no shunting problem in the device. Furthermore, the slope of the dark J-V curve around the V_{OC} was fitted to R_S~10 Ω·cm^2. Thus, more likely, a carrier transport (carrier collection) issue and not a shunting issue is responsible for the FF loss. The carrier transport issue of this device was further confirmed by the Suns-V_{OC} measurement, showing that the FF_0 and η_0 (FF_0 ~80% and η_0~16.5%) are significantly larger than the device FF and η (FF~64% and η~13.1%). By eliminating the main transport loss of the device (R_S), an overall 16% FF improvement can be achieved. This series resistance loss might be originated from different factors. On one hand, the ITO sheet resistance (~50 Ω/sq) and the contact resistance are responsible for a small portion of this resistive loss. One the other hand, the extraction loss from the (p+)a-Si to the ITO is also expected to contribute to the FF loss. However, the majority of 16% FF loss is expected to be from the GaP/Si interface. Although the conduction band offset

between GaP and n+Si is small, the GaP/Si barrier and the interface recombination velocity probably are the main contributors to the FF loss. Optimization of the GaP thickness and doping densities would lead to a low resistance loss and enhancement of carrier collection [44].

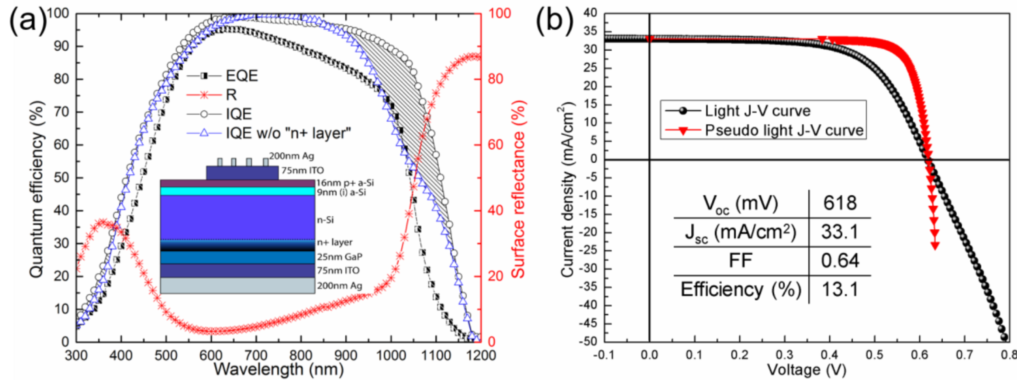

Figure 5-6 (a) EQE, IQE and surface reflectance of structure IIIA. (b) Light and pseudo J-V curves of structure IIIA (under AM1.5G condition with irradiation intensity of 1000 W.m^{-2}). The shaded region shows the optical gain at long wavelength regime (~900 nm - ~1150 nm) due to implementation of the n+ layer between the n-Si and the n-GaP layers.

5.3.4 MoO_X/n-Si/n+Si/GaP Solar Cell (structure IIIB)

The EQE of structure IIIA at the low wavelength regime is relatively low. This is mainly due to the parasitic loss, originated from the narrow bandgap of a-Si (~1.6 eV) and the high defect density of (p+)a-Si, used in the front layers [53]. For ultimate n-GaP/n-Si device performance, the frontside should be transparent in the range of ~300 to ~500 nm. MoO_X ($x<3$) can be a good alternative material to a-Si layer as a hole selective contact due its wide bandgap (~3 eV) and high work function [54]. Recently, a successful integration of MoO_X with a HIT (heterojunction with intrinsic thin layer) solar cell resulted in an efficiency of ~18.8% with a high optical gain at low wavelength regimes [55]. However, MoO_X film has not been shown before in a GaP/Si heterojunction solar cell. The novel

structure of MoO_X/Si/GaP can utilize the benefits of both GaP as an n-emitter and MoO_X as a hole selective contact. Motivated by this, a detailed investigation of the MoO_X/Si/GaP heterojunction solar cell (structure IIIB) is presented.

Figure 5-7a depicts the IQE, EQE, and light J-V characteristics of structure IIIB. The cell has a V_{OC} of ~598 mV, which is lower than the V_{OC} values reported for conventional high efficiency heterojunction solar cells [51] and structure IIIA. This suggests that the cell performance is affected by the interface passivation of MoO_x/Si. However, a J_{SC} of 34.3 mA/cm^2 for the MoO_x cell (structure IIIB) vs. 33.1 mA/cm^2 of the a-Si cell (structure IIIA) are consistent with the optical gain observed at short wavelengths (~300 to ~550 nm), determined by the IQE data.

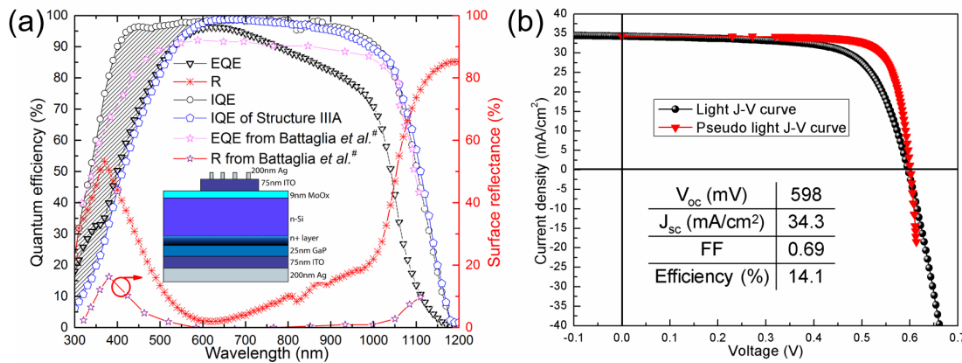

Figure 5-7 (a) The EQE, IQE and surface reflectance of structure IIIB (compared to the IQE of structure IIIA and the EQE of MoO_x/Si/a-Si solar cell reported by Battaglia et al. [56]). (b) Light and pseudo J-V curves of structure IIIB (under AM1.5G condition with irradiation intensity of 1000 W/m^2). The shaded region shows the difference between the IQE curves of structures IIIA and IIIB.

Table 5-2 Double diode device parameters of structure IIIA and IIIB

	J_{01} (mA/cm^2)	n_1	J_{02} (mA/cm^2)	n_2	R_{SH} (kΩ·cm^2)	R_S (Ω·cm^2)
Structure IIIA	3.60×10^{-10}	1.36	2.36×10^{-8}	2.6	1.2×10^{3}	10.85
Structure IIIB	6.60×10^{-13}	1.0	9.30×10^{-7}	2.5	10.6	1.06

In order to have an insight into the role of frontside absorption in structures IIIA and IIIB, ITO/(p+)a-Si/(i)a-Si and ITO/MoO_x layers, with the same thicknesses used in structures IIIA and IIIB, were deposited on glass substrates. The absorptance values of these two stacks were then compared. Figure 5-8a shows the simulated and measured absorptance of these two stacks. The simulation was performed by OPAL2 software, developed by McIntosh *et al.* [57]. It is evident from Figure 5-8a that the ITO/MoO_x stack has a lower absorptance compared to the ITO/(p+)a-Si/(i)a-Si stack. This led to a higher coupling of short wavelength photons into the device and improved the J_{SC} by 1.3 mA/cm^2. Moreover, the results show that the ITO layer is mostly responsible for the absorption of photons at wavelengths above ~600 nm. In structures IIIA and IIIB, the majority of the parasitic absorption loss below ~500 nm is originated from the a-Si layers, and, to a lesser degree, the ITO and the MoO_x layers [12]. In structure IIIB, as a result of using MoO_x layer, the short cut-off wavelength from the frontside is reduced to ~410 nm and the absorptance in long wavelengths remains below 3%. Based on these results, it is expected that by reducing the thickness of the (p+)a-Si layer in structure IIIA, the parasitic absorption loss at short wavelengths to be reduced. However, an extremely thin a-Si layer can cause the V_{OC} and FF to reduce, which then cancels out the effect of the J_{SC} improvement on the efficiency.

The dark J-V curve of structure IIIB was fitted to a double-diode model, as shown in Figure 5-8b. It shows a dark current density (J_{01}) of ~6.6×10^{-13} mA/cm^2 and an ideality factor (n_1) of ~1 (listed in Table 5-2). These values imply that there is no significant recombination mechanism in the bulk region and, thus, the lifetime of the Si absorber and the crystal quality of the GaP layer did not degrade the solar cell performance. Structure

IIIA and IIIB are not directly compared to structure I and II since many of their parameters are different (GaP thickness, carrier lifetime, and frontside a-Si thickness profile), which makes drawing a conclusive comparison between all these samples difficult.

The R_{SH} of structure IIIB with a value of 10.6 $k\Omega\cdot cm^2$ confirms a good crystal quality of the deposited layers, which means that the shunting issue is not a primary source of the loss, similar to structure IIIA. In addition, the small Rs (~1 $\Omega\cdot cm^2$) and the reduced FF offset ($\Delta FF=FF-FF_0$~11%) compared to the structure IIIA suggest that the ITO/MoO_x indeed improves the carrier transport and the conductivity of the front stack. This design shows that the (p+)a-Si/(i)a-Si layers can be successfully replaced by a thin MoO_x layer. Therefore, higher efficiency is achievable through reducing the parasitic loss and in the same time having a hole selective contact capability. The OPAL 2 simulation shows that optimizing the MoO_x thickness could further reduce the absorption loss and the front surface reflectance. The efficiency of the structure IIIB (~14.1%) is not improved significantly since it is observed a slight reduction in the V_{OC}, which can be attributed to the poor passivation of MoO_x/Si interface [55]. The high quality of the interface passivation can be achieved by inclusion of (i)a-Si layer between MoO_X and n-Si absorber layers at the expense of J_{SC} reduction [55]. The performance of structure IIIB is comparable to the best performing textured MoO_x/n-Si/(i)a-Si/(n+)a-Si solar cell reported by Battaglia *et al.* (V_{OC}=580 mV, FF=65%, and η=14.3%) [56], as shown in Figure 5-7a. The V_{OC} of structure IIIB is higher than the reported structure, which can be an indicative of better MoO_X and GaP passivation. Although, the reflection of the reported textured sample is significantly lower than that of structure IIIB, the integrated EQEs are almost similar. The difference between the EQEs is shown in Figure 5-7a. By implementing light trapping techniques,

such as texturing the surface, the MoO_x/n-Si/n-GaP structure has a potential to further increase its conversion efficiency.

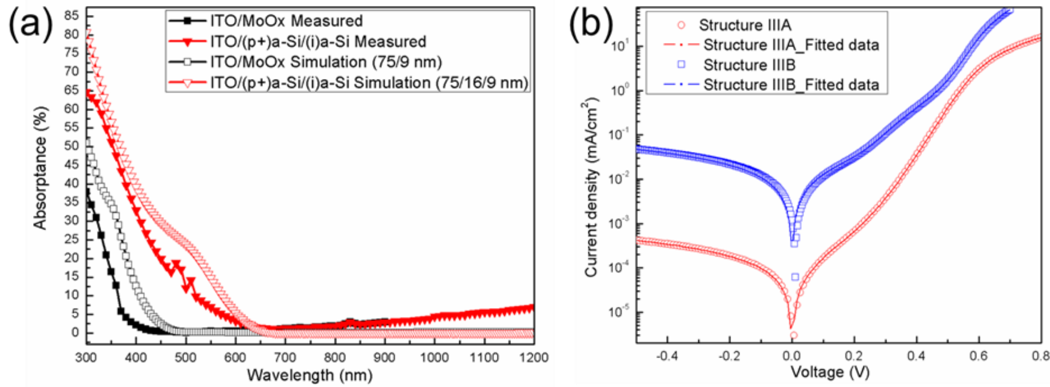

Figure 5-8 (a) Simulated and measured absorptance of ITO/MoO_x and ITO/(p+)a-Si/(i)a-Si front layers used in the GaP/Si heterojunction solar cells. (b) Experimental and simulated dark J–V curves of 13.1% and 14.1%-efficient GaP/Si heterojunction solar cells. The curve was fitted with a two-diode model with R_{SH}, R_S, and two recombination terms (no lifetime-minority correction factor was considered).

5.3.5 GaP/Si Structure with SiN_x Protection (structure IV)

A 15 nm unintentionally doped (UID) GaP layer was deposited on the n-Si wafer which was coated with a 150 nm SiN_x layer. After GaP epitaxial growth, the SiN_x layer was removed and processed into a solar cell. The solar cell performance with a short-current density of 31.3 mA/cm^2, an open-circuit voltage of 565 mV, a fill factor of 52.1%, and an efficiency of 9.2% was achieved. The external and internal quantum efficiencies are plotted in the Figure 5-9a. The GaP layer successfully acts as an electron selective contact on the n-emitter side. The GaP/Si cell IQE performance is comparable to that of the reference cell at the wavelength range of 300 – 800 nm. However, it is clear that the IQE of GaP/Si cell is much lower from 800 to 1150 nm, which indicates that the Si bulk lifetime is degraded and/or the GaP/Si interface has a poor passivation quality. The previous chapter has revealed that the SiN_x could maintain the Si bulk lifetime at milli-second level after the

GaP growth, also verified in this work. Therefore, the recombination at the GaP/Si interface is the primary factor in the IQE loss and the low open-circuit voltage.

Further, 25 nm nominally 10^{18} cm^{-3} doping GaP was deposited onto an n-type Si substrate coated with a 150 nm SiN_x layer. The sample after SiN_x removal was processed into solar cells with a structure of p-a-Si/i-a-Si/n-Si/n-GaP and ITO and Ag as the contact. The performance is shown in Figure 5-10, and one cell has 562 mV open-circuit voltage and 629 mV for the other one, however, both IV curves clearly show "S" shape, which may be due to a thicker layer of a-Si on the front layer and form a barrier for carriers transport. The EQE/IQE of the n-GaP sample is lower than the UID-GaP sample at the wavelength of ~300 - ~650 nm, and it indicates that the a-Si on the front of n-GaP sample is thicker than the other. Higher EQE at the long wavelength (~800 – ~1200 nm) of n-GaP sample indicates that doping GaP may have a better GaP/Si interface. Overall, the GaP/Si heterojunction solar cells with n+ layer for lifetime saving have a better performance than the one with the SiN_x protection layer.

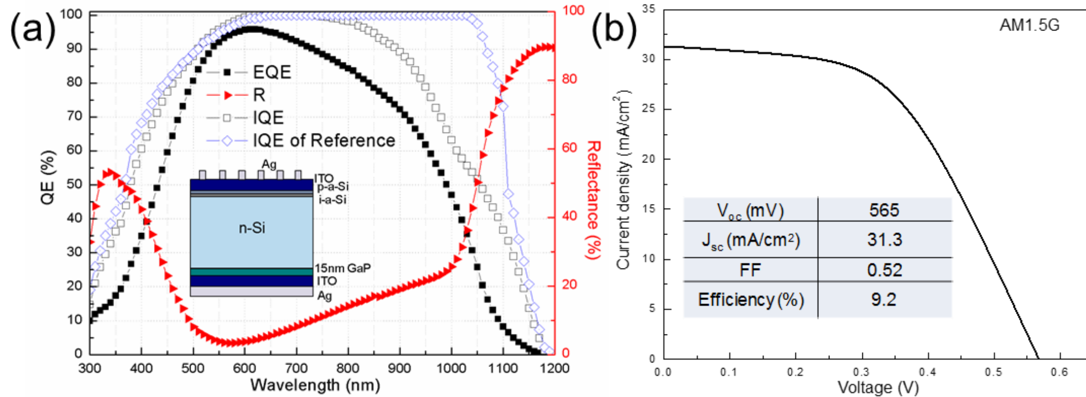

Figure 5-9 (a) EQE, IQE and surface reflectance of the n-Si/GaP solar cell and the n-Si reference cell (Inset: the n-Si/GaP schematic structure). (b) The corresponding light I-V curve.

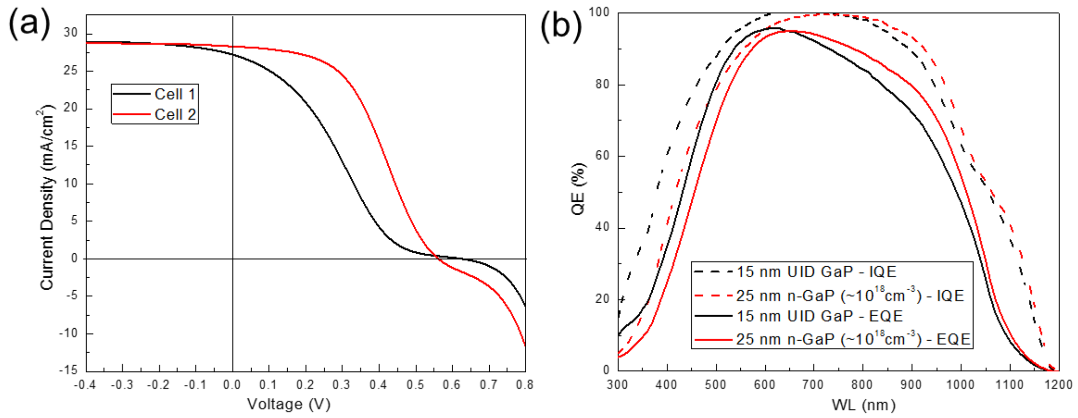

Figure 5-10 (a) Light I-V curves of n-Si/n-GaP solar cells. (b) The QE (EQE and IQE) spectra of GaP/Si solar cells with different doping in GaP layers.

5.4 Device Analysis

5.4.1 Surface Recombination of GaP/Si Interface

Deposition of GaP layer on a precisely oriented (001) Si substrate generally leads to the formation of antiphase domains (APDs) or antiphase boundaries (APBs) at the interface, as demonstrated by the high-resolution TEM image of the GaP (37 nm)/Si structure in Chapter 3. The presence of APDs, which act as recombination centers, has a detrimental effect on the open-circuit voltage (V_{oc}) and fill factor (FF)[46]. In addition to the APDs, the quality of the GaP layer can negatively impact on the solar cell performance by intruding high leakage current. The threading dislocation density (TDD) in the 37-nm thick-GaP layer of the GaP/Si structure is estimated from the HR-XRD rocking curves, showing a value of ~2.6×10^5 cm^{-2}. This relatively high TDD of the GaP can degrade the V_{oc} and consequently the total efficiency of the device, as demonstrated earlier by Yamaguchi *et al.* [58]. The misfit dislocations at the lattice mismatched interface will increase the surface recombination velocity (SRV).

In this work, the GaP layers were grown on (001) Si substrates by different methods to understand the limiting factors in the cell performance: (I) GaP (~20 nm) grown at low temperature regimes (Structure I), (II) GaP (~15 nm) grown with a SiN_x protection layer (Structure II), (III) GaP (~100 nm) grown with an n+ protection layer (Structure III), and (IV) GaP (~25 nm) grown on the n+Si layer protected by the SiN_x and n+ layers (Structure IV). It is worth to mention that all the protection layers (SiN_x and n+ layer) were etched away after the GaP growth to measure the lifetime, followed by deposition of an a-Si: H passivation layers. The effective lifetimes of the GaP/Si/a-Si samples were measured by a Sinton lifetime tester, as shown in Figure 5-11. It was shown that the a-Si: H passivation layer can reduce the surface recombination velocity (SRV) to values as low as 1 cm/s [34]. Thus, in this work, we assume that the surfaces are perfectly passivated by a-Si coating. The effective lifetime, τ, of the samples can be then calculated by [59]

$$\tau = \frac{1}{\frac{1}{\tau_{bulk}} + \frac{1}{W/_{v_s} + 4/_D \times (W/_\pi)^2}}$$

where, τ_{bulk} is the Si bulk lifetime, W is the wafer thickness (~270 μm), v_s is the surface recombination velocity (SRV) of the Si surface (GaP side), and D is the diffusivity of Si (~27 cm^2/s) [60]. By assuming different Si bulk lifetimes (0.25, 0.5, 1, and 2 ms), it is clear that the effective lifetime decreases rapidly as the SRV increases above than 10 cm/s. Thus, the effective lifetime is highly affected by the surface recombination rather than the Si bulk lifetime at high SRV values. As a result, the effective lifetime is mainly limited by the recombination at the GaP/Si interface as at high surface recombination velocities and the bulk lifetime difference (from 250 μs to 2 ms) has a negligible impact on the τ_{bulk},

although the bulk lifetime in different structures protected by different approaches may vary.

The GaP quality of Structure I is poor due to the 3D growth of GaP at a low temperature on a non-thermally cleaned Si surface, showing a lifetime of ~16 μs. From Fig. 1, the SRV is estimated to be around 7000 cm/s. For Structure II, an effective lifetime of ~32 μs was measured from the GaP/Si/a-Si structure. We speculate that the imperfect crystal quality of thin GaP layer can be the main recombination source. Structure III has a higher effective lifetime (~76 μs) compared to Structure II, which may be attributed to the n+ protection layer. The SRV value of Structure III is estimated to be around 350 cm/s. The higher lifetime indicates that the recombination impact from the GaP layer and GaP/Si interface is reduced in this structure. The mechanism is still not very clear to us, and it is possible that an n+ layer was formed at the GaP/Si interface, which can be formed during GaP/Si growth. In Structure IV, the n+ layer was intentionally introduced between the GaP and Si layers by a P-diffused layer formed in the furnace prior to the growth of the GaP. It is found that this structure has the highest lifetime value (about 110 μs), with a SRV value of around 200 cm/s. Meanwhile, another sample without the n+ layer at the GaP/Si interface shows a lifetime value of less than 20 μs (growth procedure of this sample is similar to Structure IV). It suggests that the n+ layer effectively acts as a back surface field and introduce a barrier for minority carriers moving to the rear surface [61], which can minimize the impact of recombination from GaP layers. Therefore, SRV estimated from an effective lifetime by photoconductance decay includes the ability of the doped layer to suppress minority carriers at the surface as well as the actual SRV right at the surface.

The trend in the open-circuit voltage in these four devices are consistent with their effective lifetimes, showing values of more than 600 mV for Structure III and Structure IV, while Structure I has the poorest performance as indicated by its low lifetime. To further improve the GaP/Si solar cell performance, better quality of GaP layers and passivation of the GaP/Si interface, such as hydrogen passivation, are required.

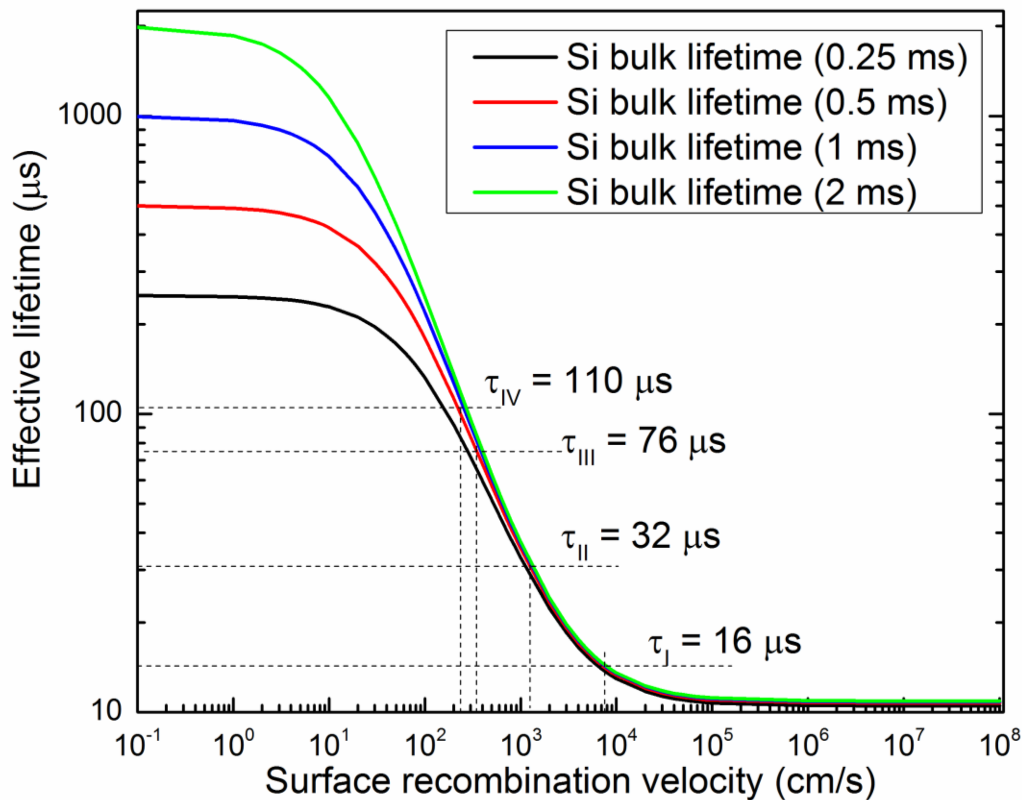

Figure 5-11 The effective lifetime as a function of surface recombination velocity at different Si bulk lifetimes. The effective lifetimes of Structure I, II, III, and IV are marked.

5.4.2 Band-alignment at the GaP/Si Interface

Figure 5-12a shows the band alignment of the GaP/Si interface derived by Anderson's rule [62]. The black curve stands for the case of lightly doped GaP and Si, the red dashed curved demonstrates the case for n+-doping of Si at the interface. It can be seen that the expected conduction band offset is only 0.25 eV and therefore, in theory should not hinder electron transport.

Combining all the results observed in our measurements [63] leads to a band diagram for the GaP/Si interface shown in Figure 5-12b. Band gap (BG) and electron affinity values were taken from literature. For this diagram, we used the measured results from our MOCVD grown samples (valence band offset 0.24 ± 0.12 eV), however, the findings for MBE grown samples were similar (0.30 ± 0.10 eV) and within the error bar. The band bending and depletion zone widths are drawn schematically for the case of slightly n-doped silicon (black) and silicon that is highly n-doped at the GaP/Si interface (red). It can be seen that n-doping of the Si at the interface bends the band down and results in a lower tunneling barrier for electrons. This explains the increase in fill factor and open circuit voltage for solar cells with highly n-doped Si at the GaP/Si interface.

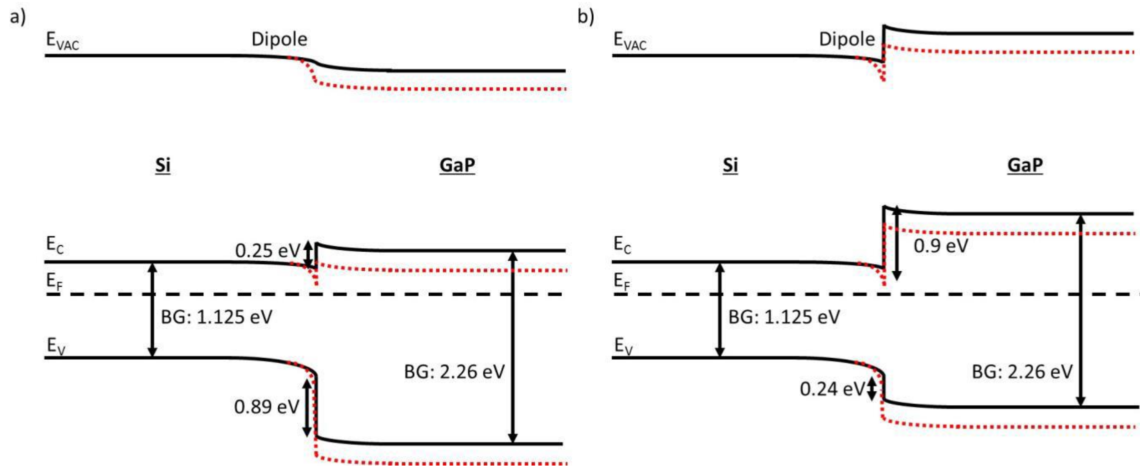

Figure 5-12 (a) Band diagram predicted by Anderson's rule and (b) band diagram derived from the extensive X-ray photoelectron spectroscopy (XPS) and cross-sectional Kelvin probe force microscopy (KPFM) data. The black curve presents the band alignment for lightly n-doped Si. The red curve takes an n+-doped Si layer at the interface into account. Therefore, the conduction band tunneling barrier is decreased. [63]

5.5 Conclusions

The n-GaP/n-Si heterojunction solar cell is a good platform to explore the possibility of achieving higher efficiencies in Si heterojunction solar cells. In this type of heterojunction solar cell, GaP serves as an electron selective contact. One of the major obstacles in GaP/Si integration is the low bulk lifetime of Si after its thermal treatment in the MBE. In this chapter, different GaP/Si solar cells were also designed and fabricated based on the lifetime saving methods descripted in Chapter 3. The solar cell with (p+)a-Si/(i)a-Si/n-Si/n-GaP structure shows an open-circuit voltage of ~618 mV and total efficiency of 13.1%. Parasitic absorption in the front (p+)a-Si layers was shown to be a major limiting factor in achieving higher J_{SC} and FF. The Suns-V_{OC} measurement and fitting of the dark J-V curves indicate that the significant FF loss originates from the R_S and some transport issues at the heterojunctions. In addition, it was shown that increasing the p-emitter bandgap and using a higher work-function hole selective contact are crucial

in further improving the GaP/Si heterojunction efficiency. Motivated by that, MoO_X was successfully used to reduce this parasitic absorption loss, caused by the (p+)a-Si hole contacts. It is observed an IQE enhancement and 10% improvement in J_{SC}, which translated into an efficiency of 14.1%.

Chapter 6

GAP ON PASSIVATION MEMBRANE LAYERS

6.1 Introduction

According to band offset between GaP and Si, GaP is good for electrons transport, while a barrier for holes. However, as mentioned earlier, notably Si bulk lifetime degradation during the GaP growth which occurs during the high temperature (>500°C) deoxidation process in MBE chambers. Also, up to now, little to no passivation of the silicon surface was obtained from directly depositing GaP on bare Si surface even for fully strained epitaxial films with a low threading dislocation density. Well surface passivation and high minority carrier lifetime are essential to approach high efficiency solar cells. It has been demonstrated in MoO_x/Si solar cells that the performance was boosted after inserting a-Si passivation layers at the MoO_x/Si interface [55]. Motivated by this, a dedicated passivation layer can be introduced before the GaP deposition. The passivation layer is also functional as a current-carrying contact, which should be thin enough or conductive enough to allow carrier collection into the GaP layer and then into metal contact. Further, the passivation layer should not degrade in the passivation during GaP deposition.

In this chapter, different passivation layer candidates including tunnel oxide, a-Si:H, low-carbon-content a-SiC:H and Al_2O_3 layers were compared; these compounds were investigated at increasingly high processing temperatures for the GaP deposition in the MBE chamber. Symmetrical stacks of passivation layer / n-type GaP were fabricated with GaP was deposited at different temperatures, and the minority-carrier lifetime of wafers was measured by operating the quasi-steady state photoconductance (QSSPC) setup.

6.2 Different Passivation Membrane Layers

6.2.1 Tunnel Oxide

Tunnel oxide which has been demonstrated to be high passivation quality [64]–[66] and excellent thermal stability is an excellent candidate as the passivation membrane. In this work, an ultra-thin (1 - 2 nm) layer of SiO_2 is formed by wet-chemical growth. Subsequently, a phosphorous doped a-Si (n+ a-Si) was deposited, and then samples were annealed in a tube furnace at 850°C for 1 hr to form the passivation layer. Substrates used were n-type 750 Ω-cm, ~275 μm thick Fz silicon wafers. After anneal, the a-Si layers coated on the wafers were crystalline and became semi-crystalline [67]. Wafers with annealed were loaded into MBE chamber, after degas processes (< 300°C), a nominal 50-nm-thick GaP layer was deposited at 440°C with Si doping via MEE method on this structure. Two doping levels were applied by controlling the Si effusion cell temperature, which was 1150°C for sample Structure I, while 1250°C for sample Structure II. Hence, the GaP doping in Structure II has a higher doping level than Structure I.

Fabricating a complete device (Figure 6-1) applying this stack as an electron-selective contact on the back side and an intrinsic/p-type a-Si:H-based hole contact at the front. A metal stack Pd/Ge/Pd was deposited on GaP surface via e-beam evaporator. The pseudo light IV curves were measured by Suns-V_{oc} for sample Structure I and Structure II (Figure 6-2). 666 mV V_{oc} for Structure I and 685 mV V_{oc} for Structure II were obtained, respectively. Quantum efficiencies including EQE and IQE are plotted in the Figure 6-3. The sample Structure I has higher quantum efficiency than Structure II at the short wavelength (300 nm – 600 nm) may be resulting from the thickness different of front a-Si or ITO layers on samples surface. Consequently, the short circuit current J_{sc} was calculated

from EQE to be 33.3 mA/cm^2 for Structure I, which is higher than sample Structure II 32.3 mA/cm^2.

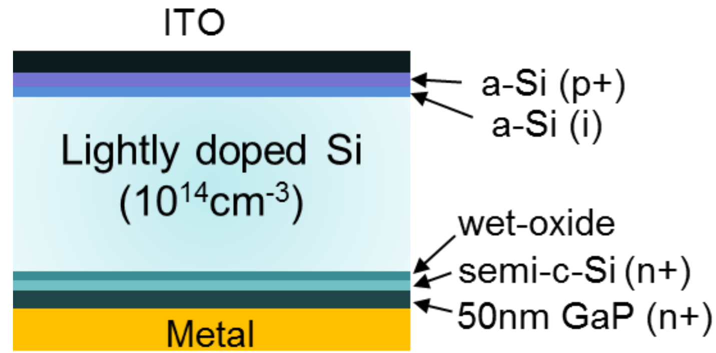

Figure 6-1 The schematic device structure of GaP integrated with tunnel oxide solar cells.

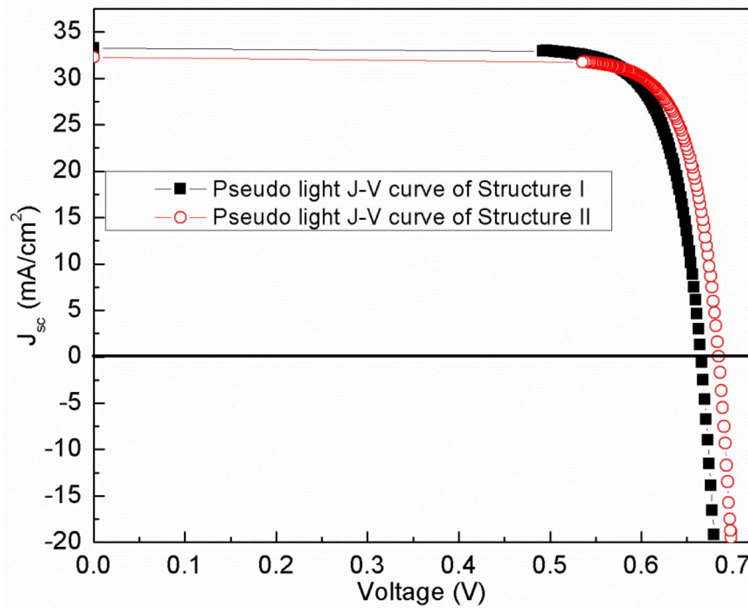

Figure 6-2 Pseudo light IV curves of the (a) Structure I, (b) Structure II.

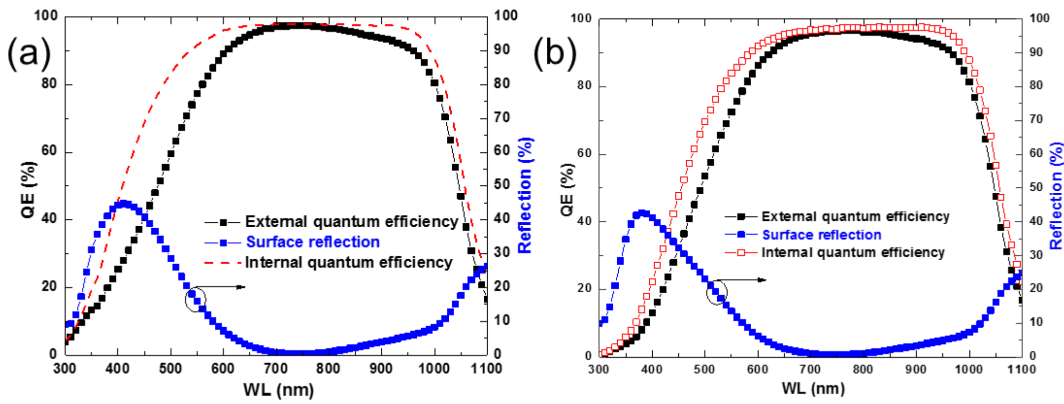

Figure 6-3 Quantum efficiency (QE) and surface reflection of (a) Structure I, (b) Structure II.

6.2.2 a-Si or SiC Layers

Figure 6-4a illustrates that the GaP deposits on Si substrates which are coated by intrinsic a-Si or SiC. As 20 nm Be doped GaP deposited at 280°C with a deposition rate of 2.05 Å/s on the the Si substrate with ~10 nm (i)a-Si surfaces, 734 mV implied open circuit voltage (iV_{oc}) under one sun illustration was achieved as shown in Figure 6-4b, which is a promising result. However, due to the high resistance GaP layer, which was deposited on a relative low temperature (280°C), and no electrical contact can be made out of this sample.

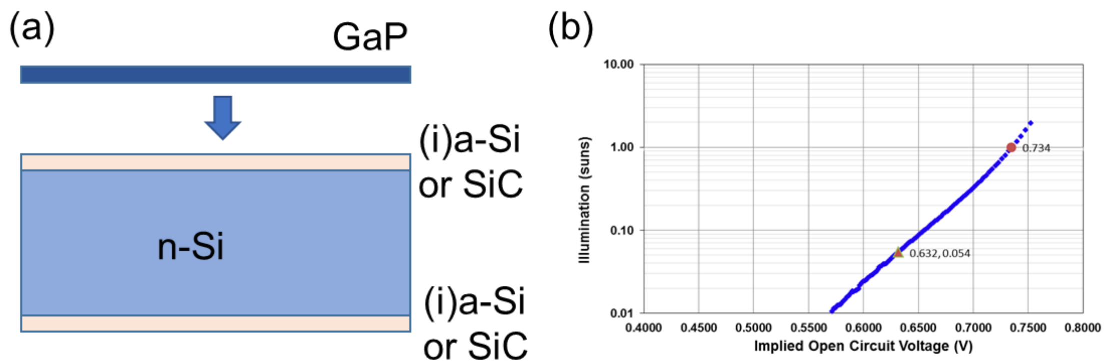

Figure 6-4 (a) Schematic of GaP deposited on a-Si or SiC passivated Si wafers. (b) Implied open circuit voltage of the sample after GaP deposition.

A higher GaP deposition temperature was applied to further investigate the GaP/Si structures with a-Si or a-SiC passivation. For the intrinsic a-Si:H as the passivation layers, after 40 nm Si-doped-GaP deposition at 350°C, the minority carrier lifetime was improved from 3.3 ms to 3.8 ms with 728 mV implied V_{oc}. A 15-nm-thick stack of a-SiC:H and a-Si:H was deposited on both sides of Si wafers via PECVD, following 40 nm of Si-doped-GaP deposition at 400°C by MBE. After deposition, the lifetime of the sample was improved from 278 μs to 1.48 ms with 703 mV implied-V_{oc}. For the lower-temperature grown GaP on a-Si:H and a-SiC:H, the formation of Ohmic contacts proves more challenging due to the dopants inactive issue in low temperature grown GaP, while as well known that a-Si:H or a-SiC:H passivation is degrading easily at high temperature.

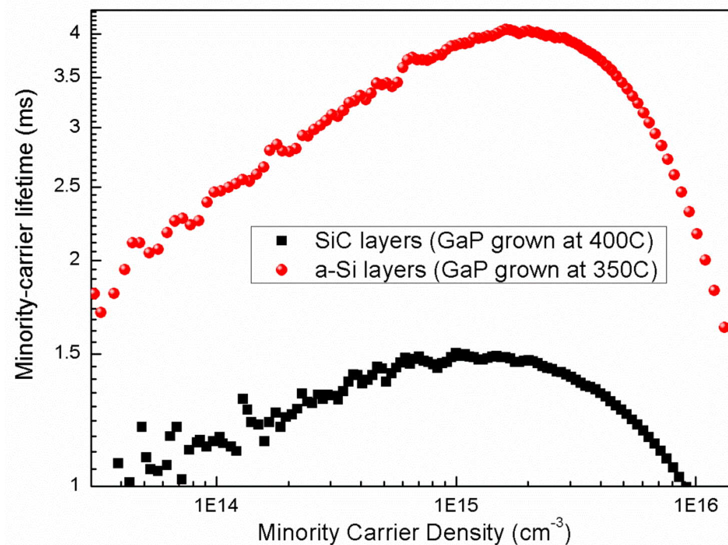

Figure 6-5 The minority-carrier lifetime of GaP/Si structures with SiC layers or a-Si layers

Further, GaP was designed to be a heteroemitter as shown in Figure 6-6a, and a 15 nm GaP layer was deposited at 360°C and 440°C, respectively. For comparison, another sample was prepared without a-Si coated and processed into a device as shown in Figure 6-6b. ITO layers were applied to contact GaP layers and collect carriers. It is worth to

mention that the wafer was not pre-heated to high T for deoxidation in order to prevent the Si minority-carrier lifetime degradation. In Table 6-1, the lifetimes of GaP/Si structures are listed, and it is clear showing that without a-Si at the GaP/Si interface, bare passivation from the GaP layer to the Si. As the GaP deposition temperature increases, the passivation from a-Si is degraded and so the lifetime is lower. From the EQE spectra plotted in Figure 6-7a, the EQE curves at 300 nm to 700 nm are separated, which indicates that the GaP quality difference among these three samples and without a-Si sample is better than the ones grown on a-Si surface, while the higher deposited temperature (440°C) is better than the one deposited on lower T. However, the I-V performances are quite poor for all these three samples as plotted in Figure 6-7b. The short-circuit currents measured from I-V measurement are much lower than the J_{sc} value integrated from EQE spectra, which may be as a result of the no uniformity of the GaP layers that some area may have more defects than others, while the EQE was measured at "good" spots.

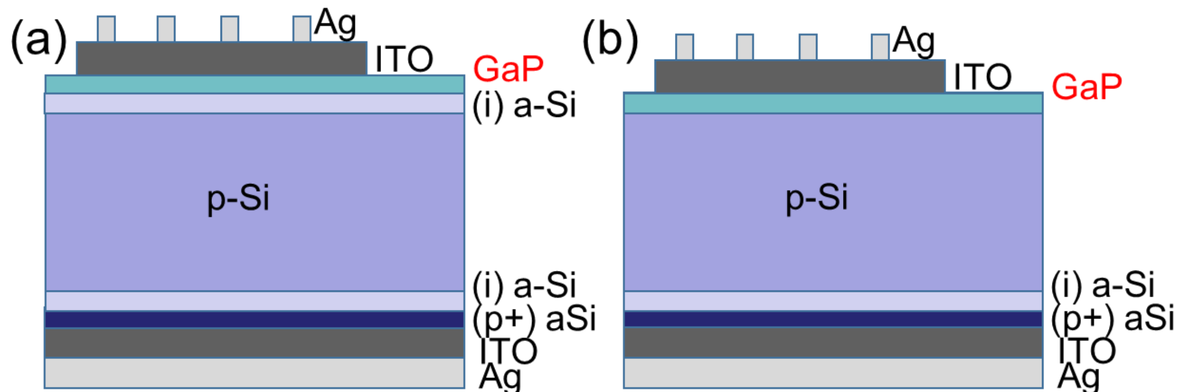

Figure 6-6 Schematic of the GaP/Si solar cell with a-Si passivation layers and GaP is as a heteroemitter.

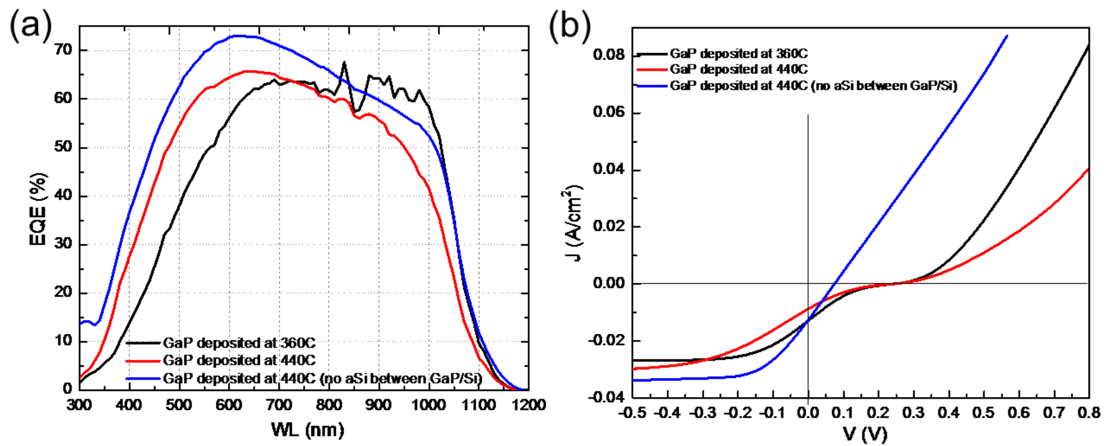

Figure 6-7 (a) The EQE spectra, and (b) light-JV curves of GaP/Si with a-Si passivation layers structures for GaP deposited at two different temperatures and compared to the sample without passivation layers.

Table 6-1 Parameters of GaP/Si with a-Si passivation layers structures

	15nm GaP deposited at 360°C	15nm GaP deposited at 440°C	15nm GaP deposited at 440°C w/o a-Si
Lifetime (μs)	232	93	3
iV_{oc} (mV)	648	612	523
J_{sc_eqe} (mA/cm^2)	21.9	22.5	25.7
V_{oc} (mV)	238	230	74
J_{sc} (mA/cm^2)	12.7	8.7	12.5
FF	0.147	0.152	0.253
Efficiency	0.44%	0.31%	0.23%

Instead of GaP as a heteroemitter, another set of samples were prepared as the schematic of Figure 6-8 that GaP was deposited on the back of the textured Si wafers. The wafers used were ~180 μm Cz Si wafers. The EQE spectra and light J-V curves were plotted in Figure 6-9. It was observed from Table 6-2 that the lifetimes of the samples are low due to the thermal damage or deposited GaP layer degraded the a-Si passivation.

Benefited from the slightly better passivation, the 280°C-deposited sample has slightly better EQE than the 350°C-deposited sample at the wavelength of 450 nm to 800 nm. For both samples, the EQE is more than 90% at 600 nm to 800 nm attributed to the light trapping from the texture surface. However, the low open-circuit voltages were obtained for both samples, which revealed that the extremely high recombination in GaP layers are still a big issue in such structures.

Therefore, it is promising to insert a-Si or SiC at the GaP/Si interface, nevertheless, in order to achieve high performance device results, the better quality of GaP layers is required, especially, the good conductivity of GaP deposited at low temperatures.

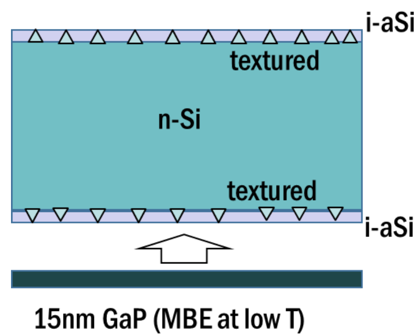

Figure 6-8 Schematic of GaP/Si structure with a-Si passivation layers and Si wafer is textured.

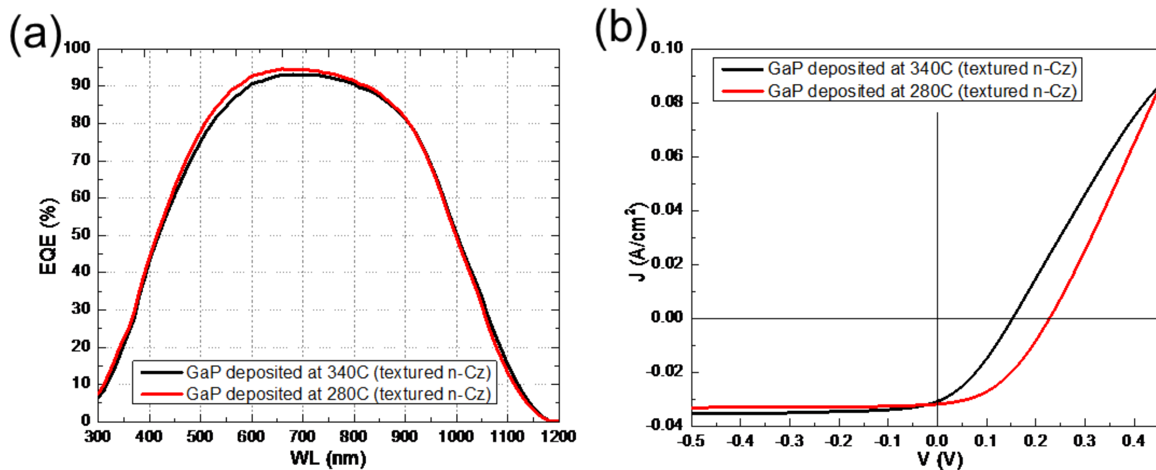

Figure 6-9 (a) The EQE spectra, and (b) light-JV curves of the GaP/Si solar cells that GaP deposited at 340°C and 280°C.

Table 6-2 The parameters of GaP/Si solar cells that GaP deposited at 340°C and 280°C.

	GaP deposited at 340°C (textured n-Cz)	GaP deposited at 280°C (textured n-Cz)
Lifetime (μs)	14	13
iV_{oc} (mV)	567	565
J_{sc_eqe}(mA/cm^2)	32.3	32.7
V_{oc} (mV)	152	228
J_{sc} (mA/cm^2)	30.7	31.7
FF	0.337	0.424
Efficiency	1.6%	3.1%

6.2.3 ALD-Al_2O_3 Layers

Another promising passivation layer is Al_2O_3 layers deposited by atomic layer deposition (ALD), which has been reported to be well passivation to Si at 600°C [68], [69]. Approximate 10 nm Al_2O_3 was coated on Si wafers via temporal atomic layer deposition (ALD) at 200°C, followed by 20 nm GaP deposition at 440°C in the MBE chamber as shown in Figure 6-10a. The PL map in Figure 6-10b shows the GaP deposited area (semicircle) is brighter than the area without deposition, which indicates the lifetime of GaP deposited area is higher than other area. Further, the doping in GaP layers was varied from n-type to p-type and for both n-type and p-type Si substrates. From Table 6-3 and Figure 6-10, the sample with p-GaP deposition has the highest lifetime and the lifetime is not higher for the heavier n-type doping in the GaP sample. All the lifetimes of GaP deposited samples are higher than both the non-annealed sample and the annealed sample, which was annealed at the exactly same thermal conditions (temperature and time) as GaP-deposition samples, except no GaP was deposited onto the surface. These interesting results

may indicate GaP deposition could enhance the Al_2O_3 passivation for Si wafers, and as high as 3 ms minority-carrier lifetime was achieved, which is promising. However, the thickness of dielectric Al_2O_3 is too thick for carriers to transport or tunnel.

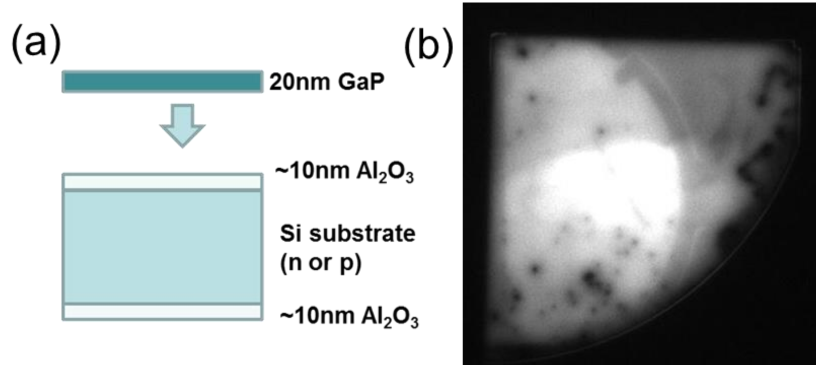

Figure 6-10 (a) Schematic of GaP deposited on Al_2O_3 coated Si substrate. (b) The PL map of the GaP deposited on Al_2O_3 coated Si substrate.

Table 6-3 Minority-carrier lifetime and iV_{oc} of different doping GaP deposited on Al_2O_3 coated n-Si and p-Si substrates.

	As-received (ALD)	Annealed in MBE	n-GaP ($\sim10^{18}cm^{-3}$)	n-GaP ($\sim10^{19}cm^{-3}$)	p-GaP ($\sim10^{18}cm^{-3}$)
n-Si	399µs/666mV	1.6ms/686mV	2.8ms/708mV	1.9ms/704mV	3.2ms/711mV
p-Si	218µs/665mV	N/A	1.0ms/706mV	665µs/696mV	1.3ms/712mV

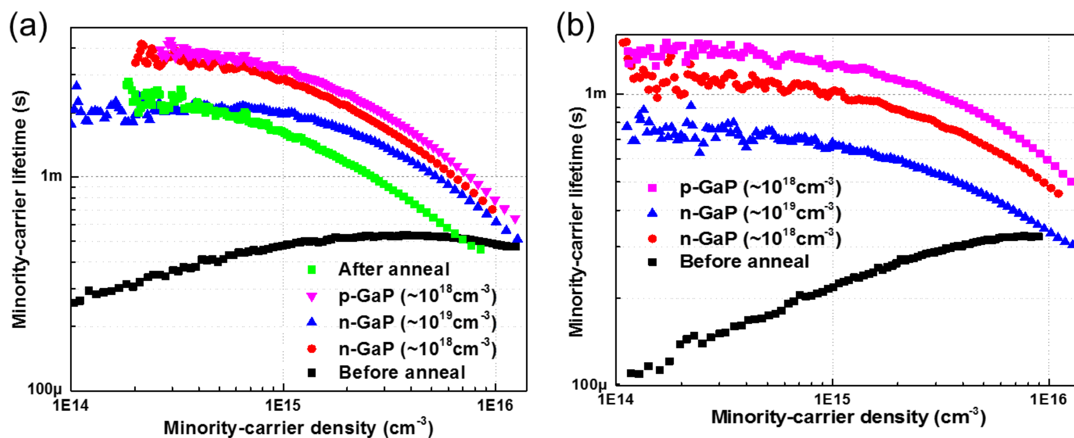

Figure 6-11 The minority-carrier lifetime of GaP with various doping deposited on Al_2O_3 coated (a) n-type and (b) p-type Si substrates.

6.3 Conclusions

In this chapter, different passivation membrane layers including tunnel oxide, a-Si, SiC and Al_2O_3 (ALD) were discussed. Good thermostability of tunnel oxide and Al_2O_3 are suitable for depositing good conductive GaP layer, unfortunately, the thickness of Al_2O_3 in this study is too thick for a functional device. 685 mV open-circuit voltage was achieved from the tunnel oxide sample, and higher performance can be achieved by optimizing the structure including GaP thickness and GaP growth conditions. The structures with a-Si or SiC layers were investigated, and the challenge is how to make more conductive GaP layers from relatively low deposition temperatures by MBE.

Chapter 7

GAP/WET-OXIDE AS A PASSIVATION CONTACT

7.1 Symmetric GaP/wet-oxide Structure

As mentioned earlier, it is difficult to realize effective passivation from GaP directly grown on silicon. As a result, it shows low minority carrier lifetime and low implied open circuit voltage (iV_{oc}), which indicates that there are high interface traps or defects at the GaP/Si interface. It has been demonstrated [66] that more than 700 mV implied open-circuit voltages can be achieved by the tunnel oxide passivated contact, which an ultra-thin tunnel oxide (wet-oxide) and a 20 nm phosphorus-doped a-Si layer were deposited on the both sides, followed by annealing at 800 ~ 900°C. In Chapter 6, the structure of a-Si/wet-oxide/c-Si/wet-oxide/a-Si were formed and annealed in tube-furnace at 850°C in the nitrogen atmosphere and it shows good passivation that 1.8 ms minority-carrier lifetime was obtained.

Inspired by this structure, instead of depositing a-Si, in this work, GaP was symmetrically deposited on wet-oxide layers by MBE as the schematic in Figure 7-1. The wafers used in this work are ~270 μm double-side polished FZ Si substrates including n-type, p-type and high resistance wafers. The ultra-thin (1~2 nm) wet-oxide was chemically grown in the nitric acid at ~100°C for 10 min. 50 nm GaP with n-type doping ((n)GaP), heavy n-type doping ((n+)GaP) or unintentionally doping ((UID)GaP) was deposited at 440°C via molecular beam epitaxy (MBE) on both sides of the silicon wafers coated by wet-oxide, forming a symmetrical GaP/wet-oxide/c-Si/wet-oxide/GaP structure. After the GaP deposition, samples were coated by 200 nm SiO_2 via PECVD to protect the GaP layers from decomposed at high T (>800°C). These structures were in tube-furnace at 850°C or

950°C in the nitrogen atmosphere. The samples were dipping in BOE for 1 min to remove the oxide on the surfaces after annealing. The effective minority-carrier lifetime and implied V_{oc} were achieved from a Sinton Tester.

A significant improvement in passivation effect was observed after thermal treatment in the tube furnace. The passivation effect from different doping levels and varied growth rates of GaP were investigated, as listed in Table 7-1. To characterize the passivation, the effective minority-carrier lifetime and implied V_{oc} were listed for every sample. The n-type dopant in GaP layers was Si. In the MBE chamber, by increasing the P flux exposure time on the silicon surface before GaP deposition, the passivation improves, and it suggests that P from GaP layers or interface may play a critical role in this passivation impact. Furthermore, increasing annealing temperature (850°C to 950°C) can also boost the minority-carrier lifetime. Promising results that 650 mV implied V_{oc} was achieved from this structure with a p-Si substrate. Further experiments revealed that the passivation effect is not related to the doping (*i.e.* Si) in the GaP layers and the structure with GaP directly on Si (*i.e.* no SiO_2 at GaP and Si interface) didn't show passivation (effective lifetime < 10 μs) after the same annealing process. The passivation mechanism is likely coming from the wet-oxide passivating the Si surface and P diffusing into tunnel oxide interface enhances the passivation.

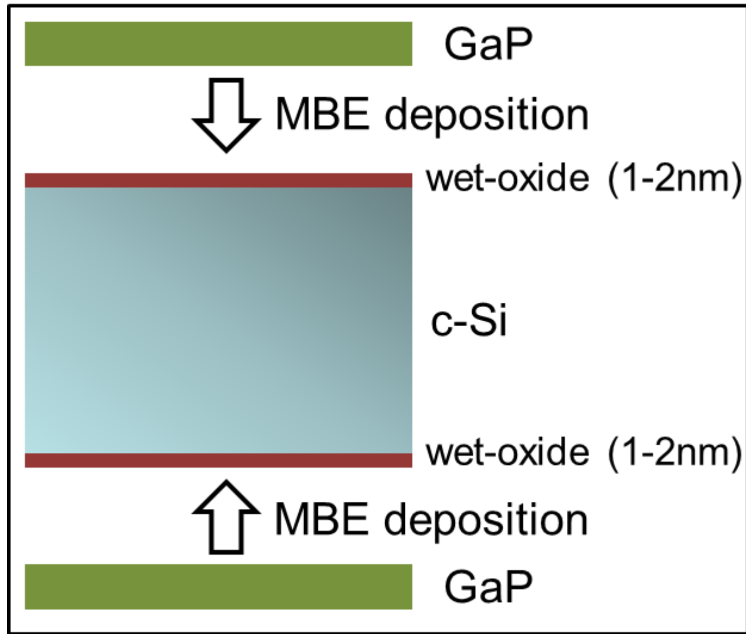

Figure 7-1 Schematic symmetrical GaP/wet-oxide/c-Si/wet-oxide/GaP structure.

Table 7-1 Lifetime & iV_{oc} for different Si substrates (high resistivity, n-type and p-type) with varied anneal conditions.

	Description	850°C1hr	950°C1hr
Sample 1	High resistivity Si, (n)GaP	227µs/619mV	N/A
Sample 2	High resistivity Si, (n+)GaP	219µs/615mV	N/A
Sample 3	n-Si, (n+)GaP	34µs/583mV	44us/584mV
Sample 4	p-Si, (n+)GaP	117µs/641mV	179us/650mV
Sample 5	n-Si, (UID)GaP	126µs/622mV	N/A
Sample 6	n-Si, (n+)GaP, fast deposition	130µs/622mV	N/A

7.2 GaP/wet-oxide for Solar Cell Applications

In this section, GaP/Si solar cells with GaP/wet-oxide as a passivation contact were demonstrated. A GaP layer with Si doped was deposited on a thin wet-oxide layer coated n-type FZ silicon wafer. The minority carrier lifetime shows less than 10 μs before annealing. The GaP was covered with 200 nm SiO_2 by PECVD and this wafer was cleaved into two pieces (G15-156-1 and G15-156-2). The two samples were annealed in the furnace at 850°C for 20 min and 1 hr, respectively. After annealing, the samples were cleaned in the buffered oxide etch (BOE) and fabricated as Figure 7-2a by depositing the a-Si and sputtering ITO and Ag.

The lifetime and implied V_{oc} of these two samples are following, G15-156-1: 46 μs / 593 mV (850°C 20 min); G15-156-2: 52 μs / 600 mV (850°C 1 hr). The EQE and IQE curves are shown in Figure 7-2b and more than 90% quantum efficiency is observed at the wavelength of ~600 nm to ~900 nm. The one hour annealed sample has a better PV response than the 20 minutes annealed sample at ~ 800 nm to 1100 nm wavelength, and it suggests that the GaP/Si interface is better in one hour annealed sample. Figure 7-3 is plotting the pseudo light IV and illuminated IV of sample G15-156-1 and G15-156-2. About a 600 mV open-circuit voltage was achieved, which indicates that GaP/wet-oxide layers are functional as a passivation layer for this structure. However, “S” shape was observed in the IV curve, which is leading to low FF. It is clear that the device performance is highly affected by the annealing conditions. Therefore, by further optimizing the annealing conditions for GaP/wet-oxide, a higher performance could be achieved.

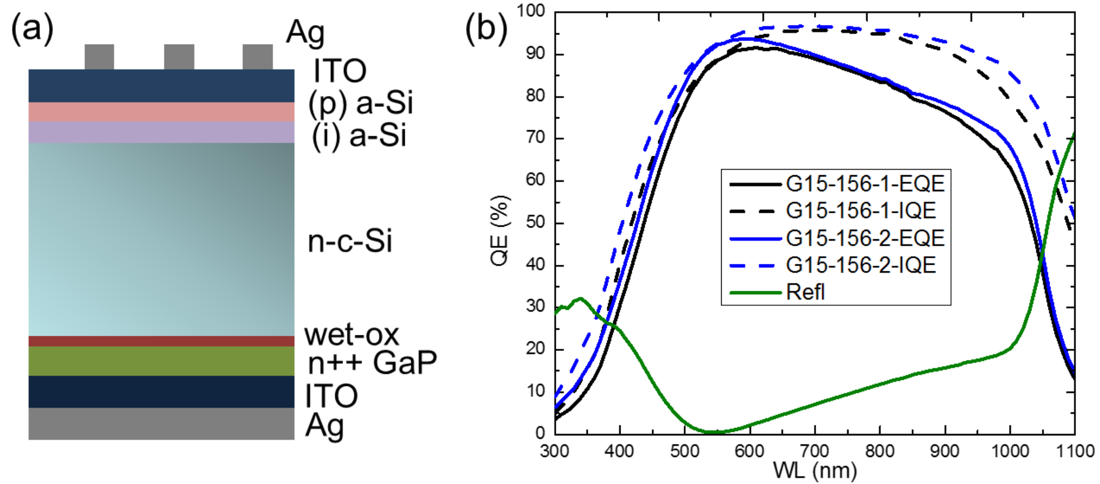

Figure 7-2 (a) Device structure with GaP/wet-oxide passivation; (b) Quantum efficiency spectrum (blue and black) of two device samples and surface reflection (green).

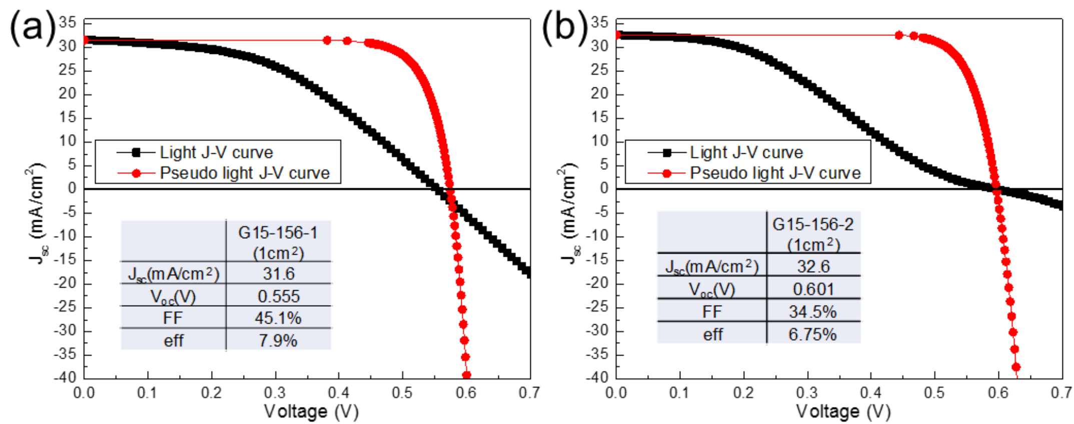

Figure 7-3 The pseudo light IV curve and illuminated IV curve of samples (a) 850°C20min (G15-156-1) and (b) 850°C1hr (G15-156-2). The inset shows the performance of the devices.

7.3 Summary

In this chapter, a symmetric GaP/wet-oxide stack was demonstrated as passivation layers for Si after thermal annealing and various annealing conditions were investigated. 650 mV and 622 mV implied open-circuit voltage was achieved for p-Si substrates and n-Si substrates, respectively. Further, GaP/Si heterojunctions solar cells with GaP/wet-oxide

as a passivation layer were demonstrated. The device (G15-156-2) has ~600 mV open-circuit voltage and it shows GaP/wet-oxide was acting at least partially as a passivation contact. The performance can be further improved by optimizing the annealing conditions and layers thickness of the GaP/wet-oxide layers.

Chapter 8

CONCLUSION AND FUTURE WORK

8.1 Conclusion

In this work, the main purpose was to develop high performance of GaP/Si heterojunction solar cells. Two main challenges were addressed including high quality GaP growth by MBE and the Si minority-carrier degradation issue during GaP growth on Si in the MBE chamber.

First, a defect-free GaP growth was achieved by optimizing the migration enhanced epitaxy (MEE) growth conditions on the 4° off-cut Si substrates. In order to obtain high quality of GaP layers on precisely oriented (001) Si substrates, growth conditions by traditional MBE growth with a growth rate of ~0.5 μm/hr were optimized, such as the P/Ga ratios. Structural defect formation was investigated for the GaP/Si structures by HR-XRD and TEM imaging.

After demonstrating high quality of GaP layers growth on Si, significant degradation of the minority carrier lifetime in the Si bulk was observed. A dramatic lifetime degradation in Si bulk was observed during thermal treatment (≥500°C, up to 850°C) in the MBE chamber. The bulk lifetime degradation of Si in GaP/Si epitaxial structures occurs primarily from the initial high-T thermal de-oxidation process. More study indicates that the fast diffusors that kill the lifetime are from the back side of the wafers during the high temperature thermal treatment. Testing of Si wafers with/without SiN_x layers revealed that high Si bulk lifetimes (>1 ms) are maintained if SiN_x is applied during the high-T treatment in the MBE chamber, which suggests that SiN_x is acting as a diffusion barrier and/or gettering agent during the thermal treatment.

Following GaP/Si integration, sufficiently high Si bulk lifetimes ($\geq$ 1.83 ms) for Si(001) substrates coated by a SiN_x barrier layer were been confirmed. In addition, high crystal quality of the GaP was established by *in-situ* RHEED patterns and *ex-situ* XRD analysis. This indicates that the SiN_x barrier layer deposited on Si back side do not affect the epitaxial growth or degrade the quality of the epi-layers on the front, and millisecond Si bulk lifetimes in the III-V/Si structures are maintained. Other than the SiN_x diffusion barrier, P-diffusion layers were demonstrated to be another effective approach to suppress the lifetime degradation during thermal treatment in the MBE chamber. Both approaches can be widely used for maintaining the silicon lifetime for III-V integration on Si in MBE chambers, such as silicon based multijunction solar cells.

To investigate GaP/Si heterojunction solar cells, firstly, GaP as a heteroemitter layer was form on p-type Si wafers. A boost at the short wavelength (400 nm to 700 nm) compared to a-Si based HIT cells in the quantum efficiency was observed. However, the poor GaP surface passivation and defects in the GaP/Si interface lead to a low open circuit voltage. A low fill factor was further observed due to the lack of contact optimizations and defects in the GaP. It is crucial to have high quality of GaP and optimize the solar cell structure to further increase the power conversion efficiency of GaP/Si structures.

Further, different GaP/Si heterojunction structures with GaP as a back electron-selective contact were fabricated with different lifetime protection methods, including avoiding high-T thermal treatment, n^+ layers and SiN_x layer protection layers. The device with an n^+ layer protection appears to have the best performances among the three methods. By inserting an n^+ layer at the GaP/Si interface, the device performance was further improved and a 618 mV open-circuit voltage and 13.1% efficiency were achieved.

Additionally, with MoO_x as a hole selective carrier contact to replace a-Si layers, the energy conversion was boosted to 14.1%.

Since GaP layer is still far from perfect as a passivation layer for silicon, inserting a passivation layer between the GaP and the silicon is critical to approach high performance solar cells with an electron-selective contact (*i.e.* GaP). Amorphous-Si and a-SiC could provide excellent passivation for Si, however, the contact issue due to the low doping level in GaP limits the a-Si/a-SiC capacity in this application. On the other hand, tunneling oxide passivation is promising. GaP was deposited with good electrical properties on the annealed tunneling oxide, and a 685mV V_{oc} was obtained with more than 32 mA/cm^2 J_{sc} estimated from the EQE.

Further, the GaP/wet-oxide/c-Si/wet-oxide/GaP structure shows significant improvement in passivation after annealing at a temperature of 800°C to 900°C in the furnace. The implied V_{oc} was as high as 651 mV from this structure, and the passivation impact is likely from the thin wet-oxide and P diffusing into the wet-oxide during the high temperature annealing. However, the exact passivation mechanism is under investigation. With a GaP/wet-oxide passivation layer, the solar device shows a more than 600 mV open-circuit voltage. Therefore, the GaP/wet-oxide passivation layer for Si solar cells is promising, but the annealing time and temperature still require optimization for boosting the performance.

8.2 Future Work

The record efficiency of Si solar cells has reached 26%, and how to further boost the efficiency is still an interesting topic for researchers. As discussed in Chapter 6, after GaP deposited on Al_2O_3 coated Si substrates, the minority-carrier lifetime of the structures

was increased up to 3.2 ms. This promising result can be designed to be the schematic structure shown in Figure 8-1, in which the stack layer of GaP/Al_2O_3 is designed to be the passivation layer on the front, and replaces the commonly used a-Si passivation layers. Both GaP and Al_2O_3 have a higher bandgap than a-Si, and as a result, the absorption loss on the front surface can be reduced.

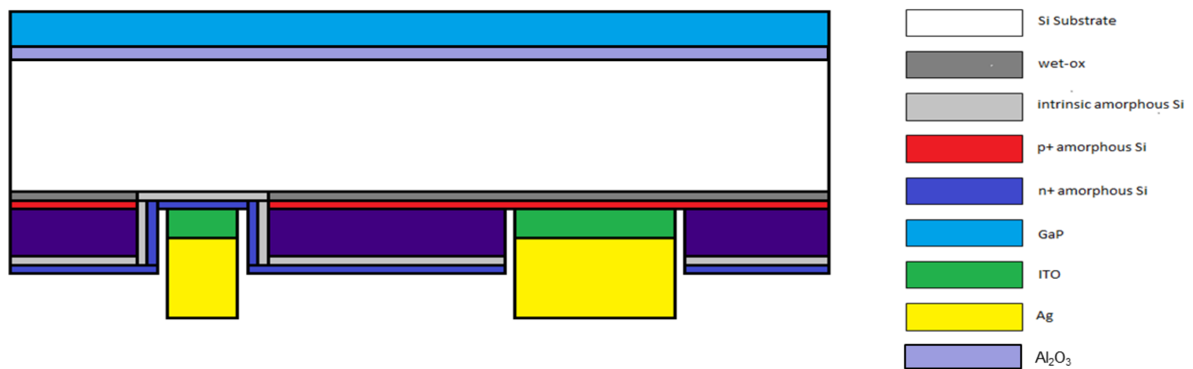

Figure 8-1 The schematic of interdigitated back-contact (IBC) heterojunction Si solar cells with GaP/Al_2O_3 integrated on the surface.

In this work, GaP/Si heterojunction solar cells have been demonstrated, and there are more approaches to potentially improve the performance, such as introducing nanostructures on the surface. Nanostructures improve the performance via the light trapping effect, and III-V nanostructures have been fabricated by different methods as reported in [70]–[78]. Defect-free III-V nanostructures can be achieved from metal assisted chemical etching (MACE), and it has been demonstrated in GaAs nanopillar arrays in [78]. Some preliminary results have been reported in [77] for nanostructures in the GaP/Si material system. The nanostructure is fabricated by patterning with a noble metal film or metal particle such as Ag, Au or Pt in a mixed solution (HF:H_2O_2:H_2O) in the MACE process. Figure 8-2 shows the GaP nanopillar structures after silica nanospheres

lithography (SNL) and MACE. The performance of GaP/Si can be boosted by the light trapping from the surface nanostructures.

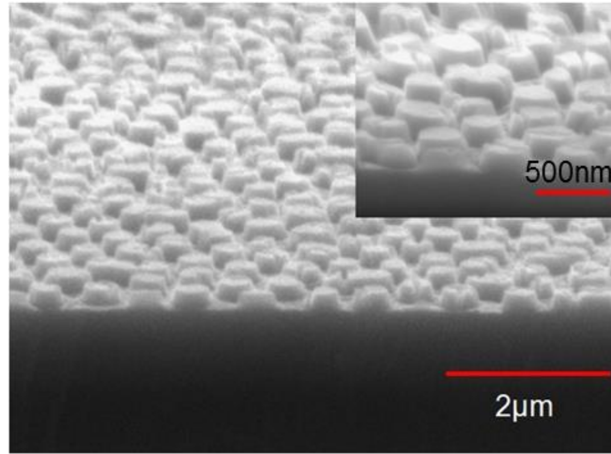

Figure 8-2 SEM image of GaP nanopillar structures fabricated by MACE. [77]

Further, the GaP/Si structure can be one important portion for Si-based tandem or multijunction solar cells [16], [79]–[81]. The high quality GaP layer grown on the Si surface enables high quality of III-V materials growth, such as GaPN growth. Dilute nitride materials such as GaPN can be grown lattice matched to Si substrates, and allow high dislocation density at the III-V/Si interface. Figure 8-3 shows a 3-terminal monolithically integrated Si tandem solar cell, from which the 35% or higher efficiency is achievable. In this structure, the GaP layer inserted in GaNP and Si is functional as a back surface filed (BSF) layer for dilute nitride solar cell and a carrier-selective contact for Si.

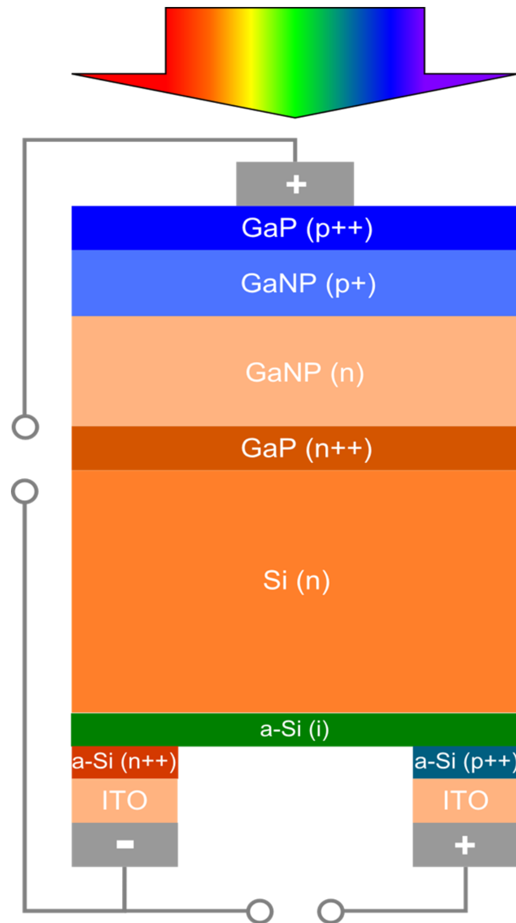

Figure 8-3 The schematic of 3-terminal monolithically integrated Si tandem solar cells.

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