High Slew-Rate Adaptive Biasing Hybrid Envelope Tracking Supply Modulator for LTE Applications

by

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ABSTRACT

As wireless communication enters smartphone era, more complicated communication technologies are being used to transmit higher data rate. Power amplifier (PA) has to work in back-off region, while this inevitably reduces battery life for cellphones. Various techniques have been reported to increase PA efficiency, such as envelope elimination and restoration (EER) and envelope tracking (ET). However, state of the art ET supply modulators failed to address high efficiency, high slew rate, and accurate tracking concurrently.

In this dissertation, a linear-switch mode hybrid ET supply modulator utilizing adaptive biasing and gain enhanced current mirror operational transconductance amplifier (OTA) with class-AB output stage in parallel with a switching regulator is presented. In comparison to a conventional OTA design with similar quiescent current consumption, proposed approach improves positive and negative slew rate from 50 V/μs to 93.4 V/μs and -87 V/μs to -152.5 V/μs respectively, dc gain from 45 dB to 67 dB while consuming same amount of quiescent current. The proposed hybrid supply modulator achieves 83% peak efficiency, power added efficiency (PAE) of 42.3% at 26.2 dBm for a 10 MHz 7.24 dB peak-to-average power ratio (PAPR) LTE signal and improves PAE by 8% at 6 dB back off from 26.2 dBm power amplifier (PA) output power with respect to fixed supply. With a 10 MHz 7.24 dB PAPR QPSK LTE signal the ET PA system achieves adjacent channel leakage ratio (ACLR) of -37.7 dBc and error vector magnitude (EVM) of 4.5% at 26.2 dBm PA output power, while with a 10 MHz 8.15 dB PAPR 64QAM LTE signal the ET PA system achieves ACLR of -35.6 dBc and EVM of 6% at 26 dBm PA output power

without digital pre-distortion (DPD). The proposed supply modulator core circuit occupies 1.1 mm^2 die area, and is fabricated in a 0.18 μm CMOS technology.

To My Parents and Family

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CHAPTER 1

INTRODUCTION

1.1 Research Background

1.1.1 Wireless Communication

In dictionary, the first explanation of Communication is “the imparting or exchanging of information or news”. People has been seeking methods of long distance wireless communication for more than two thousand years. In China, ancient emperors employed beacons to convey the message of an invasion from the border to the capital. Fig. 1.1 presents a segment of the Great Wall with several beacons on it. When soldiers detected any invasion, they would light up the firewood and sent the signal by smoke. When Soldiers on the next following beacon saw the smoke from the previous beacon, they would light up their firewood and sent the signal to the next one. The message of the enemy invasion passed by beacons one by one and finally arrived at the capital. This is the first kind of long distance wireless communication in human history.

In 1865, James Clerk Maxwell published the famous Maxwell’s equations which built the foundation of the Classical Electromagnetism [1]. In 1948, Claude Elwood Shannon proposed the Information Theory in his distinguished paper which entitled “A Mathematical Theory of Communication” [2]. With these theories and the development of semiconductor industry, the dream of the convenient wireless communication finally came true.

Fig. 1.1 The great wall with beacons

Motorola produced the first handheld mobile phone in 1973 [3]. A bulky heavy handheld box which can only talk for 30 minutes but took almost half a day to recharge. Fig. 1.2 illustrates Martin Cooper photographed in 2003 with his 1973 handheld mobile phone prototype [10]. Six years later, in 1979, the first commercial cellular network was launched in Japan by Nippon Telegraph and Telephone (NTT) [3]. It was considered as the first generation (1G) network in later days and used the analog telecommunications standards. Although the 1G mobile phone was pricy and bulky, but the demand was very strong. which led the revolution of modern communication.

In 1990s, two digital communication standards, GSM and CDMA, replaced the 1G analog network which was known as the second generation (2G) mobile phone system [3]. With the development of the battery technology, higher efficiency of the electronics and the increasing deployment of the base stations, the cell phones were no longer pricy and

bulky. Instead, they were only few hundred grams in weight and could be held in one hand easily. Comparing to the 1G network, the 2G mobile systems enhanced communications by introducing more ways to communicate, such as text messaging, and the initial multimedia access through the mobile networks.

Fig. 1.2 Martin Cooper photographed in 2003 with his 1973 handheld mobile phone prototype [10]

While the 2G cell phone swept the world, the demands for more data and faster data transmission speeds were growing. It soon became the driving force for the new multimedia era in customers' hands. The third generation (3G) technology was born, and first commercialized in Japan in 2001 by NTT DoCoMo using the WCDMA technology [3]. The enhanced speed of 3G network can let people download or stream content on the phone. Among all the competing 3G technologies, WCDMA standard occupied two third

of the global market which made it the biggest winner in the 3G era. As more and more users joined the 3G network and more data required from the applications, 3G network was no longer capable to satisfy all the demands. Then the industry began to develop the fourth generation (4G) technology. Fig. 1.3 presents Steve Jobs introduced the first iPhone to the world on Jan 9, 2007. With its powerful multimedia and computing abilities, iPhone reshaped the landscape of mobile phone industry [10].

Fig. 1.3 Steve Jobs introduced the first iPhone to the world on Jan 9, 2007 [10]

Long-Term Evolution (LTE) is one of the 4G high speed wireless communication technologies which developed by 3rd Generation Partnership Project (3GPP) [4]. It evolved from GSM and UMTS technologies and based on Orthogonal Frequency Division Multiple Access. Higher order modulation (up to 64-QAM), larger bandwidth (up to 20MHz) and downlink multiplexing are adopted to achieve faster date rate. The peak downlink rate is

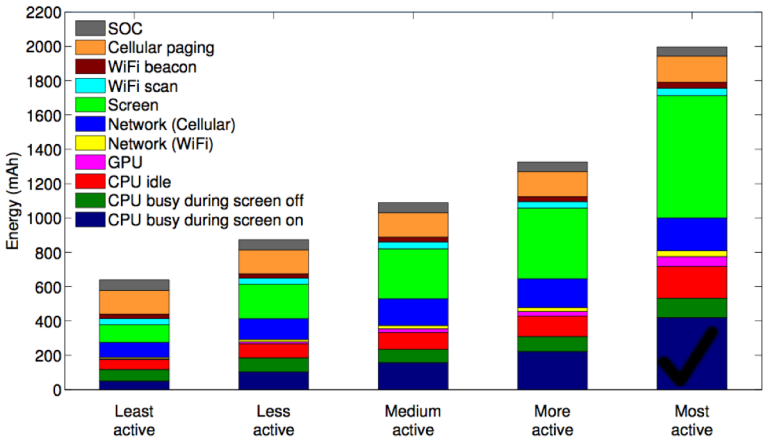
300Mbps (with 4x4 antennas and 20MHz bandwidth) and the peak uplink rate is 75Mbps [5].

1.1.2 LTE Application Market

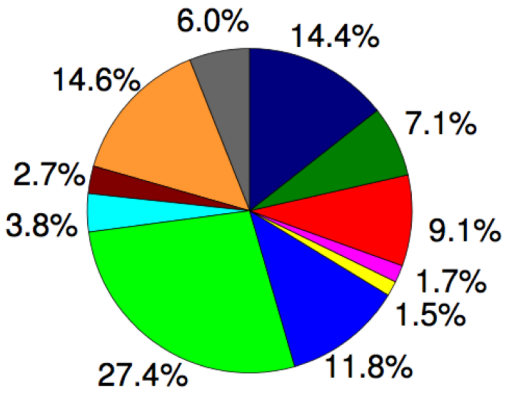
The blossom of the social networks boosts the LTE market. In 2012, there were 68 million global LTE subscriptions. This number almost doubled in 2013 to 134 million global LTE subscriptions. The forecast shows that by 2018, the global LTE subscriptions will surpass 1 billion [6]. With the enormous number of the subscriptions, the LTE global market grows at tremendous growth rate. In 2012, the entire LTE market revenues were valued at US $10.47 billion. However, in 2016 the revenues already increased to US $344.8 billion. And it will continue growing exponentially to US $610.71 billion globally in 2019 [7]. From 2012 to 2019, the compound annual growth rate of the LTE global revenues is 78.6% annually. In future, LTE market will keep increasing and the revenues will be US $926.1 billion by 2024 [8].

1.1.3 Research Motivation

As the cell phone evolved from 1G cellphone to 4G LTE smartphone, its power consumption is inevitably increased. However, the modern battery technology could not follow the rapid development of the cellphone, it became a limiting technology to modern wireless communication system. A survey in May 2014 by research company GMI revealed that 89% of 1000 Britons rated long battery life was more attractive than all the other features when buying a new smartphone [9].



(a)



(b)

Fig. 1.4 (a) The average daily energy drain breakdown within 5 groups of 1520 users. (b) Daily energy percentage breakdown, averaged over all users. [11]

Numerous researchers started to focus on improving the efficiency to prolong the battery life. Fig. 1.4 (a) and (b) illustrates the average daily energy drain breakdown within 5 groups of 1520 users [11]. The combined cellular related power consumption is 26.4%, which is the second largest source of battery usage and only 1% lower than the screen power consumption which is 27.4%. Fig. 1.5 depicts how the advanced communication systems increase the power amplifier (PA) energy consumption [12]. With the increasing waveform complexity and the higher peak to average power ratio (PAPR) from GSM to

4G LTE, the PA power consumption increased a few times. For example, the 4G LTE QPSK signal with 5.4dB PAPR increased the PA power consumption more than two times than that of GSM; the LTE-A 40MHz/200RB signal with 8.7dB could even increase the PA power consumption to almost four times than that of GSM. To reduce the cellphone power consumption and to improve the efficiency, Envelope Tracking (ET) technique has been developed which can dramatically increase the efficiency of the PA in back off region.

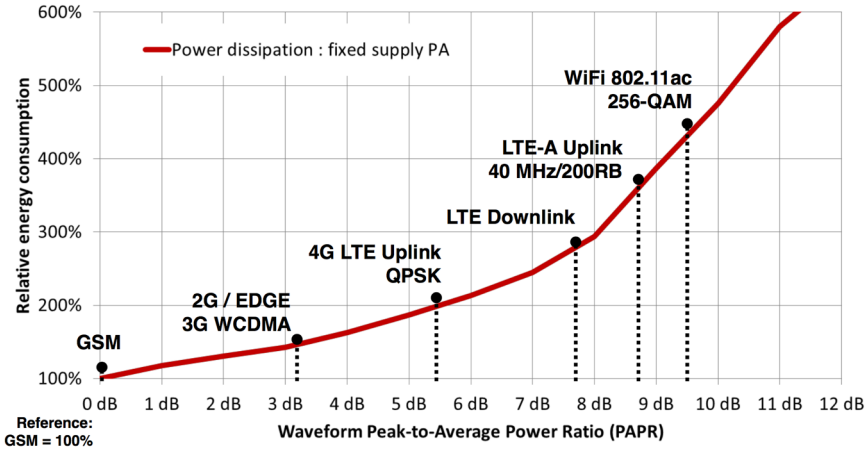


Fig. 1.5 Increasing waveform complexity is pushing up the PA energy consumption [12]

1.2 Dissertation Outline

The organization of this dissertation is as follows: Chapter 1 provides a brief introduction of the research background and the motivation. In the meantime, it explains the existing large PA power consumption issues. Chapter 2 reviews prior PA supply modulator approaches. The advantage and disadvantage of prior approaches are discussed. Chapter 3 presents a hybrid ET supply modulator. The details of the proposed high slew rate and adaptive biasing features are described. Chapter 4 demonstrates the measurement

results of the hybrid ET supply modulator. Chapter 5 illustrates a summary and a discussion of possible future work.

CHAPTER 2

STATE OF THE ART POWER AMPLIFIER SUPPLY MODULATOR DESIGN AND DESIGN CONSIDERATIONS

2.1 Envelope Tracking and Envelope Elimination and Restoration

Modern mobile communication systems employ Orthogonal frequency-division multiplexing (OFDM) to achieve high date rates within a limited bandwidth. The signals, which are modulated by the highly spectral efficient modulation schemes such as Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM), have characteristics as dynamic envelope and large PAPR. To satisfy the stringent linearity and the PAPR requirements demanded by state of the art communication systems, the RF PA is required to operate in the back-off region, which dramatically reduces the efficiency of the RF PA. Various techniques to improve the efficiency and extending the battery life of a transmitter have been investigated. One of the techniques to enhance efficiency involves controlling the power supply of the RF PA with the modulated signal's envelope power. Two commonly used techniques to achieve this are envelope elimination and restoration (EER) [13] and ET. Fig. 2.1 depicts a simplified Kahn EER transmitter block diagram. EER technique amplifies amplitude and phase signals through two separate paths and a switch mode PA (Class D/E mode) is used to transmit the phase signal. However, ET technique requires a linear PA to amplify both amplitude and phase signals together, while modulating the PA supply level to improve class AB efficiency. Theoretically EER has better efficiency due to its use of high efficiency switch-mode PA. However, it demands a wider bandwidth supply modulator in comparison to ET, to meet RF linearity requirements.

This requirement limits EER technique to narrow-band applications. Due to this reason, ET technique is a better choice for wideband LTE applications [14][19].

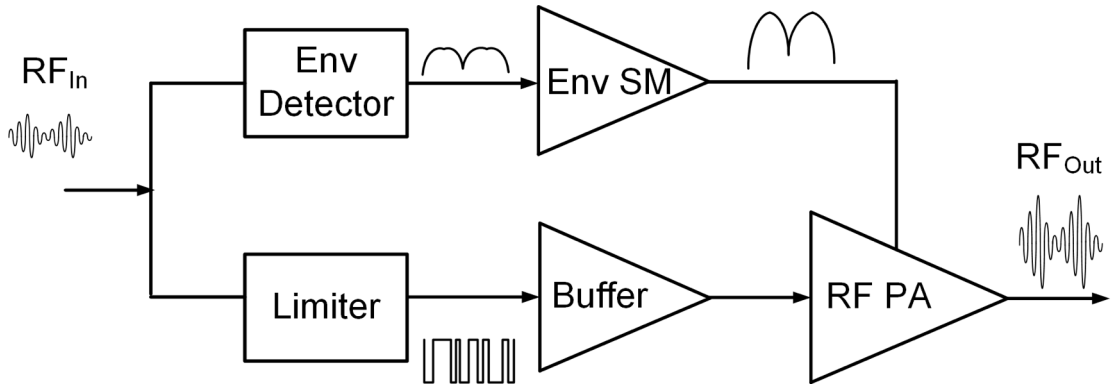


Fig. 2.1 Simplified block diagram of Kahn EER transmitter

2.2 State of the Art Power Amplifier Supply Modulator Topologies

Fig. 2.2 (a) and (b) show a simplified block diagram of an ET PA system and its waveform respectively. In an ET PA system, the drain of the PA is connected to the output of a high efficiency supply modulator which tracks the envelope of the RF signal. The power consumption of the PA is proportional to the power supply voltage, therefore with a high efficiency ET supply modulator, the PA consumes less power in comparison to a conventional PA. Although the ET supply modulator itself needs to consume some power to operate, the overall efficiency is still improved considerably due to the high current levels at the transmitter output. Linear low-dropout regulators (LDOs) have been employed to implement supply modulator for PAs. They can achieve good linearity and bandwidth, but the efficiency is limited by the voltage drop on the power transistor. In [14], LDOs are used as a class G supply modulator to smoothing class G response. On the other hand, switching amplifiers provide high efficiency at all power levels, but their bandwidth is too

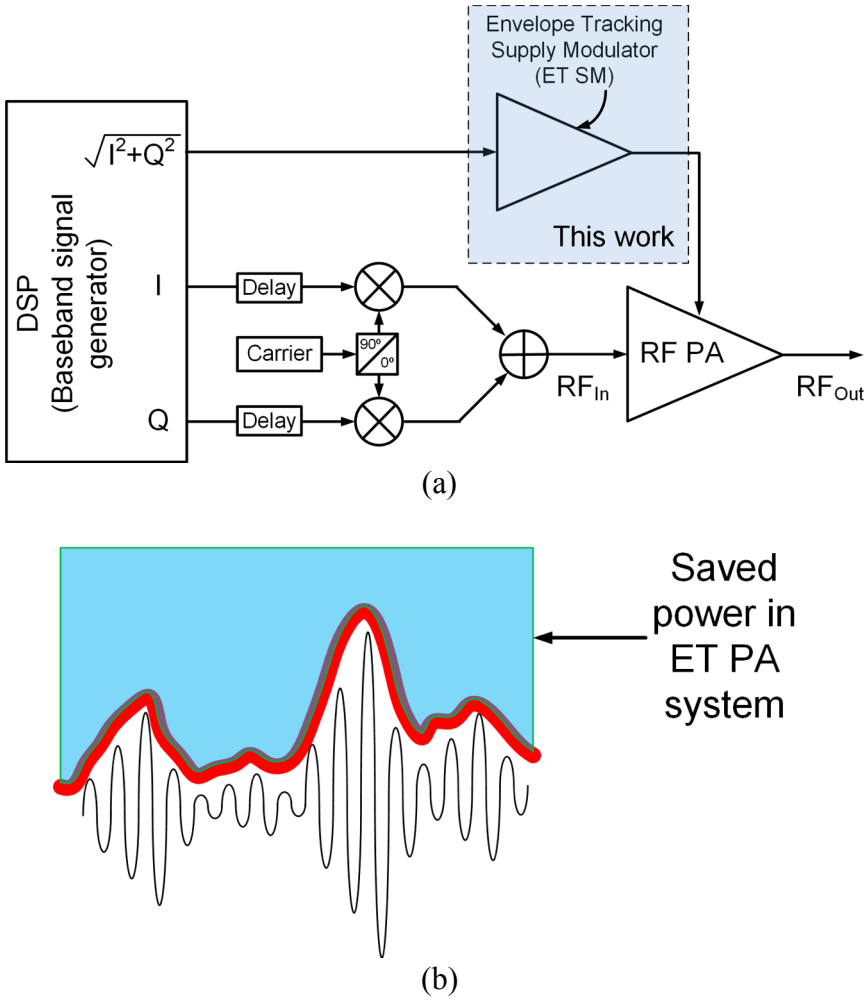


Fig. 2.2 (a) Simplified block diagram of ET PA system. (b) ET PA waveform

narrow for advanced 4G communication systems [15][16]. Recently reported switching amplifiers utilize multiphase and slew rate enhancement to achieve a medium bandwidth [17]. However, several design issues including equal current sharing among different stages and increased switching losses need to be addressed. In switching amplifiers, the output noise is much higher than that of linear amplifier which results in a relatively poor linearity for the PAs. Hybrid supply modulators, which combine linear and switching amplifier in a master-slave configuration, can achieve wide bandwidth, high linearity and

high efficiency simultaneously [18]-[35]. Various methods have been published to enhance the ET PA systems' efficiency and linearity. In [18], a switching amplifier operating in two phases to reduce current ripple and power loss is proposed. A transistor-resizing technique for the PA to increase its efficiency is described in [24]. In [22] a two level linear amplifier supply is presented, a low bandwidth dynamic linear amplifier supply is explained in [26], and a multi-level linear amplifier supply is illustrated in [30]. An envelope shaping function to reduce nonlinear characteristics in the low supply voltage region is introduced in [20].

2.3 Supply Modulator Design Considerations

In a hybrid ET supply modulator, the linear amplifier should have sufficient low-frequency gain, wide bandwidth and high slew rate as well as large drive capability to effectively track the large PAPR envelope signal, maintain a good linearity, and drive the low equivalent PA resistance. Previously, folded cascode amplifier followed by a class AB buffer was a popular choice for implementing the linear amplifier [19][21][23][24][29][30]. The use of a rail to rail input cascode amplifier followed by a class AB buffer is also reported in [25][35]. Although they achieve high dc gain through cascode devices, their slew rate is limited by the constant input biasing current. In [26] a source cross-coupled differential amplifier followed by a class AB buffer is introduced. Unlike their cascode counterparts, this topology achieves high slew rate due to its class AB input stage operation. However, the dc gain of this linear amplifier is insufficient to meet the accuracy requirements when driving a low PA equivalent load resistance. Most previously reported ET supply modulators failed to provide sufficient dc gain and slew rate simultaneously.

In this dissertation, an ET hybrid supply modulator utilizing a linear amplifier, which employs signal level tracking adaptive biasing and gain enhanced current mirror operational transconductance amplifier (OTA), in parallel with a buck switching amplifier is presented. The proposed topology can achieve high low-frequency gain, wide bandwidth, and high slew rate concurrently.

CHAPTER 3

PROPOSED HIGH SLEW-RATE ADAPTIVE BIASING HYBRID ENVELOPE TRACKING SUPPLY MODULATOR DESIGN

3.1 ET Hybrid Supply Modulator Architecture

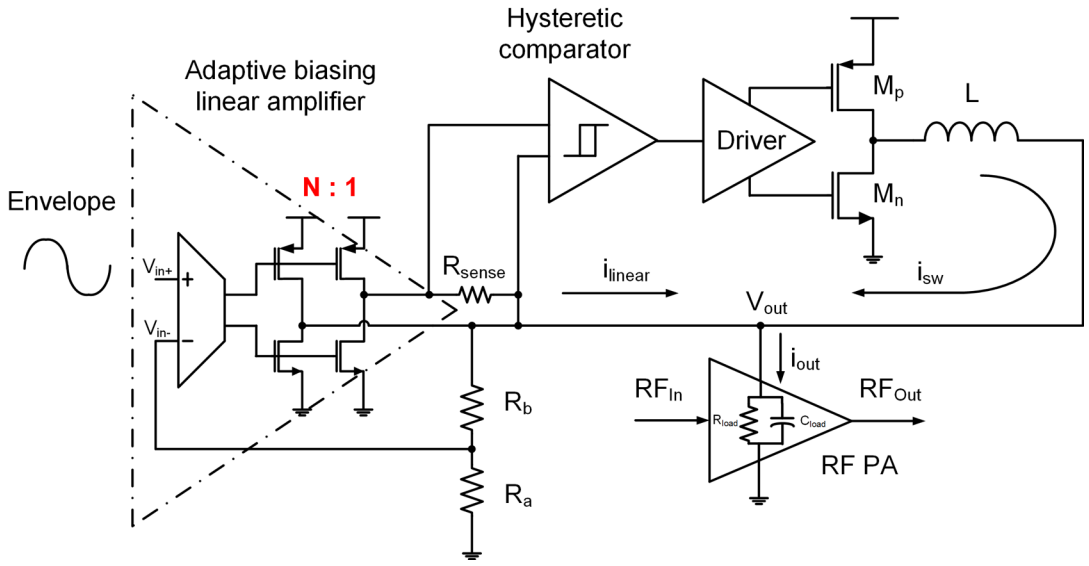


Fig. 3.1 Architecture of the proposed ET Hybrid Supply Modulator

Fig. 3.1 shows the architecture of the proposed ET hybrid supply modulator. The adaptive biasing linear amplifier works as a voltage controlled voltage source, ensuring V_{out} closely tracks the input envelope. The switching amplifier, which is controlled by the output current of the linear amplifier, works as a current-controlled current source, providing the dc and low frequency current to the PA with high efficiency. The off-chip inductor, the equivalent capacitance, and resistance of the PA form a second order low pass filter, filtering out the switching ripple. The switching amplifier current still contains considerable amount of current ripple. The linear amplifier not only provides high

frequency current to the PA but also cancels the current ripple and its harmonics from the switching amplifier. Fig. 3.2 illustrates the simulated current frequency responses of the switching amplifier and the linear amplifier with 10 MHz LTE signal. Which proves the above analysis. The frequency response of the outputs of the switching amplifier, the linear amplifier, and the combined hybrid supply modulator can be expressed as $i_{sw}(s)$, $i_{linear}(s)$, and $i_{out}(s)$ respectively. The open loop transfer function H(s) between $i_{linear}(s)$ and $i_{sw}(s)$ can be found by (3-1) after cutting off the current branch from linear amplifier to PA drain.

$$i_{linear}(s) \cdot A(s) = i_{sw}(s) \cdot \left(sL + R_{load} \parallel \frac{1}{s \cdot C_{load}}\right) \tag{3-1}$$

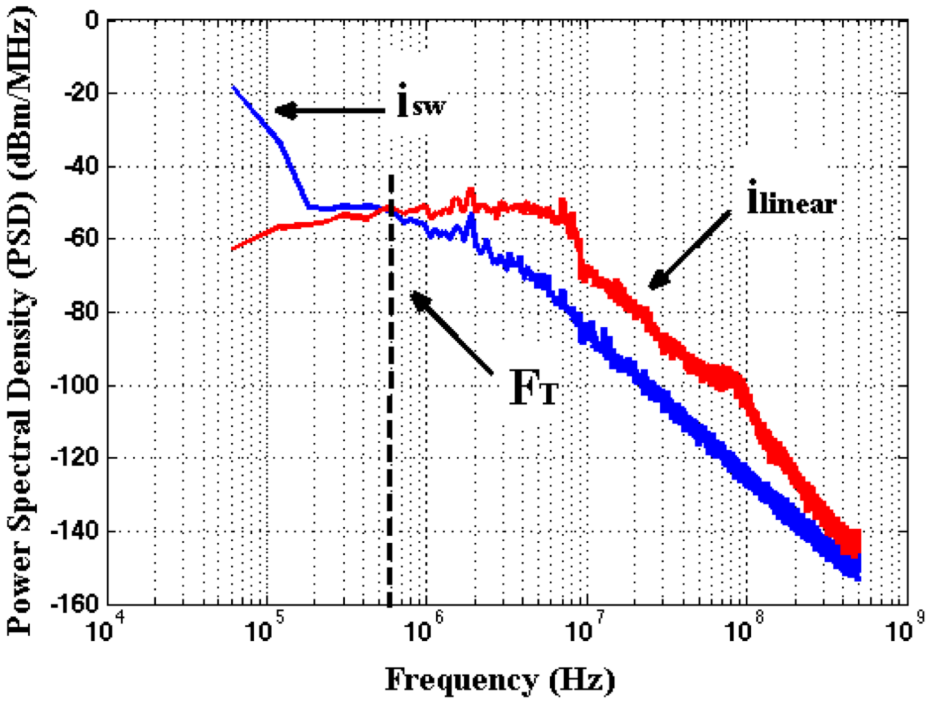


Fig. 3.2 Current frequency responses of the switching amplifier and the linear amplifier with 10 MHz LTE signal

Where $A(s)$ is the transfer function from $i_{linear}(s)$ current to the input average voltage of the inductor, R_{load} is the PA drain equivalent resistance, C_{load} is the PA drain equivalent capacitance, and L is the off-chip inductance. $H(s)$ is given by:

$$H(s) = \frac{i_{sw}(s)}{i_{linear}(s)} = \frac{A(s)\cdot(s\cdot R_{load}\cdot C_{load}+1)}{R_{load}\cdot\left(s^2\cdot L\cdot C_{load}+s\cdot\frac{L}{R_{load}}+1\right)} \tag{3-2}$$

From (3-2), it can be shown that $H(s)$ has a low pass response. Since $i_{out}(s) = i_{linear}(s) + i_{sw}(s)$, the closed loop transfer function of $i_{linear}(s)$ and $i_{sw}(s)$ to $i_{out}(s)$ can be represented as:

$$i_{linear}(s) = \frac{1}{1+H(s)} i_{out}(s) \tag{3-3}$$

$$i_{sw}(s) = \frac{H(s)}{1+H(s)} i_{out}(s) \tag{3-4}$$

As shown in (3-3) and (3-4), the switching amplifier current has a low pass characteristic while the linear amplifier current has a high pass characteristic. An ideal linear amplifier with infinite GBW can cancel the entire current ripple from the switching amplifier current and generate a ripple free current at the output of the hybrid supply. However, the linear amplifier has finite GBW and it can only cancel current ripple within its finite GBW while still leaving some residual ripple in the output current which limits the linearity of the hybrid supply modulator.

The transition frequency, F_T, which is defined as the frequency where the switching amplifier current and the linear amplifier current split, should be optimized based on the efficiency and the linearity. If F_T is too small, the low efficiency linear amplifier would supply more of the high frequency current to the PA load, which will degrade the overall efficiency of the supply modulator. If F_T is too large, the switching amplifier would generate higher frequency current ripple. Since the linear amplifier still has the same GBW,

the residual current ripple at the output of the supply modulator would increase, which would result in the hybrid supply modulator linearity problem [35]. The transition frequency, F_T, is directly proportional to the switching amplifier switching frequency F_{sw}. F_{sw} is shown in equation (3-5) [20].

$$F_{sw} = \frac{R_{sense}V_{out}(V_{dd}-V_{out})}{2V_{dd}NLV_H} \quad (3\text{-}5)$$

Where V_{dd}, V_{out}, V_H, R_{sense}, L, and N are the supply voltage, the output voltage of the supply modulator, the hysteresis voltage of comparator, the current sensing resistance, the inductance, and the current sensing gain, respectively. By selecting different design parameters V_H, R_{sense}, L, and N, the switching frequency can be optimized between efficiency and linearity, such that indirectly optimizes transition frequency F_T. In this work, the optimized transition frequency F_T is found to be around 600 kHz for 10 MHz LTE signal as shown in Fig. 3.2.

3.2 Envelope Shaping

Envelope shaping or envelope shifting plays an important role in improving the ET PA system's linearity. In the low power region, the ET supply modulator provides a low level modulated voltage to the PA drain. If the modulated supply voltage is smaller than the knee voltage (turn-on voltage of the power transistor in the PA), large AM-AM and AM-PM distortion will be generated due to the compression in transistors. To solve this problem, a dc shift is commonly applied to the envelope signal [20][23][28]. Another advanced envelope shaping technique, termed sweet spot tracking, shifts the dc level, but also tracks the minimum third-order intermodulation distortion (IMD3) at various power levels [21]. In the proposed approach, the envelope shaping function shown in (3-6) is

adopted. Where V_{Env}, V_{DC}, k, and V_{PA_drain}, are the input envelope voltage, the PA drain dc shift voltage, the envelope scaling factor to avoid clipping, and the modified PA drain supply voltage, respectively.

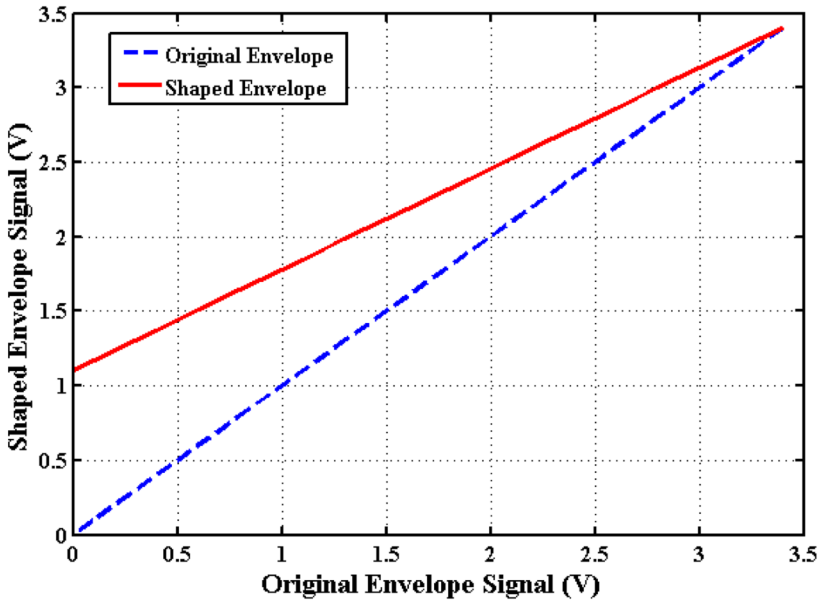


Fig. 3.3 Envelope shaping function

$$V_{PA\_drain} = k \times V_{Env} + V_{DC} \tag{3-6}$$

This approach achieves better linearity and increases the efficiency concurrently. The envelope shaping function is depicted in Fig. 3.3. A dc offset of 1.1 V is applied and the envelope signal is scaled between 1.1 V and 3.4 V.

3.3 FVF and Adaptive Biasing

To overcome the slew rate limitation in the constant input biasing linear amplifier, an adaptive biasing scheme with class AB input stage operation is implemented by the flipped voltage follower (FVF).

Fig. 3.4 (a) presents a basic FVF structure. Comparing to the PMOS version conventional voltage follower, it moves the current biasing from the top to the bottom of the transistor M_1 and adds a shunt feedback around it. This FVF can source more current to load but sinking capability is limited by the biasing current I_B. The open loop small signal analysis has been elaborated in [36]. The open loop gain can be obtained by break the loop at node Y and the value is given by (3-7). r_{olY}, shown in (3-8), is the open loop small signal impedance at node Y. Two poles in the loop are located at node X and Y, respectively. As shown in (3-9), r_{olX} is a low impedance node compared to node Y. Since the dominant pole is located at node Y, $\omega_Y < UGF < \omega_X$, in some cases compensation is required at node Y to ensure FVF loop stability [36]:

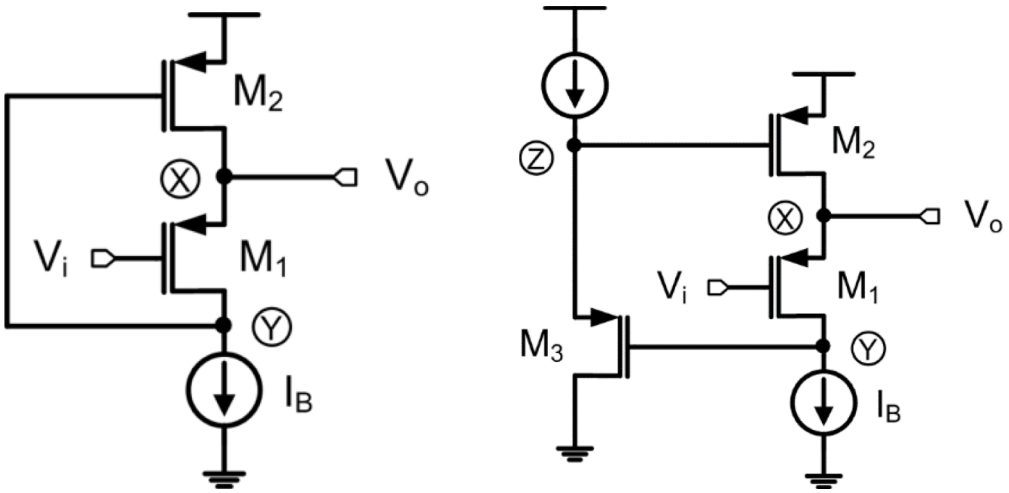


Fig. 3.4 (a) Basic FVF structure, from [36]. (b) High supply version FVF structure, after [37].

$$Av_{ol} = -gm_2 r_{olY} \tag{3-7}$$

$$r_{olY} = r_B \parallel gm_1 r_{o1} r_{o2} \approx r_B \tag{3-8}$$

$$r_{olX} = \frac{(1+r_B/r_{o1})}{gm_1} \parallel r_{o2} \approx \frac{2}{gm_1} \tag{3-9}$$

FVF is suitable for low voltage operation, since the minimum operating supply voltage for this amplifier is $VDD_{min} = V_{sg} + V_{dsat}$, and in advanced technology nodes, VDD_{min} can be lower than 1 V. However, if supply voltage is close to 3.3 V similar to our design, the common mode range of V_i would be limited by V_{sg2}. To overcome this limitation, the size of transistor M_2 should be small. Fig. 3.4 (b) shows a high supply voltage version FVF. By adding a voltage follower M_3, V_i can achieve even larger common mode range from $VDD - 3V_{sg} + V_{dsat}$ to $VDD - V_{sg} - V_{dsat}$. Node Z is an additional pole added to the loop that should be pushed out for stability.

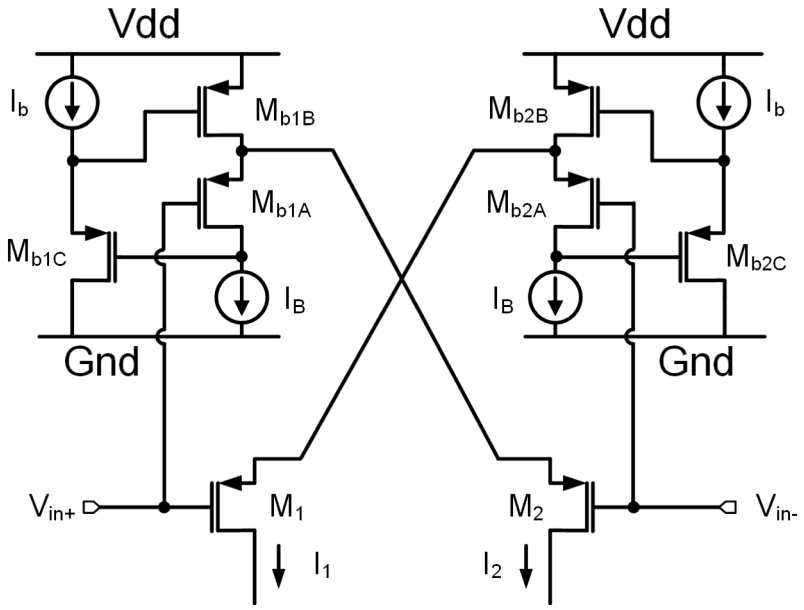


Fig. 3.5 Adaptive biasing differential pair.

Based on the previous discussion about the FVF cell, an adaptive biasing differential pair can be integrated [36]-[38]. A possible high voltage design of an adaptive biasing differential pair is illustrated in Fig. 3.5. Two high voltage version FVF outputs are cross connected to the sources of transistor M_1 and M_2. The sizes of transistors M_1, M_2, M_{b1A}, and M_{b2A} are kept to be the same. When the inputs of the differential pair V_{in+} and

V_{in-} are at the common mode voltage V_{cm}, the quiescent current through M_1 and M_2 are equal to I_B. When V_{in+} increases while V_{in-} keeps constant, the source of M_{b1A} and M_2 will increase too, and the V_{sg} of M_2. The current through M_2 which sourced from M_{b1B} keeps increasing until M_{b1B} enters the linear region. The maximum source current of M_2 can be much larger than $2I_B$. Meanwhile, the current of M_1 reduces. The currents I_1 and I_2 can be mathematically calculated by (3-10)(3-11), and the differential current $I_d = I_2 - I_1$ is expressed in (3-12)[37].

$$I_2 = \frac{\beta}{2}\left(\sqrt{\frac{2I_B}{\beta}} + (V_{in+} - V_{in-})\right)^2 \tag{3-10}$$

$$I_1 = \frac{\beta}{2}\left(\sqrt{\frac{2I_B}{\beta}} - (V_{in+} - V_{in-})\right)^2 \tag{3-11}$$

$$I_2 - I_1 = \sqrt{8\beta I_B}(V_{in+} - V_{in-}) \tag{3-12}$$

As shown in equation (3-12) the current difference depends on the input voltage difference. If the input voltage difference is large, the current difference can be much larger than $2I_B$. The chosen adaptive biasing differential pair therefore shows a class AB characteristic.

Another benefit of the adaptive biasing is the doubled input pair transconductance. Since V_{in+} and V_{in-} are connected to the gate of M_{b1A} and M_{b2A} (source follower), the small signal inputs will appear at both the gates and the sources of M_1 and M_2 with an inverting phase. The equivalent small signal voltage swings of M_1 and M_2 are doubled, so their effective transconductance will be doubled accordingly. This benefit means the constant biasing currents in M_{b1A} and M_{b2A} are being effectively utilized to amplify small signals,

rather than dissipated. With this adaptive biasing, the differential pair wideband operation can be achieved.

3.4 Linear Amplifier Design

A conventional current mirror OTA with a class AB output stage is employed as the linear amplifier in the ET supply modulator design in [33]. The equivalent transconductance of this amplifier is $Gm_{OTA} = gm_{in}K_2/K_1$, where K_1, K_2 are the transistor size ratios relative to the unit size [40]. The first stage OTA dc gain is given by (3-13), where g_{min} is the transconductance of the input pair, I_B is the biasing current in each input transistor, and λ is the channel length modulation coefficient. The nominal value of OTA's dc gain, A_{vOTA}, is approximately from 30 dB to 40 dB. In the envelope tracking applications, the supply modulator provides large biasing current to the PA. The equivalent loading seen from the PA drain is a low impedance. The proposed design can drive an equivalent of 6 Ω effective PA load. Due to this low output impedance, the class AB stage only provides a small dc gain, in the range of few dBs as shown in (3-14). The overall dc gain of this linear amplifier (3-15) is below 45 dB. To efficiently cancel the current ripple from the switching amplifier and reduce the dc error, the linear amplifier's dc gain needs to be further enhanced.

$$Av_{OTA} = gm_{in}\frac{K_2}{K_1}\left(\frac{K_1}{\lambda_8 I_B K_2} \parallel \frac{K_1}{\lambda_{12} I_B K_2}\right) = \frac{gm_{in}}{I_B(\lambda_8+\lambda_{12})} \tag{3-13}$$

$$\begin{aligned} Av_{ClassAB} &= (gm_{15} + gm_{16})(R_L \parallel ro_{15} \parallel ro_{16}) \\ &\approx (gm_{15} + gm_{16})R_L \end{aligned} \tag{3-14}$$

$$Av_{amp} = Av_{OTA}Av_{ClassAB} \tag{3-15}$$

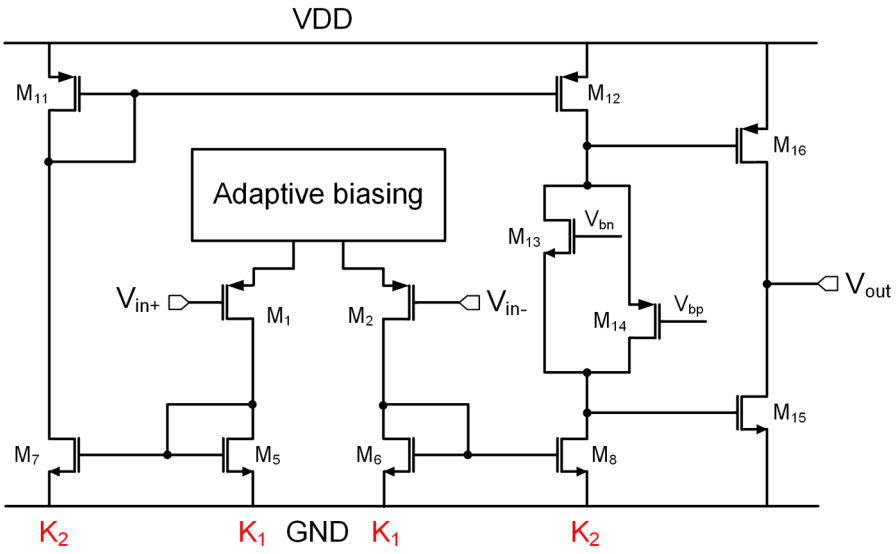


Fig. 3.6 Simplified schematic of linear amplifier with adaptive biasing current mirror OTA followed by class AB output stage.

Fig. 3.6 presents a linear amplifier with an adaptive biasing current mirror OTA followed by a class AB output stage. It not only increases dc gain by 6 dB to 51 dB, but also improves the slew rate by utilizing FVF adaptive biasing.

Fig. 3.7 shows the transistor level schematic of the proposed linear amplifier of the hybrid supply modulator. K_1, K_2 $(K_{2A}+K_{2B})$, K_3, and K_4 indicate the relative ratios of transistor sizes in each branch to unit size. Due to the high supply voltage of ET hybrid supply modulator, a high voltage version of adaptive biasing circuit is employed so that the input common voltage V_{cm} has a wider range. The input transistors M_1 and M_2 shown in Fig. 3.4 are splitted into M_{1A}, M_{1B} and M_{2A}, M_{2B} respectively. Since the sizes of transistors M_1 $(M_{1A}+M_{1B})$, M_2 $(M_{2A}+M_{2B})$, M_{b1A}, and M_{b2A} are same, the quiescent currents in M_1 $(M_{1A}+M_{1B})$ and M_2 $(M_{2A}+M_{2B})$ will be equal to I_B. The transistors M_3, M_4, M_9 $(M_{9A}+M_{9B})$, and M_{10} $(M_{10A}+M_{10B})$ act as two voltage controlled current sources (VCCS) [39]. If *Vin+*

increases, the currents in M_{1A} and M_{1B} will decrease and the currents in M_{2A} and M_{2B} will increase. Due to the VCCS formed by M_3 and M_{10}, the current in M_{10} will reduce as well. The current change in M_6 can be calculated as $I_6 = I_{2A} - I_{10}$. This indicates that by adding these VCCSs, the transconductance of the proposed OTA is enhanced. The transconductance, output impedance, and dc gain of the proposed OTA are derived in (3-16)(3-17)(3-18).

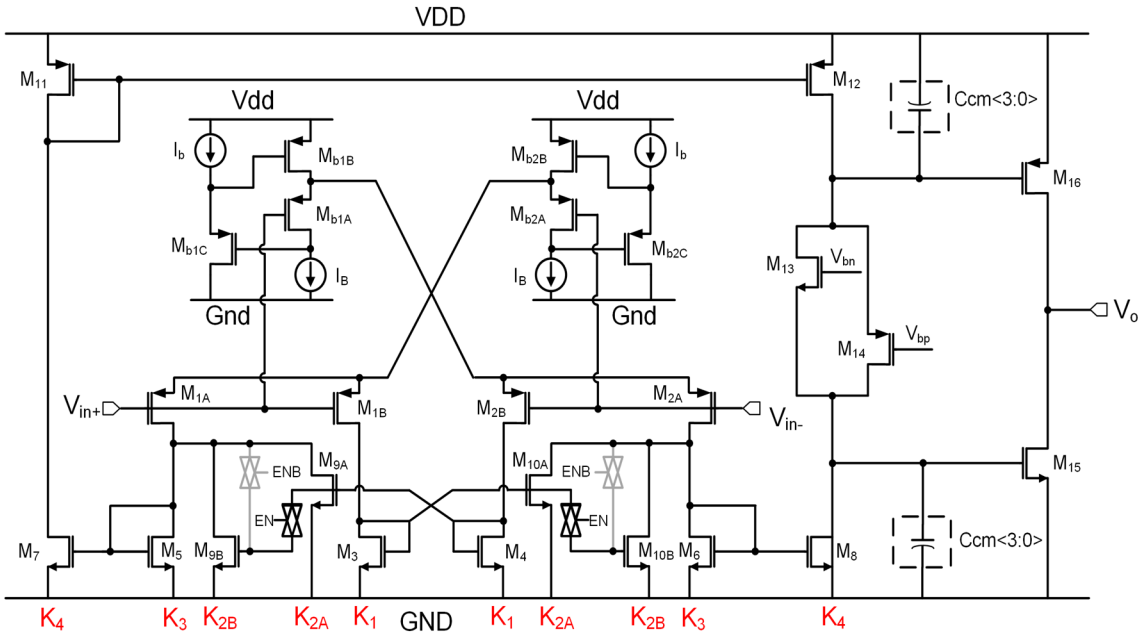


Fig. 3.7 Schematic of the proposed linear amplifier.

A small signal ac block diagram of the proposed linear amplifier is shown in Fig. 9. R_{load} and C_{load} are the PA drain equivalent resistance and capacitance. They are 6 Ω and 150 pF respectively in the design.

$$Gm_{OTA\_new} = 2gm_{in} \cdot \frac{2K_2+K_3}{K_1+K_2+K_3} \cdot \frac{K_4}{K_3} \tag{3-16}$$

$$Ro_{OTA_{new}} = \frac{K_1+K_2+K_3}{\lambda_8 I_B K_4} \parallel \frac{K_1+K_2+K_3}{\lambda_{12} I_B K_4}$$

$$= \frac{K_1+K_2+K_3}{K_4} \cdot \frac{1}{I_B(\lambda_8+\lambda_{12})} \tag{3-17}$$

$$Av_{OTA_{new}} = Gm_{OTA_{new}} Ro_{OTA_{new}}$$

$$= \frac{2gm_{in}}{I_B(\lambda_8+\lambda_{12})} \cdot \frac{2K_2+K_3}{K_3} \tag{3-18}$$

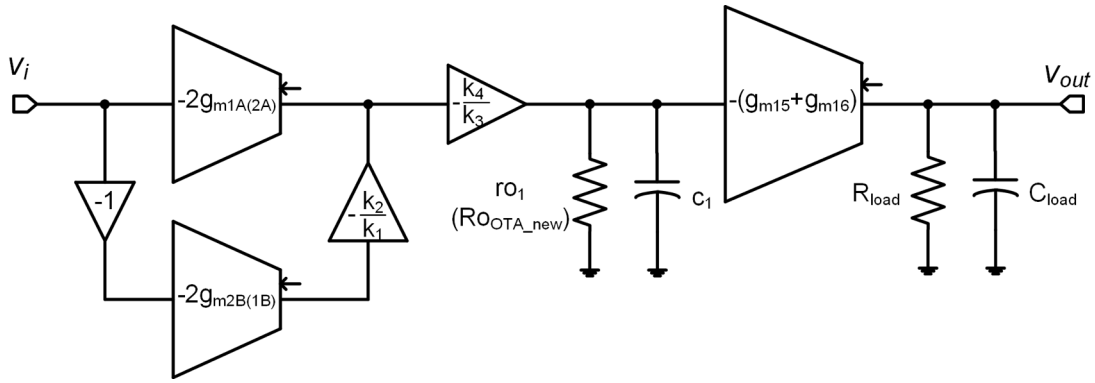


Fig. 3.8 Small signal AC block diagram of the proposed linear amplifier.

Comparing equation (3-13) and (3-18), if gm_{in}, λ and I_B are kept the same, it would show that the proposed OTA can boost dc gain by a factor of $2(2K_2+K_3)/K_3$. By choosing correct ratios, the proposed linear amplifier can achieve 61 dB loop dc gain in the gain of 2 V/V configuration, which is considered to be sufficient for accurate tracking. Comparing to the lower dc gain linear amplifier design, the higher dc gain design achieves wider unity gain frequency (UGF) under same current consumption condition. In other words, our proposed linear amplifier achieves wide bandwidth with less quiescent current and improves the efficiency of ET supply modulator.

An undesired effect of gain boosting is that the gates of M_3 and M_4 have some extra loading which pushes the high frequency pole to lower frequency and degrades the phase margin. Due to this reason, $K_2 \leq 3K_1$ should be chosen in order to trade-off between the achievable dc gain and the phase margin. Control signals, EN and ENB, are used to change the ratio of K_2 and K_3 to accommodate large PA loading variation. When EN is high and

ENB is low, $K_2 = K_{2A} + K_{2B}$ and $K_3 = K_3$; When EN is low and ENB is high, $K_2' = K_{2A}$ and $K_3' = K_{2B} + K_3$. According to (3-18), the latter scenario reduces OTA's dc gain to ensure stability in case of a large PA equivalent resistance seen by the hybrid ET supply modulator.

With adaptive biasing and gain enhancement utilized, the proposed linear amplifier achieves 93.4 V/μs positive, -152.5 V/μs negative slew rates and 43 MHz bandwidth at a closed loop gain of 2 V/V with 60° phase margin, consuming 14 mA quiescent current.

3.5 Slew Rate Comparison

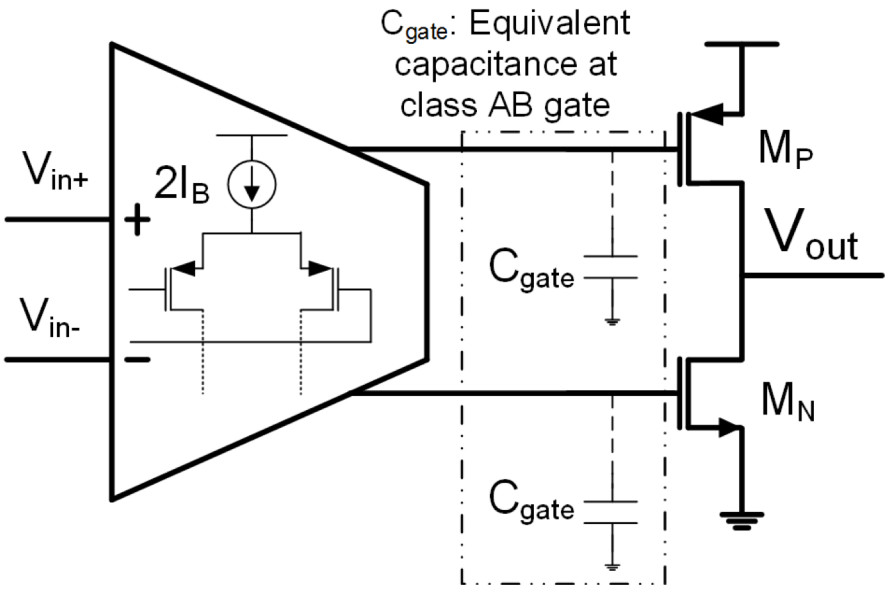


Fig. 3.9 General constant input biasing current amplifier with class AB output stage

Large-signal slew rate limiting can cause distortion and limited bandwidth in ET regulators. Compared to constant input biasing counterparts, one of the benefits of adaptive biasing is that it can achieve higher slew rate without increasing the input stage biasing quiescent current. Fig. 3.9 illustrates a general constant input biasing current amplifier with

a class AB output stage. The first stage can be implemented by a folded cascode amplifier, rail to rail input cascode amplifier, or conventional current mirror OTA. The input biasing current is $2I_B$. Since the class AB output stage needs to source and sink 500 mA peak current in our design, the sizes of MP and MN are 13.5 mm/700 nm and 4.5 mm/700 nm respectively. The capacitance at the gate of class AB stage is in tens of pF range. C_{gate} represents lumped capacitance at the gate of the class AB stage, this includes the gate capacitance of M_P or M_N plus any compensation capacitance used at this node.

In the proposed adaptive biasing current linear amplifier scenario, the slew rate is defined as:

$$SR_{ad} = \frac{I_{B\_ad}}{C_{gate}} \cdot \frac{K_2+K_3}{K_1+K_2+K_3} \cdot \frac{K_4}{K_3} \tag{3-19}$$

where SR_{ad}, I_{B_ad}, and C_{gate} are the slew rate of the proposed adaptive biasing linear amplifier, the maximum current sourced from the adaptive biasing stage and the lumped capacitance at the class AB gate, respectively. Parameters K_1, K_2, K_3, and K_4 are ratios discussed in Fig. 3.7. In the constant input biasing scenario, like the linear amplifier used in [33], the maximum slew rate is calculated as:

$$SR_{con} = \frac{2I_B}{C_{gate}} \cdot \frac{K_2}{K_1} \tag{3-20}$$

where SR_{con} and I_B are the slew rate of constant input biasing current linear amplifier in [33] and the biasing current in each input transistor. K_1 and K_2 are the ratios discussed in Fig. 3.6. Note that $I_{B\_ad} \gg 2I_B$, so that we have $SR_{ad} \gg SR_{con}$.

The adaptive biasing current scenario achieves 93.4 V/μs positive, -152.5 V/μs negative slew rates while the constant input biasing scenario only obtains 50 V/μs positive, -87 V/μs negative slew rates with same current consumption. After utilizing the adaptive

biasing technique, the positive and negative slew rates are improved by 86.8% and 75.3% respectively which making the proposed linear amplifier a perfect choice for the large PAPR envelope tracking applications.

3.6 Lossless Current Sensing Scheme

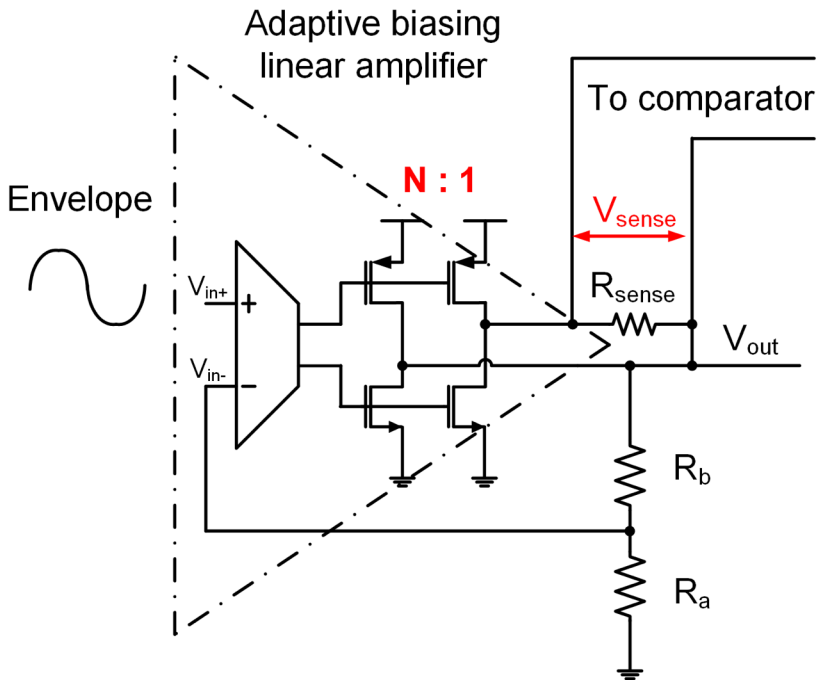


Fig. 3.10 Lossless current sensing scheme.

The class AB output buffer can be scaled down for current sensing as shown in Fig. 3.10. A sensing resistor R_{sense} is inserted between the current sensing branch's output and V_{out}. A scaled down linear amplifier's output current generates the sensing voltage V_{sense} across R_{sense} which is used as the input of hysteretic comparator. Since V_{sense} is small, the difference between I_{sense} and I_{linear}/N is negligible. This current sensing scheme reduces the power loss on sensing resistor and improves the modulator efficiency while still providing

accurate current sensing. Fig. 3.11 depicts the simulated current sensing error which is defined in (3-21).

$$\delta = \frac{I_{linear} - N \cdot I_{sense}}{I_{linear}} \times 100\% \quad (3\text{-}21)$$

Where δ, I_{linear}, I_{sense}, and N, are current sensing error, linear amplifier output current, current flows in sensing resistor and the class AB scale down ratio respectively. The maximum sensing error is 1% which means that the control signal for the switching amplifier in our design has less than 1% error. This small error does not affect the operation of the hybrid supply modulator.

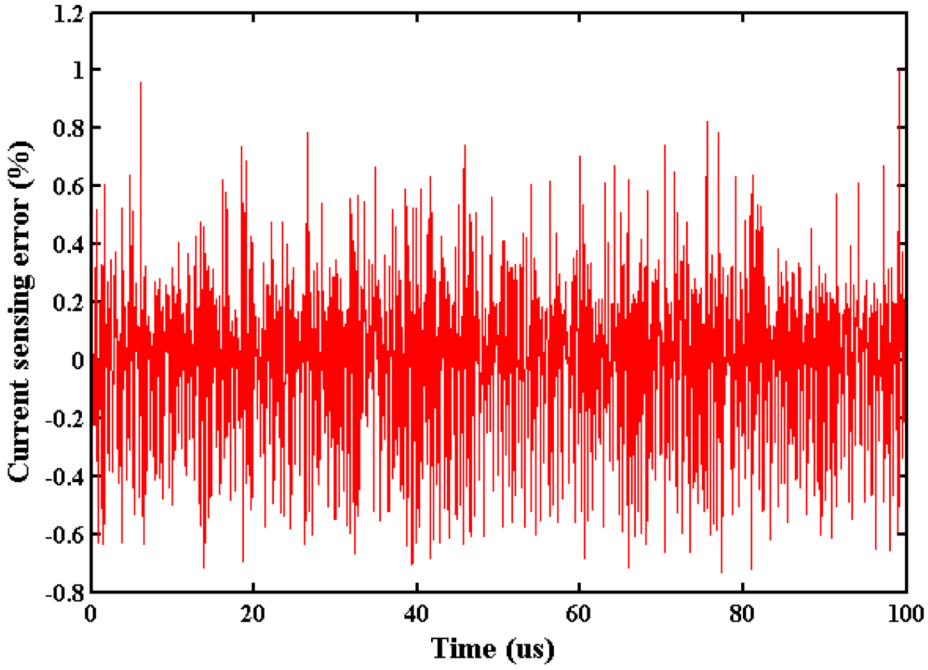


Fig. 3.11 Simulated current sensing error.

3.7 Design of Comparator and Non-overlapped Driver

Fig. 3.12 shows the hysteretic comparator schematic. M_4 and M_5 form positive feedback for input signals. α is the transistor size ratio defined in (3-22). The schematic of

Fig. 3.12 can be a high gain amplifier, a latch or a hysteretic comparator, when α<1, α=1, and α>1, respectively. To obtain a hysteretic comparator, α>1 is required. The hysteretic window at dc is defined by [41].

$$\alpha = \frac{W/L_{4,5}}{W/L_{3,6}} \tag{3-22}$$

$$V_H = \sqrt{\frac{I_o}{\beta_{1,2}}}\frac{\sqrt{\alpha}-1}{\sqrt{1+\alpha}} \tag{3-23}$$

Note that V_H calculated in (3-23) is only valid if input signals are dc or low frequency signals. If input signals are high frequency signals, V_H will increase due to the unsettled inner node voltage. Actual hysteretic window is a function of frequency, as $V_H(f)$. This effect must be considered when calculating the switching amplifier's average switching frequency.

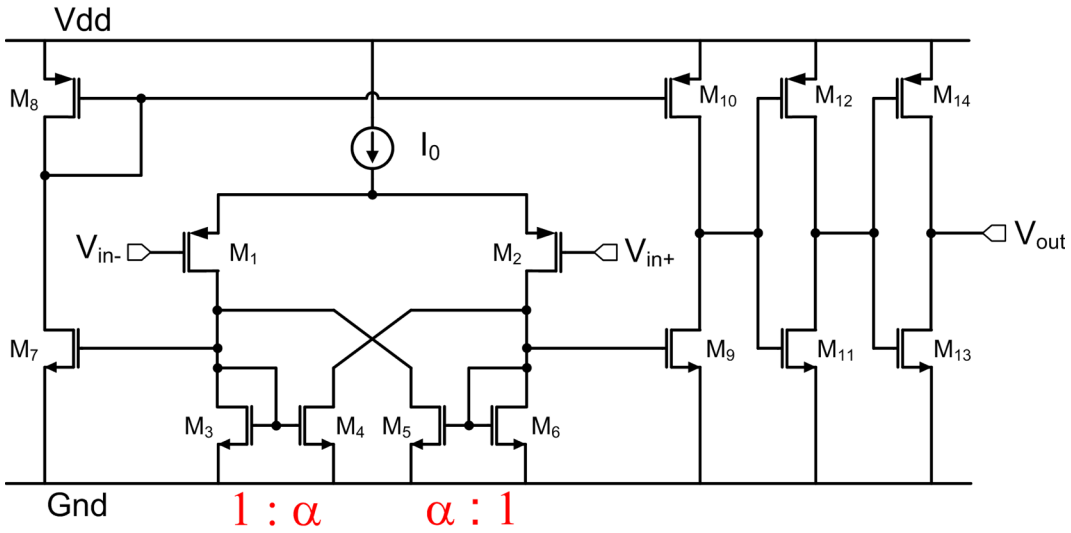


Fig. 3.12 Simplified hysteretic comparator schematic.

The comparator layout matching should be considered when choosing α. If α is some random number, it is difficult to do the matching in the layout. Numbers such as 1.25, 1.5, and 2 are relatively easier to implement. Numbers such as 1.3 or 1.7 will be a bad

choice due to matching concerns. In our design, α =1.5 is chosen and the corresponding V_H is 14 mV.

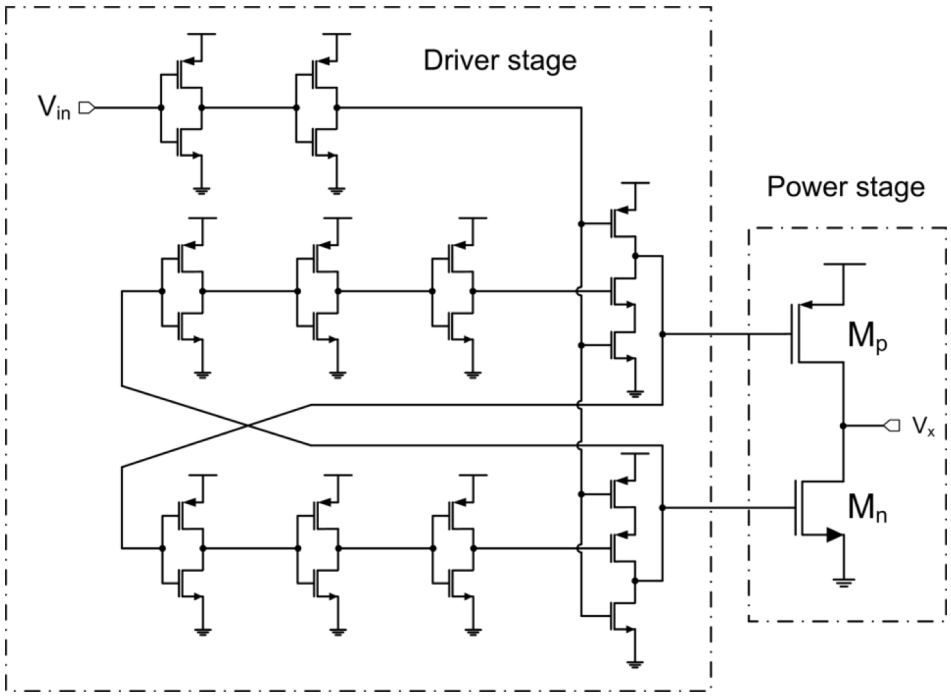


Fig. 3.13 Schematic of anti shoot-though driver with power stage.

Fig. 3.13 illustrates an anti shoot-through driver schematic [42]. The driver stage creates deadtime to prevent the power NMOS and the power PMOS turning on simultaneously. Therefore, there are no power loses from large shoot through current which improves the efficiency of hybrid supply modulator.

3.8 Design of Switching Amplifier

As discussed in Section II, the switching frequency is chosen to trade-off between the efficiency and linearity of ET supply modulator. In simulation, L from 6.8 μH to 10 μH yields optimized results. Fig. 3.14 presents the statistical probability distribution of switching frequency when L=10 μH. More than 95% of the switching frequency is located

between 1 MHz and 8 MHz. In order to suppress the current ripple from switching amplifier, linear amplifier GBW should be at least 5X of the switching frequency. The proposed linear amplifier GBW is 43 MHz which can effectively cancel the third and fifth order harmonics of majority switching frequency and improve the ET supply modulator linearity

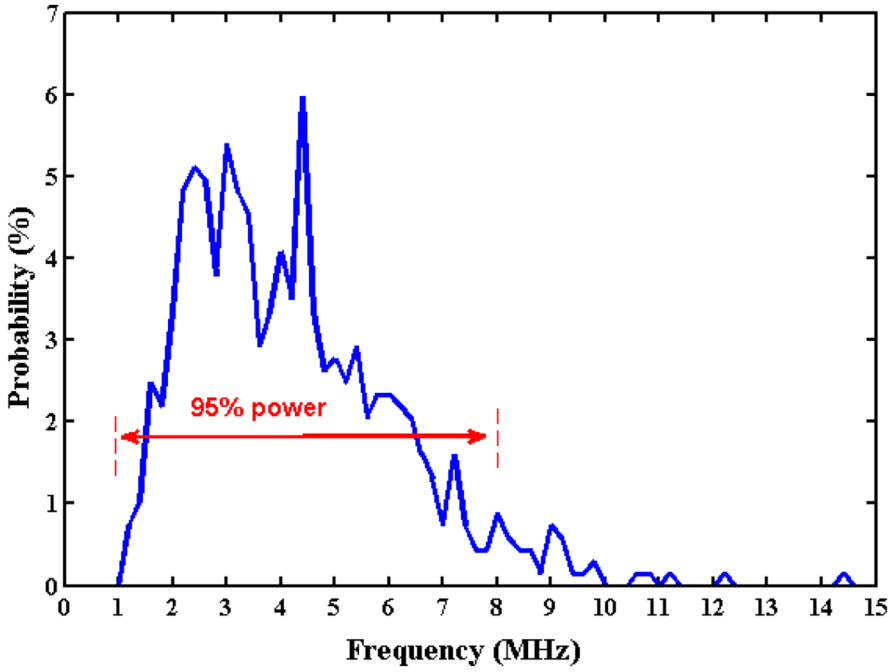


Fig. 3.14 Statistic probability distribution of switching frequency when L=10 μH.

CHAPTER 4

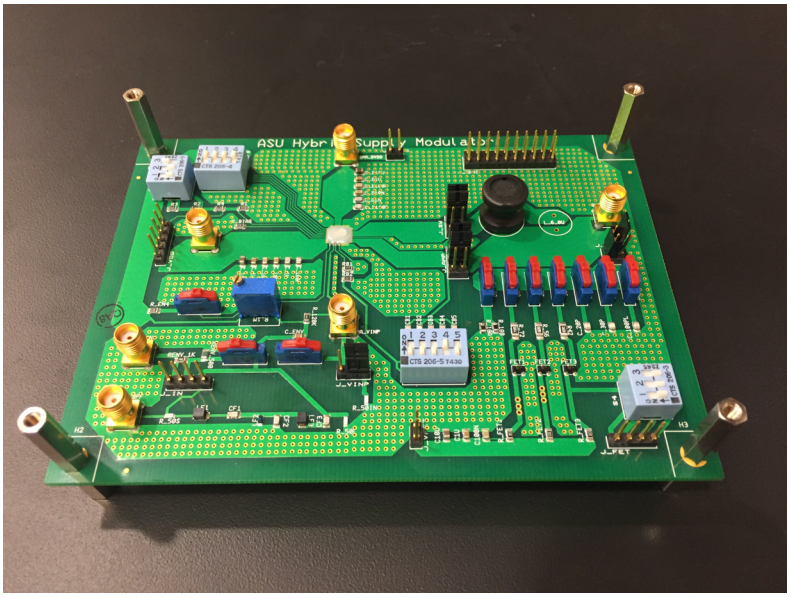
MESURAMENT

4.1 PCB Design and Test Setup

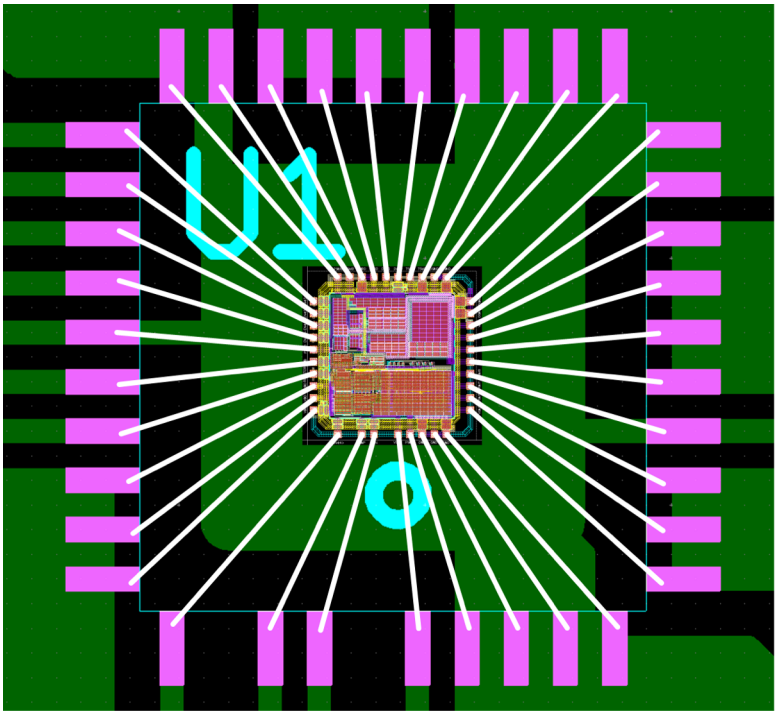
The proposed ET supply modulator is implemented in a 0.18 μm CMOS process with thick gate oxide devices which can stand up to 3.6 V. ESD cells are also designed to protect device. The layout of ESD are compliant to the foundry ESD design rules. The fabricated chips are assembled to the double layer printed circuit board (PCB) test board through wire bonding and sealed with epoxy. Fig. 4.1 (a) presents an assembled test board and fig. 4.1 (b) depicts the chip layout and the wire bonding diagram.

A micrograph of the test chip is shown in Fig. 4.2. The core area of the converter is 1.1 mm2 (1.05 mm x 1.05 mm). All ET supply modulator circuits are on the chip except the inductor in the switching amplifier. A commercial two stage HBT RF PA (Band 1, 1.95 GHz) is used to characterize the ET supply modulator. A DC blocker is also applied to protect spectrum signal analyzer.

Test bench setup is shown in Fig. 4.3. LTE baseband IQ signal is generated in Keysight Signal Studio software 7624B and then sent to the RF Vector Signal Generator and the Envelope Signal Generator respectively. Envelope shaping is applied in Signal Studio software too. The RF path and the envelope path are synchronized and aligned to get rid of any linearity distortion due to the path delay difference. Fig 4.4 illustrates the lab test bench setup. All lab ESD protection measures were taken to prevent damage to device and lab equipment.



(a)



(b)

Fig. 4.1 (a) An assembled test board. (b) The chip layout and the wire bonding diagram.

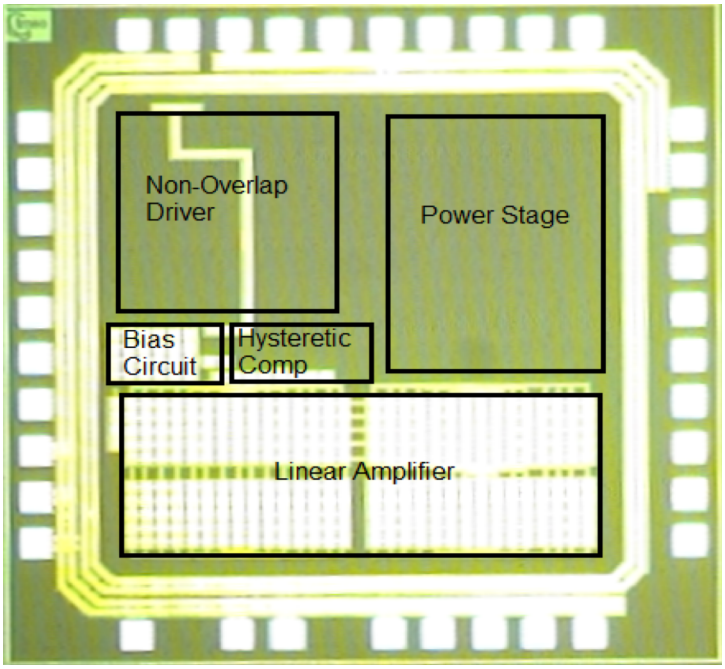


Fig. 4.2 Micrograph of proposed ET supply modulator, core area is 1.1 mm^2 (1.05 mm X 1.05 mm)

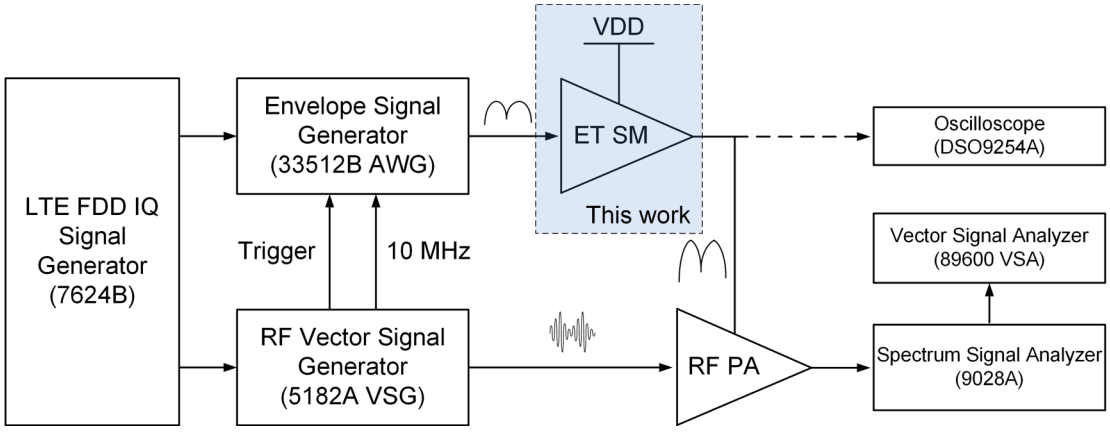


Fig. 4.3 Test bench setup to characteristic proposed ET supply modulator

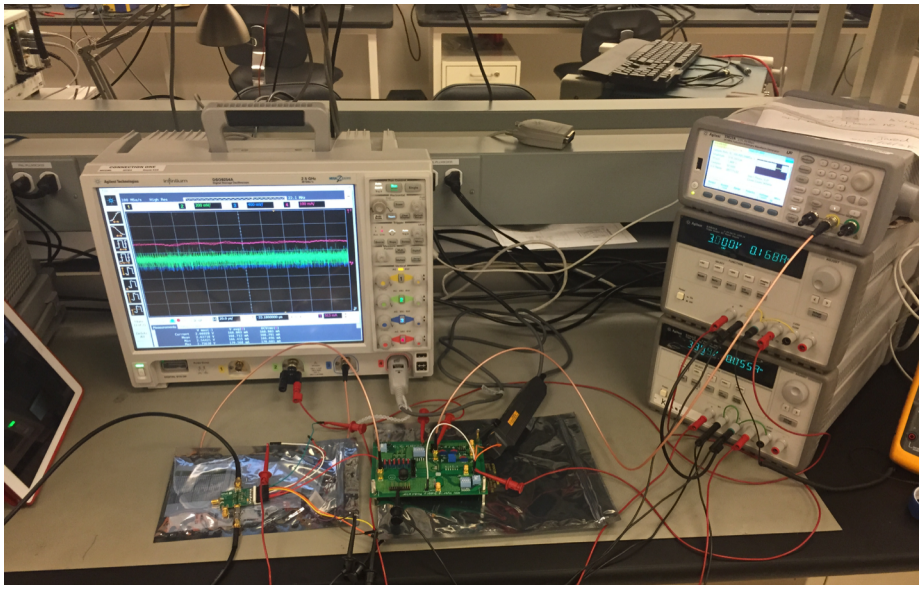


Fig. 4.4 The lab test bench setup.

4.2 Measurement Results

4.2.1 Standalone ET Supply Modulator Efficiency Characterization

The standalone ET supply modulator efficiency is characterized with an equivalent loading of 6 Ω resistance and 150 pF capacitance. A 10 MHz LTE QPSK signal with 7.24 dB maximum PAPR is employed as the envelope signal. Fig. 4.5 shows the measured transient response of the modulator's input and output. Output tracks input envelope with less than few millivolts error, when taking 6 dB gain into consideration. The efficiency of ET supply modulator is also measured and shown in Fig. 4.6. It achieves 83% maximum efficiency and over 70% efficiency when the output power larger than 0.3 W.

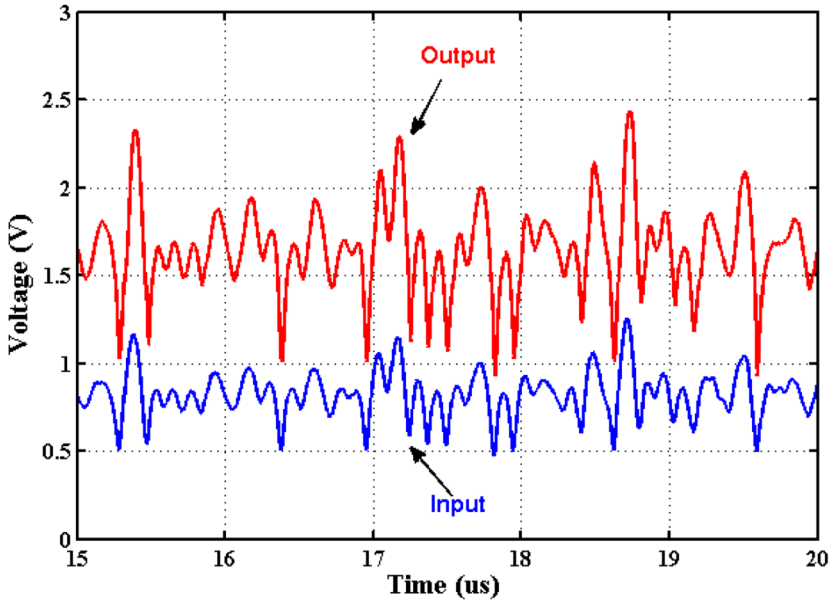


Fig. 4.5 Measured ET supply modulator input and output transient, output voltage is exactly two time of input voltage.

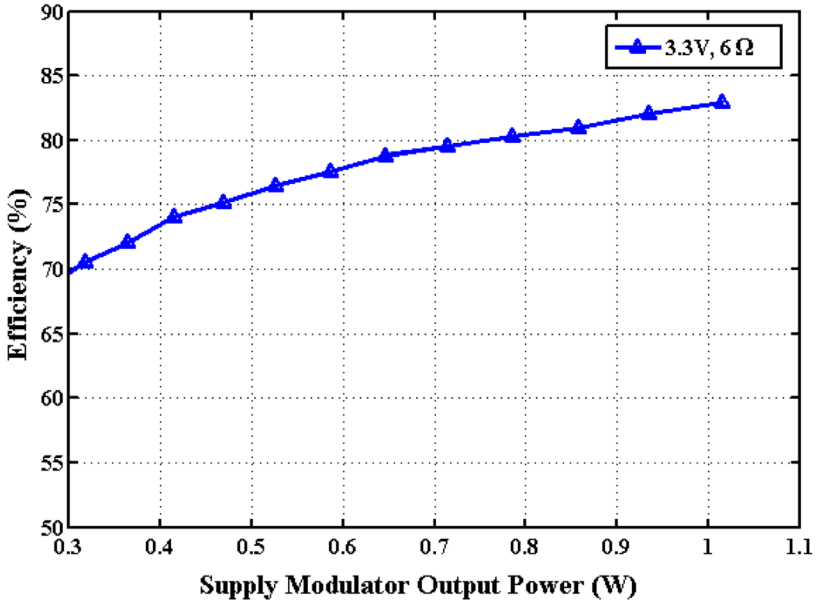


Fig. 4.6 Standalone ET supply modulator efficiency plot.

4.2.2 ET PA System Efficiency Characterization

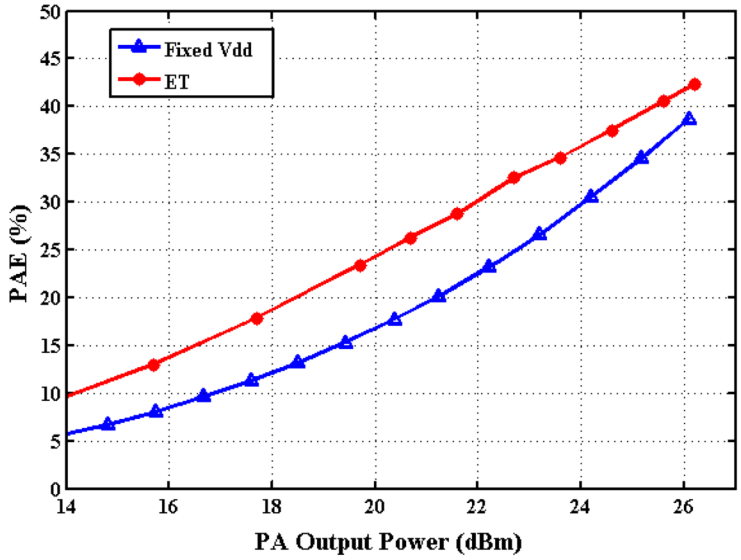


Fig. 4.7 PAE of PA with fixed supply and ET PA system with LTE QPSK 10 MHz signal at 1.95 GHz.

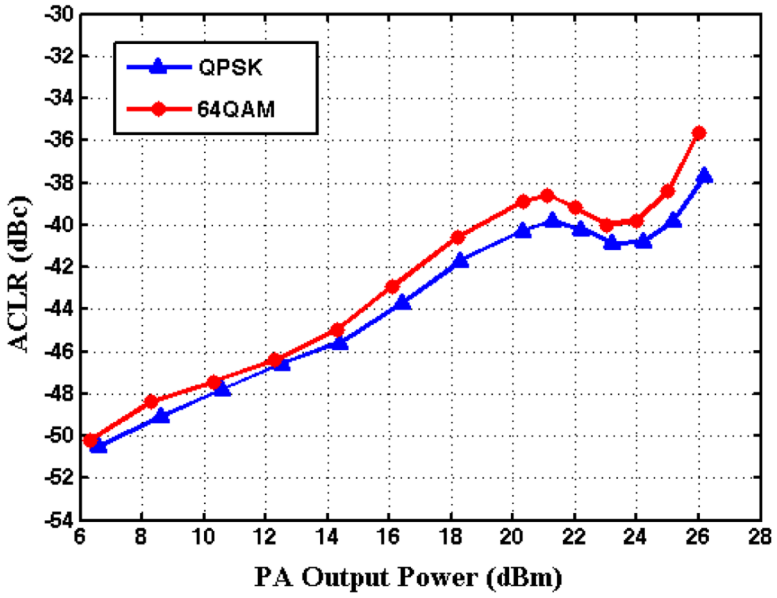


Fig. 4.8 ACLR of ET PA system without DPD for 10 MHz QPSK and 64QAM LTE signal at 1.95 GHz

To evaluate the ET PA system, a 3.6 V supply voltage is used with a corresponding maximum modulator output voltage of 3.4 V. The comparison between the measured power added efficiency (PAE) with fixed supply and the ET PA system is depicted in Fig. 4.7. The measured PAE for ET PA system is 42.3% at 26.2 dBm PA output power. At 6 dB back-off, 20 dBm PA output power, PAE is more than 24% which is improved by 8% compared to the fixed supply PA.

4.2.3 ET PA System Linearity Characterization

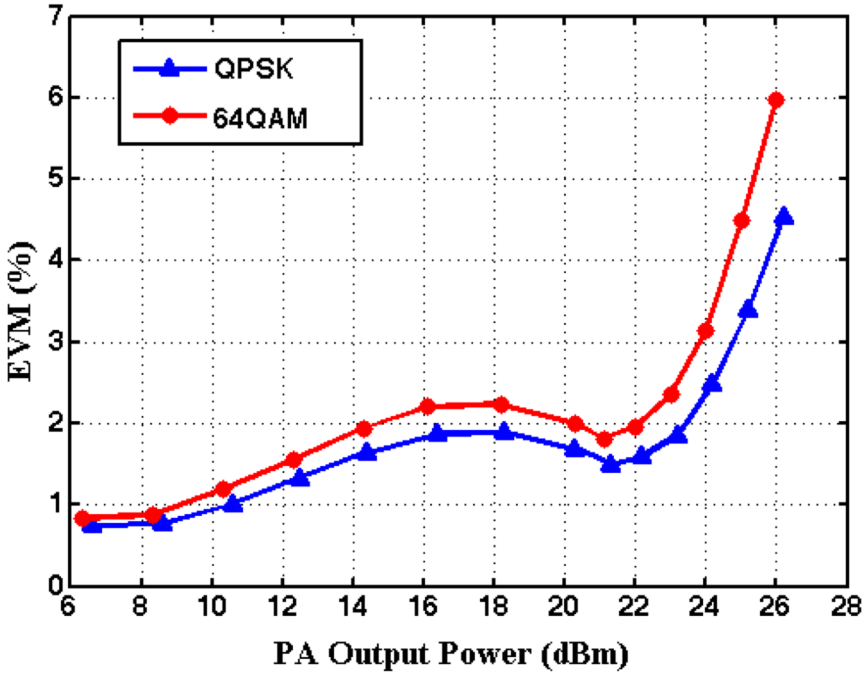


Fig. 4.9 EVM of ET PA system without DPD for 10 MHz QPSK and 64QAM LTE signal at 1.95 GHz

The linearity measurements of ET PA system are presented with both a 7.24 dB PAPR 10 MHz QPSK LTE signal and an 8.15 dB PAPR 10 MHz 64QAM LTE signal [43]. Fig. 4.8 and Fig. 4.9 depict the adjacent channel leakage ratio (ACLR) and the error vector

magnitude (EVM) measurements. At 26.2 dBm PA output power, -37.7 dBc ACLR and 4.5% EVM are achieved with QPSK modulated signal, while at 26 dBm PA output power, -35.6 dBc ACLR and 6% EVM are achieved with 64QAM modulated signal. All measurements are taken without any digital pre-distortion. The power spectral densities are shown in Fig. 4.10 with LTE mask. Without DPD, the ET PA system still meets the LTE mask. The out of band power spectral densities are shown in Fig. 4.11. The experimental results depict that the proposed adaptive biasing linear amplifier can effectively cancel the third and fifth order harmonics of the majority switching frequency and improve ET PA system linearity, with low receiver band noise up to 90 MHz offset.

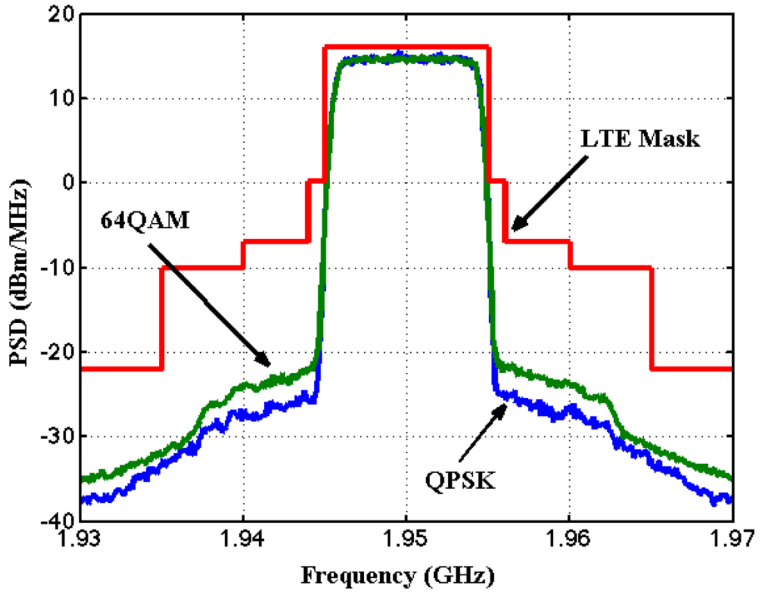


Fig. 4.10 Power spectral density of ET PA system without DPD for 10 MHz QPSK and 64QAM LTE signal at 1.95 GHz

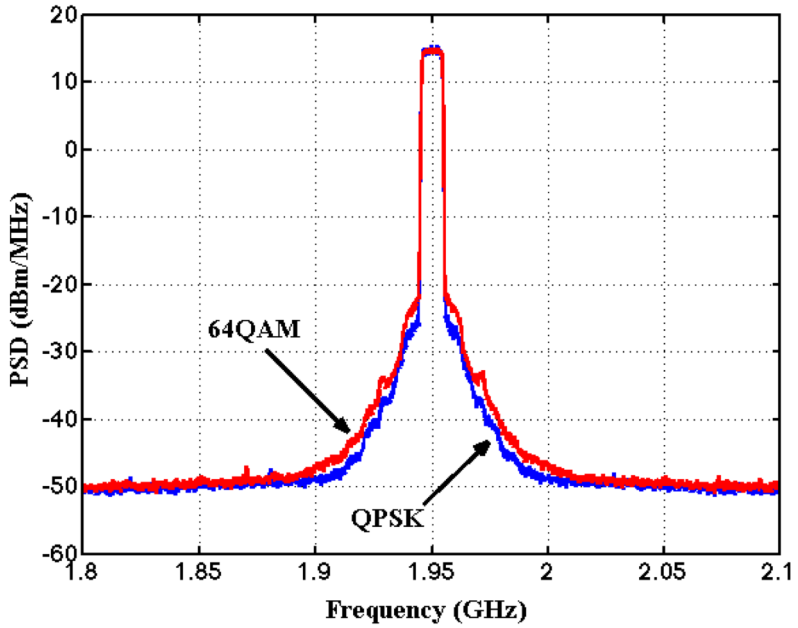


Fig. 4.11 Out of band power spectral density of ET PA system without DPD for 10 MHz QPSK and 64QAM LTE signal at 1.95 GHz

4.3 Chip Performance Summary

Table I summarizes the comparison of this work and previously reported results.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF PROPOSED ET SUPPLY MODULATOR WITH STATE-OF-THE-ART SUPPLY MODULATOR DESIGN

	Modulation	PAPR (dB)	Center Frequency (GHz)	V_{DD} (V)	η_{SM} (%)	P_{out} (dBm)	PAE (%)	EVM (%)	ACLR (dBc)	Technology	DPD
[9]	LTE 16QAM 10 MHz	6.44	1.74	5/2.5	-	27	39.8	3.81	-35.7	SM:0.18 µm CMOS PA:HBT	No
[11]	LTE 16QAM 10 MHz	-	1.9	4.2	-	23.4	38	4.9	-	SM+PA:0.35 µm SiGe BiCMOS	No
[12]	LTE 16QAM 20 MHz	-	0.7	5	78.4	27.9	40.2	5.64	-	SM:0.35 µm BCD PA:0.35 µm SiGe BiCMOS	No
[14]	LTE 16QAM 10 MHz	7.5	1.85	4	-	26.5	37.6	2.4	-36.8	SM+PA: 0.18 µm CMOS	No
[15]	LTE 10 MHz	-	1.747	-	80	26	40.2	-	-39.4	SM: 0.13 µm CMOS PA: HBT	No
[16]	LTE 16QAM 20 MHz	7.5	1.71	Multi	75.9	27	40	3.23	-35.3	SM+PA: 0.18 µm CMOS	No
[17]	LTE 16QAM 5 MHz	7.5	0.78	3.3	73	24	45.4	3.7	-31.1	SM+PA: 0.18 µm CMOS	No
[19]	LTE 16QAM 10 MHz	7.5	1.7	4.7	81.5	28.5	36.6	3	-35.6	SM+PA: 0.18 µm CMOS	No
[20]	HSUPA R6 5 MHz	6.7	-	3.8	80	26	37	<2	-40	SM:0.15 µm CMOS PA:HBT	-
[21][a]	10 MHz Sinusoid	-	-	1.2	81	-	-	-	-	SM: 0.13 µm CMOS PA: Not Present	-
This Work	LTE QPSK 10 MHz	7.24	1.95	3.6	83	26.2	42.3	4.5	-37.7	SM: 0.18 µm CMOS PA:HBT	No
	LTE 64QAM 10 MHz	8.15	1.95	3.6	-	26	-	6	-35.6		

[a]Dynamic efficiency is used for comparison.

CHAPTER 5

CONLUSION

5.1 Summary

After more than 40 years' development, mobile phone has evolved from 1G pricy, heavy, and bulky analog phone to 4G LTE affordable, small and powerful smartphone. While people are enjoying the high data rate smartphone, which brought by the advanced communication technology, reducing cellphone power consumption to increase battery life has become more and more important.

ET technique has drawn great attention due to its high efficiency, high linearity, and wideband operation. After analyzing the issues of state of the art ET supply modulator design. A high efficiency, high linearity and wideband ET hybrid supply modulator utilizing adaptive biasing and gain enhancement for the linear amplifier is proposed. The proposed adaptive biasing ET supply modulator provides high slew rate and accurate tracking concurrently.

To verify the proposed high slew rate adaptive biasing ET supply modulator, a test chip is designed, fabricated and characterized. The test chip is fabricated in a 0.18 μm CMOS process with thick gate oxide devices. The proposed ET supply modulator design efficiently achieves sufficient dc gain, wide bandwidth, and high slew rate simultaneously, which the prior works did not address. The 61 dB loop dc gain, 83% peak efficiency, and 93.4 V/μs positive, -152.5 V/μs negative slew rates which are improved by 86.8% and 75.3% respectively, make the proposed ET modulator design an excellent candidate to track the

complicated large PAPR envelope signals and improve LTE ET PA system's overall efficiency.

5.2 Future Work

The proposed ET supply modulator can be combined with other techniques to further improve efficiency, such as AC coupled linear amplifier, multi-level supply converter and even supply modulated linear amplifier. Adaptive current ripple cancellation can also improve ET supply modulator linearity and efficiency.

Due to the hysteretic control of the switching amplifier, the current control loop cannot be modeled by linear model. A more sophisticated model of the current control loop would provide more insight on the current frequency response to ET supply modulator. Which can potentially optimize current design to further improve linearity and efficiency.

REFERENCES

[1] "James Clerk Maxwell," [online Document], Wikipedia, Available: https://en.wikipedia.org/wiki/James_Clerk_Maxwell

[2] "Claude Shannon," [online Document], Wikipedia, Available: https://en.wikipedia.org/wiki/Claude_Shannon

[3] "History of mobile phones," [online Document], Wikipedia, Available: https://en.wikipedia.org/wiki/History_of_mobile_phones#1G_.E2.80.93_Analogue_cellular

[4] "LTE (telecommunication)," [online Document], Wikipedia, Available: https://en.wikipedia.org/wiki/LTE_(telecommunication)

[5] "LTE Overview," [online Document], 3gpp, Available: http://www.3gpp.org/technologies/keywords-acronyms/98-lte

[6] "LTE/4G connections will pass 100 million this week," [online Document], telecomlead, May 2013, Available: http://www.telecomlead.com/4g-lte/lte-4g-connections-will-pass-100-million-this-week-55273-31158

[7] A. Burger, "Global LTE Forecast: 78.6% Annual Growth to 2019," [online Document], telecompetitor, Dec 2015, Available: http://www.telecompetitor.com/global-lte-forecast-78-6-annual-growth-to-2019/

[8] "Global 4G (LTE) Devices Market Value to Increase from US $ 344.8 Bn in 2016 to US $ 926.1 Bn by 2024," [online Document], Persistence market research, Nov 2016, Available: http://www.persistencemarketresearch.com/mediarelease/4g-lte-devices-market.asp

[9] "Your smartphone's best app? Battery life, say 89% of Britons," [online Document], theguardian, May 2014, Available: https://www.theguardian.com/technology/2014/may/21/your-smartphones-best-app-battery-life-say-89-of-britons

[10] "The History of the Mobile Phone," [online Document], Washington Post, Sep 2014, Available: https://www.washingtonpost.com/news/the-switch/wp/2014/09/09/the-history-of-the-mobile-phone/?utm_term=.621e9f4eb3b2

[11] X. Chen, N. Ding, A. Jindal, Y. C. Hu, M. Gupta, and R. Vannithamby, "Smartphone Energy Drain in the Wild: Analysis and Implications," Proceedings of the *2015 ACM*

SIGMETRICS International Conference on Measurement and Modeling of Computer Systems, June. 2015, Portland, Oregon, USA

[12] J. Hendy, "Envelope Tracking: Fuel injection for the RF Front End," *Cambridge Wireless*, 25 Sep 2014.

[13] L. R. Kahn, "Single-sideband transmission by envelope eliminationand restoration," Proc. IRE, vol. 40, no. 7, pp. 803–806, Jul. 1952.

[14] J. S. Walling, S. S. Taylor, and D. J. Allstot, "A class-G supply modulator and class-E PA in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2339–2347, Sep. 2009.

[15] Pinon, F. Hasbani, A. Giry, D. Pache, and C. Garnier, "A single- chip WCDMA envelope reconstruction LDMOS PA with 130 MHz switched-mode power supply," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig*., Feb. 2008, pp. 564–565.

[16] B. Sahu and G. A. Rincón-Mora, "A high efficiency WCDMA RF power amplifier with adaptive, dual-mode buck-boost supply and bias-current control," *IEEE Microw. Compon. Lett.*, vol. 17, no. 3, pp. 238–240, Mar. 2007.

[17] J. Sankman, M. K. Song and D. Ma, "Switching-converter-only multiphase envelope modulator with slew rate enhancer for LTE power amplifier applications," in *IEEE Trans. Power Electron.,* vol. 31, no. 1, pp. 817-826, Jan. 2016.

[18] P. Y. Wu and P. K. T. Mok, "A two-phase switching hybrid supply modulator for RF power amplifier with 9% efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2543–2556, Dec. 2010.

[19] F. Wang, D. F. Kimball, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope- tracking OFDM power amplifier," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1271–1281, Jun. 2007.

[20] J. Choi, D. Kim, D. Kang, and B. Kim, "A polar transmitter with CMOS programmable hysteretic-controlled hybrid switching supply modulator for multistandard applications," *IEEE Trans. Microw. Theory Techn*., vol. 57, no. 7, pp. 1675–1686, Jul. 2009.

[21] D. Kim, D. Kang, J. Choi, J. Kim, Y. Cho, and B. Kim, "Optimization for envelope shaped operation of envelope tracking power amplifier," *IEEE Trans. Microw. Theory Techn*., vol. 59, no. 7, pp. 1787–1795, Jul. 2011.

[22] J. Kim, D. Kim, Y. Cho, D. Kang, B. Park, and B. Kim, "Envelope- tracking two-stage power amplifier with dual-mode supply modulator for LTE applications," *IEEE Trans. Microw. Theory Techn*., vol. 61, no. 1, pp. 543–552, Jan. 2013.

[23] Y. Li, J. Lopez, P.-H. Wu, W. Hu, R. Wu, and D. Y. C. Lie, "A SiGe envelope-tracking power amplifier with an integrated CMOS envelope modulator for Mobile WiMAX/3GPP LTE transmitters," *IEEE Trans. Microw. Theory Techn*., vol. 59, no. 10, pp. 2525–2536, Oct. 2011.

[24] Y. Li, J. Lopez, C. Schecht, R. Wu, and D. Y. C. Lie, "Design of high efficiency monolithic power amplifier with envelope-tracking and transistor resizing for broadband wireless applications," *IEEE J. Solid- State Circuits*, vol. 47, no. 9, pp. 2007–2018, Sep. 2012.

[25] R. Wu, Y. Liu, J. Lopez, C. Schecht, Y. Li, and D. Y. C. Lie, "High efficiency silicon-based envelope-tracking power amplifier design with envelope shaping for broadband wireless applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2030–2040, Sep. 2013.

[26] M. Hassan, L. E. Larson, V. W. Leung, and P. M. Asbeck, "A combined series-parallel hybrid envelope amplifier for envelope tracking mobile terminal RF power amplifier applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1185–1198, May 2012.

[27] S. Jin, K. Moon, B. Park, J. Kim, Y. Cho, H. Jin, D. Kim, M. Kwon, and B. Kim, "CMOS saturated power amplifier with dynamic auxiliary circuits for optimized envelope tracking," *IEEE Trans. Microw. Theory Techn*., vol. 62, no. 12, pp. 3425–3435, Dec. 2014.

[28] S.-C. Lee, J.-S. Paek, J.-H. Jung, Y.-S. Youn, S.-J. Lee, M.-S. Cho, J.-J. Han, J.-H. Choi, Y.-W. Joo, T. Nomiyama, S.-H. Lee, I.-Y. Sohn, T. B. Cho, B.-H. Park, and I. Kang, "A hybrid supply modulator with 10dB ET operation dynamic range achieving a PAE of 42.6% at 27.0dBm PA output power," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2015, pp. 42-43.

[29] J. Kim et al., "Highly efficient RF transmitter over broad average power range using multilevel envelope-tracking power amplifier," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 62, no. 6, pp. 1648–1657, Jun. 2015.

[30] J. Ham *et al*., "CMOS power amplifier integrated circuit with dual-mode supply modulator for mobile terminals," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 63, no. 1, pp. 157-167, Jan. 2016.

[31] Y. Cho, D. Kang, J. Kim, D. Kim, B. Park, and B. Kim, "A dual power-mode multiband power amplifier with envelope tracking for handset applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1608–1619, Apr. 2013.

[32] B. Park *et al*., "High-performance CMOS power amplifier with improved envelope tracking supply modulator," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 798-809, March 2016.

[33] P. Riehl, P. Fowers, H.-P. Hong, and M. Ashburn, "An AC- coupled envelope modulator for HSUPA transmitters with 80% modulator efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 364–365.

[34] M. Tan and W. H. Ki, "An efficiency-enhanced hybrid supply modulator with single-capacitor current-integration control," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 533-542, Feb. 2016.

[35] W. Chu, B. Bakkalogle, and S. Kiaei, "A 10 MHz-bandwidth 2 mV-ripple PA-supply regulator for CDMA transmitters," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2008, pp. 448–449.

[36] R. G. Carvajal, J. Ramírez-Angulo, A. J. Lopez-Martin, A. Torralba, J. A. G. Galan, A. Carlosena, and F. M. Chavero, "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 7, pp. 1276–1291, Jul. 2005.

[37] A. J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R. G. Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 1068–1077, Mar. 2005.

[38] S. Baswa, A. J. Lopez-Martin, J. Ramirez-Angulo, and R. G. Carvajal, "Low-voltage micropower super class AB CMOS OTA," *Electron. Lett*., vol. 40, pp. 216–217, Feb. 2004.

[39] J. Roh, "High-gain class AB OTA with low quiescent current." *Analog Integrated Circuits and Signal Processing*, vol. 47, Issue 2, pp. 225-228, May 2006.

[40] R. J. Baker, "Operational Amplifiers I," in *CMOS Circuit Design, Layout, and Simulation*, 3rd ed. Piscataway, NJ: Wiley-IEEE Press, 2010, pp. 796-798

[41] R. Gregorian, "Comparators," in *Introduction to CMOS OP-AMPs and Comparators*, New Yory: Wiley-Interscience, 1999, pp. 192-197

[42] C. Yoo, "A CMOS buffer without short-circuit power consumption," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*., vol. 47, pp. 935–937, Sep. 2000.

[43] LTE UE Category, August, 2016. Available: http://www.3gpp.org/keywords-acronyms/1612-ue-category, 36.306 table 4.1-2, Category 8