Dual Application ADC using Three Calibration Techniques in 10nm Technology

by

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ABSTRACT

In this work, a 12-bit ADC with three types of calibration is proposed for high speed security applications as well as a precision application. This converter performs for both applications because it satisfies all the necessary specifications such as minimal device mismatch and offset, programmability to decrease aging effects, high SNR for increased ENOB and fast conversion rate. The designed converter implements three types of calibration necessary for offset and gain error, including: a correlated double sampling integrator used in the first stage of the ADC, a power up auto zero technique implemented in the digital code to store any offset and subtract out if necessary, and an automatic startup and manual calibration to control the common mode voltages. The proposed ADC was designed in Intel's 10nm technology. This ADC is designed to monitor DC voltages for the precision and high speed applications. The conversion rate of the analog to digital converter is programmable to 7μs or 910ns, depending on the precision or high speed application, respectively. The range of the input and reference supply is 0 to 1.25V. The ADC is designed in Intel 10nm technology using a 1.8V supply consuming an area of 0.0705mm^2. This thesis explores challenges of designing a dual-purpose analog to digital converter, which include: 1.) increased offset in 10nm technology, 2.) dual application ADC that can be accurate and fast, 3.) reducing the parasitic capacitance of the ADC, and 4.) gain error that occurs in ADCs.

ACKNOWLEDGMENTS

There are many people that guided in this journey and I am truly grateful for everyone that has. I am not sure how I would have completed this without all of the support, kindness and understanding.

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CHAPTER 1

INTRODUCTION

Analog to digital converters (ADC) are used in a wide variety of applications, such as security, microphones, digital camera, etc. These converters aid in the translation of analog signals to an equivalent digital signal to process information. One application of an ADC, provided in Figure 1, is a monitoring system of a field-programmable gate array (FPGA). In this application, there are two parameters that are typically monitored. One being the on-die supply voltages and the other is the on-die temperature [1] [2].

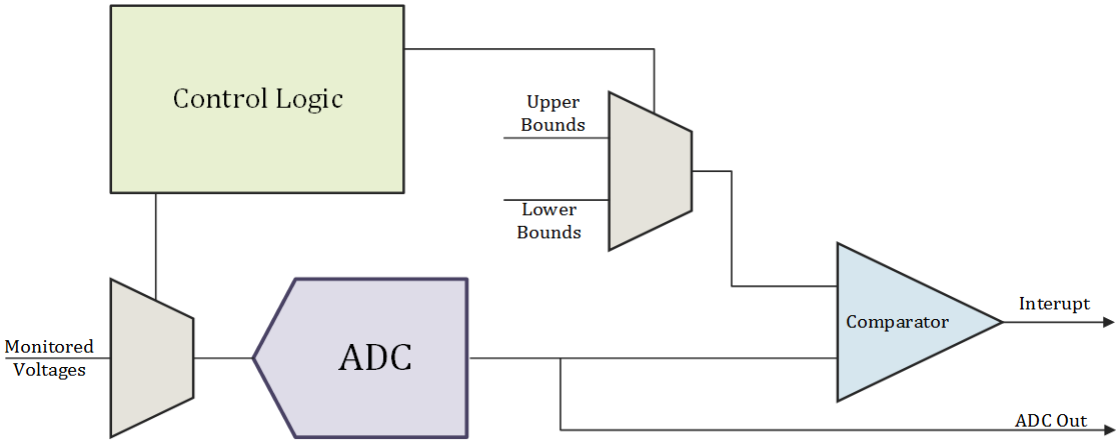

Figure 1: Monitoring System Application

In the block diagram, presented in Figure 1, the voltages are connected to the input of the ADC. The control logic regulates which mux channel will be selected to be compared to the correct upper and lower bounds. The ADC then converts the analog voltage to a digital output. The comparator checks the digital output against the acceptable upper and lower bounds. If the digital code is higher or lower than these regions the interrupt signal is triggered and the board may go into shutdown mode [1] [2].

For this type of application, the ADC must be fast and accurate up to at least 5-bits. In order to achieve accuracy, the ADC should minimize two important parameters. The first is offset and the second is gain error. These two parameters will aid in a more accurate ADC.

Offset refers to how well the ideal and real transfer functions match at a single point (the y-intercept). While, gain error refers to how well the slopes of the real and ideal transfer functions match. Figure 2, provided in the application note by Maxim [3], shows a diagram of the difference between offset and gain error and how each is defined. As the figure shows, the measured ADC curve has a different slope and y-intercept.

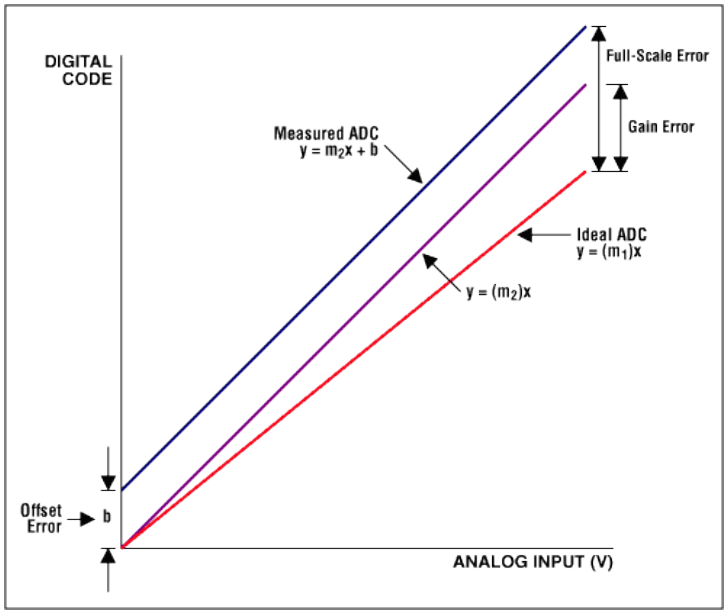

Figure 2: Offset and Gain Error

These errors are caused by multiple sources which include amplifier offset, charge injection, and clock feedthrough. Charge injection and clock feedthrough are reduced by using a four phase non-overlapping clock circuitry in switched capacitor (SC) circuitry. A non-overlapping clock circuitry ensures that the two phases of the clock are not on at the same time. Therefore, the main source of offset and gain error is caused by limitations in the amplifier such as bandwidth, offset, and noise [4].

Reducing gain error and offset are goals for any stand-alone or embedded ADCs designed for this application. In this thesis, the ADC is designed for a FPGA board (embedded system), meaning that there are more difficulties that must be accounted and designed for.

High quality ADCs can be fairly simple to implement as a stand-alone device. The problem arises when they are embedded for several reasons. One of these reasons is because stand-alone devices do not use the most current technology [5] [6] [7]. They are often several generations behind since larger widths and higher power supply voltages are more advantageous for analog design. However, for embedded designs, the technology isn't chosen to be a good fit for the analog circuitry [5]. Most of the circuitry in an embedded design is digital meaning the technology should be the latest process. This in turn makes the analog circuitry harder to design [6] [7]. Another problem with ADCs in general is that they are designed for either high precision or high speed. Most ADCs are not multi-purpose. This creates problems within FPGA boards where the ADC is used for security monitoring, where high speed is desired, and a precise voltage application, where high precision is more desirable. In order to get the same effective number of bits (ENOB) as a stand-alone ADC, embedded ADCs usually have more resolution to take into account the smaller technology sizing and other limiting factors [5].

In this thesis, three calibration techniques are used to adjust for offset and gain error. First, a correlated double sampling (CDS) integrator is used as the first stage of the delta-sigma modulator. The second calibration method is an auto-calibration technique to adjustment the common mode voltage which aid in the correction of gain error. The third calibration technique, is the auto-zero calibration. This calibration reduces offset by storing the value into a register for later use. These three calibration techniques will be explored in more depth in the next chapters.

Thesis Outline

Chapter 2 goes over the previous solutions to resolve offset and gain error problems, FinFET basics and challenges, and design specifications of the ADC. Chapter 3 discusses the implementation of the ADC at a system level, including a MATLAB model

and results. Chapter 4 reviews the schematic design and explains the new calibration circuitry that was implemented. Chapter 5 provides the results and simulations of the ADC including pre-and post-layout simulations. Lastly, chapter 6 addresses the conclusions and future work of offset and gain error correction.

CHAPTER 2

BACKGROUND

Previous Work

For any ADC, the accuracy is an important factor. As described in the previous chapter, the accuracy is dependent on errors in the ADC including offset and gain error. Other techniques to reduce offset and gain error have been accomplished. Many have used a common circuit used in discrete time ADCs, the CDS integrator [8]. A basic CDS integrator is shown in Figure 3 [9] [10].

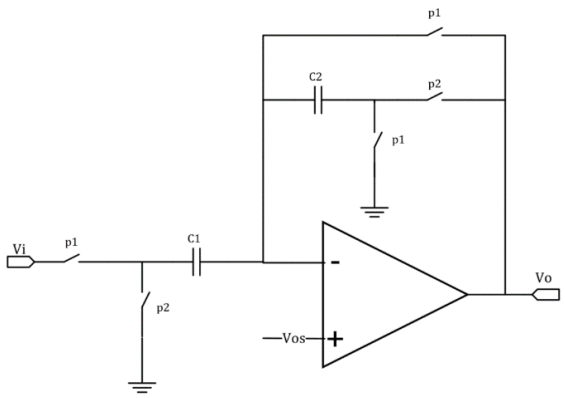

Figure 3: Typical CDS Integrator

During phase one, the sum of the charges of the CDS integrator is,

$$\sum Q(p1) = V_i(t-T)C_1 - V_{os}C_1 - V_{os}C_2 \qquad (1)$$

And during phase two, it equals,

$$\sum Q(p2) = -V_{os}C_1 + V_o(t)C_2 - V_{os}C_2 \quad (2)$$

Then setting (1) equal to (2) and taking the z-transform,

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2}z^{-1} \quad (3)$$

Equation (3) shows that by implementing this structure, the offset is sampled onto the capacitor during phase one and then subtracted off during phase two. This circuit is also parasitic insensitive to reduce accuracy errors. Along with a CDS integrator, differential amplifier is usually preferred since it helps eliminates the noise from the parasitic capacitance because of its symmetry [4].

Some have modified a CDS integrator in order to produce better results of offset correction and gain error of the amplifier. One example is provided in Figure 4 [11]. The structure is very similar to the CDS integrator in Figure 3. The problem with the circuit in the figure is that it does not compensate for charge feedthrough which is another reason to use a fully differential amplifier [11].

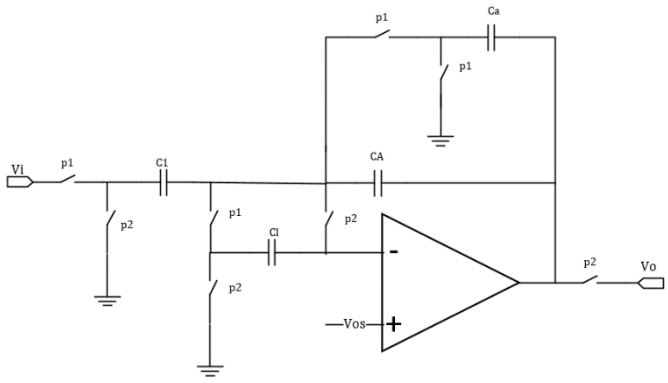

Figure 4: Improved CDS Integrator

For delta-sigma (ΔΣ) ADCs, one technique used to cancel offset and mismatch errors is provided in Figure 5 [12]. The figure shows a digital calibration block diagram. The mismatch in the feedback digital to analog converter (DAC), usually a comparator, are of concern as well as the overall offset of the ΔΣ modulator.

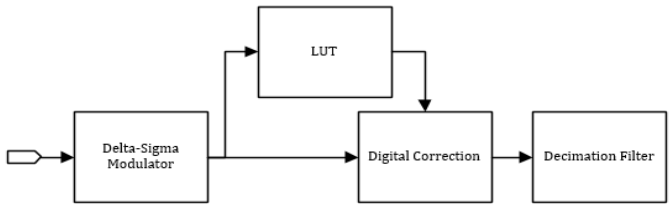

Figure 5: Digital Calibration Correction

With this scheme, the modulator goes through a calibration phase on power up. During this phase, the modulator error is stored into a LUT and subtracted out via the digital correction block. Then, the output goes through the decimation filter to output the digital value. The correction circuitry uses a look-up table (LUT) to store the DAC error based on the DAC input code [12]. With this methodology, any offset or mismatch errors, in the form of offset, are subtracted out to employ a more accurate ADC.

Several calibration techniques have been implemented in the digital domain that correct for offset or gain error. One example of this is shown by the patent algorithm in Figure 6 [13]. In the figure, the blue box is the algorithm to produce the digital result. Once the digital result is found, it is multiplied by a gain error trim coefficient. This coefficient is found after several tests [13].

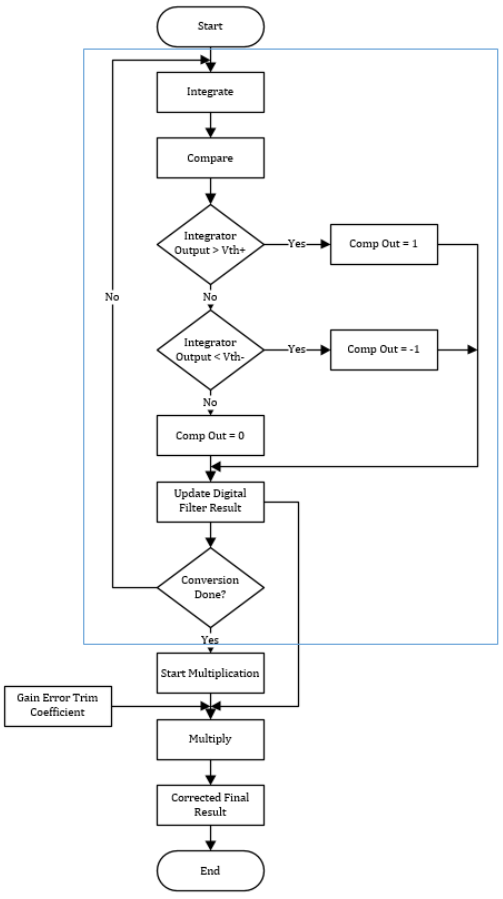

Figure 6: Algorithm for Gain Error Correction

FinFET Technology

Fin-shaped field effect transistors (FinFET) were first created during 1998 and 1999 for NMOS and PMOS transistors, respectively [16] [17]. These devices decrease power consumption, operate at a lower voltage, have a higher operating speed, and less static gate leakage current at the cost of other undesirable effects such as electromigration (EM), current density, aging, self-heat and layout effects [18]. A cross-section of a standard planar silicon-on-insulator (SOI) metal oxide field effect transistor (MOSFET) device and a FinFET device is shown in Figure 7. The main difference, appearance-wise, between the two drawings is the source and drain of the FinFET devices extend higher in the z-axis, which creates the "fins", and the gate now controls the current flow from three-sides.

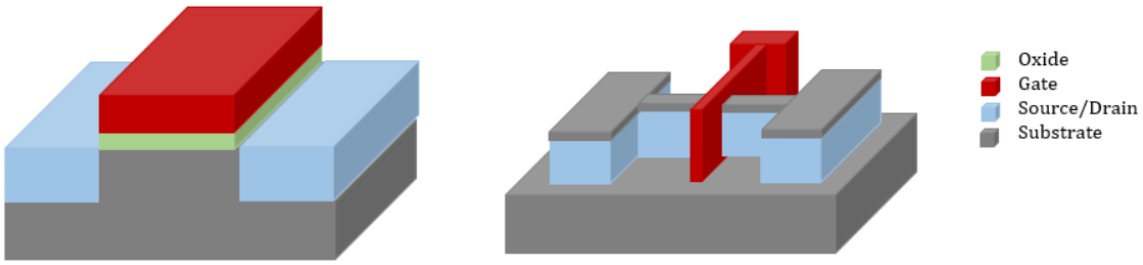

Figure 7: MOSFET (left) and FinFET (right) cross-sections

FinFETs operate similarly to MOSFETs. In simple terms, the gate controls how much current can flow between the source and the drain. Therefore, the small signal [18] model used for MOSFETs apply to FinFET devices. The small signal model of a FinFET device from [18] is shown in Figure 8. As provided in the figure, intrinsic depends on the bias conditions and dimensions while the extrinsic are independent of them. A more simple, classic, model is shown in Figure 9. The analysis of a FinFET is the same process and equations as a MOSFET. But with FinFET devices some parameters are higher or lower which affect the overall performance of the device when designing analog circuits [18].

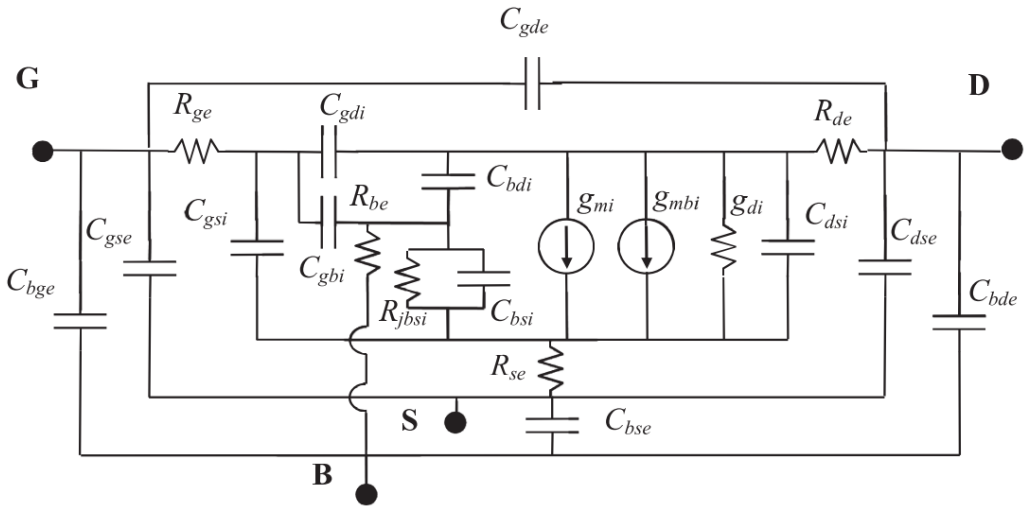

Figure 8: Small-signal model of a three-port device (provided in the paper by J. Raskin [18])

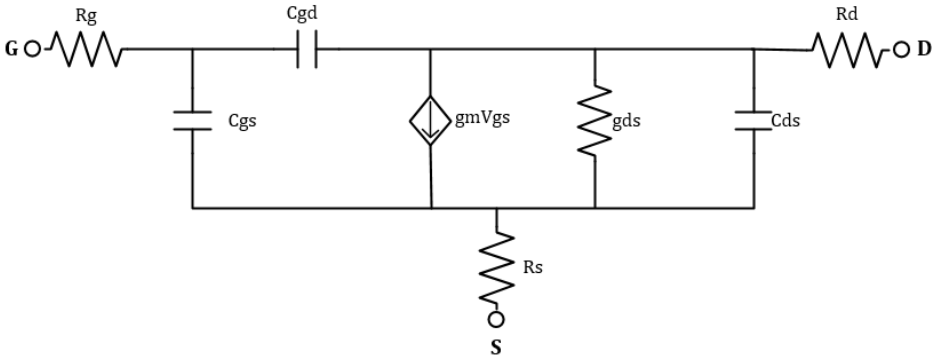

Figure 9: Simple Small-Signal Model

Performing the small signal analysis, the f_t of the FinFET transistor is the same as a MOSFET,

$$f_t = \frac{f_c}{\left(1+\frac{C_{gd}}{C_{gs}}\right)+(R_s+R_d)\left(\frac{C_{gd}}{C_{gs}}(g_m+g_{ds})+g_{ds}\right)} \quad (4)$$

Where,

$$f_c = \frac{g_m}{2\pi C_{gs}} \quad (5)$$

Ignoring the impact of the parasitics, g_m is proportional to W/L but C_{gs} is related to W×L which means that f_t is dependent on L changes but essentially independent on W changes. Therefore, with decreasing lengths the current gain cutoff frequency increases [18]. This is consistent with MOSFET analysis. The difference between the FinFET and MOSFET

varies with the extrinsic cutoff frequencies where the fringe capacitance affects FinFET device. This fringe capacitance is proportional to height of the fin to width of the fin ratio, extension of the source and drain fins, and the spacing between each of the fins [18]. Increasing the ratio and decreasing extension of the fins and fin spacing increases the extrinsic cutoff frequency [18].

FinFETs have some similar problems than MOSFETs but are more prominent with smaller technology sizing. The main problems with these FinFET devices are aging concerns, self-heat, current density, electromigration, resistance of metals, and layout effects. There are two aging phenomenon's present in FinFETs: hot carrier injection (HCI) and negative/positive bias temperature instability (NBTI/PBTI). Both of these problems effect devices by decreasing the drain current saturation.

Self-heat is another problem in FinFETs which is caused to the increase in current density. The current density is increased because of the increase in the height of the fin. Since with smaller devices the power increases, the active area is now increased causing greater impacts of self-heat [18].

EM is an issue for design when the current density is high. With smaller technology sizes, the current density is higher and therefore degrading the metal. This is a reliability issue with FinFETs so provided the correct number of tracks is important. Another problem with the metal is that lower level metals are thinner and more resistive so having as many tracks as possible is important in design. Other layout effects include length of diffusion and well proximity. These are usually solved by added multiple dummies to the transistors.

Design Specifications and Considerations

The specifications of this ADC are shown in the table below. For the high-speed application, the most important parameters are the sampling speed and the ENOB. For

voltage monitoring, a minimum of 5-bits and 1Msps is needed to detect a hacking event, i.e. voltage droop in the supply.

Parameter	**Goal**	
	Precision	High Speed
Resolution	12-bits	
ENOB	10	≥5
Conversion Rate	140ksps	1Msps
SNDR	≥62dB	≥32dB
V_{in} Range	0-1.2V	
V_{ref} Range	0-1.2V	
Clock Frequency	≤500MHz	

Table 1: Design Goals

The op-amp and switched capacitor integrator (SCI) in a ΔΣ modulator must be carefully designed in order to accomplish the correct bandwidth (to decrease gain error) as well as minimize offset. Finding the bandwidth of the op amp can be accomplished by using the curve shown in Figure 8.

In the figure, is a step response input with the output settling of a single pole response. The higher the gain the closer it settles to the correct value, less noise, and accuracy problems. From this plot,

$$e^{-\frac{t}{\tau}} = \frac{1}{2^N} \qquad (6)$$

$$t = -\tau \times \ln\left(\frac{1}{2^N}\right) \qquad (7)$$

For 12-bits,

$$t \approx 8.3\tau \qquad (8)$$

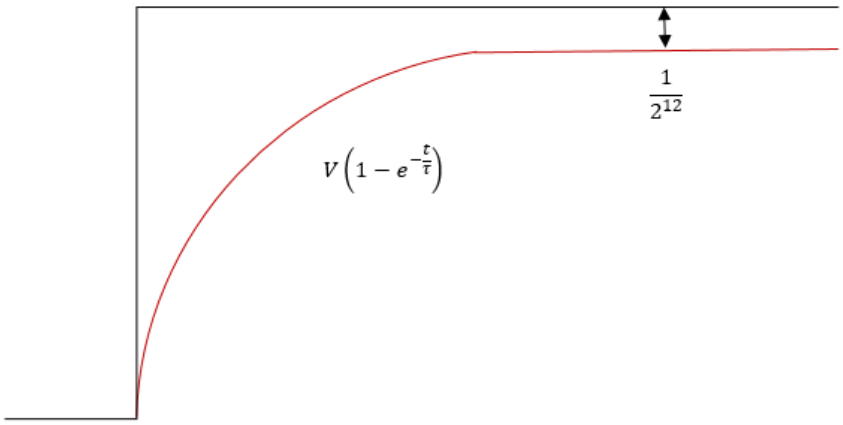

Figure 10: Settling Time Response of Step Input

Then,

$$t \approx \frac{1}{2} \times \frac{1}{f_s} \qquad (9)$$

Therefore,

$$\tau \approx \frac{\left(\frac{1}{2f_s}\right)}{8.3} \approx \frac{1}{16.6f_s} \qquad (10)$$

The amplifier should settle within the $1/16.6f_s$ in order to reduce errors of the ΔΣ [14]. The unity gain frequency can be computed as,

$$UGF = \frac{1}{\tau} \times \frac{A_{cl}}{2\pi} \quad (11)$$

Where A_{cl} is the closed loop gain. These equations will become important in the design of the amplifier used in the SCI circuits.

CHAPTER 3

SYSTEM LEVEL DESIGN

Figure 9 shows the system level design of the 2nd order ΔΣ ADC. ΔΣ ADCs are a type of oversampled ADC that provides high resolution at a relatively low cost but lower speed. The main advantage of a ΔΣ ADC is that the analog circuitry is not as stringent on matching tolerances or amplifier gains. This means more complex digital circuitry but less area [14]. When switched-capacitor circuitry is used, the matching tolerances are even

more relaxed because the accuracy does not depend on it [4]. The advantage of having a higher order modulator is they provide a greater amount of noise shaping. Going from a 1st order modulator to a 2nd order modulator provides 15dB increase in SNR. But this is at the cost of stability. When there are several integrators with feedback the circuits become harder to stabilize [4].

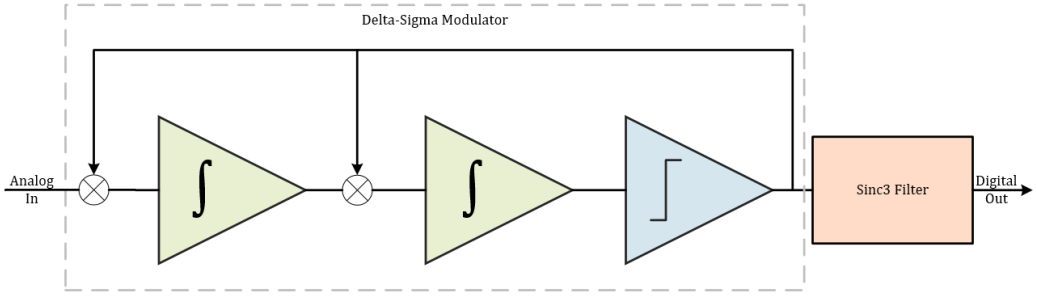

Figure 11: ADC Block Diagram

Before designing a 2nd-order modulator on the transistor level, a MATLAB model, shown in Figure 10, was created to simulate various plots important to ΔΣ modulators. Knowing the ENOB, the ideal signal to noise ratio (SNR) value can be computed (for 12-bits),

$$SNR = ENOB \times 6.02 + 1.76dB = 74dB \qquad (10)$$

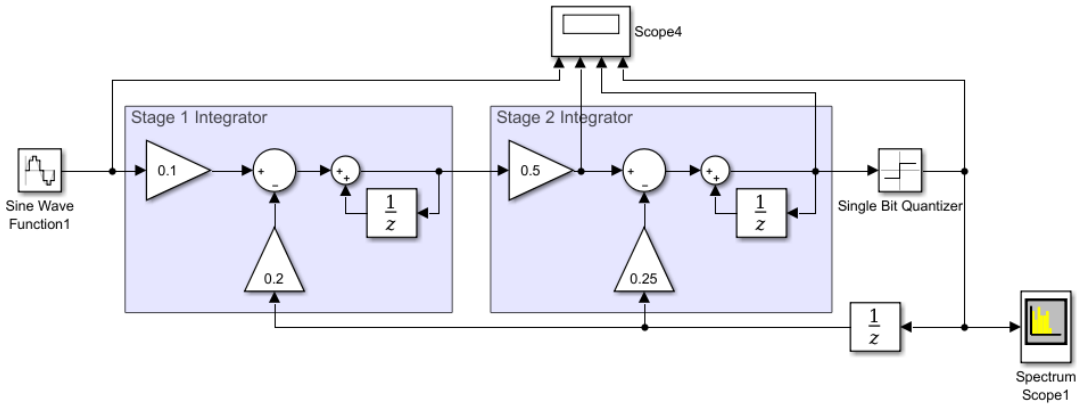

Figure 12: MATLAB Model of a 2nd Order ΔΣ Modulator

With a sampling frequency, f_s, and knowing the design has a resolution of 12-bits, the frequency of the slow sine wave can be computed as,

$$f_{sine} = f_s/2^{12} \quad (12)$$

The filter cutoff frequency, f_c, is determined by,

$$f_c = f_s/decimate \qquad (13)$$

Then, choosing a sampling frequency of 128MHz (approximately half of the maximum clock), the integrator gain can be tweaked to achieve an SNR of 74dB. Figure 11 shows the FFT for the modulator. The modulator bit stream is shown in Figure 12 and the outputs of each stage are shown in Figure 13.

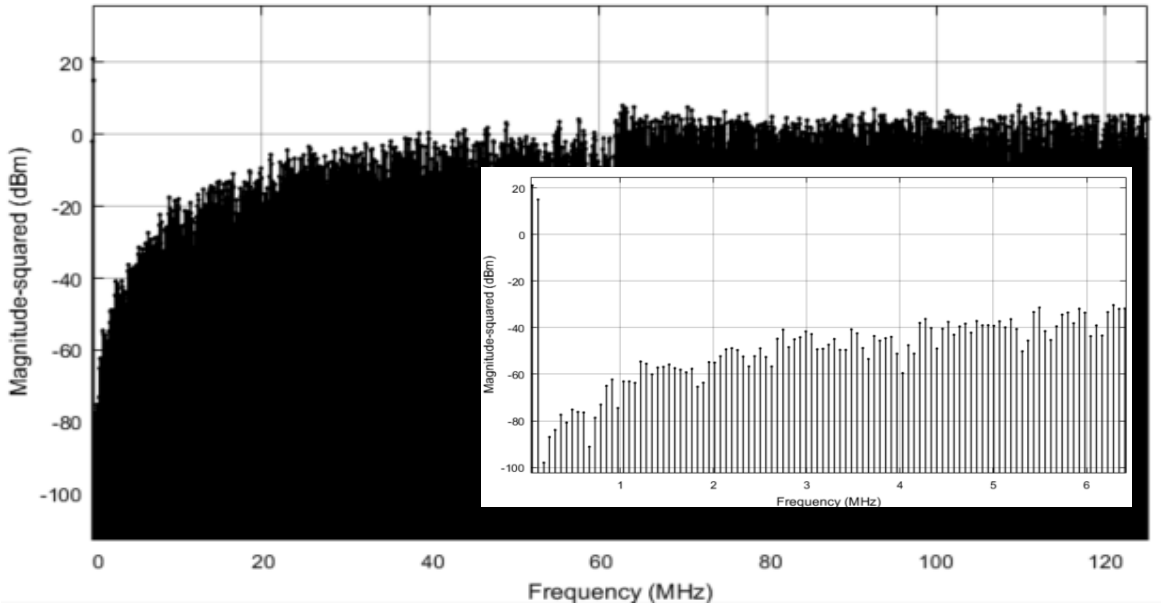

Figure 13: MATLAB FFT Plot for 128MHz

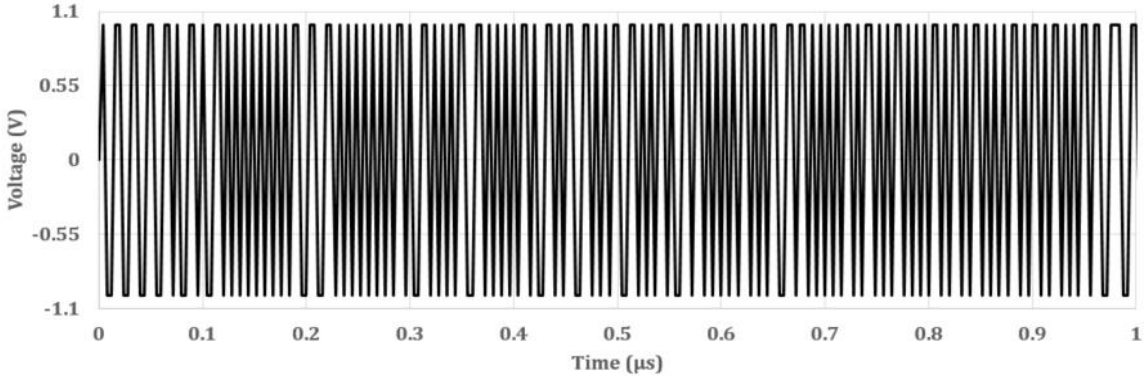

Figure 14: Modulator Output Zoomed In from 0 to 1μs

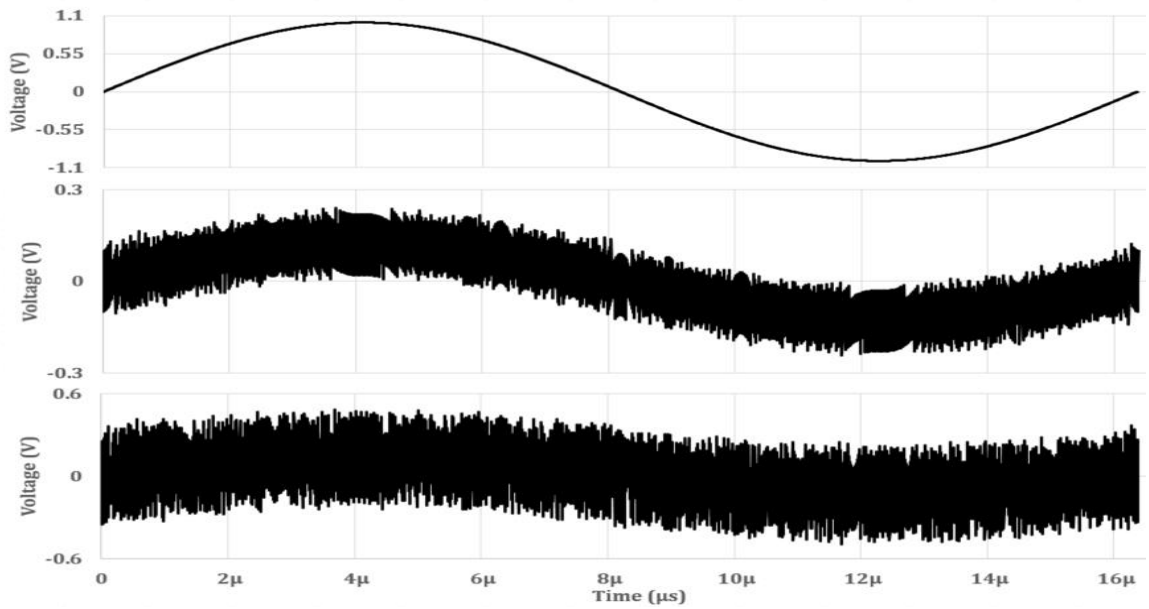

Figure 15: Plot of Integrator Outputs

Figure 14 shows the conversion rate at different sampling frequencies and decimate values. As provided in the graph, a decimate of 16 with a sampling frequency of ≥110MHz and a decimate of 32 with a sampling frequency of 250MHz should provide a ~1MSPS conversion rate.

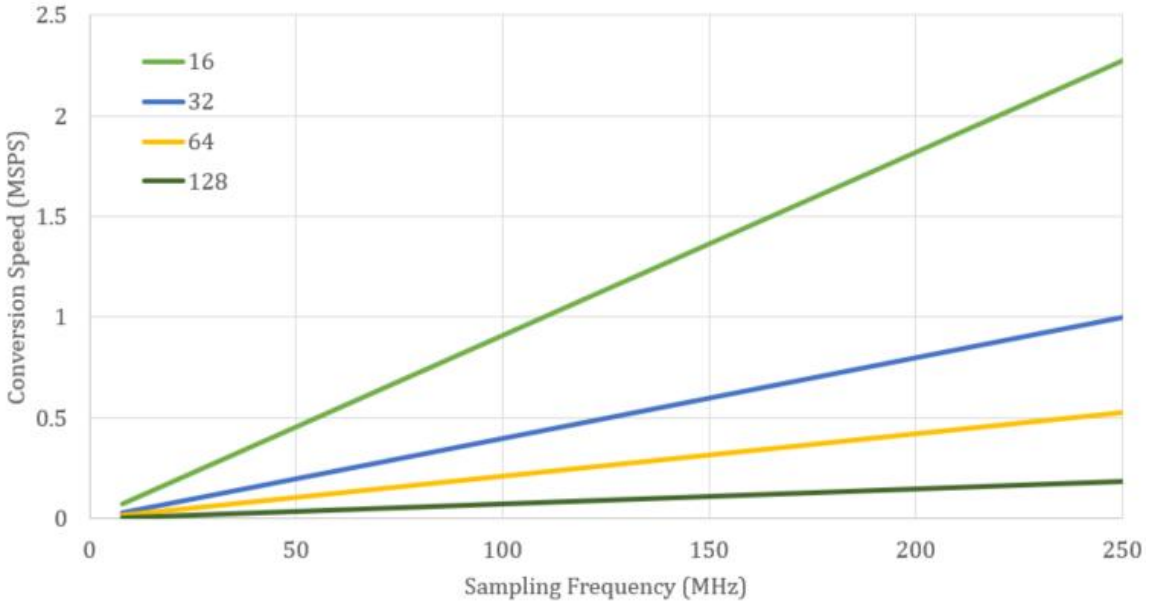

Figure 16: Sampling Frequency vs Conversion Rate at Various Decimates

With equation (12), the over sampling ratio (OSR) is calculated,

$$OSR = (f_s/2)/f_c = decimate/2 \qquad (14)$$

This means that the OSR is independent of the sampling frequency. The sampling frequency is critical to the conversion rate. In order to achieve a conversion rate of >1MSPS either the frequency must increase or the decimate must decrease.

Figure 15 shows the SNR, ENOB and OSR versus decimate values. The decimate values determine the cutoff frequency of the filter. This helps determine the OSR needed for a 5-bit ADC.

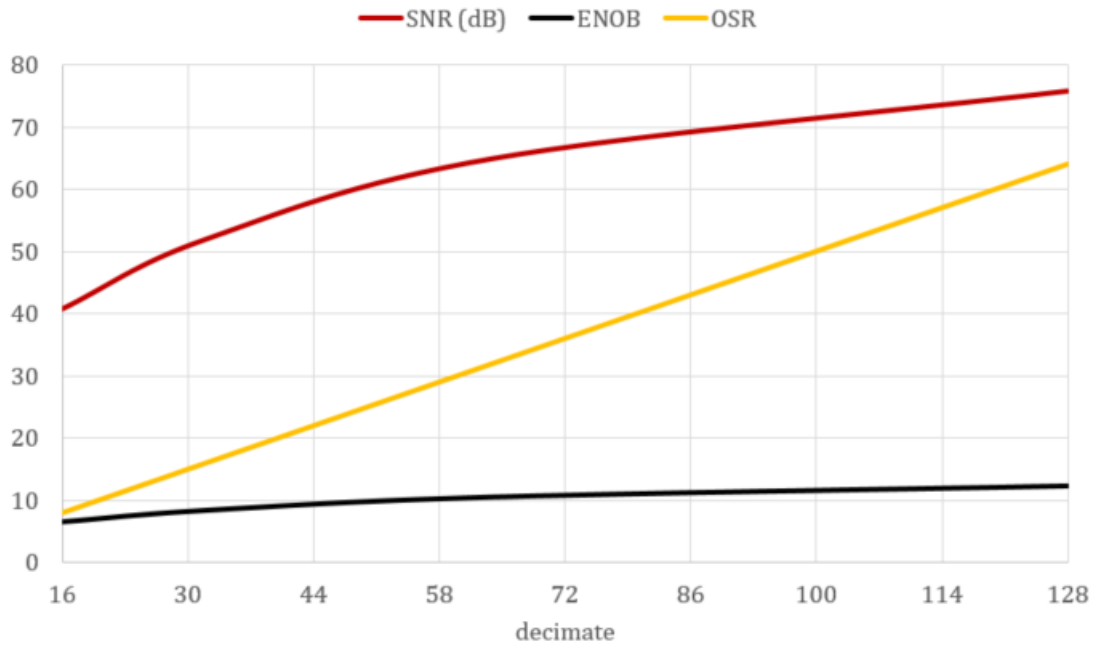

Figure 17: Decimate vs SNR, ENOB and OSR

The system level design helps to determine the variables of the ΔΣ to design it at the transistor level. The calibration techniques will be explored in the schematic implementation. With these pre-design simulations, the ΔΣ modulator with calibration can be implemented on a transistor level.

CHAPTER 4

SCHEMATIC IMPLEMENTATION

Top-Level ADC

Figure 16 shows the top-level block diagram of the ADC. As shown in the figure, there are four parts to the ADC, the ΔΣ, the bias generator, the sinc3 filter and the controller. First, the ΔΣ schematics will be shown, followed by the bias generator circuitry for the calibration and then the auto-calibration and auto-zero power on calibration will be explained.

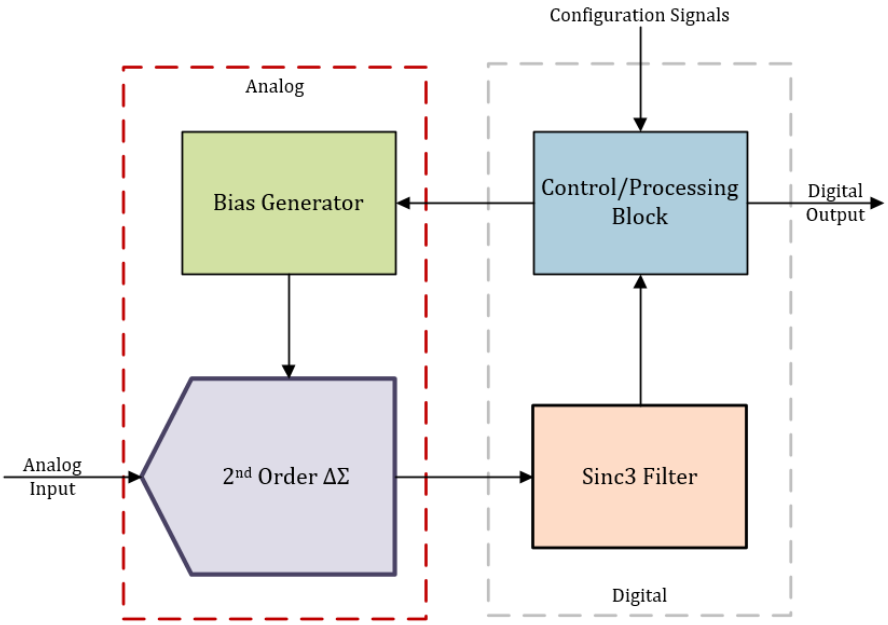

Figure 18: Top-Level ADC

2nd Order Delta-Sigma Modulator

The first stage of the ΔΣ is an integrator implemented using the CDS technique. The schematic is provided in Figure 17. This is one calibration technique used to enable more accurate results, i.e. lower offset. As explained in the previous chapters, the CDS integrator samples the offset on the capacitor connected to the input of the amplifier during phase 2. During phase one the integrator is in evaluate mode where it subtracts the offset that was sampled during phase two.

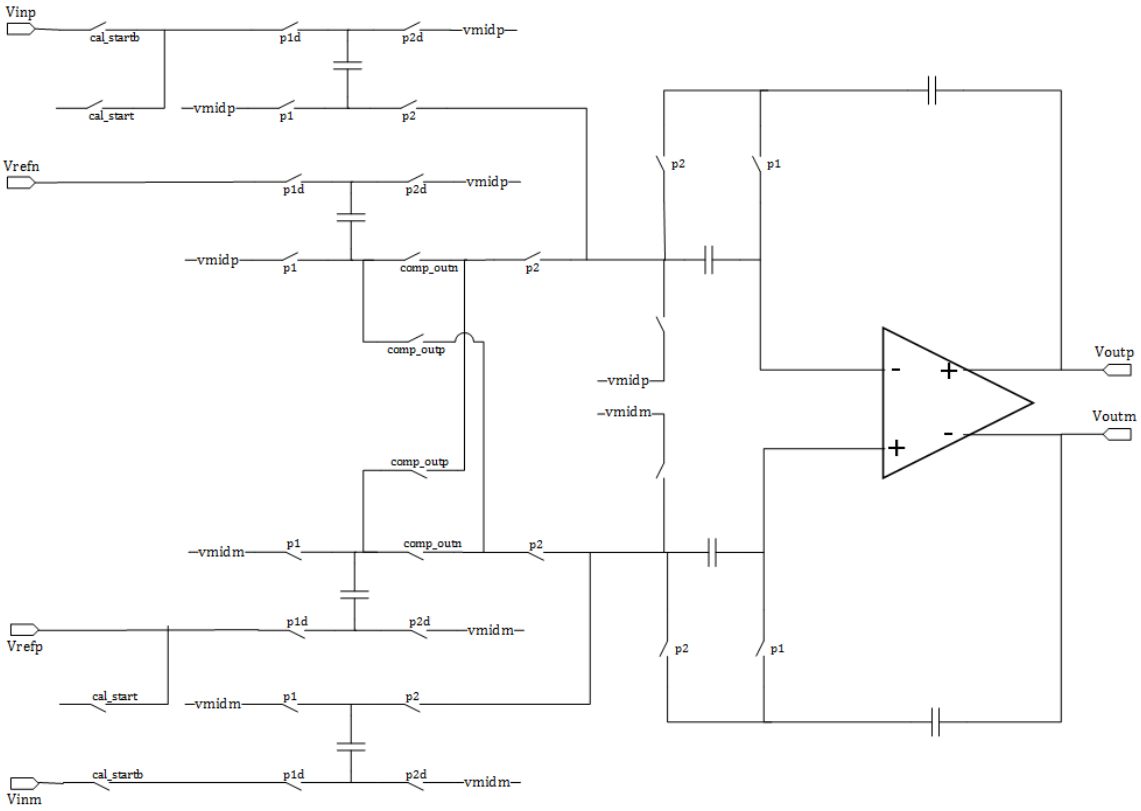

Figure 19: 1st Stage Integrator

The major contribution to noise and limiting factor of the maximum SNR is the thermal (kT/C) noise of the input capacitors of the first stage. This noise can be reduced by increasing the OSR of the modulator, using a larger input voltage range, and increasing the capacitor size. The maximum SNR is computed as,

$$SNR_{max} = 10\log\left(\frac{S_i^2}{N_i^2}\right) + 10\log(OSR) \quad (15)$$

Where, S_i^2 is the input signal power and N_i^2 is the noise power which are computed by the equations below.

$$N_i^2 = 2\times\frac{kT}{C_{in}} \quad (16)$$

$$S_i^2 = V_{rms}^2 \quad (17)$$

The second stage is an SCI which is shown in Figure 18. The second stage sample phase is during phase two and the evaluate phase is during phase one, just like the first stage. Because the 2nd order modulator is inherently unstable, the capacitor ratios should be optimized in order to stabilize the modulator and to maximize the signal swing which helps increase the SNR. The ratios of the capacitors (i.e. integrator gain) were optimized as provided in the table below.

	Stage 1	Stage 2
Cin/Cfb	0.1	0.5
Cref/Cfb	0.2	0.25

Table 2: Integrator Gain Values

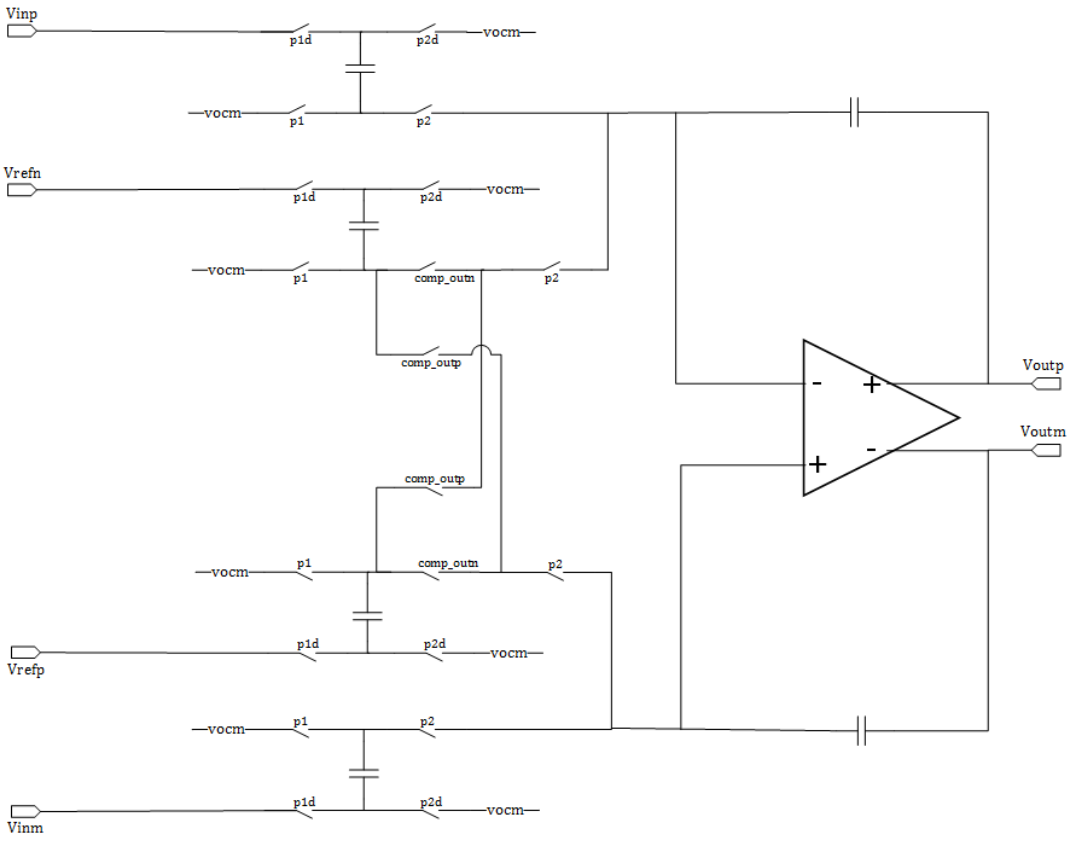

Figure 20: 2nd Stage Integrator

Both the first stage and second stage integrators include a fully differential folded cascode amplifier with PMOS inputs (shown in Figure 19), SC CMFB circuitry (shown in Figure 20) and use a four-phase non-overlapping clock which is shown in Figure 21.

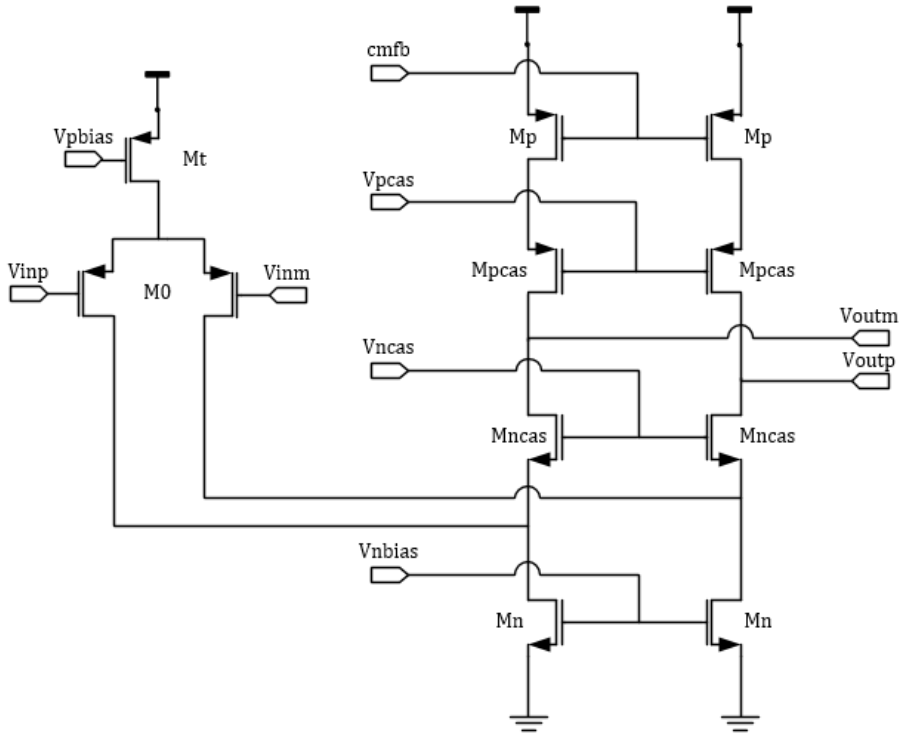

Figure 21: Single Stage Fully Differential Folded Cascode Amplifier

The cascode amplifier is a single stage PMOS amplifier chosen for its ability to be easily stabilized, robustness, and simplicity. The amplifier's main pole is at the output nodes which is calculated by [14],

$$\omega_{p1} = \frac{1}{C_L R_o} \qquad (17)$$

Where C_L is the load capacitor and R_o is the resistance at the output node which is computed as follows [14],

$$R_o = \left(gm_{pcas} r_{pcas} r_p\right) || \left(gm_{ncas} r_{ncas} (r_n || r_o)\right) \quad (18)$$

The DC gain of the amplifier is [9],

$$A_v = gm_0 R_o \quad (19)$$

Where gm_o is the transconductance of the input transistor.

The CMFB circuitry shown in Figure 20 is a standard switched capacitor common mode feedback circuit. The circuitry allows the two outputs to be centered around a specified voltage [4].

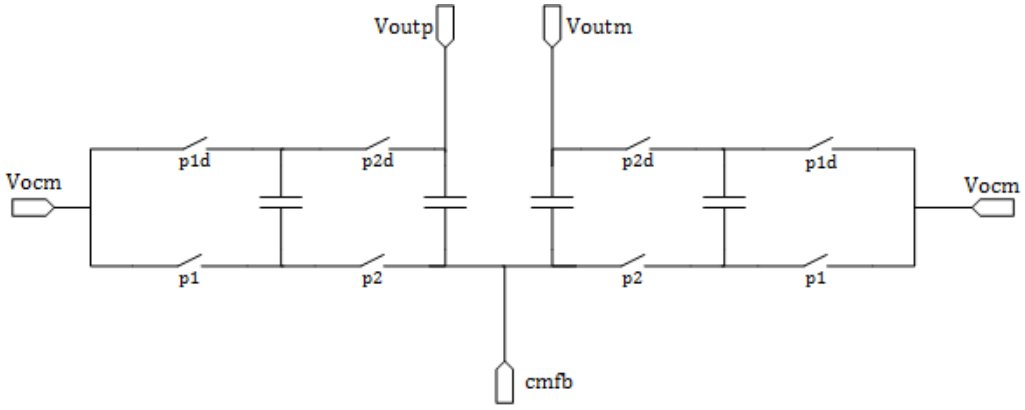

Figure 22: CMFB Circuitry

The four phase non-overlapping clock circuitry is essential for two reason clock feedthrough and charge injection. These two issues can affect the overall accuracy of the ADC. While a switch is trying to pass a value, the value before and after the switch is not the same. These errors are caused by charge injection and clock feedthrough. So, to minimize this, a four phase non-overlapping clock circuitry is used, shown in Figure 21 [14] [15].

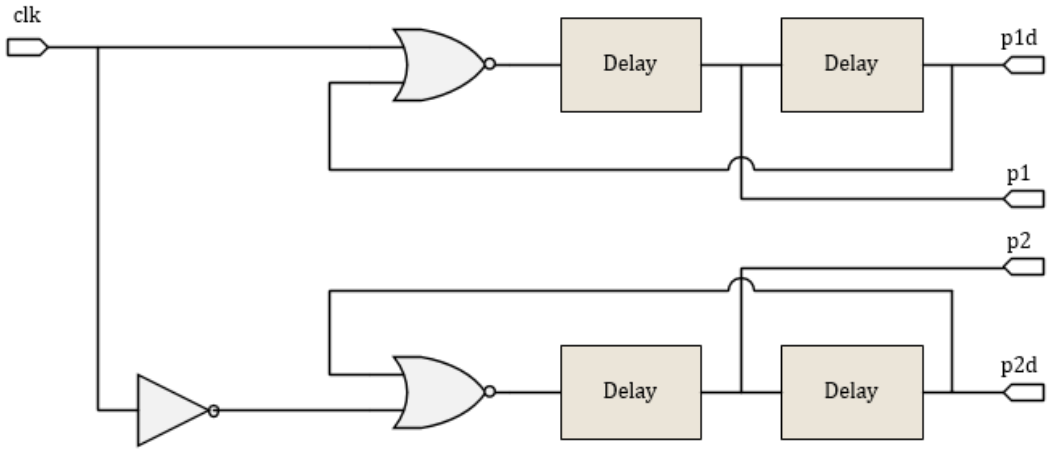

Figure 23: 4 Phase Non-Overlapping Clock

The third stage of the modulator is a 1-bit quantizer or a latched comparator. The comparator design is provided in Figure 22 [15]. This comparator is a fully differential comparator. It compares the positive and negative outputs of the second stage and outputs a one or a zero depending if the positive is greater than or less than the negative. The SR latch of the comparator holds the output when in phase two.

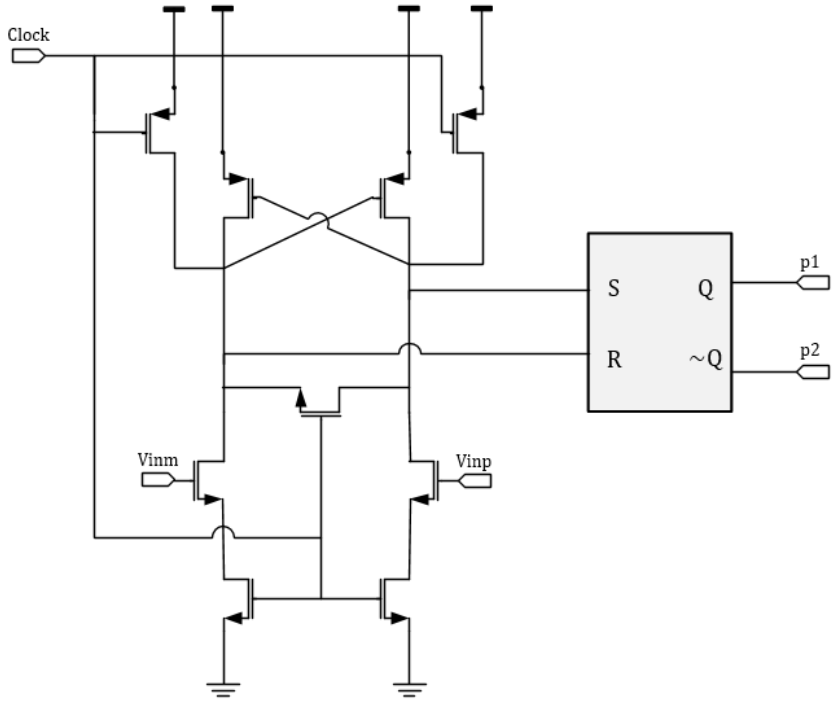

Figure 24: Latched Comparator

Calibration

Two additional calibration techniques implemented in the design are the power on common mode voltage trim and the auto zero calibration. The power on common mode voltage trim is implemented using analog circuitry as well as a digital controller while the auto zero calibration is main just a digital controller. These two techniques are combined into a Verilog-A code but will be explored individually.

The power on common mode voltage trim schematic is shown in Figure 23. The voltage trim circuitry uses a decoder and resistor divider to adjust the common mode

voltage for the ΔΣ modulator. The control is a four-bit binary number which is controlled and set by the Verilog-A code (described in the next section). With this, the common mode voltage can range from 0.55V to 0.65V for both the positive and negative common mode voltages. Figure 24 shows the Vcm control bits versus the Vcm voltage for both positive and negative common mode voltages.

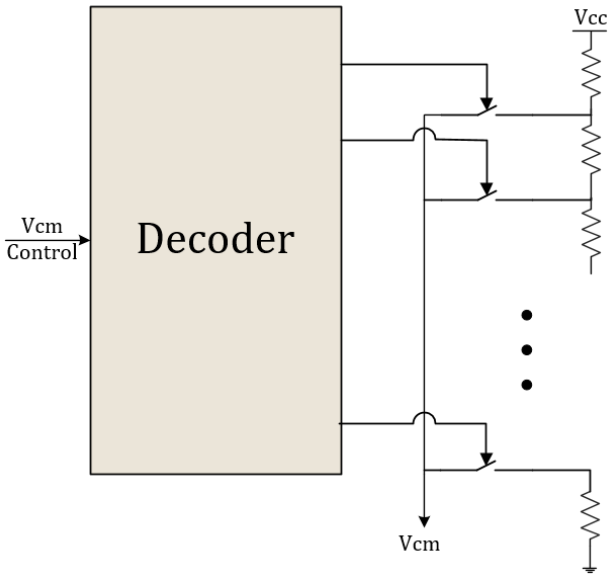

Figure 25: Calibration Circuitry used in the Bias Generator Circuit

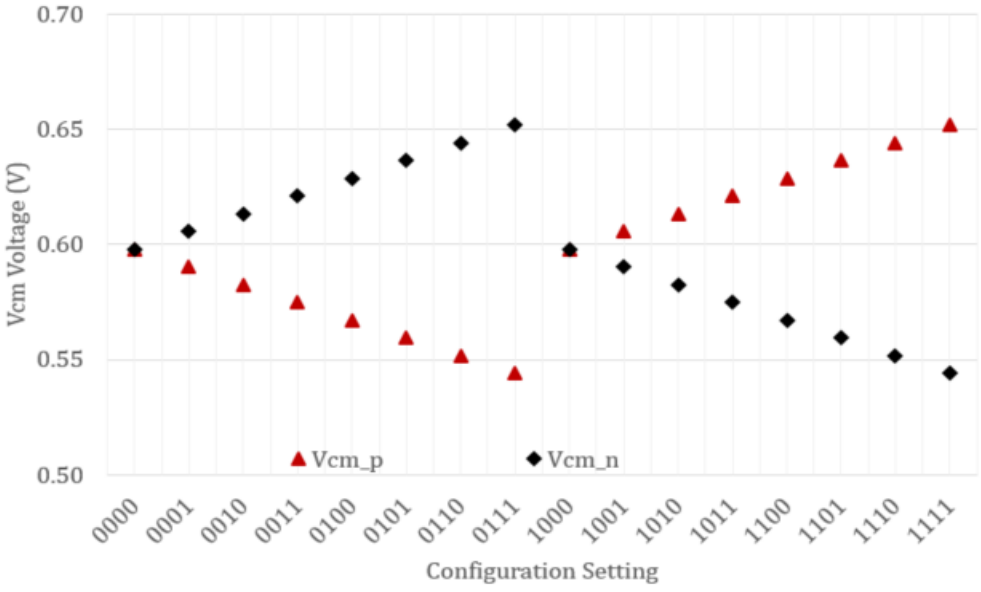

Figure 26: Vcm Control Bit vs Vcm Voltage for Both Vcmp and Vcmn

The second calibration method implemented in the design is the auto-zero calibration sequence. A block diagram of this method is show in Figure 25. This block uses the 2nd order ΔΣ, sinc3 filter and digital register.

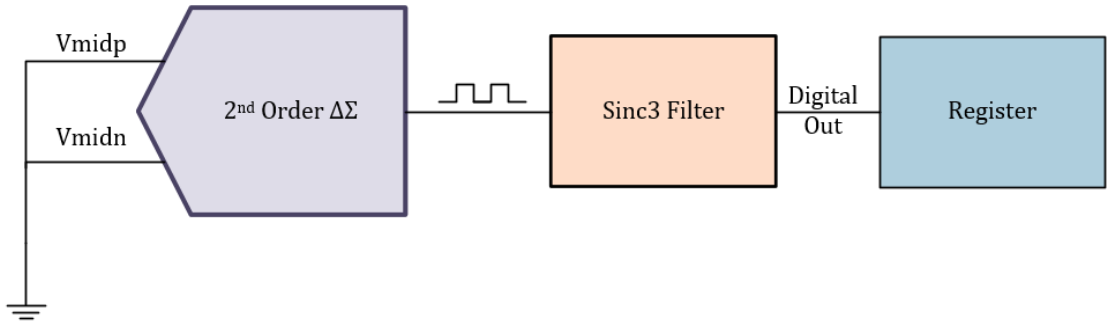

Figure 27: Power-On Calibration

The way this calibration works is first, the two common mode voltages of the ΔΣ are shorted to ground, they could be shorted to any voltage as long as the differential is zero but here ground is chosen. Then, the modulator converts the input to the bit stream which the sinc3 filter interprets into a digital number. This number is then stored into a register. Once the modulator has completed a conversion of an analog input, the output value will be the digital output minus the calibration digital output. Ideally, the calibration bit stream should be alternating ones and zeros which is equivalent to a digital value of zero. This means that if there is some error, meaning the calibrated digital output is not zero, it will be subtracted off the converted value.

Digital Section

The digital component of the ADC is implemented in Verilog-A. The main components of this block are:

1. Sinc3 filter
2. Auto-calibration controller
3. Calibration register

The main clock is divided down in this digital block based on three configurations bits manually specified. The clock can be set to 256MHz or 32MHz where the default is 32MHz. The sinc3 filter also has some options has two configuration bits to specify the decimate value which is essentially a clock divider. The sinc3 filter uses a slower clock than the ΔΣ block.

The power on common mode voltage calibration controller is a part of the Verilog-A code. The way this novel calibration technique works is that it determines the best fit line by adjusting the common mode voltages of the ΔΣ. The steps to this calibration method are as follows. First, the positive input voltage is set to either zero, 0.5V or 1.2V while the negative input voltage is set to zero. Then, the voltage mode control bits are adjusted to the default, 0000. Afterwards, the digital output is computed, via the ΔΣ and sinc3 filter, and stored. This is repeated for all 16 common mode controls and three input voltages. Once all the values are stored for each combination, the slope is computed using a standard slope equation.

$$slope = \frac{N\sum xy - \sum x \sum y}{N\sum x^2 - (\sum x)^2} \quad (20)$$

After computing the slope, error is computed against the ideal value.

$$error = |slope - slope_{ideal}| \quad (21)$$

Then, the slope that is closest to the ideal is the one that will be selected. If there is an offset (i.e. a positive non-zero when the input voltage equals zero), this value is stored in the calibration register to subtract off the offset for each conversion. A diagram of this process is provided in Figure 26. It should be noted that the calibration sets the decimate to the highest value but keeps the clock to the value specified (i.e. either 256MHz or 32MHz). This ensures a more accurate calibration since it allows the common mode voltages to settle and become stable.

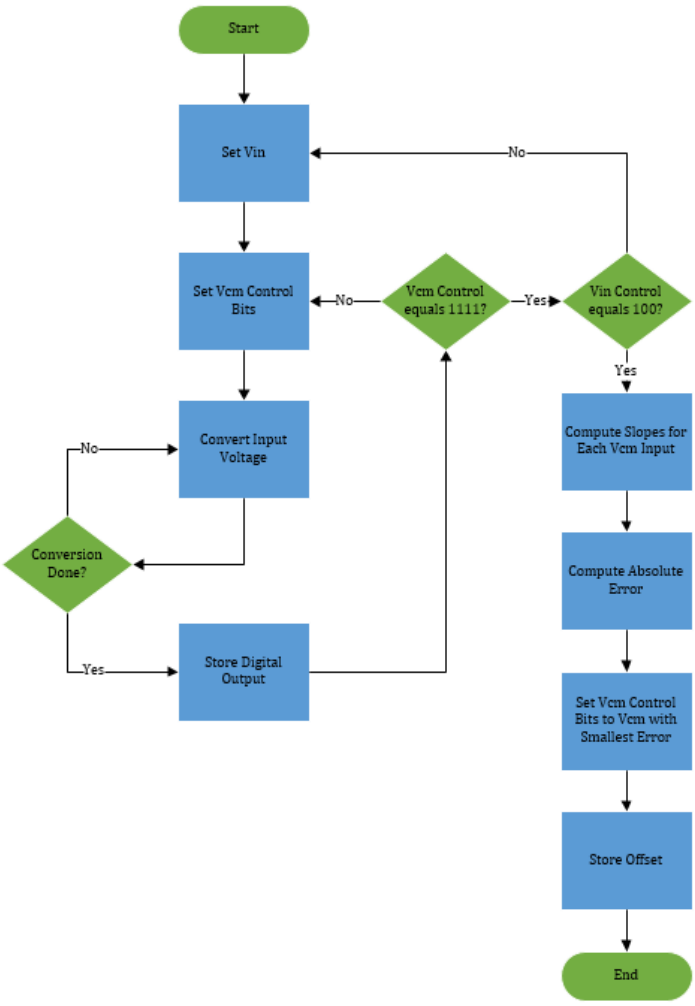

Figure 28: Flowchart of Auto-Calibration Algorithm

CHAPTER 5

RESULTS

Pre-Layout Results

The results for the delta-sigma for the precision application are shown in Figure 27 to Figure 29. As provided in Figure 27, a slow sine wave is injected in order to get the power spectral density plot of the delta-sigma. This figure also shows the modulator output which helps validate that the modulator is working properly.

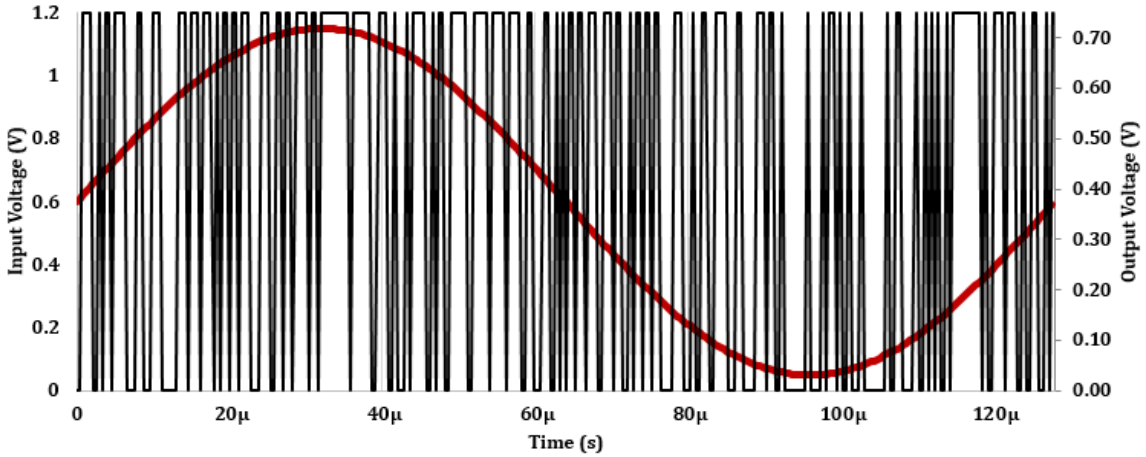

Figure 29: Input Voltage and Modulated Output for 32MHz

Figure 28 shows the first stage and second stage outputs with the slow sine wave inputs. The first stage peak to peak is approximately 0.5V whereas the second stage peak to peak is about 0.3V. This is expected because the input to the first ranges from about 0V to 1.2V while the input of the second stage is a peak to peak of 0.5V. The amplitude is much lower for the second stage so the integrator output has a lower amplitude.

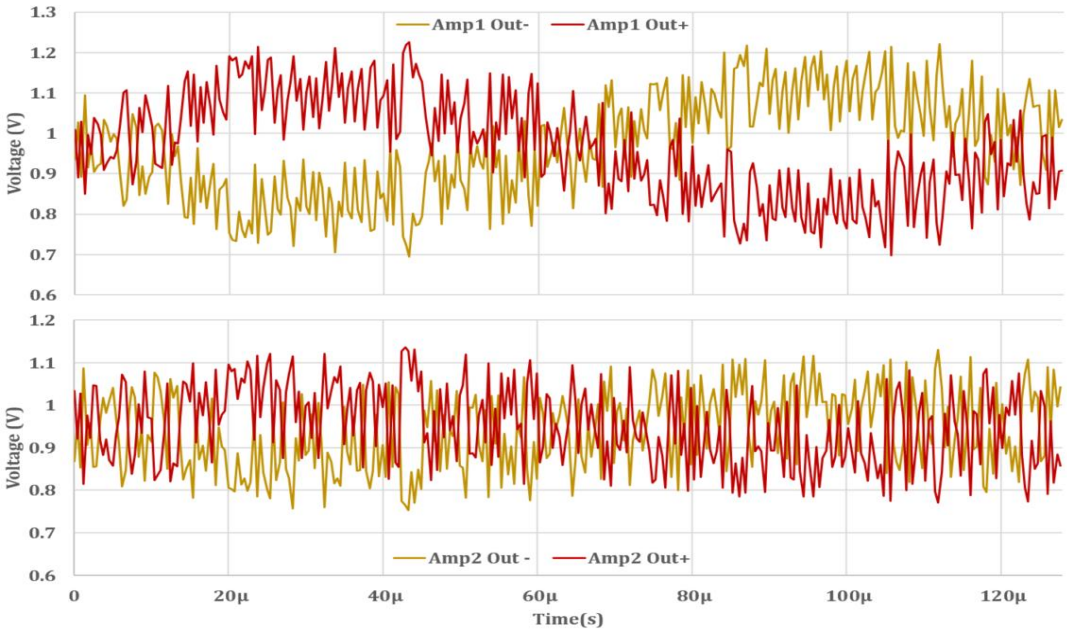

Figure 30: Integrator Output for First Stage and Second Stage for 32MHz

The PSD plot is shown in Figure 29 which includes the full spectrum and a zoomed in plot. The SNR is computed with a decimate value of 128 meaning that the filter cutoff frequency is 250kHz. The measured SNR is the output at the input frequency minus the output value at 250kHz or the highest value below 250kHz. This value is measured to be 76.48dB which is an ENOB of 12.41.

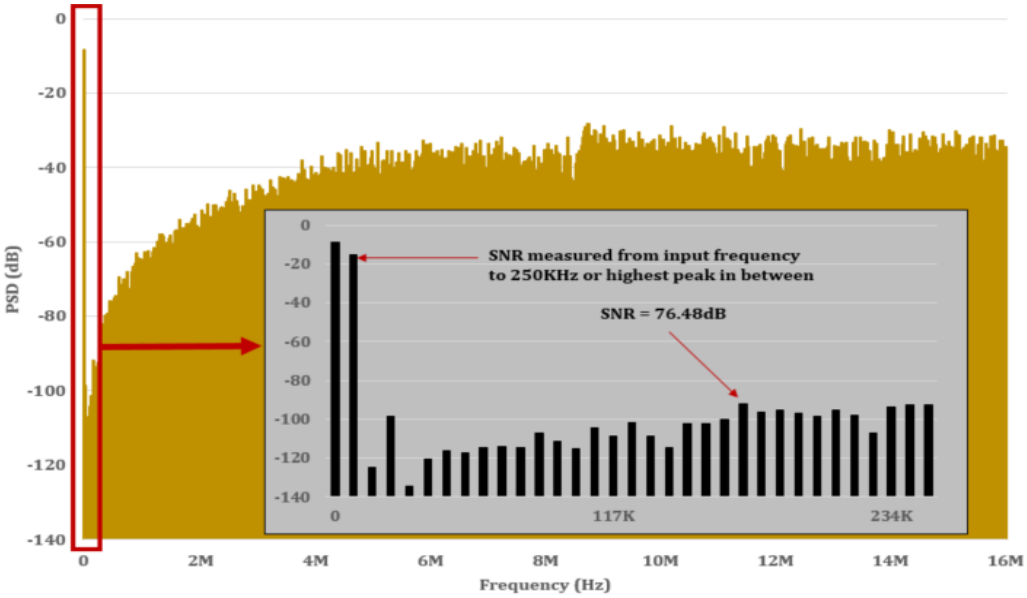

Figure 31: PSD Plot for 32MHz

Similar results are shown for the high-speed application. These results are in Figure 30 to Figure 32 using a decimate of 32. Figure 30 shows the modulator output based on the slow sine wave. Figure 31 shows the first and second stage integrator outputs. The peak to peak value for the first stage output is about 550mV and the second stage is approximately 300mV. These numbers are very similar to the precision application which is at a much lower speed.

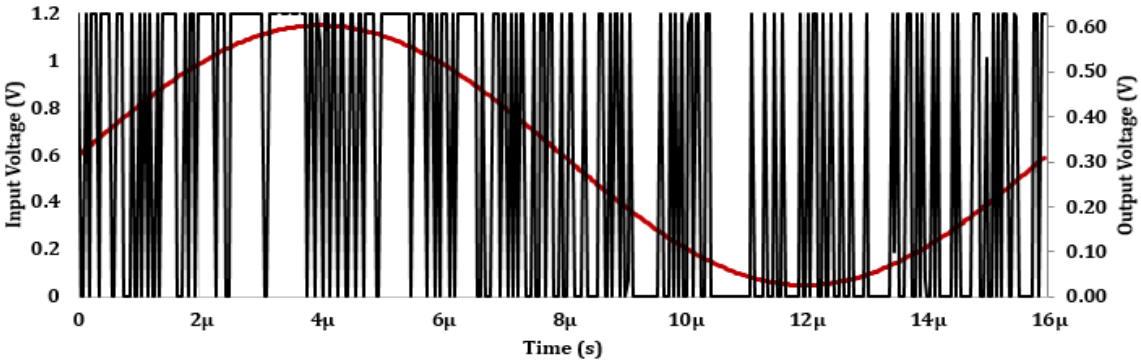

Figure 32: Input Voltage and Modulated Output for 256MHz

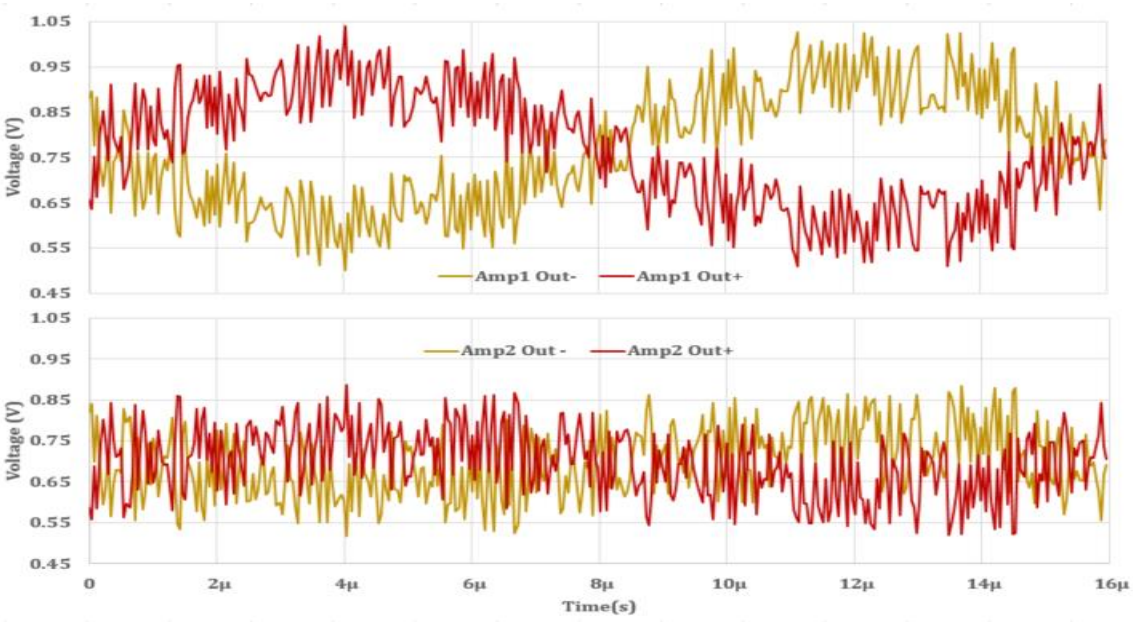

Figure 33: Integrator Output for First and Second Stage for 256MHz

Figure 32 shows the PSD plot for the high-speed application. In the figure, the SNR is measured between the input and the highest peak at or below 8MHz since 256MHz/32 = 8MHz. This is for regular conversion mode. For the calibration mode, the cut off frequency is equal to 256MHz/128 = 2MHz. The accuracy of the converter is increased and the SNR equals 63.2dB, gaining 3-bits of precision.

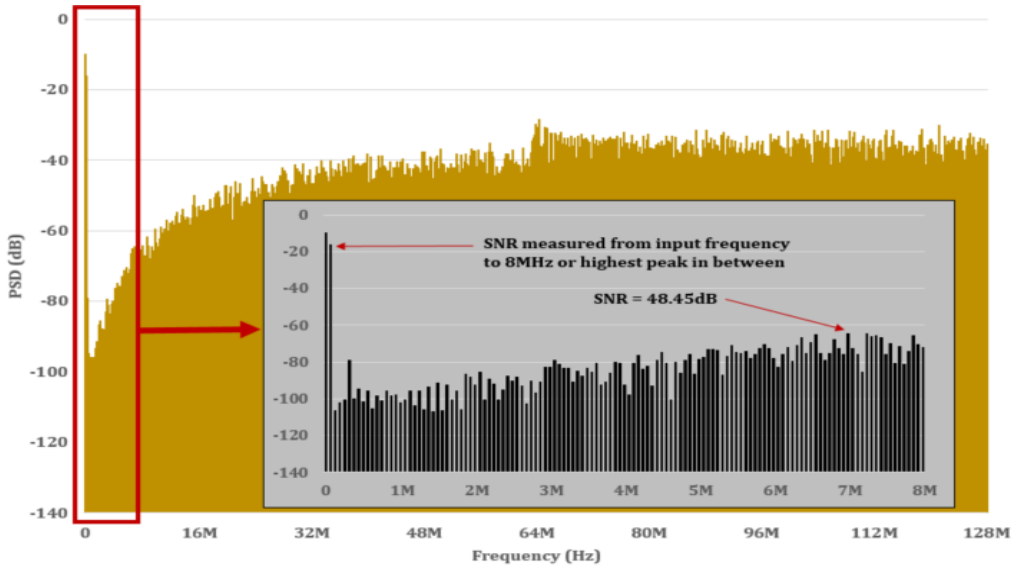

Figure 34: PSD Plot for 256MHz

Figure 33 shows the input vs output plot with two zoomed in spots at the lowest and highest analog voltages. This is to see the deviation between the two applications and the ideal. For both applications, the lines are fairly linear, but it is obvious that there is gain error more so in the high-speed application than in the precision application. One may think that since there is deviation between the actual and real values of the plot that those are caused by quantization errors. But this is not the case. A one bit quantizer is inherently linear since the output can only be a zero or one. Therefore, the cause of these errors is due to other non-idealities in the circuit. Some of these non-idealities include bandwidth error, charge injection in the switches and speed limitations of the differential amplifier.

The calibration results are shown in Figure 34 and 35 for the precision application for the slow and fast corner, respectively. The first plot shows the analog in versus digital output with and without any adjustments of the common mode voltages for the slow corner. As provided in the figure, the default mode has a gain error. The correction line is closer to the ideal slope but there is still some error. The average error for the default and correction for the slow corner is ~0.051% and ~0.048%, respectively.

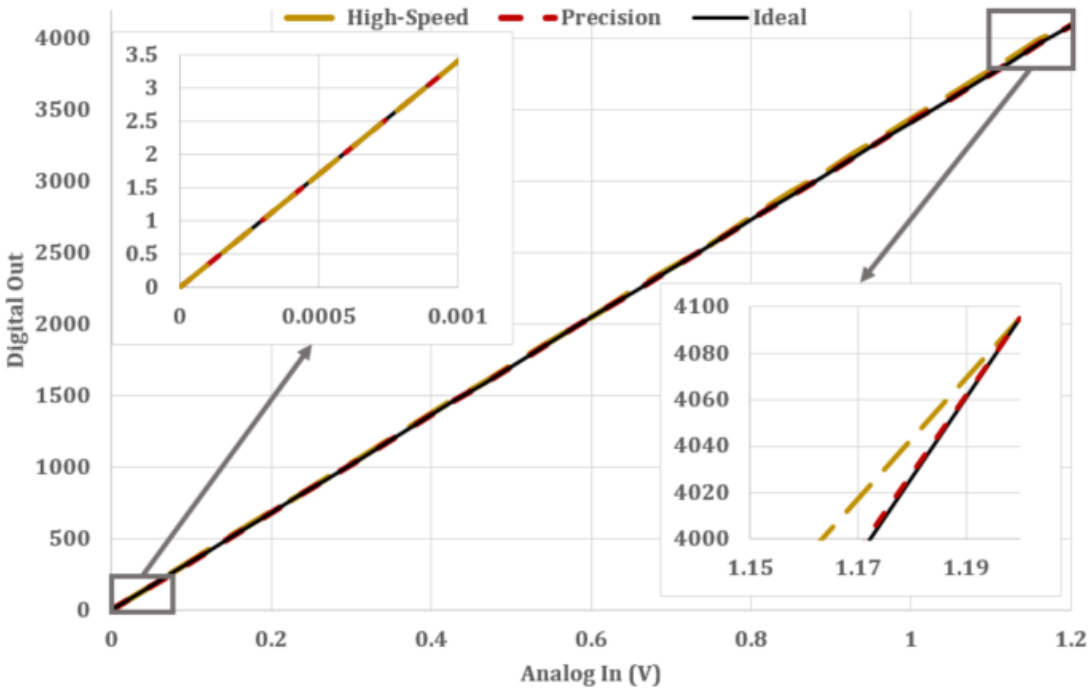

Figure 35: Analog Input vs Digital Output for Both Application at Typical Corner

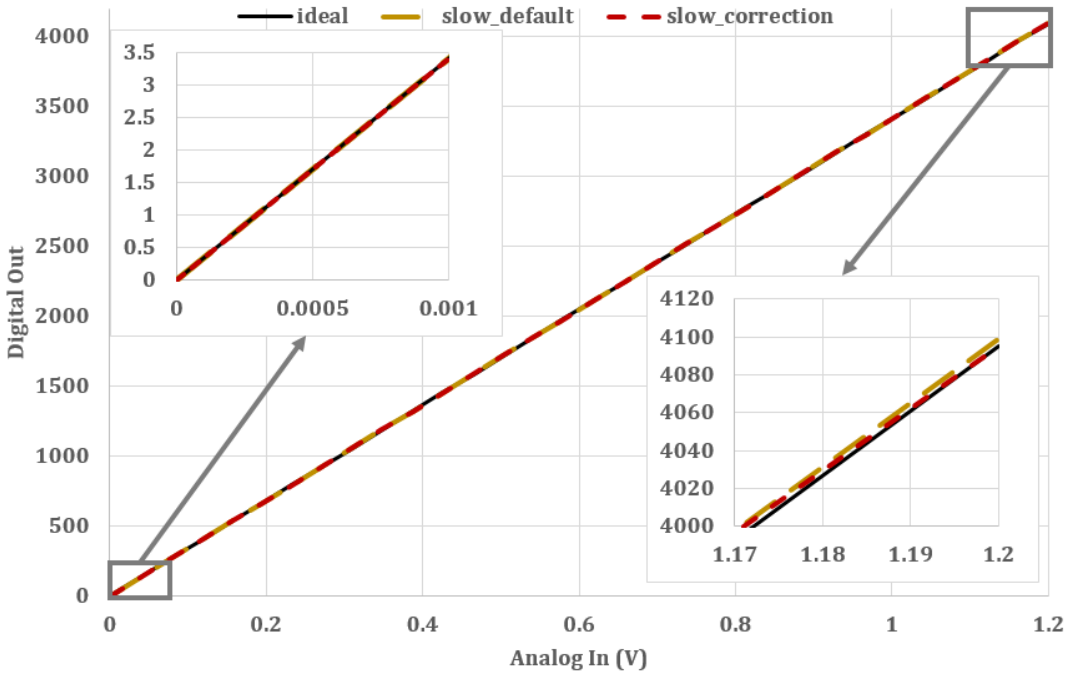

Figure 36: In vs Out with and without Calibration Adjustments at Slow Corner for Precision

Figure 35 shows the analog in vs digital out with and without calibration corrections for the fast corner. As provided in the figure, the default line has gain error. But with this calibration technique, the default is the best fit line. Since there was no offset, the common mode voltages remain at the default.

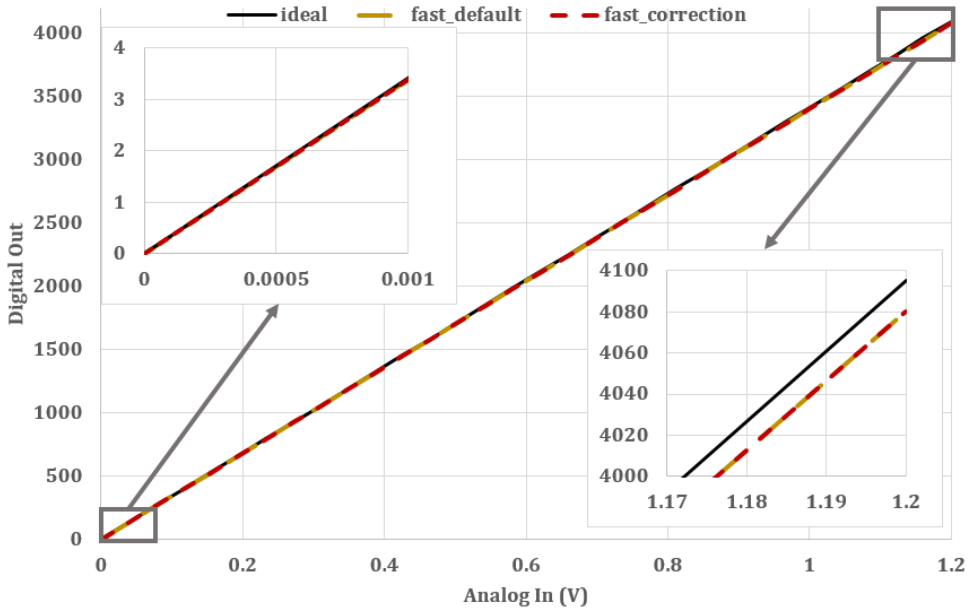

Figure 37: In vs Out with and without Calibration Adjustments at Fast Corner for Precision

The calibration results are shown in Figure 36 and 37 for the high-speed application. The first plot shows the analog in versus digital output with and without any adjustments of the common mode voltages for the slow corner. As provided in the figure, the default mode has a gain error and saturates at the input voltages around the maximum. The correction line is closer to the ideal slope but there is still some gain error. The average error for the default and correction for the slow corner is reduced by approximately half, from ~4% and ~1.5%.

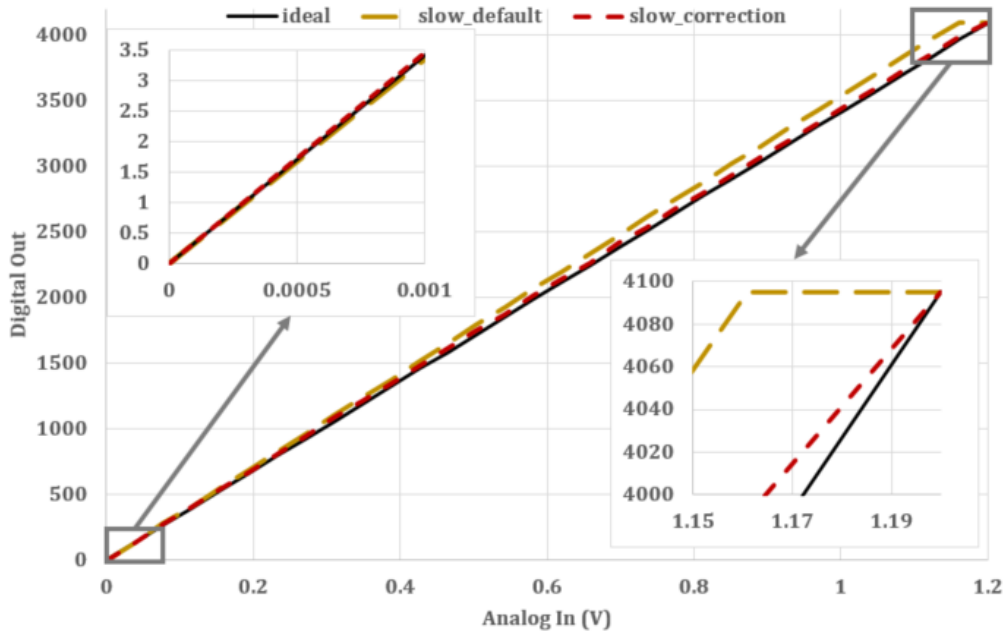

Figure 38: In vs Out with and without Calibration Adjustments at Slow Corner for High-Speed

Figure 37 shows the analog in vs digital out with and without calibration corrections for the fast corner. As provided in the figure, the default line has an offset error of 1 digital output and a slight gain error. With the corrections, the line has no offset and the average error is reduced from ~0.19% to 0.17%.

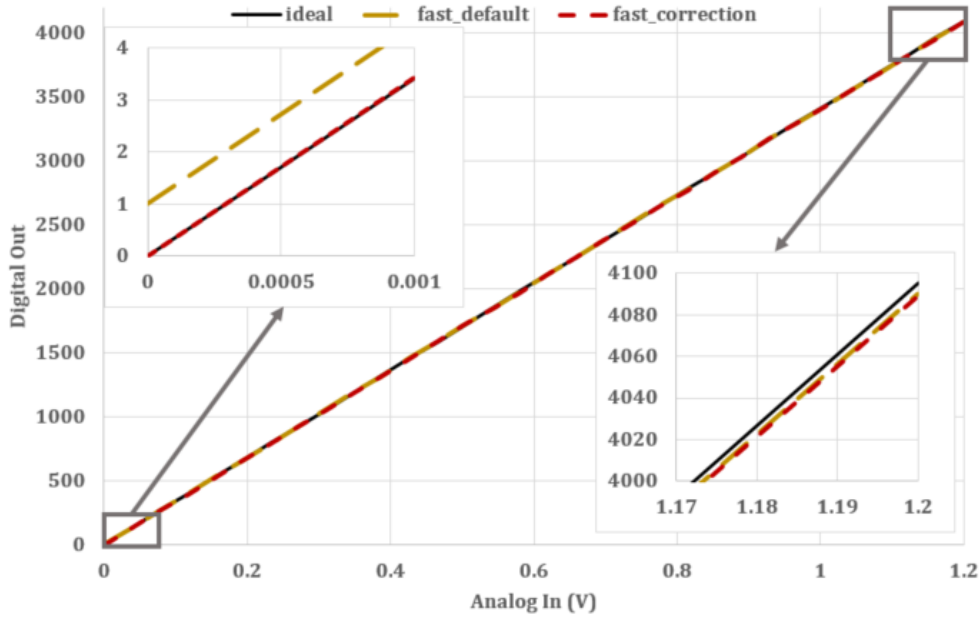

Figure 39: Analog In vs Digital Out with and without Calibration Adjustments at Fast Corner

Post-Layout Results

The proposed ADC is designed in Intel 10nm technology. The area for the analog portion, i.e. the delta-sigma modulator and bias generator, is 300µm x 235µm which is 70,500µm² or 0.0705mm². The capacitors used are metal-on-metal capacitors. The voltage supply used is 1.8V.

Provided in Figure 38 is the input voltage vs modulated output voltage for the precision application. As compared to the pre-layout simulations, it is realized that the modulator is working as it should, i.e. outputting a bit stream.

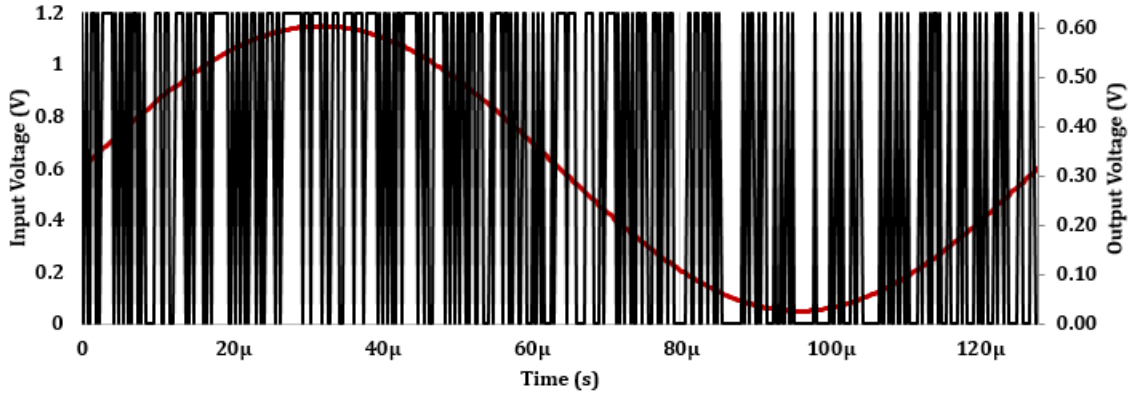

Figure 40: Input Voltage and Modulated Output for 32MHz

Figure 39 shows the amplifier outputs of the first and second stages. As provided in the figures, the first stage amplitude is greater than the second stage as expected. The peak to peak for the first stage is approximately 550mV and 300mV for the second stage which is similar to the results of the pre-layout simulations.

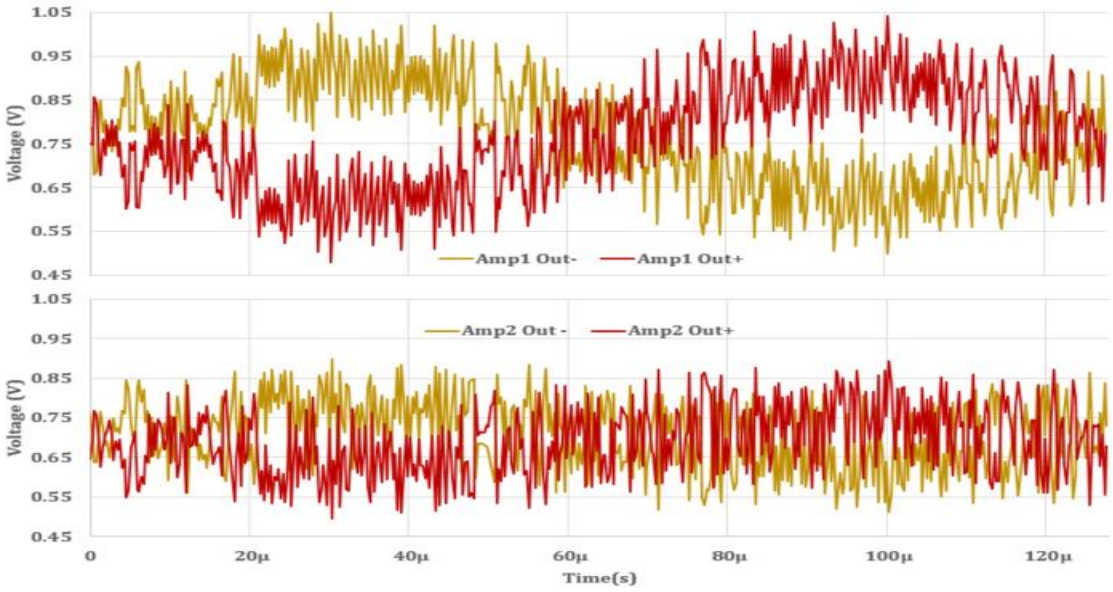

Figure 41: Integrator Output for First and Second Stage for 32MHz

Figure 40 shows the PSD plot for the precision application. For the post layout simulations, the SNR is lower than the pre-layout simulations. This is expected since the amplifier bandwidth decreases slightly which in turn reduces the SNR of the delta-sigma modulator. The post-layout SNR is 73.44dB.

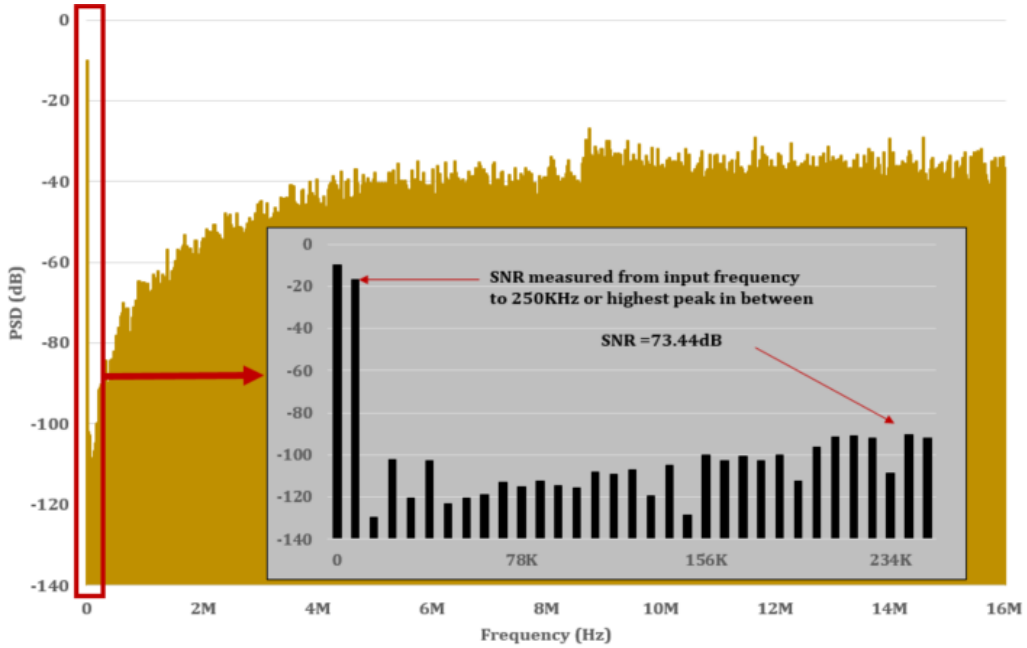

Figure 42: PSD Plot for 32MHz

The modulator has the correct operation as provided in Figure 41. There is a bit stream of ones and zeros which means the modulator is working correctly.

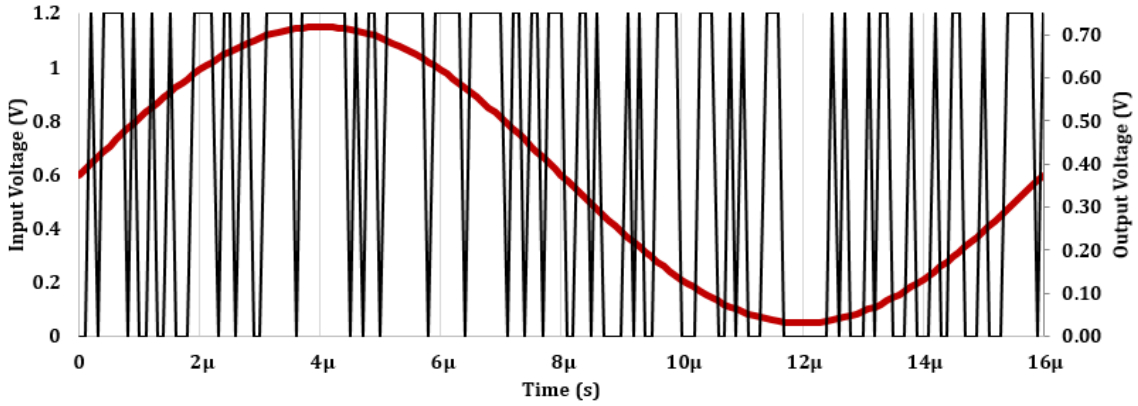

Figure 43: Input Voltage and Modulated Output for 256MHz

Figure 42 shows the integrator outputs for each stage. Compared to the pre-layout simulations, the amplitudes of the outputs are about the same (~500mV for the first stage and ~300mV for the second stage). Also, the common mode output has shifted upwards slightly from 850mV to 1V.

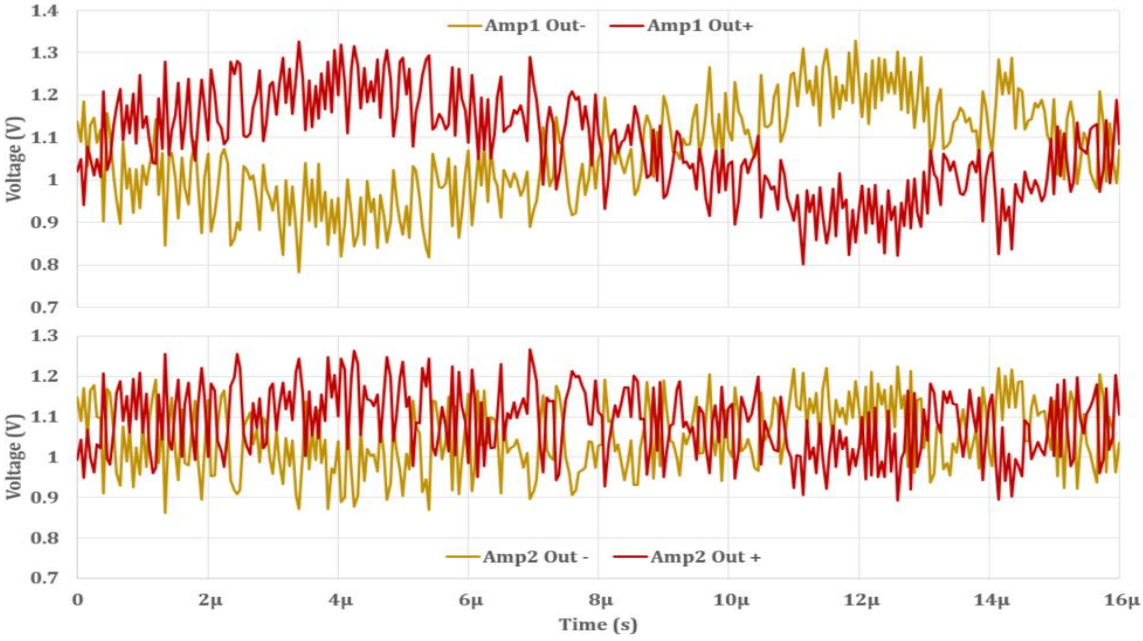

Figure 44: Integrator Output for First and Second Stage for 256MHz

The PSD plot is provided in Figure 43 with the full spectrum and the zoomed in version. Similar to the pre-layout simulations, the cut off frequency for conversion mode and calibration mode is 8MHz and 2MHz, respectively. The SNR has been reduced by about 6dB from pre-layout to post-layout. The calibration mode SNR reduced by approximately 3dB.

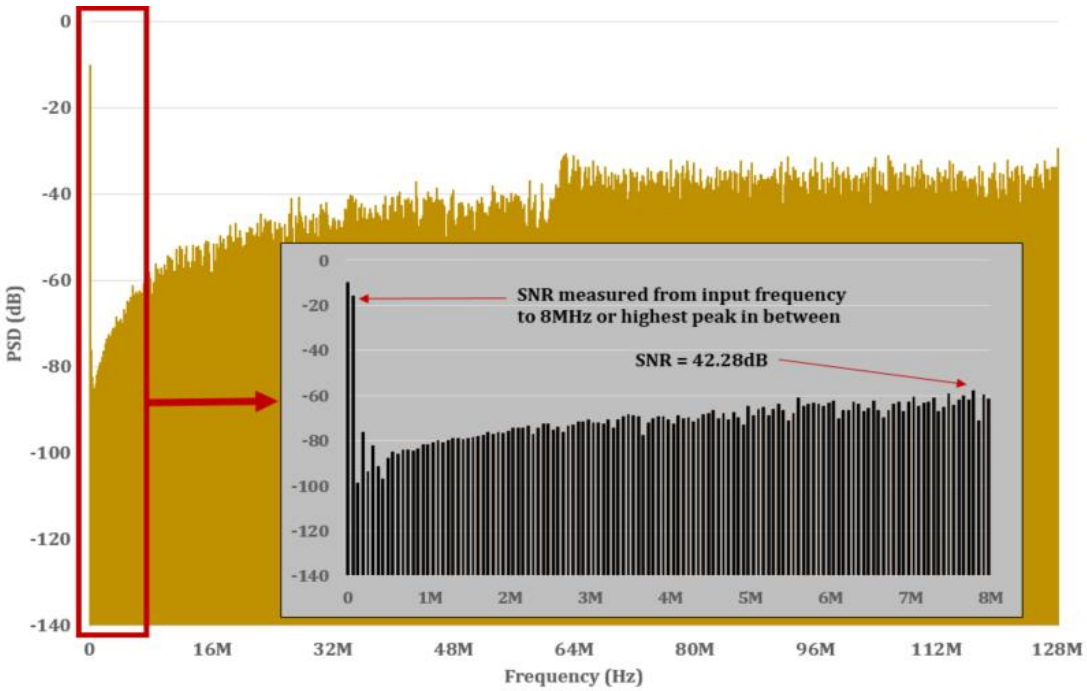

Figure 45: PSD Plot for 256MHz

Provided in Figure 44 is the post-layout simulation of the analog in versus digital output for both applications at the typical corner.

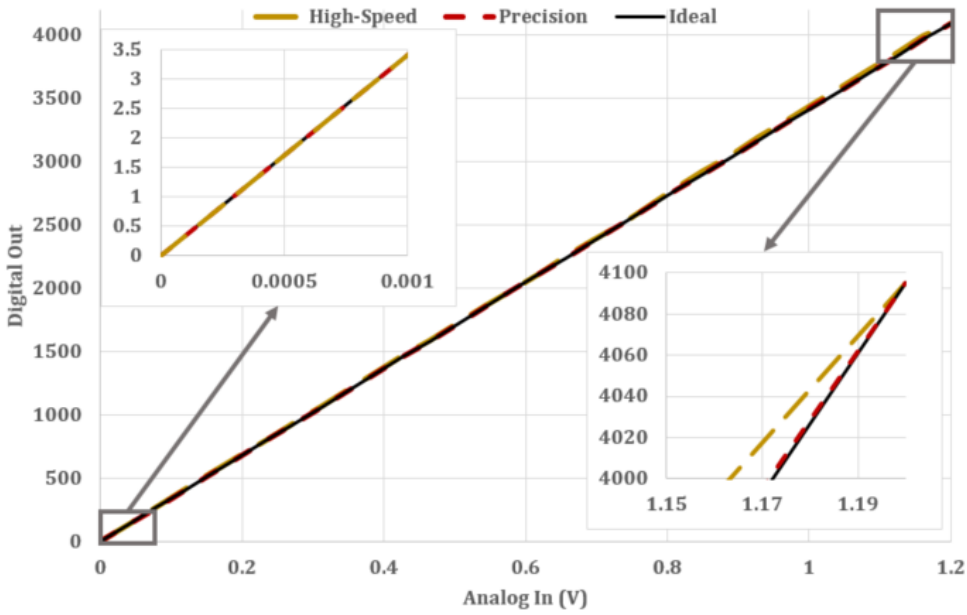

Figure 46: Analog Input vs Digital Output for Both Application at Typical Corner

The post simulation results for the precision application are provided in Figure 45 and Figure 46 for the slow and fast corner, respectively. These plots are very similar to the pre-layout simulations. There is a slight increase in average error for the default values for the slow corner from 0.050% to 0.051% and 0.31% to 0.68% for the fast corner.

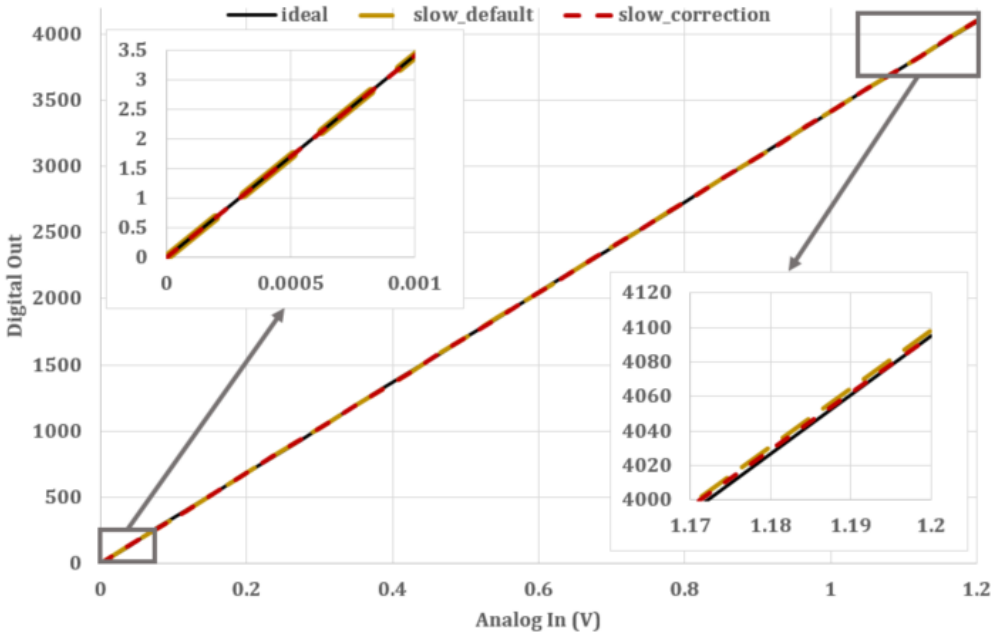

Figure 47: In vs Out with and without Calibration Adjustments at Slow Corner for Precision

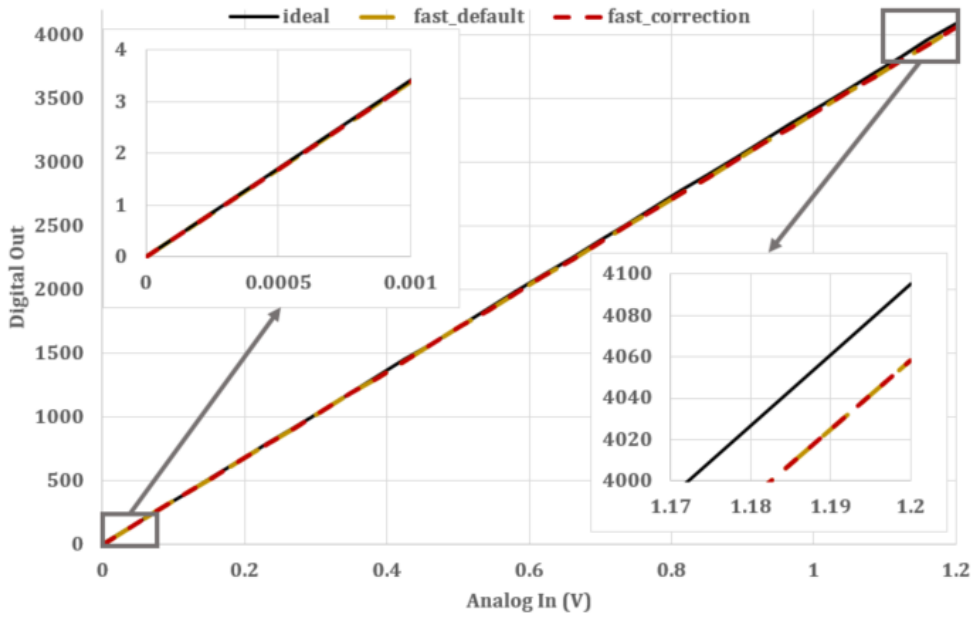

Figure 48: In vs Out with and without Calibration Adjustments at Fast Corner for Precision

For the high-speed application, the calibration plots for the slow corner and fast corner are shown in Figure 47 and Figure 48, respectively. The slow corner error is greatly increased as seen in the plot. But after the correction the error is reduced to 2.3%. For the fast corner, the error increased to 0.71% and slightly reduced to 0.7% after the calibration.

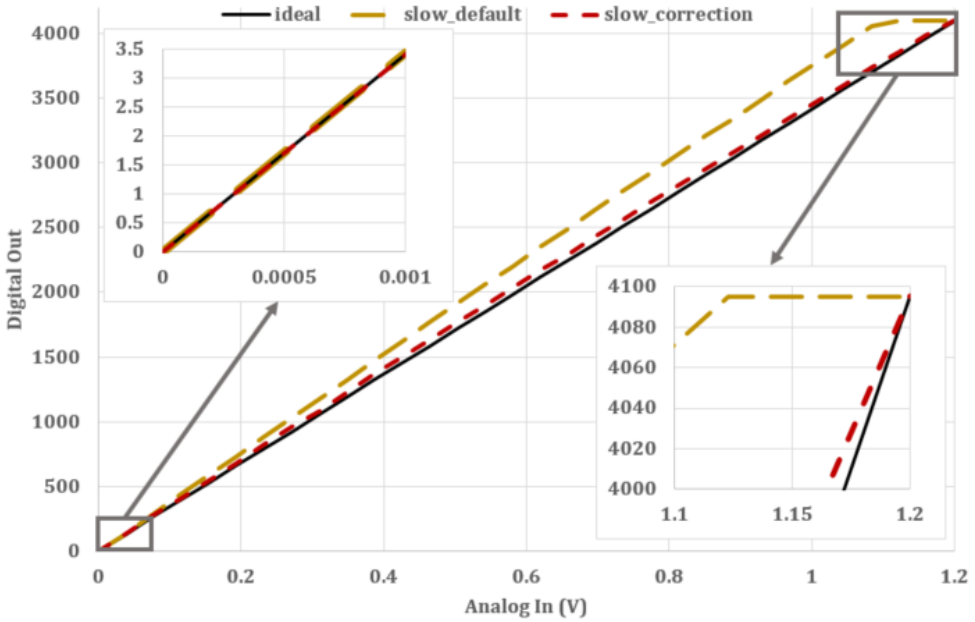

Figure 49: In vs Out with and without Calibration Adjustments at Slow Corner for High-Speed

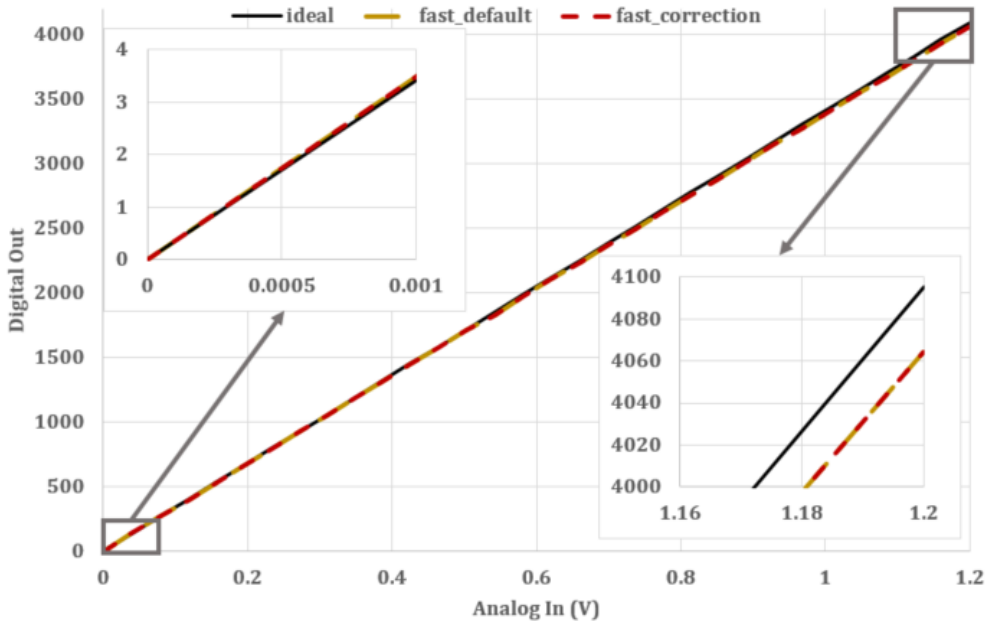

Figure 50: In vs Out with and without Calibration Adjustments at Fast Corner for High-Speed

		Pre-Layout	Post-Layout
Precision	Slow Default	0.050%	0.051%
	Slow Correction	0.047%	0.048%
	Fast Default	0.31%	0.68%
	Fast Correction	0.31%	0.68%
High-Speed	Slow Default	3.90%	10.31%
	Slow Correction	1.47%	2.30%
	Fast Default	0.19%	0.71%
	Fast Correction	0.17%	0.70%

Table 3: Average Error for Both Applications

Summary of Results

Table 3 summarizes the results of the two designs for pre- and post-layout. The ADC was able to achieve high precision and speed for the applications. The average errors shown in the table are the average errors after the correction.

Parameter	Pre-Layout		Post-Layout	
	Precision	High-Speed	Precision	High-Speed
Resolution	12-bits			
ENOB	12.41	7.76	11.91	6.73
Conversion Rate	35.7ksps	1.1Msps	35.7ksps	1.1Msps
SNDR	76.48dB	48.45dB	73.44dB	42.28dB
Clock Frequency	32MHz	256MHz	32MHz	256MHz
Decimate	128	32	128	32
OSR	64	16	64	16
Slow Average Error (%)	0.047%	1.47%	0.048%	2.30%
Fast Average Error (%)	0.31%	0.17%	0.68%	0.70%

Table 4: Summary Table

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

ADCs are used in a variety of applications. For this work, there were two possible applications. One for a 12-bit precision ADC and one for high speed voltage supply monitoring. Combining these two applications into one ADC in 10nm technology was challenging.

As provided in the paper, a 2^{nd}-order ΔΣ ADC was implemented because of the advantages transitioning into Intel's 10nm technology. Because of the low threshold voltages, there is more current leakage with transistors in this process technology. ΔΣ is less stringent on matching because of the three types of calibration. These calibration techniques were used to reduce the offset and gain error. One calibration is a CDS integrator and differential amplifier in the first stage of the delta-sigma modulator which aids in reducing offset. The other two calibration techniques were an auto-zero calibration

method, to subtract out offset, and a power on auto calibration, which minimized the gain error.

As shown in the paper, the two applications were able to serve their purposes. The security mode uses a 256MHz clock with a decimate of 32 in order to get the speed of approximately 1MSPS. The SNR was found to be ~39dB which is an ENOB of 6-bits, where the security requirement is a minimum of 5-bits. The precision ADC has an SNR of ~74dB which is an ENOB of 12-bits.

The auto-calibration technique increased the accuracy of the ADC. Future work that is needed for this calibration technique are optimizing timing of each conversion, translating the Verilog-A code to a synthesizable Verilog code, and implementing the calibration to accept negative numbers in the smaller analog inputs. These optimizations can aid in a better and more accurate ADC.

The ADC is designed in Intel 10nm technology using metal-on-metal capacitors using a 1.8V supply. The area of the delta-sigma modulator and bias generator, is 300µm x 235µm which is 0.0705mm^2.

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