High Power Density, High Efficiency Single Phase Transformer-less Photovoltaic String Inverters

by

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ABSTRACT

Two major challenges in the transformer-less, single-phase PV string inverters are common mode leakage currents and double-line-frequency power decoupling. In the proposed doubly-grounded inverter topology with innovative active-power-decoupling approach, both of these issues are simultaneously addressed. The topology allows the PV negative terminal to be directly connected to the neutral, thereby eliminating the common-mode ground-currents. The decoupling capacitance requirement is minimized by a dynamically-variable dc-link with large voltage swing, allowing an all-film-capacitor implementation. Furthermore, the use of wide-bandgap devices enables the converter operation at higher switching frequency, resulting in smaller magnetic components. The operating principles, design and optimization, and control methods are explained in detail, and compared with other transformer-less, active-decoupling topologies. A 3 kVA, 100 kHz single-phase hardware prototype at 400 V dc nominal input and 240 V ac output has been developed using SiC MOSFETs with only 45 μF/1100 V dc-link capacitance. The proposed doubly-grounded topology is then extended for split-phase PV inverter application which results in significant reduction in both the peak and RMS values of the boost stage inductor current and allows for easy design of zero voltage transition. A topological enhancement involving T-type dc-ac stage is also developed which takes advantage of the three-level switching states with reduced voltage stress on the main switches, lower switching loss and almost halved inductor current ripple.

In addition, this thesis also proposed two new schemes to improve the efficiency of conventional H-bridge inverter topology. The first scheme is to add an auxiliary zero-voltage-transition (ZVT) circuit to realize zero-voltage-switching (ZVS) for all the main switches and inherent zero-current-switching (ZCS) for the auxiliary switches. The advantages include the provision to implement zero state modulation schemes to decrease the inductor current THD, naturally adaptive auxiliary inductor current and elimination of need for large balancing capacitors. The second proposed scheme improves the system efficiency while still meeting a given THD requirement by implementing variable instantaneous switching frequency within a line frequency cycle. This scheme aims at minimizing the combined switching loss and inductor core loss by including different characteristics of the losses relative to the instantaneous switching frequency in the optimization process.

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CHAPTER 1 INTRODUCTION

High power density and high efficiency has become a very important metric in many of these applications. Increasing the switching frequency to significantly higher levels can lead to high power density but at the expense of correspondingly higher switching losses. New wide bandgap devices such as GaN and SiC are developing in rapid speed which can achieve much higher switching frequency (5-10 times) with same switching loss. Another method which is soft-switching has been pursued which can not only realize reduced switching loss, miniaturization, and lightweight, but also reduce the electromagnetic interference (EMI) and switching noise.

1.1 PV Inverters

Solar energy is among the fastest growing renewable energy resources accounting for an increasing and significant share of new generation capacity additions each year [1], [2]. In the U.S. new solar installations have exceeded 1 GW dc in each quarter since 2014, reaching a total capacity 29 GW dc in March 2016. In Q1 of 2016, solar photovoltaic (PV) systems accounted for 64% of new electric generation added in the U.S. making it the largest source of capacity addition across all fuel types [1]. The distributed PV systems are garnering the interest of both the utility providers and residential consumers with the reducing solar panel costs, government incentive programs, and regulatory policies [3]-[5]. The power electronic converter is a key component of the grid connected PV systems, extracting maximum power from PV and

interfacing with the grid. The transformer-less PV inverters are increasingly more attractive due to their lower cost, reduced footprint, and improved efficiency compared to inverters with transformer isolation. However, a major challenge with the transformer-less inverters is the presence of common mode leakage currents [6] which can increase the system loss, distort the grid current, and induce severe electromagnetic interference. In addition, similar to most single-phase converters, another main challenge is the presence of double line frequency power ripple [7], which is the difference between the instantaneous grid injected power and the constant dc power corresponding to the maximum power point (MPP) from the PV panels, necessitating the use of large filters in conventional topologies.

The frame of a PV module is required by codes to be grounded. There is significant parasitic capacitances between the positive and negative PV terminals to the frame, and hence to the ground. When the positive and/or negative terminals are connected to a switching node of the inverter with respect to ground, it can lead to significant, common mode ground currents through these parasitic capacitances. [6], [8]-[19] present different methods to mitigate this problem in transformer-less PV inverters. A preferred way to mitigate the problem of ground currents would be to directly connect the PV panel negative (or positive) to the grid neutral (and therefore to ground) known as a doubly grounded structure. Such a configuration can completely eliminate PV capacitive coupled ground currents. But direct connection of these terminals is not possible in conventional transformer-less inverters, and hence topological variations are required to achieve this feature [8]-[10].

A similar solution is to ensure by topology a low-frequency (typically fundamental frequency) or constant potential of the PV negative relative to the grid neutral. Half-bridge inverters and neutral point clamped (NPC) half bridge inverters ([6], [11], and [12]) belong to this approach, but the challenge with such solutions is that they typically require another front-end dc-dc converter to ensure operation over a wide range of PV voltages and partial shading conditions. The full bridge inverter with bipolar sinusoidal pulse width modulation (SPWM) also reduces the common mode ground currents [13].

Other solutions to the ground current issue involve isolating the grid from the PV source during certain operating interval, for example, during the zero states of the switching cycle in a 3-level H-bridge converter. These are more involved solutions with additional switches and diodes like the HERIC [14], H5 [15], H6 with ac bypass [16], or H6 with dc bypass [17]. Y. Gu et al. [18] propose a transformer-less grid connected PV inverter based on virtual dc bus concept, and B. Gu et al. [19] offer a high efficiency solution with two additional ac-side switches that decouple the PV array from the grid during the freewheeling phases. All these proposed configurations can effectively address the common mode leakage current but have the drawback of higher number of active or passive components, and do not inherently address the other problem of double line frequency power ripple.

The electrolytic capacitors presently dominate power decoupling approach of single phase inverters due to their relatively high capacitance-to-volume ratio and lower cost. However, they have relatively high equivalent series resistance (ESR) and low RMS current rating per μF. More importantly, they have limited life time and pose reliability

challenges [20]. Through physics based degradation model it has been shown in [21] that the life time of such capacitors reduces with electrical and thermal stresses, and thermal cycling. In contrast, the PV panels have lifetime warranted for 25 years [22], and there is increasing pressure on the inverter manufacturers to match such a long life time. To mitigate this reliability bottleneck imposed by electrolytic capacitors, the power decoupling can be realized by the more reliable and higher efficient film capacitors. However, a direct replacement is not a feasible solution as film capacitors have comparatively lower energy density and will increase the converter volume and cost [23].

An extensive research has already been conducted in the direction of decreasing the capacitance requirement for the power decoupling so that the electrolytic capacitor can be replaced by a longer lifetime film capacitor [2], [7], [8], [24]-[37]. Some converters address the issue by adding an additional conversion stage (an auxiliary circuit) to handle the ripple power [24]-[28], which can be connected in either series or parallel to the primary converter. The main disadvantages of such approaches are higher cost, complex circuitry, and often higher losses with the addition of more active components. They also have to encounter higher current stress on the auxiliary circuit if connected in series [24], [25] or higher voltage stress if connected in parallel [2], [27]-[28].

For power factor correction (PFC) applications, [28] achieves reduction in the capacitance by allowing higher voltage ripple across the dc-link but at the cost of distorted line input current. Other papers have discussed sophisticated control schemes to reduce the dc-link capacitor without affecting the power quality [29]-[34]. But all these approaches do not essentially stretch the limit on reducing the capacitors to the minimum

and there is still much room for improvement. As such decoupling capacitor volume reduction remains an active area of research. In a recent study in [37], several decoupling approaches have been compared including dc side decoupling and ac side decoupling, with dc side decoupling shown to outperform ac decoupling approaches. The best solution shown in [37] achieves 15 μF/kW at 800 V, but using six switches and without considering the ground current issues or non-unity power factor operation. In some recent works in [38]-[42] very high converter power densities have been achieved by using ceramic capacitors for active power decoupling. The converter in [8] has addressed both the issues of ground current and power decoupling through a bidirectional buck-boost converter and two half-bridge split phase inverters in a doubly grounded structure. For PFC rectifier applications, [43] presents a similar topology as [8] and [48] with reduced capacitance at 110 V ac.

Additionally, to satisfy the emerging grid interconnection requirements and standards, the future grid-connected PV inverter systems are expected to perform similar tasks as the conventional power plants [44], [45]. Among others, reactive power support, i.e., operation at a range of power factors depending on grid conditions is a major requirement to be met by inverter systems.

Another recent trend in grid connected power converters is the increasing use of SiC MOSFETs due to their superior performance in terms of low R_{DS_ON} especially above 900 V and significantly faster switching characteristics [46], [47]. These wide bandgap devices now enable new decoupling circuits that involve higher voltages (and therefore, smaller film capacitors), as well as high switching frequencies to reduce the volume of filter inductors.

1.2 Soft Switching Techniques in Single Phase Inverters

The single phase full bridge inverter (H bridge inverter) is nowadays widely used for modern power conversion in numerous applications such as photovoltaic applications (PV), hybrid / electric vehicles (HEVs/EVs) and bridge-less power factor corrector (PFC) [55]-[59]. Power density / energy density have become a very important metric in many of these applications in recent years [60]-[63]. Increasing the switching frequency to significantly higher levels can lead to high power density with decreased volume in the passive filter components, however it is at the expense of correspondingly higher switching losses and therefore lower efficiency and larger heatsinks [64]-[68]. Soft-switching full-bridge inverters have been pursued for power conversion applications as a result which not only reduces the switching loss, but also reduces the electromagnetic interference (EMI) and switching noise which are also important metrics of a converter [69]-[73].

A conventional method is to allow high current ripple making the current flow in the negative direction in the main inductor to achieve soft switching condition of the main switches in the full bridge converter [73][74][[75]. This scheme uses negative inductor current to discharge the snubber capacitor to achieve ZVS of main switches. The strategy does not add additional circuits but the large inductor current ripple which is around twice the fundamental value is the major problem in this scheme.

Many zero voltage transition (ZVT) techniques have been introduced previously which involve using an auxiliary active circuit to divert the current from the main circuit to discharge the device capacitance, ensuring its turn on under zero voltage [76]-[93].

Among them, the representative circuits implementing the ZVT concept are the auxiliary resonant commuted pole (ARCP) [76]-[77], stellate or triangular resonant snubber inverters [78]-[79], coupled inductor inverters [80]-[82] and resonant dc-link inverters [83]-[85]. ARCP uses one bidirectional switch, one diode, one resonant inductor and two low frequency large balancing capacitors. The arrangement of the capacitors can generate a midpoint of the input voltage which is used to generate the ZVT source voltages but causes voltage balancing problems. Moreover for the full bridge inverters using unipolar PWM, two separate auxiliary circuits - one for each leg of the inverter, are needed in ARCP [76]. [85] proposes a ZVT circuit configuration with less number of components and can realize ZVS of the main switches, but only bipolar PWM modulation can be used which will cause higher output inductor current ripple and higher THD resulting in the requirement of larger filter components.

1.3 Variable Switching Frequency Scheme

The H-bridge single phase inverter is widely used for power conversion in numerous applications [97]-[99]. For grid-connected inverters, efficiency is a key metric, and power density has also drawn more attention in recent years. Soft switching techniques can reduce switching loss, but usually at the expense of additional auxiliary switches and diodes as well as additional inductors and capacitors increasing the cost, complexity and volume [100]-[101].

Besides constant switching frequency PWM (CSFPWM), variable switching frequency PWM (VSFPWM) has been developed to utilize the variable of switching frequency to reduce the switching loss or EMI problem by spearding the frequency

spectrum. By suitably varying the switching frequency over the fundamental cycle, a higher efficiency can be achieved without introducing any change in hardware.

Hysteresis current control is one of the variable switching frequency methods. It can save some switching loss (though not optimal) but it has unpredictable switching frequency resulting in relatively poor harmonic performance and it is difficult to use this scheme in voltage control modes [102]-[103]. Random PWM (RPWM) is a kind of widely used VSFPWM method developed recently [104]-[106]. The principle of RPWM is randomly spreading the switching period for the converter to distribute the frequency spectrum. RPWM has been developed for more than 20 years and many improvements are under way for different applications. One of the improvements is to effectively reduce the acoustic and EMI noises for the converter system. However the results are usually based on statistical effects without calculation. Therefore the converter losses and current ripple under RPWM are usually not controllable. Ultimately, a controllable VSFPWM is preferred in place of RPWM.

Wei [107] proposed a method that doubles the switching frequency in the area where the ripple is bigger. This method can reduce the switching loss but it is only a rough determination of the switching frequency variation and does not fully take advantage of the THD requirement with theoretically analysis. Qian and Amirahmadi [74]-[75] proposed a variable switching frequency method to allow the inductor current ripple magnitude to be twice of the fundamental current value. In this way the inductor current reaches positive and negative value in every switching cycle which can realize ZVS of the main switches. However this method results in large inductor core loss and copper loss and is only feasible for the application that the inductor fundamental current

is small. Variable switching frequency together with SVPWM has also been studied in various papers [108]-[114]. The application is usually for motor drive and therefore the aim is to decrease EMI, noise and device switching loss while meeting the requirement such as torque performance.

Based on the analysis of current ripple distribution, Mao [115] proposed a variable switching frequency method for a single phase inverter to minimize the device switching loss while satisfying the ripple requirement. The inductor ripple current in each switching cycle is predicted with the circuit parameters such as duty cycle, switching period. Inductance and dc voltage. By implementing the optimal derived scheme. The switching frequency is arranged to control the current ripple to satisfy the THD requirement while reducing the switching loss.

However, basically all of the above methods do not take into account the fact that the inductor core loss, usually accounting for a considerable portion of the total loss, may also change at the same time with variable switching frequency. Therefore the total loss may not have a significant improvement when the optimization only considers device switching loss.

1.4 Report Organization

This report is divided into seven chapters. Chapter 2 proposes a doubly grounded, transformer-less PV inverter topology with active power decoupling built into the basic topology, and capable of supporting a wide range of power factor. Chapter 3 provides a split-phase doubly grounded, transformer-less PV inverter topology using GaN switches. Chapter 4 presents the inductor feedback ZVT technique for single phase inverters. A

variable frequency control scheme to decrease the switching loss while keep the THD same is investigated in Chapter 5. Chapter 6 discusses a T-type PV inverter with improved performance and efficiency. Chapter 7 presents the conclusions and plans for future work.

CHAPTER 2 SILICON CARBIDE (SIC) BASED CAPACITANCE MINIMIZED, DOUBLY GROUNDED TRANSFORMER LESS PHOTOVOLTAIC INVERTER WITH INHERENT ACTIVE POWER DECOUPLING

The proposed circuit topology is a unique combination of boost and half bridge circuit using only four switches overall. This topology effectively addresses both the issues of single phase, transformer-less PV inverters, with the connection of AC neutral to PV negative terminal eliminating common mode module ground currents, and the active decoupling at high dc-link voltage resulting in dc-link capacitance (15 μF/kW) that is among the lowest reported in literature, and well below the values used in state-of-the-art commercial products. The proposed circuit is a topological improvement to [8] leading to significant reduction in power decoupling capacitance requirement along with other improvements.

2.1 Operating Principles and Simulation Results

The grid connected version of the proposed topology is shown in Figure 2.1, while Figure 2.2 represents its stand-alone version. The first thing to note in Figure 2.1 and Figure 2.2 is that the ac neutral is connected directly to the PV negative terminal, inherently eliminating the common mode, high frequency ground currents through the PV module capacitance, which is a common problem in other transformer-less inverters. As seen, the proposed topology can be viewed as a unique combination of a bi-directional boost dc-dc stage coupled with an asymmetric half-bridge inverter stage.

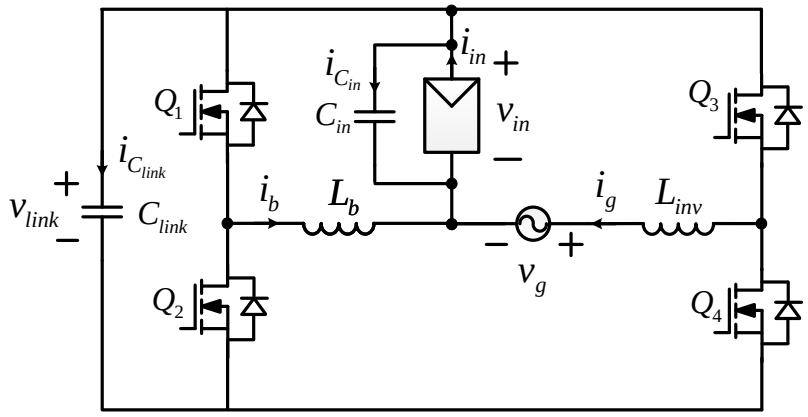


Figure 2.1. Proposed Topology in Grid Connected Configuration

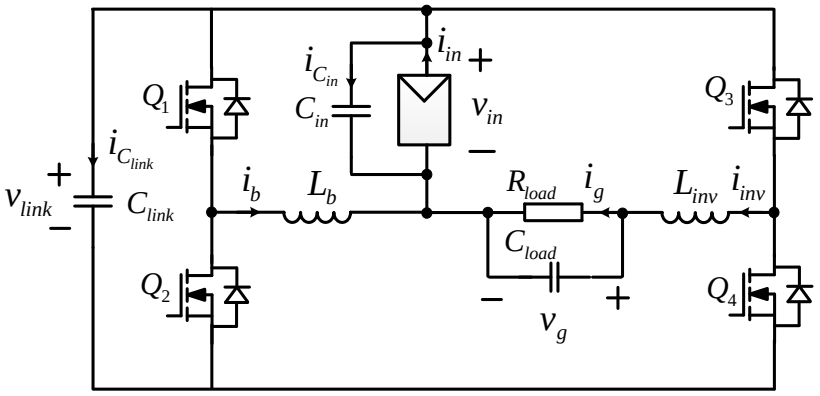


Figure 2.2. Proposed Topology in Standalone Configuration

2.1.1 Bi-directional Boost Converter Stage

The bi-directional boost stage is comprised of the switches Q_1 and Q_2, inductor L_b, and the dc-link capacitor C_{link}. Its low voltage side is the PV input voltage, v_{in} which is controlled to be a pure dc corresponding to the PV MPP voltage, thus ensuring high MPPT efficiency. The high voltage side of the boost stage is the dc-link voltage (v_{link}) which is specifically designed to swing over a wide range and have a high nominal value in order to fully support the 120 Hz power oscillations. The duty ratio of the boost stage (Q_1) is controlled by a high bandwidth input voltage controller whose reference

corresponds to the MPP voltage for grid-connected applications.

2.1.2 Asymmetric Half-bridge Inverter Stage

The half-bridge inverter comprises of switches Q_3 and Q_4 and filter inductor L_{inv} for grid-connected configuration (LC filter for stand-alone configuration, as shown in Figure 2.2). The two (asymmetric) voltage levels of the half bridge stage, as shown in Figure 2.1, are the PV voltage v_{in} and the difference voltage v_{link} - v_{in}. Clearly, the upper voltage level, v_{in} is constant, while the lower level has the same voltage swing present in v_{link} and also has a different average value than v_{in}. The duty-ratio of the half-bridge stage is controlled (sinusoidal PWM) to directly control the grid current in the grid-connected configuration (or output ac voltage in the case of stand-alone configuration). The reference for the magnitude of the grid current is derived from an outer control loop that regulates the average of dc-link voltage to a set reference value. In order to regulate the grid current or voltage without distortion the constraints in (2.1) have to be met. These two constraints place a limit on the minimum value of the PV voltage and the maximum voltage swing allowed at the dc-link.

$$\begin{cases} if \quad v_g \geq 0, \quad v_{in} > v_g(t) \\ if \quad v_g < 0, \quad v_{link}(t) - v_{in} > -v_g(t) \end{cases} \tag{2.1}$$

In Figure 2.1 and Figure 2.2, v_{in} *is* the input voltage, v_{link} is the dc-link capacitor voltage, v_g is the grid/load voltage, i_{in} is the dc input current, i_{Cin} is the input capacitor current, i_b is the boost inductor current, i_{Clink} is the dc-link capacitor current, i_g is the grid/load current, i_{inv} is the inverter stage inductor current, L_b is the boost stage inductor,

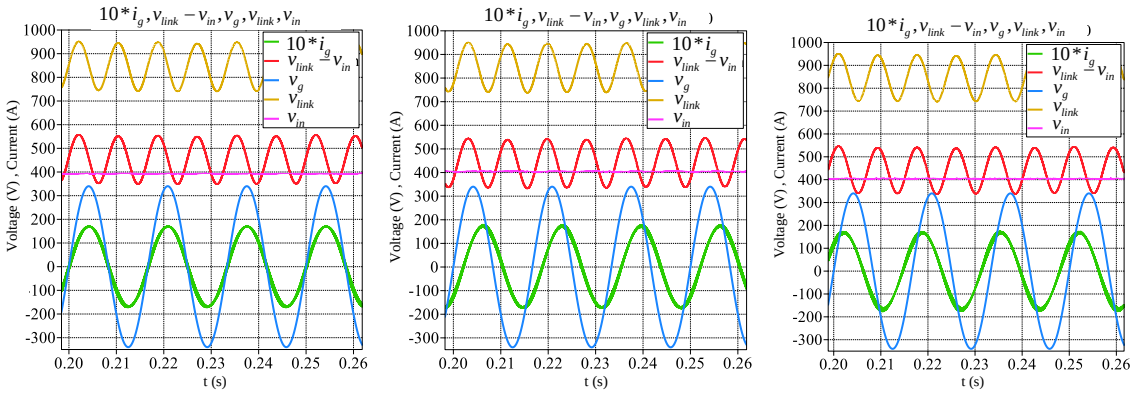
L_{inv} is the inverter stage inductor, C_{in} is the input capacitor, C_{link} is the dc-link capacitor, and C_{load} is the output filter capacitor.

The operating principles and control of the proposed topology can be better understood by observing some of the salient, ideal waveforms obtained from PLECS simulation. These simulations (and experimental results presented later) correspond to a 3 kVA inverter with specifications given in Table 2.1.

Table 2.1. Converter Specifications

Power	3 kVA
Nominal dc Input Voltage	400 V
Grid/ Load Voltage	240 V RMS
Grid/ Load Current	12.5 A RMS
Power Factor	0.7~1 lead or lag

Figure 2.3 shows the simulation waveforms of dc-link voltage, input voltage, and the difference of the dc-link and input voltages along with grid current and grid voltage. Three sets of waveforms corresponding to different power factors – unity, 0.7 lagging, and 0.7 leading respectively, are presented. As seen, the input voltage v_{in} is controlled to be a constant dc V_{in} with negligible 120 Hz ripple. The reduced peak-peak ripple of around 5 V which is around 1.3% of the average value of the input voltage, demonstrates that the power decoupling is predominantly supported by the dc-link capacitor which is decoupled from the input, leading to higher MPPT efficiency. It can also be seen that the two constraints given in (2.1) have been satisfied in all three cases, with leading power factor (Figure 2.3c) corresponding to the worst-case condition where the difference voltage is barely above $-v_g$ at the critical point.



(a) (b) (c)

Figure 2.3. Waveforms Showing Dc-link Voltage, Input Voltage, Grid Voltage, Grid Current, and the Difference of the Dc-link Voltage and Input Voltage at (a) Unity Power Factor; (b) 0.7 Lagging Power Factor; (c) 0.7 Leading Power Factor Operations

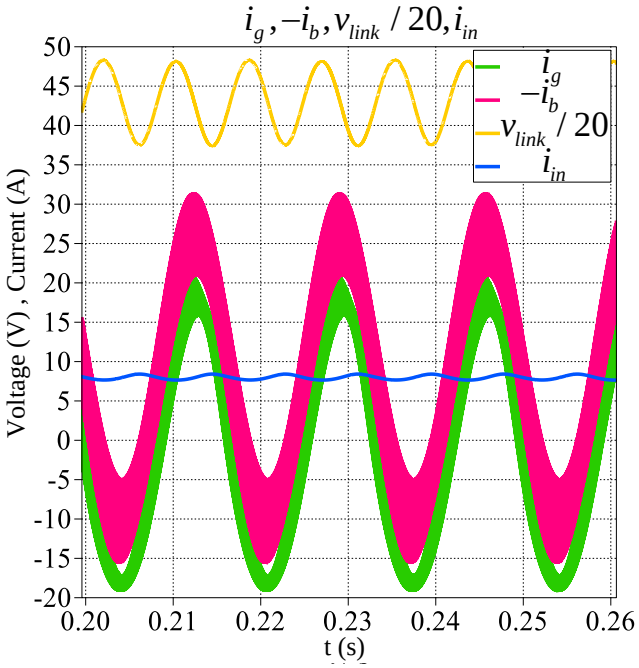


Figure 2.4. Simulation Waveforms of Inductor Currents at 3 kVA, UPF Showing i_b, i_{in}, i_{inv}, and v_{link}

Figure 2.4 shows the waveforms of input current, boost inductor current, grid current, and scaled dc-link voltage at unity power factor (UPF) operation. As seen in

Figure 2.4, and as can be verified from the schematic of Figure 2.1, the cycle-by-cycle averaged boost inductor current is bi-directional and comprises of the sinusoidal grid current and the input dc current.

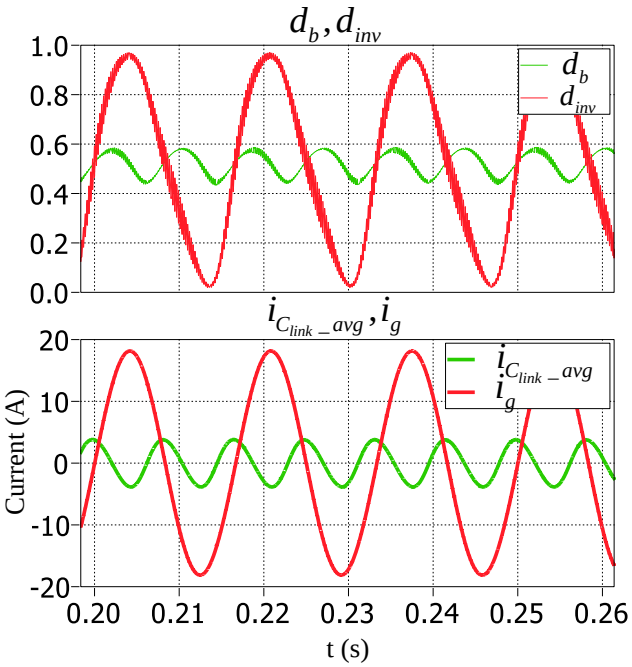


Figure 2.5. Simulation Waveforms of Boost and Inverter Duty Ratio (top), Grid Current, and Cycle-by-cycle Averaged Dc-Link Capacitor Current at 3 kVA and UPF

Figure 2.5 shows the boost stage duty ratio (d_b) and inverter stage duty ratio (d_{inv}), grid current, and dc-link capacitor average current, at UPF, where d_b and d_{inv} are duty ratio of the switches Q_1 and Q_3 respectively in Figure 2.1. It is interesting to note that, the inverter duty ratio is not only a sine waveform, but has double line frequency component to mitigate the influence of dc-link ripple on the grid output. In order to regulate the input voltage to be a pure dc, the boost duty ratio should also contain 120 Hz component as shown. These are achieved automatically by proper design of the closed loop control.

2.2 Capacitance Optimization

In single phase converters, the power decoupling capacitor accounts for a major part of the volume. So minimization of the capacitor volume is very important to achieve high power density. Active solutions for power decoupling attempt to minimize the capacitance requirement by allowing a large voltage swings. The following simple analysis establishes the relationship among the capacitance, nominal voltage, and maximum voltage swing to support the double-line-frequency pulsating power, for a given kVA rating at any arbitrary power factor.

The grid voltage and grid current at an arbitrary power factor $\cos\theta$ are given in (2.2), with the corresponding instantaneous grid power shown in (2.3).

$$v_g = V_g \sin(\omega t) \qquad i_g = I_g \sin(\omega t + \theta) \tag{2.2}$$

$$p_g = \frac{V_g I_g}{2}[\cos\theta - \cos(2\omega t + \theta)] \tag{2.3}$$

The dc-link voltage has a dc component and a double line frequency component as given in (2.4) where, V is the nominal dc voltage and V_r is the amplitude of ripple component. This is a good approximation when V_r is relatively small compared to V as is the case in many active decoupling methods.

$$v_{link} = V + V_r \sin(2\omega t + \theta) \tag{2.4}$$

(2.5) and (2.6) show the duty ratio expressions of the boost and inverter stages respectively, both of which are functions of the converter load, as V_r is dependent on the load. Further simplification of (2.5) would show the presence of a dominant dc term, a

small 2nd harmonic and an even smaller 4th harmonic term in the boost duty ratio, d_b. Similarly, further simplification of (2.6) would show that the inverter duty ratio, d_{inv} consists of dominant fundamental frequency with smaller 2nd, 3rd, and 4th harmonic components. The presence of other higher order harmonics are negligibly small.

$$d_b = \frac{V - V_{in} + V_r \sin(2\omega t + \theta)}{V + V_r \sin(2\omega t + \theta)} \tag{2.5}$$

$$d_{inv} = \frac{V - V_{in} + V_g \sin(\omega t) + V_r \sin(2\omega t + \theta)}{V + V_r \sin(2\omega t + \theta)} \tag{2.6}$$

The power processed at the dc-link can be expressed as in (2.7), and substituting for v_{link} from (2.4) in (2.7) yields (2.8).

$$p_{link} = \frac{1}{2}\frac{d}{dt}\left(C_{link} v_{link}^{\,2}\right) \tag{2.7}$$

$$p_{link} = \omega C_{link}(2VV_r \cos(2\omega t + \theta) + V_r^2 \sin(4\omega t + 2\theta)) \tag{2.8}$$

The requirements for the dc-link capacitor to support the entire double-line-frequency power ripple can be determined by comparing the $2\omega t$ terms in (2.3) and (2.8), and is given in (2.9), where S is the apparent power (VA) to the grid. The requirement given in (2.9) is general and valid for most active decoupling methods. It shows that the power decoupling can be achieved by different combinations of C_{link}, V, and V_r while meeting additional constraints imposed by the specific topology and operating conditions.

$$C_{link} V V_r = \frac{V_g I_g}{4\omega} = \frac{S}{2\omega} \tag{2.9}$$

It is well accepted that the volume of a film capacitor is proportional to the product of the capacitance and its maximum voltage rating V_{pk} (given in (2.10)) as shown in (2.11), where k is the proportionality constant.

$$V_{pk} = V + V_r \tag{2.10}$$

$$Volume = kC_{link}V_{pk} = kC_{link}(V + V_r) \tag{2.11}$$

Figure 2.6 shows a plot of the film capacitor volume vs. $C_{link}V_{pk}$ product for different film capacitors derived from datasheets of several manufacturers [50]-[52]. From this plot, *k* is found to be around 2458 $cm^3/\mu FV$ using linear interpolation, and this value is used in subsequent computations. As the energy density of a film capacitor increases with its voltage rating, it is advantageous to perform power decoupling at high dc-link voltages, as done in the proposed topology, from the viewpoint of capacitor volume. This results in need for higher voltage switches which may impact the converter efficiency and power density. High voltage (1.2 kV) SiC MOSFETs with low R_{DS_ON} can result in better trade-off in this context.

For ceramic capacitors, the volume is not strictly linear with the product of the voltage rating and the capacitance [23]. With their higher energy density and flexible placement due to smaller size, ceramic capacitors when used for power decoupling can help achieve higher power density for the inverter. However, the ceramic capacitors have the disadvantages of higher cost as a large number of ceramic capacitors are required, high series resistance under dc bias and hence higher losses, and nonlinear capacitance-voltage characteristics that result in control complexity [38], [41].

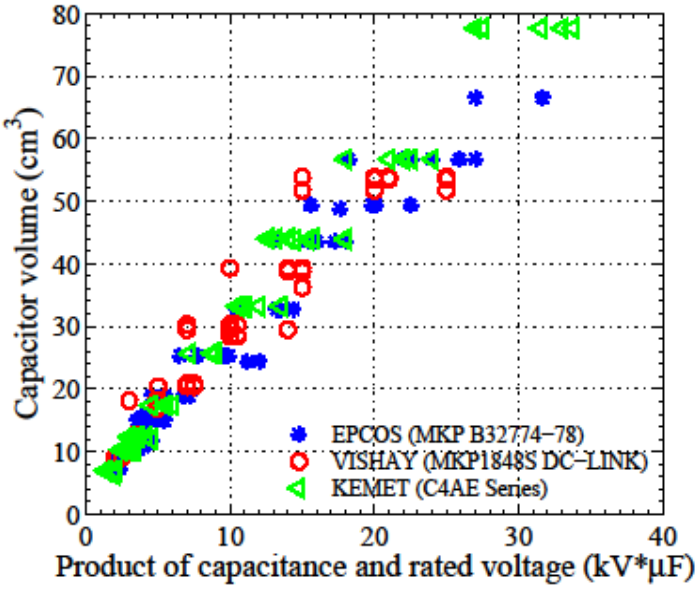


Figure 2.6. Plot of Film Capacitor Volume vs $C_{link}V_{pk}$ from Different Manufacturer Datasheets [50]-[52]

Hence, in order to optimize the capacitance requirement using film capacitors, the maximum dc-link voltage is pushed to the limit set by the voltage rating of the switches allowing sufficient safety margin, i.e., V_{pk} in (2.8) is set based on the selected MOSFET. Also, the constraints given in (2.1) must be instantaneously satisfied so that the inverter stage does not operate at over modulation and the grid current is not distorted. It is worth noting that the difference of the dc-link voltage and the input voltage in (2.1) does not need to be larger than the peak of the grid voltage always, but the difference only needs to be larger than the instantaneous grid voltage. A design based on keeping the difference voltage always higher than the peak grid voltage leads to a conservative and suboptimal capacitor design. In contrast, a design that allows the difference voltage to go below the peak grid voltage at some instants while always satisfying (2.1) relaxes some of the requirements on the decoupling capacitor to a certain extent, especially in terms of

allowable peak-peak ripple. However, while following the latter approach the range of power factor over which the inverter needs to operate needs to be carefully considered, since the instantaneous dc-link voltage as given in (2.4) is dependent on the power factor. From (2.2) and (2.4) it can be seen that as the power factor changes, the phase difference between the dc-link voltage and the grid voltage changes leading to a change in the voltage margin between v_g and $v_{link} - V_{in}$.

Figure 2.7 shows the difference of the dc-link voltage and input voltage for three different values of power factor along with $-v_g$ during the negative half-cycle. The margin in the difference voltage is also marked for each power factor case. These plots correspond to the specifications given in Table 2.1 and using a dc-link capacitance of 45 μF. As seen, the leading power factor is the worst-case scenario that limits the amplitude of the dc-link voltage ripple. This is also confirmed by the simulation waveforms shown in Figure 2.3.

The voltage margin at different points along the sinusoidal voltage waveform and at different power factors is plotted in Figure 2.8 corresponding to the same specifications as above, to further illustrate the dependence of the voltage margin ($v_{link} - V_{in} - v_g$) on point on wave and power factor.

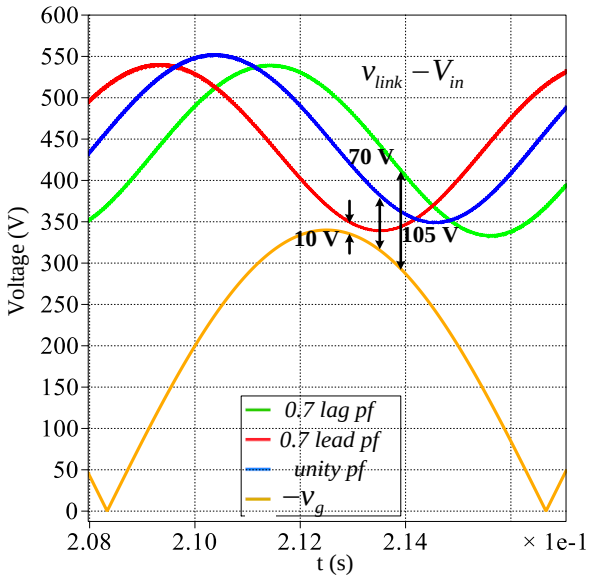


Figure 2.7. Plot Showing the Difference of the Dc-Link Voltage and Input Voltage for Three Different Values of Power Factor Along with -v_g During the Negative Half-Cycle, Highlighting the Available Voltage Margin

Based on the analysis described above, an optimization problem is solved to arrive at the minimum capacitance volume while simultaneously satisfying the two constraints in (2.1), considering the range of power factor of operation and range of variation in the input voltage. It is difficult to arrive at a closed form expression for the capacitor design given the numerous variables involved and their complex relationships. Hence, a numerical method illustrated as a flowchart in Figure 2.9 is used to determine the optimum capacitance. At first, V_r and V are obtained for different combinations of V_{pk} and C_{link} values by solving (2.7) and (2.8). From all these values, the ones which satisfy (2.1) are stored as valid combinations, from which the minimum capacitor volume is identified. The optimization is stopped once the number of iterations reached the maximum iteration length specified.

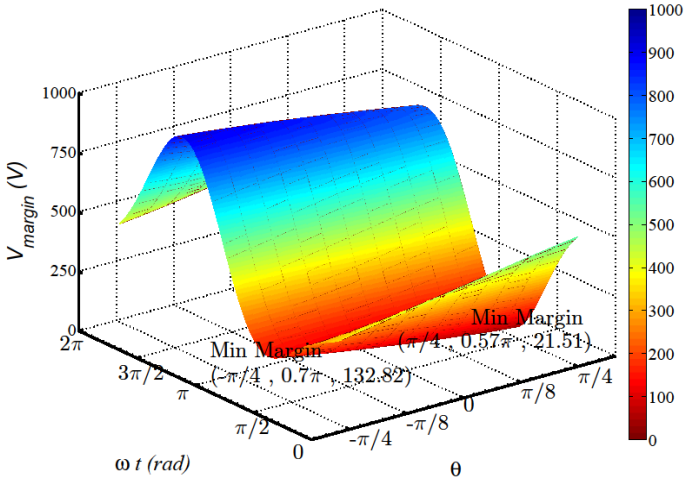


Figure 2.8. Plot of Voltage Margin for Different Power Factor Operation over One 60 Hz Cycle

In the present study, CREE C2M0080120D 1.2 kV SiC MOSFETs and 1100 V film capacitors are used, and hence the constraint on V_{pk} is set at 1000 V allowing 200 V voltage margin to the switches. The least volume is obtained as 80.53 cm^3 at 999 V, with 33 µF capacitor for decoupling for the given 3 kVA power rating with power factor allowed to vary from 0.7 lagging to 0.7 leading. If the operation is restricted to only unity power factor, then a 28.5 µF would have been sufficient.

Since the capacitor volume is roughly proportional to the product (µF*kV) of capacitance and voltage rating, a new metric of µF*kV/kW is proposed here for proper comparison of different topologies and active decoupling methods. Table 2.2 shows a detailed comparison, including the new metric µF*kV/kW, number of active switches, efficiency, and suitability for double-grounded operation of several topologies in the literature for which the above parameter values have been reported or can be calculated from the available information. As seen, the proposed topology achieves a relatively low

number for the metric μF*kV/kW compared to other topologies while using only four switches and featuring high efficiency at high switching frequency and double-grounded operation. It may be noted that Table 2.2 does not include the recent works that employ ceramic capacitors [38]-[42] since the metric uF*kV/kW may not be directly related to capacitor volume for ceramic capacitors. Some of these designs have achieved very high overall converter power density due to low profile and higher energy density of ceramic capacitors in spite of using large values of capacitance, some in the range of mF.

Table 2.2. Comparison of Various Topologies with Different Active Power Decoupling Techniques

Topology	Total capacitance (μF)	Voltage rating of capacitor (V)	Converter rated Power (kVA)	$C*V_{pk}/P$ (μF*kV/kW)	No. of switches***	Switching frequency (kHz)	Efficiency (%)	Double-grounding capable
Proposed	45	1100 dc	3	16.5	4	75	96.4****	Yes
[37] (PFC)	30	800 dc	2	12	6	30	96.5	No
[7] (PFC)	200	800 dc	6*	26.7	6	20	93	No
[25]	2000	63 dc	2	63	8	NR	NR	No
[36] (PFC)	220	240 ac**	4	22	6	2	NR	No
[35]	180	380 dc	1	68.4	4	19.2	92.8	No
[8]	102	700 dc	1	71.4	6	40	97.3	Yes
[29]	180	800 dc	1	144	4	19.2	93	No
[43] (PFC)	10	1200 dc	1	12	4	19	92	Yes

*Operating kVA for [7] estimated based on the experimental results provided

**240 ac is equivalent to 400 V dc from film capacitor datasheet in [53]

*** Total combined VA rating of all the switches is a better metric than just number of switches. However, this information is not available in the literature for all the topologies compared. For the proposed topology, the combined VA rating of all the four switches (sum of product of peak switch current and peak switch voltage) is 76800 VA.

**** Not including the loss of auxiliary power supply and fan which is around 5 W.

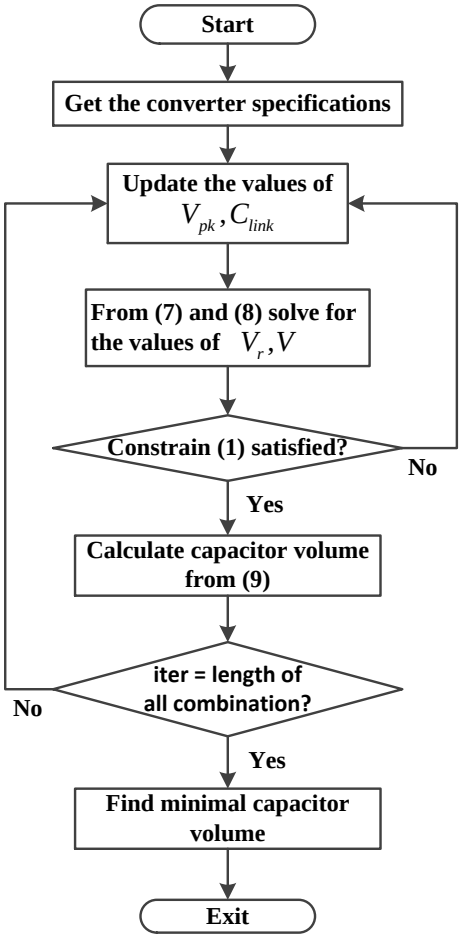


Figure 2.9. Flow Chart of Capacitance Optimization for the Proposed Topology

2.3 Comparison with Buck-boost Based Doubly-grounded Topology

As mentioned in Section 2.1, the proposed inverter is a topological improvement to another double-grounded, transformer-less inverter topology with inherent active decoupling reported in [8]. A split-phase (120 V/0/120 V) version with six switches was presented in [8] and its corresponding single phase configuration with four switches is shown in Figure 2.10 to facilitate direct comparison with the proposed topology. As seen in Figure 2.10, the circuit of [8] comprises of a bi-directional buck-boost stage coupled

with a half-bridge inverter stage interfacing to the grid (or with stand-alone ac load). The two voltage levels of the half-bridge are the input dc voltage v_{in} and the buck-boost output v_c. The capacitor C_c with dynamically variable voltage v_c provides the complete double line frequency power decoupling. The main topological difference in the proposed inverter is the use of a bi-directional *boost* stage instead of a *buck-boost* stage and having the decoupling capacitor across the entire dc-link rather than at a lower voltage level as in [8]. These changes have significant impacts in terms of decoupling capacitance and volume requirement, capacitor RMS current, RMS and peak current through dc-dc inductor (dc-dc stage), and RMS current of the input capacitor (across PV terminal). The two topologies have the same dc-link voltage and hence the same voltage stress on the MOSFETs, but current stress is different due to different inductor currents in the dc-dc stage.

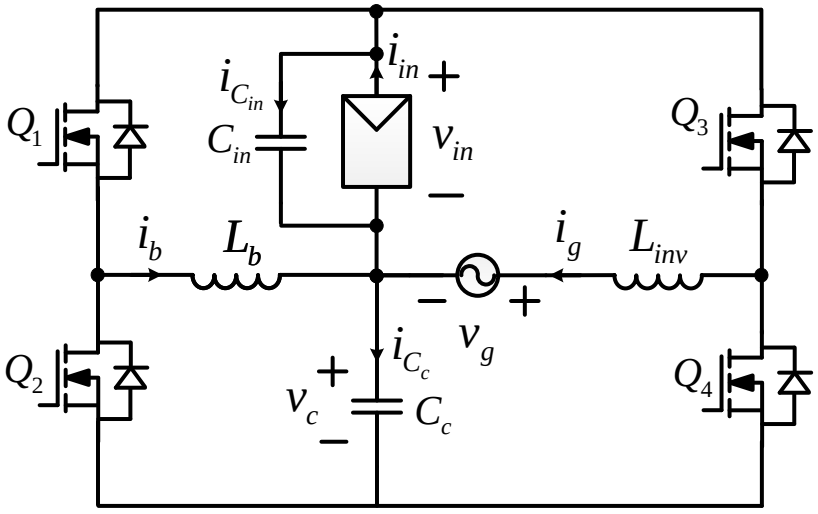


Figure 2.10. Single Phase Grid-Connected Version of the Topology Proposed In [8]

2.3.1 Capacitor Volume Comparison

A main advantage of the proposed topology compared to [8] is the reduction in the volume of the decoupling capacitor. This is due to the higher voltage operation of the decoupling capacitor in the proposed topology (by an amount equal to the maximum input voltage). The capacitor optimization procedure outlined in Figure 2.9 is applied to both the topologies for the same specifications given in Table 2.1 and for the same switch voltage ratings.

The volumes of the capacitors needed (indicated by color code) for each topology for various combinations of capacitance and peak capacitor voltage are plotted in Figure 2.11. For the topology of [8] the least volume is obtained to be 80.44 cm^3 at 608 V capacitor voltage with 54 μF capacitance, and for the proposed topology the least volume is obtained as 69.76 cm^3 at a capacitor voltage of 999 V with a capacitance of 28.5 μF all at UPF operation. Hence, the proposed topology reduces the required capacitor volume by 13.28% and the capacitance requirement by 47.22%.

The low frequency currents through the decoupling capacitors of the two topologies are compared in Figure 2.12a. The RMS capacitor current in both the topologies consist of two components - a second harmonic component and switching frequency components which is the dominant constituent. Both the topologies have same switching frequency component, but the one in [8] has twice second harmonic current than that of the proposed topology as shown in Figure 2.12a. Thus the RMS current through the capacitor in the proposed topology is around 6% smaller than that of [8].

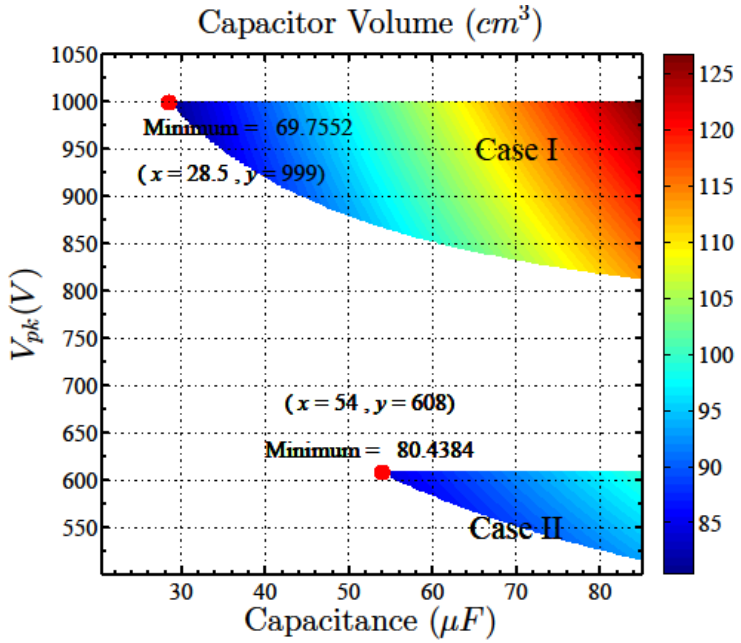


Figure 2.11. Volume of the Power Decoupling Capacitor at UPF for Different Capacitance and V_{pk} Values Showing the Minimum Volume Point for the Proposed Topology: Case I, and for Topology in [8]: Case II

2.3.2 Inductors Comparison

Due to the different placements of the decoupling capacitor, the dc-dc inductor current characteristics are quite different in the two topologies. From Figure 2.10 it can be seen that the buck-boost inductor current, i_{bb} of [8] is the sum of the input dc current, the line frequency grid current, and a double line frequency decoupling capacitor current as given in (2.12)

$$i_{bb} = I_{in} - I_g \sin(\omega t + \theta) + I_c \cos(2\omega t + \theta) \tag{2.12}$$

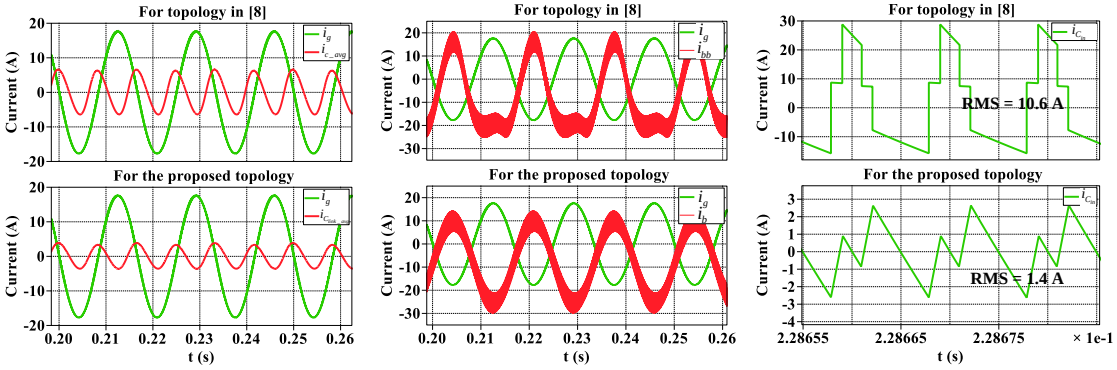
As seen from Figure 2.1, the dc-dc boost inductor current i_b of the proposed topology is the sum of the input dc current and the line frequency grid current only as

given in (2.13).

$$i_b = I_{in} - I_g \sin(\omega t + \theta) \tag{2.13}$$

The dc-dc inductor currents corresponding to the two topologies are shown respectively in Figure 2.12b. Due to the absence of the second harmonic current in inductor of the proposed topology, it has lower RMS current compared to that of [8] by 4.6% for the specifications considered here, which results in about 10% reduction in inductor conduction loss. However, the second harmonic current in the inductor of [8] leads to a reduction in the peak value of the inductor current. The reduction relative to the proposed topology is maximum at unity power factor by 25.4% and becomes progressively lower as power factor is reduced, reaching just 2% reduction at power factor of 0.7 (lag or lead).

2.3.3 High Frequency Content in Input Current



(a) (b) (c)

Figure 2.12. Comparison of Waveforms of Topology in [8] Shown in Top Plot With Those of the Proposed Topology Shown in Bottom Plot. (A) Decoupling Capacitor Current and Grid Current, (B) Inductor Currents of Dc-Ac Stage and Dc-Dc Stage, and (C) Input Capacitor Current

Another main advantage of the proposed topology is in the current drawn at the input, or more specifically the high frequency current through the input capacitor. As seen from Figure 2.10, input capacitor current in [8] is the high frequency component of the sum of two switch currents and hence has a large pulsating component. However, in the proposed topology, the high frequency content in the input capacitor current is the sum of only the ripple components of the two inductors, and hence much smaller.

Figure 2.12c shows the input capacitor current for the two topologies near $\omega t = \pi/2$ radian. The RMS current through the input capacitor for [8] is 10.6 A, whereas the corresponding RMS current in the proposed topology is only 1.4 A, resulting in 86.8% reduction. This is significant since the input capacitor does not support 120 Hz power pulsation, and hence is designed to be small with low current rating.

2.4 System Modeling and Controller Design

System modelling and controller design is studied in this section.

2.4.1 Large Signal Modeling

The large signal average model of the proposed converter can be obtained by replacing the two power poles by the corresponding ideal transformers with turns-ratios being equal to the respective instantaneous duty ratios as shown in Figure 2.13. To simplify the analysis, all the circuit components are considered lossless, i.e., ESR of the capacitors, on-resistance of the switches, and series resistance of inductors are assumed to be zero. The PV string can be modeled as a voltage source in series with a resistor R to simulate the characteristics of the PV modules.

From Figure 2.13, the dynamics of the inductor currents can be obtained based on KVL as follows,

$$L_b \frac{di_b(t)}{dt} = v_{in}(t) - d_b(t)v_{link}(t) \tag{2.14}$$

$$L_{inv} \frac{di_g(t)}{dt} = v_{in}(t) - v_g(t) - d_{inv}(t)v_{link}(t) \tag{2.15}$$

where $d_b(t)$ and $d_{inv}(t)$ are the instantaneous duty ratio of the switches Q_1 and Q_3 respectively which is same as used in Section 2.2. Q_2 and Q_4 switch in complementary to Q_1 and Q_3 respectively with appropriate dead time. The other variables can be referred from the Figure 2.13

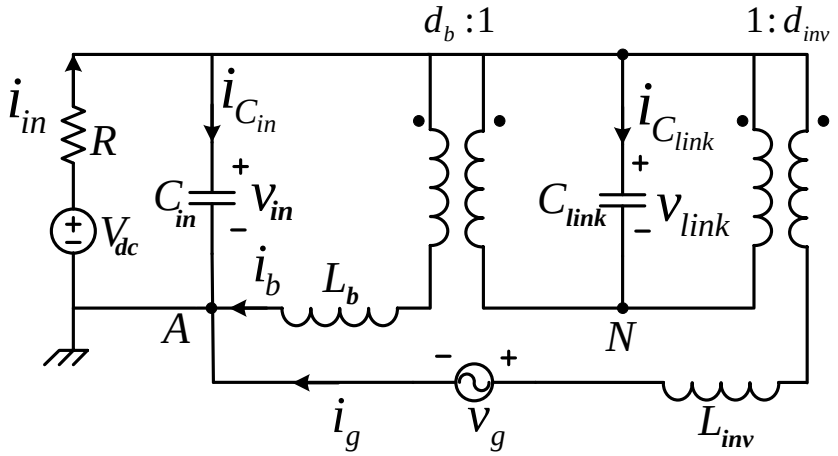


Figure 2.13. Large Signal Model of the Proposed Topology

By applying the basic KCL to points A and N in Figure 2.13, the following two differential equations are obtained.

$$C_{in} \frac{dv_{in}(t)}{dt} = i_{in}(t) - i_b(t) - i_g(t) \tag{2.16}$$

$$C_{link} \frac{dv_{link}(t)}{dt} = d_b(t)i_b(t) + d_{inv}(t)i_g(t) \tag{2.17}$$

These four equations define the large signal model of the proposed converter. Finally, the input current can be shown as follows.

$$i_{in}(t) = \frac{V_{dc} - v_{in}(t)}{R} \tag{2.18}$$

2.4.2 Small Signal Analysis

The small signal model is derived by linearizing the large signal average model about a steady operating point. The higher order terms are neglected. The equations for the buck-boost stage are as follows,

$$L_b \frac{d\tilde{i}_b(t)}{dt} = \tilde{v}_{in}(t) - \tilde{d}_b(t)V_{link} - \tilde{v}_{link}(t)D_b \tag{2.19}$$

$$C_{in} \frac{d\tilde{v}_{in}(t)}{dt} = \tilde{i}_{in}(t) - \tilde{i}_b(t) - \tilde{i}_g(t) \tag{2.20}$$

where, the capital letter denotes the variables at steady state operating point, and the tilde-terms express the perturbation quantities. The input current perturbation term $\tilde{i}_{in}(t)$, can be expressed as follows.

$$\tilde{i}_{in}(t) = -\frac{1}{R}\tilde{v}_{in}(t) \tag{2.21}$$

For the inverter stage, the small signal model is given as follows,

$$L_{inv} \frac{d\tilde{i}_g(t)}{dt} = \tilde{v}_{in}(t) - \tilde{d}_{inv}(t)V_{link} - \tilde{v}_{link}(t)D_{inv} \tag{2.22}$$

$$C_{link} \frac{d\tilde{v}_{link}(t)}{dt} = \tilde{d}_b(t)I_b + \tilde{i}_b(t)D_b + \tilde{d}_{inv}(t)I_g + \tilde{i}_g(t)D_{inv} \tag{2.23}$$

Rearranging the previous five equations, the following state space model is obtained.

$$x = \begin{bmatrix} \tilde{i}_b & \tilde{i}_g & \tilde{v}_{in} & \tilde{v}_{link} \end{bmatrix}^T,\ u = \begin{bmatrix} \tilde{d}_b & \tilde{d}_{inv} \end{bmatrix}^T$$

$$A = \begin{bmatrix} 0 & 0 & 1/L_b & -D_b/L_b \\ 0 & 0 & 1/L_{inv} & -D_{inv}/L_{inv} \\ -1/C_{in} & -1/C_{in} & -1/RC_{in} & 0 \\ D_b/C_{link} & D_{inv}/C_{link} & 0 & 0 \end{bmatrix} \tag{2.24}$$

$$B = \begin{bmatrix} -V_{link}/L_b & 0 & I_b/C_{link} & 0 \\ 0 & -V_{link}/L_{inv} & I_g/C_{link} & 0 \end{bmatrix}^T$$

$$C = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix},\ D = 0$$

2.4.3 Controller Design

The various objectives of the controllers include regulating the input voltage based on MPPT reference, controlling the dc-link voltage, and controlling the ac output current and/or ac output voltage of the inverter. The input voltage v_{in} is regulated to the reference with minimum 120 Hz ripple so that MPPT efficiency is not compromised. Figure 2.14 shows the block diagram for the different control loops including the feed forward terms.

In the present prototype, the input is derived from a dc voltage source with a series resistance of 5 ohm to approximately model a PV array, and the input voltage reference for the converter is set manually for the required output power. When an actual PV string as used as input, this voltage reference is intended to be provided by the MPPT controller. The input voltage controller is designed for a high bandwidth in order to reduce the double line frequency component in the input voltage to a low value.

The dc-link control loop regulates the average of the dc-link voltage to a reference value. A first order Butterworth filter with cut-off frequency of 10 Hz is used to filter out the 120 Hz component in the dc-link voltage before comparing it with the reference. The error is used to change the magnitude reference of grid injected current – an increase in dc-link voltage causes the current reference to increase, thereby bringing the dc-link voltage back to the desired reference. The output current controller is designed to control the grid current with the magnitude of the current reference drawn from the dc-link voltage control loop, and the phase and frequency of the sinusoidal waveform determined by a phase-locked loop. Both dc-link and inverter control loops employ simple PI controllers with appropriate feed forward terms added as shown in Figure 2.14 to simplify controller design. More advanced controllers are currently under investigation, especially to improve dynamics of the dc-link voltage control.

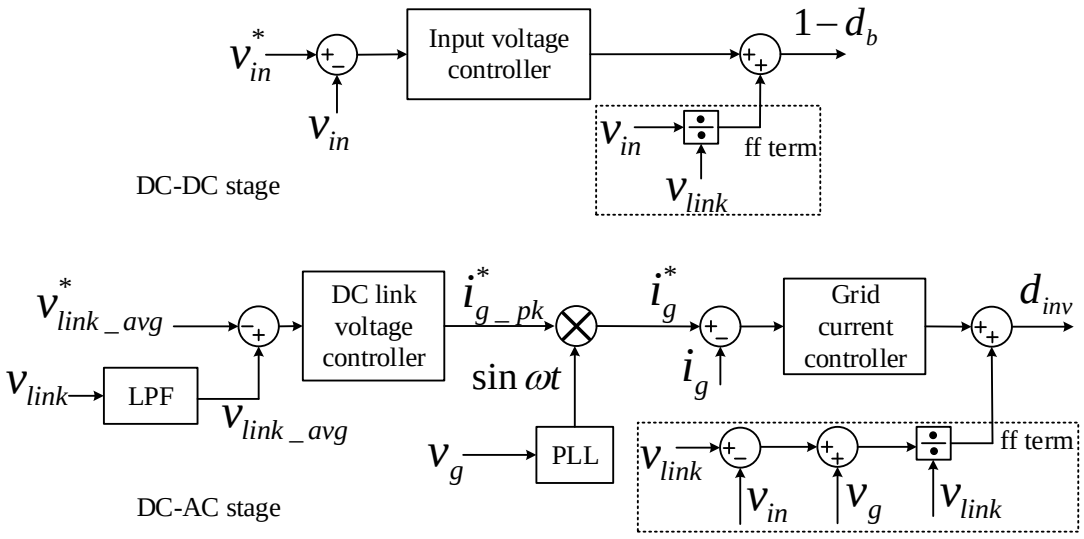


Figure 2.14. Controller Block Diagram for the Proposed Topology in Grid Connected Configuration Showing Feedforward (FF) Terms

2.5 Hardware Implementation and Results

A laboratory prototype of a 3 kVA inverter has been built to demonstrate the proposed topology with the specifications as given in Table 2.1. A 430 V voltage source in series with a 5 Ω resistor is used to emulate the PV input characteristics. The voltage at the converter input is around 390 V accounting a drop of 40 V in the input resistor at rated power.

2.5.1 Design of Components

As discussed in Section 2.3, C_{link} is designed based on the ability to decouple the 120 Hz power ripple under the worst-case condition, which is the leading power factor case. With the maximum steady-state dc-link voltage limited to 1000 V and modulation ratio limited at 0.9 at 0.7 leading power factor, C_{link} is calculated to be 33 μF. Allowing some margin in consideration of the transient conditions and the tolerance in the capacitor values, C_{link} is chosen to be 45 μF (nine 5 μF / 1100 V film capacitors connected in parallel). C_{in} is designed based on the maximum allowable high frequency voltage ripple at the input. As mentioned in previous sections, the 120 Hz ripple is controlled to be present only in the dc-link capacitor.

L_b, L_{inv}, and f_{sw} are designed through loss and volume optimization together with output THD requirements. The objective is to minimize the inductor volume and loss with switching frequency and inductance as the variables [54]. The losses include switch conduction loss (which is a function of peak current and in turn the function of inductance value), the switching loss (a function of switching frequency and peak

current), and inductor copper and core losses (a function of frequency, inductor core material, and inductance). The switching losses are calculated by using the turn-on and turn-off energy loss data from the manufacturer datasheet. Inductors are wound using planar ferrite core 3C94 to achieve low profile and small core loss and Litz wire of 400 strands AWG 40 to reduce high frequency copper loss. C_{load} is chosen primarily based on the output voltage THD requirement. The values of different components are given in Table 2.3. The savings in the volume of passive components has a significant impact in increasing the power density of the proposed converter.

Table 2.3. Component Values in the 3 kVA Prototype of Proposed Topology in Standalone Configuration

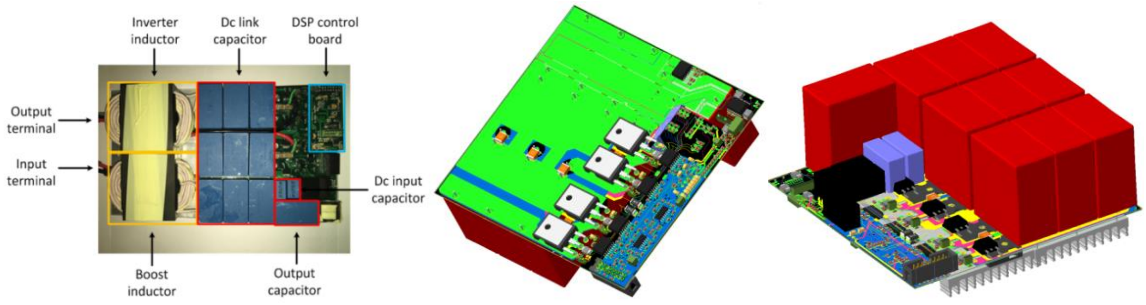
Parameter	Description	Components of 3 kVA
C_{link}	DC-link capacitor	45 μF / 1100 V
C_{in}	Input capacitor	2.2 μF / 500 V
L_b	Boost inductor	230 μH
L_{inv}	Inverter inductor	230 μH
f_{sw}	Switching frequency	75 kHz/ 100 kHz
C_{load}	Output capacitor	4.7 μF / 300 V ac

CREE C2M0080120D wide bandgap 1.2 kV SiC MOSFETs are used for each of the four switches Avago ACPL 337J is used as the driver IC. The positive gate voltage of the MOSFET (V_{gs}) is 20 V and negative is -6 V. In order to eliminate the diode recovery loss, four CREE C2D05120A SiC schottky diodes are connected in parallel to the four MOSFETs. A DSP control board based on TI TMS320F28335 is built to realize the control scheme. The driver circuit, DSP, ADC, and feedback circuits are all powered by

external auxiliary power supply which consumes around 5 W power. The dead time for each leg is set to 80 ns.

2.5.2 Power Density

Figure 2.15a shows the experimental prototype. Heatsink of the converter are assembled at the bottom. The overall converter size is 228 mm x 132 mm x 43 mm resulting in power density of 36 W/inch^3. Figure 2.15b shows the 3D bottom view and Figure 2.15c shows the 3D top view of the inverter.



(a) (b) (c)

Figure 2.15. (a) Hardware Prototype for the Proposed Topology at 3 kw, (b) 3D Bottom View of the Inverter Without Inductors and Heatsink, (c) 3D Top View of the Inverter Without Inductors

The volume distribution among different inverter components is shown in Figure 2.16 which shows that around 40% of the volume is taken up by the heat sink. The focus of the work has been on proving the performance of the topology and there is much room for further improvement in power density by optimized component placement, layout, thermal design, and packaging.

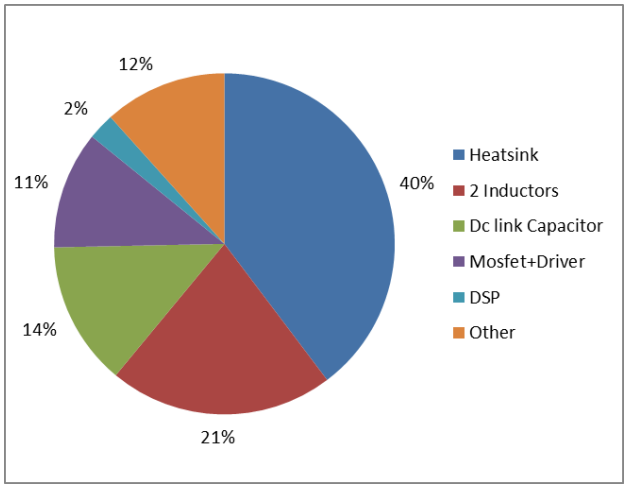


Figure 2.16. Volume Distribution Among the Inverter Components

2.5.3 Salient Experimental Waveforms

LeCroy 6200A oscilloscope is used to capture the waveforms. Power analyzer YOKOGAWA WT3000 is used to measure the efficiency. The results presented in this section correspond to the stand-alone configuration at rated power and different power factors. Figure 2.17 shows the experimental results of input voltage (v_{in}), load voltage (v_g), load current (i_g) and dc-link voltage (v_{link}) at 3 kW, UPF operation. The waveforms match very well with simulation results shown in Section 2.2. The load voltage has a THD of 2.1% calculated by using fast Fourier transform (FFT) in MATLAB on the measured load voltage data. At 3 kW, the 120 Hz ripple component is calculated to be 10 V pk-pk, which is around 2.5% of the RMS value of the input voltage.

Figure 2.18 shows the duty ratios of the boost stage and the half bridge inverter stage respectively. The duty ratio is obtained by cycle-by-cycle averaging of measured gate voltage (v_{gs}) of the two stages. As the v_{gs} is 20 V when turned on and -6 V when

turned off, the 0 and 1 of the duty ratio are plotted in Figure 2.18 correspondingly. The boost stage has a duty ratio of around 0.55 with 120 Hz component to make the input voltage a pure dc while the inverter stage duty ratio also contains 120 Hz components. It can be seen that these hardware results match well with the corresponding simulation results shown in Section 2.2.

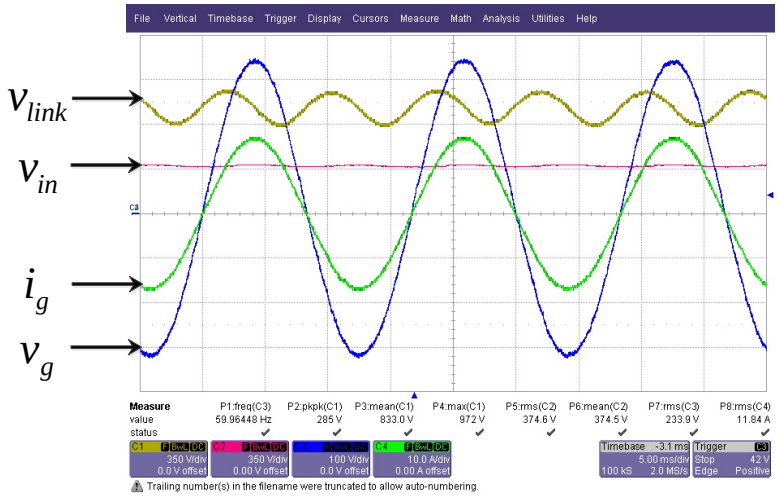


Figure 2.17. Experimental Results at 3 kVA, UPF (time scale 5 ms/div; v_{link}, v_{in}: 350 V/div; v_g: 100 V/div; i_g: 10 A/div)

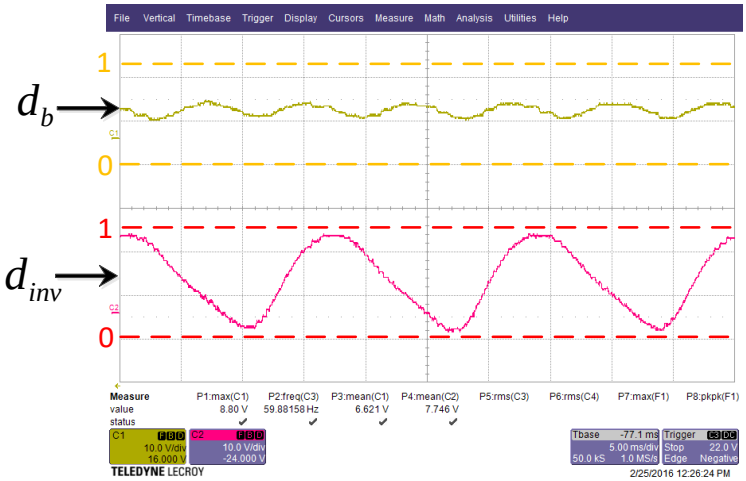


Figure 2.18. Cycle-by-cycle Averaged Duty Ratios of Boost Stage and Inverter Stage at 3 kVA, UPF (time scale 5 μs/div)

Figure 2.19 shows the drain to source voltage of the MOSFET Q_1 (v_{ds}) and the two inductor currents at 75 kHz to highlight some of the switching waveforms using SiC MOSFETs with dc-link voltage at 1 kV. The inductor currents have peak-peak ripple of around 13 A.

Figure 2.20 shows the input voltage, load voltage, load current, and dc-link voltage at 3 kVA with power factor of 0.7 leading which is the worst case operating condition as discussed previously. The experimental waveforms show excellent match with the simulation results and analysis, and confirm the undistorted operation at the worst-case power factor.

Figure 2.19. Experimental Results of Switch Drain to Source Voltage (v_{ds}) and Inductor Currents at 3 kVA, UPF (time scale 5 µs/div; v_{ds}: 200 V/div; i_b, i_{inv}: 20 A/div)

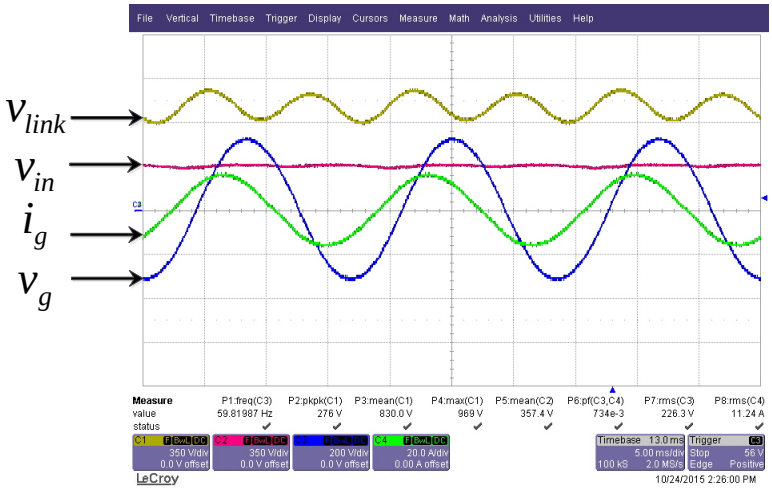


Figure 2.20. Experiment Results of 3 kVA, 0.7 Leading Power Factor (time scale 5 ms/div; v_{link}, v_{in}: 350 V/div; v_g: 200 V/div; i_g: 20 A/div)

2.5.4 Efficiency

Figure 2.21 shows the efficiency measured at different power levels based on California Energy Commission (CEC) requirement for PV converters. The measurements are done at two different switching frequencies for comparison – at 75 kHz and 100 kHz. The weighted CEC efficiency obtained is 96.4% at 75 kHz and 95.8% at 100 kHz switching frequency respectively without considering the controller power dissipation. The total auxiliary power consumption is 5.2 W with 1.6 W for fans and 3.6 W for other auxiliary components including the gate drivers, DSP controller, and other ICs. With the auxiliary power consumption included, the CEC efficiency will drop by around 0.4%. Improvements in magnetics design including integrated magnetics and optimization of the gate drive circuitry are being pursued currently to further improve the efficiency.

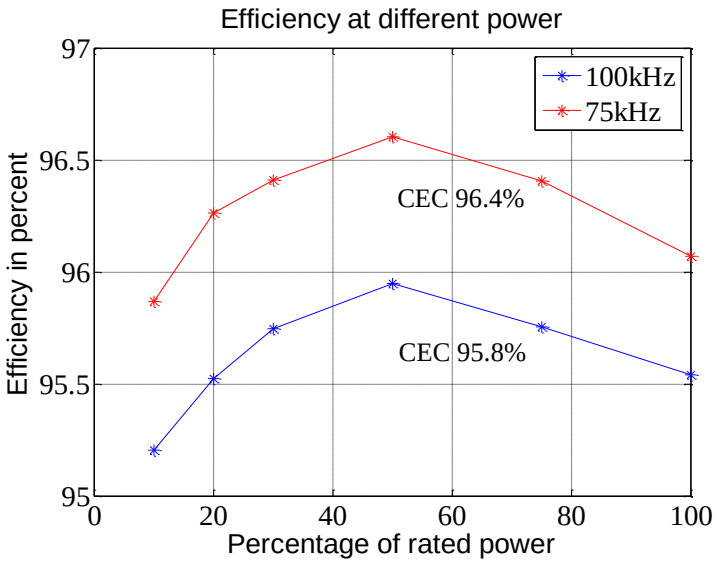


Figure 2.21. Measured Efficiency at Different Power Levels

2.5.5 Experimental Results for Dynamic Change in Power Factor and Active Power in Grid Connected Configuration

Due to the limitations of the test equipment, and to avoid operating the SiC MOSFETs too close to their absolute maximum voltage rating under transient conditions, the dynamic response experiments could be done only at lower ac voltage (120 V RMS) and dc voltage (200 V) levels. Figure 2.23 shows the transient waveforms of the inverter in grid connected configuration when the power factor command has a step change from 0.7 leading to 1 and from 1 to 0.7 lagging at 1 kVA. Good tracking of step power factor command changes and transient times well below one fundamental period can be observed from the waveforms shown in Figure 2.23.

Figure 2.23 shows the transient waveforms of the inverter in grid connected configuration when the active power command is given a step change from 500 W to 1 kW, and back from 1 kW to 500 W. Good tracking of step changes in active power command with transient times well below one fundamental period can be observed from

the waveforms shown in Figure 2.23. The input voltage also has a fast response, however, the dc-link voltage exhibits a much slower response due to the designed low bandwidth of the dc-link control loop.

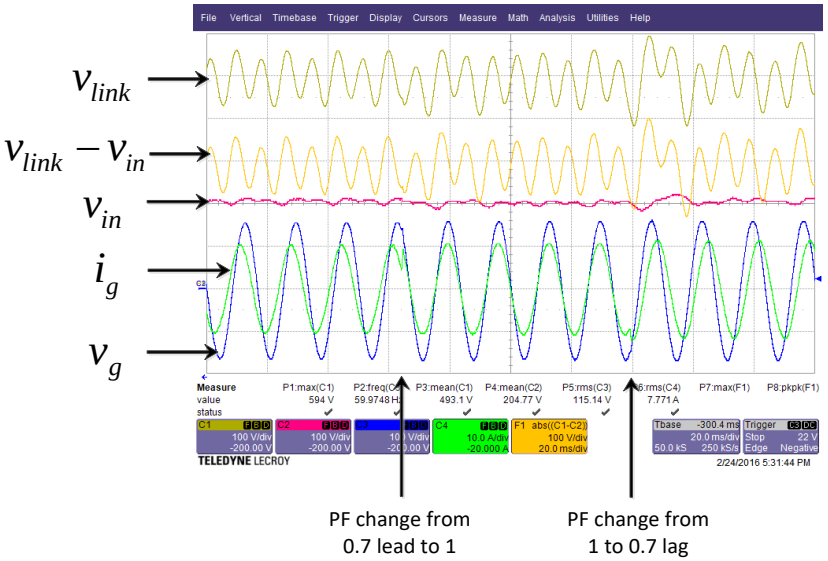


Figure 2.22. Power Factor Step Change at 1 kVA (time scale 20 ms/div; v_{link}, v_{in}, v_{link}-v_{in}, v_g: 100 V/div; i_g: 10 A/div)

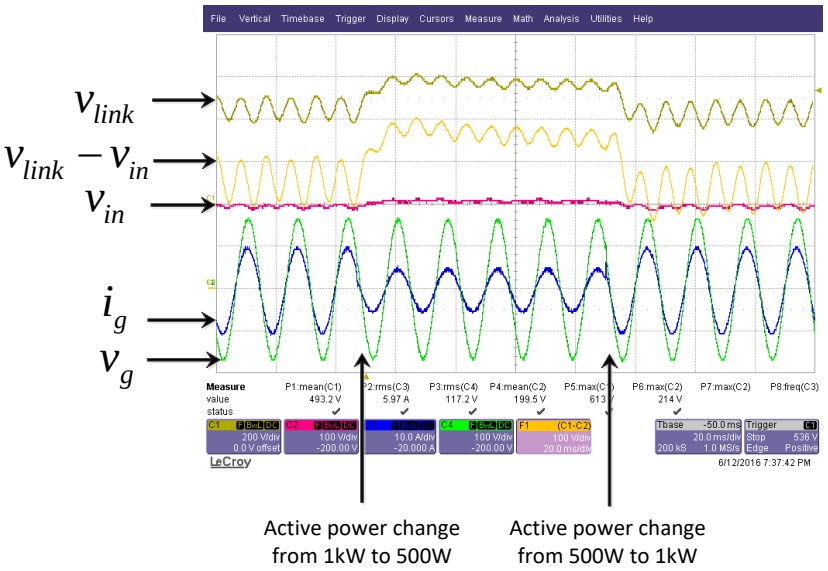


Figure 2.23. Dynamic Response to Step Changes in Active Power Command (time scale 20 ms/div; v_{link}: 200 V/div; v_{in}, v_{link}-v_{in}, and v_g: 100 V/div; i_g: 10 A/div)

CHAPTER 3 A GALLIUM-NITRIDE (GAN) BASED DOUBLY GROUNDED, REDUCED CAPACITANCE TRANSFORMER-LESS SPLIT PHASE PHOTOVOLTAIC INVERTER

A variation of the topology described in Chapter 2 for split-phase inverter applications and with significant added advantages is presented in this chapter. The proposed topology also effectively addresses the leakage current problem and 120 Hz power decoupling problem at the same time. High power density is achieved by reduced volume of both decoupling capacitors and filter inductors (by increasing the switching frequency with GaN switches). The control strategy of the proposed circuit is analyzed and the advantages of the proposed topology are shown. Compared with previous topology, the 120 Hz inductor current ripple in the boost stage is reduced significantly resulting in the decrease of the RMS current value by 14% and the peak current value by 41%. Also the RMS current in the input capacitor is decreased by 91%. The dc link capacitor volume is also decreased with the increase of the voltage level. A 3 kW single-phase prototype with 200 V DC nominal input and 120 V/60 Hz AC output in split phase configuration using GaN FETs is built and tested. Simulations results and their corresponding experimental results are presented to validate the theoretical analysis.

3.1 Topology and Control Scheme

Figure 3.1 shows the topology which consists of a boost stage and half bridge stages connected in split phase configuration which is the variation of the topology proposed in

[8] and the split-phase variation of the topology described in Chapter 2. The left part is the boost stage that controls the dc link voltage (v_{link}) to be around twice the input voltage (V_{in}) which represents the PV panel voltage. V_{in} and v_{link}–V_{in} form the two dc sources or voltage levels for the half-bridge inverter stage that controls the ac output voltage and shown at the right in Figure 3.1 The input voltage V_{in} is controlled to have negligible double line frequency ripple. The dc link voltage V_{link} is almost twice of the input voltage to supply sufficient voltage for the grid voltage modulation.

Due to the doubly grounded structure (the connection of the negative terminal of the PV panel and grid), there is little common mode leakage current which usually is a huge problem in the transformer-less PV string inverters.

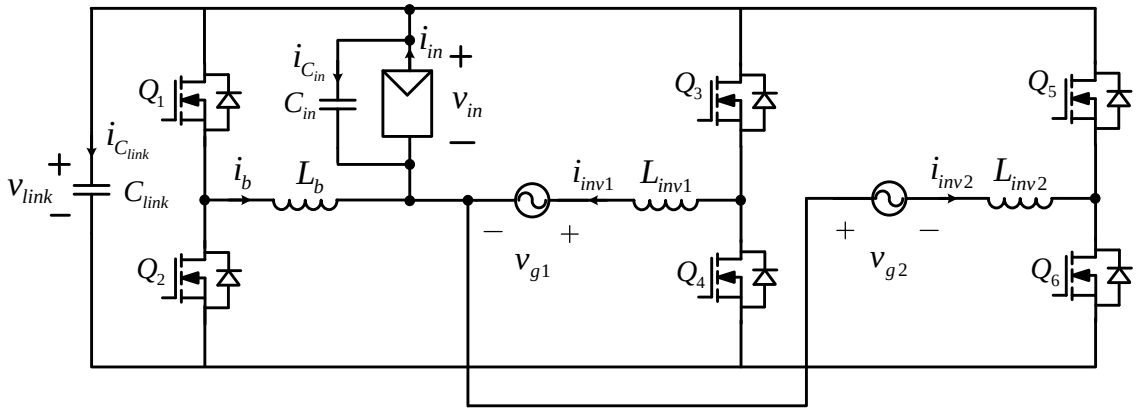


Figure 3.1. Proposed Topology of Doubly Grounded Transformer-Less Split Phase Inverter in Grid Connected Configuration

The dc link capacitor C_{link} will be used to decouple the 120 Hz power. Compared to the topology proposed in [8], the dc link capacitor C_{link} in this thesis is placed directly across the positive terminal and negative terminal to increase the voltage level of the capacitor and therefore decrease the capacitor volume. Also, instead of using 1.2 kV SiC

switches as implemented in [8] which has too much voltage margin, 650 V GaN FETs are used to improve the efficiency and get better circuit performance for the same application.

Figure 3.2 shows the control strategy for the proposed topology in Figure 3.1. V_{in} that represents the PV panel voltage and $v_{link} - v_{in}$ that is generated by the left dc-dc boost stage form 2 dc sources that will fulfill the modulation for the output voltage in standalone configuration or the output current in grid connected configuration. The PV panel voltage v_{in} is controlled to have negligible ripple to achieve high MPPT efficiency by using PR controller resonant at 120 Hz, and therefore, all the 120 Hz power component is supported by dc link capacitor C_{link}. The dc link voltage (v_{link}) average value is controlled by using a low bandwidth Butterworth filter and the output is the grid current magnitude reference which will then be used to regulate the grid current and therefore the power.

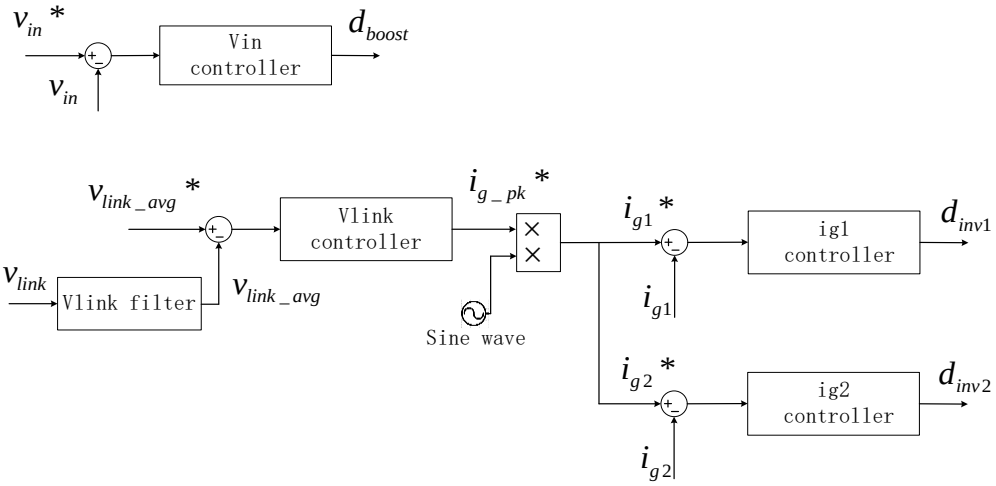


Figure 3.2. Control Strategy for the Topology in Figure 3.1

For the modulation requirement the following relationships of (3.1) always need to be satisfied to generate the output sine waves and similar requirement is true for the

second phase. (3.2) shows the decoupling capacitance relationship with power and can be used to calculate the decoupling capacitance needed.

$$\begin{cases} v_{in} > v_{g1} & v_{g1} > 0 \\ v_{link} - v_{in} > -v_{g1} & v_{g1} <= 0 \end{cases} \tag{3.1}$$

$$C_{link} = \frac{S}{\omega_0 v_{link\_avg} v_{link\_pkpk}} \tag{3.2}$$

3.2 Operating Principles and Simulation Results

The operation of the proposed inverter is analyzed and salient simulation waveforms in PLECS are shown. Simulation results are in standalone case with resistive load. To simulate the PV panel, a constant dc voltage source of 270 V will 5 ohm resistor is used.

Table 3.1 shows the specifications used in simulation as well as the designed hardware of the proposed topology.

Table 3.1. Main Circuit Specifications

Power	3 kW
Dc input voltage	200 V DC
Load voltage	120 V RMS
Load current	12.5 A RMS per phase
Power factor	1
Carrier frequency	100 kHz

Table 3.2 shows the details of the components used for the proposed topology. The dc link capacitance is around 40 uF, 550 V / kW allowing 150 V pk-pk ripple in the

dc link voltage and the max dc link voltage is 510 V which is limited by the GaN FETs voltage ratings. Also the input capacitance is very small which is only 3 uF.

Table 3.2. Components Details

Dc link capacitance (C_{link})	130 uF / 550 V
Dc input capacitance (C_{in})	3 uF / 200 V
Inverter side inductor (L_{inv})	210 uH
Boost side inductor (L_b)	210 uH
Switch	650V GaN System FET GS66516T
Inductor	Planar Ferrite Core 3C94 with Litz Wire

Figure 3.3 shows the simulation waveforms of the proposed topology. The output voltages are sinusoidal waveforms. The input voltage is controlled to be with extremely small ripple (less than 2% of the input voltage average value). The dc link voltage has large 120 Hz ripple which will decouple the 120 Hz power.

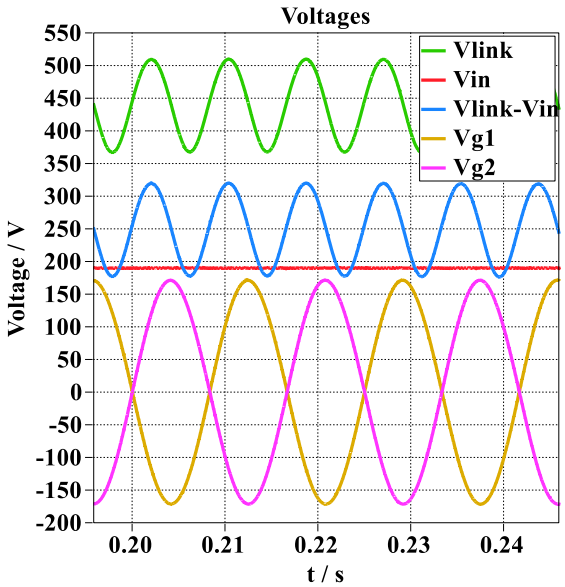


Figure 3.3. Dc Link Voltage, Input Voltage and Grid Voltages

Figure 3.4 shows the duty cycle of the boost stage and inverter stages from which it can be seen that due to the 120 Hz large swing in the dc link voltage, all duty cycles need to contain 120 Hz information to maintain the input voltage to be a pure dc and output voltage to be perfect sinusoidal waveforms which is achieved by well-designed controllers.

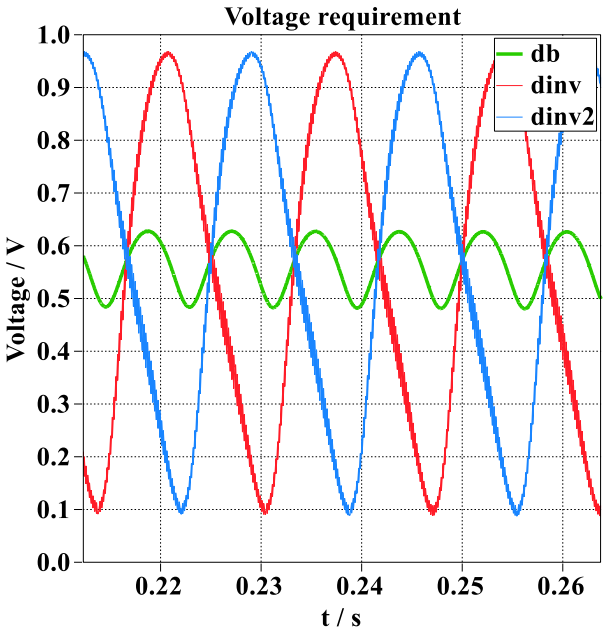


Figure 3.4. Boost Stage Duty Cycle and Inverter Stage Duty Cycles

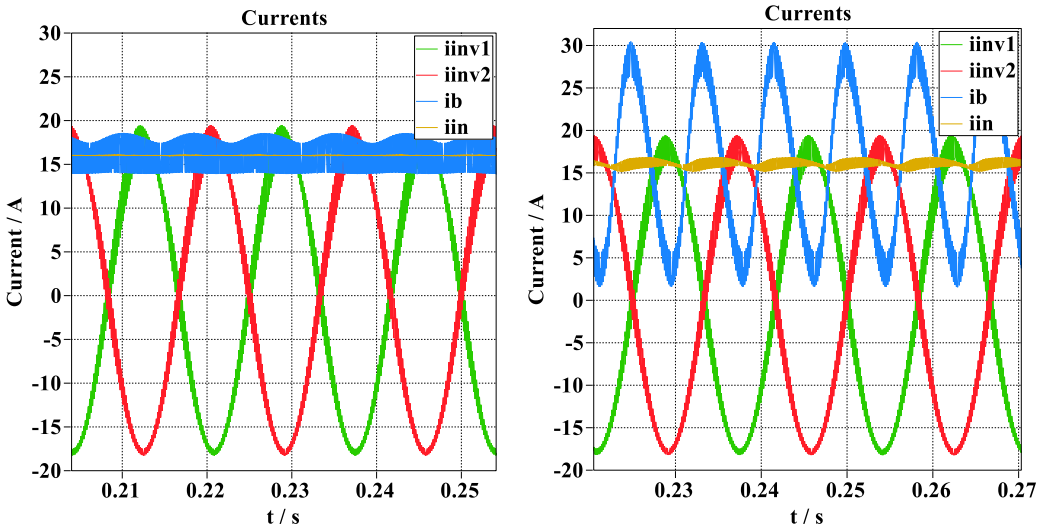
3.3 Topology Comparison

The advantages of the proposed topology will be analyzed in this section.

3.3.1 Inductors Comparison

Figure 3.5a shows the boost stage inductor current waveforms of the proposed topology. It can be seen that unlike the topology in [8] where the inductor current in dc-

dc stage has large 120 Hz ripple as shown in Figure 3.5b, the boost inductor current of the proposed topology is merely a pure dc with switching frequency ripple. Compared with previous topology in [8], the 120 Hz ripple component in the boost inductor current is reduced significantly resulting in the decrease of the RMS current value by 14% and the peak current value by 41%.



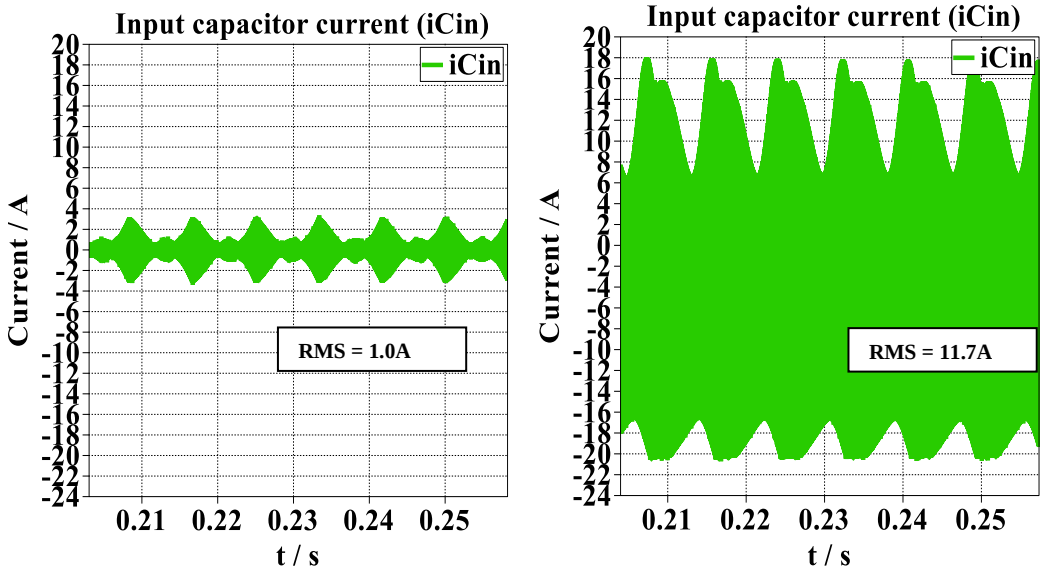
(a) Proposed topology (b) The topology in [8]

Figure 3.5. Boost Inductor Current, Input Current and Inverter Inductor Currents

3.3.2 High Frequency Content in Input Current

Figure 3.6a shows the input capacitor current of the proposed topology. As the dc-dc stage is inherently a boost stage which consists of a boost inductor at the input, the current ripple at the input capacitor is very small. Figure 3.6b shows the input capacitor current of the topology in [8]. Due to the topology difference, the dc-dc stage is a buckboost stage resulting in large current ripple in the input capacitor. The decrease of the RMS current in the input capacitor is 91% compared to the topology in [8]. The input

current is clean in the proposed topology and the input current in [8] contains large amplitude of switching frequency ripple which needs much larger input capacitor to filter which is the inherent disadvantage of the buckboost topology.



(a) Proposed topology (b) The topology in [8]

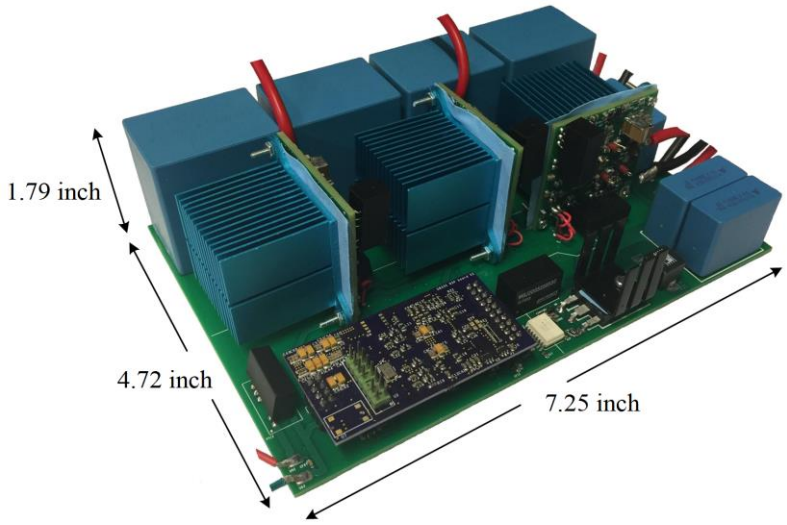
Figure 3.6. Input Capacitor Current

3.4 Hardware Implementation and Results

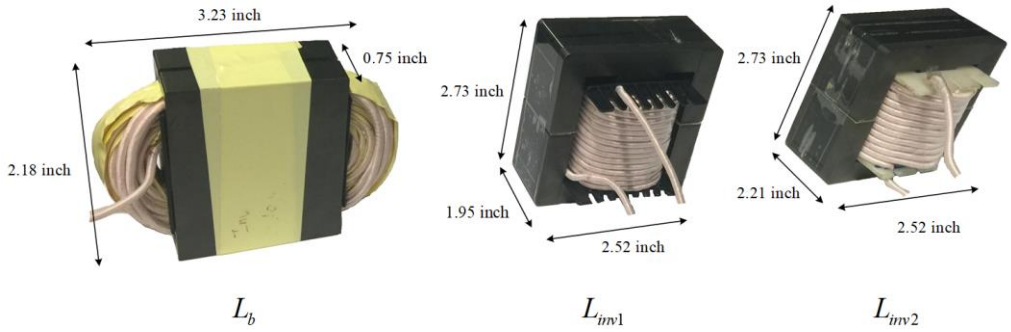
A 3 kW inverter using the proposed topology with LC filter and resistive load in standalone mode operating at 100 kHz switching frequency has been built to validate the proposed topology and corresponding benefits. All the components in Table 3.2 are designed for 3 kW operation.

Figure 3.7 shows the hardware prototype. 650 V GaN FETS GS66516T with 27 mohm R_{dson} from GAN SYSTEM are used for all the switches. A 230 V constant dc voltage source and a 5 ohm resistor in series are used to simulate the PV panel. The driver ICs are chosen as Silicon Labs Si8271. The positive gate voltage of the FET (V_{gs})

is 6.5 V and the negative is 0 V. LeCroy 6200A oscilloscope is used to capture waveforms. Power analyzer YOKOGAWA WT3000 is used to measure the efficiency. Inductors are built by hand using Ferrite core 3C94 with Litz wire. The TI DSP TMS320f28335 is used for control.



(a)



(b)

Figure 3.7. 3 kW Hardware Prototype of the Proposed Topology (a) Hardware Prototype, (b) Inductors Connected Externally

Figure 3.8 shows the experiment waveforms of the proposed topology. It can be seen that the output voltage are sinusoidal waves with THD < 2%. The dc link voltage is controlled to vary over a wide range which decouples the 120 Hz power. The input voltage (v_{in}) and the difference between the dc link voltage and the input voltage (v_{link} –

v_{in}) need to be both larger than the grid voltages as analyzed in (3.1) to ensure that the voltage modulation has enough margin and the output voltages are not distorted.

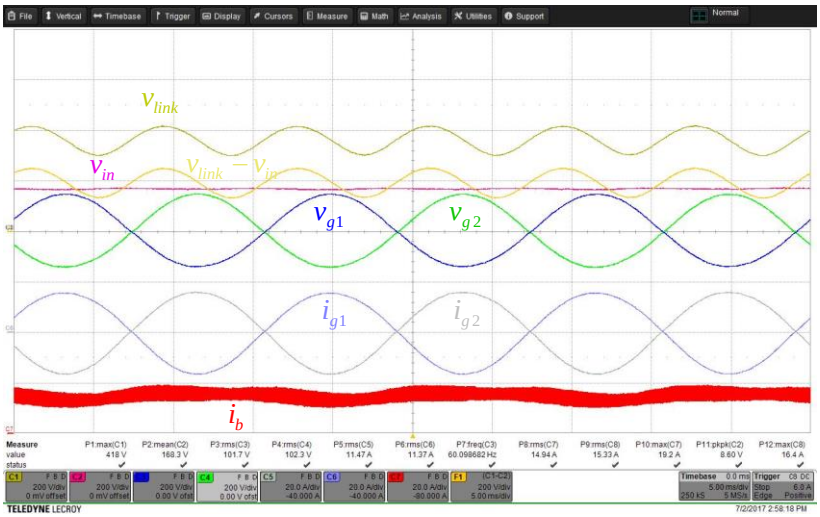


Figure 3.8. Waveforms of Dc link, Input and Output Voltages in Standalone Mode (time scale 5 ms/div, all voltages scale 100 V/div, all currents scale 20 A/div)

Figure 3.9 shows the 120 Hz ripple of the input voltage and current which is closely related to the MPPT efficiency. The input voltage is controlled to be with very small ripple (1.9% of the input voltage RMS value) and due to the 5 ohm resistor connected with the input dc voltage source to simulate the PV panel, the input current has a correspondingly 13% 120 Hz ripple of the of the input current RMS value. The boost inductor current is almost just a dc offset which is equal to the input current with some switching frequency ripple. The experiment waveforms match with the simulation results very well.

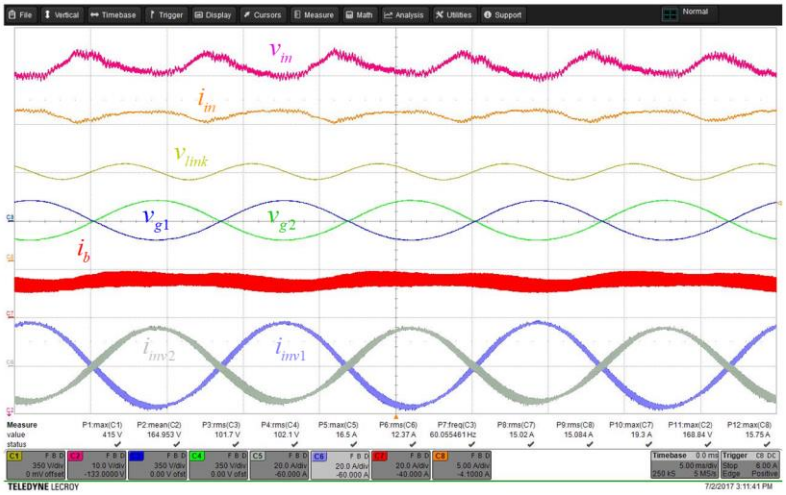


Figure 3.9. 120 Hz Ripple of Input Voltage and Current (time scale 5 ms/div, v_{link}, v_{g1},v_{g2} scale 350 V/div, v_{in} scale 10 V/div, i_{in} scale 5 A/div, i_b, i_{inv1}, i_{inv2} scale 5 A/div)

Figure 3.10 shows the duty cycle of boost stage and inverter stages from which it can be seen that to maintain a dc input voltage the duty cycle of the boost stage needs to contain some 120 Hz information. Also to have a sinusoidal output voltage the inverter stages duty cycle need to have 120 Hz information too which come from the output of the high bandwidth controllers.

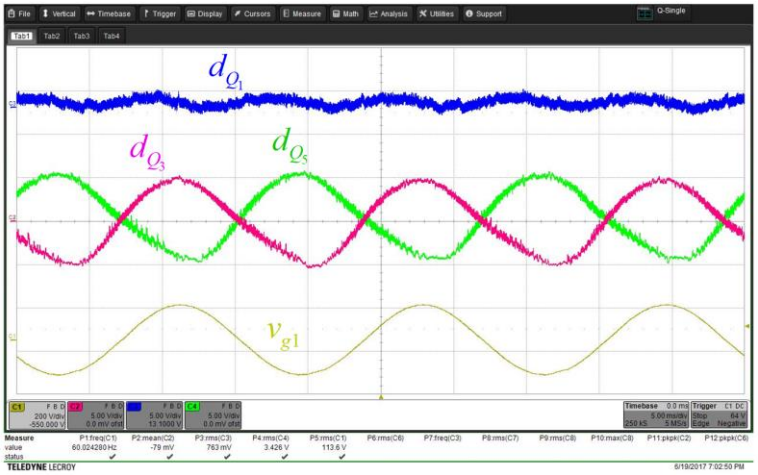


Figure 3.10. Waveforms of duty cycle of boost stage and inverter stages

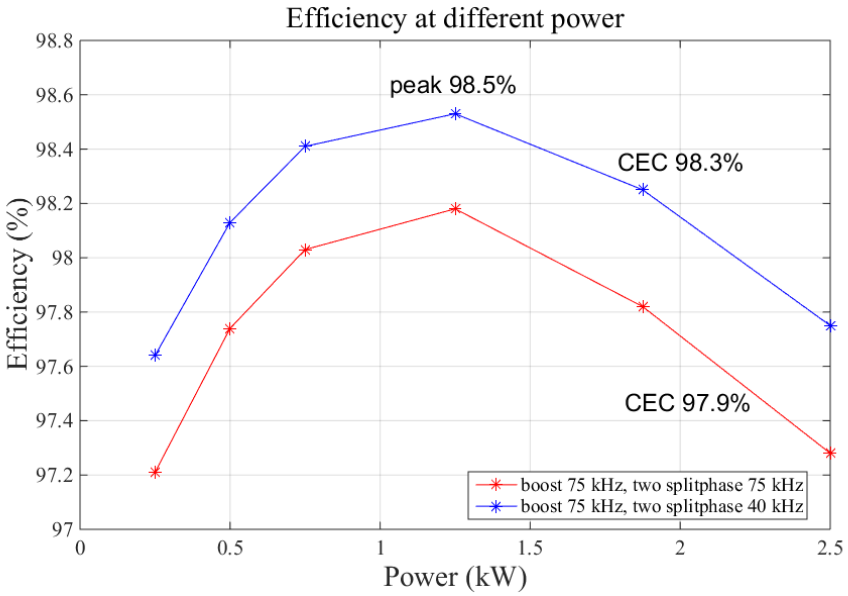


Figure 3.11. Measured Efficiency at Different Power Levels for GaN Split Phase Prototype

Figure 3.11 shows the efficiency measured at different power levels based on California Energy Commission (CEC) requirement for PV converters. The measurements are done at two different switching frequencies for comparison – at all 75 kHz and boost stage 75 kHz and inverter stage 50 kHz. The weighted CEC efficiency obtained is 98.3% with peak efficiency 98.5%. The total auxiliary power consumption is 4.1 W for other auxiliary components including the gate drivers, DSP controller, and other ICs. With the auxiliary power consumption included, the CEC efficiency will drop by around 0.3%. Improvements in magnetics design including integrated magnetics and optimization of the gate drive circuitry are being pursued currently to further improve the efficiency.

CHAPTER 4 INDUCTOR FEEDBACK ZVT BASED, LOW THD SINGLE PHASE FULL BRIDGE INVERTER WITH HYBRID MODULATION TECHNIQUE

This Chapter presents a new ZVT techniques for single phase full bridge inverters. Though the mechanism by which soft switching is achieved is similar for the numerous converters implementing ZVT technique, the exact configuration in terms of where the auxiliary circuit is connected to the main circuit, how the driving voltage for the auxiliary circuit is obtained and also the switching strategy for the auxiliary circuit have a major impact on the performance of overall converter system. To overcome some drawbacks of the aforementioned ZVT techniques as discussed in Section 1.2, this thesis proposes an inductor feedback ZVT circuit implementation that allows unipolar PWM or hybrid PWM modulation and therefore can decrease the output THD significantly with simple auxiliary circuit. In hybrid modulation, two of the four switches are driven by high switching frequency PWM signals for high quality sinusoidal output and the other two are commutated at the low, fundamental frequency [94]-[96].

4.1 Topology

Figure 4.1 shows the proposed topology employing the hybrid modulation with low-loss ZVT technique for single phase full bridge inverters. Instead of placing the auxiliary ZVT branch which consists of two switches and a small value inductor across the two switching poles as used in [85] and [88], this thesis places the auxiliary ZVT

circuit across the main filter inductor. As the output voltage v_o is always smaller than the input voltage V_{dc} because of the modulation requirement, v_o and V_{dc} - v_o can be the excitation source and the reverse excitation source respectively. Therefore, in addition to the positive state and negative state in the switching pole, zero state also can be achieved while implementing the ZVT auxiliary circuit to realize full ZVS of the main switches. To implement modulation technique including zero state, both unipolar PWM and hybrid PWM modulation can be used. However, from the perspective of easy implementation of the modulation scheme together with ZVT timing, hybrid PWM is used in this thesis.

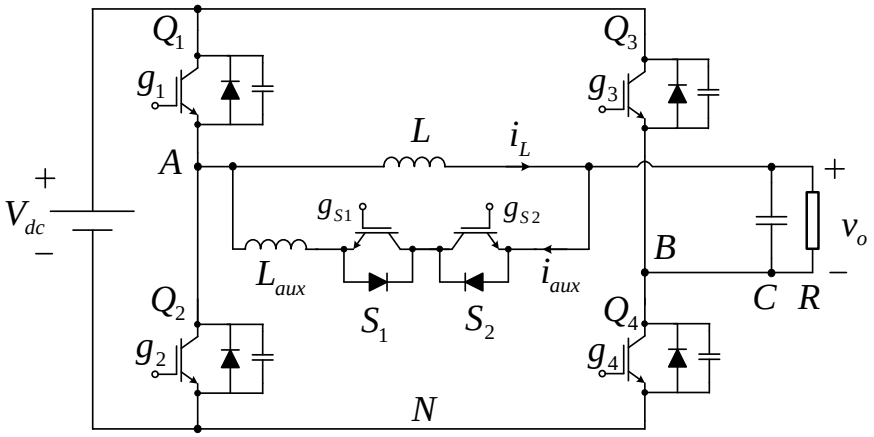


Figure 4.1. Proposed Topology of Hybrid Modulation and ZVT Technique for Full Bridge Inverters

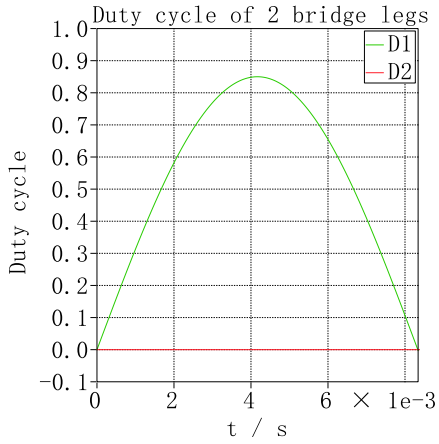
4.2 Analysis of Operation

The operation principles are analyzed in this section.

4.2.1 Hybrid Modulation with ZVT Realization

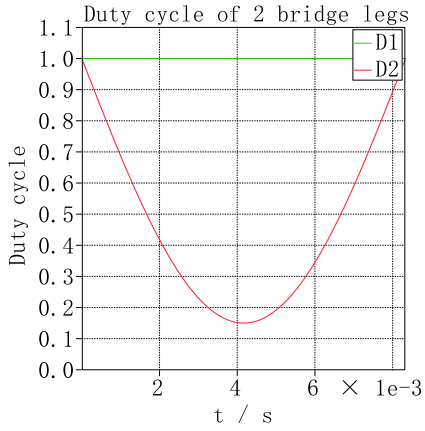
The modulation scheme is shown in Figure 4.2 where d is the duty cycle as same in the unipolar modulation (ranging from -1 to 1) and i_L is the output inductor current as

shown in Figure 4.1. The green waveforms labelled D_1 are the duty cycle given to Q_1 while the red waveforms labelled D_2 are the duty cycle to Q_3. Q_2 and Q_4 are complementary to Q_1 and Q_3 respectively. d equals to $D_1 - D_2$.



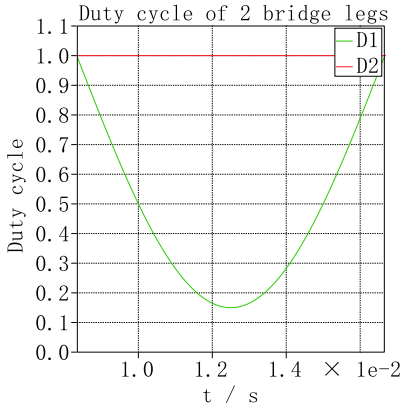
Q_4 on, Q_3 off, Q_2 achieves natural ZVS by i_L, Q_1 achieves ZVT by S_1

(a) $d > 0 \quad i_L > 0$



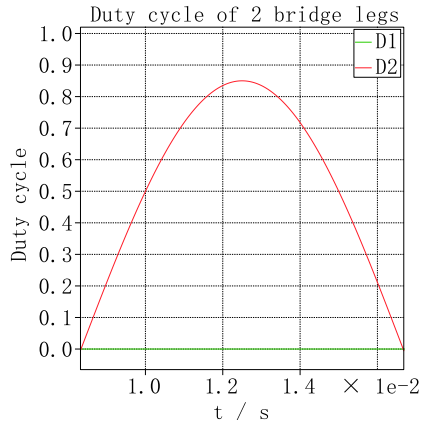
Q_1 on, Q_2 off, Q_4 achieves natural ZVS by i_L, Q_3 achieves ZVT by S_2

(b) $d > 0 \quad i_L <= 0$



Q_3 on, Q_4 off, Q_2 achieves natural ZVS by i_L, Q_1 achieves ZVT by S_1

(c) $d <= 0 \quad i_L > 0$



Q_2 on, Q_1 off, Q_4 achieves natural ZVS by i_L, Q_3 achieves ZVT by S_2

(d) $d <= 0 \quad i_L <= 0$

Figure 4.2. Hybrid Modulation Scheme with ZVT

This strategy can realize ZVS of all switches at any power factor. Take the condition of $d > 0$ and $i_L > 0$ for example, Q_2 and Q_3 can achieve natural ZVS because i_L is

positive [69]. As $d > 0$ the positive state and zero state are needed which means Q_1 and Q_4 are needed. The strategy is that Q_4 is always ON which means the second bridge is clamped to the negative bus. Then Q_1 is ON when positive state is needed, Q_2 is ON when zero state is needed. As mentioned above, Q_2 can achieve natural ZVS by i_L while Q_1 achieves ZVT by S_1. The scheme is capable of supporting non-unity power factors, but if the power factor is 1 the modulation strategy is relatively easier to implement compared to other power factors.

4.2.2 Detailed Analysis of Commutation Process

The ZVT auxiliary branch drives a different direction of current though the auxiliary inductor and thus changing the switching pole current direction to achieve ZVS turn on of the main switches. Therefore, before turn-on of the main switches which cannot realize natural ZVS, ZVT auxiliary circuit will be turned on in advance to change the switching pole current direction.

The commutation process of the ZVT will be analyzed in this section. Take the condition of $d > 0$ and $i_L > 0$ for example where Q_4 is always ON and Q_3 is always OFF and Q_1 and Q_2 are switching to generate positive and zero states. Also Q_2 can achieve natural ZVS by i_L while Q_1 achieves ZVT by S_1.

Figure 4.3 shows the timing of the proposed hybrid modulation with ZVT scheme.

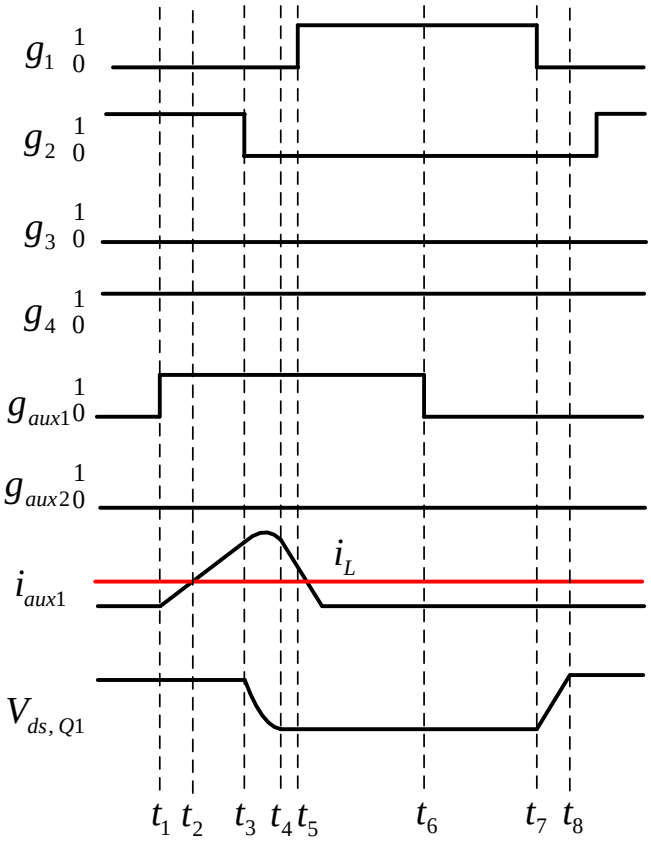


Figure 4.3. Timing Diagram of Proposed ZVT with Hybrid Modulation

Figure 4.4 shows commutation stages corresponding to the timing in Figure 4.3. The commutation stages include:

(a) Initial stage [before t_1]. Q_2 is ON, the main inductor current i_L flows through Q_2 channel and Q_4 channel

(b) Pre-charging stage [t_1~t_2]. S_1 is turned-on at t_1, the output voltage v_o is applied to the resonant inductor L_{aux}, i_{aux} which flows through the channel of S_1 and body diode of S_2 increases linearly, current in Q_2 channel decreases to zero at t_2.

(c) Boost-charging stage [t_2~t_3]. i_{aux} is linearly charged to a current well above the inductor current i_L. This will make sure $V_{ds,Q1}$ (the drain to source voltage of the Q_1 switch) resonates to zero in resonant stage t_3~t_4.

(d) Resonant stage [t_3~t_4]. Q_2 is turned-off at t_3, L_{aux} starts to resonant with C_{ds1} and C_{ds2} (the drain to source capacitance of the Q_1 switch and Q_2 switch respectively) until $V_{ds,Q1}$ resonates to zero and $V_{ds,Q2}$ resonates to V_{dc}.

(e) Clamping stage [t_4~t_5]. When $V_{ds,Q1}$ resonates to zero, D_1 (the body diode of the switch Q_1) naturally turns-on at t_4. The voltage of $-(V_{dc} - v_o)$ is applied to L_{aux}, i_{aux} decreases. During this stage, $V_{ds,Q1}$ is clamped to 0 until t_5, Q_1 can be ZVS turned-on in this stage before i_{aux} is smaller than i_L.

(f) Discharging stage [t_5~t_6]. i_{aux} is discharged to zero, current in Q_1 linearly increases to i_L. S_1 can be ZCS turned-off before t_7, ZVT transition ends.

(g) Steady-state stage [t_6~t_7]. Q_1 fully conducts the load current i_L.

(h) Snubber turn-off stage [t_7~t_8]. Q_1 is turned-off at t_7, i_L linearly charges C_{ds1} and discharges C_{ds2} until $V_{ds,Q1}$ reaches V_{dc}, dv/dt is limited by C_{ds1} and C_{ds2}.

(i) Steady-state stage [after t_8]. When $V_{ds,Q2}$ reaches to zero, D_2 is naturally turned-on, and then Q_2 can be ZVS turned-on after t_8 resulting in natural ZVS of Q_2 by main inductor current i_L.

From the analysis above it can be seen that the auxiliary switches in the ZVT circuit can achieve ZCS turn on and ZCS turn off but the energy is the C_{ds} of the auxiliary switch will be dissipated.

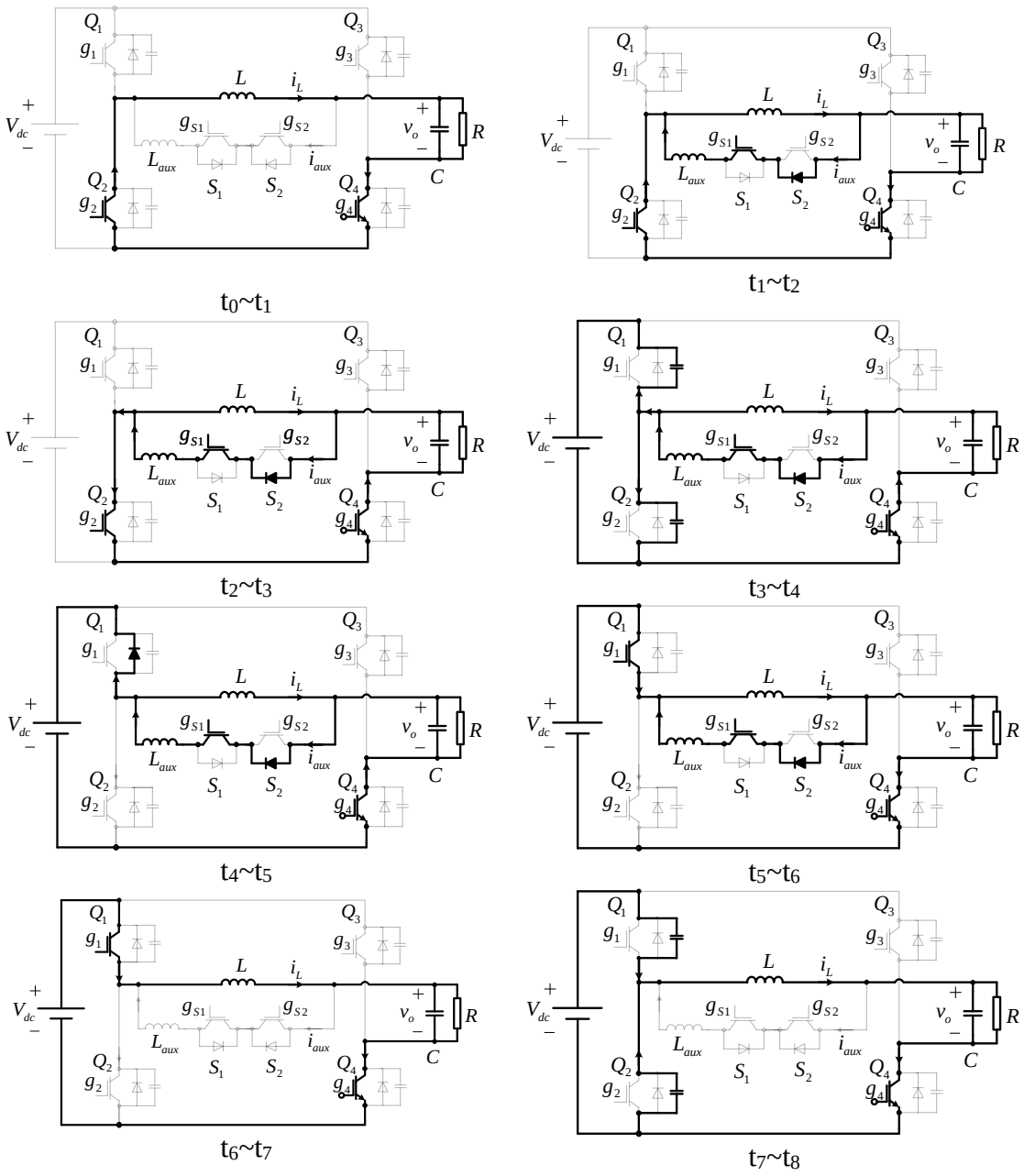


Figure 4.4. Commutation Stages of the Proposed Inverter

4.3 Modelling of the Proposed Topology

The analysis above is done when the power factor is 1. For non-unity power factor case, as the inductor current and the output voltage are not in phase, the adaptive auxiliary current is not as advantageous as the case when power factor is 1. However, for typical PV applications the power factor is usually 1 or close to 1 such as 0.8. Therefore, for typical grid connected converters with non-unity power factor, the scheme can still work well and offers most of the benefits as analyzed in the previous section.

Figure 4.5 shows the large signal model corresponding to the circuit of Figure 4.1 where the ZVT auxiliary circuit is modelled as a current source which is dependent on the circuit parameters. As analyzed in the section 4.2 the auxiliary inductor current i_{aux} will add to the main inductor current and will influence the output voltage ripple if i_{aux} is large enough or if the ZVT timing takes up to a significant portion of the switching cycle when the switching frequency is high enough.

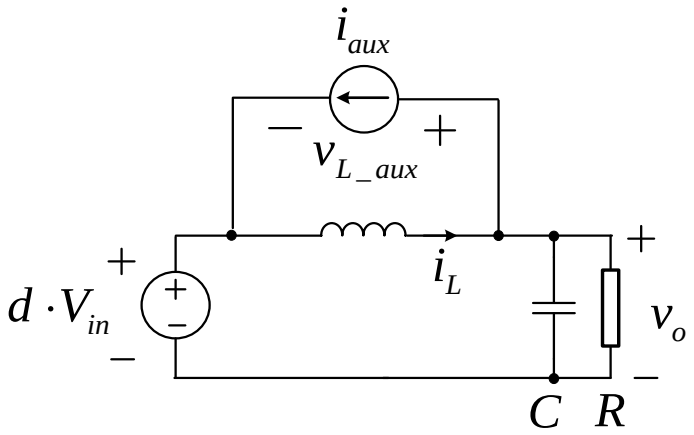


Figure 4.5. Large Signal Model of the Proposed Inverter

Figure 4.6 shows the dead time scheme implemented which is to delay the turn-on (up edge) of the switch by the dead time while still maintaining the turn-off time exactly the same as the case without dead time. Due to the ZVT circuit used, the dead time effect

that used to influence the actual duty ratio is not seen anymore. Because when the switch is turned off, the switching pole current, either the main inductor current or (?) the ZVT auxiliary current minus the main inductor current, will drive the body diode of the switch to be turned on.

For example, when the output voltage is in its positive half cycle and the inductor current is in phase of the output voltage, during positive state the switching pole current will be main inductor current and will drive on the body diode of the switch Q_2, during zero state the ZVT auxiliary current minus the main inductor current will be the switching pole current and will drive the switch Q_1. In either case the switching pole voltage relative to the common source which is the point N in Figure 4.1 will be exactly the same compared with the case with no deadtime.

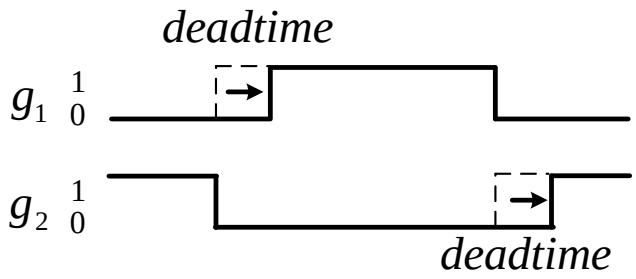


Figure 4.6. Dead Time Scheme

Therefore equation (4.1) and (4.2) can be derived, where A, B and N refer to the points in Figure 4.1.

$$V_{AN} = d_1 V_{dc} \quad V_{BN} = d_2 V_{dc} \tag{4.1}$$

$$V_{AB} = V_{AN} - V_{BN} = dV_{dc} \tag{4.2}$$

(4.3) and (4.4) are the differential equations of the main inductor current and output voltage, where i_L is the main inductor current, v_o is the output voltage, L is the main

inductance, *C* is the output filter capacitor, R is the resistive load and $\overline{i_{aux}}$ is average value of the auxiliary ZVT branch current in every switching cycle.

$$\dot{i}_L = \frac{1}{L}(d \cdot V_{dc} - v_o) \tag{4.3}$$

$$\dot{v}_o = \frac{1}{C}(i_L - \overline{i_{aux}} - \frac{v_o}{R}) \tag{4.4}$$

It should be noted that the auxiliary inductor current i_{aux} is reset to 0 in every ZVT transition so that it does not form a state in the analysis. However the average value of the i_{aux} can influence the output voltage.

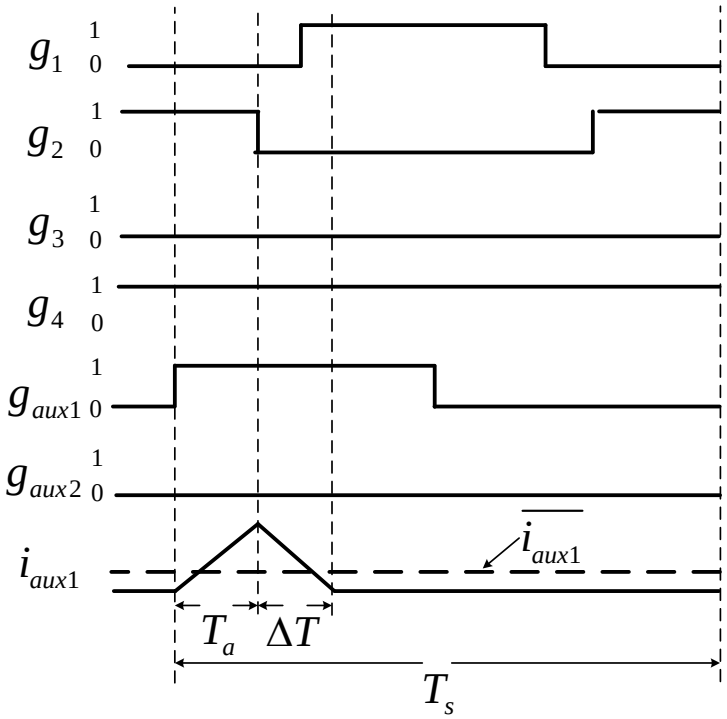


Figure 4.7. Simplified Timing for Calculation of the Large Signal Model of the Proposed Inverter

Figure 4.7 shows the simplified timing diagram for analyzing the large signal model of the proposed circuit by neglecting the resonant part in t_3~t_4 which usually takes

a small portion during the whole transition time as shown in Figure 4.7. T_a is the ahead time which is the time difference between the turn-on of the auxiliary switch and the turn-off of the main switch. ΔT is the time when the auxiliary current falls from the peak value to 0. T_s is the cycle, L_{aux} is the auxiliary inductance. From the analysis (4.5) can be derived.

$$\begin{aligned}
&(0, T_a) && L_{aux}\,\dot{i}_{aux} = v_o \\
&(T_a, T_a + \Delta T) && L_{aux}\,\dot{i}_{aux} = -(V_{dc} - v_o) \quad if\ v_o > 0 \\
& && L_{aux}\,\dot{i}_{aux} = -(-V_{dc} - v_o) \quad if\ v_o <= 0 \\
&(T_a + \Delta T, T_s) && L_{aux}\,\dot{i}_{aux} = 0
\end{aligned} \tag{4.5}$$

As the auxiliary current needs to be reset to 0 every cycle, it does not form a state and the equation (4.6) is satisfied,

$$T_a \cdot |v_o| = \Delta T (V_{dc} - |v_o|) \tag{4.6}$$

The average value of the auxiliary current over a switching cycle can be calculated as (4.7),

$$\overline{i_{aux}} = \frac{T_a v_o}{2 L_{aux} T_s} \cdot T_a + \frac{T_a v_o}{2 L_{aux} T_s} \cdot \Delta T \tag{4.7}$$

Therefore the output voltage is written as (4.8), (4.7) and (4.8) form the large signal state space model of the proposed inverter.

$$\dot{v}_o = \frac{1}{C}\left(i_L - \frac{T_a^{\,2}}{2 L_{aux} T_s} \cdot \frac{V_{dc} v_o}{V_{dc} - |v_o|} - \frac{v_o}{R}\right) \tag{4.8}$$

4.4 Design of Components and Timings

Before the linear region ends which is t_3, (4.9) satisfies,

$$i_{aux} = \frac{v_o}{L_{aux}}(t - t_1) \tag{4.9}$$

During the resonant region between t_3 and t_4, (4.10) satisfies if the time is designed to be around ¼ cycle of the resonant frequency,

$$T_{res} = \frac{2\pi\sqrt{L_{aux}2C_{ds}}}{4} \tag{4.10}$$

After t_4, as the negative voltage source is applied on the auxiliary inductor, the auxiliary current starts to decrease as shown in (4.11)

$$i_{aux} = \frac{V_{in} - v_o}{L_{aux}}(t - t_4) \tag{4.11}$$

The parameters including L_{aux}, T_{blank}, L_{ahead}, C_{ds} and be independent parameters that can affect the performance of the inverter and efficiency. Also due to the DSP control accuracy and feasibility to achieve the auxiliary inductance, optimization is done in MATLAB to determine the values of the auxiliary circuit as shown in the hardware implementation section.

4.5 Hardware Implementation and Results

A 1 kW inverter using the proposed topology with LC filter and resistive load operating at 400 kHz switching frequency has been built to verify the proposed ZVT with hybrid modulation technique. The power factor is 1 and the modulation ratio is 0.9 which represents a typical PV standalone application.

The specifications of the inverter and the ZVT auxiliary circuit parameters are shown in Table 4.1. The deadtime (which equals to $t_5 - t_3$ in Figure 4.3) is set to 70 ns.

The ahead time, which is the time between the auxiliary switch gate signal and the lower switch gate signal (which is $t_3 - t_1$ in Figure 4.3), is set to 160 ns. External capacitor of 180 pF is added in parallel with C_{ds} of the main switches of the full bridge to decrease the turn-off loss of the main switches while maintaining the ZVS turn-on. The timings and auxiliary inductance are designed based on loss calculation and optimization.

SiC MOSFETS C2M0080120D from CREE are used in full bridge main circuit and auxiliary ZVT circuits. The driver ICs are chosen as Avago ACPL 337J. The positive gate voltage of the MOSFET (V_{gs}) is 20 V and the negative is -5V. In order to reduce the diode recovery loss, 4 SiC schottky diodes are put in parallel to the 4 main switches. LeCroy 6200A oscilloscope is used to capture waveforms. Ferrite core with Litz wire are used for the main output inductor.

Table 4.1. Circuit Specifications

Power	1 kW
Dc input voltage (V_{in})	210 V
Load voltage (v_o)	120 V
Load current	8.3 A
Power factor	1
Filter inductor (L)	200 uH
Switching frequency	400 kHz
Auxiliary inductance (L_{aux})	400 nH
Blanking time ($t_5 - t_3$)	70 ns
Ahead time (T_a)	160 ns

The timings and auxiliary branch components are selected based on the optimization process to decrease the auxiliary branch loss which includes the core loss and copper loss of the auxiliary inductor, switching loss and conduction loss of the auxiliary

switch and the conduction loss of the auxiliary diode. As the auxiliary diode is Schottcky diode therefore there is basically no diode recovery loss.

Figure 4.8 shows the hybrid modulation scheme and ZVT gate signals along with the inductor current for reference. It can be seen that the hybrid modulation scheme is implemented.

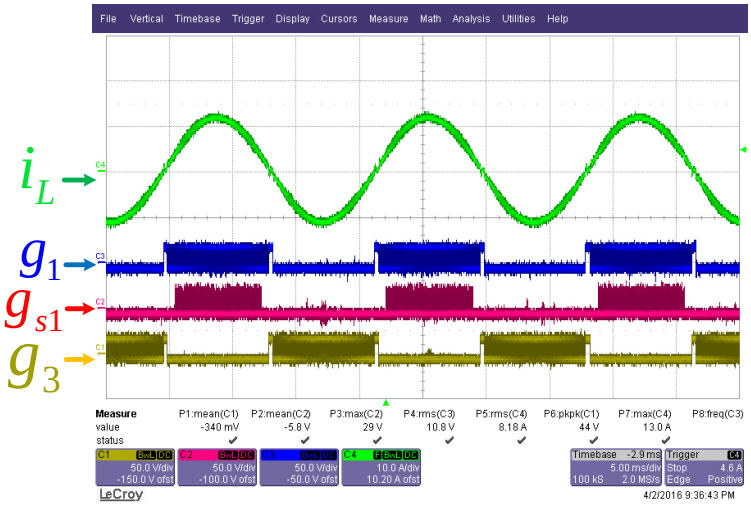


Figure 4.8. Hybrid Modulation Scheme and ZVT Gate Signal (time scale 5 ms/div, i_L scale 10 A/div, g_1, g_{aux1}, g_4 scale 50 V/div)

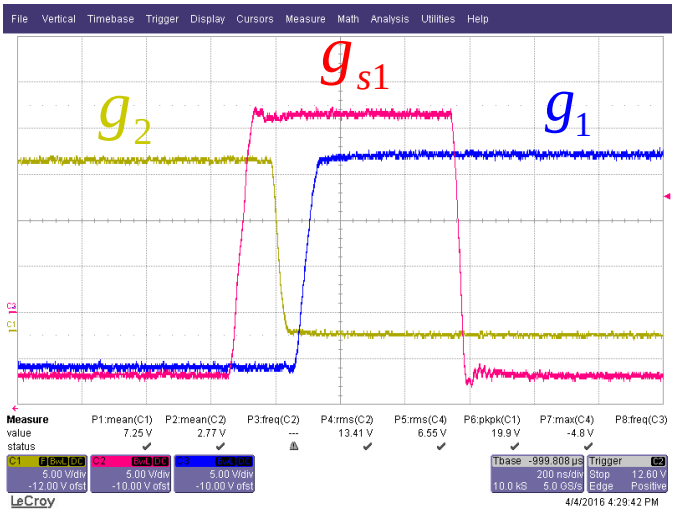


Figure 4.9. ZVT Timing with Blanking Time of 70 ns and ahead time of 160 ns (time scale 200 ns/div, g_2, g_{s1}, g_1 scale 5 V/div)

Figure 4.9 shows the timing of the ZVT where the blanking time is 70 ns and the ahead time is 160 ns as analyzed in Figure 4.3.

Figure 4.10 shows the ZVT inductor waveforms. It can be seen that the ZVT inductor current changes along with the main inductor current because the excitation source of the ZVT inductor current is the output voltage. Therefore the ZVT inductor current will always be changing adaptively to the main inductor current which is better compared with the scheme of [85] and [88] because they should design the ZVT inductor current using the largest main inductor current.

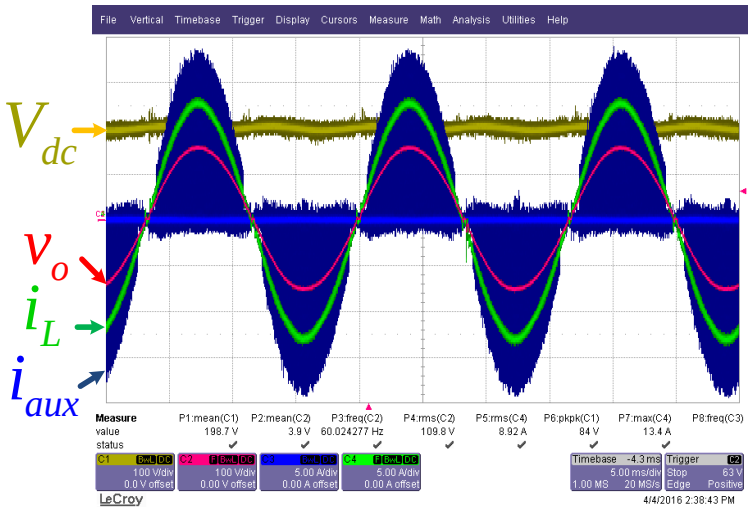


Figure 4.10. Auxiliary Inductor Current Compared to Main Inductor Current (time scale 5 ms/div, V_{dc}, v_o scale 100 V/div, i_L, i_{aux} scale 5 A/div)

Figure 4.11 shows the waveforms of the ZVT process of the main switch Q_1 which include the drain to source voltage of the Q_1 switch ($V_{ds,Q1}$), the gate to source voltage of the Q_1 switch (g_1), the inductor current (i_L) and the auxiliary inductor current (i_{aux1}). It can be seen that the auxiliary inductor current is larger than the value of the inductor current

for some time which means it can discharge the drain to source capacitance of the Q_1 switch (C_{ds1}) as analyzed in the Section 4.2 commutation stages part to achieve ZVT of Q_1. The drain to source voltage of the Q_1 switch has already fallen to 0 before the gate signal is applied proving that Q_1 realizes soft turn-on.

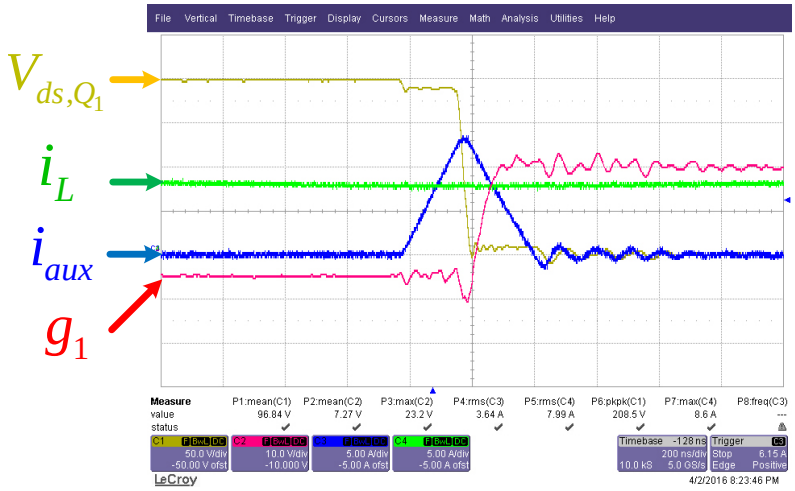


Figure 4.11. ZVS Turn on of Main Switch Q_1 (time scale 200 ns/div, $V_{ds,Q1}$ scale 50 V/div, g_1 scale 10 V/div, i_L scale 5 A/div, i_{aux} scale 5 A/div)

Figure 4.12 shows the measured loss using power analyzer YOKOGAWA WT3000 at different power levels for three different cases – base case (no ZVT) and the proposed ZVT. It can be seen that the proposed ZVT scheme can improve the system overall efficiency significantly from CEC 95.3% to CEC 96.3%.

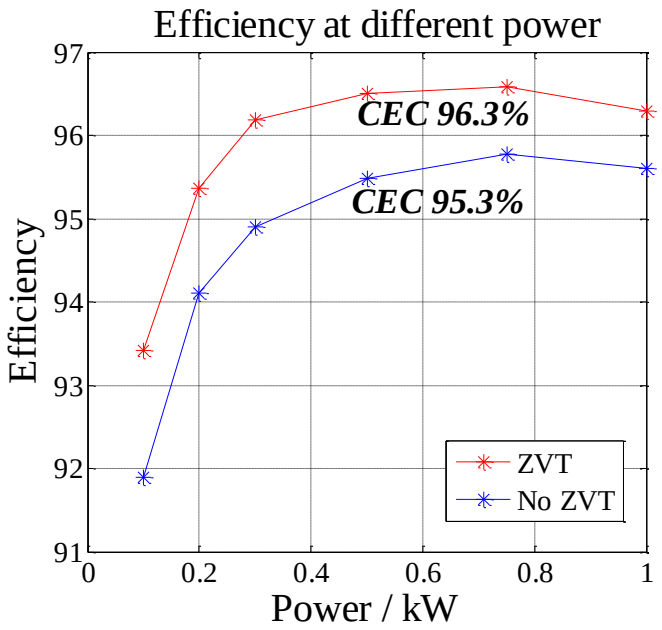


Figure 4.12. Efficiency of the Full Bridge Inverter with and without ZVT

The independent loss that cannot be changed by ZVT includes the switch conduction loss and inductor loss. The conduction loss of the main four switches which is same in all the above three schemes are calculated using $P_{con} = 2I^2R_{ds,on}{}^2$= 15.5 W. The inductor loss is estimated to be 4 W. The core loss and copper loss are small because ferrite core with Litz wire are used and the switch frequency is high enough which results in the max current ripple of 0.2 A pk-zero. The full bridge switching loss without ZVT is 44 W. The full bridge switching loss and ZVT auxiliary circuit and buck stage total loss is 36 W. After subtracting the independent loss, the proposed ZVT saves up to 32 % of the original switching loss of the full bridge inverter.

CHAPTER 5 OPTIMAL VARIABLE SWITCHING FREQUENCY SCHEME TO IMPROVE EFFICIENCY OF SINGLE PHASE GRID CONNECTED INVERTER

This chapter aims to develop the optimal variable switching frequency scheme to minimize overall loss in a grid-connected H-bridge inverter (loss in switch and inductor) that is not well studied in previous publications which mainly focus on only the device switching loss.

5.1 Analysis of Current Ripple and Losses in the Switches and Inductor

Figure 5.1 shows the studied H-bridge grid-connected inverter and four main types of losses. The optimal scheme is to minimize the total loss of the inverter while keeping the inductor current THD unchanged by designing a variable switching frequency method.

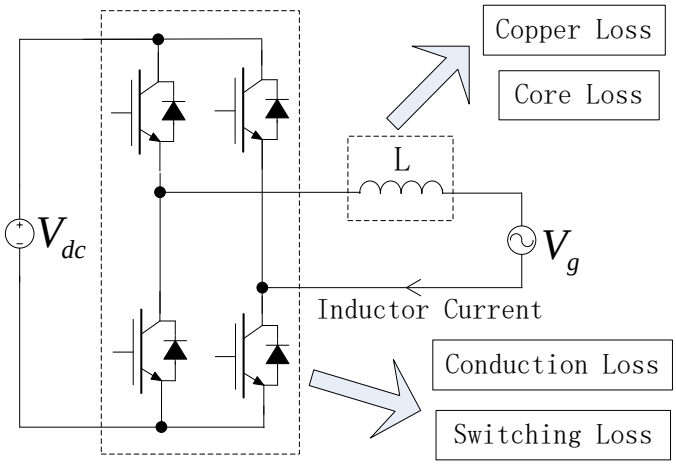


Figure 5.1. Schematic of the H bridge Converter

Figure 5.2 illustrates the basic concept of the scheme where the instantaneous switching frequency is continuously varied within a line period of the fundamental inductor current. In order to arrive at the optimal scheme, i.e., to determine the optimal switching frequency at each time instant, first the dependencies of current THD and the total loss on the instantaneous switching frequency are analyzed.

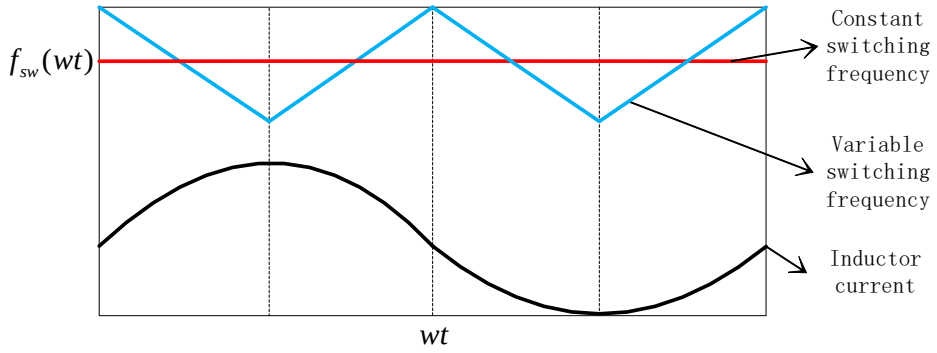


Figure 5.2. Concept of Variable Instantaneous Switching Frequency Method

5.2 Variable Switching Frequency Scheme to Reduce Combined Switching Loss and Inductor Core Loss with Unipolar Modulation

After the major types of losses in the converter and the inductor current ripple expression are analyzed, the optimal scheme is derived to find the instantaneous switching frequency resulting in loss reduction while still satisfying the THD requirement.

5.2.1 Loss Analysis

The magnitude of the current ripple is a function of time (point on sine wave) and switching frequency. The magnitude of the inductor current ripple equation is shown as

(5.1) as derived by [116] from which the THD can be calculated using the RMS value of the ripple.

$$i_{ripple}(wt,\, f_{sw}(wt)) = \frac{m_a V_{dc} \sin(wt)(1 - m_a \sin(wt))}{4 L f_{sw}(wt)} \tag{5.1}$$

There are four major types of losses for H-bridge converters as shown in Table 5.1. Due to the symmetric property of the current ripple and loss, the integration cycle used in calculation is chosen as π instead of 2π for simplicity.

As mentioned before, THD is desired to be maintained the same which means the RMS values of the fundamental and switching current components will be unchanged. Therefore the conduction loss will not be affected by the variable switching frequency scheme.

Switching loss will increase as switching frequency increases. As SiC switches are used in this study, it should be noted that the switching loss is proportional to the square of the current as shown in the product datasheet [116].

Usually for common core materials such as powdered iron or ferrite, $\alpha > \beta$ (refer Table 5.1) is satisfied which means the magnetic flux excursion has a heavier weight than the switching frequency, and therefore, core loss decreases as switching frequency increases [118].

Copper loss is generated due to ac resistance of the wire and corresponding ac current with same frequency [117]-[118]. For high frequency inductors usually Litz wire is used due to its effectiveness in having low skin effect and proximity effect and in this

study also Litz wire is used for inductor windings. The copper loss is the sum of the fundamental frequency component (60 Hz) and switching frequency component as shown in (5.2). Clearly the 60 Hz frequency copper loss will not change as the fundamental inductor current will not change, only the switching frequency component needs to be analyzed.

$$P_{cu\_sw} = i_{rms\_ripple}(wt, f_{sw}(wt))^2 R_{ac}(f_{sw}(wt)) \tag{5.2}$$

$$i_{rms\_ripple}(wt, f_{sw}(wt)) = \frac{i_{ripple}(wt, f_{sw}(wt))}{\sqrt{3}} \tag{5.3}$$

$$R_{ac}(f_{sw}(wt)) = R_{dc}K_f(f_{sw}(wt)) = R_{dc}(1 + k_{Liz} f_{sw}(wt)^2) \tag{5.4}$$

$$P_{cu\_sw} = \frac{\int_0^{\pi} [R_{dc}(i_{rms\_ripple}(wt, f_{sw}(wt)))^2 + k_{Liz} R_{dc} M(wt)]dwt}{\pi}$$
$$where \;\; M(wt) = \left(\frac{m_a V_{dc} \sin(wt)(1 - m_a \sin(wt))}{4L\sqrt{3}}\right)^2 \tag{5.5}$$

In (5.2) to (5.5), i_{rms_ripple} is the RMS value of the switching current, R_{ac} is the ac resistance of the Litz wire, R_{dc} is the dc resistance of the Litz wire, k_{Liz} is the coefficient of the Litz wire between ac resistance and dc resistance acquired in the manufacturer datasheet, P_{cu_sw} is the inductor copper loss of the high switching frequency component.

The switching frequency RMS current is calculated as shown in (5.3). As the ripple current is triangle wave, $\sqrt{3}$ is used. The ac resistance of the Litz wire has the relationship to the dc resistance shown in (5.4) which is provided in the datasheet [118]. The first term in (5.5) will not change since the high frequency RMS ripple current is same for the variable and constant switching frequency schemes. Also the second term

will not change because it is independent to the switching frequency, therefore the copper loss does not change.

Therefore in general, as switching frequency increases, THD will decrease, switching loss will increase, inductor core loss will decrease as shown in Table 5.1.

Table 5.1. Loss Analysis

Type of Loss	**Loss Equations**	**Relationship with Switching Frequency**
Conduction loss in switches	$P_{con} = I_{rms}^2 R_{on}$	Independent
Switching loss	$P_{sw} = \frac{\int_0^{\pi} K \cdot V(wt) I^2(wt) f_{sw}(wt) dwt}{\pi}$	$f_{sw} \uparrow \ P_{sw} \uparrow$
Copper loss in inductor	$P_{cu} = \Sigma K_f I_{rms\_f}{}^2 R_{dc}$	Independent
Core loss in inductor	$P_{fe} = \frac{\int_0^{\pi} k \cdot \Delta B(wt)^{\alpha} f_{sw}(wt)^{\beta} dwt}{\pi}$	$f_{sw} \uparrow \ P_{fe} \downarrow$

5.2.2 Optimal Scheme

The aim of the optimal variable switching frequency scheme is to minimize the combined switching loss and inductor core loss under the constraint that the grid current THD remains the same with the requirement. The optimization problem can be rearranged as (5.6) after combining all the constants of switching loss, core loss and current THD into a neat form. Calculus of variations and Lagrange method are used to solve this problem.

$$\min Loss = \int_0^{\pi} P_{sw} dwt + \int_0^{\pi} P_{fe} dwt = \int_0^{\pi} K_{sw} \sin^2(wt) f_{sw}(wt) dwt + \int_0^{\pi} K_{fe} \sin^{\alpha}(wt)(1 - m_a \sin(wt))^{\alpha} f_{sw}(wt)^{\beta-\alpha} dwt$$

$$s.t. \qquad \int_0^{\pi} \frac{\left[\sin(wt)(1 - m_a \sin(wt))\right]^2}{f_{sw}(wt)^2} dwt = C \tag{5.6}$$

$$where \qquad K_{sw} = KV_{dc} I_{pk}^2 \qquad K_{fe} = k(\frac{k_1 V_{dc} m_a}{4L})^{\alpha} \qquad C = \frac{48\pi I_{sw\_rms}^2 L^2}{V_{dc}^2 m_a^2}$$

In (5.6), K_{sw} is the switching loss constant, K is the coefficient of the switching loss corresponding to a certain type of switch for switching once obtained from datasheet as expressed in Table 5.1 switching loss part, V_{dc} is the input dc voltage, I_{pk} is the peak value of fundamental current. K_{fe} is the core loss constant, k is the coefficient and α, β are the exponents in the core loss equation corresponding to the core material obtained from datasheet as expressed in Table 5.1 core loss part, m_a is the modulation ratio, N is the number of turns of the inductor, A_c is the core area. C is the THD constant, I_{sw_rms} is the RMS current of the switching frequency, L is the inductance.

Use Lagrange optimization method to convert the problem into an unconstrained problem as shown by (5.7)

$$J = \int_0^{\pi} K_{sw} \sin^2(wt) f_{sw}(wt) dwt + \int_0^{\pi} K_{fe} \sin^{\alpha}(wt)(1 - m_a \sin(wt))^{\alpha} f_{sw}(wt)^{\beta-\alpha} dwt + \lambda(\int_0^{\pi} \frac{\left[\sin(wt)(1 - m_a \sin(wt))\right]^2}{f_{sw}(wt)^2} dwt - C) \tag{5.7}$$

The derivative of the function J is

$$\frac{\partial J}{\partial \eta} = \frac{\partial}{\partial \eta} J(f_{sw}(wt) + \eta \Delta f_{sw}(wt), \lambda + \eta \Delta \lambda)|_{\eta=0} \tag{5.8}$$

In detail

$$\begin{aligned}\frac{\partial J}{\partial \eta} &= K_{sw} \int_0^{\pi} \sin^2(wt) \Delta f_{sw}(wt) dwt \\ &+ K_{fe} \int_0^{\pi} (\beta - \alpha) \sin^{\alpha}(wt)(1 - m_a \sin(wt))^{\alpha} \left[f_{sw}(wt) \right]^{\beta-\alpha-1} \Delta f_{sw}(wt) dwt \\ &+ \Delta\lambda \left\{ \int_0^{\pi} \frac{\left[\sin(wt)(1 - m_a \sin(wt))\right]^2}{\left[f_{sw}(wt) \right]^2} dwt - C \right\} \\ &+ \lambda \left\{ \int_0^{\pi} -2 \frac{\left[\sin(wt)(1 - m_a \sin(wt))\right]^2}{\left[f_{sw}(wt) \right]^3} \Delta f_{sw}(wt) dwt \right\}\end{aligned} \tag{5.9}$$

To reach the optimization, for any $\Delta f_{sw}(wt)$ and $\Delta\lambda$, the derivative of J should be 0 as shown by (5.10)

$$\frac{\partial J}{\partial \eta}|_{\eta=0} = 0 \tag{5.10}$$

Therefore (5.11) can be derived

$$\begin{aligned}\frac{\partial J}{\partial \eta}|_{\eta=0} &= \frac{\partial}{\partial \eta} J(f_{sw}(wt) + \eta \Delta f_{sw}(wt), \lambda + \eta \Delta \lambda)|_{\eta=0} \\ &= K_{sw} \int_0^{\pi} \sin^2(wt) \Delta f_{sw}(wt) dwt \\ &+ K_{fe} \int_0^{\pi} (\beta - \alpha) \sin^{\alpha}(wt)(1 - m_a \sin(wt))^{\alpha} \left[f_{sw}(wt) \right]^{\beta-\alpha-1} \Delta f_{sw}(wt) dwt \\ &+ \Delta\lambda \left\{ \int_0^{\pi} \frac{\left[\sin(wt)(1 - m_a \sin(wt))\right]^2}{\left[f_{sw}(wt) \right]^2} dwt - C \right\} \\ &+ \lambda \left\{ \int_0^{\pi} -2 \frac{\left[\sin(wt)(1 - m_a \sin(wt))\right]^2}{\left[f_{sw}(wt) \right]^3} \Delta f_{sw}(wt) dwt \right\} = 0\end{aligned} \tag{5.11}$$

The final expression of $f_{sw}(wt)$ is the answer to (5.12) which is the solution to the cubic equation. Then substituting $f_{sw}(wt)$ in (5.13) leads to the value of λ by numerical method. Calculation should be done in software such as MATLAB offline first before implementing in the DSP.

$$\begin{aligned} &\left[f_{sw}(wt)\right]^3 + p\left[f_{sw}(wt)\right]^{\beta-\alpha+2} + q = 0 \\ \textit{where}\quad &\begin{cases} p = \dfrac{K_{fe}}{K_{sw}}(\beta-\alpha)\sin^{\alpha-2}(wt)(1-m_a\sin(wt))^{\alpha} \\ q = \dfrac{-2\lambda}{K_{sw}}(1-m_a\sin(wt))^2 \end{cases} \end{aligned} \tag{5.12}$$

$$\int_0^{\pi} \frac{\left[\sin(wt)(1-m_a\sin(wt))\right]^2}{\left[f_{sw}(wt)\right]^2} dwt = C \tag{5.13}$$

5.3 Hardware Implementation and Results

A 2 kVA H-bridge inverter with LC filter and resistive load has been built to verify the proposed optimal variable switching frequency scheme. Because of the large output filter capacitor used, the load voltage is almost a pure sinusoidal wave and therefore can represent the grid. The power factor is 1 and the modulation ratio is 0.9 which represents a typical grid-connected PV application. Table 5.2 and Table 5.3 show the experiment specifications and the components used.

Table 5.2. Specifications

Power	2 kVA
Dc Input Voltage	370 V
Load Voltage	235 V
Load Current	8.7 A
Power Factor	1
Modulation Ratio	0.9
Constant Switching Frequency	100 kHz

Table 5.3. Switch and Inductor Parameters

Switch	Type	SiC MOSFET
	Manufacturer / part no.	CREE / C2M0280120D
	On resistance	80 mohm
Inductor	Manufacturer	TDK
	Core Material / type	SIFERRIT N87 / Planar
	Inductance	230 uH
	Number of turns	29
	Volume	58mm x 38mm x 24mm
	Area of Core	25mm x 4mm
	Wire Type	Litz Wire
	60 Hz Resistance	38 mohm
	100 kHz Resistance	0.26 ohm

Figure 5.3 shows the H-bridge prototype with the powdered iron inductor. For comparison, the constant switching frequency scheme at 100 kHz has also been implemented. The inductor current is designed to have a THD of 4.8% at 100 kHz. The positive gate voltage of the MOSFET (Vgs) is 20V and negative is -5V. In order to eliminate the influence of the diode recovery loss of the main switches, 4 SiC Schottky diodes are put in parallel to the 4 main switches. LeCroy 6200A oscilloscope is used to capture waveforms. The driver circuit, DSP and ADC opamp circuits are all powered by

external auxiliary power supply so that those parts do not count in the input or output power. The load power and input power are measured using oscilloscope.

THD calculation is done in MATLAB using measured inductor current data with the FFT base step of 5 Hz in both constant frequency and variable frequency schemes. Only the frequencies larger than 10 kHz are considered in THD calculation in order to exclude the low order harmonics caused by the blanking time in both schemes.

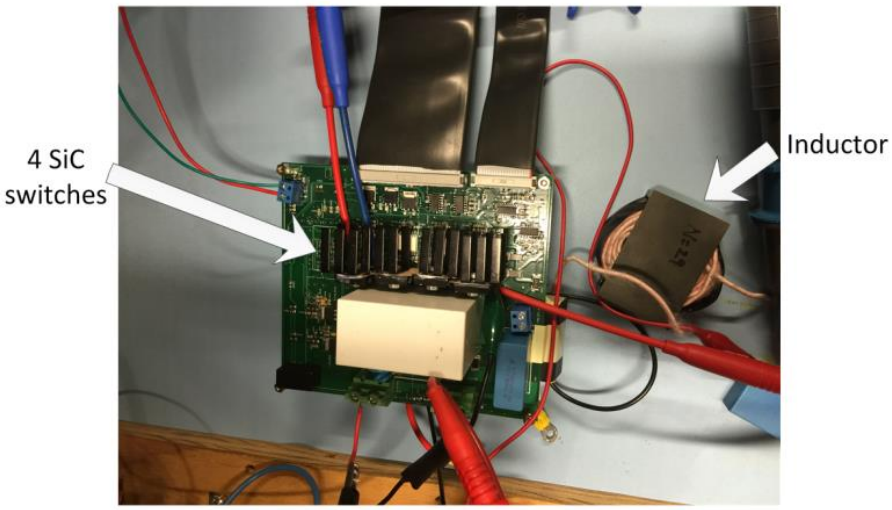


Figure 5.3. H-bridge Converter Prototype and Experimental Setup

Figure 5.4 shows the calculated $f_{sw}(wt)$ corresponding to the experiment specifications using (5.12) and (5.13) and also the scaled inductor fundamental current and ripple current profile for reference. The switching frequency changes from around 40 kHz to 220 kHz along with the inductor fundamental current. In general, the switching frequency is relatively low around the peak of the inductor fundamental current, and is relatively high around zero-crossing of the inductor fundamental current. DSP TMS320f28335 is used to control the inverter and implement the optimal variable switching frequency scheme. The $T_s(wt)$ (instantaneous switching cycle) is first

calculated offline using MATLAB and to create a lookup table in DSP. At every PWM interruption, the value of the $T_s(wt)$ is given to EPwmxRegs.TBPRD register in DSP to change the cycle of the next triangle carrier wave to change the instantaneous switching frequency. The blanking time is set to 160 ns.

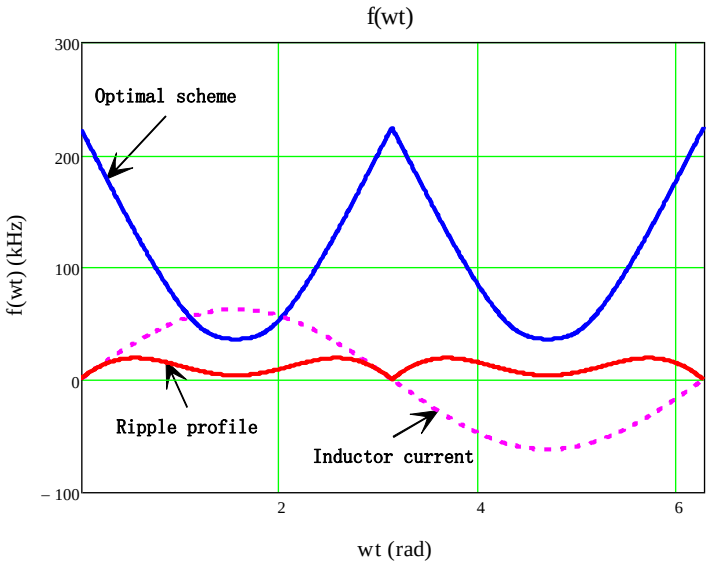
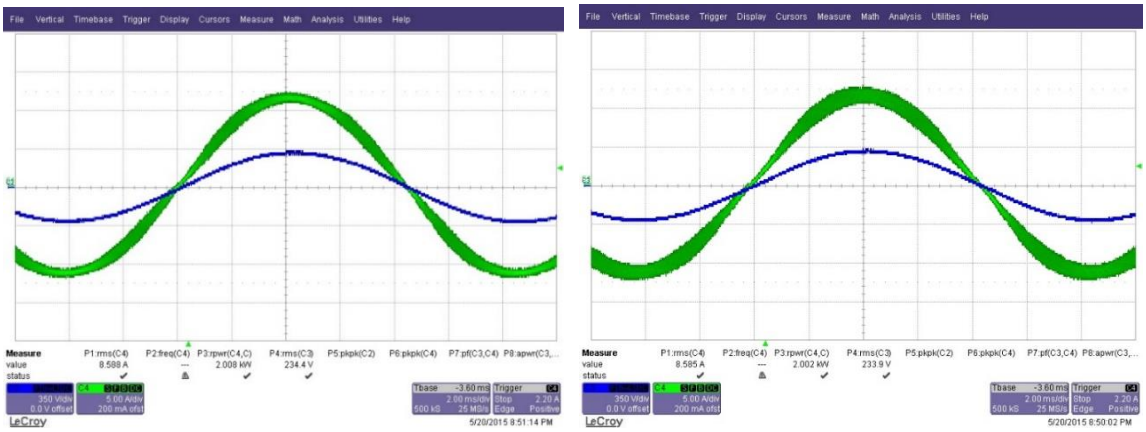


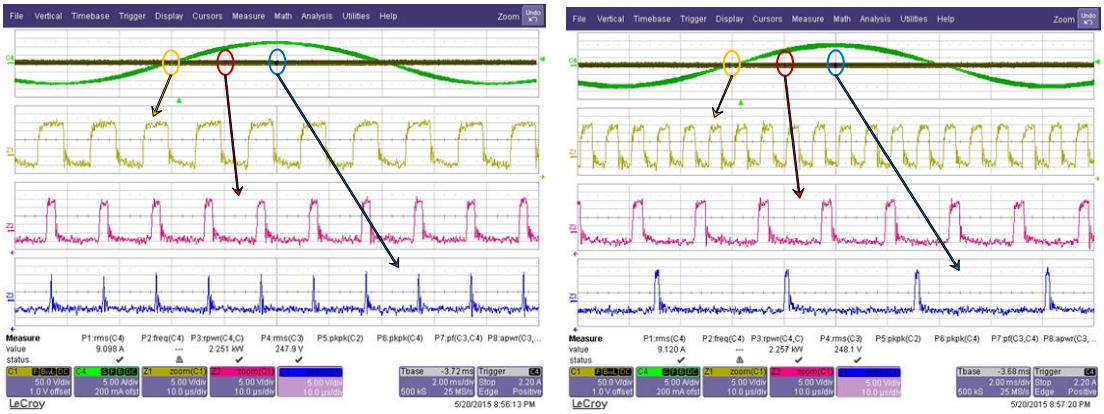
Figure 5.4. Time Variation of the Calculated Instantaneous Switching Frequency. (The Scaled Inductor Fundamental Current and Ripple Magnitude Profile are also Shown for Reference)

Figure 5.5 shows the salient inductor current waveforms comparing the constant switching frequency scheme and the optimal variable switching frequency scheme. It can be seen that the high frequency ripple in the inductor current using the optimal scheme is relatively higher near 90° and lower near 30° of the inductor current fundamental wave.



(a) (b)

Figure 5.5. Experimental Inductor Current Waveforms using Constant Frequency Scheme and the Proposed Optimally Variable Frequency Scheme. (a) Constant Frequency Scheme, (b) Variable Frequency Scheme



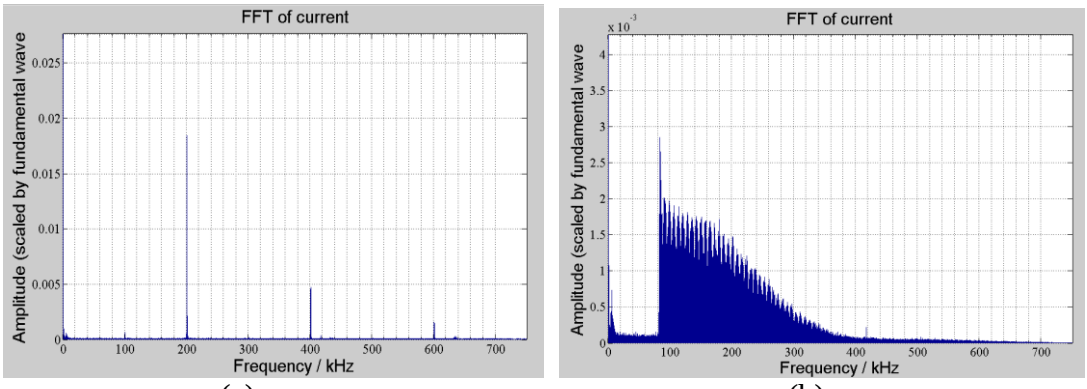
(a) (b)

Figure 5.6. Gate-source PWM Pulses and Zoomed Waveforms near 0°, 45° and 90°. Time scales are all 10 us/div for the Zoomed V_{gs} Waveforms. (a) Constant Frequency Scheme, (b) Variable Frequency Scheme

Figure 5.6 shows the zoomed PWM pulses near 0°, 45° and 90° points on the fundamental inductor current. The PWM pulses are V_{gs} of main MOSFETs (gate source voltage) changing between 20 V and -5 V. The time scales for the zoomed pulse

waveforms are all 10 us/div and the voltage scales are all 5 V/div for the three different zoomed positions of the two schemes. It can be seen that for the optimal scheme, the switching frequency is about 220 kHz near 0°, 100 kHz near 45° and 40 kHz near 90° of the fundamental inductor current which corresponds to the designed optimal scheme while for the constant switching frequency scheme it is always 100 kHz.

Figure 5.7 shows the frequency spectra of inductor current corresponding to both conventional and proposed schemes. From the spectrum it can be seen that, while for the constant switching frequency scheme the frequency components are multiples of 200 kHz, they are distributed from 80 kHz to 440 kHz (unipolar H bridge doubles the switching frequency of the inductor current) in the variable switching frequency scheme. This leads to an additional advantage that the dominant harmonic that appears in constant switching frequency scheme is reduced in the new scheme and EMI problem can be relieved [119]-[120]. The overall THD of around 4.8%, is almost the same for both schemes.



(a) (b)

Figure 5.7. Frequency Spectrum of Inductor Current. (a) Constant Frequency Scheme THD = 4.82%, (b) Variable Frequency Scheme THD = 4.77%

The conduction loss and copper loss which are same in both schemes are calculated using (5.14) and (5.15). In (5.14) the factor 2 corresponds to the fact that at any given instant exactly two switches conduct the inductor current. While the factor 1.3 corresponds to the fact that at junction temperature 75°C the on resistance of the switches will slightly increase by 1.3 times according to the datasheet. Other losses include diode recovery loss and dc link capacitor discharging resistor loss which are totally estimated to be 2W, small enough as extra Schottky diodes are put in parallel with 4 main switches.

$$P_{con} = I^2 R_{ds\_on} \times 2 \times 1.3 = 15.8W \tag{5.14}$$

$$P_{cu} = I_{60}^2 R_{60} + I_{100k}^2 R_{100k} = 2.7W \tag{5.15}$$

In (5.14) and (5.15), I is the total RMS current of the inductor, I_{60} is the RMS value of the 60 Hz inductor current, I_{100k} is the RMS value of the 100 kHz inductor current. R_{60} is the resistance of the inductor at 60 Hz, R_{100k} is the resistance of the inductor at 100 kHz as introduced in Table 5.3.

Table 5.4 shows the calculation of the loss saving in the experimental prototype. The load power and input power are measured using an oscilloscope. The conduction loss and copper loss are estimated using the RMS current and the resistance of switch and inductor as in (5.14) and (5.15), and are subtracted from the total loss to obtain the combined switching and core loss for each scheme. The loss saving of the combined switching loss and core loss components from the experimental prototype is 20.9% as compared to 24.1% predicted from theoretical analysis.

Table 5.4. Loss Analysis in Hardware Prototype

	Constant f	**Variable f**
Load power	2002.3 W	1995.8 W
Input power	2059.4 W	2045.3 W
Total power loss	57.1 W	49.5 W
Estimated conduction loss	15.8 W	
Estimated copper loss	2.9 W	
Other loss	2W	
Combined switching loss and core loss	36.4 W	28.8 W
Reduction in the combined switching loss and core loss	20.9% (compared with 24.1% from analysis)	

CHAPTER 6 A T-TYPE SINGLE PHASE TRANSFORMER LESS STRING INVERTER WITH DYNAMIC AND ADAPTIVE DC-LINK VOLTAGE CONTROL

In this chapter, a T-type doubly grounded transformer-less single phase inverter with dynamic swing of the dclink voltage is proposed for photovoltaic (PV) application which is a variation of the topology in Chapter 2. This topology is a combination of a boost stage and an asymmetric half-bridge inverter along with a T-branch. It takes advantage of the three-level switching states with reduced voltage stress on the main switches to achieve lower switching loss and almost one-half the inductor current ripple. The double line frequency power decoupling is addressed by a dynamic dc-link approach, which allows a large swing of the dc-link to reduce the decoupling capacitor requirement, enabling an all-film capacitor implementation. This converter ensures the complete elimination of high-frequency capacitive coupled ground current by directly connecting the PV negative terminal to the grid neutral. Moreover, an adaptive dc-link voltage control scheme that optimally changes the average value of the dc-link voltage as the operating conditions (load and power factor) vary, has been proposed and thoroughly investigated from the perspective of better utilization of passive components and further reduction of switching losses.

6.1 Circuit Configuration

Figure 6.1 shows the proposed topology of the T-type doubly grounded voltage swing inverter for transformer-less string inverter application. The converter has an input boost stage followed by an asymmetric half-bridge inverter stage coupled with a bi-directional T-branch. As opposed to the conventional boost converter which shares a common negative, here the boost input and output shares a common positive terminal. The bi-directional boost converter comprises of inductor L_b, dc-link capacitor C_{link}, and switches Q_1 and Q_2. The three-level T-type inverter stage is comprised of two main switches Q_3 and Q_4, with an additional bi-directional T-branch comprising of switches Q_5 and Q_6 which switches at line frequency for unity pf operation, thus having limited contribution to the converter's switching loss.

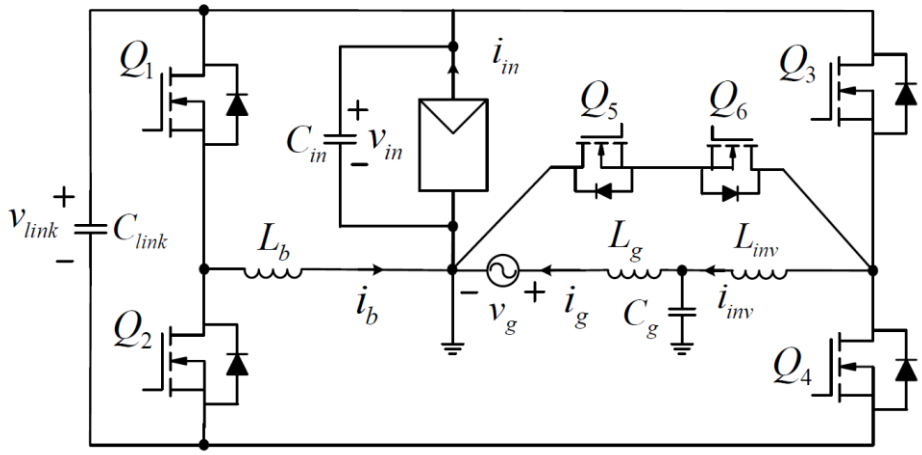


Figure 6.1. Proposed T-type Doubly Grounded Voltage Swing Inverter for Transformer-less PV Application

The grid neutral is connected directly to the PV negative terminal, commonly referred to as a doubly grounded structure, thus inherently eliminating the common-mode, high-frequency ground currents through the PV module capacitance, which is a

common problem in most of the transformer-less inverters. A dynamic dc-link approach provides the 120 Hz power decoupling as discussed in a later section. For grid connected implementation LCL (L_{inv}, C_g, L_g) filters are considered. In Figure 6.1 i_{inv} is the current through L_{inv}, and i_g is the current through L_g, which is also the grid current.

6.1.1 Operating Principles

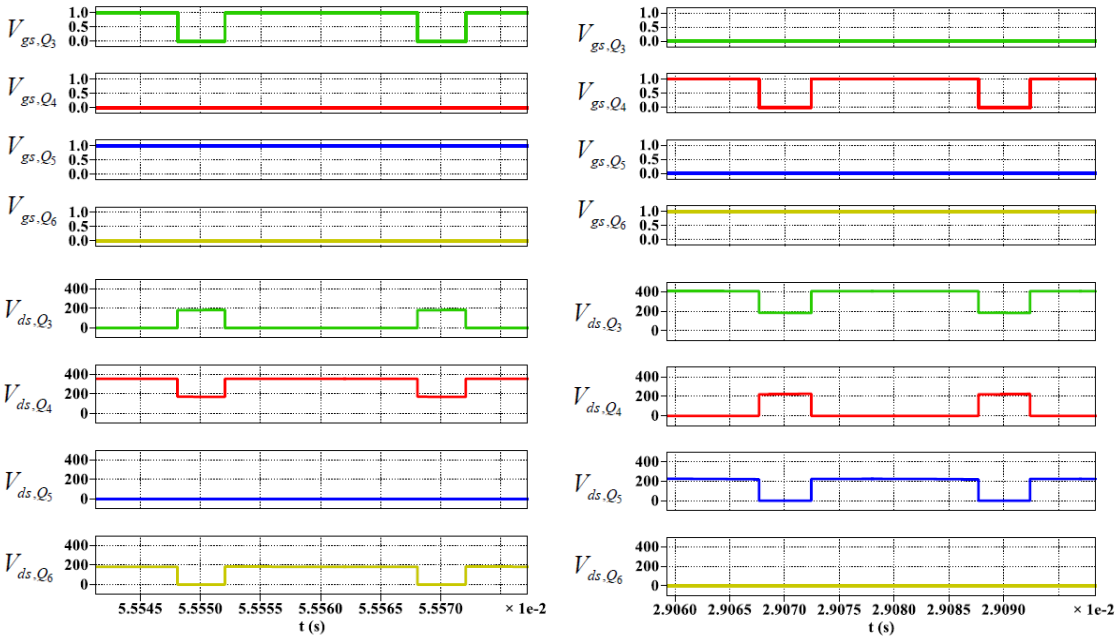
The boost stage steps up the input PV voltage v_{in} to a higher nominal dc voltage v_{link} of around 400 V. It is particularly designed to have a large 120 Hz swing of around 140 V peak-peak. The combination of higher nominal voltage of v_{link} and a very large swing is used to address the power decoupling with a greatly minimized dc-link capacitance. The input voltage v_{in} and the difference voltage v_{link} - v_{in} constitute two asymmetric voltage levels of the half-bridge. d_b and d_{inv} are respectively the boost and inverter stage duty ratio.

In every grid cycle the T-type asymmetric half-bridge inverter has three operating states - POS, ZERO, and NEG as shown in Table 6.1. The pole voltage V_{MN} with respect to a neutral-point voltage N can be one of v_{in}, 0, or v_{in} - v_{link} according to the operating state. The first operating state POS is generated with Q_3 being ON and Q_4 and T-branch being OFF with pole voltage v_{in}. The operating state ZERO corresponds to both Q_3 and Q_4 being OFF and T-branch being ON with pole voltage being 0. Essentially, ZERO state is generated with both Q_3 and Q_4 being OFF and either or both of Q_5 and Q_6 being ON, depending on the voltage polarity. NEG state has a pole voltage v_{in} - v_{link} with Q_4 being ON and Q_3 and T-branch being OFF.

Table 6.1. Switch Signal and Operating States of the Inverter Stage

State	Q_3	Q_4	Q_5-Q_6	Pole voltage, V_{MN}
POS	ON	OFF	OFF	v_{in}
ZERO	OFF	OFF	ON	0
NEG	OFF	ON	OFF	$v_{in} - v_{link}$

Different combinations of these three operating states generate the output grid voltage at different operating pf, the modulation strategy is discussed in the next section. When switching, the switch voltage stress on Q_3 and Q_4 is around half of the dc-link (v_{in} for Q_3 and v_{link} - v_{in} for Q_4). But when they are not switching, the voltage across them changes between v_{link} and v_{in} for Q_3 while, v_{link} and v_{link} - v_{in} for Q_4. This is shown in Figure 6.2 for both the switching transition between POS and ZERO states (Figure 6.2a) and between NEG and ZERO states (Figure 6.2b). Thus though the commutation voltage and hence the switching loss are reduced for Q_3 and Q_4, the absolute stress on them is still the full dc-link voltage. On the other hand, the commutation voltage and the absolute switch stress on Q_5 and Q_6 are both half the dc-link voltage. However, the main disadvantage of T-type implementation with the conventional modulation scheme (i.e., the T-branch switching at line frequency) is the additional conduction loss in the T-branch body diode, as any one of the two diodes of Q_5 or Q_6 always conducts.



(a) (b)

Figure 6.2. Switch Voltage Stress for All the Switches in the Inverter Stage when Switching between (a) POS and ZERO States, (b) NEG and ZERO States

6.1.2 Modulation Scheme

The modulation of the boost stage is straightforward with top switch Q_1 complementary to the bottom one Q_2 irrespective of the operating pf. However, the scheme is complex for the inverter stage. Table 6.2 gives the modulation strategy for the half-bridge inverter stage with the T-branch for different pf operations. Scheme I and II respectively correspond to the T-branch switching at line and carrier frequency.

Table 6.2. Modulation Scheme for the Proposed T-type Doubly Grounded Voltage Swing Inverter

<table>
<tr><th colspan="2" rowspan="2">Condition</th><th colspan="4">Switching scheme I</th><th colspan="3">Switching scheme II</th></tr>
<tr><th>Q_3</th><th>Q_4</th><th>Q_5</th><th>Q_6</th><th>Q_3</th><th>Q_4</th><th>Q_5-Q_6</th></tr>
<tr><td rowspan="2">$pf = 1$</td><td>$d_{inv} > 0$</td><td>ON:POS
OFF:ZERO</td><td>OFF</td><td>ON</td><td>OFF</td><td colspan="3" rowspan="2">NA</td></tr>
<tr><td>$d_{inv} < 0$</td><td>OFF</td><td>ON:NEG
OFF:ZERO</td><td>OFF</td><td>ON</td></tr>
<tr><td rowspan="4">$pf \neq 1$</td><td>$d_{inv} > 0, i_{inv} > 0$</td><td colspan="4">modulation scheme is similar to $pf = 1, d_{inv} > 0$</td><td>ON:POS
OFF:ZERO</td><td>OFF</td><td>OFF:POS
ON:ZERO</td></tr>
<tr><td>$d_{inv} > 0, i_{inv} < 0$</td><td>ON:POS
OFF:ZERO</td><td>OFF</td><td>OFF</td><td>ON</td><td colspan="3" rowspan="2">OFF</td></tr>
<tr><td>$d_{inv} < 0, i_{inv} > 0$</td><td>OFF</td><td>ON:NEG
OFF:ZERO</td><td>ON</td><td>OFF</td><td>ON:NEG</td><td>OFF:NEG</td></tr>
<tr><td>$d_{inv} < 0, i_{inv} < 0$</td><td colspan="4">modulation scheme is similar to $pf = 1, d_{inv} < 0$</td><td>OFF:ZERO</td><td>ON:ZERO</td></tr>
</table>

For unity pf operation, the modulation scheme is simple. The T-branch switches at line frequency, while the effective switching frequency of Q_3 and Q_4 is half of the carrier signal frequency as they are OFF for half the grid cycle as shown in Figure 6.3a. During the positive half cycle ($d_{inv} > 0$), operating states POS and ZERO (Q_4 and Q_6 being always OFF, Q_5 being always ON, and only Q_3 switching) are used to modulate the output (interval A in Figure 6.3a). And in the negative half cycle ($d_{inv} < 0$), operating states NEG and ZERO (Q_3 and Q_5 being always OFF, Q_6 being always ON, and only Q_4 switching) are used to modulate the output waveform (interval C in Figure 6.3a).

On the contrary for non-unity pf operation, the modulation is more involved as it is dependent on the switch pole current i_{inv} direction [see Figure 6.3b]. For $i_{inv} > 0$, modulation scheme is same as with pf = 1 in the positive half cycle (interval A in Figure 6.3b), and for $i_{inv} < 0$ modulation scheme is same as with pf = 1 in the negative half cycle (interval C in Figure 6.3b). But in the positive half cycle, for $i_{inv} < 0$, Q_4 and Q_5 are OFF, Q_6 is ON, and Q_3 switches to generate POS or ZERO states (interval B in Figure 6.3b). And in the negative half cycle, for $i_{inv} > 0$, Q_3 and Q_6 are OFF, Q_5 is ON, and Q_4 switches

to generate POS or ZERO states (interval D in Figure 6.3b). Here, the T-branch switches at the line frequency as shown in scheme I of Table 6.2 and also the effective switching frequency of Q_3 and Q_4 is still the same as before. But this approach is very sensitive to i_{inv} detection, and if not properly implemented, can lead to shoot-through of the T-type asymmetric half-bridge inverter leg.

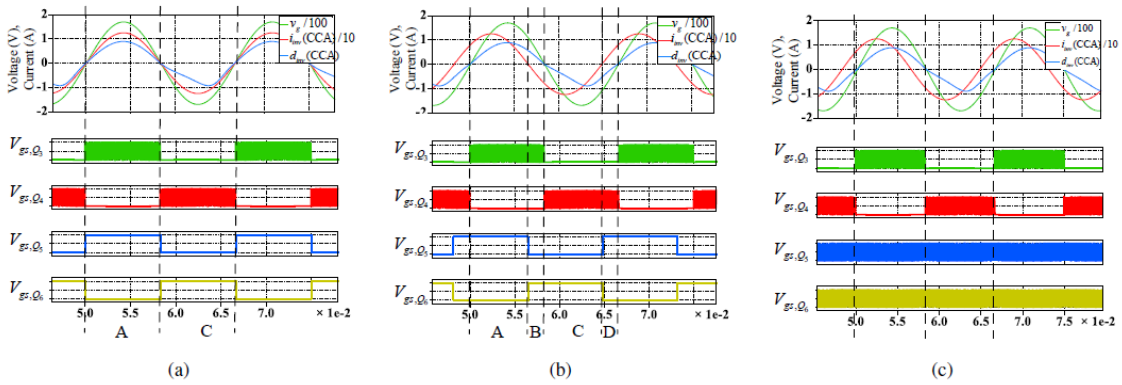


Figure 6.3. Switching Signals for the T-branch and the Half-bridge Inverter Stage for (a) Unity pf Operation, (b) Non-unity pf Operation in Scheme I, (c) Non-unity pf Operation in Scheme II

Further for non-unity pf operation, this disadvantage can be addressed by switching the T-branch throughout at the carrier frequency as shown in scheme II of Table 6.2 with the T-branch (Q_5 and Q_6) having the same gate signal. For $d_{inv} > 0$, Q_3 switches complementary to the T-branch, while for $d_{inv} < 0$, Q_4 switches complementary to the T-branch as shown in Figure 6.3c. This would increase the T-branch switching loss, but essentially increasing the turn-on loss of only one of Q_5 and Q_6 as at any instant either one will have soft turn-on depending on the current direction. Also in this scheme the conduction loss associated with the T-branch body diode occurs only during dead-

time transition, and thus carrier frequency switching of T-branch would not significantly impact the overall converter efficiency.

6.1.3 Power Decoupling – Dynamic DC Link

In a single phase inverter, considering the grid voltage, current, and power as given in (6.1) and (6.2) at any arbitrary *pf* ($\cos\theta$), it is noted that the power expression has a ripple component varying at the double line frequency (2ω).

$$v_g = V_g \sin(\omega t) \qquad i_g = I_g \sin(\omega t + \theta) \tag{6.1}$$

$$P_g = \frac{V_g I_g}{2}[\cos\theta - \cos(2\omega t + \theta)] \tag{6.2}$$

Thus the instantaneous power from input is not equal to that of the output as the input power from the PV array is ideally dc, and an additional energy storage element is required to ensure the instantaneous power balance, commonly referred to as power decoupling. In this topology, a large double line frequency voltage ripple on the dc-link v_{link}, as shown in (6.3) is designed to address the power decoupling with a much reduced capacitor value, thus ensuring the use of only film capacitors.

$$v_{link} = V_{avg} + V_r \sin(2\omega t + \theta) \tag{6.3}$$

where, V_{avg} is the dc-link average voltage, and $2V_r$ is the peak-peak dc-link ripple voltage varying at double line frequency. The ripple power supported by the dc-link capacitor P_{link} is shown in (6.4) [10]. It is to be noted that the complete 120 Hz ripple component is controlled to be supported by the main dc-link, and thus the input is free of any ripple, which would otherwise have compromised the MPPT efficiency.

$$P_{link} = \omega C_{link} V_r (2V_{avg} \cos(2\omega t + \theta) + V_r \sin(4\omega t + 2\theta)) \tag{6.4}$$

By comparing the magnitude and phase of the total ripple power supported by the dc-link to the grid ripple power i.e., from (6.2) and (6.4), the condition for double line frequency power decoupling as given in (6.5) is obtained

$$V_{avg} V_r C_{link} = \frac{V_g I_g}{4\omega} = \frac{S_g}{2\omega} \tag{6.5}$$

where, S_g is the grid VA. Finally the capacitance is optimized for the range of operating condition as given in Table 6.3 with an objective of minimizing the capacitance volume as outlined in [60].

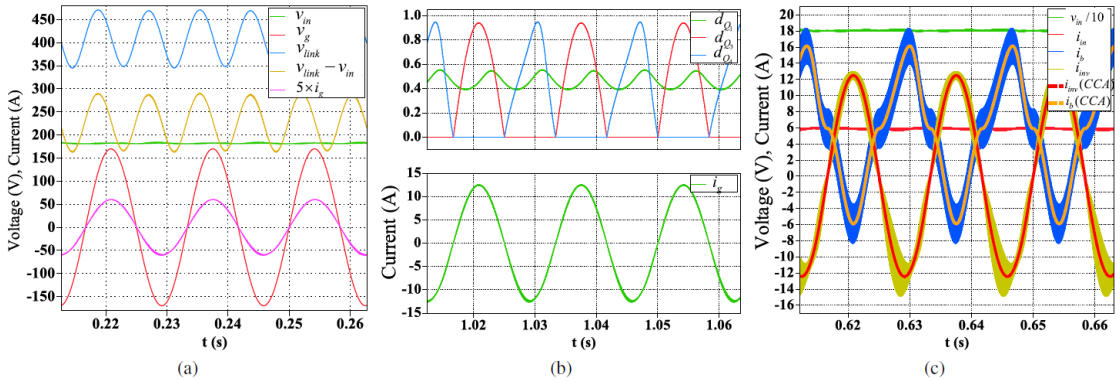


Figure 6.4. Steady State Waveforms at 1 kVA Showing (a) Dc-link Voltage, Input Voltage, Grid Voltage, Grid Current, and the Difference of the Dc-link Voltage and Input Voltage, (b) Cycle-by-cycle Averaged (CCA) Waveforms of Boost and Inverter Duty Ratio and Grid Current, (c) Inductor Currents and Scaled Input Voltage, all at Unity pf Operation

Table 6.3. Converter Specification

Parameter	Rating
Nominal dc Input	200 V
Nominal ac output	1 kVA, 120 V, 60 Hz
Operating pf	0.7 lagging - 0.7 leading
Switching frequency, f_{sw}	50 kHz

Figure 6.4 illustrates the steady state waveforms corresponding to unity pf (UPF) operation from the PLECS circuit simulation platform. These simulations (and experimental results presented later) correspond to a 1 kVA inverter with specifications given in Table 6.3. Figure 6.4a shows the dc-link voltage, input voltage, the difference of dc-link and input voltages along with grid current and grid voltage. It is to be noted that the peak-peak ripple of v_{in} is negligibly small demonstrating that the power decoupling is predominantly supported by the dc-link capacitor, which is effectively decoupled from the input, leading to a higher MPPT efficiency.

Figure 6.4b shows the cycle-by-cycle averaged (CCA) boost stage duty ratio ($d_{Q1} = d_b$), inverter stage duty ratios (d_{Q3} and d_{Q4}), and grid current at 1 kVA, UPF. It is to be noted that, d_{Q3} is purely sinusoidal as it modulates the input voltage v_{in} with no ripple component to generate positive half of v_g. On the contrary, d_{Q4} which modulates $v_{link} - v_{in}$, has double-line-frequency component to mitigate the influence of large 120 Hz dc-link ripple on the grid output. Also in order to regulate the input voltage to be a pure dc, the boost duty ratio should contain 120 Hz component as shown.

Figure 6.4c shows the waveforms of input current, boost inductor current, grid current, and scaled input voltage at UPF operation. It is interesting to note that, in the positive half cycle, i_{inv_pk} is around 15.8 A, whereas, the negative peak is around 12.8 A. The different peak values of i_{inv} is attributed to the different switching voltage component, v_{L_inv} during the positive and negative grid cycles. In the positive half cycle, $v_{L\_inv} = v_{in} - v_g$, whereas, in the negative half cycle $v_{L\_inv} = v_{link} - v_{in} - v_g$. As v_{link} has 120 Hz ripple and v_{in} is a pure dc, the ripple current is not symmetrical, though the fundamental component is symmetrical and has no dc offset as illustrated by the corresponding CCA waveforms in Figure 6.4c. Also, the boost inductor current i_b is bi-directional with both dc and sinusoidal components.

6.2 Adaptive Dc-link Voltage Control

The instantaneous values of each of the half-bridge voltage levels (v_{in} and $v_{link} - v_{in}$) needs to satisfy the constraint in (6.6) at any operating pf. These two constraints place a limit on the minimum value of the PV voltage and the maximum voltage swing allowed at the dc-link. This ensures that the half-bridge inverter stage does not operate at modulation index more than 1, which would otherwise distort the output waveforms and impact the total harmonic distortion (THD).

$$\begin{cases} v_{in} > v_g & \text{if } v_g > 0 \\ v_{link} - v_{in} > |v_g| & \text{if } v_g < 0 \end{cases} \tag{6.6}$$

As v_{in} has no double line frequency ripple, the constraint in (6.6) is instantaneously satisfied by ensuring the voltage margin, V_m [given in (6.7)] is greater than 0 only in the negative half of the grid cycle.

$$V_m = v_{link} - v_{in} - \left|v_g\right| > 0 \tag{6.7}$$

It is worth noting that to have an optimal dc-link capacitance value, it is enough to satisfy (6.6) instantaneously, rather than keeping the V_m always higher than 0 [10]. Again V_m is a function of the input voltage, operating pf, and VA of the inverter, which leaves room for improving converter efficiency by the adaptive dc-link voltage control, as discussed shortly.

This is quite different from any conventional full-bridge or three-level inverter operation which uses a very large dc-link capacitor, generally electrolytic capacitor, with a small double line frequency voltage ripple, V_r on the dc-link. Thus no additional constraint is imposed on the instantaneous dc-link value w.r.t. the grid voltage, where it is enough to satisfy $v_{link} > v_{g\_pk}$ globally.

6.2.1 Dependence of the Voltage Margin on Operating Parameters

The dependence of V_m on the operating kVA is clear from (6.5), where with a fixed dc-link capacitance C_{link}, V_{avg} and V_r, and thus V_m are dependent on S_g. Also its dependence on v_{in} is obvious from its definition in (6.7). Finally, the dependence of V_m on operating pf can be studied from (6.8). As discussed already, with ideally no ripple on v_{in}, (6.6) can be modified for only the negative grid cycle, and by substituting for V_r from (6.5), (6.8) is obtained.

$$V_{avg} + \frac{S_g \sin(2\omega t + \theta)}{2\omega V_{avg} C_{link}} - v_{in} > \left| V_g \sin(\omega t) \right| \tag{6.8}$$

Further, pf dependence can be analyzed from the steady state simulation results given in Figure 6.5. It gives the dc-link voltage, input voltage, the difference of dc-link and input voltages along with grid current and grid voltage waveforms corresponding to different operating pf - unity, 0.7 lagging, and 0.7 leading. Figure 6.5c shows that the leading pf gives the worst voltage margin [10] and thus needs a higher dc-link mean, whereas, lagging pf [see Figure 6.5b] gives the best margin requiring minimum dc-link mean. It has been accomplished by the adaptive dc-link scheme with the voltage margin V_m always being barely around 20 V at the critical point (Figure 6.5). It can be further seen that the constraints given in (6.6) have been satisfied in all three cases.

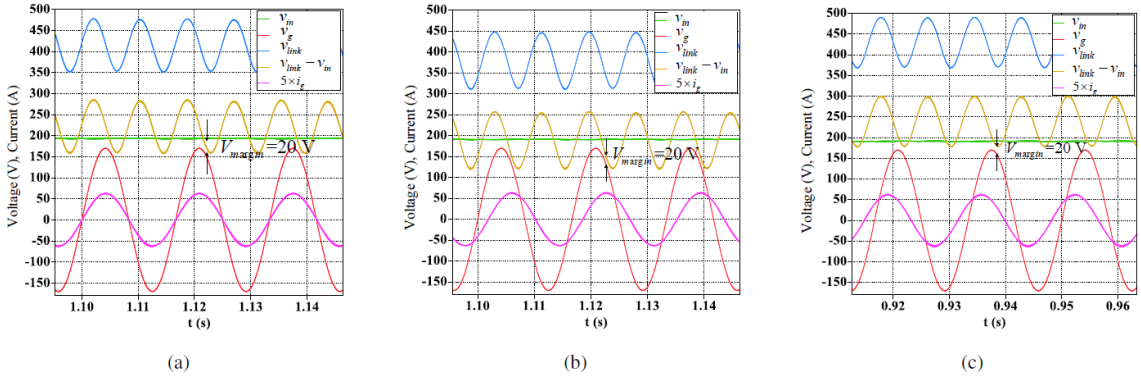


Figure 6.5. Steady State Waveforms at 1 kVA Showing Dc-link Voltage, Input Voltage, Grid Voltage, Grid Current, and the Difference of the Dc-link Voltage and Input Voltage at (a) Unity pf, (b) 0.7 Lagging pf, (c) 0.7 Leading pf Operations Highlighting the Voltage Margin of 20 V Fixed for Each Operating Point by Implementation of Adaptive Dc-link Voltage Control Scheme

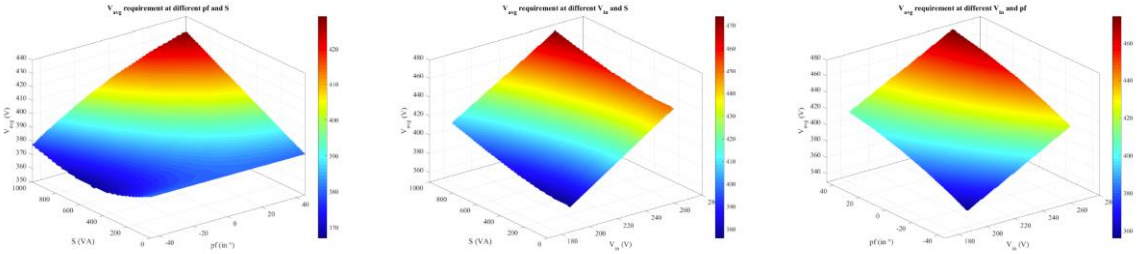
6.2.2 Adaptive Dc-link Scheme

With the dynamic dc-link approach, once the passive components are designed for the worst operating condition (leading pf at full rated VA), the dc-link average V_{avg} can be adjusted at other operating conditions instead of a fixed value. As over a grid cycle, the semiconductor switching loss is dependent on V_{avg}, it is beneficial to operate the inverter at the minimum dc-link average (implying lower switch voltage stress), which can be decided based on the constraint (6.6). Also with lower V_{avg}, the inductor current ripple can be decreased accounting for lower high frequency copper and core loss.

It can be seen that for different values of S_g, v_{in}, and pf, different minimum V_{avg} is required to satisfy (6.8).However, deriving the analytical solutions of the optimal V_{avg} for different S_g, v_{in}, and pf values is a complex assignment. Therefore, numerical method is used to find the minimum V_{avg} in MATLAB by sweeping the dc-link voltage average value over the specified operating range. 3-D plots showing the dependence of minimum V_{avg} required are given in Figure 6.6 for various combination of S_g (swept from 0 to 1000 VA), v_{in} (swept from 180 to 260 V), and pf angle (swept from -45° to 45° corresponding to 0.7 lagging and 0.7 leading pf respectively).

From the 3-D plots, the difference between the highest and the lowest V_{avg} is 24:74% for the specified range of operating conditions. It is 20.68% for UPF operation (fixed pf but varying S_g and v_{in}). But without the adaptive dc-link voltage scheme, V_{avg} will always be set to the largest value even at conditions that does not require such high dc link voltage, and loss reduction could not be achieved. With adaptive dc link scheme the voltage at the worst case condition can be reduced by 24.74% which corresponds to around 24.74% switching loss reduction (switching loss is linear with the voltage stress

across the semiconductor) and even higher percentage of savings in the high-frequency inductor core and copper loss.



(a) (b) (c)

Figure 6.6. Relationship Between the Minimum V_{avg} Required to Satisfy (6.8) for Various Combinations of S_g, v_{in}, and *pf* (a) for Different S_g and *pf* at v_{in} = 190 V, (b) for Different v_{in} and S_g at *pf* angle = 0° (UPF), (c) for Different v_{in} and *pf* at S_g = 1000 VA.

Implementation of the adaptive dc-link scheme does not interfere with the basic inverter control design. Instead of providing a constant dc-link average as conventionally done, the V_{avg} is decided based on the converter's operating point and provided as an input to the dc-link controller (further discussed in the next section). Also the values of V_{avg} can be saved in a look-up-table (LUT) off-line corresponding to different S_g, v_{in}, and *pf* to save the computation burden on the digital controller. In practice, V_{avg} should be a little higher than the calculated value considering the requirements on the switch dead-time, modulation margin (modulation index is limited to 0.95), and a non-zero ripple on v_{in}.

6.3 Converter Modeling and Controller Implementation

This section discusses the large signal average modeling of the proposed T-type doubly grounded voltage swing inverter and the controller implementation with the adaptive dc-link voltage control. To simplify the analysis, all the circuit components are considered lossless, i.e., ESR of the capacitors, on-resistance of the switches, and series resistance of inductors are assumed to be zero.

6.3.1 Large Signal Modeling

The large signal average model of the proposed converter can be obtained by replacing the two power poles by the corresponding ideal transformers with turns ratios being equal to the respective instantaneous duty ratios d_b and d_{inv} as shown in Figure 6.7. The average model will be different in two operating intervals depending on the sign of d_{inv}. Figure 6.7a and Figure 6.7b show the model for $d_{inv} > 0$ and $d_{inv} < 0$ respectively.

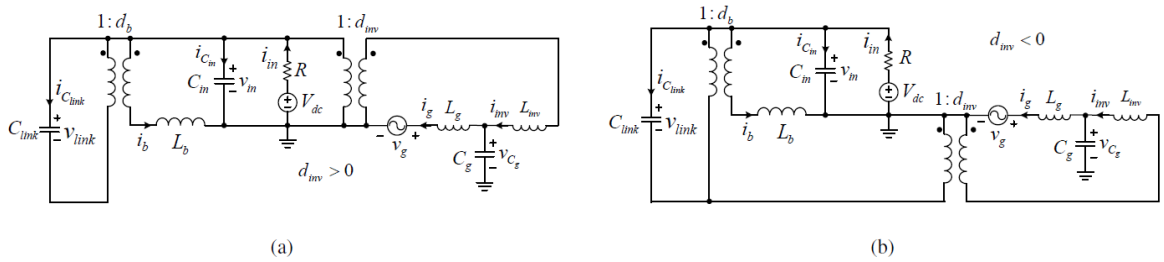


Figure 6.7. Large Signal Transformer Model of T-type Doubly Grounded Voltage Swing Inverter, (a) for $d_{inv} > 0$, (b) for $d_{inv} < 0$.

The dynamics of the capacitor voltage and inductor current are obtained by applying KCL and KVL respectively at appropriate nodes and loops in Figure 6.7. (6.9)-(6.14) define the large signal model of the proposed converter for $d_{inv} > 0$.

$$C_{in}\frac{dv_{in}(t)}{dt} = i_{in}(t) - i_b(t) - d_{inv}(t)i_g(t) \tag{6.9}$$

$$C_{link}\frac{dv_{link}(t)}{dt} = d_b(t)i_b(t) \tag{6.10}$$

$$C_g\frac{dv_{C_g}(t)}{dt} = i_{inv}(t) - i_g(t) \tag{6.11}$$

$$L_b\frac{di_b(t)}{dt} = v_{in}(t) - d_b(t)v_{link}(t) \tag{6.12}$$

$$L_{inv}\frac{di_{inv}(t)}{dt} = d_{inv}(t)v_{in}(t) - v_{C_g}(t) \tag{6.13}$$

$$L_g\frac{di_g(t)}{dt} = v_{C_g}(t) - v_g(t) \tag{6.14}$$

Whereas, (6.11), (6.12), (6.14) - (6.17) define the large signal model of the proposed converter for $d_{inv} < 0$.

$$C_{in}\frac{dv_{in}(t)}{dt} = i_{in}(t) - i_b(t) \tag{6.15}$$

$$C_{link}\frac{dv_{link}(t)}{dt} = d_b(t)i_b(t) - d_{inv}(t)i_{inv}(t) \tag{6.16}$$

$$L_{inv}\frac{di_{inv}(t)}{dt} = d_{inv}(t)(v_{link}(t) - v_{in}(t)) - v_{C_g}(t) \tag{6.17}$$

Finally, the PV string can be modeled as a voltage source in series with a resistor R to simulate the characteristics of the PV modules as shown below (6.18).

$$i_{in}(t) = \frac{V_{dc} - v_{in}(t)}{R} \tag{6.18}$$

6.3.2 Controllers

For the PV inverter operation in grid connected mode, the objective of the controller is to control the input voltage according to the MPPT voltage reference which

fixes the input power, control the grid current depending on the input power (with the fixed grid voltage), and control the average of the dc-link voltage. Without the input PV panel, the input of the converter comes from a dc source in series with a resistor to closely mimic the PV characteristic, and the input voltage reference is manually provided.

Figure 6.8 shows the overall controller block diagram. The objective of the dc-dc stage controller is to regulate the input voltage such that v_{in} is free of any double line frequency ripple, which would otherwise disrupt the MPPT efficiency when connected across the PV source as discussed earlier. To ensure this, input voltage controller has a high bandwidth to generate the boost stage duty d_b as shown.

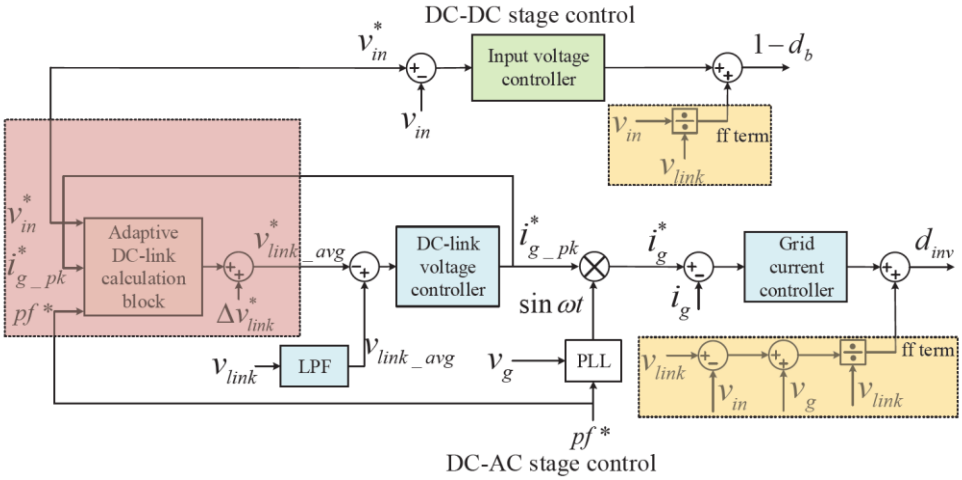


Figure 6.8. Controller Block Diagram of T-type Doubly Grounded Voltage Swing Inverter.

Both dc-link and inverter control loops in the dc-ac stage employ simple PI controllers with appropriate feed forward terms added as shown. The dc-link control loop regulates the average of the dc-link voltage to a reference value generated by the adaptive

dc-link control scheme. The calculation block (see Figure 6.8) is detailed in the next section. A first-order low-pass-filter (LPF) with cutoff frequency of 10 Hz is used to filter out the 120 Hz component in the dc-link voltage before comparing it with the reference.

The output current controller is designed to control the grid current with the current peak reference derived from the dc-link voltage control loop and the phase and frequency of the sinusoidal waveform determined by a phase-locked loop (PLL) and an external pf command. The output of the controller decides the inverter stage duty d_{inv}, which further generates the gate signals for Q_3 to Q_6 with appropriate dead-time based on the algorithm discussed in Section 6.2.

6.3.3 Adaptive Dc-link Control Block

Figure 6.8 highlights the adaptive dc-link controller in red. The calculation block is implemented with an LUT, which is stable and fast (with one switching cycle response), but is affected by the parameters uncertainty. Thus a minor correction term Δv_{link}^{*} is added to the LUT output. Δv_{link}^{*} is derived based on the flow-chart (operating at line frequency) shown in Figure 6.9, which settles $v_{link\_avg}^{*}$ to a steady state value. For every grid cycle, V_{diff} is calculated based on (6.19), where V_{margin} is user-defined. If V_{margin} is within the defined limit (between V_{band_low} and V_{band_high}), Δv_{link}^{*} is preserved as previous. But if V_{margin} is lower than V_{band_low}, the new Δv_{link}^{*} is obtained by adding a correction term $K_p V_{diff}$, or else if V_{margin} is higher than V_{band_high}, the new Δv_{link}^{*} is calculated by subtracting the same correction term. This minor adjustment loop operates

at a much slower rate (line frequency update in contrast to switching frequency response of LUT), but it ensures an accurate regulation of the dc-link reference $v^*_{link\_avg}$.

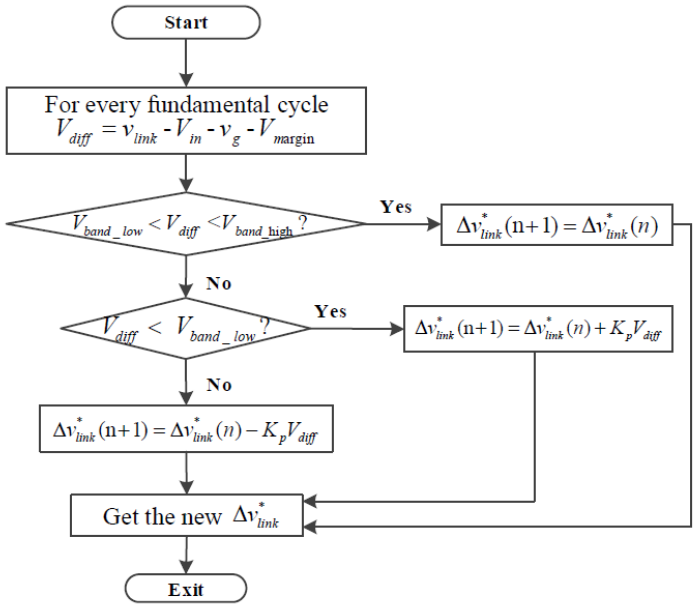


Figure 6.9. Flow-chart for Calculating Δv^*_{link} for the Adaptive Dc-link Voltage Controller Block.

$$V_{diff} = v_{link} - v_{in} - v_g - V_{margin} \tag{6.19}$$

6.4 Hardware Prototype and Experimental Results

A hardware prototype rated at 1 kVA has been built to validate the performance features of the T-type doubly grounded voltage swing inverter for transformer-less PV application as shown in Figure 6.10 (the overall converter size is 10.93 inch x 5.52 inch x 1.38 inch including the heat-sink). The input is derived from a dc source of 210 V in series with a 6.5 ohm resistor to mimic a PV panel input. LeCroy 6200A oscilloscope is

used to capture the relevant waveforms and power analyzer YOKOGAWA WT3000 is used to measure the efficiency.

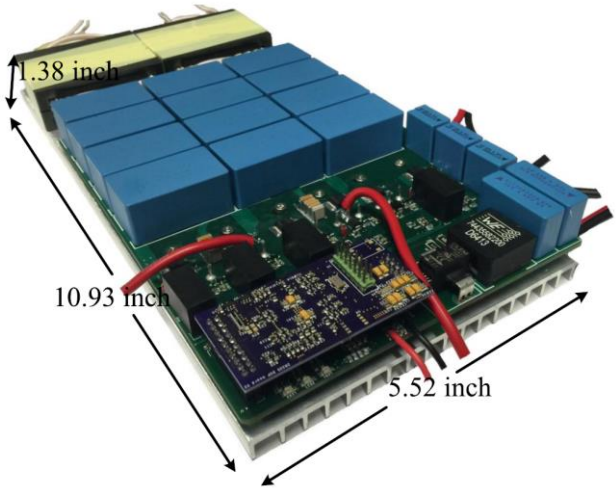


Figure 6.10. 1 kVA Experimental Prototype of T-type Doubly Grounded Voltage Swing Inverter for Transformer-less PV Application

6.4.1 Hardware Prototype

Planar ferrite core E64/10/50-3C94 with appropriate air gap on all the three limbs and Litz wire of 700 strands AWG 40 are used to custom wind both the the boost and inverter stage inductors (L_b and L_{inv}). Planar ferrite provides a low-profile design and Litz winding reduces high-frequency copper loss. L_g is an off-the-shelf component. The film capacitors for input, dc-link, and output are chosen based on the capacitance and rated voltage values as given in Table 6.4.

Table 6.4. Component Details

Component	Parameters
C_{in} , C_g	5 μF/ 250 V, 3 μF/ 200 V AC
C_{link}	55 μF/ 500 V
L_b , L_{inv}, L_g	205 μH, 180 μH, 22 μH
Q_1 - Q_6	CREE C2M0040120D (6)

CREE C2M0040120D wide bandgap SiC MOSFETs are used for all the switches including the T-branch. In order to eliminate the body diode recovery loss, CREE C4D05120E SiC schottky diodes are connected in parallel to each of the MOSFETs. Avago ACPL 337J is used as the driver IC, with a negative voltage for a reliable device turn-off. The T-branch is connected in a common emitter configuration as shown in Figure 6.1, so that they share one isolated power supply. The controller is implemented in a customized DSP board built with TMS320F28335. The auxiliary power as required by the gate driver and controller section is derived externally.

6.4.2 Steady State Experiment Results

The results represented in this section correspond to 1 kVA, UPF operation at steady state. Figure 6.11a shows the experimental results of input voltage v_{in}, grid voltage v_g, output current i_g, dc-link voltage v_{link}, and the difference voltage v_{link} - v_{in}. The grid current has a THD of 2.3% calculated by using fast Fourier transform (FFT) in MATLAB on the measured i_g data. Figure 6.11b shows the magnified input voltage and different converter currents - input, boost stage inductor, and inverter stage inductor (i_{in}, i_b, and i_{inv} respectively). It is shown that the double line frequency power has been decoupled through C_{link}, and hence, the input voltage has negligible double line frequency ripple.

The dc-link voltage ripple is 120 V with an average of 410 V. The input voltage contains both 120 Hz and switching frequency ripple. The 120 Hz ripple (obtained using MATLAB FFT) is only 4 V, which is 2.2% of the average input voltage of 180 V, demonstrating that the performance of input voltage controller is good in restricting the 120 Hz ripple only to the dc-link making the input free of double line frequency ripple. It can be seen that these hardware results match very well with the corresponding simulation results shown in Section 6.2.

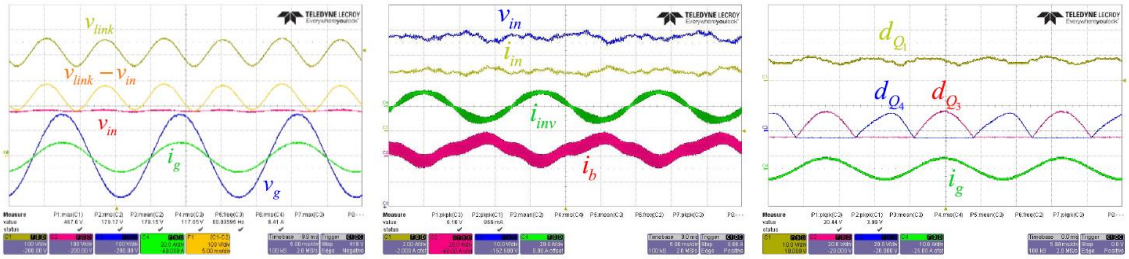


Figure 6.11. Steady State Waveforms at 1 kVA, UPF Operation with 180 V Input, 410 V DC-link Average, and 120 V/60 Hz Output (time : 5 ms/div). (a) Input and Output Voltage and Current (voltage: 100 V/div, i_g: 20 A/div), (b) Magnified Input Voltage and Converter Currents (v_{in}: 10 V/div, i_{in}: 2 A/div, i_b; i_{inv}: 20 A/div), (c) Cycle-by-cycle Averaged Duty Ratios of the Boost and Inverter Dtages (i_g: 10 A/div).

Figure 6.11c shows the duty ratios of the boost stage and the half-bridge inverter stage. The T-branch stage switches at line frequency, and hence, is not shown here. The duty ratio is obtained by cycle-by-cycle averaging of measured gate voltage V_{gs} of the two stages. As V_{gs} is 20 V when turned ON and -6 V when turned OFF, the 0 and 1 of the duty ratio can be established from Figure 6.11c accordingly. The waveforms match very

well with the analysis and simulation results shown in Section 6.2, where the presence of 120 Hz components in the duty ratio is comprehensively explained.

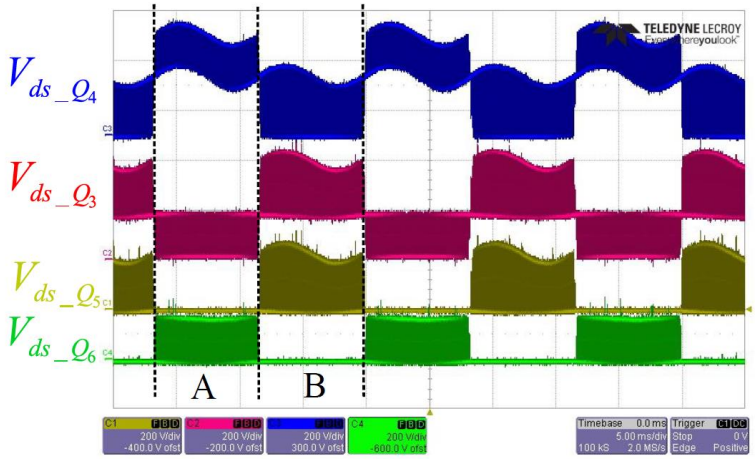


Figure 6.12. Steady State Device Drain-to-source Voltage for T-type Half-bridge Inverter Stage at 1 kVA, UPF Operation (voltage: 200 V/div, time: 5 ms/div).

Figure 6.12 shows the drain-to-source voltage of the MOSFETs in the half-bridge inverter stage with the T-branch (V_{ds_Q3}, V_{ds_Q4}, V_{ds_Q5}, and V_{ds_Q6}). As Q_3 modulates the input voltage v_{in} (which has negligibly small ripple component) to generate positive half of v_g, V_{ds_Q3} profile is a constant while it is switching (interval A). On the contrary, as Q_4 modulates v_{link} - v_{in} which has double-line-frequency component to mitigate the influence of dc-link ripple on the grid output, V_{ds_Q3} profile also contains 120 Hz ripple while it is switching (interval B).

Profiles of V_{ds_Q5} and V_{ds_Q6} can be similarly explained. While switching, the switch voltage stress on Q_3 and Q_4 is shown to be half of the dc-link as expected, while the absolute stress on them is still the dc-link as discussed previously.

Figure 6.13 shows the instantaneous drain-to-source voltage of the MOSFETs Q_2 (V_{ds_Q2}) and Q_4 (V_{ds_Q4}) and the two inductor currents at around -45° of the output voltage (between negative peak and zero crossing) at 50 kHz to highlight some of the switching waveforms using SiC MOSFETs. With almost the same inductor values for each stage, the peak-peak ripple of i_b (around 8.2 A) is around double that of i_{inv} (around 4.3 A) as the half-bridge inductor switching voltage is halved due to the T-type implementation compared to that of the boost stage. Also the boost inductor current ripple remains nearly constant while the inverter stage ripple varies with the point on the sine wave with the maximum value of 6.5 A.

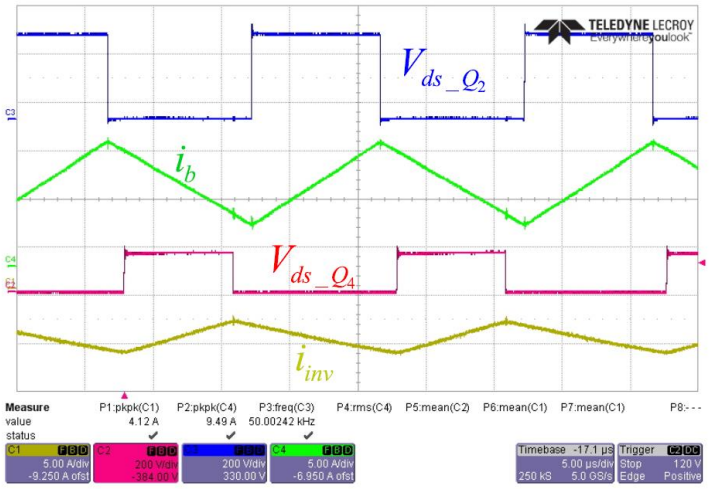


Figure 6.13. Instantaneous Switching Level Waveforms at 1 kVA, UPF Operation (voltage: 200 V/div, current: 10 A/div, time : 5 us/div).

6.4.3 Adaptive Dc-link Waveforms

This section presents the transient waveforms of the T-type doubly grounded voltage swing inverter with the adaptive dc-link voltage control scheme implemented.

Figure 6.14a shows the transient waveforms of the inverter in the grid-connected configuration when the active-power command is given a step change from 500 W to 1 kW with v_{in} = 190 V, at UPF operation, i.e., pf = 0°. As can be seen, average value of v_{link} changes from 389 V to 409 V dynamically, as calculated from the adaptive dc-link control block. Also good tracking of step changes in active power command with transient times well below one fundamental period can be observed from the waveforms shown in Figure 6.14a.

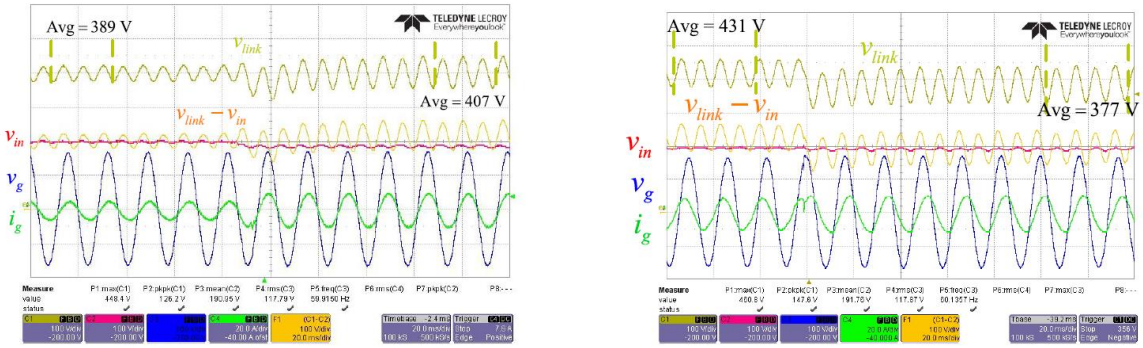


Figure 6.14. Step Change Response With the Adaptive Dc-link Control Implementation, (a) 500 W to 1 kW Step-up Load, (b) Step Change from 0.7 pf Leading to 0.7 pf Lagging at 1 kVA (voltage: 100 V/div, current: 20 A/div, time : 20 ms/div).

Figure 6.14b shows the transient waveforms of the inverter when the power factor command has a step change from 0.7 leading to 0.7 lagging, i.e., pf angle changing from 45° to -45° with v_{in} = 190 V at 1 kVA. With the implementation of the adaptive dc-link scheme, V_{avg} is noticed to change from 431 V to 377 V dynamically. It is also seen that v_{link} - v_{in} waveform is just above the instantaneous v_g at the critical point as expected with adaptive dc-link implementation. Further, good tracking of step power factor command

and transient times well below one fundamental period can be observed from the waveforms shown in Figure 6.14b.

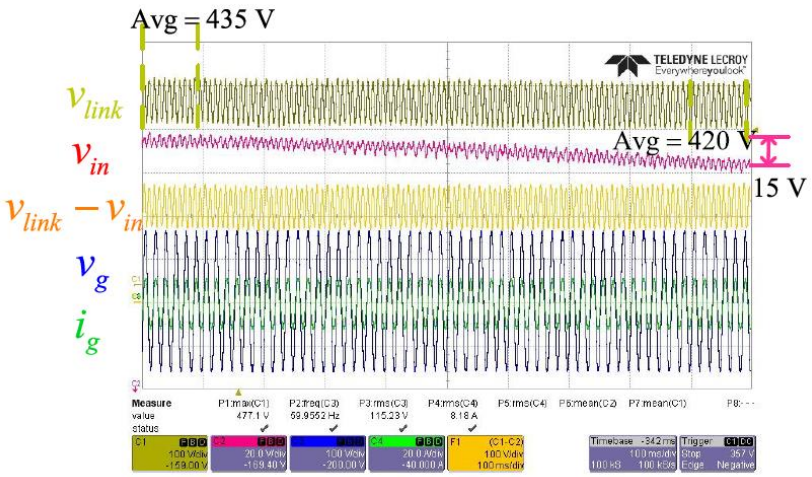


Figure 6.15. Input Voltage Step Change Response with the Adaptive Dc-link Control Implementation (v_{in}: 20 V/div, other voltages: 100 V/div, current: 20 A/div, time: 20 ms/div).

Finally, Figure 6.15 gives the transient waveforms of the inverter when the input voltage has a ramp change from 205 V to 190 V at 1 kVA UPF operation. With the the adaptive dc-link scheme, V_{avg} is noticed to change from 435 V to 420 V dynamically. Further, no change in the grid current waveforms is noticed proving good performance of the controller.

6.4.4 Efficiency

Figure 6.16 shows the efficiency measured at UPF for different power levels based on California Energy Commission (CEC) [122] requirement for PV inverters. The weighted CEC efficiency at switching frequency of 50 kHz is obtained to be 98.03% and a peak of 98.22%, without considering the controller and auxiliary power consumption

including the power for gate drivers, DSP controller, and other ICs which is around 2.7 W. It is to be noted that for UPF operation the efficiency is measured while switching the T-branch (Q_5 and Q_6) at line frequency as suggested in Table 6.2. However, for non-UPF operations, Q_5 and Q_6 will switch at carrier frequency as given in Table 6.2. In order to study the impact of this additional switching specifically, the converter was operated with Q_5 and Q_6 operating at switching frequency at UPF and the peak efficiency obtained under this scenario was 97.83% at 50 kHz switching frequency.

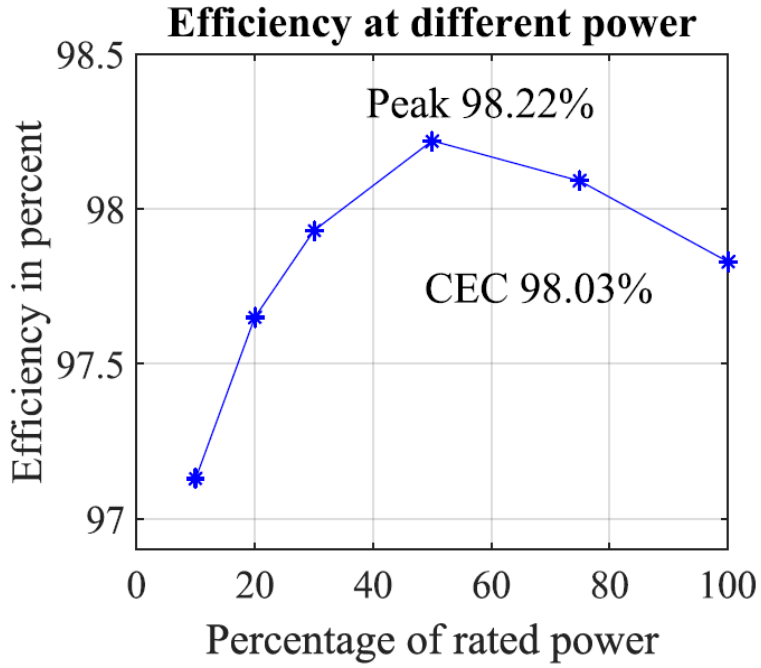


Figure 6.16. Efficiency of T-type Doubly Grounded Voltage Swing Inverter with Adaptive Dc-link Implemented

CHAPTER 7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

In Chapter 2, this thesis studied a novel transformer-less string inverter based on a single stage boost-coupled asymmetric half bridge circuit using only four active switches. It features inherent second harmonic power decoupling, achieving capacitance among the lowest reported in the literature, while ensuring negligible second harmonic content in the input PV voltage. Reduced number of semiconductor switches and use of only film capacitor lead to improved reliability and power density. By allowing direct connection of the PV negative terminal to the ac neutral, the topology inherently eliminates capacitive ground currents. Use of SiC MOSFETs leads to high CEC efficiency at switching frequencies in the range of 100 kHz. Extensive experimental results from a realistic hardware prototype validate the performance advantages of the proposed topology.

In Chapter 3, this thesis also proposes a transformer-less string inverter topology in split phase configuration using GaN switches with similar structure. Compared with previous topology, the boost inductor current 120 Hz ripple is reduced significantly to decrease the current RMS value 14% by and the peak value by 41%. Also the RMS current in the input capacitor is decreased by 91%. The dc link capacitor volume is also decreased with the increase of the voltage level. A 3 kW, 100 kHz single-phase prototype with 200 V DC input and 120 V/60 Hz AC output in split phase configuration using GaN

FETs has been built to validate the theoretical analysis. The control and modulation scheme are implemented in DSP TMS320F28335.

In Chapter 4, this thesis proposes a topology based on zero-voltage-transition (ZVT) technique to realize zero-voltage-switching (ZVS) for all the main switches of a full bridge inverter, and inherent zero-current-switching (ZCS) turn-on and ZCS turn off for the auxiliary switches. Unipolar or hybrid schemes that use zero state modulation in full bridge inverters can be implemented leading to lower THD, unlike other ZVT methods that are limited to only bipolar modulation schemes. Also this topology has naturally adaptive auxiliary inductor current and does not require large balancing capacitors. The modulation scheme and the commutation stages are analyzed in detail and the complete inverter including the auxiliary ZVT branch is modelled. Finally a 1 kW, 400 kHz switching frequency inverter of the proposed topology using SiC MOSFETs has been built to validate the theoretical analysis. The ZVT control technique and hybrid modulation scheme are implemented in DSP TMS320F28335 resulting in full ZVS for the main switches. The proposed scheme can save up to 32 % of the switching loss compared with no ZVT case leading to significant improvement in efficiency.

In Chapter 5, this thesis studied the optimal variable switching frequency scheme to minimize the combined switching loss and inductor core loss while meeting a given THD requirement. The four main types of losses in a H-bridge inverter are considered and the optimal scheme is derived based on the loss expression by using Lagrange optimization method. A 2 kW experimental prototype was built and both constant switching frequency (100 kHz) and the optimal variable frequency scheme were implemented in DSP TMS320F28335. The optimal scheme was verified by experimental

results and, while meeting the same THD requirement, it saves up to 20.9% of combined switching loss and inductor core loss compared with the constant switching frequency scheme. The optimal scheme also spreads the frequency spectrum over a wide range and reduces the dominant harmonic that appears in constant switching frequency scheme which can reduce EMI problem. This optimal scheme can be extended to other topologies or applications with similar analytical process.

In Chapter 6, this thesis proposes a high-efficiency novel T-type doubly grounded transformer-less single phase inverter with dynamic swing of the dc-link voltage which addresses the main challenges of transformer-less inverters. The proposed converter topology is a combination of a bi-directional boost and an asymmetric half-bridge stage coupled with a bi-directional T-branch to reduce the switching loss and minimize the inductor current ripple of the halfbridge inverter stage. The capacitance required for power decoupling is significantly reduced to 55 uF/kW at a 20 peak of 480 V dc-link through an active power decoupling scheme with a large swing of the dc-link voltage. Extensive experimental results from the 1 kVA SiC MOSFETs-based laboratory prototype are presented to validate the concept, design, and superior performance of the proposed topology. Moreover, the adaptive dc-link voltage control is implemented leading to a better utilization of the passive components and switching scheme under different operating (load and power factor) conditions which finally results in a peak efficiency of 98.22% and a CEC efficiency of 98.03% at 50 kHz switching frequency in the experimental prototype.

7.2 Future Work

Some improvements to the existing work are being pursued to further increase the benefits of the proposed topology and techniques.

- Variable timing control with the ZVT method can potentially increase the switching frequency to MHz level but requires complex and accurate control.
- The efficiency can also be increased with the decreased voltage rating devices.
- More integrated magnetics can be studied with complex structure to further decrease the inductor volume and loss.
- EMI behavior and the EMI filter can be studied.
- Improved thermal design can be used to optimize the volume.

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