Radiation Effects Measurement Test Structure

using GF 32-nm SOI process

by

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ABSTRACT

This thesis describes the design of a Single Event Transient (SET) duration measurement test-structure on the Global Foundries (previously IBM) 32-nm silicon-on insulator (SOI) process. The test structure is designed for portability and allows quick design and implementation on a new process node. Such a test structure is critical in analyzing the effects of radiation on complementary metal oxide semi-conductor (CMOS) circuits. The focus of this thesis is the change in pulse width during propagation of SET pulse and build a test structure to measure the duration of a SET pulse generated in real time. This test structure can estimate the SET pulse duration with 10ps resolution. It receives the input SET propagated through a SET capture structure made using a chain of combinational gates. The impact of propagation of the SET in a >200 deep collection structure is studied. A novel methodology of deploying Thick Gate TID structure is proposed and analyzed to build multi-stage chain of combinational gates. Upon using long chain of combinational gates, the most critical issue of pulse width broadening and shortening is analyzed across critical process corners. The impact of using regular standard cells on pulse width modification is compared with NMOS and/or PMOS skewed gates for the chain of combinational gates. A possible resolution to pulse width change is demonstrated using circuit and layout design of chain of inverters, two and three inputs NOR gates. The SET capture circuit is also tested in simulation by introducing a glitch signal that mimics an individual ion strike that could lead to perturbation in SET propagation. Design techniques and skewed gates are deployed to dampen the glitch that occurs under the effect of radiation. Simulation results, layout structures of SET capture circuit and chain of combinational gates are presented.

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CHAPTER 1. INTRODUCTION

1.1. Overview

Radiation effects can have a profound impact on the reliability of integrated circuits even in the relatively benign terrestrial radiation environment [Robert05]. In a radiation environment, a single event effect (SEE) results from a single, energetic particle strike. The single event effects (SEE) affect semiconductor devices and can cause both soft and hard errors. A soft error occurs when a radiation event causes enough of a charge disturbance to reverse or flip the data state of a memory cell, register, latch, or flip-flop. The error is "soft" because the circuit/device itself is not permanently damaged by the radiation. If new data is written to the bit, the device will store it correctly. A "hard" error is manifested when the device is physically damaged such that improper operation occurs, data is lost, AND the damaged state is permanent.

The single event phenomena are characterized in three effects: i) Single Event Upset (soft error), ii) Single Event Latch-up (soft or hard error), iii) Single Event Burnout (hard error). Single event upset (SEU) is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs." [Stoica04]. SEUs are transient soft errors, and are non-destructive. A SEU occurs when a radiation event causes enough of a charge disturbance to reverse or flip the data state of a memory cell, register, latch, or flip-flop. Single event latch-up (SEL) is a condition that causes loss of device functionality due to a single-event induced current state. SELs are hard errors, and are potentially destructive

(*i.e.*, may cause permanent damage). The latched condition can destroy the device, drag down the bus voltage, or damage the power supply. Single event burnout (SEB) is a condition that can cause device destruction due to a high current state in a power transistor. SEB causes the device to fail permanently. SEBs include burnout of power MOSFETs, gate rupture, frozen bits, and noise in CCDs (charge-coupled devices) [Holbert01].

In digital and analog circuits, an energetic particle strike creates a single event. A voltage pulse caused by the generation of charge by a single particle (proton or heavy ion) on a sensitive node in a circuit [NASA03] is referred to as a single event transient (SET). A sensitive node is defined as a node in a circuit whose electrical potential can be modified by internal injection or collection of electrical charges [Springer11]. This voltage pulse is only generated if the ionization impact is large enough to destabilize the sensitive node due to excess exposure for a short period of time. If the generated SET voltage pulse propagates through the circuit, it may impact its operation and potentially cause a Single Event Upset (SEU). The impact a SET has on the circuit depends on the circuit design, the voltage level of the SET pulse and the duration of the SET pulse.

SETs in linear devices were first identified following an in-flight anomaly in the TOPEX POSEIDON spacecraft [Koga93]. Since that event, SETs have been identified as the cause of several anomalies on multiple satellites including SOHO [Sorensen99] [Sorensen01], Cassini [Pritchard02], MAP [Poivey02], and TDRS. Because of the large number of both analog and digital components used in spacecraft, this phenomenon is a significant problem. To avoid the occurrence of an SEU in a radiation environment, the SET generated due to ionizing radiation must be suppressed before it gets captured by the sequential or memory element.

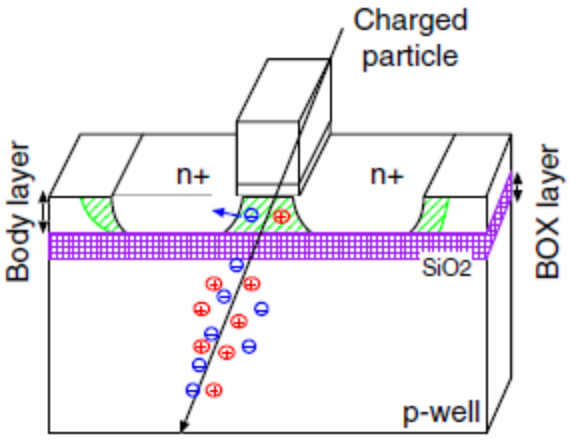


Fig. 1.1 Single event effect on a SOI transistor [Jun01]

The work in this thesis targets a SET measurement test structure that receives a SET input pulse generated due to the impact of exposure to a radiation particle strike. A SET pulse width measurement structure is required to measure the impact a SET could have on circuit functioning and its dependency on the width of the SET pulse. Building a sensitive structure that measures SET pulse widths poses serious challenges especially at deep submicron technology nodes. As the devices shrink in size and drive strength, they ought to be used redundantly to achieve the same circuit performance.

In this work, we focus on building a radiation effects measurement circuitry using the 32nm SOI process. In an SOI device, a thick, insulating, SiO2 layer isolates adjacent devices from each other and the substrate from the channels and wells as shown in Fig. 1.1. For terrestrial and space-borne electronics, implementations of SOI can result in lower power, faster switching, and improved radiation performance [Joshua01] [Corson01]. This work focusses on the latter of the three: the behavior of the Partially-Depleted SOI CMOS device under the effect of radiation. The SOI device, on the other hand poses a critical challenge: The history effect [Faynot02]. Briefly, the history effect impacts the rise and

fall transition time of frequently switching signals. For a duration measurement test circuit, the SET pulse is most vulnerable to history effect as it switches frequently while propagating through the SET collection and measurement test structure. Further, at lower nodes, the devices become more sensitive and hence result in increased SEU events under the similar ionization dosage compared to their predecessor technology nodes [Baze97].

For a circuit to operate in a radiation environment it needs to be designed such that it alleviates the SEUs created and obstructs the propagation of SETs. Techniques such as Error Detection and Correction Codes, to correct single or double bit upsets are commonly used in commercial circuits today. It is challenging to make circuits resistant to SET events since it incurs a substantial power, performance and area overhead on the design depending upon the type of hardening technique deployed.

To build a robust circuit that is hardened for SET events, it is critical to understand the i) The rate of occurrences, ii) Distribution of pulse widths and the iii) Deformation of pulse during pulse width propagation [Micro01]. Knowledge of the maximum pulse width at the output of a network of combinatorial logic is required to correctly determine the temporal gap required to implement multiple sampling techniques (double sampling for detection or TMR for mitigation) [Micro01]. The understanding of the pulse widths and the timing characteristics of the SET pulse is essential to simulate faults that may arise during SET propagation in the circuit. Large number of such simulations with varied characteristics of SET pulses can be conducted to build a robust and accurate test measurement structure. As varied types of ionizing radiations and dosage may result in SET pulse having varied widths and voltage levels, it is essential to do comprehensive

simulations and analysis. This is essential to decide the depth of the measurement structure appropriate to analyze the SET pulse produced in that specific ionization environment.

Before proceeding to the details of collection and duration measurement test structures in the subsequent chapters, a brief overview of the challenges that arise to build a radiation hardened structure are discussed.

1.2. SET Capture and SET Measurement Test Structure Challenges

A pulse width measurement test structure is designed using circuit design and sizing techniques to approximate pulse width (PW) of the SET generated with accurate resolution. In real time radiation environment, for a PW measurement structure to practically operate, a SET collection structure is essential to capture the SET pulse and propagate it to the SET PW measurement structure without distortion in its original properties, like the Pulse Width, Rise and Fall Slews and Amplitude. This collection structure must also be radiation hardened such that the propagating pulse is not disturbed by another particle strike and SET generation in a radiation environment. To maintain the original properties of the SET pulse, each stage of the collection structure must be balanced such that it propagates the exact pulse to the subsequent stage. This is challenging because each stage must be built to be radiation hardened such that it obstructs the propagation of new SET pulse and at the same time be balanced to propagate the captured pulse without any change in the pulse characteristics. For each stage to be balanced, we may choose to build each stage of the test structure using regular standard cells provided in the process design kit (PDK) or generate new custom cells using the available PDK. To make each stage of the collection structure radiation hardened, there needs to be either triple mode redundant with voting to

mitigate SETs from propagating forward in the chain or the use of specialized circuit and design techniques that help mitigate the SET.

In this work, we focus on the circuit design of such PW measurement structure that is used in a radiation environment to capture the properties of the SET pulse. We build a duration measurement test structure using a series of scan flip flops that captures the SET pulse and stores the result until the logic values are scanned out using a scan logic triggered externally. The flip flops are timed such that the setup and hold times are met with respect to the clock and the pulse is captured correctly. The propagation of pulse across the design must ensure that the characteristics of the pulse is not changed and such that the pulse is captured reliably by the measuring flip-flops. This factor is critical to ensure good resolution in the overall estimation of the pulse width of the incoming SET pulse.

1.3. Thesis Outline

Chapter 2 discusses the Thick Gate TID Structure that can be configured to be a chain of combinational gates. This concept is efficient in building stacks of INV, NAND2, NOR2 and Pass Gates by configuring the node voltages. This ensures a tillable structure that is fixed but can be configured to function like any combinational gate chain.

A 200-deep combinational gate chain for each INV, NAND2, NOR2, NAND3 and NOR3 gates is made and analyzed at all process corners for input SET pulse deformation. The chain is analyzed for pulse width and slew rate change across corners and trends are also reported. Challenges faced to maintain the pulse width across all the stages are discussed. Further, a possible solution for the issues observed in INV2 and NOR3 chain is discussed.

Chapter 3 discusses a SET duration measurement test structure. Here, we discuss details of the operation of the structure and the HSPICE simulation results that confirm the circuit behavior. The operation of a unit of two Flip Flops and capture circuit is also explained. Further, the clocking mechanism that drives the Flip Flop Chain is discussed. An essential part in the SET duration measurement test structure is the scan out logic. The functioning of the measurement structure in the scan mode is discussed. The circuit behavior is confirmed using simulation results and analysis.

Chapter 4 discusses about the SET collection structure which feeds input to the SET duration measurement structure. The techniques used to make a radiation hardened SET collection test structure are discussed in detail. Two experiments were conducted to make a robust SET collection structure are discussed using the simulation and post layout results. Pros and cons of each approach is discussed and the best among both is determined.

SET collection test structure uses combinatorial gates to function, hence the techniques used to balance the load required to maintain the pulse width and slew rate are discussed. For analysis of the SET collection structure, a SET pulse is modeled as a glitch which emulates the real scenario where an exposure to TID environment impacts a combinational gate in the collection structure. The simulation results are analyzed and discussed.

CHAPTER 2. THICK GATE – THIN GATE TID STRUCTURE

Overview

This chapter discusses about the Thick Gate and Thin Gate configurable TID effects measurement structure which is used to build a tile-able combinational logic chain. This technique is particularly useful in making the TID structure for various combinational cells with minimal changes to the underlying design. Multiple single-stage configured structures are tiled with other similarly configured TID structures to form a multi stage chain of combinational gates. The SOI technology used to build the TID structure introduces unique challenges to over the conventional planar CMOS technology.

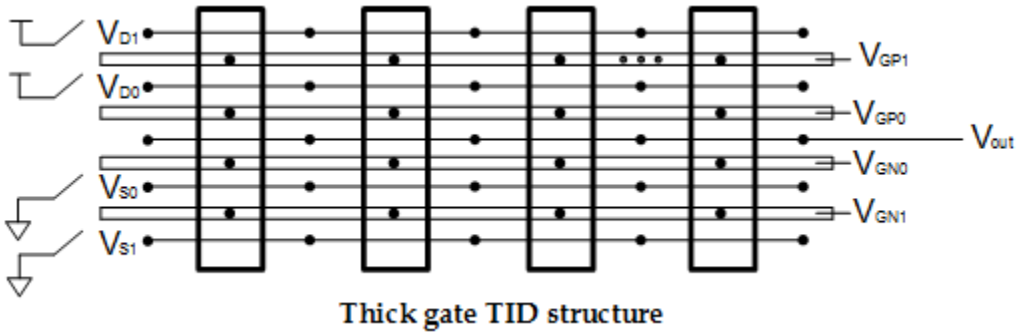
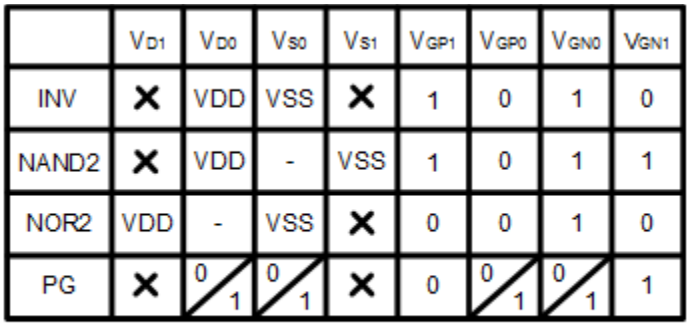


Fig. 2.1 Thick Gate TID Structure

SOI technology is particularly susceptible to the impact of TID due the presence of the thick buried oxide layer (BOX). For scaled technology nodes, the front gate oxide thickness is shrinking and therefore the impact of TID on the front gate of the transistor is negligible. Whereas, the SOI devices have a thick buried oxide layer instead of the bulk in planar CMOS devices. Under TID the charge buildup in the BOX shifts the V_{th} of the device and therefore impacts its performance. The thick oxide I/O devices may experience V_{th} shift due to the primary gate oxide as well. Previous works report that positive trapped

charge leads to a negative shift in the threshold voltage of both the NMOS and PMOS transistors [Vashisth13]. For the NMOS transistor the buildup of positive charge increases its off-state current. This increase in the off-state current affects the functioning of the circuit at macro level [Mikkola08].



	V_{D1}	V_{D0}	V_{S0}	V_{S1}	V_{GP1}	V_{GP0}	V_{GN0}	V_{GN1}
INV	X	VDD	VSS	X	1	0	1	0
NAND2	X	VDD	-	VSS	1	0	1	1
NOR2	VDD	-	VSS	X	0	0	1	0
PG	X	0/1	0/1	X	0	0/1	0/1	1

Thick gate TID table

Fig. 2.2 Thick Gate TID Table.

2.1. Single Stage Thick Gate TID structure

The tile-able single stage thick gate TID structure comprises of thick gates connected to the common control nodes as shown in Fig. 2.1. This structure can be configured to make an INV, NAND2, NOR2 and pass gate structures using the common control nodes. The common control nodes can be configured using the settings described in Fig. 2.2 to operate as an INV, NAND2, NOR2 or pass gate single stage cell. The single stage TID structure can be tiled to generate a combinational logic chain.

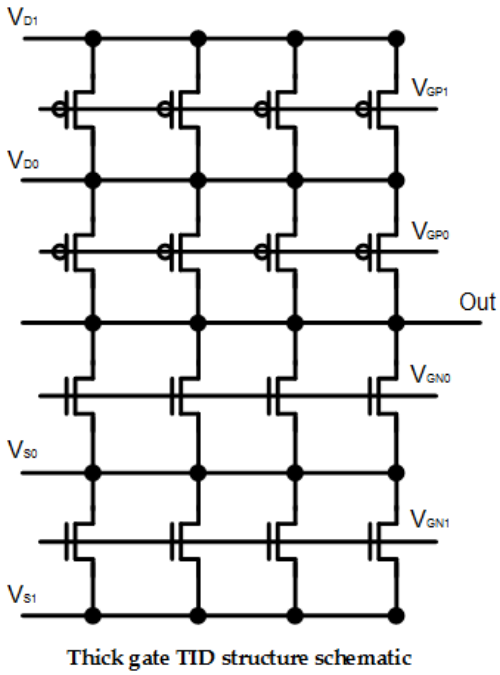


Fig. 2.3 Thick Gate TID Structure Schematic Representation.

The following sections will discuss the configurations required for the TID structure to operate as an inverter, 2-input NOR, 2 input NAND and pass gate. Further, we will also discuss about the pulse width change seen while building a high performance multi stage combinational gate chain. The combinational gate chain must ensure minimum degradation in the pulse width when a pulse propagates through it.

2.1.1. Inverter Configuration

The TID structure schematic shown in Fig. 2.3 can be configured to operate as a single stage inverter as shown in Fig. 2.4. This requires the control nodes to be configured such that the diffusion connections V_{D0} and V_{S0} are connected to V_{DD} and V_{SS} respectively and the V_{D1} and V_{S1} is set as don't care signals. The gate voltages V_{GP1} and V_{GN1} must be connected to logic 1 and logic 0 respectively. This will ensure that the stacked PMOS and NMOS transistors are turned off. The gate voltages V_{GP0} and V_{GN0} must be set as logic 0

and logic 1 respectively to turn on both the PMOS and NMOS transistors of the single stack inverter. For measurement of leakage current, the worst case is obtained when V_{GP0} and V_{GN0} is connected to logic 1 and logic 0 respectively, which turns off both the PMOS and NMOS transistors. For a multi-stage combinational chain, the TID structure shown in Fig. 2.1 is tiled in parallel with several other similar structures that are configured based on the required combinational logic chain.

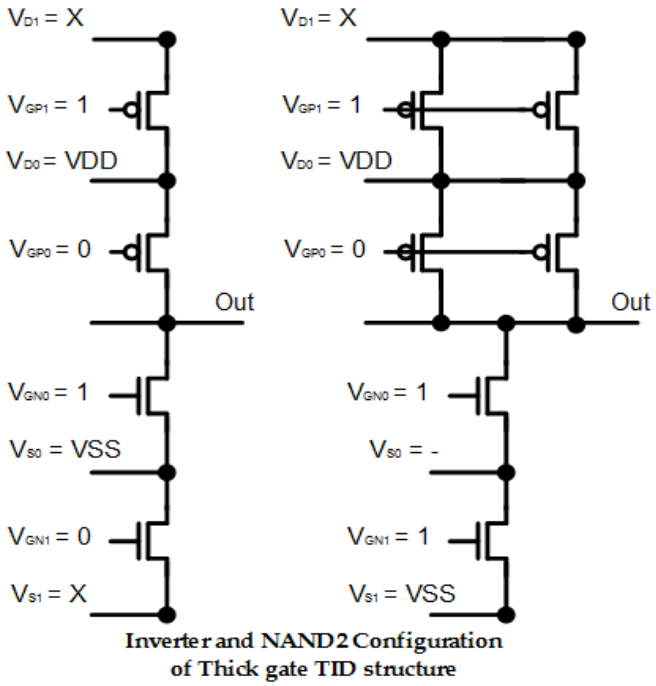


Fig. 2.4 Inverter and NAND2 Configuration of Thick Gate TID Structure.

2.1.2. NAND Configuration

The TID structure schematic shown in Fig. 2.3 can be configured to operate as a single stage 2 input NAND cell as shown in Fig. 2.4b. This requires the control nodes to be configured such that the diffusion connections V_{D0} and V_{S1} are connected to V_{DD} and V_{SS} respectively and the V_{D1} and V_{S0} are set as don't care and idle respectively. The gate voltages V_{GP1} and V_{GP0} must be connected to logic 1 and logic 0 respectively. This will

ensure that the NAND gate is a single stack 2 input NAND gate configuration where the top most stack is not functional. The gate voltages V_{GN1} and V_{GN0} must be set as logic 1 for the series NMOS devices are turned on for operation. In this configuration, both the pull up and pull-down transistors are shown as on for representation only, whereas in normal operation, only one of these networks will be on. To build a multi-stage combinational chain, the 2 input NAND structure can be repeated with several other similarly configured structures.

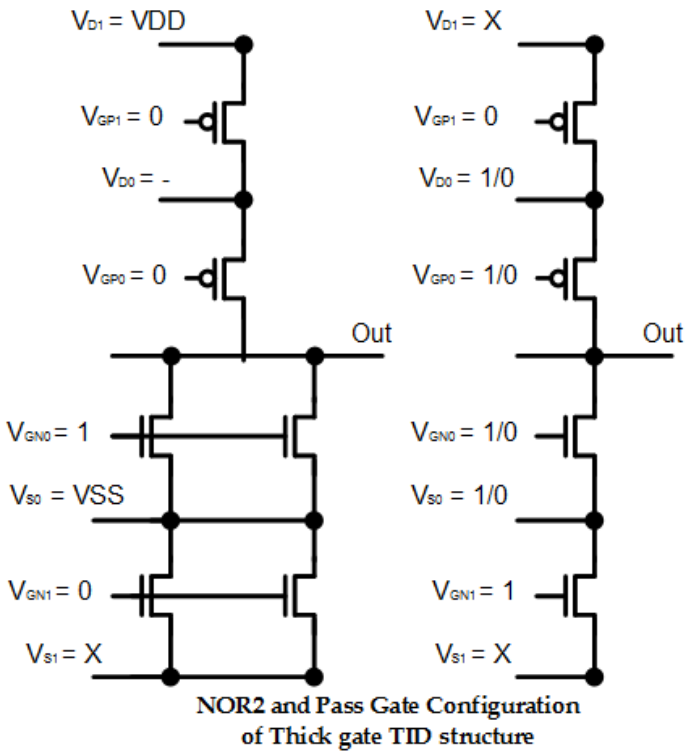


Fig. 2.5 NOR2 and Pass Gate Configuration of Thick Gate TID Structure.

2.1.3. NOR Configuration

The TID structure schematic shown in Fig. 2.3 can be configured to operate as a single stage 2 input NOR cell as shown in Fig. 2.5. This requires the control nodes to be configured such that the diffusion connections V_{D1} and V_{S0} are connected to V_{DD} and V_{SS} respectively. The V_{D0} and V_{S1} nodes are set as don't care and intermediately connected respectively. The gate voltages V_{GP1} and V_{GP0} must be connected to logic 0 for series PMOS to be turned on. The gate voltages V_{GN1} and V_{GN0} must be set as logic 0 and logic 1 respectively. This forces the NMOS connected to V_{S1} node to be in off state and the ones connected to V_{S0} to be in on state. In this configuration, for representation only, both the pull up and pull-down transistor networks are shown as being on, whereas in normal operation, only one of these networks will be on. To build a multi-stage combinational chain, the 2 input nor structure can be repeated with several other similarly configured structures.

2.1.4. Pass Gate Configuration

The TID structure schematic shown in Fig. 2.3 can be configured to operate as a single stage pass gate as shown in Fig. 2.5b. This requires the control nodes to be configured such that the diffusion connections V_{D0} and V_{S0} can be either V_{DD} or V_{SS} based on the input required for the pass gate. The V_{D1} and V_{S1} nodes are set as don't care signals. The gate voltages V_{GP1} and V_{GN1} must be connected to logic 0 and logic 1 respectively as they drive the input of the pass gate at node V_{D0} and V_{S0} respectively. The gate voltages V_{GP0} and V_{GN0} can be either set as logic 0 and logic 1 or logic 1 and logic 0 as these nodes must be complementary to turn on or off the pass gate. For a multi-stage combinational

chain of pass gates, the TID structure shown in Fig. 2.5b is tiled in parallel with several other similar structures that are configured based on the required combinational logic chain.

To make the configurable TID structure efficient, the combinational gate chain used for SET collection circuit must be compatible with the TID structure. The next section we will discuss about the challenges seen during simulation of the INV and two and three input NOR combinational gate chain which are relevant to the SET measurement and collection structure. We will see the impact of using PDK provided standard cells on the pulse width change, which is critical to maintain across a multi-stage chain.

2.2. Pulse Width Change Analysis

The TID structure must be compatible with the combinational gate chain used for SET collection structure in a hierarchically top-level circuit. This section discusses about the pulse width analysis done on single and multiple input combinational gate chain. Consistent with previous studies, in our analysis, an input SET to a multi-stage combinational gate chain is observed to change pulse width as it traverses across a chain of combinational logic cells [Cavrois07]. The degree of pulse broadening or shortening depends upon the transistor design and the length of propagation. If the input pulse generated is wide enough to be captured by a sequential standard cell within the chain of combinational logic cells then the impact of the pulse width change can be studied [Nicolaidis03]. In previously conducted studies it is presented that SET pulse broadening is induced by variations of the body (or well) potential, depending on the previous states of the transistor. This dynamic charging/discharging of the transistor body, also called a floating body or history effect [Gautier95] [Wei96], modifies the electrical response of SOI chains to SET propagation [Cavrois08]. Other researches such as the one presented in

[Harada12] report that a long combinational chain involves pulse-width variation due to propagation induced pulse broadening (PIPB) [Cavrois08] and mismatch between rise and fall delays [Furuta11], which may excessively increase the pulse-width or vanish the pulse itself.

It is critical to address the issue of pulse width modification during the propagation of a SET for the duration measurement and SET collection circuit to operate reliably. To minimize the degradation in pulse width across multi-stage chain it is essential to minimize the degradation for each stage, across each RC corner. It is our understanding that the pulse width change can be carefully minimized by using appropriate P width and N width for a single-stage in combinational gate chain. Using appropriate P and N widths ensure equal rise and fall time for an input pulse. This has also been shown through experiments, that the pulse widths are significantly impacted by the choice of standard process design kit (PDK) MOS variants and layout variations such as threshold voltage and body contact [Maharrey13]. Skewed gates help achieve unchanged pulse widths at the output of a chain of combinational logic gates. This can be confirmed mathematically using the well-known relationship between delay, current and capacitance which is proportional to the width of the transistor,

$$\tau = \frac{CV}{2I},$$

where τ is the delay, C is the capacitance, V is the voltage of operation and I is the current. As the rise and fall times are related with capacitances though the above delay formula that clearly shows changing the current and capacitance by changing the device width can yield a break-even point where the rise and fall match across all corners. The key is to balance the rise and fall delays to be equal. Thus, if the process corner increases

the PMOS delay (rise times) it affects all the gates equally, as there is a rise in every other gate in the chain for an inverting logic chain of combinational gates. Similarly, for NMOS and fall delay. The break-even point in the point where the pulse width should remain unchanged. This would enable designers to use longer SET test structure, avoiding other complex circuit techniques to maintain the pulse widths.

Our simulation results on the 32-nm SOI PDK depict that the input pulse generated through SET events does indeed change for a combinational logic chain. The pulse width varies per the P and N width of the devices chosen for simulation. The subsequent sections discuss about our experiments done to measure the change in pulse width. We discuss about an inverter and a 3 input nor chain and show the impact of using native PDK provided cells. We compare the pulse width change seen by using native cells and skewed cells using a customized P and N width.

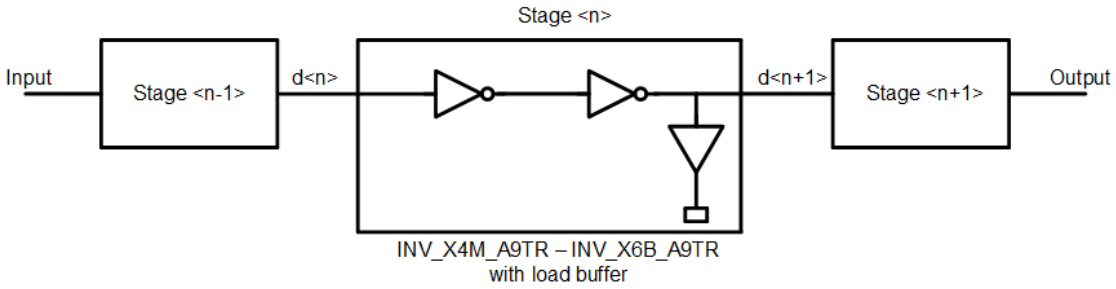


Fig. 2.6 Inverter Chain with Balanced Buffer Load. Three Stages Connected in Series.

2.2.1. Inverter Chain TID/SET Structure

A chain of inverters is required for the SET measurement structure to propagate the incoming SET pulse. The SET at each stage, i.e. after every pair of inverters is fed as input the Flip Flop, in the chain. Long chain of inverters as the target circuit is preferred to improve area efficiency. This helps improve the area ratio of the target circuit to the

measurement circuit. It is critical to maintain the SET pulse width for each stage of the inverter chain to obtain high resolution of the estimated pulse width.

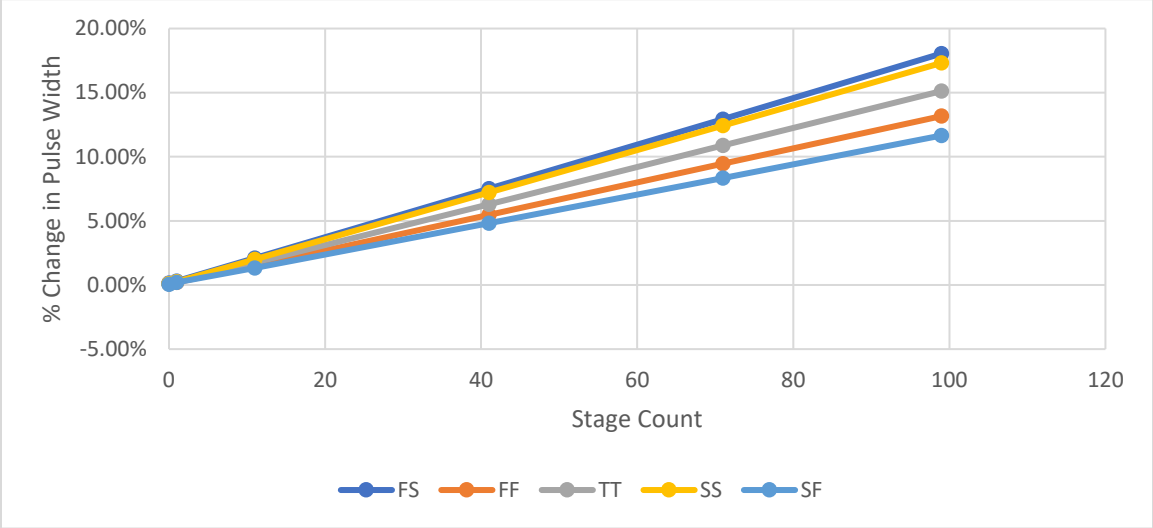


Fig. 2.7 Change in Pulse Width of Inverter Chain With 100 Stages Using Unmodified Gates.

We built an inverter chain using standard cells provided with the IBM SOI 32nm PDK. Each stage of the inverter chain comprises of an INV_X4M_A9TR and an INV_X6B_A9TR cell. The output of each stage is connected to the input of another similar stage. This configuration connects the chain with pair of inverters in series. The schematic representation of the inverter chain is shown in Fig. 2.6. The simulation of the circuit shown in Fig. 2.6 is performed for each of Slow Fast (SF), Slow Slow (SS), Typical Typical (TT), Fast Fast (FF) and Fast Slow (FS) corners. The results of the simulated schematics are captured in Fig. 2.7. As shown, the input pulse width of 205ps gets increased by +18.05% to 242ps at the FS corner. The increase in pulse width is greater than 11% for each analysis corner for an inverter chain with 100 depths, with an approximate worst case increase of 370fs per stage. The stage wise change in pulse width is reported in Table 2-1.

Corner	Stage<0>	Stage<1>	Stage<11>	Stage<41>	Stage<71>	Stage<99>
FS	0.15%	0.29%	2.10%	7.51%	12.93%	18.05%
FF	0.10%	0.20%	1.51%	5.46%	9.46%	13.17%
TT	0.10%	0.24%	1.76%	6.29%	10.88%	15.12%
SS	0.10%	0.24%	2.00%	7.22%	12.44%	17.32%
SF	0.05%	0.20%	1.32%	4.83%	8.34%	11.66%

Table 2-1 Stage Wise Percentage Change in Pulse Width for Inverter Chain

In a regular digital circuit, similar amount of degradation may not be significant as the total depth for a logic path is ~15-20 stages. Also, in a regular logic design each stage is different, this helps averaging out the pulse width increase and decrease. For a high precision, SET measurement structure this is not the case, as each stage is a replica of any other stage and therefore the impact of pulse width change increases as the SET propagates. Moreover, normal designs are edge and not pulse based. A smaller degradation or shorter chain would allow the pulse distortion to be calibrated out by simply setting a non-fixed value for each FF delay when calculating the measured width is sufficient. This is not possible in the SET target structure, where the point of impact cannot be known. Further, the pulse duration will change with the precise process corner of the fabricated silicon as is seen in the simulation results shown in Fig. 2.7. In general, the FF and SS corners do not cause much of an issue as the N and P delays are similarly affected. However, the actual silicon will deviate away from equal impact on NMOS and PMOS. Thus, the pulse lengths will be affected unless the design properly mitigates these process variation effects across other extreme corners such as FS and SF.

Various circuit design techniques can be applied to balance the circuit such that the pulse width change is minimized. As discussed earlier, we use matched capacitive stages that comprise of identically loaded gates, where sum of the delays is due to a rising PMOS

and a falling NMOS for each of the inverter output rising and falling edges. If these delays (and capacitive loads) match at each inversion, any delta in either PMOS or NMOS is reflected in both edges. Consequently, the pulse width is constant across Process Voltage and Temperature (PVT) corners.

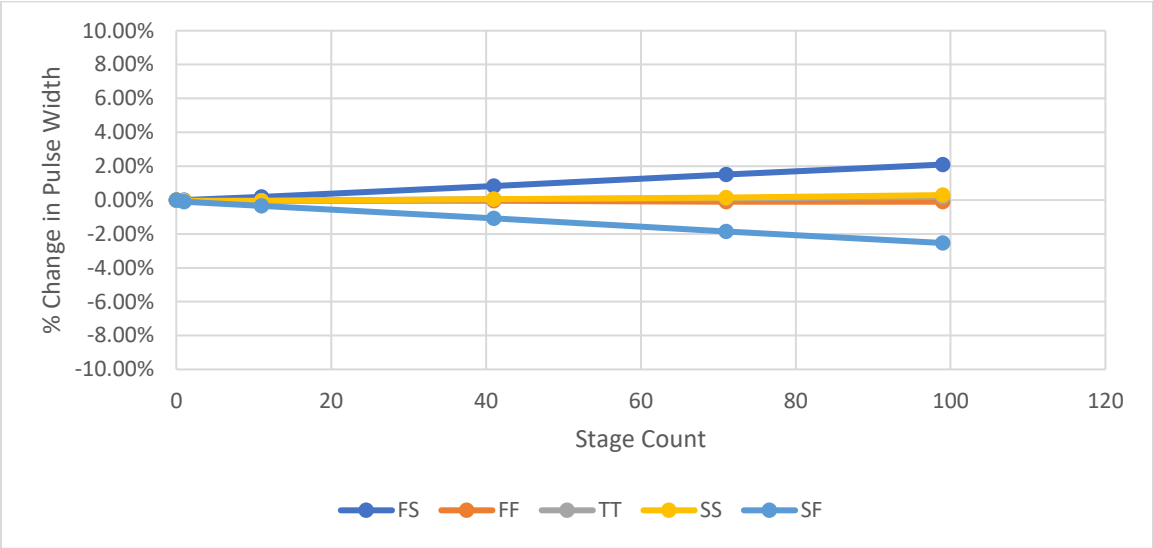


Fig. 2.8 Change in Pulse Width of Inverter Chain With 100 Stages Using Skewed Gates.

Corner	Stage<0>	Stage<1>	Stage<11>	Stage<41>	Stage<71>	Stage<99>
FS	0.00%	0.00%	0.20%	0.83%	1.51%	2.10%
FF	0.00%	-0.05%	-0.05%	-0.05%	-0.10%	-0.10%
TT	0.00%	-0.05%	-0.05%	0.05%	0.10%	0.20%
SS	0.00%	-0.05%	-0.05%	0.05%	0.15%	0.29%
SF	0.00%	-0.10%	-0.34%	-1.07%	-1.85%	-2.54%

Table 2-2 Stage Wise Percentage Change in Pulse Width for Inverter Chain with Skewed Gates

The simulation results after using skewed gates (INV_X4M_A9TR and INV_X6B_A9TR) such that each stage is matched and has balanced load capacitances shows a significant improvement in the pulse width for an inverter chain. The simulation is performed at each of the FS, SS, TT, FF, SF corner and results are represented in Fig. 2.8. The worst-case degradation of -2.54% in pulse width at the output of the inverter chain

is obtained at the SF corner. The pulse width change ranged from 2.10% at the FS corner to -2.54% in the SF corner, with

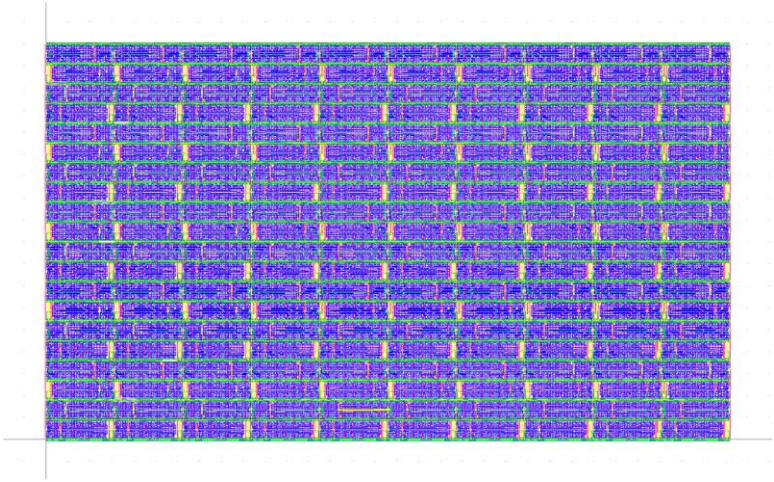


Fig. 2.9 Layout Design of The Inverter Chain With 100 Stages. The Layout Size Is 31.2 µm x 18 µm.

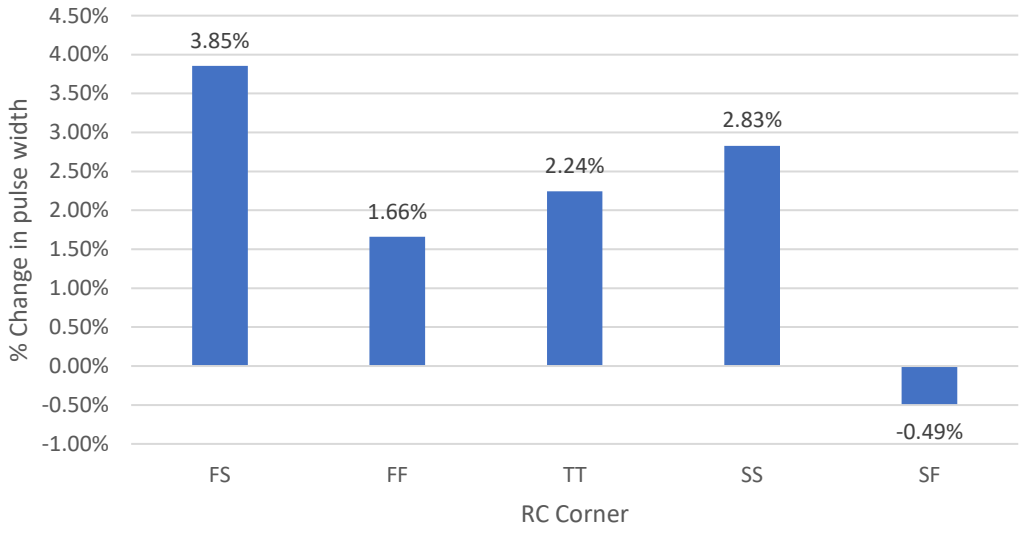


Fig. 2.10 Post Layout Results. Stage Wise Percentage Change in Pulse Width for Inverter Chain with 100 stages.

0.20% pulse width change at the TT corner. The results of the pulse width change at intermediate stages is captured in Table 2-2.

Custom layout of the inverter chain with skewed gates was done using 32 nm SOI PDK as shown in Fig. 2.9. The layout size is 31.2 µm x 18 µm. The layout is done using 'Modgen' in Virtuoso Layout Suite. The design is carefully done to match load capacitance, any change in which may significantly impact the pulse width. The connectivity in the layout is done in a serpentine manner such that the route length and metal layer used can be equalized. Modgen helps connect each stage of the inverter chain in a predefined pattern which ensures that the R and C for each connection is same. The layout is then simulated and the change in pulse width is reported in Fig. 2.10. The layout results depict the worst-case pulse width change of +3.85% at the FS corner. The layout design showing the dimensions in µm is depicted in Fig. 2.9.

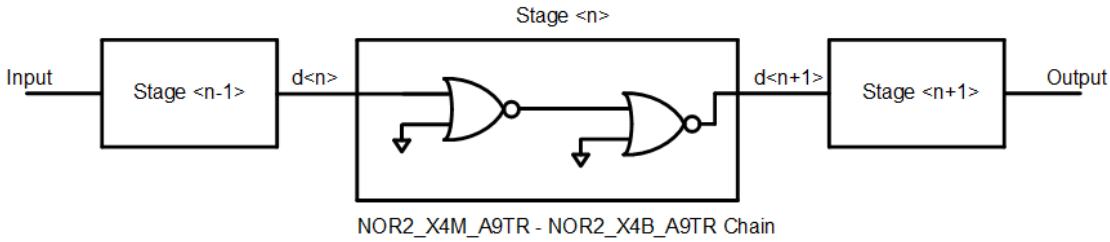


Fig. 2.11 Schematic Representation of 2-Input NOR Chain Having 3 Stages.

Similar analysis is done with input pulses with width varying from 10ps to 205ps on the balanced inverter chain and it is observed that matched capacitive load helps reducing the pulse width change as the pulse propagates through a multi-stage inverter chain. In the next section, we will see the pulse width change response of a 2 input NOR chain.

2.2.2. NOR2 Chain TID/SET Structure

The 2 input gates such as NOR gates are predominantly used in building SET collection circuits [Cannon09]. This is because of their high SET cross-section

[Cannon09]. We use NOR2 gates and inverters in the SET collection structure that will be explained in Chapter 4. For pulse width change analysis, we use two 2 input NOR gates in a single stage as shown in Fig. 2.11. Each of the NOR gates used is a 4x size gate which allows a high SET cross-section and shows less degradation in pulse width during SET pulse propagation as compared to low drive strength NOR gates. One input of each of the NOR gates is tied to ground, and the other input is driven by the output of the previous NOR gate, as depicted in Fig. 2.11.

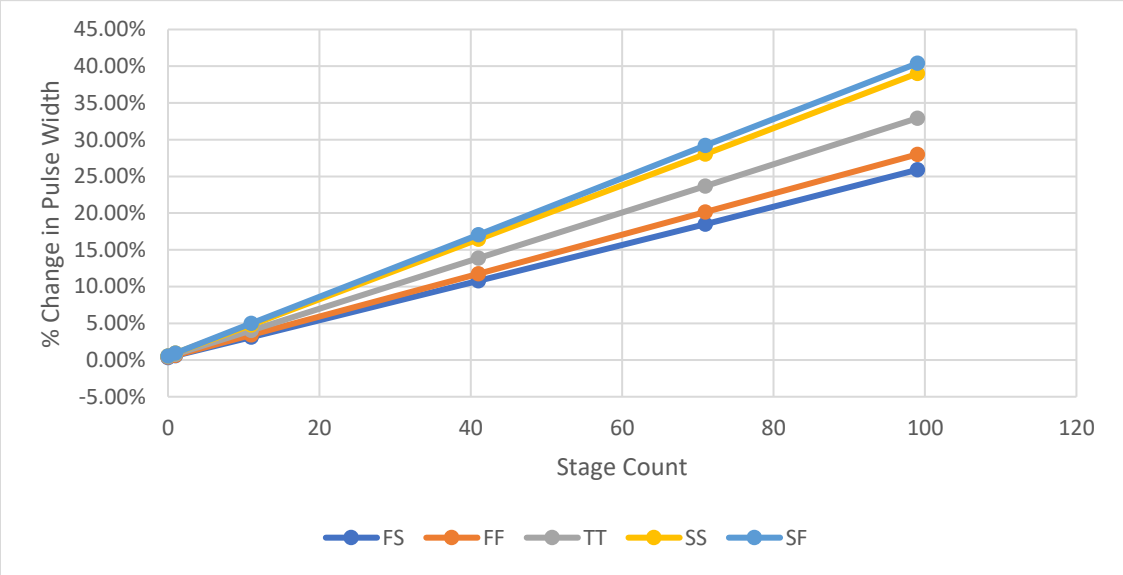


Fig. 2.12 Change in Pulse Width of 2 input NOR Chain With 100 Stages Using Unmodified Gates.

The input to the NOR chain is a SET, which is tested in simulation using varied pulse widths from 20ps to 205ps with 50% duty cycle and 5ps rise and fall transition time. The results of the simulation with input pulse width of 205ps is shown in Fig. 2.12. The pulse width seen at the output of the 2 input NOR chain has a worst-case increase in pulse width of +40.39% at the SF corner, i.e. 828fs of increase in pulse width per stage. For this analysis, the change in pulse width is >+25.90% for each of the FS, SS, TT, FF, SF corner.

The pulse width observed at each corner is listed in Table 2-3. As shown, the simulation results show a huge change in pulse width across a 2 input NOR chain. As explained earlier, pulse width changes occur due to unbalanced stages, unoptimized P/N width sizes and floating body effect which changes the V_{th} of the device thereby affecting the rise and fall times. This analysis was done using natively provided, unoptimized standard cells.

Corner	Stage<0>	Stage<1>	Stage<11>	Stage<41>	Stage<71>	Stage<99>
FS	0.34%	0.59%	3.12%	10.78%	18.49%	25.90%
FF	0.39%	0.63%	3.41%	11.76%	20.15%	28.00%
TT	0.44%	0.78%	4.05%	13.85%	23.66%	32.93%
SS	0.54%	0.93%	4.78%	16.44%	28.05%	39.02%
SF	0.54%	0.93%	4.98%	17.07%	29.22%	40.39%

Table 2-3 Stage Wise Percentage Change in Pulse Width For 2 Input NOR Chain

Another simulation analysis is done using balanced capacitive load for the 2 input NOR chain. From the previous simulations, it was observed that the fall times were too slow and had a huge impact on the overall pulse width for each stage. The driver NOR gate: NOR2_X4M_A9TR has larger NMOS transistor than the receiver gate: NOR2_X4B_A9TR and hence experimental changes in the NMOS of the driver gates showed little improvements in the overall pulse width change. In another experiment, the NMOS transistor for the receiver NOR gate in each stage is skewed to be of 207nm rather than the original 176nm in width. This resulted in improved results for the 2 input NOR gate as shown in Fig. 2.13. Using the skewed driver 2 input NOR gate in each stage of a 100 stage NOR chain, the worst-case pulse width change was reduced by 10x to +4.93% at the SF corner. The pulse width change ranged from -2.44% at the FS corner to +4.93%

in the SF corner, with 1.41% pulse width change at the TT corner. The stage-wise results are shown in Table 2-4.

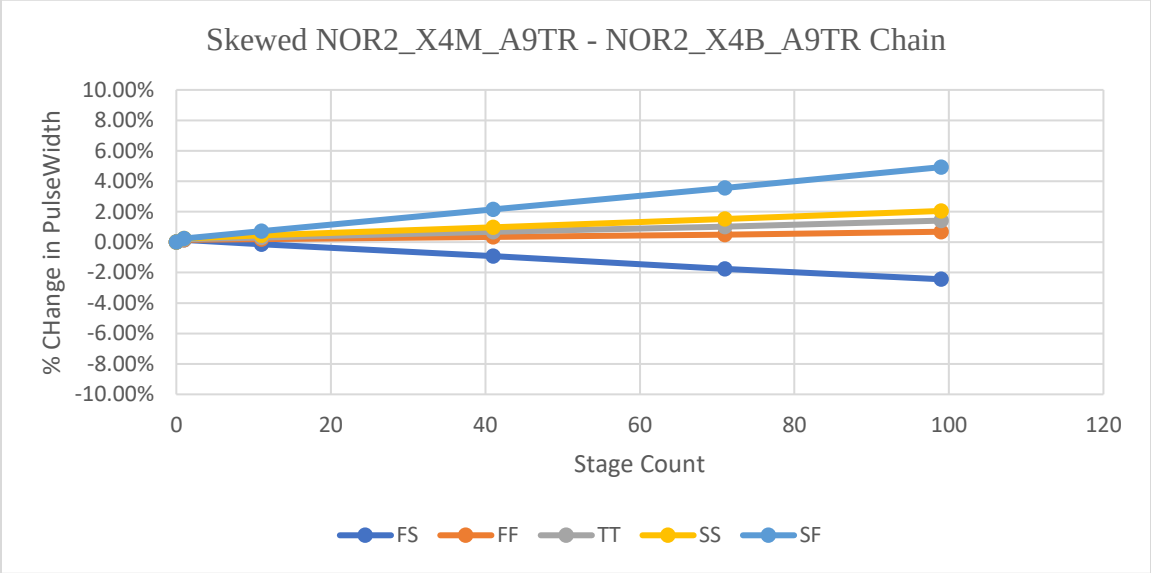


Fig. 2.13 Change in Pulse Width of 2-input NOR Chain With 100 Stages Using Skewed Gates.

Corner	Stage<0>	Stage<1>	Stage<11>	Stage<41>	Stage<71>	Stage<99>
FS	0.00%	0.15%	-0.15%	-0.93%	-1.76%	-2.44%
FF	0.00%	0.15%	0.20%	0.34%	0.49%	0.68%
TT	0.00%	0.20%	0.29%	0.68%	1.02%	1.41%
SS	0.00%	0.24%	0.44%	0.98%	1.51%	2.05%
SF	0.00%	0.24%	0.73%	2.15%	3.56%	4.93%

Table 2-4 Stage Wise Percentage Change in Pulse Width For 2 Input NOR Chain with Skewed Gates

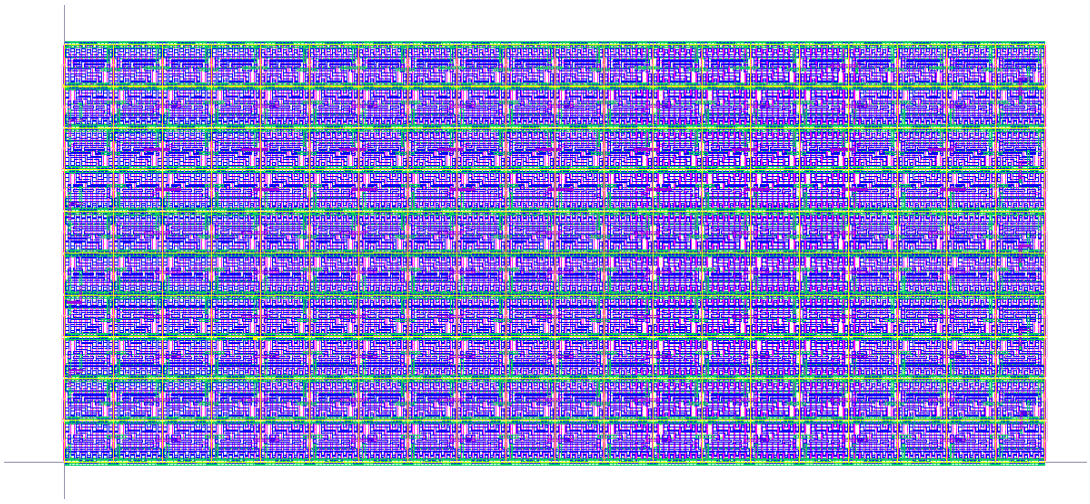


Fig. 2.14 Layout Design of the 2 Input NOR Chain Having Skewed Gates. The NMOS of the Receiver Gate is 207nm Wide.

The custom physical design of the 2 input NOR chain with skewed gates was done using Virtuoso Layout Suite. The layout was done using Modgen, which helped in placing the cells in a user-defined pattern. The size of the layout with 100 stages, each of them containing a NOR2_X4M_A9TR and a NOR2_X4B_A9TR is 23.4 μm x 9 μm. The layout is done by placing 10 rows of 10 stages each connected in a serpentine. The routing of the design is carefully performed to have matched capacitance for each stage. This is a necessity because it has a significant impact on the load capacitance of each stage. The post layout design is shown in Fig. 2.14. The parasitic extraction of the 2 input NOR chain layout is done using Calibre PEX, and the extracted netlist is simulated to observe pulse width change. It is seen that the worst-case pulse width change is +9.27% at the SF corner of the post layout design as shown in Fig. 2.15. To reduce the pulse width, change for the post layout simulation, we performed multiple other floorplans. It is seen that pulse width change improves by 1-2% if the layout contains 1 row of 100 stages connected in series. In this case, the design width increases by 10x.

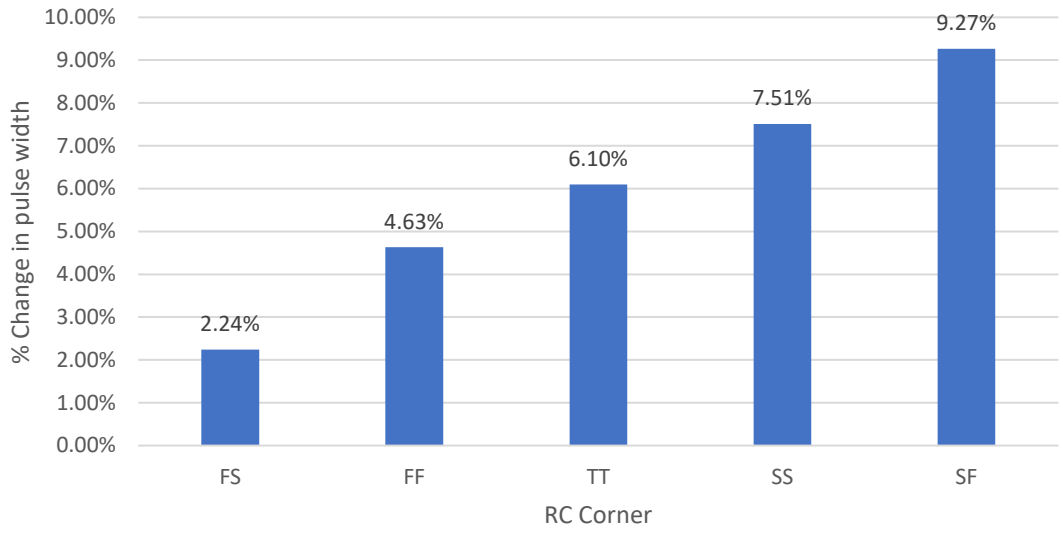


Fig. 2.15 Post Layout Stage Wise Percentage Change in Pulse Width For 2 Input NOR Chain.

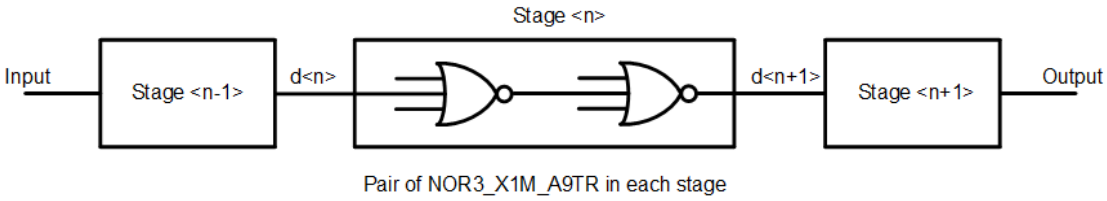


Fig. 2.16 Schematic Representation of 3 Input NOR Chain Having 100 Stages.

Now we perform similar analysis on a 3 input NOR gate, and conclude that the technique used for balancing capacitive load can be used generically on a single and multiple input combinational gate.

2.2.3. NOR3 Chain TID/SET Structure

For analysis of pulse width change and optimization of device parameters to minimize the change in pulse width we analyze a 3-input combinational NOR gate chain. NOR gates have high area of cross-section and are seen to be good targets for SET pulse width measurement. Hence, it is critical to analyze the change in pulse width for a multi-

stage 3 input NOR chain. The schematic representation of the 3 input NOR chain is shown in Fig. 2.16. 3 input NOR gates of multiple drive strengths are analyzed and the ones that yield minimum area and result in least pulse width change are chosen for optimization. The input to the 3 input NOR chain is a SET with pulse width of 205ps. Two inputs of each of the 3 input NOR gate are tied to ground and the third input is tied to the output of the previous stage. In this configuration, each stage behaves like a buffer stage.

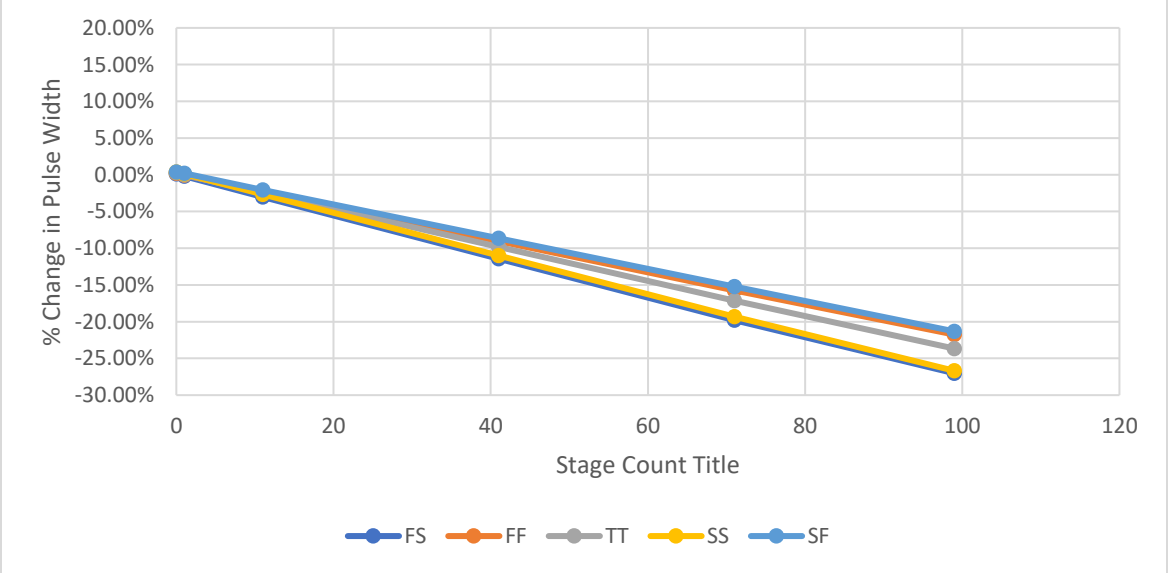


Fig. 2.17 Change in Pulse Width of 3 Input NOR Chain with 100 Stages using Unmodified Cells.

The schematic shown in Fig. 2.16 comprises of a 3 input NOR chain having a stage depth of 100. It consists of 3 input NOR gates, NOR3_X1M_A9TR, of single drive strength using 32nm SOI process NOR3_X1M_A9TR. For simulation purposes, we have chosen an input pulse width of 205ps and have calibrated the output pulse width for various P/N widths. The simulation results show a worst-case pulse with change of -27.02% at the FS corner, i.e. 554fs degradation of pulse width per stage. The pulse width change is greater than -21.32% for any of the 5 analysis RC corners: FS, SS, TT, FF, SF. Fig. 2.17 shows

the stage wise degradation in pulse width for each corner and Table 2-5 shows the percentage change of pulse width captured at intermediate stages as the SET propagates.

Corner	Stage<0>	Stage<1>	Stage<11>	Stage<41>	Stage<71>	Stage<99>
FS	0.10%	-0.20%	-3.02%	-11.41%	-19.80%	-27.02%
FF	0.20%	-0.05%	-2.29%	-9.02%	-15.76%	-21.76%
TT	0.29%	0.00%	-2.44%	-9.80%	-17.12%	-23.66%
SS	0.39%	0.10%	-2.68%	-10.98%	-19.32%	-26.68%
SF	0.39%	0.20%	-2.05%	-8.63%	-15.22%	-21.32%

Table 2-5 Stage wise Percentage Change in Pulse Width for 3 Input NOR Chain.

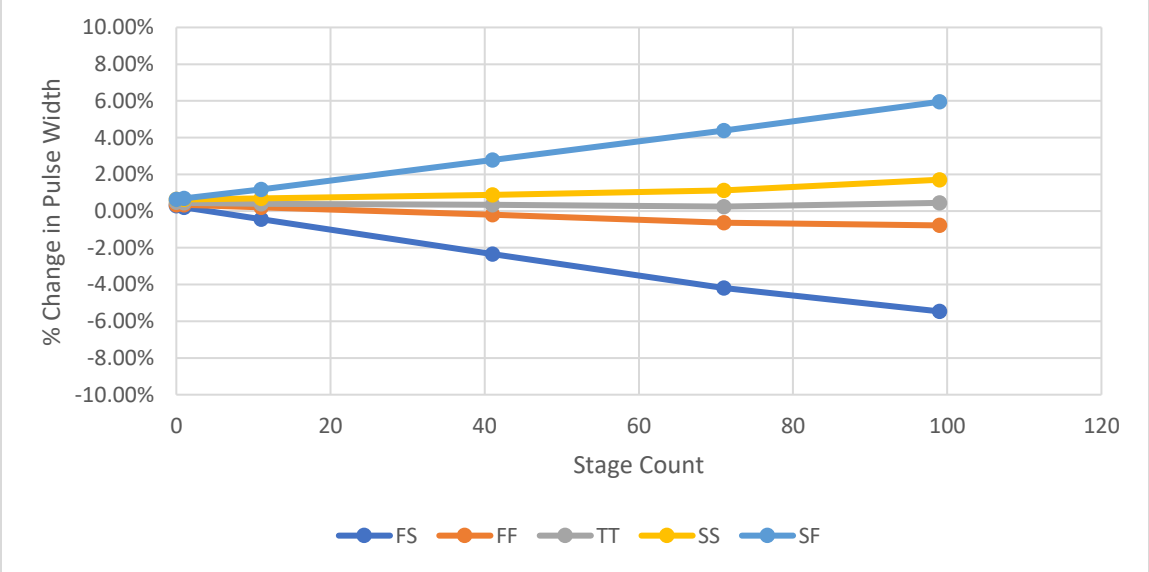


Fig. 2.18 Change in Pulse Width of 3 input NOR Chain With 100 Stages Using Skewed Gates.

The optimized version of the 3 input NOR chain comprise of skewed gates. From the previous simulation results, it was observed that the rise transition was faster compared to the fall transition for each stage. Reduction in PMOS width for the driver in each stage helped get better pulse width results at the output of a 100 stage 3 input NOR chain. But, this was not enough as the worst-case degradation post simulation remained at -10% at the FS corner. An experiment with reduced NMOS size resulted in the best pulse width change

results for a multi-stage 3 input NOR chain. The NMOS width of the receiver gate for each stage was reduced from 198nm to 178nm, which results in sharper fall times and reduced pulse width change. The simulation results with the skewed gates in each stage show a worst-case pulse width change of +5.95% at the SF corner. The pulse width change ranged

Corner	Stage<0>	Stage<1>	Stage<11>	Stage<41>	Stage<71>	Stage<99>
FS	0.29%	0.20%	-0.44%	-2.34%	-4.20%	-5.46%
FF	0.34%	0.34%	0.20%	-0.20%	-0.63%	-0.78%
TT	0.49%	0.44%	0.39%	0.34%	0.24%	0.44%
SS	0.63%	0.63%	0.68%	0.88%	1.12%	1.71%
SF	0.63%	0.68%	1.17%	2.78%	4.39%	5.95%

Table 2-6 Stage Wise Percentage Change in Pulse Width For 3 Input NOR Chain for All Corners

from -5.46% at the FS corner to +5.95% in the SF corner, with 0.44% pulse width change at the TT corner. The percentage change in pulse width for intermediate stages in a 3 input NOR chain for all RC corners, is reported in Table 2-6.

The custom layout design is done for the 3 input NOR chain that uses NMOS skewed receiver gates for each of the 100 stages. The layout is shown in Fig. 2.19. The layout is done using the automated placement and routing utility, Modgen within Virtuoso Layout Suite. The layout design is done such that each stage sees a matched capacitive load. The connection between each of the 2 consecutive stages use similar routing style and metal layers. This helps maintain balanced load capacitance and hence does not degrade the pulse width from one stage to the other. Based on the post layout results from the 2 input NOR chain, the 3 input NOR chain is designed having a single row with 100 stages instead of multiple rows, each of which contains a driver and a skewed receiver 3 input NOR gate.

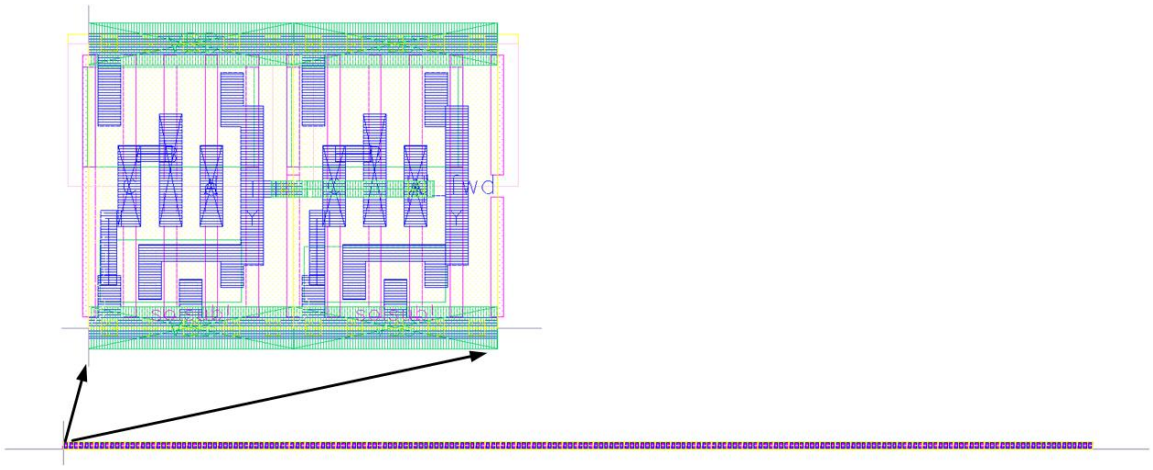


Fig. 2.19 Layout Design of 3 Input NOR Chain With 100 Stages showing a Magnified stage

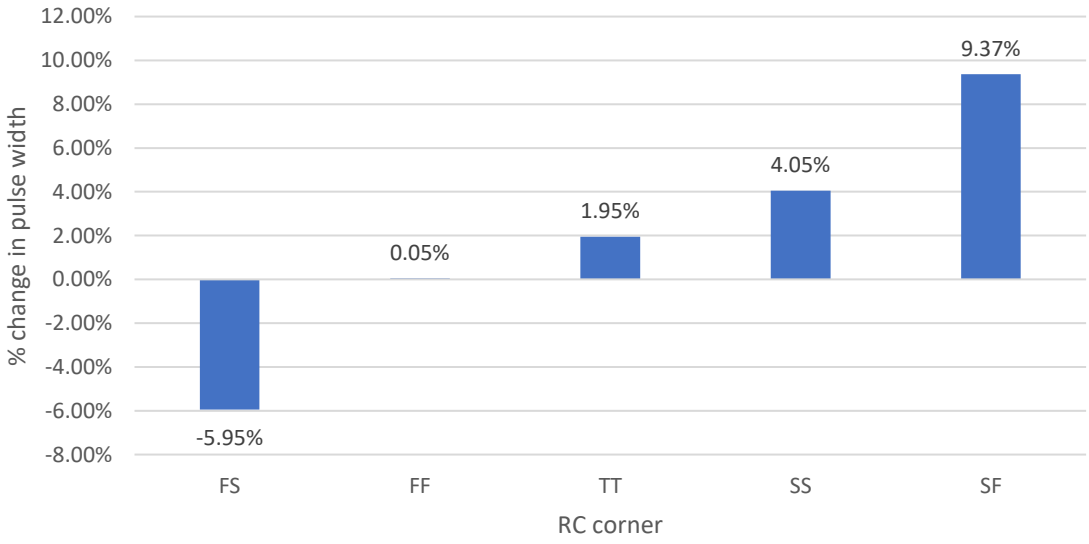


Fig. 2.20 Post Layout Results. Stage Wise Percentage Change in Pulse Width For 3 Input NOR Chain.

The layout is extracted using Calibre PEX and the post layout extracted netlist is simulated to see the post layout pulse width change. The worst-case pulse width change is +9.37% at the SF corner. The pulse width change ranged from -5.95% at the FS corner to

+9.37% in the SF corner, with 1.95% pulse width change at the TT corner. The results are reported in Fig. 2.20.

The next chapter will discuss about the SET measurement structure and its operation in functional and scan mode. The inverter chain with balanced load capacitance is used for propagation of the SET into the SET measurement structure. The SET measurement structure schematic design and operation will be explained in Chapter 3.

CHAPTER 3. SET DURATION MEASUREMENT TEST STRUCTURE

3.1. Overview

To measure the SET pulse width a digital on-die measurement array is built using the GF 32nm partially depleted SOI technology. At lower nodes, the effect of radiation is becoming very significant in the reliable operation of the integrated circuits. The failure rate created due to the SET is expected to dominate at latest technologies [Benedetto06] [Maharrey13]. In a radiation environment, a particle strike causes charge deposition on a sensitive node that creates a transient pulse. If the transient thus created propagates through the logic gates and gets captured by a sequential cell, it may lead to functional failure. For instance, if a particle strike hits a sensitive reset node in the chip, it may induce an undesired reset signal (a SET). The SET could potentially turn off the undergoing operation of the chip thereby effecting not only the functionality but also the reliability of the data. It is critical to mitigate the SET before it could be captured by a sequential cell in the path. SET pulse width and cross-section are critical parameters for consideration in building a radiation hardened circuit design [Maharrey13]. Hence, it is important to build a test structure that can reliably calibrate the SET pulse width. This information can be used to build radiation hardened circuits that help mitigate majority of the SET's in the target pulse width range. The measurement circuit is based on the principle that within an inverter or buffer chain, the propagated SET will decide the logic level of the output of each stage. This is directly impacted by the pulse width of the SET. Such a measurement test circuit was first introduced by Narasimham et al. [Narasimham06]. Many other previous works have built a similar test structure on higher technology nodes [Narasimham07] [Grouker08] [Makino09].

One of the primary structures is designed to measure SET duration. It is basically an on-die oscilloscope that can measure pulse widths. The precision is tuned by varying the skew between the clock edges that reach each stage of the test structure. The pulses are made closer by buffering the incoming pulse at each stage. This provides an effective capture time (width) for each stage of,

$t_{EFF} = (t_{CLKn} - t_{CLKn-1}) - d_{BUFFER}$,

where d_{BUFFER} is the delay through the buffer. The SET target gates are a chain of combinational gates (easiest layout but prone to pulse shortening or broadening) or trees (shorter so less pulse duration distortion, but difficult layout), that will be discussed in Chapter 4.

3.2. Circuit Design

The on-die SET duration measurement test structure is a chain of self-triggering SET capture and scan circuitry. The SET pulse propagates through the chain of inverters. This inverter chain is carefully designed to have balanced capacitive load such that the SET is reliably captured by the capture flip flops. Each stage of the SET DFF chain comprise of a pair of inverters and buffer load to balance the capacitive load for each stage. The clock signals for each stage are skewed to allow reasonable capture time based on the data path delay for each stage. The estimated data path delay for each stage is 9.337ps as shown in Fig. 3.1, which is the delay of the pair of inverter balanced using high drive strength load buffers. The timing of each stage is critical to reliably capture the logic level of the propagated SET pulse. The stage delay is a factor of the input transition time and output load capacitance. As the SET propagates through the chain of balanced inverters, any change in the output slew (input slew for following stage), will change the stage delay.

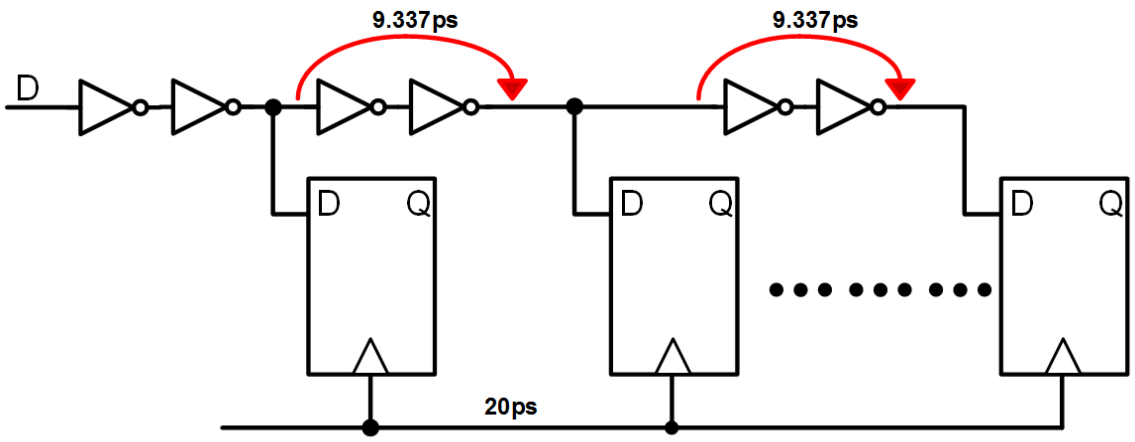


Figure – Delay across FF chain degrades the input pulse. Clock Skew is 20ps

Fig. 3.1 Delay Across Successive FF's in the SET Measurement Circuit.

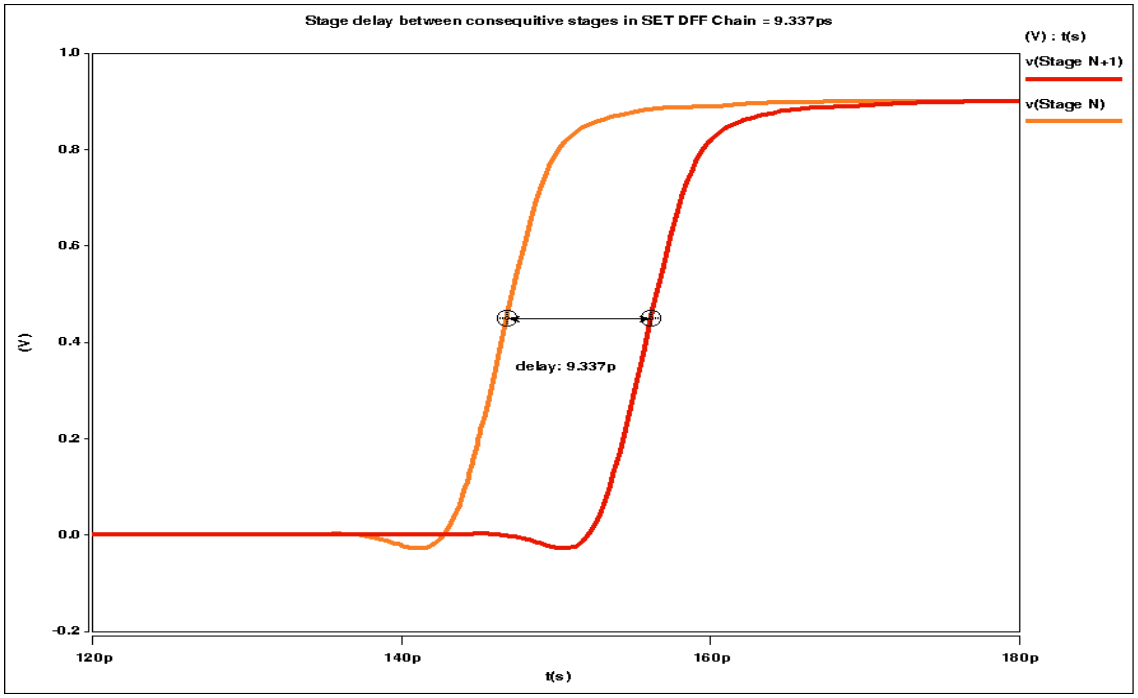


Fig. 3.2 Single stage delay for SET propagation = 9.337ps.

The SET DFF chain is an instantiation of 100 stages, each of which contains SET propagation inverter pairs with load balancing buffers, clock input, scan input, and a unique

start and stop mechanism to trigger the scan mode. The schematic representation of a stage is shown in Fig. 3.3 Single Stage Schematic of the SET DFF Chain.. The inverter pair comprise of INV_X4M_A9TR driving INV_X4B_A9TR balanced for equal rise transition time and fall transition time with BUF_X11B_A9TR. The scan path is buffered with BUF_X0P7M_A9TR to avoid any hold time violations in the scan mode of operation. This

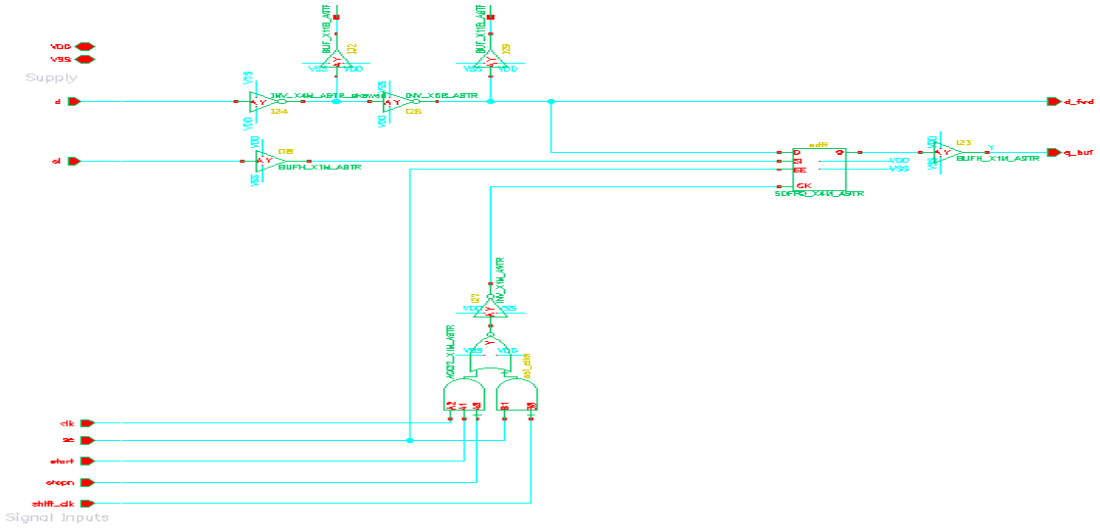


Fig. 3.3 Single Stage Schematic of the SET DFF Chain.

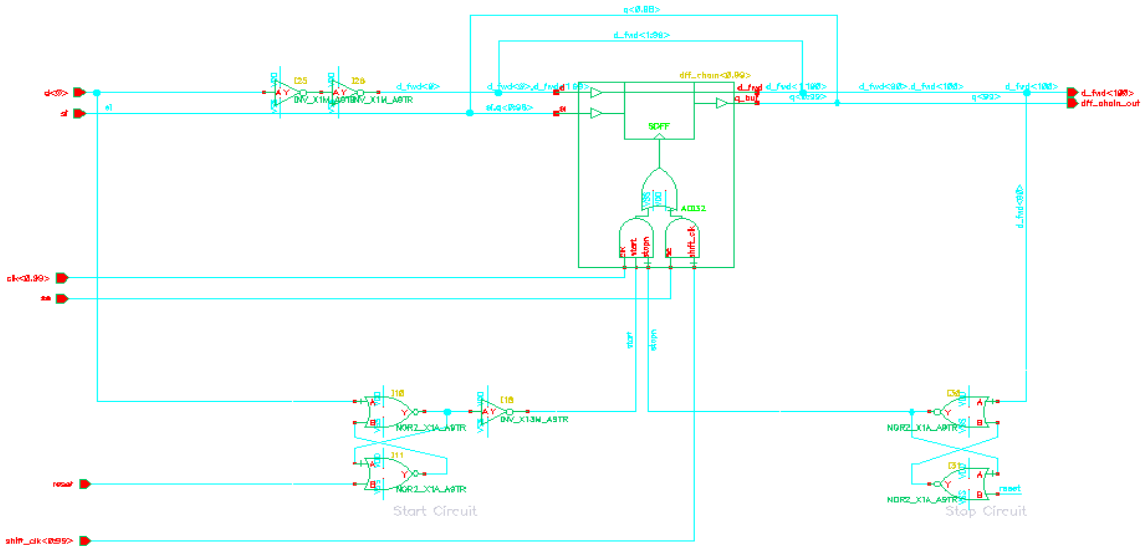


Fig. 3.4 SET Measurement Test Structure Schematic Representation.

is essential as correct operation of the scan mode being critical to have a high resolution of the estimated pulse width. The output Q of the SDFF_X4M_A9TR of each stage is buffered and connected to the scan input of the flip flop in the subsequent stage. The scan mode is enabled depending on the state of the start and stopn signals, that are inputs to each stage of the SET DFF chain. The start and stopn signals are input to the NAND2_X1M_A9TR gate, the output of which is connected to the scan enable pin of the flip flop in each stage. At the top level, the start and stop signals are generated by the output of the NOR2_X1M_A9TR gates. The input to the 2 input NOR gate are the active low reset signal and the primary input d<0> of the circuit. The stopn signal is driven by the 2 input NOR gate having an active low reset signal and the output of the 90^{th} pair of inverters in the data path. The unique start and stop mechanism ensures minimum external intervention and reliable capture and scan out of the SET.

3.3. Operation

The top-level schematic of the SET measurement structure is shown in Fig. 3.4. The SET DFF duration measurement structure works in 2 modes, functional and scan mode. Initially, the scan mode is turned on by using the stop circuit and the scan input ‘si’ is driven low. The scan clock, nominally 50 MHz is applied to initialize all FFs to a logic low state. We anticipate inverting low going SETs for maximum circuit re-use. To maintain low power consumption despite high clock rates (we anticipate the structure to have 40,000 FFs) the stages are clock-gated and thus inert when not in use.

3.3.1. Functional Mode

The functional mode of operation begins when an input SET reaches the primary input d<0>. The logic 1 level at d<0> triggers the start circuit and turns off the scan mode for each stage. This allows the input SET to be captured inside the sequential logic in each stage. Each stage receives clock edge that is skewed by 20ps with respect to the previous stage. This allows a reliable capture time and considers the data path inverter delay along with the setup time of each flip flop. In the functional mode, it is made sure that each stage receives only a single clock edge to capture the propagated SET. This is done to avoid any overwriting of the stored state before the scan mode is turned on. The timing of the clock edges and the data path inverter pair delay is critical, as any negative slack would either corrupt or miss the data to be captured. Also, the data path inverter pair must be balanced such that the pulse width across each stage remains constant. If the pulse undergoes pulse broadening or shortening it will be captured by either greater or lesser number of stages, thereby effecting the accuracy of the estimated SET pulse width. Any pulse width change during the SET propagation would trigger the stop circuit either earlier or later, which would lead to untimely scan out of the captured data. Moreover, there is a possibility of a truncated pulse due to its capture at the front or rear of the chain. These pulses will be counted towards the cross-section, but their length is not known, so they should not contribute to the pulse length statistics.

3.3.2. Scan Mode

As the propagated SET reaches the 90^{th} stage, a logic 1 level triggers the stop circuit. The stop circuit turns off the functional mode and turns on the scan mode. The time required for the stop signal to turn on the scan mode is carefully balanced with the time the

propagated SET reaches the d_fwd<99>. This is a critical timing requirement as it would keep the circuit operating in either of the functional or the scan mode. If the trigger to the stop circuit is delayed to function based on the last stage of the SET DFF chain, it would keep the circuit out of both the modes of operation and would be considered as a dead time.

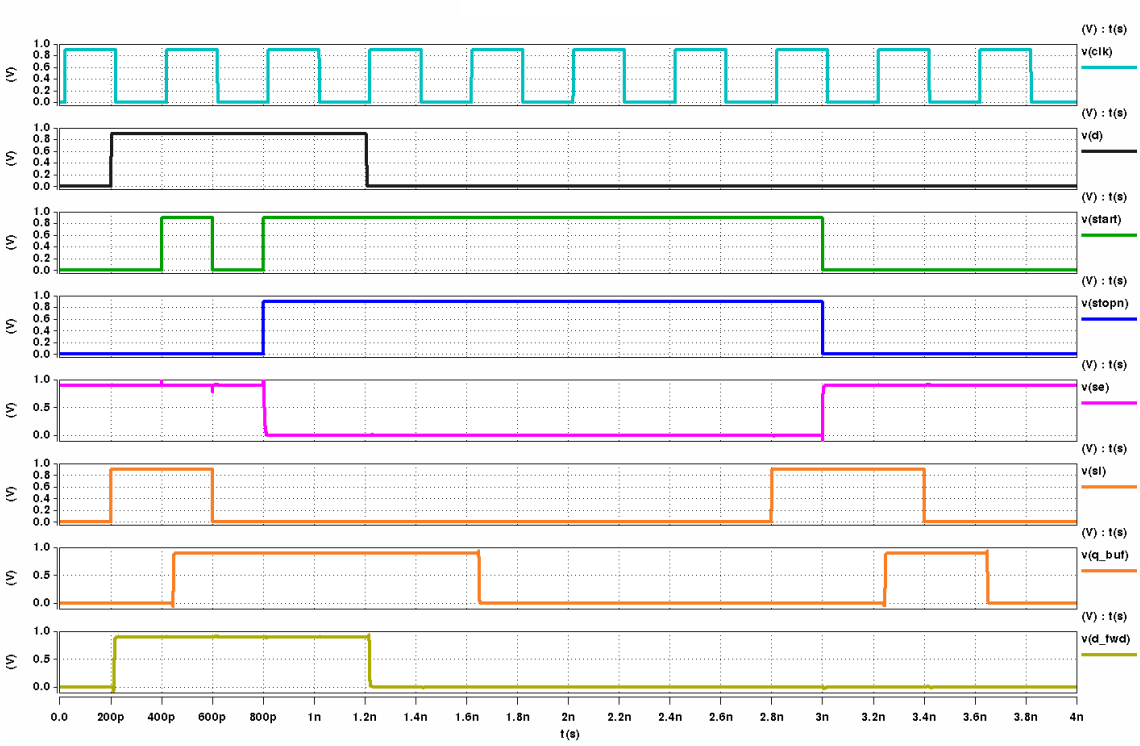


Fig. 3.5 Basic Function of Functional and Scan Mode for Single Stage

In the scan mode, high frequency clock edges reach the sink pins of each stage as shown in Fig. 3.6. Fast clocks are applied to the row to capture the SET duration as a string of 1's in the FF row (nominally 100 to 200 FFs). However, the clock wave-front is unknown since the SETs are asynchronous. Thus, the SET can be captured anywhere in the chain. Fast clock edges allow quick scan out of the captured data after which the circuit is made available to work in the functional mode again. To make the SET pulse width measurement accurate the scan input of the circuit is given logic 0. This makes it

convenient to measure the stream of 0's and 1's at the output in scan mode, with 1's indicating the captured SET pulse. A typical output of the scan mode is a stream of 0's and 1's like 000001111111110000000. The basic functionality of a single stage in both functional and scan mode is shown in Fig. 3.5 . For a very long SET DFF chain with 40,000 stages arranged in rows of 'n' number of stages, the circuit can be modified to maximize the beam time usage. Each row can be made independent such that the test can be capturing SETs in rows that are not being scanned out. This enables optimum usage of the expensive beam time. The confirmation of operation of one such row having 100 stages is shown in Fig. 3.6 and Fig. 3.7

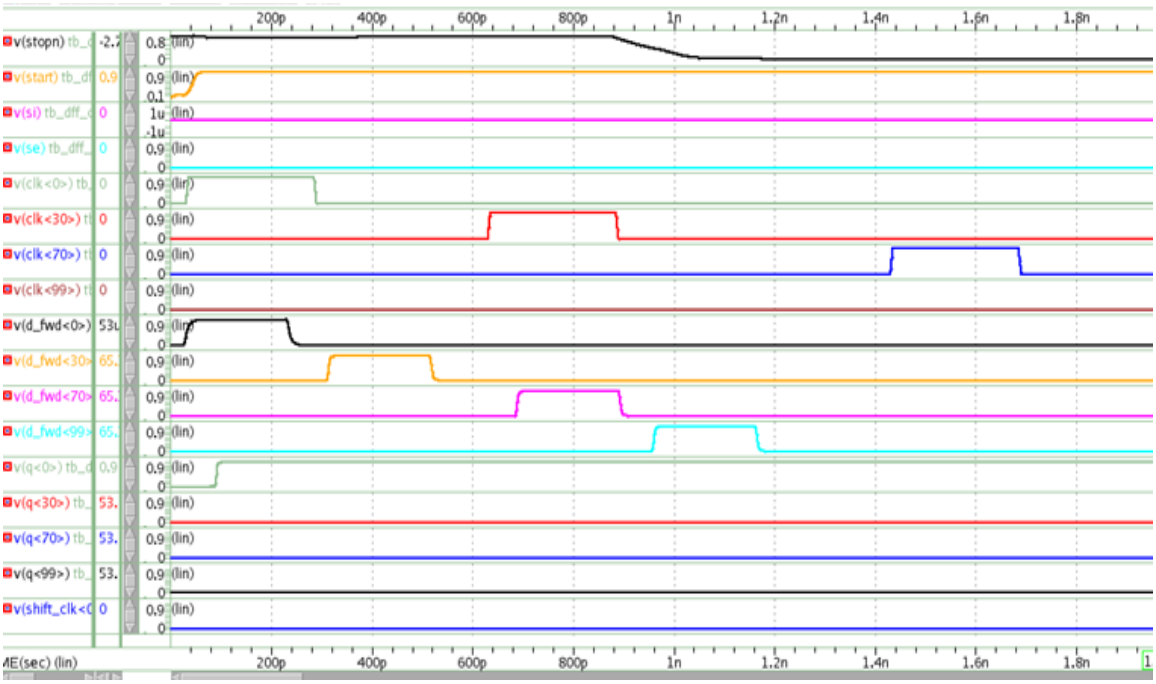


Fig. 3.6 Clocking and Confirmation of Operation of SET Measurement Circuit (Functional Mode).

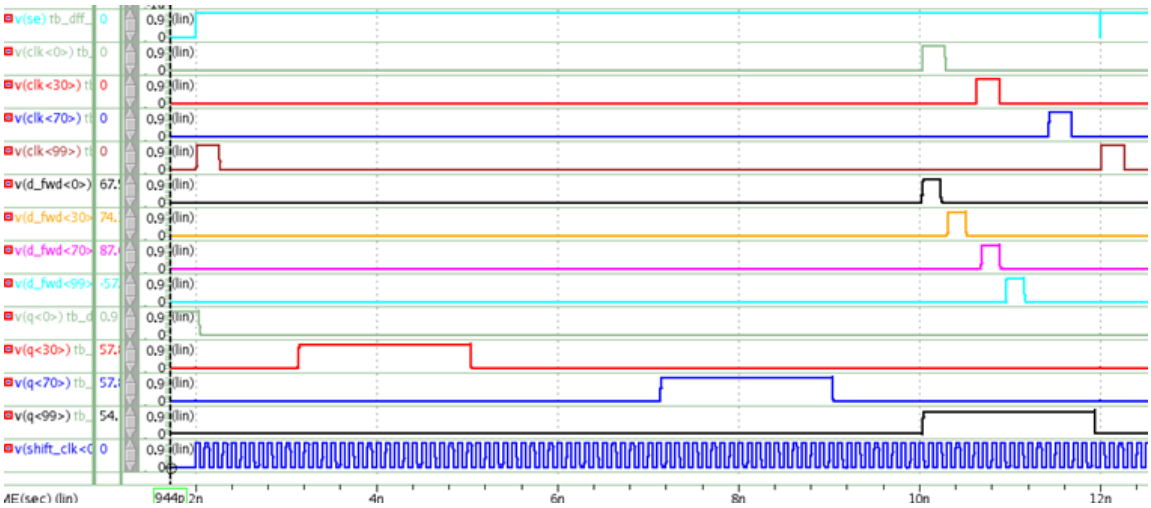


Fig. 3.7 Clocking and Confirmation of Operation of SET Measurement Circuit (Scan Mode).

3.4. Simulation Results

The confirmation of operation for each stage is shown in Fig. 3.6 and Fig. 3.7. The illustrated simulation shows the basic operation of a single stage in functional and scan mode. In the functional mode, the input at d gets captured at by the FF and is reflected at the output ‘q_buf’ at the subsequent rising edge of the clock. The scan mode is triggered by the start and the ‘stopn’ signal. The scan mode is turned on only when both the start and ‘stopn’ signals are on. In the scan mode, the scan input is captured by the FF and is reflected at the output at the following rising clock edge. Fig. 3.6 shows the input clocks and the shift register

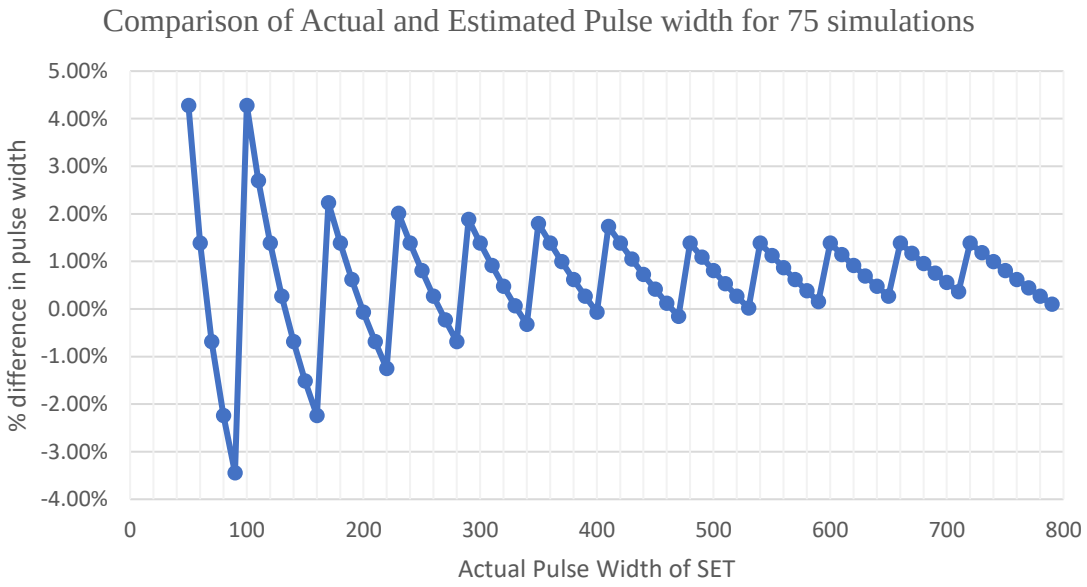


Fig. 3.8 Comparison of Actual and Estimated Pulse Width For 75 Simulations From 50ps to 790ps Pulse Width

function of the SET DFF chain. For the initial analysis, we start with a 200ps wide input pulse. The pulse is captured by FFs as shown in Fig. 3.6.

Since the pulse is extended in time (neglecting the pulse broadening or shortening) by approximately 9.333ps per stage as shown in Fig. 3.1, a 200ps pulse is captured by 200/9.33 ~ 22 FF's (+- 1 FF if pulse width broadening and shortening are considered). For the SET DFF duration measurement structure, we analyzed the estimated pulse by measuring 1's in the scan output stream of 0's and 1's for 75 different pulse widths. The pulse width chosen for experiments were in the range 50 to 790ps. Such a wide range is chosen as previous works indicate that both the bulk and SOI technologies have a wide distribution of pulse width change. Previous works indicate that at lower nodes, the pulse width extension could be in a nanosecond range [Cavrois07]. Considering the pulse width broadening and shortening, the input pulse width and the captured pulse width were plotted.

It was observed that the estimated pulse width for 75 simulations vary between -4% to +5% of the actual pulse width. The results of each simulation and its corresponding estimated pulse width is reported in Fig. 3.8.

CHAPTER 4. SET CAPTURE TEST STRUCTURE

4.1. Overview

In this chapter, we focus on building a SET capture test structure. This test structure connects to the SET measurement test structure which measures its pulse width. A SET capture structure is required for the SET measurement test structure to operate reliably. The SET capture structure is the one that is exposed to the heavy ion beam test during radiation, and carries the SET pulse to the measurement circuit. In previous works, the SET target circuit has been ubiquitously used for the generation and propagation of a SET. These structures are usually created using a chain of inverters [Bala08]. Some researches indicate that the total target area of the SET target circuit optimum enough to obtain accurate statistics during broad beam testing equals the size of 24000 minimally sized inverters[Loveless12]. Whereas, for an inverter chain, in a radiation environment, individual ion strikes on the inverters propagate to the measurement circuit. Another type of SET capture test circuit previously published contains multiple stages of parallelly connected inverters followed by the 2-input NOR or NAND gate [Gadlage10], termed as the P-hit and the N-hit circuit. In both the P-hit and N-hit circuit designed using 65 CMOS technology, the problem of SET creation by a single ion strike was resolved due to logic masking. Logic masking is a technique of restricting any change in output by setting one of the inputs of a logic gate as fixed. This technique only allows the generation and propagation of a SET if it hit the NOR or NAND gate, as any perturbation at the output of the parallel inverters due to an ion strike was logically masked. But, this technique leaves most of the circuit unusable as a SET target.

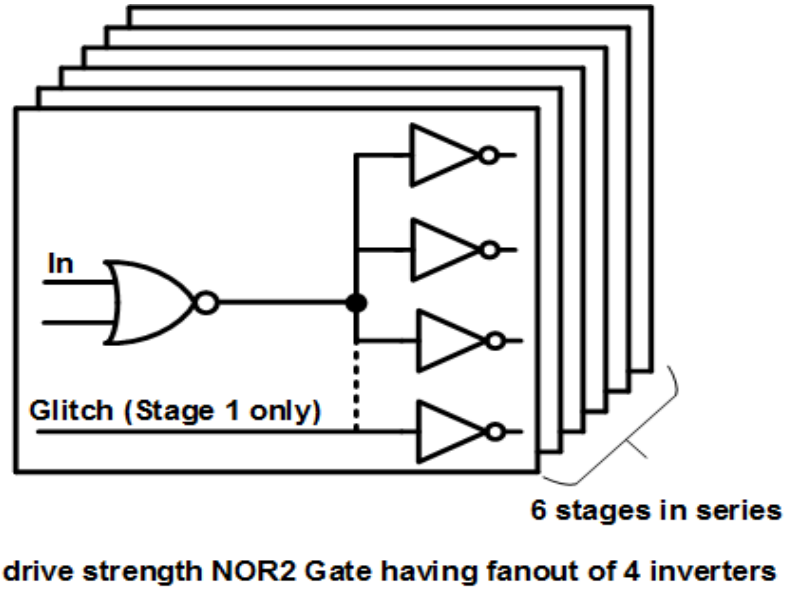


Fig. 4.1 SET Capture Test Structure Schematic, With Glitch Signal Modeled for Simulation

4.2. Circuit Design

We built a SET capture test circuit using a 2 input NOR gate followed by 4 inverters in parallel called a single stage as shown in Fig. 4.1. 6 such stages when connected in series are termed as a unit cell of the SET capture circuit. The 2 input NOR gate is chosen to have high drive strength (NOR2_X8B_A9TR) to assist in lowering the pulse width change as the SET propagates. The inverters used (INV_X0P5M_A9TR) are of minimum size but have skewed PMOS and NMOS size to provide least pulse width change during SET propagation. The size of the skewed PMOS = 167nm and the skewed NMOS = 178nm. An input of the 2 input NOR gate is tied to ground such that it operates as an inverting logic. This is necessary as any output logic level of the parallel inverters is propagated in the chain. We use 4 inverters connected in parallel to restrict the propagation of any individual ion strike on any one of the inverters. Any ion strike on any one of the 4 inverters does not

propagate to the subsequent stage as the on devices in each of the other 3 inverters overpower the inverted signal produced by the 4th struck inverter. This scheme works at all 5 process corners on 32nm SOI technology. 3 inverters connected in parallel instead of 4 also works fine, but we use 4 for guard band. This also provides greater symmetry in design the layout of the SET capture test structure. The details of the layout design will be shared in the following sections. (and it provides greater symmetry in the layout).

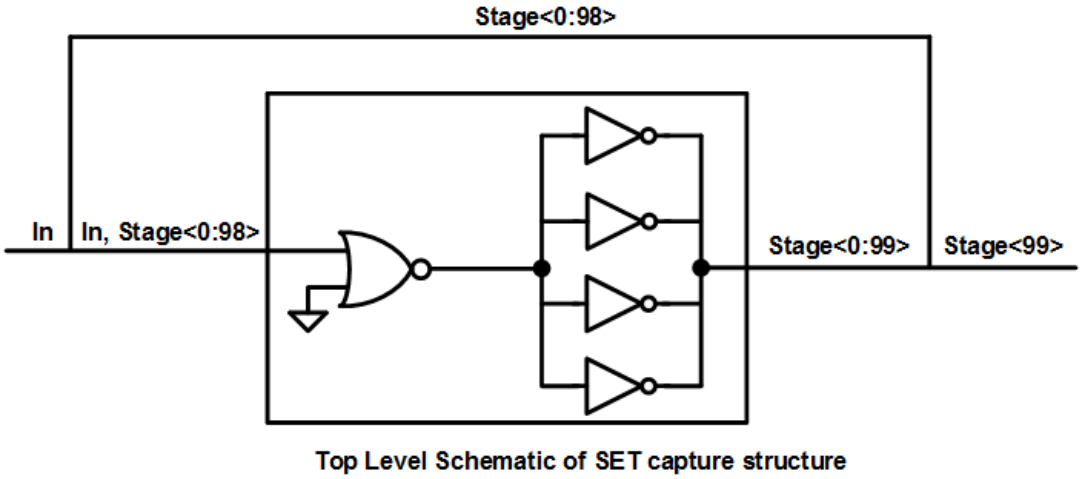


Fig. 4.2 Top Level Schematic of The SET Test Structure With 100 Instantiations of Unit Cell Connected in Series

4.3. Operation

The circuit operation is straightforward, an input SET pulse propagates through the inverting 2 input NOR gate which has a grounded input. A particle strike at the NOR gate generates a SET that is inverted and propagated. The SET reaches 4 inverters connected in parallel to the output of the NOR gate. In normal operation, without any individual ion strike on any inverter, either all 4 PMOS or all 4 NMOS transistors operate in linear mode. The output of all the 4 inverters are tied together and connected to the next set of NOR and inverter logic. This combinational logic path inverts and propagates the incoming SET

pulse and finally connected to the input of the SET measurement circuit for SET pulse width measurement. In our design, we use 100-unit cell instances connected in series for SET capture and propagation. The top-level schematic is shown in Fig. 4.2. The output of each unit cell instance is connected directly to the input of the following unit cell. Each unit cell is carefully balanced to have minimum pulse width change as the SET propagates.

In case any of the 4 parallel connected inverters is hit by an individual ion strike, a glitch could be induced. A glitch signal could be as small as a little change in the voltage (of the order of 10mV) level to as high as effecting the SET to go to the rail (0.9V). A high amplitude glitch could disturb the logic level of the propagating SET or could cause SET pulse width change. Hence, it is important to have a built-in circuit which mitigates this glitch and allows un-perturbed propagation of SET. The 4 parallelly connected inverters help mitigate any glitch induced due to individual ion strike. In case of a high amplitude glitch on any one of the inverters, the state of the inverter is changed. For example, if the SET propagating through the inverter is logic level 1, then in normal operation, the NMOS of the inverter is in linear mode and the output is a logic 0. In case of a glitch induced on the inverter, the output logic 0 signal is effected and the inverter yields a logic 1. In this case, the 3 other inverters which yield a logic 0 output dominate the glitch effected inverter, and hence the output node is maintained at logic 1. This technique is helps the reliable SET propagation and mitigates any individual ion strike that may cause a glitch. A high amplitude, long duration glitch is replicated in simulation experiments and the capture circuit design is analyzed for robustness.

4.4. Schematic Simulation Results

The confirmation of operation is shown in Fig. 4.3. In this simulation, a high amplitude glitch signal with varied durations is analyzed against the SET capture circuit design. The glitch signal is a regular input signal with the impact of a high amplitude individual ion strike. The amplitude and the duration of the glitch signal is swept and its impact on the output of each stage of the capture circuit is analyzed. The capture circuit is analyzed for both rising and falling glitch signals. This analysis is conducted at TT, SS, FF, SF and FS corners. At all corners, it is seen that the circuit is robust enough to mitigate a glitch with a duration ranging from 10ps to 50ps. Noticeably, the input SET pulse width is changed when measured at the output of a unit cell. In the presence of the glitch signal, the input pulse width of 205ps changes by a maximum of 1.78% across FS corner and by a minimum of 0.24% across SS corner, at the output of the six-stage unit cell.

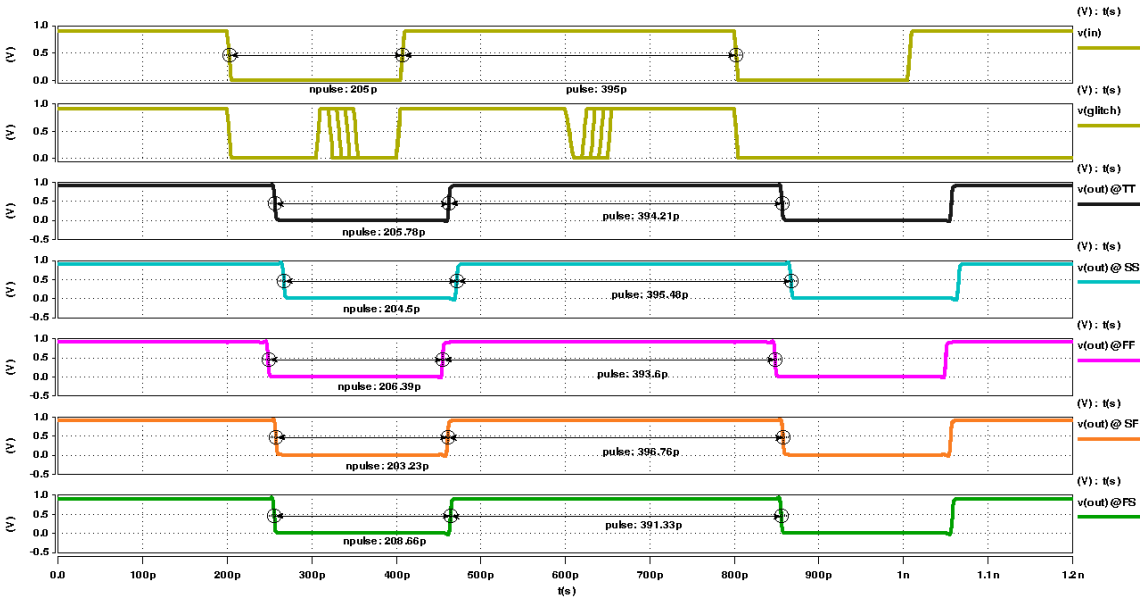


Fig. 4.3 Simulation Results of SET capture circuit Unit Cell, with Glitch Input.

Further, a varying amplitude of glitch signal was also simulated and tested for a single stage of a unit cell across all process corners. The simulation results of a single stage with a 50ps glitch of varying amplitude is shown in Fig. 4.4. As shown a single stage of a unit cell is affected by the impact of a glitch. The effect only remains for the duration the glitch is present on the circuit. Due to 3 overpowering transistors, the 4th struck transistor state is recovered rapidly. As each of the 6 stages in a unit cell is connected in series, the impact of the glitch at the 1st of the 6th stage is completely recovered by the output of the unit cell, as seen through simulation results in Fig. 4.3.

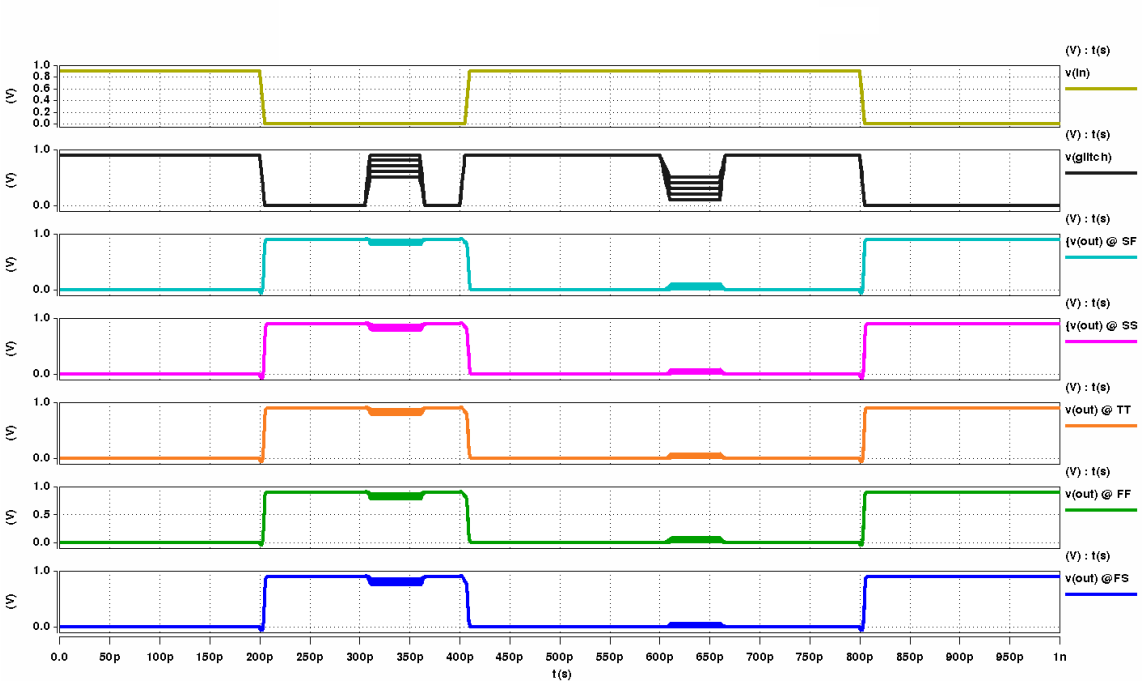


Fig. 4.4 Simulation Results of Single Stage of Unit Cell with The Impact of a Varying Amplitude 50ps Wide Glitch.

4.5. Custom Design

The layout of the unit cell schematic is done using CMOS 32nm SOI IBM PDK. An important consideration in designing the unit cell of the SET capture structure is to avoid an individual ion strike on 2 or more inverters among the set of 4 parallel inverters. This is done by placing the cells such that no two inverters in the same set are close to each other. The floorplan used as premise to place the standard cells is shown in Fig. 4.5. As illustrated in the Fig. 4.5, the N* and I* are the NOR gates and inverters respectively. "I6_1" indicate the 1st inverter in the 6th stage inside a single unit cell of the SET capture circuit. As is illustrated, any two inverters from the same stage are kept at least 1 standard cell apart. This placement technique is particularly useful in avoiding multiple upset inverters from the same set within a stage.

I6_1	I5_1	N1	I5_2	I3_3
I3_4	I4_1	N2	I4_2	I6_3
I5_4	I1_1	N3	I1_2	I2_3
I2_4	I6_1	N4	I6_2	I4_3
I1_4	I3_1	N5	I3_2	I1_3
I4_4	I2_1	N6	I2_2	I5_3

I* - Inverter

N* - NOR2 Gate

Single Stage SET Capture Structure Floorplan

Fig. 4.5 Single Stage SET Capture Structure Floorplan.

The layout is carefully done to match capacitive load due to routing. The layout of the unit cell is shown in Fig. 4.6. The dimensions of the layout for the unit cell are 5.4u by 3.77u. The layout follows the floorplan and is shown in Fig. 4.6. Special consideration is

taken to match the capacitances of the corresponding nets in each set such that the pulse width of the input pulse is affected equally across all the six stages of the unit cell across all critical process corners.

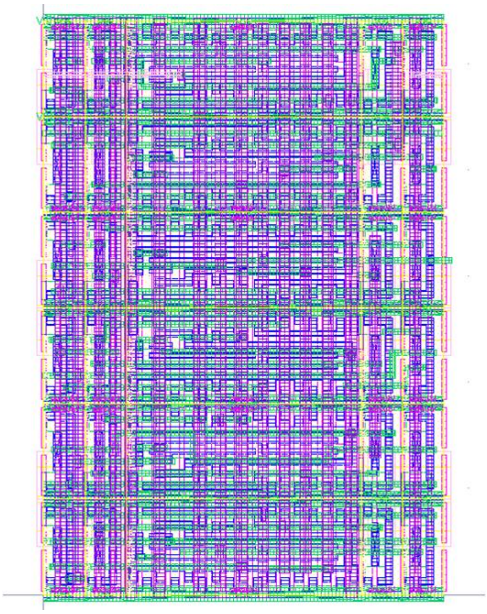


Fig. 4.6 Layout of SET Capture Circuit Unit Cell.

The top level of the SET capture test structure contains 100 instantiations of the unit cell connected in series. The layout of the top level contains the unit cells placed in a grid with 10 x 10 instantiations of the block shown in Fig. 4.7. The dimensions of the top level are 37.7 μm * 54 μm. The ability to match the delays in post-layout is clearly demonstrated, so pulses will be accurately measured across process corners.

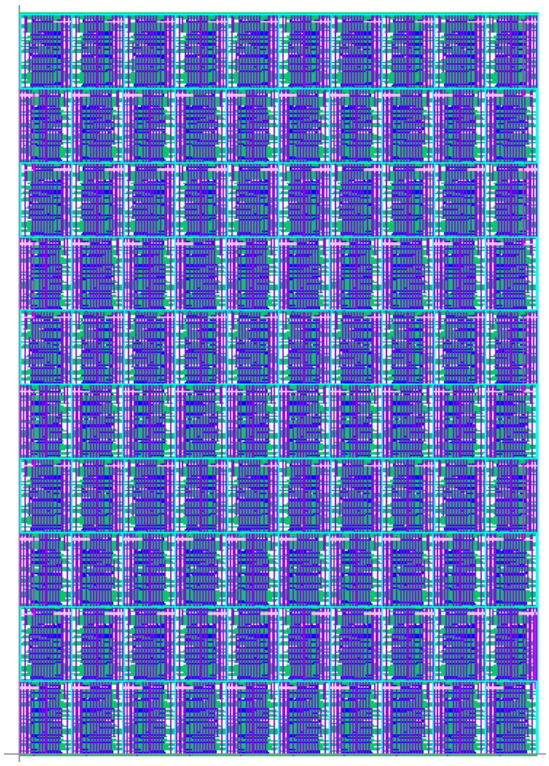


Fig. 4.7 Top level layout of the SET Capture Circuit With 100 instantiations (placed in 10x10 grid).

4.6. Post Layout Simulation Results

The post layout simulations depict that the pulse width change ranges from maximum of +2.6% across SS corner and a minimum of +0.46% across FS corner. It is also observed that the amplitude of the glitch induced due to the impact of an individual ion strike is degraded as the pulse traverses through the following stages. The results of the post layout simulation and waveforms of output pulse captured for each process corner in Fig. 4.8.

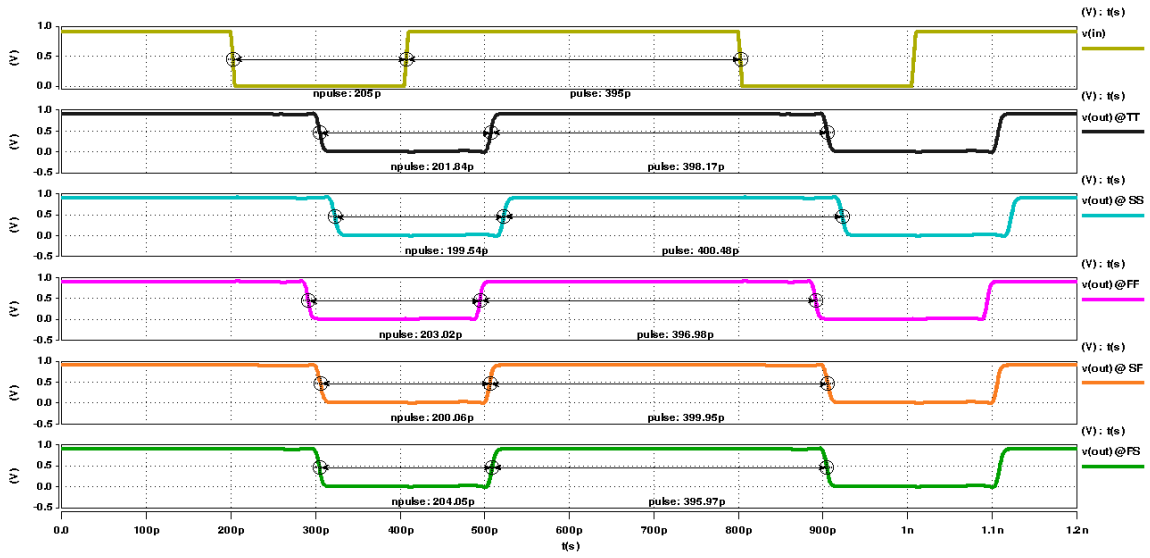


Fig. 4.8 Post Layout Simulation Results of Unit Cell Showing Pulse Width Change.

CHAPTER 5. SUMMARY

The SET measurement test circuit is confirmed to work as expected. The test circuit yields a high resolution of 10ps or +-4% of the actual pulse width, in simulation. As explained, the requirement of maintaining the pulse width during SET propagation is met using carefully skewed gates. The use of skewed gates instead of the PDK provided standard cells is found to be helpful in balancing capacitive load and reducing pulse width change across all stages of the circuit. This technique is qualified by designing a one, two and three input combinational gate chain.

The skewed gates are particularly helpful in combinational gates that show traction in the same direction across process corners. In the experiments conducted it is observed that few combinational gates show diverging nature of pulse width change across process corners. One such example is illustrated in Fig. 5.1. As shown, the pulse width change across corner does not either only increase or decrease, instead it diverges.

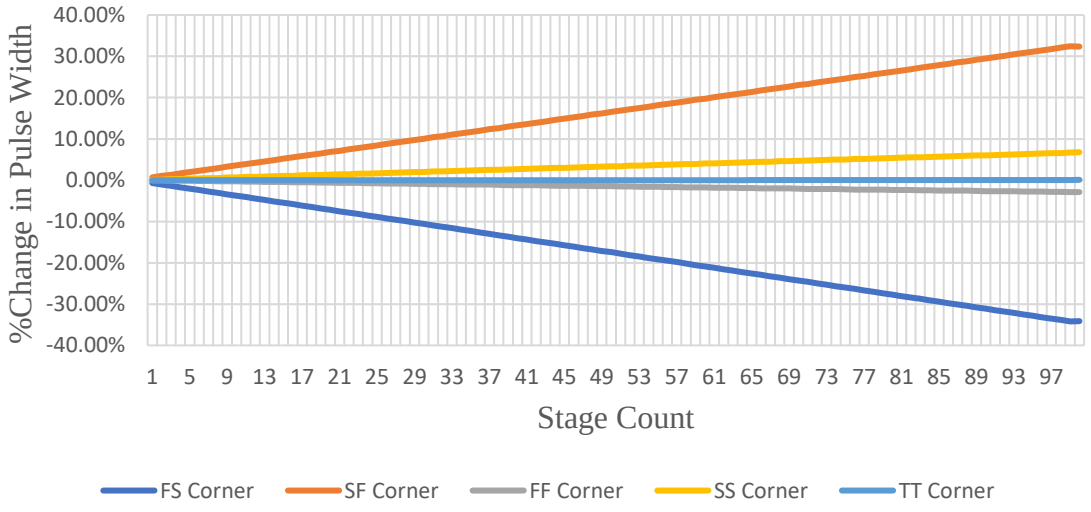


Fig. 5.1 Change in Pulse Width of Inverter Chain With 100 Stages Showing Diverging Trend Across Corners

Any change in the width of the PMOS and NMOS devices of the combinational gate would fix one corner but worsen the other corner. In such a scenario, using skewed gates do not help attain minimum pulse width. Therefore, it is necessary to find a combination of cells that yield similar trends (either increase or decrease) in pulse width change. Once such a combination is found out, then the limiting factor in skewing the gate is the permissible design rules. The PMOS and NMOS device shrinking is limited by the allowed minimum width.

After finding a combination of standard cells that depict similar trends in pulse width change across corners, the combinational gate chain needs to be simulated for various PMOS and NMOS widths. This can result into a huge number of simulations before converging to the combination which yields the least pulse width change. For results reported in Chapter 2, the PMOS and NMOS sizes are carefully analyzed in each simulation such that they yield a break-even point. A break-even point is a unique combination of PMOS and NMOS sizes that for a combination of standard cells that yield the least pulse width change across process corners. A detailed example of such simulation, is depicted in Fig. 5.2 .

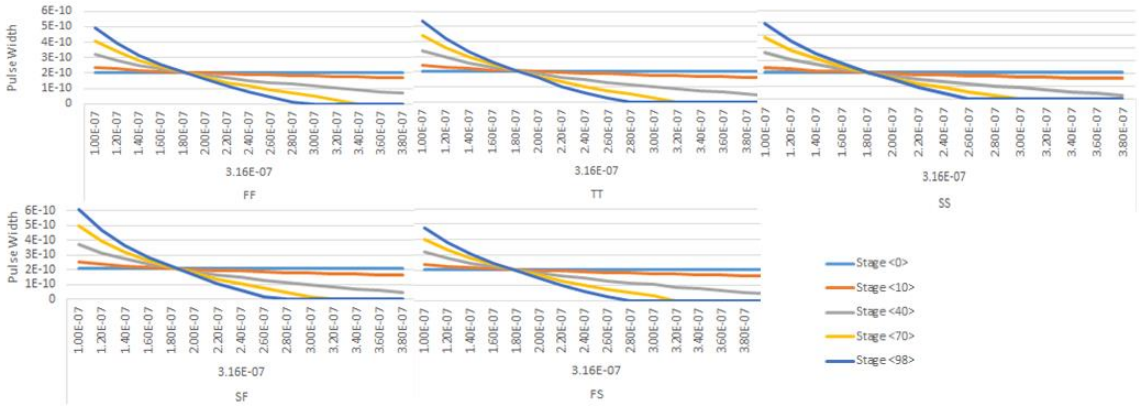


Fig. 5.2 3 *Input NOR Chain Simulation Result for PMOS width 316nm and NMOS Width*

Sweep

In this case, a 3 input NOR chain is simulated and the break-even point is observed at PMOS 316nm and NMOS 180nm. Using this configuration, it is seen that the 3 input NOR chain yields the least pulse width change.

This technique is used in building the Inverter Chain, two and three input NOR chain, SET capture test structure and SET measurement structure. In all cases, using skewed gates instead of the foundry provided standard cells has shown significant improvement in pulse width change. Based on the analysis of the test structures, using skewed gates to avoid any pulse width change is inevitable.

The SET measurement test structure is shown to function reliably for an input pulse width range of 50-790ps. The lower limit is constrained by the setup time and hold time required to capture the data reliably by the flip flop. The upper limit is constrained by the depth of the SET DFF chain. In this analysis, a SET DFF chain with 100 depths was used. It is observed that the measured pulse width is from -4% to +5% or within 10ps of the actual input pulse width. The simulation is performed by controlling the start and the stopn signals externally using HSPICE test-bench.

Lastly, the SET capture structure is built and proven to reliably work across corners. It is observed that the pulse width degrades by maximum of +2.6% across SS corner and a minimum of +0.46% across FS corner for a unit cell with six identical stages. This percentage change is significantly high even with the use of skewed gates due to the imperfect capacitive load across each stage. The parallelly connected inverters in each stage of the unit cell are of 0.5X drive which makes these cells vulnerable to slight change in PMOS and NMOS sizes. Hence, using low drive standard cells pose serious challenges

in device size optimization for reliable SET pulse propagation. The results of the pulse width change across a unit cell can be improved by using high drive strength inverters connected in parallel with a commensurate cost of increase in overall area.

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