Cu-Silica Based Programmable Metallization Cell: Fabrication, Characterization and Applications

by

Wenhao Chen

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Graduate Supervisory Committee:

Michael Kozicki, Co-Chair
Hugh Barnaby, Co-Chair
Shimeng Yu
Trevor Thornton

ARIZONA STATE UNIVERSITY

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ABSTRACT

The Programmable Metallization Cell (PMC) is a novel solid-state resistive switching technology. It has a simple metal-insulator-metal "MIM" structure with one metal being electrochemically active (Cu) and the other one being inert (Pt or W), an insulating film (silica) acts as solid electrolyte for ion transport is sandwiched between these two electrodes. PMC's resistance can be altered by an external electrical stimulus. The change of resistance is attributed to the formation or dissolution of Cu metal filament(s) within the silica layer which is associated with electrochemical redox reactions and ion transportation. In this dissertation, a comprehensive study of microfabrication method and its impacts on performance of PMC device is demonstrated, gamma-ray total ionizing dose (TID) impacts on device reliability is investigated, and the materials properties of doped/undoped silica switching layers are illuminated by impedance spectroscopy (IS). Due to the inherent CMOS compatibility, Cu-silica PMCs have great potential to be adopted in many emerging technologies, such as non-volatile storage cells and selector cells in ultra-dense 3D crosspoint memories, as well as electronic synapses in brain-inspired neuromorphic computing. Cu-silica PMC device performance for these applications is also assessed in this dissertation.

This dissertation is dedicated to my parents and my girlfriend.

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Tempe, Arizona, USA

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CHAPTER I

INTRODUCTION

I.1. History of Resistive Switching

Many thin dielectric films have been reported to exhibit resistive switching phenomenon, in which the resistance value of such dielectric film can be reversibly altered by external stimulations, such as electrical voltage or current.

The resistive switching phenomenon was firstly discovered in devices consisting binary oxide thin films in the late 1960s [1-4]. Fig. I.1.1 shows the resistive switching characteristics of Au/SiO_2/Al device, which was reported in 1967. In this figure, the applied voltage pulses (V-t) and the corresponding I-V curve are demonstrated in (a) (c) and (b) (d), respectively. As indicated by the I-V curve in Fig. I.1.1b and d, the device can be turned on at a positive voltage and turned off at a voltage with the same polarity but higher amplitude. More specifically, in Fig. I.1.1b, a continuous nonlinear current trace (OA' to A'A) was captured when a continuous voltage ramp-up (zero to a in Fig.I.1.1a) was applied on the device, when a series of discrete voltage pulses (b to j) with increased voltage amplitude was applied on the device, the device resistance was increased step by step which is indicated by the sequential current reduction (B' to B, C' to C etc.) in Fig. I.1.1b. Fig. I.1.1d demonstrates the resistive switching characteristics with a different testing procedure, i.e. the device resistance was gradually decreased first (O to A and B' to B etc.) with a series of discrete voltage pulses (a, b etc. in Fig. I.1.1c) and it then continuously increased with a continuous voltage ramp. At that time, the changing of resistance was explained by the injection (or ejection) of electrons into (or from) the energy states of gold ions which

was assumed to be located in the band-gap of amorphous silica [1]. Since the current decreases at higher voltage, this type of resistive switching was named as voltage-controlled-negative-resistance (VCNR) analog switching.

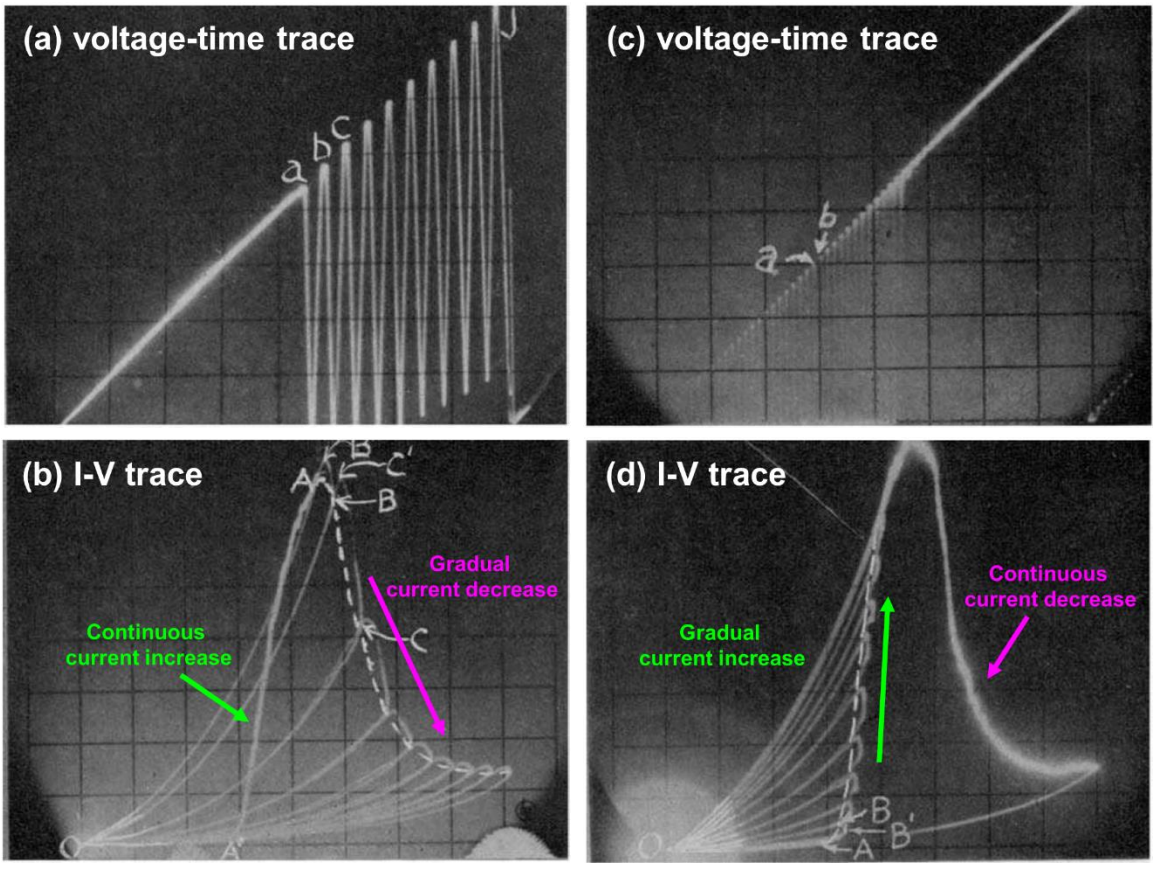

Fig. I.1.1. Resistive switching characteristics in Au-SiO_2-Al device. (a) programming scenario one, (b) continues current increase but gradual current decrease, (c) programming scenario two, (d) gradual current increase but continues current decrease. Reprint from [1].

Several years later, another type of resistive switching was discovered in a Nb-Nb_2O_5-Bi structure [5]. The switching I-V curve is shown in Fig. I.1.2, different from previous one, the "turn-on" and "turn-off" of Nb-Nb_2O_5-Bi device was only achievable by applying voltage with opposite polarity. The high resistance state was attribute to a

Schottky mechanism whereas the mechanism of low resistance state was not identified at that time. This type of resistive switching was name as bistable switching.

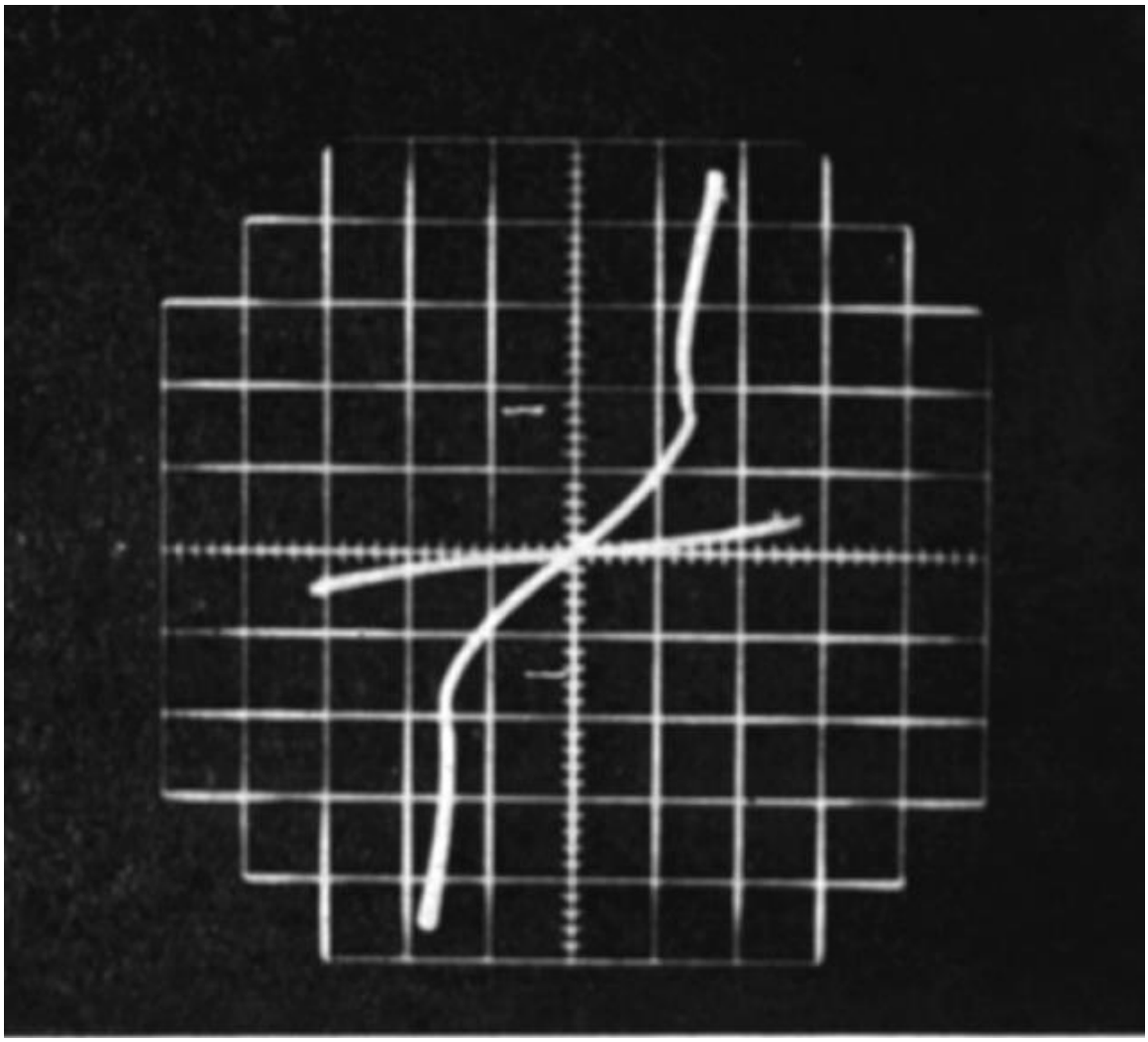

Fig. I.1.2. Bistable resistive switching I-V characteristics in Nb-Nb_2O_5-Bi device. Reprint from [5] 1970, with permission from Elsevier.

Even though repeatable resistive switching performance was reported decades ago [6], the device performance back then was not good enough for practical applications. However, things are changed in recent years due to many significant breakthroughs in

micro/nano-fabrication and thin film deposition, the device performance has been hugely improved and it regained dramatic attention from academy as well as industry [7-9].

I.2. Structure and Filament Model of Resistive Switching Device

Resistive switching device has a simple metal-insulator-metal (MIM) structure in which an insulating thin film is sandwiched between two metal electrodes. In general, the MIM structure can be fabricated into two configurations, i.e. vertical device and lateral device. Fig. I.2.1a is an illustration of vertical device, the top/bottom electrodes are separated by insulating film with a thickness from several nanometers to hundred nanometers. Fig. I.2.1b demonstrates a picture of lateral device, the left/right electrodes are fabricated on top of insulating film with a separation from hundred nanometers to hundred micrometers. To change the device's resistance, a voltage bias is applied on two electrodes with one electrode being electrically biased and the other one being grounded.

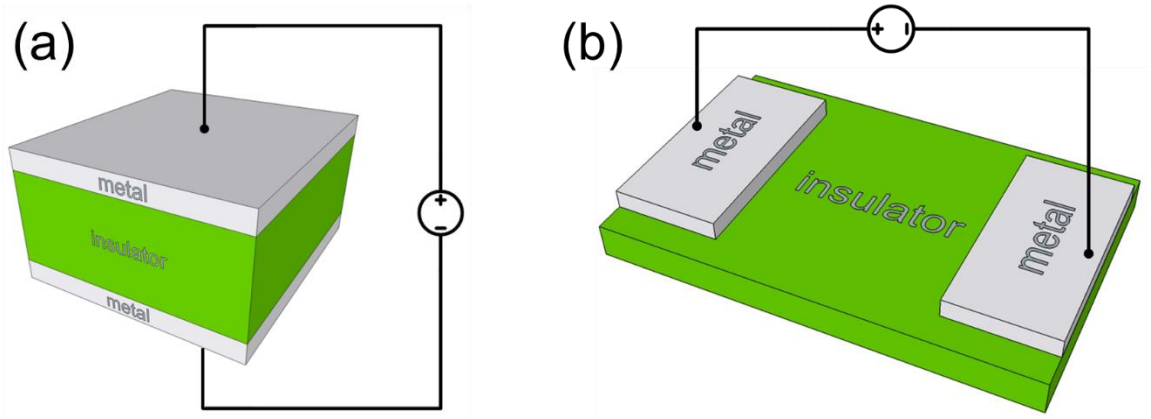

Fig. I.2.1. Basic structure of resistive switching device. (a) vertical device, (b) lateral device.

As mentioned in previous section, the mechanism was unknown at the time when resistive switching was discovered. After years of research, several models have been proposed to explain the resistance switching phenomenon, among which the 'filament' model is the most popular one [10]. This model is illustrated in Fig. I.2.2 in a vertical device. In 'filament' model, the change of resistance is associated with a formation and dissolution of conductive filament in an otherwise insulating material. With the present of conductive filament (Fig. I.2.2a), two electrodes are bridged together and electrons can move 'freely' from one electrode to the other one, thus, the device's resistance is low; while without the conductive filament (Fig. I.2.2b), electrons cannot flow from one electrode to another since they are blocked by the insulating film, thus, the device's resistance is high.

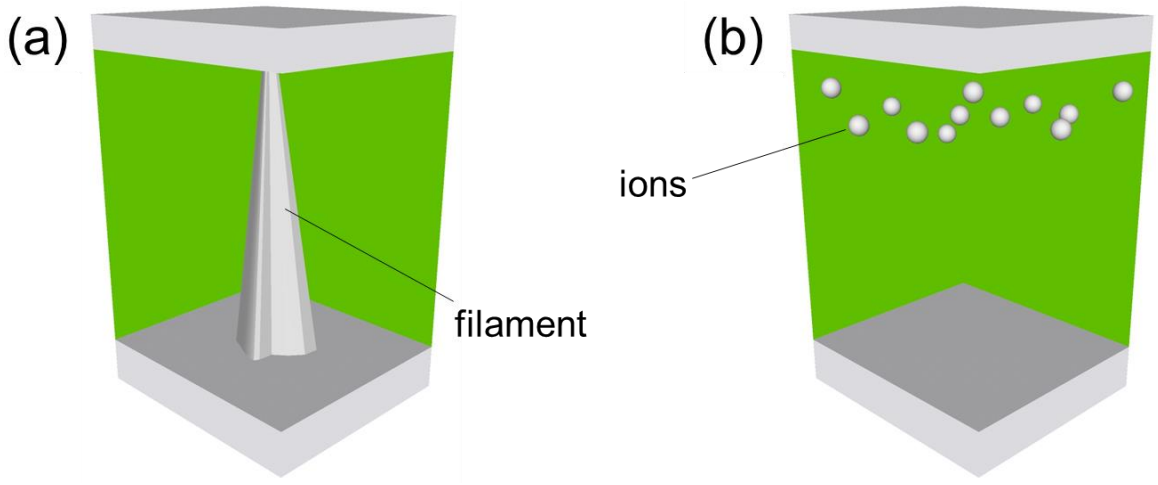

Fig. I.2.2. The 'filament' model used to explain resistive switching. (a) filament formed in insulating layer, (b) filament dissolved in insulating layer.

I.3. Three Different Resistive Switching Types

The aforementioned filament model is an overly simplified model used to describe all resistive switching phenomenon, however, the physics behind filament formation (or

dissolution) and the materials composition of filament can be completely different from one resistive switching technology to another. Three distinct resistive switching variants have been developed, i.e., unipolar resistive switching, bipolar resistive switching based on anions and bipolar resistive switching based on cations [9].

I.3.1. Unipolar Resistive Switching

NiO based devices are usually unipolar switchable [11-13], but under certain circumstances, such as high programming current or using Ni electrode, transition metal oxide based devices can be switched unipolarly as well, unipolar switching has been reportedly observed in TiO_x [14-16], HfO_x [17, 18] and TaOx [19] based resistive switching devices. The signature of unipolar switching is that the device can be programmed and erased by voltage with the same polarity, as shown in Fig. I.3.1. The device is switched from low current high resistance state (green solid line) to high current low resistance state (red solid line) under positive voltage bias, and it can be switched back to high resistance state with a smaller voltage in the same polarity. The switching event is usually too fast to be traced by DC measurement, thus the transition periods are marked by dotted lines.

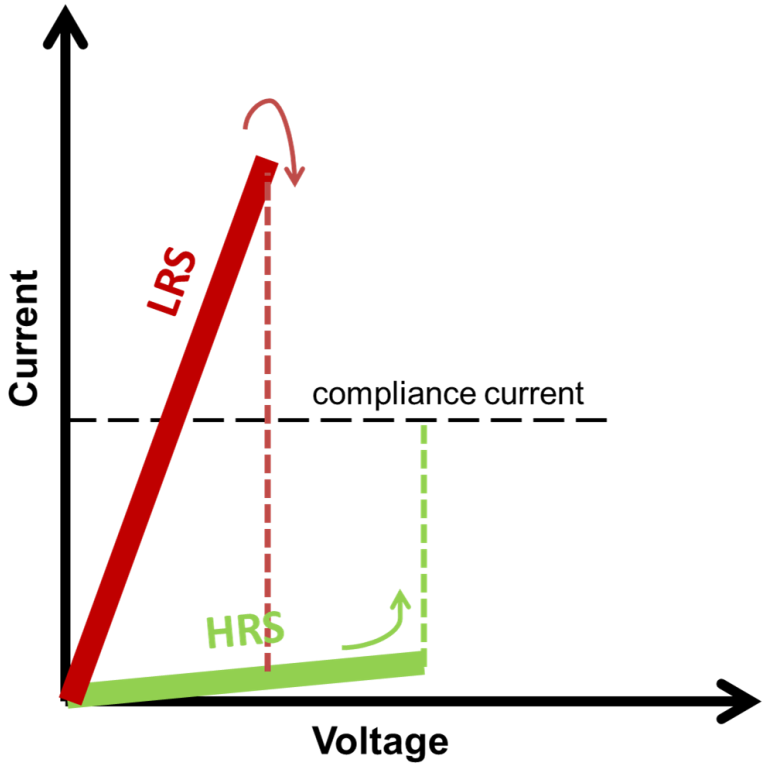

Fig. I.3.1. Schematic I-V curve of unipolar switching device.

Fig. I.3.1. illustrates another important characteristic of unipolar switching, i.e. a much higher current is required to fuse the filament and reset the device back to HRS. It is believed that Joule heating plays an important role in the switching process [20], especially for reset. The large switching current of unipolar device is not desirable for low power applications.

I.3.2. Bipolar Resistive Switching

Different from unipolar switching device, the programming and erasing of bipolar switching device is achieved by applying voltage with opposite polarity. Fig. I.3.2 demonstrates the typical resistive switching curve of bipolar device. The device is switched

from high resistance state (HRS) to low resistance state (LRS) if the applied voltage is higher than a positive threshold, while a negative voltage must be applied to switch the device back to HRS. In general, the erasing current is proportional to programming current for bipolar switching device, thus, the bipolar device's power consumption can be much smaller than unipolar device if it is programmed at low current.

In general, bipolar based resistive switching device can be divided in to two categories, i.e. anion based resistive switching device and cation based resistive switching device.

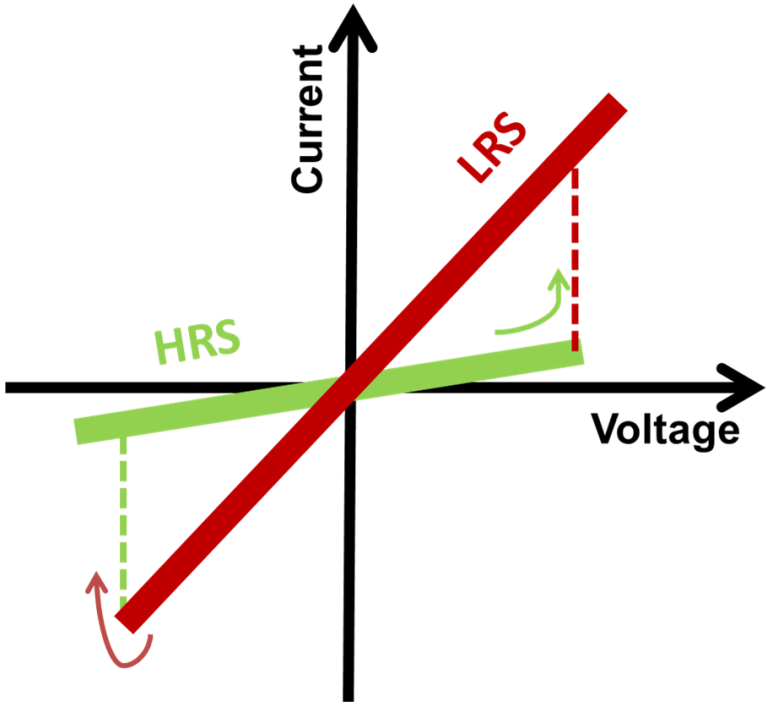

Fig. I.3.2. Schematic I-V curve of bipolar switching device.

I.3.2.1. Anion Based Bipolar Resistive Switching

In anion based bipolar switching device, the resistive switching is due to the field induced drift of oxygen anions, i.e. O^{2-}. The redistribution of anions in the oxide matrix

leads to a generation or annihilation of highly localized, conductive oxygen deficient state [14, 21]. Many transition metal oxides have been tried for bipolar resistive switching including both binary oxides, such as HfO_x [22-25], TaO_x [26-28] and TiO_x [29-31], and complex oxides such as $SrTiO_3$ [32-34].

It should be noted that the conductive filament in this resistive switching type is purely composed of reduced oxide phase and neither of the electrode is actively participate in resistive switching, in other word, they are inert electrodes. The need for oxygen transport in the switching process has led to this technology known as OxRAM when it is used as non-volatile memory for data storage [35].

I.3.2.2. Cation Based Bipolar Resistive Switching

Different from anion based bipolar switching device in which an oxide filament is existed, cation based bipolar switching device has a metallic filament which relies on electrochemical redox reaction and metal ion (typically Ag or Cu ions) transportation [36]. Another key difference between them is that, for anion based switching device, both electrodes are inert, while for cation based switching device, one electrode must be electrochemically oxidizable for metal ions supplement and the other electrode is inert. The active electrode is usually made of Ag or Cu while the inert electrode can be W, TiN, Pt, etc. The thin solid electrolyte layer in between can be chalcogenide glass, oxides, amorphous Si, or multi-layered film. Examples of solid electrolyte used in cation switching device are presented in Table I.3.1.

Table I.3.1. Examples of material systems used in CBRAM devices. Reproduced from [37]. With permission of Springer.

Chalcogenide glasses (ChG)	Dielectrics	Layered
Ge_xSe_y [38-46]	SiO_2 [59-66]	Cu_xS/SiO_2 [83]
Ge_xS_y [42, 47-54]	Ta_2O_2 [67-71]	$Ge_{0.2}Se_{0.8}/Ta_2O_5$ [84]
Ge-Te [55]	WO_3 [72-74]	
Ge-Sb-Te [56]	Al_2O_3 [75-79]	CuS/CuO [85]
As_2S_3 [57]	a-Si [80, 81]	Ge_xSe_{1-x}/SiO_2 [86]
$Zn_xCd_{1-x}S$ [58]	GdO_x [82]	

The underlying physicochemical principles in cation switching device is generally reviewed in [37], and a discussion of electrochemical process for cation switching device composed of different materials system is also provided in [87]. Cation based resistive switching device is also known as programmable metallization cell (PMC), or electrochemical metallization (ECM) or conductive-bridging RAM (CBRAM) for memory application.

I.4. Resistive Switching Mechanism of PMC

As listed in Table I.3.1, many dielectric or solid-electrolyte materials have been studied for working as switching layer of PMC, due to the structural, electronic and compositional differences between chalcogenide glass (ChG) and oxides, the filament growth dynamic in ChG based and oxide based PMC is different.

I.4.1 Filament Growth in Chalcogenide PMC

DC resistive switching can be described starting from a high-resistance state, where there is no electrodeposit of active metal (Ag or Cu) on the bottom inert electrode (Fig. I.4.1a). The device will change to a low-resistance state if the bias on active electrode is increased to a positive set voltage (V_{set}). This transition involves three steps: 1) the active

anode is oxidized (i.e., $M \rightarrow M^{n+} + ne^-$, n = 1 or 2) and the M^{n+} cations dissolve into the ChG solid electrolyte; 2) the cations drift towards the inert electrode through the thin chalcogenide film; 3) the cation is reduced and nucleates (Fig. I.4.1b) at the inert electrode according to reaction ($M^{n+} + ne^- \rightarrow M$). A filament then grows from the inert electrode towards the active electrode as more anodic atoms electrodeposit on the filament material. Finally, the device is switched to low resistance state when the metal filament reaches to the active electrode and bridges the chalcogenide (Fig. I.4.1c). At this point, the current increases dramatically until limited by the programed current compliance.

The transition from the low-resistance state back to a high-resistance state is essentially the reverse of the programming process. When a negative voltage bias is applied to the active electrode, the metallic filament will be oxidized and dissolve into the chalcogenide (Fig. I.4.1d), at negative voltage, M^{n+} cations migrate back to active electrode where they get reduced and deposited. At a voltage below the reset potential (V_{reset}), the device switches back to its high-resistance state (Fig. I.4.1a).

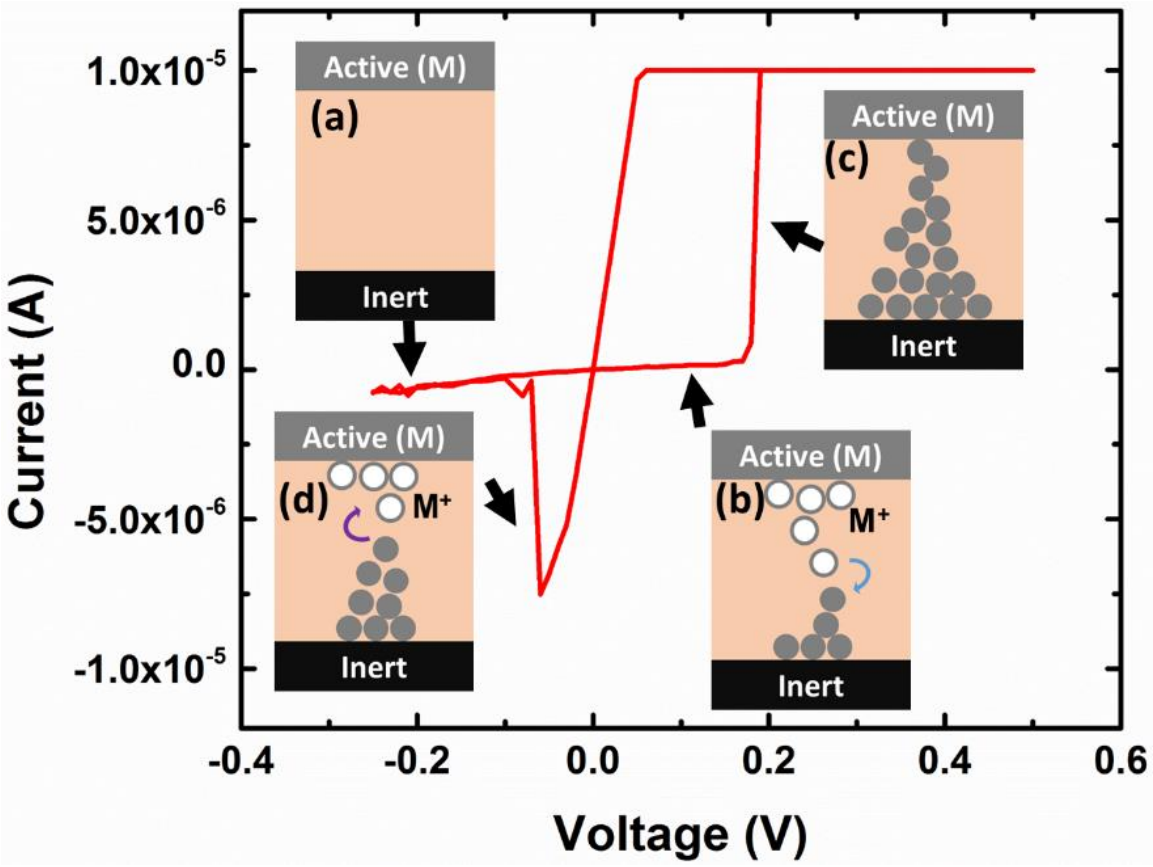

Fig. I.4.1. Filament growth model of Chalcogenide-glasses based PMC. © 2017 IEEE. Reprinted with permission from Ref. [88].

Chalcogenide based resistive switching device has been commercialized in non-volatile memory application, indicating that the characteristics and reliability of the technology are sufficient for demanding markets [51].

I.4.2. Filament Growth in Oxide PMC

The aforementioned filament growth in chalcogenide based PMC has been well described in many works [8, 36]. It is generally accepted that a metallic filament grows from inert electrode towards active electrode in chalcogenide, resulting in a conical shape

with a thicker body near inert electrode and a thinner body near active electrode (Fig. I.5.2 in next section). However, due to the low ion mobility in many oxides, the direction of filament growth in oxide based PMC may be different. Some of recent works suggest that the filament in thin film oxide grows from active electrode towards inert electrode, therefore, a reversed conical filament is formed [89-91] (details are in next section). Based on these works, a filament growth model for oxide PMC has been proposed and is depicted in Fig. I.4.2.

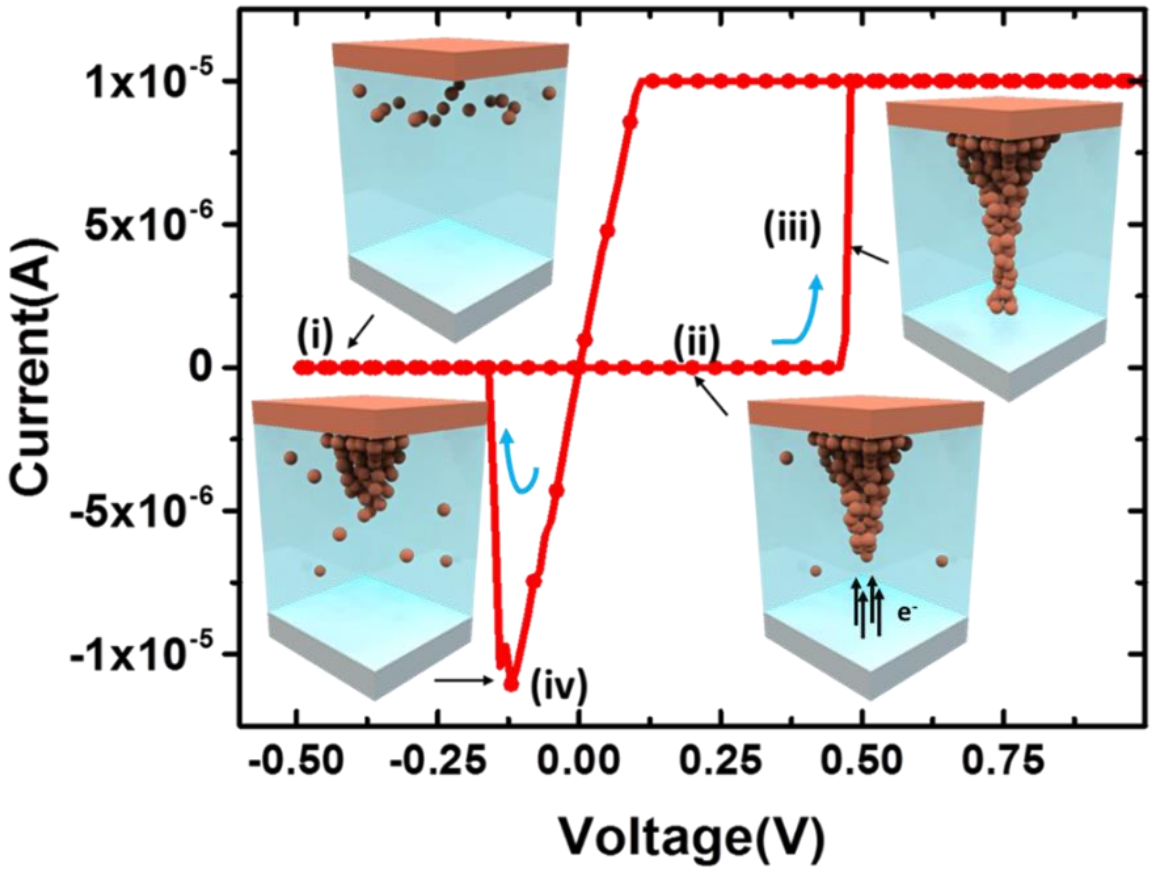

Fig. I.4.2. Filament growth model of oxide based PMC. © 2015 IEEE. Reprinted with permission from Ref. [92].

Similarly, the red solid line with solid circle marker in Fig. I.4.2 is a typical bipolar switching curve of oxide PMC. The x-axis is the applied voltage, which is measured as the potential difference from the active top electrode (Cu or Ag) to the inert bottom electrode. The y-axis is the corresponding current in PMC device. In the initial high resistance state (i), the device has only a small number of anodic ions that are located close to the active electrode. These ions might be incorporated during device fabrication. Under positive bias, the active electrode loses electrons through an oxidization reaction and generates cations ($M \rightarrow M^{n+} + ne^-$, n = 1 or 2). These cations will drift towards the inert electrode along with the electric field. Different from the cations in chalcogenide materials, the cations in oxides move much slower, thus, the reduction of cations can occur before they reach to the inert electrode by capturing the tunneling electrons within the thin oxide film ($M^{n+} + ne^- \rightarrow M$). The metal filament will grow from the active electrode towards inert electrode (ii) until a bridge between these two electrodes is formed (iii). At this point, the device is switched to a low resistance state (LRS) and the current increases dramatically until limited by current compliance. Since the ion concentration close to the active electrode is higher than the other side, the formed filament has a thicker body at the active electrode and a thinner body at the inert electrode resulting in a reversed conical shape.

Filament erasing process is an opposite process of programming. The conductive filament will be oxidized and dissolved into the oxide matrix when a negative voltage is applied on the active electrode. The device is then switched back to HRS (iv). The erasing process is initiated at the interface between the oxide switching layer and the inert electrode where the filament is the thinnest.

It should be noted that the above model only illustrates one out of many possible mechanisms for filament growth in thin film oxides, but it is good enough to explain the common approach of resistive switching and the primary redox reactions in oxide based PMC. Indeed, due to the variations in the properties of thin films, fabrication conditions and characterization environment, inconsistent filament morphology and growth direction have been reported across different works. Some in-situ microscopy of oxide PMC device also show a ChG-like filament growth, i.e. from inert electrode towards active electrode [93, 94]. In addition, recent electrochemistry studies point out that water moisture in oxides may affect the growth dynamics in significant way [95].

I.5. Microscopic Imaging of Nano-Filament

Clearly, PMC is a filament based technology. The filamentary model was proposed based on the electrical characteristics of PMC, including the dramatic change in current and an observation of non-scalable on-state resistance [96]. However, direct observation of filament is also required to support such hypothesis. A variety of characterization methods have been applied to image the conductive filament buried in insulating layer. The most popular techniques are:

- Scanning Electron Microscopy (SEM)
- Transmission Electron Microscopy (TEM)
- Conductive Atomic Force Microscopy (C-AFM)

I.5.1. Filament Observation in Chalcogenide-Glass PMC

In the work [97], the morphology of filament in Ag-Ag:Ge_xSe_y based lateral PMC has been extensively studied. An ex-situ SEM image of conductive filaments is demonstrated in Fig. I.5.1. Fig. I.5.1a shows the top view of a laterally configured PMC device, the active electrode is on the left which is made of Ag, while the inert electrode is on the right which is made of Ni. The two electrodes are separated by a Ag doped $Ge_{30}Se_{70}$ film in a distance of 15 μm. Two dendritic shape Ag filaments appeared when the Ag electrode was stressed by positive voltage. Fig. I.5.1b shows the zoomed-in image of one filament, in which the filament is thicker at Ni electrode and thinner at Ag electrode. This indicates that the growth direction is from Ni towards Ag which is consistent with the resistive switching mechanism of ChG based PMC described above.

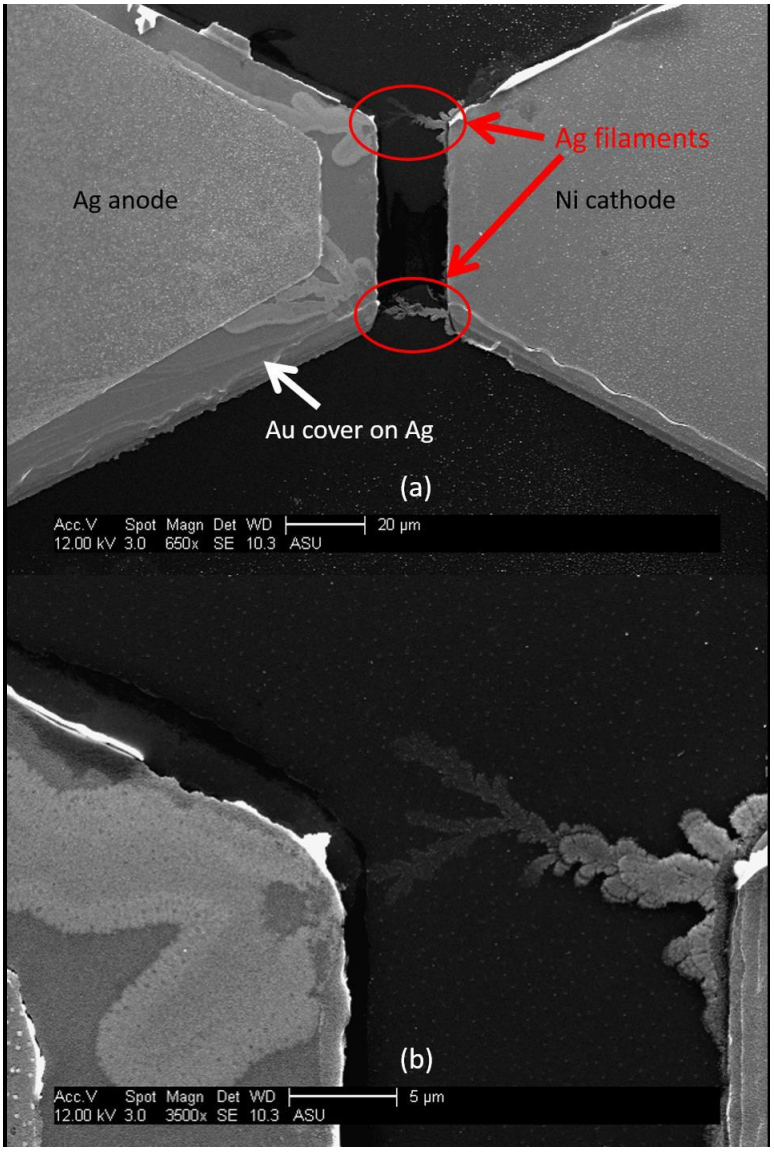

Fig. I.5.1. SEM image of filament growth in lateral chalcogenide glass based PMC. © 2015 Reprint with permission from [97].

Due to the size limitation of vertical PMC, i.e. the nanometer separation between two electrodes, cross-section TEM is the most appropriate method for filament imaging. Because of the filament is negligibly small compared to the size of device, ex-situ TEM is a time-consuming method for filament observation since the finding of a conducive

filament may require multiple focused ion beam (FIB) cuts. Therefore, in-situ TEM is a more popular way to image the conductive filament in vertical PMC. For in-situ TEM, PMC device is imaged and tested at the same time, thus, a real-time filament growth is observable.

Fig. I.5.2 demonstrates the in-situ TEM observation of a real-time filament growth in Cu-Cu:GeTe PMC device [98]. The test setup is schematically illustrated in Fig. I.5.2a, the active Cu electrode is grounded while the inert electrode (Pt-Ir probe) is electrically biased. Several TEM frames are shown in Fig. I.5.2c – f which are corresponding to the I-V data points in Fig. I.5.2b. As indicated by the TEM images, more than one filaments are found in the solid electrolyte layer. The body of filaments at inert electrode is thicker while it is much thinner at Cu electrode side, which again fulfills the filament growth direction of ChG based PMC. Upon reversing the voltage polarity, the thinner part of filament is dissolved completely (Fig. I.5.2f) and the devices was reset to high resistance state (HRS) which is indicated by the small current at +0.4V in Fig. I.5.2b.

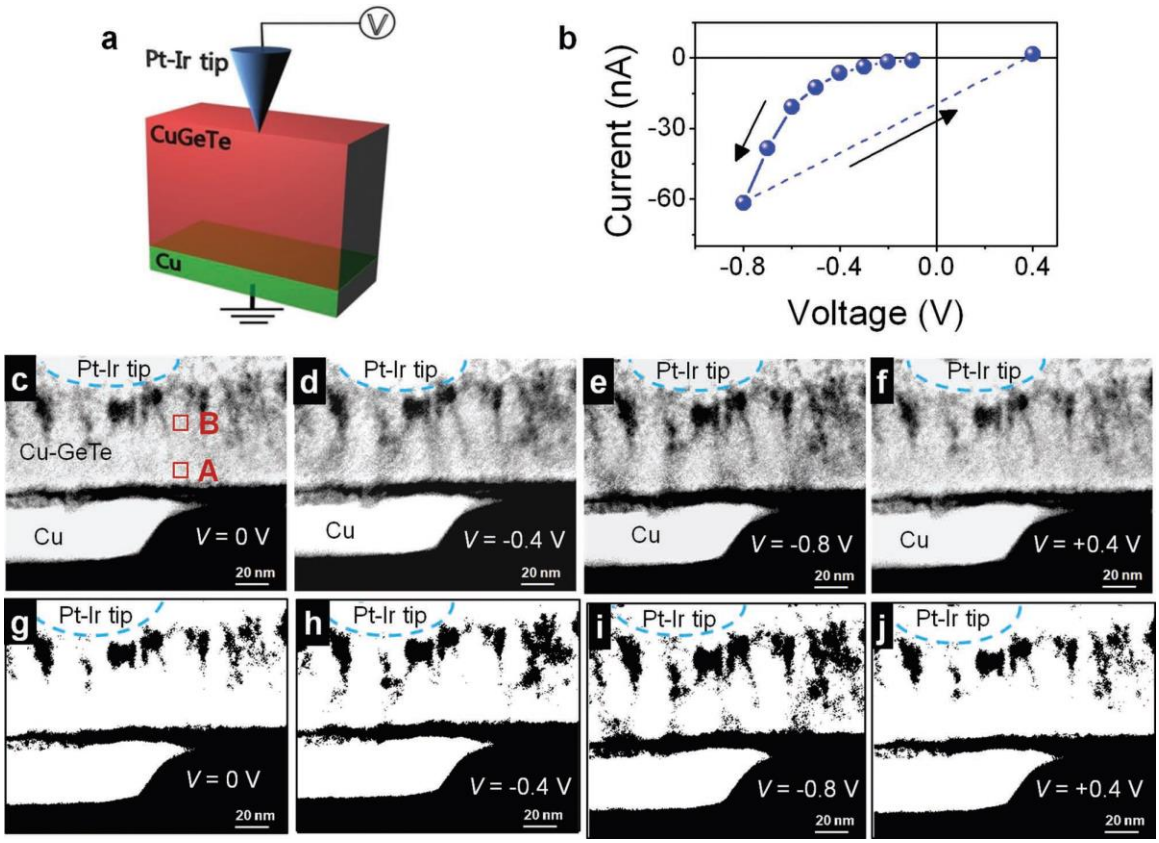

Fig. I.5.2. In-situ TEM observation of filaments in vertical chalcogenide glass based PMC device. Reprinted by permission from John Wiley and Sons: Advanced Materials, Ref [98].

I.5.2. Filament Observation in Oxide PMC

Similarly, many microscopic works have been performed in recent years to illuminate the filament growth in oxide PMC.

A series of SEM images in Fig. I.5.3 demonstrates the filament evolution in Ag/SiO_2/Pt lateral PMC [99]. Two electrodes are laterally configured with the Ag active electrode being on top and the Pt inert electrode being on bottom, they are separated by 800 nm by the SiO_2 switching layer. Because of the small mobility of Ag in SiO_2, a Ag filament only appears when a 30 V voltage was applied for 210 s, the picture of filament

is shown in Fig. I.5.3d. Referring to Fig. I.5.3b and I.5.3c, the filament was growing from the Ag active electrode towards Pt inert electrode, thus, a conical shape filament with a thicker body at Ag electrode and a thinner body at Pt electrode is formed, which is contrary to the filament growth in ChG PMC device. Moreover, rather than a continues metallic filament that is usually observed in ChG PMC [97], the filament in SiO_2 is composed of many discrete Ag particles "floating" on the surface of or partially embedded into the SiO_2 layer. This granulated filament can be a result of low ionic mobility and redox reaction rate in SiO_2 material. A similar filament type was also reported in [90].

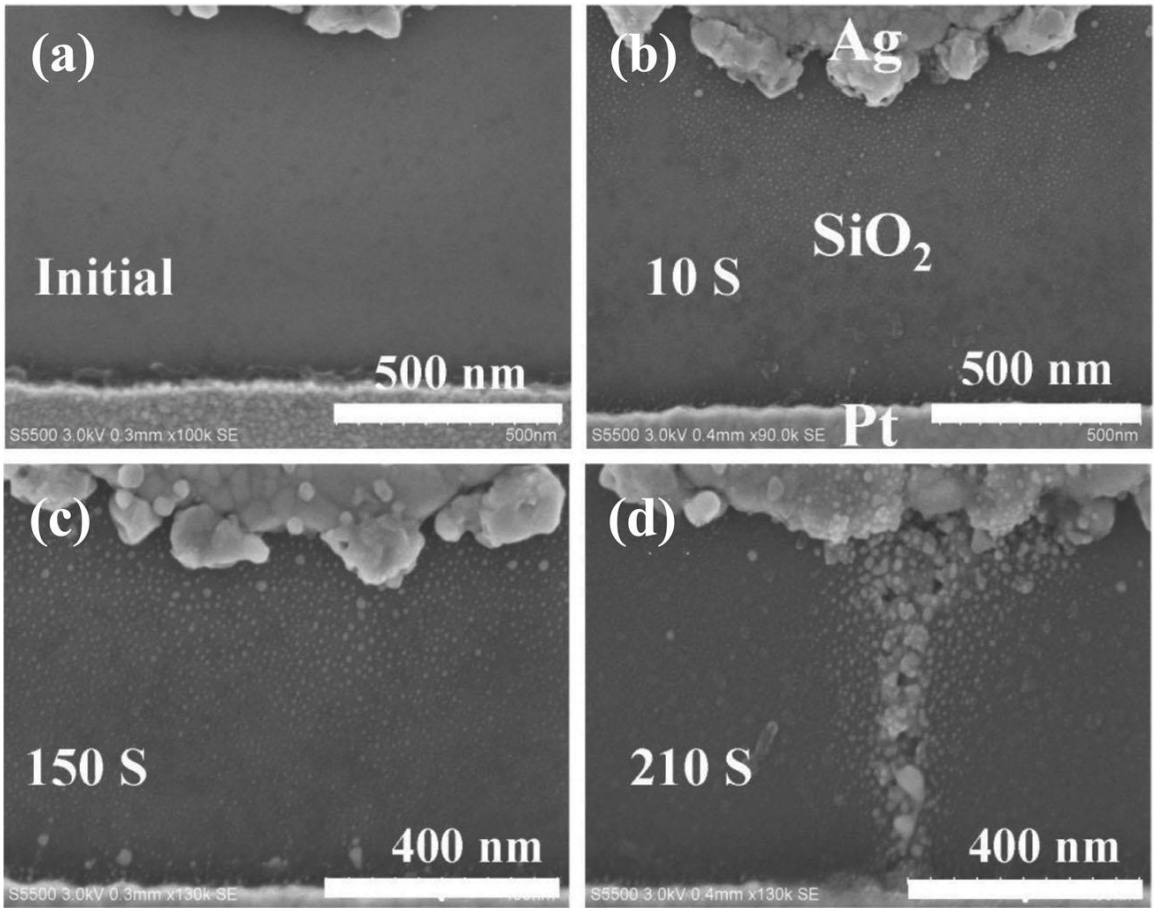

Fig. I.5.3. Dynamic filament growth in lateral Ag/SiO_2/Pt PMC. Reprinted by permission from John Wiley and Sons: Advanced Functional Materials, Ref [99].

An in-situ TEM imaging of filament in Ag/ZrO_2/Pt vertical PMC was also reported in [91]. The device structure studied in this work is shown in Fig. I.5.4a and b, to fabricate it, Ti, Pt, ZrO_2 and Ag thin films are sequentially deposited directly on the platform of W probe, then several steps of FIB cuts and milling was applied to define the PMC devices. To test the device, another W probe is manually controlled to touch the thick Pt protecting layer rather than to the metal electrode directly. In such way, the PMC device, especially the electrode/switching layer interfaces, is well preserved which helps in studying the filament growth in a more realistic way. The W platform is electrically biased while the movable probe is grounded. The programming and erasing I-V characteristics are plot in solid-circle line in Fig. I.5.4c and d, respectively, in which clear set and reset hysteresis is demonstrated. The inset picture of Fig. I.5.4c shows the TEM image after the device is programmed, an obvious filament extended from Ag electrode to Pt electrode is captured. This filament is proved to be composed of Ag by EDX analysis which is shown in Fig. I.5.4e. The filament disappears after erasing process, and the TEM image for a reset device is shown in Fig. I.5.4d.

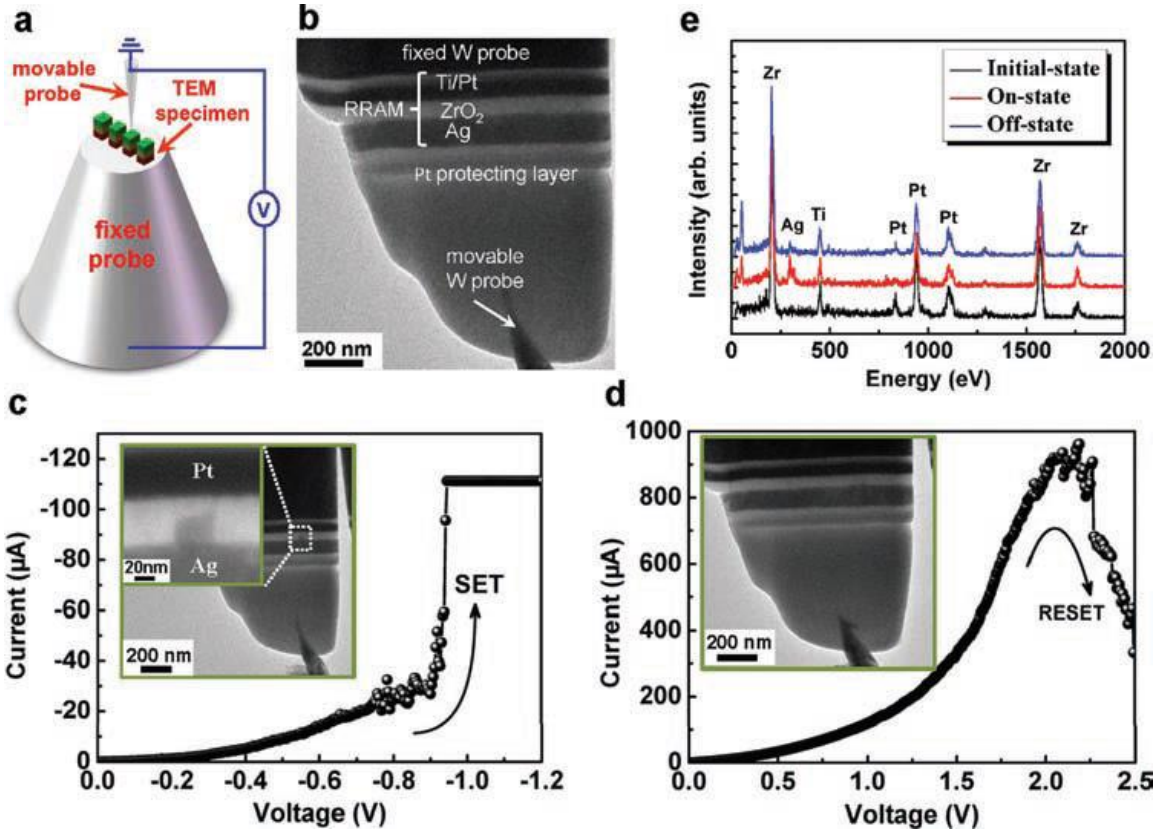

Fig. I.5.4. Real-time in-situ TEM observation of filament growth in vertical Ag/ZrO_2/Pt device. Reprinted by permission from John Wiley and Sons: Advanced Materials, Ref [91].

Other than in-situ TEM, the shape of filament in vertical PMC device was also investigated by conductive-AFM (C-AFM). C-AFM is a surface characterization technique which is built up on conventional atomic force microscopy (AFM). Rather than collecting surface tomographic information, C-AFM scan captures a conductivity map of surface. This conductivity map is helpful in targeting the location of conductive filament. Celano et al. has successfully constructed a 3D image of conductive filament using C-AFM measurement [100]. The C-AFM results of a Cu/Al_2O_3/TiN vertical PMC are shown in Fig. I.5.5. To approach to the filament, the top Cu electrode was physically removed at first, then surface current map of the active device region was captured by C-AFM scan, after

that, several atomic layers of Al_2O_3 film was physically scratched off by AFM tip and the newly exposed surface was scanned again to collect another current map. This scratch-and-scan process was repeated serval times until the highly conductive bottom electrode was exposed. The current maps of each scan are listed in Fig. I.5.5b with the blue region being conductive and the red region being insulating. For the first 5 current maps, there is a small conducting point (blue) in the middle of the insulating Al_2O_3 film (red) and this small conducting region is the filament. All the current maps are reconstructed together by computer software and the reconstructed image is shown in Fig. I.5.5c. In this figure, only high current region is plot and the low-current insulating region has been subtracted, thus, this 3D profile can be related to the conductive filament. It is apparent that the filament in Al_2O_3 has a reversed conical shape which is consistent with the filament growth model of oxide base PMC.

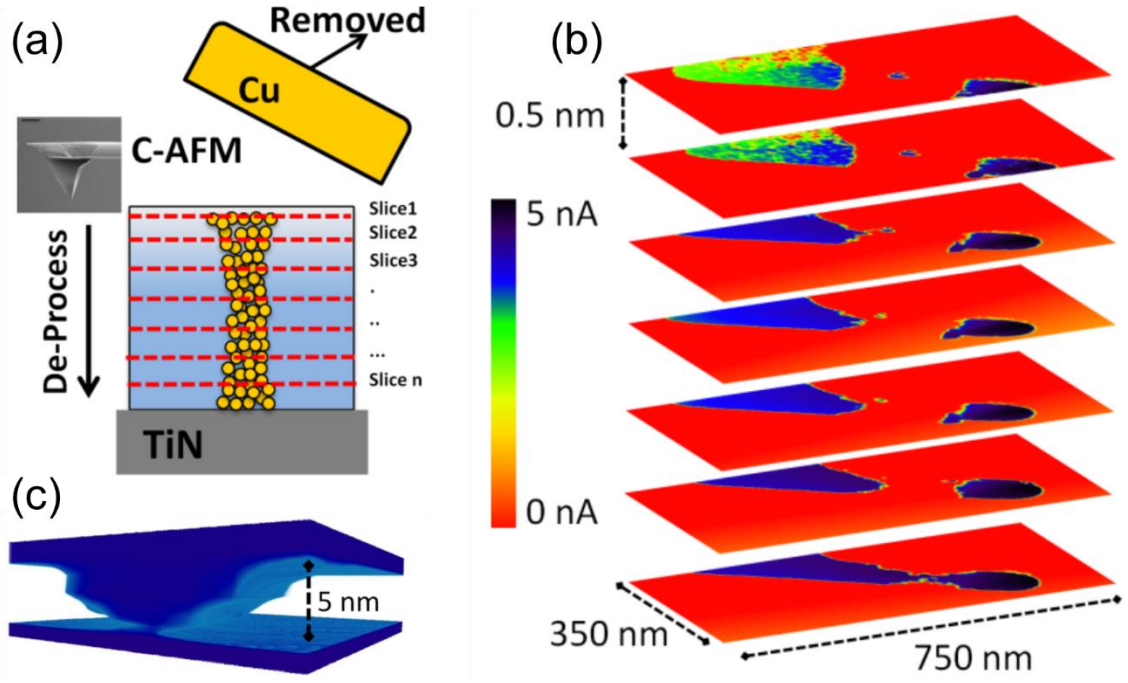

Fig. I.5.5. Conductive-AFM microscopy of 3D filament in Cu/Al_2O_3/TiN PMC. © 2013 IEEE. Reprinted with permission from Ref. [100].

I.6. Motivation of Cu-Silica Based PMC

From above discussion, it is obvious that conductive filament is responsible for the resistive switching of PMC. Both chalcogenide glass (ChG) and oxides can be used as switching layer for ion transport, however, the filament morphology are different between ChG based PMC and oxide based PMC.

Although ChG PMC has been proven to be a viable replacement for certain types of non-volatile memory technology, there is still some unwillingness for the semiconductor foundries to incorporate these materials into back-end-of-line (BEOL) processing. Ironically, a potential solution to the reticence surrounding "new materials" lies with Cu diffusion in deposited silicon dioxide films, as both materials are commonplace in advanced ICs. Cu migration in dielectrics has been a persistent problem for semiconductor manufacturers who wished to adopt Cu interconnect [101] but Cu-silica based PMC exploits this "problem" to enable controlled transport of Cu and metallic bridge switching in the silica. This approach has drawn increasing attention in recent years since the devices exhibit similar switching characteristics to those based on chalcogenide glasses while possessing inherently greater CMOS compatibility. In the following part of this dissertation, the author would like to discuss how to employ the resistive switching behavior of Cu-silica PMC to enable future applications such as ultra-high density crosspoint memory arrays and neuromorphic computing. As shown in Fig. I.6.1, by tuning the parameters in device fabrication and electrical characterization, Cu-silica PMC can possess different behaviors which can be suitable either for non-volatile memory (NVM), sneak-path-inhibition selector or electronic synapse.

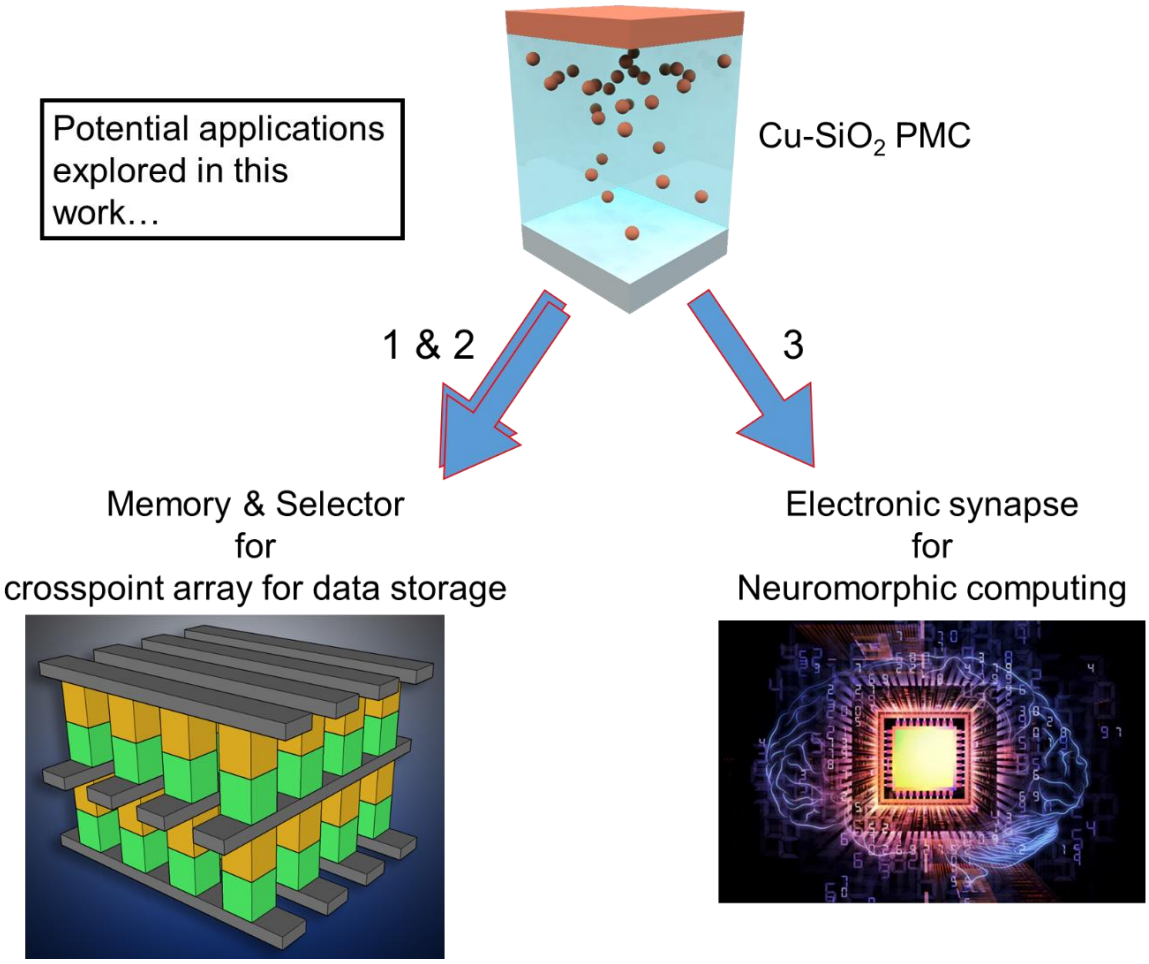

Fig. I.6.1. Potential applications of Cu-silica PMC.

CHAPTER II

CU-SILICA PMC FOR NON-VOLATILE DATA STORAGE

II.1. The Need for New Memory

In the era of information explosion, the sharing, storage and analysis of information is happening all the time at every corner of the world. The transformation from personal computing and storage to cloud type computing and storage is changing the fundamental architecture of server platform in significant way. In addition, the emerging technologies, such as interactive consumer electronics, artificial intelligence (AI) and Internet of Things (IoT), also pose great challenge for efficient data manipulating. The desire for high density, fast speed and low power non-volatile memory has never been greater.

Conventional magnetic hard disk drives (HDDs) are being relegated to back-up duty in data centers as their inherent high latency (~ milliseconds), high power consumption (~ millijoules), considerable bulk, and fragility mean that they are unsuitable for new mobile markets [102]. Flash technology bests HDDs in terms of latency and portability [103, 104]. The scaling anxiety of planar NAND Flash has been greatly relieved because of recent breakthroughs in 3D integration [105]. However, the programming speed and endurance of NAND Flash still cannot meet the requirements of many applications. In addition, the lack of ionizing radiation immunity of floating gate technology hinders its usage in the realm of medical equipment and space-based systems where radiation tolerance is required [106]. The reliability of NAND flash becomes even worse with continuous shrinking of device size since less than hundred electrons are stored in the

floating gate for 1X nm technology node, single electron loss will introduce great variations in gate threshold voltage.

II.1.1. Low Latency Storage Class Memory

In modern computing platform, several layers of memories are working together to support the data transfer and storage. A view of memory architecture is demonstrated in Fig. II.1.1. In general, these memories can be divided into two sub-groups, i.e. internal memory and external memory.

The internal memories are mainly used to temporally store the frequently used data and must be able to feed data into the arithmetic-logic unit (ALU) of CPU in fast way. Thus, the distance between internal memory and CPU is 'short'. The CPU register, all levels of caches and dynamic random access memory (DRAM) all belong to internal memory. As shown in Fig. II.1.1, internal memories have an access latency in the range of nanoseconds to tens of nanoseconds with the register being the fastest and DRAM being the slowest. Unlike internal memory which loses the stored information once the power is turned off, the external memory won't lose the stored information when the power is turned off, thus, external memories are used to "permanently" store the generated data for future usage. However, the external memory is located "far away" from CPU, it requires significant amount of time to transfer the required data from external memory to CPU. The most popular external memories are FLASH memory and hard disk drive (HDD). External memory has an access latency from tens of microseconds to tens of milliseconds with the FLASH memory being faster than HDD. Due to the dramatic different accessing time, a more than 3 order of magnitude latency gap is created between internal and external

memory. This latency gap bottlenecks the performance of entire computing system since the CPU is wasting more than thousands of active cycles waiting for the data to be sent in from external memory.

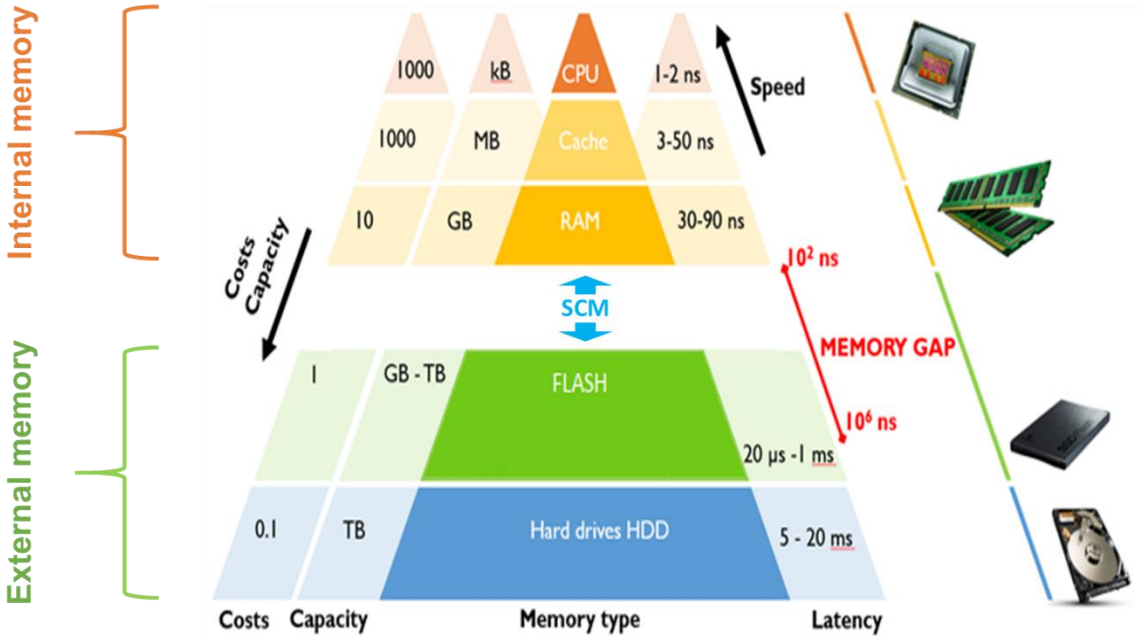

Fig. II.1.1. Memory architecture in modern computing system © 2015 Reprint with permission from [107].

To improve the performance of Von Neumann machine, this "latency gap" must be killed. Increasing the operation speed of NAND Flash is one way since NAND Flash has a lower cost and higher capacity than DRAM. In recent year, the replacement of conventional SATA (or SAS) IO interface with PCIe (NVMe) by Intel Corp. cuts off 25 microseconds of access latency in NAND Flash solid-state drive (SSD), as shown in Fig. II.1.2, a 20% latency reduction is achieved. However, this achievement is not enough to kill the "latency gap". As indicated by the blue bar in Fig. II.1.2, the "Drive Latency" is the major latency source which is mostly determined by the internal physics of NAND cell,

i.e. Fowler-Nordheim (F-N) tunneling. The operation speed of NAND cell (either floating-gate or charge-trap transistor) is dependent on F-N tunneling current which can be hardly increased for reliability reason. Therefore, engineering NAND Flash is not the best way to eliminate the notorious "latency gap". New memory solution with different physics is required.

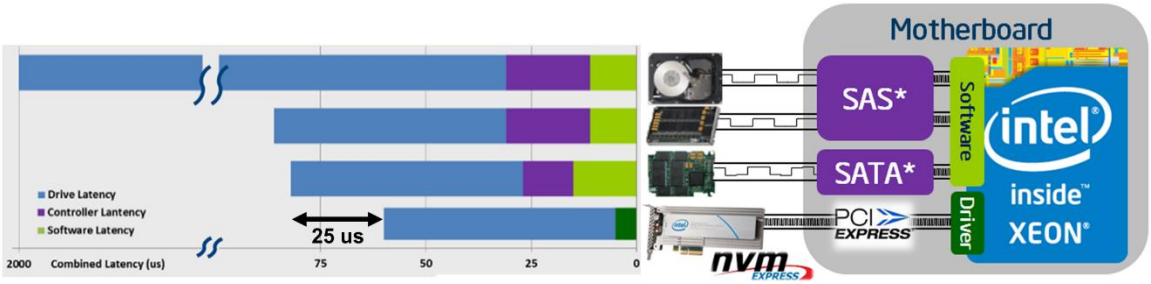

Fig. II.1.2. Access latency reduction in SSD through IO engineering [108].

The idea of storage class memory (SCM) is another way proposed to fill the "latency gap" between DRAM and NAND Flash. The ideal SCM should have an access time less than a microsecond, a higher capacity but lower cost compared to DRAM, and most importantly it should be non-volatile. Many emerging memory technologies, including PMC based CBRAM, has been demonstrated to be suitable for SCM. As exhibited by Western Digital Corp. in Fig. II.1.3, CBRAM can be operated with smaller access time than NAND and, due to the structural simplicity, it is easy to be fabricated in crosspoint stacks with no theoretical limitations on the number of stacked layers. This crosspoint architecture leads to ultra-high density and low cost memory.

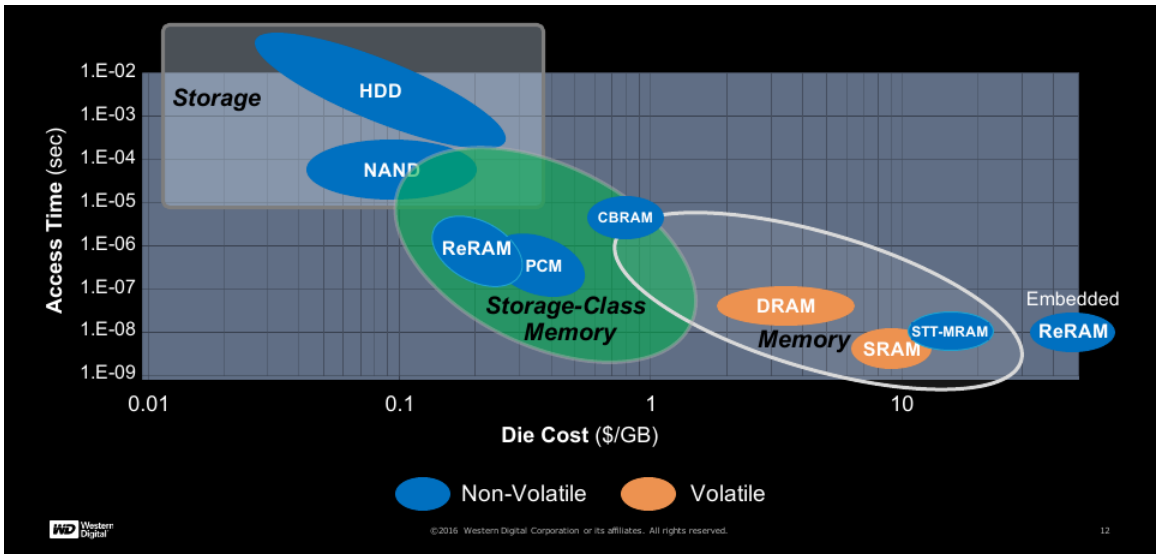

Fig. II.1.3. Emerging non-volatile memory for Storage-class Memory [109].

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II.1.2. Low Power Memory for Internet of Things

In recent years, Internet of Things (IoT) is gaining significant popularities and it is believed to be an important driving force for economic growth. IoT is the interconnection of vast number of embedded devices to form networks of hardware, the IoT idea is illustrated in Fig. II.1.4. IoT is expected to usher in automation in nearly all fields which enables advanced applications such as smart grid, smart home and smart cities.

Fig. II.1.4. Internet of Things (IoT) [110].

Extraordinary progress has been achieved and it is predicted to embrace a rapid market growth in the next five years. In Ericsson's Mobility Report, it claims that the total number of IoT devices will be 18.1 billion by 2022 which more than doubles the number of mobile phone, the prediction is summarized in Fig. II.1.5. Based on Gartner's report, the economic value of IoT market will be 1.9 trillion by the year of 2020 [111].

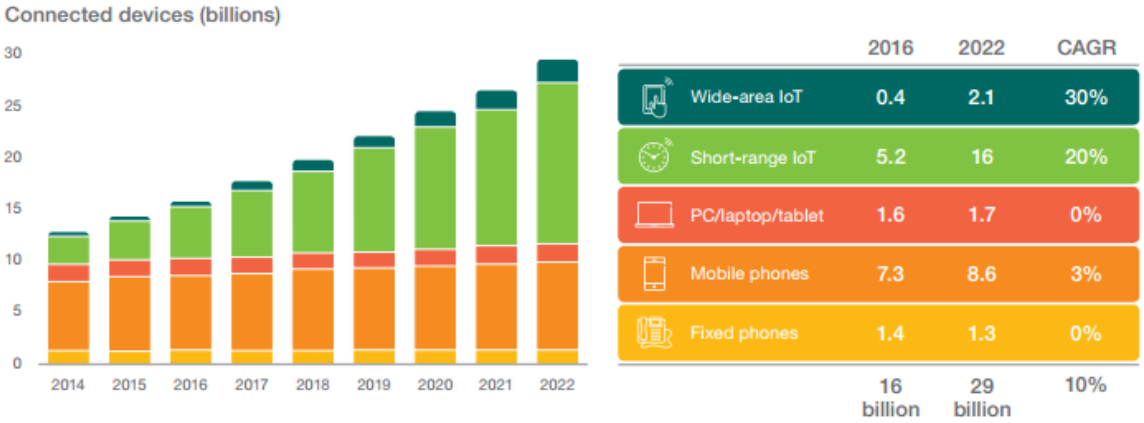


Fig. II.1.5. The market growth of IoT devices, predicted by Ericsson [112].

Even though IoT can be a strong driving force for global economic growth in the following years, there are several major challenges that threats the popularization of IoT, one of the most serious problem is the requirement of extended battery life for embedded devices. In embedded devices, significant amount of energy is consumed by memories. The non-volatile memories used for code storage in most embedded systems are arrays of floating-gate transistors, such as NOR Flash or EEPROM, in which the cell programming is based on the channel hot electrons. Almost all of energy is wasted as joule heating since only one out of millions of electrons is "lucky" enough to tunnel into floating gate. Therefore, finding novel low-power non-volatile memory is essential for the save of battery life in IoT devices. Cu-silica PMC has been reported to be capable of switching with current as low as pico-amps [40], thus, it's a promising NVM candidate for IoT applications.

II.2. Microfabrication of Cu-Silica PMC

To address the two problems mentioned above, Cu-silica based PMC is developed in this work. In this section, the microfabrication of this PMC is introduced.

Fig. II.2.1 demonstrates the partial layout of vertical PMC device, it shows an overlay of three photo-masks used for device fabrication. Mask-1 is a dark field etch mask for the creation of through-hole via and expose common ground inert electrode, this mask is colored in pink. Mask-2 is also a dark field lift-off mask which is used to pattern Cu electrode and is indicated by green squares in Fig. II.2.1. Mask-3 is another dark field lift-off mask used to create contact pads (blue polygons) for probing. For simplification, only four PMC devices are shown in Fig. II.2.1, they have private contact pads, Cu electrode and via but share a common inert electrode. The size of PMC device is defined by the area

of via, in this work, devices with via size ranging from 2.5 µm to 500 µm are studied. The detailed PMC device fabrication flow is illustrated below in cross-section view.

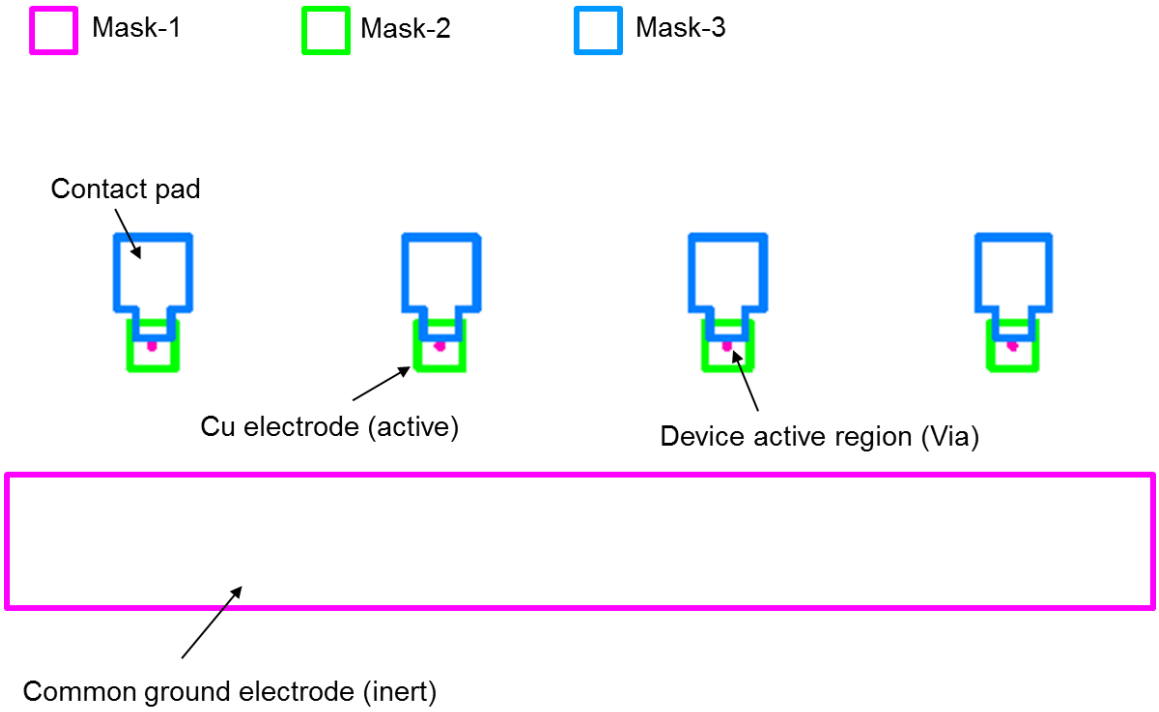


Fig. II.2.1. Layout of single-isolated PMC device (overlap of three photo-masks).

Starting from an RCA cleaned 4-inch silicon wafer, a layer of 200 nm Si_3N_4 was deposited by low pressure chemical vapor deposition (LPCVD). This silicon nitride film acts as an isolation layer between PMC devices and silicon wafer. This nitride coated wafer is used as substrate to support device fabrication.

Step 1: A 60 nm thick tungsten blanket film was DC sputtered on top of Si_3N_4 by a Lesker PVD75 system. The sputtering rate is around 1Å/s with 4 mT chamber pressure (Ar gas) at a power of 90 W. This blanket tungsten film is the inert electrode of PMC device. Then, a layer of 100 nm thick silica was deposited on top of tungsten film by plasma-enhanced chemical vapor deposition (PECVD) at 350°C with SiH_4 and N_2O gas. This

PECVD oxide is for device-device isolation, thus, a reasonable high quality oxide is preferred. Fig. II.2.2a illustrates the film stacks at this point.

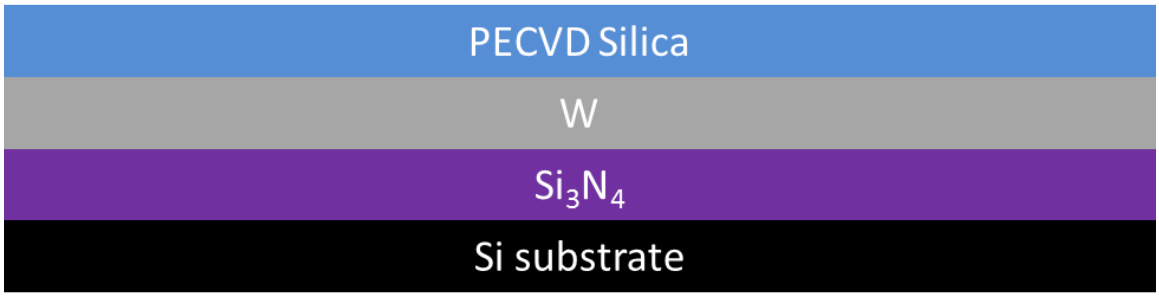


Fig. II.2.2a. Inert electrode and device-to-device isolation layer deposition.

Step 2: The PECVD silica was then patterned by photo-lithography to create vias and bottom electrode. Firstly, hexamethyldisilazane (HMDS) and AZ3312 was sequentially spin coated on the wafer at 4000 rpm for 30s followed by soft baking at 100°C for 120s. HMDS acts as the resist adhesion layer and AZ3312 positive photoresist was used for this step because of its low thickness helps in resolving small features (2.5 µm via). The total photoresist thickness after baking was around 1 µm. The wafer was then aligned with Mask-1 by OAI 808 aligner and exposed under UV light for a total dose level of 50 mJ/cm^2. This step is illustrated in Fig. II.2.2b. The shadow region of photoresist layer was removed by MIF 300 developer in the development process.

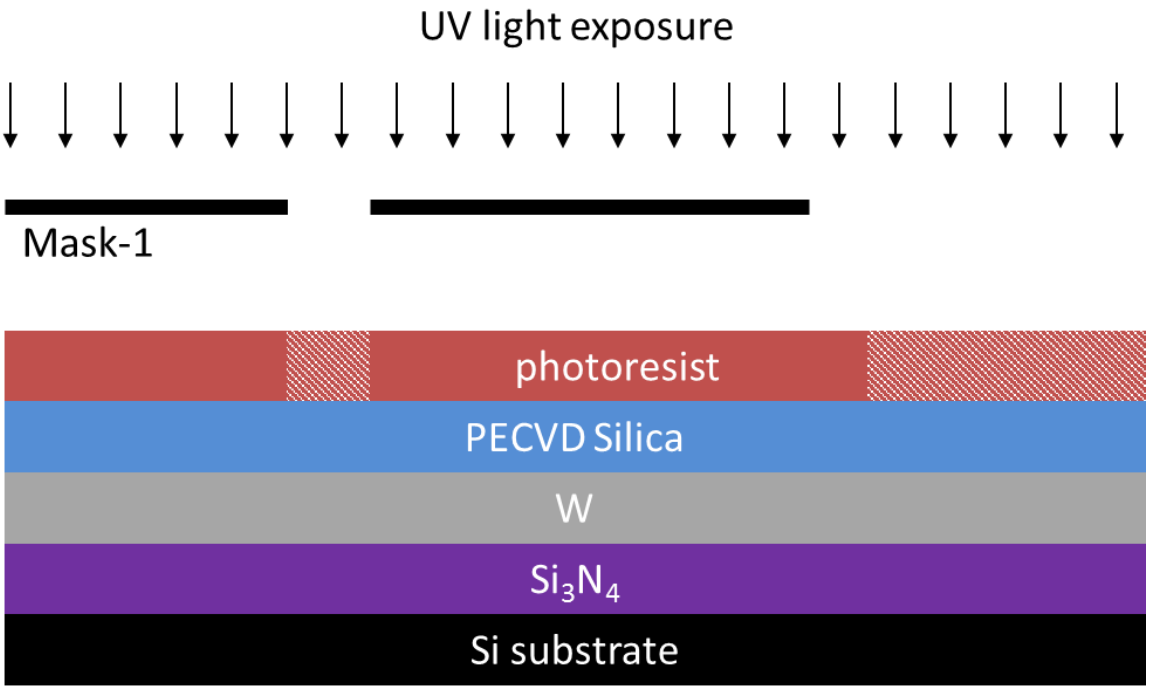


Fig. II.2.2b. Via and common inert electrode photo-lithographical patterning.

Step 3: The uncovered parts were then etched off by buffered oxide etch (BOE) solution to create vias and expose W inert electrode. The BOE (20:1) used here is a mixture of 20 parts of 40% ammonium hydrofluoric (NH_4F) and 1 part of 49% HF which provides a much better etch rate stability than diluted HF. The resulting structure after wet etch is shown in Fig. II.2.2c.

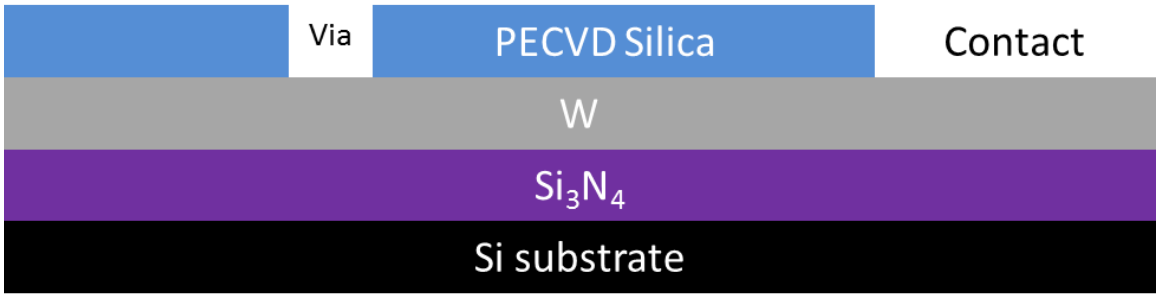


Fig. II.2.2c. Wet etch PECVD silica to create vias and expose inert electrode.

Step 4: In this step, a blanket layer of silica was deposited on the etched wafer. This silica film is the most critical layer since it is the medium for ion transport and filament growth. The film property directly affects the resistive switching characteristics. A variety of methods have been tried to deposit the switching layer:

1. Electron-beam evaporated silica: electron beam evaporated silica is the simplest way for switching layer deposition. The half fabricated wafer was transferred into Lesker PVD75 electron beam evaporator with wafer at chamber top and silica source at chamber bottom, a layer of 13 nm porous silica is evaporated at room temperature with a rate of 0.3Å/s.
2. Remote-plasma CVD (RPCVD) silica: In RPCVD chamber, the half fabricated wafer was placed bellow the precursor nozzle (SiH_4 and N_2O). A 5-nm silica layer was chemically deposited at 200°C with a deposition rate of 1Å/cycle.
3. Delta-doped silica: the delta-doping process requires two steps. The first step involves a sequential evaporation of silica layer, Cu layer and silica layer with a thickness of 10nm, 3nm and 5nm, respectively. This "sandwich" structure was then thermally annealed in rapid thermal annealing system (RTA) at 550°C for 10 minutes in a nitrogen ambient to thermally diffuse the sandwiched Cu layer into the surrounding silica layers. A schematic of "delta-doping" process is illustrated in Fig. II.2.2d.

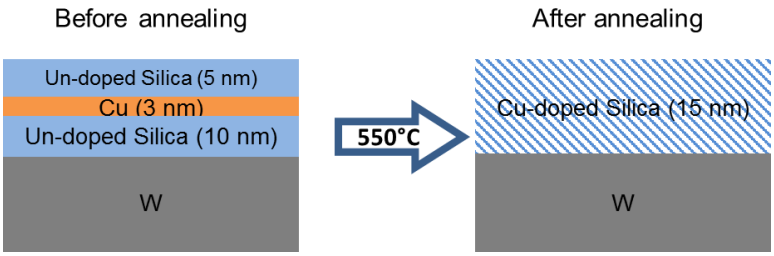


Fig. II.2.2d. Schematic of "delta-doping" process.

4. Electrode-diffusion-doped silica: different from "delta-doping", the source of copper in electrode-diffusion-doping process purely came from the Cu electrode. As shown in Fig. II.2.2e, a 100nm silica and 100nm Cu was consecutively evaporated. Then it is annealed in RTA at 500°C for 10 minutes. To protect the Cu electrode from being oxidized, either it is annealed in vacuum chamber or a thick oxide "capping" layer (not shown here) is deposited on top. It should be mentioned that the "capping layer" was removed after annealing. After thermal annealing, the silica layer has a concentration gradient of Cu with the upper part being high doped and lower part being low doped.

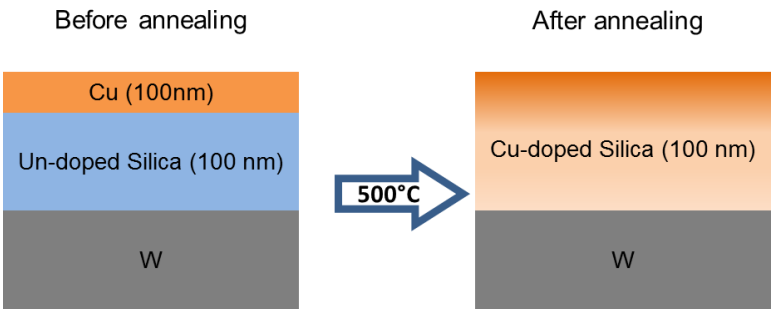


Fig. II.2.2e. Schematic of "electrode-diffusion-doping" process.

The device with different silica switching layer behaves distinctly from each other and a summary of it will be provided in next section. Fig. II.2.2f shows the device cross-section after the formation of silica switching layer.

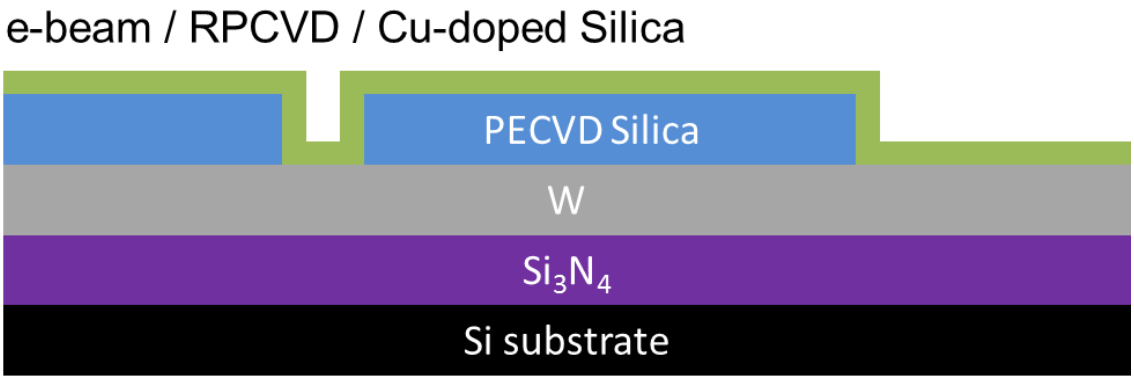


Fig. II.2.2f. Deposition of silica switching layer.

Step 5: Photolithography was performed again on top of vias to define the Cu active electrode. The photolithography detail is the same as what has been described in Step 2, except that the Mask-2 is used in this step. The resulting patterns is illustrated in Fig. II.2.2g.

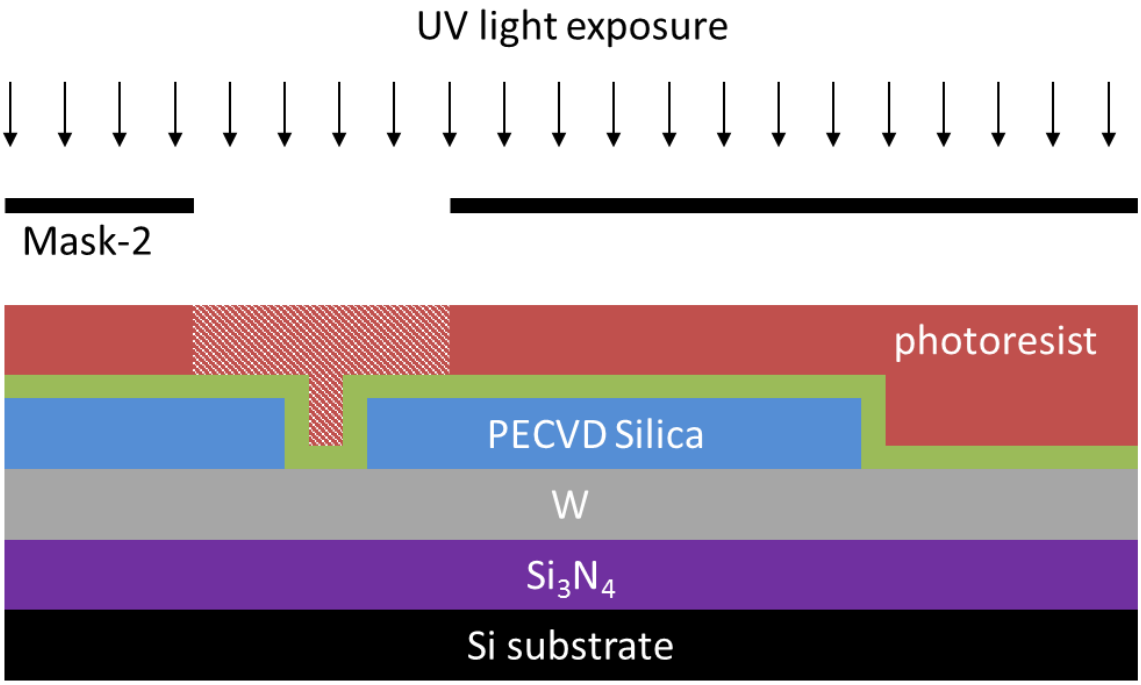


Fig. II.2.2g. Top electrode patterning.

Step 6: The patterned wafer was then transferred to a Lesker PVD75 electron beam evaporator, and 70 nm copper films were e-beam evaporated at room temperature with the holding plate rotating at 10 rpm for better film uniformity. After film evaporation, the wafer was soaked in acetone overnight to completely lift-off the unwanted metal films, the device after lift-off process is shown in Fig. II.2.2h.

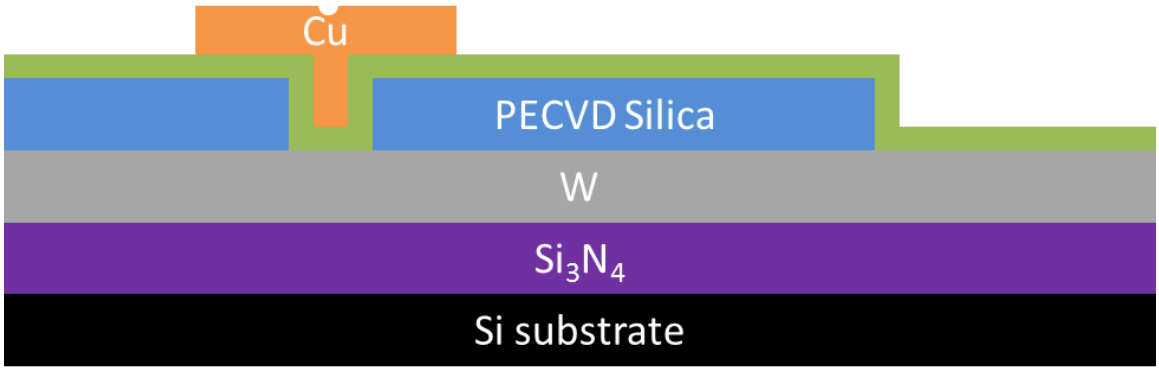


Fig. II.2.2h. PMC device with Cu top electrode after lift-off.

Step 7: Contact pad patterning. In this step, the contact is photolithographicaly patterned with the Mask-3. AZ4330 was the used here because its film thickness is higher than AZ3312, which eases the lift-off process if thick contact pad is required for low contact resistance and better wire-bonding reliability. The AZ4330 was spin-coated on the HDMS coated wafer at 2000 rpm for 30 seconds, the photoresist coated wafer was then soft-baked at 100°C for 140s to fully evaporate the solvent. The resulting photoresist has a thickness of 4.5 µm. Since it is thicker than AZ3312, a total dose of 350mJ/cm^2 is required for UV exposure. The cross-section of the developed wafer is shown in Fig. II.2.2i.

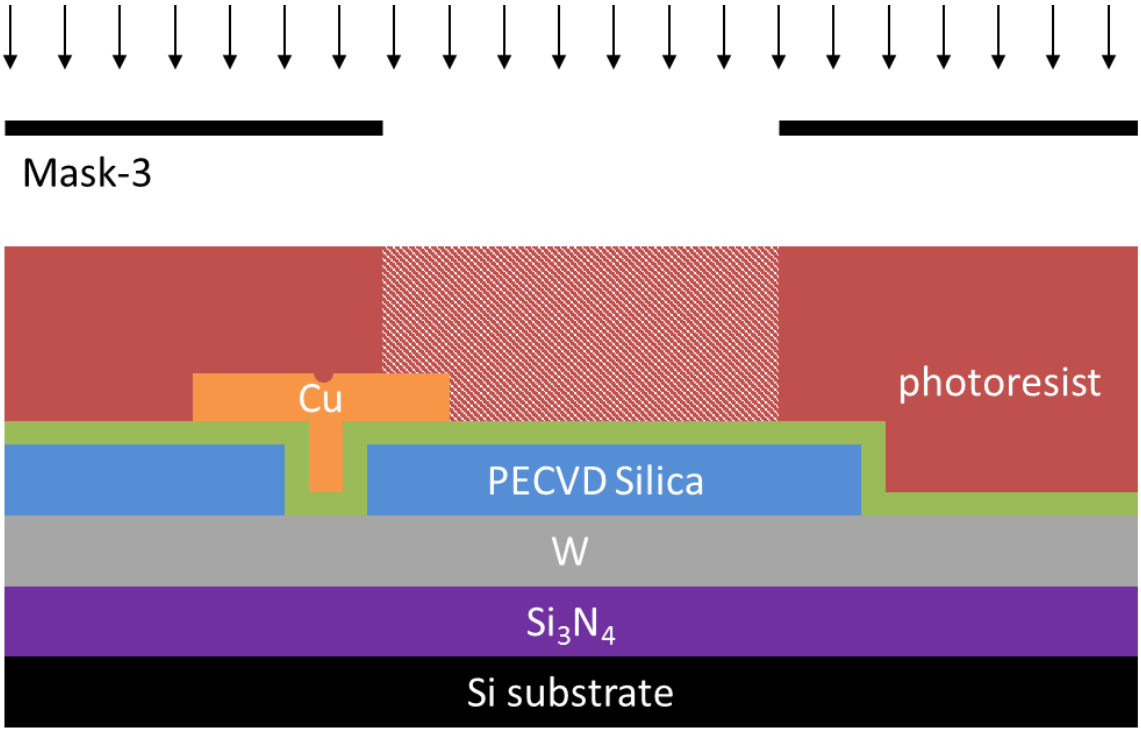


Fig. II.2.2i. Contact pad patterning.

Step 8: A thick layer (100nm – 500nm) of Cu (or Al) was e-beam evaporated and the contact was formed after a lift-off process. To complete the device fabrication, the wafer was dipped into BOE 20:1 for 3 seconds to remove the switching oxide above the W electrode. Fig. II.2.2j demonstrates the fabricated Cu-silica PMC.

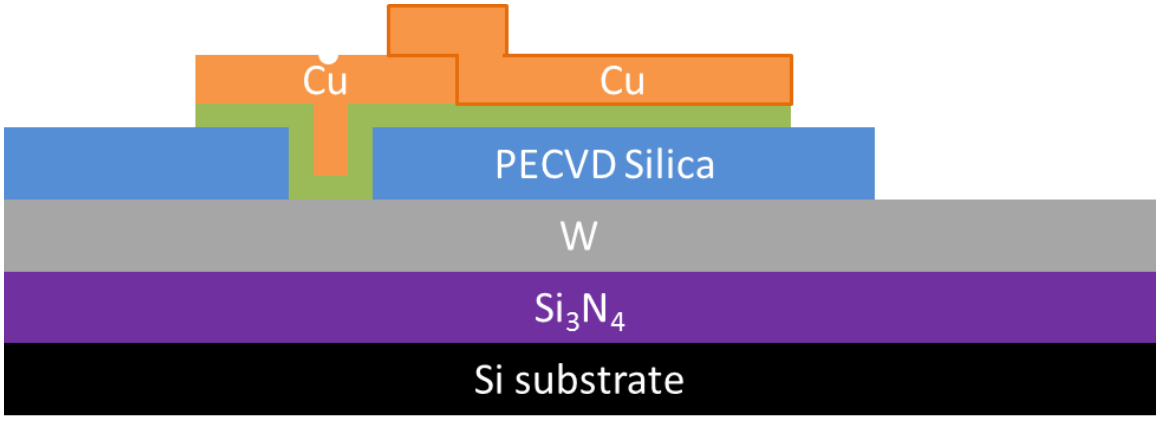


Fig. II.2.2j. The cross-section schematic of finished Cu-silica PMC.

A top-view picture of a PMC device with 5 µm via is shown in Fig. II.2.3a. This picture was captured by optical microscope. Active device region (via) is indicated by the circle in the center of the Cu electrode (upper square). Fig. II.2.3b shows a 3D illustration of the device's active region (cut along dotted line in Fig. II.2.3a). Fig. II.2.3c is the SEM cross-section image of the dotted box region in Fig. II.2.3b, the image was captured by FEI Nova 200 NanoLab after a fit cutting process.

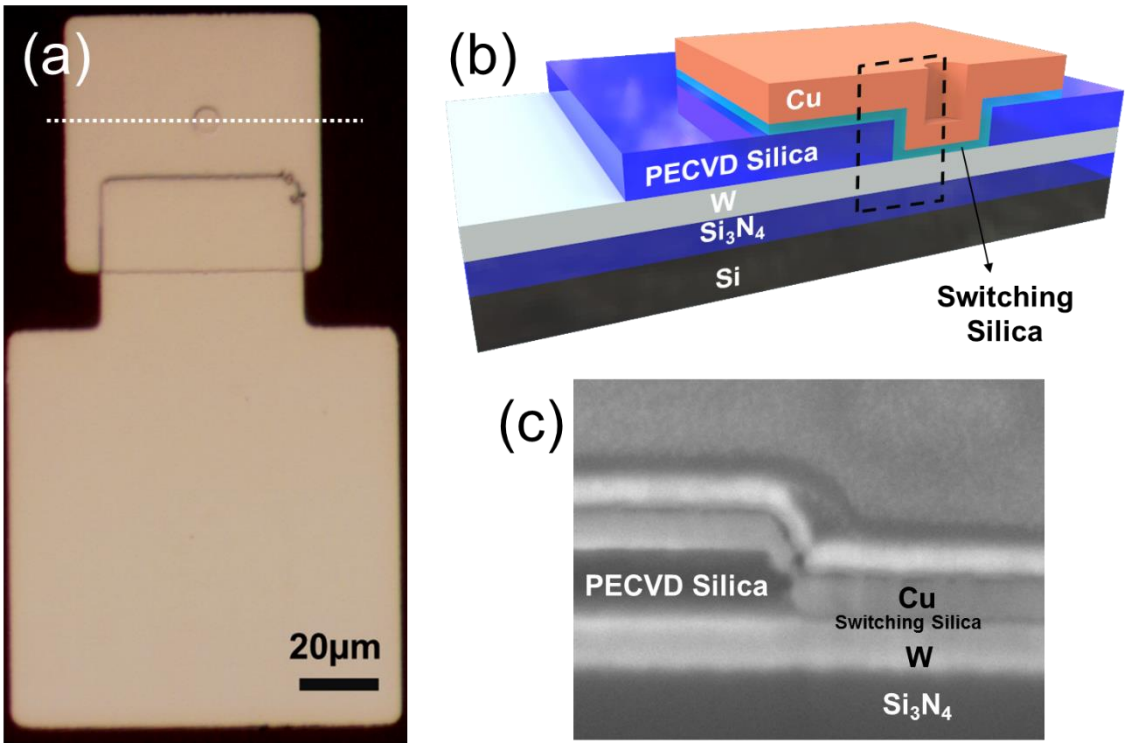


Fig. II.2.3. Image of fabricated PMC device with 5 μm via. (a) optical image of fabricated PMC device in top view. (b) 3D schematic illustration of the cross-section of fabricated PMC device. © 2015 IEEE. Reprinted with permission from Ref. [92]. (c) Cross-section SEM image of fabricated PMC device.

II.3. Memory Performance of Cu-Silica PMC

The common metrics used to evaluate the feasibility of a NVM technology are HRS/LRS ratio, multi-level capability, endurance, retention as well as programming speed. In this section, the NVM performance of Cu-silica PMC is assessed based on these metrics and the impact of nanofabrication, especially the switching layer deposition, on device performance is discussed as well.

II.3.1. DC I-V Characteristics of Cu-Silica PMC

As has been mentioned in the device fabrication section, different method has been applied to turn the property of silica switching layer. PMC devices with a variety of silica, including undoped e-beam silica, Cu-doped e-beam silica and undoped RPCVD silica, have been fabricated and characterized. The DC I-V result of these devices are illustrated below and all the devices have Cu as their active electrode.

Type 1 – undoped e-beam silica: Fig. II.3.1. demonstrates the typical DC I-V curve of PMC with a layer of 13nm undoped e-beam silica, the device was cycled for 20 times. The fingerprint property of this PMC type is the Giga-Ohm HRS resistance and the small erasing voltage. It is also notable that the device has a small HRS variation and an abrupt erasing process. The root cause of these behaviors is believed to be the porous structure of e-beam evaporated silica. The film density measured by X-ray Reflectivity (XRR) is 2.08 g/cm^3 which is 22% less dense than single crystal SiO_2 (2.65 g/cm^3). In porous silica, the reset is accelerated by a diffusion-driven self-dissolution process of Cu filament, thus, the required erasing voltage is small. In addition, the filament is dissolved thoroughly after reset since the Cu residuals are easily absorbed by the neighboring silica matrix since numerous vacant sites are presented in the porous structure. Thus, no Cu residual induced tunneling current is presented in HRS and this is the reason why the HRS distribution is tighter and the HRS resistance is larger. Note that the GΩ-range HRS resistance is particularly suitable for PMC crossbar arrays and switches in FPGA circuits, as this will reduce current leakage and standby power.

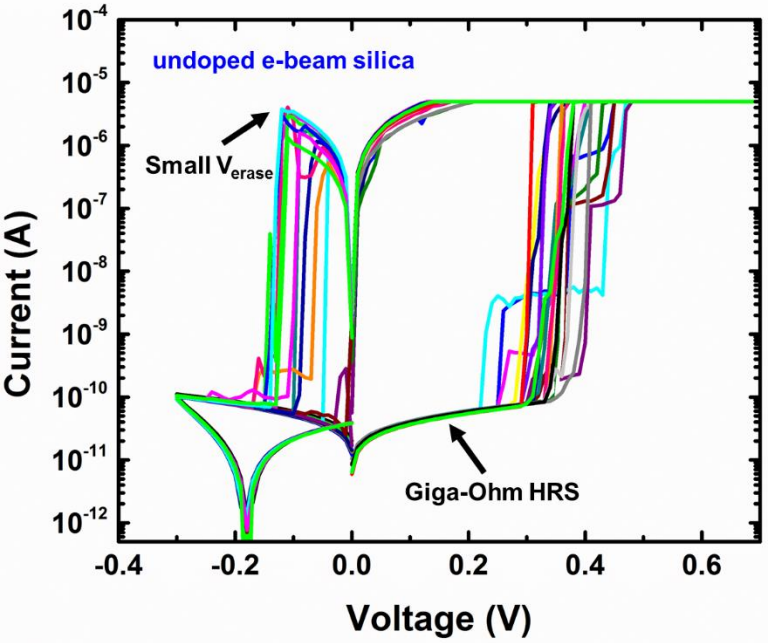


Fig. II.3.1. DC characteristics of Cu-silica PMC with undoped e-beam silica switching layer.

Since this PMC type possesses a very high HRS, the memory window (the ratio of HRS/LRS) is large and therefore the LRS can be easily differentiated from HRS even with a small programming current. Ultra-low current resistive switching is achieved with e-beam silica PMC, a 10nA resistive switching is shown in Fig. II.3.2.

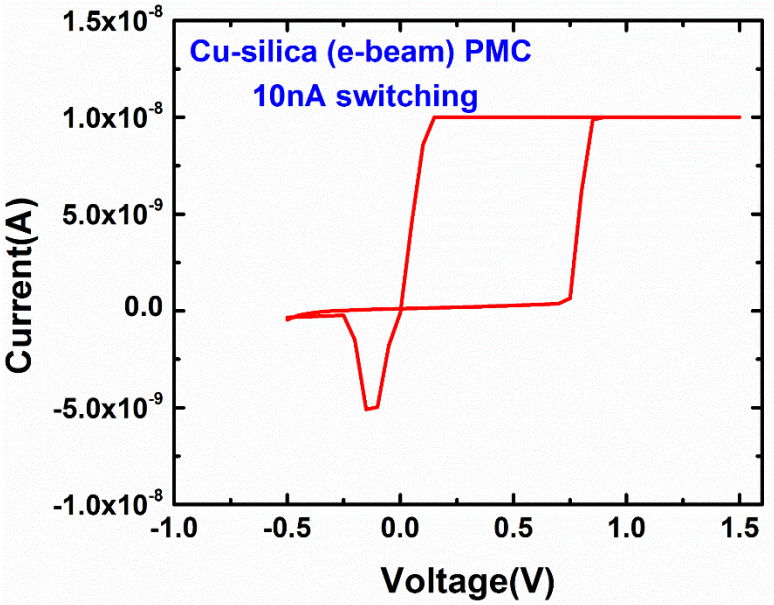


Fig. II.3.2. Resistive switching of Cu-silica (undoped e-beam) PMC at ultralow current.

Although the PMC with an undoped e-beam silica presents a favorable GΩ-HRS, the easy but abrupt reset characteristic indicates a weak filament presented in LRS, which threats the LRS memory retention. To improve the LRS retention or the stability of filament, a denser silica or Cu-doped silica is preferred.

Type 2 – undoped RPCVD silica: Compared to e-beam evaporated silica, silica deposited by RPCVD has a higher density (2.2 g/cm^3). The DC switching characteristics of PMC with a 5nm undoped RPCVD silica switching layer is plot in Fig. II.3.3. The IV curve of this PMC type significantly differs from the e-beam silica one in terms of the HRS resistance, HRS variation as well as erasing voltage. As shown in Fig. II.3.3, the filament is erased at negative voltage around - 0.7V which is higher than the e-beam silica's -0.2V, this can be due to the suppressed self-dissolution of filament in denser silica. Also, the HRS resistance of this PMC type is smaller than type-1 PMC. This is because the remaining Cu residuals after reset cannot be easily absorbed by the surrounding oxide as the number of

available vacant sites in CVD silica is less than e-beam silica. These "leftover" Cu residuals act as shortcuts for electron transport which reduces the effective thickness of silica film and lowers the HRS resistance. Moreover, the HRS current of type-2 PMC has a wider distribution than that of type-1 PMC, this can be cause by the cycle-to-cycle variation in the quantity and location of Cu residuals in silica film. Finally, the HRS current fluctuates randomly for a single switching cycle. According to the observed quantum conductance in many PMC types [113-115], this current fluctuation can be attributed to the changes in the number of single-atom contacts during DC voltage sweep. The high HRS current makes this PMC type unfavorable for ultralow power application but still the memory window is sufficiently large for normal NVM application.

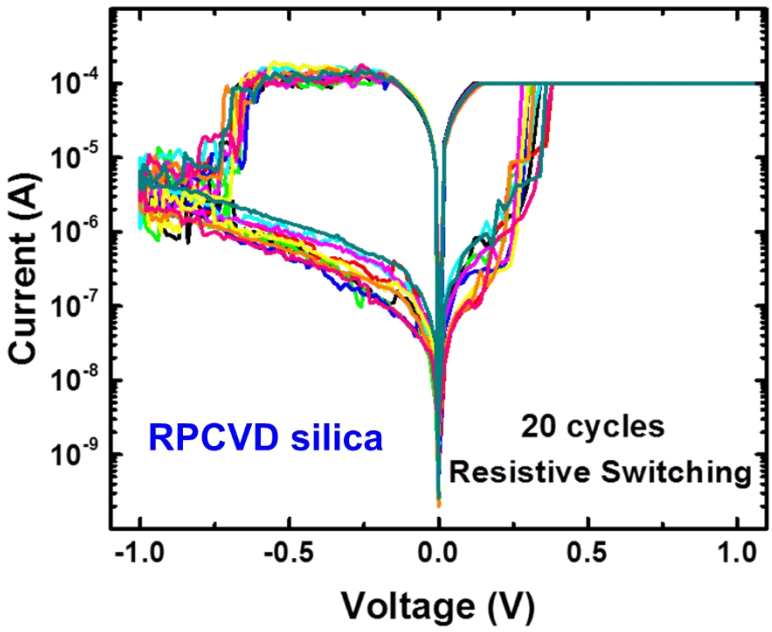


Fig. II.3.3. DC characteristics of Cu-silica PMC with undoped RPCVD silica switching layer. © 2016 IEEE. Reprinted with permission from Ref. [64].

Type 3 – Cu-doped e-beam silica (delta-doping): Besides CVD silica, Cu doping is another effective way to improve the device's LRS retention since the increased Cu concentration in silica film reduces the concentration gradient which suppresses the filament dissolution. The first doping method is delta-doping which has been described in the device fabrication section. A 15nm thick Cu-doped e-beam silica film is generated after delta-doping process and a 50-cycle IV switching curve of this PMC type is shown in Fig. II.3.4. Like type-2 PMC, a high negative voltage (1V) is required to dissolve the filament, this large reset voltage indicates a stable filament. Also, because of the existence of Cu residuals after the device being erased, the current distribution of HRS is wide and the current fluctuation is every cycle is big (indicated by the black line in Fig. II.3.4). It is hard to achieve complete reset simply by increase the erasing voltage, this is because the device will be unintentionally turned on at a large negative voltage, a detail explanation is presented in our previous work [59]. Thus, other method must be developed to reduce the HRS variation.

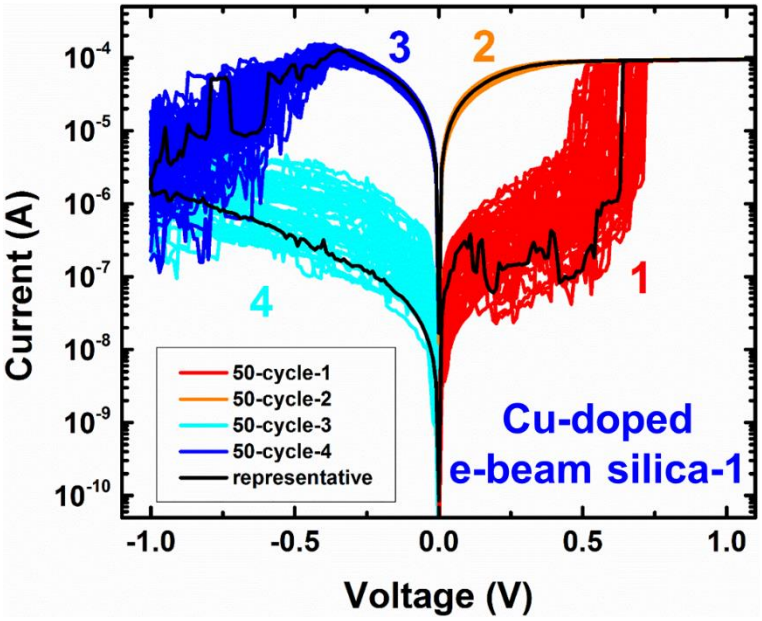


Fig. II.3.4. DC characteristics of Cu-Cu:silica PMC with a delta-doped silica. © 2016 IEEE. Reprinted with permission from Ref. [116].

Type 4 – Cu-doped e-beam silica (Electrode-diffusion-doped silica): An important reason for HRS variation is the stochastic nature in the quantity and distribution of Cu residuals in post reset silica. If the cluster size is comparable to the thickness of silica film, they are going to contribute to the electron conduction, however, the Cu residual induced tunneling current can be significantly reduced if the silica film is thick. Therefore, a thicker film should be helpful in eliminating the IV curve variation in HRS. A 100nm thick e-beam silica was doped by Cu with the second doping method in the device fabrication section. In this doping process, the Cu is thermally driven from Cu top electrode into the silica film. As shown in Fig. II.3.5, not only the "large" reset voltage is preserved, but the HRS variation is dramatically reduced. The large reset voltage suggests that a stable filament is generated after programming, and the small IV curve variation of HRS proves that the Cu cluster residuals is much smaller than 100nm. In summary, considering filament stability and cycle-to-cycle variation, the Cu-silica PMC device fabricated in this method demonstrates the best overall DC switching performance.

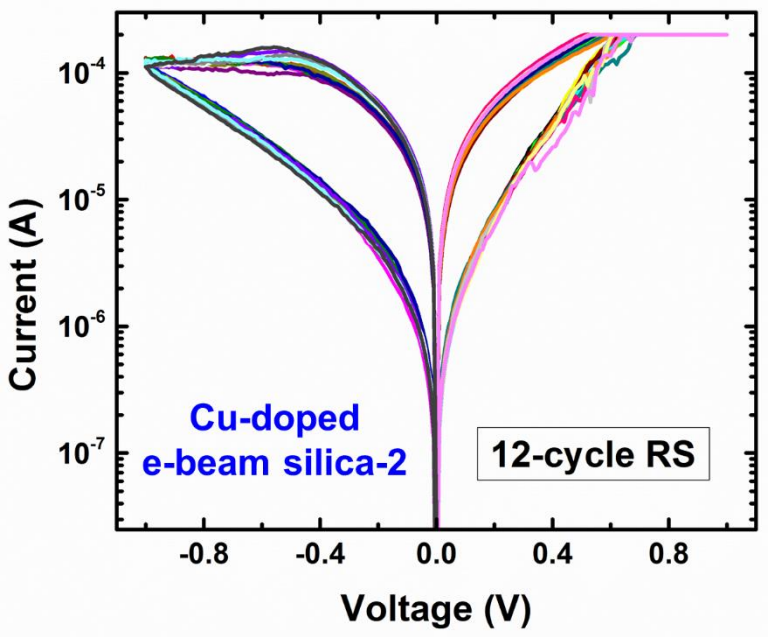


Fig. II.3.5. DC characteristics of Cu-Cu:silica PMC with an electrode-diffusion-doped silica [62].

II.3.2. Multilevel Programming of Cu-Silica PMC

In addition to be switched between two resistance states, the Cu-silica PMC can be also switched at multiple resistance states. In multi-level switching, the LRS resistance can be modulated by the programming current during the set operation. In general, the larger the programming current, the smaller the LRS resistance. Due to the high HRS resistance in undoped e-beam silica based PMC, it possesses a big memory window which allows a wider range of programmed LRS than other PMC types. Thus, this PMC type is particularly investigated for multilevel programming. Fig. II.3.6a shows the DC multilevel switching curves of undoped Cu-silica PMC, the small reset voltage and large HRS resistance behavior is valid for device being programmed at all current. The LRS resistance vs. programming current result is plot in Fig. II.3.6b in which three 10 µm devices were

switched for 10 cycles for every programming current. All resistance values were read out at 100 mV. It can be observed from Fig. II.3.6b that LRS resistance decreases monotonically with the increasing of programming current following the power law

$$LRS = A/I_{prog}^{n}$$

where *A* is a constant with a unit of voltage and *n* is a dimensionless number close to 1.

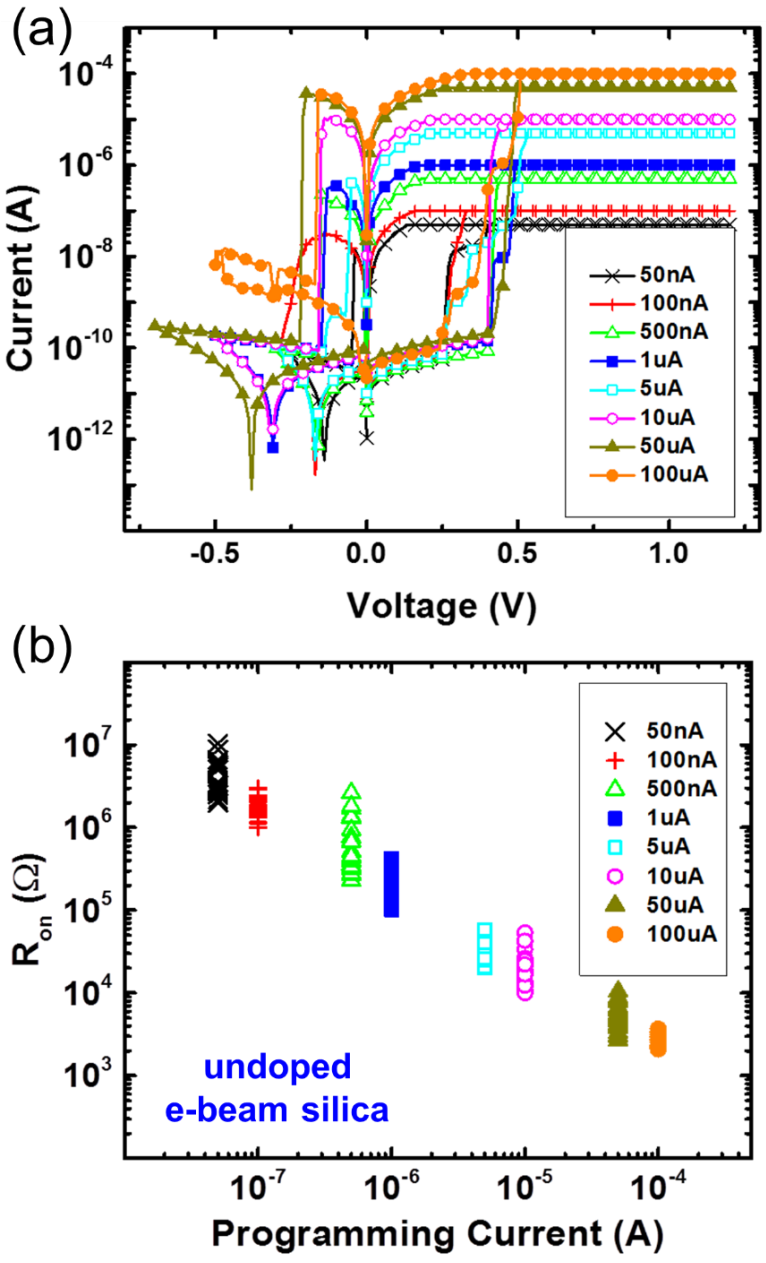


Fig. II.3.6. Multilevel programming in PMC with undoped e-beam silica film as switching layer. © 2015 IEEE. Reprinted with permission from Ref. [92].

In recent years, several mechanisms have been proposed to explain the multilevel switching phenomenon. In general, two regimes can be separated at a resistance of approximately 13 kΩ. This is because 13 kΩ is the maximum resistance before the break of a metal-metal contact, i.e., the resistance of a single atom point contact [117]. With a resistance lower than 13 kΩ, the change of resistance can be explained by lateral filament growth or increase of filaments quantity. For higher programming current, more cations are produced and electrodeposited, resulting in either a thicker filament or more number of small filaments, thus more quantum point contacts (QPC) are made between filament(s) and metal electrode. The quantized atomic point contact phenomenon has been found in silica based PMC [118], in which integer multiples of fundamental conductance ($G_0 = 2e^2 h^{-1}$ which is approximately 1/12.9 kΩ) were observed. On the other hand, there would be no complete bridging of the electrodes by filament(s) when the resistance is greater than 13 kΩ. The resistance change in this regime could be due to the modulation of tunneling gap between the filament(s) tip and the electrode [119] and/or the adjustment of width of QPC like constriction region [120].

Multilevel programming capability is a critical feature for silica based PMC as it enables multibit data storage in single cells, thereby dramatically increasing data storage density.

II.3.3. Retention of Cu-Silica PMC

Retention defines how long the stored information is maintained in a memory cell before a read error occurs. In Flash memory, retention failure is usually due to the loss of electrons from the floating gate [121]. As for PMC, the information stores in a form of physical filament which exists only in LRS, thus, the retention of LRS is more of an issue than that of HRS [48]. The retention of LRS is associated with the filament stability which can be largely affected by diffusion process. In addition to diffusion, an absorption of moisture in the silica also threats the LRS reliability. Recent cyclic voltammetry (CV) studies show that an electromotive force (emf) exists in the presence of moisture in the silica switching layer [95], and such emf generates an additional voltage which oxidizes the metallic filament and thereby deteriorates LRS retention [122]. Therefore, either a strong filament or a suppressed self-dissolution, or both, would be helpful in improving the LRS retention.

Fig. II.3.7 demonstrates the high temperature stability of a strong filament. Such strong filament is created by hardly programming a type-1 PMC device by voltage pulse with large amplitude and long duration (3V 400μs). As shown in this figure, both HRS and LRS was maintained after ten thousand seconds at 85 °C. This result proves that, even for undoped porous silica, the LRS retention can be dramatically enhanced if the formed filament is strong enough. Also, the high HRS resistance doesn't degrades at high temperature which suggests that negligible amount of Cu was diffused from active electrode into the porous silica, thus, the biggest advantage of type-1 PMC is preserved at high temperature.

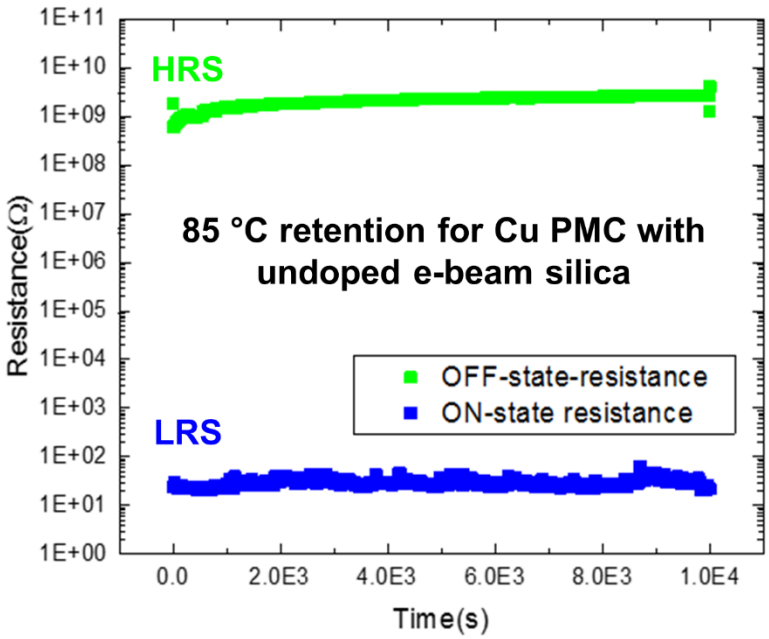


Fig. II.3.7. Retention of type 1 Cu-silica PMC.

Usually, the endurance of PMC device will be sacrificed if it is programmed too hard (will be discussed in next section), so improving retention by forming strong filament is not the best solution. As mentioned above, thermal doping of silica film is another way to improve the LRS retention. The LRS retention characteristics of the type-3 PMC was assessed and the results are shown in Fig. II.3.8. The device was switched to three different LRS, i.e. 3 kΩ, 4 kΩ and 9 kΩ. When programming the PMC to LRS, the device can be repeatedly cycled for many times. The resistance of each device was sampled for 1.2×10^4 seconds at room temperature. During the testing, 100 mV read voltage was applied for every 10 seconds. Although some fluctuations were observed for the largest LRS, a clear separation among them was preserved throughout the test. Fig. II.3.8 demonstrates that the LRS is stable for a range of LRS, which suggests that delta doping process can be used to achieve good LRS stability.

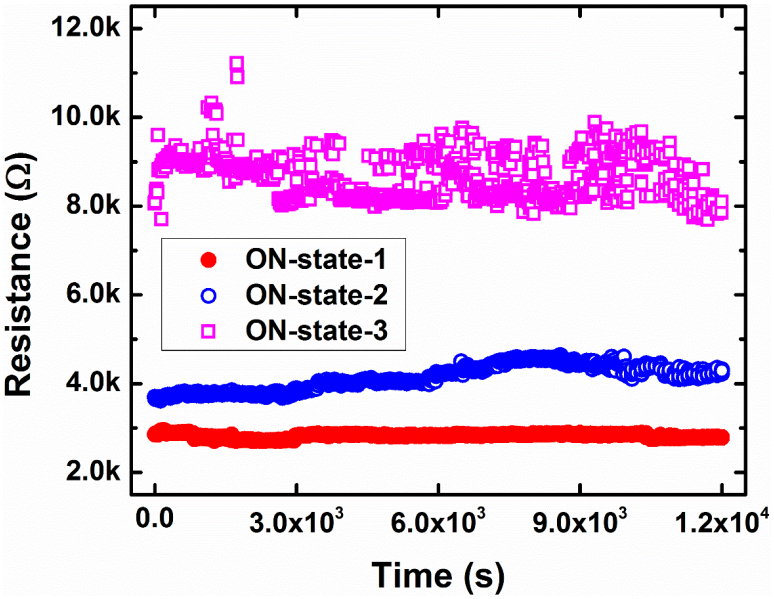


Fig. II.3.8. Retention of type 3 Cu-silica PMC. © 2016 IEEE. Reprinted with permission from Ref. [116].

The retention of type-4 PMC was also investigated. Fig. II.3.9 shows the room temperature retention of this PMC type at different resistance states ranging from 5 kΩ to 40 kΩ. The resistance states are programmed using voltage sweeps and are measured at room temperature with a 640 μs 50 mV voltage pulse at every 10 s. The resistance states are pretty stable over a 1000-second test duration. The faster degradation in the smallest programmed resistance state (blue stars) indicates that the 100nm silica film was not doped thoroughly, the Cu concentration is low at the region close to the inert electrode. Thus, in a very low resistance state, the filament extended into this low doping region where its stability is compromised.

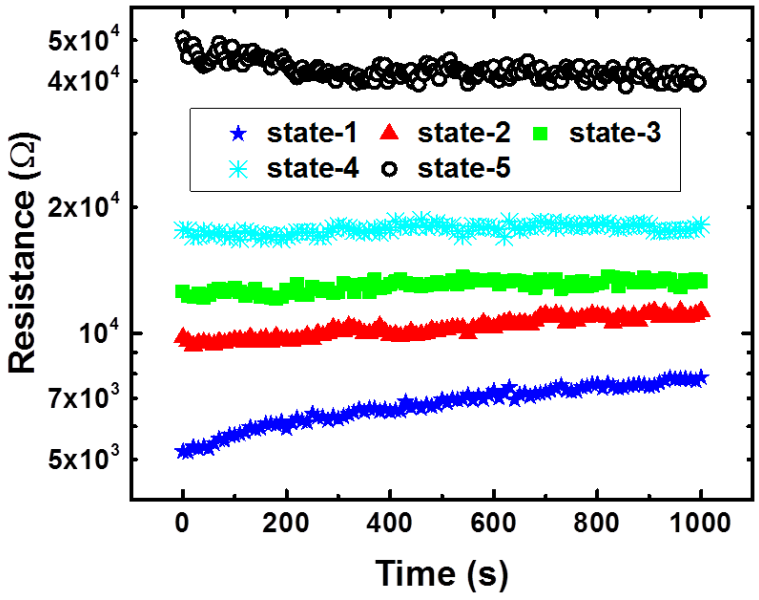


Fig. II.3.9. Retention of type 4 Cu-silica PMC [62].

II.3.4. Endurance of Cu-Silica PMC

Endurance is determined by how many write-erase cycles a memory cell can perform before failure (stuck bits) occurs. Endurance is associated to programming energy and better endurance is generally achieved when the device is programmed with smaller energy, i.e. lower programing currents and shorter voltage pulses. Endurance is also influenced by the test setup, the transient current spike, which usually arises from circuit parasitic, during programming can potentially damage a memory cell in a significant way [31, 123, 124].

Fig. II.3.10 shows the endurance characterization of type-1 PMC. DC test result is shown in Fig. II.3.10a, the HRS and LRS value is extracted at positive 100mV of each voltage sweep and the programming current was limited at 10 uA. More than 400 cycles of DC switching was achieved. It should be noted that the HRS resistance is in GΩ-range

for the first 300 cycles which is typical for type-1 PMC, however, it started to decrease to a range of several kΩ at the end of cycling test. This HRS degradation is attribute to the gradual saturation of Cu atoms in the porous silica around the filament, which greatly reduces its absorbability. Thus, the Cu residuals cannot be dissolved thoroughly and they start to contribute to the HRS conduction. However, the LRS is distributed more tightly across the entire endurance test.

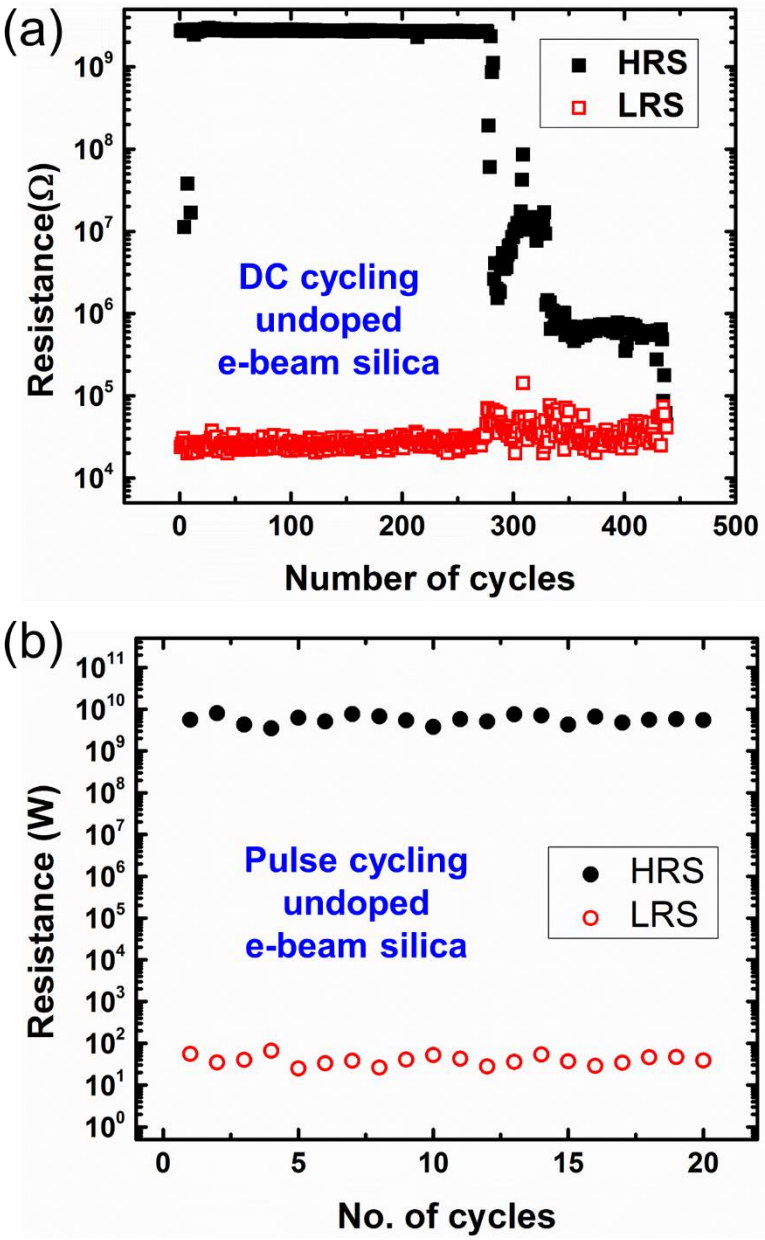


Fig. II.3.10. Endurance of type 1 Cu-silica PMC. (a) cycling with DC sweep, and the resistance value is extracted at 100mV, (b) cycling with 3.5V 1ms pulse.

Since the retention of hard programmed type-1 PMC is excellent, the endurance of this PMC type when switched by large electrical pulses was also assessed, the result is shown in Fig. II.3.10b. The device was programmed by 10ms 4V pulse and was erased by 1us -4V pulse. Only 20 switching cycles was achieved and then the device was stuck at HRS. The failure mechanism was analyzed by electron microscopy. Fig. II.3.11a shows the SEM image captured after a type-1 PMC was hard switched for 4 cycles. Four blown-off regions were generated compared to the device prior to testing, the blown-off regions were due to the joule heating generated by the high current during the reset process, the estimated electron current for a 40 Ω filament at 4V is 100 mA and the filament was completely fused by such current. Interestingly, the multiple blown-off region indicates that the resistive switching didn't occur at the same location, a new filament was randomly created for the following pulse programming. The device was further analyzed by FIB and was cut along the dash line in Fig.II.3.11a where two blown-off regions were existed. The overall cross-section SEM image is shown in Fig. II.3.11b, and the zoomed-in images of two blown-off regions are illustrated in Fig. II.3.11c and d, respectively. It can be seen that the top Cu electrodes above the blown-off regions were gone, and based on the explosion area, the filament size can be estimated to be less than ~50 nm. Finally, because of the amount of energy dumped into the device was gigantic, not only the filament was blown off, the surrounding region was also distorted which causes a physical delamination

between the silica film and the metal electrode. This explains why the device was stuck at HRS and cannot be further programmed.

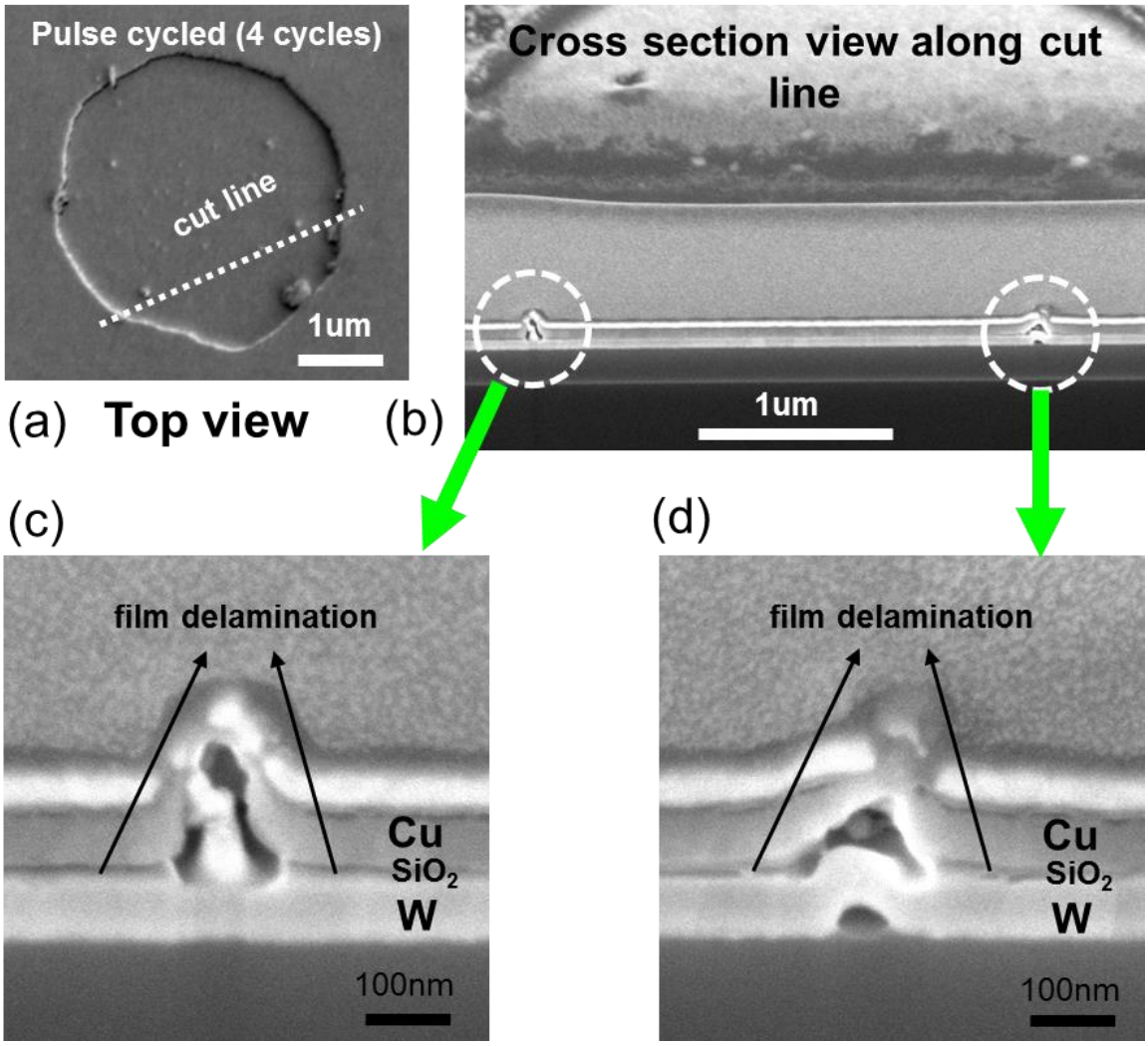


Fig.II.3.11. SEM and focused ion beam (FIB) analysis of the failure mechanism of pulsed type 1 Cu-silica PMC.

The endurance of type 2 PMC was also assessed. Fig. II.3.12 plots the HRS and LRS resistance extracted from 400 consecutive switching cycles with 10 mV read voltage. Unlike the tightly distributed LRS, the HRS resistance fluctuated during the DC cycling. As has been discussed in previous section, the fluctuation is attributed to the stochastic

nature of Cu residual after reset process. Nevertheless, a memory window with a factor of 10 was still achieved for this PMC type.

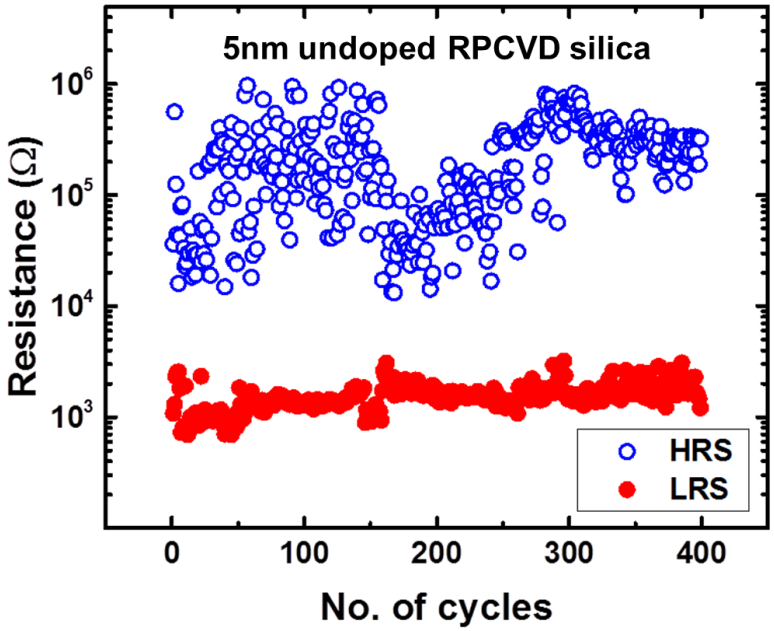


Fig. II.3.12. Endurance of type 2 Cu-silica PMC. © 2016 IEEE. Reprinted with permission from Ref. [64].

Furthermore, the endurance of type-4 PMC was evaluated and the result is demonstrated in Fig. II.3.13. In the endurance test, the device was programmed/erased by 10 us, ±1.2 V electrical pulses. Note that the pulse used here is much smaller and shorter than that used to program type-1 PMC. This is because this PMC type doesn't have to be hard programmed to achieve good retention. The device can be switched on and off for more than eight hundred cycles and both HRS and LRS was tightly distributed.

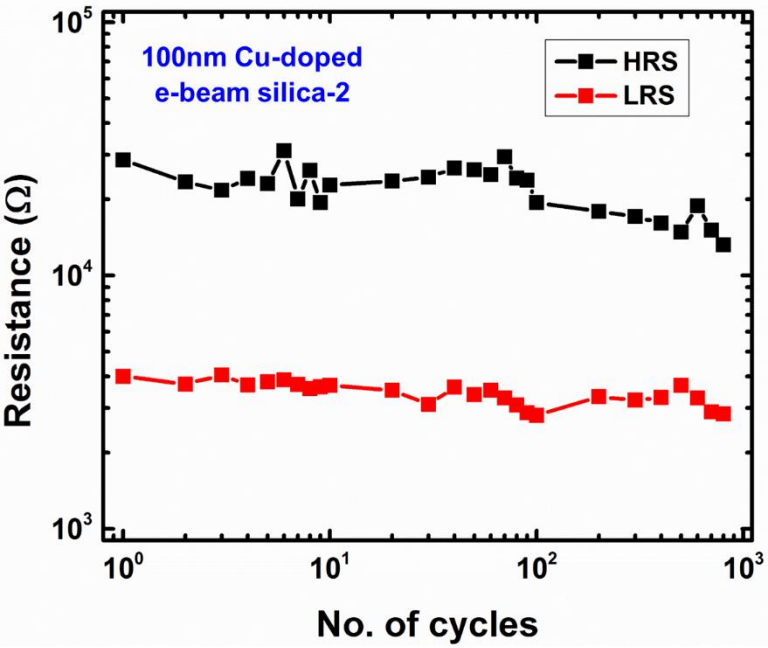


Fig. II.3.13. Endurance of type 4 Cu-silica PMC [62]. © IOP Publishing. Reproduced with permission. All rights reserved.

In summary, for type-1 Cu-silica PMC, it is unlikely to achieve both good retention and good endurance. If the device is programmed by DC sweep with small programming current, the endurance is good but the retention is bad, on the contrary, if the device is programmed by large electrical pulses, the retention is good but the endurance is bad. This endurance-retention dilemma is resolved by changing the property of the switching silica, both denser CVD silica and Cu-doped PVD silica show promising memory performance.

II.3.5. Speed of Cu-Silica PMC

The important driven force for the research and development Cu-silica PMC is the undesirable slow programming and high operating voltage of Flash memories. The speed of Cu-silica PMC is a critical metric which determines whether it the technology can

replace Flash or not. The speed testing was done on as-fabricated PMC with both Cu-doped and undoped e-beam silica, the results indicates how fast the device can be electroformed, the electroforming speed is especially important since it is the slowest process in device operation.

Fig. II.3.14 illustrates the circuit for speed test. The input signal is connected to an arbitrary waveform generator which generates the programming voltage pulses, the output is connected to a digital oscilloscope which captures the output voltage waveform coming out from the operation amplifier. The operation amplifier is configured in negative feedback mode with the positive input being grounded. The negative input is tied to a serially connected PMC-resistor(1 kΩ) combination, and a 2 kΩ resistor is inserted between the op amp's negative input and output to complete the feedback loop. With this configuration, the subtle changes in PMC resistance can be amplified based on the equation:

$$V_{OUT} = 2000 * \frac{V_{IN}}{R_{PMC} + 1000}$$

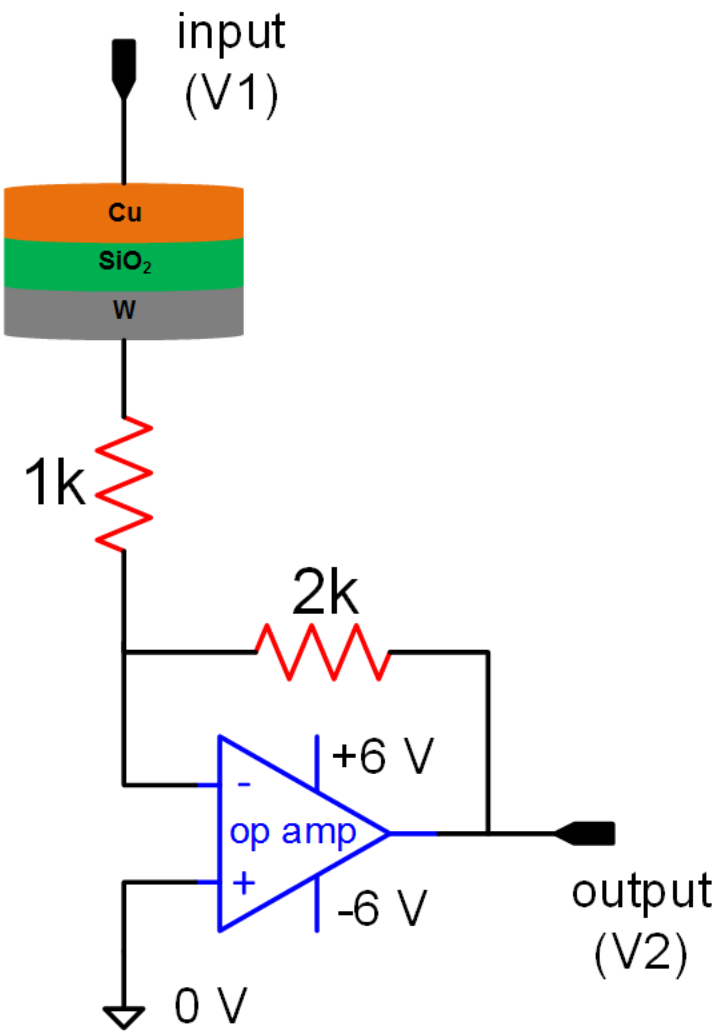


Fig. II.3.14. Schematic of the circuit used for Cu-silica PMC speed measurement.

Fig. II.3.15 demonstrates a typical electroforming waveform from this circuit setup, the input pulse (black curve) has an amplitude of 2.8V and a width of 10μs, the sudden jump of output pulse (red curve) indicates the electroforming and the time when the voltage jumped is recorded as electroforming time.

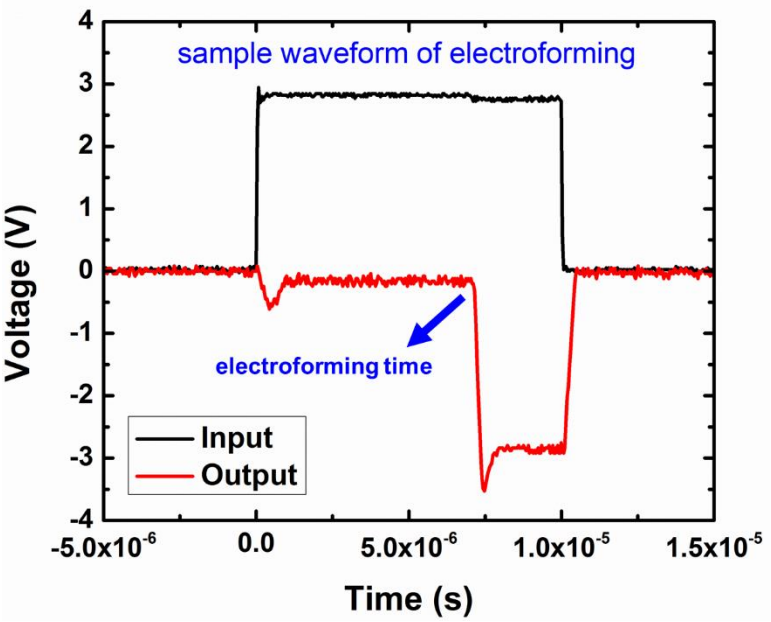


Fig. II.3.15. Typical electroforming waveform captured by digital oscilloscope.

20 devices were tested and the electroforming time is summarized in Fig. II.3.16. In general, the higher the voltage the shorter time it takes to form the device, and this voltage-time relationship can be well fitted by an exponential equation which is shown in the inset of II.3.16. This exponential voltage-time relationship originates from the nature of electrochemical reaction and ion transportation [8] within the silica layer. Extrapolated from this equation, a sub-10ns forming can be achieved at 6 V. This results indicates that Cu-silica PMC can be programmed much faster than Flash memory with a lower supply voltage.

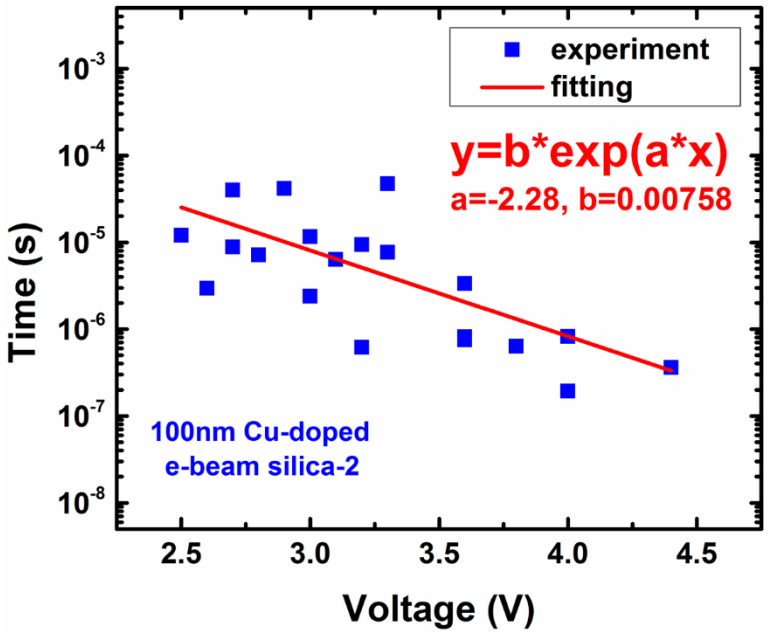


Fig. II.3.16. Electroforming speed of type 4 Cu-silica PMC.

The electroforming speed of PMC with an undoped e-beam silica layer was also characterized and the result is shown in Fig. II.3.17 [107]. Again, the time and voltage are exponentially related. Two different voltage-time region with different slope were found and they are fitted with different physical model. When the voltage is higher than 1 V, the switching speed is found to be limited by charge transfer; when the voltage is smaller than 0.5 V, the switching speed is found to be nucleation limited.

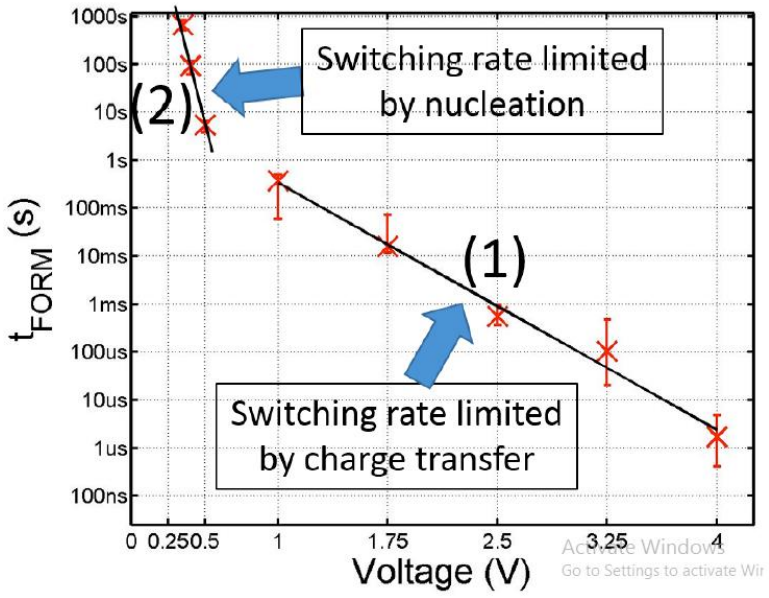


Fig. II.3.17. Electroforming speed of type 1 Cu-silica PMC. © 2015 Reprint with permission from [107].

II.4. Total-Ionizing-Dose Effects on Cu-Silica PMC

II.4.1. Total-Ionizing-Dose Effects on Modern Electronics

Energetic particles, such as photons, electrons and protons, generate electron-hole pairs (ehps) when striking at solid-state materials. This effect causes total ionizing dose (TID) damage [125] which may degrade the performance of electronic devices over time. TID generally leads to excess charged defects/traps buildup in dielectrics, electrons tend to escape from these defects/traps through a trap assisted tunneling effect. As a result, conventional charge-storage based NVMs, such as Flash and EEPROM, are not desirable for medical or space-exploration rated electronics which are commonly exposed at abnormal ionizing radiation environment [126]. Therefore, finding radiation tolerant NVM is critical to improve the reliability and extend the service life of special electronics.

Owing to the fact that the operation of resistive switching memory is based on physical filament, it possesses better ionizing radiation immunity than charge-storage based NVMs. Extensive studies have been performed to assess the TID tolerance of resistive switching memories including cation based PMC [106, 127-129] and anion based OxRAM [130-133]. A comprehensive study of TID response of Cu-silica based PMC is presented in this section. TID effects on the resistance stability of silica based PMC and $Ge_{30}Se_{70}$ based PMC are also compared in this section. The investigated PMC devices are illustrated in Fig. II.4.1.

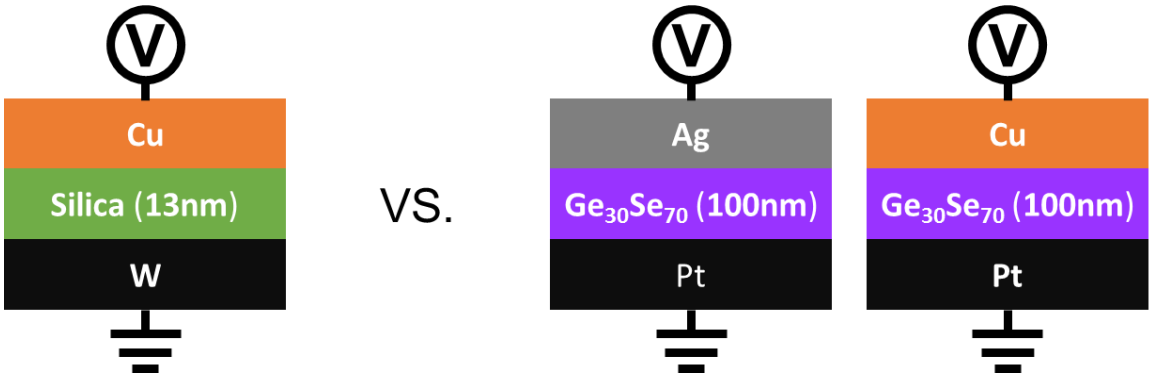


Fig. II.4.1. Schematics of gamma-ray irradiated PMC device.

II.4.2. Gamma-Ray Irradiation Experiments

The details of device fabrication have been covered in section II.2. In this work, electron beam evaporated silica and thermal evaporated $Ge_{30}Se_{70}$ was selected for PMC's switching layer, with a film thickness of 13 nm and 100 nm, respectively. The cross-section TEM image of the Cu-silica PMC is shown in Fig. II.4.2.

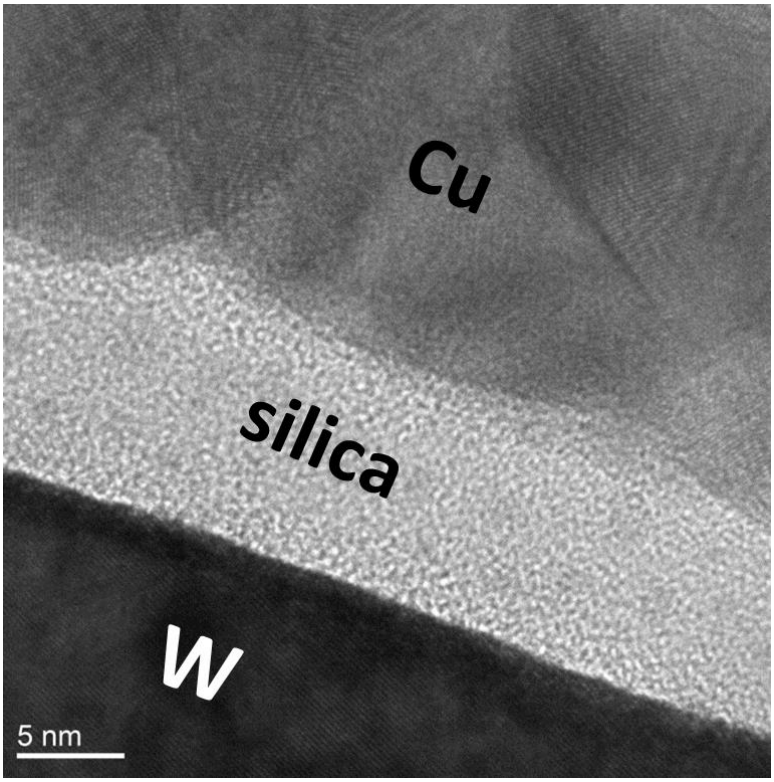


Fig 4.2. TEM bright-field image of the Cu-silica PMC (this picture was captured with JEOL 2000FX HR-TEM). © 2015 IEEE. Reprinted with permission from Ref. [92].

Several dies were put into a Gammacell 220 irradiator. They were exposed to ^{60}Co gamma-rays at a dose rate of 511 rad(silica)/min with all electrodes left floating, the radiation experiment setup is shown in Fig. II.4.3. In order to evaluate the evolution of resistive switching properties with dose level, silica and $Ge_{30}Se_{70}$ devices were step-stressed to a maximum TID of 7.1 Mrad(silica) and 4.36Mrad(GeSe), respectively. Electrical characterization was performed at each dose level shortly after being taken out of the radiation chamber. PMCs were DC characterized on a probe station with an Agilent 4156C semiconductor parameter analyzer.

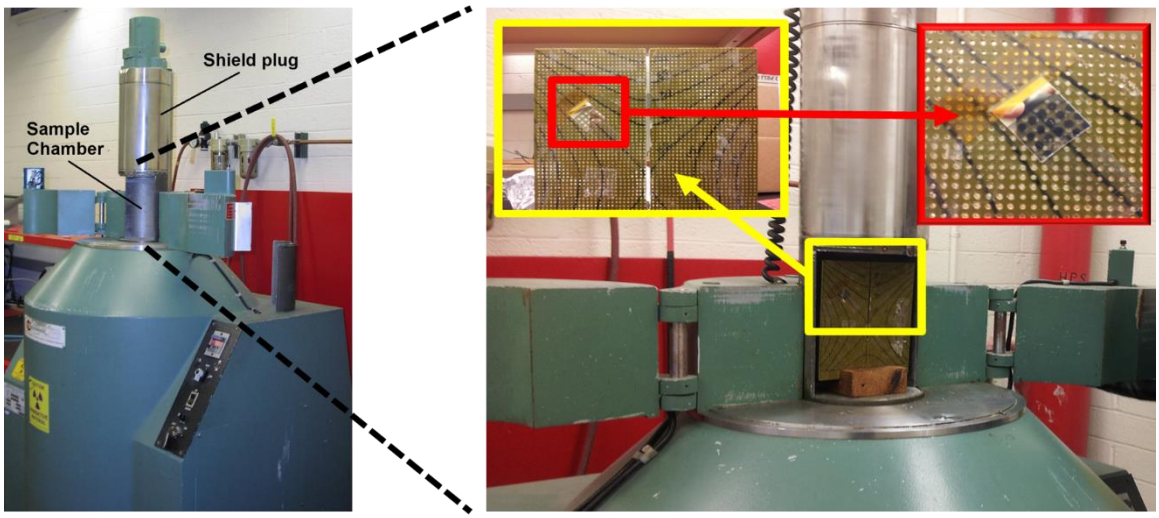


Fig. II.4.3. Experimental setup for gamma-ray irradiation.

II.4.3. Gamma-Ray Irradiation Results

Prior to irradiation experiment, PMC devices were DC tested to ensure the resistive switching functionality. Typical DC switching curves of these devices are shown in Fig. II.4.4. As can be seen, silica device has similar I-V characteristics compared to $Ge_{30}Se_{70}$ device but with much higher HRS resistance.

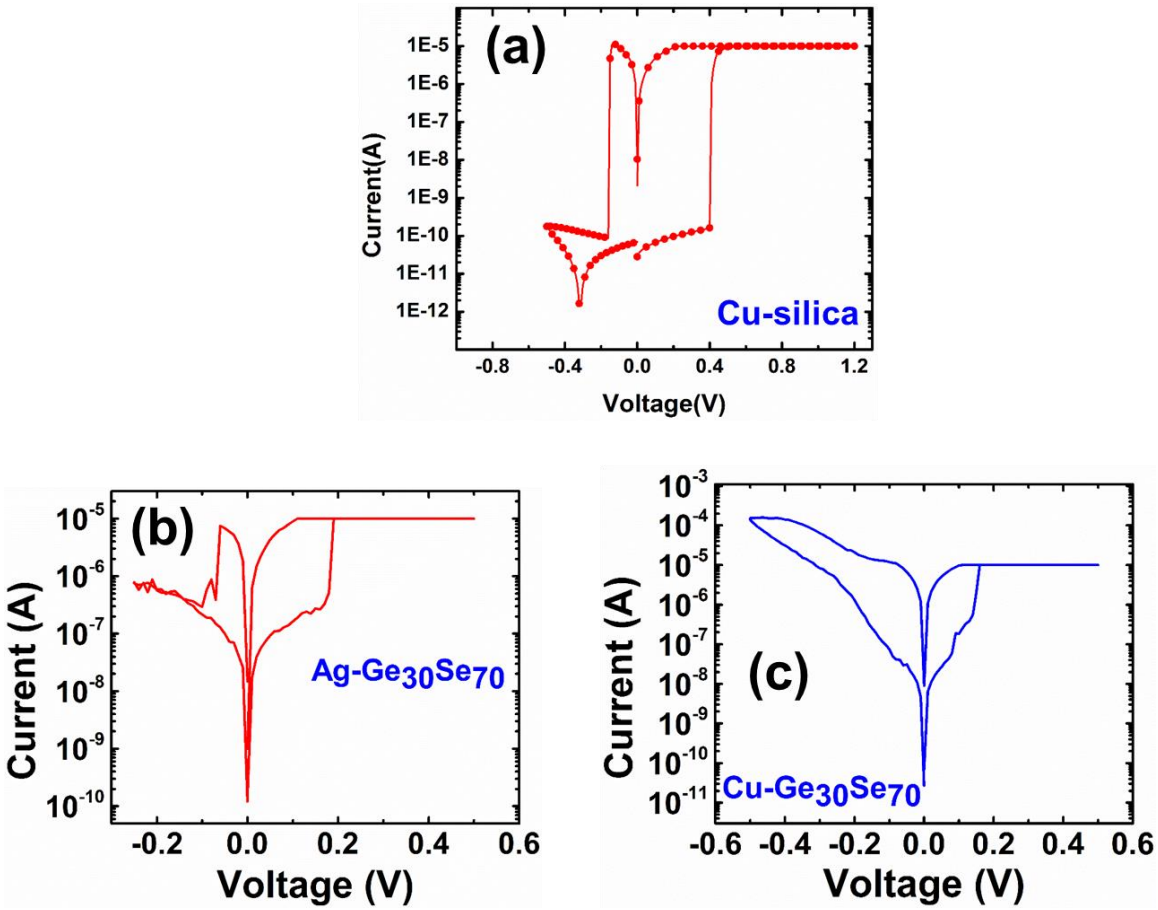


Fig. II.4.4. Resistive switching (DC) of PMC with a silica or $Ge_{30}Se_{70}$ switching layer.

II.4.3.1. TID Effects on Virgin-State Resistance

Virgin-state resistance is defined as the resistance of a PMC prior to any switching event. Fig. II.4.5 shows the resistance value of virgin Cu-silica PMCs before and after different levels of ionizing dose. Devices with 10 µm and 100 µm size are investigated to find if area impacts the radiation response, which it does not. For each size, three devices were measured before and after each dose step. The read voltage is 100 mV to avoid electroforming and unintentional incorporation of Cu ions. The data indicate that there are no significant shifts in virgin resistance caused by TID exposure.

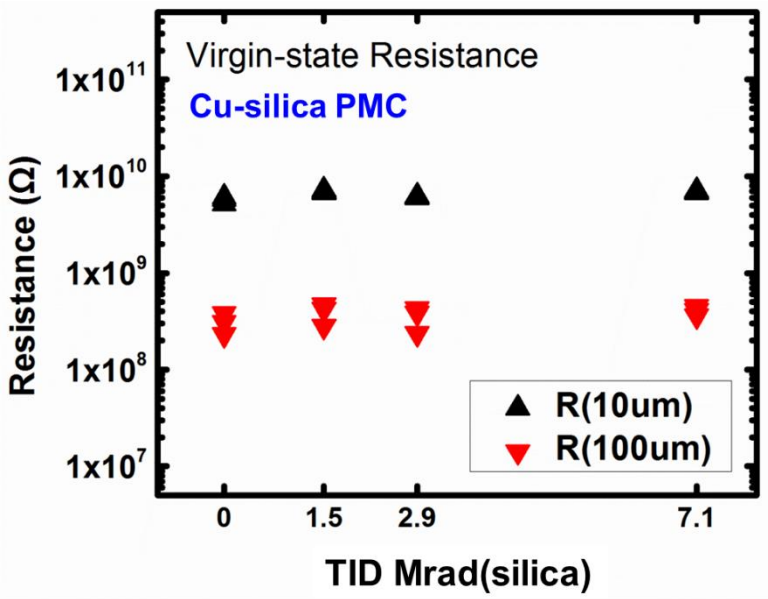


Fig. II.4.5. Resistance of virgin Cu-silica PMC with 10 µm and 100 µm at different TID levels.

Fig. II.4.6 demonstrates the virgin-state resistance evolution during gamma-ray exposure for two $Ge_{30}Se_{70}$ PMC types. Three 5 µm diameter devices for each type of PMC were tracked and the results are shown in Fig. II.4.6, normalized to the virgin HRS resistance prior to irradiation. Note that the virgin-state resistance of $Ge_{30}Se_{70}$ PMCs decreased almost three orders of magnitude after exposure. This result is consistent with what has been reported on Ag-ChG radiation sensors [134]. The reduction of virgin-state resistance is attributed to radiation-induced doping of Ag or Cu into the chalcogenide glasses. It should be noted that the Cu-ChG PMCs exhibited less change in resistance than the Ag-ChG PMC, which indicates that copper might be a better material choice for PMCs when used in ionizing radiation environment.

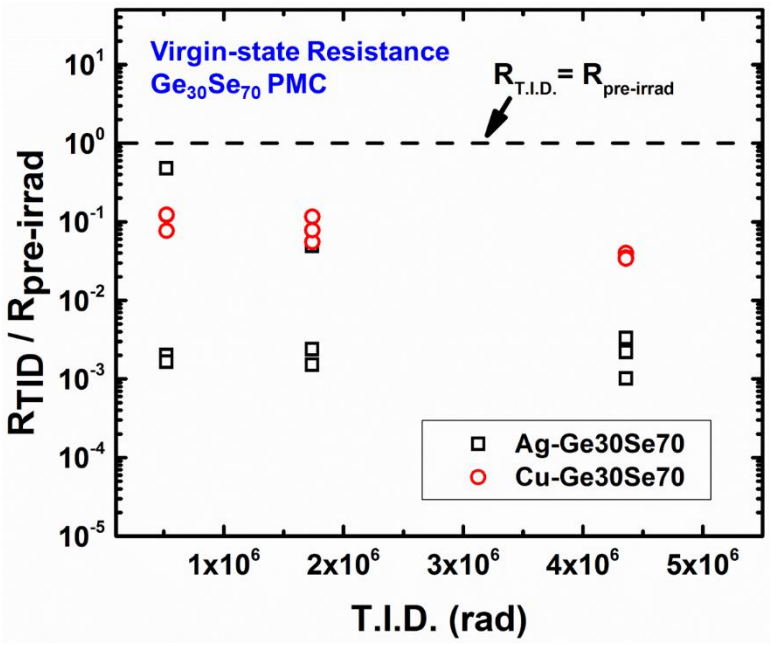


Fig. II.4.6. Effects of TID on virgin-state resistance of two PMCs – Cu-$Ge_{30}Se_{70}$ (empty circles) and Ag-$Ge_{30}Se_{70}$ (empty squares). © 2017 IEEE. Reprinted with permission from Ref. [88].

II.4.3.2. TID Effects on HRS and LRS Resistance

Ionizing radiation effects on the LRS and HRS of silica and $Ge_{30}Se_{70}$ PMCs are investigated and compared in this subsection.

For Cu-silica PMC, a set of 10 devices (five for LRS and five for HRS) with 10 µm size were tested at different dose levels. Each device was dc swept for 10 cycles with a compliance current of 5 µA. Devices were step stressed up to 7.1 Mrad(silica). Dose levels are differentiated by colors as shown in Fig. II.4.7. Another set of control samples, labeled as "non-irrad" were measured at the same test frequency as the irradiated samples.

Fig. II.4.7a plots the cumulative probability distribution of resistance for LRS PMCs prior to and after ^{60}Co irradiations up to 7.1 Mrad(silica). While the distribution in

HRS resistance is considerably broader than the LRS resistance, it can be observed in Fig. II.4.7b, that even a high level of TID does not change the distribution in any significant way. A potential explanation for the higher skew in the HRS distribution even prior to exposure may be due to some devices not being fully reset, which is somewhat common in resistive switching memory. For irradiated samples, the average LRS resistance for different dose level ranges from 27.3 kΩ to 35.3kΩ, while the average HRS resistance is between 1.41 GΩ and 2.47 GΩ, which is significantly higher than the reported MΩ-range OFF-state resistance in Ag-ChG PMCs [127]. The LRS resistances of these two technologies are comparable.

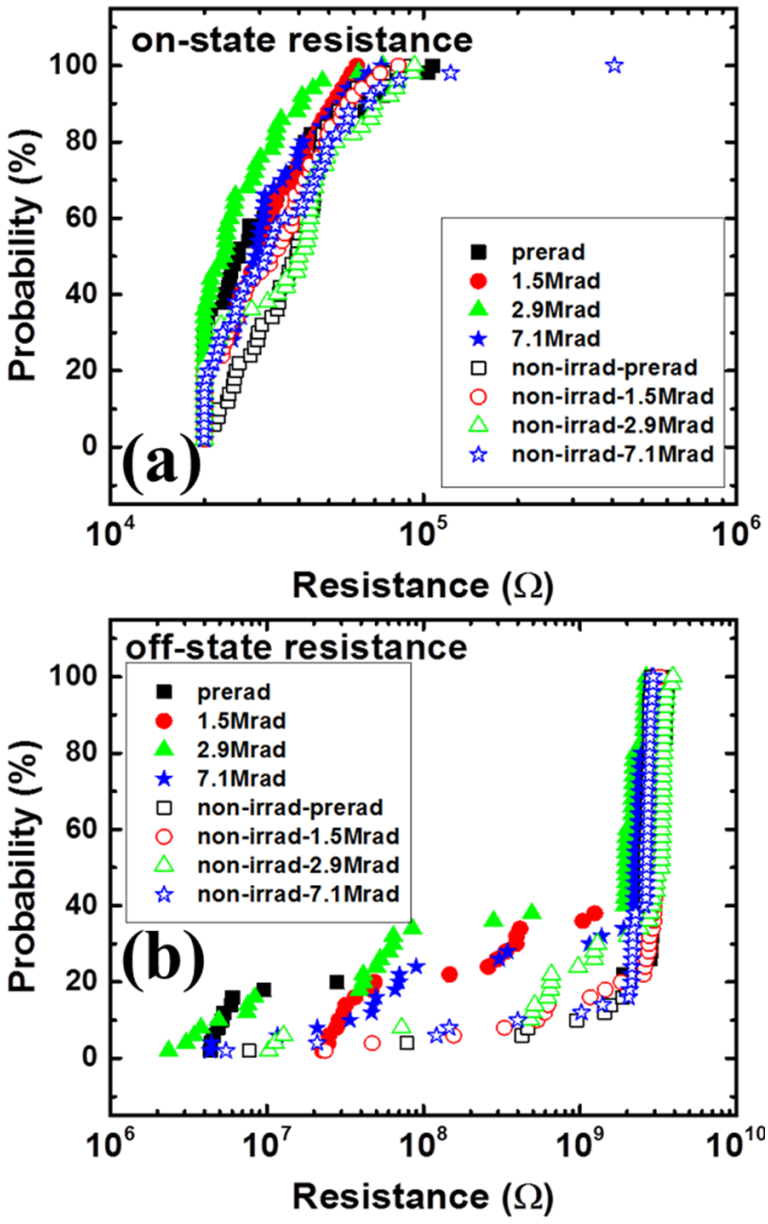


Fig. II.4.7. Cumulative probability of LRS (ON-state) resistance (a) and HRS (OFF-state) resistance (b) at different TID. © 2015 IEEE. Reprinted with permission from Ref. [92].

Since the cumulative distribution reflects only general trends, it is possible that subtle changes are not observable in the above plots. Thus, it is necessary to investigate how each individual device responds to TID. Fig. II.4.8 shows the device-to-device

comparison results. In each graph, irradiated and control samples are plotted in the left and right half windows, respectively. Fig. II.4.8a compares LRS resistance value after different TIDs. Again, the same as the cumulative plots have shown, for both irradiated and non-irradiated samples we find that data overlap randomly at different dose levels, which means the irradiation has no significant influence on LRS resistance. The situation for HRS resistance is slightly different. Here, we focus only on HRS resistances in GΩ-range (complete reset). It can be seen in the left-half of Fig. II.4.8b that the overall average HRS resistance decreases slightly after the 1.5 Mrad(silica) exposure but this reduction saturates if the devices are exposed to higher TID levels. This is not the case for the control samples, where no discernable change is observed.

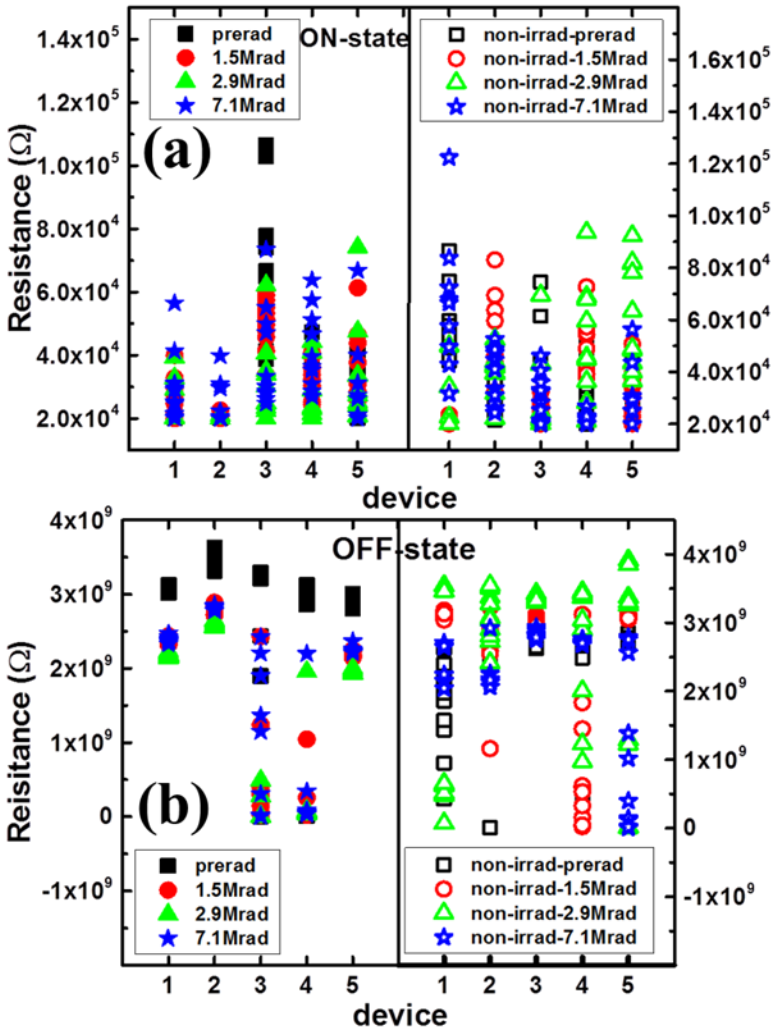


Fig. II.4.8. Device-to-device comparison of TID effects on LRS (ON-state) resistance (a) and HRS (OFF-state) resistance (b) at different TID. © 2015 IEEE. Reprinted with permission from Ref. [92].

Other than the dynamic resistance which is measured during each switching cycle, the retention of HRS and LRS before and after different TID exposure was also investigated, the results are shown in Fig. II.4.9. Ten devices were hard programmed (or erased) to LRS (or HRS) by 100ms 4V pulse prior to TID exposure. Then the device resistances were track at every TID level. As seen in Fig. II.4.9, no obvious degradation in

the device can be observed for both HRS and LRS. This result demonstrates that the retention of Cu-silica isn't affected by gamma-ray irradiation.

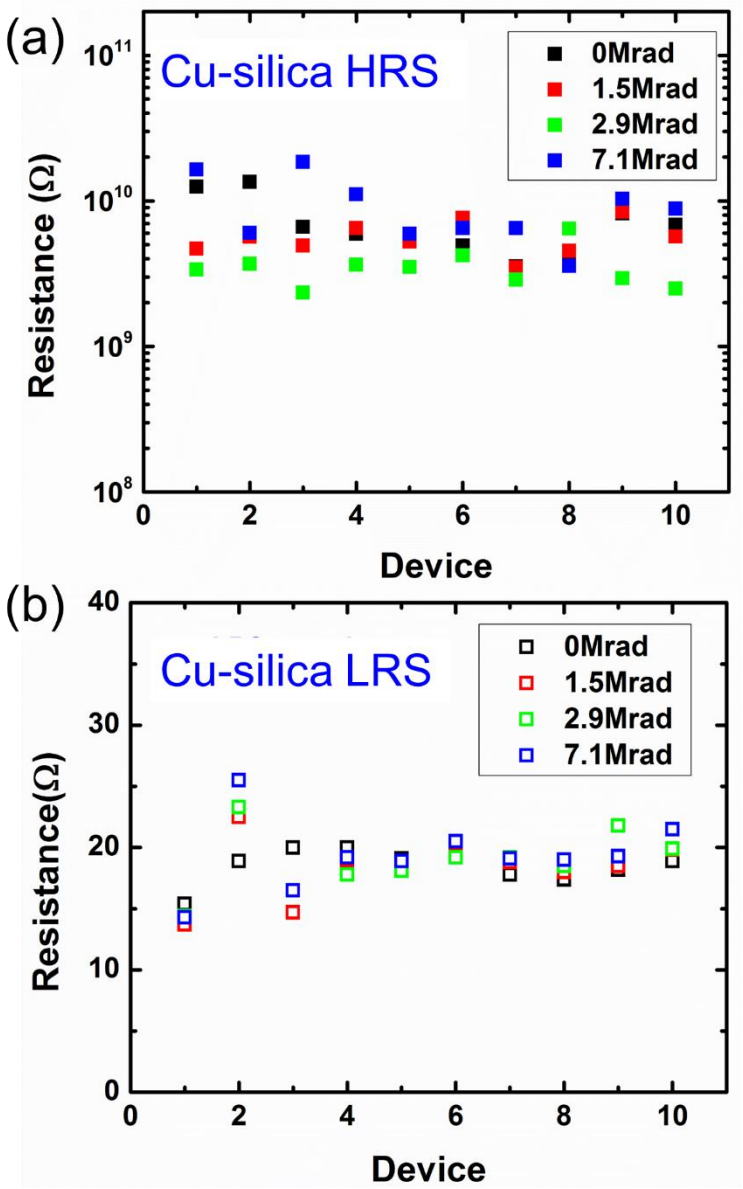


Fig. II.4.9. TID impact on the retention of Cu-silica PMC.

On the contrary, for $Ge_{30}Se_{70}$ PMC, a set of five 5 µm devices were DC switched for 10 cycles prior to and after 4.36 Mrad(GeSe) ^{60}Co irradiation and LRS and HRS data were extracted at 20 mV. Fig. II.4.10a and II.4.10b plot the cumulative probability

distribution of resistance for LRS and HRS of Ag-$Ge_{30}Se_{70}$ PMCs and Cu-$Ge_{30}Se_{70}$ PMCs respectively. The results show a clear reduction of HRS for both Ag and Cu cases after TID. Before irradiation there is a substantial resistance gap between LRS and HRS in both ChG PMC types. However, this gap shrinks significantly after irradiation. The reduction of the reading window (separation in HRS and LRS distributions) is undesirable and it causes an increase in read errors. This type of HRS degradation was not observed in the work [127]. This is because the ChG film investigated in [127] has already been saturated with Ag ions through a UV photodoping process, which reduces the impact of any additional radiation-induced ionization effects such as electron-hole generation in the ion conducting film. The photodoping process has been investigated for many years. It is generally believed that radiation (UV or high energy photons) is absorbed in the chalcogenide layer and generates electronhole pairs. Generated electrons get trapped in the chalcogenide layer, these filled electron traps are negatively charged and attract positively charged Ag ions into the ion conducting ChG film. As a result, Ag ions move into undoped chalcogenides which facilitate photodoping [135]. Once Ag or Cu ions have moved into the ChG layer enough to saturate the film, additional radiation exposure will not lead to more metal incorporation. Photodoping not only enhances the device performance (since it stabilizes the ChG ionic conductor and increases the LRS retention) it is also a necessary process step to improve the PMC's TID tolerance.

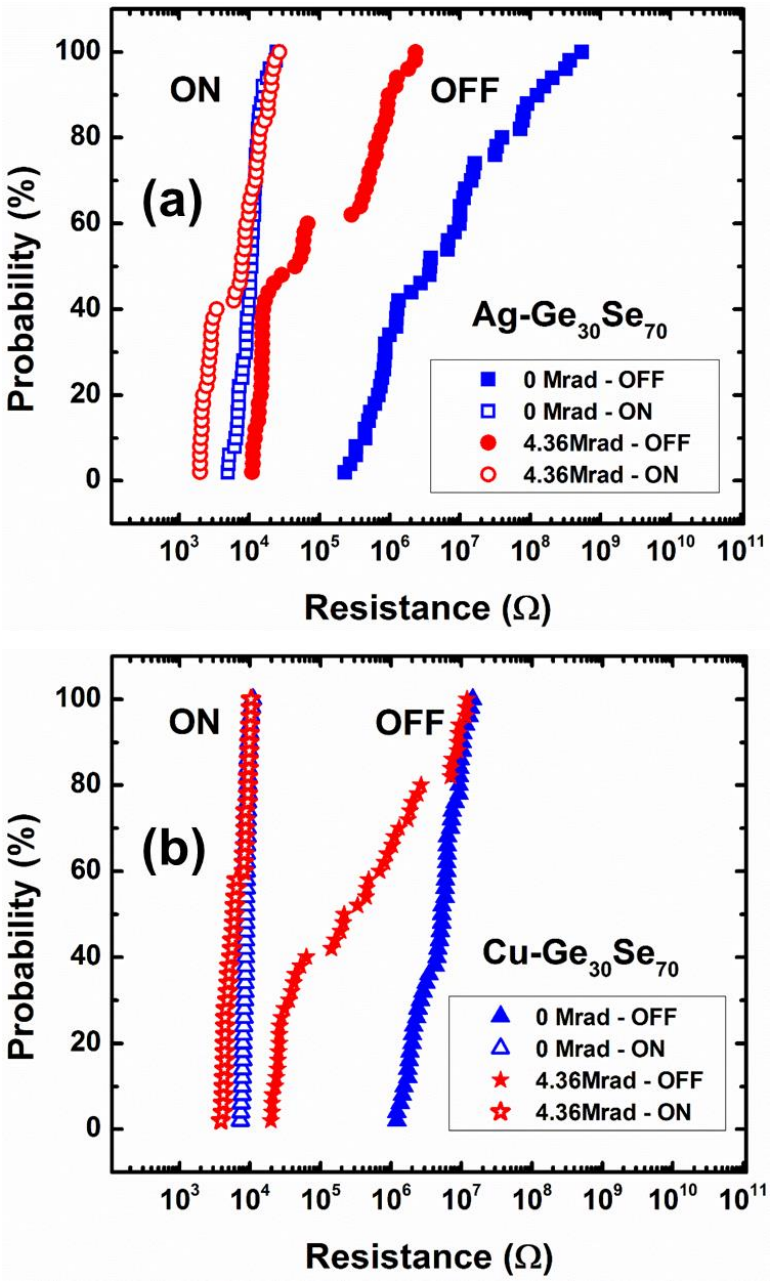


Fig. II.4.10. Cumulative distribution of LRS (ON-state) and HRS (OFF-state) resistance of (a) Ag-$Ge_{30}Se_{70}$ and (b) Cu-$Ge_{30}Se_{70}$ before and after TID. © 2017 IEEE. Reprinted with permission from Ref. [88].

II.4.3.3. TID Effects on Set (Threshold) Voltage of Cu-Silica PMC

As has been discussed in section I.4, ions move much more slowly in oxides than in ChG. The result is that the ions in oxide tend to be neutralized by electrons before reaching the inert cathode. Recent studies suggested that there has been an observed correlation between the leakage current in oxide and filament growth [89, 136]. The source of electrons can be tunneling electrons and/or trapped electrons in the film. Filaments grow faster in oxides with higher leakage current. Since ionizing radiation is capable of inducing leakage current [137], it is necessary to investigate the impact of ionizing radiation on the filament growth speed in silica. This speed can be qualitatively related to the set voltage (Vset) if a fixed voltage-sweep rate is applied. The faster a filament grows, the smaller the Vset. Fig. II.4.11 plots the cumulative distribution of the set voltage at different radiation dose levels. As shown in the graph, the Vset of irradiated and control samples randomly overlap each other, suggesting that gamma-ray irradiation has a negligible impact on the speed of filament growth. This may be due to the fact that in evaporated silica there is typically a very high density of pre-existing defects. The leakage current induced by those pre-existing defects overwhelms any potential effect from leakage current enhanced by irradiation. Another explanation could be the relatively long voltage stress in DC sweeps. Even if the leakage current does increase after ionizing radiation, as observed in Fig. II.4.8a where the HRS resistance decreases after 1.5 Mrad(silica) exposure, the increment is very small, resulting in a small difference in growth speed. Such subtle changes in growth speed are likely concealed in a long DC stress. For example, either the device is set at the beginning or the end of a 0.4 V voltage step, the DC curve can only reflect that the device

is turned on at 0.4 V. Thus, the conclusion that ionizing radiation does not affect filament growth speed is at present only valid for a quasi-DC condition.

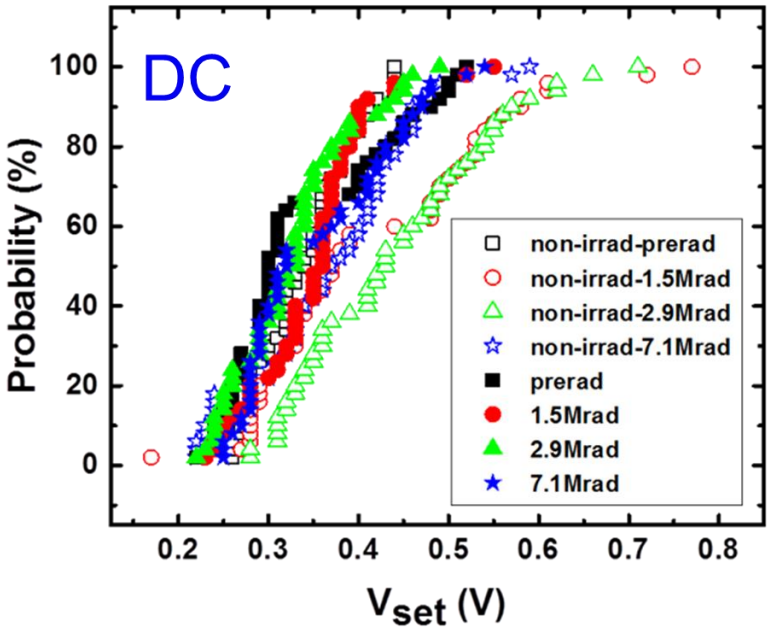


Fig. II.4.11. Cumulative probability of V_{set} at different TID for Cu-silica PMC. © 2015 IEEE. Reprinted with permission from Ref. [92].

To further illustrate the TID impacts on the speed of filament's growth (or dissolution), pulse testing was performed. Two sets of 5 devices were pulse cycled, each was cycle for 10 times. The first set of devices were pulsed without TID while the other set of devices were pulsed after 7.1Mrad TID. Devices were hard programmed by 4V 100ms electrical pulses and were hard erased by 4V 1us electrical pulses. The forming and erasing time were summarized in Fig. II.4.12. No observable difference can be found for both programming and erasing since the speed of irradiated sample and non-irradiated sample are randomly overlap together.

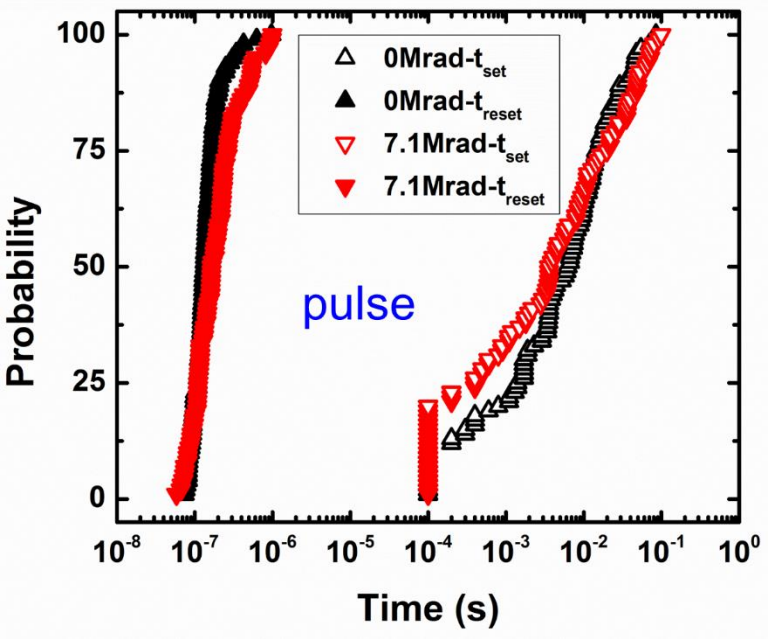


Fig. II.4.12. Cumulative probability of programming and erasing speed at different TID for Cu-silica PMC.

II.4.3.4. TID Effects on Multilevel Switching of Cu-Silica PMC

The multilevel switching ability is a key property of Cu-silica PMC that supports their use in multi-level cell (MLC) memory or neuromorphic computation. Assessing the reproducibility of multilevel switching after ionizing radiation exposure is therefore of interest. Similar to the multilevel test mentioned in Section II.3.2, the same number of PMCs were tested after gamma-ray exposures. Fig. II.4.13 plots the LRS resistance (R_{on}) vs. programming current (I_{prog}) for non-irradiated PMCs and PMCs that were irradiated for 7.1 Mrad(silica). Both pre- and post-irradiation responses satisfy the power-law dependence. The extracted A and n for irradiated samples are 3.9 and 0.8, respectively, which is essentially the same as the values extracted for non-irradiated control samples. Thus, the data show that ionizing radiation has a negligible impact on multilevel switching.

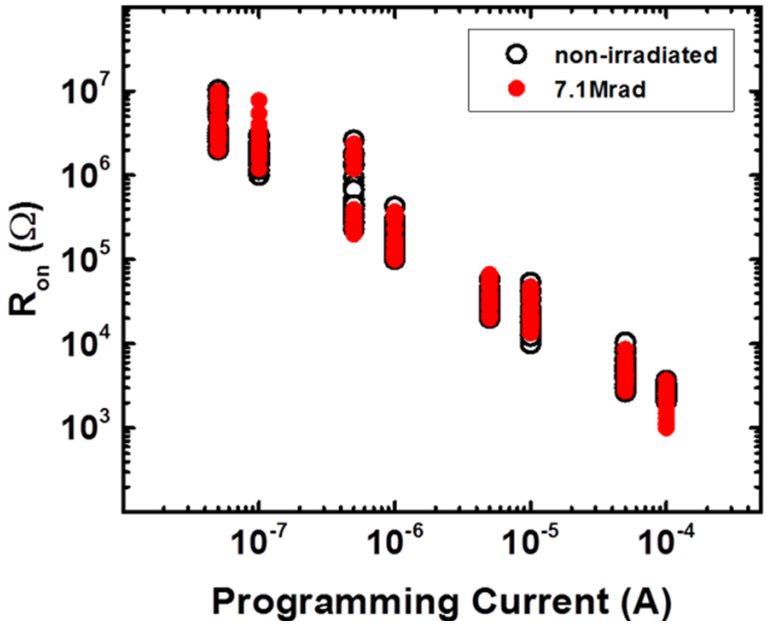


Fig. II.4.13. Comparison of R_{on} vs. I_{prog} before and after 7.1 Mrad(silica) TID for Cu-silica PMC. © 2015 IEEE. Reprinted with permission from Ref. [92].

II.4.3.5. TID Effects on Endurance of Cu-Silica PMC

Data presented in the previous sections show only minor changes in the characteristics of Cu-silica PMCs caused by TID. This could be because the effects are too subtle to be observed. Endurance tests were performed on two sets of five Cu-silica devices to potentially amplify these small changes. One set was irradiated up to 7.1 Mrad(silica) and the other was an un-exposed control sample set. In order to minimize the effect of long-term annealing of radiation-induced-traps [138, 139], all devices were cycled until failure or manually stopped at a maximum of 500 cycles to shorten the test duration. Fig. II.4.14a shows a typical endurance result for an irradiated device and a non-irradiated device. Both of them show resistive switching gets stuck in the LRS. It is likely caused by the introduction of excess Cu ions into oxide during cycling [140]. Fig. II.4.14b summarizes

the results from this endurance test. For the control sample, two out of five devices can be cycled at least 500 times, the other three fail before 500 cycles. For the irradiated samples, one device can be cycled for 500 times. Even though some differences in endurance between irradiated and control samples are observed, this is most likely caused by process variations, not radiation damage.

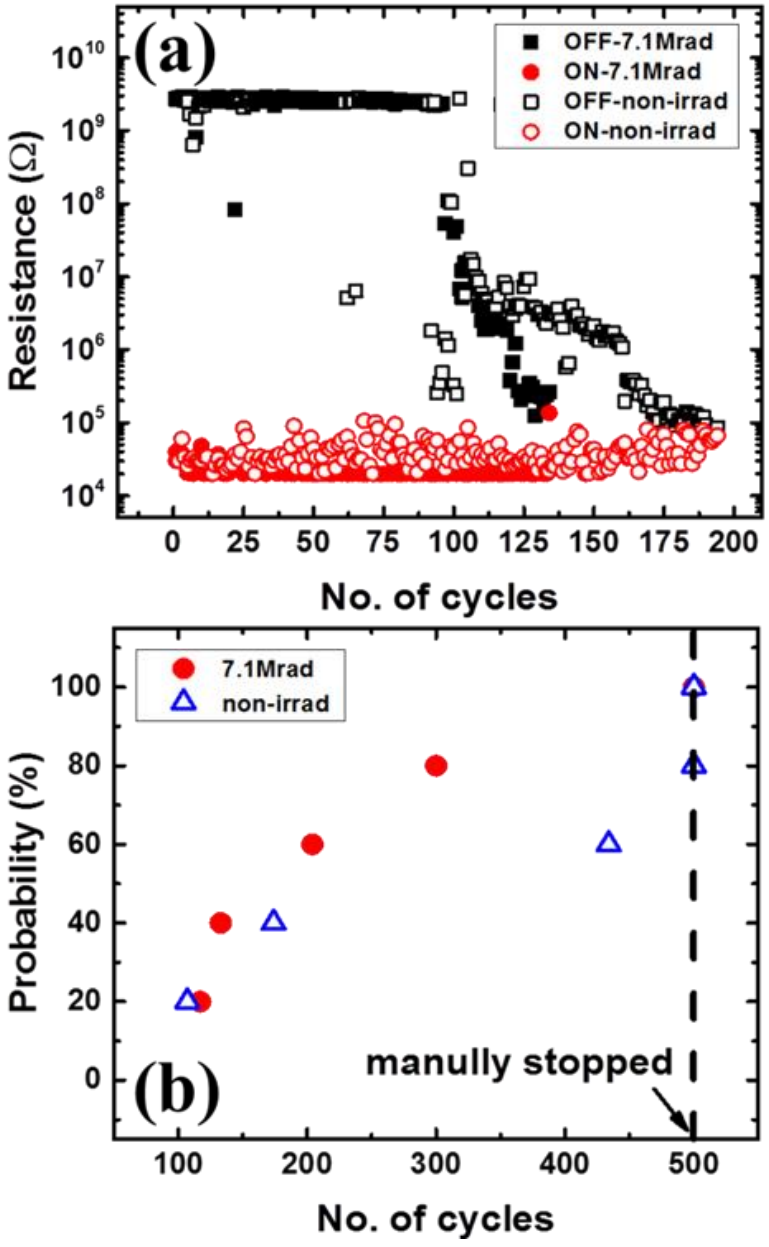


Fig. II.4.14. (a) Typical cycling performance of irradiated and control Cu-silica devices, (b) Cumulative plot of number of cycles for 5 irradiated and control Cu-silica devices. © 2015 IEEE. Reprinted with permission from Ref. [92].

II.4.4. Analysis of Radiation Results

From the experimental radiation results shown in last section, it is obvious that the virgin-state and HRS Cu-silica PMC does not seem to be affected by ionizing radiation up to 7.1 Mrad(silica). This is not the case for PMCs fabricated with $Ge_{30}Se_{70}$ films, which normally exhibit a reduction in device resistance after irradiation. As discussed, the resistance degradation for virgin-state or HRS is attributed to ionizing radiation induced photo-doping process which causes the diffusion of Cu or Ag in ChG. Photo-doping process is triggered by the interaction between Cu (or Ag) electrode and electron-hole pairs (ehps) generated in the electrolyte. The number of generated ehps per rad is determined by the bandgap [141] of the target material according to

$$\frac{\#ehp}{cm^3 rad} = 100 \cdot \frac{1}{1.6 \times 10^{-12}} \cdot \frac{1}{E_P} \cdot \rho$$

where ρ is the material density and E_P is the mean energy needed to ionize a material. E_P is proportional to the bandgap (approximately 2X to 3X). Based on this, a potential explanation for the suppression of photo-doping process in the virgin-state or HRS Cu-silica PMC is the much larger bandgap of silica (> 8 eV) relative to $Ge_{30}Se_{70}$ (< 2 eV). Many ehps are generated in $Ge_{30}Se_{70}$ by gamma-rays because of its relatively small bandgap. However, this is not the case in Cu-silica films. Because of its larger bandgap, the number of ehps generated in silica may be considerably lower than the $Ge_{30}Se_{70}$.

In addition to the impact of material bandgap, an added distinction between the $Ge_{30}Se_{70}$ and silica systems is the nature of carrier traps. It is well known that ehps generated in dielectrics can be trapped in defect precursor sites, the prevalent type of trap is different from one material to another. Electron traps play a major role in chalcogenide glasses, such as $Ge_{30}Se_{70}$. Density functional theory (DFT) calculations predict that electrons tend to be self-trapped in pairs because of the Ge-Ge dimers [142]. The electron-traps may play an important role in photo-doping of Ag in the $Ge_{30}Se_{70}$ layer, either by breaking Ge-Ge and Ge-Se bonds that act as sites for Ag (or Cu) incorporation or by attracting cations into the ChG film through drift mechanisms [143], this process is illustrated in Fig. II.4.15a. This causes the resistance of virgin or HRS $Ge_{30}Se_{70}$ films to drop by orders of magnitude after gamma-ray irradiation. However, the trapped charge in silica is net positive due to the capture of holes in neutral oxygen vacancies [144]. Thus, the positively charged hole would repel rather than attract Cu since the trapped hole has the same charge polarity as any residual Cu ions, shown in Fig. II.4.15b. Radiation induced hole-traps in silica is thus another potential explanation for why the virgin-state and HRS resistance is barely impacted by ionizing radiation.

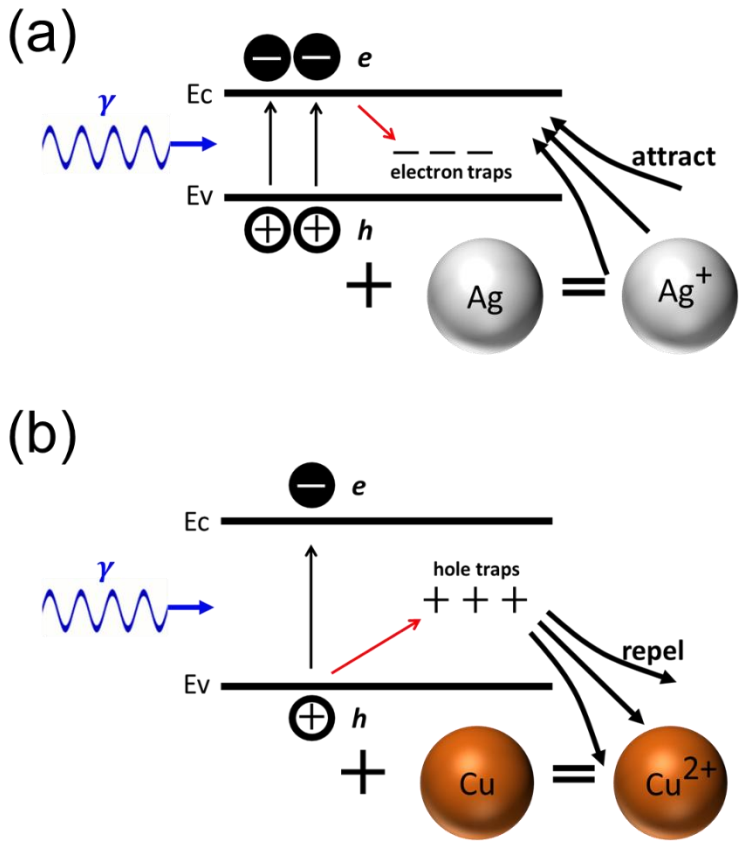


Fig. II.4.15. Schematics of charged trap assisted doping process in $Ge_{30}Se_{70}$ (a) and silica (b).

Another potential explanation for the difference in virgin-state and HRS responses may be related to the charge state of active metal in the respective electrolytes. We show in Fig. II.4.16 the projected density of states (PDOS) for the Ge_2Se_3:M(M= Cu or Ag) material systems, Ge_2Se_3 is simulated as an equivalent replacement of $Ge_{30}Se_{70}$ because of their structural similarity. In the simulation, the metal atoms are in local interstitial equilibria. The valence band edge is at ∼−5.51 eV and the conduction band edge is at ∼−4.46 eV, determined by the PDOS edges of bulk Se. We include the calculated Fermi level for both bulk Ge_2Se_3, and for the defect calculation, showing that in the neutral charge

state the presence of a metal atom moves the Fermi level to the edge of the conduction band. Note that the 5s and 4s density (for Ag and Cu, respectively) starts several eV above the conduction band edge, making it obvious that both metal ions spontaneously autoionize, dropping the outer electron into the conduction band.

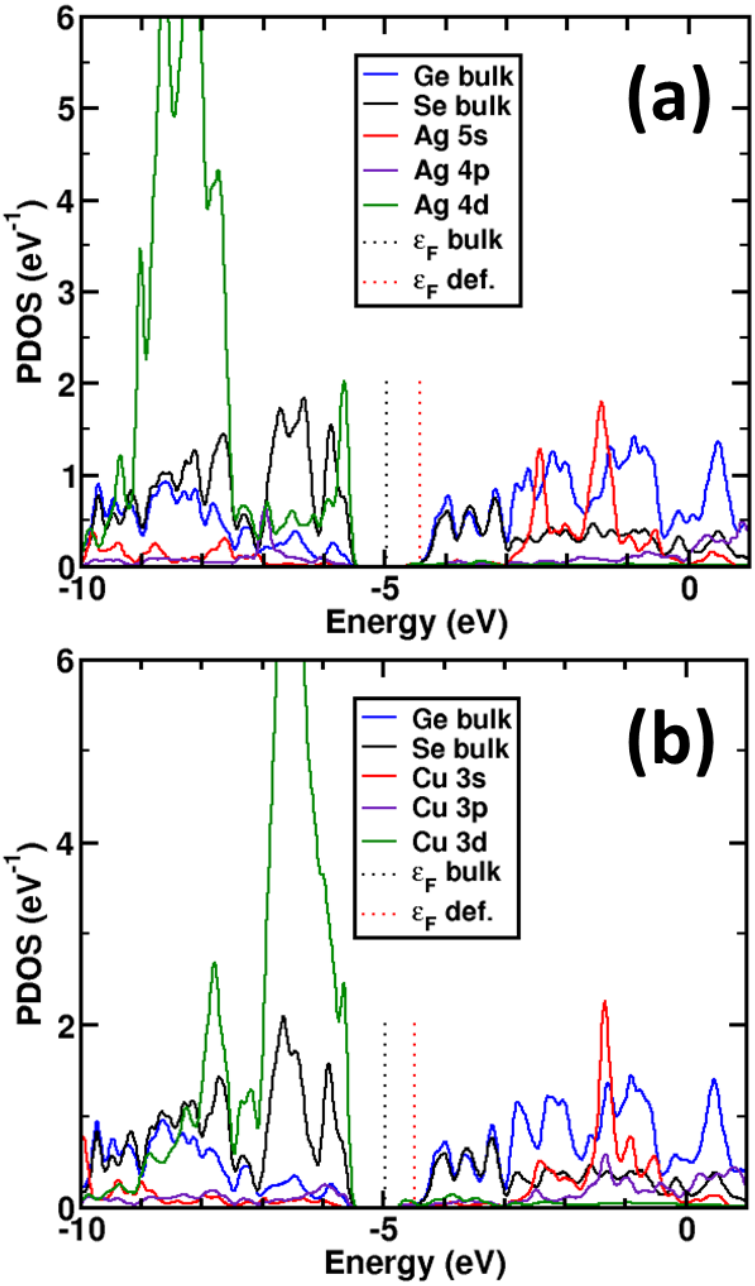


Fig. II.4.16. Results of DFT calculations showing the projected density of states (PDOS) for (a) Ag- Ge_2Se_3 system, (b) Cu- Ge_2Se_3 system. © 2017 IEEE. Reprinted with permission from Ref. [88].

In Fig. II.4.17, we show the PDOS for interstitial Cu in silica. Here the band edges are delineated by the Silicon (red) density, with the CBE at -2.0 eV, confirmed in separate, bulk silica calculations. The Cu density is in green. Here Cu has a continuum and two apparent discrete states in the band gap. The continuum is predominantly Cu 3d. Thus, the calculations predict that Cu^{2+} is not stable, i.e., it will readily trap electrons and neutralize, suppressing ion transport, particularly in its virgin state.

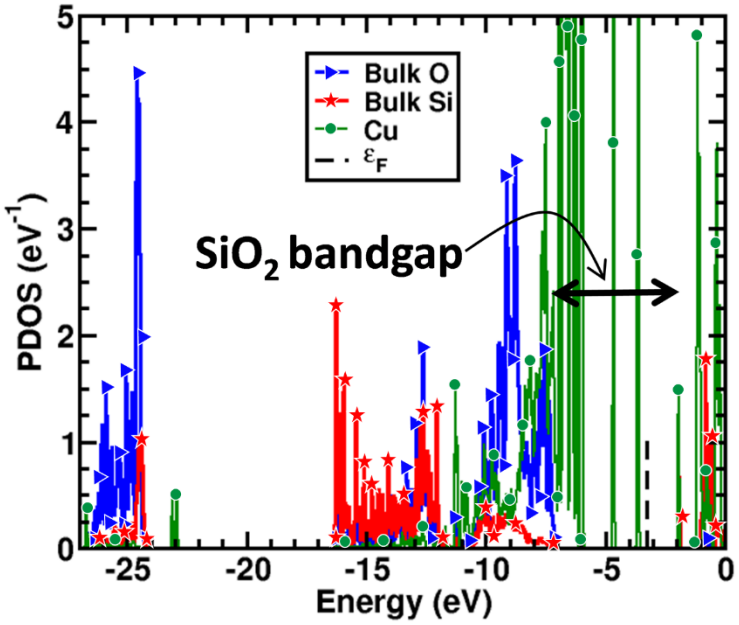


Fig. II.4.17. Results of DFT calculations showing the projected density of states (PDOS) for Cu- silica system. © 2015 IEEE. Reprinted with permission from Ref. [92].

In summary, the radiation experiment demonstrates that gamma-ray irradiation has a negligible impact on the virgin-state, HRS and LRS resistance of Cu-silica PMC, while it reduces the virgin-state and HRS resistance of $Ge_{30}Se_{70}$ base PMC. Three mechanisms, i.e. low ehp generation rates, hole trapping and neutral Cu in silica, are reasonable explanations for the suppression of the photo-doping process and reduced resistance in irradiated Cu-silica PMCs. The superior reliability of Cu-silica PMC in ionizing radiation environment proves that it is a promising non-volatile memory solution for radiation-hardened system design.

II. 5. Equivalent RC Circuit Extraction by Impedance Spectroscopy

II. 5.1. Fundamentals of Impedance Spectroscopy

Impedance spectroscopy (IS) is a pure electrical method, due to its simplicity and powerfulness, it has been extensively used to investigate electrochemical systems, such as batteries, electroplating, corrosion, etc [145]. The general approach is to apply an electrical stimulus, i.e. current or voltage, to the device-under-test (DUT) and observe the responses. The responding signal (voltage or current) depends on multiple microscopic processes in the DUT such as transfer of electrons and diffusion of ions, etc.

The equation below shows the fundamental theory of impedance spectroscopy. It has a similar format as classic Ohm's law, where the resistance is a result of voltage over current. However, instead of DC signal for resistance measurement, an AC signal with angular frequency ω is applied for impedance measurement. The phase shift angle (θ) and amplitude of responding current (I) is then measured by the equipment and the calculated impedance is recorded in the format of real part $Z(\omega)$' and imaginary part $Z(\omega)$''.

$$\boldsymbol{Z(\omega) = \frac{V(\omega)}{I(\omega, \theta)} = |Z(\omega)|e^{j\theta} = Z(\omega)' + j \cdot Z(\omega)''}$$

By sweeping the frequency, a number of Z' – Z'' pairs is measured and they are plot in the format of Z'' vs Z' with the former being y-axis and the latter being x-axis. This is also known as Cole-Cole plot. By fitting the Cole-Cole plot with equivalent R-L-C circuit, the nature of electrochemical process happening at interfaces and electrolytes of DUT can be analyzed and identified. The flow diagram that describes the IS measurement procedure is presented in Fig. II. 5.1.

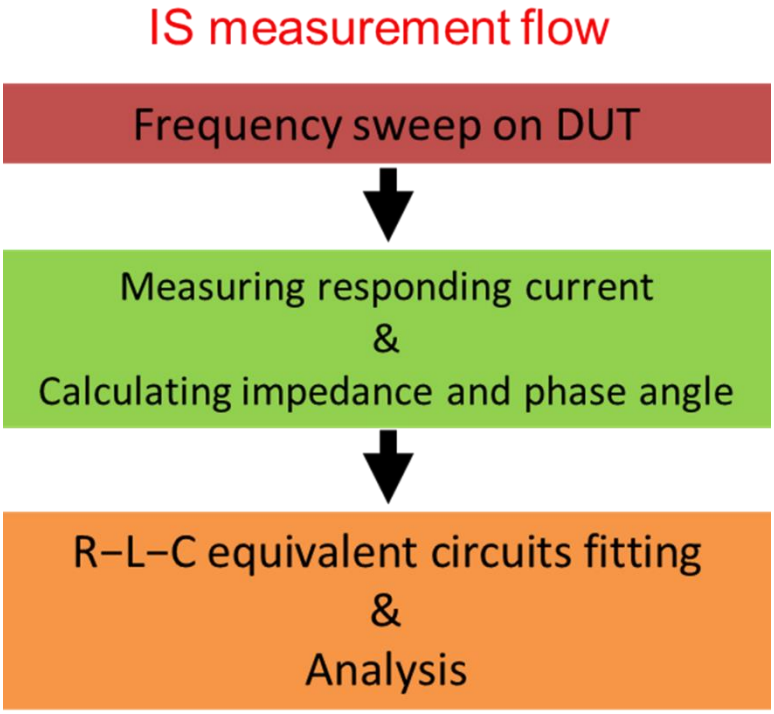


Fig. II. 5.1. Flow diagram of impedance spectroscopy measurement.

In recent years this non-destructive method has also been employed to explore the materials properties of resistive switching devices. Numerous meaningful results have been

obtained, for example, a percolation network was identified for the resistive switching of Ag/a-Si PMC [146], layered electrolyte with a high- and a low-doped region was found in Ag/Ge_xSe_y PMC [147], and a filament model was identified for a TiO_2 based OxRAM [148].

II. 5.2. Impedance Spectroscopy Experiment Setup

Impedance spectroscopy (IS) was performed with a Solartron SI 1260 Impedance/Gain-phase Analyzer. The impedance of Cu-silica PMC was measured by an AC signal with the frequency sweeping from 10Hz to 1MHz. The AC signal has a peak-to-peak amplitude of 10 mV and is centered at 0 V DC bias. The connections between equipment's IO ports and PMC device is shown in Fig. II.5.2, where the voltage stimulus is output from "GEN OUTPUT" port to the device active electrode, the corresponding current is measured at "CURRENT" port which is tied to the device inert electrode, the resulting voltage drop across device is input to "VOLTAGE 1 HI" and "VOLTAGE 1 LO" and measured by the differential amplifier inside. Thus, the ratios of voltage and current yield the impedance of Cu-silica PMC.

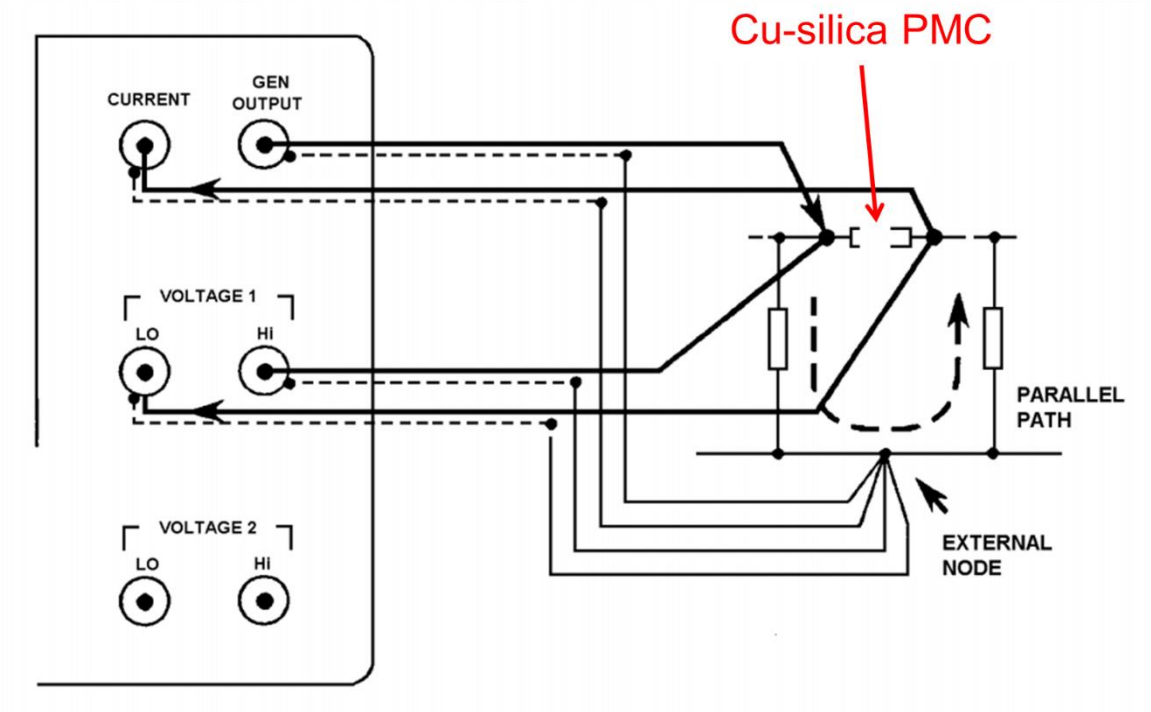


Fig. II.5.2. Test setup for Cu-silica PMC impedance spectroscopy.

II. 5.3. Impedance Spectroscopy of PMC with Thin CVD Silica

Fabrication details of Cu-silica PMC has been discussed in section II.2, the silica switching layer is 5 nm and is deposited by RPCVD. The reason for choosing RPCVD silica is because the better LRS retention and better film homogeneity than e-beam silica. In this work, impedance spectra data obtained from measurements on Cu-silica PMCs with different areas (from 100 × 100 μm^2 to 500 × 500 μm^2) and a range of programmed resistance states (200 Ω to 3 MΩ) were analyzed. The Z' and Z'' data were fit to the results of SPICE circuit simulations on equivalent circuit models representative of Cu-silica PMCs in both virgin and electroformed states.

Prior to device measurement, the background noise from parasitic RLC elements should be characterized and taken into account for future data fitting. The parasites can be

contact resistance, capacitance and inductance from BNC cables, capacitance and inductance from the equipment etc. The impedance of parasitic elements was measured by contacting the two probes on the same W inert electrode. Fig. II.5.3a shows the IS results of parasitic elements. The black squares are experimental results and the red solid line is the equivalent-circuit fitting result. The equivalent circuit used to model the system parasites is shown in Fig. II.5.3b, which is composed of a parallel connected capacitor (Cp) and resistor (Rser) in series with an inductor (Lp). The value of the parasitic capacitor, resistor and inductor is 424 pF, 97 Ω and 9.8 μH, respectively.

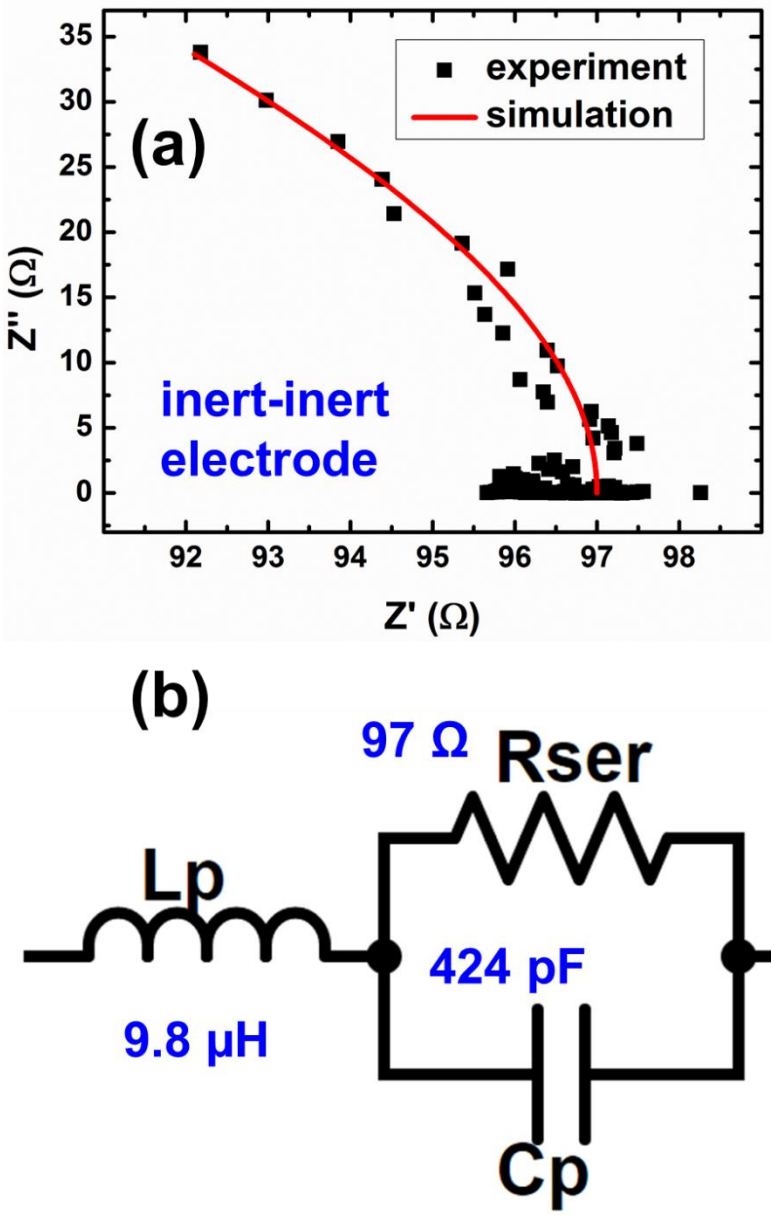


Fig. II.5.3. Impedance spectroscopy results (a) and equivalent circuits (b) of parasitic elements.

Due to equipment/setup limitations, the smallest device that can be properly characterized in AC mode is 100×100 μm^2. Fig. II.5.4a shows the IS results of virgin devices (prior to electroforming) with different side lengths. Before electroforming, it is

assumed that the device is a conventional MIM capacitor without any filamentary structures. The results are plotted in a Cole-Cole plot format, in which the x-axis is the real part and the y-axis is the imaginary part of the measured impedance. The virgin-state IS results are fit to a parallel RC network (red dashed box in Fig. II.5.4b) in series with the parasitic elements discussed in the previous paragraph. The formulae for Z' and Z" for the complete circuits are

$$Z' = {R_{ser}}\Big/{R_{ser}^2\omega^2 C_p^2 + 1} + {R_1}\Big/{R_1^2\omega^2 C_1^2 + 1}$$

$$Z'' = \omega \cdot \left(L_p - {R_{ser}^2 C_p}\Big/{R_{ser}^2\omega^2 C_p^2 + 1} - {R_1^2 C_1}\Big/{R_1^2\omega^2 C_1^2 + 1}\right)$$

which summarizes the device impedance response to frequency ($f = \omega / 2\pi$). The fits (red lines in Fig. II.5.4a) show excellent agreement with the experimental data (symbols).

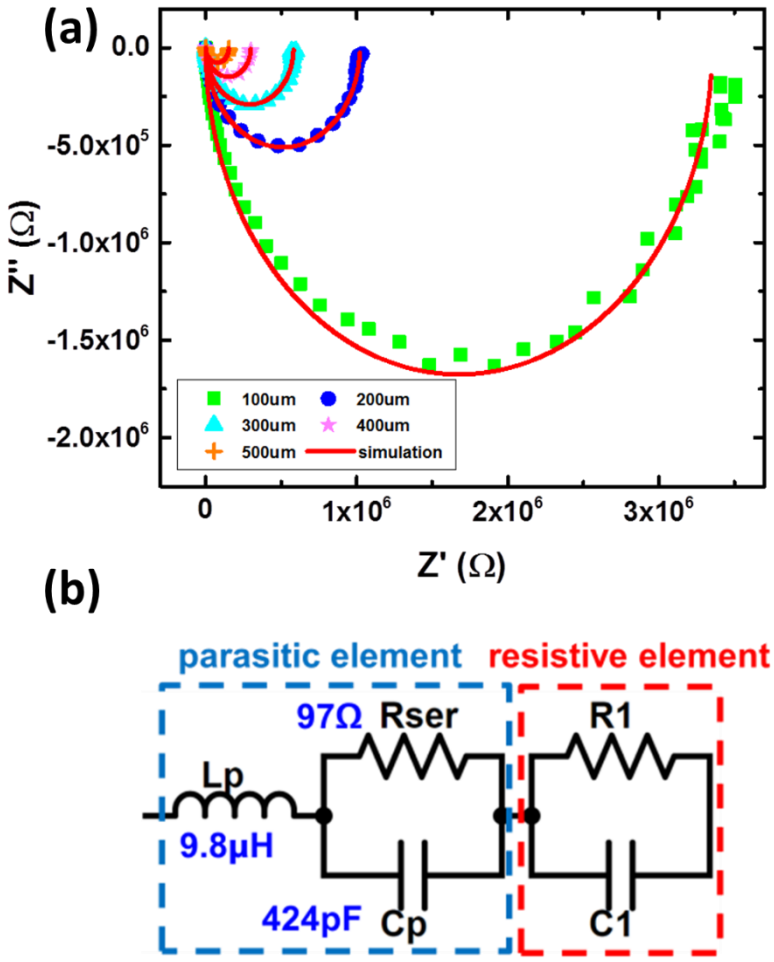


Fig. II.5.4. (a) Impedance spectra of virgin-state devices with different sizes, symbols are experimental data and solid lines are simulation data. (b) Equivalent circuit: dash-dot blue is box parasitic part, dash red box is PMC device. © 2016 IEEE. Reprinted with permission from Ref. [64].

The extracted resistance (R1) and capacitance (C1) values for the virgin elements are plotted in Fig. II.5.5. Both R1 and C1 follows the classical dependence on device size, i.e., resistance changes inversely with area (R_{ideal}) and capacitance is proportional to area (C_{ideal}). The calculated dielectric constant is ~5, which is slightly greater than pure silica

(3.9). This could be attributed to the incorporation of Cu atoms into switching layer during processing.

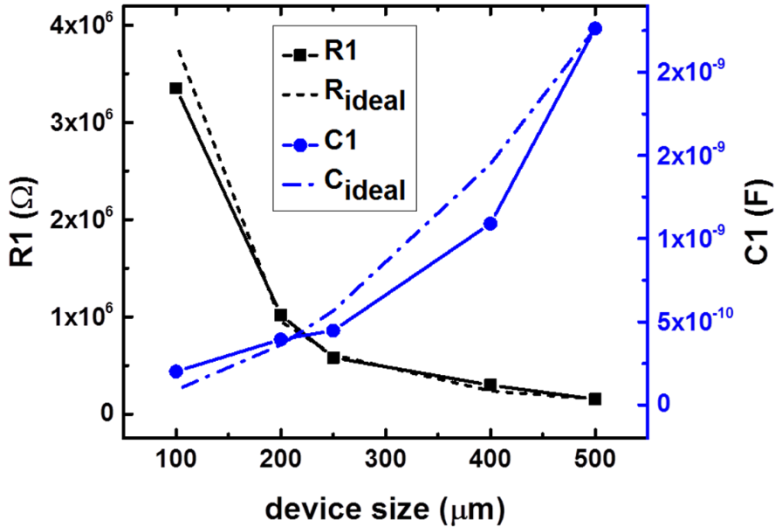


Fig. II.5.5. Extracted resistance and capacitance value vs. device size for as-fabricated device. © 2016 IEEE. Reprinted with permission from Ref. [64].

Fig. II.5.6 plots the IS results obtained on a 500 × 500 μm^2 device with programmed resistances (post electroforming) between 230 Ω and 55 kΩ. In order to obtain the theoretical impedance curves, values of the five components shown in Fig. II.5.4b are required. R1 is calculated by subtracting the series resistance (Rser) from the DC programmed resistance, the values of other parameters, i.e., Lp (9.8 μH), Rser (97 Ω), Cp (424 nF) and C1 (2.3 nF), are fixed. By inserting all these values into the two equations (Z' and Z'') above, the theoretical results are obtained and plotted as red solid lines in Fig. II.5.6. This clearly shows that all red lines go through the symbols which indicate that the experimental results fit well to the equivalent circuit shown in Fig. II.5.4b.

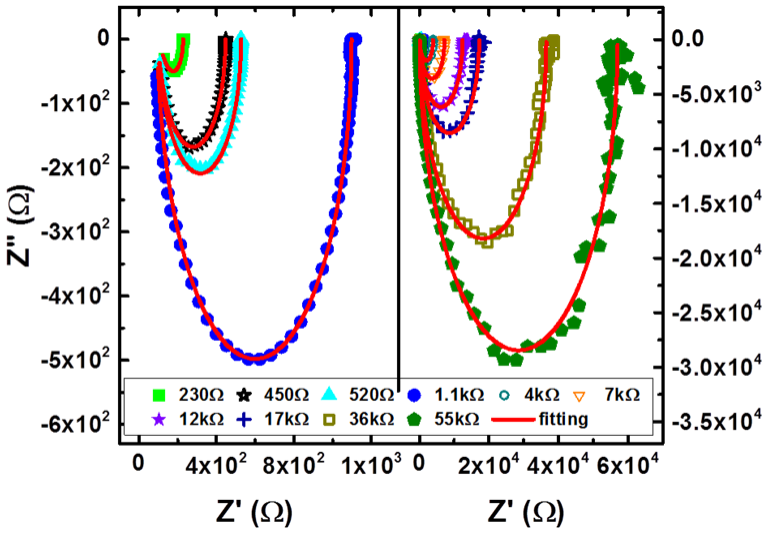


Fig. II.5.6. Impedance spectra of a 500 × 500 μm^2 device switched to various resistance states. © 2016 IEEE. Reprinted with permission from Ref. [64].

IS measurements were also performed on devices with similar resistance states (about 250 Ω) but different sizes. These results are shown in Fig. II.5.7. For theoretical impedance curves, R1 is calculated in the same way as mentioned above but C1 varies with the device size (using the same value from the virgin state impedance results shown in Fig. II.5.5), and the value of other parameters are fixed. By comparing the theoretical results to experimental data, the same equivalent circuit once again is shown to be appropriate. However, the Lp used to fit the data is 12 μH, which is slightly higher than the previous value. We attribute the shifts in inductance to slight variations in the test setup.

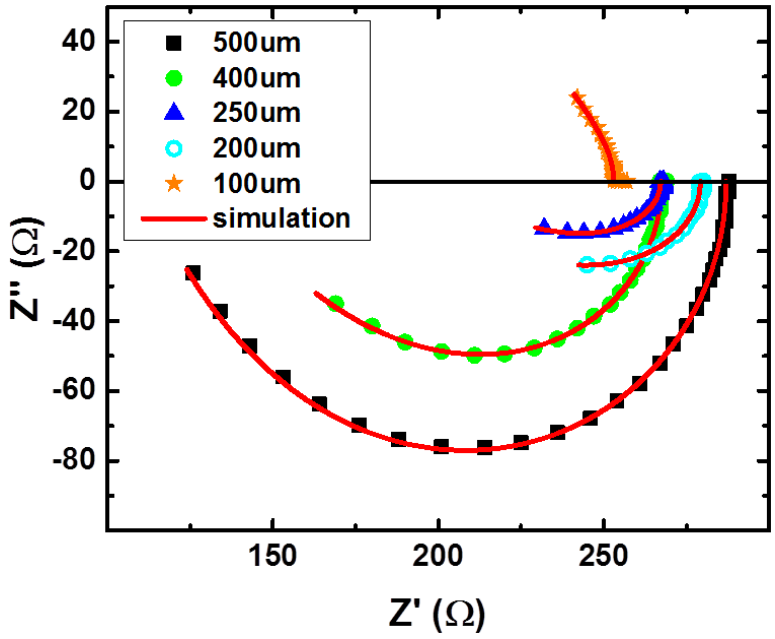


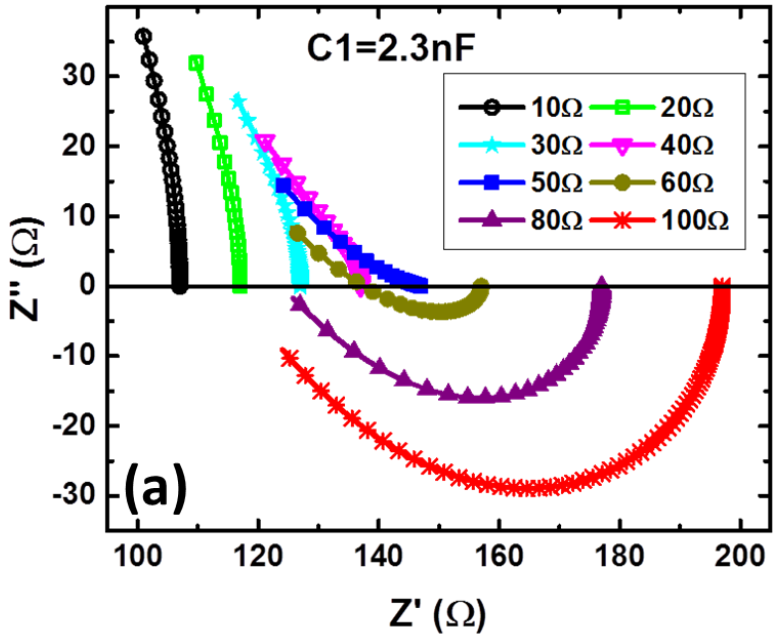
Fig. II.5.7. Impedance spectra of switched devices at similar resistance states but different sizes. © 2016 IEEE. Reprinted with permission from Ref. [64].

This data reported in Fig. II.5.6 and II.5.7 confirms that the device capacitance is dependent on area but independent of resistance state. This is reasonable since the filament size is thought to be negligibly small compared to the overall area of the device.

It can be observed in Fig. II.5.7 that the imaginary part of the impedance (Z") for devices with smallest area (100×100 μm^2) changed from a negative to a positive value when the resistance state is very low. This is because the parasitic inductor (Lp) dominates when the capacitance and resistance of the device is small. This was verified by SPICE simulation as discussed below.

SPICE simulations were performed on the equivalent circuit depicted in Fig. II.5.4. with the same frequency range as the IS experiment. The values of parasitic elements are fixed; only C1 and R1 are varied. Two scenarios are investigated: 1) fixed device size (i.e.,

fixed C1) and variable resistance (R1) and 2) fixed resistance (R1) and variable C1 (i.e., variable device size). The result for scenarios 1 and 2 are shown in Fig. II.5.8a and II.5.8b, respectively. Fig. II.5.8a confirms that the imaginary part changes sign when the resistance (R1) value is small and Fig. II.5.8b confirms that the imaginary part flips when the capacitance (C1) value is small.



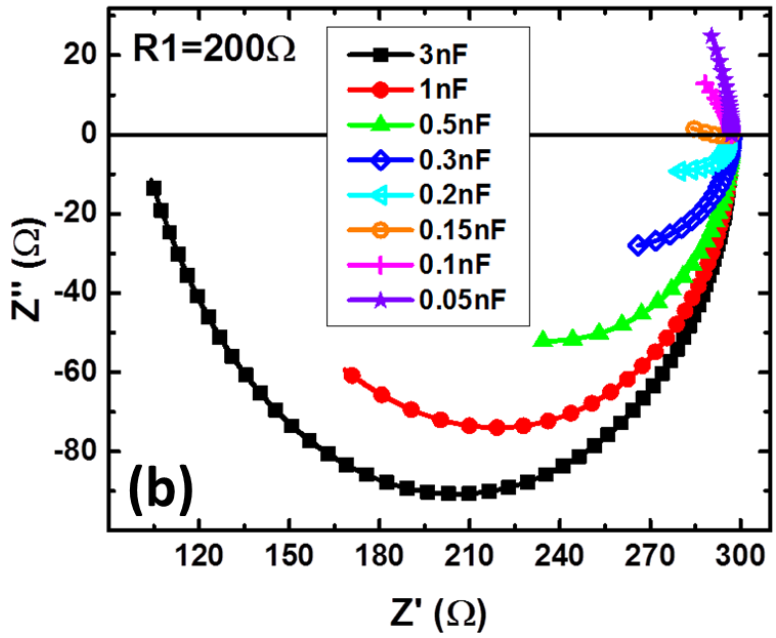


Fig. II.5.8. SPICE simulation of the impedance spectra of a PMC device with fixed device area (capacitance) but changeable resistance (a), fixed resistance but changeable device area (capacitance) (b). © 2016 IEEE. Reprinted with permission from Ref. [64].

Both the experimental and simulation results show that the Cu/silica PMC devices with different programmed resistance states can be accurately modeled as a parallel RC circuit. The capacitance has a constant value for a fixed device size regardless of the resistance. This non-correlation between resistance and capacitance indicates that the multilevel resistive switching occurs only in localized conducting region that has negligible size compared to the much larger device area. Thus the capacitive properties of the PMC, i.e., dielectric constant and film thickness, are independent of resistance. The localized switching region is likely composed of one or perhaps multiple conductive filaments. Variations in resistance state is attributed to the modulation of filament dimension and/or number by the current compliance. In the lowest resistance state, strong filaments are present which appear to penetrate the entire silica layer and short the cathode to the anode. At high resistance states, the filaments exist but are likely reduced in size and quantity, and they likely do not extend across the film. Previous experiment have shown that a single filament connection between electrodes would result in a maximum resistance of 12.9 kΩ [113]. It is also possible that the filaments in highly resistive states are composed of small discrete clusters, nevertheless, they are still distributed in localized regions which have negligible area compared to the devices. Thus, the parallel RC circuit is still valid. This result is different from a previous impedance spectroscopy analysis of HRS Ag/$Ge_{30}Se_{70}$ PMCs [147], in which the equivalent circuit was defined by two parallel RC circuits. The

two RC elements correspond to two chalcogenide layers with different Ag doping concentrations. For the Cu-silica PMC, however, there appears to be only one homogeneous layer characterized by low densities of Cu that have diffused into the thin silica (5nm) film during device fabrication. Furthermore, it should be noted that the proposed equivalent circuit could no longer be accurate when the size of the device and filament are comparable and this needs further investigation.

II. 5.4. Impedance Spectroscopy of PMC with Thick Cu-Doped Silica

As has been described in device fabrication section, the switching layer of type-4 PMC was created by thermal diffusion of Cu atoms from the Cu electrode into a 100nm e-beam evaporated silica. Unlike homogenous RPCVD thin silica, the silica layer doped by this method will present a concentration gradient with more Cu dopant at the active electrode and less Cu dopant at the inert electrode. In order to prove the assumption of a layered silica film in type-4 PMC, impedance spectroscopy experiment was performed on this type of device with a constant area, i.e. $30 \times 30\ \mu m^2$. The impedance of a range of resistance states (350 Ω to 37 kΩ) were measured under frequency from 10Hz to 1MHz and the spectra data were fit by SPICE equivalent circuit simulations.

For the lowest programmed resistance state (350Ω), the impedance spectra is shown in Fig. II.5.9. It has a linear shape across the entire frequency domain. According to the discussion in last section, the positive Z'' indicates a strong inductive element. Moreover, the nearly 90 degree slope suggests that the capacitive impact is small. This is reasonable because the device has a small area. The result can be fitted by a serially connected R-L

equivalent circuit with R being 350 Ω and L being 6μH. The resistance and inductance comes from metallic filament and the metal electrodes.

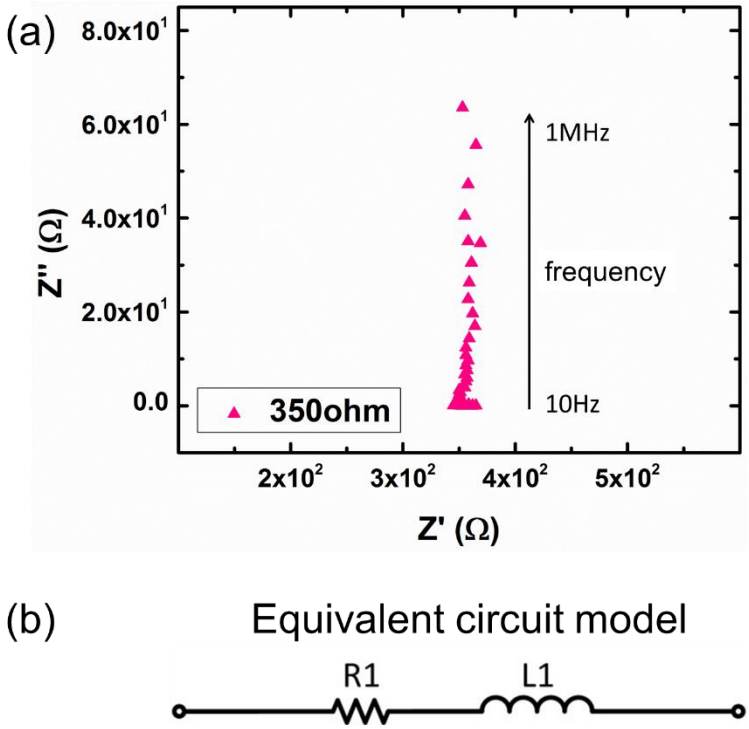


Fig. II.5.9. Impedance spectra (a) and equivalent circuit model (b) of hard programmed PMC device.

Since the resistance range between 3kΩ and 37kΩ is where the device can be reliably switched, it is more of interest to study the impedance characteristics in this range. Prior to IS measurements, the device was pre-programmed to target resistance. The IS results for these resistance states are shown in Fig. II.5.10a, in which the colored symbols are experimental data and the red lines are fitting results. The experimental data are adequately fitted using a two parallel resistor–capacitor (2 R-C) model, as illustrated in Fig. II.5.10b. Each R-C element corresponds to a single layer within the silica, each layer having distinctive electrical and therefore different physical properties from the other.

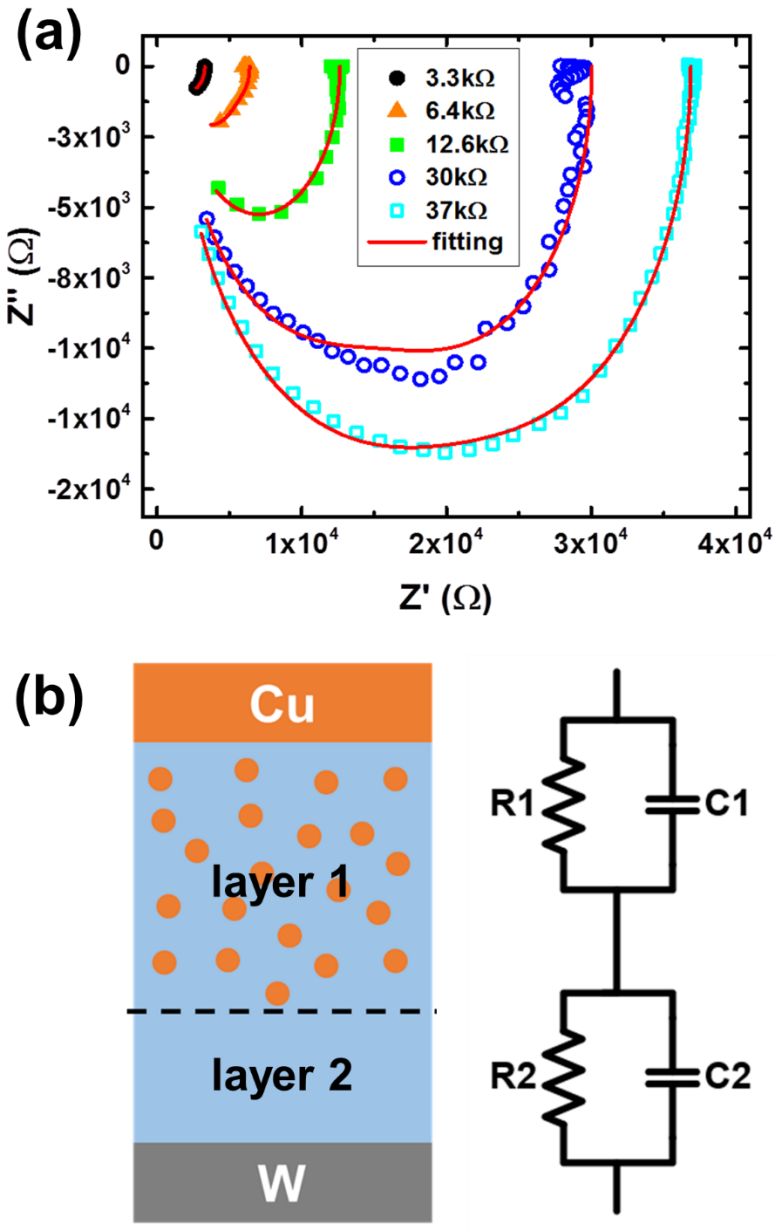


Fig. II.5.10. Impedance spectra of Cu-Cu:silica-W PMC (a) and the equivalent circuits used for fitting (b).

The extracted R-C values are given in Fig II.5.11. The resistance of layer 1 (R1) and layer 2 (R2) both decrease with the lowering of the programmed resistance states. For R1, the reduction is most likely due to Cu ion injection into layer 1 due to the anodic

reaction resulting in more conduction paths. The reduction of R2 is due to Cu ion migration toward the cathode under the influence of the electric field, which can also be treated as a movement of the front of layer, which reduces the effective thickness of layer 2. Meanwhile, the capacitances of layer 1 (C1) and layer 2 (C2) both increase with a decrease of the programmed resistance state. For layer 1, the capacitance increase could be due to an increase in dielectric constant due to Cu incorporation in the oxide or it could arise from the reduction of the effective thickness of the layer as a result of the significant amount of Cu ions near the anodic region acting as a pseudo-anode. For layer 2, the capacitance increase is thought to occur due to the effective thickness reduction in this layer. Furthermore, the resistance changes more in layer 2 than in layer 1 and the capacitance of layer 2 is always larger than layer 1 regardless of programmed resistance state, which indicates that layer 2 is thinner than layer 1 and is the determinant of switching resistance. Thus, from impedance spectroscopic experiments we conclude that two layers with different Cu concentrations exist and the thickness of the Cu poor layer is decreased with the increase of positive voltage.

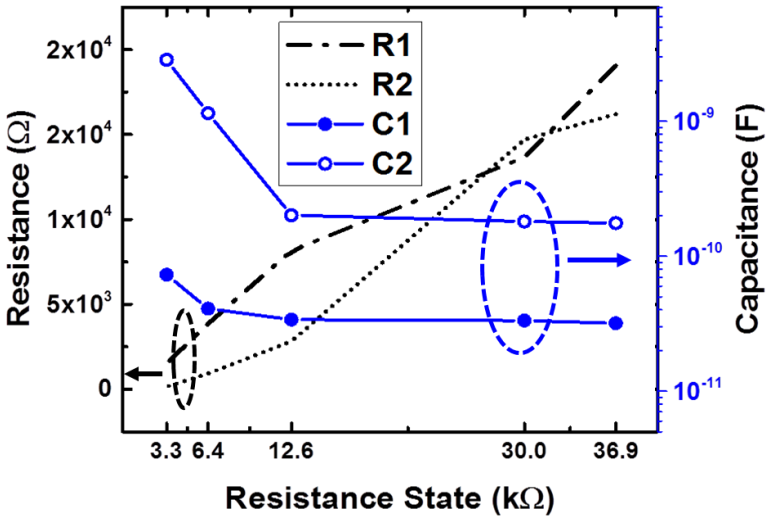


Fig. II.5.11. Extracted resistance and capacitance data from Fig. II.5.10a.

In summary, fabrication method directly influences the property of silica film and the frequency response of PMC with distinct silica film varies a lot. Different PMC devices are modeled by different equivalent circuits. For undoped silica, it is modeled by a single parallel R-C circuit which indicates a homogenous switching layer. While for Cu-doped silica, it is modeled by two parallel R-C circuits in which a high-dope and low-dope region are identified. This work also provides important guidance for Cu-silica PMC compact modeling and circuit design.

CHAPTER III

VOLATILE CU-SILICA PMC FOR SELECTOR

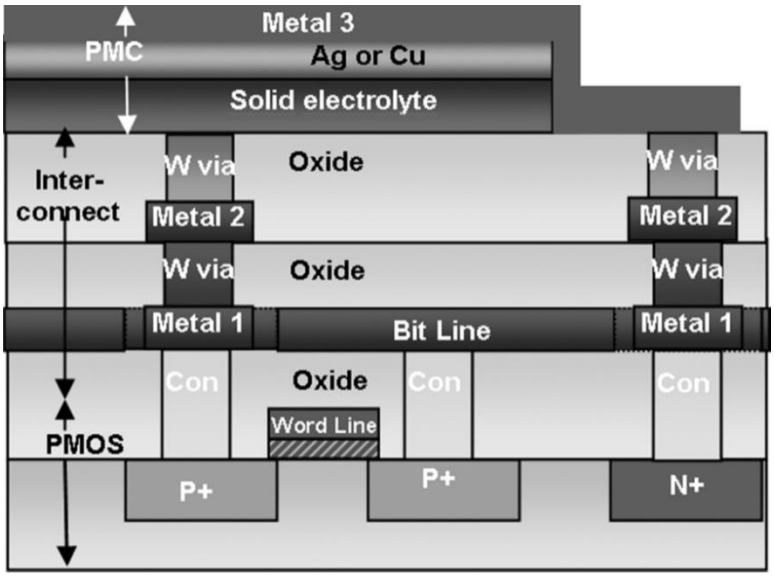
III.1. Memory Arrays

Above discussion demonstrates the performance and reliability of single memory cell. In order to make non-volatile memory product, the individual memory cells have to be connected together to form arrays. At the array level, it is impossible to correctly store and retrieve information without good cell-to-cell isolation. "Sneak paths" current in memory array is one of the fundamental causes of reading and writing failures [149]. In order to resolve this problem, an access device (AD) must be integrated in series with each memory cell.

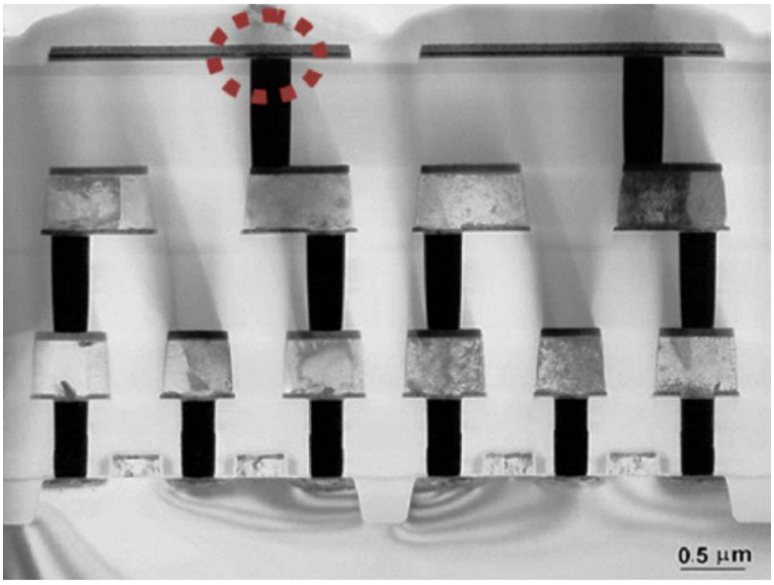
Access devices can be active elements, such as a transistor, or passive elements, such as a diode or other non-linear selector. A one-transistor and one-RRAM (1T-1R) configuration forms the building block of active arrays, whereas a one-selector and one-RRAM (1S-1R) configuration is the basic unit for passive arrays.

III.1.1. Active Array

1T-1R arrays have been demonstrated by various groups [51, 150-155]. In 1T-1R configuration, the selecting transistor is fabricated at the front-end-of-line (FEOL) of CMOS process while the PMC is fabricated at the back-end-of-line (BEOL). Fig. III.1.1. shows an example of the cross section view of 1T-1R configuration, in which the memory cell is integrated at Metal-3, and the TEM cross-section image of a 1T-1R product is shown in Fig. III.1.1b.



(a)



(b)

Fig. III.1.1. Cross-section view of 1T-1R configurations which consists of a selecting transistor (PMOS here), PMC device and interconnects. (a) Schematic illustration. © 2007 IEEE. Reprinted with permission from Ref. [150]. (b) TEM image. Reprint from [51] 2011, with permission from Elsevier.

A schematic of 1T-1R arrays is shown in Fig. III.1.2 In this case, the transistor's source is connected to the bit-line, the transistor's gate is connected to the word-line, the cell's inert electrode and the transistor's drain are tied together and the cell's active electrode is connected to a shared programming voltage (V_{prog}). With this configuration, the cell can be randomly accessed by applying voltages on the addressed word-line and bit-line simultaneously. In order to program the cell, V_{prog} is pulled up to a positive voltage and bitline is pulled down to ground, in the meantime, the wordline is positively charged (for NMOS) to turn on the transistor, thus a positive voltage (V_{active} - V_{inert}) is developed across the PMC to create the conductive filament. Similarly, to erase the cell, the bitline voltage is high and the V_{prog} is grounded, by turning on the transistor, a negative voltage is built across the PMC to dissolve the filament.

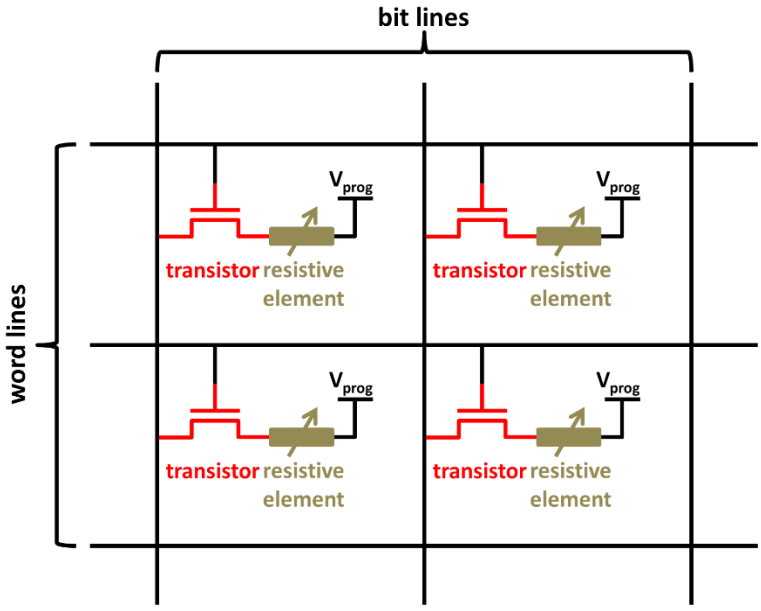


Fig. III.1.2. Schematic of 1T-1R architecture. Each node consists of a PMC and a transistor. Reproduced from [37]. With permission of Springer.

Belmonte et al. studied 1T-1R integrated Cu-silica PMC and compared its performance to Cu-Al_2O_3 PMC [138]. They found that CBRAM with a silica switching layer works better than its counterparts when programming current is small (< 10 μA). This low power attribute of silica based PMC is desirable for low power applications, such as embedded memory for code storage in IoT devices. However, considering that the area of an individual storage unit 1T-1R is governed not by resistive switching element but by the selecting transistor, which is typically $20F^2$ to $6F^2$, PMC with 1 T-1R configuration loses its advantage when competing with NAND Flash ($4F^2$) for massive data storage, especially with the continuous maturation of 3D NAND technology.

III.1.2. Passive Array

A passive array differs from active array in that it employs a two terminal passive device instead of transistor for accessing device. This passive device is also known as a selector which has a non-linear voltage-current relationship. Every selector has a non-zero threshold voltage, below this voltage, the selector is effectively off and the current is small, while above the threshold voltage, the selector will be turned on and the current will increase dramatically. The ideal I-V curve of a selector device is illustrated below in Fig. III.1.3 in which the selector device turns on at threshold voltage of ±1 V. As demonstrated in this figure, the selector has a threshold switching characteristics, which means that the device will switch from LRS back to HRS automatically once the applied voltage is below the threshold voltage. This threshold switching behavior is the fundamental difference between selector and PMC.

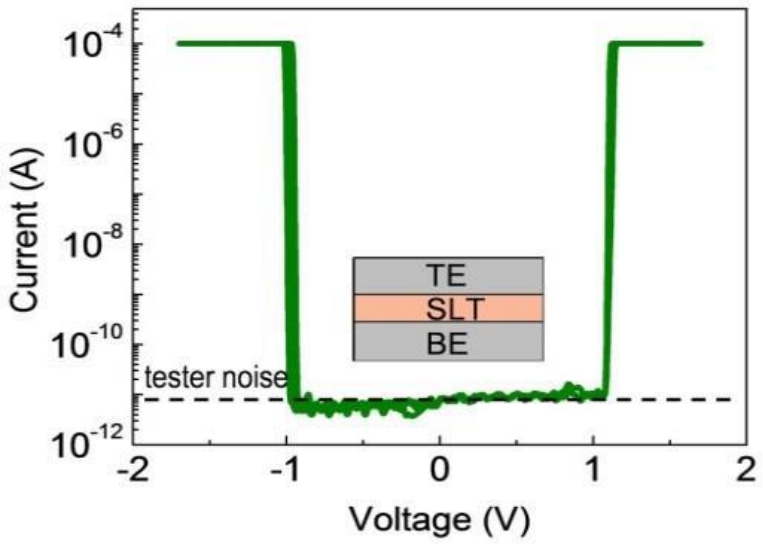


Fig. III.1.3. DC I-V characteristics of ideal selector device. © 2014 IEEE. Reprinted with permission from Ref. [156].

Since both selector and PMC are two terminal devices with a same "MIM" vertical structure, they can be easily integrated together by simply stacking one on top of the other. This results in the 1S-1R configuration which is illustrated in Fig. III.1.4a. The elimination of three terminal transistors leads to the most compact circuit layout – $4F^2$. The crosspoint array made by 1S-1R stacks is shown in Fig. III.1.4b, in which a 1S-1R stack is presented at every overlap region between top and bottom metal lines. Moreover, the passive array can be further stacked to create an ultra-dense 3D crosspoint (Fig. II.1.4c) memory array which can compete with 3D NAND Flash for massive data storage.

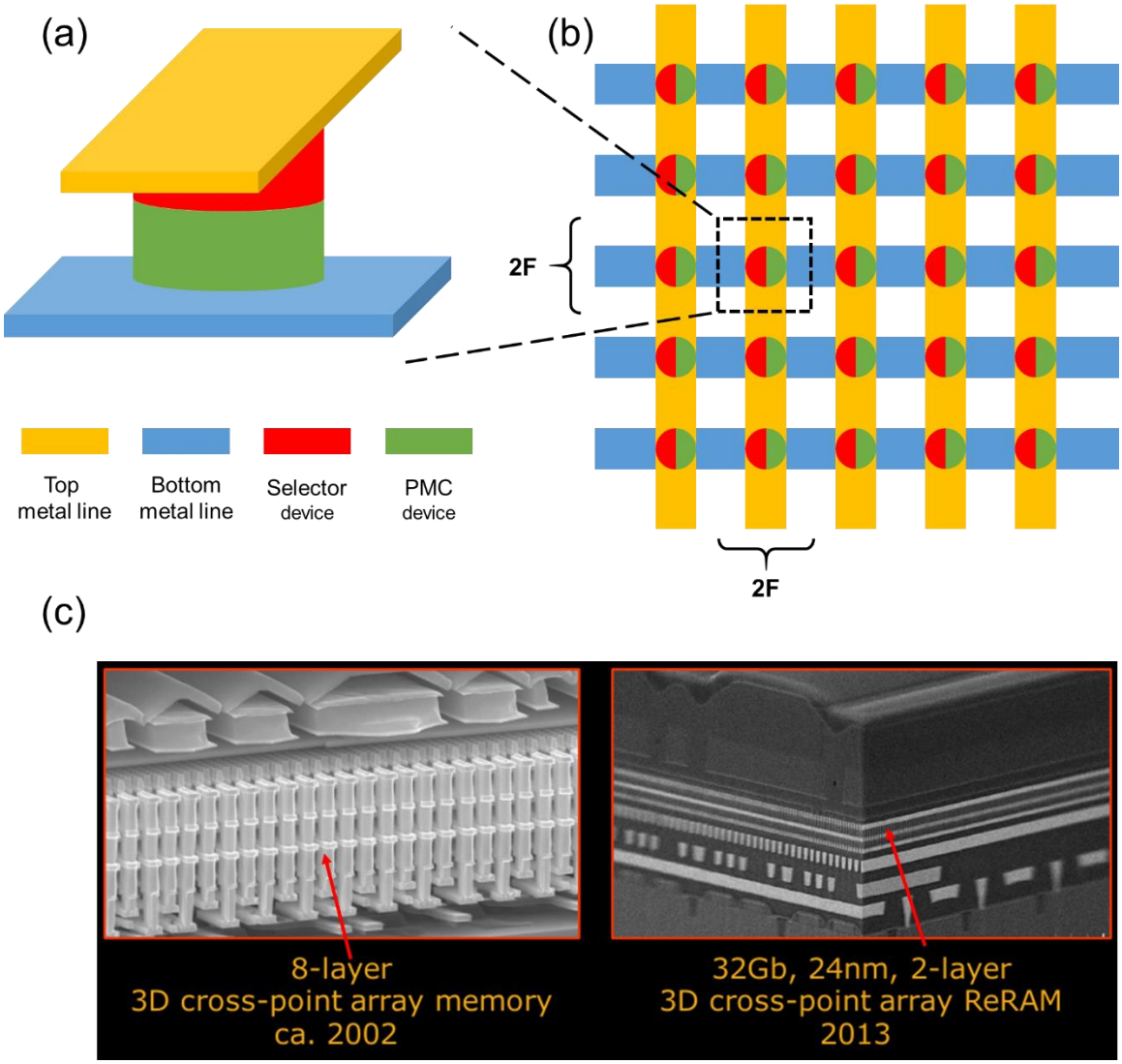


Fig. III.1.4. (a) individual 1S-1R configuration, (b) cross point $4F^2$ layout, (c) TEM image of WD's 3D cross point memory array [109].

The architectural schematic of 1S-1R array is illustrated in Fig. III.1.5. Memory cell are connected in series with selector and they can be randomly accessed by applying voltages on corresponding word-line and bit-line. For example, to program an individual cell, a positive voltage is applied to the bit-line while the word-line is grounded; the cell can be erased with a reversed voltage polarity.

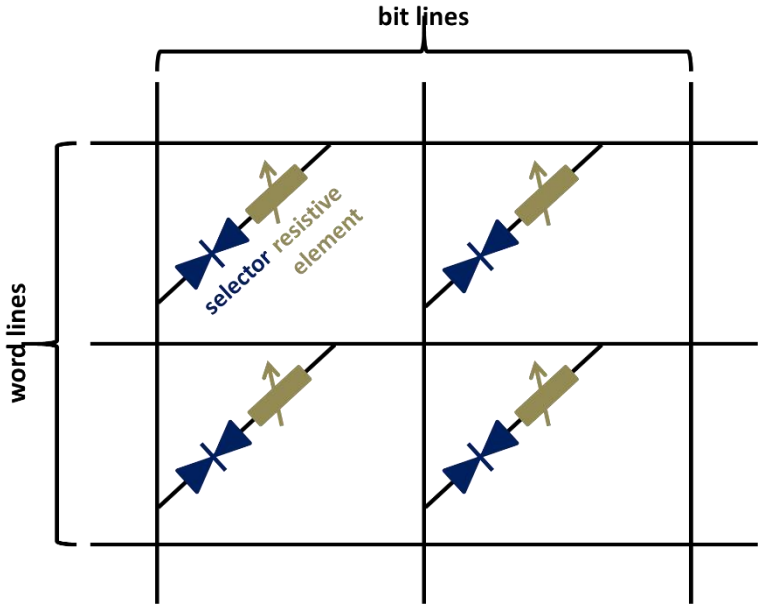


Fig. III.1.5. Schematic of 1S-1R architecture. Each node consists of a PMC and a selector. Reproduced from [37]. With permission of Springer.

III.2. “Sneak-Path” Current Inhibition in Passive Array

Two terminal selectors are used in crosspoint array to provide cell-to-cell isolation. To demonstrate how selector helps in solving “sneak-path” current problem, it is required to understand what is “sneak-path” current. Fig. III.2.1 illustrates the “sneak-path” current in a 2 x 2 crosspoint array without selector device. Suppose the device located at the bottom right corner is going to be read, which is in HRS. A reading voltage is applied to the corresponding top metal line and bottom metal line and a small reading current (marked by blue arrow in Fig. III.2.1) is expected. However, since the three neighboring memory cells are in LRS, a big reading current (marked by orange arrow in Fig. III.2.1) which passes through the three LRS devices will be detected instead. This unwanted big current is called “sneak-path” current and it causes a false reading.

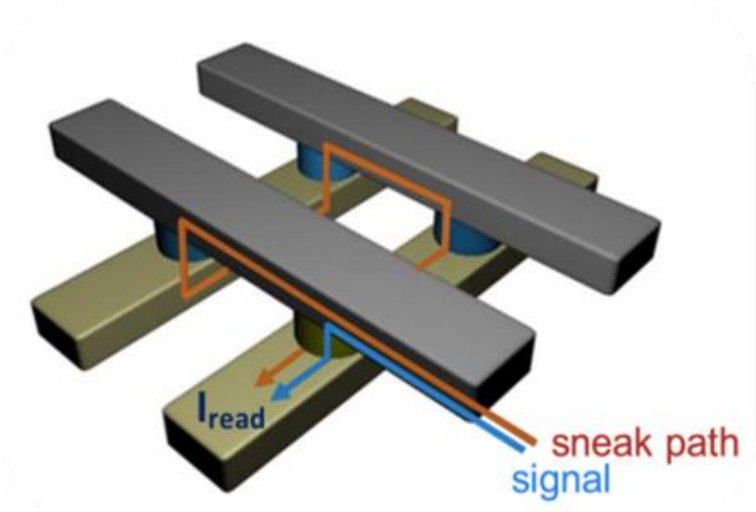


Fig. III.2.1. Sneak-path issue in crosspoint memory array. Source Crossbar Inc.

By adding a selector device to every memory cell, combining with special reading (or writing) scheme, the "sneak-path" current can be eliminated. One example of reading 1S-1R memory array is demonstrated in Fig. III.2.2. The three figures in Fig. III.2.2a shows an ideal DC I-V curve of a single memory cell, a single selector and an integrated 1S-1R stack, respectively. In order to read the stored information, a reading voltage is applied to the wordline of targeting 1S-1R stack (the red horizontal line labeled as Vrd in Fig. III.2.2b) and the corresponding bitline is grounded. The reading voltage should be higher than the selector's threshold voltage. Meanwhile, all unselected metal lines are half reading voltage (Vrd/2) biased. The bias scheme for reading is illustrated in Fig. III.2.2b. In such way, only the targeting 1S-1R stack (the upper left corner one in Fig. III.2.2b) sees the full reading voltage, the 1S-1R stacks located either on the top row or the left most column see half of the reading voltage, and all other cells in the array see zero voltage. As shown in Fig. III.2.2a, if the amplitude of Vrd/2 is smaller than the selector's threshold voltage, the

current will be blocked by the selector. Therefore, the resulting current can be only from the selected cell and false reading is resolved. It has to be noted that the amplitude of reading voltage should be designed less than double of the selector's threshold voltage for successful reading operation.

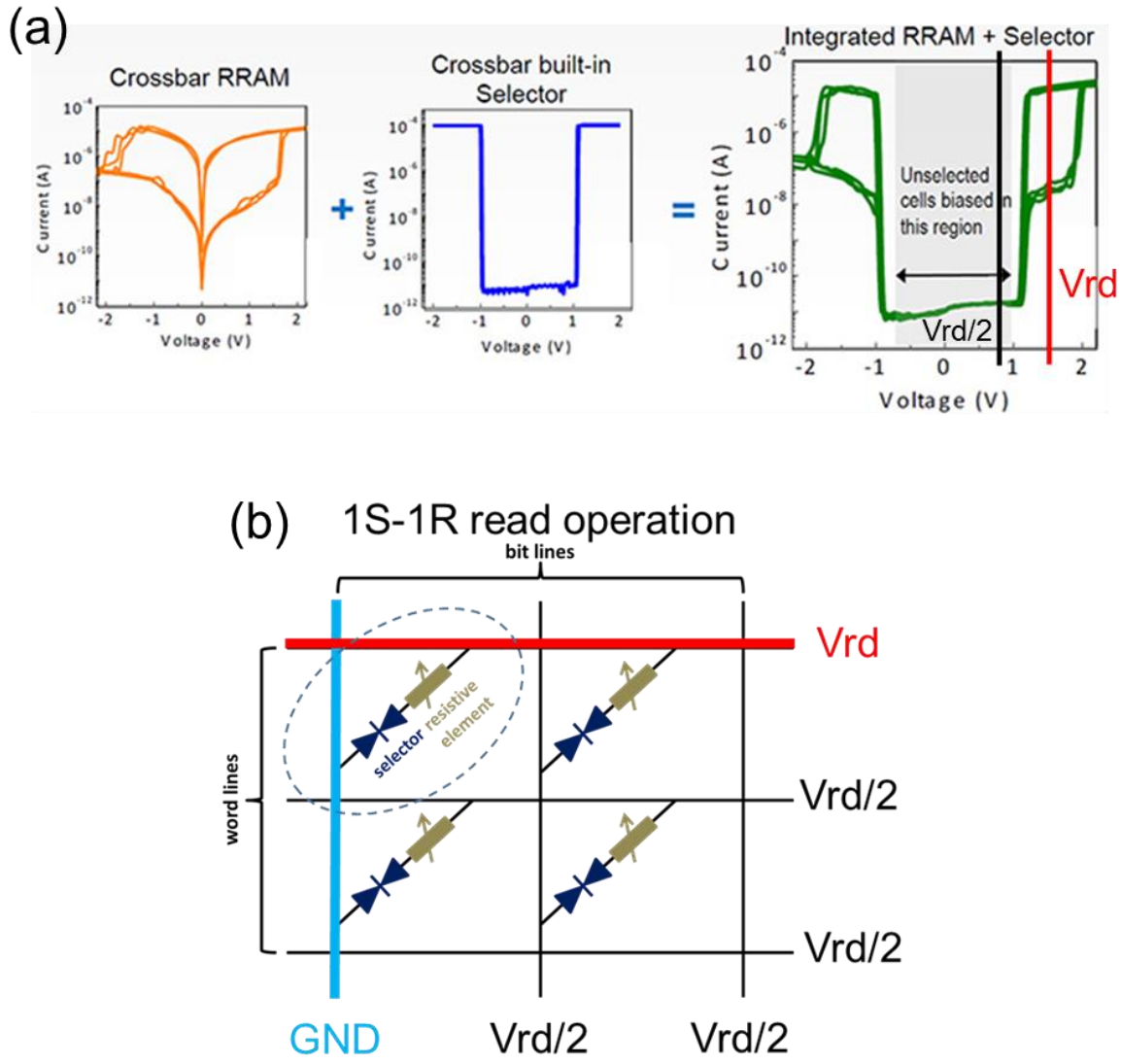


Fig. III.2.2. Illustration of sneak-path inhibition strategy for read operation in crosspoint array [156]. (a) I-V characteristics of 1S-1R stack, source: Crossbar Inc. (b) reading schematic.

Several types of selectors have been proposed including the chalcogenide based Ovonic switch [157], transition oxide (VO_2 and NbO_2) based metal-insulator transition (MIT) devices [158, 159], a mixed-ionic-electronicconduction (MIEC) selector technology [160, 161] as well as above demonstrated Field Assisted Superlinear Threshold (FAST) Selector. Except for the MIEC and FAST selector, the other two selectors (Ovonic, MIT) suffer a high-off state leakage current problem and CMOS compatibility issue. A previous study of Cu-silica PMC demonstrated an inherent diode characteristic based on the creation of a Cu/n-Si Schottky contact [162], which also shows great potential for crosspoint array implementation.

Since PMC is a filamentary technology, the concentration gradient between the metal filament and the surrounding oxide matrix can be gigantic which may allow for fast filament dissolution. Therefore, a PMC can show threshold switching behavior if it is engineered to be a volatile switch by greatly enhancing the filament dissolution rate.

III.3. Volatile Switching in Cu-Silica PMC

For device switching layer, 15 nm porous silica was deposited by e-beam evaporation at a high deposition rate.

Fig. III.3.1 shows the typical volatile switching I-V curve of a 5×5 um^2 Cu/silica/Pt PMC device. The device was swept with a range of compliance currents from 10 nA to 500 μA with a threshold voltage (Vth) between 0.5 V and 0.8 V. For each test, the Cu electrode voltage is first swept from 0 V to +1 V and back to 0 V in one continuous double sweep. Then the Cu electrode voltage is swept from 0 V to −0.8 V and back to 0 V. The device's LRS value is maintained when the positive voltage is sufficiently large; but the filament

ruptures spontaneously when the voltage is reduced to a small, typically positive voltage, thus restoring the device to its HRS condition. This volatility is clearly shown in Fig. III.3.1 by the very low currents measured over the reverse bias range (between 0V and −0.8 V). In all cases the device has spontaneously transitioned to the HRS regime. The results demonstrate that volatility is independent of compliance current up to 500 μA for this Cu/silica/Pt PMC. Moreover, the threshold switching behavior over the 0 to +1V sweep resembles the I-V characteristics of a diode in breakdown. A rectifying ratio of about 5×10^{7} can be obtained if the current is read at ±0.8 V with a 500 μA programming current. The rectifying ratio can be further increased in smaller devices since the HRS resistance is inversely proportional to the device area while LRS resistance is not dependent on device size. Such a high rectifying ratio suggests the potential for this device as a sneak path blocking selector.

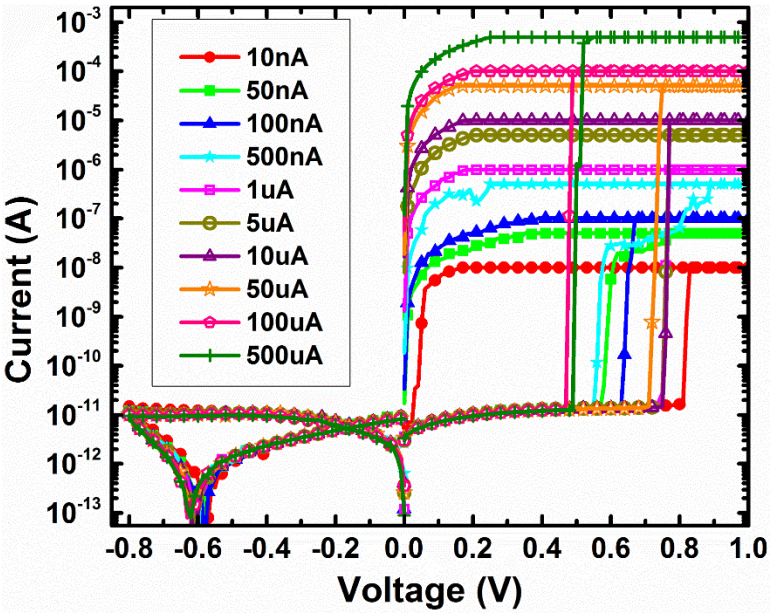


Fig. III.3.1. Volatile switching I-V characteristics of Cu/silica/Pt PMC at different programming current. © 2016 IEEE. Reprinted with permission from Ref. [116].

The HRS stability of the Cu/silica/Pt device was also investigated because this is important for the suppression of sneak path currents. The device was DC swept for 50 cycles with a relatively high programming current (for normal resistive device operation) of 100 μA in order to accelerate the degradation of the HRS. The test schematic is illustrated in Fig. III.3.2a. The switching current is limited by the saturation current of the transistor. The voltage was swept between −0.8 V and 0.8 V and the labeled numbers indicate the sweeping sequence in each cycle. As can be seen in Fig. III.3.2b, the filament spontaneously ruptures even when the positive voltage is still applied and no memory trace was found in the negative voltage side for all repeated cycles. The HRS current is below 10^{-10} A out to −0.8 V and is tightly distributed from cycle to cycle with no obvious degradation being observed. The small variation in HRS current indicates that no significant Cu residues are left in the filament region after it dissolves. It should be noticed that the threshold voltage is not tightly distributed in Fig. III.3.2b. Such variation poses threats to reliable reading/programming operations when the memory cell is integrated, but this problem may be alleviated through a better process control during device fabrication.

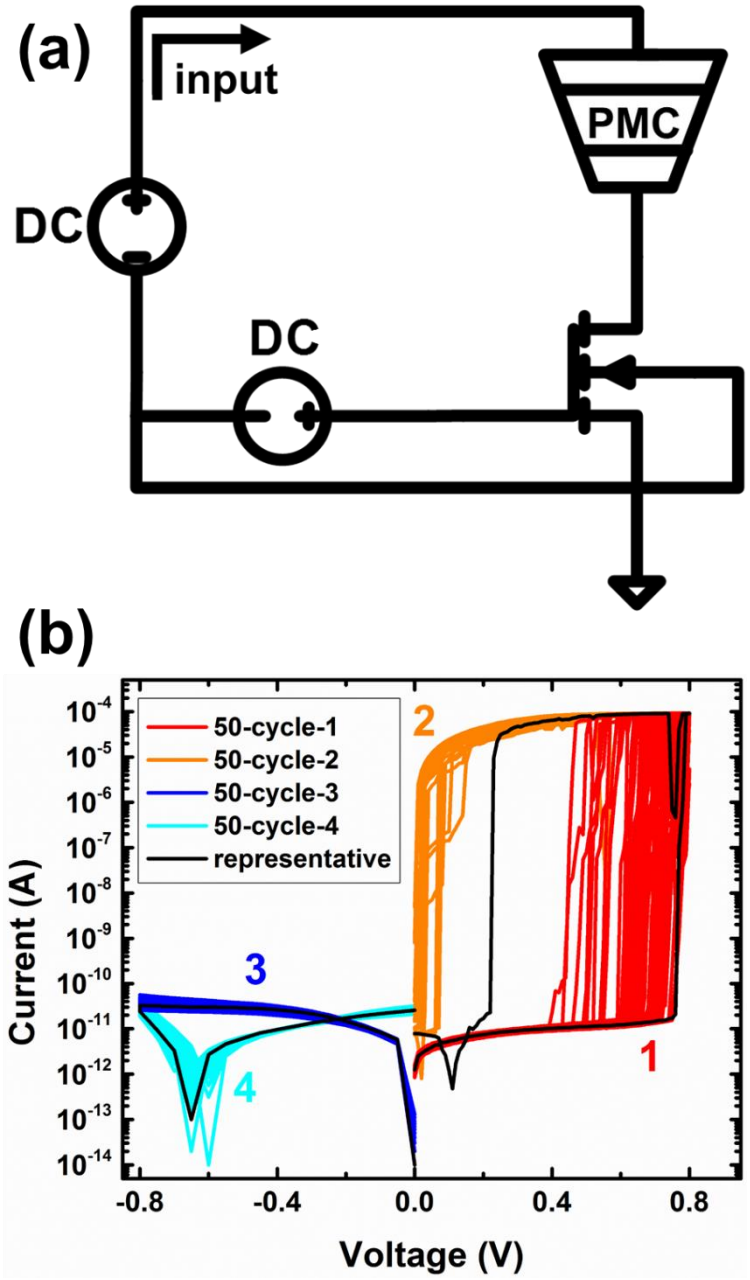


Fig. III.3.2. Test setup schematic (a) and DC cycling result (b) of volatile switching in Cu-silica PMC. © 2016 IEEE. Reprinted with permission from Ref. [116].

Another important property of threshold switching is the volatilizing speed, i.e., the speed of filament rupture when the voltage bias is removed. A pulse test scenario was

conducted to assess this on five Cu/silica/Pt devices and the results are shown in Fig. III.3.3b. The test schematic is illustrated in Fig. III.3.3a. A compliance current of 100 μA was set with the transistor. Write pulses were first generated to program the devices to their LRS followed by smaller amplitude but longer read pulses as shown in Fig. III.3.3b. No bias was applied in the period between the write and read pulse. The write pulse was 1.2 V high and 10 ms long, the read pulse was 0.3 V high and 20 ms long, and a minimum of 1 ms time gap was chosen in order to clearly distinguish the effects of the write and read pulses. By comparing the waveform received by channel-1 (output-1) and channel-2 (output-2) of an oscilloscope, it can be seen that the devices were programmed to their LRS in a few milliseconds. The LRS were randomly programmed to be 390 Ω, 860 Ω, 1.83 k Ω, 2.04 k Ω and 2.45 kΩ, and, all of devices quickly recovered to their HRS in less than 1 ms once the voltage is removed as a negligible readout voltage was observed in output-2 over the read time interval.

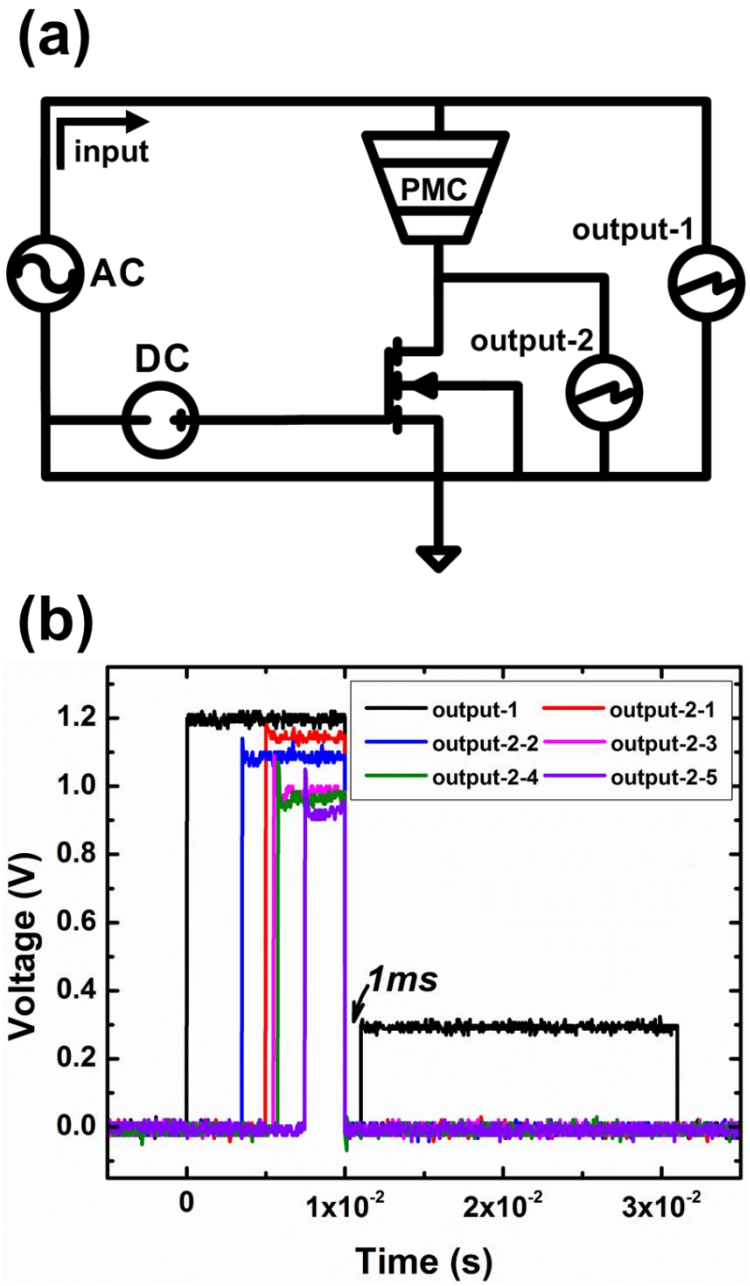


Fig. III.3.3. Test setup schematic (a) and transient pulse testing result (b) of volatile switching in Cu-silica PMC. © 2016 IEEE. Reprinted with permission from Ref. [116].

It is worth noting that the volatile threshold switching behavior is preserved in the Cu/silica/Pt devices even for a compliance current as high as 500 μA. This is more than

enough to achieve non-volatile switching in resistive memory devices according to previous reports [163, 164]. In our undoped devices, simply increasing compliance current is not enough for the device to exhibit memory switching, i.e., stable filament formation. The volatility of the Cu/silica/Pt device is likely due to the dissolution of Cu filament in the porous e-beam evaporated silica, as shown in Fig. III.3.4.

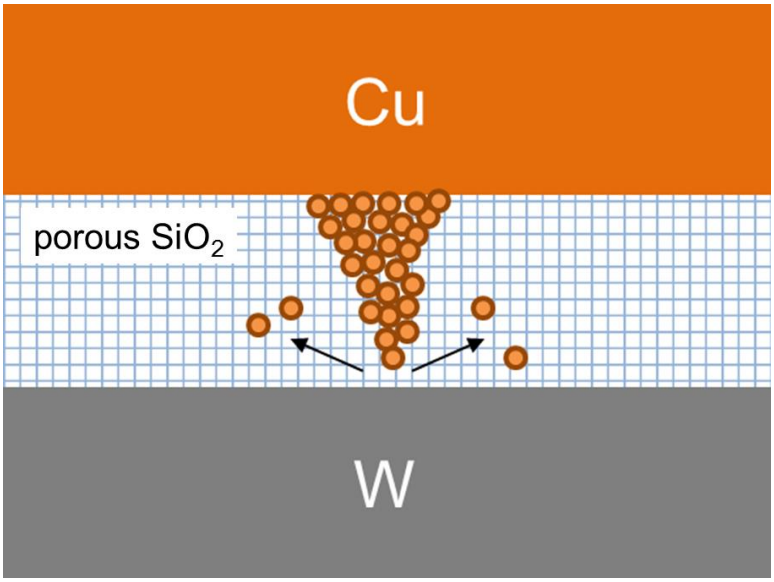


Fig. III.3.4. Illustration of Cu filament dissolution in e-beam evaporated porous silica.

According to Fick's first law [165]

$$J_{diff} = -D\frac{dC}{dx}$$

the diffusion flux J_{diff} is a function of multiplication of diffusion coefficient D and concentration gradient. Since the surrounding silica matrix is not doped with Cu, the concentration gradient between the Cu-rich conducting region and the surrounding

(undoped) oxide is significant which enables fast dissolution of Cu filament. Furthermore, the diffusion coefficient is determined by the equation

$$D = \alpha * \exp(^{-E_a}/_{kT}) * \exp(^{-E_b}/_{kT})$$

where α is a constant, the first exponential part represents the frequency of random jump of Cu atoms and the second exponential part indicates the probability of finding vacancy in an adjacent lattice site. In porous silica, it is much easier to find an adjacent vacant site for Cu to occupy. Thus, the diffusion coefficient for e-beam silica is larger than CVD or thermal silica, the enhanced diffusion coefficient further accelerates the dissolution of Cu filament.

It should be mentioned that absorbed moisture in porous oxides can be another reason for filament instability. Recent cyclic voltammetry (CV) studies show that an electromotive force (emf) exists in the presence of moisture in PMC devices [95], and such emf creates an additional voltage that oxidizes the Cu filament and impacts LRS retention [122]. Finally, considering that the selector is strongly rectifying in the voltage range used, a 1S1R configuration would only suit unipolar memories where programing and erasing occurs with the same voltage polarity. For bipolar switching devices, either a 2S1R configuration, with two selectors connected in an anti-parallel configuration, or devices fabricated with Cu/porous silica/Cu stacks, would be required for a successful erase operation.

III.4. Total Ionizing Dose Test on Cu-Silica Selector

The above section demonstrates that a Cu-silica PMC can be fabricated to exhibit threshold switching when it has a low concentration of Cu in the thin silica ion conducting

switching layer. Investigating the impact of TID on the resistance evolution of the undoped silica layer is critical since the selector's OFF-state resistance determines its current blocking capability.

III.4.1. Gamma-Ray Irradiation Experiment

In addition to Cu-silica PMC, Ag-silica PMC was also fabricated, the detailed fabrication process for Ag-silica is similar to Cu-silica. Fig. III.4.1a illustrates the cross-sections of the two PMC stacks. The devices top view are shown in Fig. III.4.1b.

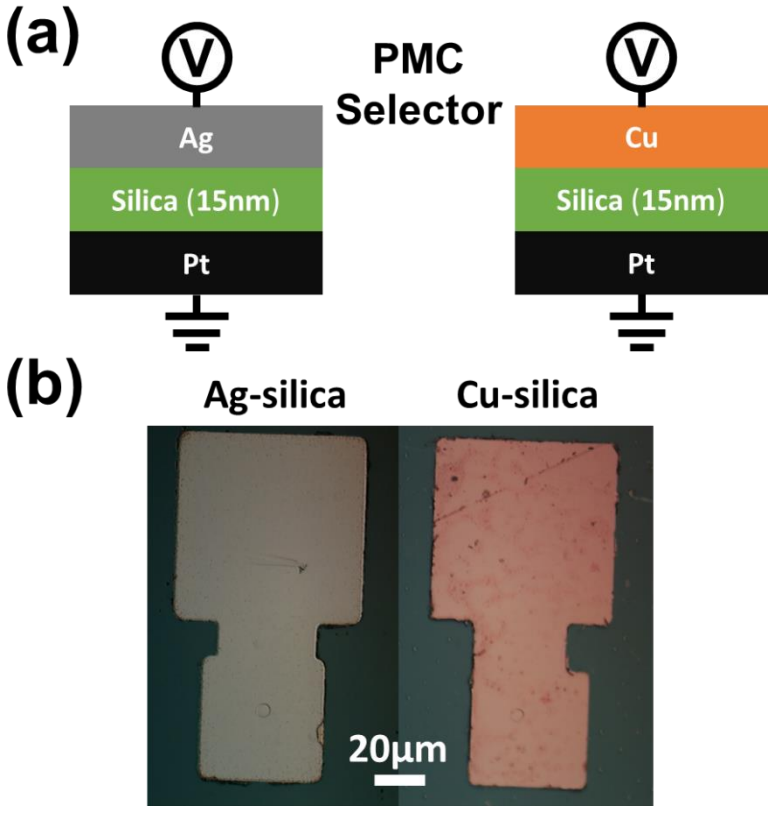


Fig. III.4.1. (a) Cross-section illustration of silica based volatile PMC selector, (b) Optical microscope image of PMC selectors, from left to right are Ag/silica/Pt and Cu/silica/Pt.

The scale bar is 20 μm. The circular features centered in the smaller pads are the actual 5 μm devices.

Fig. III.4.2 demonstrates the resistive switching I-V curves of silica based PMCs with an Ag anode (Fig. III.4.2a) and a Cu anode (Fig. III.4.2b). Both devices were repeatedly swept for 10 cycles. The Ag-silica device has a positive threshold voltage of ~200 mV which is lower than the Cu-silica threshold voltage, which averages 600 mV. The difference in threshold voltage is consistent with the lower diffusion barrier for Ag (1.24 eV) than for Cu (1.82 eV) in silica [166], which would allow Ag filaments to form more readily. Note also that there is negligible LRS current over all the negative bias range for both silica based PMCs, which indicates that the filament has ruptured prior to the application of a negative voltage. As discussed above, the rupture of the filament may be due to the active metal concentration gradient between the filament and its surrounding silica matrix.

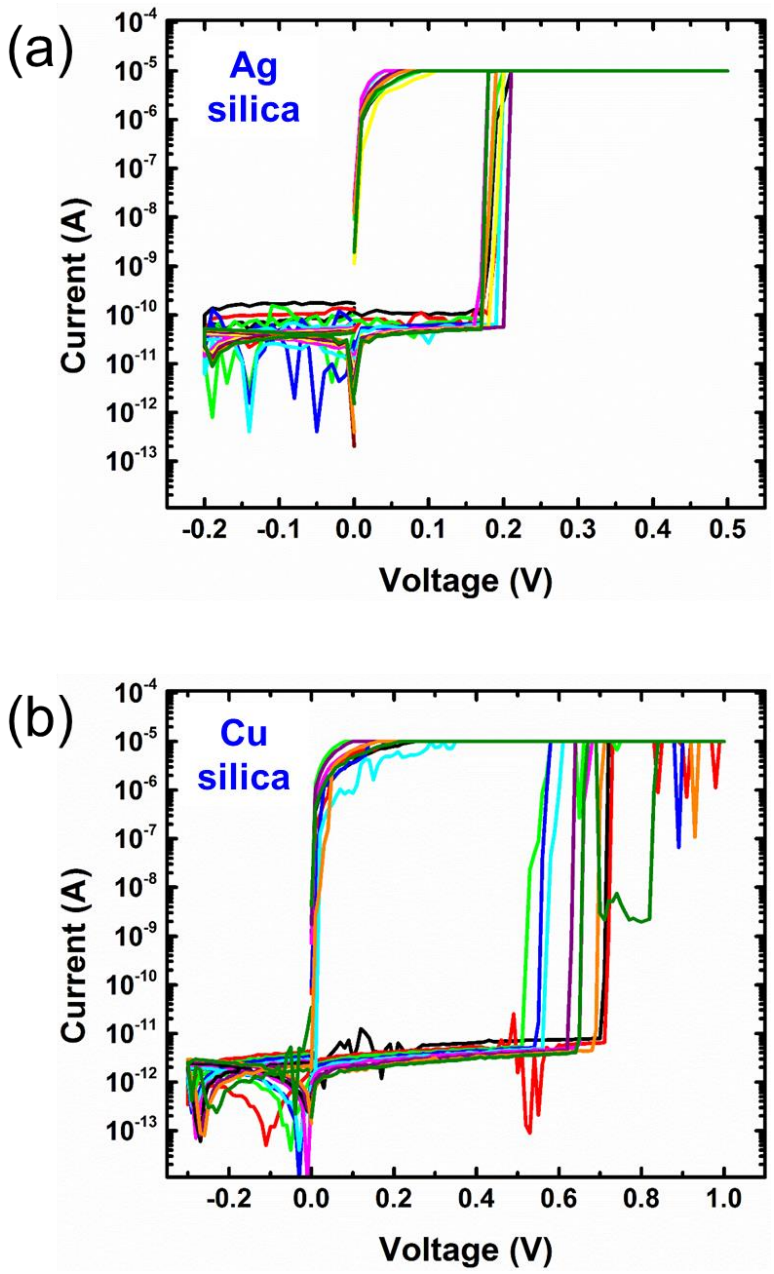


Fig. III.4.2. Volatile resistive switching of PMC with e-beam silica switching layer. (a) PMC with a Ag anode and (b) PMC with a Cu anode.

The gamma-ray irradiation setup is the same as section II.4. The two types of PMCs were exposed to ^{60}Co gamma-rays in a Gammacell 220 with all electrodes floating. To

evaluate the effect of ionizing radiation on resistance stability, the devices were step-stressed to a maximum TID of 5 Mrad(silica). The high virgin-state resistance, defined as the resistance of a PMC prior to any switching event, was sampled at–50 mV at each dose level shortly after being taken out of the radiation chamber. To avoid any disturbance caused by a redistribution of metal ions during the I-V sweeps, the resistive switching (I-V) characteristics were obtained only after the completion of the 5 Mrad(silica) irradiation.

III.4.2. Gamma-Ray Irradiation Results and Analysis

III.4.2.1. TID Effects on Virgin-State Resistance

Fig. III.4.3 demonstrates the virgin-state resistance evolution during gamma-ray exposure for the two selector types. Three 5 μm diameter devices for each type of PMC selector were tracked and the results are normalized to the virgin HRS resistance prior to irradiation. As shown in this figure, the ratio of pre- and post-irradiated virgin-state resistance is around 1, thus, there is no significant change in virgin resistance of the PMCs with a silica switching layer. The absence of resistance degradation of Ag-silica and Cu-silica PMCs suggests that Ag or Cu is not incorporated into the silica layer by gamma-ray exposure.

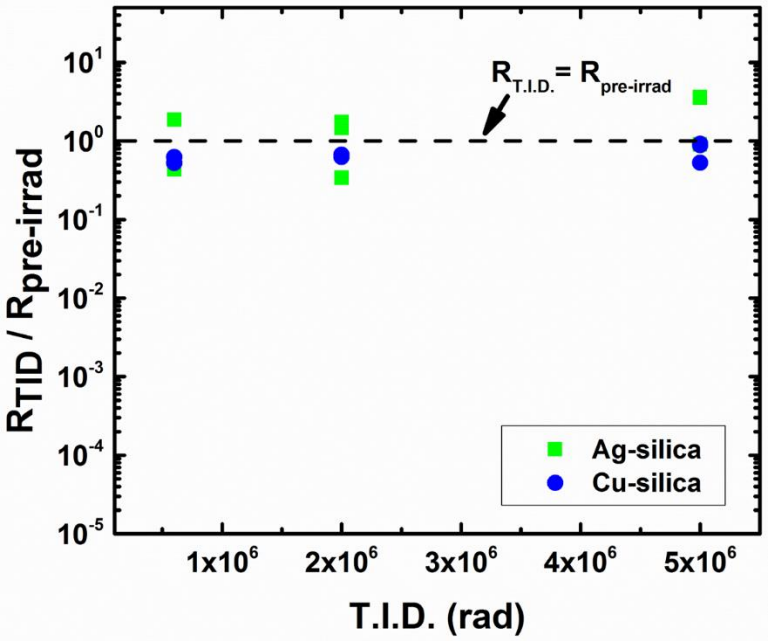


Fig. III.4.3. Effects of TID on virgin-state resistance of Ag-silica (solid squares) and Cu-silica (solid circles). © 2017 IEEE. Reprinted with permission from Ref. [88].

III.4.2.2. TID Effects on Switching Resistance of Silica PMC Selector

After the first cycle resistive switching (or electroforming), the switching layer is altered. Additional defects may be introduced by resistive switching. How TID impacts the electrically altered dielectric layer is studied through a comparison of resistive switching prior to and after gamma-ray exposure.

Because the silica devices are intended to be used as selectors, we chose a more relevant parameter to measure. Defined in the equation below, selectivity quantifies the device's ability to suppress sneak path current from nearby crosspoint cells,

$$Selectivity = I_{LRS}/I_{HRS}$$

Here the HRS and LRS current are extracted at 0.1 V for a Ag-silica selector and 0.35V for Cu-silica selector, which are all half of the selector's threshold voltage. Fig. III.4.4a

and III.4.4b demonstrate how ionizing radiation impacts the selectivity of Ag-silica and Cu-silica selector devices, respectively. The results are plotted as cumulative probability distributions. For each selector type, five 5 μm devices were tracked and each one was switched for 10 cycles before and after ionizing radiation exposure. As shown in both figures, the selectivity of pre-irradiated and post-irradiated samples randomly overlap each other, suggesting that gamma-ray irradiation has little impact on selectivity. Since the LRS current at the extracting voltage has already reached the compliance current limit (10 μA), the ILRS is actually a constant value (10μA) in the selectivity calculation. The well preserved selectivity is actually attributed to the fact that the IHRS does not change with TID. The difference in TID response between silica selector and ChG memory/sensor implies that the gamma-rays do not photodope anode metal into silica. In addition, it can be also observed from Fig. III.4.4 that the selectivity of Cu-silica is about an order of magnitude higher than Ag-silica. This is because of the Cu-silica selector's high HRS resistance. The reason why a Cu-silica selector has a higher HRS resistance than an Ag-silica selector needs further investigation. It may be related to the higher Ag mobility in silica than Cu. Nevertheless, it indicates that the Cu-silica selector possesses a better current blocking capability.

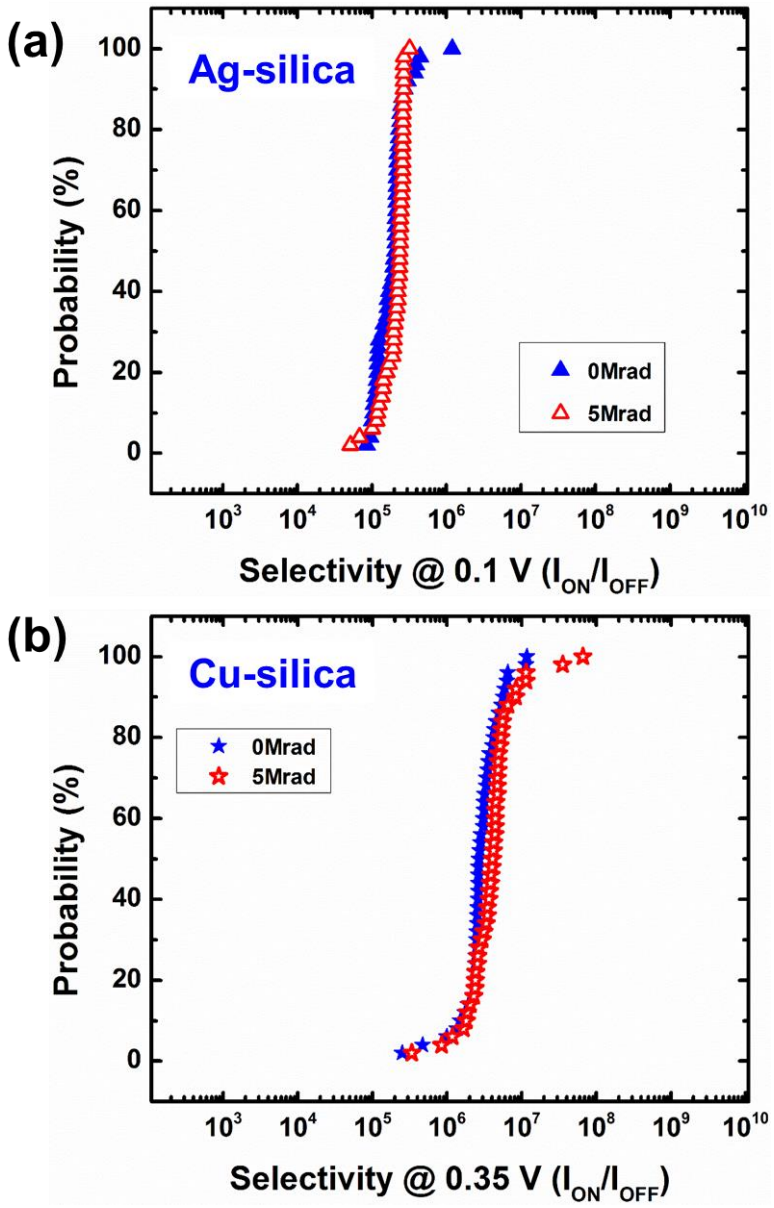


Fig. III.4.4. Cumulative distribution of selectivity response to TID of (a) Ag-silica and (b) Cu-silica. © 2017 IEEE. Reprinted with permission from Ref. [88].

III.4.2.3. Analysis of TID Results

For silica based PMCs, the selectivity of both Ag and Cu devices remains almost unchanged since the virgin-state resistance or the HRS is not affected by TID. This suggests

that radiation enhanced diffusion of Cu or Ag into silica is negligible. The lack of such radiation-induced doping has been discussed in previous section, i.e. larger bandgap of silica, positively charged traps in silica. In addition to density function theory (DFT) calculation of Cu-silica system, DFT of Ag-silica system is also demonstrated here which shows similar results. We show in Fig. III.4.5 the projected density of states (PDOS) for both materials systems. In all cases, the metal atoms are in local interstitial equilibria. For the silica:M material systems (Fig. III.4.5a and III.4.5b), the valence and conduction band edges are at ~ -7.0 eV and ~ -2.0 eV, respectively, as determined by the oxygen PDOS edge for the valence band and by the silicon PDOS edge for the conduction band. Here, the metal atoms introduce discrete levels in the band gap. Note that the two peaks are actually the result of a spin-unrestricted calculation, where only the lower is occupied. We predict that both Ag and Cu can be neutralized in silica. In fact, for high metal densities, most of the metal species should be charge neutral.

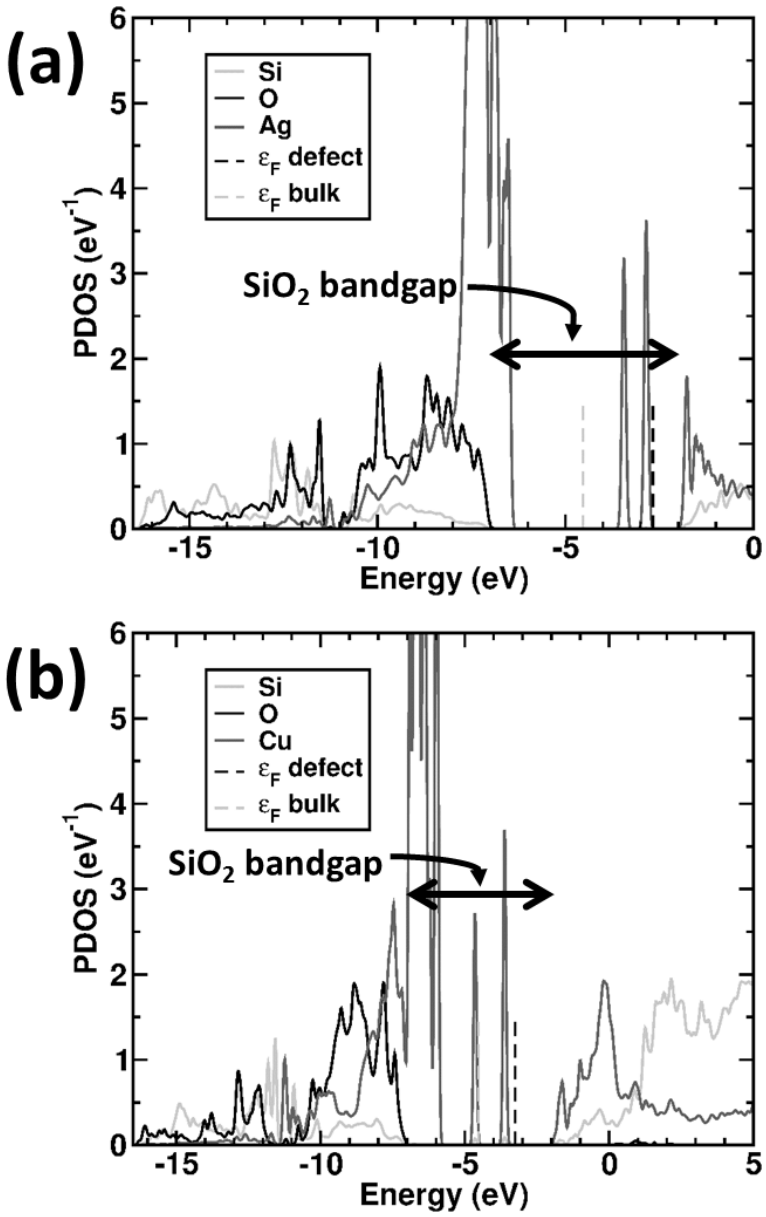


Fig. III.4.5. Results of DFT calculations showing the projected density of states (PDOS) for (a) Ag- silica system and (b) Cu- silica system. © 2017 IEEE. Reprinted with permission from Ref. [88].

Our experiments clearly show that in terms of TID effects on resistance stability, the dielectric material matters more than the active metal. Active metal atoms, either Ag or

Cu, are hard to be incorporated into silica switching layer. These TID results provide meaningful guidance for the design of radiation hardened crosspoint memory arrays.

CHAPTER IV

CU-SILICA PMC BASED ELECTRONIC SYNAPSE FOR NEUROMORPHIC COMPUTING

IV.1. Bio-Inspired Neuromorphic Computing

Artificial intelligence (AI) is gaining great popularity in recent years due to its impacts on machine learning, data mining as well as advance computer vision. However, it has yet been fully realized after years of unremitting effort. Although computing capability has been significantly improved thanks to the industry's adherence to Moore's law [167], the efficiency of executing complex instructions, especially for pattern recognition, is bottlenecked by the binary-based von Neumann architecture. For example, despite being equipped with 147456 processors and a 144 TB memory, IBM's Blue Gene supercomputer is still 83 times slower than a cat brain when performing cortical simulations [168]. Improving computing power by simply adding transistors is an inefficient strategy, particularly since silicon based CMOS technology is approaching its scaling limit, and thus novel computing paradigms have to be developed to realize human brain functionality. In this respect, bio-inspired neuromorphic computation has been extensively investigated as an alternative to the von Neumann approach. In neuromorphic computing, the computing and memory are tightly integrated together, thus, it is a highly parallel computing paradigm which is superior to Von Neumann machine in terms of pattern/voice recognition as well as lower power consumption.

Neuromorphic computing system mimics the way that human brain operates. The basic unit of human brain is neuron which is shown in Fig. IV.1.1. A neuron is composed

of a body and a tail, the body has dendrites which receives electrical stimulus from other neurons, the stimulus gathered by all dendrites are sent to nucleus, if the cumulative energy is larger than a certain threshold, the nucleus will fire and produce a new stimulus which will propagate through the tail (axon) and output to the dendrites of another neuron. Neurons are connected by synapse which is a connection point between the pre-neuron's axon terminal and post-neuron's dendrite, as illustrated in Fig. IV.1.1. The energy of input stimulus depends on the conductance of synapse. The higher the synaptic conductance, the faster the energy accumulates and the easier the nucleus fires. The synaptic strength (conductance) is changeable. It can be adjusted through the number of neurotransmitters released by the presynaptic terminal when input stimulus are received. These neurotransmitters diffuse across the synapse and bind to the specialized receptors in the postsynaptic membrane. The binding of transmitter molecules to the receptors triggers direct or indirect opening of channels for ion transportation which causes the conductance change in the postsynaptic terminals [169]. Biological learning occurs through gradually and continuously changing the strength of the synaptic connection. It also should be noted that, in biological learning processes, the increase of synaptic strength is known as potentiation while decrease of strength is referred to as depression.

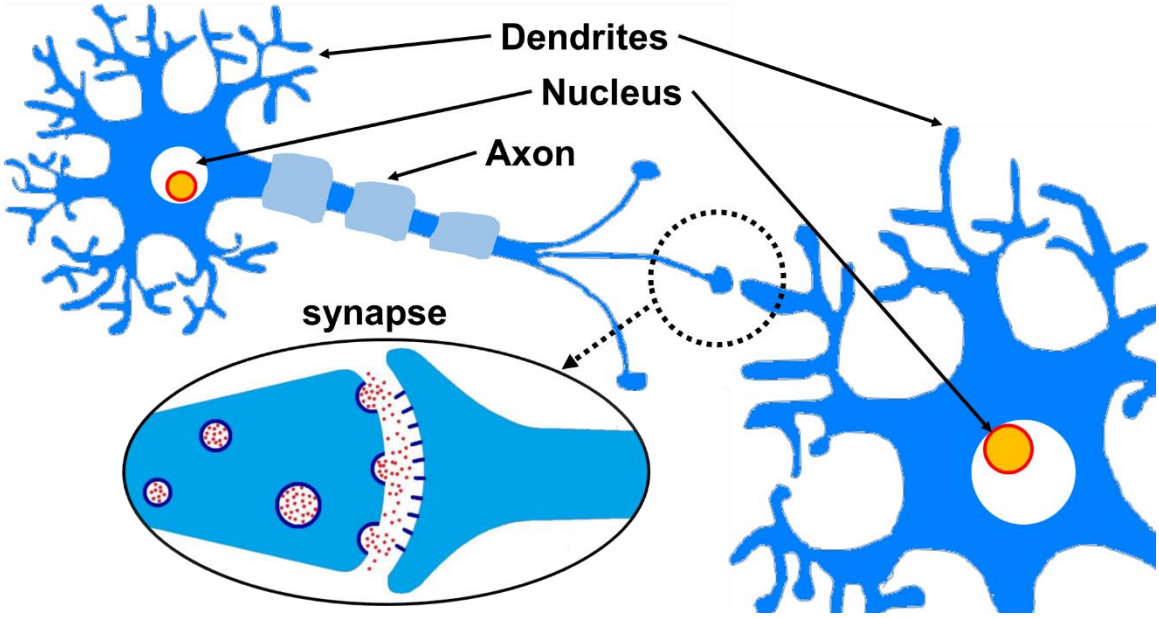


Fig. IV.1.1. Schematic representation of a biological synapse between two neurons, i.e. a presynaptic neuron and a postsynaptic neuron [62]. © IOP Publishing. Reproduced with permission. All rights reserved.

Base on the biological operation described above, a mathematical model is built which is shown in Fig. IV.1.2. In this figure, the vector [x^1, x^2… x^m] indicates the input stimulus, the vector [w^1, w^2 … w^m] represents the synapses conductance, the product of vector [x^1, x^2… x^m] and vector [w^1, w^2 … w^m] is summed up via the "Summing Node" block,

$$A = \sum_i x_i w_i$$

and the sum-up value A is input to the "Threshold Function" block which is usually a "sigmoid function",

$$Output = \frac{1}{1 + e^{-t}}$$

the resulting *Output* is sent to the neurons in next layer as their input value. This mathematical model emulates how nucleus works.

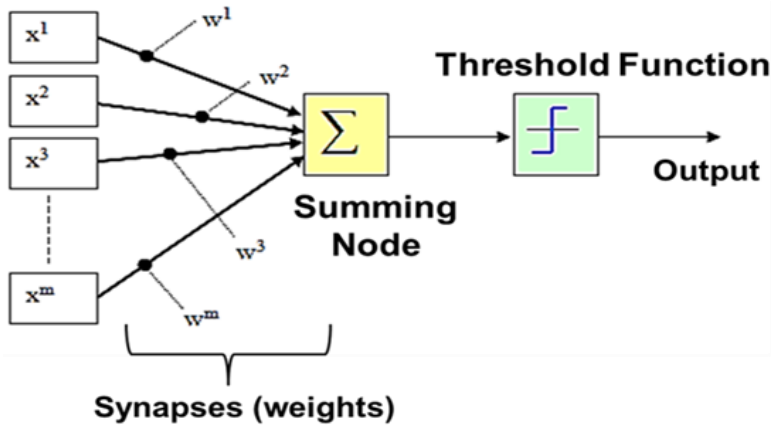


Fig. IV.1.2. A mathematical emulation of bio-inspired neuromorphic computing.

By connecting many of the neurons together, an Artificial Neural Network (ANN) is formed. Fig. IV.1.3 demonstrates one example of ANN which is known as Multilayer Perceptron (MLP) ANN. It consists three neuron layers (empty circles), i.e. an input layer, a hidden layer and an output layer. These neurons are connected together by synapses (solid black lines). Based on the mathematical model discussed above, the outputs of output layer depends on its connectivity (synaptic weights) with hidden layer as well as the outputs of hidden layer, which further depends on the outputs of the input layer and the connectivity between these two layers. Therefore, by adjusting the synaptic weights (w^m), the outputs will have special patterns which can be used to identify images or voices, this is how learning occurs. The synaptic weights are adjusted by a so-called training process where pre-defined input-output pairs are used to update the weights of synapse. After that, the ANN can perform real tasks, in which a prediction is made from unknown inputs. Based

on this idea, IBM has developed a neuromorphic chip which has been demonstrated to be able to perform handwritten digits recognition [170].

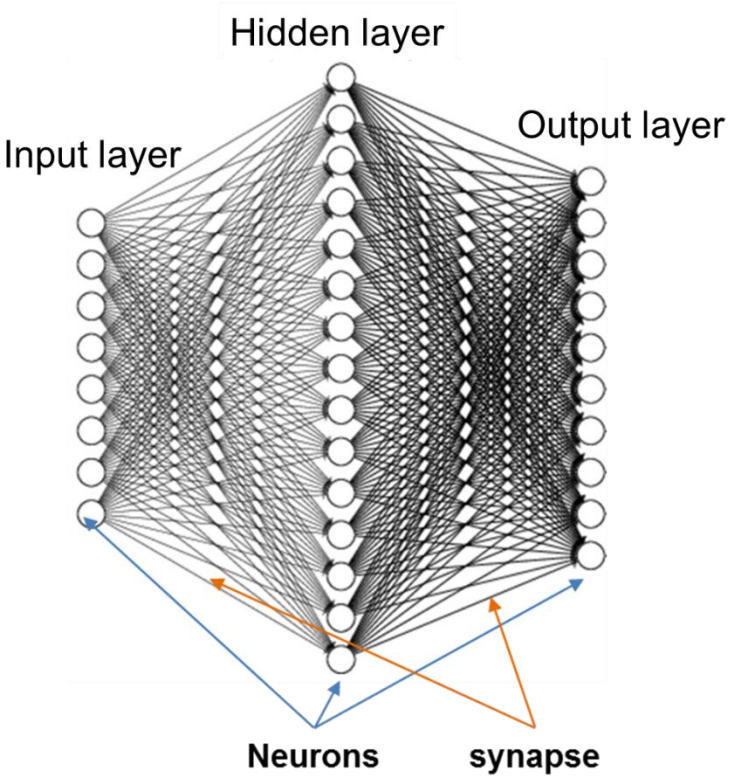


Fig. IV.1.3. Multilayer Perceptron – an example of Artificial Neural Network.

It is obvious that the synapse is the most critical element in ANN since its adaptability directly impacts the performance of ANN, thus, finding a reliable electronic synapse is critical for the implementation of ANN hardware. The electronic synapse must possesses a similar plasticity, i.e., gradual conductance/resistance change, in order to emulate a biological synapse. For CMOS based synapse, tens of transistors and capacitors are needed to build a single electronic synapse [171]. However, due to the fact that the typical number of neurons in a human brain is around 20 billion and each neuron is connected by 7000 synapses, which means that about 0.15 quadrillion synapses are needed

to form the full human neural network [172], so a CMOS-based implementation would be unpractical given that the area occupied by this type of synapse is huge.

In recent times, resistive switching memory elements have been considered for the emulation of synapses due to their structural simplicity and excellent scalability. These two terminal devices can be designed and manufactured into crosspoint arrays for synapse implementation in ANN. An architecture design of RRAM-synapse based ANN is illustrated in Fig. IV.1.4 in which two RRAM crosspoint arrays are inserted into three neuron layers. In such way, the input current of one neuron is the sum-up current from all its connected RRAM devices. The synapse weight is represented by RRAM resistance.

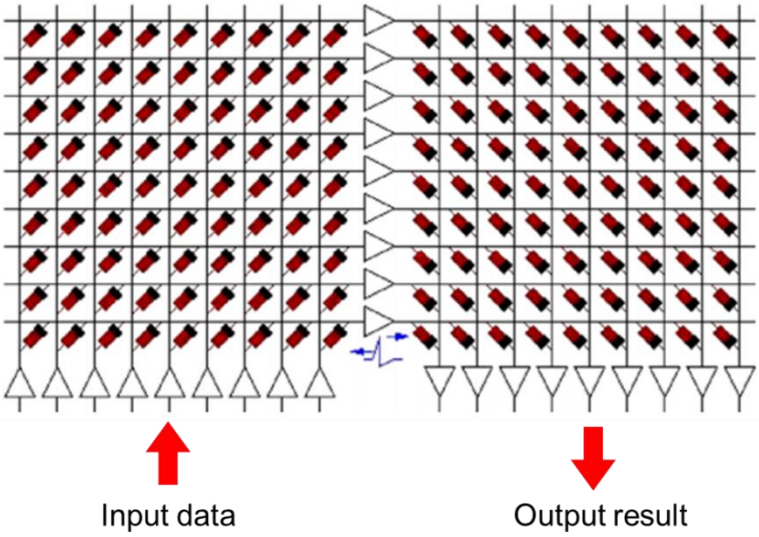


Fig. IV.1.4. An architecture design of RRAM-synapse based ANN [173]. © IOP Publishing. Reproduced with permission. All rights reserved.

A variety of resistive switching devices have been shown to be capable of changing resistance incrementally, thereby displaying the potential for synaptic applications. For example, fundamental learning mechanisms, such as spike timing dependent plasticity

[174], has been observed in Ag/a-Si crossbar arrays [175] and in Ag-$Ge_{30}Se_{70}$ PMC/silicon neuron integration [176] as well as $Ge_2Sb_2Te_5$ chalcogenide memristors [177]. However, the use of CMOS incompatible materials greatly hinders their further development or volume production in standard semiconductor foundries. The use of CMOS-compatible materials will greatly influence the success of neuromorphic computation products. Many efforts have been made to solve this problem by introducing novel materials and processes. Synaptic devices composed of highly reduced binary oxides have been reported to show excellent resistance plasticity [178-180]. Even though the compatibility with back-end-of-line processes has been greatly improved, most of these devices require multiple thin film deposition steps which increases the fabrication cost and complexity. Recently, an electronic synapse that consists only one oxide layer has also been demonstrated. However, single direction resistance adjustability in the HfO_2 synapse limits its application to offline training only [181], and the high programming voltage required in the silica synapse complicates peripheral circuit design [182].

In this chapter, I'd like to present a novel synaptic device based on Cu/silica/W PMC. By a simple thermal annealing process, the device can be adjusted to show perfect analog behavior which exhibits great potential for the elimination all above mentioned problems. In particular, the device is fabricated with the most CMOS compatible approach compared to any other resistive memory based synaptic technology which makes it a realistic candidate for production in standard foundries.

IV.2. Fabrication of Cu-Silica Electronic Synapse

The Cu-silica synapse is fabricated in crosspoint array, the mask layout is illustrated in Fig. IV.2.1. It consists three masks, Mask-1 for W bottom metal line patterning, Mask-2 for Cu top metal line patterning and Mask-3 for contact pads patterning. The device size is around 30 x 30 μm^2 which is defined by the overlap of top metal lines and bottom metal lines. The detailed array fabrication flow is illustrated below in both cross-section view and top view.

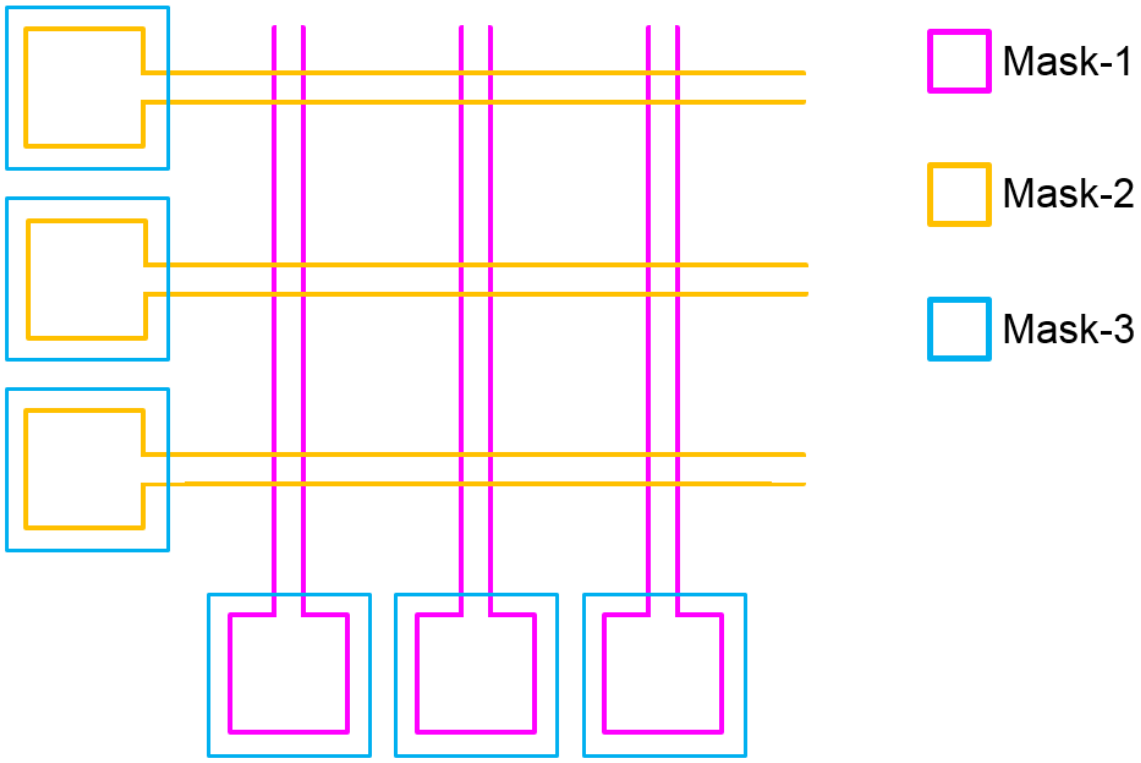


Fig. IV.2.1. Layout of crosspoint PMC design (overlap of three photo-masks).

Step 1: A 60 nm thick tungsten film was DC sputtered on the Si_3N_4 coated wafer by a Lesker PVD75 system. The sputtering rate is around 1Å/s with 4 mT chamber pressure (Ar gas) at a power of 90 W. The upper image in Fig. IV.2.2a shows the top view and the

lower image illustrates the cross section view of film stacks along the dotted line in upper image. The rest of process flow is illustrated in the same way.

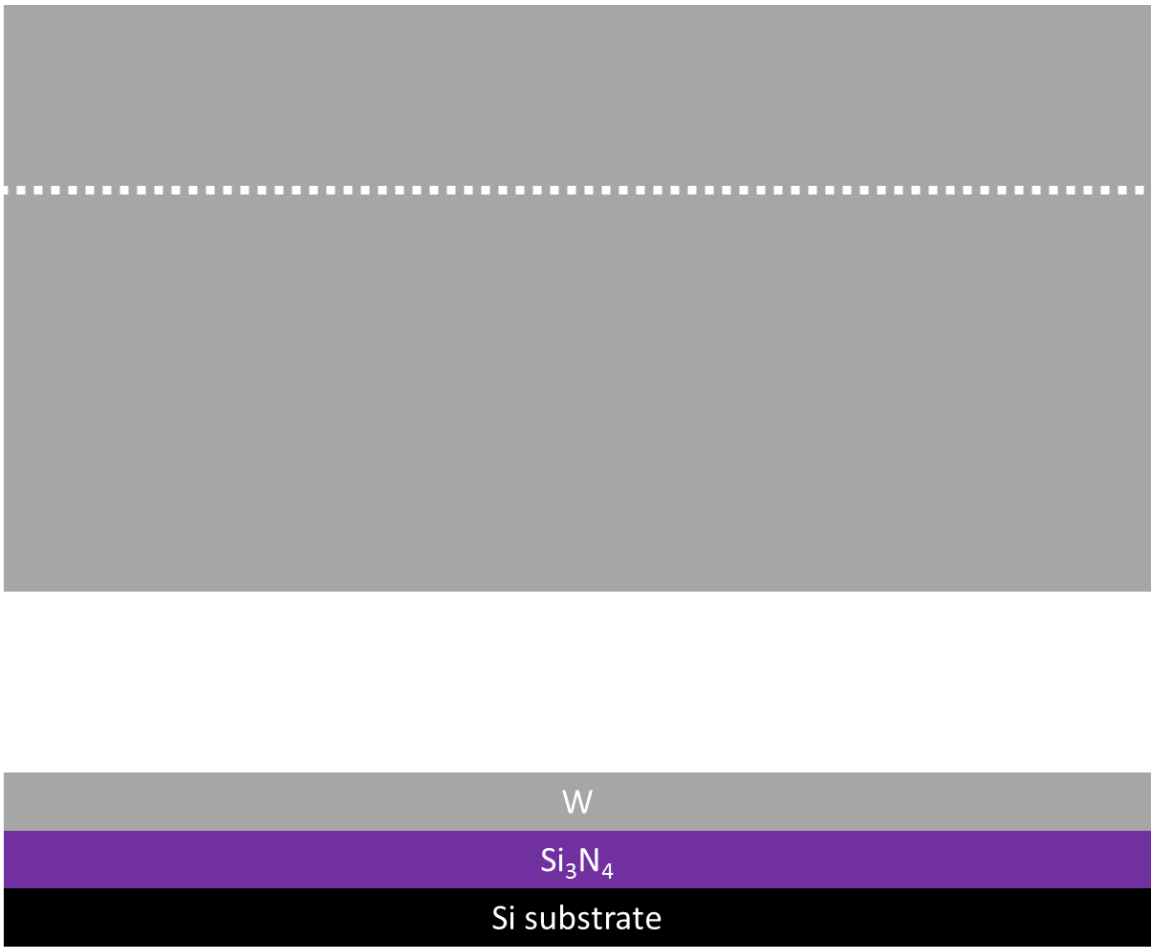


Fig. IV.2.2a. W film (inert electrode) deposition.

Step 2: This W film was then patterned by photo-lithography to create bottom metal lines. Firstly, HMDS and AZ4330 positive photoresist was sequentially spin coated on the wafer at 2000 rpm for 30s followed by soft baking at 100°C for 140s resulting in a total photoresist thickness of 4um. AZ4330 was used for this step because of its large thickness which provides better physical stability for the following wet etch process. The wafer was then aligned with Photomask-1 by OAI 808 aligner and exposed under UV light for a total

dose of 350 mJ/cm^2. This step is illustrated in Fig. IV.2.2b. The shadow region in photoresist layer was removed by MIF 300 developer during the development process.

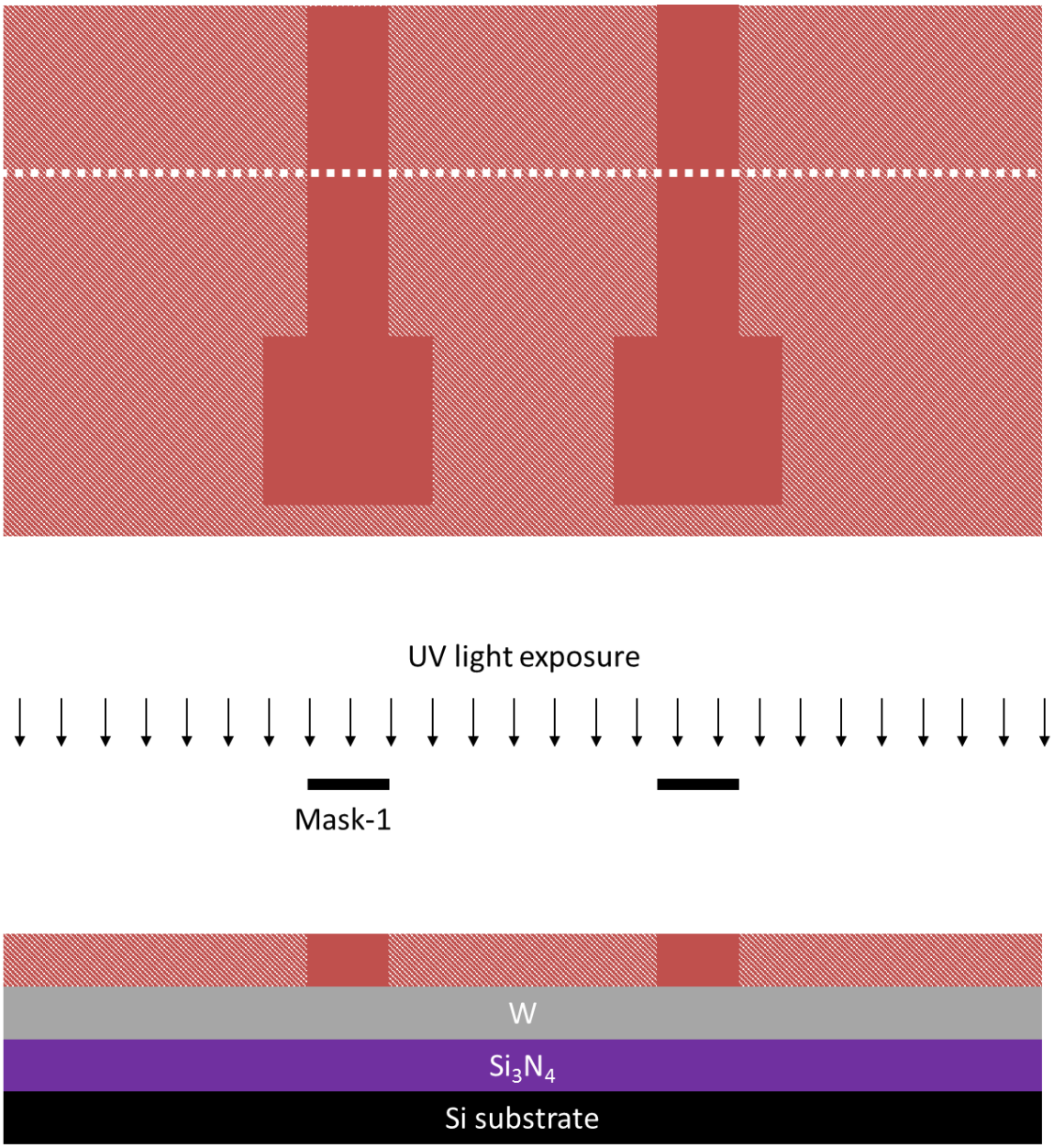


Fig. IV.2.2b. Photolithography patterning of bottom metal lines.

Step 3: The uncovered W film were then etched off by 5% H_2O_2 solution to create bottom metal lines. The wet etch rate at room temperature is about 4Å/s. The reason for

choosing wet etch over dry etch is because of its better selectivity and uniformity. The resulting structure after wet etch is shown in Fig. IV.2.2c.

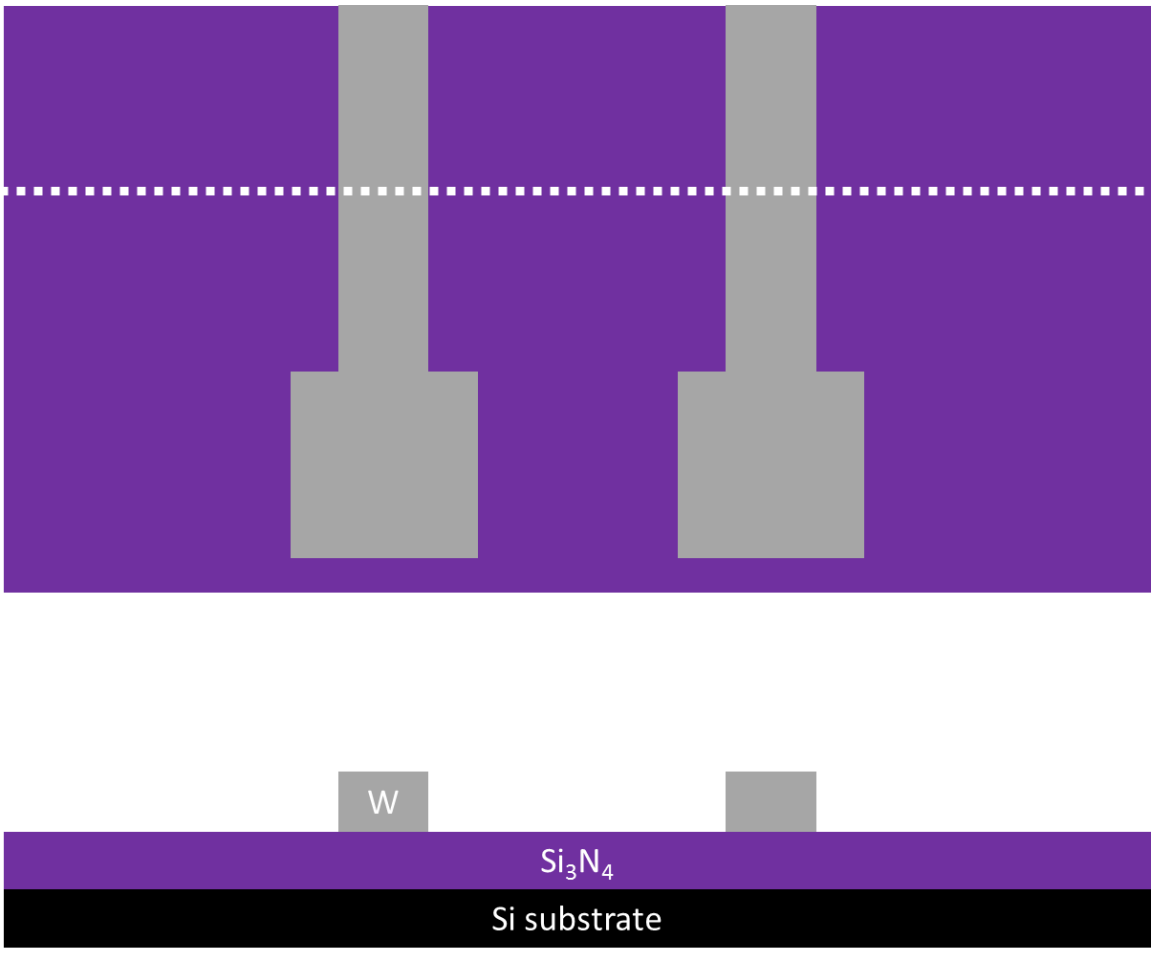


Fig. IV.2.2c. Finished bottom metal lines after wet etch process.

Step 4: In this step, a blanket layer of silica was deposited on top of bottom metal lines. This silica film is the most critical layer for resistive switching because it is the medium for ion transport and filament formation. The film property directly affects the resistive switching characteristics of PMC device. Electron-beam evaporated silica is the simplest way for switching layer deposition. The sample was transferred into Lesker PVD75 electron beam evaporator with wafer at chamber top and silica source at chamber

bottom, a layer of 100 nm porous silica is evaporated at room temperature with a rate of 1Å/s. The porous structure facilitates the Cu diffusion in later thermal annealing step. Then, a layer of 100 nm Cu was e-beam evaporated on top of porous silica without breaking the vacuum, the deposition rate is maintained at 1Å/s.

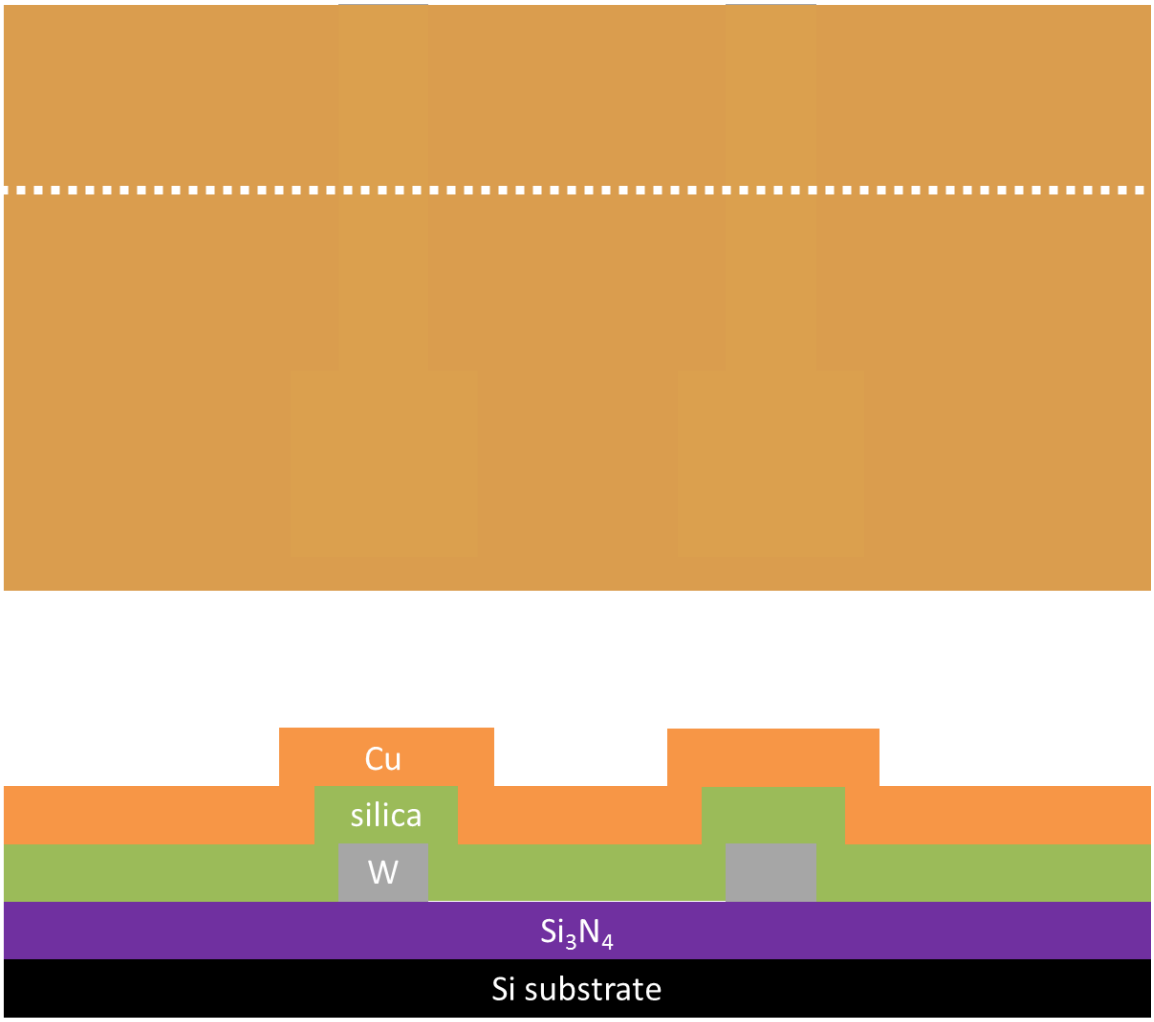


Fig. IV.2.2d. Blanket silica film and Cu film evaporation for resistive switching layer and active electrode, respectively.

Step 5: In this step, the top metal line was patterned by photolithography. To create sharp and clean metal line edges, etching is selected over lift-off. In order to form bright-

field pattern with dark-field mask, negative photoresist (AZ5214) is used. For negative photoresist, the exposed region remains while the covered region will be removed by MIF 300 developer. HMDS and AZ5214 negative photoresist was sequentially spin coated on the wafer at 4000 rpm for 30s followed by soft baking at 100°C for 90s. The coated wafer was then aligned with Photomask-2 and exposed under UV light for a total dose of 90 mJ/cm^2. After the first exposure, the wafer was hard baked at 120°C for 150s, during baking, the property of exposed photoresist changed to be hardly developed, the unexposed photoresist remains the same. After baking, the photoresist layer was UV exposed again for $160mJ/cm^2$ without a mask (flood exposure). And the entire wafer was then soak into MIF 300 for developing. The resulting pattern is illustrated in Fig. IV.2.2e.

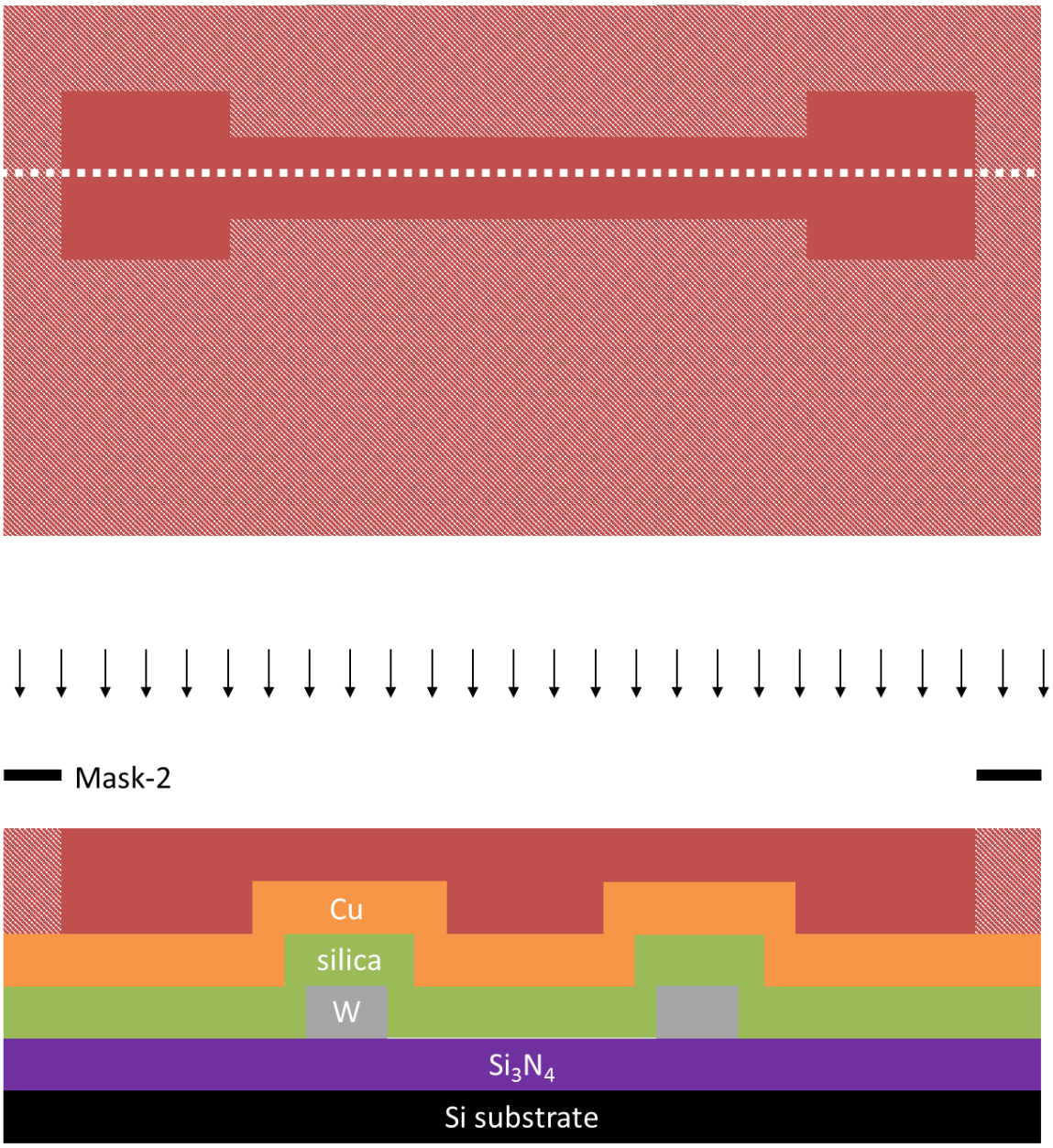


Fig.IV.2.2e. Photolithography patterning top metal lines (Cu) with negative photoresist.

Step 6: The top metal lines were created by wet etching with a mixed solution of NH_4OH (29%), H_2O_2 (30%) and H_2O with a ratio of 1:1:1. The etch rate is about 40nm – 50nm/s at room temperature. Since the etchant reacts with the photoresist as well, after etching, the photoresist has to be removed by 400T solution at 130°C for 15minutes.

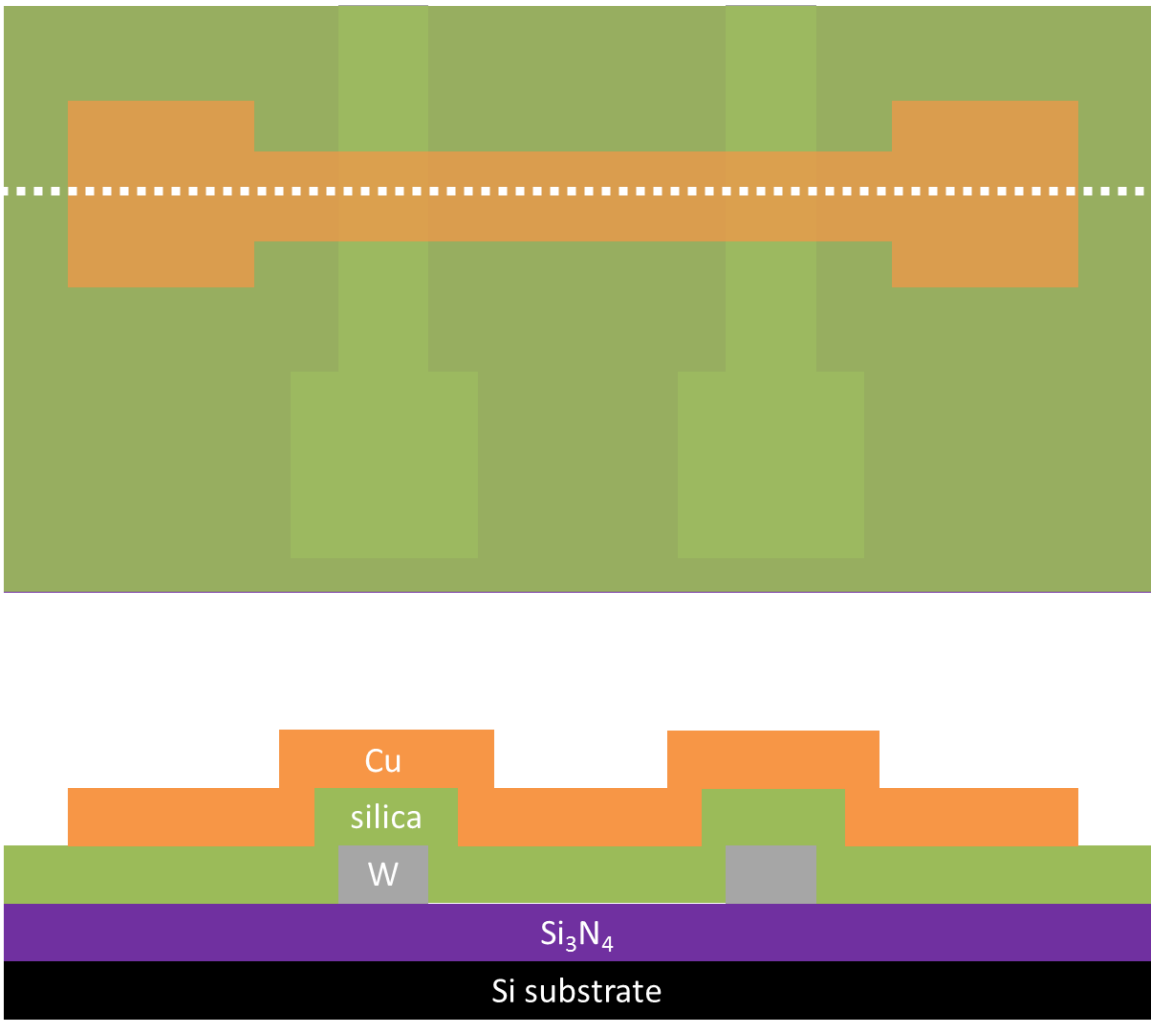


Fig. IV.2.2f. Finished top metal lines (Cu) after wet etch process.

Step 7: The wafer was then put into e-beam evaporator and a blanket film of 400nm silica was evaporated on top of everything. This thick silica layer works as sealing film which prevents the oxidization of Cu electrode during thermal annealing process. Then, the wafer was annealed by Heatpulse RTP system at 500°C for 10 min in a N_2 ambient to thermally diffuse Cu into the 100nm silica switching layer to achieve reliable switching functionality.

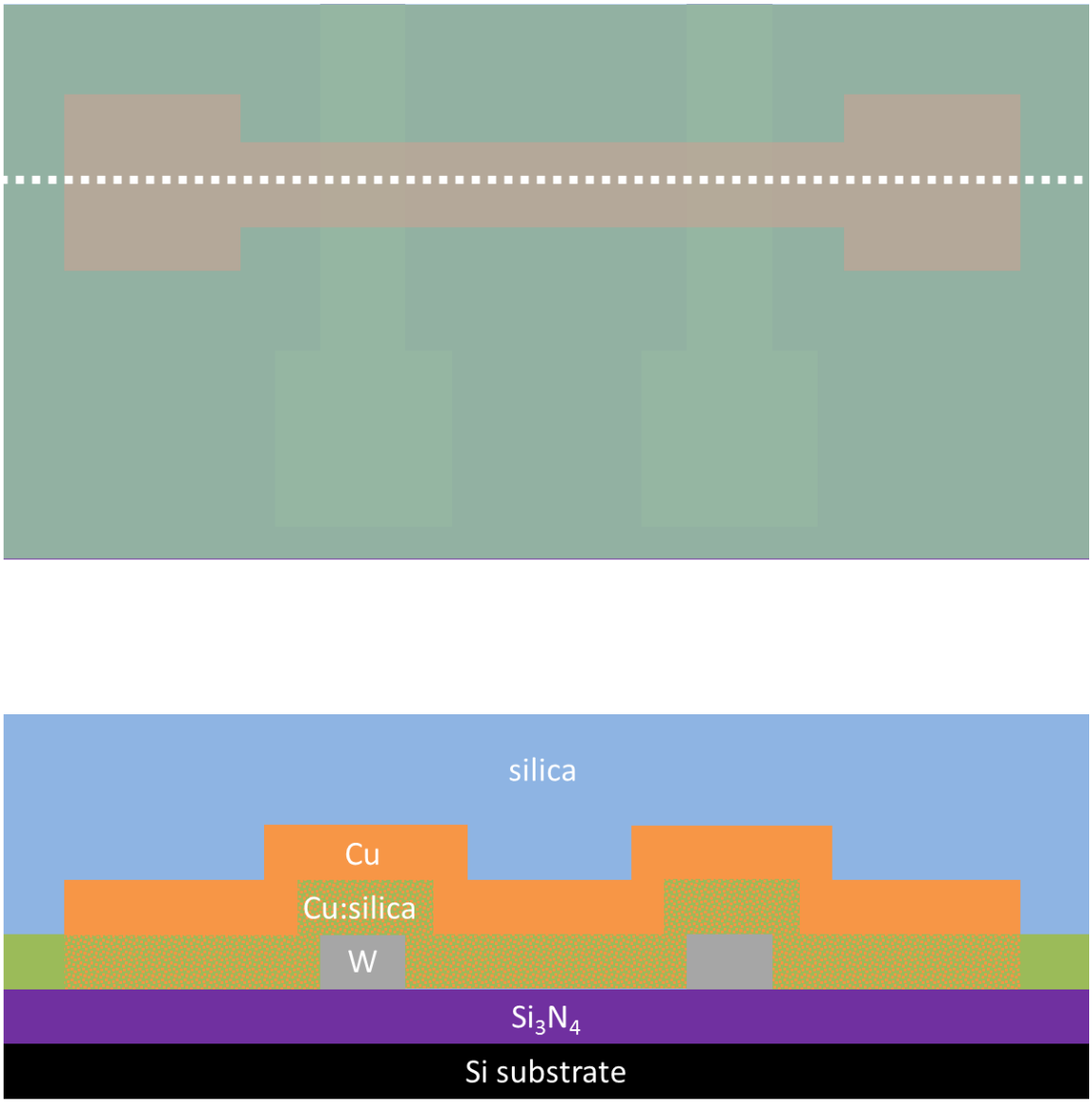


Fig. IV.2.2g. The crossbar device is thermally annealed with a 400nm silica "capping" layer.

Step 8: In order to electrically test the PMC device, contact pads has to be uncovered from the "capping" silica. In this step, the contact pads was pattered with Photomask-3 with the same recipe as Step 2. The silica "capping" layer above contact pads

was then etched off by buffered oxide etch (BOE) 20:1 solution. The finalized sample structure after wet etch is shown in Fig. IV.2.2h.

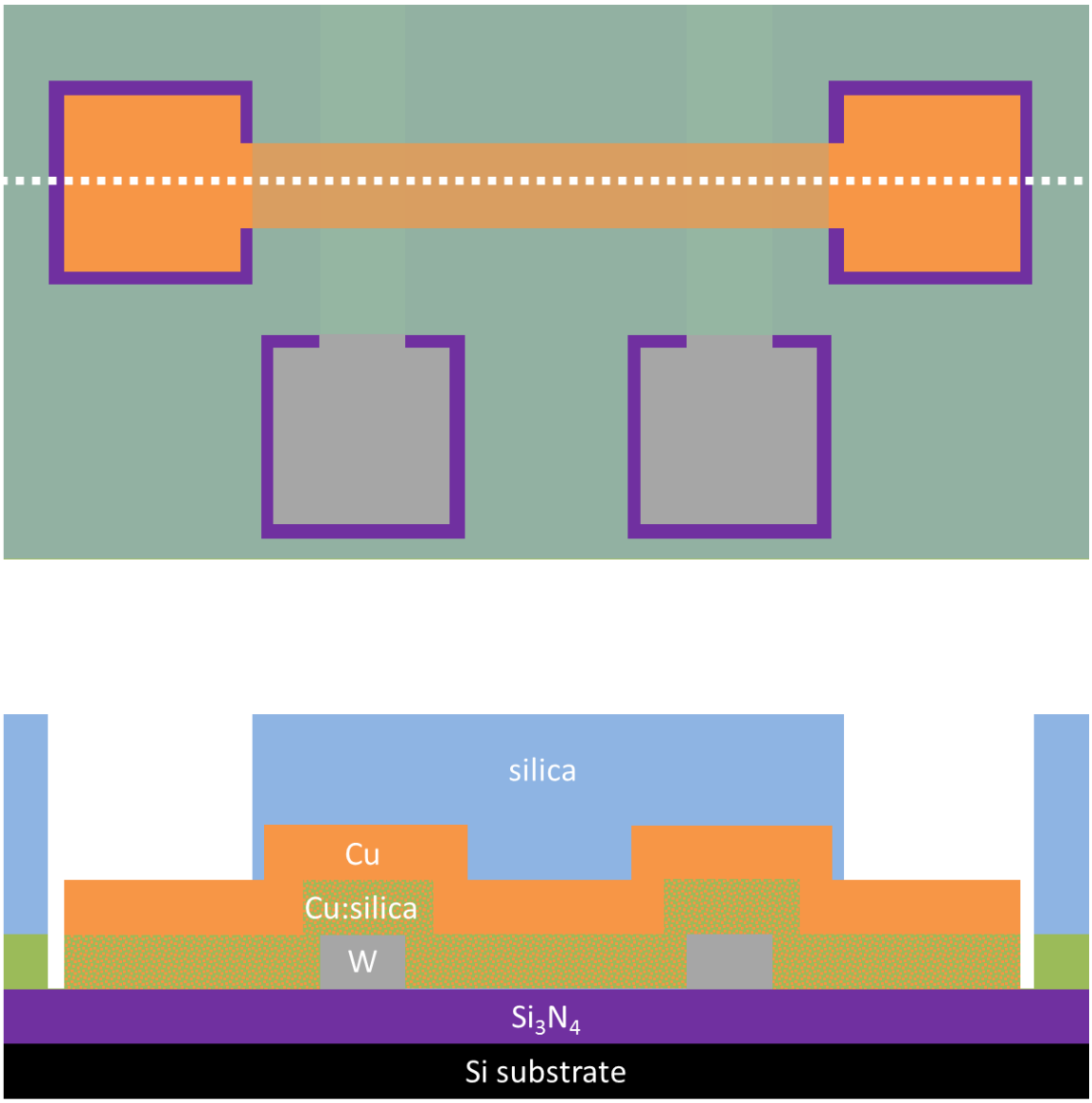


Fig. IV.2.2h. Finished Cu-silica PMC crosspoint array.

The optical image of fabricated wafer, a 12 x 12 crosspoint array and single PMC device is demonstrated in Fig. IV.2.3a, Fig. IV.2.3b and Fig. IV.2.3c, respectively. Note

that this fabrication sequence involves no lift-off steps which significantly enhances device yield and uniformity.

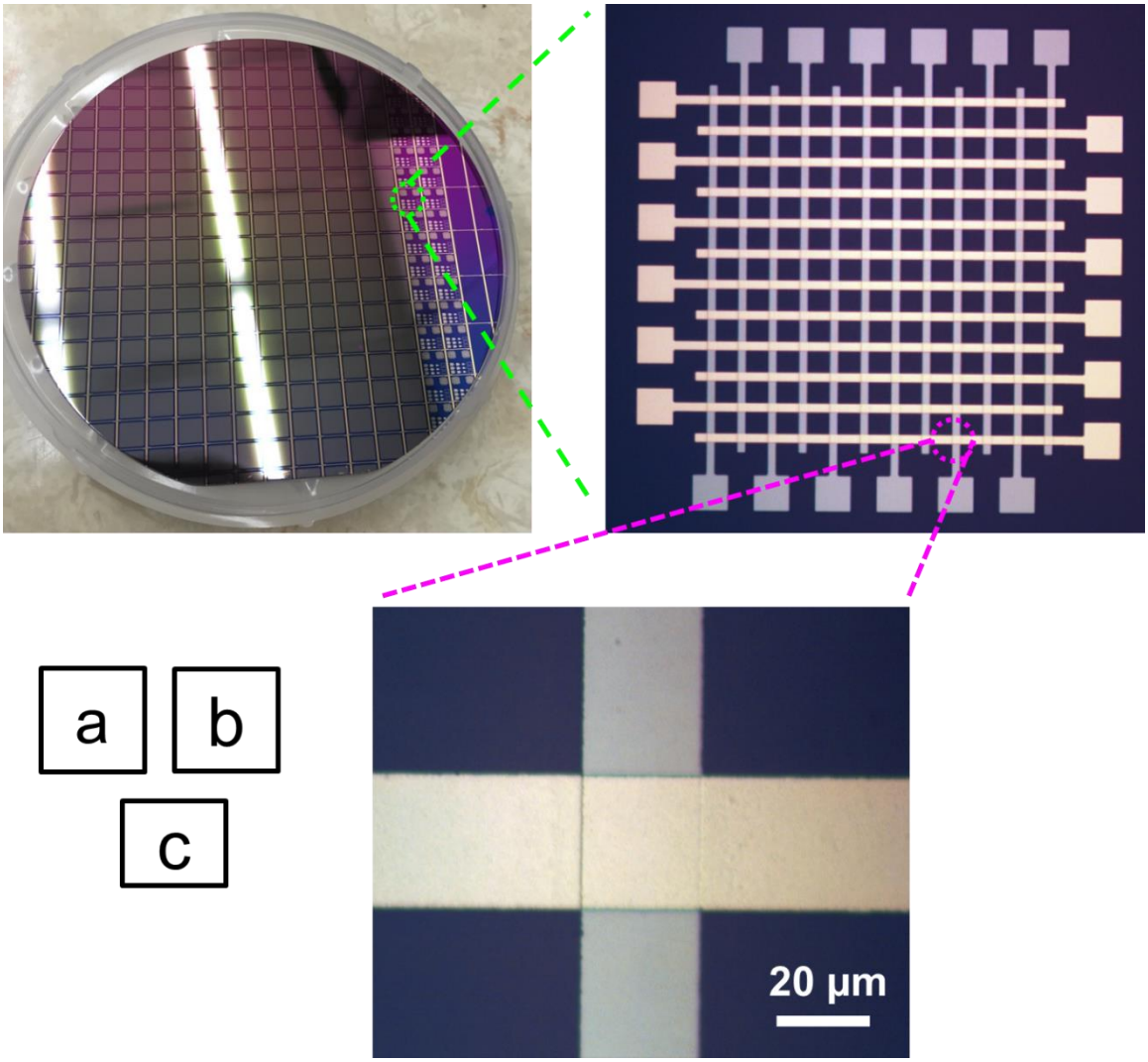


Fig. IV.2.3. Optical image of PMC crosspoint array. (a) Fabricated 4 inch wafer. (b) A 12 × 12 array with Cu/silica/W devices at each crosspoint. (c) Magnified image of a single cell [62].

IV.3. Analog Behavior of Cu-Silica PMC

For electrical characterization, the Cu top metal lines were biased while the W bottom metal lines were fixed at ground potential. Only the memory cells along the diagonal of the array were measured in order to avoid the sneak path problem. The dc characterization was carried out using an Agilent 4156C Semiconductor Parameter Analyzer. In the pulse programming experiment, the voltage pulses were generated using an Agilent 81150A arbitrary waveform generator and the results captured using a 54832D Infiniium digital oscilloscope.

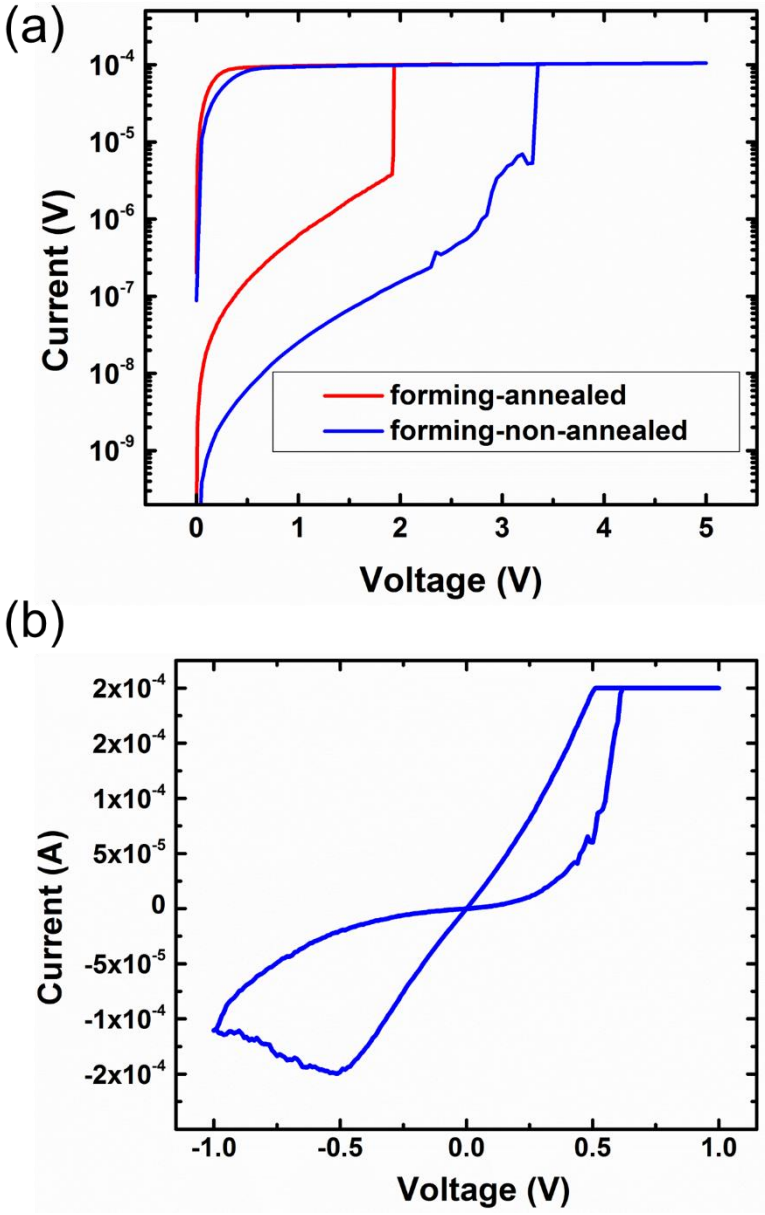


Fig. IV.3.1. DC characteristics of Cu-Cu:silica PMC device. (a) electroforming, (b) switching [62].

The thermal annealing step diffuses Cu into the oxide and the as-fabricated device resistance is significantly reduced, as illustrated in Fig. IV.3.1a, in which the blue curve is the current versus voltage (I–V) plot for the un-annealed device and the red curve is for the

annealed device. The electroforming process is believed to be a soft-breakdown process that makes conductive filaments (or percolation paths) through the relatively porous e-beam silica matrix (with a density of 2.08 g/cm^{-3} compared to α-quartz' 2.65 g/cm^{-3}) and connects the pre-doped Cu regions to form a conductive network [183, 184]. Note that the forming/abrupt switching occurs at 1.9 and 3.3 V for the thermal annealed and non-annealed devices respectively. A higher electroforming voltage is observed for non-annealed devices because more electrically generated Cu ions are required to form an equivalent amount of conductive filaments (or percolation paths) compared to thermally annealed devices since the former have less initial Cu ions in silica.

After electroforming, the devices were switchable between high and low resistance states with a compliance current of 200 μA, typical DC switching curve is shown in Fig. IV.3.1b. The switching voltages were around 1 V for both program and erase which is compatible with the supply voltage of current CMOS, thereby eliminating the need for charge pumps. Just as interesting is the less abrupt switching characteristics of the device which makes it more ideal for a synaptic element. Furthermore, the variability of fabricated devices in terms of electroforming voltage ($V_{forming}$), virgin state resistance (R_{virgin}), LRS resistance (R_{ON}), and HRS resistance (R_{OFF}) is summarized in table IV.3.1. As shown in this table, the as-fabricated device-to-device variation is small ($V_{forming}$ and R_{virgin}) due to improved process control. The variation is more obvious during resistive switching (R_{ON} and R_{OFF}). This may be because the devices are conditioned slightly differently due to a poorly controlled electroforming process [31, 185].

Table IV.3.1. Variability of fabricated device [62].

	$V_{forming}$ (V)	R_{virgin} (Ω)	R_{ON} (Ω)	R_{OFF} (Ω)
Average	1.9	2.6 M	7.3 k	34 k
Standard Deviation (σ)	0.13	40 k	3.6 k	8.1 k

*$V_{forming}$ and R_{virgin} data is collected from eight devices in two different array.
**R_{ON} and R_{OFF} data is collected from the same eight devices with five switching cycles per device.

Rather than just performing binary (LRS/HRS) operations such as those commonly used in digital systems to represent Boolean states, it is critical that the resistance can be gradually tuned in an analog fashion in order to emulate a biological synapse. To demonstrate such characteristics, incremental voltage sweeps were applied to the devices, each sweep starting from 0 V to a successively higher positive (or negative) value. As illustrated in Fig. IV.3.2a, the resistance of the device decreases with an increase in positive bias. In biological terms, this represents the potentiation (P) in the synapse. Conversely, the resistance of a low resistance (programmed) device increases with increasing negative bias magnitude, which corresponds to the depression (D) in a biological synapse (Fig. IV.3.2b). The device resistance measured at 10 mV for each sweep, shown in table IV.3.2. Unlike transition metal-oxide based synaptic devices which sometimes only present either potentiation or depression [186, 187], the simultaneously present potentiation and depression in our device makes it a suitable technology for both online and offline training. Note that all incremental plots are generally contained within the dotted curve obtained from a full range voltage sweep, which indicates that a complete sweep is equivalent to a combination of discrete sweeps. This combinational characteristic is useful for learning speed adjustment and will be discussed later in this paper.

Based on the "bi-layer" model identified in section II.5.4, the continuous change of resistance is explained. Following programming at low voltage bias, a small number of conductive paths exist in layer 1 (heavily doped region) and the thickness of layer 2 (lightly doped) is large. By increasing the positive bias, more conductive paths are formed and layer 2 simultaneously gets compressed because the Cu ions migrate along the electric field. Both effects work together to reduce device resistance.

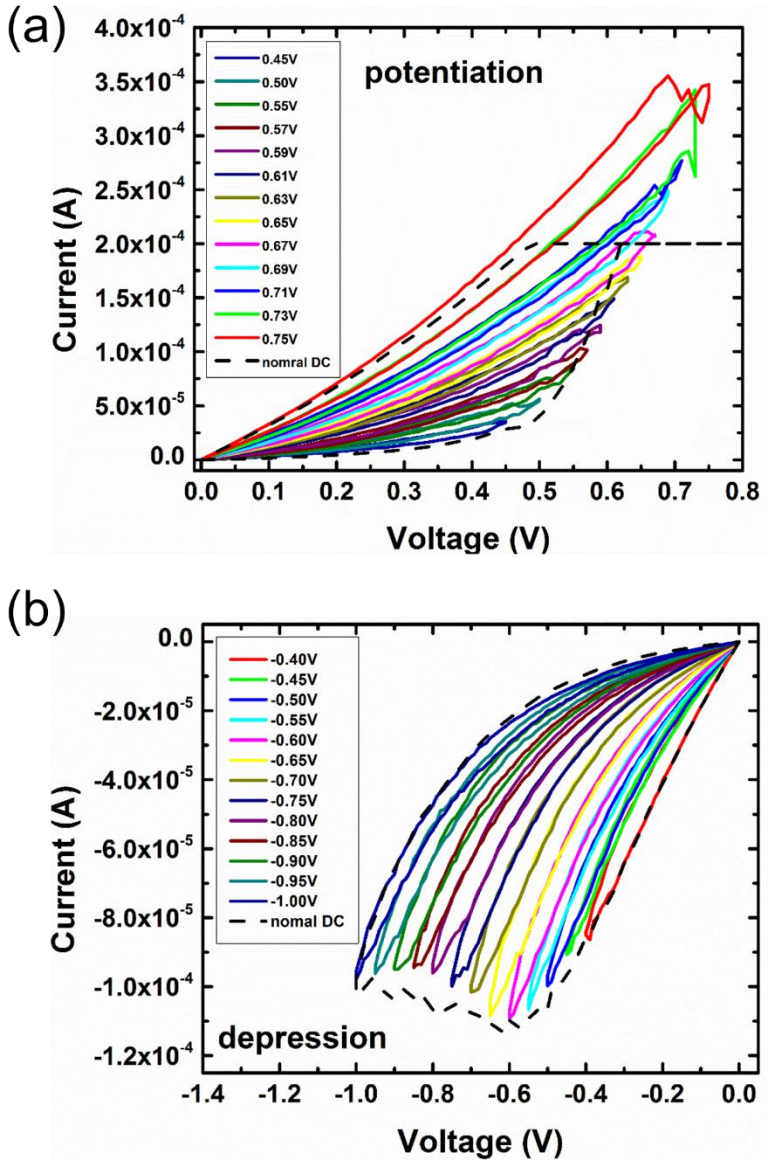


Fig. IV.3.2. DC characteristics of gradual resistance change in Cu-silica PMC. (a) Potentiation, (b) Depression [62].

Table IV.3.2. Resistance value for voltage sweeps with different stop voltage (V_{stop}) [62].

P	V_{stop} (V)	0.45	0.5	0.55	0.57	0.59	0.61	0.63
	R_{stop} (Ω)	37.7k	29.1k	24.2k	19.5k	14.6k	10.4k	9.26k
	V_{stop} (V)	0.65	0.67	0.69	0.71	0.73	0.75	
	R_{stop} (Ω)	8.20k	7.53k	6.39k	5.26k	4.82k	3.97k	
D	V_{stop} (V)	-0.4	-0.45	-0.5	-0.55	-0.6	-0.65	-0.7
	R_{stop} (Ω)	5.62k	7.47k	8.29k	9.38k	11.2k	13.8k	17.6k
	V_{stop} (V)	-0.75	-0.8	-0.85	-0.9	-0.95	-1.0	
	R_{stop} (Ω)	21.9k	26.1k	31.1k	36.9k	42.2k	46.1k	

To evaluate the plasticity performance of our electronic synapse device in a more realistic programming environment, electric pulses were applied to tune the resistance state. Fig. IV.3.3 schematically illustrates the pulsing scenario, with groups of potentiating pulses (red) and depressing pulses (blue) applied with a voltage increment (for potentiating) or decrement (for depressing) of ΔV between two consecutive groups. Each group is composed of a pulse train consisting of ten sub-pulses that have a same amplitude and pulse width (t_{ON}). Through this scenario, the effect of pulse amplitude and pulse counts on the resistance change can be investigated.

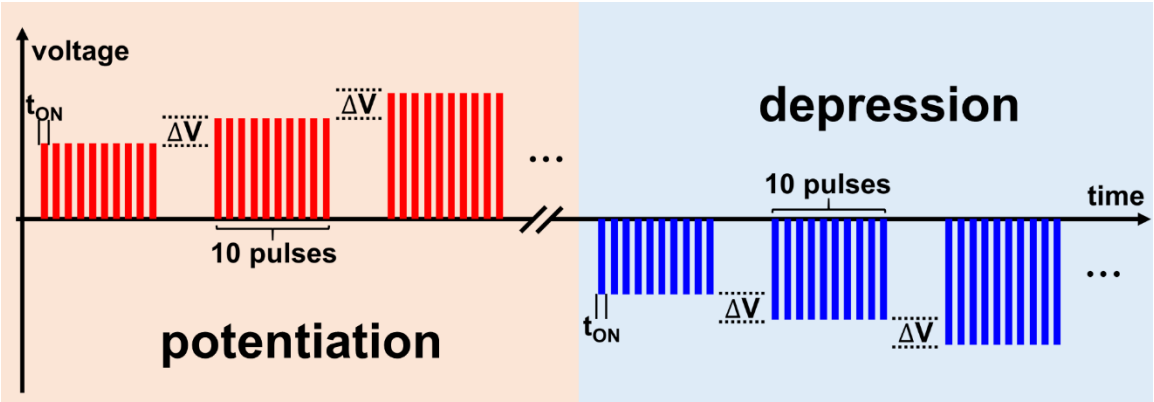


Fig. IV.3.3. Pulsing scenario for gradual resistance change in Cu-silica PMC [62]. © IOP Publishing. Reproduced with permission. All rights reserved.

The pulse experiment setup is shown in Fig. IV.3.4. The generated square pulses were applied on the load circuit consisting of a device and a 6.8 kΩ series resistor, and the waveforms were captured by one oscilloscope channel marked as V1. An additional oscilloscope channel, V2, was used to capture the waveforms across the series resistor. Thus, the resistance change of PMC device can be calculated based on the equation

$$R_{PMC} = R_s * (V_1 - V_2)/V_2$$

where Rs is the resistance of the series resistor.

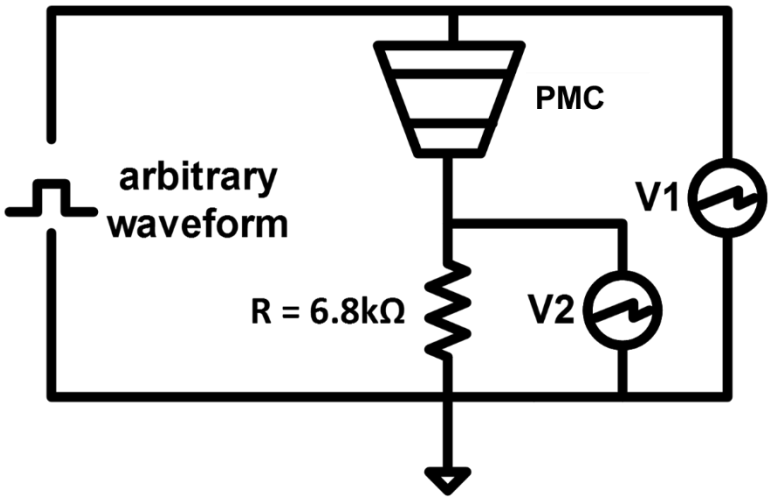


Fig. IV.3.4. Test setup for electric pulse experiment [62]. © IOP Publishing. Reproduced with permission. All rights reserved.

Fig. IV.3.5a and b show the experimental waveforms for a sequence of potentiation and depression pulses, respectively. The colored curves are V1 and the black curves are V2. For potentiation, the pulse train starts from 0.79 V and ends at 1.15 V with a ΔV of 20 mV. For depression, the pulse train starts from -0.75 V and ends at -1.01 V with a same ΔV. The width of the sub-pulse (t_{ON}) is 10 μs for both cases. It is also observable that the magnitude of readout pulses (black curve, V2) is gradually increased (decreased) with the increase of the magnitude and number of applied pulses (V1), which implies a gradually tuned resistance.

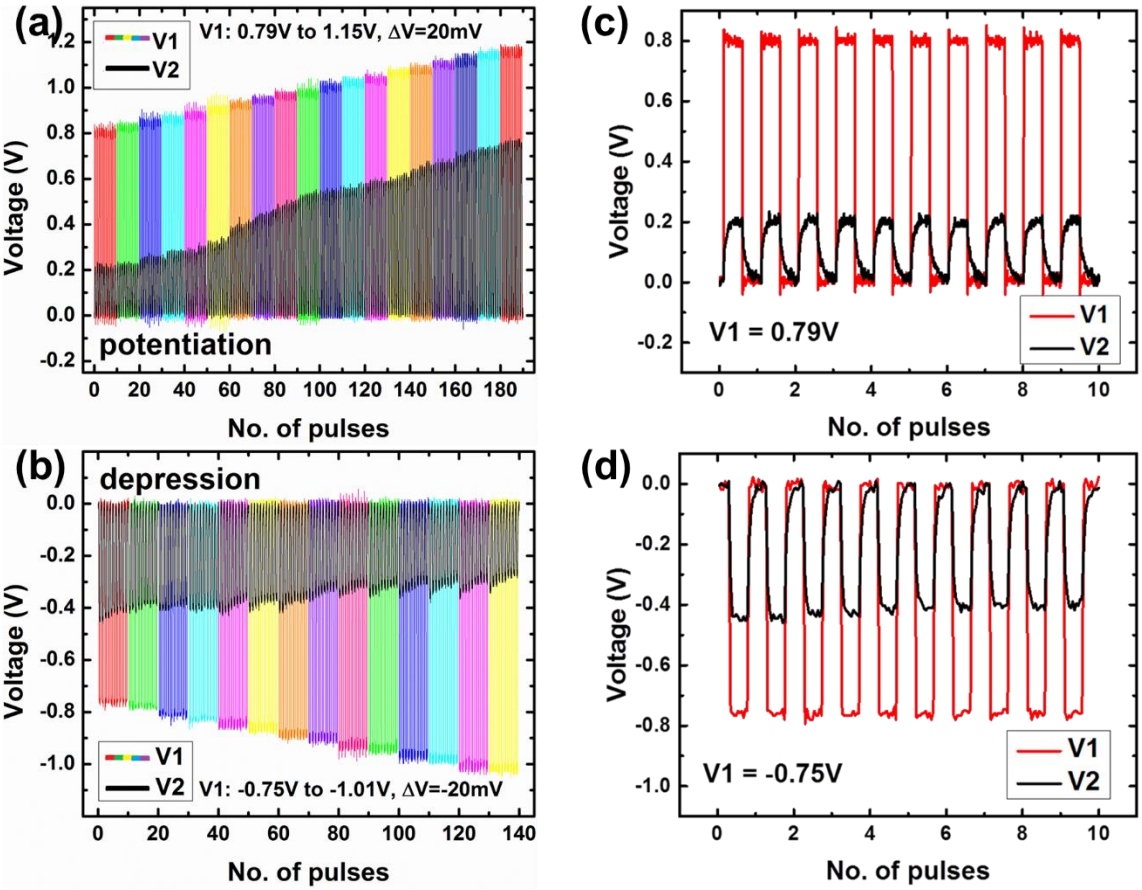


Fig. IV.3.5. (a) Pulse potentiation experimental waveforms. (b) Pulse depression experimental waveforms. (c) zoom-in waveform which shows the 10 sub-pulses of the first potentiation pulse group in (a) (0.79V). (d) zoom-in waveform which shows the 10 sub-pulses of the first depression pulse group in (b) (-0.75V) [62].

The calculated resistance of 3 continuous pulse tuning cycles is shown in Fig. IV.3.6. As expected from the described waveforms, the device resistance is incrementally reduced from 20 kΩ to 3 kΩ by applying potentiating pulses, and it is incrementally increased by applying depressing pulses. This incremental resistance change is distinct from the abrupt resistance change which has been widely observed in resistive switching

devices [7]. Moreover, as shown in Fig. IV.3.6, a significant number of resistance states are achieved due to the pulsing scenario, and this densely distributed resistance enriches the learning capability. It should be noted that there is a small kink in potentiating and depressing cycles when the resistance is small. This kink marks the speed change of resistance tuning as discussed below.

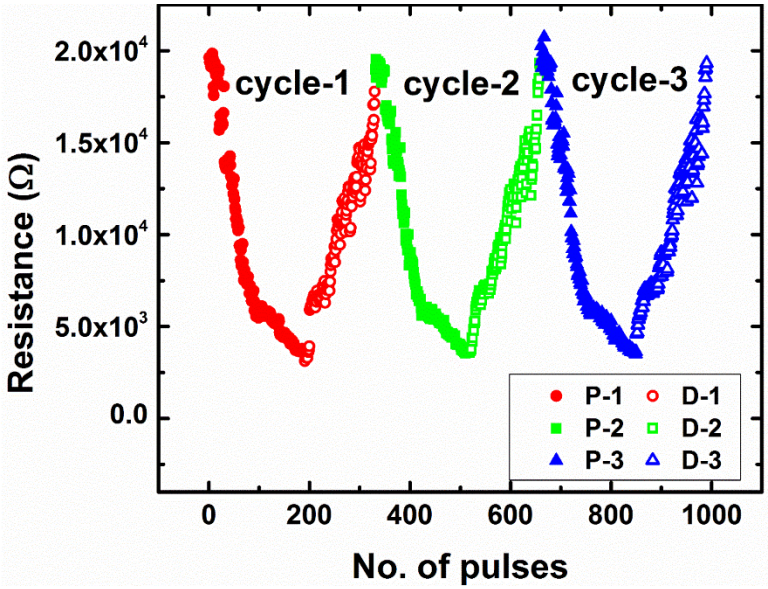


Fig. IV.3.6. Resistance response to electric pulses. The resistance of the Cu/silica/W electronic synapse can be incrementally increased or decreased by potentiating and depressing pulses [62].

The effect of varying pulse width (t_{ON}) and voltage increment (ΔV) on the change in device resistance was investigated and the results summarized in Fig. IV.3.7. The device was tested with the pulsing scenario described earlier but using 4 different pulse widths of 10 µs, 20 µs, 50 µs and 1 ms. For potentiation, the applied pulse is from 0.81 V to 1.05 V with a 20 mV ΔV for all 4 t_{ON} cases; the depression is same as its potentiating counterpart except it starts from -0.75 V to -1.01 V. A similar starting resistance was assured before

applying pulses. It should be mentioned that for the black curve (1 ms pulses) shown in Fig. IV.3.7a, the resistance has already been lowered by tens of kilo-ohms by just one 0.81V pulse. This suggests that we may lose fine control over resistance states if the applied pulse is too long. Nevertheless, both potentiation and depression cases show the same trend, that is, the resistance changes faster with longer pulses in the low voltage region. In the higher voltage region, the resistance tuning speed slows down and the final resistance is approximately the same regardless of the pulse width. This behavior is expected, considering the bi-layer model built-up in impedance spectroscopy experiment, as longer positive pulses should allow more vertical movement of the front of Cu rich layer towards the cathode but once the front reaches the cathode, the excessive Cu ions pile up at the interface and the increased chemical gradient of Cu ions balances the Cu migration so the pulse width no longer contributes to resistance change. In addition, the magnitude of voltage across the device is greatly reduced when the device resistance is in the same range as that of the series resistor. Thus, further resistance decrease can be realized only through pulse magnitude increase and this also explains the similar final resistances. The same explanation applies for depression except in this case the Cu ions are accumulated in the Cu rich region.

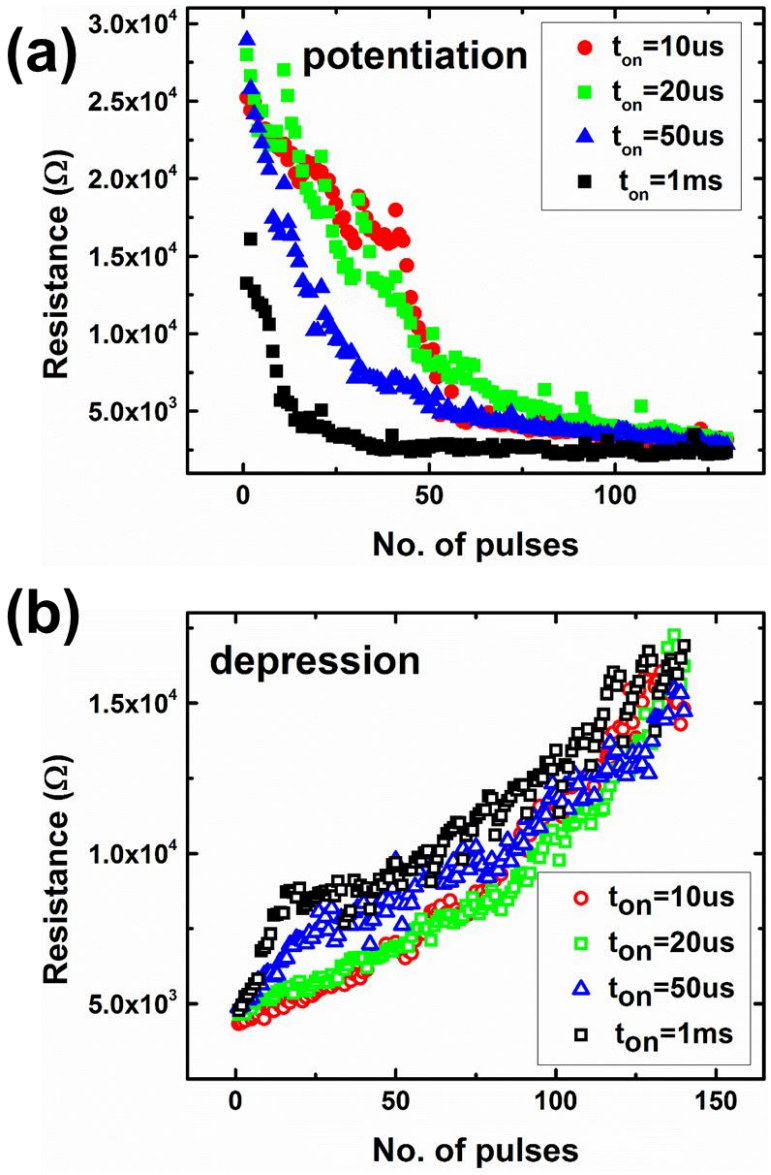


Fig. IV.3.7. Impact of pulse width (t_{ON}) on resistance tuning. (a) Pulse width effects on potentiation. (b) Pulse width effects on depression [62].

This voltage-determined resistance change behavior was further investigated by varying the voltage increment (ΔV). In this experiment, t_{ON} is fixed at 10 μs and ΔV increases from 20 mV to 60 mV. The start and stop voltage is same for potentiation (0.79

V – 1.15 V) and depression (- 0.75V – - 0.99V). The results of this experiment are shown in Fig. IV.3.8a and b. It can be seen that the device resistance changes faster (with fewer pulses) for larger ΔV, with the fastest change occurring for 60 mV and the slowest for 20 mV. Moreover, the final resistance is more or less the same regardless of the total number of pulses applied. These results demonstrate that voltage is a more important factor than pulse width in the determination of resistance state for our synapse device.

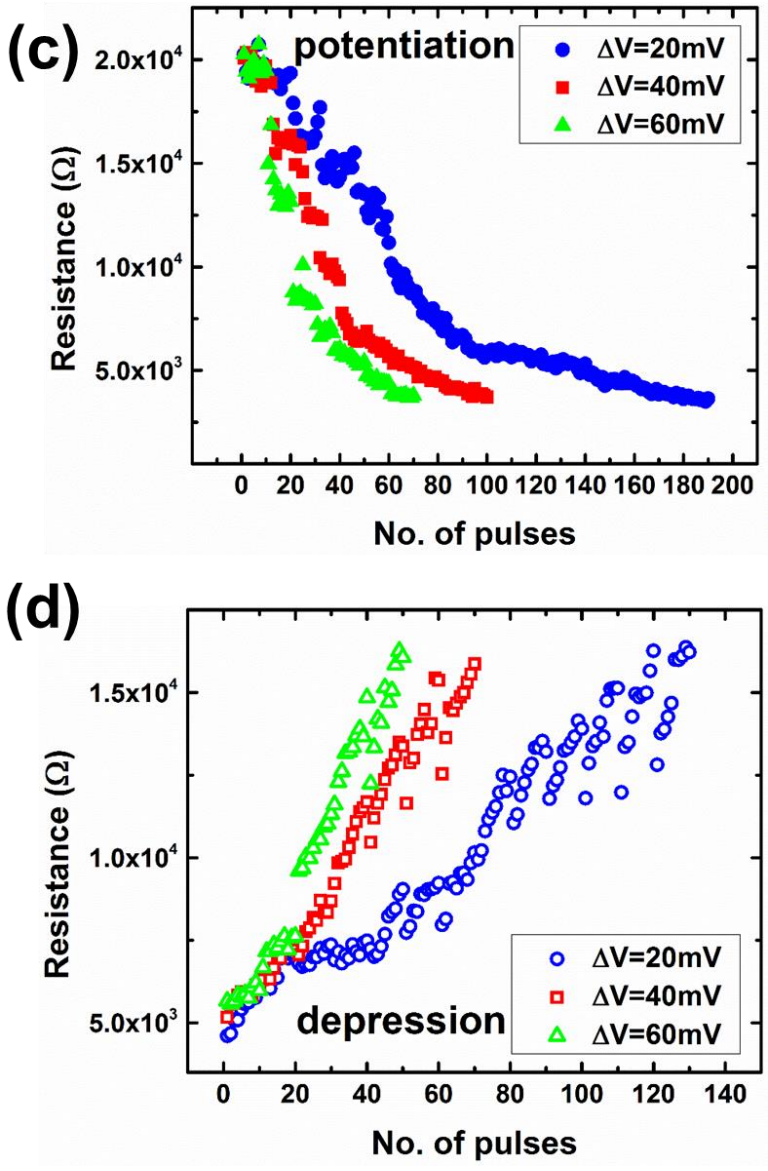


Fig. IV.3.8. Impact of magnitude increment (ΔV) on resistance tuning. (a) Pulse magnitude increment effects on potentiation. (b) Pulse magnitude increment effects on depression [62].

Besides it is tested by pulses with incremental magnitude, the Cu/silica/W PMC device can be also tuned by constant pulses. The result is shown in Fig. IV.3.9. The device can be potentiated or depressed by 1μs pulses at 0.7V or - 0.8V, respectively. For each turning cycle 20 potentiation pluses were applied to the device which is followed by 20 depression pulses. And this operation is repeated for 10 times. The resistance is read by small DC voltage right after every pulse. As shown in Fig.IV.3.9, the device conductance (resistance) can be fine turned after the first pulse of every turning cycle.

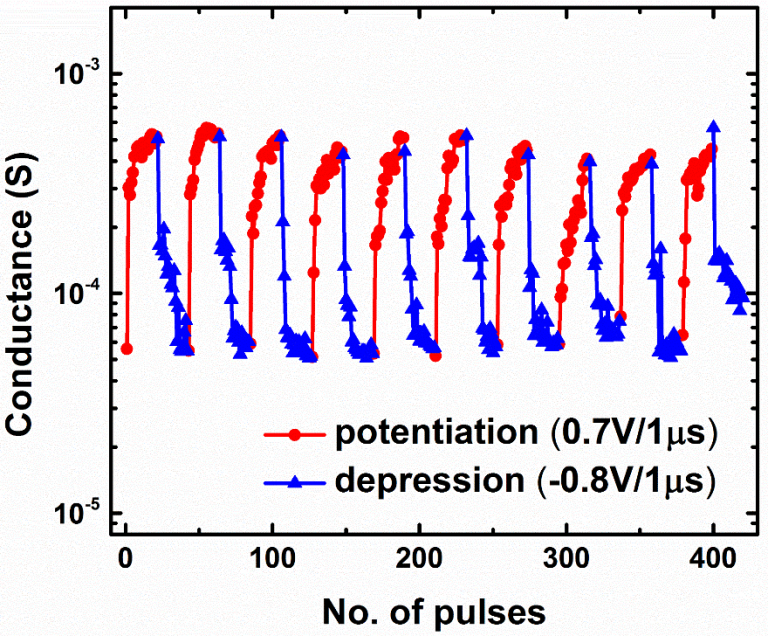


Fig. IV.3.9. Gradual resistance change by constant electrical pulses.

Finally, it should be noted that the device characterized in this paper is too large to be integrated into silicon integrated circuits for realistic neuronal network emulation. However, given the fact that there is not much difference between the fabrication of such devices and the standardized CMOS fabrication in current foundries, there should be no limitation on the scaling of our synaptic device although a re-optimization of device aspect ratio (thickness vs. size) and annealing condition would likely be required. It is also possible to achieve ultralow current operation as off-state current scales with device size, which will significantly reduce the power consumption of a single synaptic device at the nanometer scale. Our synapse device is characterized with a minimum pulse length of 1 μs owing to the limitations of our test setup. Such a slow operational speed would definitely be problematic in a sequential processing scheme but is less of an issue in highly parallelized processing as employed by neuronal networks. Successful parallel write/read operations in crosspoint arrays has recently been demonstrated [180].

A Cu/silica/W PMC electronic synapse which has excellent CMOS-compatibility in terms of materials composition, back end of line processing, and operating voltage, has been developed. The synapse device exhibits promising plasticity in resistance change and, importantly, its resistance can be bipolarly tuned by voltage DC sweeps or pulses. The resistance change is attribute to thickness modulation of a ‘dual-layer’ material system created during processing with different Cu concentration in each layer which is supported by impedance spectroscopy. By varying the pulse parameters, it is seen that the magnitude of pulses contributes more to resistance change than pulse width, especially in the high voltage regime, which provides important guidance for circuit design and algorithm

development. Overall, the results shown here indicate potential applications for these devices as electronic synapse in neuromorphic computing.

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