# High-Speed Low-Power Analog to Digital Converter for Digital Beam Forming Systems

by

Ali Nazari

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved April 2017 by the
Graduate Supervisory Committee:

Hugh Barnaby, Chair
Bahar Jalali-Farahani
Bertan Bakkaloglu
Jennifer Kitchen

ARIZONA STATE UNIVERSITY

May 2017

ABSTRACT

Time-interleaved analog to digital converters (ADCs) have become critical components in high-speed communication systems. Consumers demands for smaller size, more bandwidth and more features from their communication systems have driven the market to use modern complementary metal-oxide-semiconductor (CMOS) technologies with shorter channel-length transistors and hence a more compact design. Downscaling the supply voltage which is required in submicron technologies benefits digital circuits in terms of power and area. Designing accurate analog circuits, however becomes more challenging due to the less headroom. One way to overcome this problem is to use calibration to compensate for the loss of accuracy in analog circuits.

Time-interleaving increases the effective data conversion rate in ADCs while keeping the circuit requirements the same. However, this technique needs special considerations as other design issues associated with using parallel identical channels emerge. The first and the most important is the practical issue of timing mismatch between channels, also called sample-time error, which can directly affect the performance of the ADC. Many techniques have been developed to tackle this issue both in analog and digital domains. Most of these techniques have high complexities especially when the number of channels exceeds 2 and some of them are only valid when input signal is a single tone sinusoidal which limits the application.

This dissertation proposes a sample-time error calibration technique which bests the previous techniques in terms of simplicity, and also could be used with arbitrary input

signals. A 12-bit 650 MSPS pipeline ADC with 1.5 GHz analog bandwidth for digital beam forming systems is designed in IBM 8HP BiCMOS 130 nm technology. A front-end sample-and-hold amplifier (SHA) was also designed to compare with an SHA-less design in terms of performance, power and area. Simulation results show that the proposed technique is able to improve the SNDR by 20 dB for a mismatch of 50% of the sampling period and up to 29 dB at 37% of the Nyquist frequency. The designed ADC consumes 122 mW in each channel and the clock generation circuit consumes 142 mW. The ADC achieves 68.4 dB SNDR for an input of 61 MHz.

DEDICATION

*In the Name of **Allah,** the Compassionate the Merciful*

*To the Greatest,*

*The Remainder of Allah,*

*The Imam of the Time*

*And*

*To the Unexcelled Character of All Time,*

*The Noble Lady,*

*Hazrat Zainab*

*Peace Be Upon Them*

# ACKNOWLEDGMENTS

The ultimate gratitude belongs to Allah, the God of the worlds for our creation at the first place and his guidance afterwards, and peace be upon all his prophets especially the last and the greatest, Prophet Muhammad and his household, the Ahl al-Bait. I also thank Allah for granting me the great benefits of my life, my mother and my father, who lived their life for our sake and never stopped to dedicate for us. I also thank my dears, my sister and my brother for all their devotions to me.

I would like to thank my sweet love, Fatemeh, for all she did to support me to complete this dissertation with all the difficulties she encountered. I would also like to thank her parents and family for their extensive help and support.

I would like to thank Dr. Bahar Jalali-Farahani who helped me in my PhD from the beginning and never stopped her provision even after she left ASU. I would also like to thank Dr. Hugh Barnaby for his great and extensive support during the course of this dissertation. I would like to thank Dr. Bertan Bakkaloglu and Dr. Jennifer Kitchen for their interest and helpful suggestions on my dissertation.

I would also like to thank all my friends who supported me during my graduate life in the US.

I would never be able to do this dissertation if I didn't have any of all these helps and supports. Thank you.

TABLE OF CONTENTS

Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

# 1 INTRODUCTION

## 1.1 Motivation and Design Goal

The objective of this research is to design a high speed and high resolution Pipeline ADC for digital beam forming applications. The targeted specifications are 12 bits of resolution with effective number of bits (ENOB) of 11 bits and 650 MSps. Pipeline ADCs with high sampling rates and medium to high resolution, have been reported recently (1), (2), (3), (4), (5), (6), (7), (8), (9), (10), (11), (12), (13), (14), (15), (16), and (17). Table 1 compares the specifications of recent designs of pipeline ADCs in this range of speed and resolution. However, to the best of author's knowledge the targeted Pipeline ADC in this research has one of the toughest requirements reported in the literature so far.

Most of the ADCs reported in prior work that have high sampling rates use time-interleaved structures (2), (3), (6), (11), (12), and (13). Time-interleaving increases the speed of the ADC by a factor equal to the number of parallel channels. However, time-interleaved ADCs suffer from three main problems: offset, gain and phase mismatch between sub-ADCs in different channels. Other impairments such as bandwidth and nonlinearity mismatch between channels also degrade the performance but are considered second-order effects (6) and are not limiting factors in this application. While gain and offset mismatch could be eliminated using traditional techniques such as digital calibration (12), phase mismatch between channels is harder to compensate and needs

more attention. Considering all these issues, a time-interleaved structure is chosen for this design.

Another alternative in this design is the front-end sample-and-hold amplifier (SHA). A front-end SHA adds extra power consumption to the ADC while contributing to significant noise and nonlinearity. An SHA-less architecture has been used by many recent works such as (1), (5), and (10), and in (4) only a buffer is used at the input. However, for a time-interleaved structure, a front-end SHA is almost essential as it removes the problem of phase mismatch (clock and data skew) in parallel channels. Without an SHA, calibration techniques are needed to decrease the effect of phase mismatch between channels (14). In this work, a front-end sample-and-hold amplifier is also designed as an alternative to demonstrate the effectiveness of the proposed technique.

The high sampling rate is an incentive to exploit another commonly used technique which increases the effective sampling rate without imposing extra settling requirements on the operational amplifiers (Opamps). This technique is called double-sampling and was first introduced in (18). Double-sampling was used in pipeline ADCs and many other architectures as in (19) and (20). This technique doubles the sampling frequency while keeping the Opamp settling requirements unchanged. However, it has its own drawbacks such as the memory effect and gain and offset mismatch. Therefore, extra care is needed to overcome these non-idealities (21). The memory effect can be cancelled by resetting the Opamps between the two phases if the sampling frequency is not very high. For high

**Table 1. Summary Of The Prior Art.**

| Reference | Year | Resolution | Sampling Rate | SNDR | Power | Process | Structure |
|---|---|---|---|---|---|---|---|
| (1) | 2009 | 10 bit | 500 MS/s | 52 dB | 55 mW | 90 nm CMOS | Single-core |
| (2) | 2011 | 11 bit | 500 MS/s | 59 dB | 105 mW | 40 nm | 4x Time-interleaved |
| (3) | 2007 | 11 bit | 800 MS/s | 54 dB | 350 mW | 90 nm | 4x Time-interleaved |
| (4) | 2010 | 16 bit | 250 MS/s | 76.5 dB | 1 W | 0.18 um CMOS | Single-core |
| (5) | 2010 | 10 bit | 100 MS/s | 53.9 dB | 4.5 mW | 90 nm CMOS | Single-core |
| (6) | 2006 | 11 bit | 1 GS/s | 55 dB | 250 mW | 0.13 um CMOS | Time-interleaved |
| (7) | 2006 | 14 bit | 125 MS/s | 72 dB | 1.85 W | 0.35 um BiCMOS | Single-core |
| (8) | 2010 | 16 bit | 160 MS/s | 74.5 dB | 1.6 W | 0.25 BiCMOS | Single-Core |
| (9) | 2009 | 16 bit | 125 MS/s | 78.6 dB | 385 mW | 0.18 um CMOS | Single-core |
| (10) | 2008 | 14 bit | 100 MS/s | 72.4 dB | 230 mW | 0.18 um CMOS | Single-core |
| (11) | 2008 | 10 bit | 1.35 GS/s | 50 dB | 175 mW | 0.13 um CMOS | 16x Time-interleaved |
| (12) | 2009 | 10 bit | 1 GS/s | 56 dB | 2.5 W | 0.18 um CMOS | 2x Time-interleaved |
| (13) | 2011 | 12 bit | 3 GS/s | 59 dB | 500 mW | 40 nm CMOS | 2x Time-interleaved |
| (14) | 2014 | 12 bit | 1.6 Gs/s | 58 dB | 1.15 mW | 0.18 um BiCMOS | 4x Time-Interleaved |

sampling frequencies, calibration techniques can be used to suppress this problem. Calibration can also take care of gain and offset errors.

## 1.2 Organization of Dissertation

After the introduction in chapter 1, this dissertation first reviews the design of a 12-bittime-interleaved ADC in chapter 2. In this chapter a brief introduction precedes the circuit design and the simulation results of the ADC. In chapter 3 calibration of errors in time-interleaved ADCs is discussed and more simulation results are presented. In chapter 4 the proposed calibration technique is explained and simulation results are shown. The work is concluded in chapter 5.

# 2 DESIGN OF A 12-BIT 650MSPS TIME-INTERLEAVED ADC

## 2.1 Introduction

As discussed in chapter 1, the objective of this research is to design a high speed and high resolution Pipeline ADC for digital beam forming applications with 12 bits of resolution (ENOB of 11 bits). Since the signal has 120 MHz bandwidth and is located at frequencies between 1.2 GHz and 1.3 GHz, we can exploit undersampling to save a considerable amount of power. Therefore, the sampling frequency is chosen to be 650 MSps. This selection of the undersampling frequency is discussed in the next section. The analog signal bandwidth of the whole ADC should be 1.5 GHz and the power consumption should be less than 500 mW. The technology which has been used in this design is the IBM BiCMOS 8HP with a power supply of 2.5 V for analog blocks and 1.2 V for digital blocks. Design specifications of the sub-blocks are explained in the following sections.

### 2.1.1 Undersampling

Undersampling is the process of sampling a band limited signal whose spectrum is centered at a frequency of f0 with a sampling frequency less than f0. As a result, the signal spectrum will be shifted and centered around +/-(fs-f0). Figure 1 illustrates the method with two examples.

In the first example, the sampling frequency is less than f0 (Figure 1.b) and moves a replica of the signal from the third Nyquist zone to the base-band. The signal is not

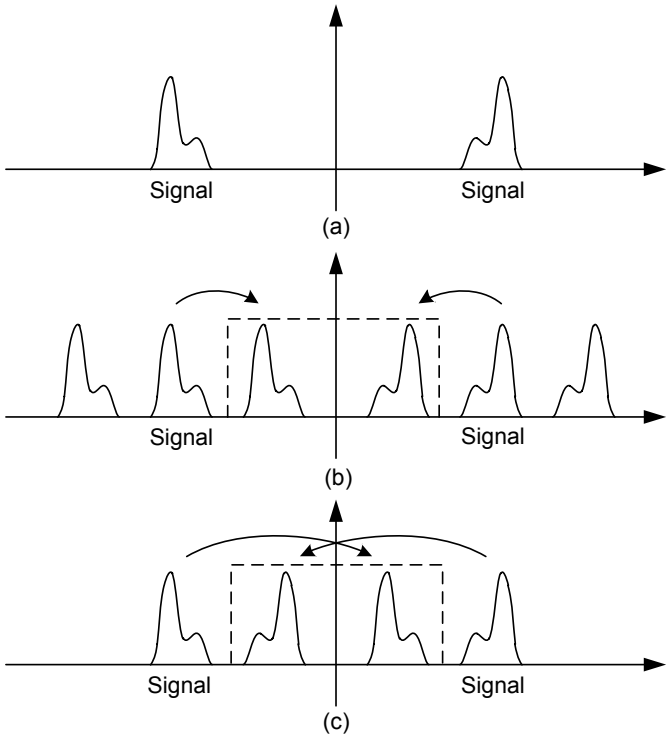



**Figure 1. Undersampling of a signal in the second and the third Nyquist band (22).**

mirrored in this case. In the second example (Figure 1.c), however, the sampling frequency is larger than f0. That results in the replica of the signal from the second Nyquist zone to be moved to the base-band and therefore the signal is mirrored.

Using the same procedure, we can set the sampling frequency such that higher Nyquist zones are in the base-band and hence reduce the sampling frequency. However, the minimum sampling frequency is twice the bandwidth of the signal to avoid the loss on the data, i.e.,

$$f_S > 2BW \quad . \qquad (1)$$

To make sure that no aliasing will occur, the following equation should be satisfied,

$$f_S = \frac{4f_C}{2N-1}, \qquad (2)$$

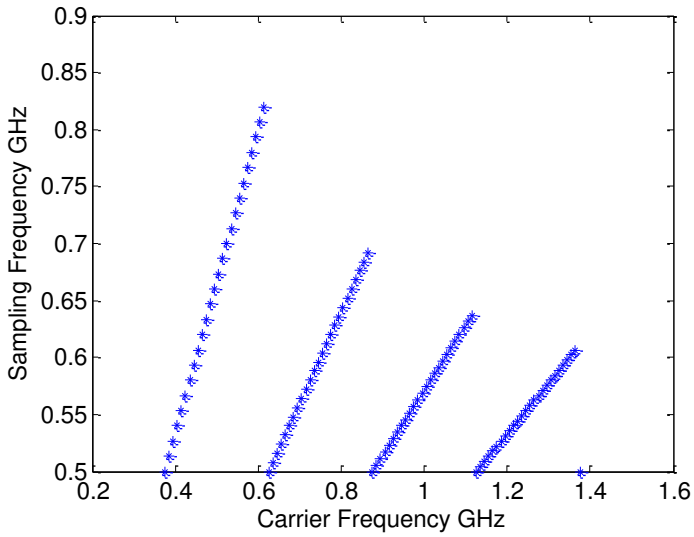



**Figure 2. Minimum possible value for the sampling frequency (largest N) vs. the carrier frequency for the signal bandwidth of 120 MHz according to equation (2).**

where N=1, 2, 3, … is the Nyquist zone in which the carrier and its signal fall (23). By choosing a proper sampling frequency much lower than the Nyquist rate, we can relax the requirements on the input sample and hold circuit. The value of N can be varied to support the trade-offs between sampling frequency and the complexity of the input anti-aliasing filter (Figure 2). Since the carrier frequency is larger than 1.12 GHz, the minimum possible sampling frequency (largest N according to equation (2)) of the SHA is 650 MHz.

### 2.1.2 ADC Structure

The ADC structure is shown in Figure 3. It is a 2-channel time-interleaved pipeline ADC with a front-end SHA. The maximum sampling frequency of the SHA is 650 MHz. After the input signal is sampled with the SHA, two channels of pipeline ADCs take the baseband signal to digitize. The sampling rate of each channel is half of the sampling rate of the SHA. Also, the linearity of the SHA must be as good as the linearity of the total ADC.

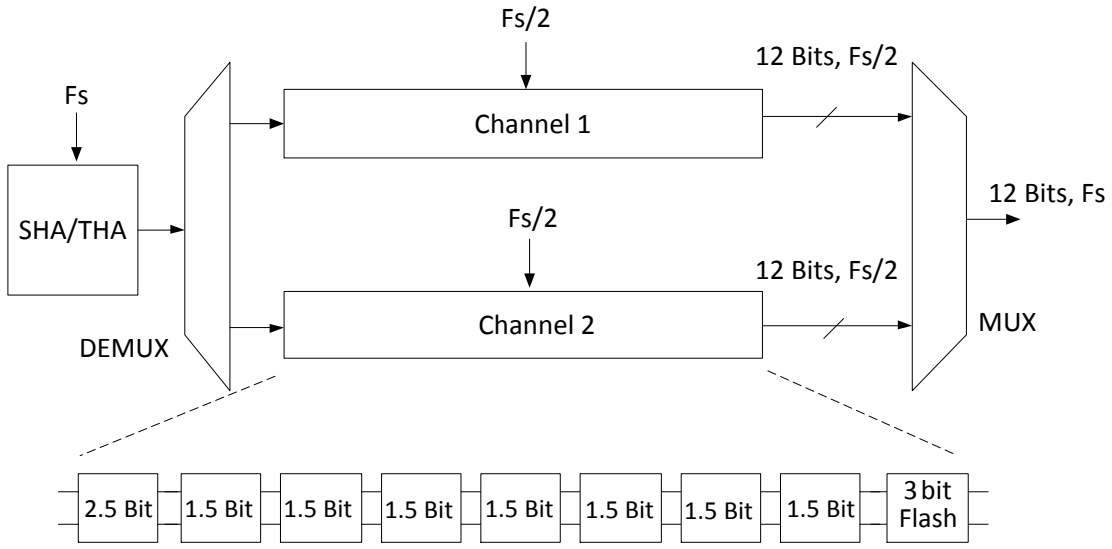



**Figure 3. ADC Architecture.**

Each block of the ADC will be discussed in detail in the following sections. Many different considerations factor into the design of a 12 bit (11 bit effective) 650 MSPS ADC. These considerations include the number of stages, the gain of each stage, different

techniques to improve the performance of the stages, Opamp topology, capacitor scaling, use of a front-end SHA, the number of channels if a time-interleaved structure is selected, budgeting for different types of noise sources which are quantization noise, thermal noise and distortion, and the sampling frequency since the input signal is an intermediate frequency (IF) signal. Figure 4 shows the design and optimization procedure.

### 2.1.3 Noise Calculations

Considering the front-end SHA, the total input referred noise of the ADC is equal to

$$V_{n,th,ADC}^{2} = V_{n,th,SHA}^{2} + V_{n,th,S1}^{2} + \frac{1}{G_1^2} V_{n,th,S2}^{2} + \frac{1}{G_1^2 G_2^2} V_{n,th,S3}^{2} + \ldots \quad . \qquad (3)$$

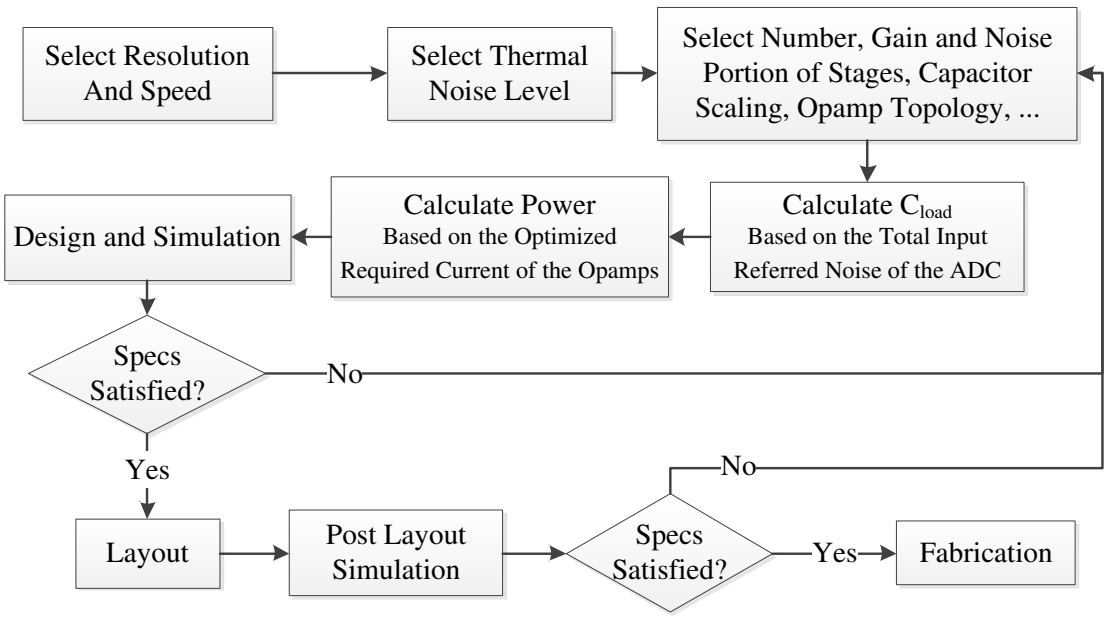



**Figure 4. The ADC Optimization Procedure.**

In this equation, the input referred noise of the $i_{th}$ gain stage as in Figure 5 is equal to

$$V_{n,th,Si}^{2} = 2kT\left(\frac{1}{C_{si}} + \frac{\omega_{ui}}{G_i}\left(\frac{2R_i}{G_i} + R_{opi}\right)\right), \qquad (4)$$

where $C_{si}$ is the total sampling capacitor of the stage, $\omega_{ui}$ is the gain-bandwidth of the amplifier, $G_i$ is the gain of the stage, $R_i$ is the on-resistance of the switches, and $R_{opi}$ is the equivalent resistance to model the Opamp input referred noise (24). Using the same size capacitors for each stage, the thermal noise for each stage is the same and can be written as

$$V_{n,th,ADC}^{2} = V_{n,th,SHA}^{2} + V_{n,th,S1}^{2} + \frac{1}{G_1^2}V_{n,th,S1}^{2} + \frac{1}{G_1^2 G_2^2}V_{n,th,S1}^{2} + \ldots \quad . \qquad (5)$$

The thermal noise of stages after the third stage will be negligible since they are divided by a large value which is the product of the gain of all previous stages. Therefore,

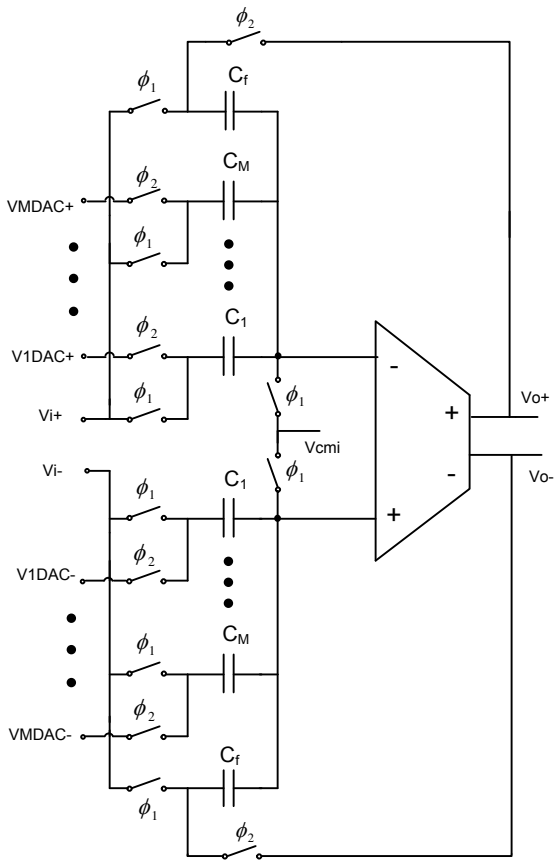



**Figure 5. Switched-capacitor gain stage with the gain of $G_i$ .**

$$V_{n,th,ADC}^2 = V_{n,th,SHA}^2 + V_{n,th,S1}^2 \left(1 + \frac{1}{G_1^2} + \frac{1}{G_1^2 G_2^2}\right). \qquad (6)$$

$$V_{n,th,ADC}^2 = V_{n,th,SHA}^2 + 1.3 V_{n,th,S1}^2$$

Now we consider the SHA contribution to the total noise. To get the optimized value for the SHA contribution, the value of the FOM is swept over the SHA noise contribution. Figure 6 shows the FOM vs SHA noise portion. As can be seen in this figure, the optimum value of the SHA noise portion is around 50%. If we select the SNR due to the total thermal noise to be 80 dB (as a rule of thumb the noise level is chosen to be 6-8 dB

below the total SNDR which is 74 dB), we can calculate the value of the thermal noise of the SHA and hence the value of the thermal noise of the gain stages.

$$SNR_{n,th} = 10\log\left(\frac{V_{ref}^{2}/2}{V_{n,th,ADC}^{2}}\right) = 80\,dB$$

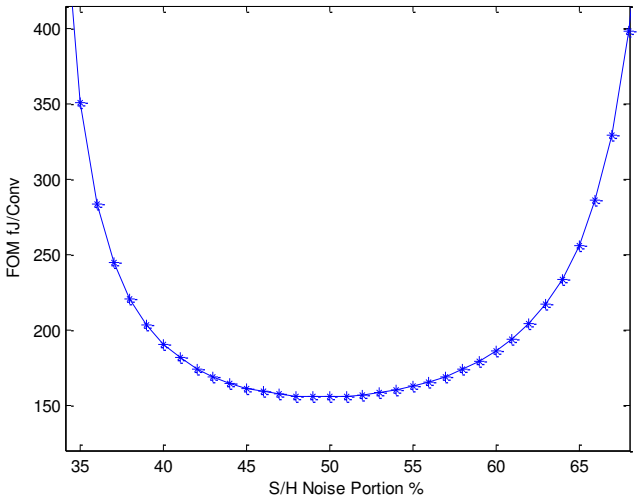



**Figure 6. FOM vs SHA noise contribution.**

By having the value of the thermal noise for the gain stages, we can calculate the value of the capacitors. These values are listed in Table 2.

**Table 2. The values of the capacitors of the gain stages.**

| Stage | SHA | 1 | 2 | 3 to 9 |
|---|---|---|---|---|
| Cap Size (pF) | 5 | 0.6 | 0.3 | 0.15 |

### 2.1.4 Clocks

Considering the ADC specifications, *Fin*=1.5 GHz, *Vref*=1, and a resolution N=12 bits, the jitter requirements of the clock for the SHA/THA can be calculated by

$$\Delta t < \frac{1}{2^{N+1}\pi F_i}. \qquad (7)$$

Therefore, Δt<12.9 fs. The equivalent rms voltage of the jitter is then

$$V_{jitter,rms} = \sqrt{2}\pi F_i V_{ref}\,\sigma = \sqrt{2}\times\pi\times 1.5GHz\times 1\times 12.9fs = 85\,uV \ .$$

Using the same procedure, the clock jitter for the gain stages can also be calculated. In this case *Fin*=162.5 MHz, and the resolution is 12 bits for the first stage, 11 bits for the second stage and decreases by 1 bit at each stage. Table 3 shows the value of the clock jitter needed for different stages.

**Table 3. The jitter requirements of the stages.**

| Stage # | SHA/THA | 1 | 2 | 3 | 4 | 5-9 |
|---|---|---|---|---|---|---|
| Clock Jitter (fs) | 12.9 | 120 | 480 | 960 | 1920 | >3800 |

Figure 7 shows the clock waveforms. There are three main sets of clocks used in the ADC. They are

The sample and hold clock set ($\phi_{1,SH}$), the gain stage 1 clock set ($\phi_{1i,GS}$) and the second gain stage ($\phi_{2i,GS}$). Each of these sets of clocks has four versions. For example, for the SHA clock these versions are: phase one ($\phi_{1,SH}$), phase 2 ($\phi_{2,SH}$), delayed phase one ($\phi_{1d,SH}$), and delayed phase 2 ($\phi_{2d,SH}$).

## 2.2 Circuit Design

### 2.2.1 Sample-and-Hold Amplifier

The SHA is shown in Figure 8. A flip-around structure is selected to reduce the power consumption since its feedback factor is less in comparison with the charge-redistribution structure.

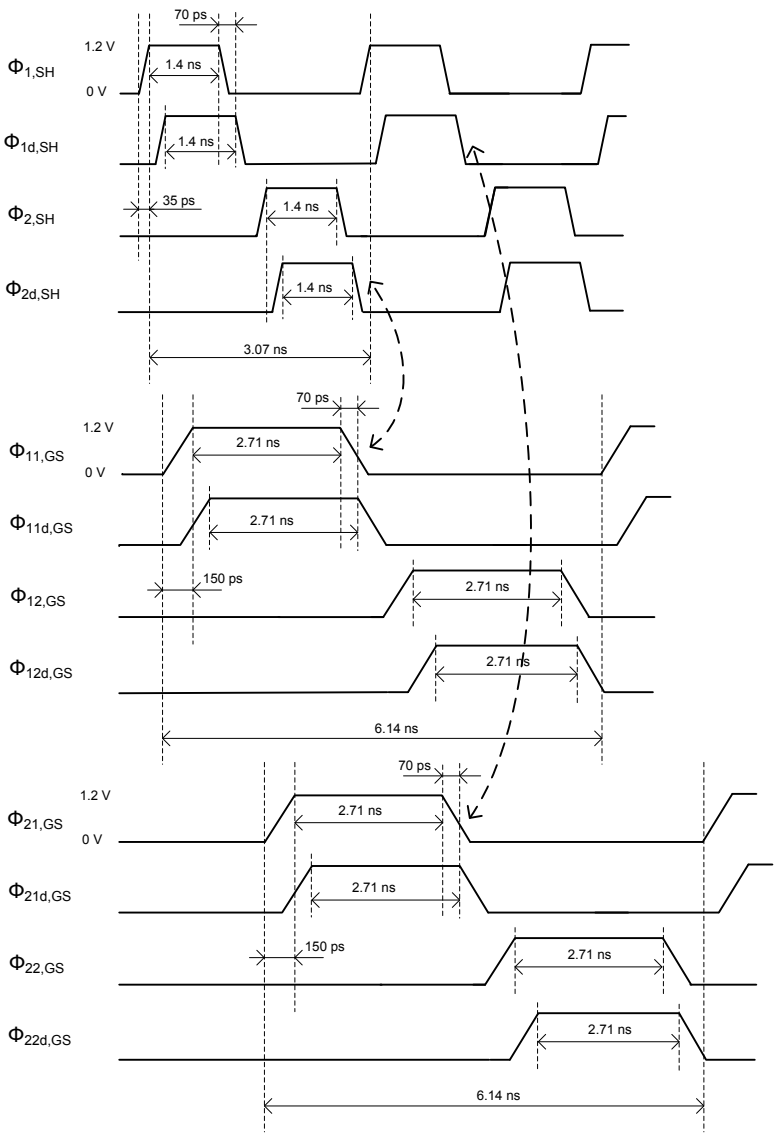



**Figure 7. The clocks used for the whole ADC. The first four clocks are used for the SHA and the next four are used for the gain stages. The falling edges which should be aligned are shown with arrows.**

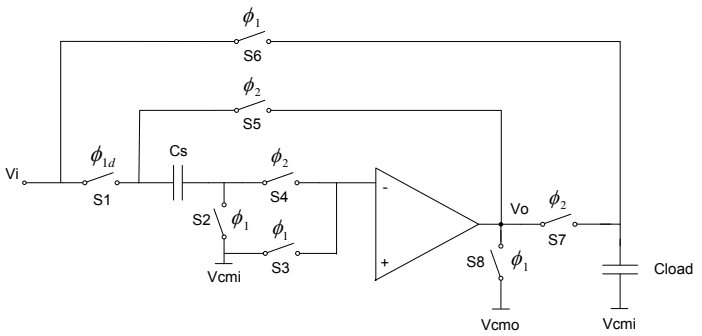



**Figure 8. The SHA circuit (single-ended shown for simplicity).**

Table 4 reports the details of the SHA block.

**Table 4. The specs of the SHA stage.**

| | | |
|---|---|---|
| Opamp | Gain | 90 dB |
| | Bandwidth | 2.5 GHz |
| | Load Cap | 4 pF |
| | Linearity | 12 bits |
| | Settling Time | 1.4 ns |
| | Supply Voltage | 2.5 V |
| | Voltage Swing | 2 Vp-p |
| | Power | 40 mW |
| Switches | On Resistance | 3.7 Ω |
| | Linearity | 12 bits |
| Clock Frequency | | 325 MHz |
| Clock Voltage Levels | Bootstrap | 0 – 1.2 V |
| | Transmission Gate | 0 – 2.5 V |
| Sampling Cap | | 5 pF |
| Clock Jitter | | 12 fs |
| Input Referred Noise rms Voltage within the band of interest (250 MHz) | | 51 uV |
| Analog Bandwidth | | 1.5 GHz |
| Vcmi | | 1.85 V |
| Vcmo | | 1.2 V |
| Total Power of the Stage | | 40 mW |

As discussed previously, by using the double-sampling structure which improves the performance and reduces power consumption, the clock frequency of the SHA circuit could be divided by two which is 325 MHz. The input switches should be bootstrapped switches for higher linearity but other switches could be transmission-gate switches. Behavioral simulations were run with ideal components and showed more than 12 bits linearity.

#### *2.2.1.1 Bootstrapped Switches*

The sampling network consists of two switches (S1 and S2) and a sampling capacitor. Bottom-plate sampling is done to reduce the effect of charge injection. S1 is a bootstrap switch and S2 is a transmission gate. Figure 9 shows the circuit of the bootstrap switch.As discussed before, the sampling frequency of the SHA circuit could be as low as 325 MHz. However, since the input signal is an IF signal which might have components up to 1.5 GHz, this switch should be able to sample a 1.5GHz signal. The value of the on-resistance of the switch can be found according to the RC time constant of the switch which should be as linear as the required linearity for the whole ADC. Therefore, the

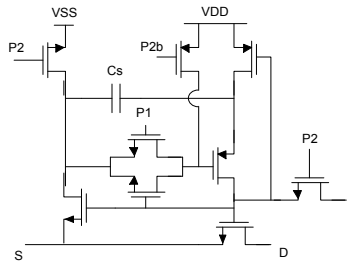



**Figure 9. The Bootstrap Switch.**

switch should have 12 bits linearity and works at 1.5 GHz to be able to track the input signal

$$e^{-t/\tau} < \frac{1}{2^{13}} \rightarrow \quad \tau < \frac{1}{2f_{in} N \ln(2)} \qquad (8)$$

where $\tau = RC$ . The sampling capacitor C is 5 pF from thermal noise considerations. Therefore, the value of the on-resistance should be less than or equal to 8 Ohms. The designed value is less than 5 Ohms considering both resistances of the bootstrap and the transmission-gate switch.

Figure 10 shows the input and the output of the test circuit. The input is a 1.5 GHz sinusoidal and the sampling frequency is 325 MHz. As shown in this figure, the output is able to track the input in the first phase, and hold it in the second phase. The linearity of the switch is measured by taking the FFT of the output which is shown in Figure 11. The SFDR is 83 dB.

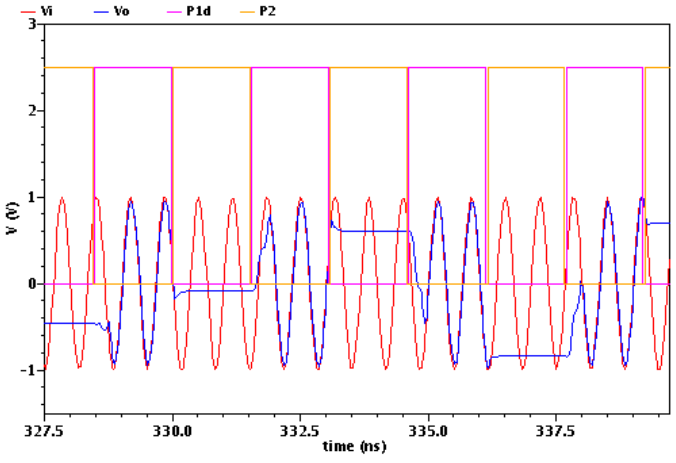



**Figure 10. The input and the output of the test circuit.**

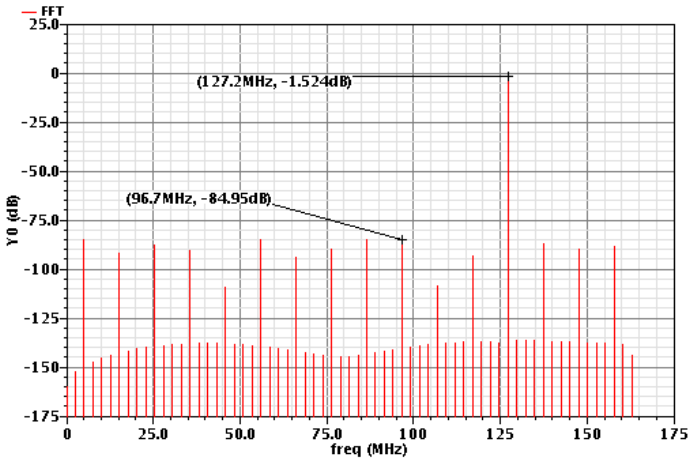



**Figure 11. The output FFT of the switch test circuit.**

*2.2.1.2 Operational Transconductance Amplifier*

A single stage telescopic cascode structure is used for the Opamp and a buffer stage is added at the input to increase the input impedance. The schematic of the Opamp is shown in Figure 12.

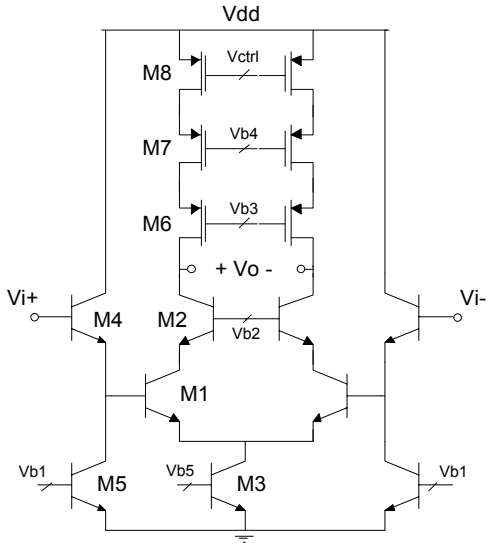



**Figure 12. The schematic of the Opamp.**

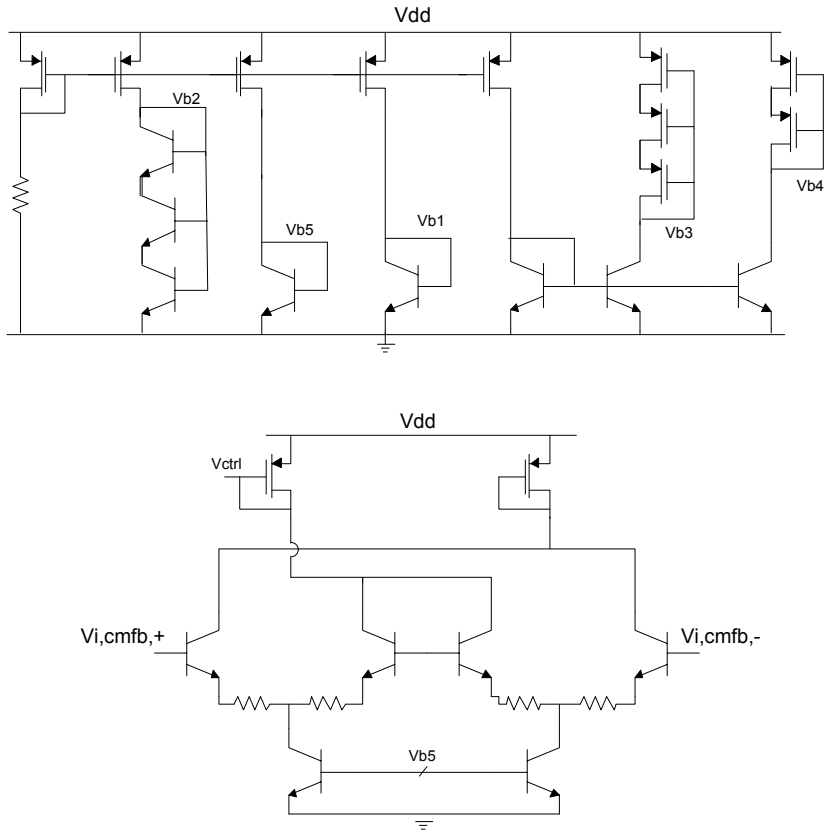



**Figure 13. The bias and the CMFB circuit of the Opamp.**

The bias circuit is shown in Figure 13. An off-chip resistor of 15 KΩ drives the total bias circuit. Figure 13 also shows the common-mode feedback (CMFB) circuit used for the Opamp which has a continuous-time structure. Figure 14 shows the frequency response of the opamp.

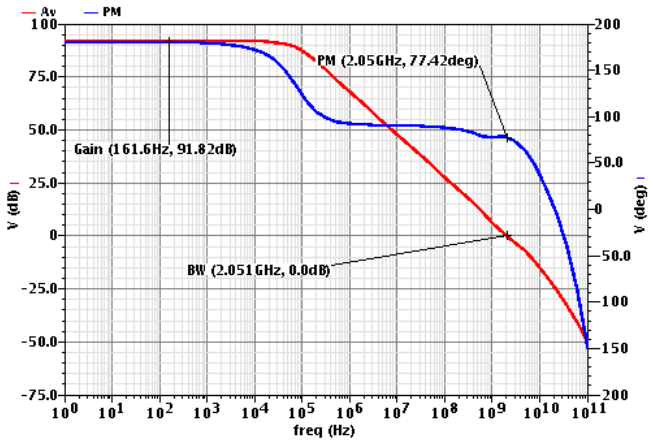



**Figure 14. The frequency response of the opamp.**

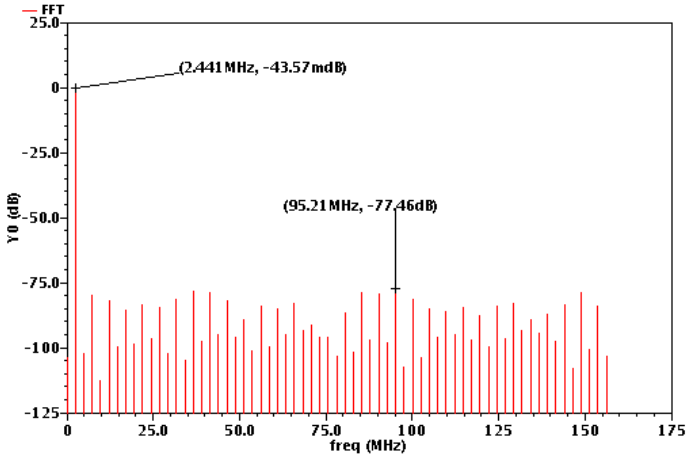



**Figure 15. The FFT of the output of the SHA with a 1.5-GHz input and sampling frequency of 325 MHz.**

For assessing the Opamp's transient response, it is placed in the SHA structure shown in Figure 8. Figure 15 shows the FFT of the output of the SHA for a 1.5 GHz sinusoidal input and the sampling frequency of 325 MHz. The SFDR is 77 dB. Table **5** reports the characteristics of the Opamp.

**Table 5. The characteristics of the designed Opamp.**

| | | |
|---|---|---|
| DC Gain | | 91 dB |
| BW | | 2 GHz |
| PM | | 77 Deg |
| Supply Voltage | | 2.5 V |
| Output Swing | | 2 V p-p |
| Cload | | 4 pF |
| Clock Frequency | | 312 MHz |
| Power Consumption | Total | 38.1 mW |
| | Opamp | 19.3 mW |
| | Bias | 9.3 mW |
| | CMFB | 9.5 mW |
| SFDR | | 77 dB |

*2.2.1.3 SHA Simulation*

As Figure 8 shows, the sample and hold circuit uses a pre-charging technique. In this technique, the load capacitor is pre-charged during the first phase as well as the sampling capacitor (25). Therefore, in the hold phase the Opamp does not need to provide the whole current to charge the load capacitor completely and it only provides the current for a small portion of it since it has already been charged to a value close to its final value. Therefore, $C_{load}$ does not need to be charged with high accuracy during phase 1 and the linearity requirement for the added sampling switch is relaxed. Using this technique, the Opamp slew rate requirement is relaxed which in turn helps to save power.

Figure 16 shows the SHA and its connection to the first gain stage. A total of 12 clock waveforms are needed for the whole ADC.

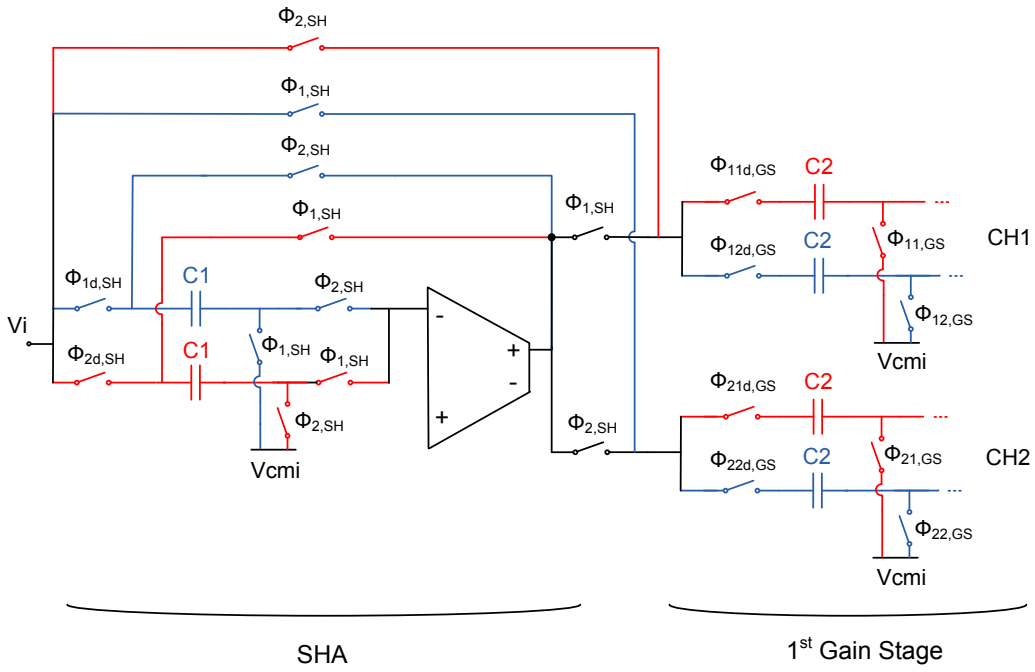



**Figure 16. The front-end SHA and its connection with the first gain stage. Single-ended is shown for simplicity.**

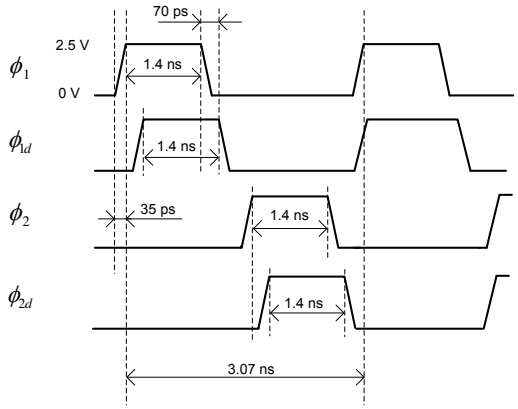



**Figure 17. The clocks used in the SHA circuit.**

Figure 17 shows the clock waveforms used for the SHA. As discussed before, bottom-plate sampling is done to reduce the charge-injection effect which improves the linearity. Therefore, we have $\phi_1$, a delayed version of $\phi_1$ which is called $\phi_{1d}$ for the bottom-plate sampling, $\phi_2$ and a delayed version of $\phi_2$. To simplify the clock generation circuit, $\phi_{1d}$ is generated by delaying $\phi_1$ and the same is for $\phi_2$. The details of the clock timings are demonstrated in Figure 17.

The input switches which sample the input, connect the sampling caps to the output of the Opamp and connect the load caps to the output of the Opamp are all bootstrap switches. All other switches are transmission-gate switches.

Figure 18 shows the transient output of the SHA for a step input with 400 mV amplitude. As the figure shows, the output settles very well after the caps are pre-charged which obviously improves the settling behavior. The other thing to note in this circuit is

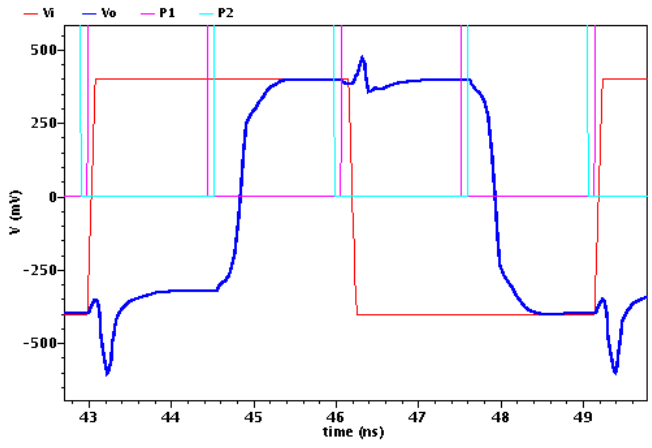



**Figure 18. The step response of the SHA.**

that usually we have the problem of memory effect in SHAs which is commonly taken care of by resetting the output of the Opamp to the common-mode (CM) voltage value during the sample phase in which the opamp is not used. Since we are using double sampling, we do not have that alternative and the Opamp is working in both phases. Using the pre-charging technique also helps to solve the memory effect problem to some extent.

To verify and measure the linearity of the SHA, a 1.55 GHz sinusoidal input is applied and an FFT is taken from the output which is shown in Figure 19. Therefore, a 1.55 GHz input is sampled with the sampling rate of 650 MHz using this SHA. The SFDR is 74.7 dB which is equivalent to 12.1 bits resolution. To measure the analog bandwidth of the SHA, input signals different frequencies are

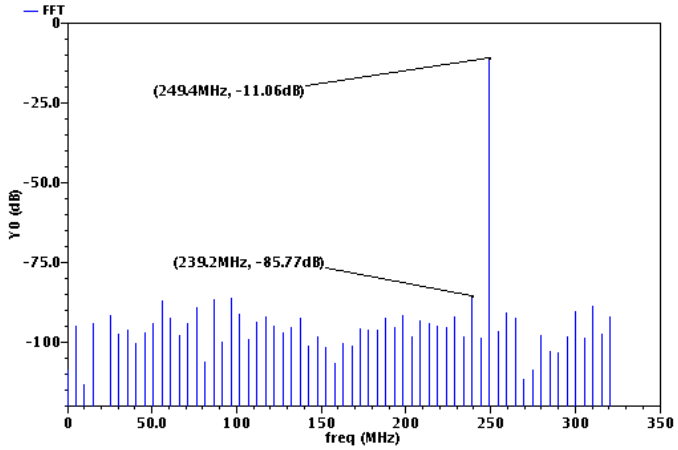



**Figure 19. Output spectrum for a 1.55 GHz sine input and sampling rate of 650 MHz. The SFDR is 74.7 dB.**

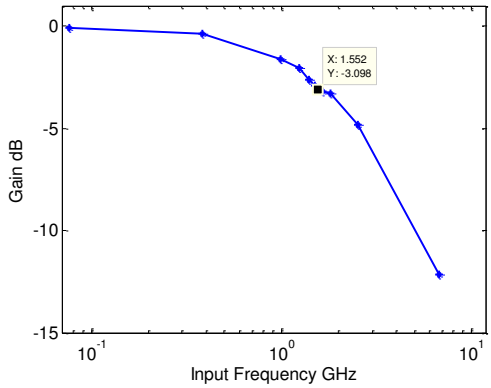



**Figure 20. The gain of the SHA vs. the input frequency. The analog bandwidth of the SHA is 1.55 GHz.**

applied to the SHA and the gain of the SHA is measured. Figure 20 shows this plot. According to this figure, the bandwidth of the SHA is around 1.55 GHz.

Figure 21(a) shows another plot which is the SFDR vs. the output swing. As shown in this figure, the SFDR is around 75 for output swings up to 800 mV and

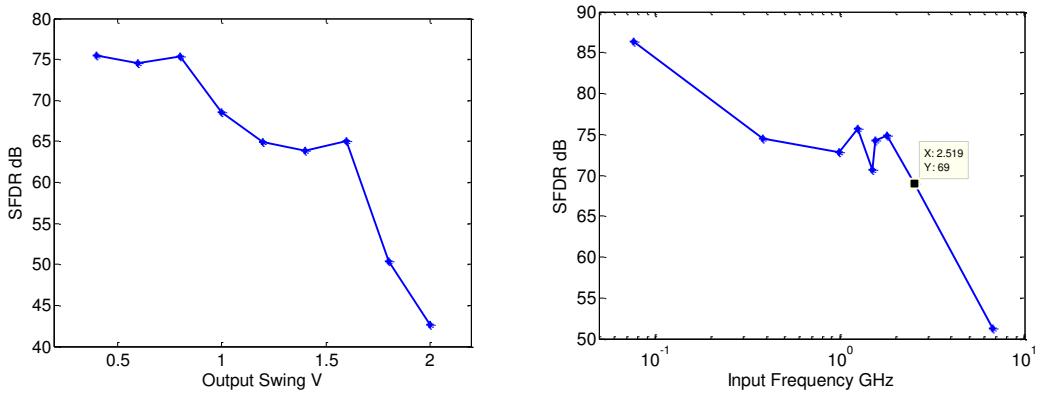



**Figure 21.a) The SFDR vs. the output voltage swing with 1.24 GHz input frequency. b) The SFDR vs. the input frequency with 0.8 V voltage swing.**

decreases as the output swing increases. If we are looking for a larger dynamic range, we should try to increase the output swing which is possible to be done by decreasing the parasitic cap of the switches, which in turn can be done by decreasing the size of these switches. Figure 21(b) shows the SFDR of the SHA vs. the input frequency. According to this plot, the linearity of the SHA is assured up to frequencies close to 2.5 GHz. Moreover, this figure shows that the linearity of the SHA is better than 12 bits when signals around 100 MHz are applied. This highlights the importance of the input signal frequency. For example, if this circuit is used in a regular Nyquist sampling architecture it could reach more than 80 dB linearity, while when used in an under-sampling structure the SFDR degrades by around 10 dB.

Table 6 shows the characteristics of the designed SHA. As it is seen in the table, the power consumption of the clock generation circuit dominates the total power consumption. This could be explained by the huge capacitor values which the clock

**Table 6. SHA specifications.**

| | | |
|---|---|---|
| Clock Frequency | 325 MHz | |
| Sampling Rate | 650 MSps | |
| Input Frequency | 1.5 GHz | |
| Input Amplitude | 800 mVp-p | |
| Analong Bandwidth | 1.55 GHz | |
| Power Consumption | SHA | 38 mW |
| | Clock Generation Circuit | 50 mW |
| | Total | 88 mW |
| SFDR | Ideal clock | 74 dB |
| | Real clock | 65 dB |

generation circuit should drive. Therefore, trying to decrease the parasitic caps will help to save power too. As shown in

Table 6 the performance of the SHA is also degraded as ideal clocks are replaced with the real circuit.

*2.2.1.4 Design Comparison: Track-and-Hold versus Sample-and-Hold Amplifier*

A comparison between the designed SHA and an example track-and-hold amplifier (THA) is presented. The THA uses a switched emitter-follower structure to track and hold the signal.

**Table 7. Comparison between the SHA and THA.**

| | Designed SHA | Sample THA |
|---|---|---|
| Sampling Frequency (MSPS) | 650 | 650 |
| Voltage Supply (V) | 2.5 | 2.5 and 3 |
| Power (mW) | 88 | 150 |
| SFDR (dB) | 65 | 55 |

Table 7 reports a comparison between the performances of the two blocks. As this table shows, the performance of the SHA is better in terms of SFDR and power consumption but the SHA needs non-overlapping clocks while THA works with overlapping clocks.

### 2.2.2 Gain Stages

*2.2.2.1 Operational Transconductance*

A second OTA is designed for the first stage, which is a 2.5-bit gain stage. To decide on the optimum topology, a comparison between a bipolar and a CMOS input pair OTA has been made. Figure 22 shows these two topologies.

Table 8 shows the major differences between these two OTAs for two example designs with the same power. As Table 8 shows, the bipolar-input OTA has a larger $G_m$ and at the same time a lower noise level, while both of the OTAs consume the same amount of power.

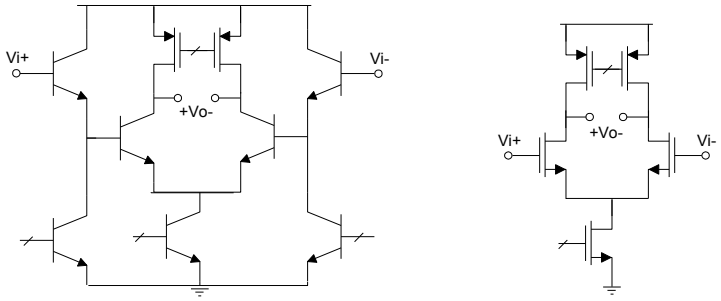



**Figure 22. Bipolar input and CMOS input OTAs.**

**Table 8. Comparison between a bipolar and a CMOS input OTA.**

| | Bipolar | CMOS |
|---|---|---|
| Gm (mA/V) | 85 | 35 |
| Noise Power $(nV)^2/Hz$ | 1.87 | 3.74 |

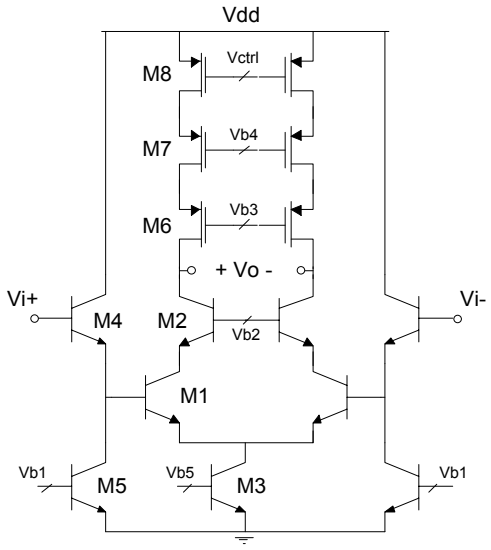


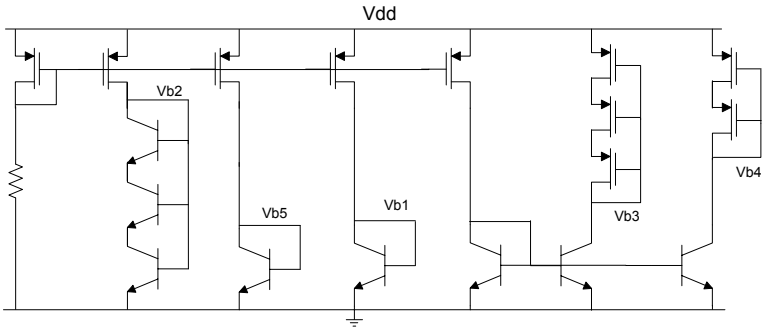

**Figure 23. The Second OTA.**

Therefore, this obviously suggests the choice bipolar transistors for the input pair of the OTA. Based on this argument, a telescopic cascode OTA with bipolar inputs was selected and designed. Figure 23 shows the schematics of this OTA.

High-breakdown bipolar transistors and thick oxide PMOS transistors are used since the supply voltage is relatively large at 2.5 V. The input CM voltage of the OTA is 1.85 V and the output CM voltage is 1.2 V. Figure 24 shows the bias and the CMFB circuits used for the OTA.

Figure 25 shows the frequency response of the second OTA. In order to measure the linearity of the OTA, it is put in a 1.5-bit gain stage but in a slightly different architecture. Figure 26 (left) shows the residue versus input signal transfer curve of the 2.5 bit gain.

a)




b)

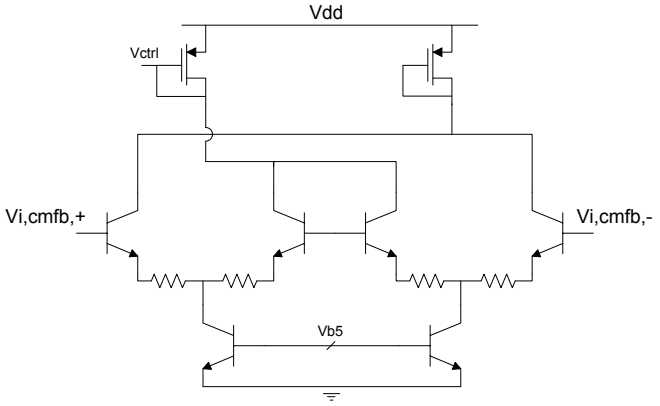



**Figure 24. a) The bias and b) CMFB circuits used for the second OTA.**

As this transfer curve is not linear in all parts, the linearity cannot be measured for the whole full-scale voltage range. Therefore, to measure the linearity for the full-scale voltage range, the structure of the gain stage is changed so that it produces a linear function for the full-scale voltage range. Therefore, the transfer characteristic will be similar to Figure 26 (right). Figure 27 shows the FFT plot of the output of the circuit for

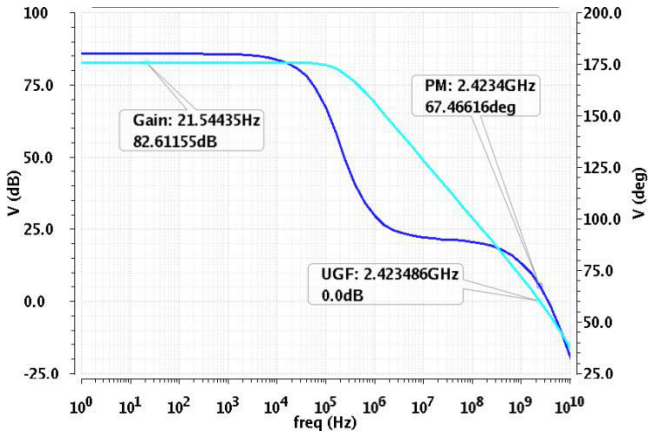



**Figure 25. The frequency response of the second OTA.**

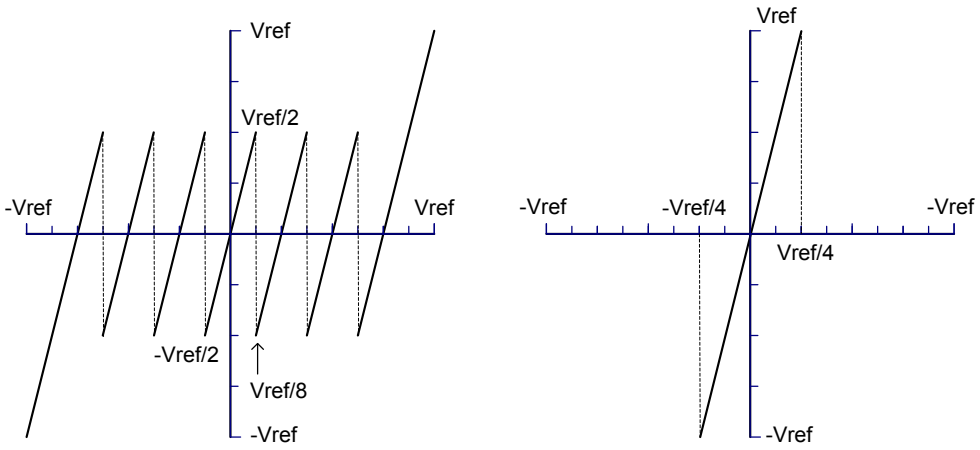



**Figure 26. The transfer characteristic of a 1.5-bit gain stage (left), and the modified gain stage to measure the linearity of the second OTA for the full-scale voltage range (right).**

1.6 Vp-p output voltage swing. Table 9 shows the performance of the OTA at the corners and Table 10 lists the specifications of the OTA.

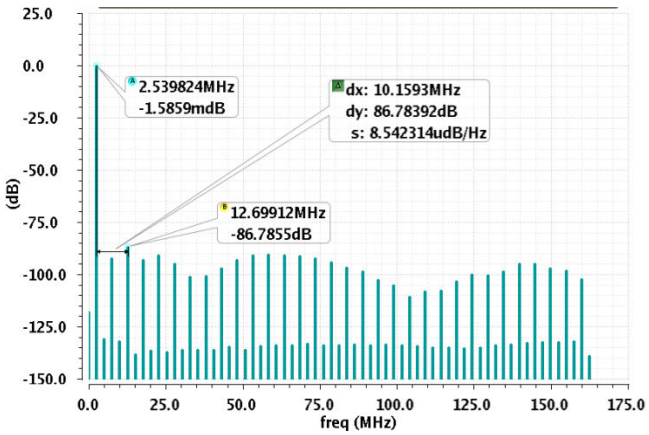



**Figure 27. The FFT of the output of the modified gain stage.**

**Table 9. OTA performance in corners.**

| Bias Vcmi = 1.85 V | | 1 Vp-p Output Swing | |
|---|---|---|---|
| corner | Temp | Vdd | SFDR dB |
| SF | 0 | 2.25 | 62 |
| FS | 85 | 2.75 | 96 |
| TT | 27 | 2.5 | 83 |

**Table 10. The specifications for the second OTA.**

| | | Required | Achieved |
|---|---|---|---|
| Gain | | 80 dB | 82.6 dB |
| BW | | 1.5 GHz | 2.4 GHz |
| PM | | - | 64 Deg |
| Cload | | 1 pF | 1 pF |
| SFDR/Resolution | | 62 dB/10 Bits | 86 dB/14 Bits (@2 Vp-p Output Voltage Swing) |
| Settling Time | | 3 ns | 3 ns |
| Maximum Output Swing (with 10 Bit Resolution) | | 1 Vp-p | 2.8 Vp-p |
| Power Consumption | OTA | - | 4 mW |
| | CMFB | - | 1.1 mW |
| | Bias | - | 4.7 mW |
| | Total | 10 mW | 9.8 mW |

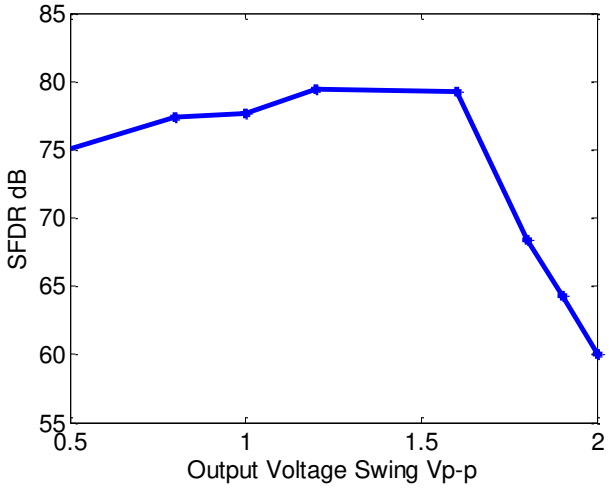



**Figure 28. The SFDR vs. the output voltage swing.**

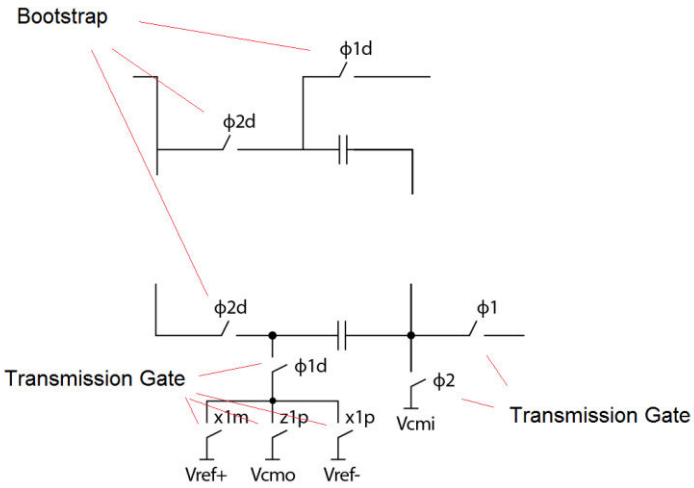



**Figure 29. The switches of the 2.5 gain stage.**

Figure 28 shows the SFDR vs. the output voltage swing. As this figure shows, the maximum output swing for which the 11-bit resolution is achieved is 1.8 Vp-p which is much greater than the required specifications for this stage.

#### *2.2.2.2 2.5-Bit Gain Stage*

For all the gain stages, a flip-around structure is used for lower power consumption. All the stages work with a 162.5-MHz clock and have the double sampling structure. Figure 29 shows the types of switches in the 2.5-bit gain stage. The switches that are on the signal path are bootstrap switches and other switches are transmission gate switches.

Table 11 shows the detailed characteristics of the 2.5-bit gain stage. A double-sampling technique is used for the gain stages as well. Therefore, theOopamps in the double-sampled stages work with a clock frequency of fs/4. Figure 30 shows the 2.5-bit gain stage with flip-around structure.

**Table 11. The characteristics of the 2.5-Bit gain stage.**

| | | |
|---|---|---|
| Opamp | Gain | 90 dB |
| | Bandwidth | 2.4 GHz |
| | Load Cap | 2 pF |
| | Linearity | 11 Bits |
| | Settling Time | 2.7 ns |
| | Supply Voltage | 2.5 V |
| | Voltage Swing | 2 Vp-p |
| | Power | 20 mW |
| Switches | On Resistance | 250 Ω |
| | Linearity | 12 bits |
| Clock Frequency | | 162.5 MHz |
| Clock Voltage Levels | Bootstrap | 0 – 1.2 V |
| | Transmission Gate | 0 – 2.5 V |
| Sampling Cap | | 0.6 pF |
| Clock Jitter | | 120 fs |
| Input Referred Noise rms Voltage within the band of interest (250 MHz) | | 51 uV |
| Analog Bandwidth | | 1.5 GHz |
| Vcmi | | 1.85 V |
| Vcmo | | 1.2 V |
| Vref | | 1 V |
| Vref+ | | 1.7 V |
| Vref- | | 0.7 V |
| Comparators | Offset | <125 mV |
| | Power | 0.4 mW |
| Total Power of the Stage | | 25 mW |

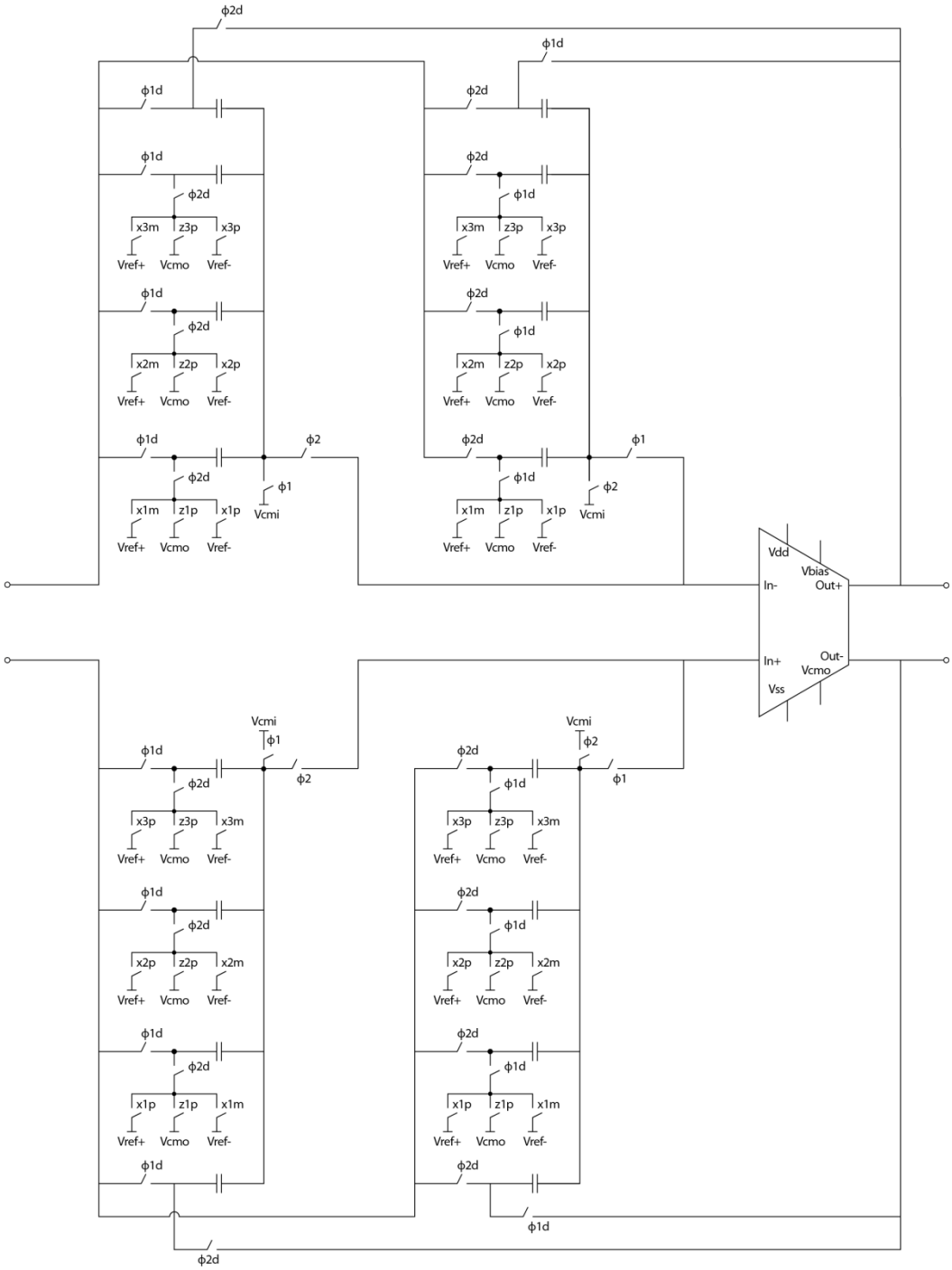



**Figure 30. The 2.5-bit gain stage circuit.**

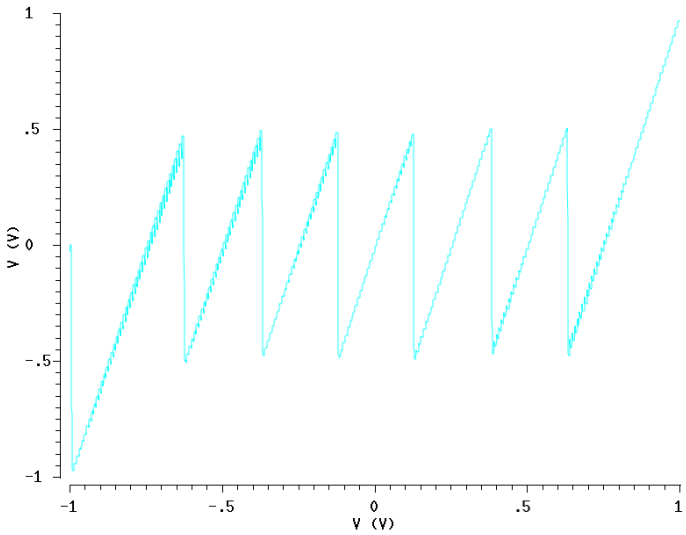



**Figure 31. The 2.5-bit gain stage residue versus input transfer curve.**

The DAC switches are controlled by the logic circuit. The outputs of the comparators generate the signals to control the switches of the gain stage. The logic circuit generates the output bits of the stage.

Figure 31 shows the residue versus the input signal transfer curve of the 2.5-bit gain stage. Since a double-sampling technique is used, the output is valid in both phases and the transfer characteristic will be continuous.

#### *2.2.2.3 1.5-Bit Gain Stage*

For this gain stage a flip-around structure is also used. Figure 32 shows the schematic of the 1.5-bit gain stage.

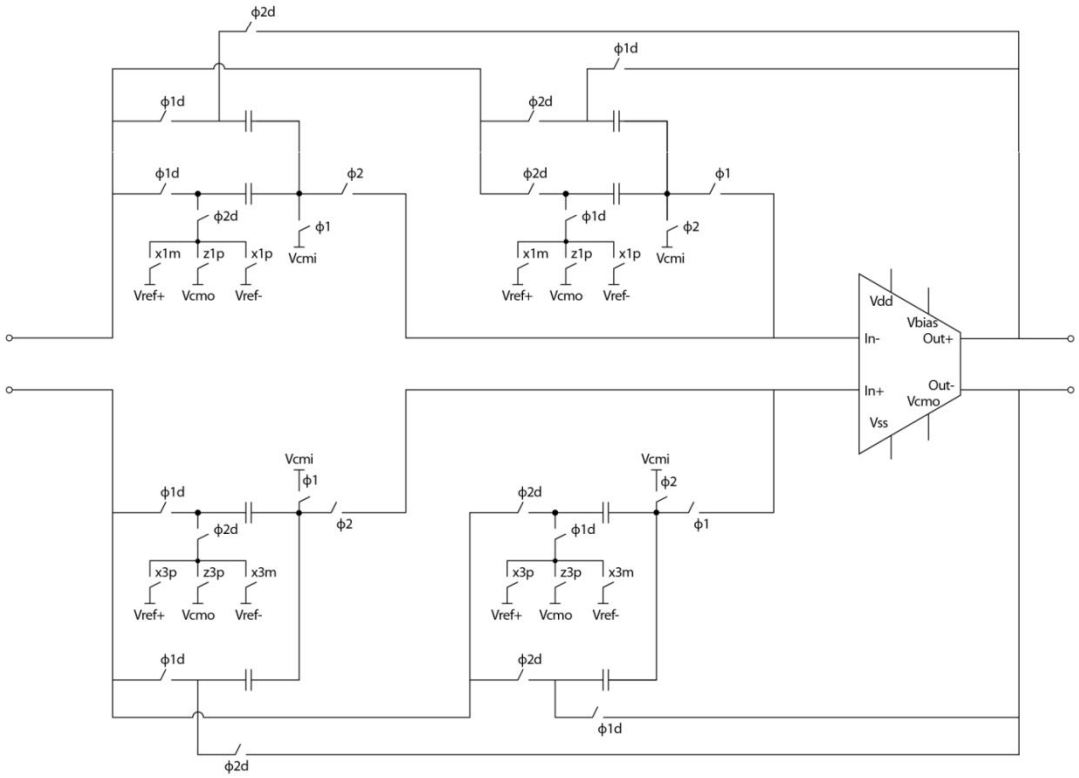



**Figure 32. The 1.5-bit gain stage.**

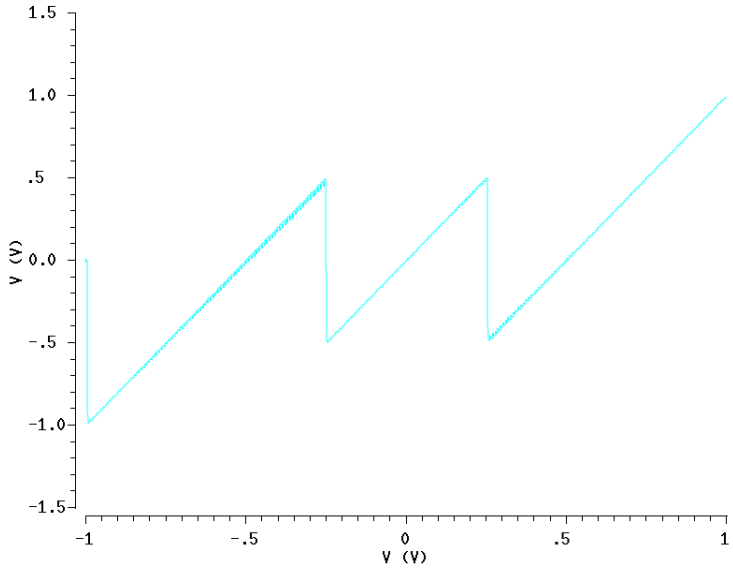



**Figure 33. 1.5-bit gain stage residue versus input transfer curve.**

In all the 1.5-bit pipeline stages which include stage 2 onward all switches are implemented with transmission gates.

**Table 12. The specs of the 1.5-Bit gain stage.**

| | | |
|---|---|---|
| Opamp | Gain | 78 dB |
| | Bandwidth | 1.5 GHz |
| | Load Cap | 1 pF |
| | Linearity | 10 Bits |
| | Settling Time | 2.7 ns |
| | Supply Voltage | 2.5 V |
| | Voltage Swing | 2 Vp-p |
| | Power | 10 mW |
| Switches | On Resistance | 650 Ω |
| | Linearity | 11 Bits |
| Clock Frequency | | 162.5 MHz |
| Clock Voltage Levels | Bootstrap | 0 – 1.2 V |
| | Transmission Gate | 0 – 2.5 V |
| Sampling Cap | | 0.3 pF |
| Clock Jitter | | 120 fs |
| Input Referred Noise rms Voltage within the band of interest (250 MHz) | | 51 uV |
| Analog Bandwidth | | 1.5 GHz |
| Vcmi | | 1.85 V |
| Vcmo | | 1.2 V |
| Vref | | 1 V |
| Vref+ | | 1.7 V |
| Vref- | | 0.7 V |
| Comparators | Offset | 250 mV |
| | Power | 0.4 mW |
| Total Power of the Stage | | 25 mW |

Table 12 shows the specs of the 1.5-bit gain stage. Other stages will use the same structure but the Opamp specs will be relaxed as we get closer to the end of the ADC. For 1.5-bit stages, the double-sampling technique is used as well. Figure 33 shows the 1.5-bit gain stage residue versus input transfer curve.

Other blocks of the ADC were designed and tested separately and integrated. These were a comparator, clock generation circuit, and digital sections (RSD logic and the 3-bit flash).

## 2.3 Simulation Results

Figure 34 shows the entire ADC schematics including the input SHA, two pipeline channels and two DACs at the output. Gain stages, 3-bit flash, delay elements and digital error correction are shown for each channel.

Figure 35 shows the FFT of the output of the ADC for a test sine wave. The SNDR is 65.1 dB.

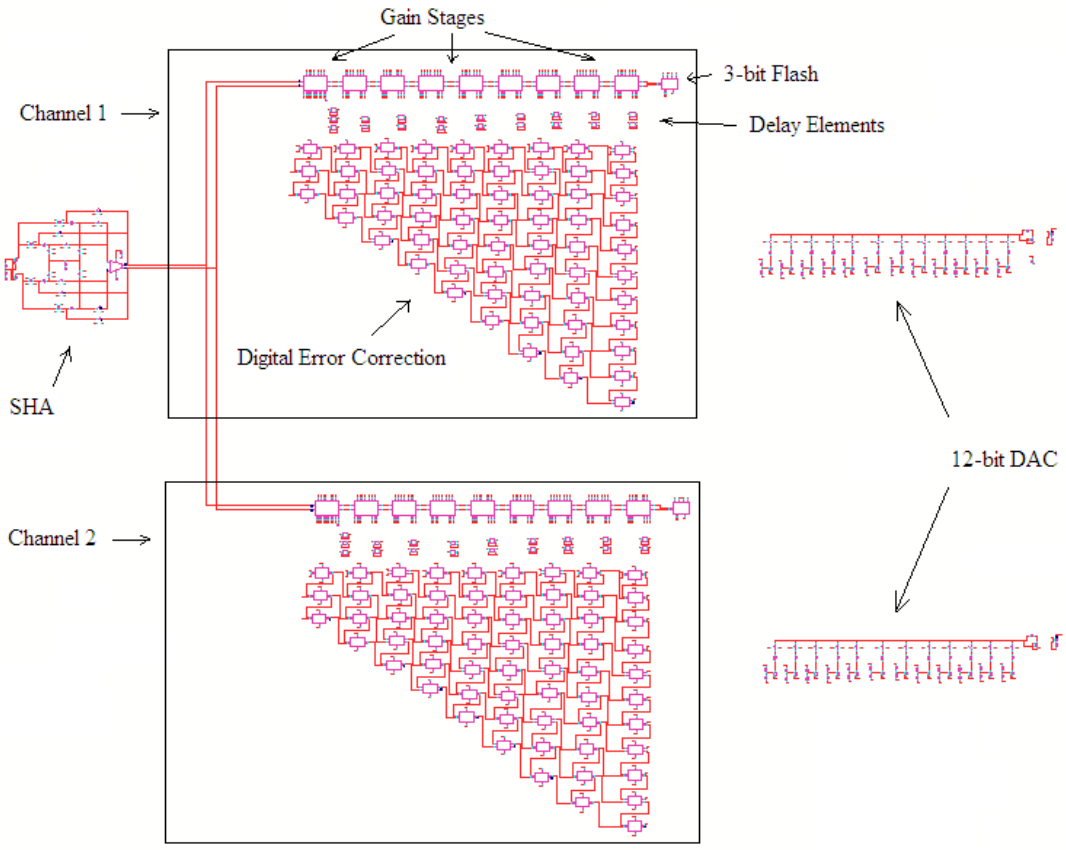



**Figure 34. The complete ADC schematic: the input SHA, the two channels, digital error correction and two DACs**

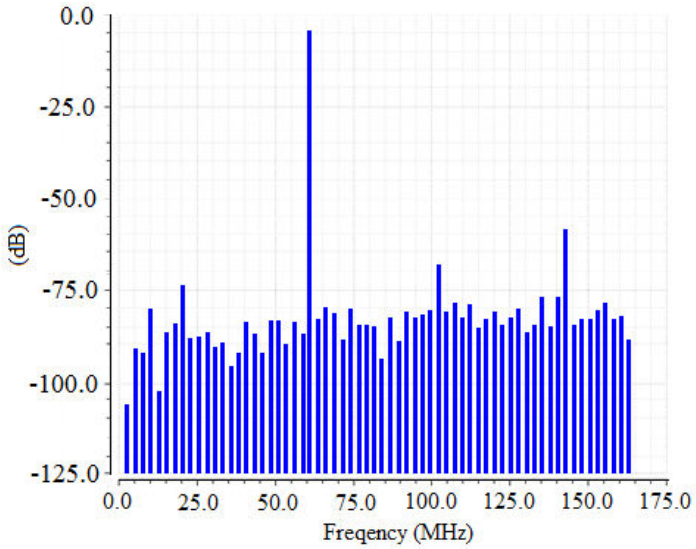



**Figure 35. The FFT of the output of the ADC.**

Top level simulations were run for the 12-bit ADC. The results are shown in Table 13. Table 14 reports the performance of the ADC at the corners and Figure 36 shows the layout of the whole ADC.

**Table 13. Top-level Simulation Results**

| | | | | | |
|---|---|---|---|---|---|
| Simulation Corner | Typical<br>27 C<br>Nominal Supplies | | Power Consumption mW (excluding input buffer, voltage references and bandgap circuit) | 12 bit Pipeline | 121.8 |
| | | | | Clock Generation Circuit | 142.3 |
| Fin | 61 MHz | | | SHA | 38 |
| Clock | 162 MHz | | | Total | 423.9 |
| SFDR | 68.4 dB | | | | |
| SNDR | 65.1 dB | | | | |
| ENOB | 10.52 Bits | | | | |

**Table 14. Performance of the ADC in some corners**

| Corner | tt | tt | tt | ff | ff | ss |
|---|---|---|---|---|---|---|
| T © | 27 | 85 | -45 | 85 | 85 | -45 |
| SNDR | 65.1 | 58.65 | 48.68 | 65.03 | 63.04 | 52.28 |
| ENOB | 10.52 | 9.45 | 7.79 | 10.51 | 10.18 | 8.39 |

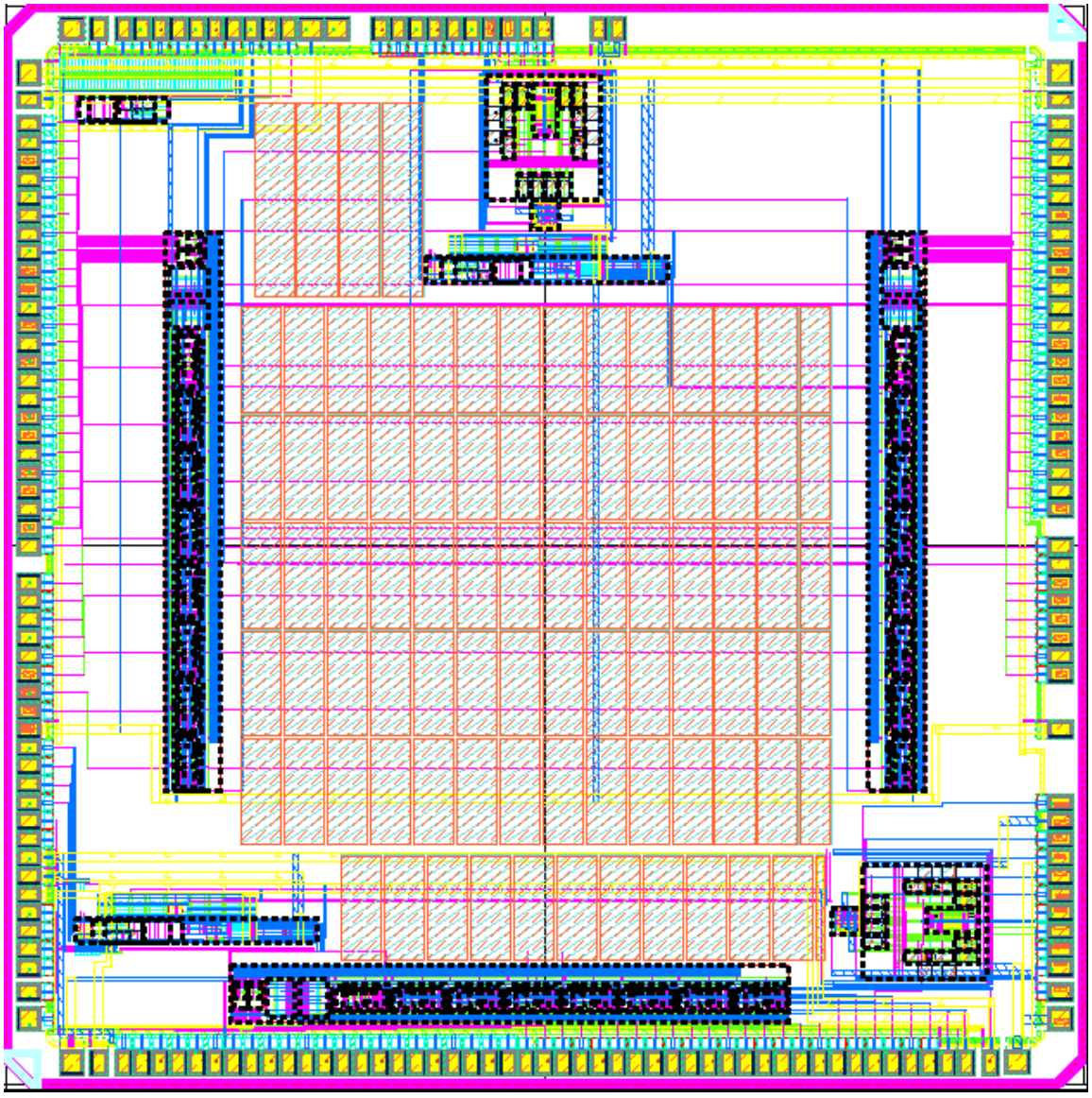


**Figure 36. The Layout of the ADC**

# 3 CALIBRATION OF ERRORS IN TIME-INTERLEAVED ADCS

## 3.1 Introduction

Pipeline ADCs are very popular for high-speed and low–power applications. However, the accuracy of the analog circuit limits the accuracy of the whole ADC. This issue becomes more challenging as we move into deep submicron technologies. Analog techniques (26) add circuit complexity and analog hardware and may require additional clock phases, which can limit the conversion speed (27). Using digital calibration relaxes the design requirements of analog circuits and reduces power consumption.

In this section, some basic concepts about non-idealities of pipeline ADCs are presented. After that calibration for channel mismatch in time-interleaved ADCs are discussed. In this section, the best option to use in this design is selected and models are developed and demonstrated. Finally, simulation results are presented and the validity of the techniques are verified.

Apart from the quantization noise which limits the performance of the ADC, there are different specific types of errors in pipeline ADCs. These can be divided into two categories:

- Non-deterministic errors
- Deterministic errors

Non-deterministic errors are those caused by noise and clock jitter. Deterministic errors are: offset error, gain error, non-linear errors, mismatch in DACs and memory effects.

## 3.2 Calibration for Channel Mismatch in Time-Interleaved Adcs

Time-interleaving has widely been used to increase the maximum sample-rate (28), (29), (30), (31), (32), (33), and (34). In this section calibration for mismatch in time-interleaved ADCs is presented which covers gain, offset, and sample-time calibration(35).

### 3.2.1 Offset Calibration

Figure 37 shows the block diagram of the chopper-based offset cancellation system. First, we assume all the offsets of the SHA and ADC are modeled with an additive voltage of $V_{OS}$ at the input. The concept is to multiply the input with a pseudo-random binary random signal C[m] = ±1. C[m] is white with zero mean and is uncorrelated with the input. At the output, a variable offset V[m] is subtracted from the output signal S[m]. The result is multiplied by $\mu_0$ which is a parameter to control the convergence rate and then is input to an accumulator which generates the offset voltage V[m]. Finally, the output is again multiplied by the same signal C[m]. Since $V_i(t)$ and C[m] are uncorrelated with each other, the result will only contain $V_i(t)$ as $C^2[m] = 1$.

Since the analog input signal has been converted to a white signal by the random chopper at the input, the chopped input has little dc information. Therefore, the dc component at the input of the accumulator is mainly due to the difference of the offset of

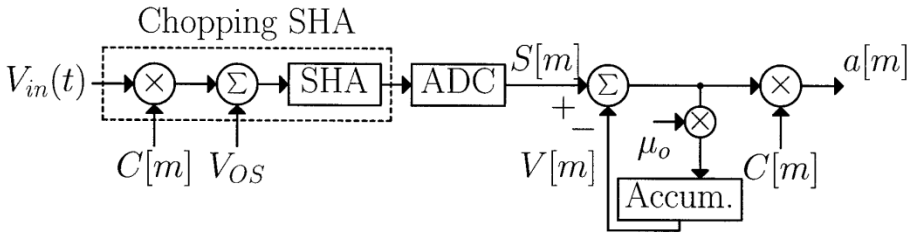



**Figure 37. Block diagram of the chopper-based offset-calibration scheme [14].**

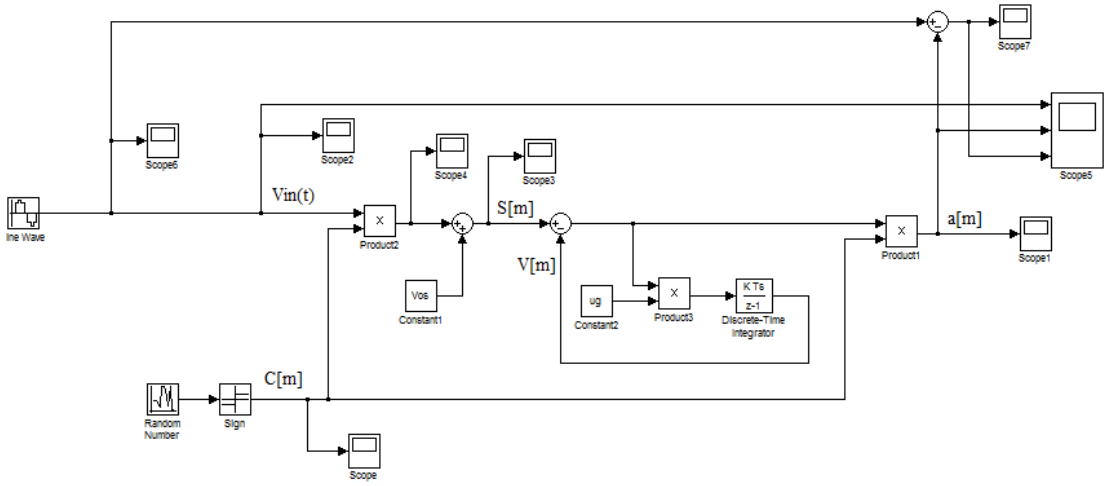



**Figure 38. Simulink model for offset calibration.**

the SHA and ADC and the output of the accumulator. In the steady state, the feedback forces the input of the accumulator to be zero. Therefore, the offset of the SHA and ADC is cancelled by the inserted offset voltage V[m]. This technique could be done for each channel to cancel the offset of that channel.

Figure 38 shows the Simulink model developed for offset calibration. The SHA and ADC has been replaced by a transfer function of one which represents ideal conversion. Other blocks are as described before.

Figure 39 shows the offset of the output of the offset calibration system for fi=10 MHz and offset of 100 mV added as the total offset of the SHA and the ADC. As this figure shows, the output offset is decreased to around 1 mV.

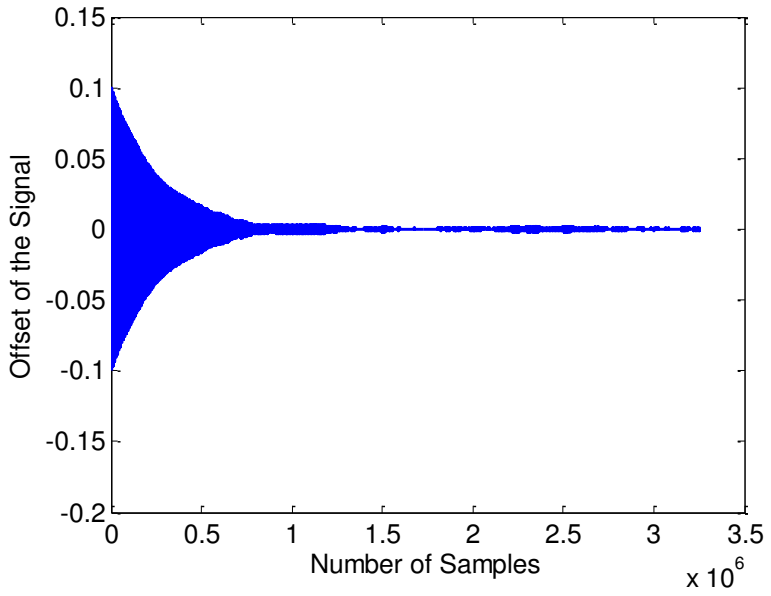



**Figure 39. Offset of the output of the offset calibration system**

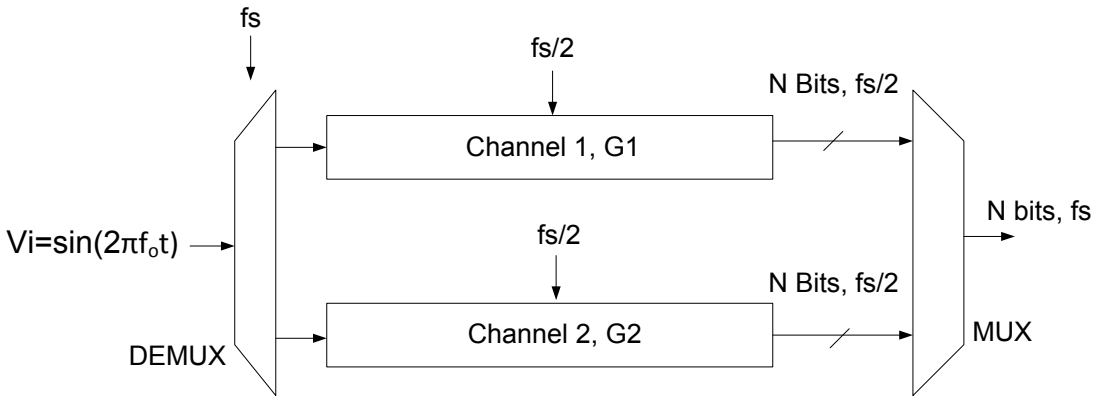
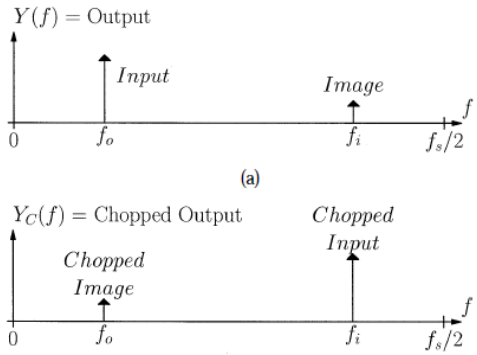



**Figure 40. A two-channel time-interleaved ADC**

### 3.2.2 Gain Calibration

Figure 40 shows a two-channel time-interleaved ADC with a sine input with frequency of $f_o$ and sampling frequency of $f_s$ and gain mismatch between channel. This mismatch causes an amplitude modulation and an image appears at the frequency of $f_i = f_s/2 - f_o$ which has an amplitude proportional to the gain mismatch $\Delta G = G_1 - G_2$, where




(b)

**Figure 41. ADC output spectrum for two time-interleaved channels with (a) a sinusoidal input at fi and gain mismatch between the channels and (b) spectrum of chopped output(35)**

$G_1$ is the gain of the top ADC channel and $G_2$ is the gain of the bottom ADC channel (36). Figure 41 (a) shows the signal and its image at the mentioned frequencies.

The proposed technique uses the proportion of the image to the gain mismatch and compensates for the gain mismatch. The procedure is to first generate the chopped version of the signal which is also shown in Figure 41. Then the signal and the chopped version are multiplied together. The output of this multiplication has a DC component

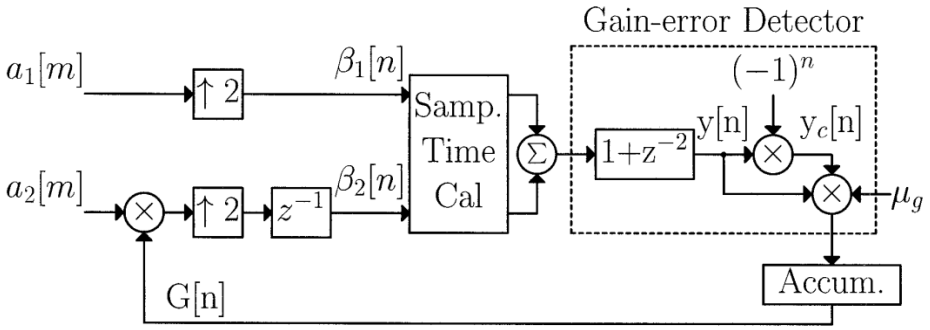



**Figure 42. Block diagram of the gain-calibration scheme (35)**

which is proportional to the gain mismatch. Figure 42 shows a system block diagram that performs this function.

Signals $a_1$ and $a_2$ are the outputs of each channel. To combine them together, they are up-sampled by a factor of 2 and one delay is added to one of the channels, which is the second channel in this case. This delay is added so that the zeros inserted into each signal do not overlap. After that sample-time calibration is done and then the two signals are added together. The result is given to a filter which is described in the sample-time

calibration section. The output of the filter is multiplied by $(-1)^n$ to generate the chopped version of the signal. The result is multiplied by $\mu_g$ which controls the convergence of the loop. Finally, the output which has a DC value proportional to the gain mismatch is input to an accumulator. The output of the accumulator is fed back and multiplied with one of the signals, here the second channel. The final value of the output of the accumulator, G[n], is G1/G2. It should be mentioned that in this technique no calibration signal is used. The signal itself is used for calibration.

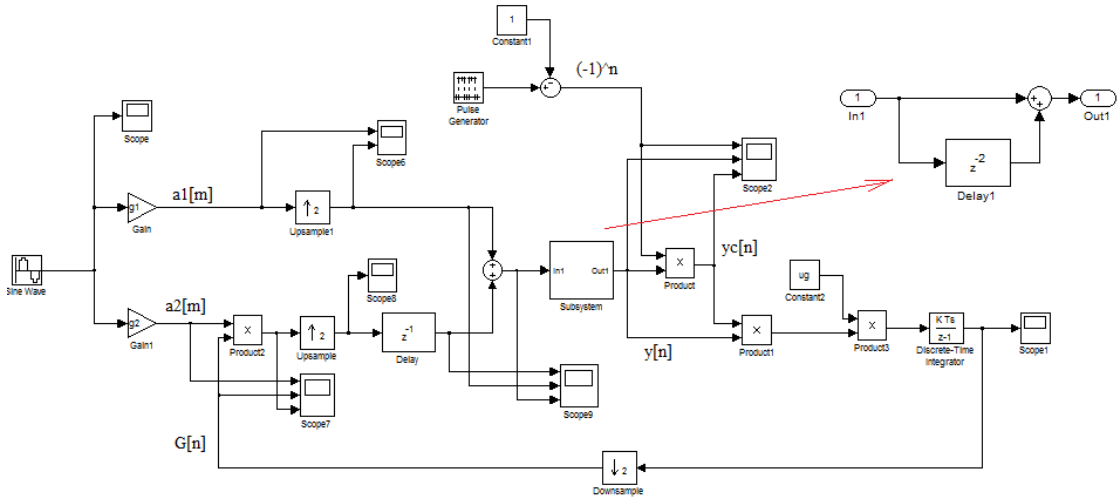



**Figure 43. Simulink model for the gain calibration**

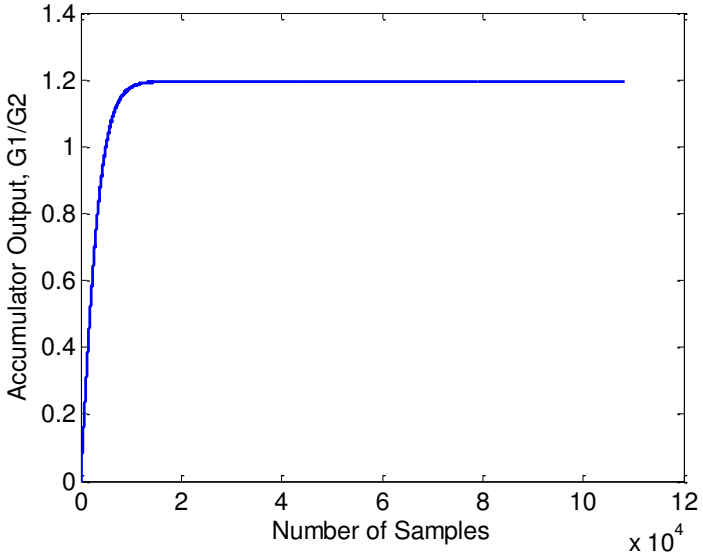



**Figure 44. The output of the gain calibration block**

Figure 43 shows the block diagram of the gain calibration which is developed in Matlab Simulink to investigate the performance of the technique. A sine input of 30 MHz was applied to the input. The gains of the channels are g1=0.92 and g2=0.77. Figure 44 shows the output of the gain calibration system. The output has settled to g1/g2=1.1948. In this run ug=$2^{-10}$.

### 3.2.3 Sample-time Calibration

Figure 45 shows the block diagram of the sample-time calibration system. The inputs $\beta_1$ and $\beta_2$ are the outputs of the gain calibration system.

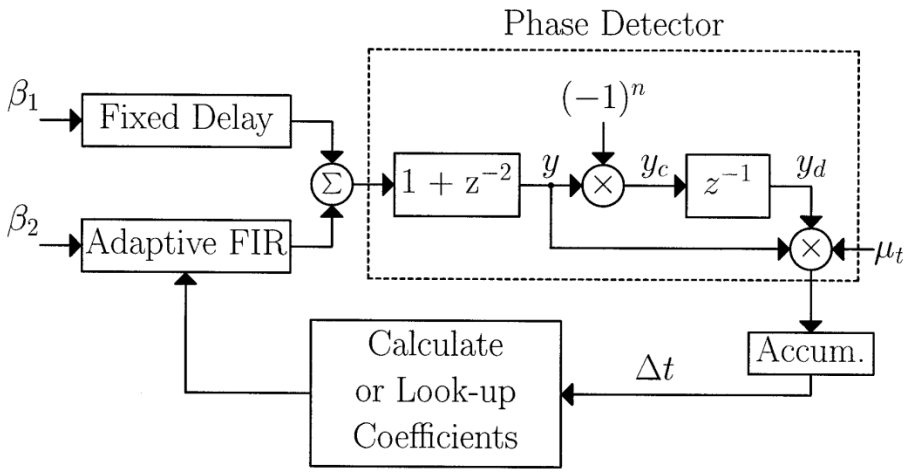



**Figure 45. Block diagram of the adaptive sample-time calibration scheme (35).**

An essential feature of the sample-time calibration presented here is the use of an adaptive filter to compensate for the sample-time mismatch between the channels. To explain the ideal, let us assume the input is a sine wave with frequency $f_o$. If the second channel samples the input $T+\Delta t$ seconds after the first channel (instead of T seconds), a sample-time error occurs. To compensate for this error, the adaptive FIR filter introduces a fractional-delay in the second channel. In other words, the transfer function of the filter is $H(z) = z^{-\Delta t/T}$. However, since this filter also introduces a fixed delay in the second channel, and in order to keep the delays of the channels the same, a fixed delay is also inserted in the first channel.

To implement the adaptive FIR filter, a look-up table is developed which generates the coefficients of the FIR filter. The goal is to implement a filter with an impulse response of

$$h[n] = -\frac{\sin\left(\pi\left(n - \frac{\Delta t}{T}\right)\right)}{\pi\left(n - \frac{\Delta t}{T}\right)} \quad (9),$$

where $T$ is the sampling period and $\Delta t$ is the sample-time error. However, since we need a casual filter we have to implement this impulse response with a delay. Therefore, the impulse response will be

$$h[n] = -\frac{\sin\left(\pi\left(n - n_0 - \frac{\Delta t}{T}\right)\right)}{\pi\left(n - n_0 - \frac{\Delta t}{T}\right)} \quad (10).$$

The Z transform of this function is

$$H(Z) = \sum_{n=0}^{\infty} h[n] z^{-n} \quad (11).$$

Also, as we cannot have an infinite number of taps for the filter, we have to choose a limited number of taps. Here with the required resolution, 20 taps will be adequate. Therefore, the coefficients which are generated by the look-up table will be h[0] to h[20]. Now each coefficient h[n] needs to be adaptive. Therefore, the look-up table consists of 20 blocks and each of these blocks accepts $\Delta t$ as input and gives h[n] at the output. Figure 46 shows the schematics of a look-up table with a 10-tap filter.

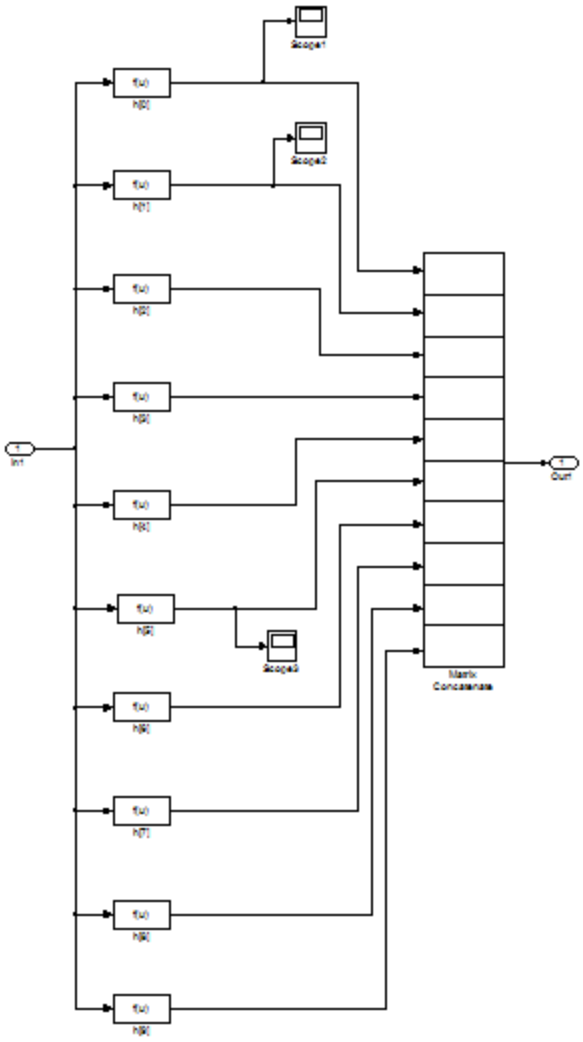



**Figure 46. Look up table with 10-tap filter.**

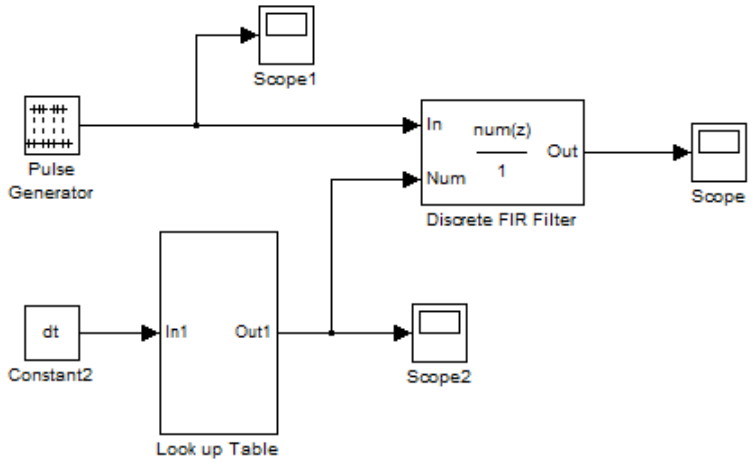



**Figure 47. Test bench to test an example FIR filter.**

The outputs of all the blocks are concatenated to produce an array of coefficients which is passed to the FIR filter block. Figure 47 shows the test bench to plot the transfer function of the adaptive FIR filter.

An impulse is given to the input of the filter and the output is plotted for two different cases. First, the value of $\Delta t$ is set to zero (the actual value of $\Delta t$ cannot be exactly zero since this function is discontinuous at 0 and a value very close to zero was given instead). In this case $\Delta t$ of zero represents ideal sampling. Therefore, the filter is a fixed delay. The impulse response of the filter in this part is shown in Figure 48.

In the second test, the value of $\Delta t$ is set to 0.6T. As Figure 49 shows, the coefficients are not zero anymore and the filter introduces a non-fractional delay in the time domain. After verifying the performance of the adaptive filter, the whole sample-time calibration system is implemented with the filter. Figure 50 shows the block diagram of this system.

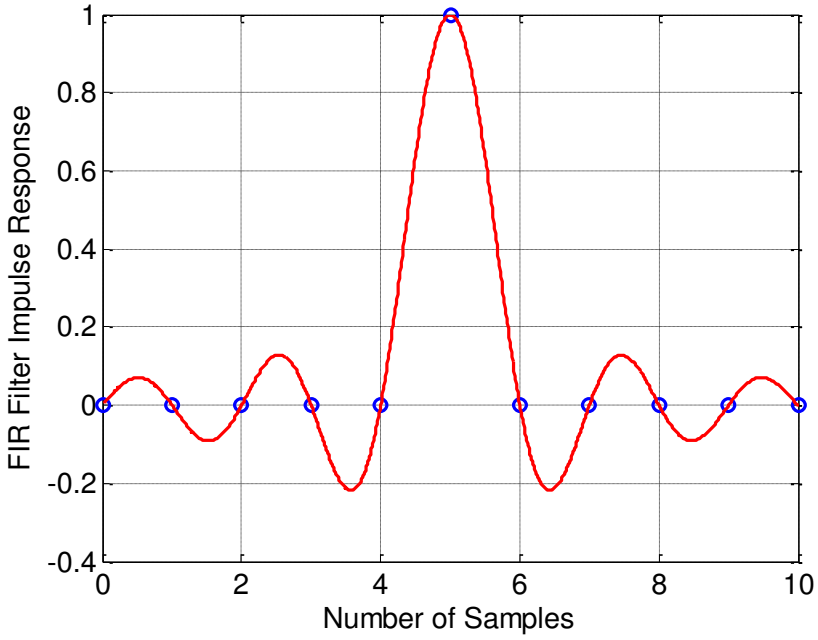



**Figure 48. The impulse response of the example FIR filter Δt = 0.**

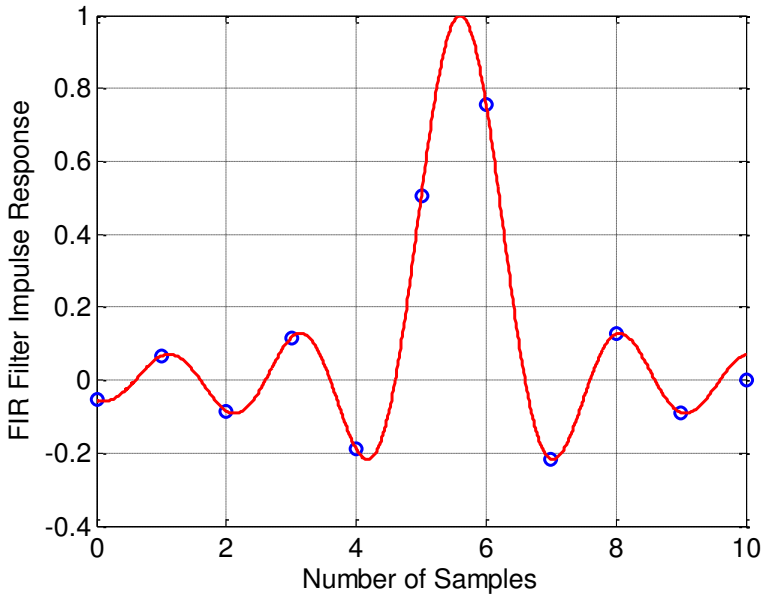



**Figure 49. The impulse response of the example FIR filter Δt = 0.6T.**

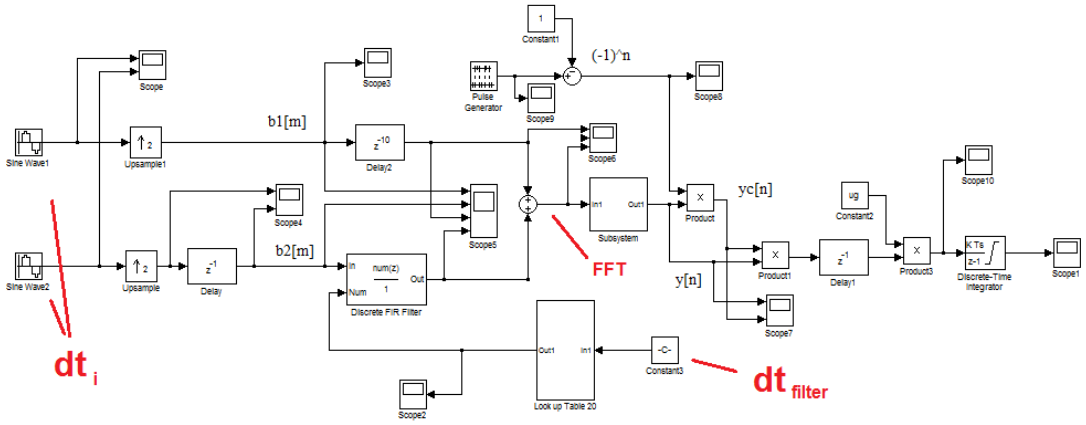



**Figure 50. Sample-time calibration. The loop is broken and the input of the filter ($dt_{filter}$) is set to zero.**

In order to investigate the effectiveness of the system two tests are run. The inputs of the channels are the same sine waves with a phase mismatch which represents the sample-time error.

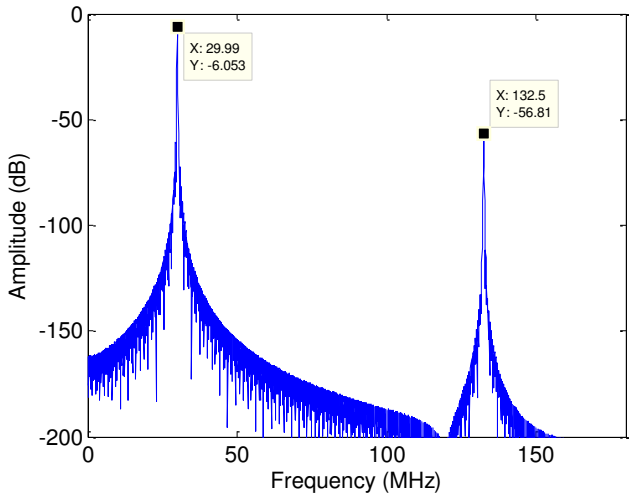



**Figure 51. FFT of the signal after summation for$dt_i$ = 0.01T (≈ 30 ps) and $dt_{filter}$ = 0 (no filtering). The spur is at 132.5 MHz and its amplitude is around -56 dB.**

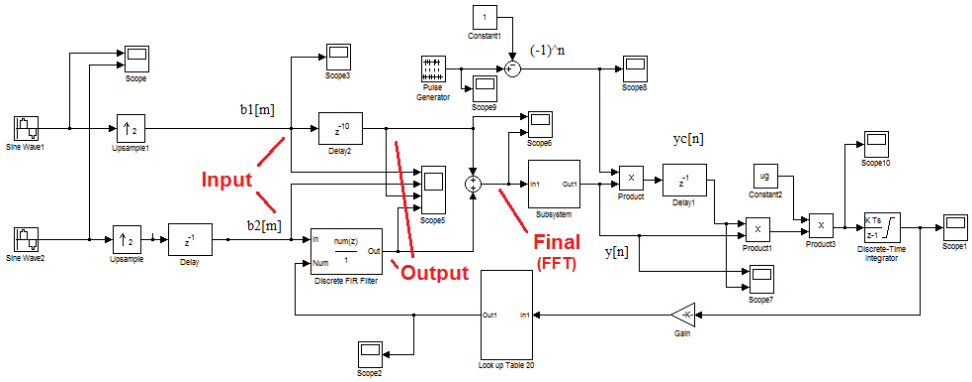



**Figure 52. Sample-time calibration. The loop is closed for the filter to compensate for the phase mismatch between the two channels.**

In the first test, the loop is broken and a zero value for $\Delta t$ in the look-up table is fixed. Therefore, the sample-time error is seen at the output of the summation node in Figure 50. Figure 51 shows the FFT plot of the output of the summation node. As this figure shows, the sample-time error of the two channels results in a spur of -56 dB at 132.5 MHz.

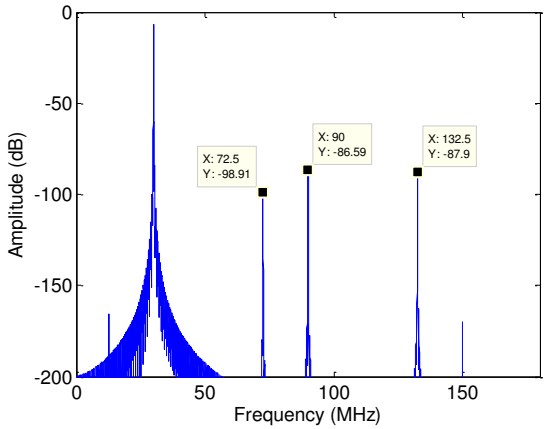



**Figure 53. FFT of the final signal (after summation node) with the filter in the loop. The spur has been decreased to -87.9 dB.**

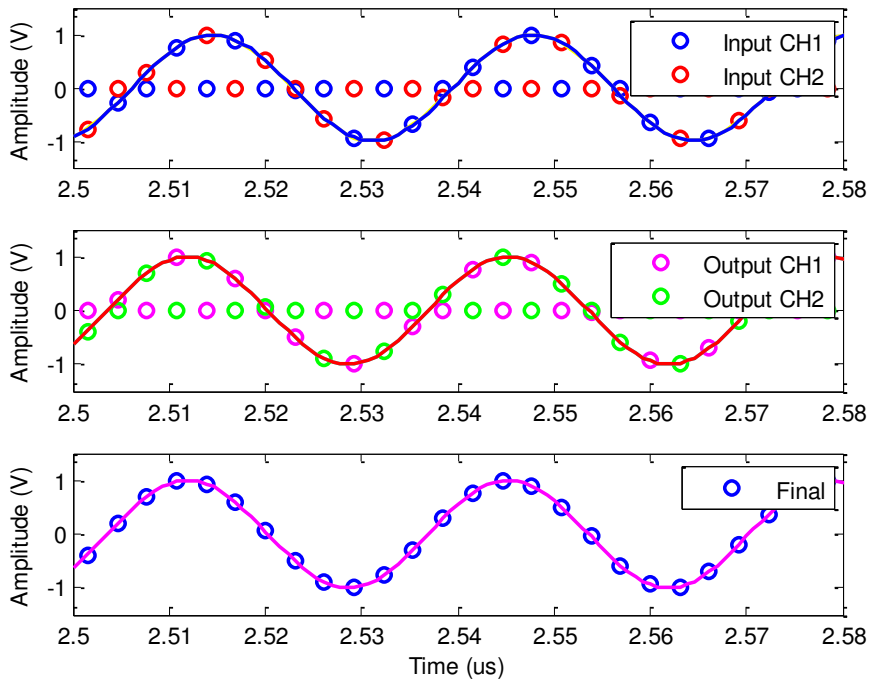



**Figure 54. The time-domain waveforms of different parts of the sample-time calibration system. The first figure shows the signals of each channel before the filter and delay. The second figure shows the signals after the filter and the delay. Finally, the last figure shows the final signal after adding the two channels.**

In the second test, the loop is closed and the system is run and the output of the summation node is plotted. Figure 52 shows the block diagram of the system in the second test. Figure 54 shows the inputs and output of the channels and the output of the summation block as shown in Figure 52. Figure 53 shows the FFT of the output of the summation block. As this figure shows, the spur at 132.5 MHz has been decreased to -87 dB. Another spur appears at 90 MHz but still the amplitude is so low that it is not major issue.

# 4 PROPOSED CALIBRATION SCHEME

## 4.1 Overview

As discussed earlier, time-interleaving increases the effective data conversion rate in analog-to-digital converters while keeping the circuit requirements the same for a desired speed. While benefiting recent designs by decreasing circuit complexities, this technique needs special considerations as other design issues associated with using parallel identical channels emerge. The first and the most important consideration is the practical issue of timing mismatch between channels, also called sample-time error, which can directly affect the performance of the ADC. Many techniques have been developed to tackle this issue both in the analog and digital domains (37), (38), and (39). Most of these techniques have high complexities especially when the number of channels exceeds 2 and some of them are only valid when input signal is a single tone sinusoidal. This would limit the application for which these techniques can be used. The proposed technique in this thesis bests the previous techniques in terms of simplicity, and also could be used with arbitrary input signals, which improves the merit of the design.

Sample-time calibration of TIADCs consists of error detection and correction. Error correction is more straightforward and can be done in analog, using a Variable Delay Line (VDL), or in the digital domain, using an adaptive FIR filter. The detection part is more elaborate and is best done in digital domain. The proposed technique focuses on the detection part of sample-time error minimization.

## 4.2 Proposed Calibration Technique

Each channel in an ADC has different non-idealities. The main nonidealities are offset, gain, and sample-time error. If we approximate the sample-time error with $\Delta V_1 = \frac{dV_{i,1}}{dt} t_1$, we have

$$V'_{O,1} \approx G_1 V_{i,1} + \frac{dV_{i,1}}{dt} t_1 + V_{off,1}. \qquad (12)$$

In equation (12), $G_1$ is the gain error, $t_1$is the sample-time error, and $V_{off,1}$ is the offset of the first channel. The proposed technique uses an extra channel to detect the sample-time error between the extra channel and each channel of the ADC and removes the mismatch between them. Figure 55shows the scheme of the proposed technique for the extra channel and the clocks. At the end of the calibration procedure since the sample-

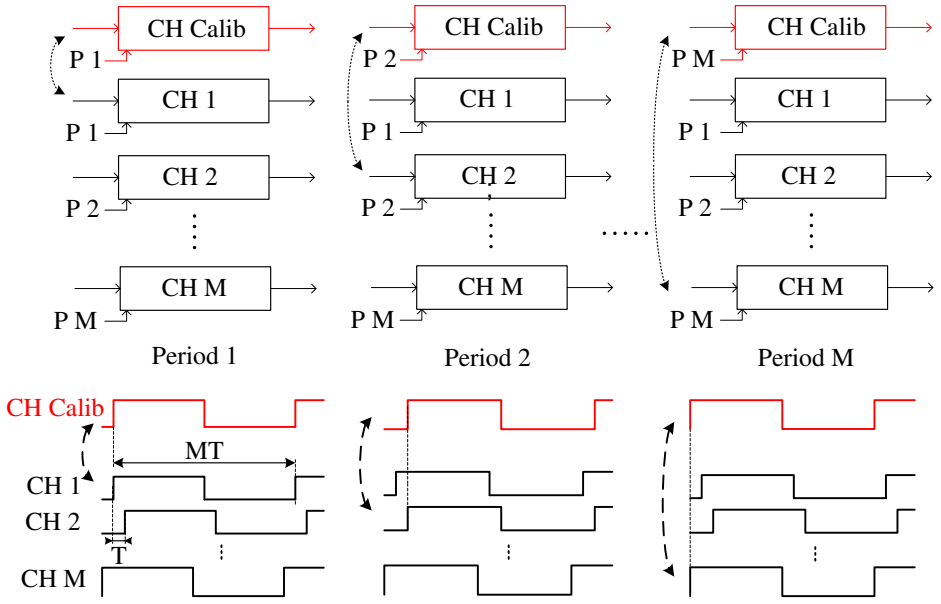



**Figure 55: The proposed technique uses an extra channel to detect the sample-time error of each individual channel in each clock period.**

time error between the extra channel and each individual channel has been removed, the mismatch between the channels will also be cancelled. It should be mentioned that the extra channel does not need to be a well-tuned channel and it could be a normal copy of the regular channels of the ADC. Also, the clock does not need to be aligned precisely since it is already included in the sample-time error and the calibration procedure will remove this error.

For a better explanation of the proposed technique, we call the extra channel the calibration channel, $CH_{Calib}$, and each ADC channel which is under calibration, $CH_{ADC,j}$ (j=1, 2, …, M). In each clock period, the calibration channel mimics the operation of the ADC channel which is under calibration. This means the two channels are using the same input and clock. If it is the case that there is only sample-time error at the output and the two channels have the same input signal and clock, we have

$$V_{O,2} - V_{O,1} = \frac{dV_i}{dt}(t_2 - t_1). \qquad (13)$$

Thus, the subtraction of the two outputs is directly proportional to the sample-time mismatch between the two channels. Since mismatch also depends on the input signal we cannot use it directly. In order to remove the effect of the input signal we take discrete integral of equation (13). The result includes the constant of the integral and yields a term which is proportional to the sample-time mismatch between the two channels

$$\sum_n \Delta V_{O,21} = \Delta t_{12} C + \Delta t_{12} \sum_n \frac{dV_i}{dt} \qquad (14)$$

Now, in order to use this as an input to the correction circuit, we need to diminish the effect of the rightmost term in equation (14), which is varying with the input. This could be done by multiplying the output of the subtraction, before integrating, with a very small

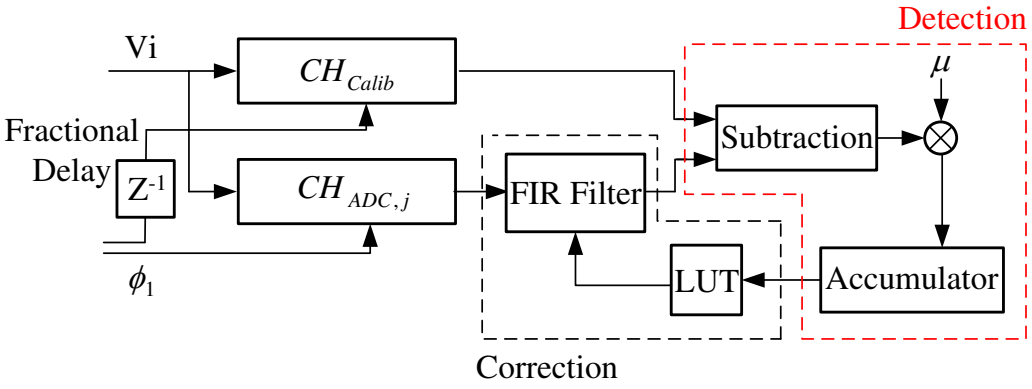



**Figure 56.Proposed sample-time calibration technique.**

value $\mu$. This is shown in Figure 56. The term which includes the input signal does not have any effect on the value to be used for the correction. Therefore, this technique could be used with arbitrary input signal. After integration the result is used as the input for the correction which is done digitally here using a look-up table and an FIR filter to shift the output of one channel, which is the channel under calibration, in the time domain(35). After specific amount of clock cycles, the output of the accumulator converges to the value which is equal to the sample-time mismatch between the two channels and hence the mismatch between the two channels is removed using the adaptive FIR filter.

The proposed technique does not use a correlation function or Hilbert transform for sample-time error detection which is a considerable advantage in simplicity over some prior techniques (38) and (40). Also, unlike some other techniques that has been

proposed previously such as the one in(35), this technique could be generalized to an arbitrary number of channels without adding extra complexity since all the channels are calibrated with one channel. For a generalized model of an M-channel TIADC, if we assume the channels have mismatch errors of $\Delta t_1, \Delta t_2, \ldots, \Delta t_M$, with the calibration channel, the same procedure could be applied to correct the errors. As mentioned before, this technique is able to correct errors for arbitrary input signals, while some of other techniques can only be used with single-tone input signals.

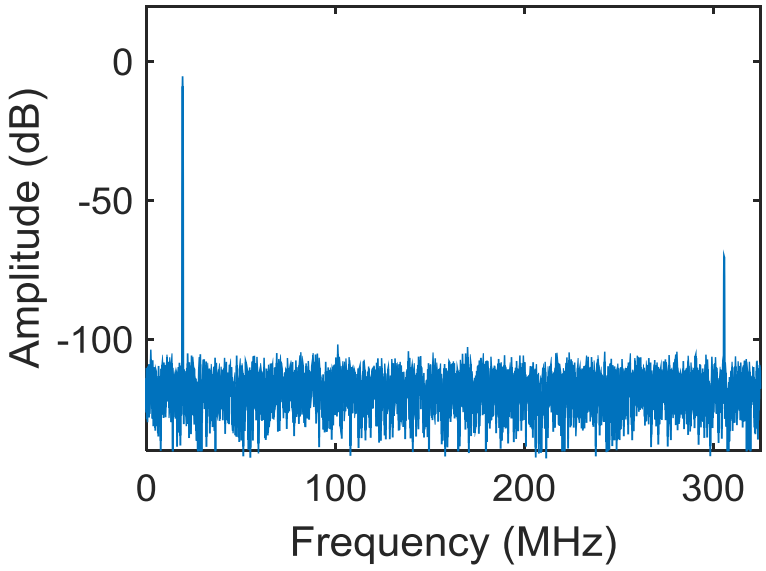



**Figure 57. The simulated output of the overall ADC before calibration.**

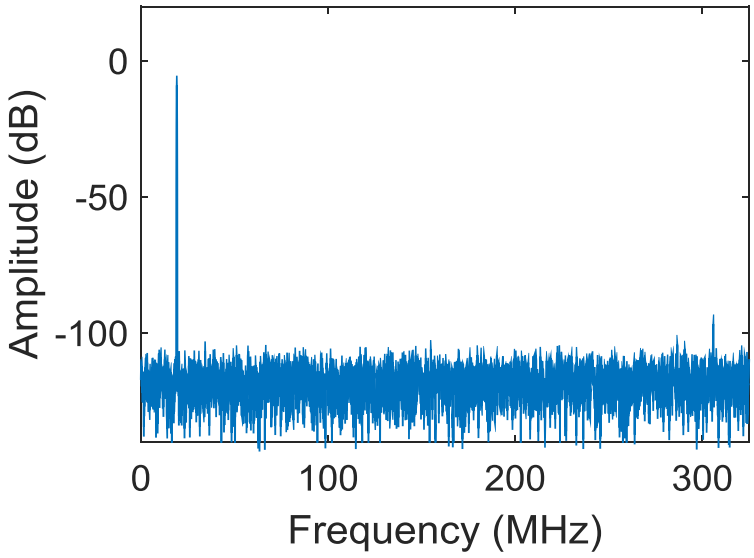



**Figure 58. The simulated output of the overall ADC after using the proposed technique.**

As we assumed here, the output of the channels has no other errors, such as offset or gain error, which is not valid in practice. Therefore, offset and gain error calibration should be done before applying this technique.

## 4.3 Simulation Results

To demonstrate the validity of the proposed technique, a two-channel 12-bit 325-MS/s ADC is designed, implementing the calibration technique. The calibration engine consists of an extra ADC channel, detection and a correction circuitry for each ADC channel. For the correction part, a similar approach as in(35) is used. An LUT which generates the coefficients of the FIR filter according to the input and an FIR filter which

shifts the output of the channel in the time domain with a fractional delay. A 20-tap FIR filter is used here. Figure 57 and Figure 58 show the simulation results.

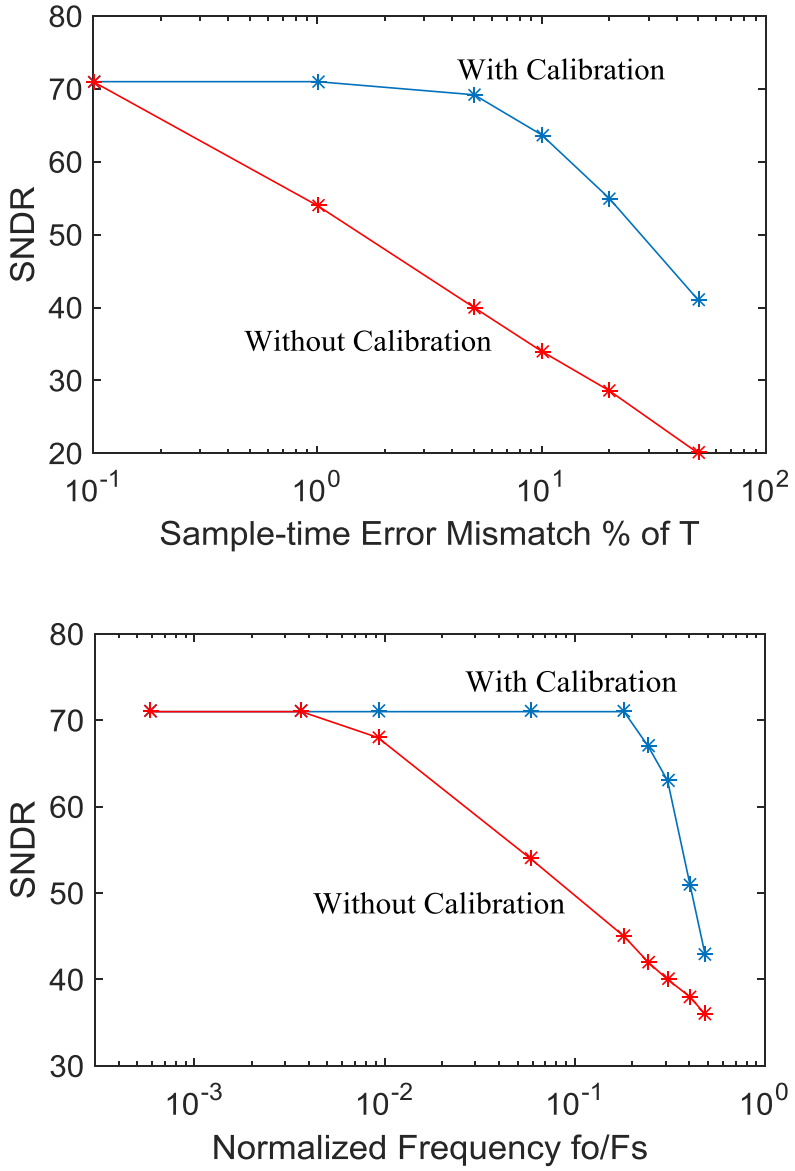



**Figure 59. Performance of the proposed technique. a) SNDR versus thesample-time error mismatch, with and without calibration.b) SNDRversus input frequency with and without calibration.**

Figure 57 shows the output spectrum before calibration and Figure 58 shows the output spectrum after calibration for $\Delta t/T = 0.01$. As these figures show, the unwanted image

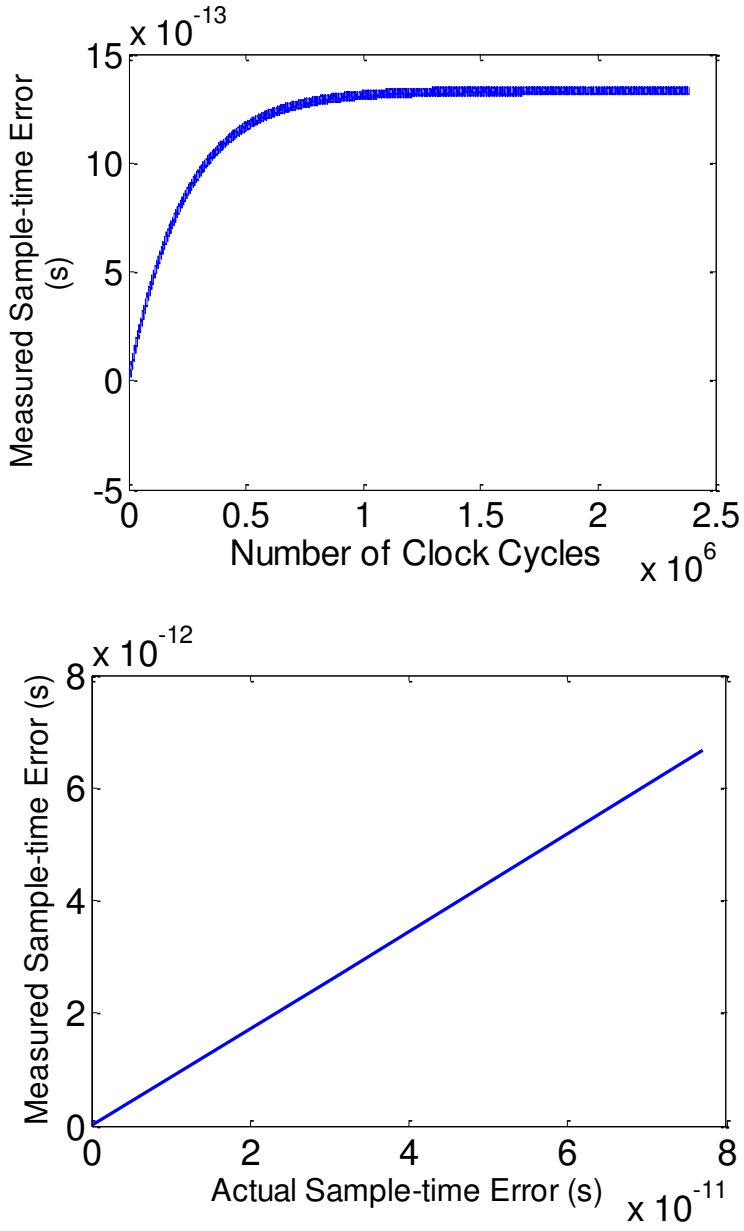



**Figure 60. a) Actual sample-time error versus measured sample-time error. b) number of clock cycles versus measured sample-time error**

due to sample-time error has been considerably suppressed from the output using the proposed technique. The SNDR has been improved from 54 dB to 73.8 dB. Figure 59 (a) shows the SNDR vs. the sample-time error mismatch as percentage of the ADC sampling period $\Delta t/T\%$, with and without the proposed calibration technique. As this figure shows, the proposed technique is able to improve the overall performance for the error mismatches up to 20% of the sampling period by 26 dB and achieve around 20 dB improvement for a mismatch of 50% of the sampling period. Since the input is a narrowband sinusoidal signal a large mismatch error is considered. For wideband signals the matching constrains are more relaxed (41). Figure 59 (b) shows the improvement of SNDR using the proposed technique for different input frequencies close to $F_S/2$. As this figure shows, the improvement is up to 29 dB at 37% of the Nyquist frequency. Figure 60 (a) shows actual sample-time error versus measured sample-time error, and Figure 60 (b) shows the number of clock cycles versus measured sample-time error. It should be mentioned that in order to save the overall power consumption of the ADC, the calibration channel could be turned off after the calibration procedure has been done.

Table 15 reports a comparison between this work and top two recent designs with best specifications. As this table reports, this work stands in the second place in terms of figure of merit. However, the results of this work is based on simulations and if fabricated, we expect degradation of SNDR while the other two references report measurement results.

**Table 15. Comparison of this work and top two references with best specifications.**

| Reference | Year | Resolution | Sample Rate | SNDR | Power | Process | FOM (fJ/con) |
|---|---|---|---|---|---|---|---|
| This Work | 2017 | 12 bit | 650 MS/s | 70.8 dB | 335 mW | 0.13 um BiCMOS | 192 |
| (13) | 2011 | 12 bit | 3 GS/s | 59 dB | 500 mW | 40 nm CMOS | 229 |
| (14) | 2014 | 12 bit | 1.6 Gs/s | 58 dB | 1.15 mW | 0.18 um BiCMOS | 1.1 |

# 5 CONCLUSION AND FUTURE WORK

This research involved using novel analog and digital techniques to enhance performance of analog-to-digital converters. A 12-bit 650Msps ADC was designed to showcase the proposed techniques. Double-sampling, pre-charging, and time-interleaving were among the analog techniques that used to improve the performance of ADC combined with optimization of design variables. In addition to these analog methods, digital signal processing techniques were used to compensate for the remaining analog imperfections. A sample-time error calibration technique has been proposed which uses an extra channel to detect the sample-time mismatch between the channels. The proposed technique decreases the complexity of the calibration system and could be used with arbitrary input signals. Simulation results of a 12-Bit TIADC show that the proposed technique is able to improve the SNDR by 20 dB for a mismatch of 50% of the sampling period and up to 29 dB at 37% of the Nyquist frequency.

As CMOS technology evolves quickly, analog designers encounter more and more challenges designing high performance circuits. As new technologies more benefit digital designs, a good combination of digital and analog techniques to improve performance of circuits are the optimum solution. The proposed technique in this work corrects the errors due to sample-time mismatch between the channels and uses other techniques to correct offset and gain mismatch between channels. However, for future

work the proposed technique could be generalized for the correction of offset and gain mismatch errors.

## REFERENCES


1. *A 10-Bit 500-MS/s 55-mW CMOS ADC.* A. Verma and B. Razavi. 11, 2009, IEEE J. Solid-State Circuits, Vol. 49, pp. 3039-3050.

2. *A 12 bit 200 MS/s zero-crossing-based pipelined ADC with early sub-ADC decision and output residue background calibration.* S. Shin, J. C. Rudell, et al. 6, 2014, IEEE Journal of Solid-State Circuits, Vol. 49, pp. 1366-1382.

3. *An 11b 800MS/s time-interleaved ADC with digital background calibration.* C. Hsu, et al. 2007. IEEE ISSCC. pp. 464-465.

4. *A 16-bit 250-MS/s IF sampling pipelined ADC with background calibration.* A. Ali, et al. 12, 2010, IEEE Journal of Solid-State Circuits, Vol. 45, pp. 2602-2612.

5. *A 12 bit 160 MS/s two-step SAR ADC with background bit-weight calibration using a time-domain proximity detector.* Y. Zhou, et al. 4, s.l. : IEEE Journal of Solid-State Circuits, 2015, Vol. 50, pp. 920-931.

6. *A 1-GS/s 11-bit ADC With 55-dB SNDR, 250-mW Power Realized by a High Bandwidth Scalable Time-Interleaved Architecture.* S. Gupta et al. 12, 2006, IEEE J. Solid-State Circuits, Vol. 41, pp. 2650-2657.

7. *An 85 mW 14-bit 150MS/s pipelined ADC with a merged first and second MDAC.* L. Weitao, et al. 5, s.l. : Communications,, 2015, Vol. 12, pp. 14-21.

8. *A 16-Bit 100 to 160 MS/s SiGe BiCMOS Pipelined ADC With 100 dBFS SFDR.* R. Payne et al. 12, 2010, IEEE J. Solid-State Circuits, Vol. 45, pp. 2613-2622.

9. *A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS Pipeline ADC.* S. Devarajan et al. 12, 2009., IEEE J. Solid-State Circuits, Vol. 44, pp. 3305–3313.

10. *A 14-b 100-MS/s Pipelined ADC With a Merged SHA and First MDAC.* B. Lee et al. 12, 2008, IEEE J. Solid-State Circuits, Vol. 43, pp. 2613–2619.

11. *A 1.35 GS/s, 10 b, 175 mW Time-Interleaved AD Converter in 0.13 μm CMOS.* S. Louwsma et al. 4, 2008, IEEE J. Solid-State Circuits, Vol. 43, pp. 778–786.

12. *A 1.8V 1.0GS/s 10b Self-Calibrating Unified-Folding-Interpolation ADC with 9.1 ENOB at Nyquist Frequency.* R. Taft et al. 2009. IEEE ISSCC. pp. 78-79.

13. *A 12b 3GS/s Pipeline ADC with 500 mW and 0.4 mm2 in 40 nm Digital CMOS.* C.-Y. Chen, and J. Wu. s.l. : Symposium on VLSI Circuits, 2001. pp. 120-121.

14. *12 Bit 1.6 GS/s BiCMOS 2 * 2 hierarchical time-interleaved pipeline ADC.* M. El-Chammas, et al. 9, s.l. : IEEE Journal of Solid-State Circuits, 2014, Vol. 49, pp. 1876-1885.

15. *A 14-bit 125 MS/s IF/RF Sampling Pipelined ADC With 100 dB SFDR and 50 fs Jitter.* A. Ali et al. 8, 2006, IEEE J. Solid-State Circuits, Vol. 41, pp. 1846-1855.

16. *An 800MS/s Dual-Residue Pipeline ADC in 40nm CMOS.* J. Mulder et al. 2011. IEEE ISSCC. pp. 184-185.

17. *A 10b 100MS/s 4.5mW Pipelined ADC with a Time Sharing Technique.* Y. Huang and T. Lee. 2010. IEEE ISSCC. pp. 300-301.

18. *Considerations for High-Frequency Switched-Capacitor Ladder Filters.* T. C. Choi and R. W. Brodersen. 1980, IEEE Trans. Circuits and Systems, Vols. cas-27, pp. 545–552.

19. *8b 75MSample/s 70mW parallel pipelined ADC incorporating double sampling.* Bright, W. s.l. : ISSCC Dig Tech Papers, 1998. pp. 146-147.

20. *Low-Voltage Double-Sampled DS Converters.* D. Senderowicz et al. 1997, IEEE J. Solid-State Circuits, Vol. 32, pp. 1907–1909.

21. Waltari, M.*CIRCUIT TECHNIQUES FOR LOW-VOLTAGE AND HIGH-SPEED A/D CONVERTERS.* Helsinki : Helsinki University of Technology, 2002. PHD Dissertation.

22. Maloberti, F.*Data Converters.* The Netherlands : Springer, 2007.

23. Analog Devices.*The Data Conversion Handbook.* Newnes, USA : s.n., 2005.

24. *Thermal noise analysis of multi-bit SC gain-stages for low-voltage high-resolution pipeline ADC design.* M. Azizi, et al. 2003. International Symposium on Signals, Circuits and Systems.

25. *A CMOS 15-Bit 125-MS/s Time-Interleaved ADC with Digital Background Calibration.* Z. Lee, et al. 2006. IEEE Custom Intergrated Circuits Conference. pp. 209-212.

26. *A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3-um CMOS.* Y.-M. Lin et al. 4, 1991, IEEE J. Solid-State Circuits, Vol. 26, pp. 628–636.

27. *Background Interstage Gain Calibration Technique for Pipelined ADCs.* J. Kean et al. 1, 2005, IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 52.

28. *Time interleaved converter arrays.* W. C. Black et al. 6, 1980, IEEE J. Solid-State Circuits, Vols. SC-15, pp. 1022–1029.

29. *A 1-GHz 6-bit ADC system.* K. Poulton et al. 6, 1987, IEEE J. Solid-State Circuits, Vols. SC-22, pp. 962–970.

30. *Digital spectra of nonuniformly sampled signals: Fundamentals and high-speed waveform digitizers.* Jenq, Y. C. 1988, IEEE Trans. Instrum. Meas., Vol. 37, pp. 245–251.

31. *Digital spectra of nonuniformly sampled signals: A robust sampling time offset estimation algorithm for ultra high-speedwaveform digitizers using interleaving.* Jenq, Y. C. 1990, IEEE Trans. Instrum. Meas., Vol. 39, pp. 71–75.

32. *Analysis of mismatch effects among A/D converters in a time-interleaved waveform digitizer.* A. Petraglia et al. 1991, IEEE Trans. Instrum. Meas., Vol. 40, pp. 831–835.

33. *A 10-b 50-MHz pipelined CMOS A/D converter with S/H.* M. Yotsuyanagi et al. 1993, IEEE J. Solid-State Circuits, Vol. 28, pp. 292–300.

34. *An 8-b 85-MS/s parallel pipeline A/D converter in 1-_m CMOS.* C. S. G. Conroy et al. 1993, IEEE J. Solid-State Circuits, Vol. 28, pp. 447–454.

35. *A 10-bit 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration.* S. M. Jamal et al. 12, 2002, IEEE J. Solid-State Circuits, Vol. 37, pp. 1618–1627.

36. Conroy, C. S. G.*A high-speed parallel pipelined A/D converter technique in CMOS.* Berkeley : Univ. California at Berkeley, 1994. Ph.D. dissertation.

37. *A four-channel timeinterleaved ADC with digital calibration of interchannel timing and memory errors.* C. Law, et al. 10, s.l. : IEEE Journal of Solid-State Circuits, 2010, Vol. 45, pp. 2091-2103.

38. *An 8 Bit 4 GS/s 120 mW CMOS ADC.* H. Wei, et al. 8, s.l. : IEEE Journal of Solid-State Circuits, 2010, Vol. 49, pp. 1751-1761.

39. *A background sampletime error calibration technique using random data for wide-band high-resolution time-interleaved ADCs.* A. Haftbaradaran, et al. 3, s.l. : IEEE Transactions on Circuits and Systems II, 2008, Vol. 55, pp. 234-238.

40. *Calibration of sample-time error in a two-channel time-interleaved analog-to-digital converter.* S. Jamal, et al. 1, s.l. : IEEE Transactions on Circuits and Systems I, 2004, Vol. 51, pp. 130-139.

41. *General analysis on the impact of phase-skew in time-interleaved ADCs.* M. El-Chammas, et al. 5, s.l. : IEEE Transactions on Circuits and Systems I, 2009, Vol. 56.