Soft-switching Techniques for Power Conversion System in Automotive Chargers

by

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ABSTRACT

This thesis investigates different unidirectional topologies for the on-board charger in an electric vehicle and proposes soft-switching solutions in both the AC/DC and DC/DC stage of converter with a power rating of 3.3 kW. With an overview on different charger topologies and their applicability with respect to the target specification a soft-switching technique to reduce the switching losses of a single phase boost-type PFC is proposed. This work is followed by a modification to the popular soft-switching topology, the dual active bridge (DAB) converter for application requiring unidirectional power flow. The topology named as the semi-dual active bridge (S-DAB) is obtained by replacing the fully active (four switches) bridge on the load side of a DAB by a semi-active (two switches and two diodes) bridge. The operating principles, waveforms in different intervals and expression for power transfer, which differ significantly from the basic DAB topology, are presented in detail. The zero-voltage switching (ZVS) characteristics and requirements are analyzed in detail and compared to those of DAB. A small-signal model of the new configuration is also derived. The analysis and performance of S-DAB are validated through extensive simulation and experimental results from a 1 kW hardware prototype.

Secondly a low-loss auxiliary circuit for a power factor correction (PFC) circuit to achieve zero voltage transition is also proposed to improve the efficiency and operating frequency of the converter. The high dynamic energy generated in the switching node during turn-on is diverted by providing a parallel path through an auxiliary inductor and a transistor placed across the main inductor. The paper discusses the operating principles, design and merits of the proposed scheme with hardware validation on a 3.3 kW/ 500 kHz PFC prototype. Modifications to the proposed zero voltage transition (ZVT) circuit is also investigated by implementing two topological variations. Firstly, an integrated magnetic structure is built combining the main

inductor and auxiliary inductor in a single core reducing the total footprint of the circuit board. This improvement also reduces the size of the auxiliary capacitor required in the ZVT operation. The second modification redirects the ZVT energy from the input-end to the DC link through additional half-bridge circuit and inductor. The half-bridge operating at constant 50% duty cycle simulates a switching leg of the following DC/DC stage of the converter. A hardware prototype of the above-mentioned PFC and DC/DC stage was developed and the operating principles were verified using the same.

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Chapter 1

INTRODUCTION

1.1 Battery Chargers for Electric and Plug-In Electric Vehicles

Aggressive emission reduction mandates in states, ozone depletion, mounting health problem in densely populated areas and the realization that oil dependence is an economic and political issue that increasingly threatens global security has led to unprecedented changes in the automotive industry. State and federal government initiatives have been established to focus on the development of vehicular technologies for both fully electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs) [2]. With the advent of attractive, affordable 200 mile range cars the popularity for sustainable transportation among large section of consumers is ever increasing. The global electric vehicle market for electric vehicles reached about 83.5 million U.S. dollars and is expected to grow at 19% annually [3]. Moreover, the popularity of these sustainable transportation have also increased globally with a major push seen at the chinese market [1] as shown in Fig 1.1. Some of the factors that slowdown the EV sales are high vehicle and battery cost, fluctations in oil prices, vehicle mileage between charges, charging time, infrastructure and public knowledge on environmental effects.

Despite these factors with the continuous reduction of battery prices per kWhr, Bloomberg's advanced transportation analyst have predicted EVs to be 35 % of the total global new car sales by 2040 [4]. And by the year 2022 the electric vehicles will cost the same as their internal combustion counterparts. The advances in power electronics are required to meet these increasing power demands of the electric drive

system while minimizing the system size and weight. In addition to the performance enhancement these technologies requires usability, reliability and consumer acceptance of these products.

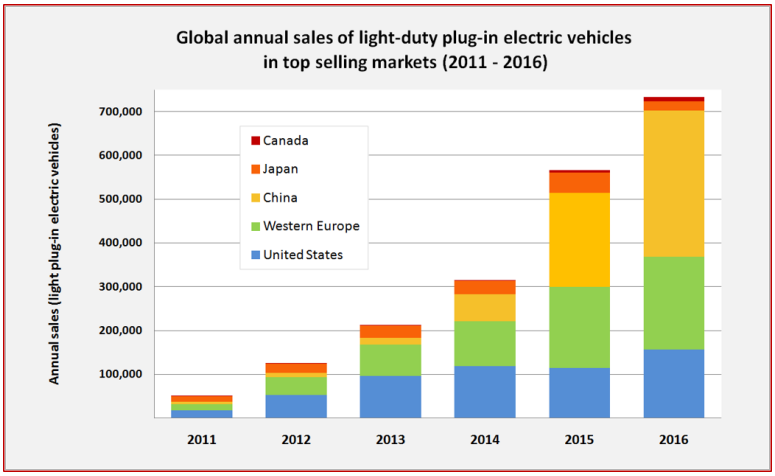


Figure 1.1: Annual sales of Electric Vehicles worldwide (2011-2017) [1]

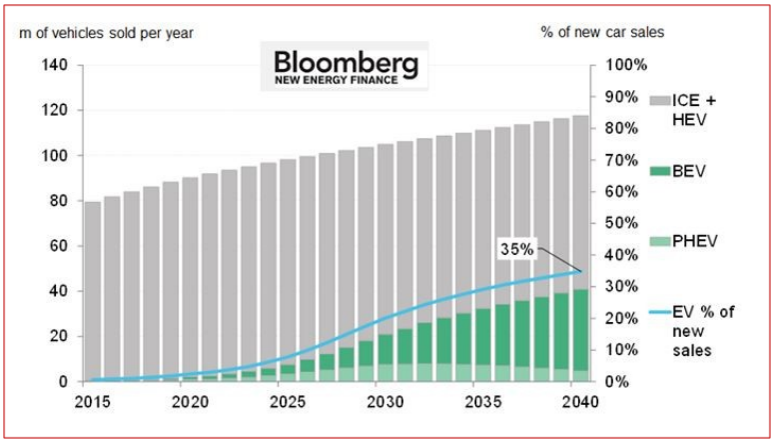


Figure 1.2: Predicted sales of Electric Vehicles worldwide

A typical power architecture of a light duty EV consists of a high voltage (300 400 V) battery back with energy capacity ranging from (20 $\sim$ 90 kWhr). Energy density and weight of the battery are two critical parameters that determine the range of the electric vehicle. Li-ion cell has much higher energy density than other battery chemistries in the market such as lead-acid, nickel cadmium and Ni-metal

hydride cells. Li-ion battery pack is still the expensive and heaviest component in the vehicles and manufacturers are constantly striving on bringing its price lower. There are three main power electronic interfaces for a) Electric motor propelling b) On-board appliances power supply c) On-board charging unit. The propulsion electronics consist of a bidirectional DC/DC converter followed by an variable speed drive for driving the induction motors. The interface for on-board appliances consists on an isolated DC/DC converter stepping the 400 V battery voltage down to 12 V for functions such as air conditioning, window systems, headlights, navigation and stereo systems etc.

The on-board charger is one such component that alleviates the customer's range anxiety by enabling the vehicle to recharge from any available power outlet, 90-240V/ $50 \sim 60$Hz. Most EV charging takes place at home overnight where the EV is plugged into an outlet for Level 1 (slow) charging. Typically a 25 kWhr battery pack takes about 17 hours to charge from 20% state of charge (SOC) to full. Battery chargers play a critical role in the development of EVs as charging times and battery life are directly linked to the performance of these units. A battery charger is required to be efficient, reliable with high power density, low volume and low cost. A compact and lightweight charger is desired to provide the high range requirements and to reduce system cost in comparison to competing IC engine designs. An EV charger must also ensure that the utility current drawn has low harmonic content to minimize power quality impact and maximize the real power drawn from the grid by having unity power factor.

1.2 Charger Power Levels and Infrastructure

Deployment and availability of charging infrastructure and power supply equipment is an important factor for many consideration such as charging time, extent,

standardization of charging units and policies. Moreover, with the availability of charging infrastructures manufacturers can reduce the on-board requirements and costs. Most EV owners plug in their vehicle to the grid during night and for this reason the Level 1 and Level 2 chargers are the primary options for customers.

Level 1 charging : In the U.S., Level 1 uses standard 120V/ 15A (12A useable) single phase grounded outlet. The connection may use a standard J1772 connector to the EV ac port. Level 1 only provides a small amount of power (maximum of 1.4 kW) and results in prolonged charge times as this was established during introduction of battery electric vehicles and were not the final charging solution. This infrastructure has an approximate installation cost of $500-$800 [5], [6] and it is generally integrated with the vehicle.

Level 2 charging : Is the primary or the preferred method for both private (garage) and public facilities and require 240V outlet [7]. This charging option can operate at up to 80A and 19.2 kW, but many such units operate at up to 30 A, delivering a maximum of 7.2 kW of power. In comparison with Level 1 this charging method saves considerable charging time with an installation cost for the residential electric vehicle supply equipment (EVSE) ranging anywhere between $1000 to $3000 [8]. These price level makes Level 2 chargers one of the dominant equipment in the EV market.

Level 3 charging : And DC fast charging are used for commercial purposes and as public filling stations [9]. It can be installed in highway rest areas and city refueling points, analogous to gas stations. It typically operated with 480 V or higher three-phase circuits and requires an off-board charger to provide AC-DC conversion. There are three types of DC fast charging systems, depending on the type of charge port on the vehicle. Level 3 chargers comes with extremely high costs, that includes the installation cost, infrastructure cost, as well as the maintenance cost [10]. These charging power levels are summarized in Table 1.1.

Table 1.1: Charging power levels

Power Level Types	Charger Location	Energy Supply Interface	Power Level	Charging Time
Level 1 120Vac(US) 230Vac(EU)	On-board 1-phase	Convenience outlet	1.4kW(12A) 1.9kW(20A)	4-11hr (5-15kWh) 11-36hr (16-50kWh)
Level 2 240Vac(US) 400Vac(EU)	On-board 1/3-phase	Dedicated EVSE	4kW(17A) 8kW(32A) 19.2kW(80A)	1-4hr (5-15kWh) 2-6hr (16-30kWh) 2-3hr (3-50kWh)
Level 3(Fast) (208-600Vac or Vdc)	Off-board 3-phase	Dedicated EVSE	50kW 100kW	0.4-1hr (20-90kWh) 0.2-0.5 hr

EV battery chargers can be classified as on-board and off-board chargers with unidirectional and bidirectional power flow. The chargers are also categorized as conductive and inductive systems. Conductive systems have direct contact between the connector and receptacle whereas, inductive charger employ magnetic coupling. At present, the unidirectional and conductive chargers are prevalent as they limit cost, weight, volume and losses in the system [11]. This work focuses on techniques for improving the performance of these unidirectional on-board chargers.

1.3 Topological Review of On-board Chargers

An EV with unidirectional charging can draw power but not inject energy into the grid. On-board charger power level varies from 3.3 kW - 19.2 kW providing 10-40 mile per hour rate of charge [12]. These chargers use a diode bridge in conjuction with a filter and DC/DC converter. These are often implemented in a single stage solution to limit the cost and weight of the unit. But high frequency isolation is a desired feature for protecting the battery pack from the grid surges. Designs with active front ends can provide local reactive power support with discharging the battery. Hence the research in unidirectional charger seek optimal charging topologies that

maximizes benefits, lowers cost and that are easy to control thereby avoiding safety concerns that are associated with bidirectional converters. Moreover, bi-directional power flow increases the battery degradation due to frequent energy cycling hence, necessary distribution system upgrades and extensive safety is required before market introduction.

Typically an on-board charger consists of two stages, a AC/DC power factor correction and a DC/DC conversion stage with galvanic isolation [13] as shown in Fig 1.3. The first stage PFC stage rectifies the AC input voltage and transfers the power to a regulated intermediate DC link capacitor that is designed to handle twice the line frequency ripple. The following DC/DC stage then converts the bus voltage into regulated output DC voltage for charging the battery.

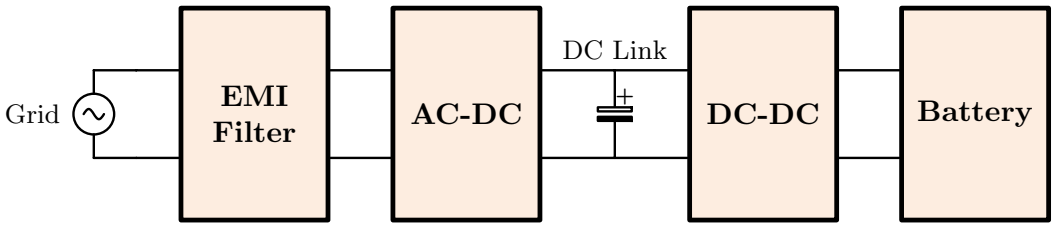


Figure 1.3: Simplified block diagram of universal two stage on-board charger

1.3.1 Front End AC/DC Converter Topologies

As a key component of a charger system, the front end converter must achieve high efficiency and power density as well as meeting the power factor requirements and regulatory standards. The densification of the charger unit can be achieved through high switching frequencies thereby reducing the size of passive components and through miniaturization of thermal system by achieving high efficiency values.

Conventional Boost PFC converter: is the most popular topology in this application. It consists of a diode bridge rectifier followed by a single switch and diode combination as shown in Fig. 1.4. With this topology, the output capacitor ripple

current is very high [14]. Futhermore, as the power level increases the diode bridge losses significantly degrade the efficiency and hence heat dissipation in a limited area is challenging. There are other topological derivation that further improves the performance of the conventional boost PFC and they are as follows

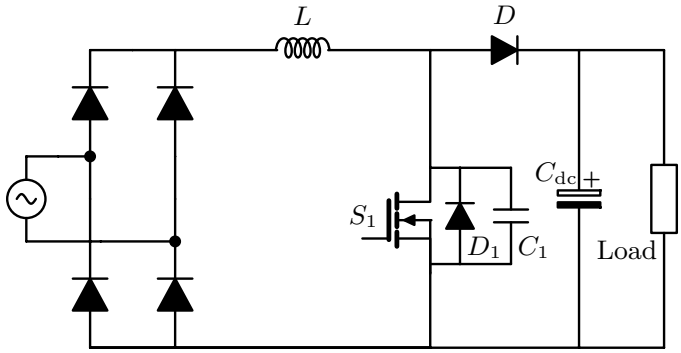


Figure 1.4: Conventional PFC boost converter

Interleaved Boost PFC Converter: As shown in Fig. 1.5 this topology consists of a diode bridge followed by two boost sections in parallel, operating at 180° out of phase [15,16]. The input current is the sum of two input inductor currents and as the inductor's ripple current are out of phase they tend to cancel each other, it reduces the ripple component. Futhermore, the effective switching frequency of the converter is doubled and thus the input EMI filter requirement is reduced [17]. Paralleling the semiconductors reduce the conduction losses at each switch but affects the overall switching losses. Finally interleaving also reduces the output capacitor high frequency ripple current.

Bridgeless Boost Converter: avoids the need for rectified input bridge maintaining the classic boost topology [18–20] as shown in Fig .1.6. It is an attractive solution for applications with high power density requirement and efficiency is paramount. This converter solves the heat management problem in the input diode bridge but introduces increased EMI [21]. The voltage sensing circuit also requires a low frequency transformer or an opto-coupler for reliable measurement. Moreover, in order to sense

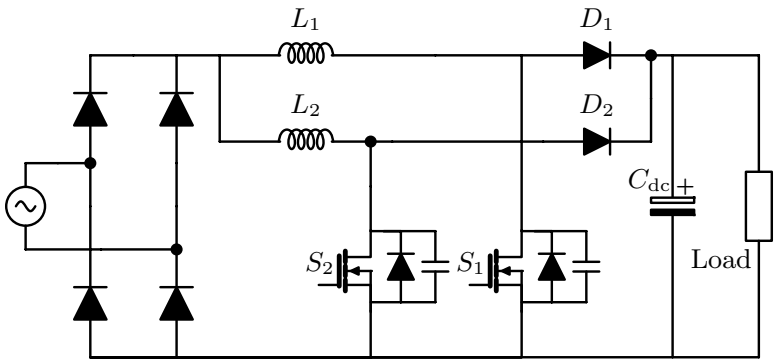


Figure 1.5: Interleaved PFC boost converter

the input current, current in the MOSFET and diode path are measured separately as they do not share a common ground. In order to address these issues a phase shifted semi-bridgeless boost converter was introduced [22, 23].

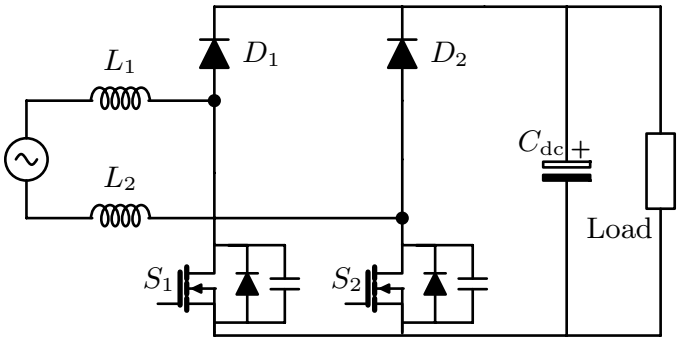


Figure 1.6: Bridgeless/Dual boost PFC converter

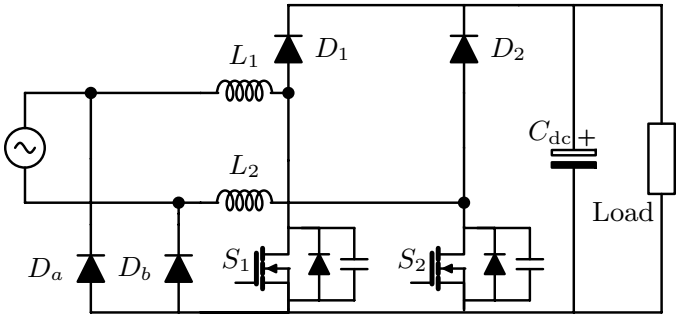


Figure 1.7: Phase-shifted semi-bridgeless boost PFC converter with return diodes

The topology introduces two more slow diodes (D_a and D_b) to the bridgeless configuration that connects to the input line as shown in Fig. 1.7. The conduction

losses associated with these diodes are minimal as large portion of the current flows through the FET intrinsic body diode.

1.3.2 Isolated DC/DC Converter Topologies

The DC/DC stage regulates the battery voltage from the voltage level at the DC link. Current-fed bridges and voltage-fed bridges, resonant converters and a combination of these are the most commonly used in isolated DC/DC converter. Isolated dc-dc converters can be broadly classified into voltage-fed and current-fed topologies or combination of both as depicted in Fig. 1.8. Placing an inductor after the dc bus ensures continuous current to the voltage source with minimum ripple thereby, making it a current-fed terminal. In general, these converters consist of an inverter followed by a HF (high frequency) transformer with desirable leakage inductance and a high frequency rectifier.

The directionality of the converter is determined by the type and number of switching devices used. Topologies can be further categorized based on primary and secondary bridge converter configuration. Fig. 1.9 shows some of the typical DC/AC (inverter) configurations and they include full bridge (FB), half bridge (HB), push pull and L-type half bridge converters [24]. The corresponding AC/DC (rectifier) configurations have the similar structure and are depicted using a single throw switch which can be replaced with a switch-diode combined device or just a diode depending on the operating directionality. Among these isolated topology combination some of the converter that are predominantly used in the industry are

ZVS FB Converter with Capacitor Output Filter: is illustrated in Fig. 1.11 . Current-fed topologies with the capacitive output filter minimized the diode rectifier current oscillating with the transformer leakage inductance as the resonant inductor is placed in series with the leakage. Moreover, high efficiency can be achieved using zero voltage

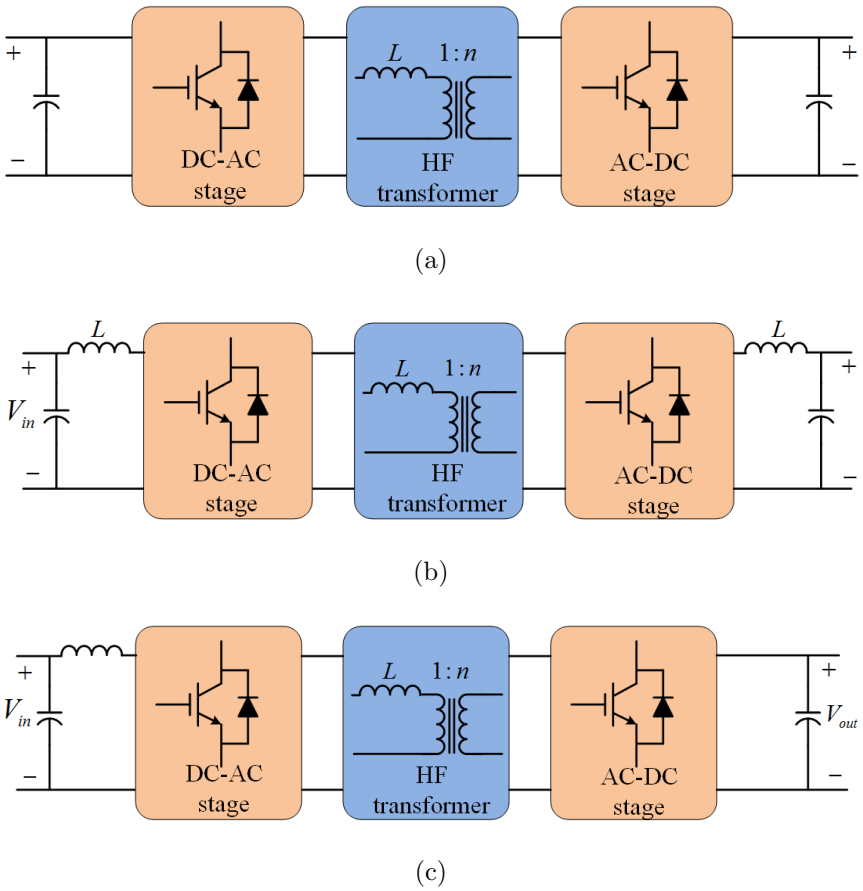


Figure 1.8: (a) Voltage-fed topology (b) Current-fed topology and (c) Voltage and current-fed topology

switching (ZVS), with specific PWM schemes [25].

FB Series-parallel resonant LLC Converter: The series resonant tank is formed by L_r and C_r as shown in Fig. 1.12 and the current through the resonant tank circuit is full-wave rectified at the output and it feeds the output stage. The LLC is widely used for its high efficiency at the resonant frequency and its ability to regulate the output voltage during hold-up time. The output voltage of the SPRC (series parallel resonant converter) can be controlled at no load and the range of switching frequency is smaller than for a series resonant converter. Moreover, compared to the parallel resonant converter, low switch and transformer RMS current are achieved at low load conditions. A frequency control is implemented, where the voltage is regulated by

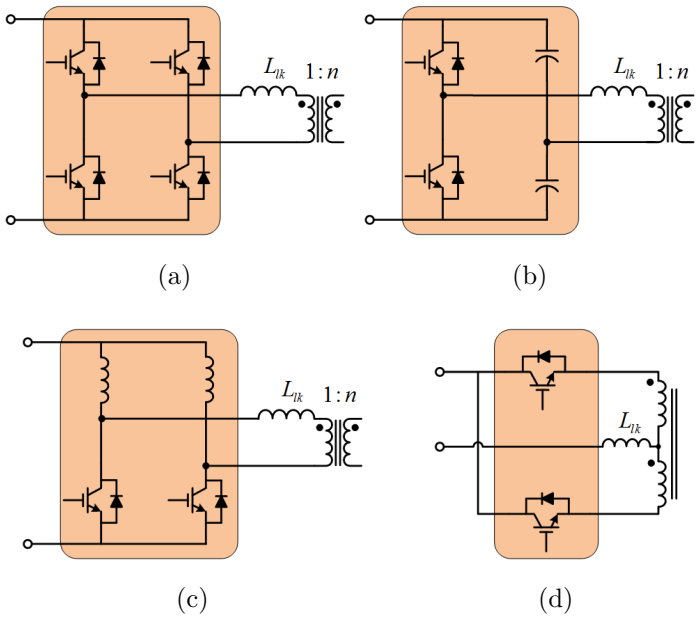


Figure 1.9: Primary bridge inverter configurations (a) Full-bridge topology (b)Half-bridge topology (c) L-type half-bridge topology and (d) Push-pull topology

moving the frequency above and below the resonant frequency [26].

Phase-Shifted FB Converter: This topology is ideal for medium to high-power applications where isolation is required. Its advantages are low voltage stress on the primary side switches, low current stress and ZVS capability without additional components or control complexity [27]. ZVS is critical for volume and weight sensitive equipments as it increases the efficiency and reduces thermal management unit. A similar architecture to this topology that can achieve high power density is the dual active bridge converter (DAB) shown in Fig.1.14 The major drawback to this topology is that it requires four additional switches and gate circuitry along with the switches that would increase the cost and complexity of the converter for an unidirectional operation.

Full bridge converters are usually preferred over the half bridge configuration as they facilitate freewheeling states which adds a degree of freedom to the converter. Though the voltage stresses on the switching devices remain the same, the current

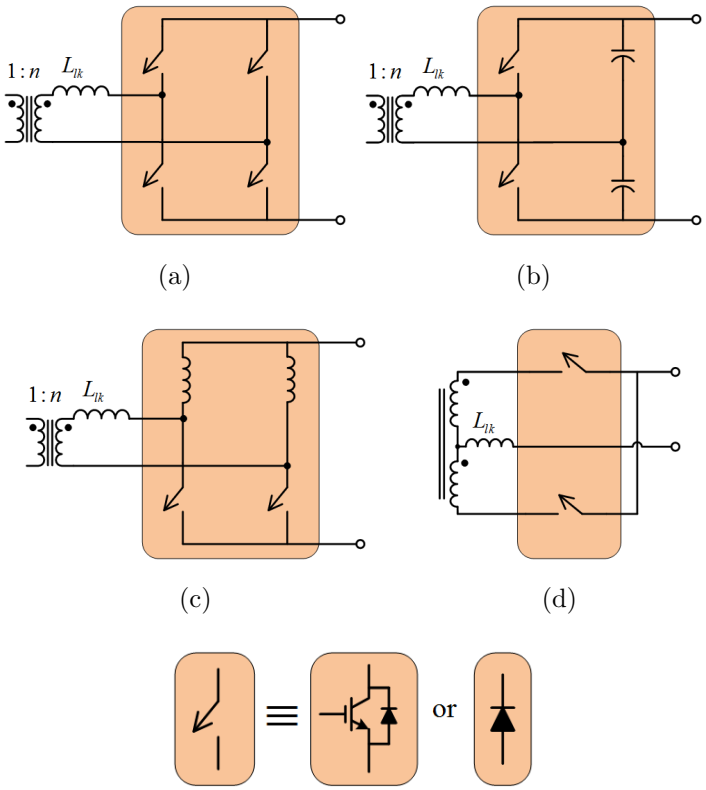


Figure 1.10: Secondary bridge configuration with switch-diode and diode configuration is preferred for bidirectional and unidirectional power flow respectively (a) Full-bridge topology (b) Half-bridge/ voltage doubler topology (c) Current doubler topology and (d) Push-pull topology

stress on the switches is reduced by half [28]. A comparison of high power DC/DC isolated converters is made in [24, 29] bringing out the pros and cons of the different topologies. Due to their suitability for high frequency operation, the isolated boost [30] (current-fed full bridge inverter with diode rectifier) and the phase modulated converter [31] (voltage-fed full bridge inverter with diode rectifier) rank among the most prominent converter candidates for high power applications. The current-fed topologies have additional snubber circuitry to reduce the voltage spikes and large inductors to improve the current quality. Hence, voltage-fed topologies are preferred to current-fed topologies with respect to reliability and cost.

Based on the finding in [32] among the bi-directional converters considered in this

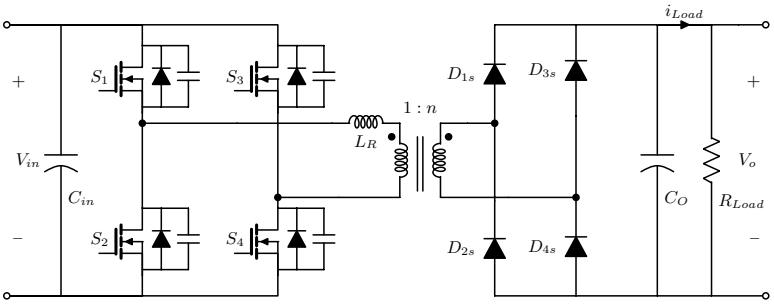


Figure 1.11: Full-bridge converter with capacitive output filter

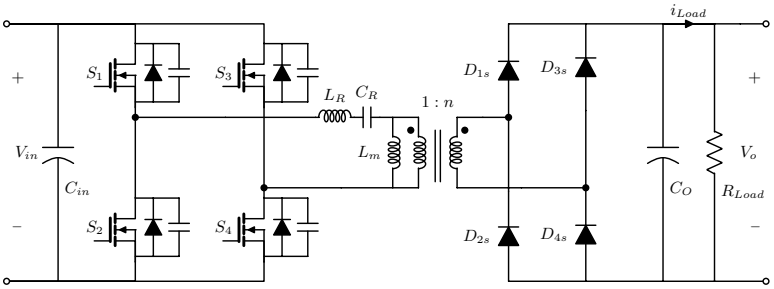


Figure 1.12: Full-bridge LLC resonant converter

work, a single-phase dual active bridge (DAB) converter topology is considered most promising with respect to the achievable converter efficiency and the power density (lower number of passive components). The DAB utilizes the leakage inductance of the transformer and employs DC capacitors at the input and output bridges as shown in Fig.1.14 ,thereby reducing the component count.

1.4 Specification of the On-Board Charger

The specifications of the unidirectional DC/DC converter in this work have been compiled in collaboration with industry partners and is shown in Table. 1.2. The AC/DC converter operates at 90-265 V/ 50-60 Hz input voltage feeding into the DC link voltage operating at 400 V dc followed by a battery pack ($300V \leqslant V_1 \leqslant 400V$). A nominal output power P_{out} of 3.3 kW is required within the specified voltage ranges with an input current limitation of 18 A rms.

Further objectives regarding the selection and the design of the on-board charger

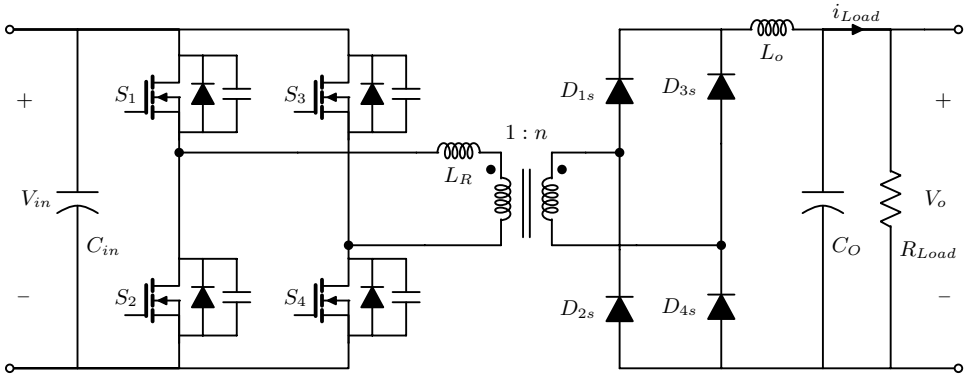


Figure 1.13: Phase-shifted full-bridge converter

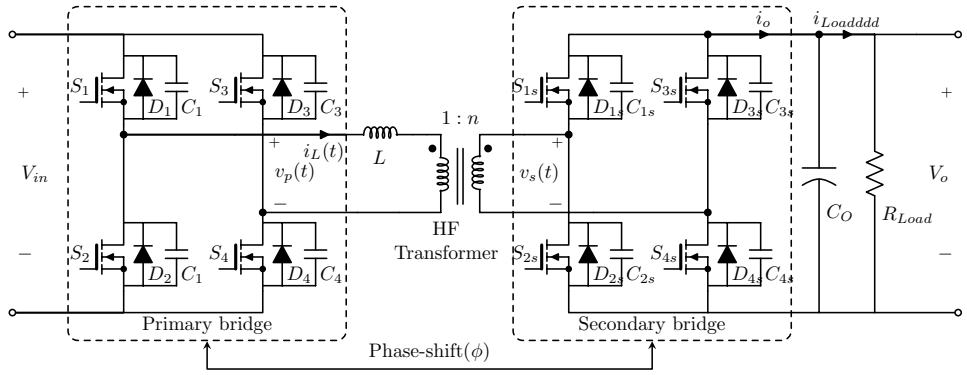


Figure 1.14: Phase-shifted dual active bridge converter

are listed below:

1. Converter efficiency $> 95\%$ at the nominal operating point ($V_{ac} = 240V, V_{dc} = 400V, P_{out} = 400V$)

2. Converter efficiency $> 90\%$ within reasonable input and output voltage ranges

3. Low converter volume for high power density

An important design parameter that was selected for these chargers is the switching frequency. The frequency of operation was chosen as 500 kHz by the industry partners for the front-end converters based on a general consideration than from an optimization process. With no thermal limitation in the design, the volume of the inductor, transformer and capacitors decrease with increasing switching frequency.

Table 1.2: On-board charger target specifications

Parameter	Value	Description
V_{in}	90 V $\leq V_{in} \leq$ 265 V	minimum and maximum voltages at the AC input side
	240 V	nominal voltage
V_{dc}	400 V	nominal DC link voltage
V_{batt}	300 V $\leq V_{batt} \leq$ 400 V	minimum and maximum voltages across the battery
f_s	500 kHz	switching frequency of AC/DC stage
	250 kHz	switching frequency of DC/DC stage

Additional requirements:
• galvanic isolation in the converter
• high power density
• high efficiency ($>$ 95% at nominal operating point)
• constant switching frequency

However, the conduction loss due to skin and proximity effects, core losses and switching losses in the circuit increases. Thus the efficiency number dictates the limitation of the circuit. The following DC/DC stage is designed to operate at 250 kHz.

1.5 Objectives and New Contributions of the Work

This dissertation focuses on achieving the targeted efficiency and power density using soft-switching techniques and converters. Power converter topology, soft-switching circuit and control strategies was given precedence over the optimization of existing converters. The new contributions of this work are:

- a new soft-switching full-bridge converter with phase-shifted secondary bridge is proposed. A modification of the popular dual active bridge, that retains all the advantages and suited for uni-directional power flow is analyzed and presented in this work;

- a detailed small signal model of the semi-dual active bridge with modulation scheme for the lossless converter are investigated;
- a novel soft-switching mechanism was implemented on the popular single phase boost type power factor correction circuit. An efficiency improvement of 40% was obtained at the targeted switching frequency of the front-end converter compared to the hard-switching converter;
- an improvement to the zero voltage switching mechanism utilizing an integrated magnetics setup and a half-bridge addition has been proposed.

The scientific papers published during the course of this dissertation are:

- S. Kulasekaran and R. Ayyanar, "A 500 kHz, 3.3 kW power factor correction circuit with low loss coupled auxiliary ZVT circuit," 2017 IEEE Applied Power Electronics Conference (APEC), 2017.
- S. Kulasekaran and R. Ayyanar, "A 500 kHz, 3 kW power factor correction circuit with low loss auxiliary ZVT circuit," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-7.
- S. Kulasekaran and R. Ayyanar, "Analysis, Design, and Experimental Results of the Semidual-Active-Bridge Converter," in IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5136-5147, Oct. 2014.
- S. Kulasekaran, R. Ayyanar and S. Atcitty, "Switching frequency optimization of a high-frequency link based energy storage system," IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, 2014, pp. 1847-1853.

- S. Kulasekaran and R. Ayyanar, "A 500 kHz, 3 kW power factor correction circuit with low loss auxiliary ZVT circuit," 2016 IEEE Energy Conversion Congress and Exposition, accepted.

- A. Sastry et al., "Failure modes and effect analysis of module level power electronics," Photovoltaic Specialist Conference (PVSC), 2015 IEEE 42nd, New Orleans, LA, 2015, pp. 1-3.

1.6 Chapter Overview

Chapter 2 gives an overview on the modifications to DAB converter and investigates the working principle of the unidirectional semi-dual active bridge converter. This includes the lossless model of the converter which facilitates basic synthesis of simple modulation schemes. This model is verified using a 1kW prototype and the experimental results are presented.

Chapter 3 presents a detailed analysis of the low-loss auxiliary circuit proposed and implemented on a single phase boost-type PFC converter. The design of auxiliary circuit and operating principle of the soft-switching mechanism is explained in detail.

In **Chapter 4**, two modifications of the existing ZVT circuit is implemented that aims at further reducing the total footprint of the converter by utilizing an integrated magnetic structure and/or one half-bridge leg of the following DC/DC stage. **Chapter 5** summarizes the obtained results and concludes this work by presenting an outlook regarding the future research in this field.

Chapter 2

ANALYSIS AND DESIGN OF SEMI-DUAL ACTIVE BRIDGE CONVERTER

2.1 Introduction

For power conversion applications requiring bi-directional power flow and galvanic isolation, the dual active bridge (DAB) is a preferred topology due to its many advantageous features [33], [34]. It offers zero-voltage switching (ZVS) of all the power devices without requiring additional active or passive components, and making effective use of the leakage inductance of the transformer. Thus reducing the voltage stress on devices and the requirement on passive filter components in comparison to competing solutions. Above all, the topology is completely symmetric when viewed from the primary and secondary sides, and allows for seamless, dynamic reversal of power flow simply by adjusting the phase-shift between the two active bridge voltages. The controllers are simple to design, for example, using a gyrator-based average model [35], and the fixed duty-ratio of approximately 0.5 for all the switches makes the gate-drive circuitry also simple. Comparisons of soft switching topologies for high power (few kW to hundreds of kW) applications are presented in [29], [24] which show the DAB to be a preferred topology. At lower power levels, dual half-bridge configuration can also be used to reduce the number of active switches [36]. The DAB is well-suited for multiport operation where multiple DC sources and loads can be interfaced through a single converter [37], [38]. The DAB also lends itself well for modular power conversion architecture and has been proposed as a building-block for modular high-power converters [39], [40]. In addition to traditional DC/DC conversion applications, the DAB has also been used in the DC/DC stages of several

inverters and solid-state transformers [41], [42] where the requirement on arbitrary power factor requires bi-directional power converter stages.

Some of the disadvantages of the DAB topology include limited ZVS range with a strong dependence on the voltage conversion ratio and load, relatively higher RMS currents through the transformer and semiconductor devices due to circulating currents, and a negative pulse in the input and output currents with the duration dependent on the phase-shift leading to higher capacitor RMS currents. The transformer size is also relatively higher owing to the application of full pulse-width square wave at the primary and secondary of the transformer with the applied volt-sec increasing with the input and output voltages. Several approaches have been proposed to address the above-mentioned disadvantages, and methods that have direct relevance to the topology proposed here are related to pulse-width control of the DAB in addition to phase-shift control. PWM control (by controlling the phase-shift between the two legs of the primary or secondary bridge) of a single H-bridge of DAB was proposed in [43] and [44] for extending the ZVS range. An overall loss reduction strategy was discussed in [45] using single PWM control of DAB. In [46] a scheme which maintains equal duty ratios of primary and secondary bridge voltages which controls the phase shift between them was proposed. A comprehensive analysis and validation for dual PWM control wherein both the H-bridges are individually and independently controlled in addition to phase-shift control were presented in [47] to extend ZVS range and significantly improve light load efficiency and reduce transformer size.

While the advantages of DAB are especially striking for bidirectional power flow applications, many of its features are equally appealing for DC/DC conversion where the power flow needs to be only unidirectional. There are numerous unidirectional power flow applications including various types of DC power supplies, DC/DC stage of different types of photovoltaic (PV) inverters, battery chargers in electric vehicles

and other applications where the discharging is not through the same converter, and power converters for fuel cell applications. Some of the popular topologies for the high power, isolated DC/DC converters include the phase-shift controlled full-bridge converter [48], [31] series resonant converters [49], [50] and isolated boost especially for PV converters [51] (which are compared with the proposed topology in Section IV).

This work proposes the semi-dual active bridge (S-DAB) converter for the unidirectional power flow applications. Here, the active H-bridge on the source side (primary) is retained, but the load side (secondary) H-bridge is replaced by a semi-active bridge with two switches and two diodes. In addition to reducing the number of switches, it alters the operating characteristics leading to advantages similar to PWM control of DAB. It may be noted that the primary H-bridge may also be replaced by a half-bridge for lower power applications.

This chapter is organized as follows. Section II introduces the proposed S-DAB topology, analyzes the various operating intervals to obtain the power transfer and ZVS characteristics. A brief description of the small-signal model is also presented. Section III validates the converter operation and analysis through simulation, and experimental results from a hardware prototype. Section IV gives a brief discussion on the benefits of the S-DAB over other isolated DC/DC converters, and suggests possible improvements to S-DAB. Finally, a summary and conclusions are presented in Section V

2.2 Topology Development

A schematic of the proposed unidirectional converter is shown in Fig.2.1. The converter has two H-bridges, an active, leading full-bridge (HB1) comprising of four MOSFETs or IGBTs with anti-parallel diodes, and a semi-active, lagging bridge

(HB2) comprising of two diodes for the upper switches and two MOSFETs or IGBTs with anti-parallel diodes for the lower switches. The diodes for the upper switches of HB2 limit the power flow to be unidirectional from the source connected to the active bridge to the load connected to the semi-active bridge. The two bridges are connected by a transformer which provides galvanic isolation and voltage step-up or step-down functions.

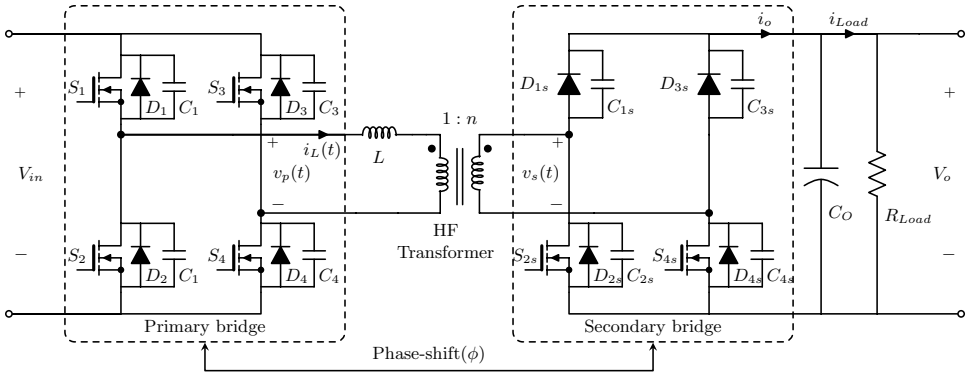


Figure 2.1: Circuit schematic of the proposed S-DAB converter

Similar to the DAB, the leakage inductance is a key element in determining the power handling capacity of the S-DAB converter. The high frequency transformer in the DAB or S-DAB is fabricated with high leakage inductance. The inductance is either implemented as an integrated magnetic structure or as an external component to achieve the desired value. The switches in HB1 and HB2 are typically driven by square waveforms of 50% duty cycle and the power flow is controlled by varying the phase shift angle ϕ between the bridges. By ensuring proper direction of the pole current during switch transitions (i.e., current should leave the midpoint of each leg for transition from upper switch to lower switch in that leg and vice versa), the switch capacitances can be charged and discharged appropriately resulting in ZVS for each of the six active switches. It may also be noted that both the controlled switches on the secondary side are referenced to output ground which results in easier gate drive.

2.2.1 Operation and Analysis of Semi-DAB

Analysis of the S-DAB converter can be simplified by referring the entire model to the primary of the transformer such that the two bridges are linked by the leakage inductance of the transformer. Resistances of the transformer and semiconductor switches, and the threshold voltages of diodes and MOSFETs are neglected in this analysis. The primary side bridge HB1 produces a square wave voltage waveform (PWM control of HB1 is possible and is pursued as future work) at constant frequency indicated as v_p in Fig.2.1. The voltage produced by the secondary bridge indicated as v_s in Fig.2.1, has a quasi-square waveform with the pulse-width determined by the operating conditions, in particular by the conduction of the diodes in the secondary bridge. The control of the converter is achieved by phase shifting (delaying) the rising edge of v_s with respect to the rising edge of v_p. Shifting the phase of the secondary bridge by an angle ϕ changes the effective voltage across the leakage inductance thereby controlling the current through the transformer. The net power always flows from the leading (primary) to the lagging (secondary) bridge.

Similar to the DAB, many of the converter waveforms depend strongly on the voltage ratio, m, where, $m = V_o/nV_{in}$ and n is the secondary to primary turns ratio of the transformer. Fig. 2.2 shows the operating waveforms of the converter for different voltage ratios, $m < 1$ (buck) and $m > 1$ (boost). Unlike in the DAB, the operation here involves inherent freewheeling of the secondary winding for an angle α_s as the diodes on the upper section of each leg in the secondary bridge prevent reverse current flow.

Three intervals of operation can be identified in a half cycle that also repeats in the negative direction in the second half cycle as illustrated in Fig. 2.2. In each interval the current through the leakage inductance i_L is a function of $\theta = \omega t$, where

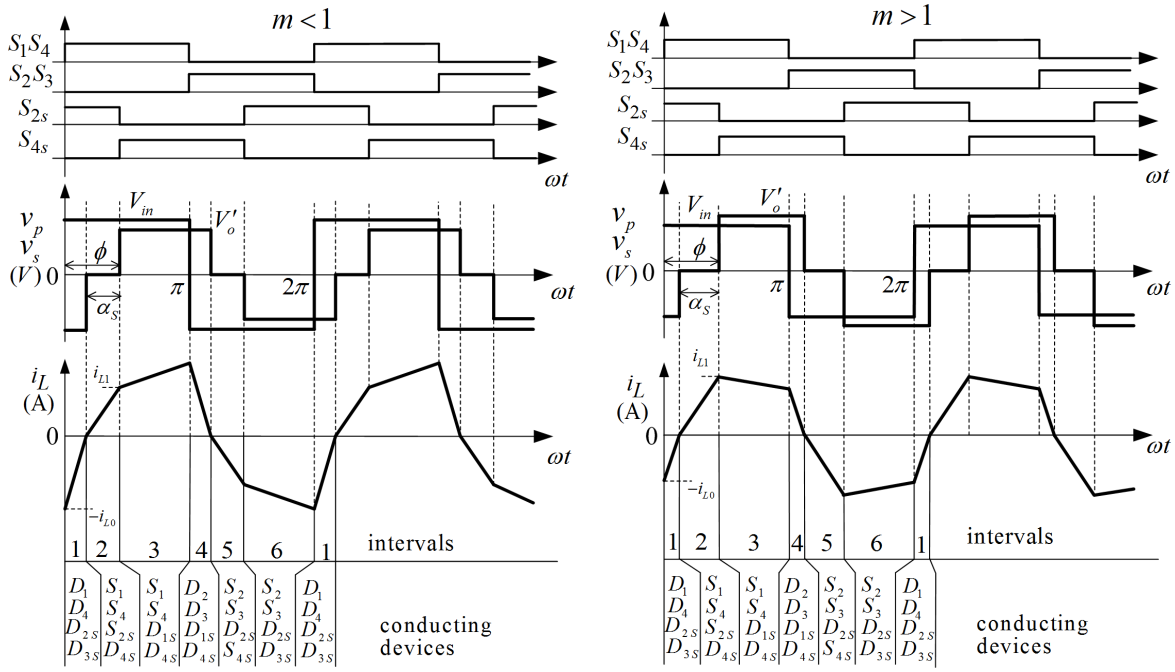


Figure 2.2: Voltage across the transformer ports and converter current waveforms

ω is the switching frequency in rad/s. Referring to Fig. 2.2, the inductor current is given by

$$i_L(\theta) = \frac{[v_p(\theta) - v_s'(\theta)]}{\omega L}(\theta - \theta_i) + i_L(\theta_i) \quad \text{for } \theta_i < \theta < \theta_f \tag{2.1}$$

where θ_i and θ_f are the initial and final angles of each interval of operation, v_p is the voltage across the primary of the transformer, v_s' is the voltage across the secondary of the transformer referred to the primary and L is the leakage inductance.

Also, the current and power quantities have been normalized to the following base:

$$\text{Current base: } I_{base} = \frac{V_{in}}{\omega L}; \quad \text{Power base: } P_{base} = \frac{V_{in}^2}{\omega L}$$

Fig. 2.2 and (2.1) can be used to analyze the operation of S-DAB in the six intervals of a complete cycle. The devices conducting and the current path during

various intervals and during the transition between the intervals are shown in Fig. 2.3.

Interval 1: $0 < \theta < (\phi - \alpha_s),\ v_p(\theta) = V_{in}$ and $v_s^{'} = -V_o^{'}$

Interval 1 begins when the negative-to-positive transition in v_p initiated by the turn-off of S_2 and S_3, is complete, and ends when the inductor current reaches zero. The operation during Interval 1 is similar to that of DAB, but the conditions for transitioning to Interval 2 are different in the two topologies. Fig. 3(a) shows the current flow in the primary and secondary bridges through diodes D_1, D_4, D_{2s} and D_{4s} , and it can be seen that $v_p = V_{in}$ and $v_s^{'}(\theta) = -V_o^{'}$ Therefore, the current expression from (2.1) is

$$i_L(\theta) = \frac{V_{in} + V_o^{'}}{\omega L}\theta - i_L(0) \tag{2.2}$$

At the end of mode 1, the equation for the normalized current can be written as

$$i_L(\theta - \alpha_s) = (1 - m)(\theta - \alpha) - i_{L0} \tag{2.3}$$

where i_{L0} as defined in Fig. 2.2 is the current at the start of Interval 1.

Transition from Interval 1 to Interval 2:

The inductor current becomes zero and starts to increase in the positive direction with the voltage across the inductor initially as $V_{in} + V_o^{'}$. At this point in the first leg of the secondary bridge, the inductor current transfers automatically from the anti-parallel diode D_{2s} to the switch S_{2s} which was already gated on ensuring zero voltage switching. In the second leg, the current splits equally amongst the capacitors C_{3s} and C_{4s} charging and discharging them respectively. Capacitor C_{3s} is charged from zero to a final value of $V_o^{'}$, while C_{4s} simultaneously discharges from $V_o^{'}$ to zero. The current directions are illustrated in Fig. 2.3(b). The operation enters Interval

2 when the charging and discharging respectively of C_{3s} and C_{4s} are completed, and D_{4s} begins to conduct.

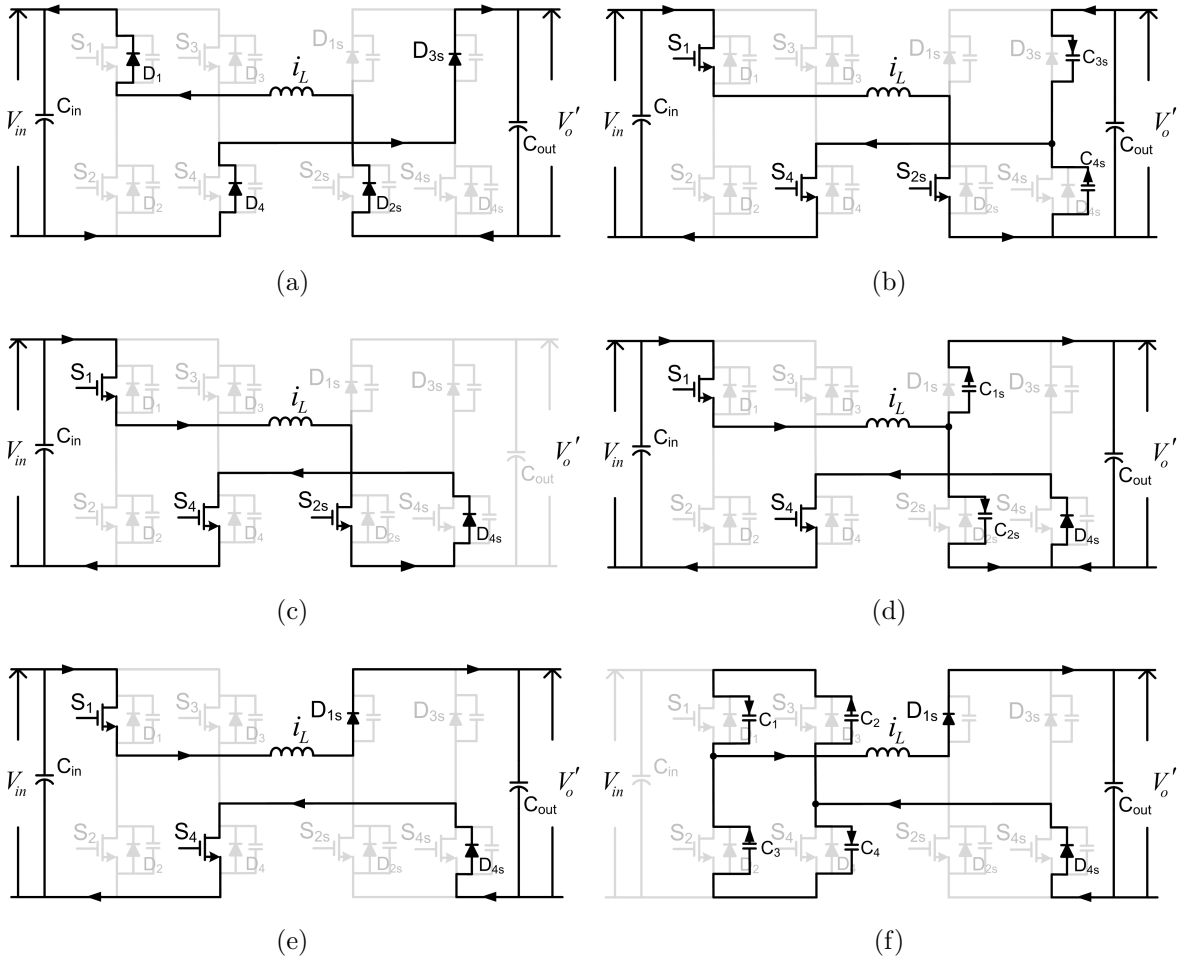


Figure 2.3: Current paths and conducting devices in S-DAB during the three intervals in the positive half cycle and during the transitions between the intervals (a) Interval 1 (b) Transition from Interval 1 to Interval 2 (c) Interval 2 (d) Transition from Interval 2 to Interval 3 (e) Interval 3 (f) Transition from Interval 3 to Interval 4

Interval 2: $(\phi - \alpha_s) < \theta < \phi,\ v_p(\theta) = V_{in}$, and $v_s'(\theta) = 0$

S-DAB differs from DAB mainly in Interval 2 in terms of the freewheeling on the secondary side and the voltage applied across the inductor. Fig. 2.3(c) shows the conducting elements in Interval 2. During this interval the current freewheels in HB2

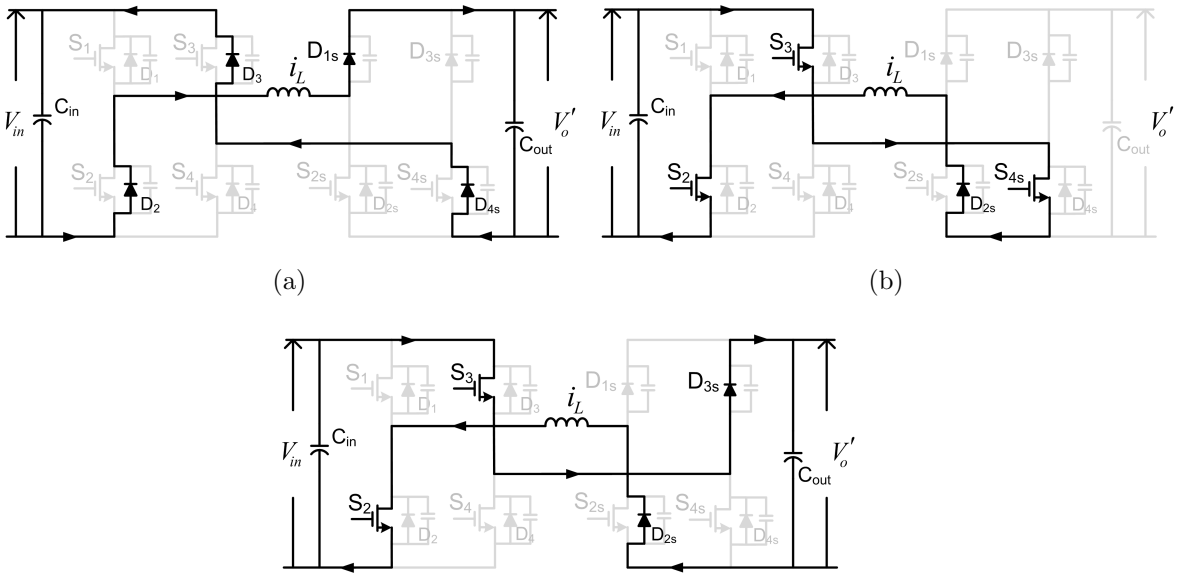


Figure 2.4: S-DAB operation in the negative half cycle (a) Interval 4 (b) Interval 5 (c) Interval 6

through S_{2s} and D_{4s}. The expression for the current can be written as

$$i_L(\theta) = \frac{V_{in} + 0}{\omega L}\theta + i_L(\phi - \alpha_s) \tag{2.4}$$

At the end of Interval 2, the equation for the normalized current can be written as

$$i_L(\phi) = i_{L1} = \alpha_s + 0 \tag{2.5}$$

where i_{L1} as defined in Fig. 2.2 is the current at the end of Interval 2.

Transition from Interval 2 to Interval 3:

The transition into Interval 3 is triggered by turning off S_{2s} of HB2. Switch S_{2s} experiences small turn-off losses during this period as the residual current through the switch overlaps with switch capacitor voltage that increases from 0 to $V_o^{'}$. These losses can be reduced by introducing an additional capacitance across the switch. However, when the converter is operating outside the ZVS range, turn-on losses increase with

larger capacitance. Hence, selecting the optimum capacitance is a tradeoff between the turn-on and turn-off losses depending on the operating conditions. This transition ends when C_{2s} is fully charged to $V_o^{'}$ and C_{1s} is fully discharged and the diode D_{1s} begins to conduct.

Interval 3: $\phi < \theta < \pi,\ v_p(\theta) = V_{in}$ and $v_s^{'}(\theta) = V_o^{'}$

Figure 2.3(e) depicts the current flows in Interval 3. The current flows through switches S_1, S_4 in HB1 and D_{1s}, D_4 in HB2. This creates a voltage difference of $V_{in} - V_o^{'}$ across the inductor. The expression for current in the interval based on (2.1) is given in (2.6), and the expression for the normalized current at the end of the interval is shown in (2.7). This interval ends when S_1 and S_4 are turned off.

$$i_L(\theta) = \frac{V_{in} - V_o^{'}}{\omega L}\theta + i_L(\phi) \tag{2.6}$$

$$i_L(\pi) = (1 - m)\pi + i_{L1} \tag{2.7}$$

Transition from Interval 3 to Interval 4:

The ZVS operation can be observed in Fig. 2.3(f) for an appropriate operating condition of the converter. The transition begins when S_1 and S_4 are switched off, which forces the current to flow into C_1, C_4 and simultaneously discharge C_2 and C_3. The voltage across switches S_2 and S_3 reduces from V_{in} to 0 and the corresponding diodes D_2 and D_3 begin to conduct before the start of the next interval thereby ensuring zero turn-on loss.This transition is similar to transition between Mode 1 and 2 for a conventional DAB [33].

Interval 4: $\pi < \theta < \pi + \phi - \alpha_s,\ v_p(\theta) = -V_{in}$ and $v_s^{'}(\theta) = V_o^{'}$

Interval 4 with diodes D_2 and D_3 conducting is similar to Interval 1 with the direction of currents reversed. Intervals 5 and 6 are similar to Intervals 2 and 3. Hence, similar analyses can be performed for these operating conditions. The operation of S-DAB in these three intervals is illustrated in Fig. 2.4.

2.2.2 Power Transfer and Control

Let us consider i_{L0} as the value of current at the start of Interval 1 and i_{L1} as the value at the end of Interval 2 as shown in Fig. 1. From (2.3), (2.5) and (2.7) the solution for i_{L0} and i_{L1} can be obtained using $i_L(0) = -i_L(\pi)$ through the symmetry condition. The expressions describing the complete current waveform are given in (2.8), (2.9) and (2.10).

$$i_{L0} = \frac{(1-m)\pi + m\phi}{m+2}(m+1) \tag{2.8}$$

$$i_{L1} = \frac{2\phi - (1-m)\pi}{m+2} \tag{2.9}$$

$$\alpha_s = \frac{2\phi - (1-m)\pi}{m+2} \tag{2.10}$$

The output power equation is derived as

$$P = i_{o,avg}V_o^{'} = i_{in,avg}V_{in} \tag{2.11}$$

The power transferred is the product of the average current and voltage at the input. The average current $i_{in,avg}$ is the area under i_L in a complete cycle for a positive V_{in} as illustrated in Fig. 2.2. The normalized power equation is given in (2.12) as

$$P_{p.u.} = \frac{1}{2}[-i_{L0}\phi + (i_{L0} + i_{L1})(\pi - \phi - \alpha_s)] \tag{2.12}$$

Substituting values for $i_{L0},\ i_{L1}$ and α_s we obtain the final power transfer expression given in (2.13)

$$P_{p.u.} = \frac{1}{2}\left[\frac{4m(m^2+m+1)}{(m+2)^2}\pi\phi - \frac{2m(m^2+m+2)}{(m+2)^2}\phi^2 + \frac{m(2m+1)(1-m)}{(m+2)^2}\pi^2\right] \tag{2.13}$$

The power transfer expression in (2.13) differs significantly from that of a conventional DAB which is given in (2.14) as comparison.

$$P_{p.u.} = m\phi\left(1 - \frac{\phi}{\pi}\right) \tag{2.14}$$

When the magnitude of voltages V_{in} and $V_o^{'}$ are equal i.e. when $m = 1$ then, (2.13) for the case of S-DAB simplifies to (2.15) which resembles the power expression for DAB.

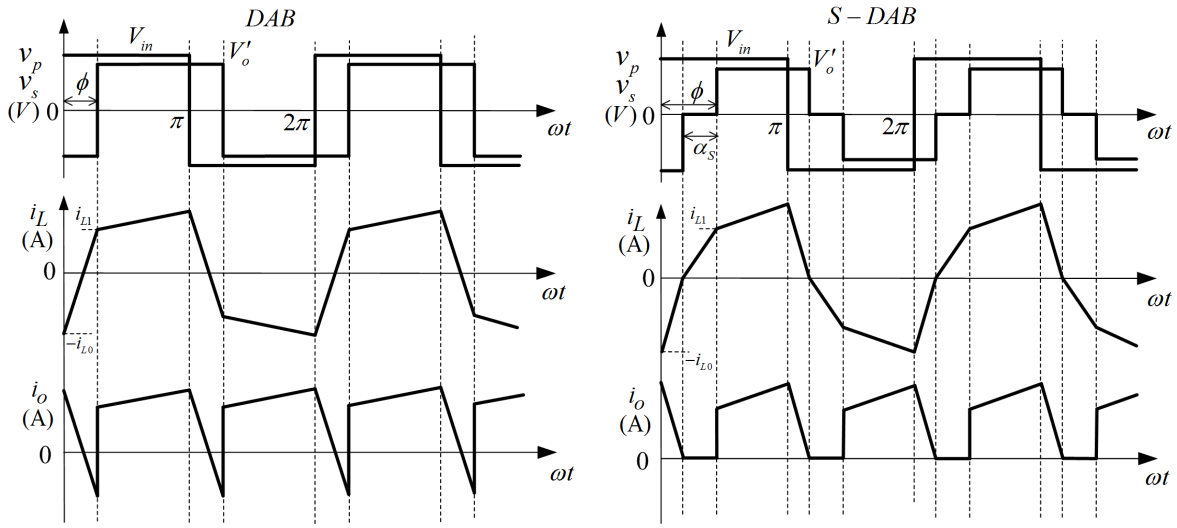
$$P_{p.u.} = \frac{\phi}{9}(6 - 5\frac{\phi}{\pi}) \tag{2.15}$$

From the above expressions by varying ϕ the power transferred can be controlled which can in turn be used to control other variables such as output voltage and output current depending on the requirement of the specific application.

2.2.3 Output Capacitor Current Ripple

The ideal waveforms of the output current i_o (before the output capacitor) along with the bridge voltages corresponding to conventional DAB and S-DAB are shown in Fig. 2.5(a) and 2.5(b) respectively. One of the advantages of the S-DAB compared to conventional DAB with phase-shift control is the absence of a negative pulse in the current i_o as seen from Fig. 2.5. With four switches and diodes in the secondary bridge of DAB the output current has a significant negative value and for a duration dependent on the phase shift. However, in S-DAB, the diodes in the secondary bridge block this reverse current flow, causing the converter to freewheel during this interval.

This leads to reduction in the rms current of the output capacitances as well as smaller capacitance requirement for a given voltage ripple.



(a) (b)

Figure 2.5: Voltage across transformer ports, inductor and output current waveforms (a) DAB converter (b) S-DAB converter

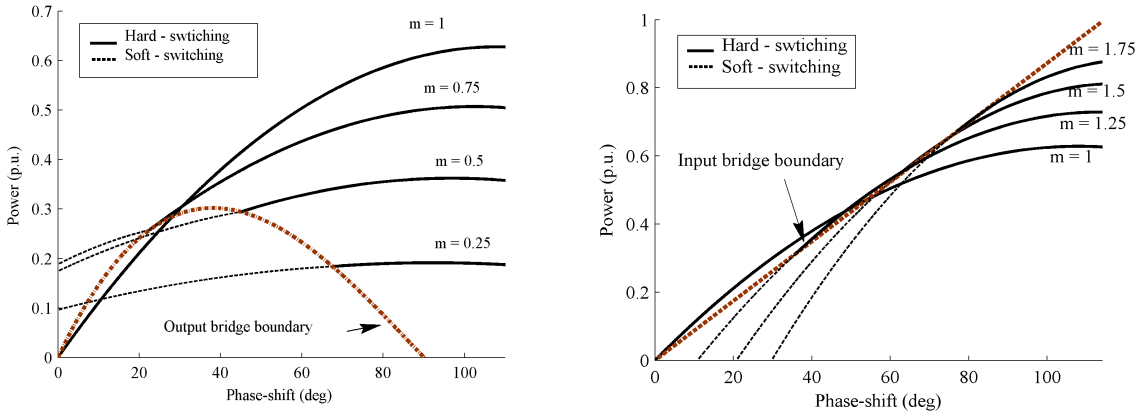
2.2.4 ZVS Range and Constraints

Fig. 2.6 shows the range of control on the output power with the variation of phase-shift ϕ as the varying parameter for the DAB and its derivative. Neglecting the small current required to charge and discharge the capacitances, the condition $i_{L0} > 0$ ensures ZVS in HB1, while switches in HB2 require $i_{L1} > 0$. Therefore, for any $m \neq 1$ there is a minimum phase-shift associated to maintain soft-switching as inferred from (2.16) and (2.17). These inequalities are obtained from (2.8), (2.9). From (2.8), ϕ requirement for bridge HB1 ($i_{L0} > 0$)

$$\phi > \frac{(m-1)}{m}\pi \quad (0 < m < \infty) \tag{2.16}$$

and from (2.9), ϕ requirement for bridge HB2 ($i_{L1} > 0$)

$$\phi > \frac{(1-m)}{2}\pi \quad (0 < m < \infty) \tag{2.17}$$



(a) (b)

Figure 2.6: Family of output versus phase-shift curves of an S-DAB with m as a parameter (a) $m < 1$ (b) $m > 1$

From (2.16) and (2.17) it can be concluded that the leading bridge HB1 always operates with ZVS when $m < 1$, whereas the lagging bridge has a minimum requirement on the phase-shift angle. Similarly, HB1 has a minimum ϕ condition when operated in the boost mode, whereas HB2 operates inside the soft-switching region.

The solid line as illustrated in Fig. 2.6 corresponds to the soft-switching boundary which is the locus of minimum power for varying ϕ , below which the converter loses ZVS. The equivalent m value for the phase-shift angle is attained by equating (2.17) to zero. The full range of control over the power can be achieved when the voltage ratio is unity which is similar to that of a DAB as seen in Fig. 2.7.

Circuit designers are usually interested in the output voltage versus the output DC current (I_{Load}) characteristics of the converter. In Fig. 2.8 (a), (b), the voltage in the y-axis is normalized with respect to the input bridge voltage and the current is represented in per units and constant R lines indicate the normalized load to the system. The shaded region in the illustration corresponds to the soft-switching operation, where the output current increases with increase in the phase-shift angle at a particular operating voltage. The region is bounded by three constraints, where the

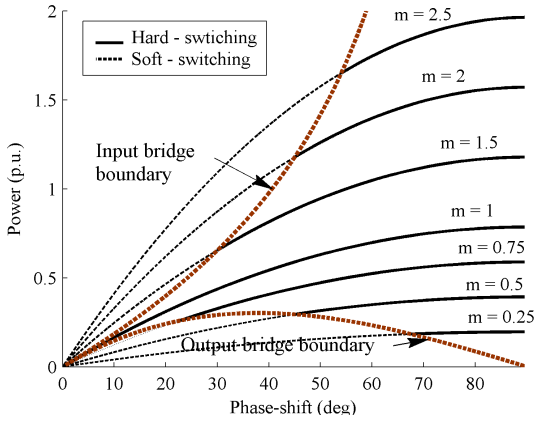
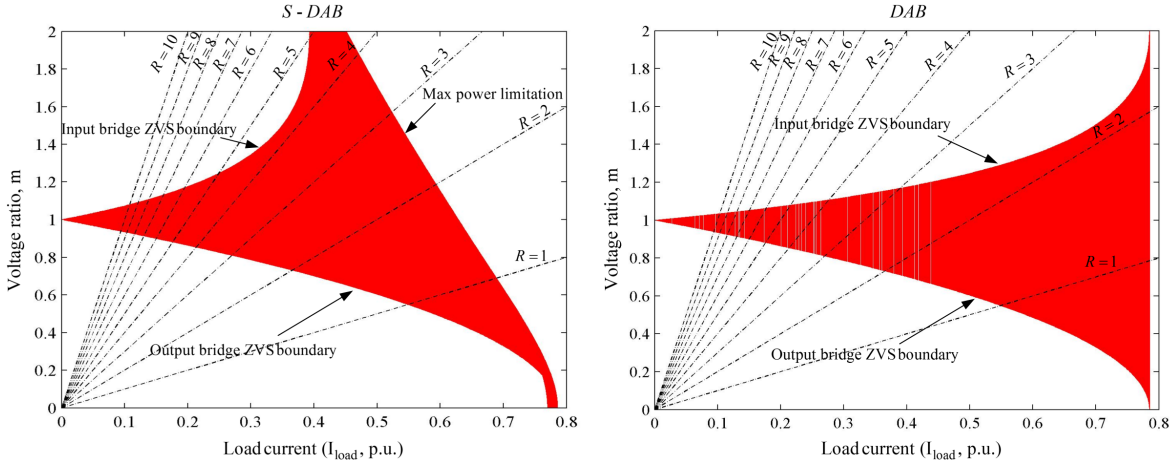


Figure 2.7: Family of output power versus phase-shift angle curves with m as a parameter for a conventional DAB



(a) (b)

Figure 2.8: ZVS boundaries on the output voltage plane (a) S-DAB (b) Conventional DAB

lower bound is a locus of minimum output currents required to maintain ZVS with $m < 1$ and ϕ as the varying parameter. Equality of (2.17) yields the upper bound or the locus of minimum current for varying ϕ and $m > 1$. The maximum power carrying capability of the converter forms the right most bound to the region. External load to the circuit and the voltage difference between the primary and secondary bridges are key factors in determining the soft-switching range of these converters.

2.2.5 Small Signal Model of the Converter

A simple current source model of the DAB as shown in Fig. 9 has been presented in [33] and [34] for small signal analysis and controller design. The same model is applicable for the S-DAB as well with suitable modification in the expression for the current source

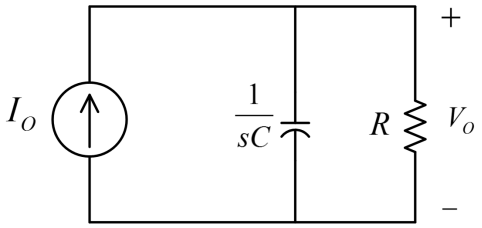


Figure 2.9: Low frequency small signal model of the S-DAB

The output current I_o, in steady state can be obtained from (2.13) for a particular angle ϕ as,

$$I_{o,p.u.} = \frac{1}{2\pi mn}\left[\frac{4m(m^2+m+1)}{(m+2)^2}\pi\phi - \frac{2m(m^2+m+2)}{(m+2)^2}\phi^2 + \frac{m(2m+1)(1-m)}{(m+2)^2}\pi^2\right] \tag{2.18}$$

The control to output transfer function can be derived by holding the input voltage V_{in} and the frequency constant. In the S-DAB $\Delta\phi$ is assumed to be a small disturbance around the operating point ϕ which causes a small disturbance ΔI_o around the output current I_o. This in turn produces a disturbance ΔV_o around V_o. Hence from (2.16) the following can be derived.

$$\begin{aligned} & I_o + \Delta I_o = f(\phi + \Delta\phi) \\ & \Rightarrow \Delta I_{o,p.u.} = \left[\frac{2m(m^2+m+1)}{(m+2)^2}\Delta\phi_o - \frac{2m(m^2+m+2)}{(m+2)^2}\frac{\phi\Delta}{\pi}\right] \\ & \Rightarrow \frac{\Delta I_{o,p.u.}}{\Delta\phi_o} = \frac{2}{(m+2)^2}\left[(m^2+m+1) - (m^2+2m+2)\frac{\phi}{\pi}\right] \end{aligned} \tag{2.19}$$

The small-signal model to a resistive load as shown in Fig. 2.9 can be obtained from (2.19) as,

$$\frac{\Delta V_o(s)}{\Delta \phi_o(s)} = \frac{2R}{(1+sCR)(m+2)^2}\left[(m^2+m+1)-(m^2+2m+2)\frac{\phi}{\pi}\right] \tag{2.20}$$

For $m = 1$, (2.18) reduces to

$$\frac{\Delta V_o(s)}{\Delta \phi_o(s)} = \frac{2}{9}\frac{R}{1+sCR}\left[3-5\frac{\phi}{\pi}\right] \tag{2.21}$$

2.3 Simulation and Experimental Results

The proposed topology is validated experimentally with a 1 kW prototype converter. Experimental results verifying the simulation results from PLECS have been presented in this section.

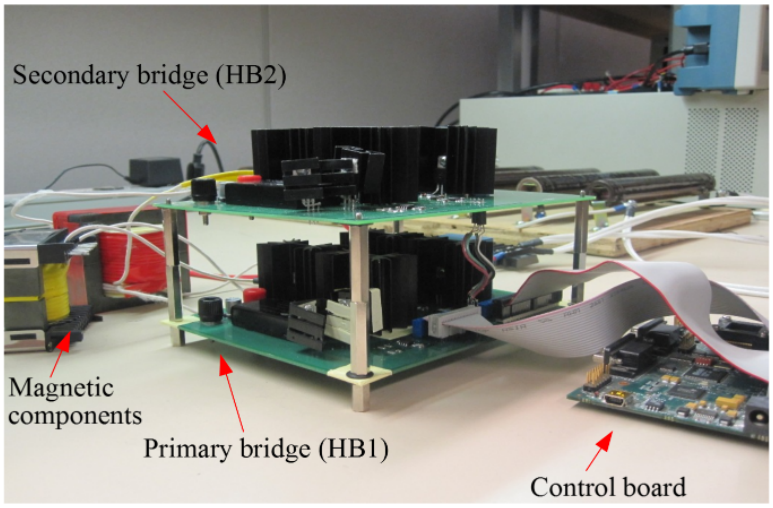


Figure 2.10: Photograph of the experimental prototype

2.3.1 Converter Design

The prototype seen in Fig. 10 has been designed for a rated power of 1 kW, at a switching frequency of 50 kHz. The basic specifications and some of the design parameters are shown in Table 1. A closed loop voltage controller based on the plant transfer function as shown in (20) was designed to regulate the output voltage.

IPP65R280E6 MOSFETs were selected to meet the desired voltage and current requirements for HB1 and the two switches of HB2. The upper devices on the secondary bridge were HFA15TB60PBF HEXFRED ultrafast diodes rated with a reverse blocking voltage of 600 volts. Ceramic capacitances of 680 pF were incorporated in parallel to the switching devices, to reduce the turn-off losses during hard-switching. The current ripple at the DC link is filtered using EPCOS Inc. polypropylene capacitors. A Ferroxcube 3C93 MnZn ferrite core and litz wire was used to construct the transformer. The entire control of the system was implemented on a Texas Instruments^{TM} TMS320F2808 digital signal processor (DSP). TI Code Composer Studio loads the C-code onto the DSP that resides on the eZDSP2808 evaluation board [52].

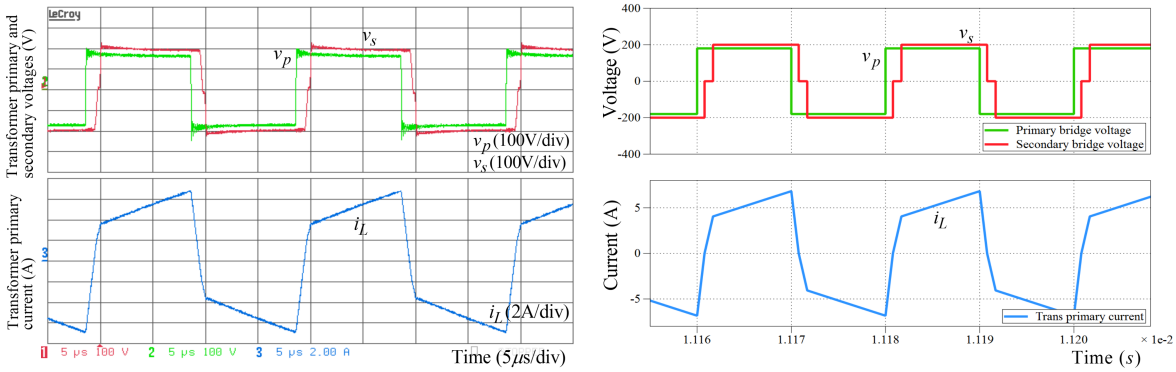
Table 2.1: S-DAB specifications and selected design parameters

Parameters	Specifications
rated power	1000W
Input votlage	100V- 200V
Output voltage	200V
Frequency	50 kHz
Transformer turns ratio	1:1.2
Leakage inductance	40μH
Output capacitance	15μF
Input capacitance	20μF

2.3.2 Experimental Waveforms and Comparison with Simulation

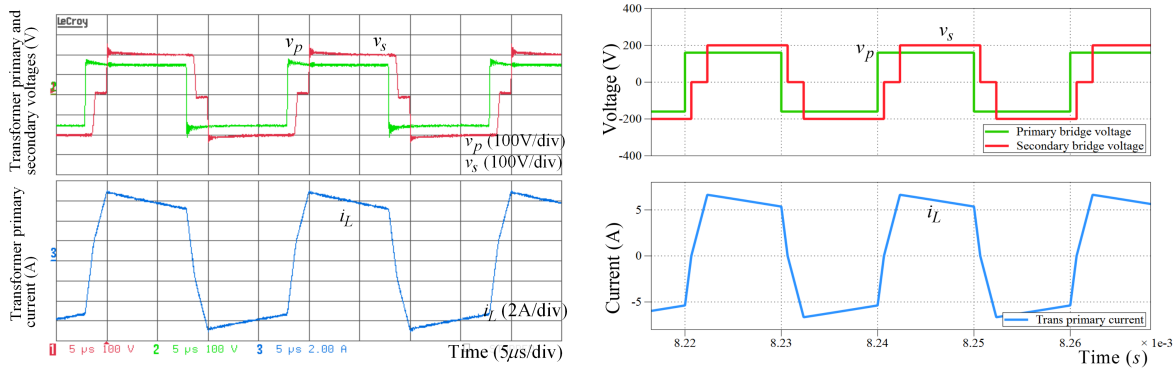
Fig. 11 (a) and (b) show the operating waveforms of the S-DAB in buck mode ($m < 1$) at a power level of 800 W. The output voltage of the converter was regulated at 200 volts, the input maintained at 180 volts and the corresponding phase-shift

angle required was 70 degrees. It can be seen that the experimental and simulated results match very well



(a) (b)

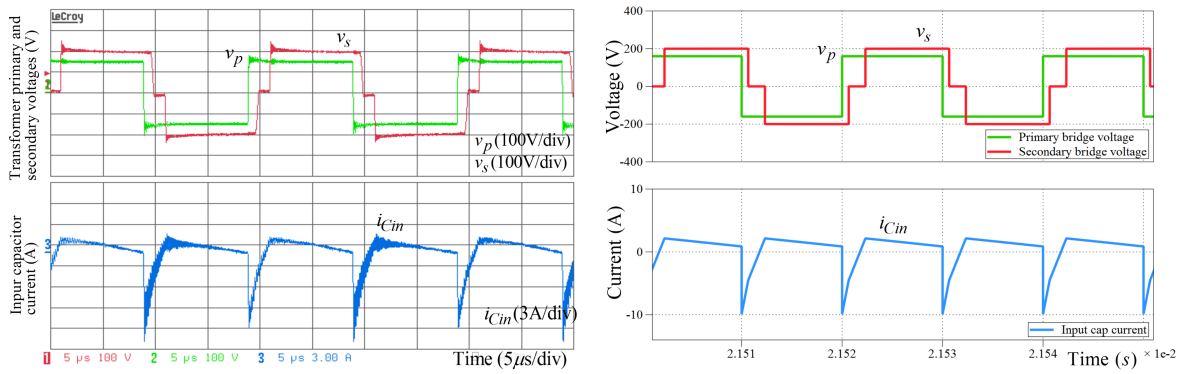
Figure 2.11: Waveforms of the bridge voltages and transformer primary current of S-DAB in buck mode ($m < 1$) (a) Experimental waveform (b) Simulated waveform



(a) (b)

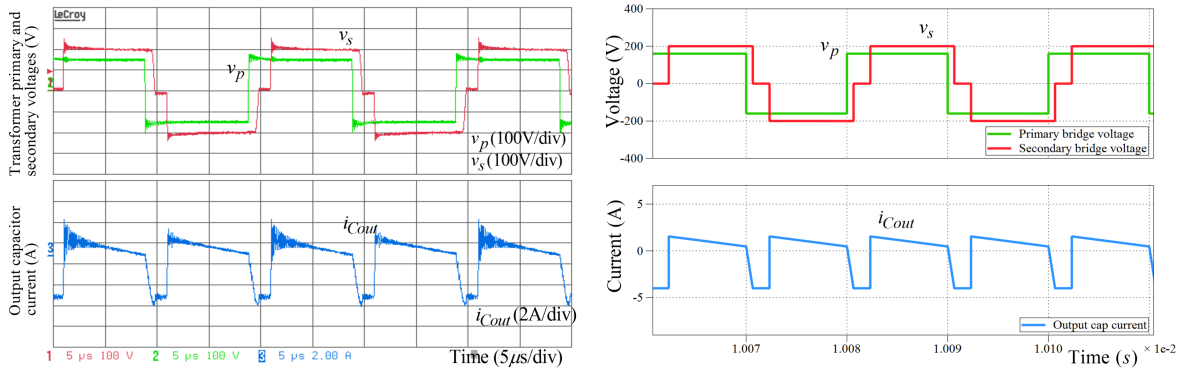
Figure 2.12: Waveforms of the bridge voltages and transformer primary current of S-DAB in boost mode ($m > 1$) (a) Experimental waveform (b) Simulated waveform

Similar tests were conducted to verify the boost mode of operation. The experimental waveforms of v_p, vs ,i_L corresponding to buck mode of operation ($m < 1$) are shown in Fig. 12(a). The converter was operated at a power level of 800 W. An output voltage regulation of 200V was attained for an input of 160V. ZVS in these cases are easily achieved as inferred from the fact that i_{L0} and i_{L1} are positive and



(a) (b)

Figure 2.13: Waveforms of bridge voltages (for reference) and the current through the primary bridge input capacitor(a) Experimental waveforms (b) Simulated waveforms



(a) (b)

Figure 2.14: Waveforms of bridge voltages (for reference) and the current through the output capacitor at the secondary bridge (a) Experimental waveforms (b) Simulated waveforms

large values. The corresponding simulation results for comparison are shown in Fig. 12(b).

Fig. 13 shows the experimental and simulated waveforms of the current through the input capacitor showing good match. Fig. 14 shows the waveforms of the current through the output capacitor. The negative pulse in the capacitor current equals to the load current in S-DAB, this feature is clearly seen in Fig. 14.

The analytical, simulated (under ideal and non-ideal conditions of switches) and

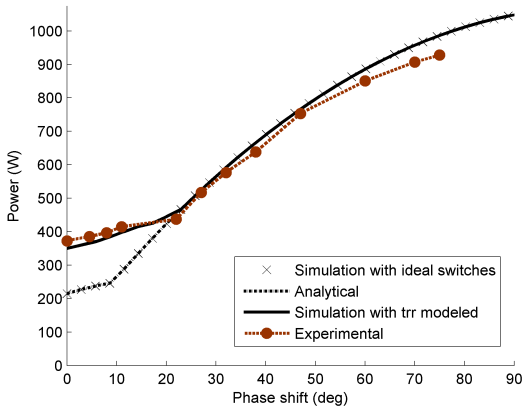


Figure 2.15: Comparison of analytical, simulated (ideal and non-ideal with t_{rr}) and experimental output power versus phase-shift ϕ curves for $m = 0.9$

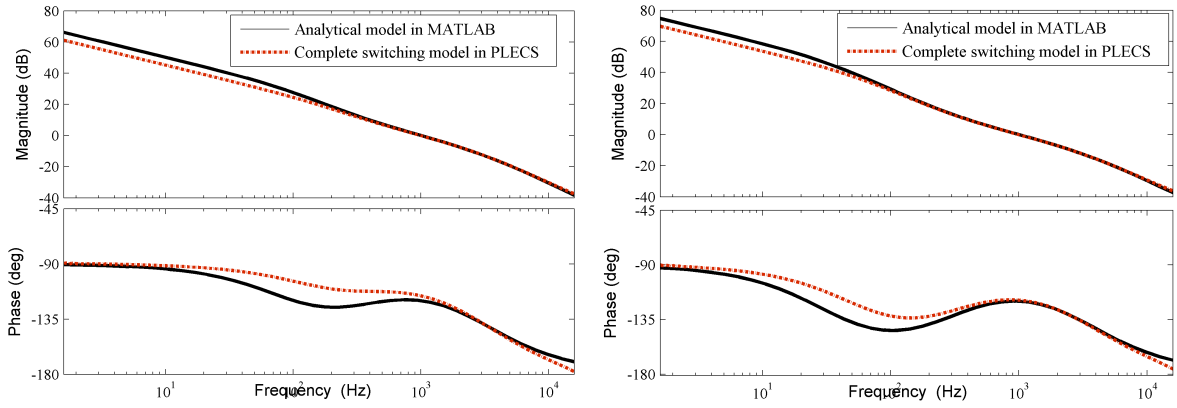
experimental output power versus phase-shift curves are depicted in Fig. 15 to validate the power flow expression given in (13). The experimental, analytical and simulation results match well under complete soft-switching region. When the operation begins to enter hard-switching region at low values of phase-shift and output power, the reverse recovery characteristics of the diodes across the secondary side MOSFETs begin to influence the power flow relationship by lengthening the duration of Interval 2 by the reverse recovery time of the diode (t_{rr}) and resulting in correspondingly higher output power. The t_{rr} of the diodes of MOSFET IPP65R280E6 was obtained as 300 ns from the datasheet and was modeled in PLECS simulation. The resulting curves from simulation match well with those obtained from the experimental prototype in both hard-switching and soft-switching regions, as seen from Fig. 15.

Fig .16(a), shows the loop gain of the S-DAB converter including the controller, $G_c(s)$ given in (22).

$$G_c(s) = \frac{0.0614s + 124.1}{5.112e^{-5}s^2 + s} \tag{2.22}$$

The loop gain plots are obtained by two different methods for validation 1) the black, solid curve is from the analytical small signal model given in (20) and the controller transfer function given in (22), and obtained using MATLAB, and 2) the dashed line

is obtained from the complete, switch model of S-DAB operating under closed-loop control of output voltage with the controller of (22), obtained using the 'small signal gain block of PLECS simulation tool. The operating conditions corresponding to both the loop gain plots are $V_{in} = 170$ V, $V_o = 200$ V, $m = 0.98$, $\phi = 48^0$ and a power level of 1 kW.



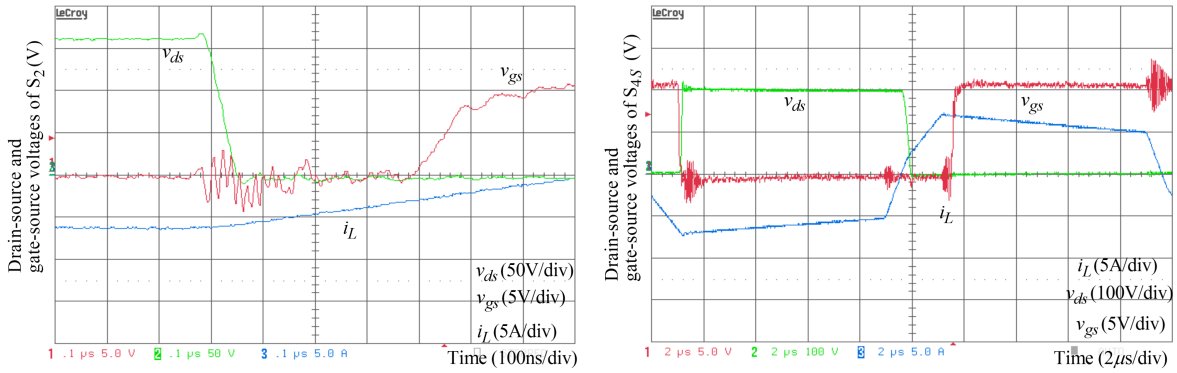
(a) (b)

Figure 2.16: Loop gain of S-DAB including the controller at 1 kW output power and $m = 0.98$ obtained using the analytical model and the full, switch-mode simulation model. (a) with an output capacitance of 15μF (b) with an output capacitance of 120μF

The analytical and switch model simulation match well in the frequency range of interest for controller design. The deviation observed at lower frequencies is due to the impact of perturbation in the output voltage, and therefore in the conversion ratio m, affecting the magnitude of the current source model in Fig. 9, especially for the low value of output capacitance (15μF) used. As the value of output capacitance is increased, the switch-mode simulation matches better with the analytical model as verified in the loop gain plots of Fig. 16 (b) under the same operating conditions but with a higher output capacitance of 120μF.

Fig. 17(a) shows the experimental gate-to-source and drain-to-source voltages during the turn-on transition of the MOSFET S_2 in HB1. As seen, the drain voltage

of S_2 falls to zero before the gate signal is applied, thereby demonstrating ZVS turn-on. Similarly, Fig. 17(b) shows the experimental gate-to-source and drain-to-source voltages of S_{4s} of HB2. As seen, the drain voltage reaches zero and the current taken up by the anti-parallel diode well before the gate voltage is triggered. These results were obtained at an input voltage of 150 V and at 800 W to validate the basic ZVS mechanism.



(a) (b)

Figure 2.17: (a) Drain-to-source and gate-to-source voltages demonstrating ZVS of switch S_2 in HB1 (b) Drain-to-source and gate-to-source voltages demonstrating ZVS of switch S_{4s} in HB2

2.4 Discussion and Possible Improvement to S-DAB

Among the popular isolated converters for unidirectional power flow applications, the phase-shift controlled full-bridge [48], [31] offers ZVS but with a restricted load range and requires large filter inductors. The series resonant converters [49], [50] require variable frequency operation with corresponding disadvantages such as larger filters designed for the lowest frequency of operation. The isolated boost converter [51] widely used in two-stage PV inverters is hard switched and hence not suitable at higher switching frequencies. The leakage inductance of the power transformer in the isolated boost converter poses challenges and loss penalty, and usually necessitates

the use of active clamps or snubber circuits. The advantage of S-DAB compared to the above solutions include ZVS over a wider range, the possibility of using just the leakage inductance of the transformer in the power transfer process, smaller overall filter requirement (with only capacitive filters), and the ability to operate seamlessly in the step-up and step-down modes. The disadvantage compared to the above unidirectional converters is the additional active switches on the secondary side of S-DAB.

The ZVS range of the S-DAB converter can be further improved by introducing PWM at the primary bridge (phase-shift control between its two legs) similar to such implementations in DAB as discussed in [45], [47]. By applying PWM at the primary bridge, the transformer size and the device conduction losses can also be lowered due to the reduction in the transformer rms current. The primary side full-bridge can be replaced by a half-bridge with two capacitors instead of the switches S_1 and S_2 for lower power applications. Additionally, rather than fixing the duty ratio at 50% the switches can be controlled with an asymmetrical duty cycle resulting in different characteristics [53]. Also, the proposed topology can be extended to multi-port configurations [37], [38], employing active bridges for the ports requiring bi-directional power flow and semi-active bridge for load ports that require only unidirectional power flow.

2.5 Summary

The S-DAB is well-suited for several applications requiring only unidirectional power flow such as the DC/DC stage of a PV power conversion system, chargers for electric vehicles, and other DC/DC converters requiring multiple, regulated outputs. It retains all the advantages of the popular DAB (except bidirectional power flow) including zero voltage switching, high power density, high efficiency and simple control. The important advantages of the proposed configuration over DAB are reduced num-

ber of switches with simpler gate drive, extended ZVS range allowing a wide range of variation in the input and/or output voltages, and reduction in the rms current through the output capacitor and hence smaller capacitor requirement. Some of the characteristics of S-DAB are similar to those obtainable using DAB with PWM control of the secondary side bridge, but here the advantages are obtained with reduced number of active switches. The operating principles, analysis, performance improvement and small-signal models have been presented in detail supported by simulation results. The analysis and performance have also been fully validated experimentally on a 50 kHz, 1 kW hardware prototype.

The S-DAB compares favorably with other popularly used isolated DC/DC converter topologies for a typical, unidirectional power flow applications. The method could thus be applied to automotive charging converters with high power density requirement.

Chapter 3

ZERO-VOLTAGE TRANSITION CONVERTER FOR BOOST-TYPE POWER FACTOR CORRECTION CIRCUIT

3.1 Introduction

On-board chargers are an important part of electric vehicles (EVs) as they impact the charging time and battery life. The battery charger is required to have high power density, high efficiency and reliability with low volume and cost. A typical on-board charger consists of an ac-dc power factor correction (PFC) stage followed by a dc-dc stage with galvanic isolation. A single stage isolated ac-dc approach has also been considered for cost-effective and power dense designs by eliminating the DC link [54, 55]. However, this is at the expense of increased filter requirements at the output due to double line frequency pulsation. A key component of a two-stage EV charger is the front-end PFC, as it ensures that the utility current drawn has low harmonic content to minimize power quality impact and maximizes the real power drawn from the grid by operating at unity power factor in order to comply with IEC 61000-3-2 and IEEE 519 standards. An extensive review of unidirectional and bidirectional single-phase PFC rectifier topologies with improved power quality is presented in [11], where the most popular and widely used topology is a boost-type PFC that consists of a diode bridge followed by a boost circuit. To achieve high power density and faster transient response, the boost PFC is pushed to operate at high switching frequencies. However, with increased frequency the output diode operating at DC-link voltage produces significant reverse-recovery losses that appear as additional turn-on losses along with switching related loss in the circuit [56].

Although the current trend is shifting towards wide band gap devices such as SiC and GaN, these devices may not yet be an economically viable solution for many applications. Soft switching topologies ease this transition by pushing the frequency and efficiency higher with lower cost silicon technology. Many circuit topologies have been investigated to achieve zero voltage switching (ZVS) in the power factor correction circuits (PFC) [57–63]. Among the major classification of soft-switched topologies, the proposed ZVT circuit falls in the category of PWM converters extended by auxiliary circuitry. The auxiliary circuit usually consists of an active switch and passive components that aid in briefly lowering the current through the main switch to zero for ZVS to occur. The ZVT concept was first presented in [58] where a switch, a diode and an inductor are implemented to achieve the loss-less switching transition. A main drawback of this converter is that the auxiliary switch is turned off while it is conducting current. These hard-switching losses offset the benefits gained with the auxiliary circuit. Converters in [57] and [64] use a dissipative snubber to limit this loss but the auxiliary switch still operates in a hard-switched condition.

The use of an auxiliary DC voltage source to ensure soft-switching for both the active devices by a self-resonance principle was first introduced in [60]. Authors improved upon this concept by replacing the voltage source with a transformer in [61], [65] and [66]. Variation in this self-resonance strategy was presented in [60] where the input of PFC's rectified voltage is used as the auxiliary DC voltage. This converter imposes a limitation on the input voltage to remain less than half the DC link voltage ($2V_{in} < V_o$). Moreover, the sharp current pulses generated during the ZVT operation is reflected as harmonic content in the input current and voltage waveforms. The soft-switching limitation can be eliminated by using synchronous switches where the top switch is kept on even after the auxiliary switch turns on to increase the energy stored in the auxiliary inductor [67–69]. However, for unidirectional power ap-

plications, typically the addition of an extra switch at full voltage and current rating to implement a synchronous boost configuration is not preferred due to cost constraints. [70], [71] and [63] have identified the issues for unidirectional converters and have proposed a family of self-commutated auxiliary circuits to overcome these problems. These converters achieve zero-current switching (ZCS) in the additional switch but experience higher voltage stresses in their passive components and moreover, the ZVT switch requires accurate timing control to prevent the resonant cycle continuing beyond the desired interval. The timing control would be more challenging at frequencies higher than 100kHz. Auxiliary Resonant Commutated Pole (ARCP) converter, Snubber Assisted Zero Voltage and Zero Current Transition (SAZZ), Zero Current Transition Quasi Zero Voltage Transition (ZCT-QZVT) [72], [73] are a few examples that have similar objectives in terms of sinking current from the pole slightly larger than pole inductor current in order to achieve ZVS.

This work proposes a boost-based PFC converter with a low-loss auxiliary circuit circumventing many of the above-mentioned drawbacks [74], [75]. Section 3.2 introduces the proposed ZVT scheme and presents detailed analysis of the various operating intervals over a complete switching period, as well as the operation of discharge circuit over a complete fundamental period. Based on this analysis, Section 3.3 provides a detailed design and optimization methodology for choosing the parameters of the ZVT circuit components. Section 3.4 presents extensive simulation and experimental results that validate the proposed concept, analysis and benefits of the topology on a 3.3kW/500kHz hardware prototype. Finally, the summary and conclusions are presented in Section 3.5.

3.2 Circuit Topology and Operation

The schematic of the proposed auxiliary ZVT circuit is shown in Fig. 3.1. A typical power factor correction circuit consists of a single phase diode bridge rectifier followed by a boost converter. The simple boost topology allows low-distortion in the input current, with almost unity power factor. To achieve ZVS condition during the turn-on of the main switch, the conduction of its body-diode prior to the turn-on gate signal is required. The proposed auxiliary circuitry to achieve this ZVS condition comprises of a switch S_{aux}, a fast switching diode D_{aux} and a resonant inductor L_{aux} connected in series. L_{aux} resonates with the capacitances C_{S1} and C_{D1}, across the main switch S_1 and diode D_1 respectively, just prior to the turn-on transition of S_1. These components are connected between the switch node and the mid-point of diode D_{dis} and capacitor C_{dis}, that aids in discharging the stored turn-on energy into the PFC circuit through the boost inductor. C_{dis} is large enough such that its voltage does not change appreciably within a switching period.

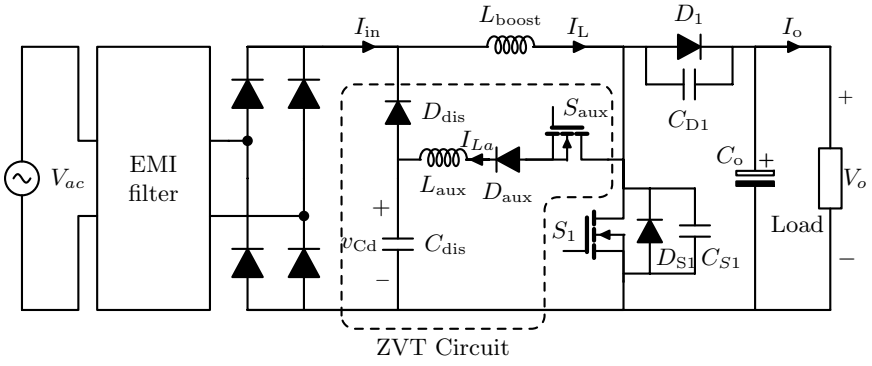


Figure 3.1: Circuit schematic of the proposed ZVT circuit

When the auxiliary switch is turned on, current through the main diode D_1 is softly diverted through the auxiliary circuit with a controlled di/dt that depends on the value of L_{aux} and voltage across C_{dis}. With the turn-off of D_1, L_{aux} resonates with C_{S1} and C_{D1} which brings down the voltage across S_1, v_{S1}. Once v_{S1} reaches

zero and the body diode D_{S1} conducts, switch S_1 is gated on at ZVS. The current through the resonant circuit falls linearly till it reaches zero. With D_{aux} preventing reverse current, S_{aux} turns off with zero current switching (ZCS) with its gate drive removed any time before the turn off of S_1. The linear and resonant components of the auxiliary inductor current charge C_{dis} slowly increasing its voltage. This energy is eventually discharged to the load through D_{dis} and the PFC circuit when the voltage v_{Cd} equals the instantaneous magnitude of the rectified input voltage. It may be noted that the operation and the control parameters of the boost converter are independent of the auxiliary circuit operation.

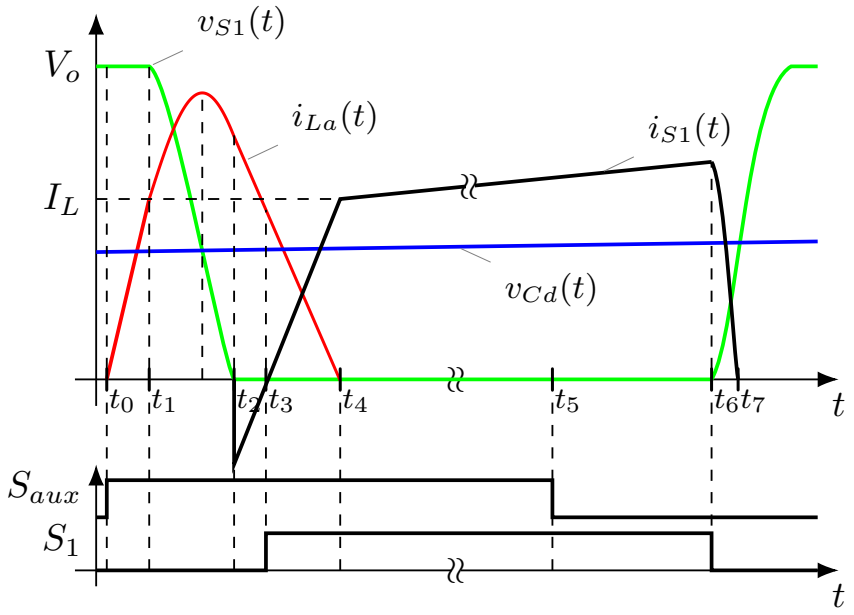
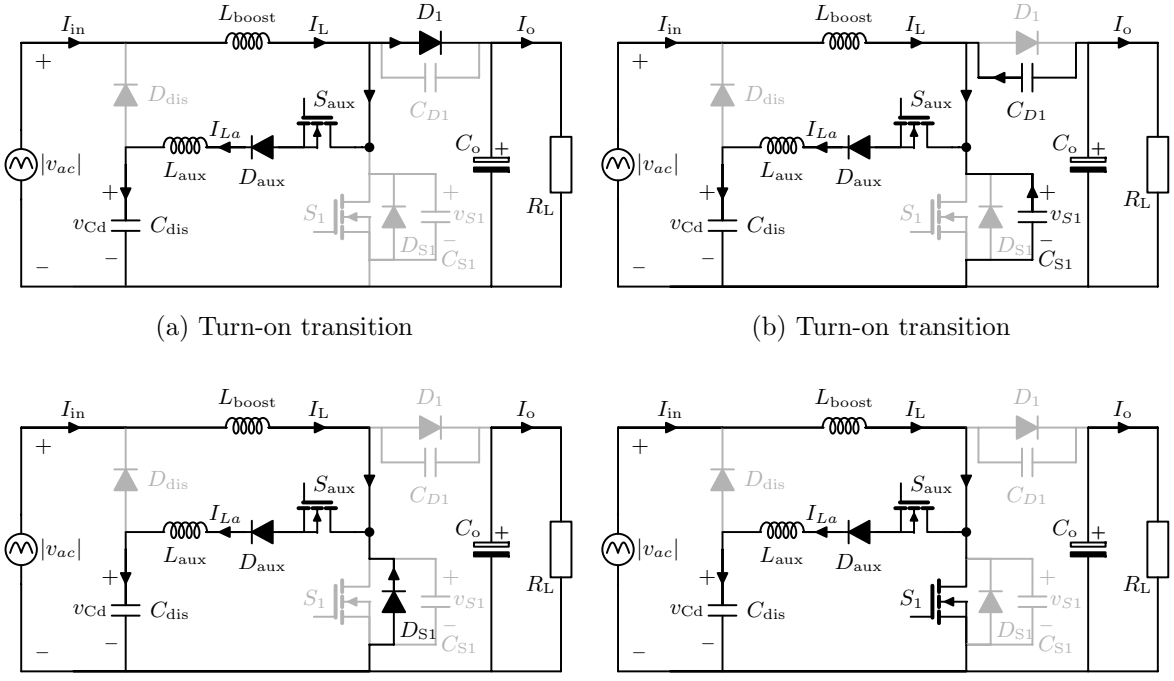


Figure 3.2: Current and voltage waveforms during ZVT circuit operation at switching frequency level

3.2.1 Operating Principle: Analysis over a Switching Period

To simplify the analysis, diode bridge shown in Fig. 3.1 can be replaced with a rectified voltage input. The turn-on resistances of the switches and threshold voltages of diodes and MOSFETs are neglected in this analysis. Four intervals of operation



(a) Turn-on transition

(b) Turn-on transition

(c) Turn-on transition

(d) Turn-on transition

Figure 3.3: Current Paths and Conducting Devices During Operation of PFC with ZVT circuit (a) Interval 1 (b) Interval 2 (c) Interval 3 (d) Interval 4 (Note that the Diode D_{dis} is OFF Over the Entire Switching Period as shown here During Part of the 60 Hz Cycle when $v_{Cd} <= |v_{ac}|$, and D_{dis} is ON Over the Entire Switching Period During the Remaining Part when $v_{Cd} >= |v_{ac}|$

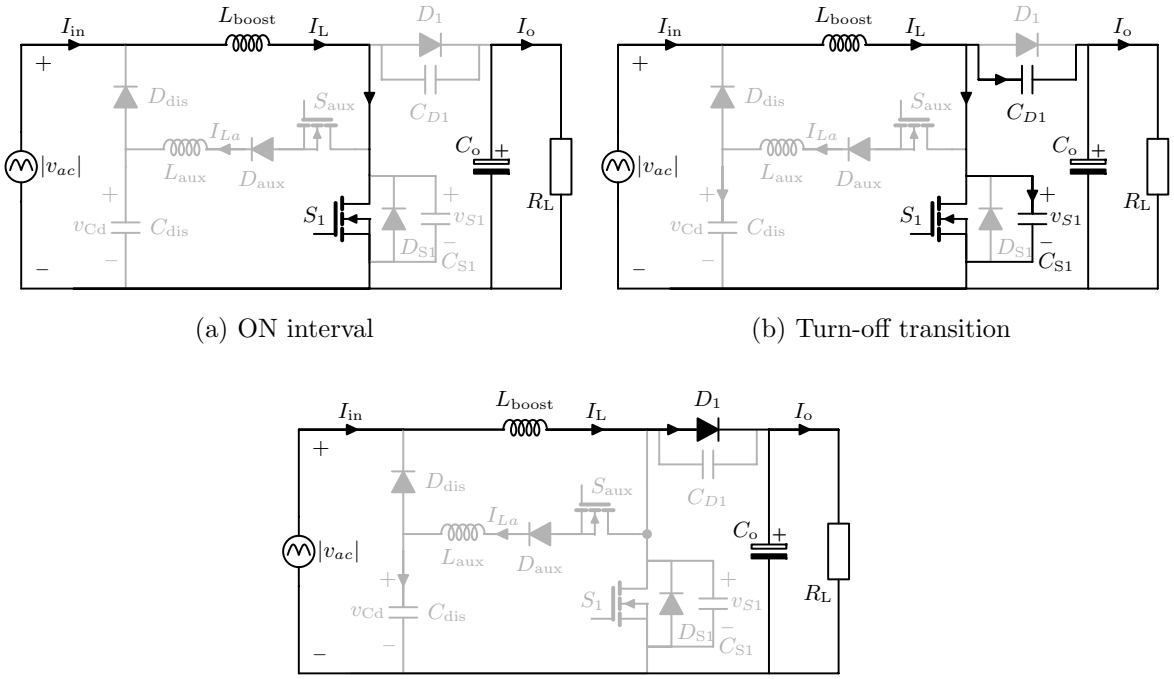
can be identified in the each switching cycle of this converter as illustrated in Fig. 3.3 and the ideal waveforms are shown Fig. 3.2.

Interval 1 ($t_0 - t_1$):

Interval 1 is initiated when the auxiliary switch S_{aux} is turned on prior to switch S_1 to redirect the flow of node current. The design of this time interval is discussed in detail in section 3.3.2. Current through the auxiliary inductor I_{La} rises linearly as given in (3.1) This interval ends when the auxiliary current reaches the instantaneous main inductor current.

$$Ldi/dt = V_o - V_{Cd} \tag{3.1}$$

Interval 2 ($t_1 - t_2$):



(a) ON interval

(b) Turn-off transition

(c) OFF interval

Figure 3.4: Current paths and conducting devices during operation of PFC with ZVT circuit (e) Interval 5 (f) Interval 6 (g) Interval.

The interval begins when the current i_{La} equals the main inductor current and D_1 turns off softly. A resonant cycle is initiated and the voltage of the pole v_{S1} swings from V_o to zero by the resonance between L_{aux} and the capacitance at the pole ($C_{eq} = C_{S1} + C_{D1}$), where C_{D1} is the junction capacitance of the main diode D_1. The expressions for i_{La} and v_{S1} are given in (3.2) and (3.3) respectively. The peak current in the resonant inductor depends on the magnitude of v_{Cd} in the given switching period, which changes from close to zero to about $V_o/2$ (see Section 3.3.1). The requirement to ensure ZVS operation is $v_{Cd} < V_o/2$. The range of peak current value is from $(V_o/2)/Z$ to V_o/Z and the range of the duration of the resonant interval is from

π/ω to π 2ω where characteristic impedance $Z = \sqrt{L_{aux}/C_{eq}}$ and resonant frequency.

$$i_{La}(t) = I_L + (V_o - V_{Cd}).sin(\omega t)/Z \tag{3.2}$$

$$v_{S1}(t) = V_o + (V_o - V_{Cd}).cos(\omega t) \tag{3.3}$$

Interval 3 ($t_2 - t_3$):

At t_2, voltage across the switch becomes zero and the current in C_{S1} transfers to the anti-parallel diode D_{S1}. With v_{S1} clamped at zero volts, i_{La} falls linearly as given in (3.4). This interval ends at t_3 when i_{La} reaches I_L. To ensure ZVS, S_1 needs to be gated on any time between t_2 and t_3, since after t_3 if S_1 is still not turned on, $I_L - i_{La}$ would recharge the capacitance at the pole, thus losing the soft-switching benefits.

$$i_{La}(t) = I_{La}(t_2) - \frac{V_{Cd}}{L}t \tag{3.4}$$

Interval 4 ($t_3 - t_4$):

The current through S_1 ($I_L - i_{La}$) is positive in this interval, with i_{La} still given by (3.4). This interval ends at t_4 when i_{La} reaches zero. With D_{aux} preventing reverse current, S_{aux} turns off naturally with zero current switching (ZCS). The gate drive for S_{aux} can be removed any time after t_4 and before the turn off of S_1. Note that for very low values of v_{Cd} and high peak current value of i_{La} the auxiliary inductor may not reach zero before turn off of S_1 and for such cases it is desirable to have a diode between S_{aux} source terminal and ground to provide a path for i_{La} if S_{aux} is turned off before i_{La} reaches zero.

Interval 4 ($t_4 - t_5$):

This is the main ON interval of the PFC with S_1 conducting I_L. The operation is identical to conventional boost PFC in this interval.

Interval 4 ($t_5 - t_7$):

This interval begins when S_1 gate drive is removed. Assuming that the switch current falls linearly in a duration of t_f , the switch voltage v_{S1} is given by (3.5). Larger values of C_{S1} limits the voltage rise when the switch current is falling, thereby significantly reducing the turn-off losses. Once the switch is fully off, the voltage rise is given by (3.6) and the interval ends when v_{S1} reaches V_o.

$$v_{S1}(t) = \frac{I_L t^2}{2C_{S1}t_f}, I_{S1}(t) = \frac{I_L t}{t_f} \tag{3.5}$$

$$v_{S1}(t) = \frac{I_L t}{C_{S1}} \tag{3.6}$$

Interval 4 ($t_5 - t_7$):

This is the main OFF interval of the PFC with D_1 conducting I_L. The operation is identical to conventional boost PFC in this interval.

3.2.2 Operating Principle: Analysis over a Complete Fundamental Period

The ZVT circuit operates for a short interval of time before and after the turn-on instant typically in the range of 40-100ns. At every switching cycle the capacitor C_{dis} is charged by a large current pulse i_{La}, gradually increasing its voltage. Once the voltage equals the rectified line voltage $|V_{ac}|$, the energy stored in C_{dis} is transferred to the load through the main inductor, thereby resetting its value to zero. Two intervals can be identified in the line frequency scale as seen in Fig. 3.5

Interval I ($T_0 - T_1$):

The voltage across the auxiliary capacitor increases gradually during this interval and the average current through the capacitor ($I_{La,avg}$) can be expressed as

$$i_{La,avg}(t) = \frac{1}{T}\int_0^T i_{La}(t)dt \tag{3.7}$$

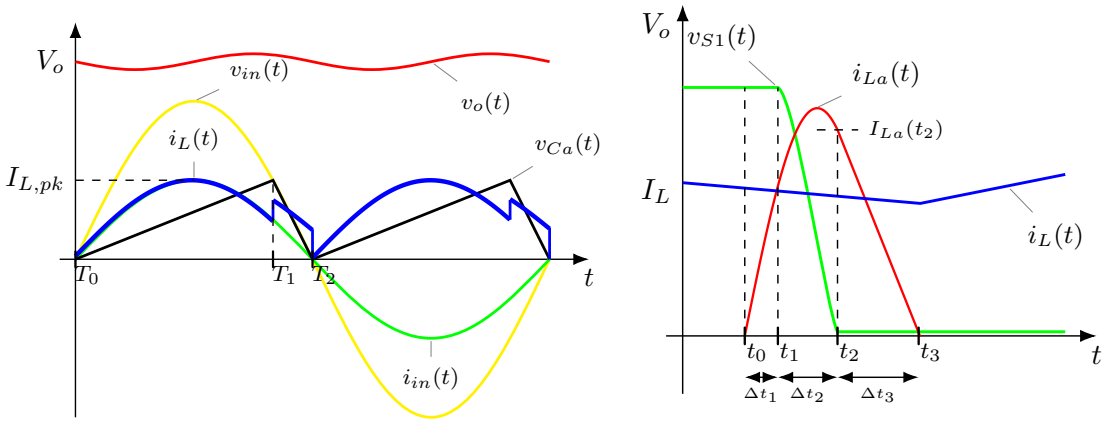


Figure 3.5: Current and voltage waveforms during ZVT circuit operation at (a) line frequency level (b) turn-on switching transition

where, T is the time period of the switching cycle. The time intervals Δt_1, Δt_2 and Δt_3 and are given by the expressions (3.8), (3.9) and (3.10) respectively.

$$\Delta t_{lin,rise} = \Delta t_1 = ZI_L/(\omega(V_o - V_{Cd})) \tag{3.8}$$

$$\Delta t_{res} = \Delta t_2 = \left(\pi - \cos^{-1}\left(\frac{V_{Ca}}{V_{dc} - V_{Ca}}\right)\right)/\omega \tag{3.9}$$

$$\Delta t_{lin,fall} = \Delta t_3 = ZI_{La}(t_2)/(\omega V_{Cd}) \tag{3.10}$$

$I_{La}(t_2)$ is the instantaneous value of the auxiliary current when the switch voltage V_{Cd} goes to zero. The resonant period is dependent on the instantaneous voltage difference across the inductor and changes along the line frequency cycle. The expression for the auxiliary inductor current during each of these intervals are given by the following expressions

$$\Delta t_{res} = \begin{cases} \left(\frac{V_o - V_{Cd}}{L}\right) t \\ I_L + \frac{(V_o - V_{Cd})sin(\omega t)}{Z} \\ I_{La}(t_2) - \frac{V_{Cd}}{L} t \end{cases} \tag{3.11}$$

The instantaneous value of the auxiliary inductor current at t_2 is expressed as

$$i_{La}(t_2) = I_L + \frac{V_o - V_{Cd} sin(\omega \Delta t_2)}{Z} \tag{3.12}$$

The average current can be obtained by substituting (3.8), (3.9), (3.10) and (3.11) in (3.7) and is expressed as

$$i_{La,avg}(t) = \frac{1}{T}\left[\left(\frac{V_o - V_{Cd}}{2L_{aux}}\Delta t_1^2 - \frac{V_{Cd}}{2L_{aux}}\Delta t_3^2\right) + I_L \Delta t_3 + I_L \Delta t_2 + \frac{V_o - V_{Cd}}{Z} sin(\omega \Delta t_2)\Delta t_3 + \frac{(V_o - V_{Cd})}{Z\omega}(1 - cos(\omega \Delta t_2))\right] \tag{3.13}$$

Interval II ($T_1 - T_2$):

The energy accumulated in capacitor C_{dis}, is discharged back into the DC link through the inductor during this interval. This period begins when $v_{Cd}(t)$ equals the instantaneous ac voltage of the PFC and follows the input voltage until it reaches zero. The current discharged from the capacitor I_{Cdis} in addition to the inductor current is given by the expression

$$i_{Cdis}(t) = V_{ac} C_{aux} \omega_1 cos(\omega_1 t), T_1 < t < T_2 \tag{3.14}$$

Where, ω_1 is the line frequency of the input voltage waveform and $\hat{V}_{ac}$ is the peak input voltage. The excess current appears as sharp rise in the inductor current during this operating period, that end when the auxiliary capacitor is completely discharged. It may be noted that this discharge current appears only in the inductor current and not in the input ac current which is controlled to be purely sinusoidal.

3.3 Design Considerations

3.3.1 Design of L_{aux} and C_{eq}

Optimum values for the auxiliary components L_{aux} and C_{eq} are desired as the energy stored in these components impact the losses in the auxiliary circuit. Capacitor

C_{eq} acts as the turn-off snubber of the main switch by delaying the voltage rise across the switch during the turn-off transition. The inductor L_{aux} controls the rate of current rise at the auxiliary switch during its turn-on. The assumptions made in this analysis are that the voltage fall across the auxiliary switch during its turn-on and the current fall in the main switch during its turn-off transitions are linear time functions determined by the semiconductor characteristics. The power dissipated in the main switch during the turn-off process is given by [76],

$$W_{S1,turn-off} = \int_0^{t_f} v_{S1}(t) i_{S1}(t) dt = \frac{I_{S1}^2 t_f^2}{24 C_{eq}} \tag{3.15}$$

Where, t_f is the linear fall time of the switch current. Similarly, the loss involved in the auxiliary switch during its turn-on is given by

$$W_{Saux,turn-on} = \frac{(V_o - V_{Cd})^2 t_r^2}{24 L_{aux}} \tag{3.16}$$

where, t_r is the linear fall time in voltage across switch S_{aux}. The total conduction loss in the auxiliary circuit can be expressed based on the RMS current in the circuit as

$$W_{cond} = I_{La,rms}^2 (R_{ds,on} + R_{L,aux}) + I_{La,avg} V_f \tag{3.17}$$

$$\begin{aligned} i_{La,rms}^2(t) = \frac{1}{T}\Bigg[& \int_{t_0}^{t_1} \left(\frac{(V_o - V_{Cd})t}{L} \right)^2 dt + \int_{t_1}^{t_2} \left(I_L + \frac{V_o - VCdsin(\omega t)}{Z} \right)^2 dt \\ & + \int_{t_2}^{t_3} \left(I_{La}(t_2) - \frac{V_{Cd}}{L} t \right)^2 dt \Bigg] \end{aligned} \tag{3.18}$$

Where $R_{ds,on}$ is the on state resistance of the switch, $R_{L,aux}$ is the series resistance of the inductor and V_f is diode forward voltage drop. The total loss in the analysis is given by the summation of (3.15),(3.16) and (3.18).

The optimal values of L_{aux} and C_{eq} based on the minimal losses is depicted in Fig. 3.6(a). The core loss in the auxiliary inductor is directly proportional to the peak flux density in the inductor core and is modeled as a constant loss, as variable core sizes

can be implemented. To capture this effect, a cost function with equal weight on loss and area product (core area x window area) was used to obtain the optimal L_{aux} and C_{eq} values as shown in Fig. 3.6(b). The optimization is performed for the worst case switching current condition in the entire line frequency cycle (peak boost inductor current), where C_{eq} is swept from intrinsic drain-source capacitance of the MOSFET (at 100 V) to five times this value. L_{aux} is swept from 50 nH to 700 nH. The reverse recovery characteristic of the main diode is one of the main reasons for switching related losses in the converter. The data sheet value of di/dt parameter of the diode determines the lower limit of the auxiliary inductance whereas, the upper limit is based on ZVT operation time. A value corresponding to duty ratio of 0.1, i.e., 200ns for 500 kHz operation was chosen as the maximum allowable time ($\Delta t_1 + \Delta t_2 + \Delta t_3$). It may be noted that the realization of complete ZVS is dictated by the condition $2V_{Cd} < V_o$, and is independent of the L_{aux} and C_{eq} values.

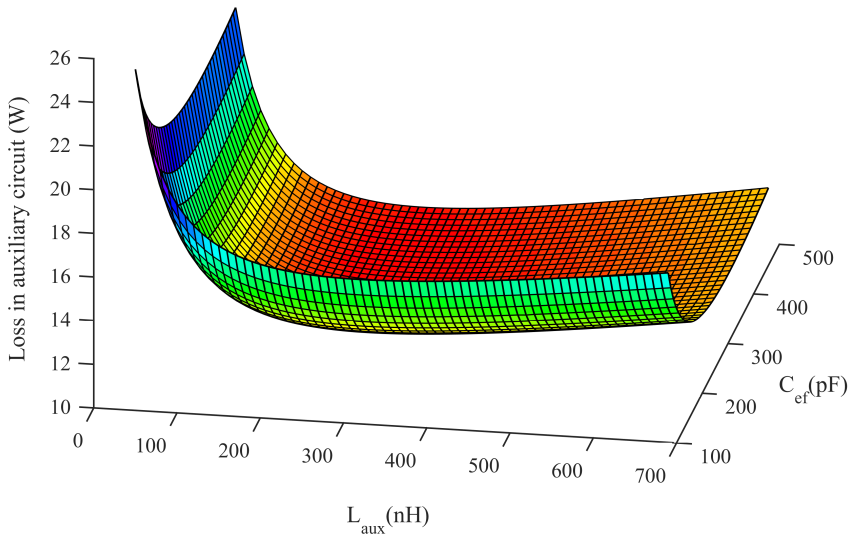


Figure 3.6: Optimal value of L_{aux} and C_{eq} based on minimum loss in the auxiliary circuit

3.3.2 Timing Selection

ZVS is realized when S_1 is turned on when its anti-parallel diode is conducting. The maximum allowable time delay t_{delay} between the turn-on of the switches S_{aux} and S_1, to prevent the recharging of the capacitance C_{eq} is the sum of the linear time rise and the quarter resonant period of the LC combination. The timing intervals of the resonant circuit comprises of the three segments, the linear rise time Δt_1 followed by the quarter resonant period Δt_2 and finally the linear fall time in current as shown in Fig. 3.2. The time delay required based on the equations (3.8), (3.9) and (3.10) are

$$t_{delay} = t_{lin,rise} + t_{res} = \frac{\pi\sqrt{L_{aux}C_{eq}}}{2} + \frac{L_{aux}i_L}{V_o - V_{Cd}} \tag{3.19}$$

An adaptive time delay dependent on the instantaneous main inductor current and the instantaneous auxiliary capacitor voltage can also be implemented to further reduce the losses incurred by the auxiliary circuit and avoid recharging of switch capacitance beyond the quarter resonant period.

A synchronous boost configuration of the PFC would further improve the ZVT performance as an additional degree of control, namely the turn-off time of the synchronous MOSFET relative to the turn-on of the auxiliary switch. By turning on the auxiliary switch before the synchronous switch turns off, the current through the synchronous switch can be controlled to reach a desired negative value, allowing the pre-charging of the auxiliary inductor to a higher magnitude before the resonant interval starts. With this available additional energy in the auxiliary inductor, the soft switching region can be extended beyond the $2V_{Cd} < V_o$ condition. However, the synchronous boost configuration was not considered in this work due to economic constraints in the design.

3.3.3 Switch Voltage and Current Stress

From Fig. 3.2 it can be seen that the voltage waveforms of the switches in this converter are square waves except during the turn-on and turn-off switching intervals. The time intervals between t_0 - t_4 are very short with respect to the switching cycle, so the operation of the new topology resembles the PFC during significant portion of the cycle. The power switch and the diode are not subjected to any additional voltage and current stresses and the soft-switching is attained with minimum penalty in conduction loss. Moreover, the maximum voltage stress seen by the auxiliary switch is the dc link voltage Vo and the rms current through this device is about 20% of the main switch at 500 kHz switching frequency.

3.4 Simulation and Experimental Results

The proposed topology is validated experimentally with a 3.3kW prototype. Experimental results verifying the simulation results from PLECS have been presented in this section.

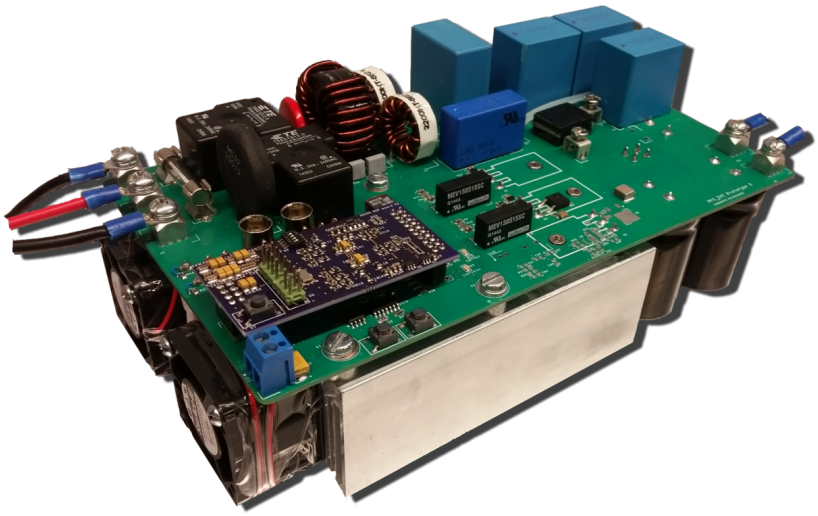


Figure 3.7: Photograph of the experimental prototype

3.4.1 Converter Design

The prototype seen in Fig. 6 has been designed for a rated power of 3.3kW, at a switching frequency of 500kHz. The specifications and the design parameters are shown in Table. 3.1. At the front end of the converter, relays along with inrush current limiters are implemented followed by EMI filters as this system is designed to comply with EMI standards in electric vehicles (EVs). A diode bridge rectifier provides the rectified voltage to the input of the boost converter. Infineon Si-MOSFET is selected to meet the desired voltage and current requirements for S1. A ceramic capacitance (C_{S1}) of 360 pF was incorporated in parallel to the main MOSFET, to reduce the turn-off losses, as per the design outlined in Section 3.3.1. A SiC schottky diode with a reverse blocking voltage of 650 volts was selected as the boost diode. The boost inductor was designed with the high frequency ripple component limited to 20% of the peak current. A Ferroxcube 3C93 MnZn ferrite core and Litz wire were used to construct the auxiliary inductor L_{aux}. The output capacitor needs to support twice-the-line-frequency current and meet any holdup time requirement. A capacitance of 1.9mF was chosen based on the voltage ripple requirement of $< 3\%$. The ZVT circuit comprises up of a low current SiC MOSFET in series with SiC schottky diode C3D06065E and 300nH, 3F3 ferrite core auxiliary inductor.

A closed loop current controller along with over-voltage and over-current protection schemes was implemented on a Texas Instruments^{TM} TMS320F28335 digital signal processor (DSP) control card. This DSP has a 12-bit sequential ADC for sampling multiple analog signals and also has six enhanced PWM modules (ePWM), for high resolution signals. The ZVT circuit requires accurate time delays in the order of few tens of nanoseconds for its operation and the DSP is selected to handle this demand.

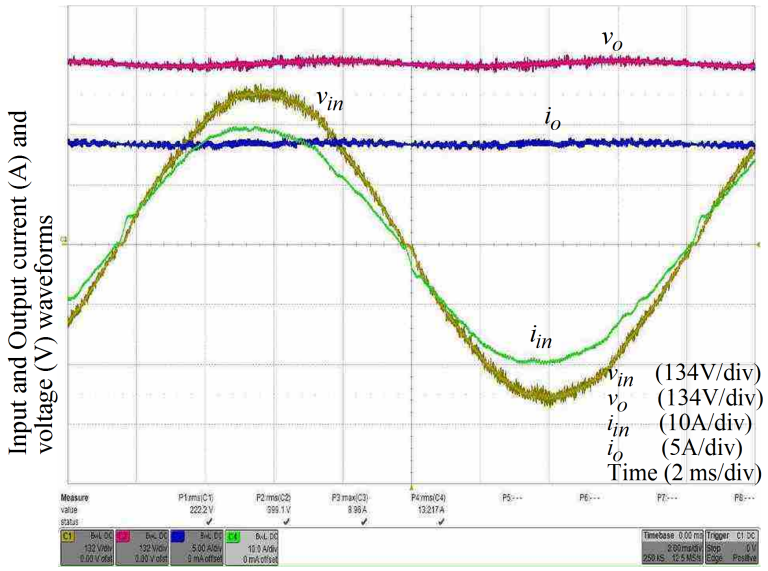
Table 3.1: Target specifications and selected design

Parameters	Symbol	Specifications
Rated power	P	3300W
Input votlage	V_{in}	240V
Output voltage	V_o	400V
Frequency	f	500 kHz
Boost inductance	L_{boost}	60 μH
Output capacitance	C_o	1.9 mF
Auxiliary capacitance	C_{dis}	30 μF
Additional S_1 capacitance	C_{S1}	360 pF
Auxiliary inductor	L_{aux}	300 nH

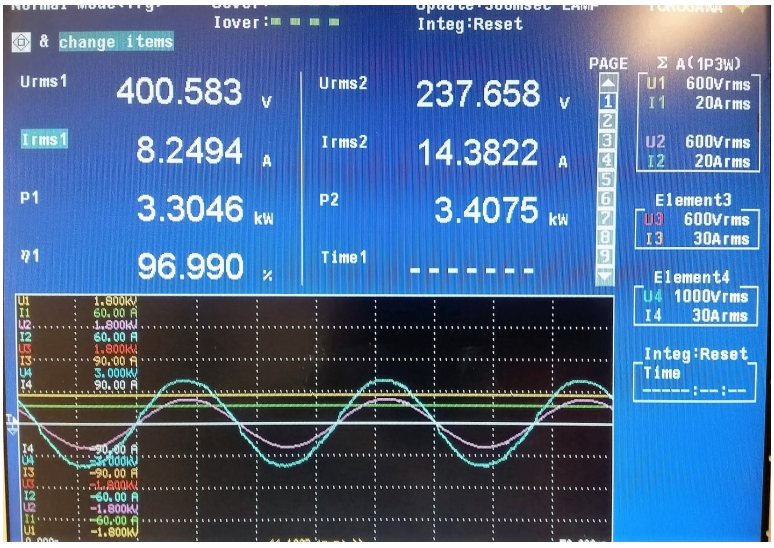
3.4.2 Experimental Waveforms and Comparison with Simulation

Fig. 3.8(a) shows the operating waveforms of the PFC with the ZVT circuit at a power level of 3300W. The output voltage of the converter was regulated at 400 volts with a peak input current of 20A at 240Vrms. Fig. 3.8(b) shows the efficiency reading on the power analyzer, YOKOGAWA WT3000 with the converter operating at 500kHz.

Fig. 3.9(a) depicts the salient internal simulation waveforms of the converter related to the discharge of the energy processed in the ZVT circuit to the output (through the discharge network and main PFC), that matches well with the experiments as shown in Fig. 3.9(b). The voltage across the capacitor C_{dis}, shown in red, varies at twice the line frequency resetting once its voltage reaches the absolute instantaneous value of the input voltage. The energy stored in the capacitor is fed back into the converter through diode D_{dis} and this can be observed as the increased current during part of the cycle in the boost inductor that matches closely with simu-



(a)

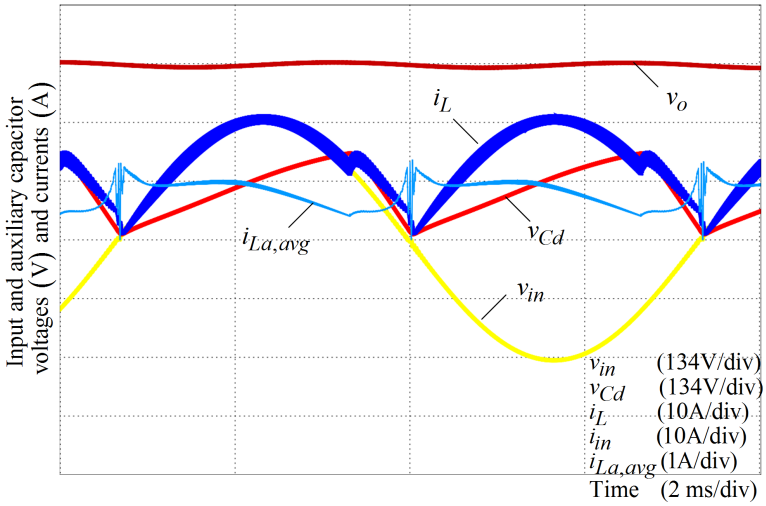


(b)

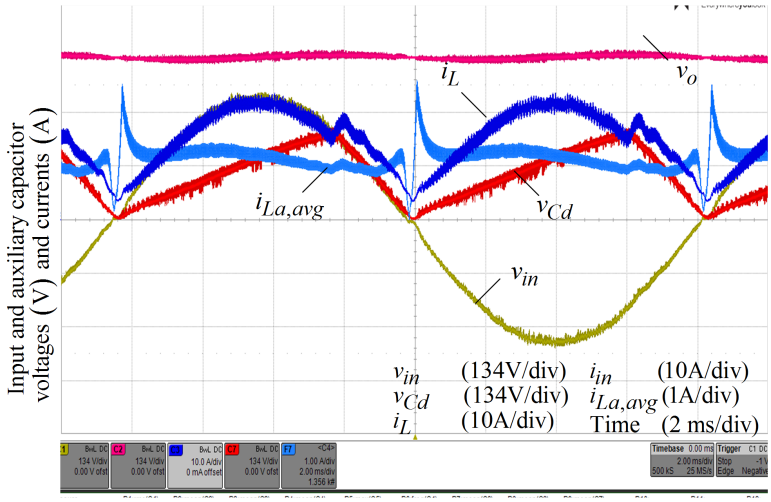
Figure 3.8: (a) Measured input current (green), input voltage (yellow), output voltage (red) and output current (blue) waveforms with ZVT circuit at 3.3kW (Current THD: 3.29%) (b) Efficiency measurements on the PFC converter with ZVT at 3.3kW and 500 kHz

lation. Also, note that the average current through the auxiliary circuit is low across the line frequency cycle.

Fig. 3.10(b) shows the experimental results of the gate-to-source and drain-to-



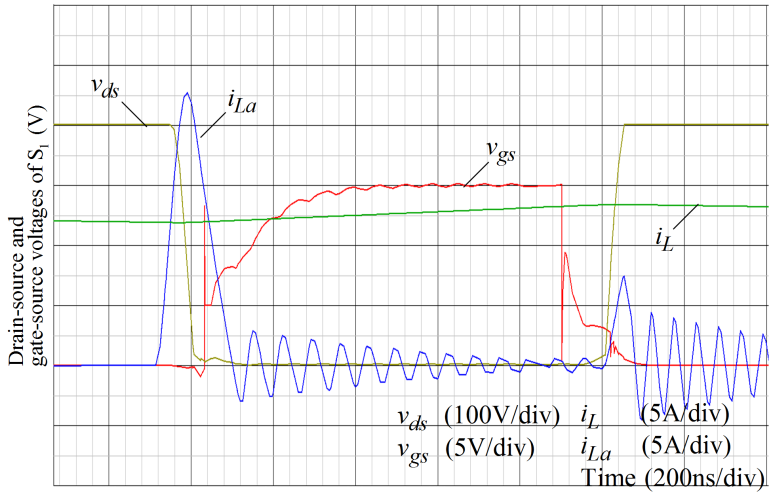
(a)



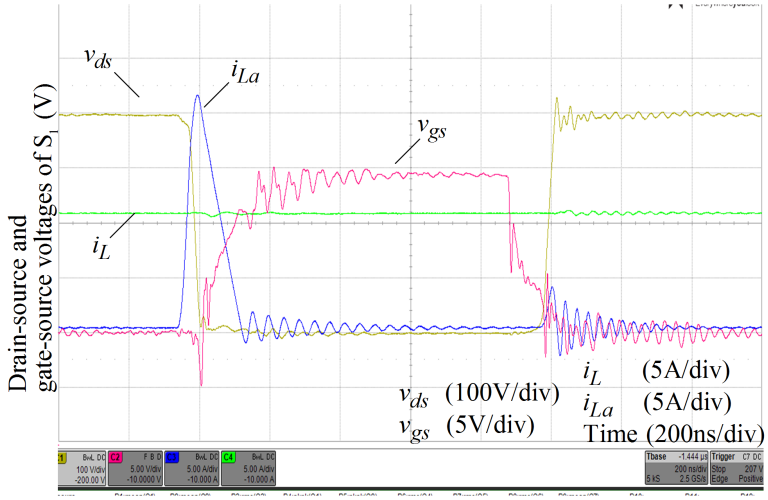
(b)

Figure 3.9: Input (v_{in}) and auxiliary capacitor (v_{Cd}) voltage waveforms along with inductor current (i_L) and cycle-by-cycle average value of auxiliary inductor ($I_{La,avg}$) (a) simulated waveforms (b) measured waveforms.

source voltages during the turn-on transition of the MOSFET S_1. As seen, the drain voltage of S_1 falls to zero before the gate signal is applied, thereby demonstrating ZVS turn-on. These results were obtained at a DC link voltage of 400V and at 2000W to validate the basic ZVS mechanism. It matches well with the simulation results in Fig. 3.10(a) that shows the waveforms of S_1 obtained from SIMPLIS by incorporating



(a)

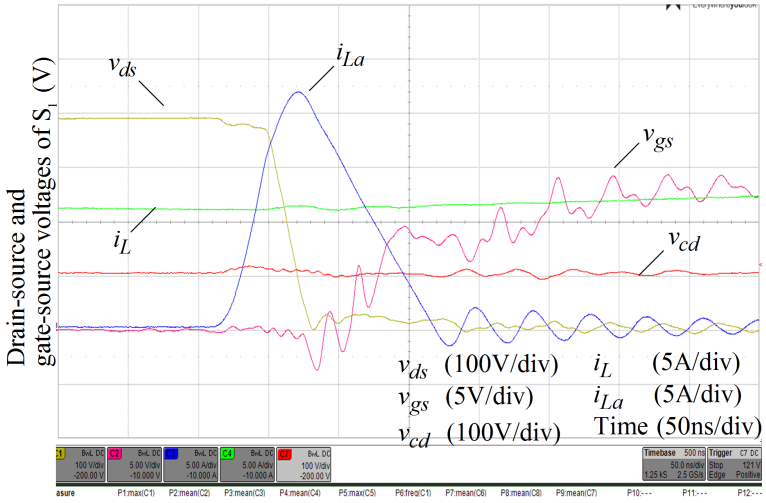


(b)

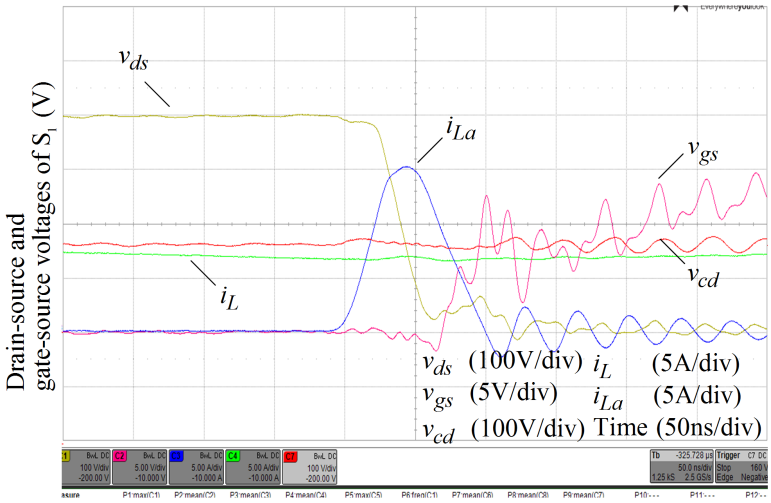
Figure 3.10: Waveforms of S_1 and inductor currents, drain-to-source voltage (yellow), gate-to-source voltage (maroon), auxiliary inductor current (blue), main inductor current (green) (a) Simulated waveforms with non-idealities (b) Measured waveforms.

the detailed Spice model of IPW65R100CFDA CoolMOS used in the hardware. The drain voltage reaches zero and the current taken up by the anti-parallel diode before the gate voltage is triggered. Fig. 3.11(a) and (b) show the waveforms corresponding to the turn-on transitions during the peak input current and auxiliary voltage value respectively. In Fig. 3.11(a) the flat region in the gate voltage v_{gs} just after i_{La} falls

below iL is due to the channel current rising at a constant and relatively high rate (same as the rate at which i_{La} falls) through the large parasitic inductance of the source lead of the TO-247 package. The gate voltage in this region is dominated by the resulting Ldi/dt drop in the parasitic lead inductance.



(a)



(b)

Figure 3.11: Waveforms of S_1 and inductor currents, drain-to-source voltage (yellow), gate-to-source voltage (maroon), auxiliary inductor current (blue), main inductor current (green) (a) Simulated waveforms with non-idealities (b) Measured waveforms.

Fig. 3.11(b) corresponds to the worst-case condition for ZVS as the v_{Cd} voltage

is at its maximum. With ideal components complete ZVS should be achieved for $v_{Cd} < V_o/2$, however, due to the relatively large series resistance in the inductor and auxiliary switch and diode, the resonance is significantly damped resulting in a low but non-zero voltage at turn-on instant.

Fig. 3.12 shows the auxiliary switch current, and drain-source and gate-source voltages. As seen, the current turns-off naturally (due to D_{aux} blocking negative current) with the gate voltage still applied demonstrating ZCS operation. The voltage across the auxiliary switch rises only when the main switch S_1 is turned-off. L_{aux} resonates with C_{eq} during this transition leading to the ringing observed in Fig. 3.12. During turn-on transition of S_{aux}, the inductor L_{aux} limits the rise of channel current as the drain-source voltages falls, hence significantly reducing the turn-on losses.

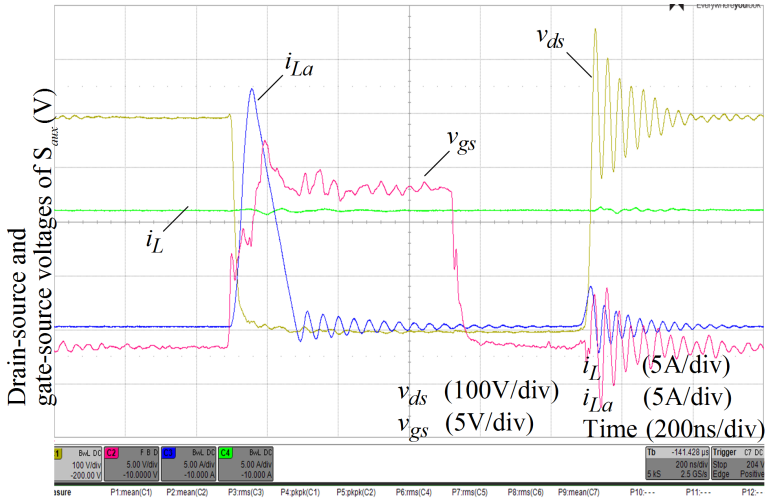


Figure 3.12: Waveforms of auxiliary switch S_{aux}, drain-to-source voltage (yellow), gate-to-source voltage (maroon), switch current (blue), main inductor current (green) from experimental prototype.

The total loss breakdown of the PFC, using an analytical loss model, at both hard-switching (ZVT circuit disabled) and soft-switching conditions at 3.3kW is depicted in Fig. 3.13. The reverse recovery loss in the SiC diode is negligible and hence was not considered in this analysis. The total loss predicted from simulation/analysis match well with those obtained from the experimental prototype as seen in Fig. 3.13.

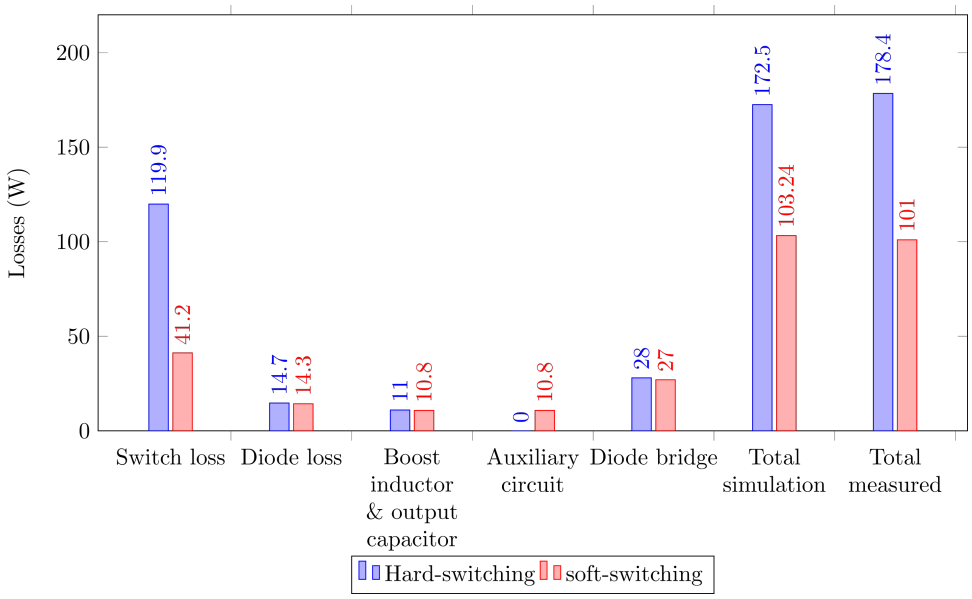


Figure 3.13: Loss breakdown of the PFC converter with and without the ZVT circuit corresponding to operation at 3.3kW/ 500kHz.

The efficiency curves of the converter with and without the ZVT are shown in Fig. 3.14. The measurements were obtained from YOKOGAWA WT3000 power analyzer and the total losses are reduced from 178W in the hard-switching case to 101W in the proposed scheme (corresponding to 43.3% loss reduction). The resulting overall efficiency improvement at full load is 2.08%. Also, the efficiency with the ZVT scheme remains high over a wide range of load conditions.

3.5 Summary

In this chapter, an efficient zero voltage transition technique is proposed for a boost-type PFC converter which requires high frequency of operation. The operating principle and design requirements of the ZVT circuit are presented. Both the main and the auxiliary switches achieve ZVS and ZCS respectively. The analysis and performance of this system has been validated experimentally using a 3.3 kW /500 kHz prototype and simulation results showing the internal waveforms of the converter has been presented in this chapter. The auxiliary circuit improves the overall efficiency

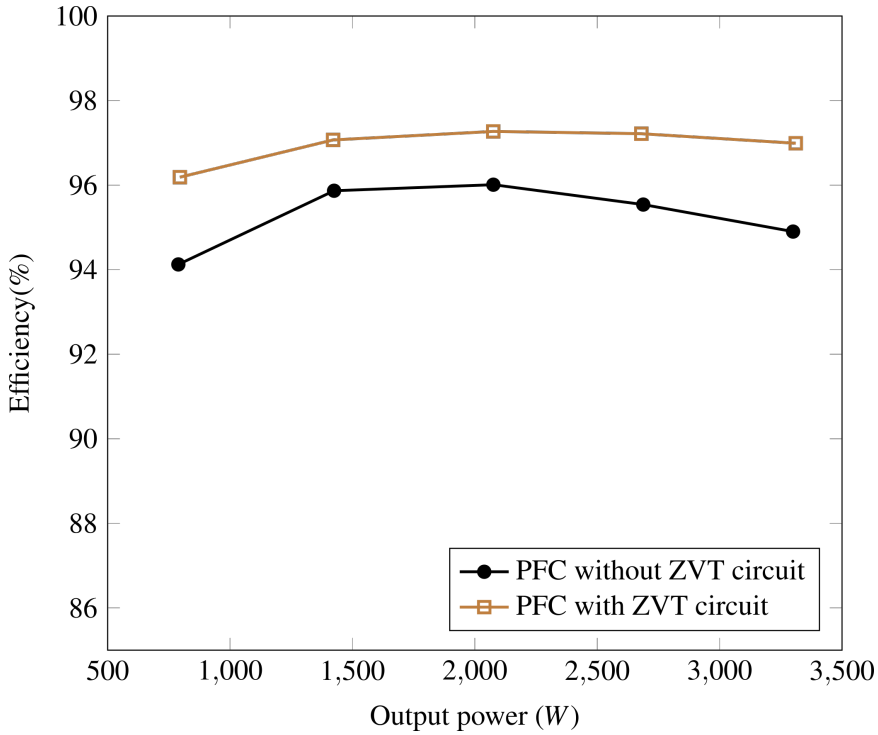


Figure 3.14: Efficiency of the PFC converter with and without the auxiliary ZVT circuit.

by 2% reducing the total losses by 41% compared to hard-switched operation near full load. At the rated output power, $P_{out} = 3.3kW$ and at the nominal input voltage, the efficiency obtained from the high frequency operation is $> 95\%$. Moreover, the auxiliary circuit has low part count that enables a compact and efficient design making the proposed solution an attractive one to achieve the target specifications.

Chapter 4

IMPROVED FEATURES ON ZVT CIRCUIT FOR BOOST-TYPE PFC CONVERTER

4.1 Introduction

A simple way to implement a low loss auxiliary circuit at the switching node was demonstrated in Chapter. 3. The proposed ZVT scheme achieves switching loss reduction of PFC without increasing voltage/current stress of switches and therefore suitable for high power applications. In proposed PFC with ZVT topology the auxiliary capacitor C_{dis} limits the peak input voltage across it to remain less than half the DC link voltage ($2V_{in} < V_{dc}$). The sharp current pulsation generated during the ZVT operation is absorbed by this capacitor and prevents the ingress of harmonic content into the input current and voltage waveforms. The capacitor used in this design is a bulky film capacitor rated at $30\mu F$ to achieve desirable voltage levels. This chapter presents modifications to ZVT-PWM topology to further reduce the footprint of C_{dis} and also reduce the losses in the auxiliary circuit. Utilizing an integrated magnetic structure for the boost and the auxiliary inductor reduces the current requirement in the auxiliary circuit depending on the turns ratio. Moreover, an improved configuration of the proposed ZVT circuit where the energy accumulated in C_{dis} is transferred to the output of PFC through essentially a boost dc-dc converter. In general, the additional boost converter would be a drawback in terms of cost, size and losses. However, it is a viable solution for the charger application where the PFC is followed by another isolated dc-dc converter for battery management, typically a phase-shifted full-bridge, dual-active bridge or a full bridge LLC topology. The simulation and the

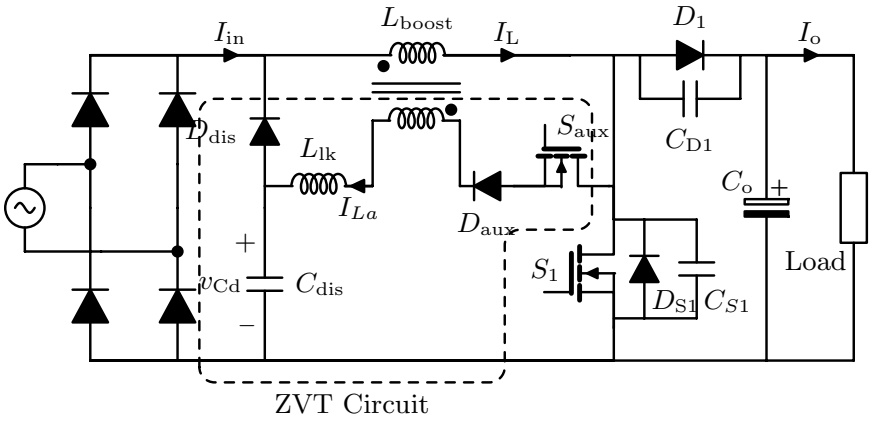
experimental verification of these modifications are shown in this chapter using a 3.3 kW/ 500 kHz PFC.

4.2 PFC with Coupled Auxiliary ZVT Circuit

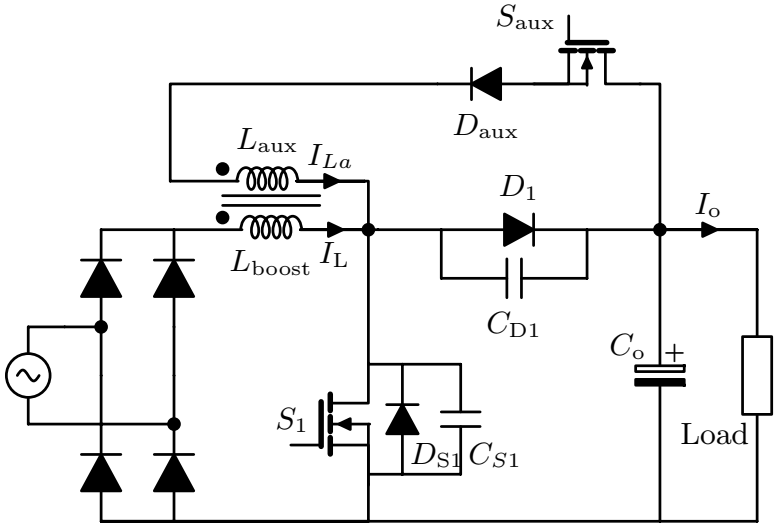
4.2.1 Analysis of Coupled ZVT Circuit

Several variations fo the ZVT circuit using integrated magnetic structures are possible where the auxiliary inductor is coupled with the main boost inductor [74]. Two such coupled inductor topologies are shown in Fig. 4.1 which are promising based on simulation results. In both these configurations the current through the auxiliary inductor winding can be reduced, and therefore the size of the discharge circuit can be made smaller in the case of Fig. 4.1(a), and the capacitor can be eliminated in the case of Fig. 4.1(b). This comes at the expense of increased voltage rating for the auxiliary switch. Detailed analysis and results for the first variations is presented in this section.

The PFC circuit consists of a single phase diode bridge rectifier followed by boost converter. The additional circuitry required for ZVT comprises of a switch S_{aux}, fast switching diode D_{aux} and resonant inductor L_{aux} connected in series across the main inductor L_{boost}. These components are connected between the switch node and the mid-point of diode D_{dis} and C_{dis}. By magnetically coupling the inductors the current in auxiliary circuit is reduced. Polarity of the primary (boost main inductor) and the secondary winding (auxiliary inductor) is designed in such a way that increasing the secondary winding current decreases the current at the primary. This mechanism in-turn reduces the conduction losses of switch S_{aux} and the size of the auxiliary capacitance required as the current pulsation due to the ZVT operation have lower peak value in comparison with discrete inductor. In counterpart, it also increases the



(a)



(b)

Figure 4.1: Schematic of the PFC (a) with coupled ZVT circuit (b) coupled ZVT connected across top device.

voltage across the auxiliary switch, increasing its turn-on capacitive losses. With an optimal choice of turns ratio, the total losses in the auxiliary switch can be minimized. With a coupled inductor structure the leakage inductance of this element L_{lk} functions similar to the discrete auxiliary inductor and the schematic of the patented auxiliary ZVT circuit and its modification is shown in Fig. 4.1(a). All the inductors are built in the same magnetic core and this eliminates the necessity of an additional core and

allows for a compact design.

4.2.2 Operating Principle

The turn-on resistances of the switches and threshold voltages of diodes and MOSFETs are neglected in this analysis. The coupled inductor is modeled as a controlled current source and a voltage source at the primary and secondary respectively. Four intervals of operation can be identified in the each switching cycle of this converter as illustrated in Fig. 4.2(a) and the ideal line frequency waveforms are shown Fig. 4.2(b).

Interval 1 ($t_0 - t_1$): Switch S_2 is turned on prior to S_1 to redirect the flow of node current. Current I_{La} through the coupled inductor secondary rises linearly as the difference in voltage across L_{lk} is $(V_o - V_{Cd})$, where V_{Cd} is the voltage across the capacitor C_{dis}. Simultaneously, the current in the main inductor I_L decreases due to the coupled inductor effect as shown in Fig. 4.2. This interval ends when the current at the switching node goes to zero.

Interval 2 ($t_1 - t_2$): A resonant cycle is initiated when the node current reaches zero. Pole voltage v_{S1} swings from V_o to 0 by the resonance between L_{lk} and the capacitance at the switch node $(C_{S1} + C_D)$. Main switch S_1 is turned on at negative device current, as beyond this i_{La} reverses polarity and recharges the capacitance at the pole, thus losing the loss benefits.

Interval 3 ($t_2 - t_3$): The leakage inductance experiences self-commutation and its current gradually reduces to zero as C_{dis} appears as a voltage source reverse biasing the inductor thereby causing ZCS turn-off at S_{aux}.

Interval 4 ($t_4 - t_6$): The gate turn-off signal for S_2 is triggered at t_4 and the t_5 is the turn-off time of the switch S_1. The turn-off time of the auxiliary switch is not critical and is ensured to be triggered before the main switch turn-off. The turn-off

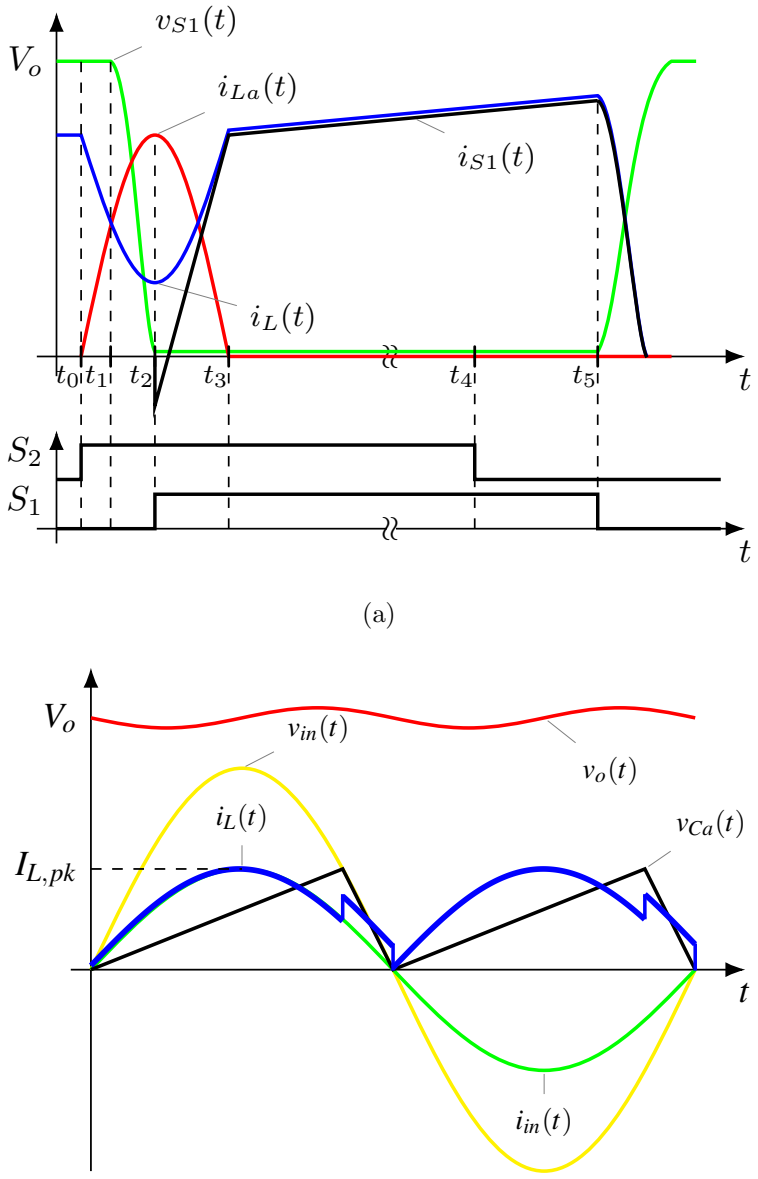


Figure 4.2: Current and voltage waveforms during ZVT circuit operation (a) switching level transition (b) average line frequency

losses can be further minimized by adding capacitors across the switch.

At every switching cycle the capacitor C_{dis} is charged by large current pulses i_{La} gradually increasing its voltage until input line voltage V_{in}, where the energy stored in C_{dis} is transferred to the load through the D_{dis}.

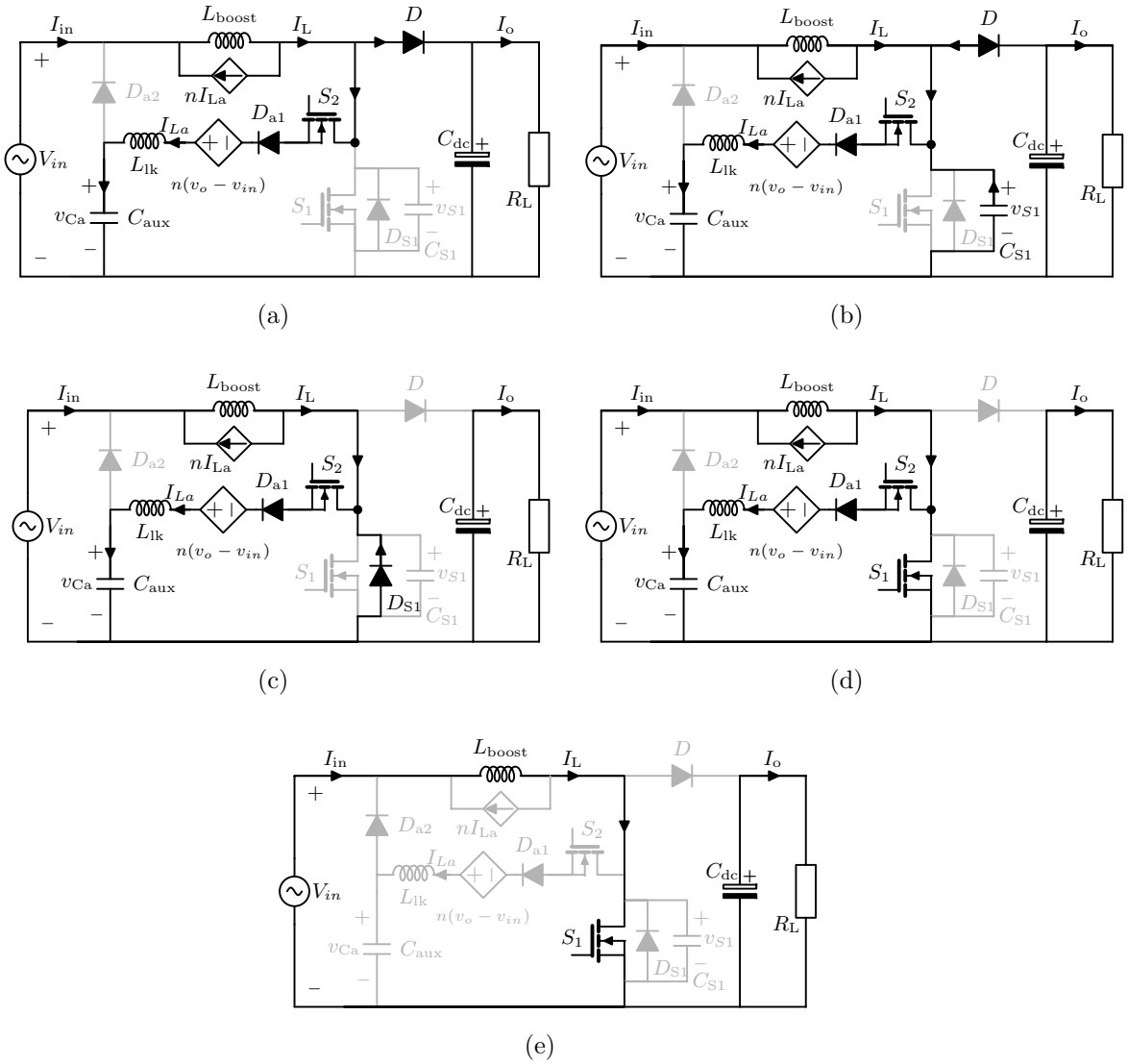


Figure 4.3: Current paths and conducting devices during operation of PFC with ZVT circuit (a) Interval 1 (b) Interval 2 (c) Interval 3 (d) Interval 4

4.2.3 Design Considerations

Design of L_{aux} and C_{S1}:

Optimum values of auxiliary components L_{lk} and C_{S1} are based on the energy stored thats is directly proportional to the conduction losses in the circuit. Capacitor C_{S1} acts as the turn-off snubber of S_1 and the leakage inductor L_{lk} limits the current

rise in the auxiliary switch during its turn-on. The optimal values based on [77] are $C_{s1}(\text{opt}) = I_{s1}t_f/(\sqrt{12}V_o)$ and $L_{lk}(\text{opt}) = (V_o - V_{Cd})t_r/(\sqrt{12}I_L)$. The requirement for ZVS is independent of the L_{aux} and C_{S1} values, but are determined by the relation $2V_{Cd} < V_o$.

Timing selection:

The optimal time delay between the turn-on of switches S_{aux} and S_1, to prevent the recharging of the capacitance C_{S1} is the sum of both linear time rise and the quarter resonant period of the LC combination.

$$t_{delay} = t_{lin,rise} + t_{res} \tag{4.1}$$

$$t_{lin,rise} = \frac{n}{n+1}\frac{ZI_L}{(\omega(V_o - V_{Cd} + n(V_o - V_{in})))} \tag{4.2}$$

$$t_{res} = \left[\pi - \frac{1}{\omega}cos^{-1}\frac{V_{Cd}}{V_o - V_{Cd}}\right] \tag{4.3}$$

An adaptive time delay can also be implemented to control the turn-on timings of the main switch to further reduce the losses incurred by the auxiliary circuit and recharging of switch capacitance beyond the quarter resonant period.

4.2.4 Switch Voltage and Current Stresses

From Fig. 4.2 it can be seen that the voltage waveforms of the switches in this converter are square waves except during the turn-on and turn-off switching intervals. The time between $t_0 - t_3$ is short with respect to the switching cycle, so the operation resembles the PFC during significant portion of the cycle. The main switch S_1 and D have no additional stresses whereas, the voltage stress seen by the auxiliary switch is the dc link voltage $V_o - v_{cd} + n(V_o - v_{in})$ and the rms current through this device is reduced significantly through coupling. An optimal value of turn ratio to minimize

the total losses of the converter in comparison to the discrete inductor variation would be performed as a future work.

4.3 Coupled Inductor Results

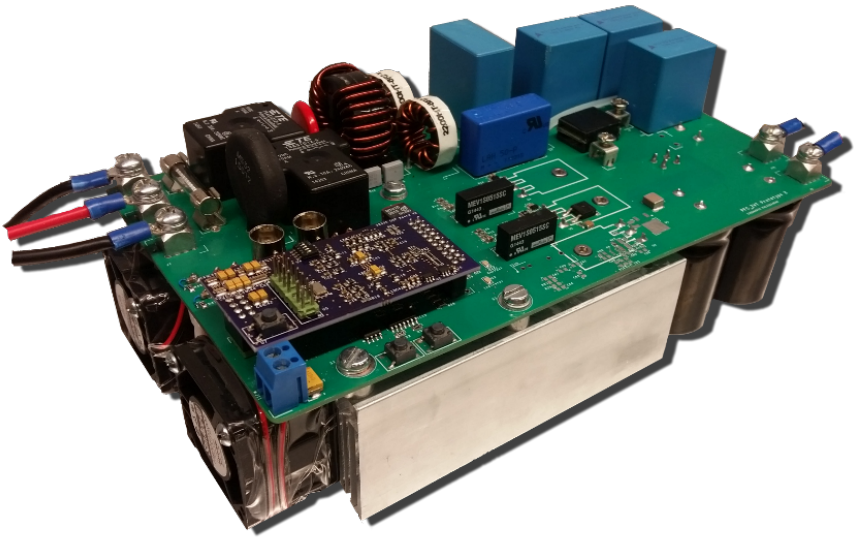
The proposed topology is validated experimentally with a 3.3kW prototype. The prototype seen in Fig. 4.5 is designed for 3.3 kW/ 500 kHz and the specifications are shown in Table 4.1.

Table 4.1: Boost PFC with integrated magnetic: design parameters

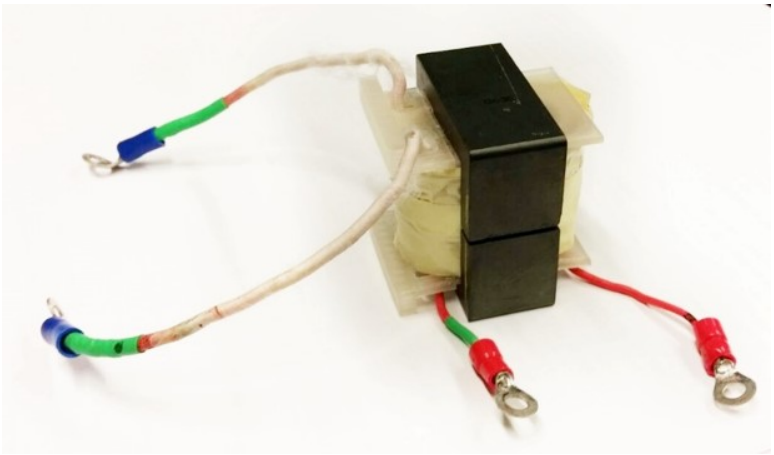
Parameters	Symbol	Specifications
Rated power	P	3300W
Input/Output voltage	V_{in}, V_o	240V/ 400V
Frequency	f	500 kHz
Boost/ leakage inductance	L_{boost}, L_{lk}	60 μH/ 0.8μH
Output capacitance	C_o	1.9 mF
Auxiliary capacitance	C_{dis}	10 μF

Infineon Si-MOSFETs were selected to meet the desired voltage and current requirements for S_1. SiC schottky diode with a reverse blocking voltage of 650 volts was selected as the boost diode. Ceramic capacitance (C_{S1}) of 480 pF was incorporated in parallel to the switching device, to reduce the turn-off losses. The inductor comprises of Ferroxcube 3C93 MnZn core and litz wire for both the primary and secondary turns. The ZVT circuit comprises of Cree SiC MOSFET in series with SiC schottky diode and secondary winding. The ZVT circuit requires accurate time delays for its operation and the TI TMS32028335 micro-processor is selected to handle this demand.

Fig. 4.5(a) shows the operating waveforms of the PFC with the ZVT circuit



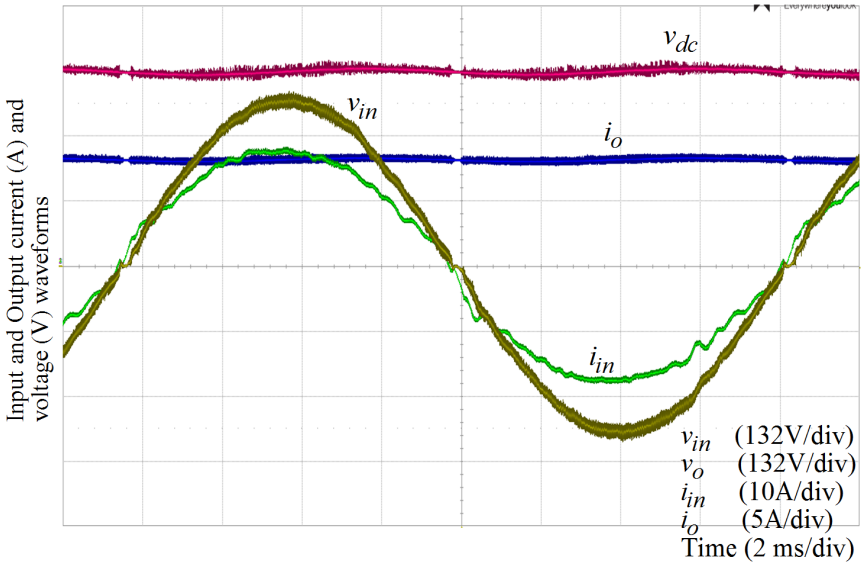
(a)



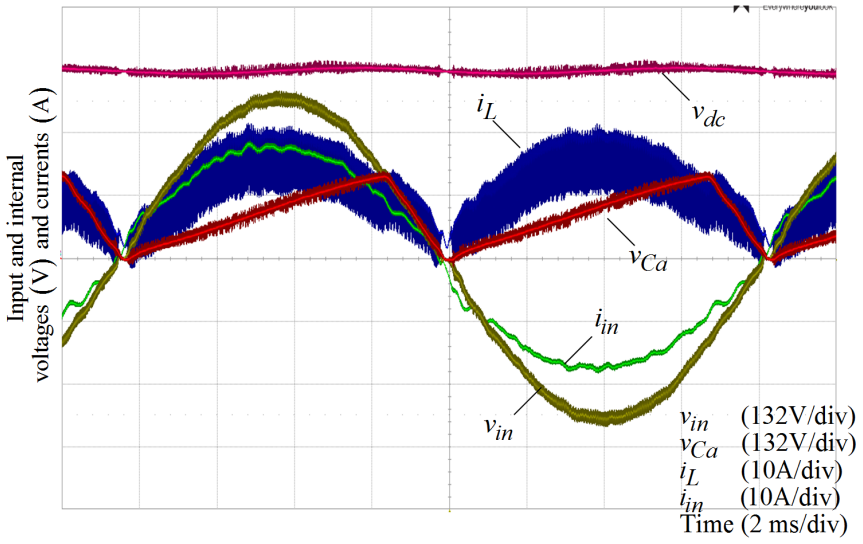
(b)

Figure 4.4: (a)Photograph of the experimental prototype (b) Coupled inductor structure

active at 3300 W. Fig. 4.5(b) depicts some of the salient internal waveforms of the converter. Voltage across the capacitor C_{dis} shown in red varies at twice the line frequency resetting once its voltage reaches the input voltage value. Fig. 4.6 depicts the gate-to-source and drain-to-source voltage waveforms of switch S_1 and the inductor currents. As seen, the drain voltage of S_1 falls to zero as the auxiliary current goes above the primary current after which the gate voltage is triggered,



(a)



(b)

Figure 4.5: Measured input current ripple (green), input voltage (yellow), output voltage (red) and current ripple (blue) waveforms with ZVT circuit at 3 kW (Current THD − 9%) (b) Input (v_{in}) and auxiliary capacitor (v_{Cd}) voltage waveforms along with inductor (i_L) and input current

thereby demonstrating ZVS turn-on. The efficiency curves of the converter with and without the ZVT is shown in Fig. 4.7.

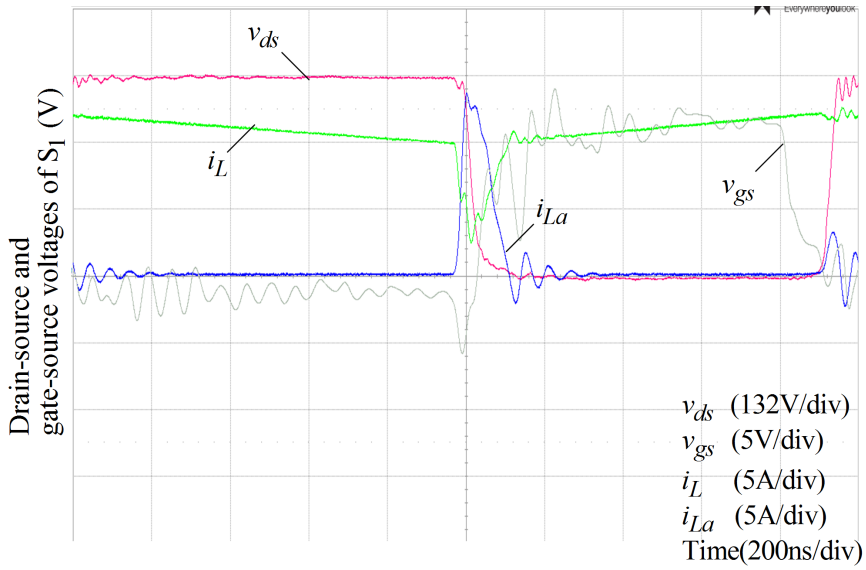


Figure 4.6: Waveforms of switch S1 and inductor currents, drain-to-source voltage (red), gate-to-source voltage (grey), auxiliary inductor current (blue), main inductor current (green)

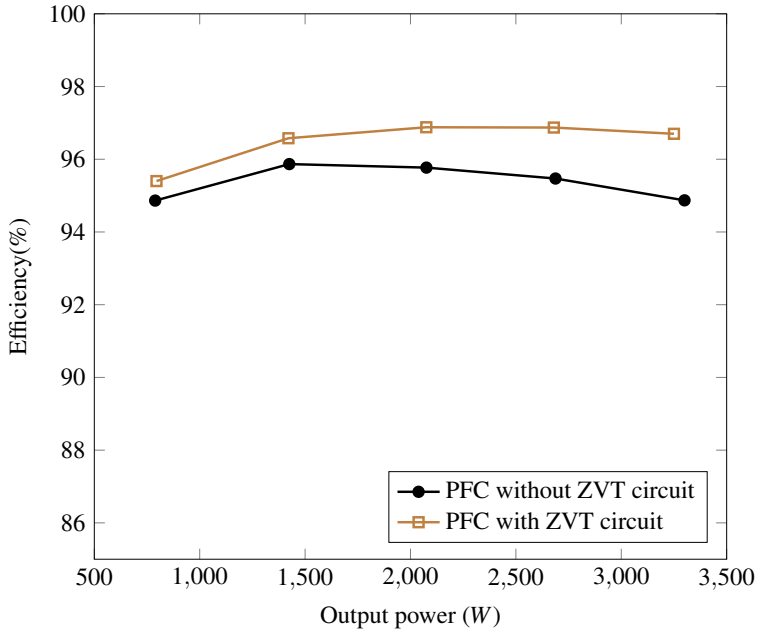


Figure 4.7: Efficiency of the PFC converter with and without the ZVT circuit

Though the integrated magnetic performance is significantly better than the hard-switching counterpart, the efficiency values are lower compared to the discrete inductor implementation. This increase in losses are attributed to the increased core and

copper loss in the main inductor due to the high ripple current content.

4.4 PFC with ZVT and Half-bridge Circuit

Another modification to the ZVT circuit is to include another inductor and direct the energy stored in the auxiliary circuit to the DC link. The resonant pole that is made up of S_1 that connects to an auxiliary inductor (L_{aux1}), diode D_{aux} and capacitor (C_{dis}). The capacitor is followed by another small inductor (L_{aux2}) that connects to the mid point of the half-bridge. There are several advantages to this configuration, the size of C_{dis} can be significantly reduced (for example from 35uF to $<$ 5uF in this work); unlike the configuration in Fig. 4.8, here the voltage across C_{dis} is constant, as the half-bridge in the above mentioned isolated dc-dc topologies operate with fixed duty ratio (and rely on controlling phase-shift or frequency for regulation), and this results in smaller voltage stress for the auxiliary switch ($V_o/2$ instead of V_o for this work) and allows to better optimize the ZVT design for lower losses and extend the ZVT range. The new inductor added, L_{aux2}, carries a very low dc current leading to small size and negligible losses. The size of the new C_{dis} and L_{aux2} together is significantly smaller than the original C_{dis}. There are no additional switches or gate drive as it uses the switches of the post regulator. Moreover, the inductor current in the PFC stage has smoother, rectified sine waveform compared to the previous design where the current has a jump at the instant when the discharge process starts in each fundamental cycle. A validation of these characteristics is shown in this section.

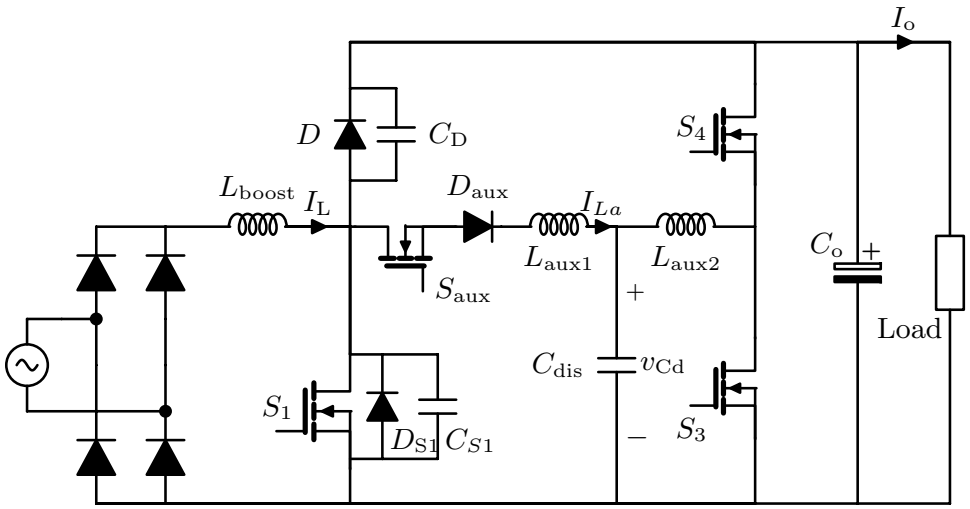


Figure 4.8: Schematic of the PFC with modified ZVT that uses a half-bridge of post dc-dc converter

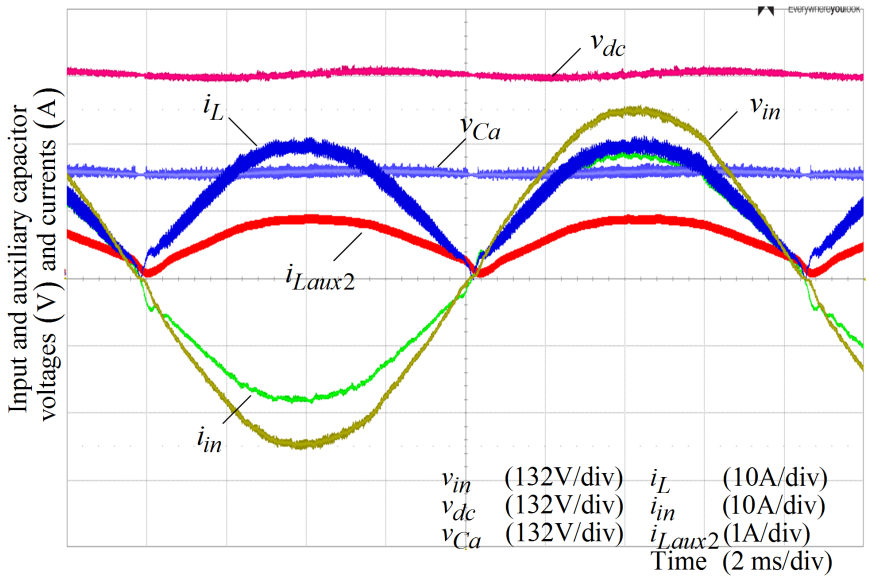
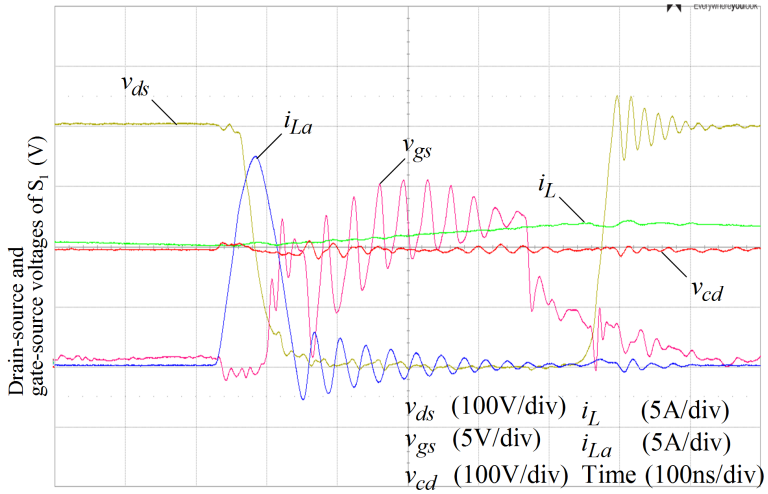
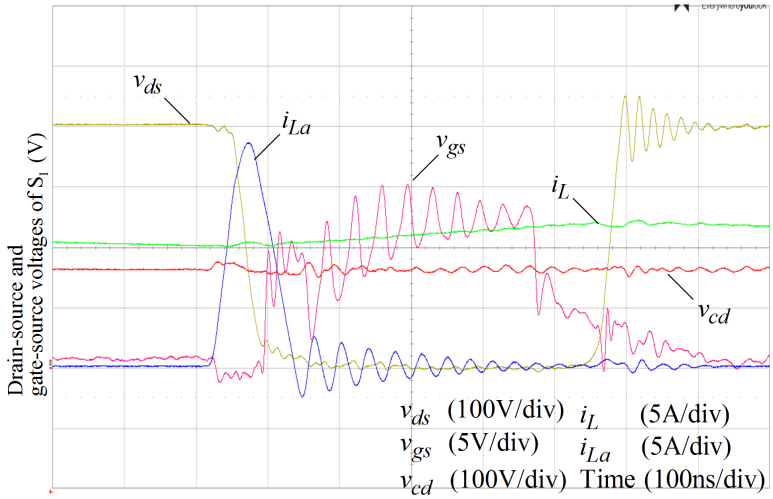


Figure 4.9: Salient experimental waveforms of the modified ZVT circuit of Fig. 3.1 at 3.3 kW - input current (green), input voltage (yellow), output voltage (pink), boost inductor current (blue), auxiliary capacitor voltage (violet) and cycle-by-cycle averaged Laux2 current (red) waveforms. The measured THD in the input current is 3.7%.

This topological change significantly reduces the footprint of the input capacitance as shown in Fig. 4.9. The additional inductor is designed for $200\mu H$ and the film capacitor is reduced from $30\mu F$ to $5\mu F$.



(a)



(b)

Figure 4.10: Waveforms of drain-to-source voltage (yellow), gate-to-source voltage (maroon), auxiliary inductor current (blue), main inductor current (green) (a) Switch S_1 with half-bridge at d=0.5 (b) Switch S_1 with half-bridge at d=0.4 (c) Switch S_{aux}.

The salient experimental waveforms including input voltage and current, boost inductor current, and auxiliary capacitor voltage at an output power of 3300 W, 400 V dc link and 500 kHz are shown in Fig. 4.9. The input current THD is 3.7% which is better than the previous configuration. As seen in the figure, the boost inductor current is close to a pure rectified since wave and free of the jump seen in the earlier

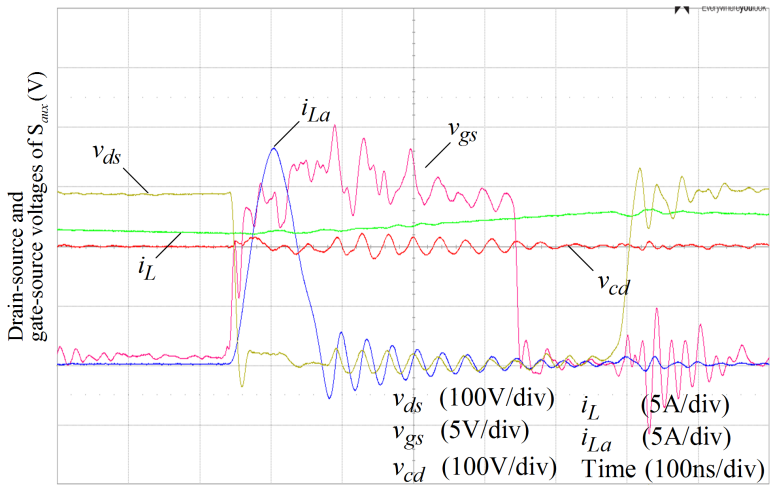


Figure 4.11: Waveforms of drain-to-source voltage (yellow), gate-to-source voltage (maroon), auxiliary inductor current (blue), main inductor current (green) of Switch S_{aux}.

configuration. The auxiliary capacitor voltage is roughly one-half the dc link voltage as the half-bridge is operated at 0.5 duty ratio.

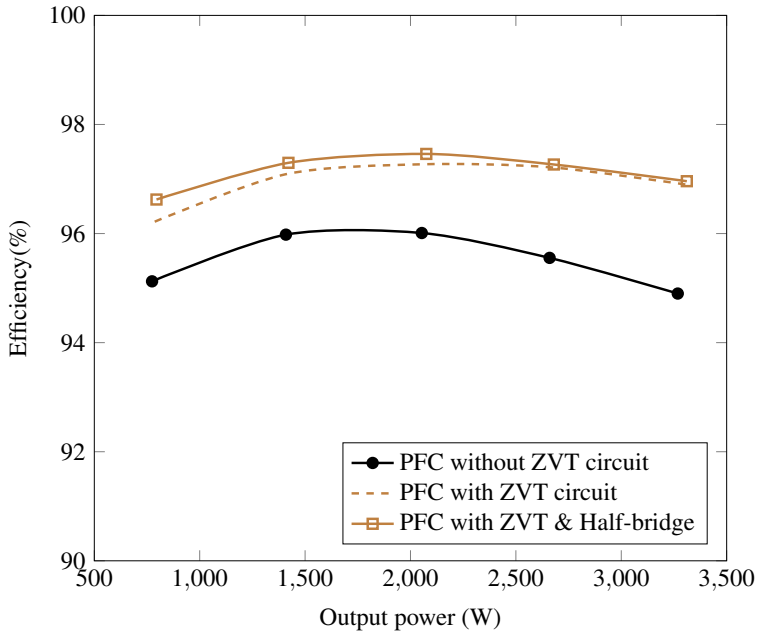


Figure 4.12: Efficiency of the PFC converter at 500 kHz comparing hard-switching, PFC with ZVT circuit (Fig. 3.1), and PFC with modified ZVT using half-bridge (Fig. 4.8)

Fig. 4.10(a) depicts the gate-to-source and drain-to-source voltages of switch S_1,

the auxiliary inductor current (S_{aux} current) and the boost inductor current. It can be seen from the waveform that the main power switch operates at the border of ZVS and the auxiliary switch with ZCS Due to the resistive damping in the auxiliary circuit, the main switch turns-off at a non-zero voltage. This effect can be addressed by operating the half-bridge at duty ratio lower than 0.5 to maintain ZVS as shown in Fig. 4.10(b). Voltage and current across switch S_{aux} is shown in Fig. 4.11 demonstrating a significant reduction in current and voltage stress in this device compared to previously proposed converter shown in Fig. 3.11. The performance of the PFC with the two ZVT configurations are compared and the corresponding efficiency plots over the full operating range and at 500 kHz are presented in Fig. 4.12.

4.5 Full On-board Charger System

A 1kW prototype based on the previously proposed topological changes is presented in this section. Fig. 4.13(a) shows the two stage boost PFC circuit used for the front-end converter, which is connected to a dual-active bridge converter. The PFC circuit in this configuration experiences soft-switching based on the topology proposed in Section 3.2, whereas the system configuration shown in Fig. 4.13(b) implements the ZVT discharge mechanism proposed in Section 4.4.

The photograph of the entire system can be seen in Fig. 4.14. The design of the PFC stage is similar to the one elaborated in Section 4.3 which operates at 500kHz switching frequency. In case of the dual-active bridge converter SiC C2M0065090D TO-247 packages were selected to meet the desired voltage and current requirements for both primary and secondary bridges. The current ripple at the DC link is filtered using EPCOS Inc polypropylene capacitors. A Ferroxcube 3F3 MnZn ferrite core and litz wire was used to fabricate the transformer. An additional leakage inductance of 80uH was added through a discrete inductor that was placed on top of the main circuit

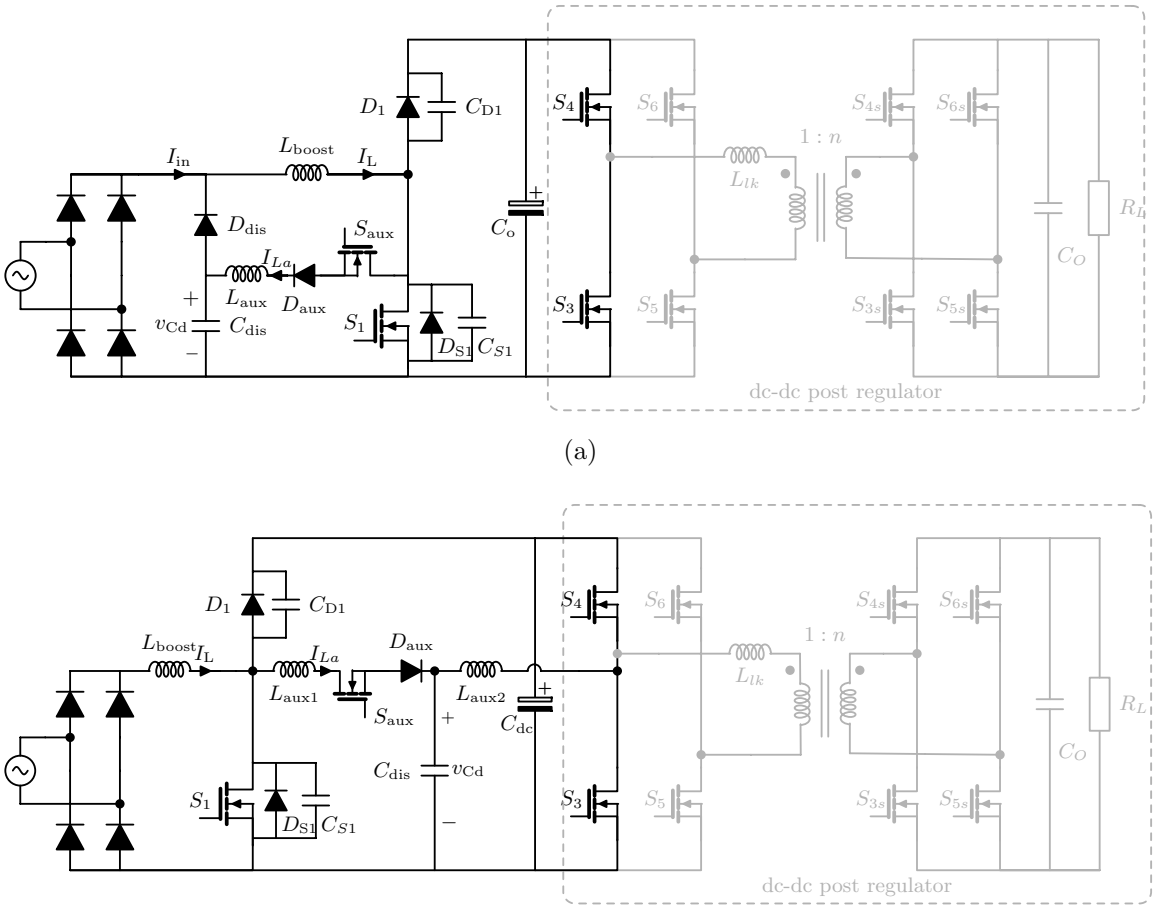


Figure 4.13: Circuit diagram of the completely integrated charger system (a) discrete auxiliary ZVT circuit with discharge through main inductor (b) Integrated auxiliary ZVT with discharge through post dc-dc stage.

board. A stacked approach using board-to-board headers was utilized for the gate driver to the main PCB. Discrete gate driver boards for each bridge was designed as shown in Fig. 4.15 and placed in close proximity to the switches soldered to the main PCB. A heat sink was designed to span the base of the entire converter to maximize the heat spreading. An external TI DSP28335 evaluation board was used to generate the gating pulses and implement the control for the dc-dc stage.

Closed loop control was added and the two converters were cascaded to form the full charger system. The input was grid tied with an isolation transformer to

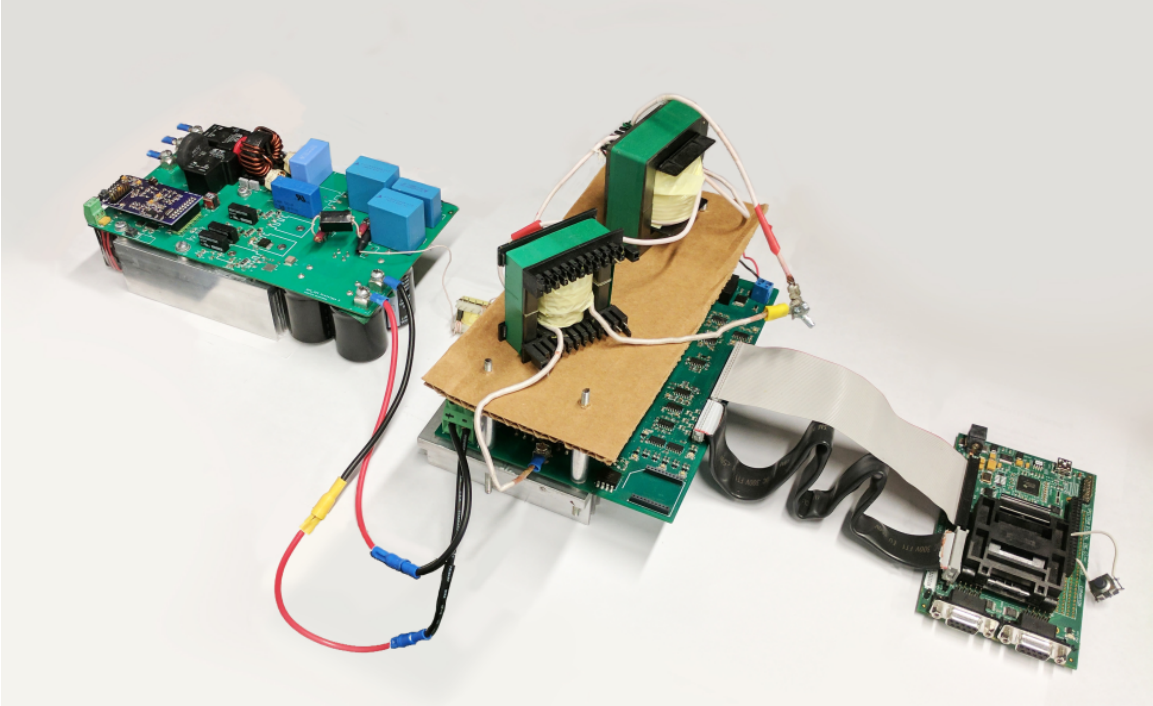


Figure 4.14: Photograph of the full charger system prototype

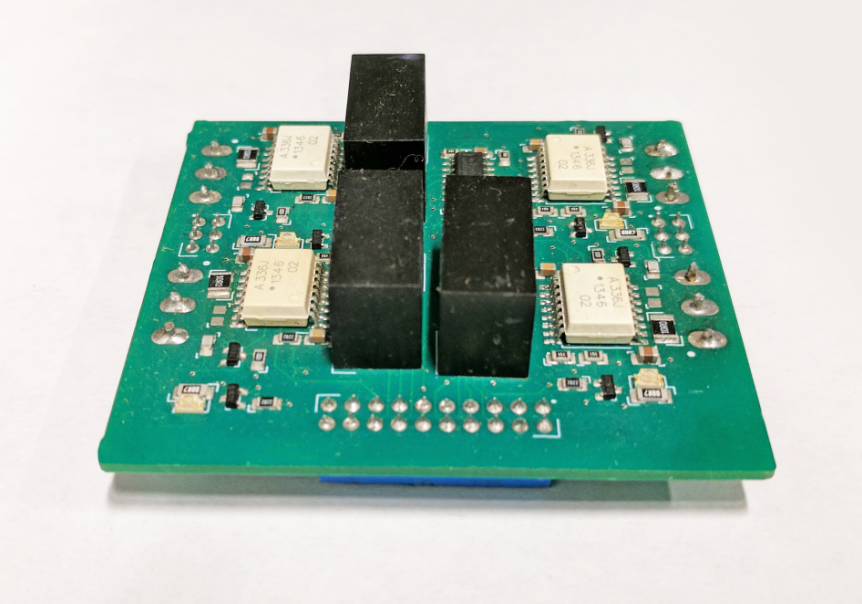


Figure 4.15: Photograph of the dual active bridge gate drive circuit

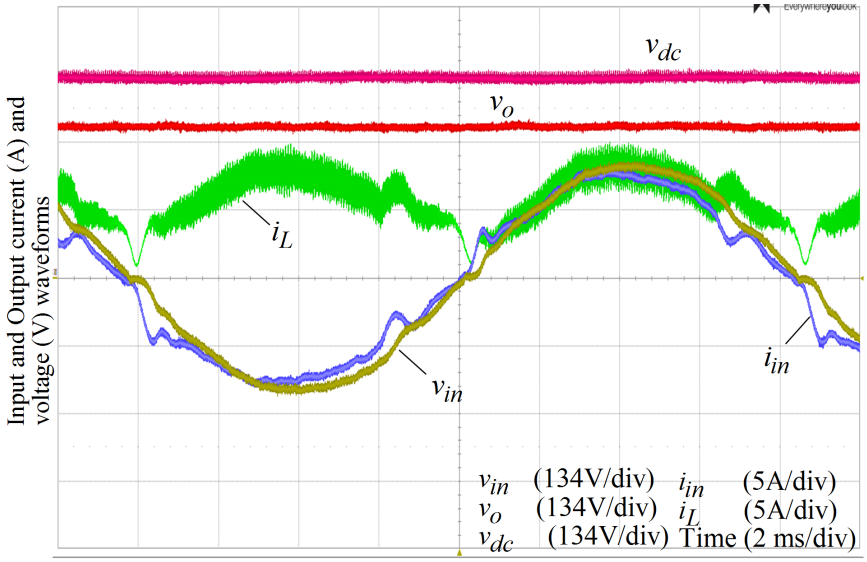


Figure 4.16: Measured input current (blue), input voltage (yellow), boost inductor current (green), dc-link voltage (pink) and output voltage (red) waveforms with soft-switching at 1kW

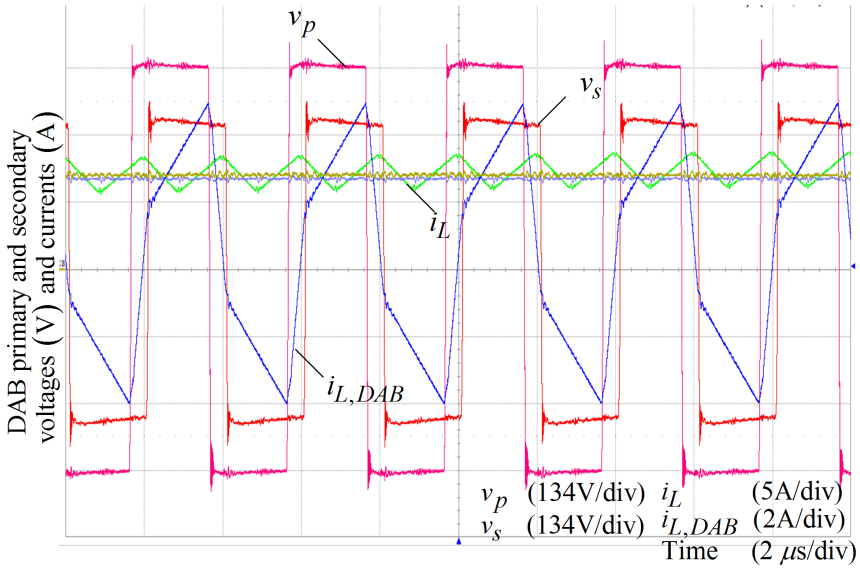


Figure 4.17: Switching level waveforms of bridge voltages and current through the primary of the transformer connected to DAB

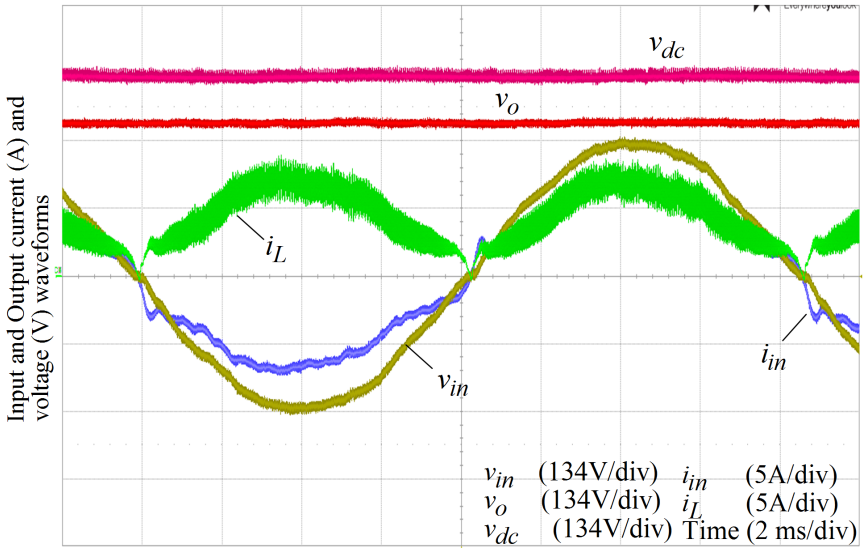


Figure 4.18: Measured input current (blue), input voltage (yellow), boost inductor current (green), dc-link voltage (pink) and output voltage (red) waveforms with soft-switching at 1kW

protect the measurement equipment and the output was resistively loaded using light bulbs. The dc-dc stage was operated at 250 kHz and the ac-dc stage at 500kHz with asynschronous operation. The input voltage and current, dc bus voltage and the output load voltage are shown in Fig. 4.16 for an output power of 1kW. The input current amplitude of the PFC stage was regulated at 9A peak using a current loop controller. The current waveform is slightly distorted around the line voltage zero crossings and this is due to sluggish response of the large boost inductor. Also the boost inductor current i_L has a noticeable jump in current magnitude that coincides with the discharge of C_{dis} capacitance. The output DC link voltage was held at 400V and the following post regulator maintained the voltage at the resistive load at 300V. The voltage across the primary and secondary bridge of the dual-active bridge and the current through primary winding of the high frequency transformer is shown in Fig. 4.17. The boost inductor current i_L (green) is also shown in the figure showing the operating frequency. The efficiency of the full system is 91.3% at this low power level.

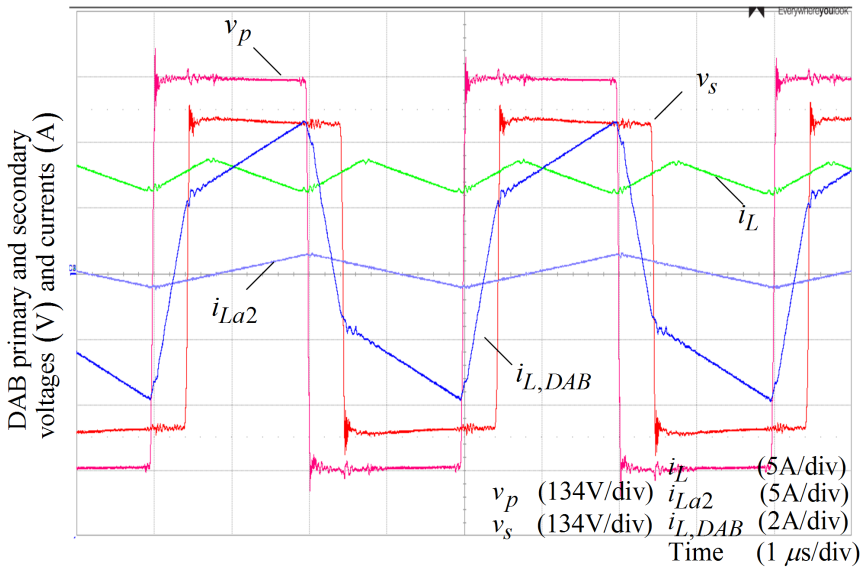


Figure 4.19: Switching level waveforms of bridge voltages and current through the primary of the transformer connected to DAB

Fig. 4.18 and Fig. 4.19 shows the low frequency and switching frequency level waveforms for the ZVT circuit connected to the following dc-dc stage. The converter was operated at 1kW by regulating the dc-link voltage at 400V similar to the previous configuration. The output voltage is tightly regulated at 300V to eliminate the 120Hz ripple across the resistive load. The boost inductor current shown in Fig. 4.18 has a rectified sine wave envelope and the input current current (violet) i_{in} follows in-phase with the input voltage. The cycle-by-cycle value of auxiliary inductor (blue) as seen in the figure processes a fraction of the total power of the circuit and hence a small value of inductance is sufficient to handle this. The switching level waveforms of DAB bridges and the current through primary winding of the high frequency transformer is shown in Fig. 4.19. Current through the auxiliary inductor L_{aux2}, i_{La2} is bipolar depending on the load level, thus the switches in the DAB primary leg experiences minimal losses due to the additional circuit.

4.6 Summary

In this chapter, simple modifications tp the zero voltage transition circuit is proposed for a boost-type PFC converter which requires high frequency of operation. The operating principle and design requirements of the ZVT circuit are presented. Both the main and the auxiliary switches achieve ZVS and ZCS respectively. The analysis and performance of this system has been validated experimentally using a 3.3 kW /500 kHz prototype and simulation results showing the internal waveforms of the converter has been presented in this paper. The auxiliary circuit employing the coupled inductor improves the overall efficiency by 1.85% reducing the total losses by 39% and the half-bridge configuration by 46% compared to hard-switched operation near full load.

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