High Speed CMOS Image Sensor

by

Akshay Zol

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Graduate Supervisory Committee:

Hugh Barnaby, Chair
Esko Mikkola
Jennifer Kitchen

ARIZONA STATE UNIVERSITY

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ABSTRACT

High speed image sensors are used as a diagnostic tool to analyze high speed processes for industrial, automotive, defense and biomedical application. The high fame rate of these sensors, capture a series of images that enables the viewer to understand and analyze the high speed phenomena. However, the pixel readout circuits designed for these sensors with a high frame rate (100fps to 1 Mfps) have a very low fill factor which are less than 58%. For high speed operation, the exposure time is less and (or) the light intensity incident on the image sensor is less. This makes it difficult for the sensor to detect faint light signals and gives a lower limit on the signal levels being detected by the sensor. Moreover, the leakage paths in the pixel readout circuit also sets a limit on the signal level being detected. Therefore, the fill factor of the pixel should be maximized and the leakage currents in the readout circuits should be minimized.

This thesis work presents the design of the pixel readout circuit suitable for high speed and low light imaging application. The circuit is an improvement to the 6T pixel readout architecture. The designed readout circuit minimizes the leakage currents in the circuit and detects light producing a signal level of 350µV at the cathode of the photodiode. A novel layout technique is used for the pixel, which improves the fill factor of the pixel to 64.625%. The read out circuit designed is an integral part of high speed image sensor, which is fabricated using a 0.18 µm CMOS technology with the die size of 3.1mm x 3.4 mm, the pixel size of 20µm x 20 µm, number of pixel of 96 x 96 and four 10-bit pipelined ADC's. The image sensor achieves a high frame rate of 10508 fps and readout speed of 96 M pixels / sec.

DEDICATION

To my parents

for their sacrifices, care and love

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CHAPTER 1

INTRODUCTION

Image sensors built in CMOS technologies are often referred to by the acronym CIS (CMOS Image Sensors). The CMOS sensor delivers images when irradiated by light at frequencies covering roughly the visible and near infrared band of electromagnetic spectrum ($400nm < \lambda < 1000nm$). This thesis deals with the design of a pixel readout circuit for a high speed camera using CMOS technologies. The ultimate goal of this research is to design and fabricate a pixel circuit which has a high readout speed, low leakage and a higher fill factor. This chapter describes the motivation for this research and organization of the thesis.

1.1 Motivation

High speed cameras are used as a diagnostic tool to analyze high speed processes for industrial, automotive, defense and biomedical applications. They are also required for a myriad of opto-electronic applications used in integral machine vision, time-of-flight imaging and topographic imaging [1-16]. These cameras capture a series of images at a very high frame rate which enables the viewer to analyze and understand the details of the high speed phenomena. These applications must analyze high speed phenomena from 100 fps (frames/sec) to 10 Mfps and have resulted in significant progress in the design of high-speed image sensors. Advances in deep submicron CMOS technologies have made high speed imaging possible. Fabrication of an image sensor in a standard CMOS technology allows for integrating the sensor with processing and control circuits on the same chip. This system-on-chip integration helps to reduce power consumption, cost and sensor size and

addition of new functionalities to the sensor. Moreover, CMOS technology scaling has made it possible to integrate increased number of transistors in a pixel to improve detection and on-chip signal processing. This helps to achieve the image quality and global shuttering performance necessary to meet the demands of high speed applications.

For a high speed image sensor, light sensitivity and frame rate are very important specifications. Light sensitivity is determined by the physical aspects of the silicon (i.e., quantum efficiency), pixel size and the conversion gain. These properties are dependent on the pixel design and choice of technology [18]. Moreover, the fill factor of a pixel also plays a very important role for high speed and low light applications.

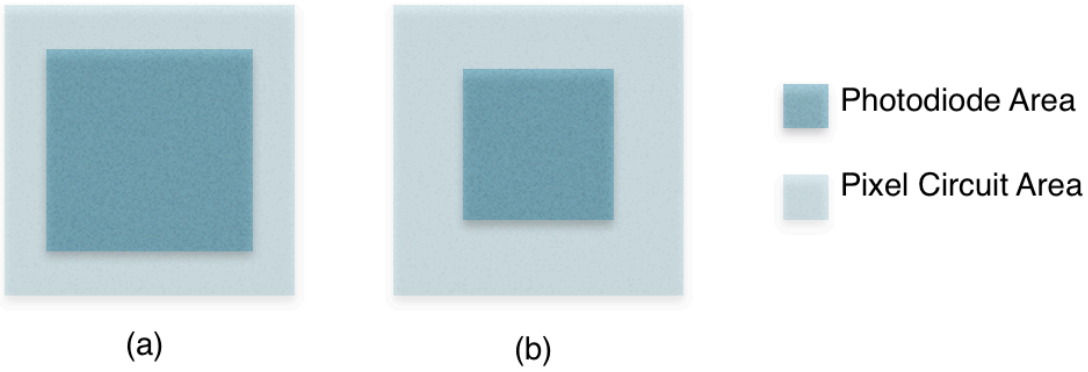


Figure 1:Pixel with different fill factors (Photodiode area corresponds to the light sensitive area) (a) Pixel with a fill factor of 50% (b) Pixel with a fill factor of 25 %

The fill factor of a pixel describes the ratio of light sensitive area versus total area of a pixel, since part of the area of an image sensor pixel is always used for transistors, electrodes or registers, which belong to the structure of the pixel. Only the light sensitive part contributes to the light signal, which the pixel detects.

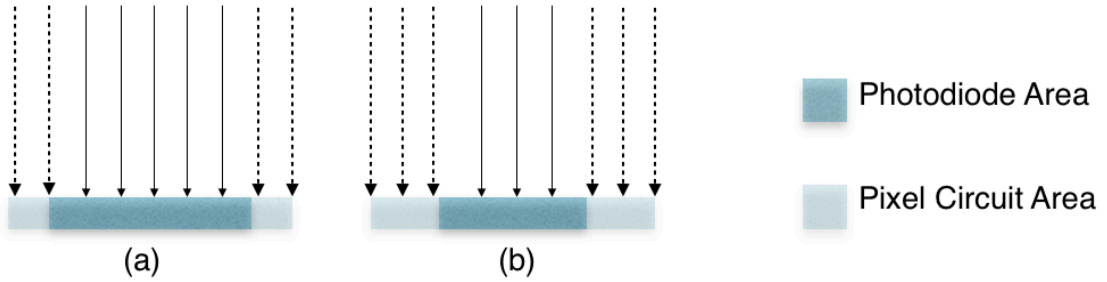


Figure 2: Cross sectional area of the pixel with different fill factors (photodiode area corresponds to the light sensitive area) and the light which impinge on them (black arrows). Dashed light rays indicate, that this light does not contribute to the signal. (a) Pixel with a fill factor of 50% (b) Pixel with a fill factor of 25 %

Table 1: Summary of various high speed imagers available in literature

REF	TECH	Frame Rate fps	Array Size	Pixel Area	FF %
[18]	0.18µm	6242	1280 x 800	20µm x 20µm	58
[20]	-	485	1696 x 1710	8µm x 8µm	37
[21]	-	1M	360 x 360	50µm x 50µm	13.5
[24]	0.25µm	2k	256 x 1	20µm x 20µm	48
[25]	0.18µm	7.8k	400 x 256	32µm x 32µm	37
[26]	0.5µm	100	1024 x 768	11µm x 22µm	45
[27]	0.18µm	1.18k	924 x 768	30µm x 30µm	11
[29]	0.18µm	10k	352 x 288	9.4µm x 9.4µm	15
[9]	0.35µm	10k	64 x 64	35µm x 35µm	25
[12]	0.35µm	3.3k	320 x 240	11.2µm x 11.2µm	53
This Work	0.18µm	5.5k	96 x 96	20µm x 20µm	64.625

Table 1, above, summarizes the specifications of various high speed image sensors reported in literature. It can be seen that for high speed imagers, the fill factor is less than 58%. Fill factor plays an important role for high speed imaging where there is low light and (or) less exposure time. Under either of these conditions the number of photons incident on each pixel (photon flux) can be very small. A higher fill factor increases the photosensitive area, thereby enabling the detection of faint light signals. An image sensor's

capability to detect low light signals also decreases due to the losses of signals stored in the pixel readout circuit, through leakage paths in the circuit. Thus, minimizing leakage is very important in the detection of very low light signals. Therefore, both fill factor and leakage play a very important role in low light and high speed imaging applications.

The frame rate of a camera is the frequency (rate) at which the camera displays consecutive images, called frames. High speed applications require high frame rates. The speed advantages offered by scaled CMOS, as described by Moore's Law, can be fully exploited in the design of high speed image sensors. Leveraging CMOS technology for these applications has led to continuous increase in the sensor speed [31-35]. High frame rates are achieved by increasing parallelism through the use of multiple output channels. Traditionally the maximum frame rate achievable by a CMOS image sensor was determined by the maximum bandwidth in the column multiplexer or output amplifier, or the maximum data rate of the column or output stage analog-to-digital (AD) converter. This limitation could be ameliorated by good design practices including: pipelined operation of pixel sampling, column AD conversion and column readout; the development of faster column ADCs; massive parallel readout. Thus the fundamental limitation for frame rate is imposed by the time to sample the signals from the pixel array into the column amplifiers [22]. An image core consisting of the pixel readout circuit is the main design bottleneck to high speed operation. Therefore, a focus on designing a high performance pixel readout circuit is critical for high speed, low light operation.

The goal this thesis is to present a design of a CMOS readout circuit for an image sensor which improves fill factor, image accuracy and gives a high readout performance suitable for high speed and low light applications. The research work discusses the design,

layout and simulation results of the readout circuit. The design is simulated and taped out in 0.18 μm CMOS process.

1.2 Overview of thesis

Chapter two provides an introduction to the pixel sensor architecture used in CMOS image sensors. The focus is on the different pixel architectures used for CIS. It gives the details of the 6T architecture used for high speed imaging and the problems associated with the architecture., chapter five provides a summary and some potential new research directions. Chapter three describes the chip architecture of the image sensor designed. It describes the pixel readout architecture designed and it operations principle to get a higher readout speed, higher fill factor and low leakage. It discusses the design considerations made while designing the pixel readout circuit and also the novel layout technique used to improve the fill factor. Chapter four discusses the results obtained for the pixel designed focusing on the settling time of pixel, noise analysis, minimum exposure time, readout speed and layout of the pixel. Finally, chapter five provides a summary and some potential new research directions.

CHAPTER 2

BACKGROUND

2.1 CMOS sensor Functionality

A typical CMOS image sensor is an integrated circuit with an array of pixel sensors. Each pixel contains its own light sensor (photodetector) and pixel readout circuit. An analog-to-digital converter and other components critical to the operation of the pixel sensor are located on the CMOS sensor.

Light coming through a lens reaches the pixel sensor array. Each pixel sensor converts light into a voltage signal which is further processed by the rest of the CMOS sensor. The CMOS sensor consists of three main parts: pixel array, the digital controller and the analog to digital converter. Figure 3 shows the main parts of the CMOS image sensor.

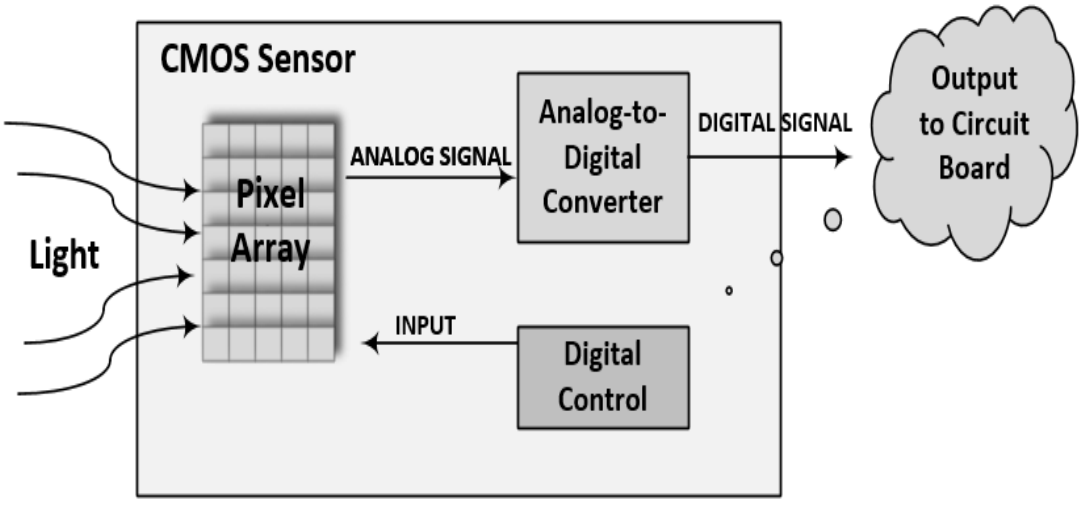


Figure 3: Components in a CMOS sensor.

(i) Pixel array

The pixel array, shown in figure 4, consists of an array of active pixel sensors which are responsible for capturing the intensity of light incident on the array. The orange part shows the read out circuit area and the blue part shows the photosensitive area. Each individual pixel sensor converts the detected intensity level into a voltage signal before passing it to the analog-to-digital converter.

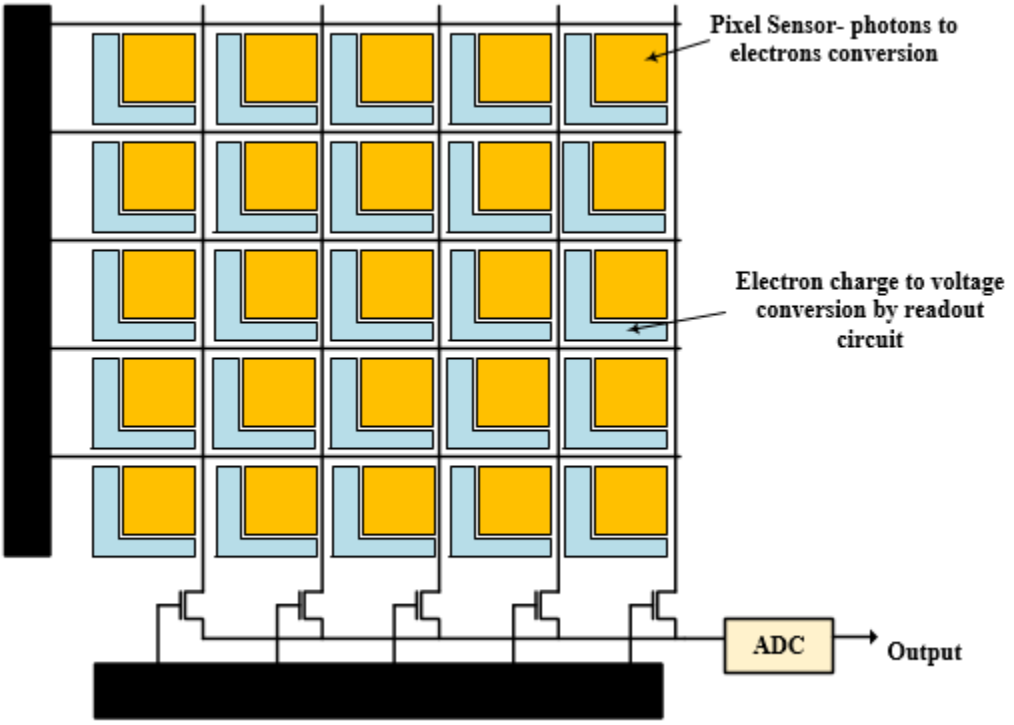


Figure 4: Pixel array

The sensor works by using the principle of photoelectric effect. The photoelectric effect is a phenomenon for which there is emission of electrons from a solid state material when energy from electromagnetic radiation is absorbed by the material. For image sensors, the source of the electromagnetic radiation is light, which can be interpreted as particles called photons. The intensity of light is proportional to the photon flux. Similarly,

the amount of electrons emitted is relative to the amount of photons striking the sensitive material in a pixel sensor. The incident photons generate electrons and the resulting charge from the emitted electrons is converted into a voltage signal by the readout circuit of the sensor. The voltage signals from the pixel sensors in the pixel array are then sent to the analog-to-digital converter.

(ii) Digital control

The digital controller consists of circuits integrated onto the CMOS sensor that control the pixel array. It is responsible for generating the timing signals for the pixel readout circuit and control its operation. It takes care of the electronic shuttering control signal for the pixel, resetting the pixels after each exposure and telling the pixel array to start and stop capturing light. It also takes care of the row and column addressing for the readout of the pixel array. Thus any circuitry that is required for the array of pixels to function correctly is included in the digital controller.

(iii) Analog to digital converter (ADC)

The function of the ADC is to take the analog voltage signals from the pixel array and convert them into a digital signal. The final digital signal is sent as output to an image processor or another device independent of the CMOS sensor which further processes the digital signal into an image which is viewable by the user.

2.2 Photodetectors

A photodetector performs one of the main functions in all image sensors, that is, detection of light. It is therefore a critical component of the pixel sensors. Photon sensing done in photodetector is based on the basic principle of Einstein's Photoelectric effect wherein photons hitting a semiconductor generate electrons through ionization, thereby

creating “charge”. The photodetector device used in most CMOS image sensors is a photodiode.

A photodiode is formed by joining a p-type silicon and n-type silicon junction on a solid state substrate. Silicon absorbs light in the range from 260nm to 1100nm making it suitable for photo sensing. In the p-type silicon region, a large concentration of holes is available, whereas in the n-type silicon region, a large concentration of electrons is available. The holes in the p region tend to diffuse into the n region, whereas the free electrons in the n region tend to diffuse in the p region, thereby recombining. This recombination leads to formation of bound positive charge and bound electron near the transition region as shown in figure 5(a). This diffusion of free carriers creates a depletion region at the junction where no free carriers exist, and which has a net negative charge on the p side and a net positive charge on the n side. The total amount of exposed or bound charge on the two sides of the junction must be equal for charge neutrality. There is a formation of electric field going from the n side to the p side and gives rise to a potential difference between the n side and p side, called as a built-in voltage of the junction. This voltage opposes the diffusion of free carriers until there is no net movement of charge under open-circuit and steady- state conditions. The p-n junction and the depletion region play an important in photon sensing using photodiode.

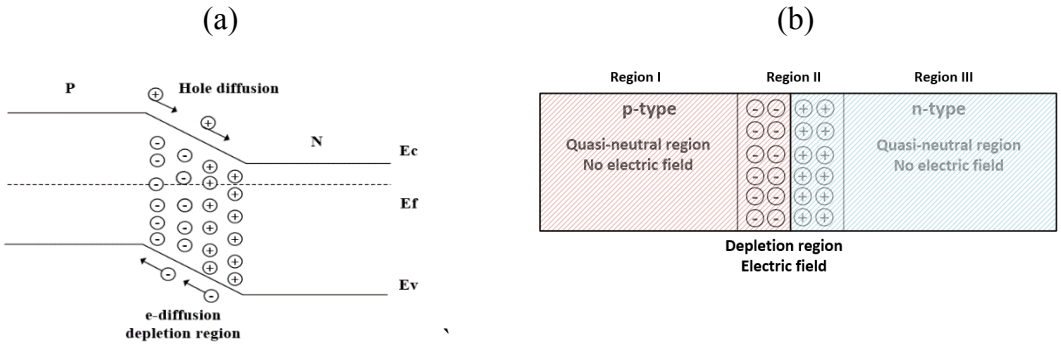


Figure 5: (a)Diffusion in p-n junction photodiode (b) Regions in p-n junction diode

When a photon of energy greater than the bandgap energy of silicon ($Eg > 1.1$eV) is incident on the photodiode, it is absorbed by the silicon material. The incident photon energy excites an electron into the silicon conduction band and produces a pair of charge carriers i.e. an electron-hole pair (EHP). The number of EHP's generated depend on the photon flux incident on the photodiode. The EHP generated ideally occur throughout the p-n junction. The electrons (in p-type silicon) and holes (in n-type silicon) generated are meta-stable and will only exist for a time equal to the minority carrier lifetime before they recombine. If the carriers recombine, the light generated EHP are lost and do not contribute to photocurrent. In a p-n junction, it is assumed that electric field is confined to the depletion region; and region I and III as shown in figure 5(b) which do not have electric field are termed as quasi-neutral region. If the EHP are generated more than a diffusion length away from the depletion region in the quasi neutral region or near the surface of the device, the carriers have to travel a larger distance to reach the depletion region and thus have a high probability of recombining. However, if the EHP are generated in or close to the depletion region, they are swept by the electric field leading to a useful photocurrent. Moreover, increase in the width of the depletion layer will allow the photodiode to collect

more photons, thereby producing more EHP's and contributing to photocurrent. Thus the photodiode is reverse biased for image sensors.

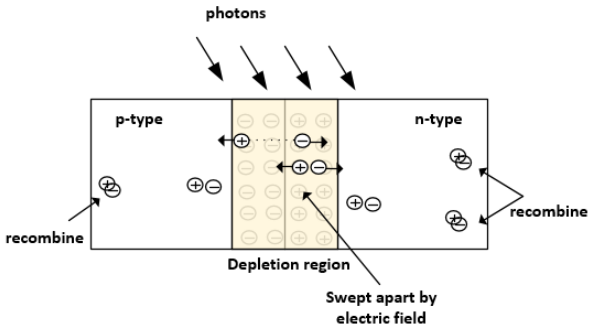


Figure 6: Photodiode operation

In voltage mode active pixel sensors, the photocurrent generated from the incident photons discharges a photodiode capacitance which has been precharged to some reference level using a reset signal. The output voltage signal of the photodiode depends on the photocurrent and the junction capacitance.

Figure 7 shows the photodiode model for the p-n junction diode proposed by Swe and Yeo [40]. The photodiode can be modelled by a current source, a diode, a capacitance and two resistances. Resistance R_S is a series resistance and arises from the contacts and resistances of the undepleted silicon. Resistance R_J is a junction resistance which varies along with the current of the photodiode. C_{PD} is the depletion capacitance or junction capacitance of the reverse biased photodiode. Current source I_P models the photocurrent in the photodiode and diode is a p-n junction diode to represent the core of the photodiode.

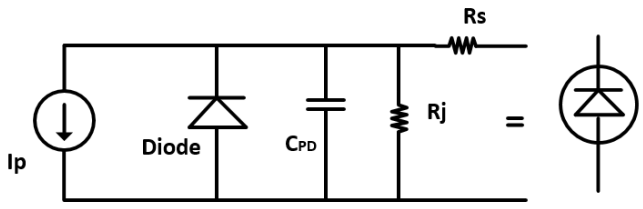


Figure 7: Photodiode model

Quantum efficiency (QE) and collection efficiency are important specification factors for the photodiode. Quantum efficiency is defined as the percentage of photons hitting the photosensitive surface that produce an electron hole pair. Collection efficiency is defined as the fraction of the generated electron hole pair that contribute to a current flow external to the detector. These parameters determine the sensitivity of the photodiode. [36] The other important photodiode parameters are dark current, thermal and shot noise which depend on the diode material. Dark current is the relatively small electric current that flows through the photodiode even when no photons are entering the device. These parameters of photo sensing depend on the structure and type of junction.

In a standard n-well CMOS process, there are three p-n junctions that can be used in light detection:

(i) n+/p-sub

(ii) n-well/p-sub

(iii) p+/n-well/p-sub

The photodiode designed for the sensor described in this thesis is a n+/p-sub photodiode. Figure 8, below, shows the schematic diagram of the n+/p-sub photodiode.

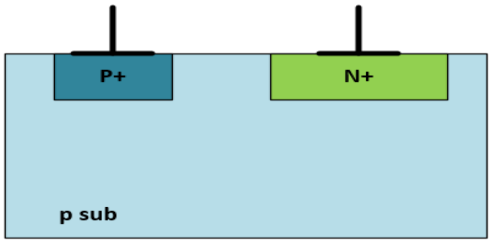


Figure 8: Photodiode structure

This structure is the most compact photodiode of the three diode types. It was selected to maximize the light detecting area and make it suitable for low light imaging. It is formed

by creating a highly doped n-region in the p substrate. Tian et al compared n+/p-sub and n-well/p-sub photodiodes in 0.18um CMOS process [37], where gate leakage currents on the order of photocurrents under normal lighting conditions require optimizing design beyond photodiode selection. The ultimate performance of the sensor also depends on the pixel and peripheral circuitry in addition to the photodiode. Material parameters control photodiode performance and cannot be changed by the designer unless the CMOS fabrication process is modified. Thus the focus of this work is to optimize the design of the pixel circuitry.

2.3 Types of CMOS image sensors

The basic block diagram of CMOS image sensor is shown in figure 9. The key component of the image sensor is the pixel array. The row decoder selects the row of the array, one row at a time, with the timings from the control signal block.

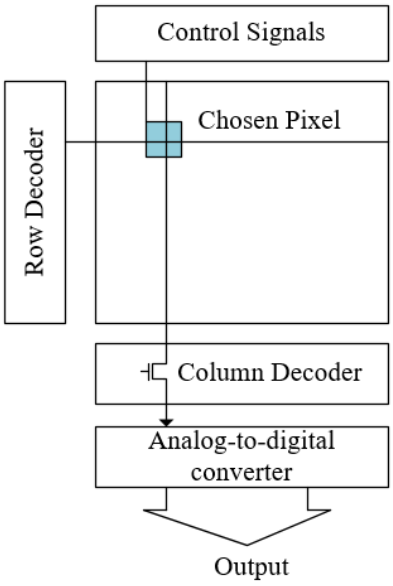


Figure 9: Block diagram of a CMOS image sensor

Similarly, the column decoder performs the function of selecting the column. As the figure indicates, the sensor output is typically passed to the ADC through the column decoder. CMOS image sensors are mainly classified into two categories

1. Passive pixel sensors (PPS)
2. Active pixel sensors (APS)

2.3.1 Passive pixel sensors (PPS)

Passive pixel sensors were introduced by Weckler in 1967. The structure of a passive pixel sensor consists of a photodiode and a metal-oxide-semiconductor field effect transistor (MOSFET). The schematic view of a PPS is shown in figure 10. The MOSFET ("addressing transistor") performs the function of selection of the pixel in the array. The pixels are read by selecting the pixel using row decoder and column decoder.

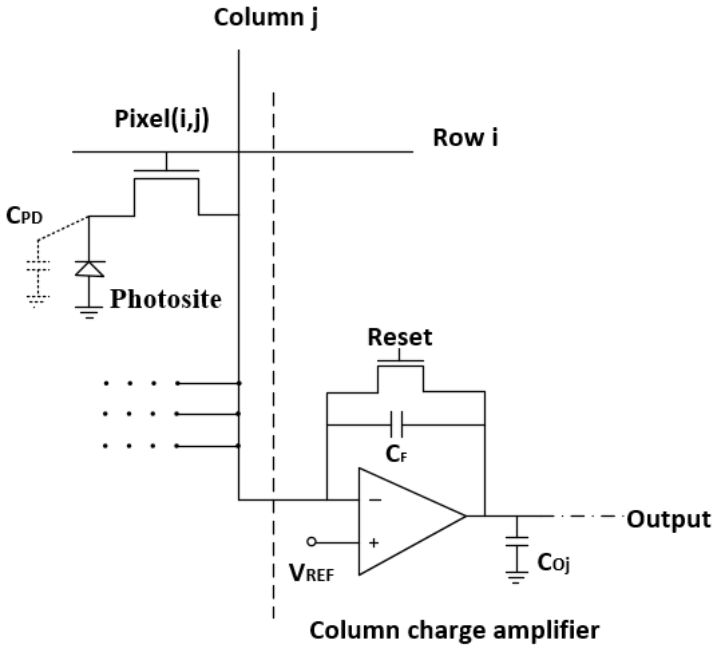


Figure 10 : Architecture of a passive pixel sensor

PPS are small since they have a very basic structure, which involves an area large enough for photodiode, 'addressing transistor' and connections. Though PPS are not as efficient as APS, they have an important advantage: higher fill factor in a lower area, which leads to higher quantum efficiency.

PPS has a column charge amplifier for each column in the array. It has a feedback capacitor (C_F) on which the charge from the pixel is read out during the readout phase. It also has a reset transistor connected across C_F.

PPS have three modes of operation: reset mode, integration mode and readout mode. In the reset mode, it performs two functions: the reset transistor is turned ON which resets the charge across the feedback capacitor, and the reverse biased voltage across the photodiode in all the pixels is reset to a reference voltage (V_{REF}), for carrying next pixel information. This is done before the decay of charge during the photocurrent integrated phase. During integration, the photodiode discharges the capacitor (C_{PD}) with photocurrent, which is proportional to the amount of incident light illuminating the photodiode. In this mode, the MOSFET is switched ON and the signal accumulates the charge on the photodiode according to the incident photon flux on the pixel. In the readout mode, the modified voltage is sampled from the row to the column capacitor (C_{Oj}) via column charge amplifier and then the pixel values are read from these column capacitors as the PPS output. The PPS has a major disadvantage due to its large capacitive loads, as, the larger bus is directly connected to each pixel during its readout. Therefore, PPS cannot be used for larger array sizes or faster pixel readout rates. Moreover, the photodiode capacitance is very small as compared to column bus and row bus capacitance and this leads to a large noise

component being added to the readout of the photodiode. PPS are more useful for small pixel sizes and for lower cost systems.

2.3.2 Active pixel sensors

The active pixel sensor was introduced by Fossum in 1992 [38] at NASA's Jet Propulsion Laboratory. Active pixel sensors have more than one active transistor, to buffer and amplify the signal and read out the output as a voltage signal. These active transistors boost the photodiode signal fed to the column lines and solves the noise problems of the large column lines observed in PPS. Thus, APS are preferred over PPS because they give a better SNR. Many functionalities can be added to the APS by adding active transistors, which provide advantages like high sensitivity, high readout speed, less power consumption, computability with CMOS technology due to the capability to build more pixel arrays resulting in more SOC integration, and lower cost.

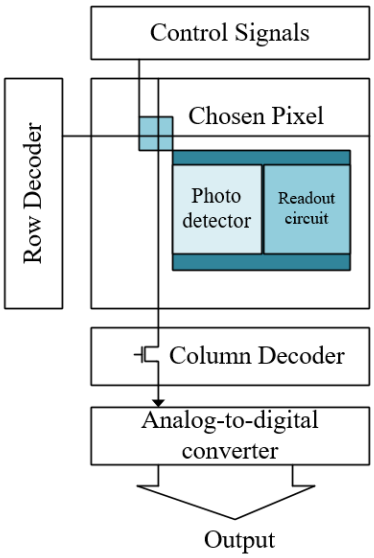


Figure 11 : Architecture of an active pixel sensor

Figure 11 shows the architecture of an APS. As with the PPS, the pixel array forms the core part of the APS. The row decoder and the column detector select the pixel to be read out from the array.

Active pixel sensors are categorized as:

- Photodiode active pixel sensors
- Photogate active pixel sensors
- Pinned photodiode active pixel sensors

2.3.2.1 Photodiode active pixel sensor (3T architecture)

A basic photodiode active pixel sensor is shown in the figure 12. It is also called as a 3T (three transistor) architecture. It consists of a photodiode and three NMOS transistors: the reset transistor, source follower transistor and the row-select transistor.

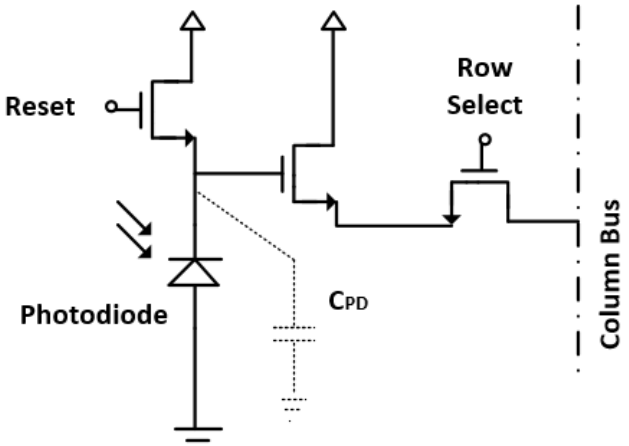


Figure 12 : Photodiode active pixel sensor (3T architecture)

Initially when the pixel is exposed to light, the reset transistor is turned OFF. The photodiode has a junction capacitance C_{PD} associated with it, also known as the sense node capacitance. When not detecting light, the reverse bias voltage across the photodiode is reset to a reference voltage through the reset transistor, which is turned ON. The NMOS transistor yields a lower reset noise as compared to PMOS transistor [37]. When the light rays are incident on the photodiode they are converted into photocurrent through ionization. The photocurrent discharges the sense node capacitor and the voltage at the sense node capacitor decreases depending on the intensity of the incident light. The voltage sensed by the photodiode after light exposure time is transmitted to the source follower transistor which behaves like a voltage buffer amplifier. The source follower transistor is used in each pixel to reduce the pixel to pixel variation. The row select transistor is used to read out the data from the photodiode.

2.3.2.2 Photogate Active pixel sensor (4T architecture)

Figure 13 (a) shows the basic photogate active pixel sensor. It is also known as a 4T (four transistor) architecture for reading out pixels.

Figure 13 : (a) Schematic of photogate active pixel sensor (4T architecture) (b) Modes of operation of photogate

Photogate APS has four modes of operation: reset mode, integration mode, charge transfer mode and read out mode. Before capturing of the image, the photogate APS is reset. In the reset mode, floating node FD of the sensor is reset to a reference voltage of V_{DD}-V_{THN}. In the integration mode, when the pixel is exposed to light, the photogate is turned ON, the incident photons generate charge and they are accumulated underneath the photogate in the potential well as shown in figure 13 (b). In the charge transfer mode, the transfer gate is turned on to an intermediate voltage of approximately $V_{DD}/2$ and the photogate is turned OFF. In this mode, the charge accumulated under the photogate is transferred to the floating node X. The floating node has a well capacity which is determined by the voltage swing and the capacitance of the node (C_D). Charge to voltage conversion occurs during this mode of operation. In the readout mode, the output signal is read by transmitting the signal through the source follower and reading it by turning ON

the row select transistor. The reference voltage is read out from the photogate when the pixel is reset using reset transistor. The difference between the reference voltage and the voltage signal during integration mode gives the output as the light signal detected.

Photogate APS has a higher conversion gain as compared to photodiode APS. The floating node (C_D) is very useful in doing Correlated-double sampling (CDS). The reset and fixed pattern noise observed in this pixel due to threshold voltage variations can be reduced by using a correlated double sampling (CDS). CDS helps improve the dynamic range and the signal-to-noise ratio (SNR) of the photogate active pixel sensor.

There are few disadvantages of photogate active pixel sensor. The shot noise produced due to photogate cannot be removed. The number of transistors are increased to reduce the shot noise effect, but this decreases the fill factor of the pixel, increases the power consumption and the complexity of the circuit.

2.3.2.3 Pinned photodiode APS

Figure 14 shows the structure of a pinned photodiode APS. The operation of a pinned photodiode APS is similar to that of photogate APS; the primary difference being that the photogate is replaced by a pinned photodiode. In the reset phase, floating node FD is reset to a reference voltage V_{DD}-V_{THN}. In the integration phase, when the pinned photodiode is exposed to light, charge is accumulated below the pinned diode. The transfer gate (TX) is pulsed to transport the charge from the photodiode to the floating diffusion node. In the readout phase, signal is read from the floating node FD through the source follower and row-select transistor.

During the charge transfer process, when the charge accumulated under the pinned photodiode is transferred to the floating node FD by turning ON the transfer gate (TX), some electrons are left under the pinned photodiode when the TX transfer process comes to an end. This is known as image "lag". In other words, lag occurs when traces of previous frame appear in the future frame i.e. when the pixel is not completely reset. Moreover, noise reduction can be realized in a photodiode when all the mobile electrons are removed during the reset phase. Pinned photodiode performs the function of resetting the photodiode completely. This is achieved by pinning the photodiode at one end by a p+ implant and this eliminates the image "lag" making it more suitable to detect low signals.

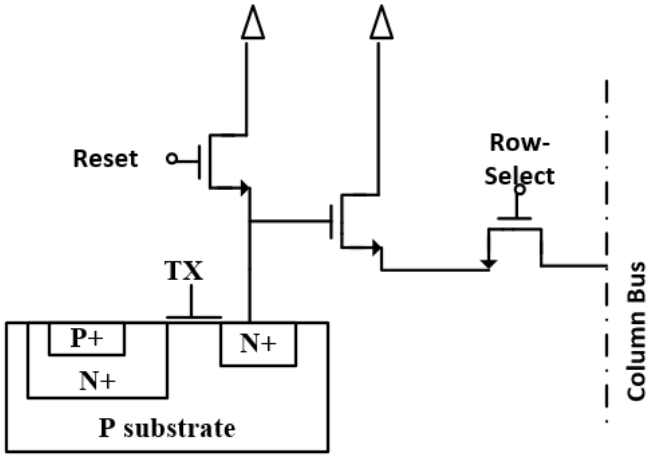


Figure 14 : Pinned photodiode active pixel sensor

A pinned photodiode has four transistors and five control lines. It has a higher fill factor compared to the photogate APS and a lower fill factor compared to photodiode APS. The pinned photodiode is good for removing dark currents, has a higher conversion gain and high sensitivity. A pinned photodiode APS has ability to reduce reset noise levels by using CDS.

2.4 Modes of operation for CMOS sensor

In CMOS image sensors the shutter is controlled by the sensor itself. When the sensor is exposed to light, the readout depends on the type of shutter used. Photo sites are read row by row in rapid succession, then reset between exposures, then read again for the next exposure. Although both technologies record light for the necessary duration, not every portion of the image starts and stops receiving light at the same time. Based on this, the readout architecture feature two types of shutters: rolling shutters and global shutters [39].

2.4.1 Rolling shutter

In rolling shutter mode, all the pixels in the array are not exposed to light simultaneously during the capture of image. For rolling shutter, exposures of pixel array to light moves as a wave from one side of the image to the other as shown in figure 15. Thus, each row in the array will expose to light for same amount of time but will begin the exposure at a different time.

For imaging moving objects, the object size and the speed of the object need to be considered to sample the image properly and to avoid motion blur. If an object moves a significant distance during exposure, image of the object is subjected to motion blur and has to be within limit. In rolling shutter, distortions are observed in the imaging of fast moving objects even with very short exposures that avoid motion blur. Due to the time delay between each row's exposure, it is possible that if an object is moving at a high speed, the relative structure of an object will appear to change.

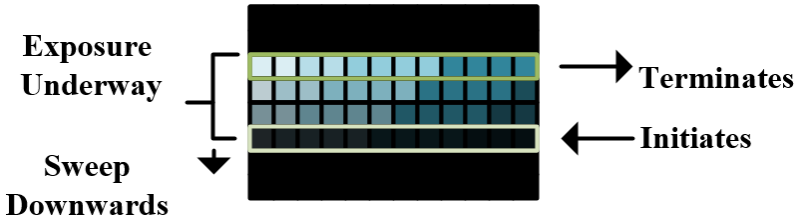


Figure 15: Rolling shutter

Thus, fast-moving objects can appear angled or sheared, and rapid camera movements are more likely to appear as a wobble making rolling shutter more suitable for digitally still cameras.

2.4.2 Global shutter

A global shutter controls incoming light to all the photo sites simultaneously. At any given point in time, all the photo sites are therefore, either equally closed or open. A global shutter works by abruptly exposing and then obstructing all the photo sites at once. Thus, in global shutter mode, exposure of each pixel begins and ends simultaneously.

In global shutter mode, after the exposure is complete, the charge accumulated is sampled on the pixel, the analog front end reads the pixel charges one by one, resets the pixels and gets ready for the next frame. In other words, in a global shutter mode the entire image is captured at the same time and then the readout of information is performed when the capture is complete. This is beneficial when the object is moving at a very high speed. The result is an image with no motion blur and distortion. Figure 16 shows the working of global shutter.

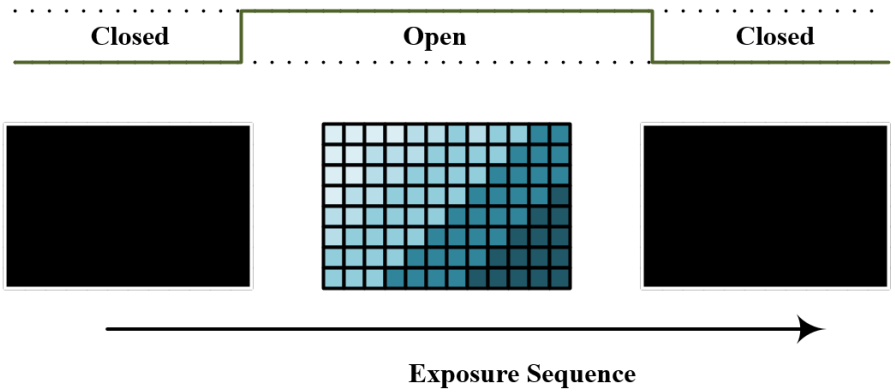


Figure 16: Global shutter

A global shutter is typically considered the most accurate representation of motion and is suitable for high speed imaging.

2.5 6T Pixel readout architecture

For a high speed image sensor with higher fill factor and to enable low light imaging a pixel read out architecture with photodiode and global shutter mechanism was chosen [20]. 6T (six transistor) pixel architecture is shown in the figure 17. It features global shutter has high sensitivity.

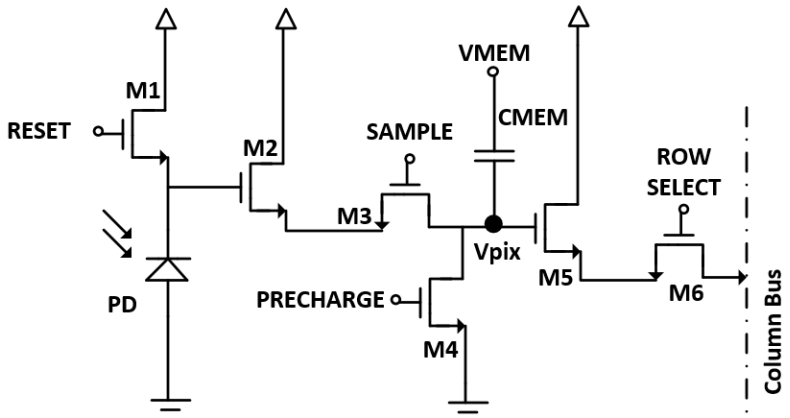


Figure 17 : 6T architecture

2.5.1 Operating principle

The photodiode is reset to a reference voltage when the reset transistor is turned ON. The reference voltage is set to VDD-V_{TH} after the reset operation. In integration mode, the reset transistor is turned OFF and the pixel is exposed to light. The incident photons generate electrons and a photocurrent flows through the photodiode proportional to the incident photon flux. This decreases the voltage at the cathode of the photodiode node. At the end of the integration mode, the signal is obtained at the photodiode node. This signal is then sampled on the C_{MEM} capacitor using the sample and hold circuit which incorporated the first source follower transistor and the sample and precharge switches. The timings of the switches, control the working of the sample and hold circuit. The C_{MEM} capacitor holds the charge till it is read out from the pixel. The signal stored on the C_{MEM} is read by transmitting the signal through the source follower and reading it by turning ON the row select transistor. This is the working principle of 6T pixel read out architecture [20].

The timings for the pixel decide: the integration time, the readout time and the working of the pixel. Figure 18 shows the timings for the pixels.

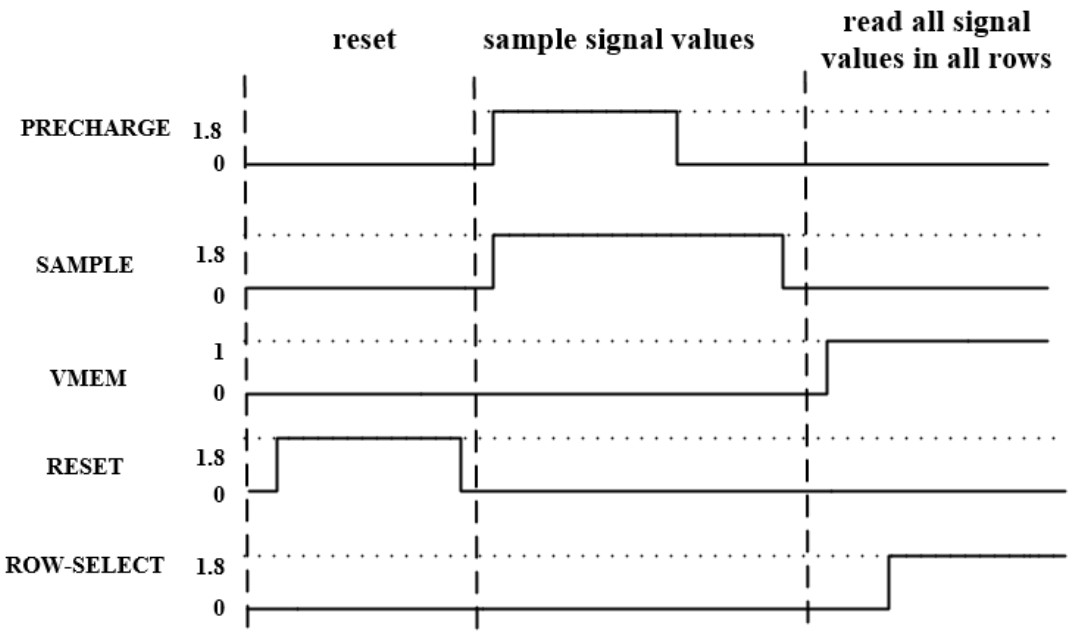


Figure 18 : Pixel timings for 6T architecture

2.5.2 Global shutter mode

The 6T pixel read out architecture features the global shutter mode. In this mode, light integration of all the pixels occurs at the same time. The subsequent read out is a sequential operation. Figure 19 shows the integration and readout sequence for the global shutter. As seen in the figure 19, all the pixels are exposed to light at the same time, the whole pixel array is reset simultaneously and after the integration, all the pixel values are sampled together on the capacitor inside each pixel. The pixel array is read line by line after integration. Integration and readout of the pixel array can be done in parallel or sequentially.

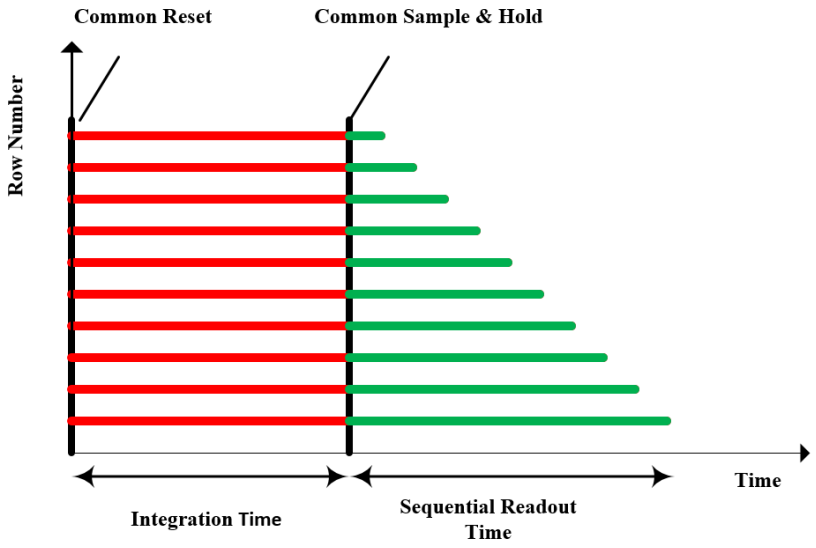


Figure 19 : Global shutter mode of 6T architecture

2.5.3 Problems

2.5.3.1 Leakage

After the exposure of the pixel array to light is complete, the signal is sampled on the C_{MEM} capacitor. This capacitor has to retain the charge stored on it till the readout of the pixel array is complete. Leakage of this charge can occur through various pathways in the circuit. Figure 20 shows the three most important leakage paths in the 6T circuit.

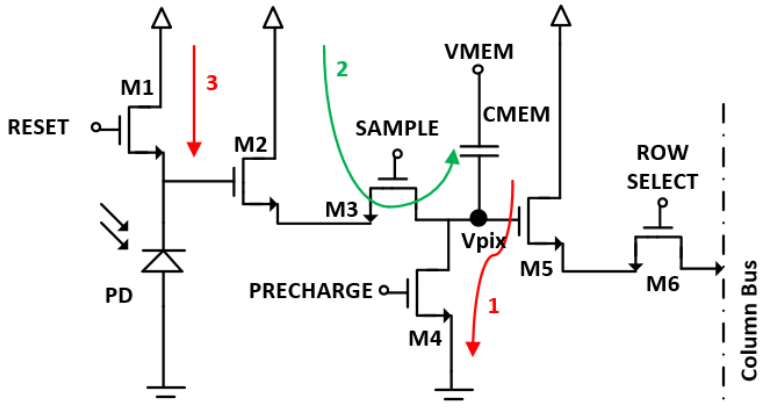


Figure 20 : Leakage paths in 6T architecture

(i) Leakage current occurs through the precharge switch to the ground which decreases the charge on C_{MEM}. This leakage current is shown by 1 in figure 20 and is an undesired leakage.

(ii) Leakage from VDD -source follower 1-sample switch –capacitor path, contributes positively to the capacitor. This leakage path is shown by 2 in figure 20. However, the dominant leakage path is through the precharge transistor, which makes it difficult to read low voltage signals at the input and decreases the image accuracy.

(iii) In the reset phase, the reset transistor is turned ON which resets the cathode of the photodiode to a reference voltage V_{DD}-V_{TH}. During the integration phase, the reset transistor is turned OFF and the pixel is exposed to light. After the exposure is complete, the signal voltage is obtained at the sense node capacitance of the photodiode. However, a leakage current flows from V_{DD} to the cathode of the photodiode through the reset transistor as shown by the leakage path 3 in figure 20. This leakage increases voltage at the cathode of the photodiode, thereby increasing the voltage signal obtained at the node close to the reference voltage. This makes it difficult to detect very low light signals.

Leakage causes problems in image accuracy and makes it difficult for low light and high speed imaging applications.

2.5.3.2 Fill factor

For low light and high speed imaging, the number of photons incident on the pixel array is very low. This leads to less charge generation, which leads to less photocurrent and

less voltage swing at the photodiode node. Quantum efficiency and collection efficiency of the photodiode play an important role in the generation and collection of charge and are dependent on the photodiode material. The area of the photodiode also plays an important role in total number of electrons generated. The greater the area of photodiode, more the electrons generated. Thus, increasing the fill factor plays a very important role in detecting low light signals. The sensor using this 6T architecture has a very low fill factor, which makes it difficult for low light and high speed imaging application.

This research work, deals with minimizing the leakage in the 6T architecture and improving the fill factor to make it suitable for low light and high speed application.

CHAPTER 3

DESIGN

Figure 21 shows the architecture of the camera chip designed which consists of a 96 x 96-pixel array, four 25MSPS 10-bit pipelined ADCs, four programmable gain amplifiers (PGAs), pixel control signal block, column registers and row registers. Each pixel consists of a n+/p-sub photodiode and the designed pixel readout circuit.

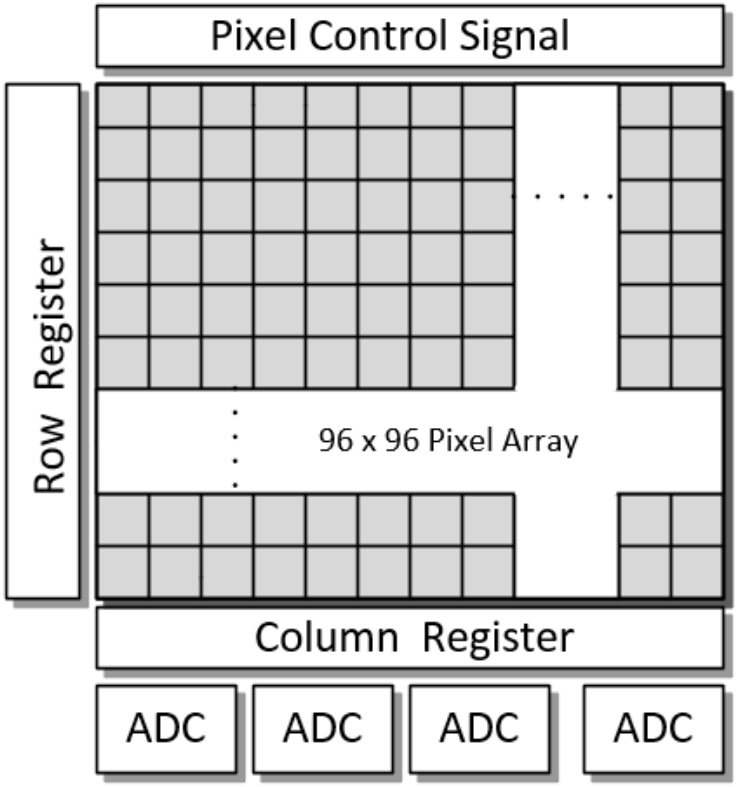


Figure 21 : Chip architecture

The chip operates like a typical CMOS image sensor chip which has three modes of operation: reset mode, integration mode and readout mode. In the reset mode, all the pixels in the array are reset to a reference voltage before the exposure time starts. In the

integration mode, pixel array is exposed to light. After the exposure of light is complete, charge is accumulated under the photodiode depending on the intensity of light incident on it. Charge to voltage conversion is carried out by the pixel readout circuit, then the signal is sampled and stored inside the pixel. In the read out mode, the signal stored in pixel is read out to the PGA by selecting appropriate pixel using the column and row registers. PGA has different gain settings to amplify the signal received from the pixel. The amplified signal is then sent to the ADC where the signal is digitized into a 10-bit value. The ADC digitizes all the pixel values making it ready for signal processing. Pixel control block decides the timing and the operation of the pixel circuitry. Row register and column register decide the pixel to be readout.

The readout time of a pixel is defined as the time required to digitize one pixel. The readout of the pixel is done in two stages: first, the value stored inside the pixel is transferred to the input capacitor of the PGA as shown in the figure 22.b); second, PGA and ADC amplify and digitize the signal. The ADC operates at 25MSPS and reads one pixel in each clock cycle. Therefore, the readout time of the pixel is equal to sampling time of ADC i.e. 40ns. The chip is designed in a way that, the first stage of the read out takes 20ns to read the signal from the pixel to the PGA and second stage takes 20ns to amplify and digitize the signal. The first stage of readout is critical, as it has to drive the RC network of the column line and charge the input capacitor of the PGA. So the pixel architecture has to be designed in a way that it drives the RC network and settles the signal on the PGA input capacitor in less than 20ns. Moreover, for low light and high speed imaging, the fill factor of the pixel plays an important role and needs to be maximized. This implies that the photodiode area should be maximized and the pixel readout circuit should be designed in

a way that the area covered by the circuit is minimized. This sets the design requirements for the pixel readout circuit.

3.1 Chip Architecture

Figure 22 shows the top level illustration of the chip architecture.

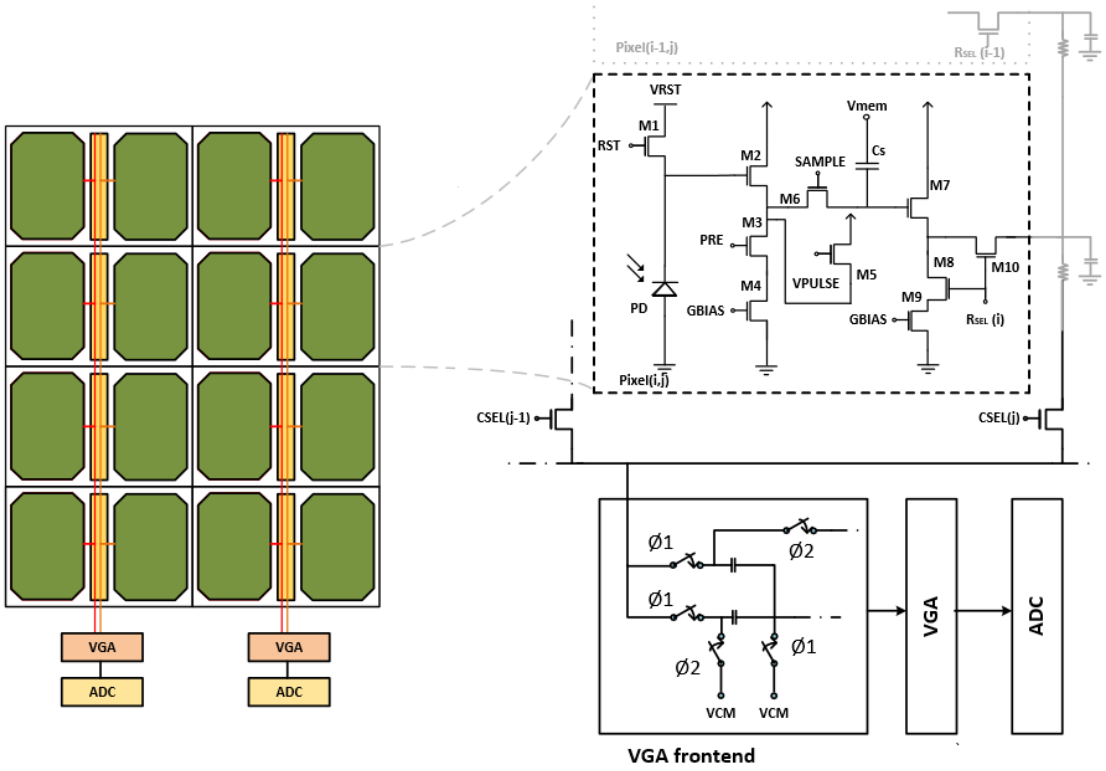


Figure 22:a.) Top level illustration of the chip architecture: the upright round rectangles in green are the light sensitive area, or cathodes of the photodiode. (b) The schematics of the mixed signal readout front-end and the switched-capacitor sampling at the input of the PGA- ADC tandem.

3.1.1 Photodiode

The rectangles in green show the light sensitive area which is the photodiode. The photodiode used is a n+/p-sub photodiode. This photodiode is available in the CMOS process and has a more compact design. Pinned photodiode performs better as compared

to n+/p-sub photodiode, has more sensitivity and requires a more expensive fabrication process.

3.1.2 Pixel readout architecture

Figure 23 shows pixel readout architecture designed to meet the design specification.

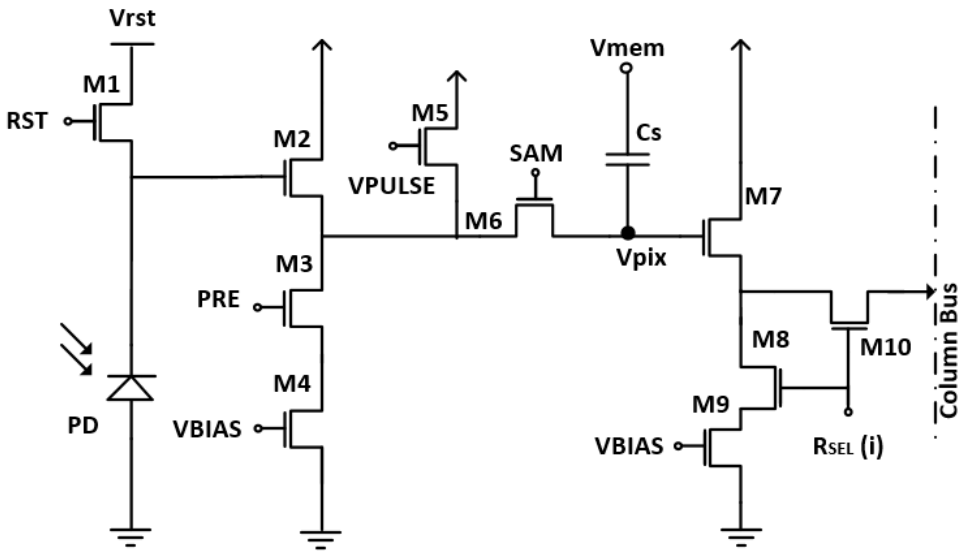


Figure 23: Transistor schematic of single pixel readout

It is an improvement to the 6T architecture shown in Figure 17. This novel pixel architecture designed has ten transistors.

3.1.2.1 Structure of the pixel readout architecture.

Photodiode, the light sensing element of the pixel is shown by PD and is a n^+/p-sub photodiode. M1 is a reset transistor while M2 transistor is a buffer between the photodiode and the sample capacitor (C_S). M3 and M4 are current load to the source follower transistor M2 while M5 transistor is used to minimize the leakage. M6 is a sample transistor used to sample the signal on the capacitor. M7, M8 and M9 are the second source follower which

are used to drive the column. M10 is a row-select transistor which is used to select the pixel for readout. The pixel circuit has eight control signals: RST, V_{RST}, $V_{MEM,}$ VBIAS, SAM, VPULSE, PRE and R_{SEL}(i).

3.1.2.2 Operating principle of pixel readout architecture

The operation of the proposed pixel readout front-end is explained by using the detailed schematics given in figure 23 and the timing diagram of figure 24.

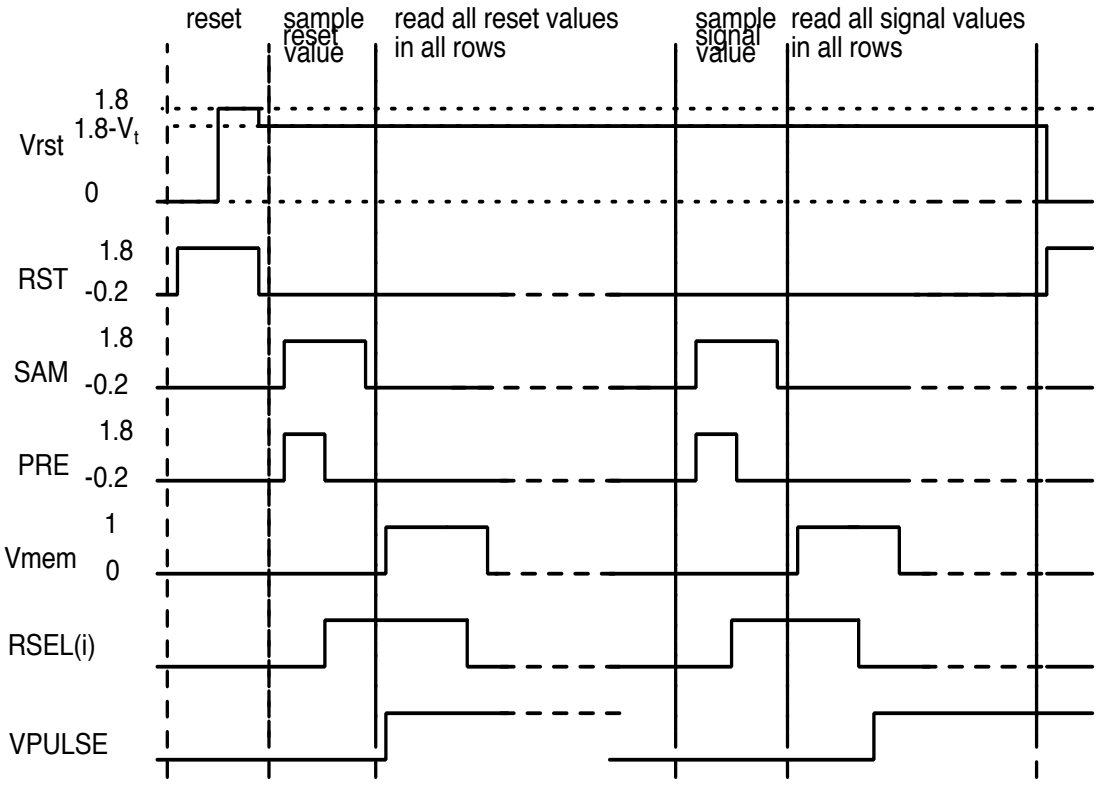


Figure 24: Timing diagram of the pixel readout

Prior to registering its share of an image, the pixel is reset, i.e. the PD is reverse biased by turning M1 on via pulling RST 'HIGH'[1]. In fact, the resetting proceeds in three

[1] A digital 'HIGH' is represented by 1.8V whereas a digital 'LOW' by 0V or ground.

phases: First, the reset signal RST is driven 'HIGH', and the reset transistor M1 starts conducting. At the onset of the RST pulse, voltage V_{RST} is at zero volts, forcing the voltage across the PD to be equal to zero. This essentially eliminates image lag, i.e. erases residual charge that might have been left on the cathode of the PD from the previous sample. During the second half of the reset pulse, V_{RST} is driven to $1.8V$, and the voltage across the photodiode, V_{PD}, is dialed to the reset voltage, approximately $1.8V–V_{TH}$, where V_{TH} is the threshold voltage of the switch transistor M1. The reset voltage is also called as the reference voltage. Once the reset pulse RST is pulled 'LOW', M1 is turned off. It should be noted that the use of an NMOS transistor yields a lower reset noise than a PMOS transistor [37].

After the pixel has been reset and exposed to light, electron-hole pairs generated by incident photons (photocurrent) start to pull V_{PD} towards zero. At the end of the exposure time, the voltage signal obtained at the cathode of the photodiode is V_{PD}. The difference between reference voltage and V_{PD} gives the actual signal incident on the pixel.

After the reset phase, the reset value (reference voltage) is sampled on the MIMCAP capacitor C_S within the pixel. In order to do that, signal SAM is activated first, and then the signal PRE is pulled 'HIGH' so that the voltage V_{PIX} is connected to V_{PULSE} which, at that point, is at ground. Then PRE is deactivated, and the source follower transistor M2 drives the voltage at V_{PIX} to ~(V_{PD} - V_{TH}) or about two threshold voltages below $V_{DD}(1.8V)$. In order to guarantee proper signal range (high dynamic range), the voltage at V_{PIX} is pulled higher by connecting the other terminal of C_S to V_{MEM} following a short delay after the signal SAM is pulled 'LOW'.

The row-select signal, $R_{SEL}(i)$, are activated one at a time and the reset values of all rows are read out and stored digitally outside the chip. Next, the signal value (V_{PD}) of each row of the particular column is sampled in the form of node voltage V_{PIX} and read out and stored onto the off-chip memory similar to what was done for the reset value. The difference between the reset value read out and signal value read out (V_{PD}) gives the output proportionate to the light signal detected. Notice that the sampling of the signal value starts with the second activation of the SAM signal. It should be noted that the second in-pixel source follower stage, M7-M9, also includes the load transistor in order to meet readout speed specifications. As there are four ADCs in the test chip, each ADC reads out a total of 96 × 96⁄4 = 2304 pixels, whether in the reset or the actual signal sampling phases. As the sampling period of each ADC is $40ns$, the sampling period of the whole array is ~$92\mu s$. With the Correlated Double Sampling (CDS), that is explained further below, an effective sample is taken every ~$184\mu s$.

CDS is a method that is used to reduce the effects of background noise from the imaging system; pixel reset value is subtracted from the actual pixel value digitally, effectively performing a high-pass filtering operation. In order to perform correlated double sampling, all reset values need to be read out of the pixel array before sampling the signal to V_{PIX}. Therefore, if the exposure time is longer than $92\mu s$, full CDS is possible for the chip. If the exposure time is shorter than $92\mu s$, CDS cannot be carried out. However, double sampling (DS) is possible. In DS, the reset value is read following the pixel value, and thus the reset and sample values correspond to different frames. Therefore, although DS eliminates *e.g.* offsets from the signal path, it cannot reduce the background low

frequency reset noise.

3.2 Design considerations

In the design of the pixel readout circuit, various parameters are considered to optimize the design. These parameters are discussed in the following section.

3.2.1 Leakage

As discussed in section 2.5.4 the pixel architecture has various leakage paths. Figure 25 shows the three most important (1,2 and 3) leakage paths in the pixel readout architecture.

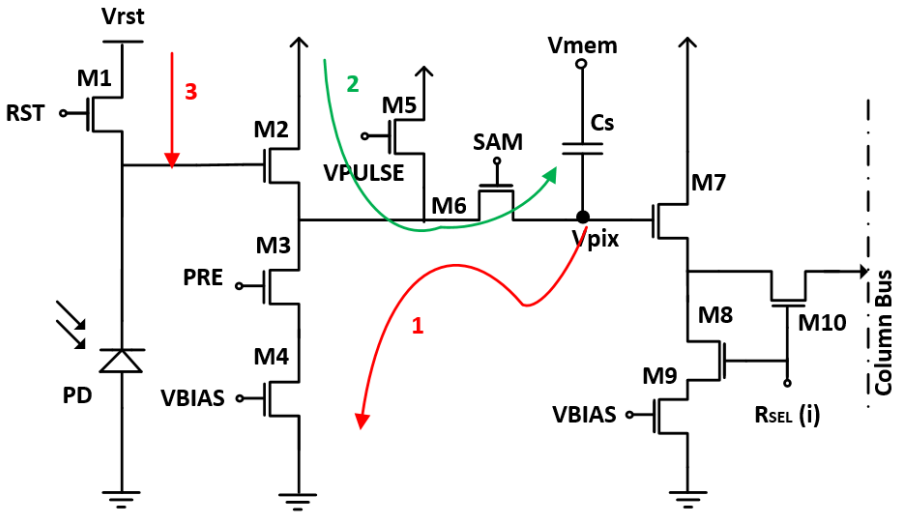


Figure 25: Leakage paths in the pixel readout circuit and the improvements to minimize the leakage

After the pixel has been reset, V_{PD} is dialed to reset voltage of V_{DD}-V_{TH}. Then the RST is pulled 'LOW' and M1 is turned OFF. When the pixel is exposed to light, the electron-hole pairs generated by incident photons (photocurrent) start to pull V_{PD} towards

zero. However, in addition to this photo-generated current, there are unwanted current components that need to be minimized as shown by 3 in figure 24. This leakage current through the reset switch start to pull V_{PD} voltage towards the reset voltage. This makes it difficult to read low light signals which provide a very small swing at the input. Thus, to be able to detect low light signals, this leakage current needs to be minimized. The value of this leakage current is around 1-5pA.

This leakage current is minimized by pulling the RST below ground level by ~0.2*V* after reset. This makes it completely OFF. Moreover, V_{RST} is driven towards the reset voltage so that the voltage across the reset switch (and thus its current) is minimized. This basically involves the principle of making ΔV (V_{DS}) across the reset switch approximately zero which minimizes the subthreshold current. V_{RST} is therefore set to V_{DD}-V_{TH}. This is a tunable voltage and can be tuned to minimize the leakage. This improves the leakage current to 24fA.

In the pixel readout circuitry, memory capacitor Cs plays an important role. The voltage across the memory capacitor is the actual light signal captured and is the actual input to the ADC. Therefore, the charge retention capability of the capacitor is important.

After the global shuttering of the pixel array is done and the integration time of the pixel is over, the input signal is sampled and stored on the memory capacitor. Thus after the global shuttering, the time required to readout the pixel array is ~92us. Therefore, the time required to read the last pixel is 92us. So, the memory capacitor has to retain the charge for a period of 92us.

The transistor used as switches to time the readout of consecutive pixels is not ideal and pass current in their OFF states. There is leakage of charge through the transistors along path 1 and 2. So, the amount of charge lost due to leakage between the readout of the first pixel and the last pixel is important. V_{PIX} node keeps charging through path 2 and loses charge through path 1. Thus, when the PRE and SAM transistors are turned off, V_{PIX} node voltage starts dropping due a leakage current flowing from the V_{PIX} node to GND through the PRE transistor. This voltage drop makes it difficult to read small signals at the input.

To overcome this leakage problem two transistors are added in the pixel readout circuit. One transistor is added in series with the PRE transistor whose gate is controlled by the GBIAS control signal. This transistor has large length to increase the resistance path for the leakage current. One more transistor is added at the drain of the PRE transistor whose gate is controlled by the V_{PULSE} signal. The drain of this transistor is connected to VDD. When SAM and PRE are turned off, V_{PULSE} drives the node to VDD. This decreases the leakage current from V_{PIX} node and thus allows to read lower input voltages.

Figure 26 shows the total drift of the V_{PIX} node for a period of 92us is 777µV or less than 976µV which corresponds to 1LSB of a 10-bit ADC with 1Vp-p full dynamic range.

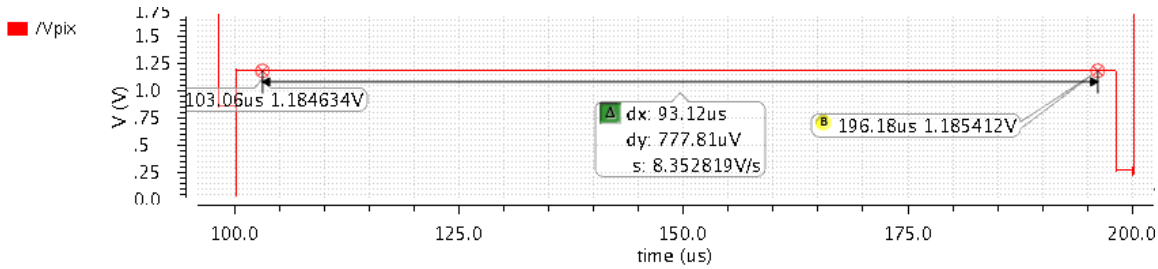


Figure 26:Voltage drift at the memory node due to leakage of the sampling transistor.

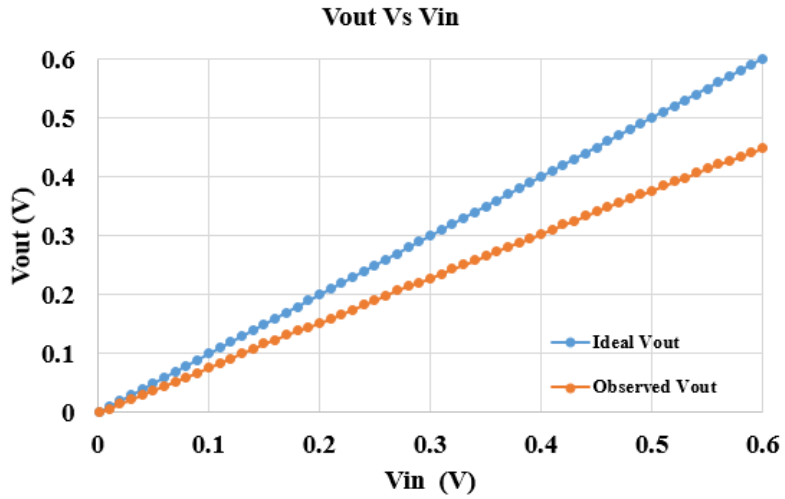
3.2.2 Gain

The design of the pixel readout circuit consists of all NMOS transistors with their bulk tied to ground. The signal at the gate of the source follower depends on the intensity of incident light. Depending on incident input light signal, V_{TH} variation is observed in the source followers due to the body effect. Thus, non-linearity is introduced in the circuit due to the two source followers and switches. The source followers and switches used are not ideal and the output column line being a RC delay line, there is voltage loss along the path. This leads to an offset between V_{IN} and V_{OUT}, where V_{IN} is the input signal voltage observed at the PD (difference between VPD and reset voltage) and V_{OUT} is the voltage at the input of the PGA (difference between reset voltage and VPD voltage read at this node). The gain of the pixel architecture designed is tested by carrying out transient simulations for different input voltages.

Table 2: Incident input voltage at the cathode of the photodiode Vs ideal and observed output voltage at the PGA node

V_{IN} (mV)	Ideal V_{OUT} (mV)	Observed V_{OUT} (mV)
1	1	0.643
10	10	6.16
100	100	76
200	200	152
300	300	228
400	400	303.79
500	500	377
600	600	449

(a)



(b)

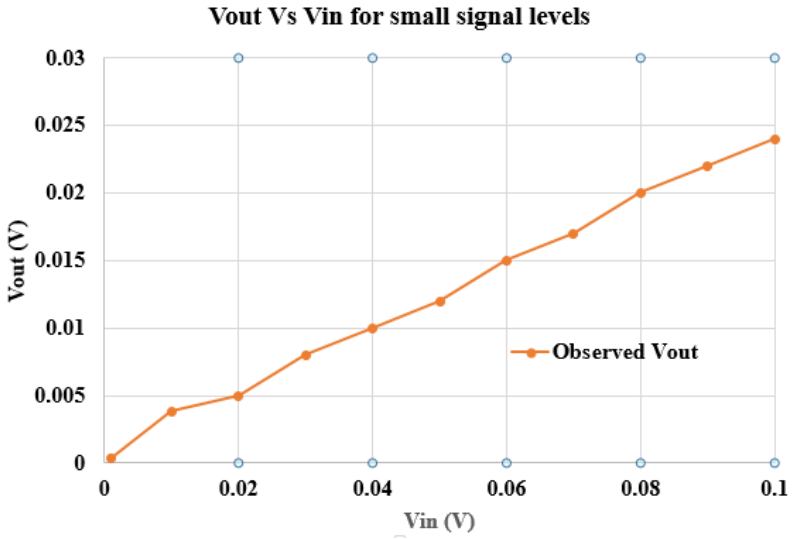


Figure 27 (a) Plot for incident input voltage at the cathode of the photodiode Vs ideal and observed output voltage at the PGA node (b) Plot for small incident input voltage at the cathode of the photodiode Vs observed output voltage

Table 2 and figure 27 show that there is an offset observed at V_{OUT}, for an incident input voltage. Figure 27 (a) shows the ideal VOUT and observed VOUT. As seen from

figure 27(a), V_{IN} and ideal V_{OUT} follow a linear behavior showing that the gain is constant. The observed V_{OUT} also follows a linear behavior which indicates that the gain is constant for the designed pixel readout circuit. Figure 27(b) shows the linear behavior of the circuit for small signal values. Thus, the pixel readout circuit has a constant gain for a range of input signals.

3.2.3Capacitor types and their characterization

(i) Capacitor value

The value of the capacitor is calculated using KT/C noise of the ADC. Equation 1 and 2 are used to calculate the value of the capacitor.

Equation 1

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

Equation 2

$$C \geq 12\, k_B T \left(\frac{2^B - 1}{V_{FS}}\right)$$

Where,
kB, Boltzmann constant = 1.38 x E-23 J/K
T= 300K
B= 9 bit
VFS= 1V

The capacitor value should be more than 13fF. A capacitor value of 30fF is chosen.

(ii) Capacitor types

In the pixel circuit, memory capacitor CS is used to retain the charge sampled from the

photodiode till the pixel is readout. One terminal of the CS is connected to V_{MEM} and after the signal is sampled on the capacitor, this terminal is switched to a higher voltage. So, it is important that the capacitor value should be same for different voltages across the capacitor. Three types of capacitors are considered.

a.) MOS capacitor

b.) Poly capacitor

c.) Metal-insulator-metal (MIM) capacitor

To observe the change in the capacitance as a function of voltage, C-V characteristic are plotted for different capacitor types as shown in figure 28. It can be seen from the figure that there is 60% variation in the capacitor value across voltage range for a MOS capacitor and Poly capacitor which is unacceptable. Monotonous change of this capacitor by the terminal voltage hints at the possibility of calibration. However, MIM capacitors stay very constant across the voltage range of 4V and provide a high linearity and high density.

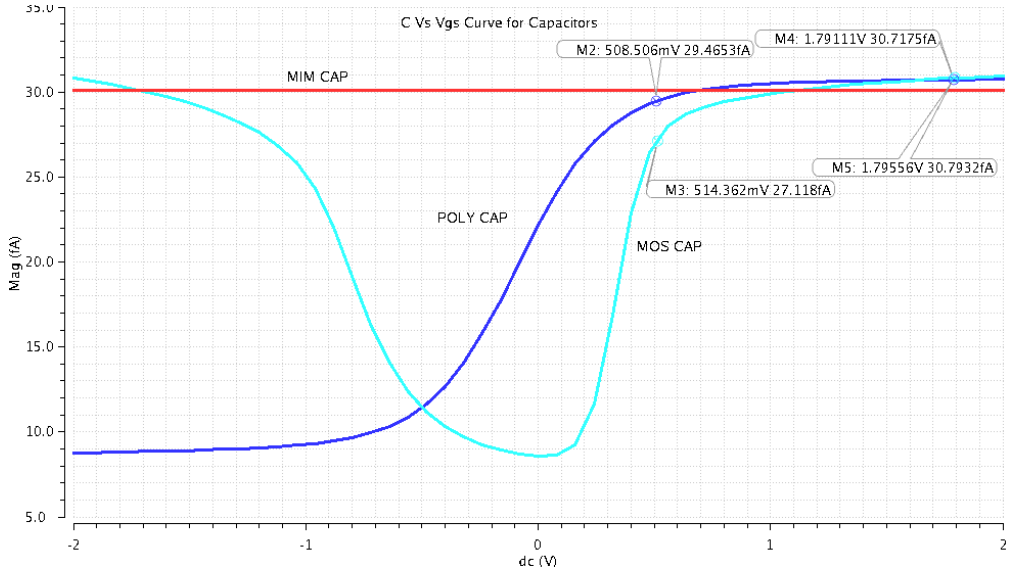


Figure 28: Capacitance Vs Voltage curve for the MOS, Poly and MIM capacitor

The capacitors C-V curve is simulated across the process corners to observe the change in the capacitance. It can be seen from figure 29 that the capacitance of MIM capacitors change considerably across the process corners for a given voltage. Yet, for a given process corner model they do not exhibit great variation across the voltage span. The absolute value of the memory capacitor is not critical as long as that cap charges and discharges in half a clock cycle which is about 20ns long.

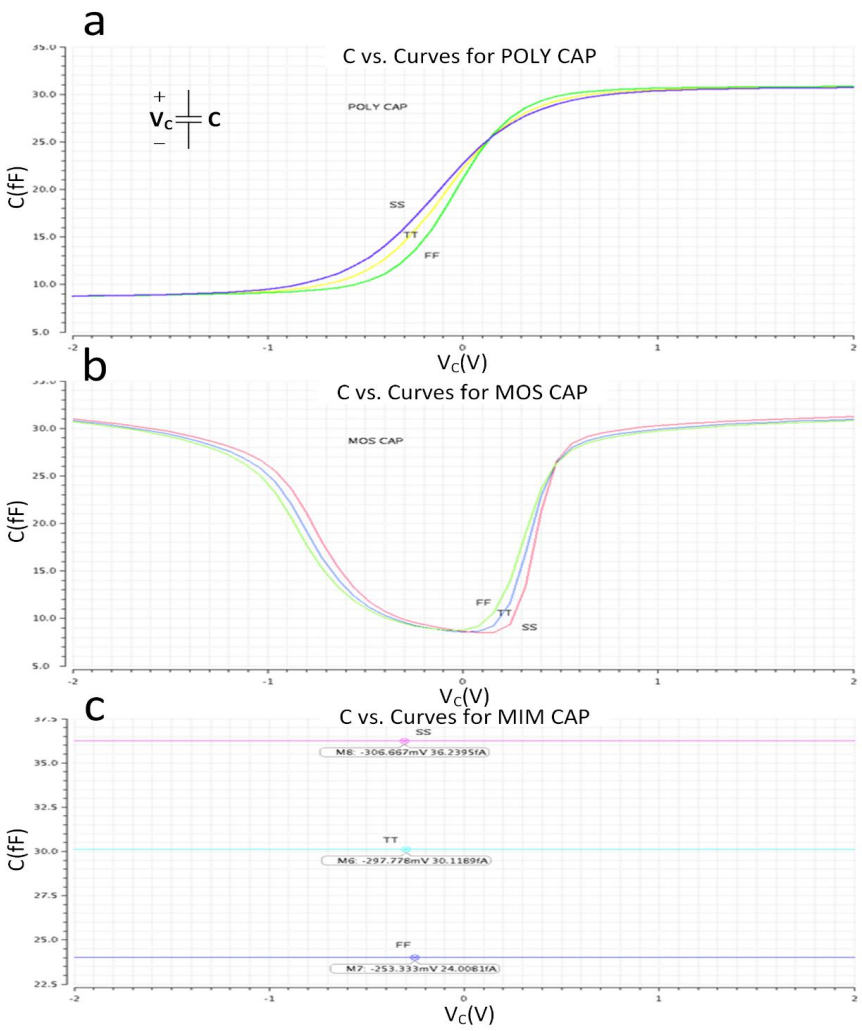


Figure 29:Capacitance Vs applied voltage across all corners for Poly, MOS and MIM capacitors

(iii)Layout of the capacitors

One of the aspects used for comparison of the capacitors is the layout sizes of the capacitors to obtain a 30fF capacitance. Table 3 shows possible ways of obtaining a 30fF capacitance. For MOS and Poly capacitors, three different aspect ratios are provided.

Table 3: Various ways of obtaining a 30fF capacitor

CAPACITOR	W	L	Layout Dimensions
MOS CAP 1	6μm	600nm	2μm x 7.61μm
MOS CAP 2	16.2μm	200nm	1.6μm x 17.81μm
MOS CAP 3	3.65μm	1μm	2.4μm x 5.26μm
POLY CAP 1	5.5μm	600nm	2.42μm x 7.52μm
POLY CAP 2	15μm	200nm	2.02μm x 17.02μm
POLY CAP 3	3.3μm	1μm	2.82μm x 5.32μm
MIM CAP	3.7μm	1.5μm	5.5μm x 8.5μm

Considering all these factors, MIM capacitors is chosen as the memory capacitor for its high linearity, high density of 5.6fF/um2 and layout size.

3.2.4 Readout of Pixel array

The pixel architecture with control lines, output lines and source follower as a column driver is modeled as shown in figure 30.

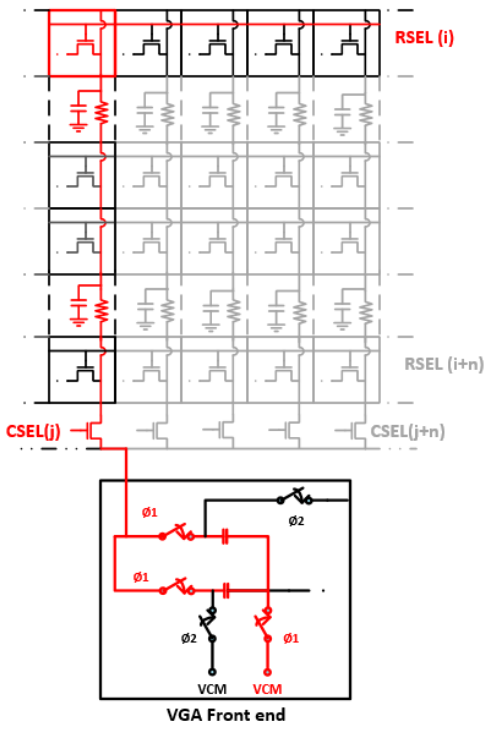


Figure 30: Top level illustration of the readout of the pixel with modelling of resistance and capacitance

After the exposure of the pixel is complete, image is sampled and stored in the memory capacitor C_S. For high frame rate operation, the image stored in the memory capacitor is scanned at a very high speed. The read out path of the capacitor is via source follower, row select transistor and column bus. When a pixel in the column is being readout, the row select transistor of all the other pixels in the column are turned OFF. This introduces a load capacitance on the column line. Moreover, the metal lines used for routing the column lines have a sheet resistance. Thus, the pixel control line can be modelled as a distributed or lumped RC line [8]. Figure 30 shows the readout path of a pixel with RC network and the input capacitor at the VGA front end. For high speed operation, column line plays an important role as it is operated at line frequency which is the ADC operation frequency of 25MSPS. Resetting and sampling of the image on the

memory capacitor is done only after the image capture, which occurs only once in each frame and can operate at slower timing. Thus, it is important that the column line should be designed for low load capacitance and resistance.

When read out of the pixel is complete, it has to drive the RC network and settle the signal on the input capacitor of the front end of VGA in less than 20ns. This is the critical part of the readout time and therefore a fundamental limitation for the frame rate of an image sensor. [25] specifies the limiting factors of the readout of the image sensor being the RC delay of the pixel pulse wire and pixel output wire. Considering the architecture of the chip, pixels in the first row of the array are the farthest from the ADC. Thus, they have to drive the load capacitance and resistance of the entire column, making it the limiting case for readout time of the pixel. In this thesis, the pixel from the first row are simulated for the readout time and time to settle on the input capacitor of the front end of the VGA is observed. This time is referred to as settling time and a settling time of 5RC time constants is considered. The settling time should be less than 20ns across all corners to readout one pixel as the time to readout the signal from the memory capacitor to the VGA is limited to 20ns.

Moreover, the position of current source for the source follower driving the column line plays an important role [25]. The pixel source followers ae required to allow sufficiently large current in the order of 60uA in order to drive the RC network. The position of the current sources is determined by considering the voltage drop on the pixel output wire, linearity at the output observed and settling time. The current sources considered were in-column current source and in-pixel current source. The settling time

and linearity at the input of the VGA was observed for both the cases. Figure 31 shows the schematic for in-column and in-pixel current source.

It was observed that for in-column current source, the steady state current of the pixel source-follower flows on the pixel output wire which causes a different voltage drop at the pixel output wire for different rows and leads to shading of image. This also decreases the linearity observed at the input of the VGA. While in the in-pixel current source the steady state current flows inside the pixel and does not flow on the pixel output wire. This leads to same readout voltage for all rows [25] and gives better linearity as compared to in-column current source.

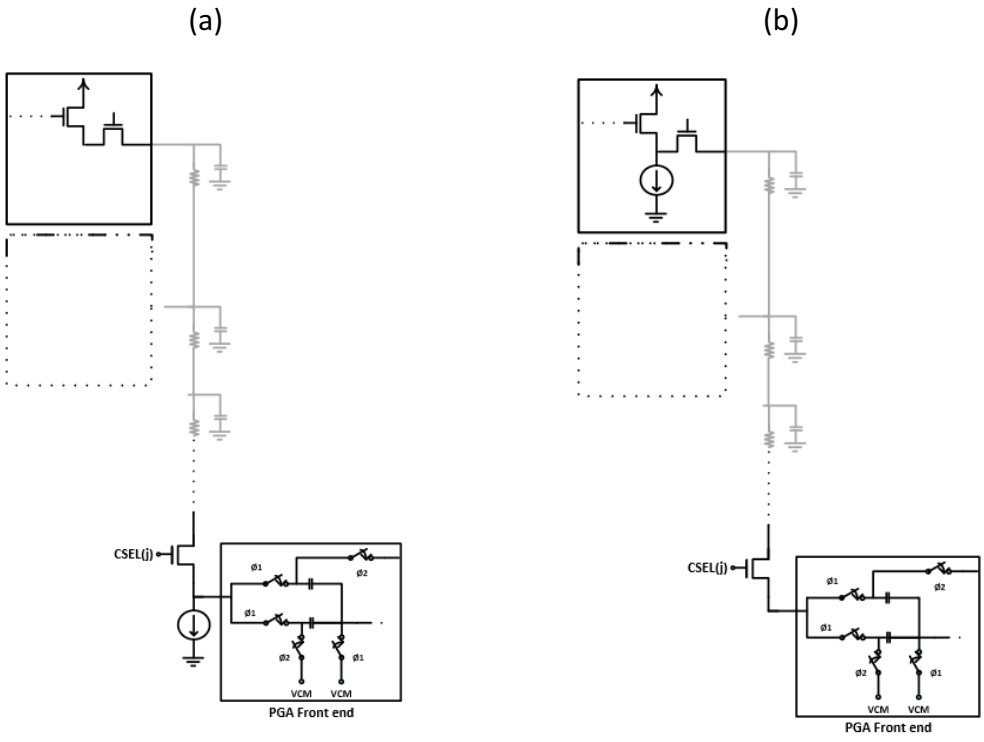


Figure 31: (a) Schematic of in-column current source for source follower (b)Schematic of in-pixel current source for source follower

In-pixel source follower was selected to avoid shading of image and obtain a settling of

less than 20ns. Settling time was considered to be 5RC constants and was achieved to be less than 18ns across all corners.

3.2.5 Layout of the pixel

The size of the pixel used to design the image sensor is 20µm x 20µm. The main aim of the layout is to maximize the fill factor of the pixel by maximizing the photodiode area and minimizing the pixel readout circuit area. Pixel readout circuit consists of 10 transistors, 7 control signals for the pixel, MIM capacitor, VDD line, GND line and interconnects between transistors. As shown in figure 32, layout of the pixel readout circuit is done in a way that the transistors and their interconnection use metal 1, control signals use metal 2, MIM capacitor uses metal 3, metal 4 and metal 5; VDD and GND lines use metal 6. This way the pixel is made dense and area is minimized. Figure 33(a) shows the structure of the pixel where the photodiode area is 220µm^2 and the readout circuit area is 180µm^2. This gives a fill factor of 55%.

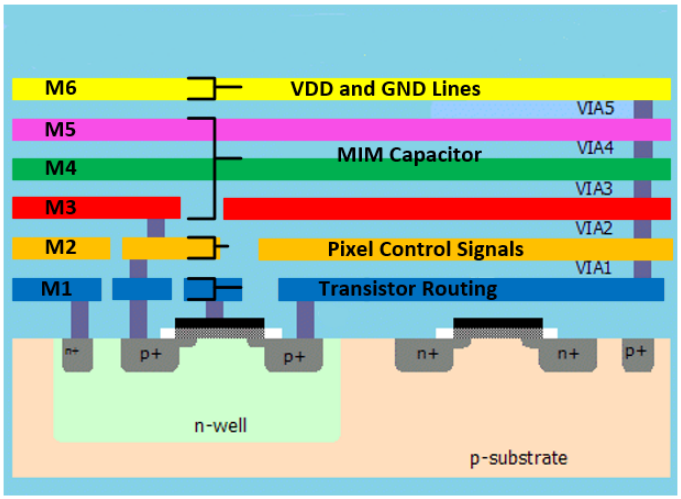


Figure 32: Layout structure for the pixel readout circuit indicating the use of metal layers for different components of the pixel readout circuit

Limitation in the layout of the pixel

Figure 33(b) shows the main limitation for layout of the pixel read out circuit being the width of the pixel readout structure which is limited by the control signals and the V_{DD} and GND lines.

- The minimum width of Metal 2 for the control signal is 0.4μm and the minimum metal-to-metal spacing for metal 2 is 0.28μm. There are eight metal 2 routings for the pixel read out. This gives a total width of 5.44μm.
- V_{DD} and GND lines are routed using metal 6. The minimum width for metal 6 is 2.5μm and the minimum metal-to-metal spacing for metal 6 is 2μm. There are 2 metal 6 lines of V_{DD} and GND spaced at a minimum distance as shown in figure 33(b). This give a total width of 7μm.

Thus V_{DD} and GND lines are the limiting case for the area of the readout of the pixel circuit and thus limit the fill factor.

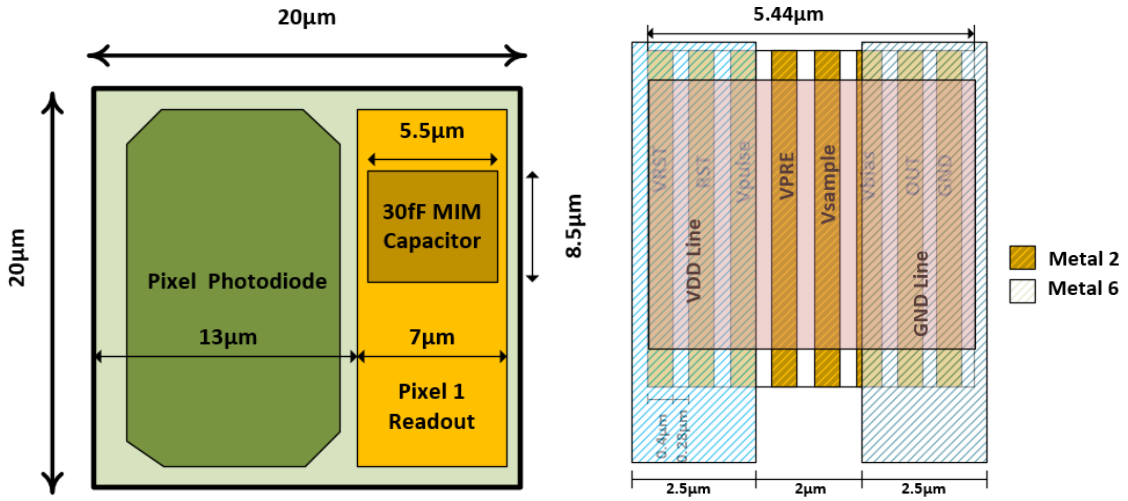


Figure 33: (a) Structure of the pixel with the photodiode and the readout circuit (b) Routing of the control signals showing the limiting case for width of the readout circuit

3.2.5.1 Principle of pixel sharing:

To improve the fill factor more than 55%, a novel layout technique is used. It involves the principle of sharing the control signals between two adjacent pixels and sharing the area for the readout circuit. Figure 34 shows the pixel sharing principle implemented in the chip.

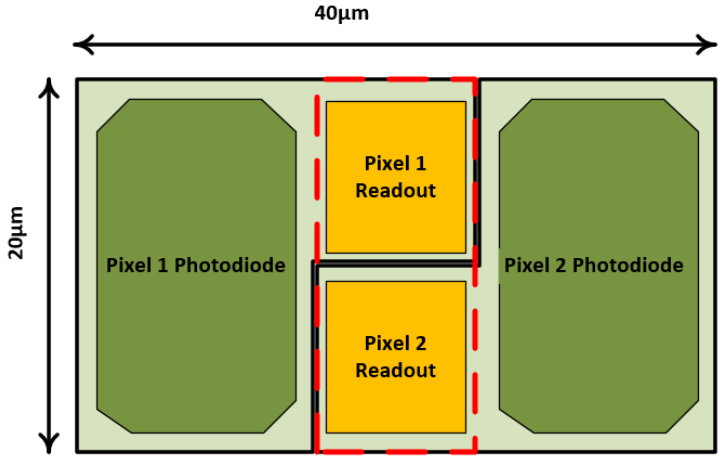


Figure 34: Illustration of pixel sharing principle.

The layout of the pixel is done in such a way that two adjacent pixels share a common read-out circuitry. This effectively allows more area for the photodiode as the control lines are shared between two columns, thereby increasing the fill factor. Pixel sharing technique improves the fill factor to 64.625 %.

CHAPTER 4

RESULTS

The high speed image sensor is designed and fabricated in 0.18 µm CMOS process. This chapter gives the summary of the calculations, the simulation results, layout and the post-layout results of the chip.

4.1 Settling time of the pixel

One of the main parameters in this design is the delay from the end of the exposure time to the time instant the voltage appears on the sampling capacitor of the PGA. This delay is the settling time of the pixel and determines how fast the pixel information can be read out. As shown in the figure 35, the settling time is measured from the time row-select signal is turned on till the signal settles up to 5RC constants on the input capacitor of the VGA.

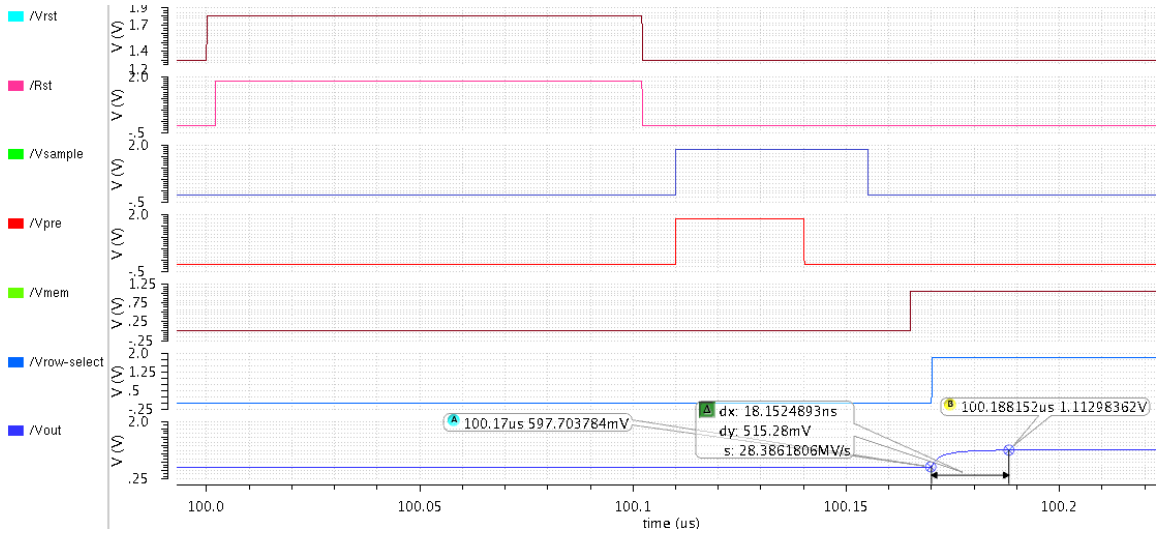


Figure 35: Pixel timings and settling time

As the ADCs are connected to the columns with 96 pixels, the parasitic capacitor associated with 96 row-select transistors forms the main load. Moreover, each metal line (metal 2 is used for routing control signals) has a sheet resistance which is 82mΩ/square. Now as each pixel is 20μm long, the metal line passing each pixel will have a resistance of 4.1Ω. The metal wire was modeled and pixel readout was simulated for this configuration in Cadence.

(i) Resistance Calculation

Metal wires used for routing the control signals and output wire to the PGA, row-select transistor and column select transistor contribute to the resistance the pixel has to drive. Total resistance contributed by the metal routing for a 96-pixel column in 96 x 96 pixel array is 393Ω, by the row-select transistor is 2.2kΩ and by the column select transistor is 550Ω. The dominant contributor being the on resistance of the row-select switch. Therefore, the total resistance that the first row pixel need to drive is 2.3kΩ.

(ii) Capacitance calculation for each pixel

During the readout of every column, only the desired pixel's row-select transistor is turned ON that is being read at a particular time instant. Thus, capacitance is contributed by the row-select transistors of the 95 pixels that are turned OFF. Moreover, the column-select transistor and coupling capacitance between the control signals also contributes to the load capacitance on the pixel being readout. The total capacitance that the first row of pixel needs to drive is calculated to be 1.817pF including the 200fF input capacitance of the PGA.

(iii) Delay calculation

A signal is passed from the first transistor and the time delay to reach the output is calculated. The output is sampled at 20ns from the time signal is send. So the output need to settle to 9bits of accuracy (in terms of linearity) in less than 20ns. Total delay calculated to settle to 5RC time constants is 20.8ns.

(iv) Settling time observed

As shown in the Cadence spectre simulation results Figure 36, the settling takes less than 18.06ns. Layout is performed carefully to optimize delay and settling accuracy. The post-layout simulation Figure 37 shows a settling time of 18.829 ns which is equal to that of the schematic simulation still maintaining the accuracy of 9-bits (in terms of linearity). The calculated value, schematic simulation and post-layout simulation show consistency.

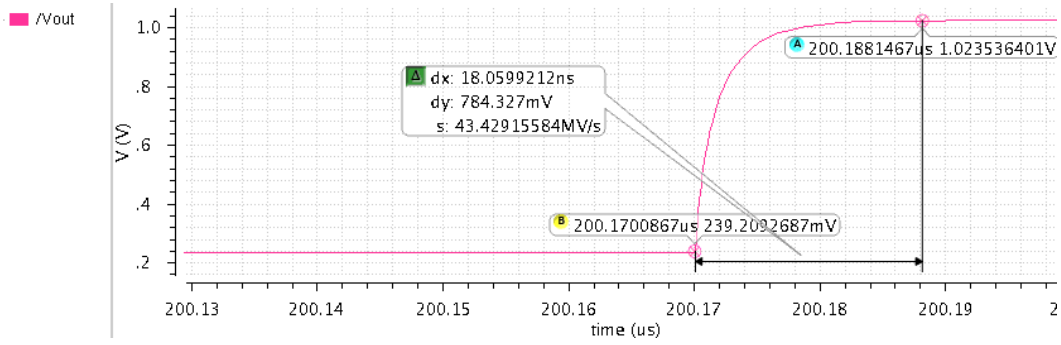


Figure 36: Schematic simulation showing the settling time of the first row of pixel

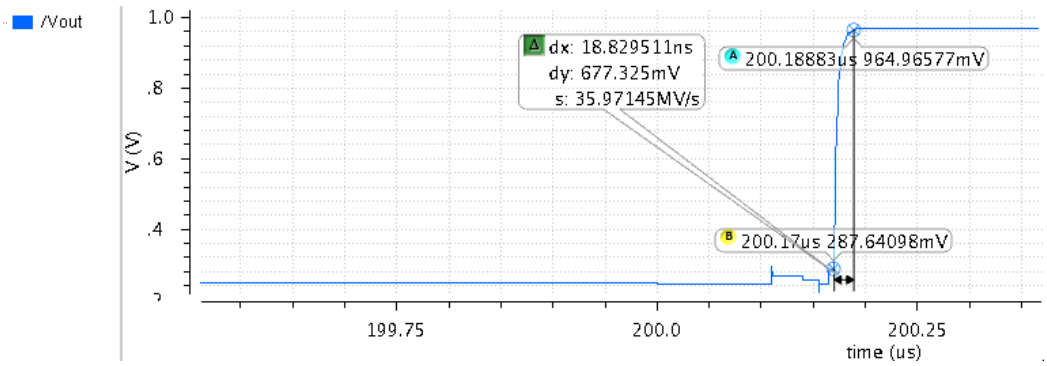
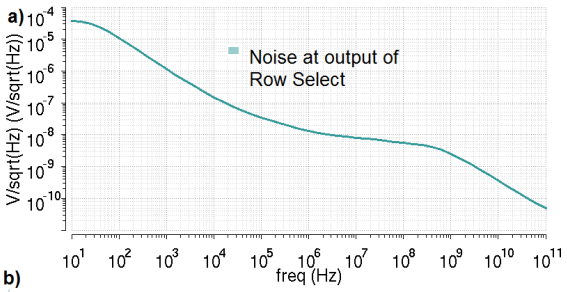


Figure 37: Post-layout simulation showing the settling time of the first pixel

4.2 Noise Analysis

Noise analysis is one of the critical aspects in the design of the image sensor. The image sensor is designed to have a large dynamic range as well as detect signals as small as few millivolts. The complexity in identifying small signals is that the system should generate very low noise. ADC is a 10-bit ADC with signal swing of 1Vp-p. This means the noise floor is around 1mV ($1V/2^{10}$). Thus signals smaller than 1mV cannot be detected. In order to minimize the noise and detect smaller signals, PGA is designed in a way that it uses larger sampling capacitors and keeps the noise level low. Moreover, PGA gain can be tuned to reduce the noise at the input of the PGA plus ADC system and also provide variable gain factor for good dynamic range (meaning smaller signals are amplified to fit in to ADC's dynamic range, ADC's dynamic range being 1mV to 1V). Figure 38 shows the noise at the output node of Row Select switch and is 173µV/√Hz. The noise contribution from the column select switch (M28), as shown in Figure 38 b) is 85uV.

a)



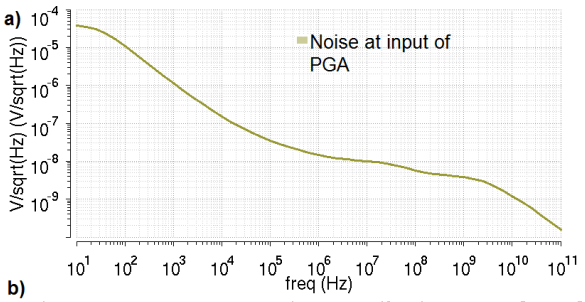
b)

Device	Param	Noise Contribution	% Of Total
I13.MM7.mds	id	0.000103324	35.43
M28.mds	id	8.50133e-05	23.99
I13.MM6.mds	id	6.46579e-05	13.88
M257.mds	id	4.29289e-05	6.12
I13.MM0.mds	id	3.66165e-05	4.45
M256.mds	id	2.88558e-05	2.76
I13.MM6.mds	fn	2.8638e-05	2.72
M258.mds	id	2.81537e-05	2.63
I13.MM23.mds	id	2.05597e-05	1.40
I13.MM23.mds	fn	1.77949e-05	1.05

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000173578
No input referred noise available
The above noise summary info is for noise data

Figure 38 : a) Noise plot at the output node of row select switch b) Top 10 noise contributors at this node.

The noise at the input of the PGA as shown in Figure 39 and the noise is increased to 296µV/√Hz. The noise contribution from the column select switch (M28) is the dominant factor and increased to 175µV/√Hz at the input of PGA. This is because of the parasitic resistance of the routing metal from row select switch to column select switch, which contributes to the noise through M28. PGA and ADC system are designed in a way to lower the noise observed at the PGA input. Thus, figure 38 and figure 39 show the noise contribution from the pixel readout circuit and the column line at the PGA node is approximately 296µV/√Hz. Considering the attenuation of the signal along the readout path, the pixel readout circuit can detect signal as low as 350µV at the cathode of the photodiode for a very low SNR.



b)

Device	Param	Noise Contribution	% Of Total
M28.mds	id	0.000175586	35.08
M257.mds	id	0.000130039	19.24
M256.mds	id	0.000120745	16.59
M258.mds	id	0.000119123	16.15
I13.MM7.mds	id	6.17005e-05	4.33
I13.MM6.mds	id	3.9473e-05	1.77
I13.MM0.mds	id	3.66163e-05	1.53
I13.MM6.mds	fn	2.75344e-05	0.86
I13.MM23.mds	fn	1.71097e-05	0.33
I13.MM155.mds	fn	1.48875e-05	0.25

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000296458
No input referred noise available
The above noise summary info is for noise data

Figure 39: a) Noise plot at the input node of PGA (which is also the output node of column select switch b) Top 10 noise contributors at this circuit node.

4.3 Minimum exposure time

The daylight (not direct sunlight) illumination can be quantified as 10,000 to 25,000 lux. Bright sunlight can provide up to 120,000 Lux on the surface of the earth. For this image sensor, it is assumed that the illumination level is 10,000 Lux for the calculation of minimum exposure time. 10,000 Lux is approximately 15W of visible light power over a $1m^2$ area, which translates to 15pW over a $1\mu m^2$ pixel area.

If an object is assumed to be a Lambert surface, and the tests are carried at 10klux (cloudy midday), only 60 Lux, equivalent to $90mW/m^2$ or $90fW/\ \mu m^2$, is observed at the surface of the sensor. Thus, a 1 μm^2 pixel area receives 9E-20 joules of photon energy over a 1µs exposure time, whereas a 20x20 μm^2 pixel receives 36E-18 joules of photon energy. The energy of a visible photon (green) is approximately 3.5E-19 joules, and 400 μm^2 area thus receives 102 photons every microsecond. 33 electrons will be generated every

microsecond for a pixel quantum efficiency of 50% and a fill factor of 65%. The quantum efficiency and fill factor limited signal-to-noise ratio (SNR), calculated for 1µs exposure time, arising from photon noise, also known as the Poisson noise is $20*\log(N/\sqrt{N}) = 15dB$ which is for a 20µm x 20µm pixel. However, with large area pixels (20µm x 20µm) and low light levels, the readout noise tends to dominate the photon noise. Thus, the minimum signal detected is limited by the readout noise and is calculated to be 350µV. The capacitance of the photodiode is 39fF. This gives a minimum exposure time of 2.58µs for daylight condition and a full well capacity of $121ke^-$ for the sensor. For an exposure time of 2.58µs, 263 photons are captured and generate electrons, and the SNR is 24dB which is approximately 3.69 bits. The SNR for the pixel readout circuit can be increased by increasing the exposure time.

4.4 Readout rate and frame rate

Readout rate is defined as the inverse of readout time of the pixel array, that is, the time required to digitize all pixels. Readout rates are usually given in pixels/second.

Readout time for one pixel is 40ns and one ADC reads 2304 pixels. Therefore, the total readout time is 92.16µs. For an exposure time of 3µs in daylight condition, the time required to read one frame is 95.16µs. Therefore, the frame rate for the image sensor is 10508 fps at full resolution. Thus the frame rate of the image sensor is 10508 fps and the readout rate is 96 M pixels/sec.

4.5 Layout of the pixel

The layout of the pixel based on the principle of pixel sharing is shown in figure

40. The control signals of V_{RST}, RST, V_{MEM}, V_{BIAS}, V_{PULSE}, PRE, Row-select are shared between the two adjacent pixels. This helped in increasing the fill factor of the pixel.

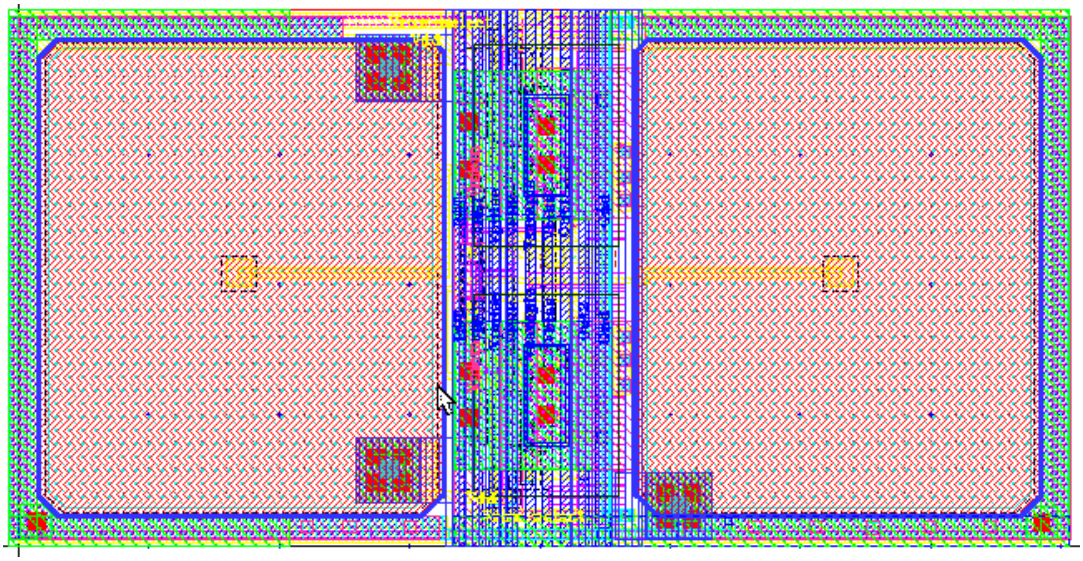


Figure 40: Layout of 1 x 2 pixels

Minimum metal widths and minimum spacing is used to make a dense layout of the pixel readout circuit. This dense layout of the readout helps in increasing the fill factor of the pixel. The blue part between two diodes shows the readout circuit shared between two pixels.

The Layout of the pixel optimized the following things

i) Fill factor of the pixel

Fill factor of the pixel is decided by the active area of the photodiode. Diode active area is 14.705 x 17.63 μm^2. Considering it as an octagon, the active area is 258.500μm^2. Therefore, the fill factor is FF= 258.5 / 400 = 64.625%. The novel design of the pixel helped achieve a high fill factor 0f 64.625%.

ii) Voltage drop on V_{DD} and GND lines

In a pixel array, V_{DD} and GND lines are routed throughout the array and are connected to each pixel, forming a mesh like structure with the input coming from either side of the mesh. The total size of the pixel array is 1.92mm x 1.92mm. Thus the V_{DD} and GND lines are routed for 1.92 mm distance. The current flowing through these power lines and the resistance of the metal layer used to route the power lines causes a voltage drop across the line. This leads to variation in V_{DD} across the pixel array and each pixel receives a different V_{DD}. This variation in V_{DD} needs to be minimized.

Use of metal 2 of minimum width (0.4μm) to route the power lines causes a voltage variation of 40mV across the pixel array for an average current of 100μA flowing on the power lines. The voltage variation needs to be minimized to less than 1mV so that every pixel receives the same V_{DD}. The voltage variation is minimized to 0.75mV with the use of metal 6 of width 2.74μm to route the power lines across the pixel array.

For pixel array length of 1.92mm and VDD wire width of 2.74μm, the total number of squares is 720. Metal 6 sheet resistance is 10.5mΩ /square, which gives a total resistance of 7.56Ω for routing the power lines across the pixel array. For an average current of 100μA, the voltage variation across the whole pixel array is 0.75mV. Thus, use of metal 6 to route the power lines improves the voltage variation across the pixel array to 0.75mV.

iii) Density check

The density requirements of the layers are poly > 12% and metal 1-metal 6 > 20%. The diode occupies 65 % of the pixel. It consists of active layer, silicide block, poly block and

metal 1-6 blocks. Therefore, it becomes difficult to meet the density check for poly and metal1-6 as the readout circuits is just 35% of the pixel area concentrated at the center. The density check fails at the corners of the pixel.

To meet the density check, poly is routed all around the pixel diode and connected to GND. The active area of the diode is reduced to make space for routing the poly around the diode which decreases the fill factor from 72% to 65%. metal 1- metal 5 are placed above the poly. This ensures the density check at the expense of reduced fill factor.

4.6 Layout of the chip

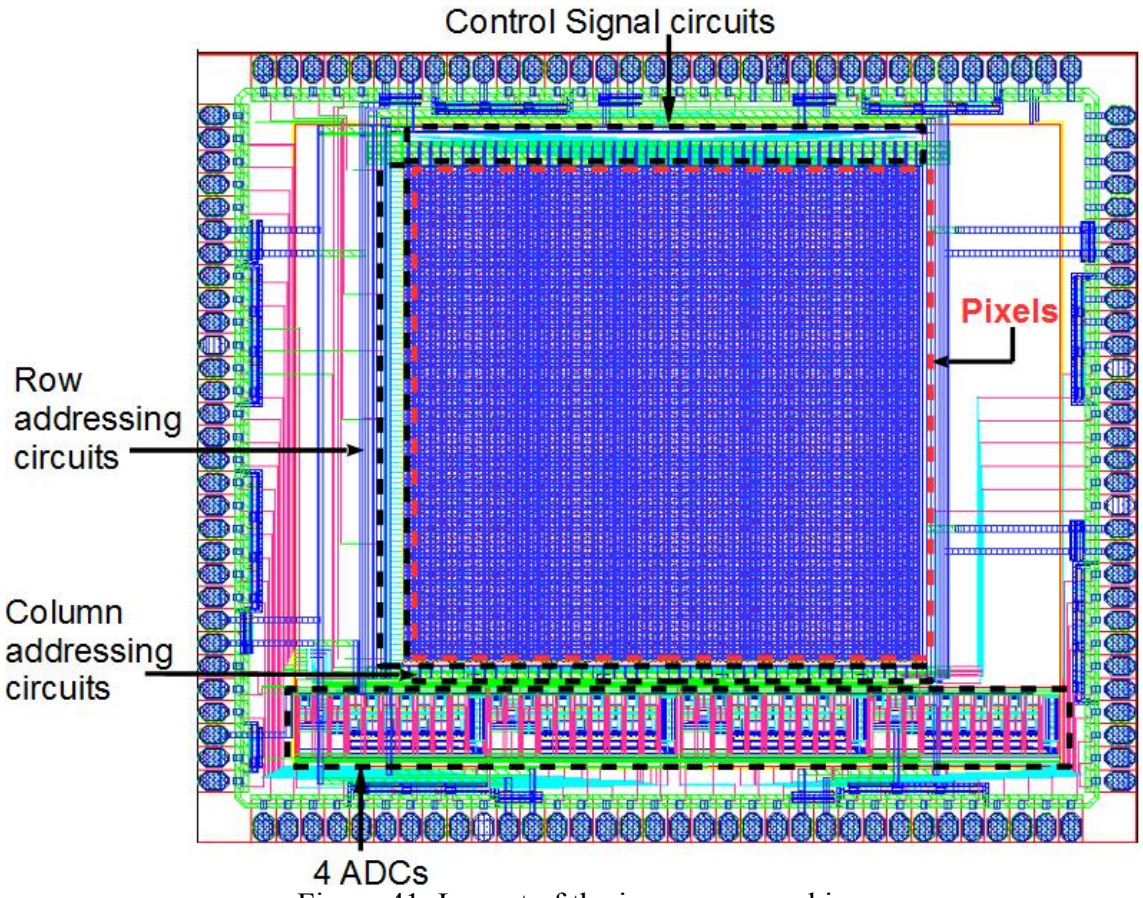


Figure 41: Layout of the image sensor chip

Figure 41 shows the final layout of the image sensor chip which is fabricated. It

highlights the sections in the image sensor: control signal circuits, row addressing circuits, column addressing circuits, pixels and four ADC's.

4.7 Micrograph of the chip

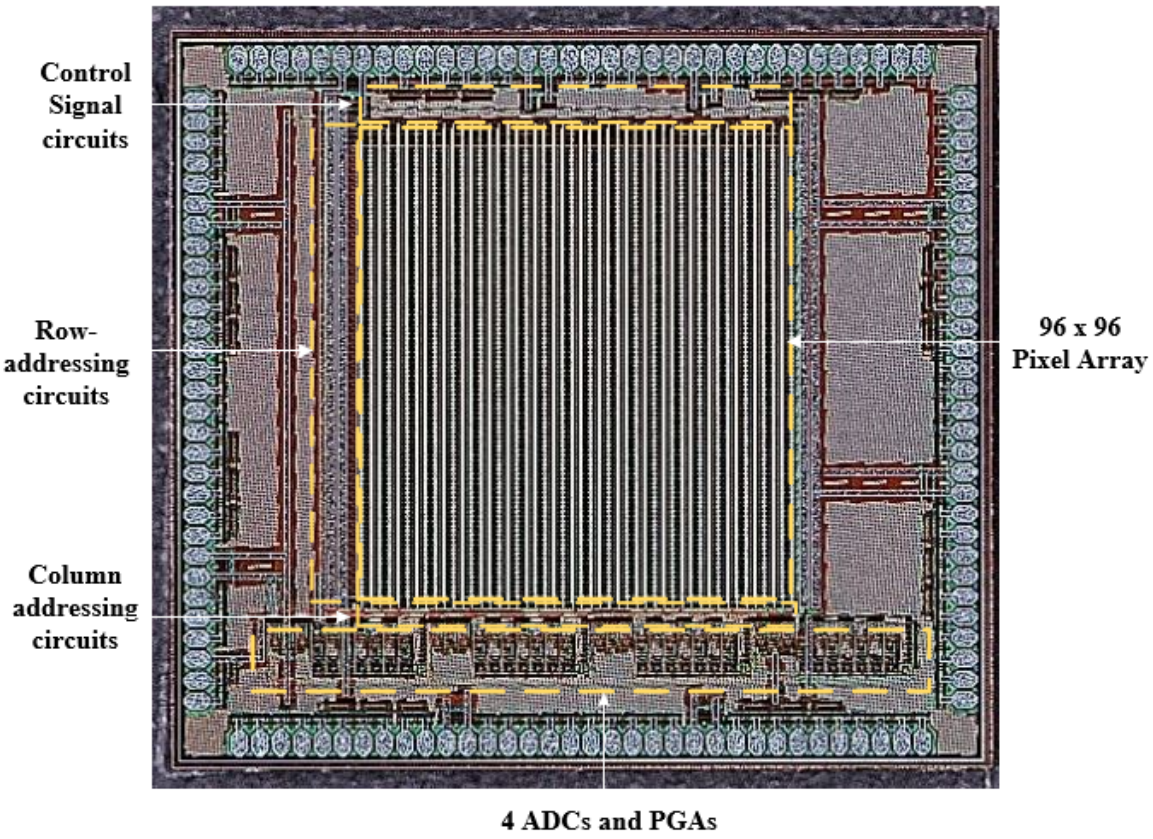


Figure 42: Die micrograph for image sensor chip

Figure 42 shows the die micrograph of this image sensor chip fabricated in 0.18μm standard CMOS process. The main components of the image sensor: 96 x 96-pixel array, four ADC's and PGA's, control signal circuits, row addressing circuits and column addressing circuits are highlighted.

4.8 Summary of the Results

Table 4: Summary of the performance of the designed image sensor

Technology	0.18μm
Die size	3.1mm x 3.4mm
# of Pixels	96^{H} x 96^{V}
Pixel size	20μm x 20μm
Fill factor	64.625 %
Maximum frame rate (continuous mode)	10508 fps
Readout rate	96 M pixels/sec
Full well capacity	$121ke^{-}$

Table 4 gives a summary of the performance of the image sensor chip designed and fabricated in 0.18μm CMOS process with an area upward of 3.1mm x 3.4mm.

CHAPTER 5

CONCLUSION

A high speed image sensor designed and fabricated in 0.18μm standard CMOS process has been presented in this thesis. The designed novel pixel read out circuit makes it suitable for high speed and low light imaging application. The image sensor designed operates in a continuous capture mode. The design minimizes the leakage currents in the pixel readout circuit, thereby, enabling the image sensor to detect low light signals and increasing the accuracy of the image. The innovative pixel layout of the readout architecture i.e. pixel sharing technique, maximizes the fill factor to ~65 %, making it suitable to detect low light signals, which produce an input swing of 350μV at the cathode of the photodiode. The image sensor achieves a frame rate of 10508 fps with a continuous capture mode and a readout speed of 96 M pixels/sec. The calculation, simulation and the post-layout simulation result for settling time of the pixel are a good match. The results prove the high frame rate, high readout, high fill factor, constant gain and minimized leakage of the designed pixel readout circuit.

Though the simulation and post-layout simulation results are a good match, the image sensor operation can be improved further by using a pinned photodiode in the pixel readout circuit. It is good at removing dark currents, providing higher conversion gain and high sensitivity. This will enable to detect very small signals having voltage swing around 10-100 μV. Moreover, CDS can be effectively implemented with a pinned photodiode which will reduce the reset noise levels. Micro lens can be used for the pixel array to improve the fill factor of the pixel. The use of micro lens and pinned photodiode requires an expensive

fabrication process. The image sensor leakage can be improved by using high V_T transistors and triple well transistors. This will, further, improve the overall design and enhance the speed and sensitivity of the image sensor.

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