Integrated CMOS-based Low Power Electrochemical Impedance Spectroscopy for Biomedical Applications

by

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ABSTRACT

This thesis dissertation presents design of portable low power Electrochemical Impedance Spectroscopy (EIS) system which can be used for biomedical applications such as tear diagnosis, blood diagnosis, or any other body-fluid diagnosis. Two design methodologies are explained in this dissertation (a) a discrete component-based portable low-power EIS system and (b) an integrated CMOS-based portable low-power EIS system. Both EIS systems were tested in a laboratory environment and the characterization results are compared. The advantages and disadvantages of the integrated EIS system relative to the discrete component-based EIS system are presented including experimental data. The specifications of both EIS systems are compared with commercially available non-portable EIS workstations. These designed EIS systems are handheld and very low-cost relative to the currently available commercial EIS workstations.

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CHAPTER ONE

MOTIVATION

In this work our aim is to develop a low-cost, handheld device that can be used to detect the presence of specific molecules from a fluid sample. While this work will present results for a very specific set of biomolecules for a particular application. The system has been design to be broadly applicable to detection of molecules. Generally detection can be performed through a wide variety of techniques such as fluorescence [1], SPR[2], mechanical resonance, FTIR[3], etc. Our goal was to implement a low-cost, handheld device capable of label-free molecular detection. Toward this goal we chose to implement our system using electrochemical analysis.

Electrochemistry is the branch of chemistry that studies the relationship between electrical and chemical phenomena [4]. It includes a variety of techniques that introduce variations in a chemical system and records the system response, see Table 1.1. These techniques can be used to study a huge range of systems including molecular binding, electroplating, semiconductors, electrodeposition, and batteries. Furthermore these techniques can provide very specific information and characteristics of electrochemical systems including binding efficiencies, corrosion rates, synthesis characteristics, dopant distributions in photovoltaic semiconductor cells, reaction mechanisms, etc.

In Table 1.1 electrochemical analysis techniques are categorized as either time domain or frequency domain. Time domain techniques are most useful in chemical systems that we wish to drive between states to understand this transition; they induce electrolyte oxidation/reduction, phase transition, as well as surface and volume changes.

TIME DOMAIN	FREQUENCY DOMAIN
Polarization (V- I)	Electrochemical Impedance Spectroscopy
Potential Step (ΔV- I(t))	
Cyclic Voltammetry (V_f(t)- I(V))	
Coulometric Titration (ΔV- ∫I dt)	
Galvanostatic Intermittent Titration (ΔQ- V(t))	

Table 1.1: Electrochemical Techniques in the Time and Frequency Domain

For instance, cyclic voltammetry pushes the system back and forth between oxidizing and reducing the species in the system. They can also suffer from a lack of specificity, since the current can drive multiple reactions. In this work, we explore the use of frequency domain techniques to detect specific biomolecules. Frequency domain is preferred since only a small perturbation is introduced into the system, so reactions do not take place. We can also examine the response of the system over a spectrum of frequencies, which greatly increases the specificity of the detection. Electrochemical detection in the frequency domain is called Electrochemical Impedance Spectroscopy (EIS).

There are many commercial EIS systems on the market which are far too expensive for point of care applications. These EIS systems are also bulky and heavy which are far from ideal for handheld devices. Table 1.2 shows some of the available commercial EIS systems on the market.

Instrument	Dimensions (inches)	Weight	Cost
EZstat Pro	10 x 9.625 x 4	10.75 lbs	$6500
Powerstat-05 CE	19 x 7.5 x 22	50 lbs	$15300
Powerstat-20	19 x 7.5 x 22	50 lbs	$33600

Table 1.2: Commercial EIS Systems [5]

These commercial EIS systems use their own sophisticated software tools which cost extra beyond the price listed in Table 1.2. However, these systems are multipurpose meet not only the specifications for this work, but they can also be used in analysis of fuel cells, electroplating, high current electro-synthesis etc. We can modify the specifications for our system, since the large currents and high frequencies necessary for other applications aren't as useful in biomolecular detection. These changes will allow us to engineer a system that can be used for molecular detection that is both low-cost and portable.

Our system will be characterized specifically as a handheld device that will allow optometrists and ophthalmologists to detect and quantify biomarkers associated with the diagnosis and treatment of external ocular disorders. The characterization of our system will focus on lactoferrin and IgE to assist clinic with diagnosis of dry eye and ocular allergies. Lactoferrin is used to assess lacrimal glad function to assess Dry Eye Syndrom, and IgE provides an assessment of the allergic component of ocular inflammation [6]. The work herein represents the first steps toward a highly specialized point-of-care (POC) system for detection of these biomarkers in tear fluid. The POC system should be very small so that it can be used to sample tear fluid during an eye exam. The general size

and shape of our device is shown in figure 1.1; its shape and weight distribution are based on specific techniques used to sample tear fluid. Commercial EIS systems are far too bulky for such handheld devices. Hence there is need for an inexpensive EIS system specially designed for handheld diagnostics applications. In addition to being handheld and low-cost the system must be accurate enough to diagnose patients.

Figure 1.1: Handheld Tear Diagnosis POC Device

The handheld device shown in figure 1.1 is used for tear fluid sampling diagnosis. Its size is approximately 2 x 5 inches, a very small form factor severely constraining the

electronic. The specifics of this project provide a set of aims that align with the more general goal of designing an EIS system for point of use applications: a low cost, compact size, light weight, low-power EIS system.

CHAPTER TWO

INTRODUCTION

2.1 Electrochemical Impedance Spectroscopy Basics

According to Ohm's law, an impedance of any component can be measured by applying electric potential (V) across it and measure the current (I) passing through it. The ratio of electric potential (V) to the current (I) passing through component gives the impedance of that component.

$$R = \frac{V}{I}$$

This law is valid only if the component is linear in nature for the range of electric potentials of interest. An ideal resistor shows such linear characteristics. The plot of current passing through an ideal resistor for different voltages is shown below[7]. It is a straight line passing through zero. Impedance of the resistor is inverse slope of line at any point.

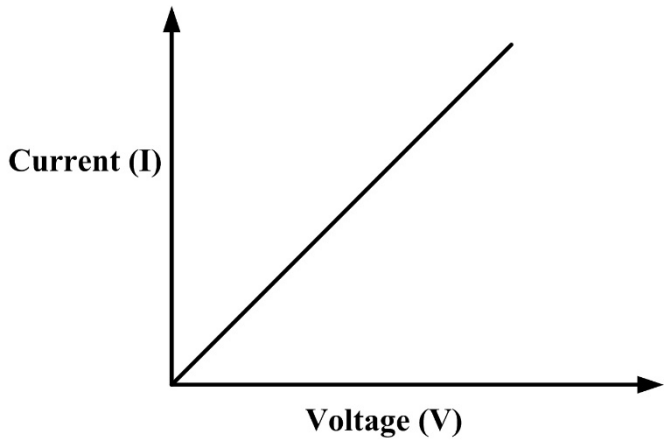

Figure 2.1: Current Vs. Voltage Plot for an Ideal Resistor

However in practical world, resistors exhibit non-linear nature at certain region in above graph such as at extremely high potentials where the current passing through the resistor

is so high that it will physically damage resistor by burning it. The above mentioned type of impedance is called resistance. An ideal resistor exhibit following properties:

1. It follows Ohm's law at all voltage and current values.
2. The resistance is independent of frequency.
3. If alternating current or voltage is applied across a resister, they are always in phase.

Unlike resistors, other circuit elements exhibit more complex behavior. The ability of circuit elements to resist or impede the flow of electric current passing through it is called the "impedance" of the circuit element. In the case of resistors, it's called "resistance" and is equivalent to impedance. Unlike ideal resistors, real world circuit elements are not limited by the properties mentioned above.

To measure the electrochemical impedance of an electrochemical cell, an AC potential is applied as an input and the current passing through the cell is measured. If an electrochemical cell exhibits purely resistive impedance then there is no phase shift between input voltage signal and current passing through the cell assuming the input AC potential is sinusoidal in nature [8]. Also the frequency of both current and voltage waveform will be same. If electrochemical cell exhibits purely capacitive impedance then current waveform will lead the voltage waveform by 90^{o}. If an electrochemical cell exhibits purely inductive impedance then the current will lag the voltage by 90^{o}. In the real world, an electrochemical cell with solution exhibits a combination of resistive, capacitive and inductive impedance.

2.2 Representation of Complex Impedance

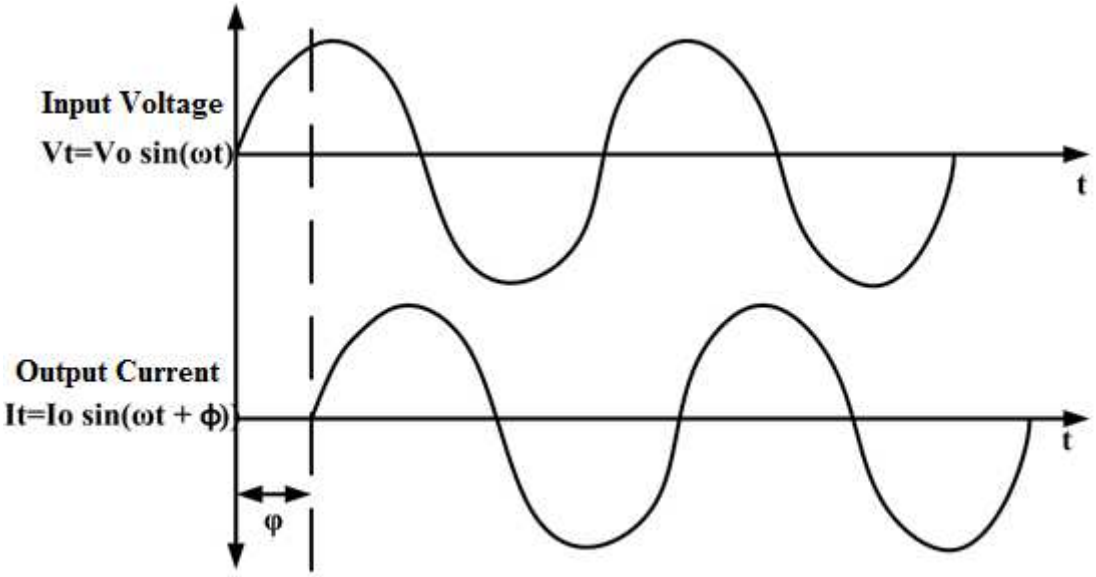

Figure 2.2: Input Excitation Voltage Signal and Current Response

Given an input excitation signal in time domain with the form:

$$V_t = V_0 \sin(\omega t)$$

Where,

V_t : Voltage at time t

ω : Radial frequency in rad/sec

t : Time

V_0 : Voltage amplitude of the signal

Radial frequency ω can be expressed in terms of frequency f in Hertz as $\omega = 2\pi f$.

The response signal I_t is shifted in phase by φ degrees and is given by,

$$I_t = I_0 \sin(\omega t + \phi)$$

Where, I_0 : Amplitude of response current

Φ : Phase shift in current response

A complex impedance is given by dividing instantaneous voltage signal with instantaneous response current.

$$Z = \frac{V_t}{I_t}$$

$$Z = \frac{V_0 \sin(\omega t)}{I_0 \sin(\omega t + \phi)}$$

$$Z = \frac{Z_0 \sin(\omega t)}{\sin(\omega t + \phi)}$$

Such complex impedance is represented in terms of phase shift φ and magnitude Z_0. The same impedance can be represented using Euler's relationship as follows:

$$Z(\omega) = Z_0(e^{j\phi})$$

$$Z(\omega) = Z_0(\cos\phi + j\sin\phi)$$

From above expression, impedance can be plotted over the spectrum ω rad/sec (or in frequency Hz) by only measuring two components: magnitude Z_0 and phase shift φ.

2.3 Electrochemistry Basics

Oxidation is a chemical reaction involving the loss of one or more electrons whereas reduction is a chemical reaction with an acquisition of electron(s). Oxidation and reduction reactions occur simultaneously in redox reactions [9]. Oxidation-reduction (Redox) reactions in a chemical solution causes electron movement from one element to another element. This electron transfer results in a current, and the study of these chemical processes is electrochemistry. In electrochemical cells, the same redox reaction causes electrons to move from one electrode to the other is highly non-linear. The focus of this dissertation will be measuring systems that exhibit this type of non-linear impedance over a frequency spectrum.

These measurements generally involve exchanging energy from chemical energy to electrical energy or vice versa, with electrodes placed in a chemical solution. Precise electrochemical measurements require three electrodes in a conductive electrolyte: working electrode, reference electrode and counter electrode. This structure is called a potentiostat which is further described in chapter 3.

2.4 Non-Linearity of Electrochemical systems

For biomedical applications, potentiostats are used to determine the I-V characteristics of electrochemical cells using an input voltage and output current. The current versus voltage plot of a typical electrochemical cell is shown in figure 2.3.

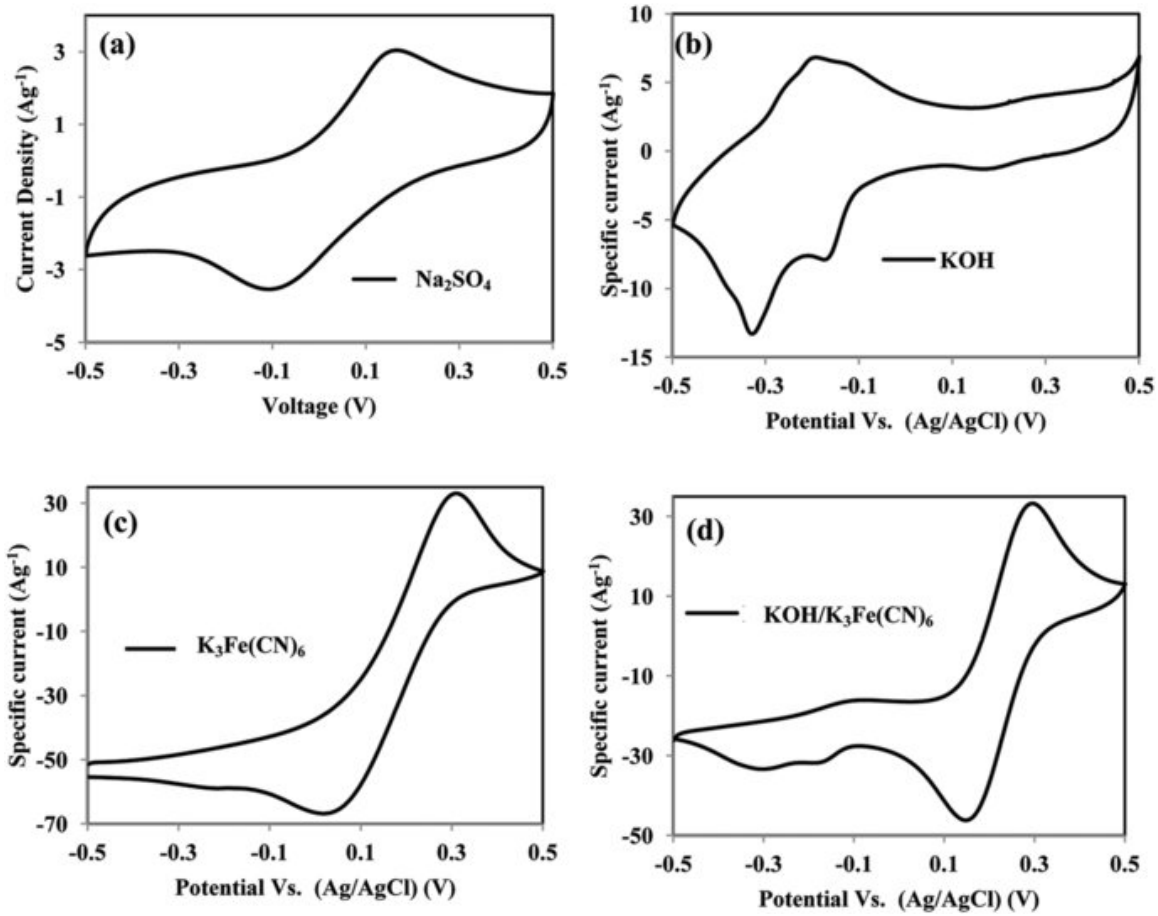

Figure 2.3: Non-linear Electrical Characteristics of an Electrochemical Cell [11]

From the graph, the highly non-linear nature of electrochemical cells is evident. Measuring the impedance of a non-linear system has numerous challenges. Hence to measure the impedance of a non-linear electrochemical cell, a small, linear portion of the non-linear response curve is used. As shown in the inset of figure 2.3, the magnified small portion of the curve looks approximately linear. We use an input excitation that is a very small amplitude AC voltage signal with DC shift to target the portion of the response with this approximately linear characteristic. The magnitude of the DC shift is dependent on which part of the curve is being targeted for measurement. We can determine a region of approximately linear behavior in electrochemical systems by measuring a parameter called the "formal potential". This potential is the midpoint between the oxidation and reduction peak, so it is both relatively easy to determine and consistently demonstrates nearly linear behavior. Normally, a small 1 mV to 10 mV peak to peak AC signal is applied on top of the DC shift or "formal potential" of the cell to linearize its response.

CHAPTER THREE

ELECTROCHEMICAL IMPEDANCE SPECTROSCOPY (EIS)

Electrochemical impedance spectroscopy (EIS) is a technique that measures impedance of an electrochemical systems over a frequency spectrum [10]. This impedance is plotted against frequency using either Nyquist plot or Bode plot. For biomedical applications potentiostat-based electrochemical cells are used for EIS. Bodily fluids such as tears or blood act as a solution in a cell. There are three electrodes in such cells: working electrode, reference electrode, and counter electrode.

3.1 Electrical specifications of EIS

In practice, the system under test needs to be in steady state during EIS measurements. Unfortunately there are many parameters like temperature, build-up of reaction products in solution, oxide growth, etc., that hinder maintaining a steady state. Also the non-linear nature of the electrochemical cell produces harmonic response signals which give inaccurate results. To improve measurements in our experiments for the tear diagnosis application, electrical characteristics the EIS system are defined below:

I. Sinusoidal signal with DC shift (formal potential) is used for excitation.

II. Peak to peak amplitude of sine wave is 10 mV with 150 mV DC shift.

III. Frequency range of the sinusoidal signal is from 1Hz to 3 KHz.

IV. Each measurement needs sufficient duration to achieve steady state.

3.2 Issues in designing EIS system

To design an electronic circuit for an EIS system with the described electrical specifications, there are several challenges for the designer. A very accurate sinusoidal

waveform generator needs to be designed with very high resolution for frequencies below 100 Hz. Ambient noise needs to be filtered from the 10 mV sinewave excitation signal. Ambient noise superimposes up to ±5 mV onto the signal, hence it becomes very difficult to separate signal from noise. A very accurate phase difference measurement instrument or circuit is needed as well. Since the strength of the signal is very low, a lock-in amplifier is needed to measure the phase difference.

3.3 Potentiostat

An electronic circuit or instrument that measures and controls the potential between a working electrode and a reference electrode while measuring the current flow between the working electrode and counter electrode is called a "potentiostat"[12]. The potentiostat can drive a redox reaction in an electrochemical cell by setting the potential or voltage across the cell. A potentiostat requires an electrochemical cell with all three electrodes to function properly.

The working electrode is the node in the circuit where the voltage bias is applied to offset for the formal potential, and it is the node where the current is measured. The counter electrode is the node at which we apply the sinusoidal excitation, and it is the electrode that provides the current that flows into the solution completing the circuit. The reference electrode is used to set a constant potential for the solution, since no current flows through the electrode it can maintain a very consistent potential. The potentiostat requires low impedance for reference electrode, since in practice the reference electrode has parasitic capacitance and resistance. Hence it forms an R-C low-pass filter. A high resistance would reduce the corner frequency of the filter and bypass low frequency

excitation signals given through the working electrode. Therefore a low resistance reference electrode is needed to increase the cut-off frequency of the parasitic low-pass filter. It should also be noted that none of the electrodes should take part in the chemical reaction. For this reason the selection of the electrode materials for a given system and potentials is important.

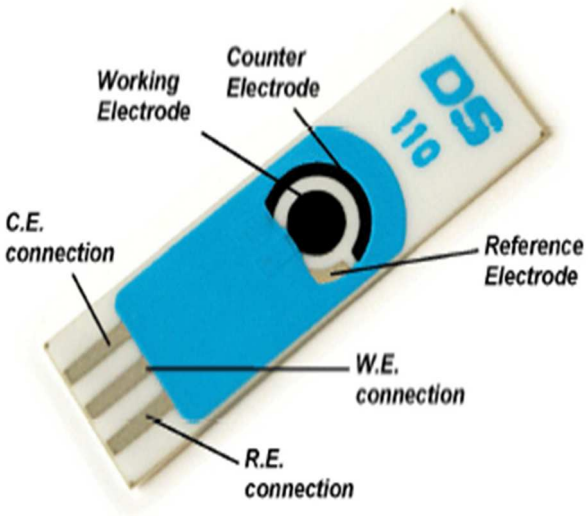

Figure 3.1: Screen-printed Electrode[13]

For handheld devices, such three electrodes must be compact and inexpensive. Screen-printed carbon electrodes are most commonly used as an interface between biomarkers and electronic circuits. One such screen-printed electrode is shown in figure 3.1.

3.4 Analyzing EIS using electrical circuit elements

An electrochemical cell impedance can be modelled using purely electrical circuit elements such as resistors, capacitors, and inductors. The combination of these circuit elements gives an approximate model for EIS. A solution or electrolyte resistance between a working electrode and counter electrode can be modelled as a simple resistor

R_s. However this electrolyte resistance depends on many varying parameters such as concentration of solution, temperature of solution, types of ions etc. An electrical double layer exists between an electrode and its surrounding electrolyte which can be modelled using a simple capacitor C_{dl}. There are other reactions as well which opposes flow of current and can be modelled as simple resistor such as charge transfer resistance[14].

3.5 Randles Circuit Model

There are many different models that can be used to describe an electrochemical cell impedance using basic electrical elements. Using different combinations (serial or parallel or both) of resistors and capacitors or even inductors many more models can be created. For our application, the Randles model provides the best tradeoff between a simplified architecture and a fairly accurate representation of the impedance of a cell. We will assume this model for electrochemical cells throughout the discussion that follows. A simplified Randles cell includes a solution resistance, double layer capacitance and a charge transfer or polarization resistance[15]. The double layer capacitance is in parallel with the charge transfer resistance, and this combination is in series with the solution resistance; the three components comprise a Randles cell.

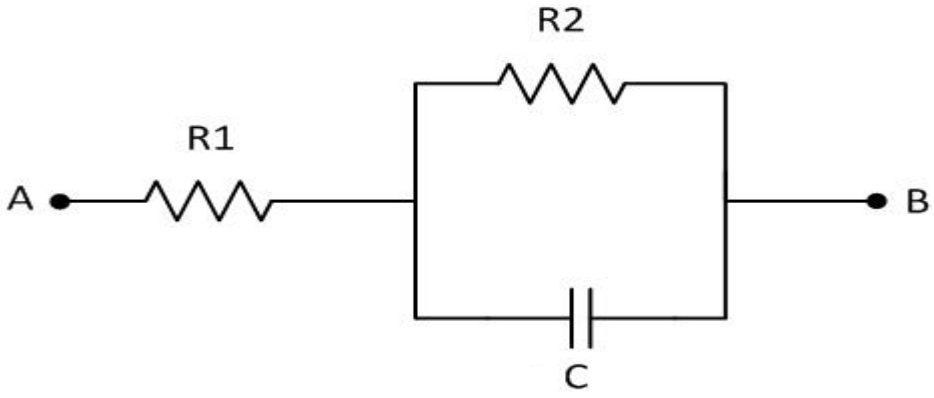

Figure 3.2: Randles Cell Model

In the Randles cell model as shown in figure 3.2, resistors R1 and R2 are solution resistance and charge transfer resistance respectively. Capacitor C is the double layer capacitance.

CHAPTER FOUR

DISCRETE ELECTRICAL COMPONENTS BASED EIS

There are two design approaches to design handheld EIS system – discrete electrical components based EIS and integrated EIS system.

4.1 Block diagram of Discrete EIS

Electrochemical impedance spectroscopy (EIS) system is designed using electrical discrete components and its block diagram is as shown below:

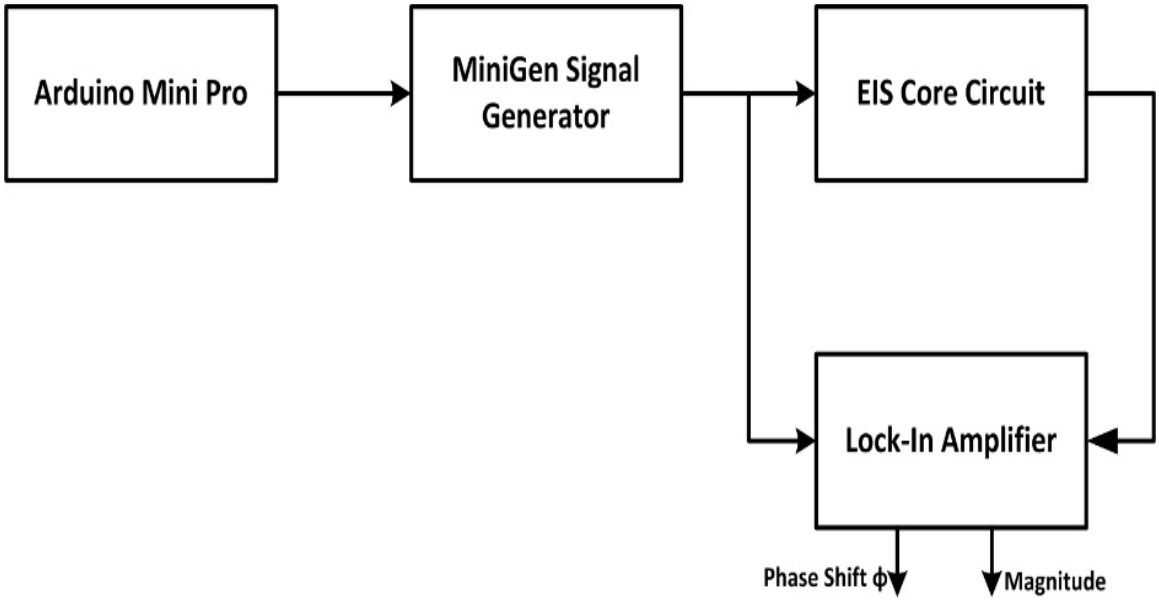

Figure 4.1: Block Diagram of EIS Using Discrete Components

Arduino Mini Pro board and MiniGen Signal Generator board has same form factor in size and they overlap on each other due to compatible pin configuration[16]. This further reduces the size of electronics. Arduino Mini Pro board is programmed to communicate with MiniGen Signal Generator board[17] and generate a sine wave. EIS core circuit converts down this sine wave signal to appropriate amplitude and formal potential and gives as an input excitation signal to the cell. Output current is converted

into voltage signal in the same EIS core circuit. Input excitation signal and output voltage signal are compared using lock in amplifier to find magnitude and phase change due to cell. Using magnitude and phase information Nyquist plot or bode plot can be plotted as an output data format.

4.2 Design specifications

As described earlier the minimum electrical specifications of an EIS needs to be met by the circuit. Minimum specifications of the system are:

I. 10 mV peak to peak sinusoidal voltage signal

II. Frequency range of sinusoidal signal is from 1Hz to 3 KHz.

Using above circuit, 1 V peak to peak sinusoidal voltage signal with 2.5 V DC shift and frequency range of 1 Hz to 3 MHz is achievable. These specifications are well beyond the minimum requirements needed for EIS.

4.3 Arduino Mini Pro

Arduino being an open source hardware, is a really handy tool for any electrical engineer in their research. Out of several arduino based controller boards, preference is given to small dimension board size and high speed microcontrollers. Arduino Mini Pro board with 5V power supply seems a perfect choice for handheld EIS applications. Some of the salient features of this board are small dimensions, 16MHz operating frequency, USB connectivity, analog and digital I/O pins and weighs less than 2 grams. The detailed configuration is given in appendix-A. The dimensions of this board are just 18x33 mm which is a good feature for the desired form factor of portable EIS device. Following image compares the size of this Arduino mini Pro with a standard US quarter coin.

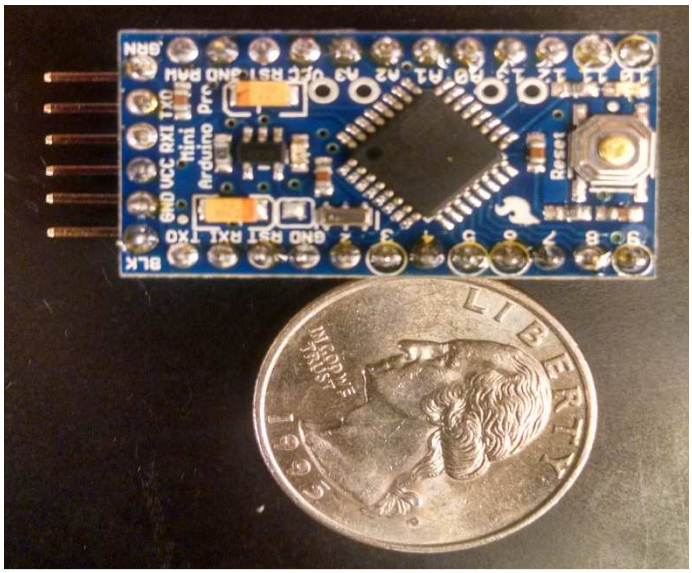

Figure 4.2: Arduino Mini Pro Board Dimension Comparison

Left hand side six pins are used for programming Arduino mini Pro board. To program this Arduino board, FTDI basic breakout board is used due to lack of on-chip programmer on Arduino mini Pro.

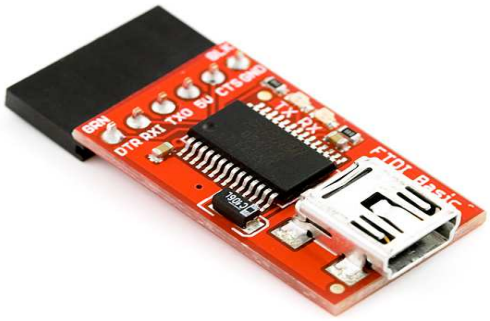

Figure 4.3: FTDI Basic Breakout Board [18]

This breakout board has mini-USB port that can be connected to laptop through USB to mini-USB cable. It communicates with Arduino Mini Pro through serial communication protocol. Hence receiver (Rx) pin of breakout board should be connected to transmitter (Tx) pin of Arduino board and vice versa.

4.4 MiniGen Signal Generator

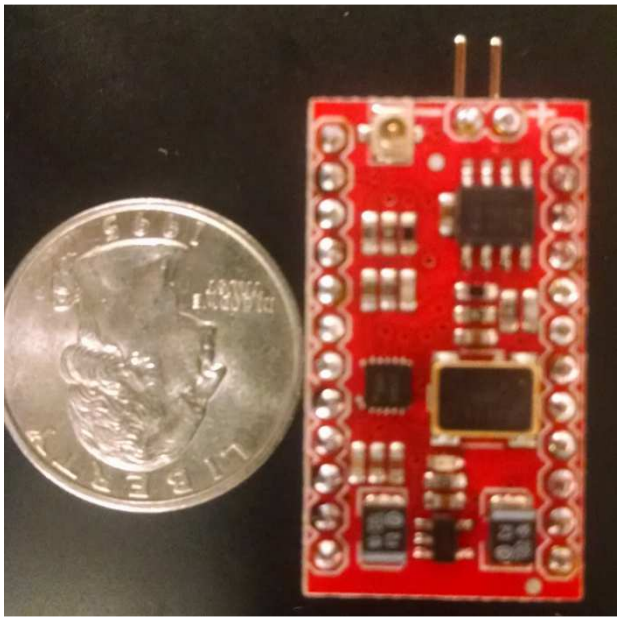

Figure 4.3: MiniGen Signal Generator Dimension Comparison

To generate sinewave signal with variable frequency which can be controlled using Arduino Mini Pro, MiniGen Signal Generator shield is used from Sparkfun. This shield is basically of same dimensions as of Arduino Mini Pro and can be mounted on top of it. This reduces form factor in size by two. This significant change in dimensions is possible due to compatible pin configuration with Arduino Mini Pro board.

4.5 EIS Core Circuit

EIS core circuit as shown in figure 4.4 drives biomarker (electrochemical cell sensor) and collects output signal in the form of voltage signal. Input to this circuit is an output from MiniGen Signal Generator i.e. sinewave signal of 1V peak to peak with 2.5 V DC shift. For tear diagnosis application an excitation signal required is 10 mV peak to peak sine wave with 0.15 V formal potential. Resistors R1, R2 and potentiometer scales down generated sine wave from MiniGen to required values. Excitation signal is given at

working electrode (WE). Reference electrode (RE) is at formal potential. Current coming from counter electrode (CE) is converted into voltage by second opamp and feedback resistor Rf. For testing of Randles model, reference electrode terminal and working electrode terminal are shorted together. Randles model has only two terminals. One terminal is connected to RE-CE connection and other terminal is connected to inverting input of second opamp.

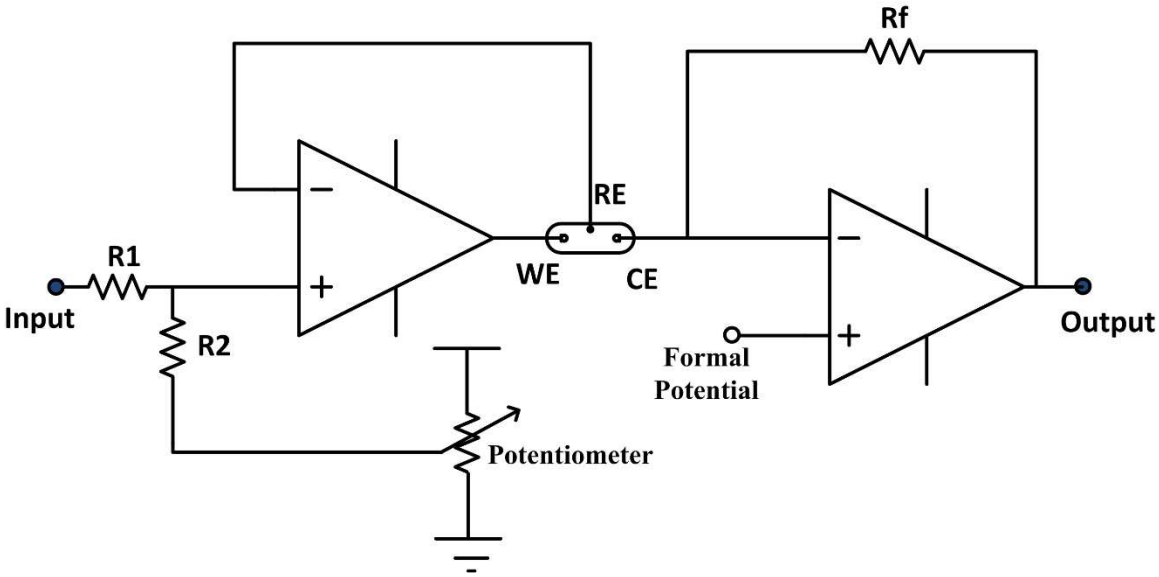

Figure 4.4: EIS Core Circuit Using NTE987 Quad Opamp IC

Operational amplifiers in the core circuit are implemented using NTE 987 quad opamp IC whose pin configuration is shown in figure 4.5. This is single power supply IC (used with 5V power supply) with four individual opamps in it. The common mode input range include negative supply hence eliminates necessity of external biasing components. Output voltage range also includes negative power supply. These all four opamps are internally compensated. Common mode rejection ratio is 70 dB and power supply rejection ratio 100 dB.

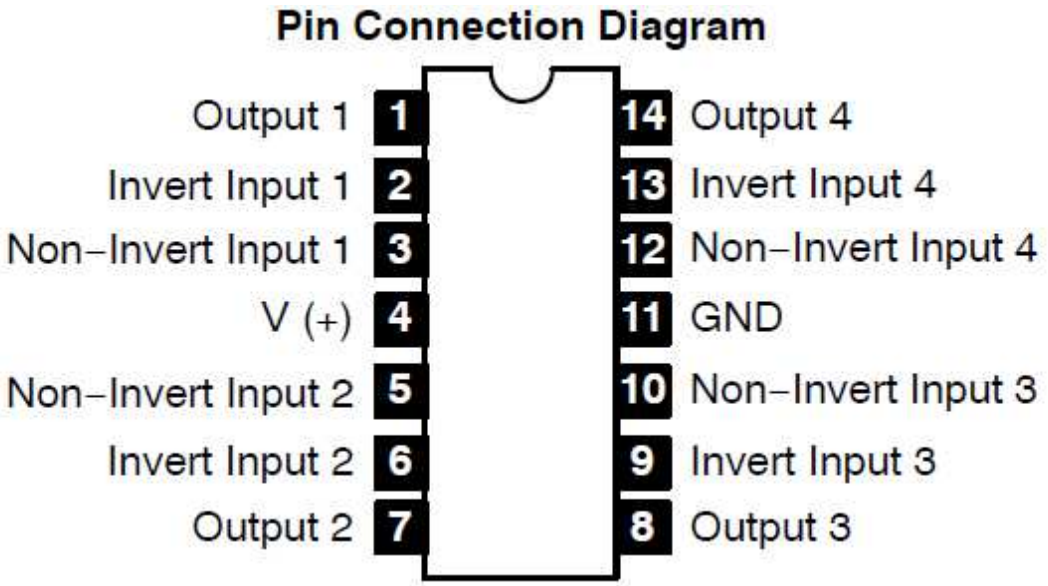

Figure 4.5: NTE 987 Quad Opamp IC Pin Configuration [19]

This IC consumes maximum of 1.2 mA of power supply current at 5V power supply voltage. Hence maximum total power consumed by this unit is merely 6 mW. Input offset voltage at room temperature is 2 mV. This low power and low input offset voltage makes this IC a suitable choice.

4.6 Lock-in Amplifier

Figure 4.6: Stanford Research SR850 Digital Lock-in Amplifier[20]

There are many noise sources when using discrete components based EIS system. Hence it will affect very small AC signal of 10mV peak to peak and there is a huge error while measuring phase shift and magnitude change using an oscilloscope. To minimize noise effects from ambience, SR850 digital lock-in amplifier is used.

CHAPTER FIVE

INTEGRATED EIS

5.1 Block Diagram of Integrated EIS CMOS IC:

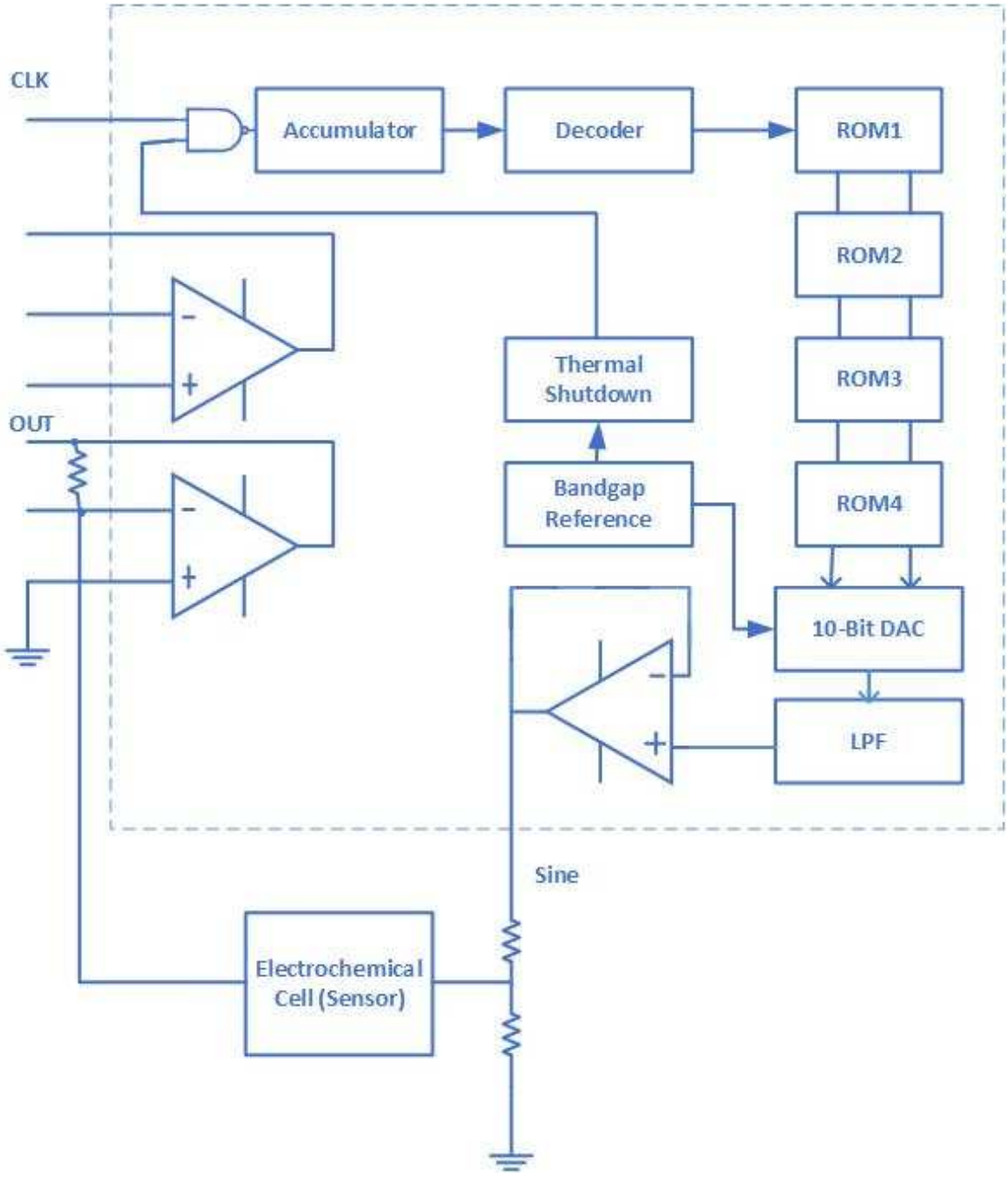

Figure 5.1: Block Diagram of Integrated EIS CMOS IC

Sinewave generator (Arduino Mini Pro and MiniGen Signal Generator Shield) and EIS core circuit (NTE 987 IC) from discrete components based EIS system is integrated using MOSIS service ON semiconductor 0.5µ CMOS fabrication process. Figure 5.1 shows block diagram of Integrated EIS system. This custom IC contents each blocks in dotted square. This IC has three independent operational amplifiers and each of these pins can be accessed. Control input for this IC is CLK signal. This CLK signal is given to 8-bit accumulator. This accumulator is a counter which resets after 256 cycles. Decoder decodes 8 bits from accumulator and selects a 10-bit word from one of the four ROM memory modules. ROM memory module contains information points of sine wave. 10-bit words are chosen to get better resolution of sine wave. This 10-bit word is given to 10-bit digital to analog converter (DAC). This 10-bit DAC converts digital data into analog sinusoidal waveform. This signal is then passed through low pass filter (LPF) for better smoothing of curve. At the output of filter, a sinusoidal waveform of frequency f_{sine} with (Vcc-Vss)/2 DC shift is generated. Frequency of sine wave is dependent on input CLK frequency f_{clk}. The relationship between these two frequencies is given by following expression.

$$f_{sine} = \frac{f_{clk}}{256}$$

Bandgap reference circuit is designed for 1.225 V at 27^0C (300K). Bandgap voltage varies ±3mV from -40^0C to 160^0C. A thermal shutdown voltage is designed using the same bandgap circuit and it's tripping temperature is 160^0C. Since this is a low power application circuit, such high temperature is not expected to meet.

5.2 Schematics

Main component in designing EIS CMOS IC is an operational amplifier. Two configurations of an opamp circuit are designed in 0.5µ CMOS process using cadence tool. The schematic of folded cascode opamp is shown in figure 5.2[21]. Symmetry technique is used while designing this opamp. Constant-gm bias circuit is used to bias transistors in this circuit. PMOS as an input is chosen to get very low input referred noise. Due to its symmetry, this circuit has high stability.

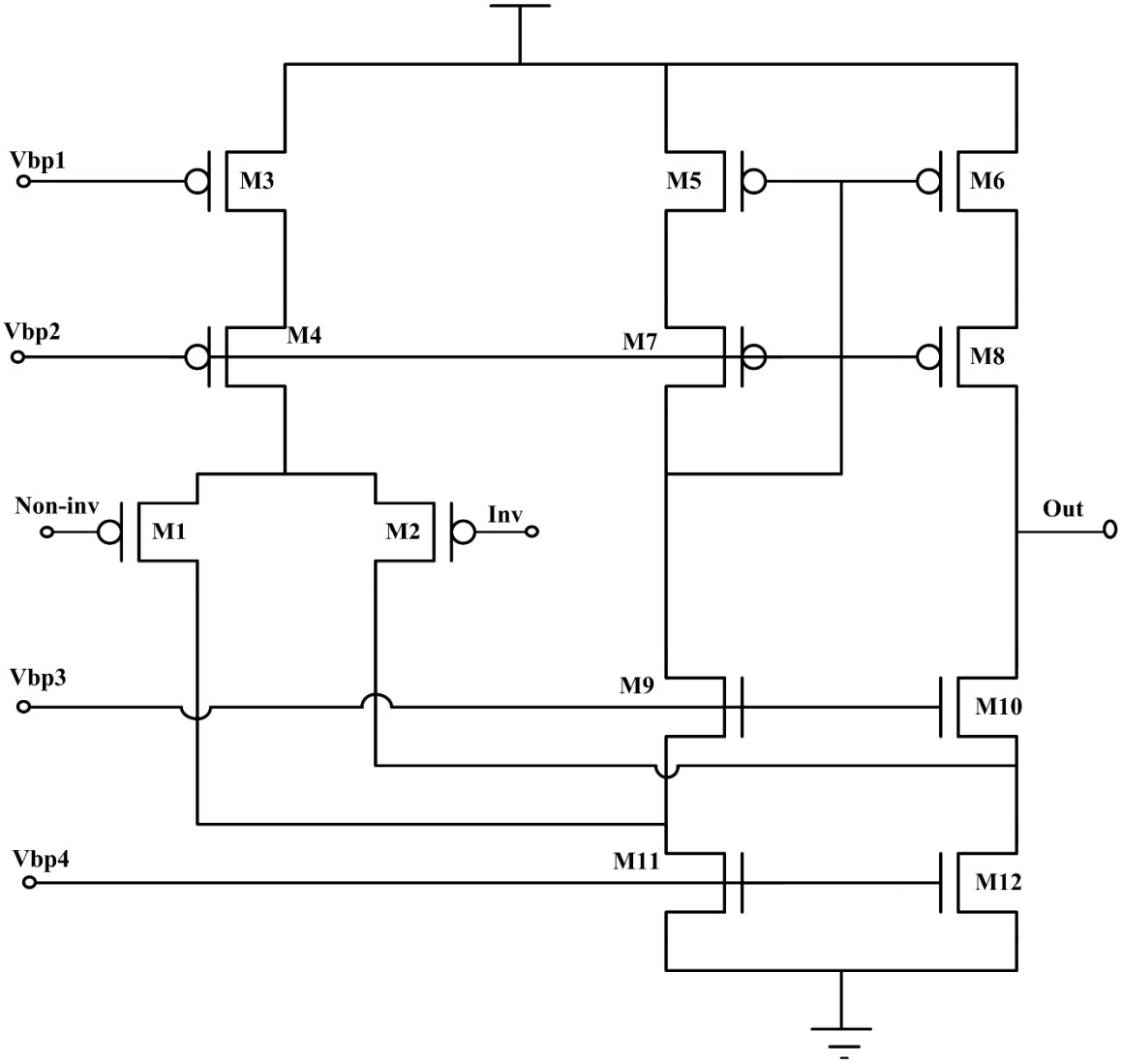

Figure 5.2: Cascode Operational Amplifier

The other type of operational amplifier is of two stage opamp configuration as shown in figure 5.3. This opamp is lead-lag compensated by using passive components resistor R and capacitor C. This opamp can serve better for driving high capacitive loads. Hence this opamp is used as a buffer after sine wave is generated.

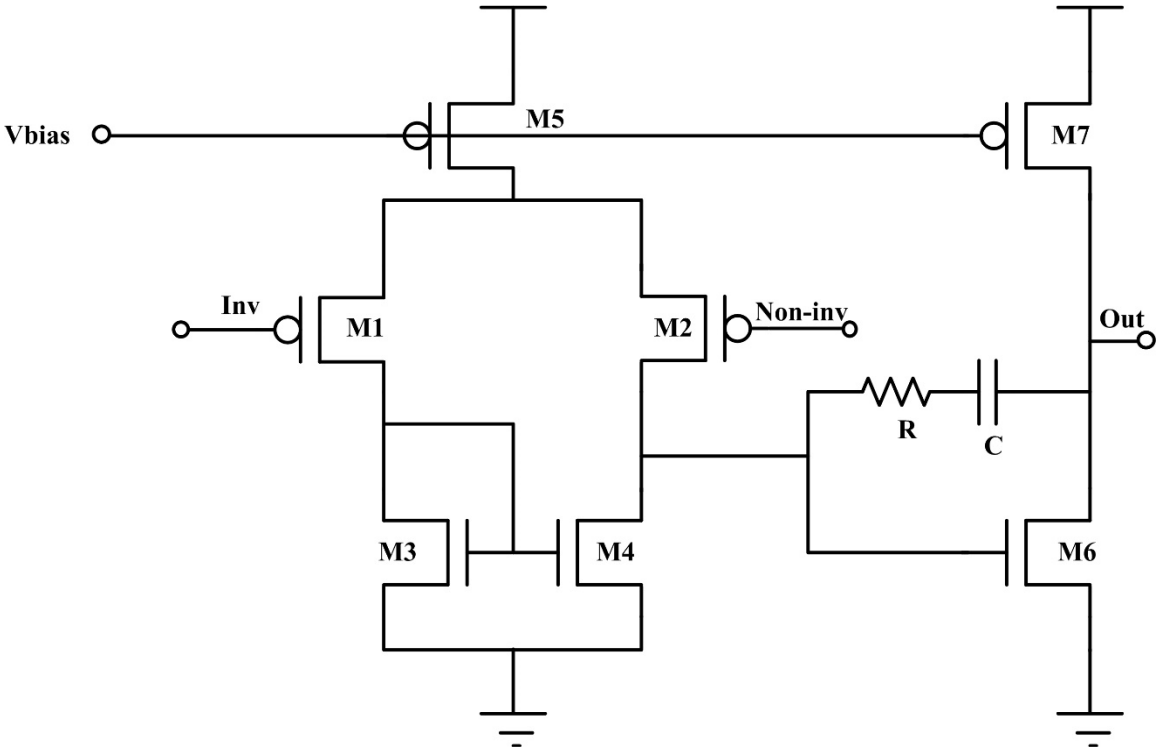

Figure 5.3: Two Stage Operational Amplifier

To generate frequency controlled sine wave, a digital method is chosen over traditional oscillator method. For generating low frequency sine wave in traditional oscillator method, device size is very huge and it is hard to integrate on a chip. Another advantage of digital method is that it can be programmable and scale down using advanced processes. Hence more reduction in size and power can be achieved using digital sine wave generator. The only input required for generating a sine wave is the

clock signal. This clock signal is first processed by an accumulator block. Accumulator block diagram is shown in figure 5.4.

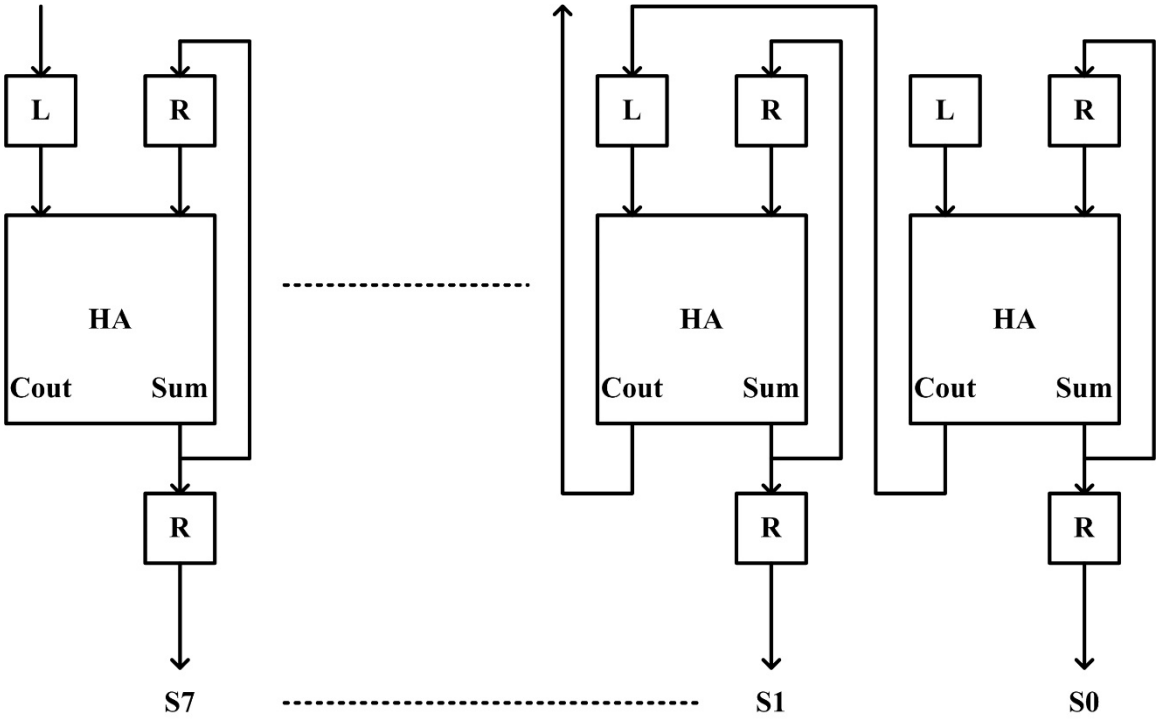

Figure 5.4: Block Diagram of an Accumulator

This accumulator block contains half adder (HA), latch (L) and register (R). It is an 8-bit accumulator. S7 is an most significant bit (MSB) whereas S0 is an least significant bit (LSB). Latch input of LSB is a positive terminal of power supply i.e. digital logic 1. After each clock cycle, this accumulator increments it's 8-bit value by one. Once it reaches its highest value of decimal 255 (0x FF), it resets to 0 in the next clock cycle. And again counting starts from 0 to 255. Same registers and latches are used in entire circuit. Transistor level circuit diagrams of register and latch are given in figure 5.5 and figure 5.6 respectively. Due to high number of registers and latches in circuit, few number of transistors based circuits are preferred to design both.

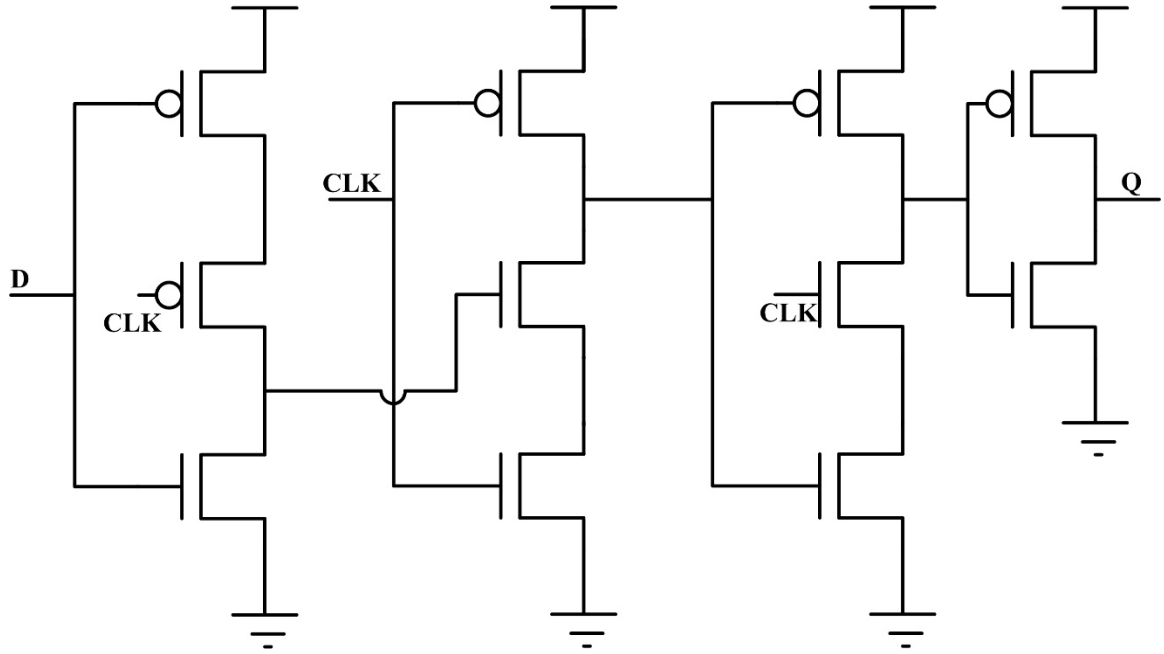

Figure 5.5: Register Circuit Diagram

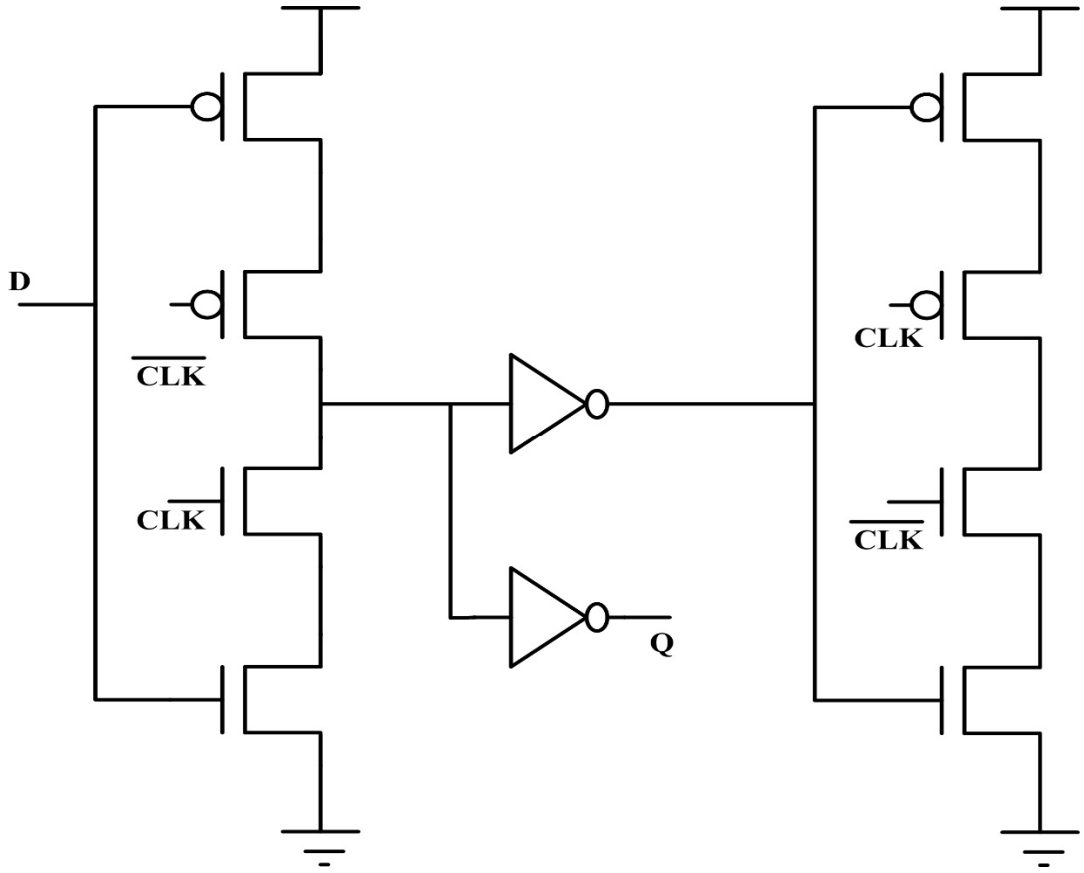

Figure 5.6: Latch Circuit Diagram

As seen in figure 5.5 and figure 5.6, registers and latches require non-overlapping clock signals. Hence to generate complementary non-overlapping clock signals, following circuit as shown in figure 5.7 is implemented.

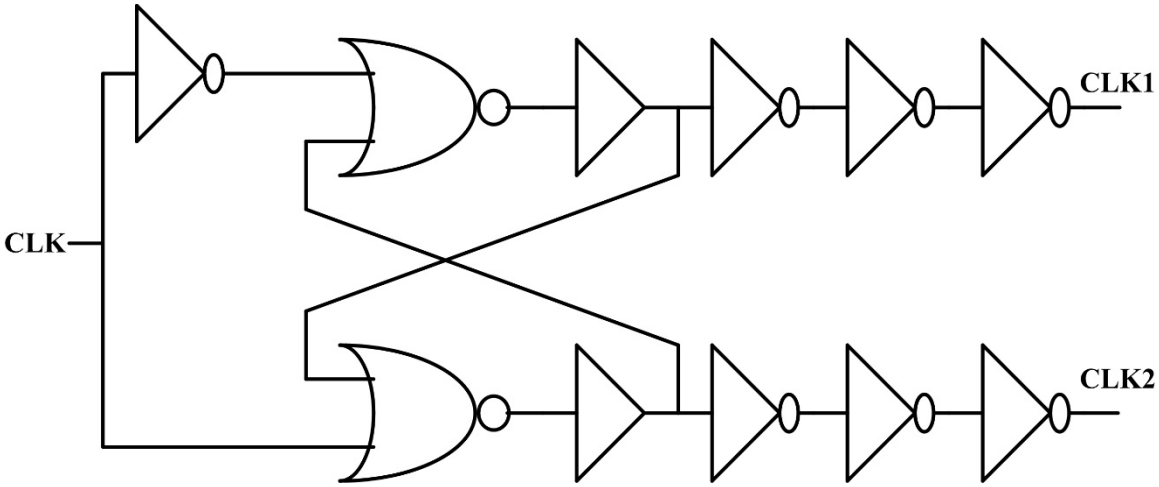

Figure 5.7: Non-overlapping Clock Generator Circuit

Input clock signal (CLK) is converted into two non-overlapping clock signals CLK1 and CLK2. Two buffers after NOR gates are sized accordingly so that CLK1 and CLK2 signals do not overlap on each other. Three inverters following buffer are of increasing size to drive high capacitive loads.

Accumulator gives 8-bit information to decoder block which uses two MSB bits to select one ROM module out of four. There are two decoders in circuit- 2:4 decoder and 6:64 decoder. Diagrams of these decoders are given in figure 5.8 and 5.9 respectively. 2:4 decoder selects one of the four ROM modules. Six LSB bits of accumulator are decoded using 6:64 bit decoder to select one 10-bit word out of 64 words from selected ROM module. Three inverters of increasing size after NAND gate are implemented to drive high capacitive loads. This decoder operates only in positive clock cycle duration.

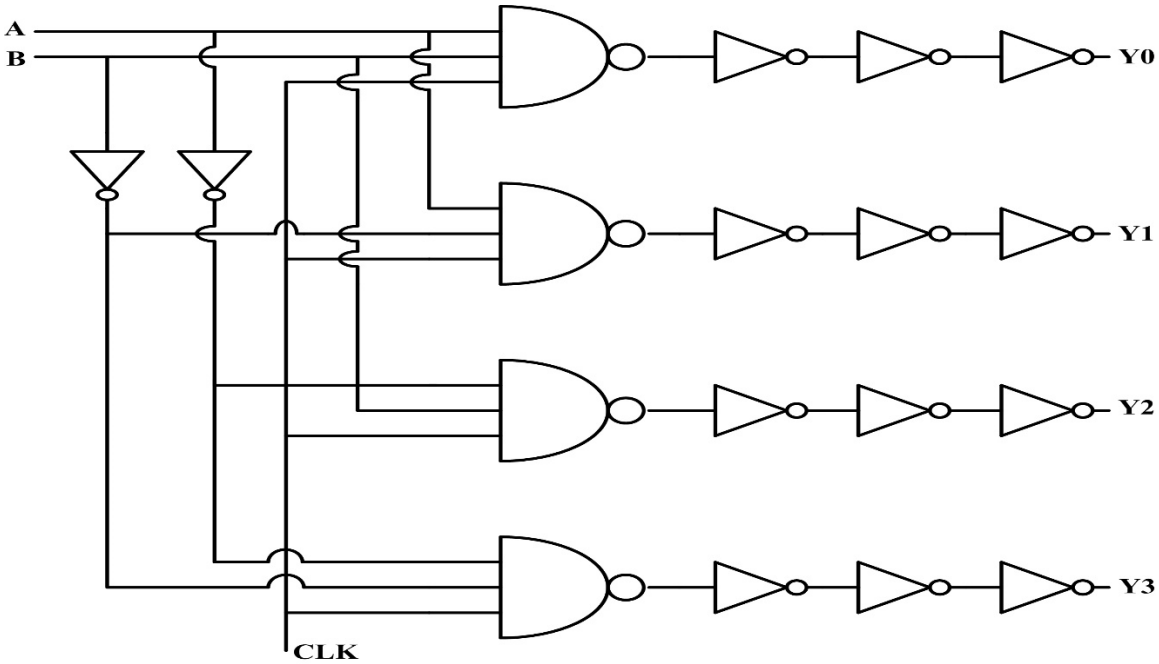

Figure 5.8: 2 to 4 Bit Decoder Circuit Diagram

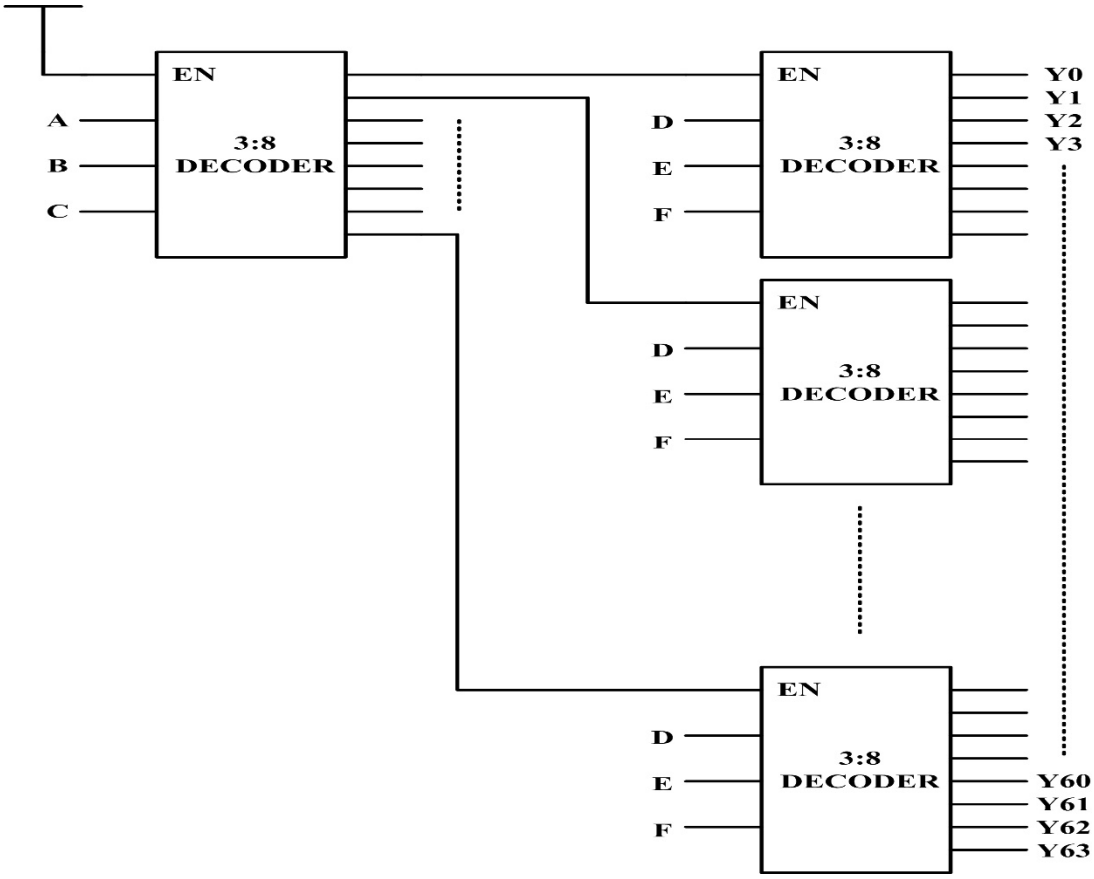

Figure 5.9: 6 to 64 Bit Decoder Circuit Diagram

Sine wave information points are stored in four ROM memory modules. Each sine wave is divided into four parts and each part is stored in its corresponding memory module as shown in figure 5.10.

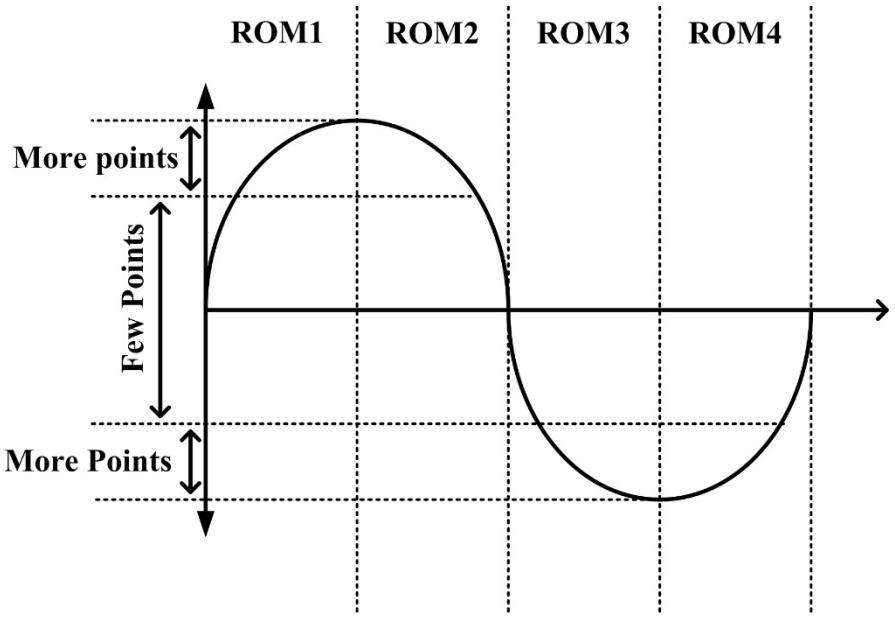

Figure 5.10: Sine Wave Stored Points

Each ROM module contains 10-bit wide 64 words. Hence resolution of amplitude of sine wave (step size) is Vcc/1024. As frequency of operation increases then sine wave will change to triangular wave if points are stored linearly. To avoid this situation, more number of points are stored at its peak where sine wave is more non-linear and very few number of points are stored from middle portion of sine wave. This technique is required due to limited size of ROM memory.

Transistor level ROM memory module is shown in figure 5.11. Decoder outputs are given to read line (0:63) and it selects a word from this memory. A pull up/ pre-charge circuit pulls up bit values where there is a connection between horizontal and vertical line by a transistor. Dummy transistors are put for symmetric layout purpose

where there is no connection. Horizontal lines are the word output data (10 bits). This word data is given to digital to analog converter (DAC) as an input. Each vertical read line is connected to one pull up/pre-charge circuit to keep node voltage at logic 1.

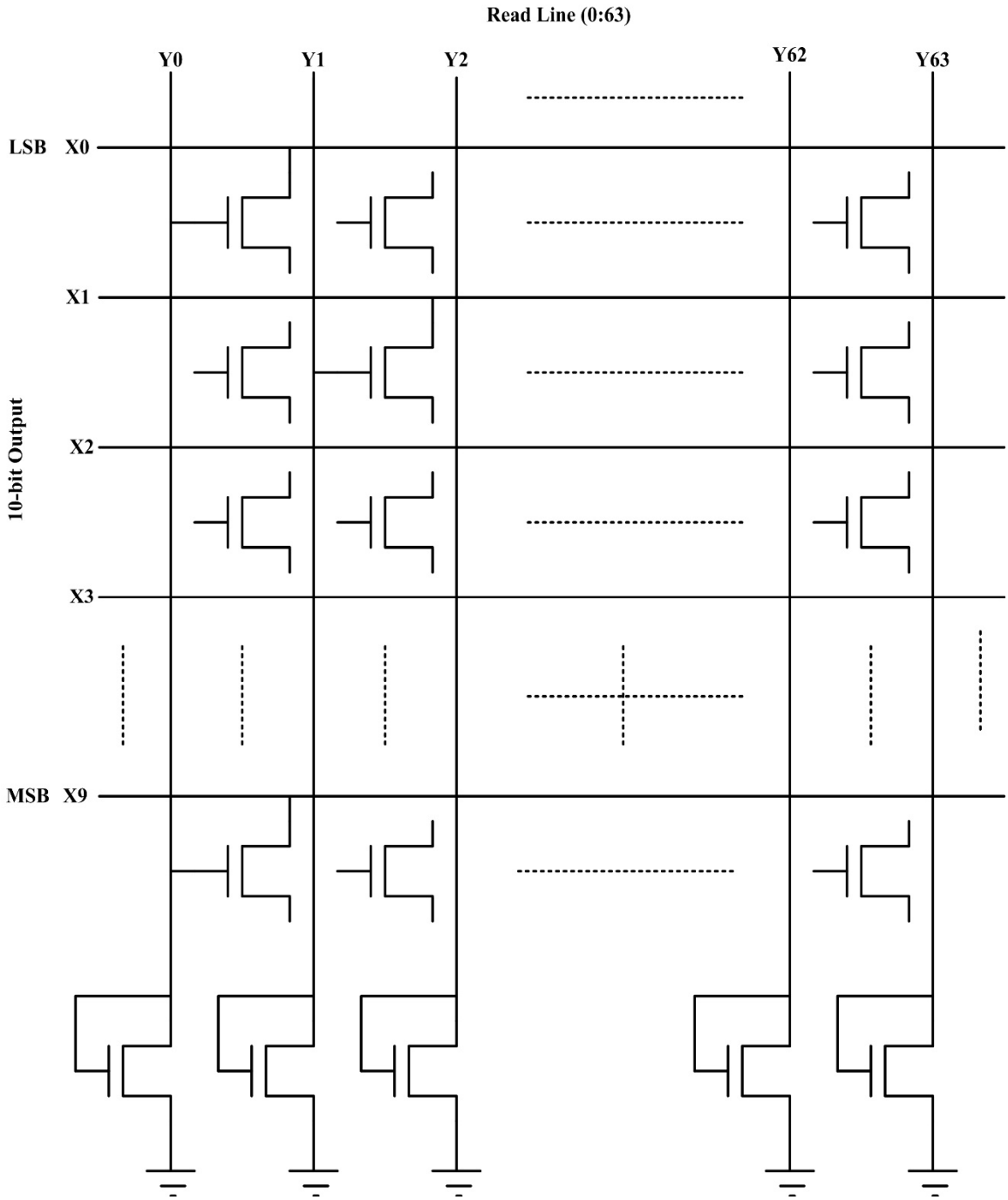

Figure 5.11: Rom Memory Module Circuit Diagram

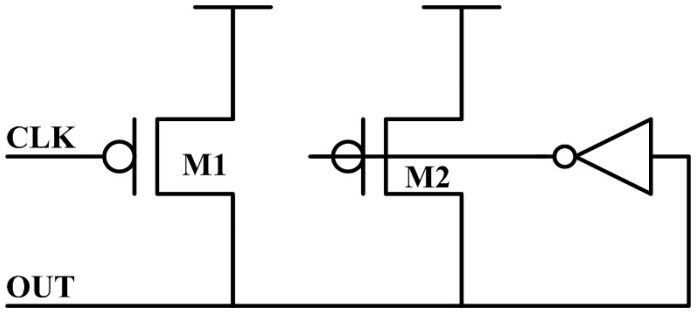

Figure 5.12: Pull-Up/ Pre-Charge Circuit Diagram

Output data word from each ROM memory modules is multiplexed and given to 10-bit DAC. Only one ROM module will output data on DAC input at a given time. 12-bit DAC is implemented for future use and it's two MSB bits are tied up to Vcc. Only 10-bits are used by this circuit. The block diagram of this DAC is shown in figure 5.13.

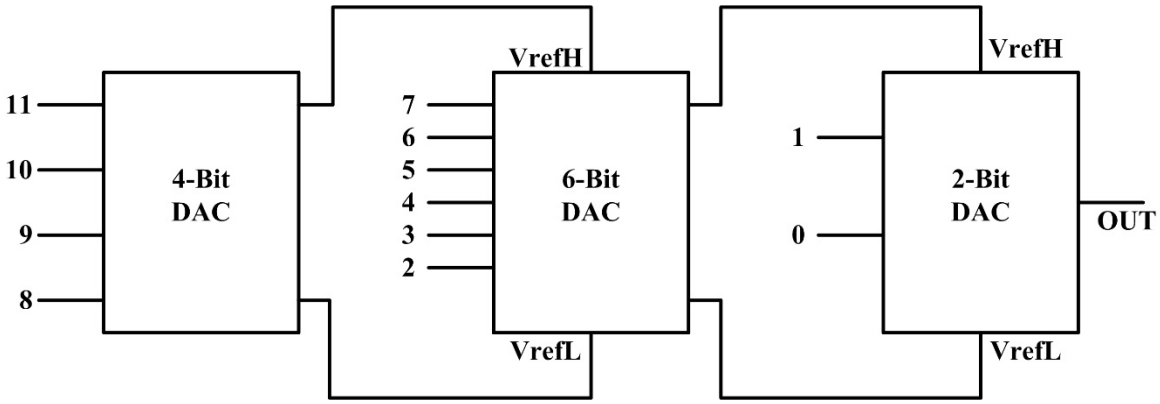

Figure 5.13: Digital to Analog Converter Circuit Diagram

Simple R-2R ladder circuit diagram is used for each digital to analog converter (DAC) block and it's architecture is shown in figure 5.13. 4-bit DAC output is given as reference voltage to 6-bit DAC (High reference- VrefH, Low reference- VrefL). 6-bit DAC output is given as reference voltage to 2-bit DAC. This architecture is useful for sine wave generator due to non-linear stored points.

5.3 Layout Techniques

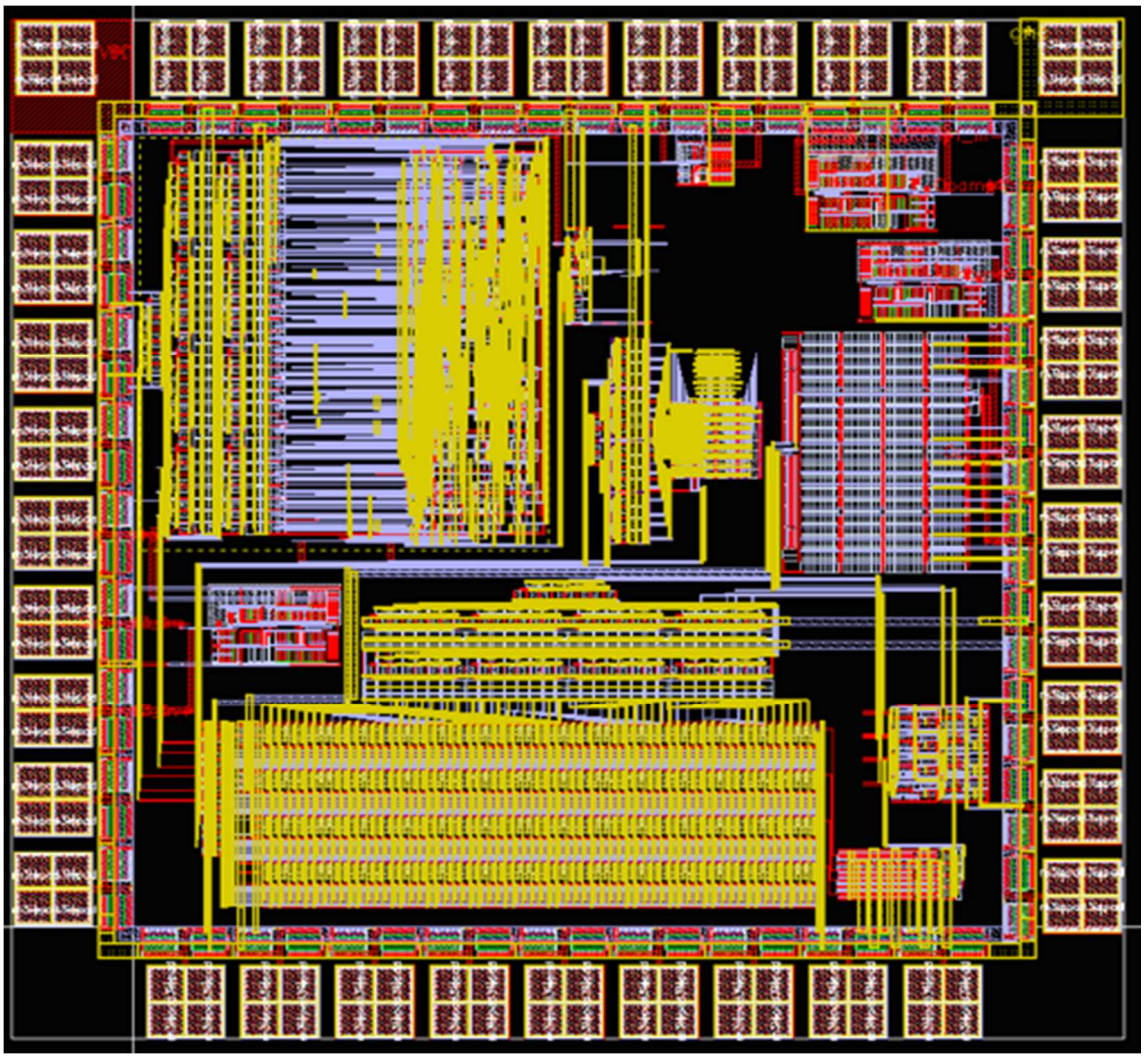

Figure 5.14: EIS CMOS IC Layout in Cadence Virtuoso Layout Tool

EIS CMOS IC layout is designed using Cadence Virtuoso Tool. Common centroid and interdigitized layout techniques are used to avoid manufacturing defects, gradients or electromigration. Common centroid technique is used for operational amplifiers to get very low input offset voltage. Dummy transistors are implemented in ROM memory layout to avoid manufacturing defects. Electrostatic discharge blocks (ESD) and bondpads are designed for protection of pins. Pin configuration of this custom

IC is shown in appendix. Blocks in layout are shown in figure 5.15. The size of this IC is 1.5 x 1.5 mm. 65-pin Pin Grid Array (PGA65) packaging is chosen for this IC. This is 1 inch square package with 0.4 inch cavity size. The pins of this package are arranged on an 10 x 10 pin grid at 0.1 inch centers. There are two full rows of pins around the outside.

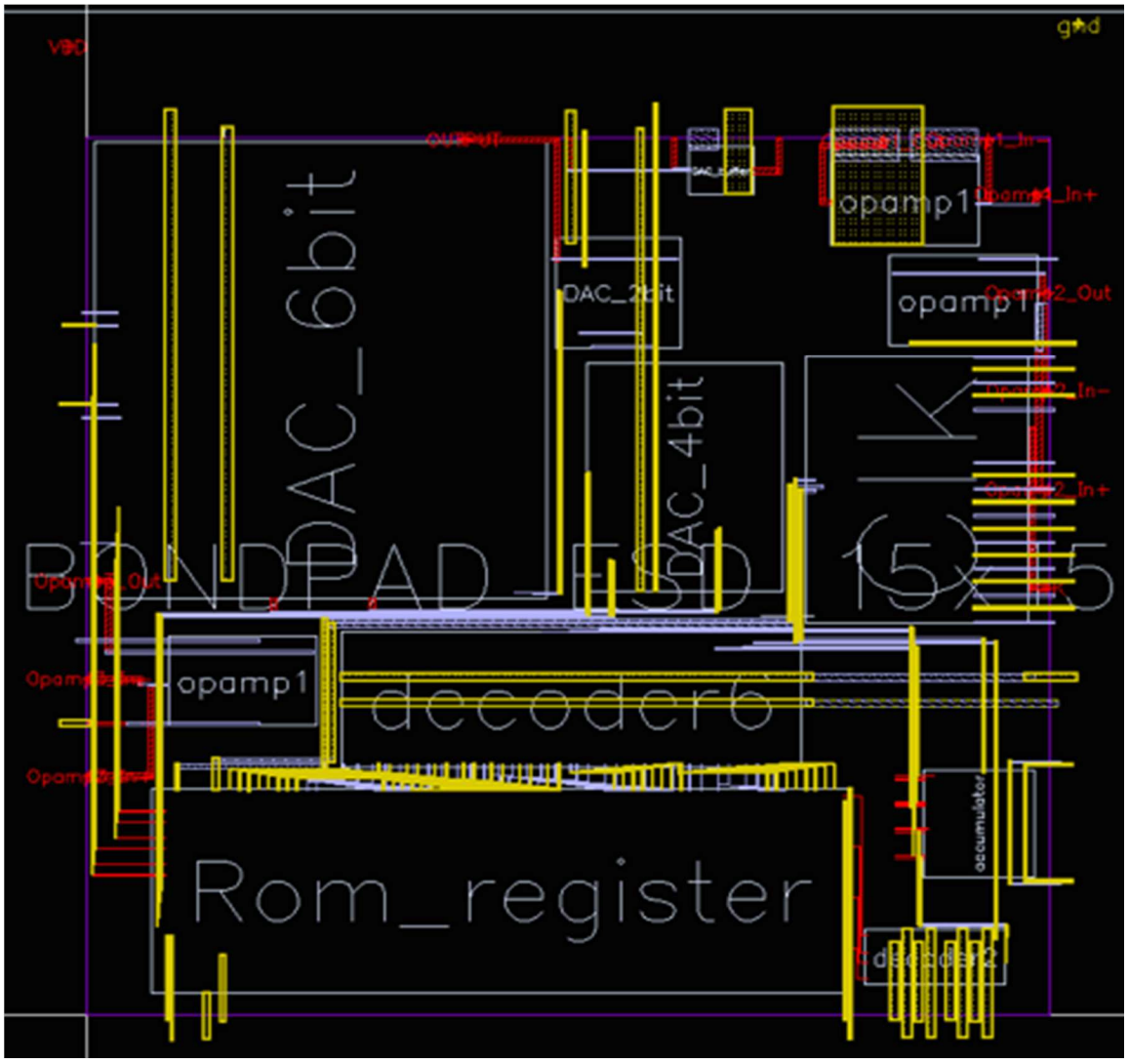

Figure 5.15: Block Layout of IC

5.4 Simulation Results

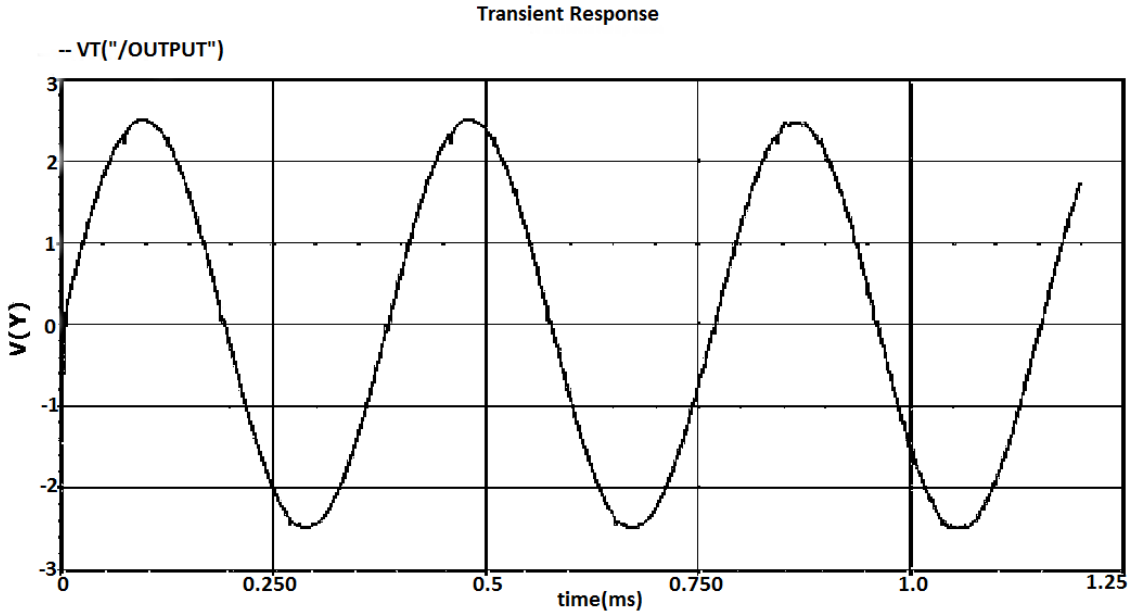

Figure 5.16: Transient Response of EIS CMOS IC in Cadence Spectre Simulation

Entire EIS block is simulated in typical PVT corner in Cadence spectre simulation tool. An output of sine wave generator block is shown in figure 5.4. For this simulation an input clock of 2 MHz is given. Sine wave has no DC shift since power supply of ±2.5 V is used. There is some ripple noise in sine wave but it can be reduced by using external RC filter. In the next generation of this EIS custom IC, an internal filter can be used to reduce these ripples.

Three opamps are simulated in typical PVT corner. AC response of one of the opamps is shown in figure 5.5. This opamp is simulated from DC to 1 GHz frequency for AC response. Unity gain frequency of 1.532 MHz is achieved in typical PVT corner. Phase margin of 88^{o} is achieved. Hence these opamps are highly stable. Noise, PSRR and

CMRR are tested but not the most important parameter. This opamp has 66.5 dB DC gain with 1kHZ of 3-dB frequency.

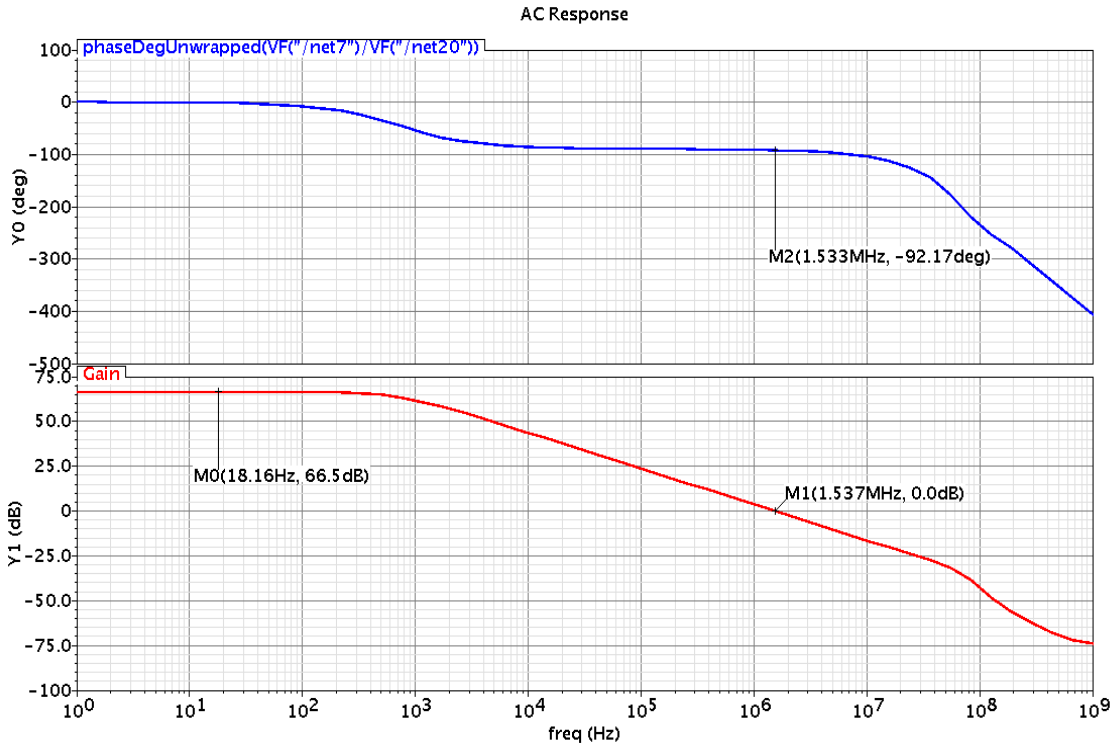

Figure 5.17: AC Response of Opamps in Cadence Simulation Tool

CHAPTER SIX

TESTING

Testing of both the discrete component and integrated configurations presents numerous challenges. Since EIS requires a very low magnitude (10 mV) peak to peak AC excitation signal, ambient noise sources have a significant effect on the measurements. The following two methods were used to characterize each of the systems.

6.1 Testing of Randles Circuit Model with the Discrete EIS configuration:

In testing the discrete configuration with the Randles circuit model the following components and equipment was needed:

- 9V battery
- Arduino Mini Pro
- FTDI basic breakout board
- MiniGen Signal generator
- NTE987 quad opamp IC
- Randles model
- Lock-in amplifier
- Resistors and capacitors
- Jumpers and connectors

The entire circuit was assembled and tested as shown in figure 6.1. The FTDI basic breakout board was connected to a laptop through a USB to mini-USB adapter cable to supply power to the boards. The MiniGen generator shield was mounted on top of the Arduino mini pro board reducing footprint for the circuits

to better match the aforementioned form factor. Connections were made using jumper cables as shown in figure 6.1.

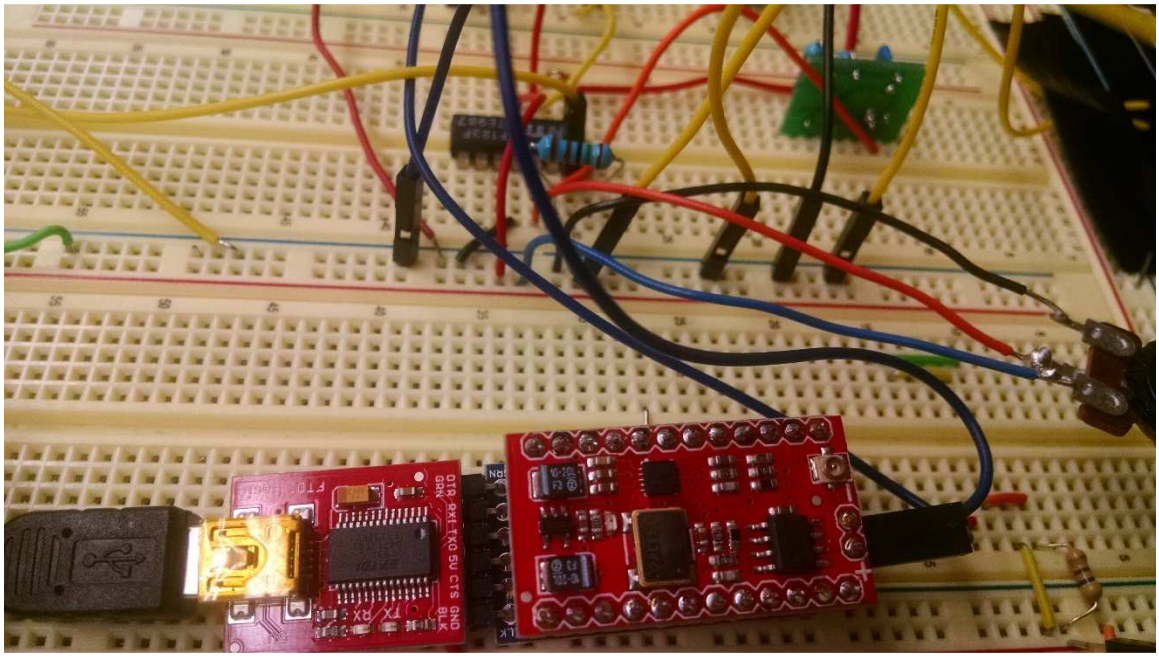

Figure 6.1: Testing of Discrete EIS System

EIS testing has an advantage over other molecular detection methodologies, since the electrochemical cell can be represented by electronic model for both simulation and testing. Hence for our tear diagnosis application, a set of Randles model cells was designed using table 6.1. The Randles model was described in Chapter 3 and is shown in figure 3.2.

Due to the lack of availability for such specific value discrete components, an approximation was made and the nearest value components were selected; these values are shown in Table 6.2.

Solution	Concentration	R1(Ω)	R2(Ω)	C(nF)
IgE	1 ng/ml	56.24	2549	73.06
	200 ng/ml	53.48	3969	71.2
	10 mg/ml	53.67	6117	70.51
Lactoferrin	0.5 mg/ml	58.61	1939	80.97
	1.5 mg/ml	60.19	4301	79.39
	2.5 mg/ml	60.26	7404	79.1

Table 6.1: Theoretical Randles Model Values

Solution	Concentration	R1(Ω)	R2(Ω)	C(nF)
IgE	1 ng/ml	56	2700	100
	200 ng/ml	56	3900	100
	10 mg/ml	56	5600	100
Lactoferrin	0.5 mg/ml	56	1800	100
	1.5 mg/ml	56	4700	100
	2.5 mg/ml	56	8200	100

Table 6.2: Practical Randles Model Values

Each Randles model cell was implemented as a component designed in Eagle as a printed circuit board. After manufacturing of PCB and soldering selected components as shown in table 6.2, the Randles model cells were populated as shown in figure 6.2. Six different Randles model cells were soldered and the size of each Randles model cell is approximately 10 mm x 15 mm.

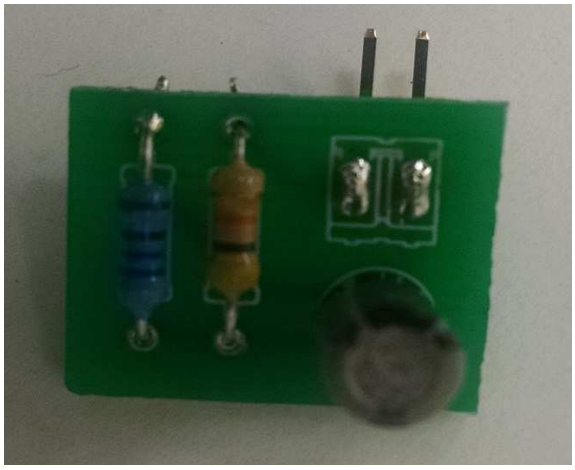

Figure 6.2: Randles Model PCB

6.2 Testing of Randles Model with Integrated EIS:

The Randles model was also used to characterize the Integrated EIS CMOS IC. The following components and equipment were used:

- 9V battery
- Custom designed board for EIS CMOS IC
- EIS CMOS IC
- Lock-in Amplifier
- Arduino Uno microcontroller board
- Jumpers and connectors
- Resistors and capacitors

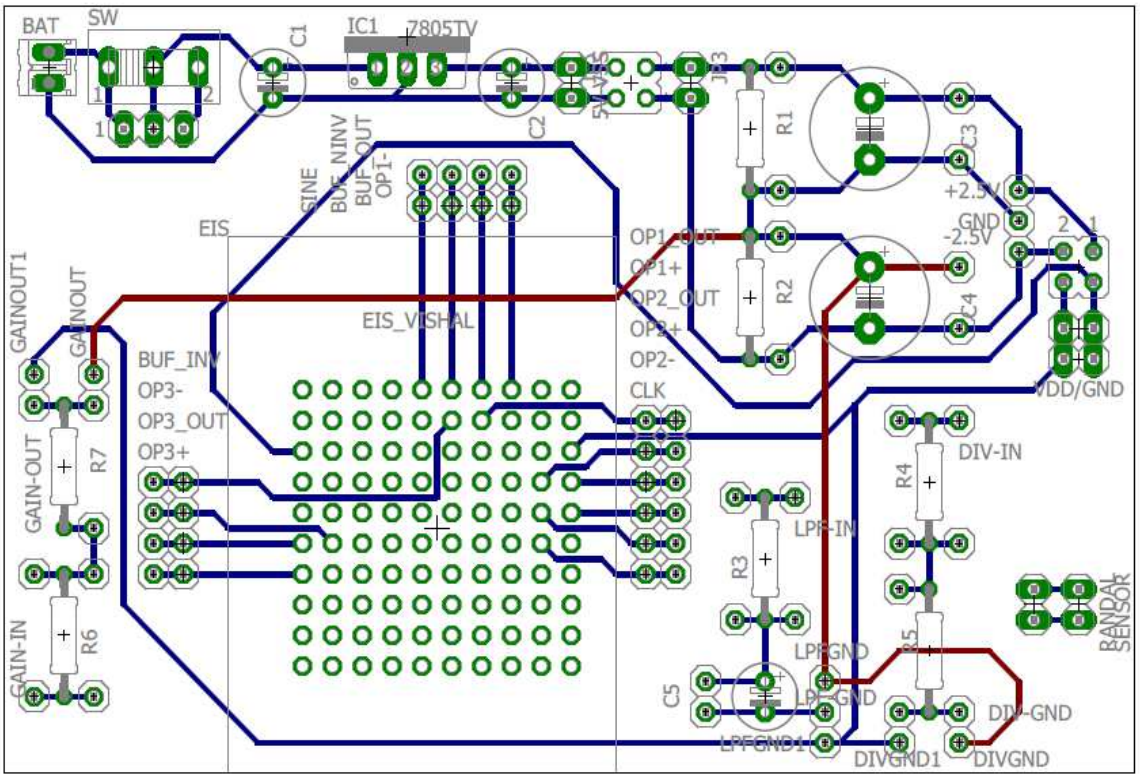

Figure 6.3: EIS CMOS IC Testing Board Layout in Eagle PCB Layout Tool

In order to complete the setup and fully characterize the EIS IC, a PCB was designed for the chip as well as all the necessary discrete components and batteries. This EIS CMOS IC testing board is designed using Eagle PCB design tool. This board contains a regulated 5V power supply to power the chip. This means any battery greater than 5V can be connected to power up the board for testing. This is the only power supply needed to test the entire Integrated EIS system. A battery was used as the power supply for testing, because they have very low noise. Figure 6.2 shows the manufactured board with all components soldered onto the board. A battery can be mounted at the bottom of this board and the EIS CMOS IC can be mounted on the black

ZIF (zero in force) socket. A ZIF socket is used to easily remove and mount custom ICs. The final circuit test assembly is shown in figure 6.5.

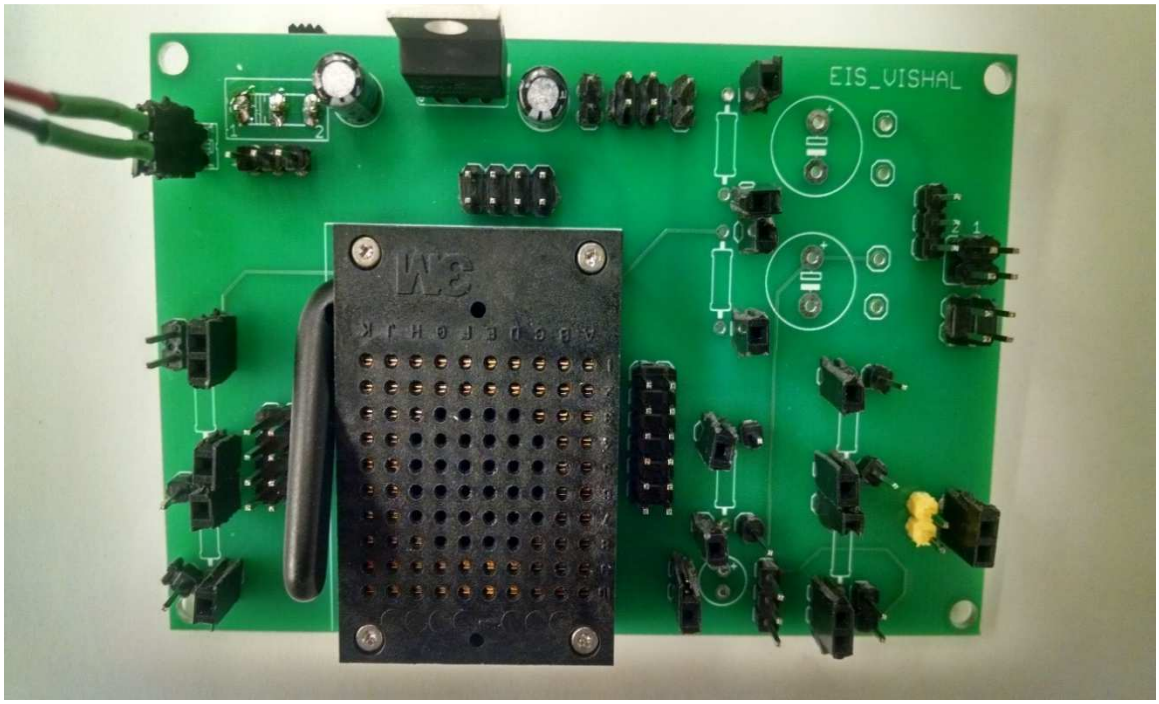

Figure 6.4: EIS CMOS IC Testing Board

The external components such as resistors, capacitors, and the Randles model cell are mounted on a breadboard. Connections were made using jumper wires, and a potentiometer was used to set the formal potential offset. A Lock-in amplifier was used to measure phase and magnitude differences between the input and output signals.

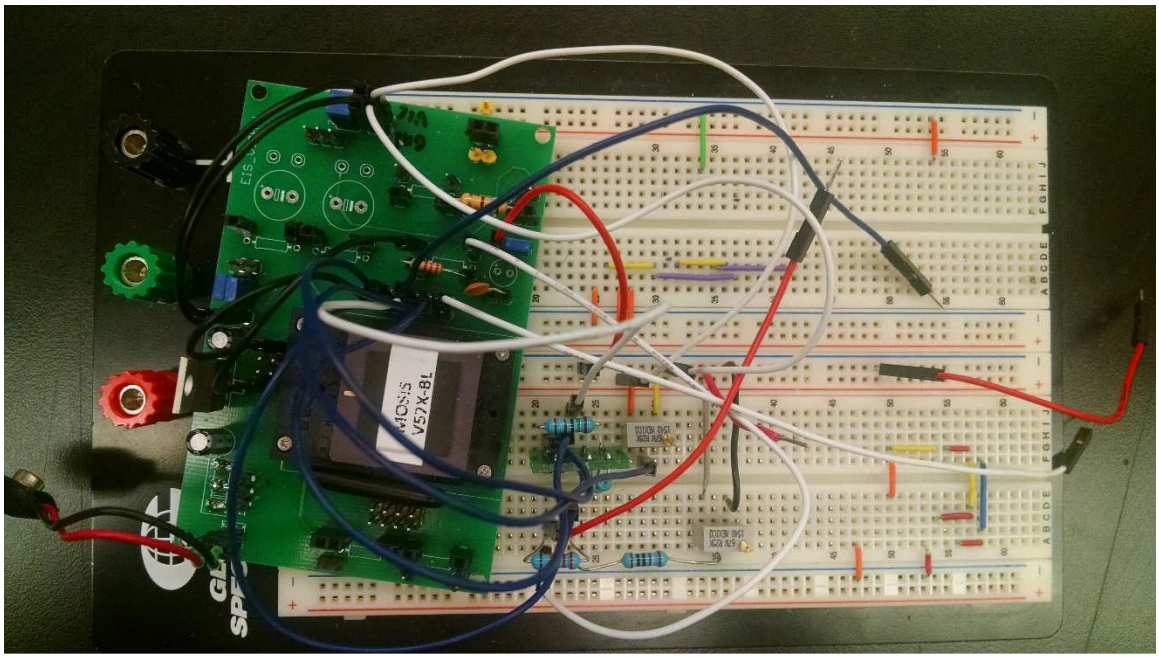

Figure 6.5: Testing of Integrated EIS System

CHAPTER SEVEN

RESULTS AND CONCLUSION

The discrete component EIS system has a Sparkfun MiniGen Signal generator shield which can generate sine, triangular or square waves at up to 3MHz and approximately 1V peak to peak amplitude. This waveform is offset by half the power supply magnitude, which is 2.5 V. For biomedical applications, an excitation frequency of 10 KHz or below is required. After our testing unit was set up as mentioned in previous chapters, an arduino code was flashed to the Arduino Mini Pro board (code is included in Appendix A) to generate a sine wave signal at the output.

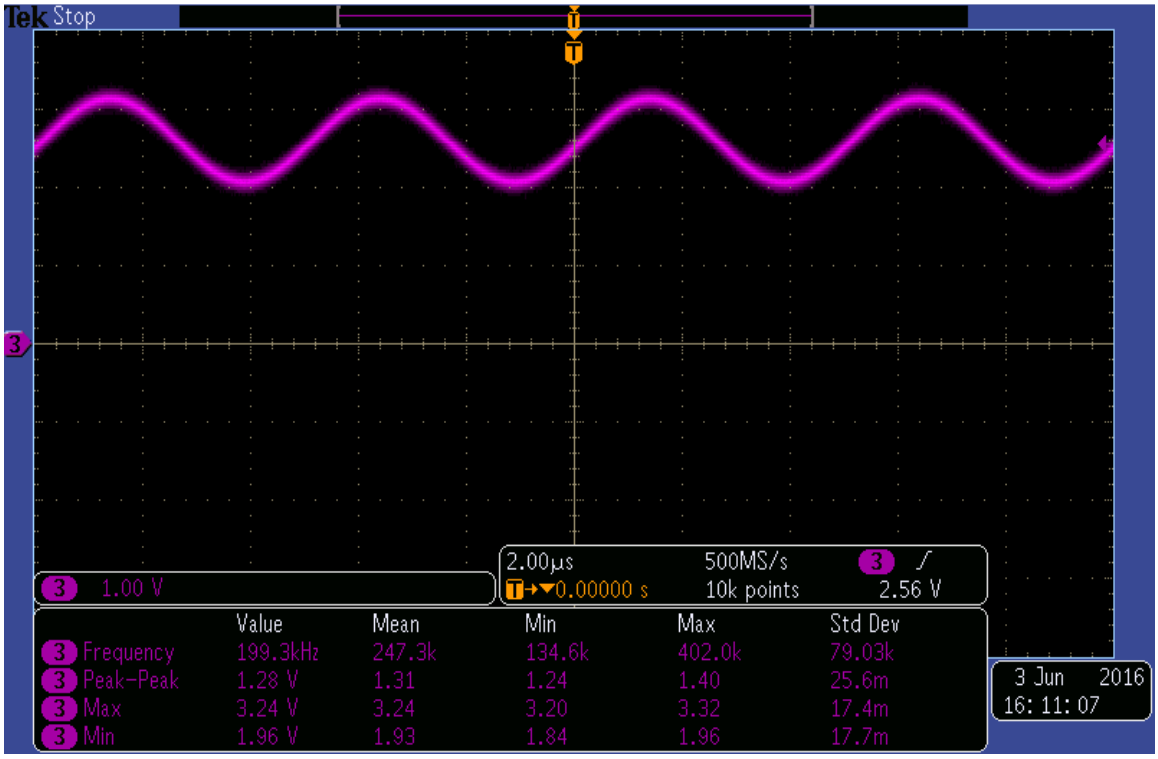

Figure 7.1: Output Sine Wave of MiniGen Signal Generator

Figure 7.1 is a screenshot which shows one of the tested sine waves generated at MiniGen signal generator output. The sine wave generated is very stable with a DC offset

of 2.5 V and peak to peak voltage of 1.28 V. There is not much noise in sine wave signal and its analysis is shown later in this chapter.

The custom EIS CMOS chip was tested to assess the sine wave output generated. Figure 7.2 is a screenshot of the sine wave output at 121.5 Hz. The output is again DC shifted by half the power supply, 2.5V. The peak-to-peak amplitude of this sine wave is approximately 3V which is a significant improvement over the discrete component implementation of the system.

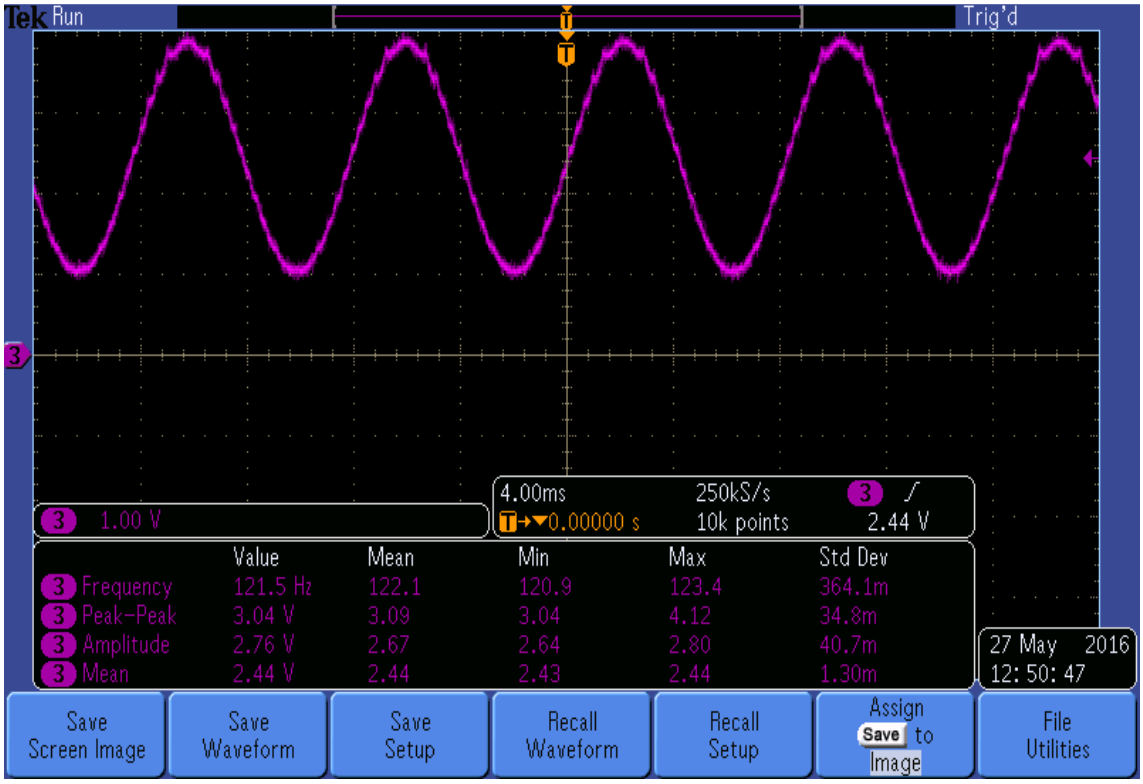

Figure 7.2: Output Sinewave of EIS CMOS IC

It is evident from the screenshot in figure 7.2, the sinewave has significant noise at frequencies well above the base frequency. This means the noise can be removed by applying an external RC filter. The output of the RC filter is very smooth and low noise.

To generate this sine wave, an input clock frequency of 32 KHz was provided using the Arduino UNO board which was programmed to generate the sinusoidal signal. The clock signal generated by the Arduino UNO is shown in figure 7.3.

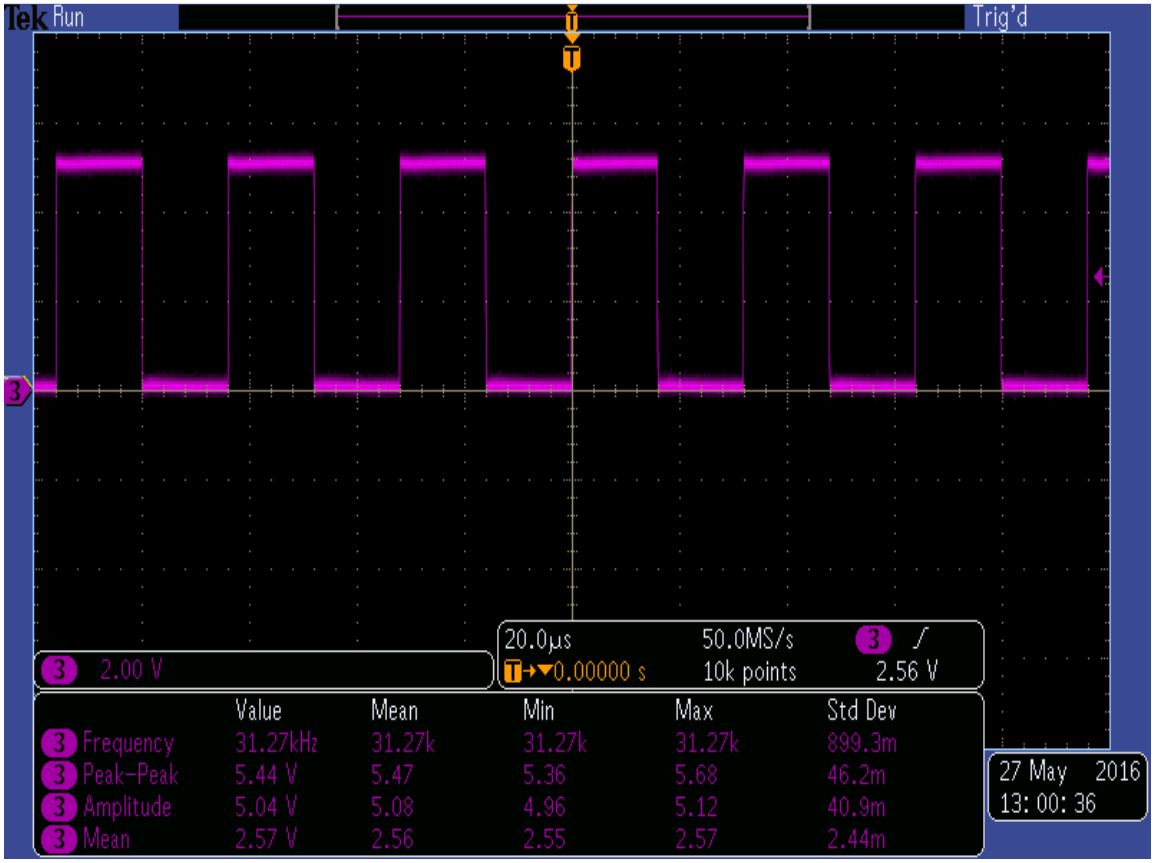

Figure 7.3: Input Square wave to EIS CMOS IC

To find the harmonic distortion in the sine wave generated by the integrated EIS chip, a fast Fourier transform was applied to the waveform by the oscilloscope. Figure 7.4 shows the harmonic distortion of the sine wave. The fundamental frequency of sine wave was 122 Hz, and its amplitude at 122 Hz was -3.284 dB. The amplitude at the second harmonic frequency of 244 Hz was -48.15 dB. The difference between the amplitude of the first and second harmonics was 44.87 dB. This ripple noise on the fundamental frequency led to inaccurate measurements of the EIS system.

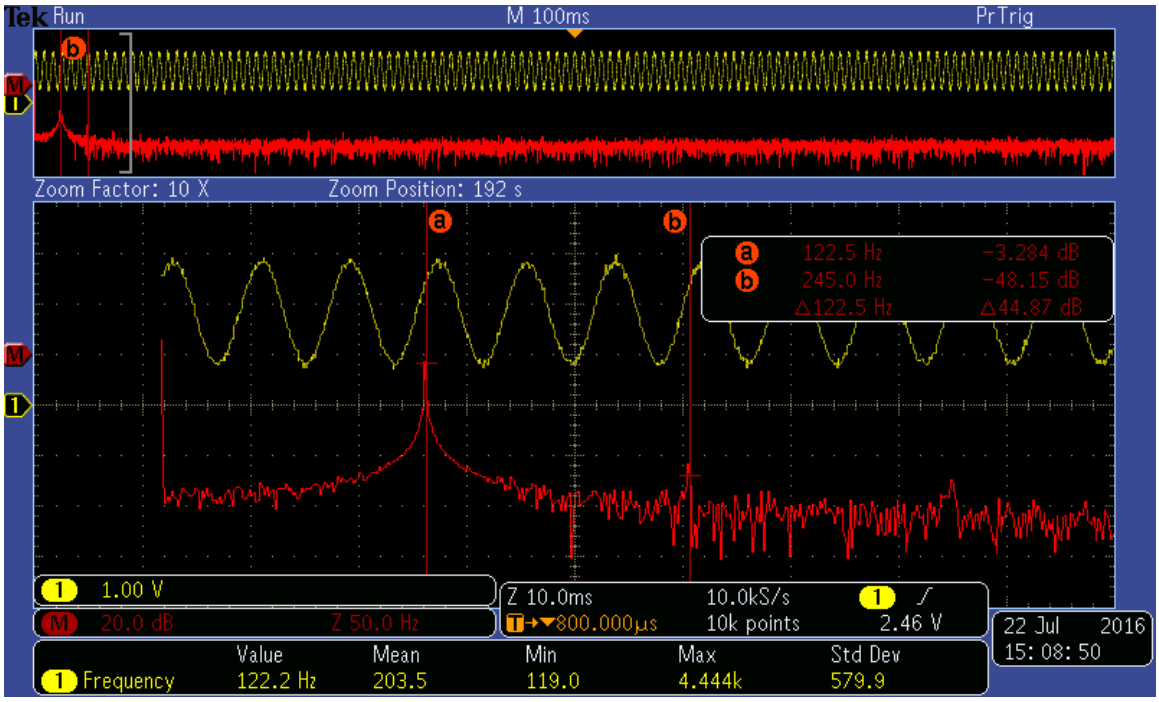

Figure 7.4: Fourier Transform of Sine Wave Without Filter

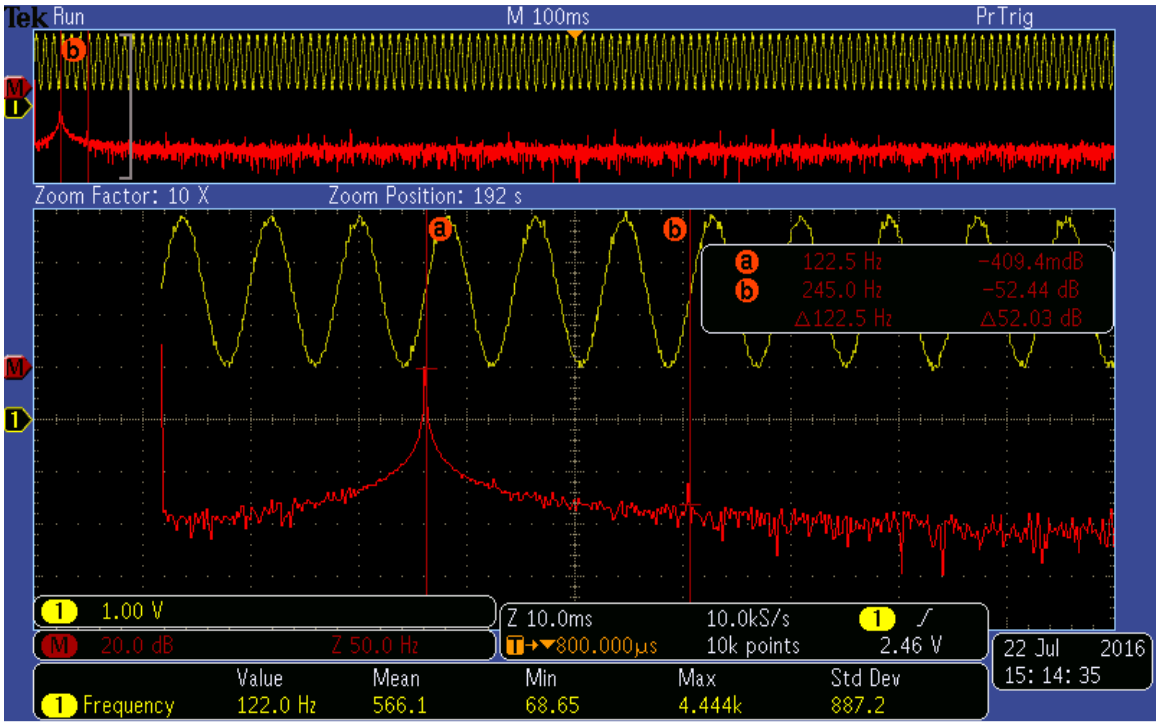

Figure 7.5: Fourier Transform of Sine Wave With Filter

To reduce the noise, an external RC low pass filter was applied. After passing sine wave signal through low pass filter, a smooth sine wave is achieved with the fast Fourier Transform shown in figure 7.5. The magnitude of the sine wave at its fundamental frequency is -409.4 mdB, whereas the magnitude at its second harmonic frequency is -52.44 dB. The difference between the magnitude of the first and second harmonics is 52.3 dB which is a 7.43 dB improvement over the integrated EIS system without the filter.

For our tear diagnosis application, testing was performed using the discrete component-based EIS configuration with the Randles circuit model cells. These Randles circuit models were based upon the information from Table 6.1. The excitation signal frequency range is from 1Hz to 3 KHz. The results are compared with theoretical values, and the following graphs compare experimental data with these theoretical values.

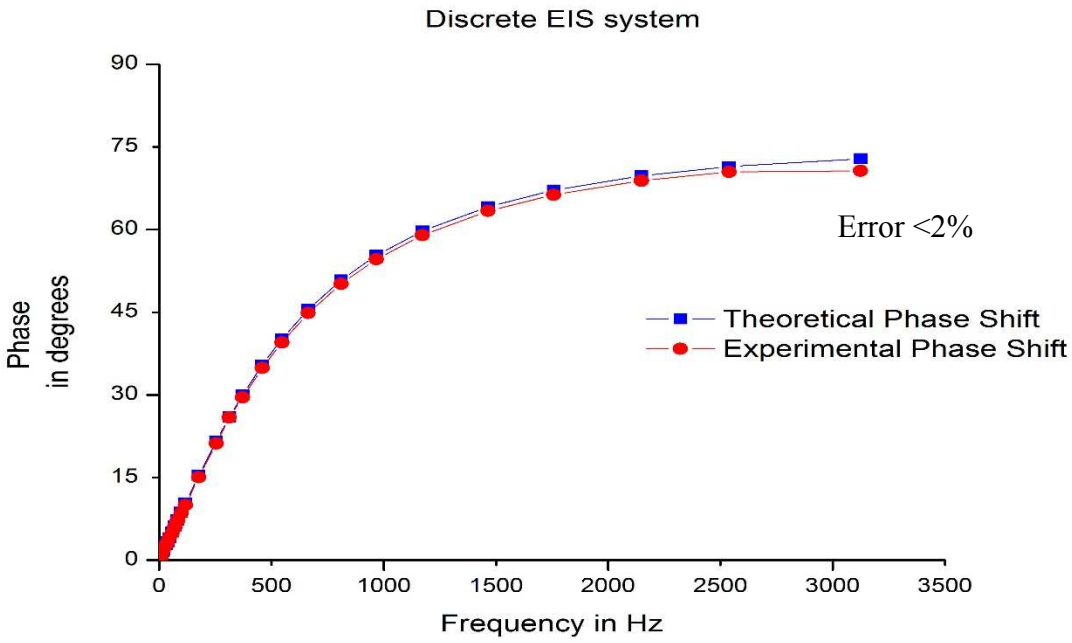

Figure 7.6: Phase Shift of 1ng/ml IgE Solution Randles Circuit Model

The phase plot in figure 7.6 is for a Randles circuit model cell representing IgE protein solution with a 1ng/ml concentration. The error between the two curves for the phase shift is less than 2%. Similarly magnitude change is plotted against the frequency as shown in figure 7.7. The magnitude change due to

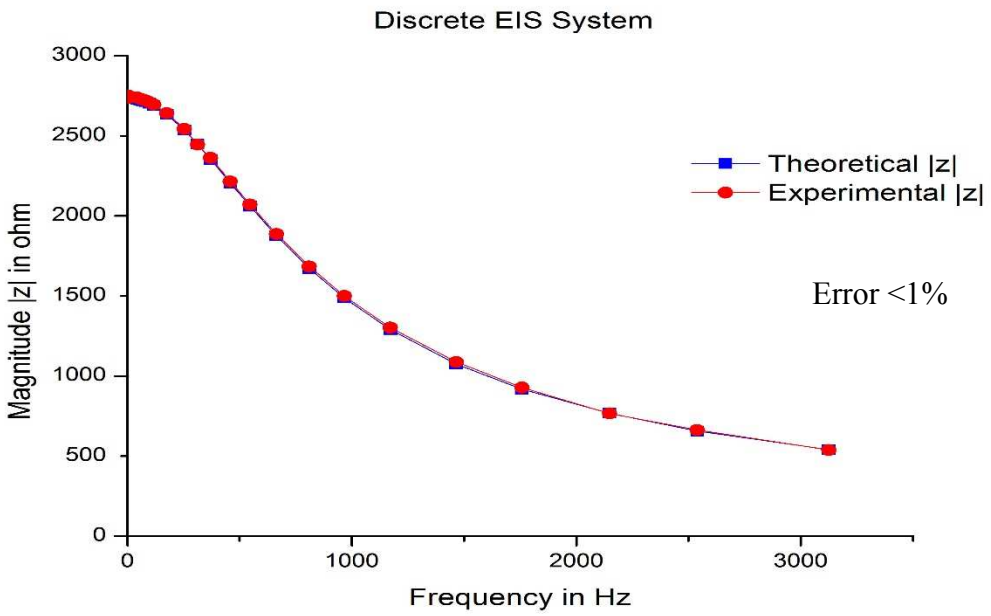

Figure 7.7: Magnitude Change of 1ng/ml IgE Solution Randles Circuit Model

the same Randles cell closely follows the theoretical values. The maximum error in the experimental magnitude relative to the theoretical change is less than 1%. The phase shift and magnitude values were used to characterize the accuracy of the system in measuring a 1ng/ml IgE protein solution. The theoretical and experimental data is compared in the graph shown in figure 7.8.

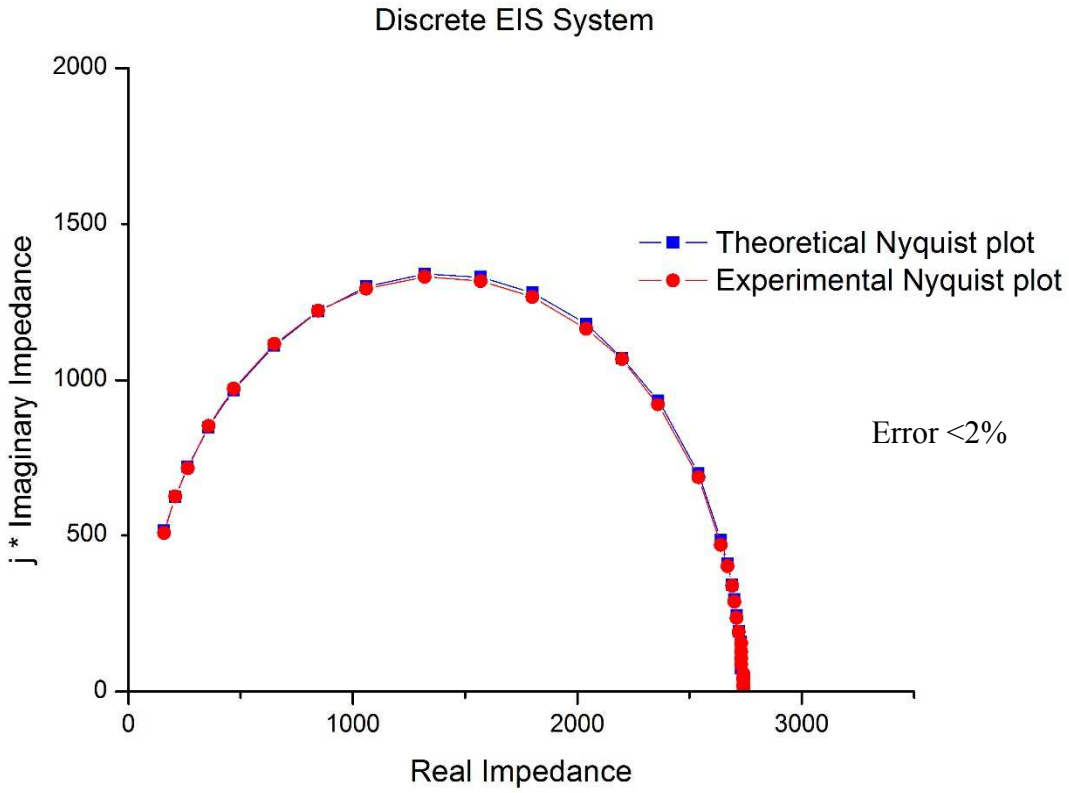

Figure 7.8: Nyquist Plot of 1ng/ml IgE Solution Randles Circuit Model

The imaginary impedance is plotted against real impedance to characterize the 1ng/ml concentrated IgE protein solution. The experimental values closely follow the theoretical values, and the error is just over 1%. The Nyquist plot was based on the values for solution resistance, double layer capacitance, and charge transfer resistance.

7.1 Summary:

Aims of this project is to design a compact, lightweight, handheld battery operated EIS system that is low cost. Table 7.1 summarizes the specifications for discrete and integrated EIS systems and compares them with commercial EIS systems.

Specification / EIS system	Dimensions (inch)	Volume (Cu. inch)	Weight (g)	Cost ($)
EZstat Pro	10 x 9.625 x 4	385	4876	6500
Powerstat-05 CE	19 x 7.5 x 22	3135	22680	15300
Powerstat-20	19 x 7.5 x 22	3135	22680	33600
Discrete EIS	4 x 1 x 1.2	4.8	60	1500*
Integrated EIS	4 x 3 x 2	24	100	2500**

Table 7.1: Comparison of EIS Systems

It is evident from above table that both discrete and integrated EIS offer better solutions for handheld devices. It should be noted that the integrated EIS was implemented on a test board, so its size and weight can be further reduced by designing a smaller board with surface mount devices. The cost of the integrated EIS configuration could be further be reduced by increasing the manufacturing volume for the IC parts.

7.2 Future Improvements:

The integrated EIS system could be further improved by designing an on chip PLL to control the sine wave frequency. This will reduce the external circuits required and thus reduce the system size and weight. For better harmonic distortion for the sine wave, a tracking low pass filter can be integrated on chip. The ROM size can also be reduced by implementing an up and down counter and using only two ROM modules. Finally, an integrated lock-in amplifier will improve phase and magnitude measurements.

For the discrete EIS system configuration, it can further be improved using a bluetooth module along with the Arduino Pro to transmit data wirelessly to Bluetooth

devices such as phone or laptop. This data can be processed on the devices, so the data can be plotted in Nyquist or bode plot form. Finally, the data can be stored into its database.

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APPENDIX A

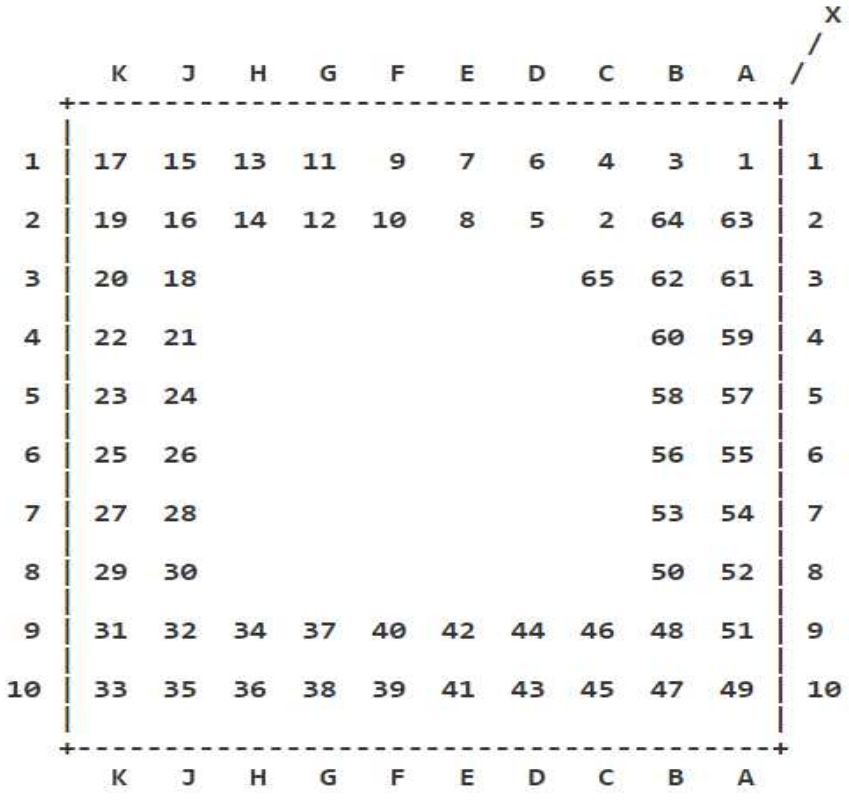
ARDUINO MINI PRO CODE FOR GENERATING SINE WAVE

```
#include <SparkFun_MiniGen.h>
#include <SPI.h>

MiniGen sig_gen;


void setup() {
  // put your setup code here, to run once:
sig_gen.reset();                          // Resets the registers and gives default output

sig_gen.setMode(MiniGen::SINE);   /* parameters can be - MiniGen::TRIANGLE,
MiniGen::SINE, MiniGen::SQUARE, or MiniGen::SQUARE_2 */

sig_gen.selectFreqReg(MiniGen::FREQ0);          /* parameter passed can be FREQ0 or
FREQ1  */

uint32_t freqRegVal = sig_gen.freqCalc(1000);    /* parameter is desired frequency in Hz
and returns 32 bit register value to be passed to FREQ register */

sig_gen.adjustFreq(MiniGen::FREQ0, MiniGen::FULL, freqRegVal);
/*sig_gen.adjustFreq(reg, mode, newFreq); reg can be either MiniGen::FREQ0 or
MiniGen::FREQ1, depending on where the user wants to write the value. Mode can be
either MiniGen::FULL, MiniGen::COARSE, or MiniGen::FINE. For the first, newFreq
should be an 32-bit unsigned value freqRegVal */


}

void loop() {
  // put your main code here, to run repeatedly:

}
```

APPENDIX B

INTEGRATED CIRCUIT PACKAGING

For custom designed IC, PGA65 ceramic packaging is chosen through MOSIS service. Detail information of this package taken from MOSIS website is as following: This is a 1.000" square package with a 0.400" cavity (topside) with Kyocera part number KD-P86542-A. The pins of this package are arranged on an 10 x 10 pin grid at 0.1" centers. There are two full rows of pins around the outside. The following diagram depicts the bonding pad to pin connectivity as viewed from the top of the package (or the top of the socket into which the package is plugged), with the index at the upper right corner. (This view corresponds to the MOSIS bonding diagram that has pin #1 in the upper right hand corner and proceeds counterclockwise around the die.) The columns of the grid are labelled alphabetically and the rows numerically.



Pad to Pin Layout -- TOP View

Pin Configuration:

PIN	FUNCTION
4	OPAMP1_IN-
5	OPAMP1_OUT
6	BUFFER_OUT
7	BUFFER_IN+
8	BUFFER_IN-
9	OUTPUT (SINE)
20	VDD
25	OPAMP3_OUT
26	OPAMP3_IN-
27	OPAMP3_IN+
56	CLK
57	OPAMP2_IN+
58	OPAMP2_OUT
59	OPAMP2_IN-
60	OPAMP1_IN+
61	GND