PID Controller Tuning and Adaptation of a Buck Converter

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved August 2016 by the
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August 2016

ABSTRACT

Buck converters are electronic devices that changes a voltage from one level to a lower one and are present in many everyday applications. However, due to factors like aging, degradation or failures, these devices require a system identification process to track and diagnose their parameters. The system identification process should be performed on-line to not affect the normal operation of the device. Identifying the parameters of the system is essential to design and tune an adaptive proportional-integral-derivative (PID) controller. Three techniques were used to design the PID controller. Phase and gain margin still prevails as one of the easiest methods to design controllers. Pole-zero cancellation is another technique which is based on pole-placement. However, although these controllers can be easily designed, they did not provide the best response compared to the Frequency Loop Shaping (FLS) technique. Therefore, since FLS showed to have a better frequency and time responses compared to the other two controllers, it was selected to perform the adaptation of the system. An on-line system identification process was performed for the buck converter using indirect adaptation and the least square algorithm. The estimation error and the parameter error were computed to determine the rate of convergence of the system. The indirect adaptation required about 2000 points to converge to the true parameters prior designing the controller. These results were compared to the adaptation executed using robust stability condition (RSC) and a switching controller. Two different scenarios were studied consisting of five plants that defined the percentage of deterioration of the capacitor and inductor within the buck converter. The switching logic did not always select the optimal controller for the first scenario because the frequency response of the different plants was not significantly different. However, the second scenario consisted of plants with more noticeable different frequency responses

and the switching logic selected the optimal controller all the time in about 500 points. Additionally, a disturbance was introduced at the plant input to observe its effect in the switching controller. However, for reasonable low disturbances no change was detected in the proper selection of controllers.

To my mom and my sister

ACKNOWLEDGMENTS

I want to thank my advisor Dr. Konstantinos Tsakalis for his continuous support, motivation, patience and knowledge that lead me to successfully complete my PhD degree.

Besides my advisor, I also want to thank the rest of my committee members: Dr. Bertan Bakkaloglu, Dr. Armando Rodriguez, Dr. Andreas Spanias and for their insight and feedback that incented me to broaden my research from different points of view.

A special thanks to my friends who always listened, cheered me up and reminded me that I could achieve my goals: Michael Thompson, Margarita Olivera and Raquel Riande.

I also want to thank my fellow labmates: Ashfaque Shafique and Rakesh Joshi for stimulating discussions, for working together, and for all the joyful moments shared during the last four years.

I would also like to acknowledge SENACYT for providing the funds to study my doctorate program at Arizona State University.

Last but not least, I want to thank my mom and my sister for always being there for me. Mom, you always encouraged me to go far and I have listened to your advice. I could not have done this without your support.

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Chapter 1

INTRODUCTION

What if we could have electronic devices that did not degrade over time? This is a question that many engineers around the world have been trying to answer for a long period of time. Everyday many electronic manufacturing companies are trying to come up with new theoretical and experimental analysis to create more efficient electronic prototypes. In that sense, the system identification and control of buck converters have become a topic of interest. Buck converters, which are also known as power converters or DC-DC converters, are electronic devices that change a voltage from one level to another one at a very high frequency. The LM27402 is a synchronous DC-DC converter which switching frequency can vary in a range that goes from 200 kHz to 1.2 MHz [30]. It incorporates an input feed-forward voltage that enables it to maintain stability for the entire input voltage range. Some applications of the LM27402 buck converter go from telecommunications, data-communications and networking to distributed power architectures. Additionally, they can be used for any general buck converter purposes which may include Field Programable Gate Arrays (FPGA) and Application Specific Integrated Circuit (ASIC). However, due to factors like aging, degradation or failures, the DC-DC converters require a system identification process to track and diagnose their parameters.

The parameter estimation of a buck converter is a topic that has attracted a lot of attention in the recent years due to the extended use of these devices in everyday applications. However, the system identification process should be performed on-line to not affect the normal operation of the device.

Identifying the parameters of the system is essential to design and tune a proportional-integral-derivative (PID) controller that can compensate for failures in the system. This does not only represent a big advantage for monitoring purposes, but also allows the implementation of adaptive controllers [17], [34]. Therefore, buck converters may become more efficient and their lifetime may increase dramatically.

In summary, our motivations to study the control of DC-DC converters lie on the fact that high switching frequency converters tend to have lower filter component values, with a larger variation and sensitivity. Moreover, the component values degrade over the lifetime of operation of the circuit and a change in the component values can lead the system to instability.

1.1   Preliminary Work

In the recent years we have seen a lot of progress in the identification of the buck converter [4]. Some of that work lies on the cross-correlation technique which is a non-parametric system identification method [20] that allows the digital control of the system [23], [22]. Similarly, a circular cross-correlation technique was used to obtain the transfer function of a power converter [25]. In this paper, a maximum-length pseudo random binary sequence (m.l.b.s) was used to excite the system. Their use has become popular because it is easy to generate by using shift registers and an appropriate feedback [18]. Additionally, it has nice properties in the means of periodicity and frequency attributes [29]. The uncertainty of the system is computed by using a fuzzy density approximation. Yet, the signal-to-noise (SNR) ratio plays an important role in the circular correlation technique [16].

Other approaches have also been used to perform a system identification of the

power converter such as the black-box technique [9]. In that approach, the authors aimed to obtain a small-signal linear model in discrete time that describes the system as a time-invariant structure. Additionally, the impulse response data has offered an alternative to perform system identification of discrete systems that do not require the numerator to be of a lower degree than the denominator [28].

In addition, thanks to the advance of digital devices that are capable of providing faster responses, some approaches have been suggested for the control of buck converters in discrete time [21]. Furthermore, these controllers are programmable and small in size which makes the controlled system more efficient. Another digital control has been developed by superimposing a small control signal at each switching cycle and using a pole-placement algorithm [24]. Digital control was also used for a DC-DC converter for a radio frequency (RF) power amplifier [37]. In this paper a FPGA-based digital controller was implemented which allowed to program the mode transition as well as other controller parameters.

This document is organized as follows: chapter 2 describes the buck converter design. It provides information on what parameters are indispensable to obtain the capacitance, inductance, diode and MOSFET. These parameters are: the input voltage range, the regulated output voltage, the maximum output current and the converter's switching frequency. It also presents some recommendations for the selection of every component to avoid inappropriate performance or elements that can be operating in the limit of safety conditions.

Chapter 3 describes the plant modeling of the DC-DC converter from the nominal point of view. It also describes the parameters to generate the Pseudo Random Binary Sequence (PRBS) and how to verify that the signal has enough strength within the frequencies of interest through the Fast Fourier Transform (FFT) plot.

Furthermore, it describes the process to scale the plant down to simplify computations in the simulation and system identification stages. The chapter also makes reference to the closed-loop plant that is obtained by performing system identification on an evaluation board. This allows to obtain the open-loop plant by having information of the controller that we are using. Therefore, a comparison of the simulated data and experimental data can be performed. The on-line system identification was performed for the simulated data and the estimation and parameter error were calculated to describe how fast the system was converging.

In chapter 4 we start with a description of the type 3 controller used in this study. The controller can be described as a transfer function that has two zeros and three poles. This is also the same type of controllers that has been implemented in the evaluation board. Three different techniques were performed to design the PID controller: first, classical control was used to obtain the gains of the PID controller using gain and phase margin specifications together with a low pass filter. Second, a pole-zero cancellation technique was also utilized to design a PID controller. For both techniques the values of resistors and capacitors were obtained based on the type 3 controller circuit. Finally, the Frequency Loop Shaping (FLS) technique was described and used to design another PID controller. This method is based on an optimization problem in which we try to obtain the gains of the controller by approximating the compensated open-loop to a specific target in an L_∞ sense. Results showed that this controller provided a better frequency and time responses compared to the other types of controllers; however, it does not provide feasible values for resistors and capacitors consistent with the type 3 controller. Therefore, an optimization problem is necessary in order to obtain a controller that satisfies the constraints for resistor and capacitor values or a digital controller should be implemented instead. A digital controller

requires a suitable sampling time to avoid instabilities in the system. This chapter also describes all the discretization methods and the best selection of the sampling time for our application.

Chapter 5 gives reference to the different methods to adapt a system: direct and indirect. An indirect method attempts to find the parameters of the system prior designing the controller. On the other hand, the direct method seeks to obtain the parameters of the controller without having to wait until the system identification has been performed. The results from the full adaptation using the indirect scheme showed that the system will take around 2000 points to identify the scaled plant before the controller can be designed on-line. Two different scenarios were described to observe how the system was adapting using both the indirect method and the robust stability condition computation.

Scenario 1 consisted of the following plants: 1) The original plant, 2) A decaying plant with 10% of deterioration in the inductor while the capacitor remained the same, 3) A decaying plant with a 10% of deterioration in the capacitor while the inductor remained the same, 4) A decaying plant with a 10% of deterioration in both the capacitor and the inductor, and 5) A decaying plant with a 15% of deterioration in both the capacitor and the inductor. However, although this scenario is conceivable in real life, the frequency response of all the plants do not depict a significant difference from each other which affected how the controller was selected using robust stability conditions. That's why we also studied a second scenario with more remarkable different frequency responses.

Scenario 2 consisted of the following plants: 1) The original plant, 2) A decaying plant with degradation of 10% in both the capacitor and inductor, 3) A decaying plant with a deterioration of 20% in both the capacitor and the inductor, 4) A decaying plant

with a degradation of 30% in the capacitor and inductor values, and 5) A decaying plant with a deterioration of 40% for the capacitor and the inductor. The results showed that by using PID controllers for each of the above plants designed using the Frequency Loop Shaping (FLS) technique, the optimal controller is selected when the robust stability condition is evaluated. The controller selection is performed in about 500 points for the scaled plant which makes it more suitable than performing a full adaptation.

Chapter 6 makes a description of uncertainties and how they are taken into account so that the designed controller can maintain stability of the closed-loop system and provides an acceptable performance of the plant even in the presence of uncertainties. A especial emphasis is put into the additive uncertainty and how it is represented so that the current plant can be written as the result of the nominal plant plus a weighting term (which increases at high frequencies) times the uncertainty. This result leads to the computation of the robust stability condition which provides a measure of error to determine which controller should be selected at every plant transition. The controlled output of the system using this method is also presented. It also makes a comparison of the frequency and time response if any of the other controllers is selected for each plant. Furthermore, it provides an insight of what happens at each plant transition and studies the possibility that more than one controller may produce an acceptable performance. Additionally, it studies how the controlled output is affected by disturbances. A uniformly distributed random signal was introduced at the plant input and was progressively increased. For low values of disturbances between $\pm 1 \times 10^{-6}$ to $\pm 1 \times 10^{-6}$ no changes were detected in the proper selection of controllers. However, when the disturbance was increased to ± 1 or higher, the optimal controller was not properly selected at one of the plant transitions. Though this was

necessary to observe a change in the switching controller scheme, it was probably not so significant since the system would be completely unstable. A similar result was also observed when a sinusoidal disturbance was introduced in the system.

Chapter 7 describes the switching controller logic used to perform the adaptation of the buck converter. A function determines the controller parameters by evaluating the robust stability condition for each of the candidate controllers. The controller selected will depend on the minimum robust stability condition associated to that candidate. The plant transition is performed at 1000, 5000, 10000 and 15000 points for plants P1, P2, P3 and P4, respectively. To avoid a large number of oscillations in the controller selection during the transition time, a hysteresis parameter is also introduced during the evaluation of the switching logic.

Chapter 8 describes the conclusion drawn from this study. It provides an explanation of the system identification for the buck converter and how the estimation error and parameter error gives an insight on how fast the system is converging to the true parameters. Additionally, it outlines the three different types of controller used to compensate the DC-DC converter and why one controller is better than the other two. However, it also highlights the drawbacks of this controller that does not allow the immediate implementation on the system. It also summarizes the results from the adaptation using an indirect scheme and the robust stability condition. Furthermore, it shows the outcomes when the system is under disturbances.

Finally, chapter 9 summarizes the future work for this study. It makes reference to the achievement obtained so far, but it also provides some recommendations that can be performed to successfully complete this study. Some of them involve the use of a discrete controller to implement the frequency loop shaping technique or perform an optimization problem to minimize the compensated-open loop system subject to

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constraints given by resistor and capacitor values. Additionally, one more variability test in the adaptation of the system is of interest. That is the nonlinear nature of the voltage which is usually present in the capacitors. Furthermore, all the simulation results will need to be verified on a physical system.

Chapter 2

BUCK CONVERTER DESIGN

Considering that a buck converter is working with an invariant switching frequency, pulse width modulation (PWM) and its operation is in continuous-current mode (CCM), the converter design relies on four important parameters for the selection of the inductor (L), output capacitor (C_{out}) and the transistor. These parameters are described as follows:

- Input voltage range: It determines the maximum and minimum value that will be introduced to the buck converter. The voltage range for our design is between 5 and 8.125 volts. This parameter will be assigned as V_{in}.

- Regulated output voltage: According to the way of operation of the buck converter, the objective is to step down the input voltage to a lower level that seems to be constant over time. Although the voltage output will be oscillating, as long as the ripple voltage is kept inside the specified bounds, the design will be acceptable. The output voltage for our design is 3.3 volts with a regulation of ±2% the output voltage. This parameter will be assigned as V_{out}.

- Maximum output current: The maximum current that the buck converter will be handling plays an important role since in the transient response the output current may increase until the system stabilizes. A maximum output current of 0.125 A was selected to design the buck converter. This parameter will be assigned as I_{outmax}.

- Converter's switching frequency: Choosing the optimal switching frequency may affect the overall operation of the buck converter. It is important to know the

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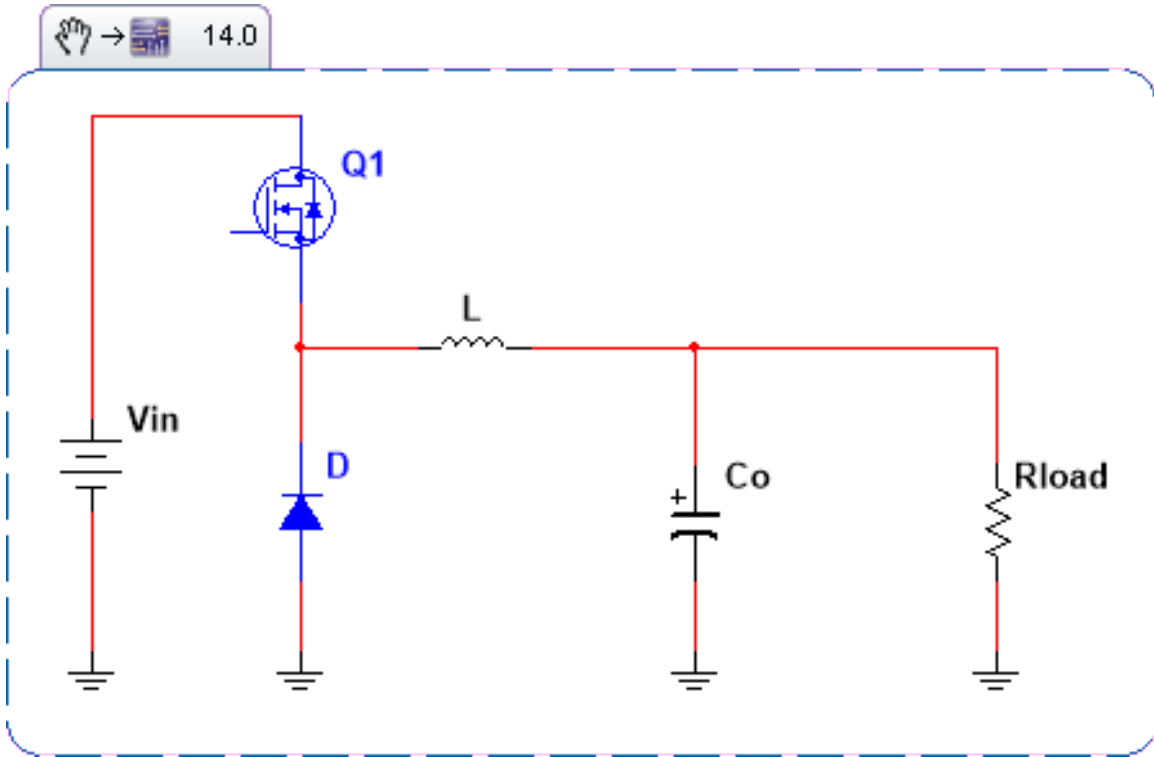
Figure 1. Simple buck converter structure

application that will be given to the converter, so that cost can be minimized and the requirements can be satisfied. A switching frequency of $5kHz$ was chosen for our design. This parameter will be assigned as f_{sw}.

After these parameters have been specified, one can proceed to calculate the values for inductance and capacitance of the simple buck converter structure shown in Fig. 1.

2.1 Inductor Selection

To properly select the inductor for the given specifications, we need to solve for the value of L from eq. 2.1.

$$\triangle I_{inductor} = LIR * I_{outmax} = (V_{inmax} - V_{out}) * \frac{V_{out}}{V_{inmax}} * \frac{1}{f_{sw}} * \frac{1}{L} \qquad (2.1)$$

Where LIR is the inductor current ratio. This value is usually given as a percentage of the output current (I_{out}). For example, if we have a ripple current of $300mA$ peak to peak and a output current of $1A$, LIR would be calculated as in eq. 2.2.

$$LIR = \frac{I_{ripple}}{I_{out}} = \frac{0.3}{1} = 0.3 \qquad (2.2)$$

A value of 0.3 for LIR is usually acceptable since it provides a good trade-off between how efficient the system is and the load-transit response. Having a lower LIR value usually means that the ripple current is minimized, but the load-transit response becomes slower. In similar fashion, when the LIR constant increases, the load-transit response is faster; however, the ripple current increases at the inductor.

Therefore, after using the parameters design in eq. 2.1, the inductor L can be obtained from eq. 2.3.

$$L = \frac{(V_{inmax} - V_{out}) * \frac{V_{out}}{V_{inmax}} * \frac{1}{f_{sw}}}{LIR * I_{outmax}} \qquad (2.3)$$

$$= \frac{(8.125 - 3.3) * \frac{3.3}{8.125} * \frac{1}{5 \times 10^6}}{0.3 * 0.125} \qquad (2.4)$$

$$= 10.45 \times 10^{-6} H \qquad (2.5)$$

However, since this value is not commercially available, either an inductor with a value of $9\mu H$ or $10\mu H$ will be acceptable.

Additionally, we would like to determine the current peak that the inductor can handle. This is obtained by solving eq. 2.6.

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$$I_{peak} = I_{outmax} + \frac{\triangle I_{inductor}}{2} \tag{2.6}$$

$$= 0.125 + \frac{0.3 * 0.125}{2} \tag{2.7}$$

$$= 0.14375A \tag{2.8}$$

Therefore, a saturation current should be higher than $0.14375A$. An acceptable margin would be 20% above the calculated value. Additionally, a DC resistance range (DCR) for the characteristics calculated above is usually between 5 and 8 $m\Omega$. Consequently, it is recommended to choose the lowest DCR for the inductor commercially available.

2.2   Output Capacitor Selection

The main purpose of the capacitor is to minimize the voltage overshoot as well as the ripples at the output. Having an insufficient output capacitance means that the system will have a large overshoot. Similarly, having an insufficient capacitance and a high equivalent-series resistance (ESR) in the output capacitor causes the system to have high ripples. Therefore, since parameters such as the maximum voltage overshoot and ripples are given in the design specifications, the output capacitor should be selected such that it has enough capacitance and a low ESR.

Hence, to properly select the output capacitor, we need to solve eq. 2.9.

$$C_{out} = \frac{L(I_{outmax} + \frac{\triangle I_{inductor}}{2})^2}{(\triangle V + V_{out})^2 - V_{out}^2} \tag{2.9}$$

Where C_{out} is the output capacitance, L corresponds to the inductor calculated in section 2.1, $\triangle V$ is the maximum output-voltage overshoot, I_{outmax} is the maximum

current at the output, V_{out} is the output voltage and $\triangle I_{inductor}$ is the maximum current overshoot in the inductor.

Once all the design parameters are replaced in eq. 2.9 and setting a maximum output-voltage overshoot at $100mV$, we obtain the output capacitance for the buck converter in eq. 2.10 as follows:

$$C_{out} = \frac{10 \times 10^{-6}(0.125 + \frac{0.3*0.125}{2})^2}{(100 \times 10^{-3} + 3.3)^2 - 3.3} \tag{2.10}$$

$$= 0.308\mu F \tag{2.11}$$

However, it is a good practice to select a capacitor whose capacitance is 20% above the calculated value obtained in eq. 2.10. This can bee seen in eq. 2.12.

$$C_{out\,selected} = C_{out} + C_{out} * 0.20 \tag{2.12}$$

$$= 0.308 + 0.308 * 0.20 \tag{2.13}$$

$$= 0.3696\mu F \tag{2.14}$$

Nevertheless, since this value is not commercially available, we could choose a capacitor with $0.47\mu F$ capacitance.

Additionally, the equivalent-series resistance (ESR) should be determined to guarantee that the voltage ripple is low. The ESR can be obtained by solving eq. 2.15.

$$ESR_{Cout} = \frac{1}{\triangle I_{inductor}} * \left(V_{outripple} - \frac{1}{2C_{out}} * \frac{V_{inmax} - V_{out}}{L} \left(\frac{V_{out}}{V_{inmax}} * \frac{1}{f_{sw}} \right)^2 \right) \tag{2.15}$$

$$= \frac{1}{0.3 * 0.125} * \left(66 \times 10^{-3} - \frac{1}{2 * 0.47 \times 10^{-6}} * \frac{8.125 - 3.3}{10 \times 10^{-6}} \left(\frac{3.3}{8.125} * \frac{1}{5 \times 10^6} \right)^2 \right) \tag{2.16}$$

$$= 1.67\Omega \tag{2.17}$$

Where the output-voltage ripple has been calculated by having a 2% of regulation in eq. 2.18.

$$V_{outripple} = 3.3 * 0.02 \tag{2.18}$$

$$= 66mV \tag{2.19}$$

Therefore, a capacitor should be chosen so that the ESR is lower than 1.67Ω or a similar value depending on what it is commercially available.

2.3 Diode Selection

The limiting factor to select a diode is the dissipated power. The worst-case scenario for power dissipation in a diode can be calculated in eq. 2.20.

$$P_{DIODE} = \left(1 - \frac{V_{out}}{V_{inmax}}\right) * I_{outmax} * V_D \tag{2.20}$$

$$= \left(1 - \frac{3.3}{8.125}\right) * 0.125 * 0.7 \tag{2.21}$$

$$= 0.05196W \tag{2.22}$$

Where V_D is the forward voltage drop across a silicon diode while the rest of the parameters have been declared as specification design. Therefore, the selected diode should be capable of dissipating at least $0.05196W$ of power. Additionally, for reliable operations, we must ensure that the peak repetitive reverse voltage (V_{RRM}) is greater than the maximum input voltage (V_{inmax}). At the same time, the average forward output current (I_{FAV}) should be greater than the maximum output current (I_{outmax}). For our design specifications, we could then select one of the following diode options: 1N4001, 1N4002, 1N4003, 1N4004, 1N4005, 1N4006, 1N4007.

2.4 MOSFET Selection

For the MOSFET selection, there are certain parameters that should be known such as the maximum junction temperature (T_{JMAX}) and the maximum ambient temperature (T_{AMAX}). The following calculations are based on the NTE2382 N-MOSFET. T_{JMAX} is $150°C$ while T_{AMAX} was set up with a value of $60°C$ due to chassis packaging where this temperature may be common. This allows us to determine the maximum allowable temperature rise in eq. 2.23.

$$T_{JRISE} = T_{JMAX} - T_{AMAX} \tag{2.23}$$

$$= 150 - 60 \tag{2.24}$$

$$= 90°C \tag{2.25}$$

T_{JMAX} allows us to determine the maximum power dissipated in the MOSFET. This dissipation is caused by on-resistance and switching losses. The total dissipated power can be then calculated in eq. 2.26.

$$P_{D_{TOT}} = \frac{T_{J_{RISE}}}{\Theta_{JA}} \tag{2.26}$$

$$= \frac{90°C}{62.5°C/W} \tag{2.27}$$

$$= 1.44W \tag{2.28}$$

Where Θ_{JA} is the MOSFET junction to ambient thermal resistance. Θ_{JA} is affected by the MOSFET package and the amount of PC-board copper to the MOSFET package. Also, the total dissipated power calculated in eq. 2.26 will be used to determine the on-resistance loss.

The on-resistance loss can be described in eq. 2.29.

$$P_{D_{R_{DS}}} = \frac{V_{out}}{V_{in_{min}}} * I_{out_{max}}^2 * R_{DS_{(on)HOT}} \qquad (2.29)$$

Where $R_{DS_{(on)HOT}}$ is the static drain to source on-resistance. However, $R_{DS_{(on)}}$ is only provided in the data-sheet when $T_J = 25°C$. Therefore, $R_{DS_{(on)HOT}}$ needs to be calculated at $T_{J_{HOT}}$. As a rule of thumb, one may consider $0.5\%/°C$ of temperature coefficient at any temperature. Therefore, $R_{DS_{(on)HOT}}$ can be calculated in eq. 2.30.

$$R_{DS_{(on)HOT}} = [1 + 0.005\left(T_{J_{HOT}} - 25°C\right)] * R_{DS_{(on)25°C}} \qquad (2.30)$$

Where $T_{J_{HOT}}$ is the hot junction temperature and needs to be estimated. Assuming that the on-resistance losses only represents a 60% of the MOSFET's losses, then $R_{DS_{(on)25°C}}$ can be calculated in eq. 2.31.

$$R_{DS_{(on)25°C}} = \frac{V_{in_{max}}}{V_{out}} * \frac{1}{I_{out_{max}}\left[1 + 0.005 * (T_{J_{HOT}} - 25°C)\right]} * P_{DTOT} * 0.6 \qquad (2.31)$$

$$= \frac{5}{3.3} * \frac{1}{0.125^2\left[1 + 0.005 * (150 - 25)\right]} * 1.44 * 0.6 \qquad (2.32)$$

$$= 51.56\Omega \qquad (2.33)$$

Therefore, $R_{DS_{(on)HOT}}$ can be calculated in eq. 2.34

$$R_{DS_{(on)HOT}} = [1 + 0.005\left(T_{J_{HOT}} - 25°C\right)] * R_{DS_{(on)25°C}} \qquad (2.34)$$

$$= [1 + 0.005\left(150 - 25\right)] * 51.56 \qquad (2.35)$$

$$= 83.78\Omega \quad \text{at} \quad 150°C \qquad (2.36)$$

And the dissipated power due to the on-resistance loss is given in eq. 2.37.

$$P_{D_{R_{DS}}} = \frac{V_{out}}{V_{in_{min}}} * I_{out_{max}}^2 * R_{DS_{(on)HOT}} \tag{2.37}$$

$$= \frac{3.3}{5} * 0.125^2 * 83.78 \qquad\qquad = 0.864W \tag{2.38}$$

Finally, it is important also to consider the losses due to switching frequency. Although they only represent a small fraction of the total dissipated power in a MOSFET, they should be taken into account. The switching losses in eq. 2.39 only provide a rough estimate and it is always recommended to verify these parameters with a lab test.

$$P_{D_{SW}} = \frac{C_{RSS} * V_{in_{max}}^2 * f_{sw} * I_{out_{max}}}{I_{gate}} \tag{2.39}$$

$$= \frac{40 \times 10^{-12} * 8.125^2 * 5 \times 10^6 * 0.125}{1.5} \tag{2.40}$$

$$= 0.0011W \tag{2.41}$$

Therefore, the resulting dissipating power due to the on-resistance and the switching losses are given in eq. 2.42.

$$P_{DTOTAL} = P_{DRDS} + P_{DSW} \tag{2.42}$$

$$= 0.864 + 0.0011 \tag{2.43}$$

$$= 0.8651W \tag{2.44}$$

And for a $P_{DTOTAL} = 0.8651W$, $T_{JRISE} = 0.8651/62.5 = 54°C$, which is between the temperature range of the specified MOSFET.

Chapter 3

PLANT MODELING

Modeling a plant requires a procedure that can be broken down as follows:

- First-principles model: First-principles allows us to obtain a preliminary mathe-
  matical description of the structure of the system. Having this approximation
  lets us determine the required excitation to accurately identify the system.

- System excitation: After obtaining the first-principle model, the input signal can
  be designed so that the interested frequencies are properly identified. Thus, we
  may be interested in identifying about one decade of the expected gain crossover
  frequency.

- Parameter estimation: Although there are several methods available for para-
  metric system identification, we have used a least-square parameter estimation.

- Uncertainty estimation: The uncertainty estimation provides a measure of how
  acceptable the system will be and how suitable the model is for controller design
  purposes. This information is relevant from the point of view of robust control,
  so that we can determine if a model unfalsifies the identified plant [19].

Having said that, we can start describing the buck converter in eq. 3.1:

$$Tu(s) = \frac{H}{Vm(s)}P(s) \tag{3.1}$$

$$P(s) = P_o \frac{\frac{2\pi f_o^2}{f_{esr}} + (2\pi f_o)^2}{s^2 + \frac{2\pi f_o}{Q}s + (2\pi f_o)^2} \tag{3.2}$$

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{3.3}$$

$$H = \frac{V_{ref}}{V_{reflow}} \tag{3.4}$$

Here H is known as the feedback factor, P_o stands for the minimum gain that can be used or the average between minimum and maximum input value, Q is the quality factor and V_m is the Pulse Width Modulation (PWM) gain. The values of inductor and capacitor correspond to the TI 62675 power converter.

3.1 Open-Loop Plant

Once all the parameters have been specified in eq. 3.1, the open loop plant is given by eq. 3.5.

$$Tu(s) = \frac{9820s + 1.403 \times 10^{11}}{s^2 + 1.419 \times 10^5 s + 2.778 \times 10^{11}} \tag{3.5}$$

The Bode plot of the open-loop plant is shown in Fig. 2. The plant depicts a resonance peak at a value which is below of $6.22 \times 10^5 rad/s$.

However, to be able to work better during the system identification and controller design steps, we scaled the plant down by a factor of 10^6. Then, we defined a new variable called $s' = s/10^6$. The resulting transfer function for the buck converter is given by eq 3.6:

$$Tu(s') = \frac{0.00982s' + 0.1403}{s'^2 + 0.1419s' + 0.2778} \tag{3.6}$$
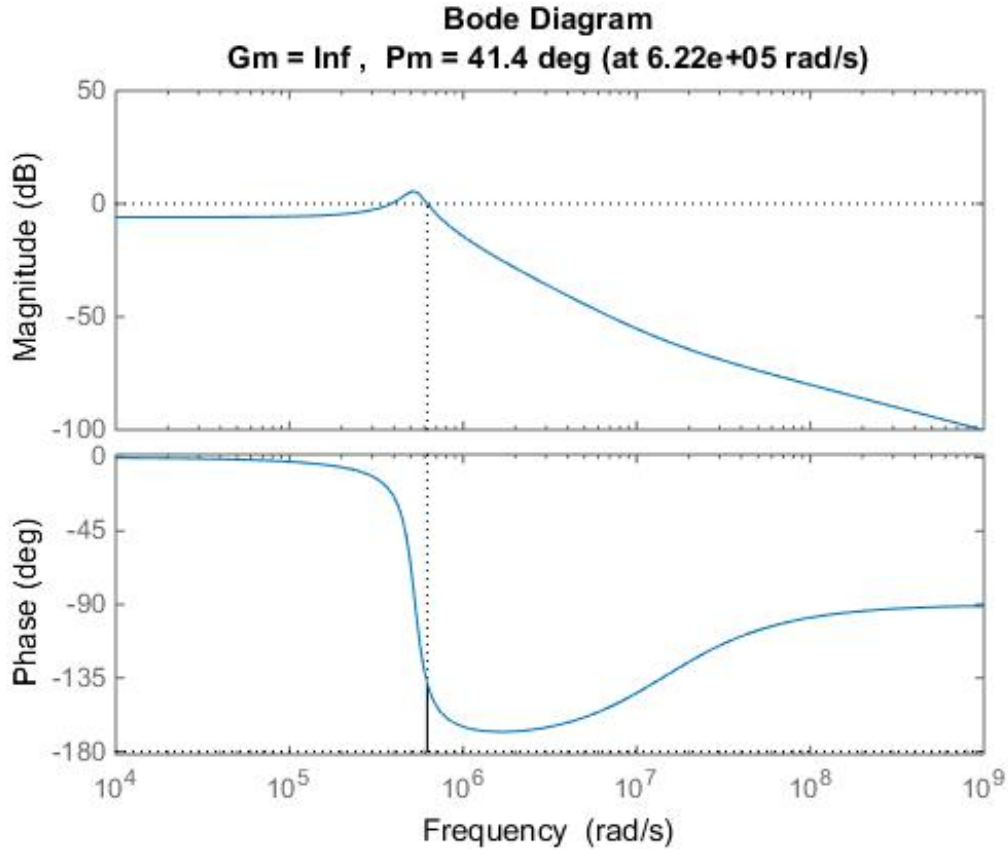
Figure 2. Uncompensated Plant

A Bode plot was generated for the scaled plant. Fig. 3 shows the frequency response of the scaled plant. The response looks very similar to Fig. 2 where the only difference lies on the frequency values. Therefore, the Bode plot of the scaled plant now is depicted in a scale that spans in $\text{rad}/\mu s$.

A Pseudo Random Binary Sequence (PRBS) was generated to be introduced to the simulation model for system identification purposes [38]. A Fast Fourier Transform (FFT) plot was generated for the PRBS signal used in the simulation and is shown in Fig. 4. This allows us to check if the signal has enough strength in the frequencies of interest. The bandwidth of the scaled system is 0.8084 rad/s which corresponds to

Bode Diagram
Gm = Inf , Pm = 41.4 deg (at 0.622 rad/s)
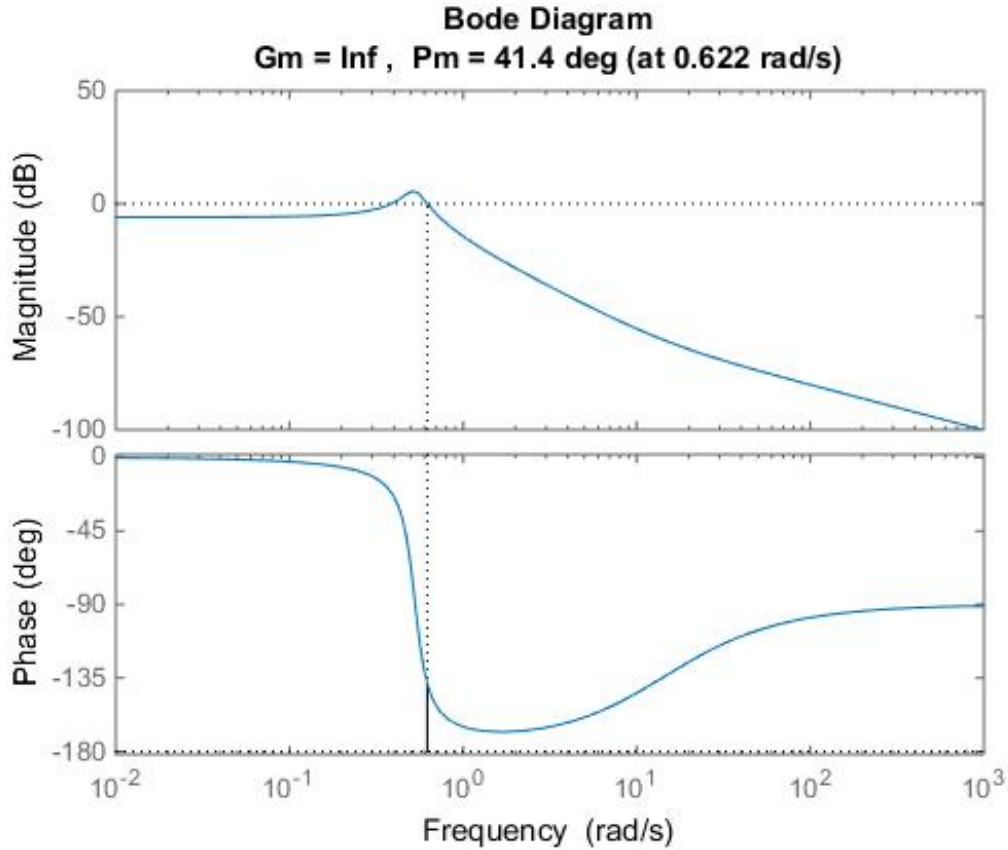
Figure 3. Uncompensated Scaled Plant

an approximately value of 0.12868 Hz. The excitation of the generated PRBS signal should have sufficient energy around the desired closed-loop bandwidth. According to [33], the signal should be large enough, so that the signal to noise ratio is good, but small enough for the system to be approximately linear around the operating point.

We performed the recursive least-square system identification of the scaled plant. The Simulink model shown in Fig. 5 executes an on-line system identification for the nominal plant of the buck converter. All the simulation parameters have also been scaled down by a factor of 10^6. Therefore, when we define a simulation time of 1, we
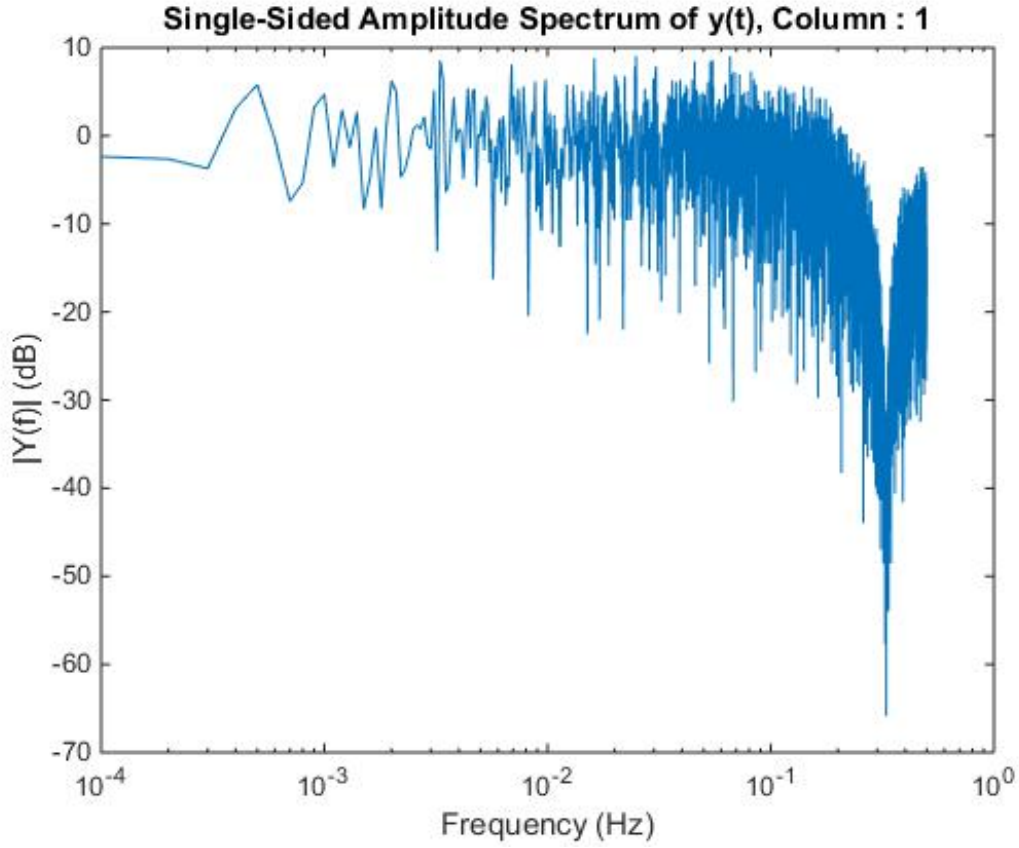
Figure 4. FFT of the PRBS signal for the Scaled Plant

mean a simulation time of 1 µs. The parameters of the system were initialized with
the values shown on table 1.

Table 1. Initial values for the on-line system identification of the buck converter

Designator	Parameter	Value
$\theta 1$	Parameter 1	$8.5 \times 10^{-}3$
$\theta 2$	Parameter 2	0.4
$\theta 3$	Parameter 3	0.5
$\theta 4$	Parameter 4	0.5

After running the Simulation, we can observe that the parameters shown in the
display corresponds exactly to the parameters given in the scaled plant. The estimation
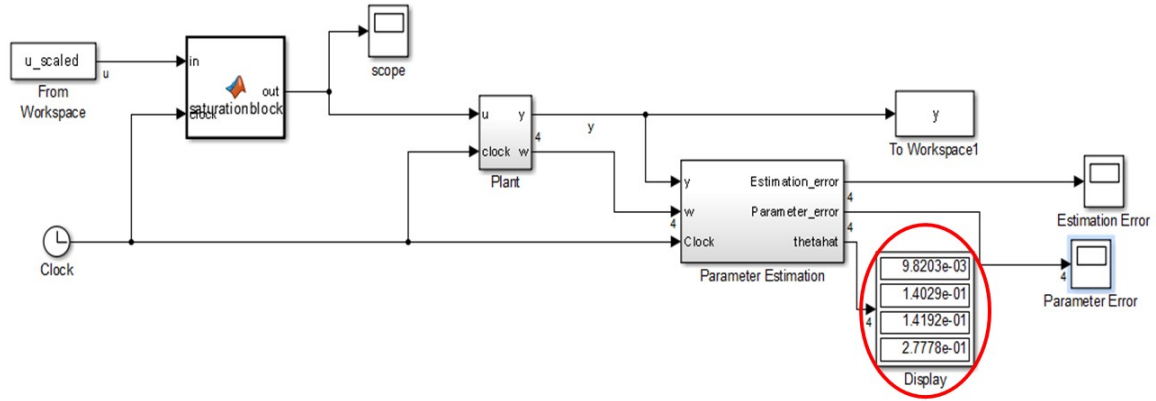
Figure 5. Simulink Block of the Online System Identification for the Buck Converter

error and parameter error are shown in figures 6 and 7, respectively. The clock has been introduced for a future work to study the effects of a bursting scenario. However, it has not been used yet. The estimation error is calculated in eq. 3.7 while the parameter error is computed by eq. 3.8

$$Estimation \quad error = \hat{y} - y \tag{3.7}$$

$$Parameter \quad error = \theta_* - \hat{\theta} \tag{3.8}$$

Here $\hat{y}$ stands for the estimated output, y is the true output, θ_* is the true parameter and $\hat{\theta}$ is the estimated parameter.

After observing the estimation error plot, we can point out that the estimated values of the plants are converging since the error is decreasing. After allowing the simulation run for about 10000 μs, the estimated error is below 0.1. A similar behavior happens

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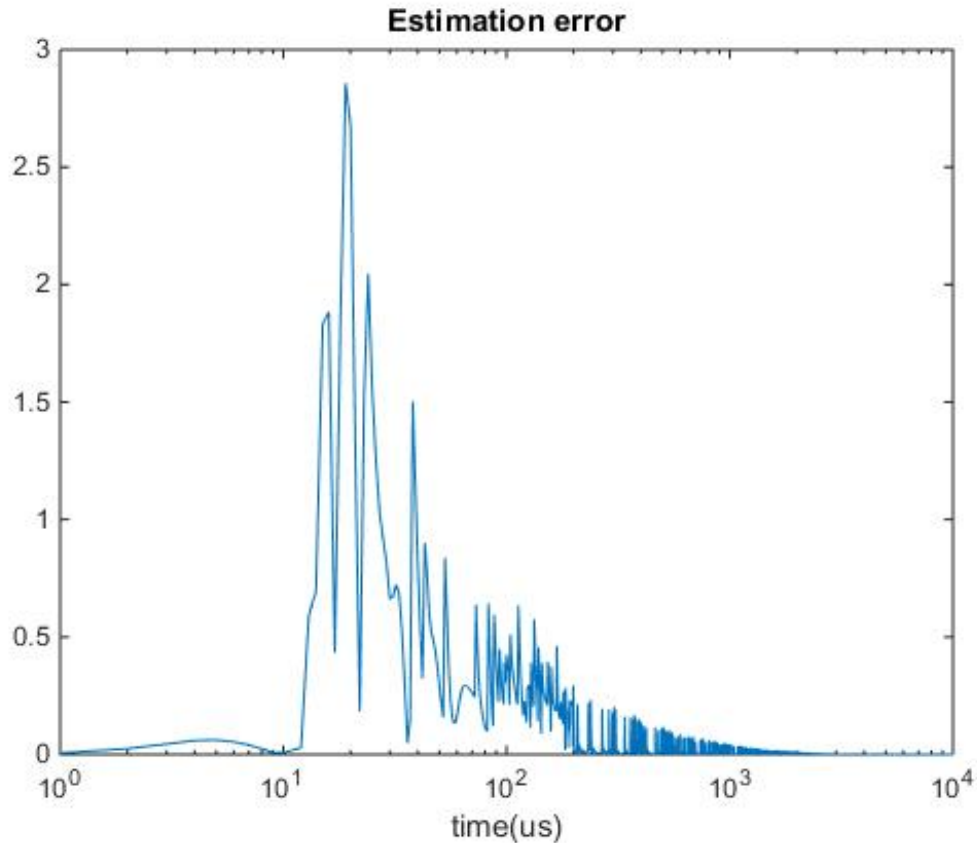
Figure 6. Estimation Error

when the parameter error is analyzed. Each parameter was initialized at a value which was different from the true value. But when the on-line system identification was performed, the parameters converged in 100 μs approximately. These two metrics allow us to determine that the system was converging to the true parameters.

For simulation purposes, we have scaled the plant down to perform the system identification of the buck converter. However, in a physical system, the rate of convergence will be determined by the hardware used to run the experiment and how fast we are capable of collect data from the buck converter. These characteristics will be addressed in section 3.2.

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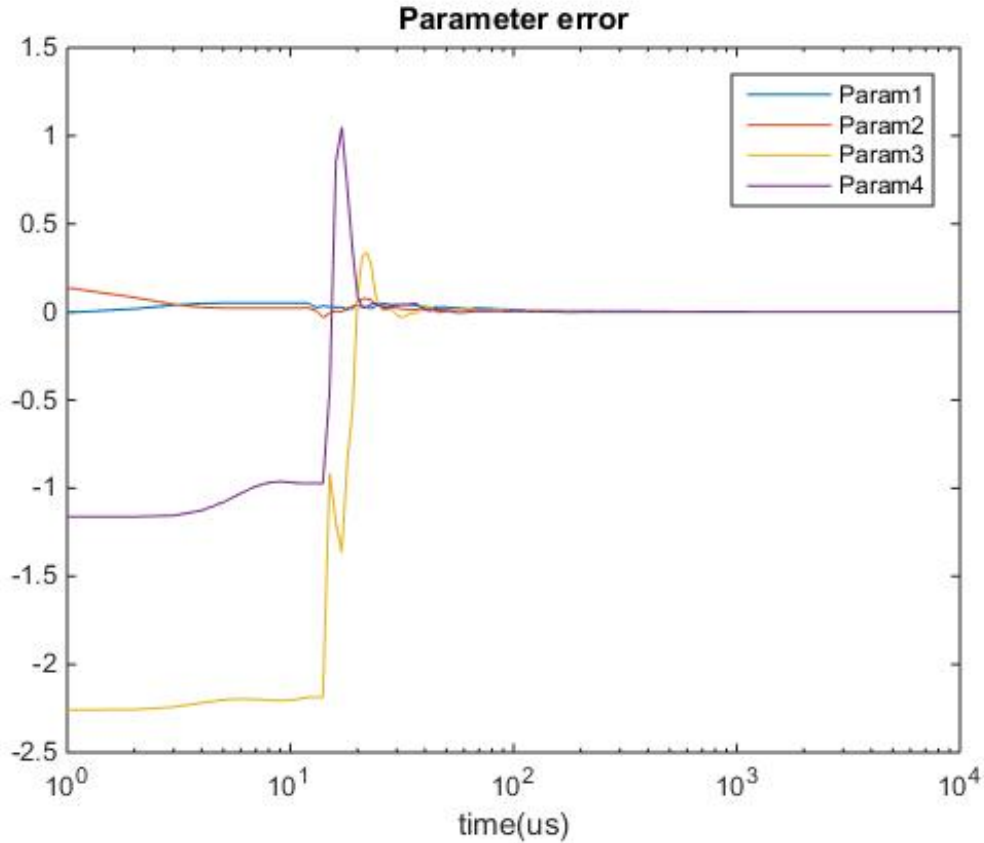
Figure 7. Parameter Error

3.2   Experimental Data

An evaluation board helps us identify the buck converter in closed loop form considering that we know the controller that is implemented in the loop. Fig. 8 illustrate a picture of the evaluation board. It comes with a LM27402 buck converter that incorporates an input feed-forward voltage which is capable of maintaining stability for the entire input voltage range. Its frequency can be varied in a range that goes from 200 kHz to 2 MHz.

The evaluation board allows us to collect data for system identification purposes by introducing a PRBS signal to the reference node and reading the output of the system.

However, since this is a closed-loop system, the open loop plant will be obtained by eq. 3.9.

$$P = -\frac{G_{CL}}{G_{CL}CH - C} \qquad (3.9)$$

Here G_{CL} corresponds to the identified closed-loop plant, C is the controller, and H is the feedback factor. Fig. 9 shows the schematic of the control loop plant where the compensator is known as a type 3 controller.

Fig. 10 shows the frequency response of the identified plant using the evaluation board for a capacitance value of $270\mu F$ and a sampling time of $1/(fs_{experimental}/6)$ where $fs_{experimental} = 300 \times 10^3 Hz$. After $fs_{experimental}/6$ the system cannot be characterized. This allows us to observe that the frequency response of the buck converter will change depending on the value of capacitor and inductor that the system has at a specific time which will vary as a result of deterioration and failure of these components.
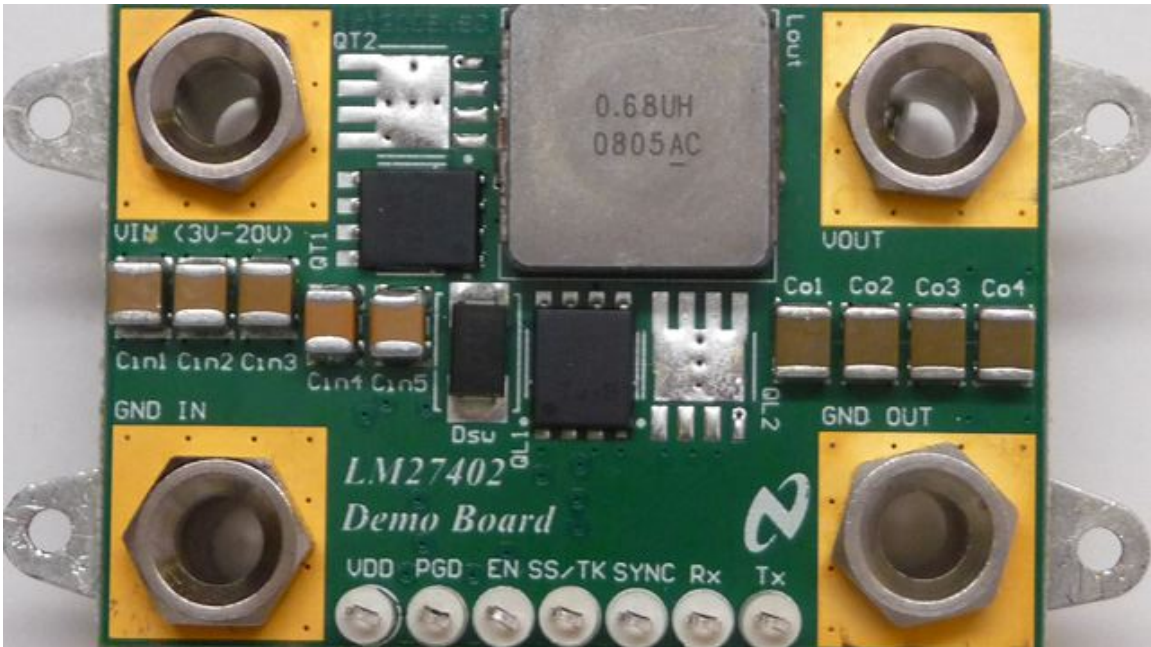
Figure 8. Evaluation Board
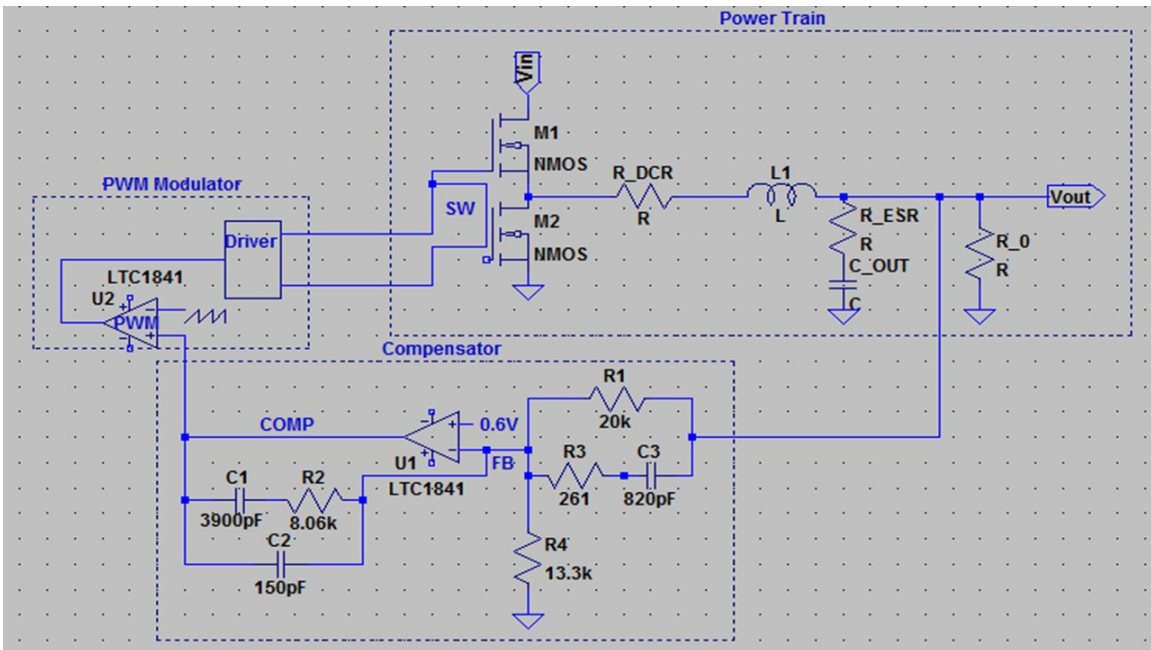
Figure 9. Control Loop of the Buck Converter
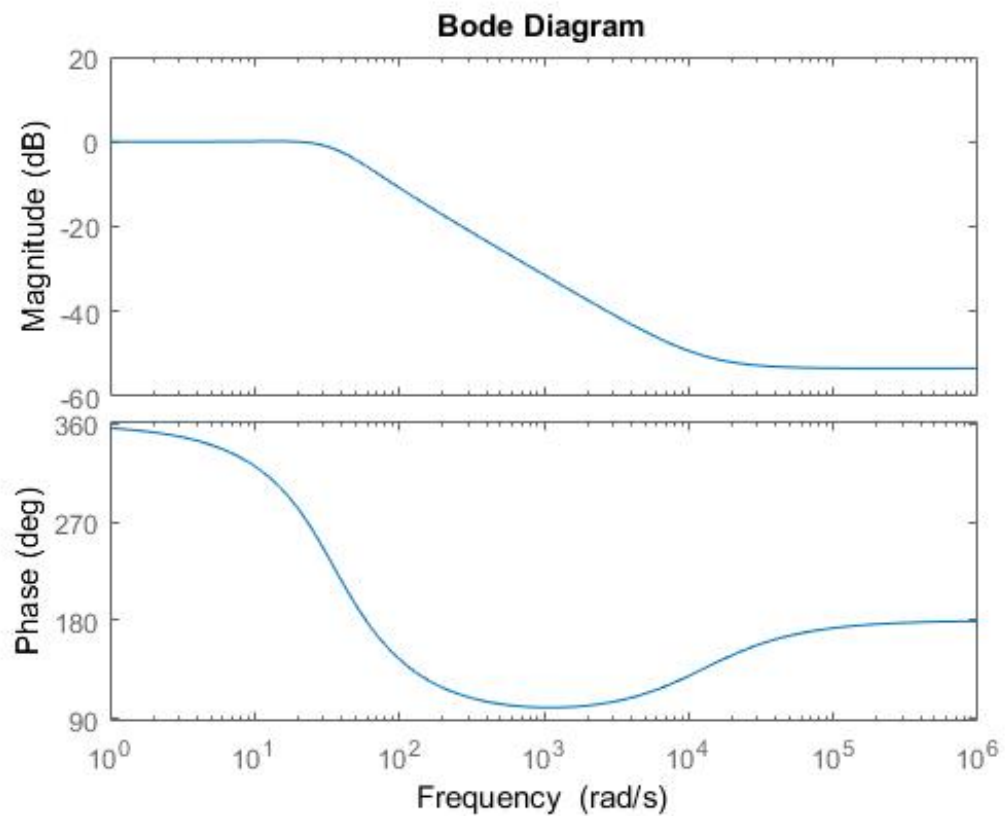
Figure 10. Frequency Response of the Identified Plant

Chapter 4

CONTROLLER DESIGN

Despite the advances in controller design, Proportional-Integral-Derivative (PID) controllers are still the most common type of controllers used in many applications. With an extensive literature available on tuning and properties of PID controllers [1], [2], [26], [12], they offer integral action to eliminate set-point errors and disturbance offsets, phase lead to adjust crossover properties like phase-margin –and, hence, closed-loop damping. At the same time, their simplicity allows for relatively straightforward implementation including discretization [15], [6], and ad-hoc, but very important, modifications for anti-windup, parameter scheduling. Additionally, a lot of studies have been conducted to consider quantization levels for discrete controllers [10], [13], [14], [8].

4.1 Type 3 Controller

The type 3 controller is shown in Fig. 11 and has been chosen to compensate the buck converter [27]. The main reason to select this controller was its nice frequency response since it can boost the phase up to 180 degrees. This characteristic might be needed to control the physical system.

The type 3 controller is a comparator which transfer function corresponds to a system that has two zeros, three poles as given in eq. 4.1.

$$G(s) = \frac{Vout(s)}{V_1(s)} = -\frac{sR_2C_1 + 1}{sR_1(C_1 + C_2)(1 + sR_2\frac{C_1C_2}{C_1+C_2})} \cdot \frac{sC_3(R_1 + R_3) + 1}{sR_3C_3 + 1} \qquad (4.1)$$
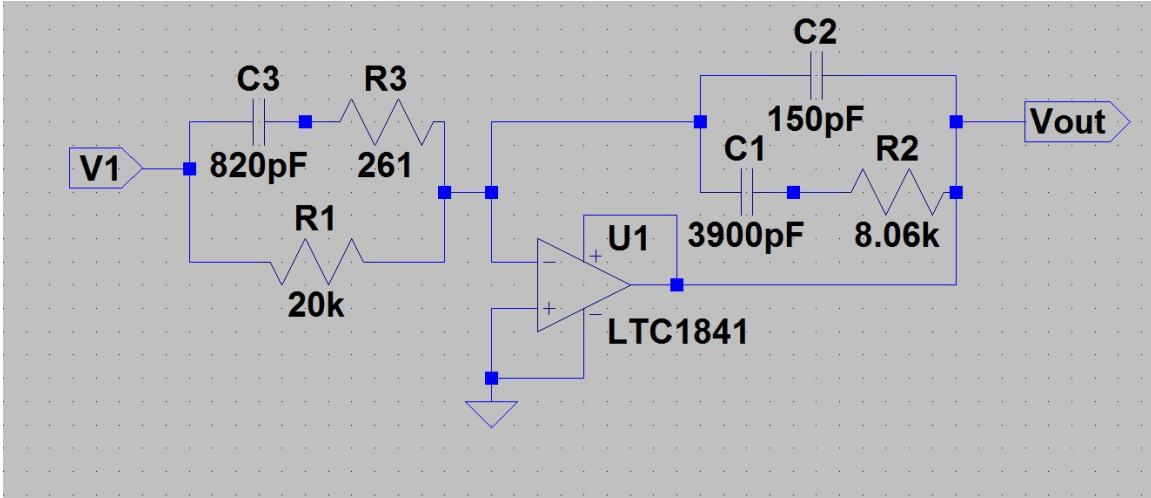
Figure 11. Type 3 Controller

An evaluation board has been used to run a system identification of the buck converter. The values for resistors and capacitors corresponding to the type 3 controller used in this evaluation board are given in table 2.

Table 2. Resistor and Capacitor Values for the Type 3 Controller Used in the Evaluation Board

Designator	Component	Value
R1	Resistor	20 kΩ
R2	Resistor	8.06 kΩ
R3	Resistor	261 Ω
C1	Capacitor	3900 pF
C2	Capacitor	150 pF
C3	Capacitor	820 pF

Source: High Performance Synchronous Buck Controller with DCR Current Sensing Data Sheet.

4.2 PID Controller Based on Phase and Gain Margin Specifications

A PID controller has been designed using classical control together with a low-pass filter. The low-pass filter was designed to be at five times the bandwidth (BW) value to attenuate the resonance peak, so that the closed-loop magnitude response does not exceed the unity. Since the plant has been scaled down by a factor of 10^6, the initial closed-loop desired bandwidth has been also scaled down. Therefore, the new desired BW is given by $BW = 2fc$ where $fc = 190 \times 10^3/10^6$. The phase margin was selected to be equal to 60°. The structure for the PID controller has been chosen so that both zeros are place at the same location. The resulting controller is given in eq. 4.2.

$$C_{PID}(s) = \frac{6.754 \times 10^{-12}s^2 + 3.584 \times 10^{-6}s + 0.4754}{1.675 \times 10^{-20}s^3 + 2.675 \times 10^{-13}s^2 + 1 \times 10^{-6}s} \tag{4.2}$$

The values of resistors and capacitors for the type 3 controller when a PID controller was designed using phase and gain margin specifications are detailed in tables 3 and 4.

Table 3. Resistor and Capacitor Values for the Type 3 Controller based on the PID controller design-Option 1

Designator	Component	Value
R1	Resistor	54.33 kΩ
R2	Resistor	100 kΩ
R3	Resistor	2.53 kΩ
C1	Capacitor	37.69 pF
C2	Capacitor	1.03 pF
C3	Capacitor	66.30 pF

Table 4. Resistor and Capacitor Values for the Type 3 Controller based on the PID controller design-Option 2

Designator	Component	Value
R1	Resistor	53.33 kΩ
R2	Resistor	100 kΩ
R3	Resistor	1.45 kΩ
C1	Capacitor	37.69 pF
C2	Capacitor	1.75 pF
C3	Capacitor	68.81 pF

4.3   Pole-Zero Cancellation Controller

Pole-Zero Cancellation [3], [7] is a method to obtain the gains of a PID controller which is based on pole-placement for systems with known parameters. This method together with a least-square algorithm can be very useful in systems with unknown parameters which varying slowly in time. The controller obtained using the pole-zero cancellation technique is give in eq. 4.3.

$$C_{PZ}(s) = \frac{1.093 \times 10^9 s^2 + 7.653 \times 10^{14} s + 1.34 \times 10^{20}}{s^3 + 2.622 \times 10^7 s^2 + 1.705 \times 10^{14} s} \tag{4.3}$$

The values of resistors and capacitors for the type 3 controller using a pole-zero cancellation technique are detailed in tables 5 and 6.

Table 5. Resistor and Capacitor Values for the Type 3 Controller based on the Pole-Zero Cancellation Technique-Option 1

Designator	Component	Value
R1	Resistor	43.78 kΩ
R2	Resistor	100 kΩ
R3	Resistor	1.31 kΩ
C1	Capacitor	28.56 pF
C2	Capacitor	717.58 fF
C3	Capacitor	63.77 pF

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Table 6. Resistor and Capacitor Values for the Type 3 Controller based on the Pole-Zero Cancellation Technique-Option 2

Designator	Component	Value
R1	Resistor	43.26 kΩ,
R2	Resistor	100 kΩ
R3	Resistor	1.31 kΩ
C1	Capacitor	28.56 pF
C2	Capacitor	862.96 fF
C3	Capacitor	64.40 pF

4.4   Frequency Loop Shaping Controller

Frequency Loop shaping [36], [11] is another type of controller that can be used to determine the gains of a proportional-integral-derivative (PID) controller. The objective of the Frequency Loop Shaping (FLS) controller is to obtain the gains of the PID controller so that the compensated open loop system is the closest possible to a specified target in an $L\infty$ sense. In other words, we try to solve the optimization problem given in eq. 4.4

$$\min_{k} \quad ||S_o(PC_k - L)||_{L\infty} \tag{4.4}$$

The controller obtained using a frequency loop shaping technique is given by eq. 4.5.

$$C_{FLS}(s) = \frac{7.697 \times 10^{-12}s^2 + 4.132 \times 10^{-6}s + 2.403}{1 \times 10^{-20}s^3 + 2 \times 10^{-13}s^2 + 1 \times 10^{-6}s} \tag{4.5}$$

Although Frequency Loop Shaping (FLS) produces the best responses compared to the other two controllers, we cannot obtain feasible values for resistors and capacitors consistent with the type 3 controller. Therefore, its implementation would need to be

addressed by either implementing a digital controller or by performing an optimization problem. The optimization should be performed so that we try to minimize the frequency response of the compensated plant using the pole-zero cancellation technique with the compensated plant using frequency loop shaping. This is subject to the constraints for all the values that each resistor and capacitor can take. In other words, we seek to solve the optimization problem given in eq. 4.6.

$$\text{minimize} \quad ||C_* P - C(R1, R2, R3, C1, C2, C3)P||$$
$$\text{subject to} \quad 50m\Omega \leq R_i(x) \leq 1M\Omega, \ i = 1, \ldots, 3. \tag{4.6}$$
$$100f\text{F} \leq C_i(x) \leq 1000\mu\text{F}, \ i = 1, \ldots, 3.$$

4.5   Results from Controller Design

Fig. 12 shows the frequency response of the compensated plant. Although the response looks very similar around the crossover frequency for all the controllers implemented in the system, the magnitude of FLS controller is bigger at lower frequencies compared to the other two controllers. Additionally, all the responses depict a little peak that is present due to the resonance characteristic of the open loop plant. Although all the designs try to attenuate this resonance peak, it cannot be eliminated completely.

The sensitivity and complementary sensitivity responses shown in Fig. 13 and Fig. 14 describe the frequency response of the compensated loop. The ideal case for the sensitivity response would seek to attenuate the gain at lower frequencies to have a good command following characteristic and disturbance attenuation at the plant output. On the other hand, the complementary sensitivity should depict a small gain
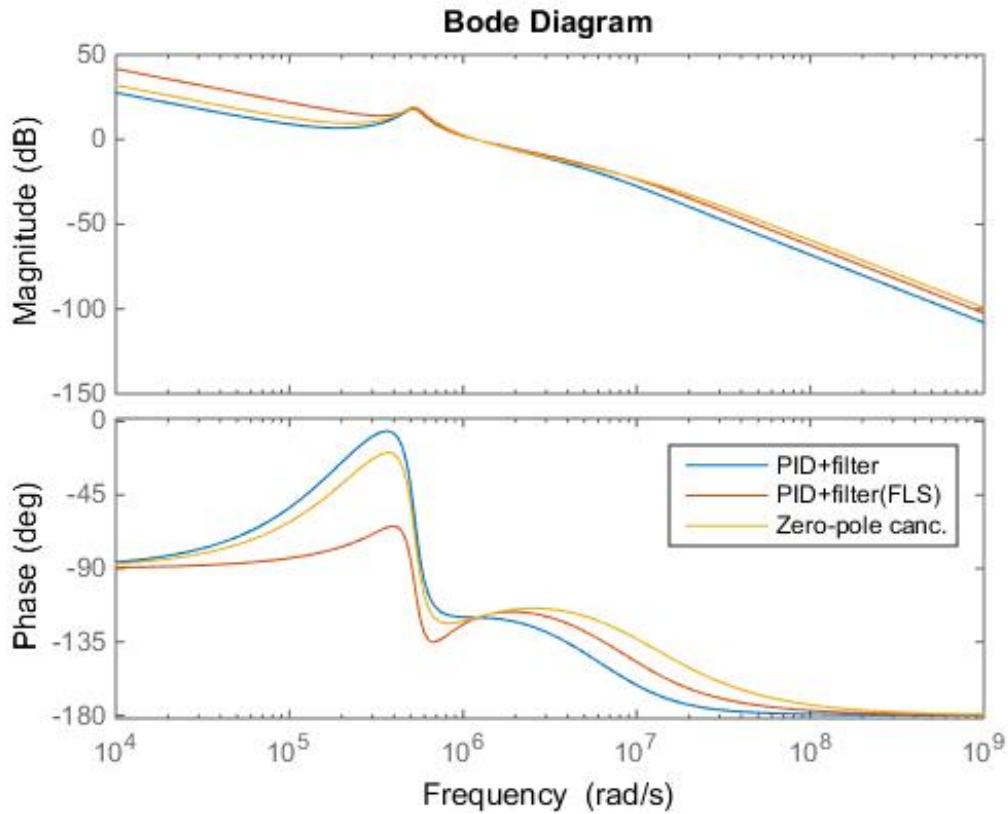
Figure 12. Compensated loop using different controllers

at higher frequencies for noise attenuation. In the ideal case, the sum of sensitivity and complementary sensitivity responses should be equal to an identity matrix.

In the sensitivity plot, all the responses corresponding to the different controllers depict a "slump" characteristic at around $50 \times 10^5 rad/sec$ which is due to the resonance peak of the open-loop plant.

On the other hand, the complementary sensitivity plot is very similar for all the controllers tested in the compensated loop.

In general, having good responses for sensitivity and complementary sensitivity allows the system to have desired stability robustness properties. However, our analysis in controller design is not limited to only observe the frequency response
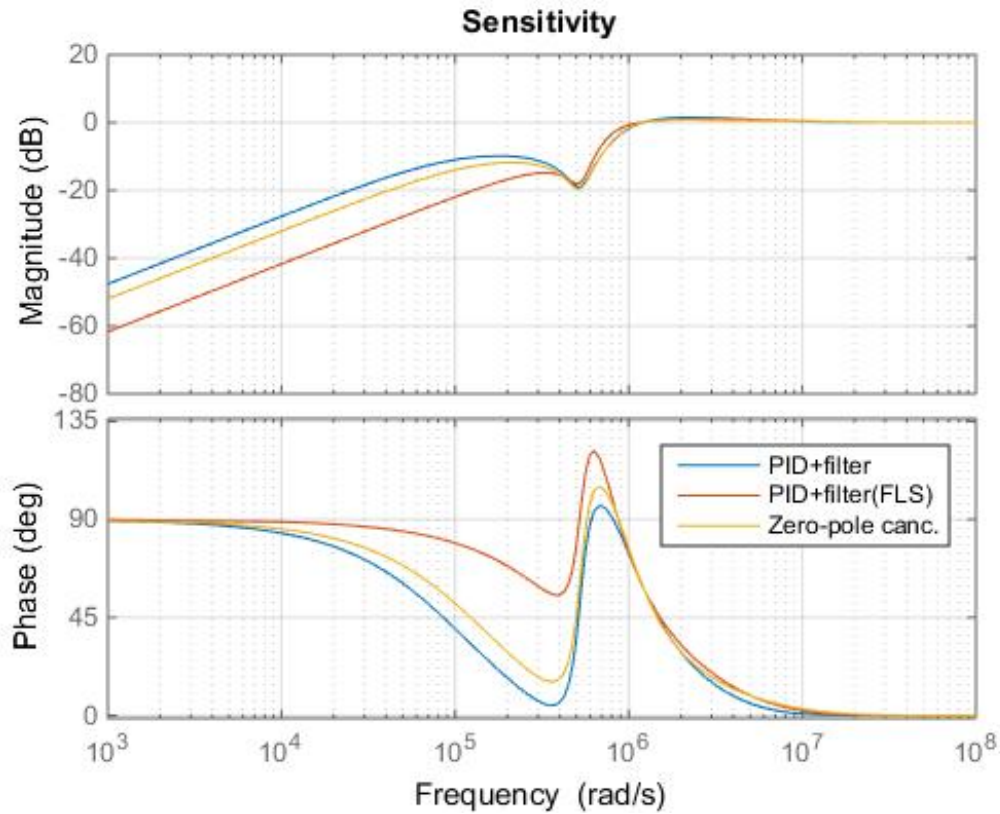
Figure 13. Comparison of Sensitivity Responses

of the compensated loop. Characteristics such as the step response and disturbance rejection allows us to determine how the system is behaving in a closed-loop scenario.

The step response in Fig. 15 shows the time that each controller is taking to stabilize the plant. It is clear that by using a PID+filter controller, the system takes more time to reach stabilization. Additionally, it does not have any overshoot but it does not reach the unit step input until around 60 μs. We can also observe that the response goes down which can make the system to oscillate between two different states prior stabilization. This might not be an ideal scenario for electronic systems
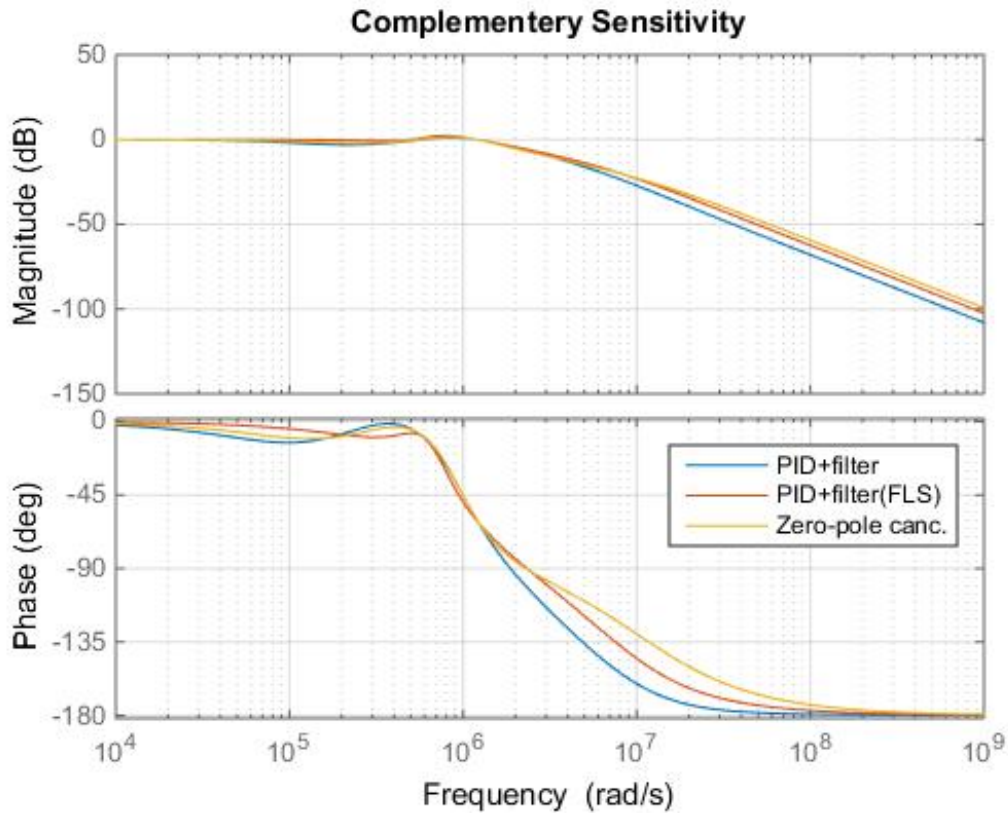
Figure 14. Comparison of Complementary Sensitivity Responses

because the DC-DC converter could be remaining at a low digital value when it is suppose to be high.

When the pole-zero cancellation controller was used, the step response was faster compared to the PID+filter technique. It also stabilizes faster with the implementation of this controller. In addition, it reaches the unit input, but then goes down below 80 percent which can probably make the system to oscillate between two different states as with the use of a PID+filter controller. It certainly provides a better response compared to the previous controller, but it can still be improved.

Finally, the frequency loop shaping technique allows the system to stabilize much faster than the other two controllers. Although there is an overshoot of about 10
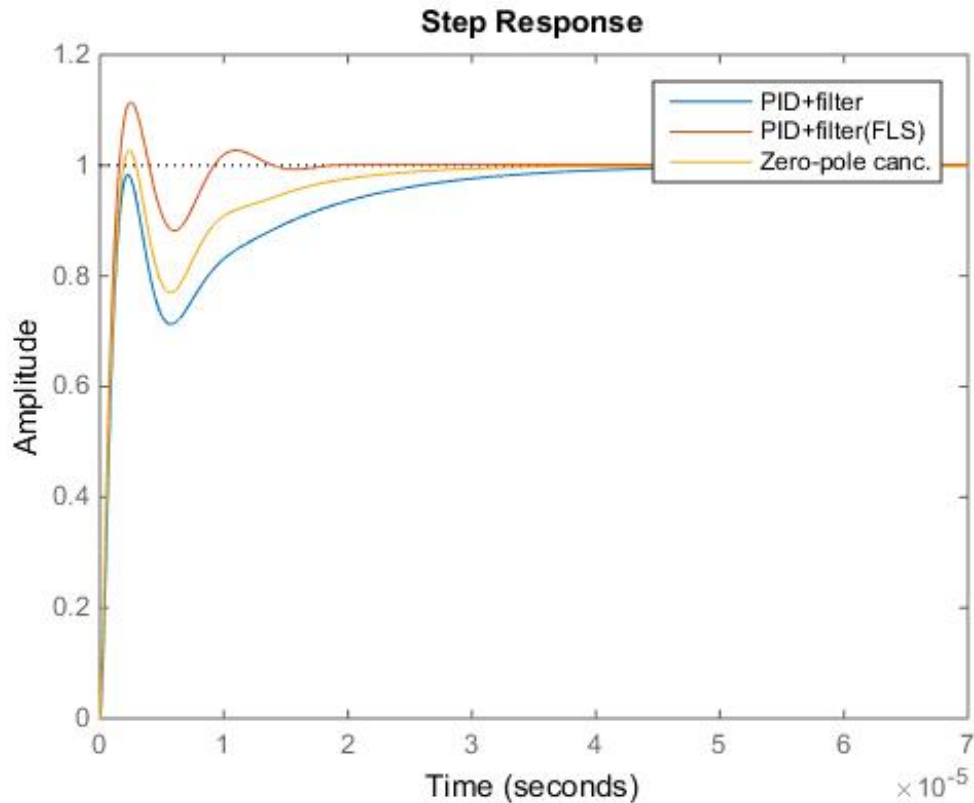
Figure 15. Comparison of Step Responses

percent, this characteristic can be improved by the implementation of a pre-filter in the compensated loop. This controller definitely depicts a better response since in the buck converter we are seeking to stabilize the system the fastest possible.

Furthermore, the disturbance rejection has been evaluated at the plant input as shown in Fig. 16. The analysis is done so that we can evaluate if our system is able to reject any disturbance at the input of the plant in the smallest time possible. Based on that fact, the FLS controller also provides a better response compared to the other two type of controllers. First, we observe that the PID+filter controller rejects the disturbances in at least $60\mu s$. The pole-zero cancellation controller rejects
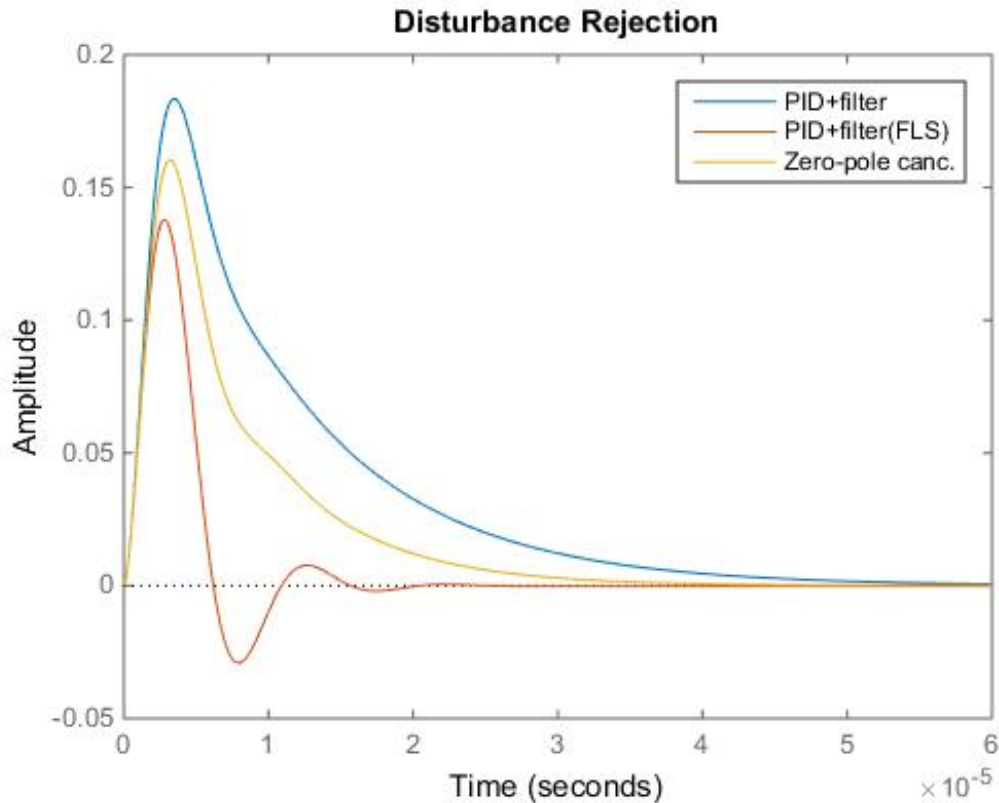
Figure 16. Comparison of Disturbance Rejection Responses

the disturbances in about $35\mu s$. However, the FLS controller is capable of rejecting

disturbances in about $20\mu s$. However, we should also point out that this controller

initially oscillates in the disturbance rejection response. The ideal scenario would be

to rejects disturbances in the smallest time possible without having big oscillations to

have nice robutsness properties.

Therefore, based on the frequency and time response analyses, the frequency loop

shaping controller provides a better scenario for the feedback control of the buck

converter. However, as it was pointed out in section 4.4, an optimization problem

should be addressed in order to obtain feasible values for resistors and capacitors consistent with the type 3 controller.

4.6   Discretization of the Controller

The PID controller in eq. 4.7 can be discretized using different methods such as Forward Euler, Backward Euler and Tustin. Each of this methods offer advantages and disadvantages in terms of phase and how close we want our discrete controller to approximate to the continuous one.

$$C(s) = Kp + \frac{Ki}{s} + \frac{Kds}{\tau s + 1} \tag{4.7}$$

Here Kp corresponds to the proportional term, Ki the integral term and Kd is the derivative term with a pseudo-pole τ of the PID controller. The pseudo-pole should be located one or two decades above bandwidth and a decade below Nyquist. According to the sampling theorem, to avoid aliasing conditions, the sampling time for the Nyquist frequency should be around 1/(2*maximum frequency). However, it is reasonable to do a practical selection of 1/(20*maximum frequency).

Based on the previous information, we calculated the bandwidth (BW) of the original plant and it is approximately 0.80849 rad/s. Therefore its corresponding Nyquist rate is given in eq. 4.8:

$$\text{Nyquist rate} = \frac{2 * BW}{2\pi} \tag{4.8}$$

$$= \frac{2 * 0.80849}{2\pi} \tag{4.9}$$

$$= 0.25735 \text{ Hz} \tag{4.10}$$

A reasonable choice for sampling time would be an order of magnitude faster as expressed in eq. 4.11:

$$\text{Reasonable sampling rate} = \frac{2 * 10 * BW}{2\pi} \tag{4.11}$$

$$= \frac{2 * 10 * 0.80849}{2\pi} \tag{4.12}$$

$$= 2.5735 \text{ Hz} \tag{4.13}$$

Therefore, the corresponding sampling time would be calculated as in eq. 4.14:

$$T_s = \frac{1}{\text{Reasonable sampling rate}} \tag{4.14}$$

$$= \frac{1}{2.5735} \tag{4.15}$$

$$= 0.3886 \text{ s} \tag{4.16}$$

By selecting a sampling time of 0.2 seconds, we would not be violating the aliasing condition. Also, the controller using phase and gain margin has been designed using this sampling time. However, the scaling for the simulation has been done such as every second corresponds to an equivalent of $1\mu s$.

Therefore, once we have selected an appropriate sampling time, we can discretize the controller using the Tustin discretization method and a value of 0.2 seconds for the sampling time (T_s). The resulting controller will contain a derivative term as described in eq. 4.17:

$$\text{Derivative Term}_{(Tustin)} = \frac{K_d s}{\tau s + 1} \tag{4.17}$$

$$= \frac{K_d \left(\frac{2}{T_s} \frac{z-1}{z+1} \right)}{\tau \left(\frac{2}{T_s} \frac{z-1}{z+1} \right) + 1} \tag{4.18}$$

$$= \frac{2K_d(z-1)}{2\tau(z-1) + T_s(z-1)} \tag{4.19}$$

$$= \frac{2K_d(z-1)}{z(2\tau + T_s) + (T_s - 2\tau)} \tag{4.20}$$

Additionally, other discretization methods could be used to obtain the derivative term of a PID controller. For a Forward Euler, $s = (z-1)/T_s$; therefore, the derivative term is given in eq. 4.21:

$$\text{Derivative Term}_{(F.Euler)} = \frac{K_d s}{\tau s + 1} \tag{4.21}$$

$$= \frac{K_d \left(\frac{z-1}{T_s} \right)}{\tau \left(\frac{z-1}{T_s} \right) + 1} \tag{4.22}$$

$$= \frac{K_d(z-1)}{\tau(z-1) + 1} \tag{4.23}$$

$$= \frac{K_d(z-1)}{\tau z + (1 - \tau)} \tag{4.24}$$

Finally, after implementing the Backward Euler method for $s = (z-1)/T_s z$, the derivative term is given in eq. 4.25:

$$\text{Derivative Term}_{(B.Euler)} = \frac{K_d s}{\tau s + 1} \tag{4.25}$$

$$= \frac{K_d\left(\frac{z-1}{T_s z}\right)}{\tau\left(\frac{z-1}{T_s z}\right) + 1} \tag{4.26}$$

$$= \frac{K_d(z-1)}{\tau(z-1) + \tau z} \tag{4.27}$$

$$= \frac{K_d(z-1)}{z(\tau + T_s) - \tau} \tag{4.28}$$

Since the Backward and Forward Euler methods have constraints in the selection of the sampling time before the system becomes unstable, we have used Tustin to discretize the controller.

Chapter 5

ADAPTATION

There are several methods that can be used to adapt a system. They can be classified as: indirect and direct methods. An indirect method or full adaptation seeks to obtain first the plant parameters and then design the controller based on the identified plant. Direct methods, however, can obtain the parameters of the controller without waiting for the plant estimation to be finalized. A full adaptation has been performed for the buck converter using this method together with a PID controller along with a low-pass filter as shown in section 5.2. Additionally, an adaptation using robust stability condition and switching controller was used in chapter 6.

5.1 Different Plants-Bode Plot

Since it is difficult to predict exactly the way in which a buck converter is going to degrade over time, we have considered two different scenarios with five distinct plants to evaluate the adaptation of the buck converter.

5.1.1 Scenario 1

Scenario 1 studies five different scaled plants: the original plant, a decay of 10% in the inductor while the capacitor was the same, a decay of 10% in the capacitor while the inductor remains the same, a degradation of 10% of both the inductor and capacitor and a deterioration of 15% of both the inductor and capacitor.

- Original Plant: the values of the inductor and capacitor do not change. $L = 9\mu H$ and $C = 0.4\mu F$. Therefore, the scaled plant is given by eq. 5.1.

$$P_{0(scn1)}(s) = \frac{0.00982s^2 + 0.1403}{s^2 + 0.1419s + 0.2778} \tag{5.1}$$

which state space representation is given by eq. 5.2.

$$\dot{x} = Ax + bu \tag{5.2}$$

$$y = Cx + Du \tag{5.3}$$

where the matrices A, B, C and D are given by:

$$A_{0(scn1)} = \begin{bmatrix} -0.1419 & -0.2778 \\ 1 & 0 \end{bmatrix}$$

$$B_{0(scn1)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{0(scn1)} = \begin{bmatrix} 0.00982 & 0.14030 \end{bmatrix}$$

$$D_{0(scn1)} = 0$$

A PID controller has been designed using the Frequency Loop Shaping (FLS) technique. The controller is given by eq. 5.4.

$$C_{0(scn1)}(s) = \frac{7.6968s^2 + 4.1318s + 2.4034}{0.01s^3 + 0.2s^2 + s} \tag{5.4}$$

where eq. 5.4 can be written as a combination of a PID controller together with a low pass filter as shown in eq. 5.5.

$$C_{0(scn1)}(s) = \left(3.8915 + \frac{2.4034}{s} + \frac{7.3077s}{0.1s + 1} \right)\left(\frac{1}{0.1s + 1} \right) \tag{5.5}$$

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- Decaying Plant 1: the value of the inductor decays by 10% ($L = 0.9 * 9\mu H = 8.1\mu H$) while the capacitor remains unchanged ($C = 0.4\mu F$). The corresponding scaled plant for the above specifications is given in eq. 5.6.

$$P_{1(scn1)}(s) = \frac{0.01091s^2 + 0.1559}{s^2 + 0.1472s + 0.3086} \tag{5.6}$$

And the corresponding matrices A, B, C and D from eq. 5.2 are given by:

$$A_{1(scn1)} = \begin{bmatrix} -0.1472 & -0.3086 \\ 1 & 0 \end{bmatrix}$$

$$B_{1(scn1)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{1(scn1)} = \begin{bmatrix} 0.01091 & 0.15590 \end{bmatrix}$$

$$D_{1(scn1)} = 0$$

The controller for the above plant is given by eq. 5.7.

$$C_{1(scn1)}(s) = \frac{6.408s^2 + 3.296s + 2.008}{0.01s^3 + 0.2s^2 + s} \tag{5.7}$$

which equals to a PID controller together with the low pass filter described in eq. 5.8.

$$C_{1(scn1)}(s) = \left(3.0951 + \frac{2.0075}{s} + \frac{6.0988s}{0.1s + 1} \right) \left(\frac{1}{0.1s + 1} \right) \tag{5.8}$$

- Decaying Plant 2: the value of the inductor remains unchanged ($L = 9\mu H$) while the capacitor changes by 10% ($C = 0.9 * 0.4\mu F = 0.36\mu F$). The corresponding scaled plant for the above specifications is given in eq. 5.9.

$$P_{2(scn1)}(s) = \frac{0.00982s^2 + 0.1559}{s^2 + 0.1524s + 0.3086} \tag{5.9}$$

And the matrices A, B, C and D for the state space representation given in eq.
5.2 is given by:

$$A_{2(scn1)} = \begin{bmatrix} -0.1524 & -0.3086 \\ 1 & 0 \end{bmatrix}$$

$$B_{2(scn1)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{2(scn1)} = \begin{bmatrix} 0.00982 & 0.15590 \end{bmatrix}$$

$$D_{2(scn1)} = 0$$

The corresponding controller for the specified plant is given by eq. 5.10.

$$C_{2(scn1)}(s) = \frac{6.404s^2 + 3.295s + 2.011}{0.01s^3 + 0.2s^2 + s} \tag{5.10}$$

The above controller is equivalent to a PID compensator together with a low
pass filter as written in eq. 5.11.

$$C_{2(scn1)}(s) = \left(3.0938 + \frac{2.0114}{s} + \frac{6.0943s}{0.1s + 1}\right)\left(\frac{1}{0.1s + 1}\right) \tag{5.11}$$

- Decaying Plant 3: both the value of the inductor $(L = 0.9 * 9\mu H = 8.1\mu H)$ and
  the capacitor changed by 10% $(C = 0.9 * 0.4\mu F = 0.36\mu F)$. The corresponding
  scaled plant for the above specifications is given in eq. 5.12.

$$P_{3(scn1)}(s) = \frac{0.01091s^2 + 0.1732}{s^2 + 0.1577s + 0.3429} \tag{5.12}$$

And the state space representation for eq. 5.2 is given by the following matrices
A, B, C and D:

$$A_{3(scn1)} = \begin{bmatrix} -0.1577 & -0.3429 \\ 1 & 0 \end{bmatrix}$$

$$B_{3(scn1)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{3(scn1)} = \begin{bmatrix} 0.01091 & 0.1732 \end{bmatrix}$$

$$D_{3(scn1)} = 0$$

A controller was designed for the plant given in eq. 5.12 and is displayed in eq. 5.13.

$$C_{3(scn1)}(s) = \frac{5.254s^2 + 2.569s + 1.666}{0.01s^3 + 0.2s^2 + s} \tag{5.13}$$

which can be rewritten as a PID controller together with a low pass filter as shown in eq. 5.14.

$$C_{3(scn1)}(s) = \left(2.4029 + \frac{1.6659}{s} + \frac{5.0141s}{0.1s + 1} \right) \left(\frac{1}{0.1s + 1} \right) \tag{5.14}$$

- Decaying Plant 4: both the value of the inductor ($L = 0.85*9\mu H = 7.65\mu H$) and the capacitor changed by 15% ($C = 0.85*0.4\mu F = 0.34\mu F$). The corresponding scaled plant for the above specifications is given in eq. 5.15.

$$P_{4(scn1)}(s) = \frac{0.01155s^2 + 0.1942}{s^2 + 0.167s + 0.3845} \tag{5.15}$$

And the corresponding matrices A, B, C and D of the state space representation given in eq. 5.2 is as follows:

$$A_{4(scn1)} = \begin{bmatrix} -0.1670 & -0.3845 \\ 1 & 0 \end{bmatrix}$$

$$B_{4(scn1)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{4(scn1)} = \begin{bmatrix} 0.01155 & 0.1942 \end{bmatrix}$$

$$D_{4(scn1)} = 0$$

The corresponding controller for the specified plant is given by eq. 5.16.

$$C_{4(scn1)}(s) = \frac{4.136s^2 + 1.897s + 1.342}{0.01s^3 + 0.2s^2 + s} \tag{5.16}$$

This controller is equivalent to a PID controller together with a low pass filter as shown in eq. 5.17.

$$C_{4(scn1)}(s) = \left(1.7627 + \frac{1.3425}{s} + \frac{3.9593s}{0.1s+1}\right)\left(\frac{1}{0.1s+1}\right) \tag{5.17}$$

The Bode plot in Fig. 17 shows the frequency response of all different plants together.

5.1.2   Scenario 2

Scenario 2 describes the analysis of five different plants: the original plant, a decay of 10% in the inductor and the capacitor, a decay of 20% in the inductor and the capacitor, a degradation of 30% of both the inductor and capacitor and a deterioration of 40% of both the inductor and capacitor.

- Original Plant: the values of the inductor and capacitor remain the same. $L = 9\mu H$ and $C = 0.4\mu F$. The resulting scaled plant is given by eq. 5.18.

$$P_{0(scn2)}(s) = \frac{0.00982s^2 + 0.1403}{s^2 + 0.1419s + 0.2778} \tag{5.18}$$

And the corresponding matrices A, B, C and D of the state space representation given in eq. 5.2 are:

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Figure 17. Bode Plot of Plants in Scenario 1
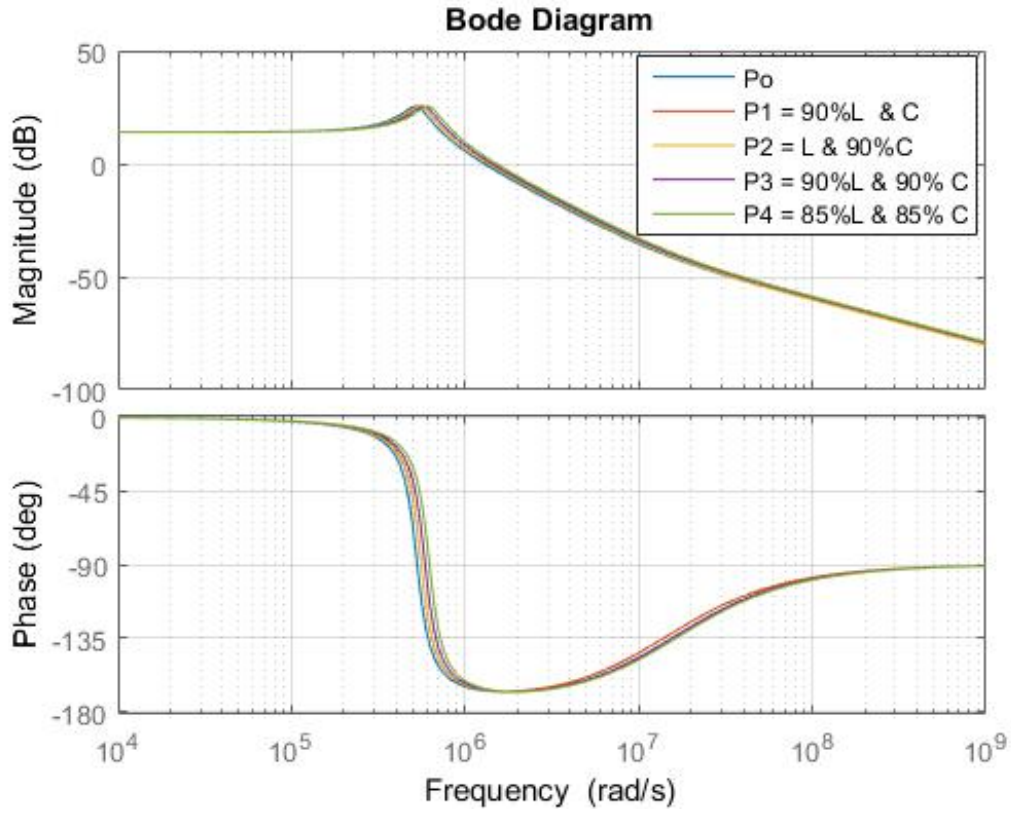
$$A_{0(scn2)} = \begin{bmatrix} -0.1419 & -0.2778 \\ 1 & 0 \end{bmatrix}$$

$$B_{0(scn2)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{0(scn2)} = \begin{bmatrix} 0.00982 & 0.1403 \end{bmatrix}$$

$$D_{0(scn2)} = 0$$

The controller designed in eq. 5.19 corresponds to the plant on eq. 5.1.

$$C_{0(scn2)}(s) = \frac{7.6968s^2 + 4.1318s + 2.4034}{0.01s^3 + 0.2s^2 + s} \tag{5.19}$$

This controller can be rewritten as a PID controller together with a low pass filter as shown in eq. 5.20.

$$C_{0(scn2)}(s) = \left(3.8915 + \frac{2.4034}{s} + \frac{7.3077s}{0.1s+1}\right)\left(\frac{1}{0.1s+1}\right) \qquad (5.20)$$

- Decaying Plant 1: both the inductor and the capacitor degrades by 10% ($L = 0.9 * 9\mu H = 8.1\mu H$, $C = 0.9 * 0.4\mu F = 0.36\mu F$). The scaled plant for the given specifications is described by eq. 5.21.

$$P_{1(scn2)}(s) = \frac{0.01091s^2 + 0.1732}{s^2 + 0.1577s + 0.3429} \qquad (5.21)$$

The state space representation from eq. 5.2 is given by the following matrices A, B, C and D:

$$A_{1(scn2)} = \begin{bmatrix} -0.1577 & -0.3429 \\ 1 & 0 \end{bmatrix}$$

$$B_{1(scn2)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{1(scn2)} = \begin{bmatrix} 0.01091 & 0.1732 \end{bmatrix}$$

$$D_{1(scn2)} = 0$$

The controller designed for the plant in eq. 5.21 is given by eq. 5.22.

$$C_{1(scn2)}(s) = \frac{5.8387s^2 + 3.041s + 1.9672}{0.01s^3 + 0.2s^2 + s} \qquad (5.22)$$

This controller can be rewritten as a PID controller together with a low pass filter as shown in eq. 5.23.

$$C_{1(scn2)}(s) = \left(2.8443 + \frac{1.9672}{s} + \frac{5.5542s}{0.1s+1}\right)\left(\frac{1}{0.1s+1}\right) \qquad (5.23)$$

- Decaying Plant 2: in this plant, the inductor and capacitor degrade by 20% $(L = 0.8 * 9\mu H = 7.2\mu H,\ C = 0.8 * 0.4\mu F = 0.32\mu F)$. This scaled plant is given in eq. 5.24.

$$P_{2(scn2)}(s) = \frac{0.01228s^2 + 0.2192}{s^2 + 0.1774s + 0.434} \tag{5.24}$$

And the corresponding matrices A, B, C and D from eq. 5.2 are given by:

$$A_{2(scn2)} = \begin{bmatrix} -0.1774 & -0.434 \\ 1 & 0 \end{bmatrix}$$

$$B_{2(scn2)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{2(scn2)} = \begin{bmatrix} 0.01228 & 0.2192 \end{bmatrix}$$

$$D_{2(scn2)} = 0$$

A controller designed for the plant given in eq. 5.24 is provided in eq. 5.25.

$$C_{2(scn2)}(s) = \frac{4.5100s^2 + 2.3570s + 1.7508}{0.01s^3 + 0.2s^2 + s} \tag{5.25}$$

which is equivalent to a PID controller together with a low pass filter as written in eq. 5.26.

$$C_{2(scn2)}(s) = \left(2.1819 + \frac{1.7508}{s} + \frac{4.2918s}{0.1s + 1}\right)\left(\frac{1}{0.1s + 1}\right) \tag{5.26}$$

- Decaying Plant 3: both the value of the inductor $(L = 0.7 * 9\mu H = 6.3\mu H)$ and the capacitor changed by 30% $(C = 0.7 * 0.4\mu F = 0.28\mu F)$. The corresponding scaled plant for the above specifications is given in eq. 5.27.

$$P_{3(scn2)}(s) = \frac{0.01403s^2 + 0.2863}{s^2 + 0.2027s + 0.5669} \tag{5.27}$$

And the corresponding state space representation from eq. 5.2 is given by:

$$A_{3(scn2)} = \begin{bmatrix} -0.2027 & -0.5669 \\ 1 & 0 \end{bmatrix}$$

$$B_{3(scn2)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{3(scn2)} = \begin{bmatrix} 0.01403 & 0.2863 \end{bmatrix}$$

$$D_{3(scn2)} = 0$$

The corresponding controller for the plant in eq. 5.27 is given in eq. 5.28.

$$C_{3(scn2)}(s) = \frac{3.981s^2 + 2.302s + 1.989}{0.01s^3 + 0.2s^2 + s} \tag{5.28}$$

This controller can be expressed as a PID controller together with a low pass filter as shown in eq. 5.29.

$$C_{3(scn2)}(s) = \left(2.1032 + \frac{1.9888}{s} + \frac{3.7708s}{0.1s + 1}\right)\left(\frac{1}{0.1s + 1}\right) \tag{5.29}$$

- Decaying Plant 4: in the last case, both the value of the inductor ($L = 0.6*9\mu H = 5.4\mu H$) and the capacitor degraded by 40% ($C = 0.6 * 0.4\mu F = 0.24\mu F$). The scaled plant for the above specifications is described in eq. 5.30.

$$P_{4(scn2)}(s) = \frac{0.01637s^2 + 0.3897}{s^2 + 0.2365s + 0.7716} \tag{5.30}$$

And the corresponding matrices A, B, C and D from eq. 5.2 are given by:

$$A_{4(scn2)} = \begin{bmatrix} -0.2365 & -0.7716 \\ 1 & 0 \end{bmatrix}$$

$$B_{4(scn2)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$C_{4(scn2)} = \begin{bmatrix} 0.01637 & 0.3897 \end{bmatrix}$$

$$D_{4(scn2)} = 0$$

The designed controller in eq. 5.31 corresponds to the plant given in eq. 5.30.

$$C_{4(scn2)}(s) = \frac{2.884s^2 + 1.688s + 1.787}{0.01s^3 + 0.2s^2 + s} \tag{5.31}$$

which can be written as a combination of a PID controller together with a low pass filter as it is expressed in eq. 5.32.

$$C_{4(scn2)}(s) = \left(1.5090 + \frac{1.7868}{s} + \frac{2.7326s}{0.1s + 1}\right)\left(\frac{1}{0.1s + 1}\right) \tag{5.32}$$

The Bode plot in Fig. 18 depicts the frequency responses of all the plants in scenario 2.

It is important to highlight that we should expect a certain amount of error during the transition time when we perform instantaneous changes between different plant coefficients.

5.2   Full Adaptation

All the simulation results have been obtained for the scaled plant as it was explained on section 3.1. Therefore, 1 second of the simulation results is equivalent to 1 microsecond of the original plant. We considered five different plants and two distinct scenarios according to the percentage of degradation of the capacitor and inductor over time. During full adaptation, the parameter estimation is achieved in about 2000 seconds as shown in Fig. 19. Therefore, to properly identify the system, we need to wait first for 2000 seconds to design the controller on-line.
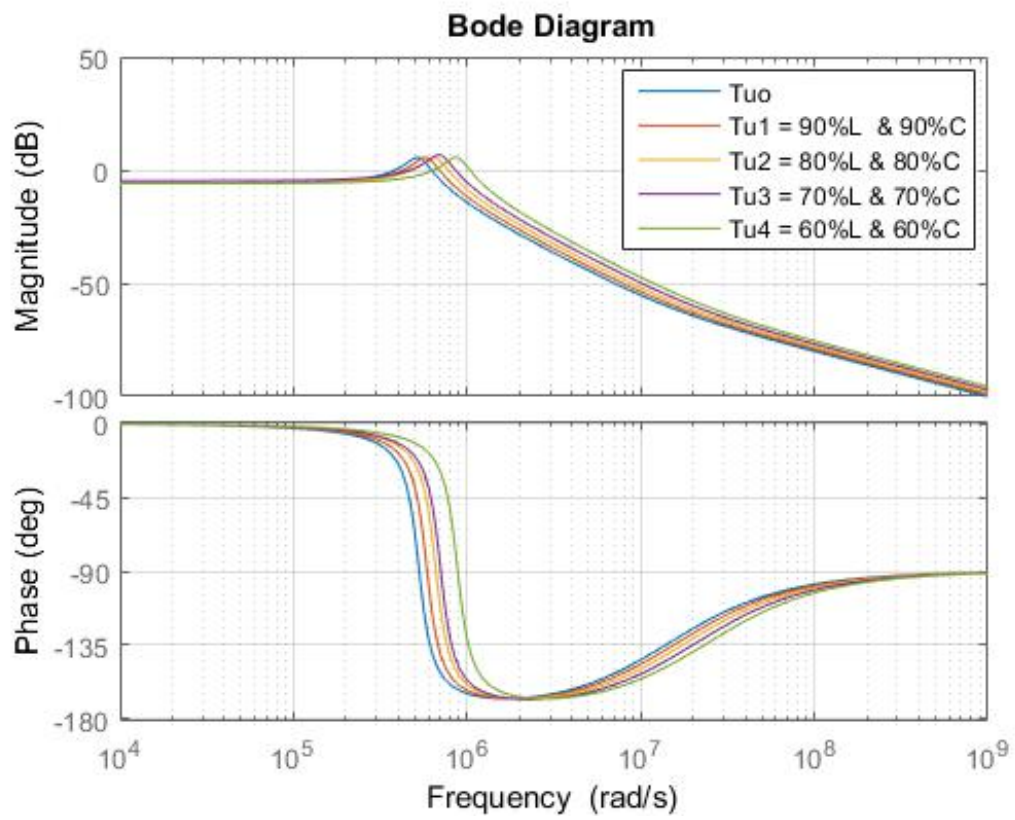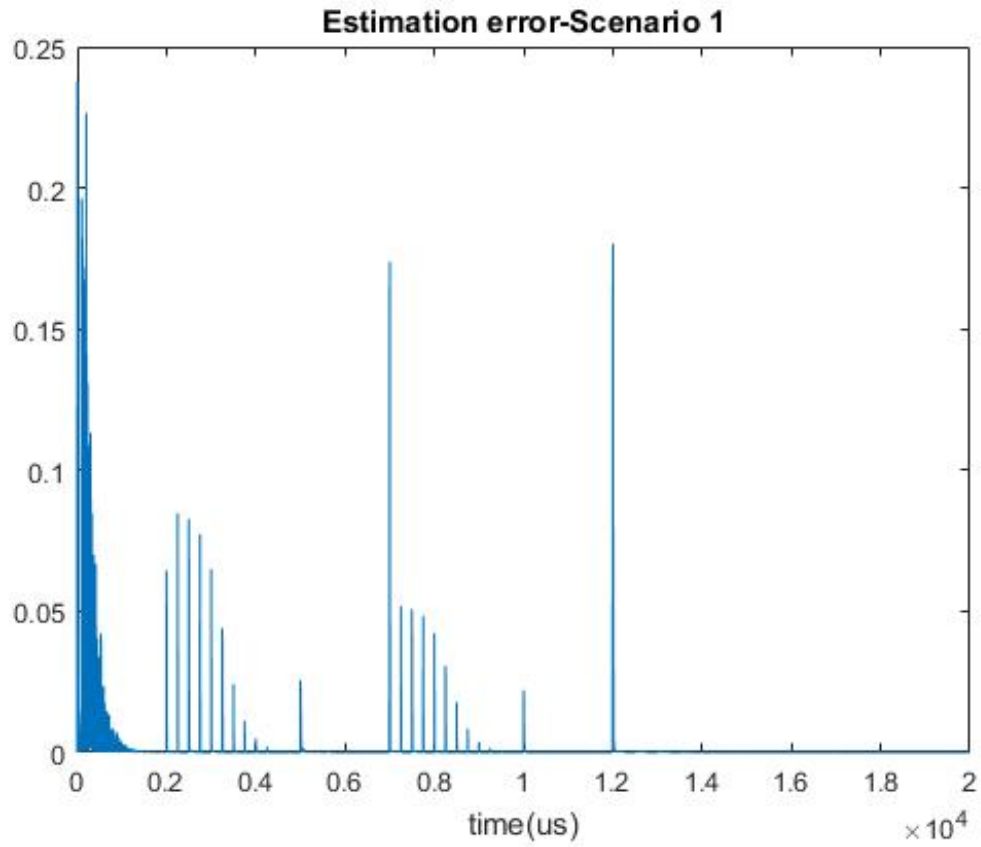
Figure 18. Bode Plot of Plants in Scenario 2

Figure 19. Estimation Error of the Full Adaptation Using the Indirect Scheme

Chapter 6

ROBUST STABILITY CONDITION AND CLOSED LOOP PERFORMANCE

6.1   Uncertainties

In feedback control, we try to design a controller such as the effect of the noise
and disturbances can be reduced as well as the tracking of command signals can be
improved. Additionally, it is good to have a reduction of the effects of the plant
uncertainties. However, the mathematical description of the plant is almost never
perfect. Yet, a good controller should be designed such that we can maintain stability
of the closed-loop system and an acceptable performance of the plant even in the
presence of uncertainties. That is what we know as robust stability and robust
performance, respectively. We will start our study of robust stability and robust
performance by assuming that the transfer function that describes our system belongs
to an uncertainty set Ω. We will start our study by describing the effects of considering
additive uncertainties.

6.1.1   Additive Uncertainty

In practice, it is common to find a nominal plant that is accurate at low frequencies
and degrades over the high frequencies. This is due to effects such as parasitic,
nonlinearities or plants that change over time and their effect is more significant at
high frequencies. As a result, these high frequency effect could have been left out
during the modeling process. This effect is usually mitigated by the fact that the

plant is defined as a proper transfer function, so that the system starts to roll off at high frequencies. For this scenario, based on the fact that the nominal plant is given by $P_o(s)$ and the difference between the actual plant $P(s)$ and the nominal plant is stable, we can characterize the model uncertainty by obtaining some bounds as given in eq. 6.1.

$$|P(j\omega) - P_o(j\omega)| \leq \ell_a(\omega) \tag{6.1}$$

where the bounds are given by eq. 6.2

$$\ell_a(\omega) = \begin{cases} \text{``Small''}; & |\omega| < \omega_c \\ \text{``Bounded''}; & |\omega| > \omega_c \end{cases} \tag{6.2}$$

This shows that the actual plant lies on values that are inside a band of uncertainties around the nominal plant. Additional attention should be put to the fact that there is no any information related to the phase of the plant to derive the modeling error. Therefore, the results from this analysis may be conservative.

Based on the previous results, one might describe the additive characterization of the uncertainty set by eq. 6.3.

$$\Omega_a = P(s)|P(s) = P_o(s) + W(s)\Delta(s) \tag{6.3}$$

where $\Delta(s)$ is a stable transfer function that satisfies the condition in eq. 6.4

$$||\Delta||_\infty = \sup_\omega |\Delta(j\omega)| \leq 1 \tag{6.4}$$

Additionally, $W(s)$ is a weighting stable proper term that is used to describe how accurate the nominal plant is as the frequency changes. When the weighting term increases at high frequencies, it is reasonable to model it as a high pass filter with a
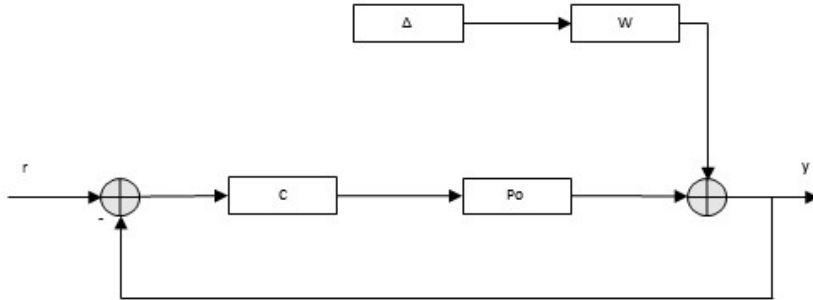
Figure 20. Additive Uncertainty

small magnitude at lower frequencies and a high but bounded magnitude at higher frequencies.

Figure 20 shows the representation of the additive uncertainty. From this representation, we can point out that $P(s)$ is the actual plant with minimal realization which can be written as $P_o(s) + W(s)\Delta(s)$.

There are some important aspects about the uncertainty set:

- The unstable poles of the plants in the set corresponds to the nominal plant. Thus, in the system identification process, one has to be careful to properly capture the unstable poles of the system.
- The uncertainty set includes models of large order. If the major concern is a particular model, then the uncertainty set would overestimate the plants around that particular model.

The control that we will design is guaranteed to work for every member within the uncertainty set. Thus, the controller will treat every plant in the uncertainty set as a possible candidate for the system. However, since not all the members of the set are possible plants, the results derived with the use of additive uncertainty will be conservative.

Suppose that we have a set with possible plants Π and the nominal plant P_o is a member of that set. Then, for the rest of the plants in that set, we can write eq. 6.5.

$$P(j\omega) = P_o(j\omega) + W(j\omega)\Delta(j\omega) \tag{6.5}$$

The weight $|W(j\omega)|$ satisfies the inequalities given in eq. 6.6 and eq. 6.7.

$$|W(j\omega)| \geq |W(j\omega)\Delta(j\omega)| = |P(j\omega) - P_o(j\omega)| \tag{6.6}$$

$$|W(j\omega)| \geq \max_{P \in \Pi}|P(j\omega) - P_o(j\omega)| = \ell_a(j\omega) \tag{6.7}$$

Since we described the lower bound of ℓ_a in eq. 6.2, we can find a stable system $W(s)$ such that $|W(j\omega)| \geq \ell_a(j\omega)$.

6.1.2   Robust Stability Condition

The robust stability condition (RSC) provides a certain value of error. The computation is performed as follows:

- Compute the sensitivity (S) of the target loop (L) and multiply it by each of the designed controllers $(C_0, C_1\ C_2, C_3, C_4)$. The controller also has a low pass filter to minimize the effects of the resonance peak. All controllers and low pass

filters have been discretized using Tustin. Additionally, this result is multiplied by the filter bank. We chose 50 filters for the filter bank since this will allow us to obtain the frequency responses at fifty points within the bandpass filter. This could be convenient since our five different plants to be evaluated do not differ significantly from each other in their frequency response in scenario 1. Multiplying by the filter bank makes the response available in time and will be seen in the simulation as $SC1y$, $SC2y$, $SC3y$, $SC4y$, $SC5y$).

- Compute the complementary sensitivity (T) using the target loop information and multiply it by the filter bank to obtain Tu.

- Use the output of the plant to pass it through another filter bank to obtain u.

- Compute the error (E) by calculating the result from sensitivity times the controller (with the low pass filter) times the filter bank for each of the controllers ($SC1y$, $SC2y$, $SC3y$, $SC4y$, $SC5y$) minus Tu.

- Obtain the error square (E^2) and u^2.

- Compute the transfer function given in eq. 6.8

$$\frac{1}{s + \varepsilon} \tag{6.8}$$

where ε is determined by the number of samples times the sampling time. The transfer function has been also discretized using the Tustin method. The number of samples will determine the duration in which the robust stability condition is going to be evaluated. This method will allow to compute the robust stability condition during a window as opposed to have instantaneous changes in the robust stability computation.

- The square root of the previous result is calculated.

The description listed above for the robust stability condition (RSC) can be summarized in the eq. 6.9.

$$RSC = \frac{||SCy - Tu||}{||u||} \tag{6.9}$$

6.2 Results from Robust Stability Condition

The robust stability condition described in subsection 6.1.2 was used to determine which controller was most suitable at each specific time when the plant changed its parameters. All the plants have been scaled down as it was described in sections 3.1 and 5.1. Since these simulation results have been scaled down, when we refer to a simulation time of 1 second, this corresponds to a 1μsecond of the original plant. The plant transition occurs at times 1000, 5000, 10000 and 15000 seconds. Fig. 21 displays the robust stability condition for scenario 1. It takes about 750 samples to reach the steady state value for the first, second and fourth plant transition and around 500 samples for the third one.

The controller parameters are shown in Fig. 22. The controller for the nominal plant is properly selected after computing the robust stability condition. Similarly, the right controller is selected for the first plant transition at 1000 seconds. However, the controller remains the same in the second plant transition at 5000 seconds. This is be due to the almost negligible difference between those plants. Similarly, when the third transition occurs at 10000 seconds, the controller remains the same, although there should have been changed. Finally, in the last plant transition at 15000 seconds, the controller changes, but it does not correspond to the correct one for that specific plant.
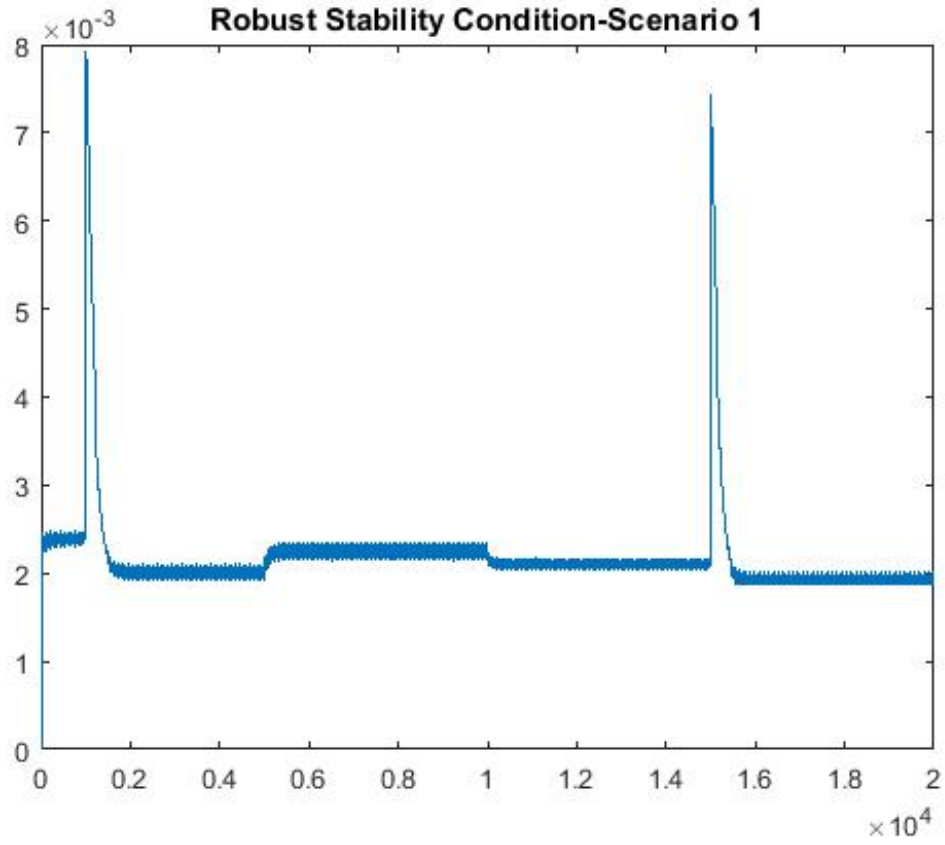
Figure 21. Robust Stability Condition in Scenario 1

Fig. 23 shows the results of the robust stability condition for scenario 2. The computation settles at around 750 samples after the first and second plant transition at 1000 seconds and 5000 seconds, respectively. Then, it takes about 500 samples after the third and fourth plant transition to reach the steady state value. The results shown here corresponds to the correct selection of controller for each of the plants specified at times 1000, 5000, 10000 and 15000 seconds.

The transition for all the controller parameters in scenario 2 are shown in Fig. 24. The plant transition occurs at times 1000, 5000, 10000 and 15000 seconds and the controller parameters changed accordingly to the proper optimal candidate.

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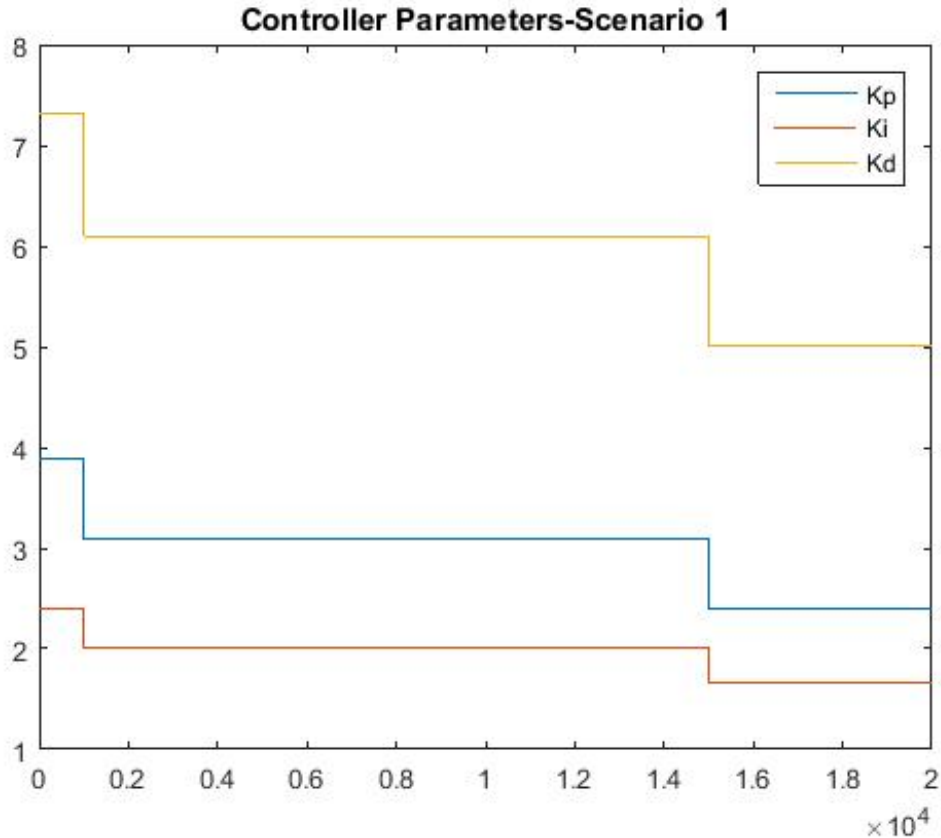
Figure 22. Controller Parameters in Scenario 1

6.3 Controlled Output

The voltage at the output of the buck converter will depend on what controller is selected for each plant transition based on the computation of the robust stability condition. The transition is happening at times 1000, 5000, 10000 and 15000 seconds of the scaled plant. That is the reason why a mismatch is observed during those transition times. For example, at t=1000 seconds the response displays a higher peak compared to the rest of the responses during that period between $t = 1000s$ and $t = 5000s$.

For comparison purposes, we plotted the voltage at the output for plant P1 in

Figure 23. Robust Stability Condition in Scenario 2
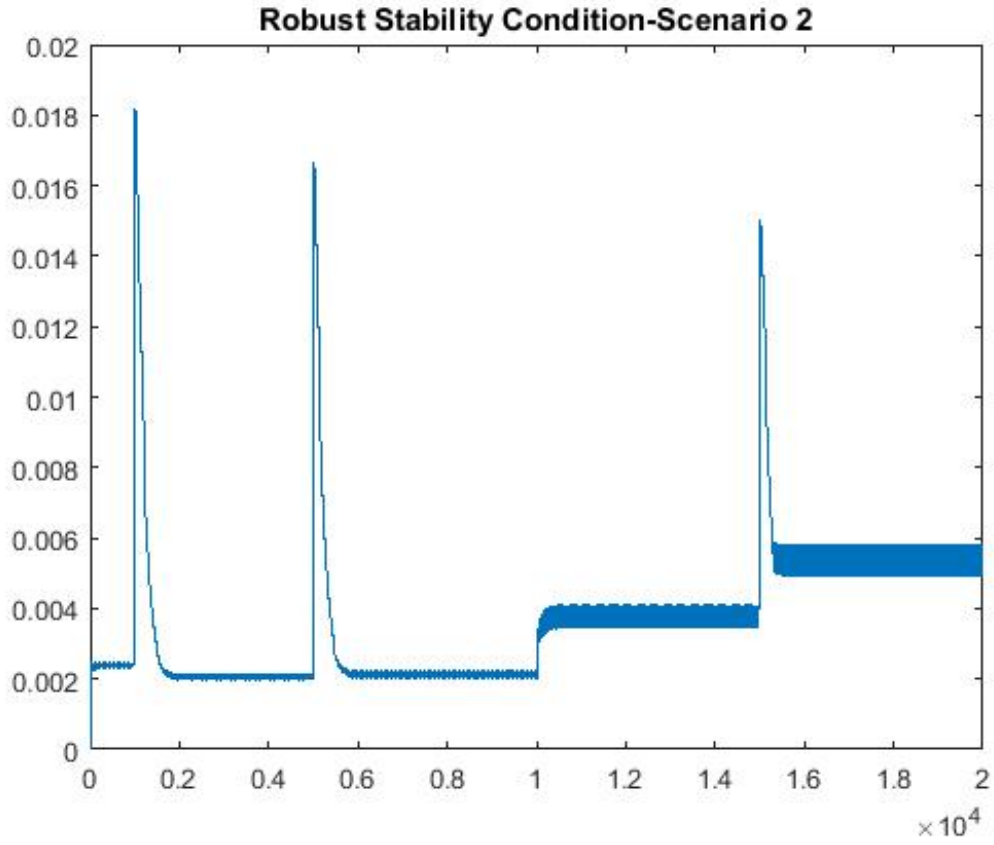
scenario 1 as shown in Fig. 25. Since the first plant transition happens at $t = 1000$ seconds, it is expected to have a little error signal that does not occur at other transitions before $t = 5000$ seconds when the second plant transition takes place. The response of the controller chosen using robust stability condition was compared to the response if we keep five PID controllers constant. The higher peak occurs when either controller C3 or C4 are selected producing about a 20% of overshoot. Additionally, the system takes more than 20 seconds to reach steady state. On the other hand, the best responses are obtained by either implementing the controller selected by the robust stability condition computation or C0. The overshoot in both cases is less than 10% and the settling time less than 20 seconds.
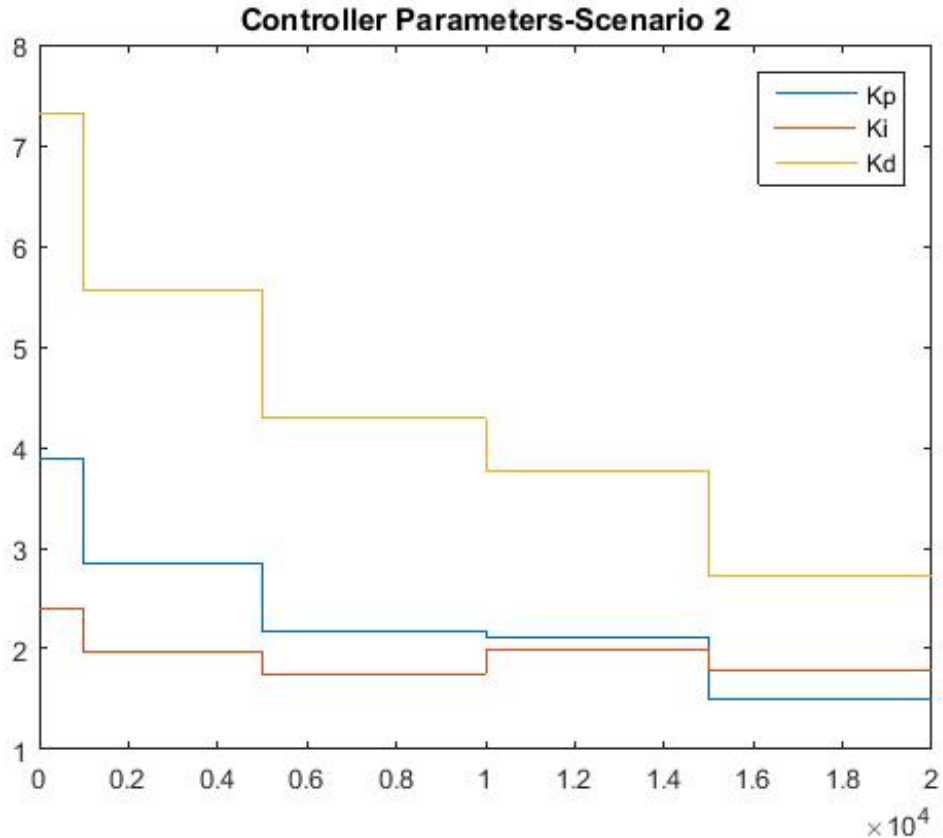
Figure 24. Controller Parameters in Scenario 2

These results are consistent with the frequency response shown in Fig. 26. The Bode plot shows a comparison of the frequency response of plant P1 when all the fixed controllers are applied to that plant. The phase margin and cutoff frequency are summarized in table 7.

A second analysis was performed for plant P2 when we observe a comparison of the voltage at the output when we apply the controller selected using the robust stability condition versus all the five fixed controllers as shown in Fig. 27. The controller that was selected at this transition was controller C1 which is acceptable because the difference between plants P1 and P2 are almost negligible. Although the transition

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Figure 25. Comparison of the Voltage at the Output of Plant P1 for Scenario 1 Using all the Fixed Controllers versus RSC

Table 7. Frequency Response of Plant 1 in Scenario 1 With Five Different PID Controllers

Controller	Phase Margin (deg)	Cutoff Frequency (rad/sec)
C0	69.1	1.32
C1	66.8	1.14
C2	66.8	1.14
C3	64.2	0.981
C4	60.5	0.84

occurred at $t = 5000$ seconds, there is not a significant higher overshoot at that transition compared to the responses in the rest of that period. An overshoot of less than 20% is obtained when we keep either controller C3 or C4 fixed and it also takes
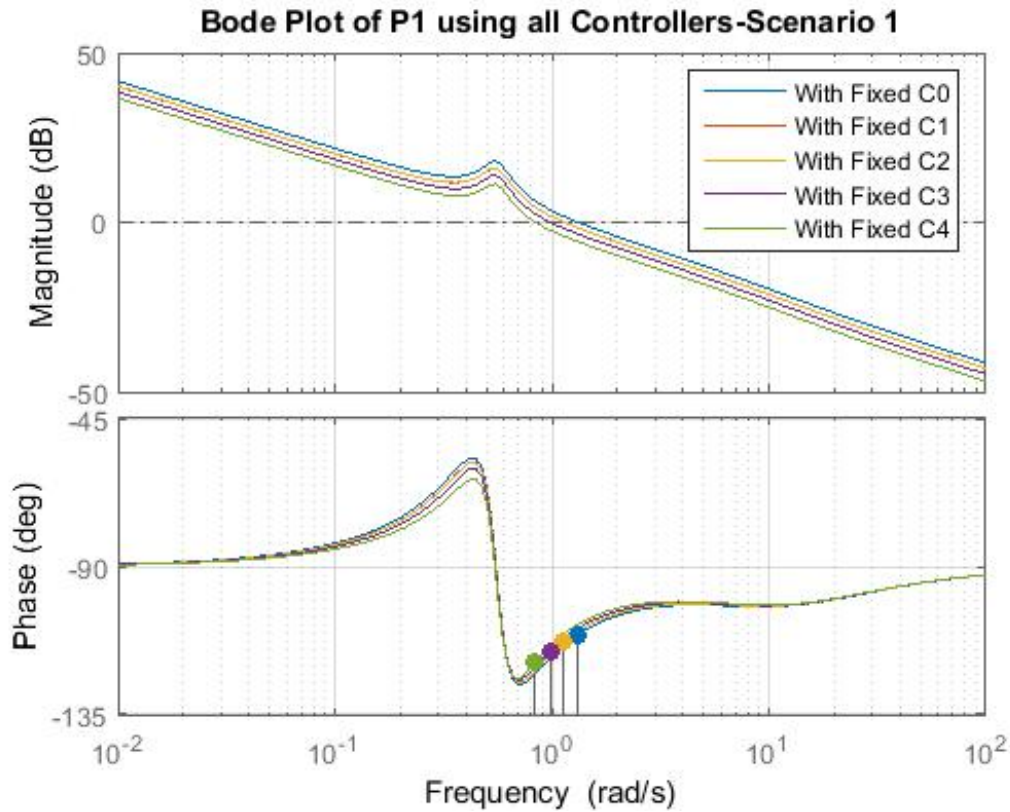
Figure 26. Comparison of the Frequency Response of Plant P1 for Scenario 1 Using all the Fixed Controllers

more than 20 seconds to stabilize. A smaller overshoot of about 10% is visible when the controller chosen by the robust stability condition or C0 is selected. These results are consistent with the Bode plot shown in Fig. 28 which has been summarized in table 8.

A plant transition to P3 took place at $t = 10000$ seconds and the voltage at the output for the controller chosen by robust stability computation versus all the fixed controllers is shown in Fig. 29. Although the plant was different from plants P1 and
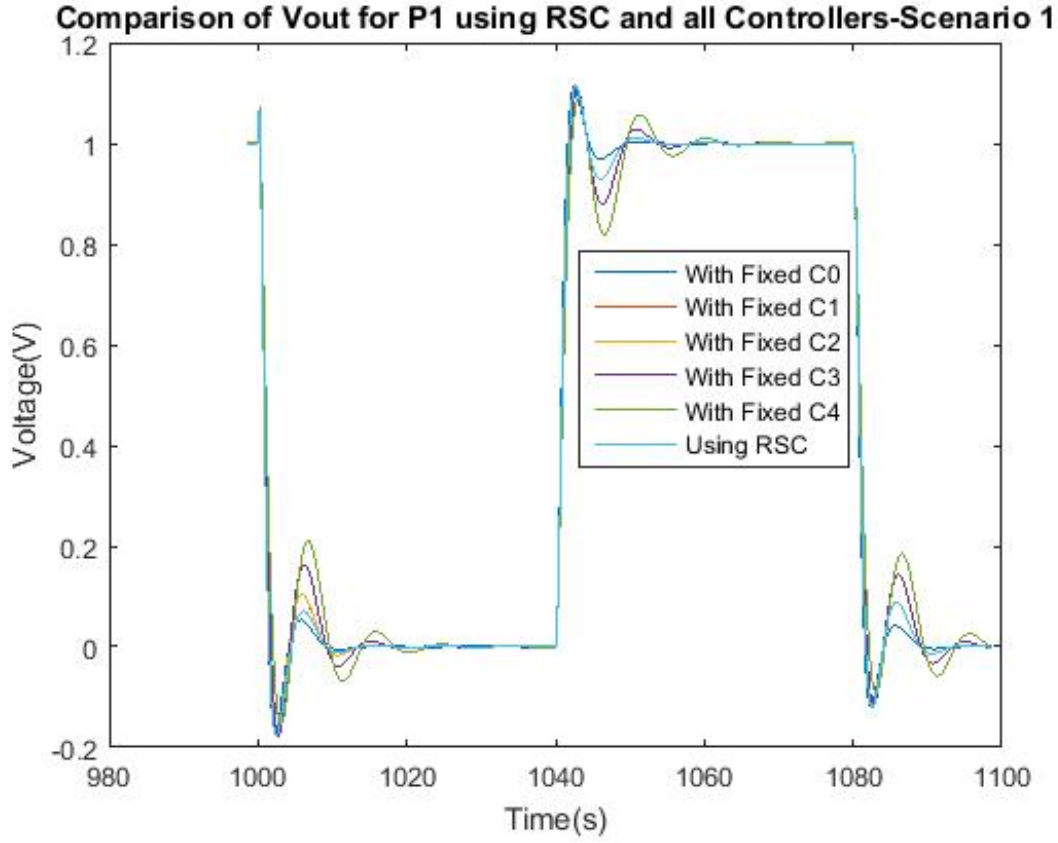
Figure 27. Comparison of the Voltage at the Output of Plant P2 for Scenario 1 Using all the Fixed Controllers versus RSC

Table 8. Frequency Response of Plant 2 in Scenario 1 With Five Different PID Controllers

Controller	Phase Margin (deg)	Cutoff Frequency (rad/sec)
C0	68.8	1.32
C1	66.7	1.14
C2	64.2	0.98
C3	64.2	0.98
C4	60.7	0.838

P2, the controller selected was still C1. This may be due to the trivial difference between these plants which is not so remarkable.
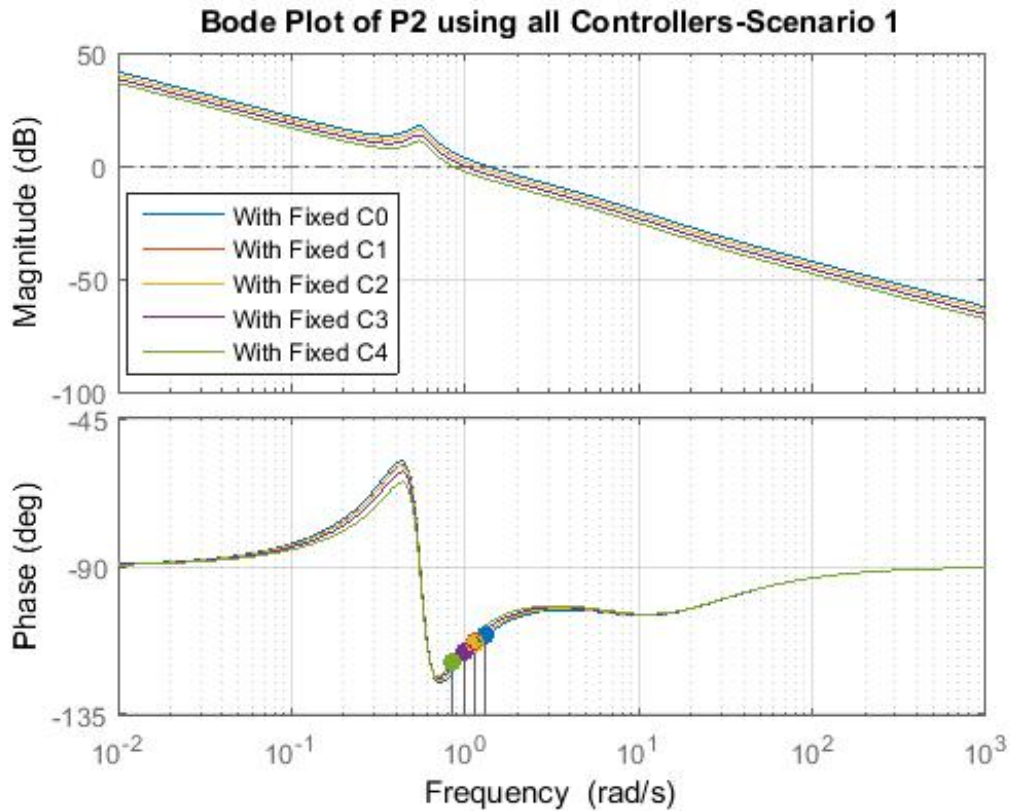
Figure 28. Comparison of the Frequency Response of Plant P2 for Scenario 1 Using all the Fixed Controllers

This is consistent with the results obtained in the frequency response shown in Fig. 30 where the response of all the controllers acting on P3 are summarized on table 9.

Table 9. Frequency Response of Plant 3 in Scenario 1 With Five Different PID Controllers

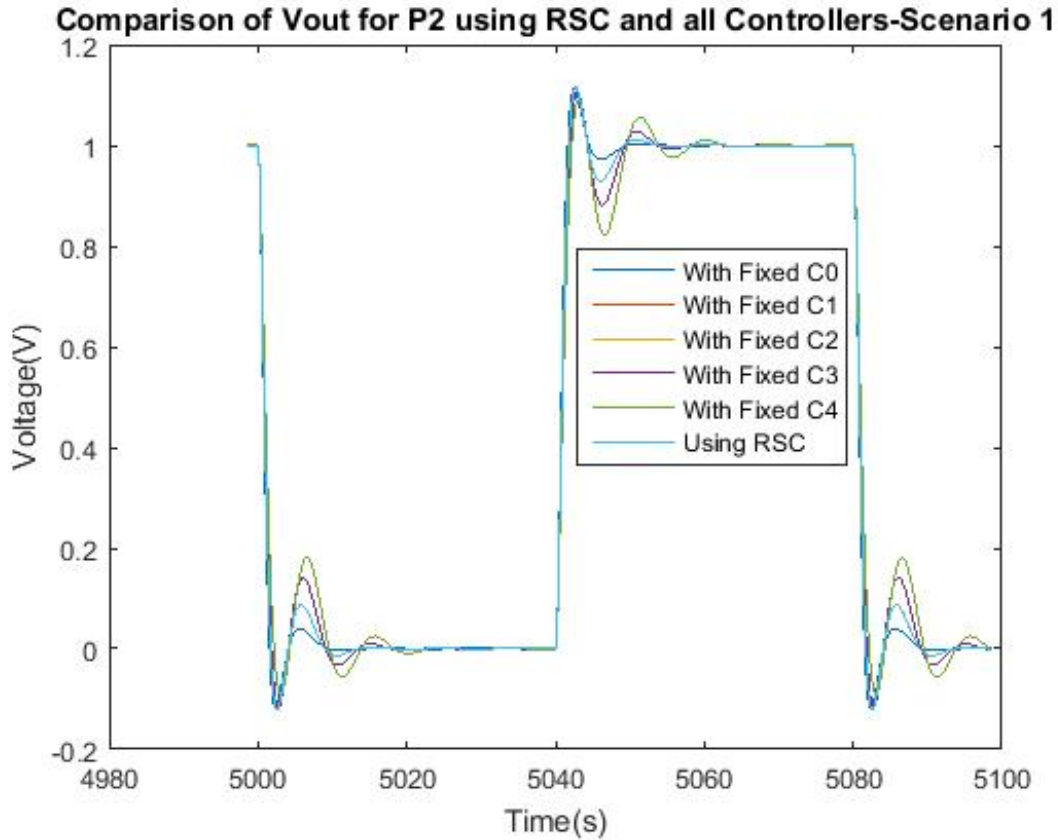| Controller	Phase Margin (deg)	Cutoff Frequency (rad/sec)
C0	70.9	1.46
C1	69.4	1.25
C2	69.4	1.25
C3	67.5	1.08
C4	65.1	0.917

Figure 29. Comparison of the Voltage at the Output of Plant P3 for Scenario 1 Using all the Fixed Controllers versus RSC

The final plant transition in scenario 1 takes place at time $t = 15000$ seconds. The voltage at the output shown in Fig. 31 displays a bigger overshoot when the transition happens as it is expected. Controller C4 has the highest overshoot from all the responses with a percentage of about 20% and it takes almost 20 seconds to stabilize. Controller C3 produces an overshoot of less than 20% and more than 10 seconds to stabilize. It is also observed that the optimal controller chosen by the robust stability condition and C2 provide and overshoot of about 10% and the system stabilizes in about 15 seconds. Controller C0 causes the system to have the smallest overshoot of about 5% and reaches steady state in about 10 seconds.
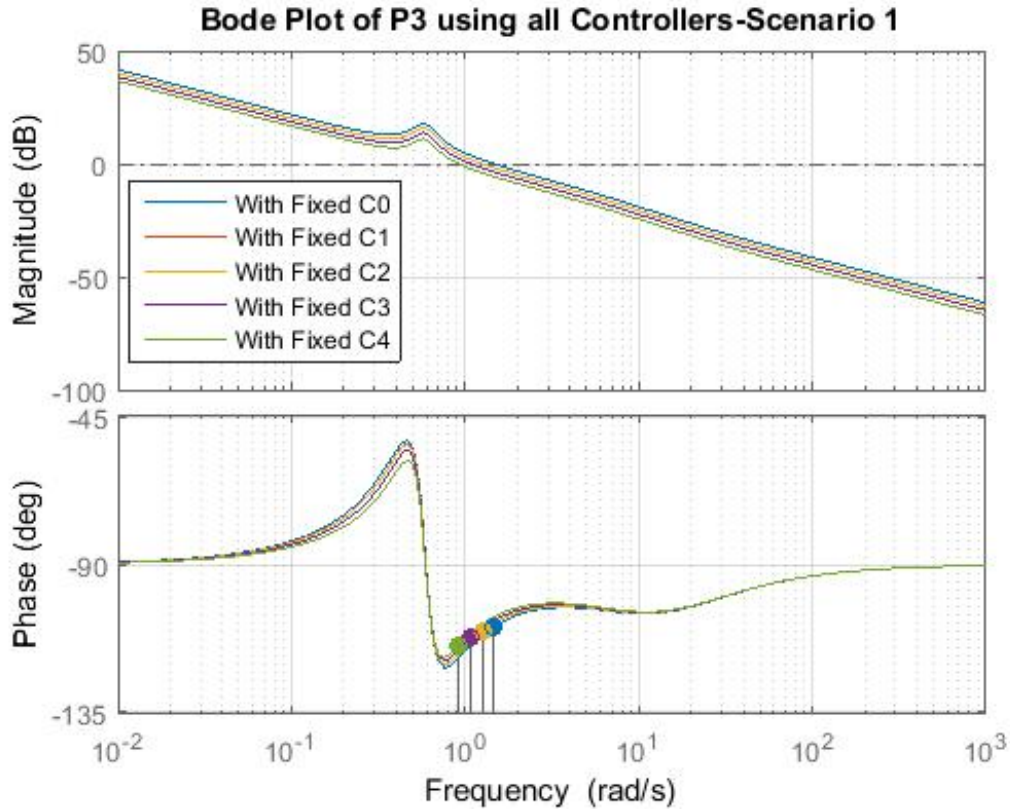
Figure 30. Comparison of the Frequency Response of Plant P3 for Scenario 1 Using all the Fixed Controllers

All of the previous results are also consistent with the responses obtained from the Bode plot shown in Fig. 32 where all the fixed controllers are compared against each other acting on plant P4. A summary of these results are provided on table 10.

A similar analysis was performed for scenario 2. The voltage at the output for plant P1 in scenario 2 is shown in Fig. 35. Plant P1 takes place from $t = 1000$ to $t = 5000$ and we can observe a bigger overshoot at the plant transition at $t = 1000$ as it was expected. The controller selected using robust stability condition is C1 which is the corresponding controller for the given plant. For comparison purposes, we also
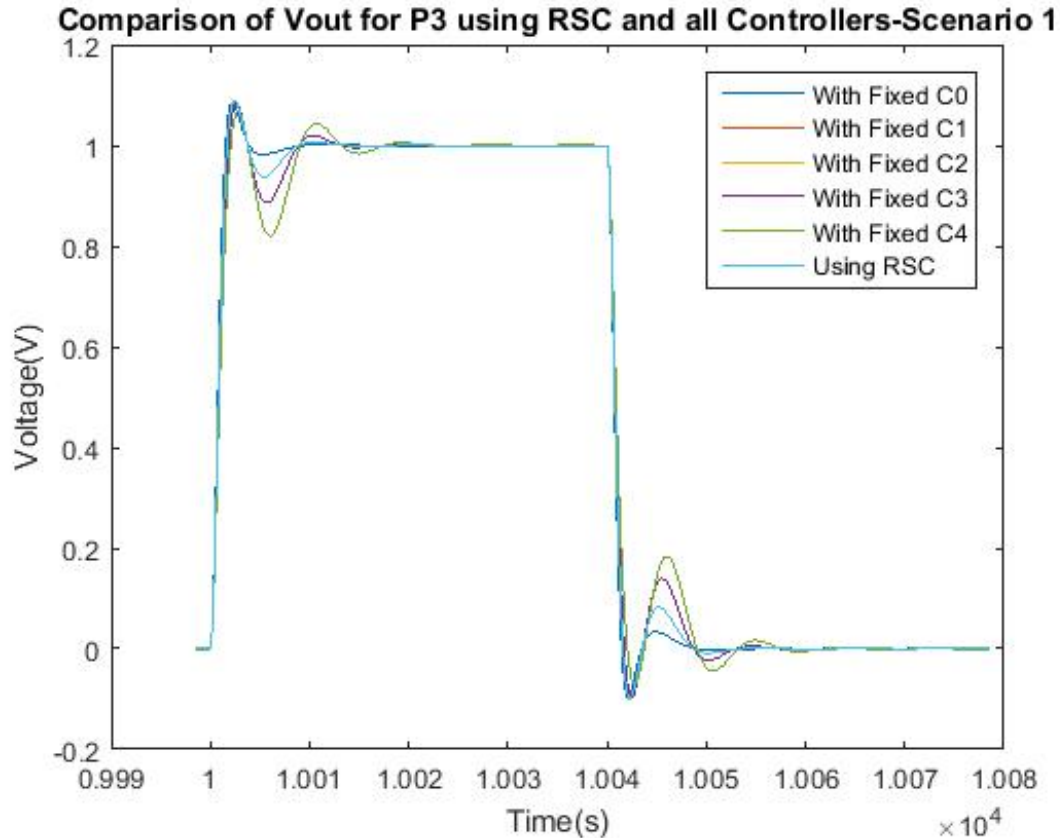
Figure 31. Comparison of the Voltage at the Output of Plant P4 for Scenario 1 Using all the Fixed Controllers versus RSC

Table 10. Frequency Response of Plant 4 in Scenario 1 With Five Different PID Controllers

Controller	Phase Margin (deg)	Cutoff Frequency (rad/sec)
C0	72.6	1.62
C1	71.5	1.40
C2	71.5	1.40
C3	70.4	1.20
C4	68.9	1.01

show the results if we keep the other fixed controllers during the plant transition. It is clearly visible that controller C4 will make the system unstable and controller C3 will stabilize in about 40 seconds. Both controllers have an overshoot of more than

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Figure 32. Comparison of the Frequency Response of Plant P4 for Scenario 1 Using all the Fixed Controllers

20%. Controller C2 stabilizes faster in about 20 seconds, but it also has an overshoot of about 20%. Controller C1 reaches steady state in about 10 seconds and has an overshoot of about 10%. These results are consistent with the compensated loop shown in Fig. 34 which is summarized on table 11.

The voltage at the output was also plotted for plant P2. The plant transition occurs at time $t = 5000$ seconds and that is why we observe a bigger overshoot (almost double) at that time compared to the rest of the of the transitions within that period. The robust stability condition selected controller C2 as the optimal choice and this
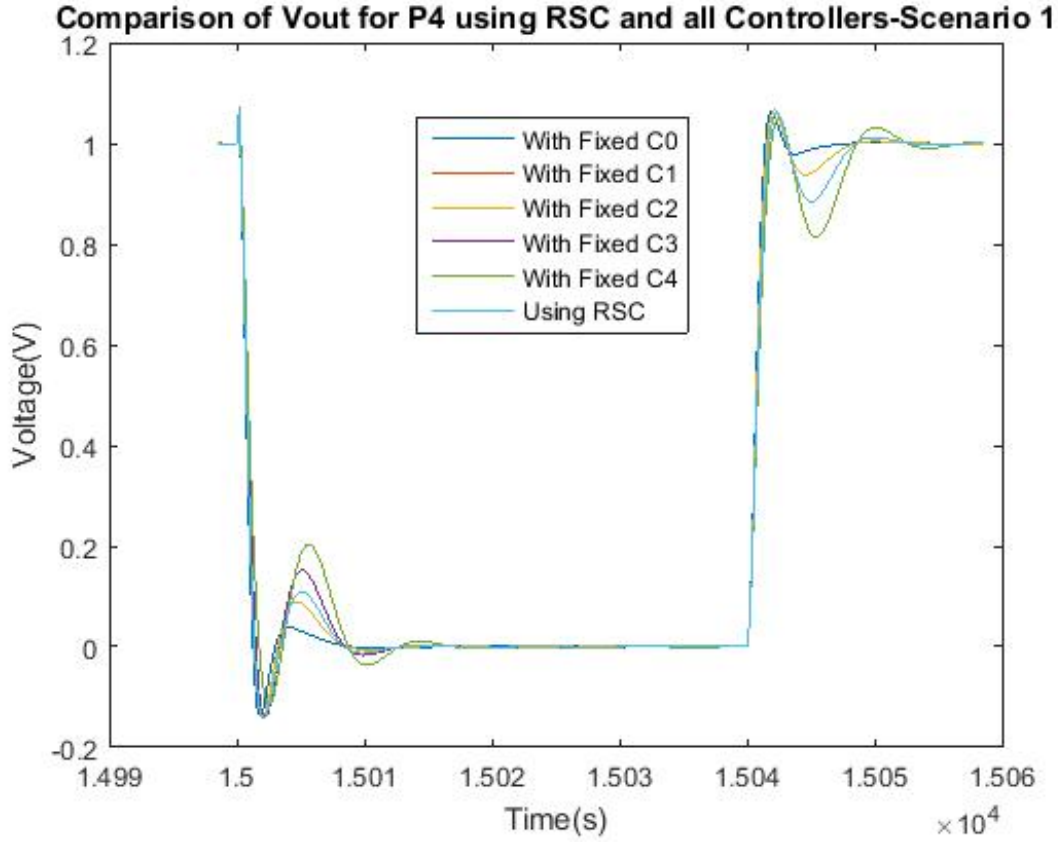
Figure 33. Comparison of the Voltage at the Output of Plant P1 for Scenario 2 Using all the Fixed Controllers versus RSC

Table 11. Frequency Response of Plant 1 in Scenario 2 With Five Different PID Controllers

Controller	Phase Margin (deg)	Cutoff Frequency (rad/sec)
C0	70.9	1.46
C1	67.0	1.01
C2	59.3	1.08
C3	44.3	0.879
C4	21.8	0.78

corresponded to the plant defined during that time-frame. For comparison purposes, we also plotted what the response would look like if we chose any fixed controller. The biggest overshoot of more than 20% is obtained when controller C4 is used. Similarly,
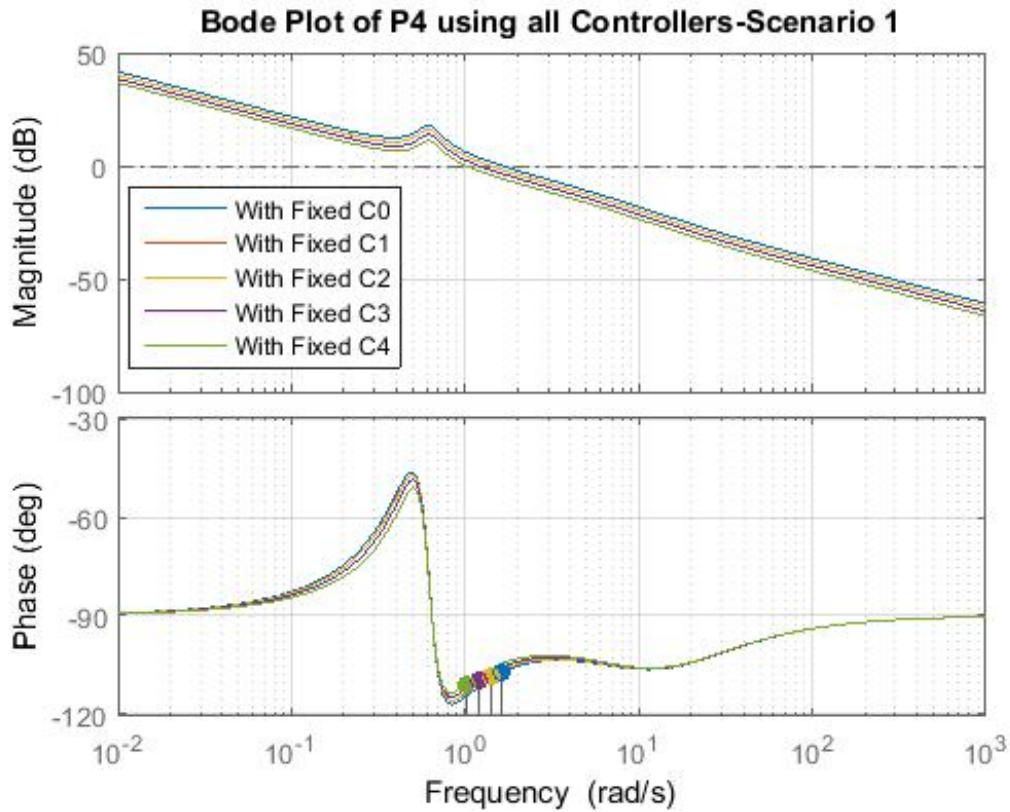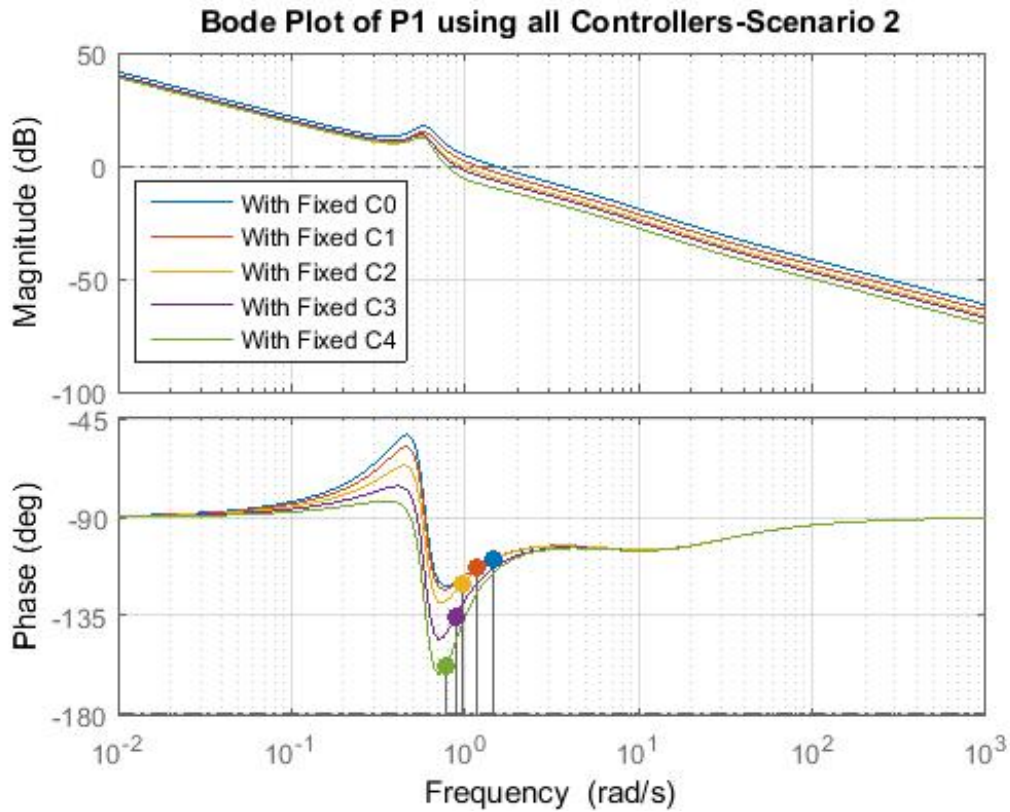
Figure 34. Comparison of the Frequency Response of Plant P1 for Scenario 2 Using all the Fixed Controllers

controller C3 produces an overshoot of about 20% and stabilizes in more than 20 seconds. Controller C1 creates an overshoot of 10% approximately and stabilizes in more than 10 seconds. All these results are consistent with the frequency response provided in Fig. 34 where we made a comparison of all the fixed controllers acting on plant P2. These results are summarized on table 12.

The voltage at the output was also plotted for plant P3. The transition occurs at time $t = 10000$ seconds. The optimal controller chosen after computing the robust
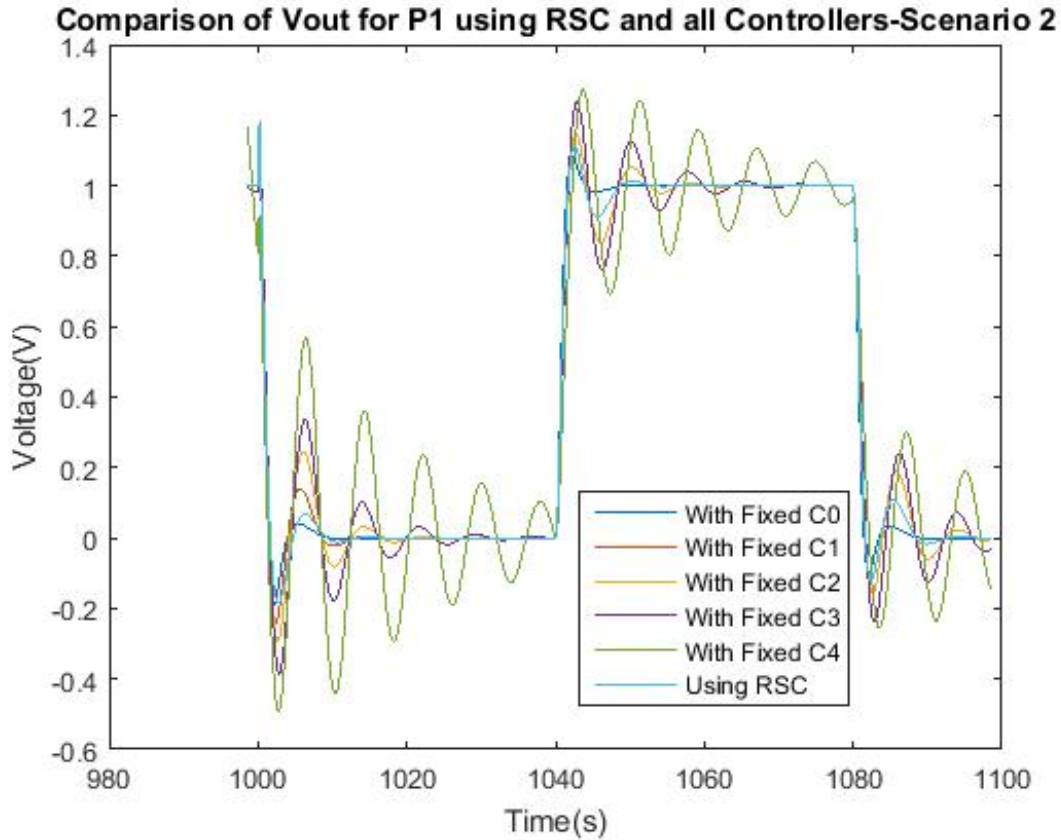
Figure 35. Comparison of the Voltage at the Output of Plant P2 for Scenario 2 Using all the Fixed Controllers versus RSC

Table 12. Frequency Response of Plant 2 in Scenario 2 With Five Different PID Controllers

Controller	Phase Margin (deg)	Cutoff Frequency (rad/sec)
C0	73.9	1.82
C1	72.0	1.45
C2	67.8	1.18
C3	58.2	1.06
C4	39.7	0.781

stability condition is C3 that corresponded to the controller for P3. For comparison purposes, we also plotted the response when we used any of the five fixed PID controllers. The biggest overshoot of about 20% occurs when controller C4 is used.

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Figure 36. Comparison of the Frequency Response of Plant P2 for Scenario 2 Using all the Fixed Controllers

The system stabilizes in about 20 seconds. Although a similar overshoot happens when controller C2 is used, the system stabilizes in about 15 seconds. An overshoot of less than 20% occurs when controller C1 is used. All of these results are consistent with the frequency response observed in Fig. 38 and summarized on table 13.

Finally, the voltage at the output for plant P4 is shown in Fig. 39. The optimal controller using the robust stability condition was C4 as we were expecting. A comparison was made to observe the response of the optimal controller versus all the other fixed controllers. A bigger overshoot is happening at the plant transition which
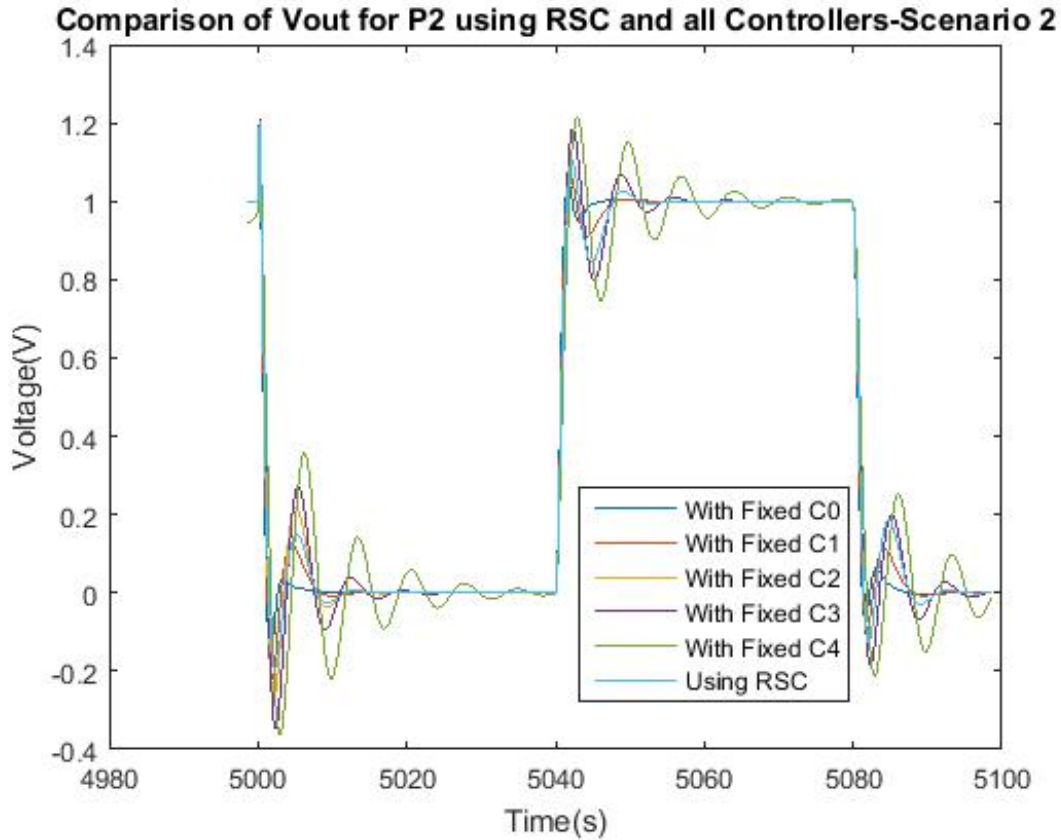
Figure 37. Comparison of the Voltage at the Output of Plant P3 for Scenario 2 Using all the Fixed Controllers versus RSC

Table 13. Frequency Response of Plant 3 in Scenario 2 With Five Different PID Controllers

Controller	Phase Margin (deg)	Cutoff Frequency (rad/sec)
C0	75.2	2.33
C1	74.8	1.85
C2	73.1	1.51
C3	67.9	1.35
C4	57.7	1.08

is expected since the previous plant was different. All the controllers display almost the same overshoot of about 20% and stabilize in about 15 seconds or less. However, controller C1 presented particular oscillations even before reaching the step level. All
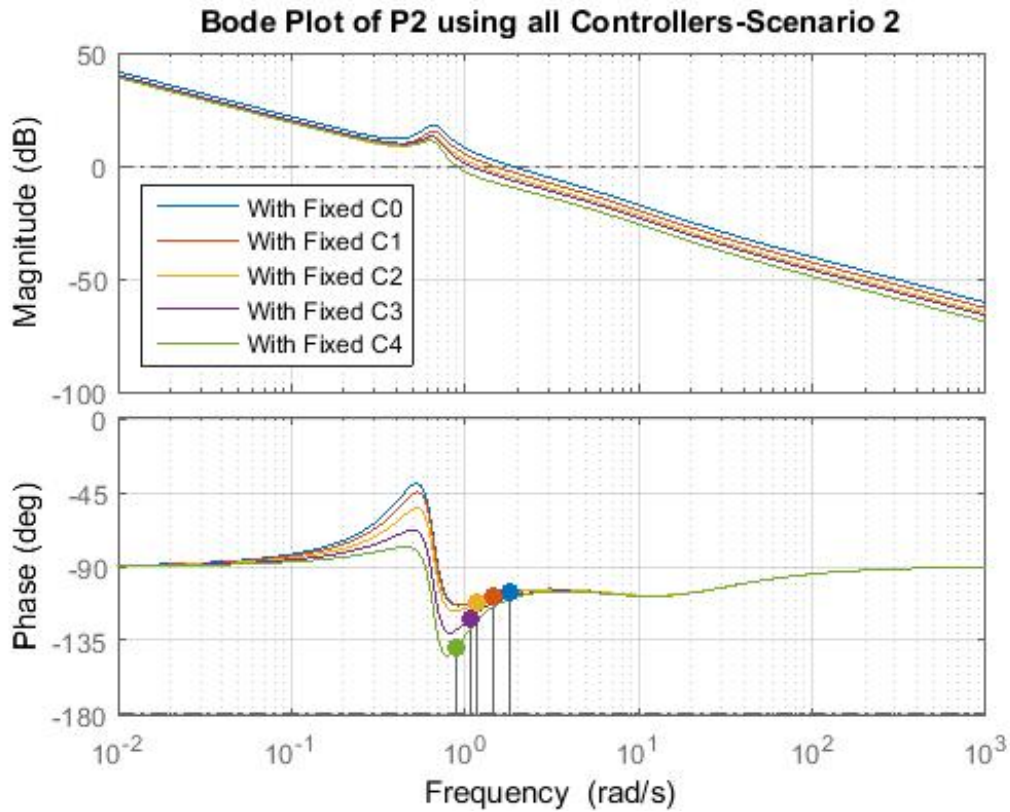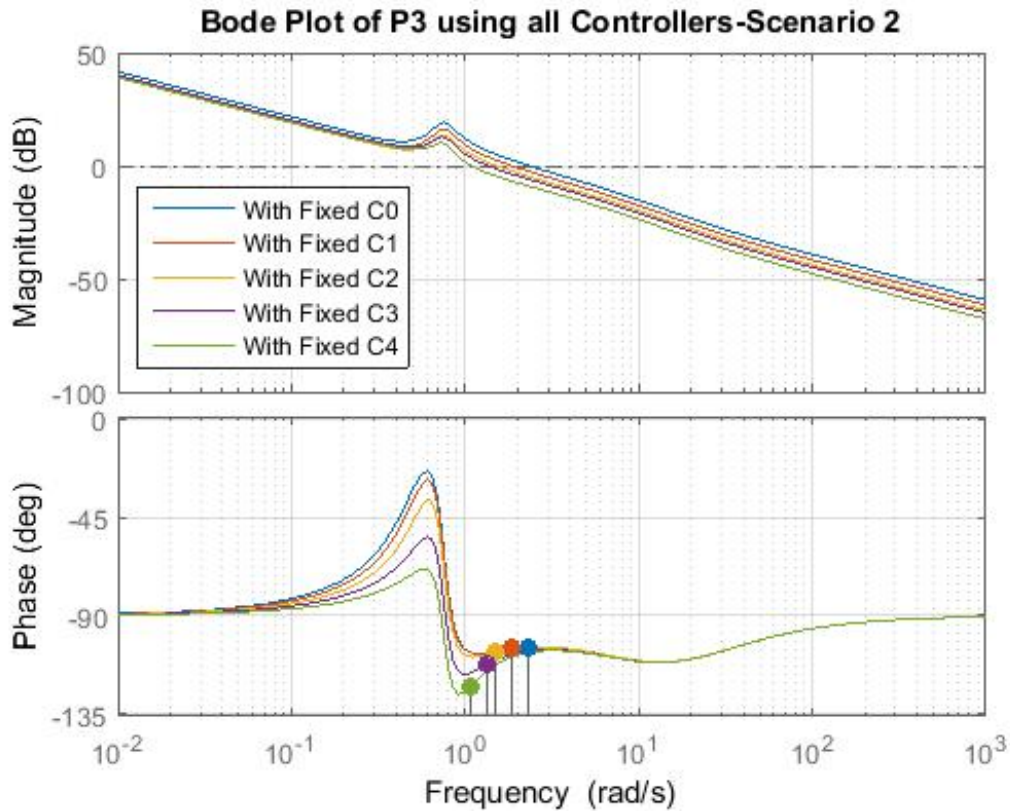
Figure 38. Comparison of the Frequency Response of Plant P3 for Scenario 2 Using all the Fixed Controllers

of these responses are consistent with the frequency response shown in Fig. 40 and summarized on table 14.

Table 14. Frequency Response of Plant 4 in Scenario 2 With Five Different PID Controllers

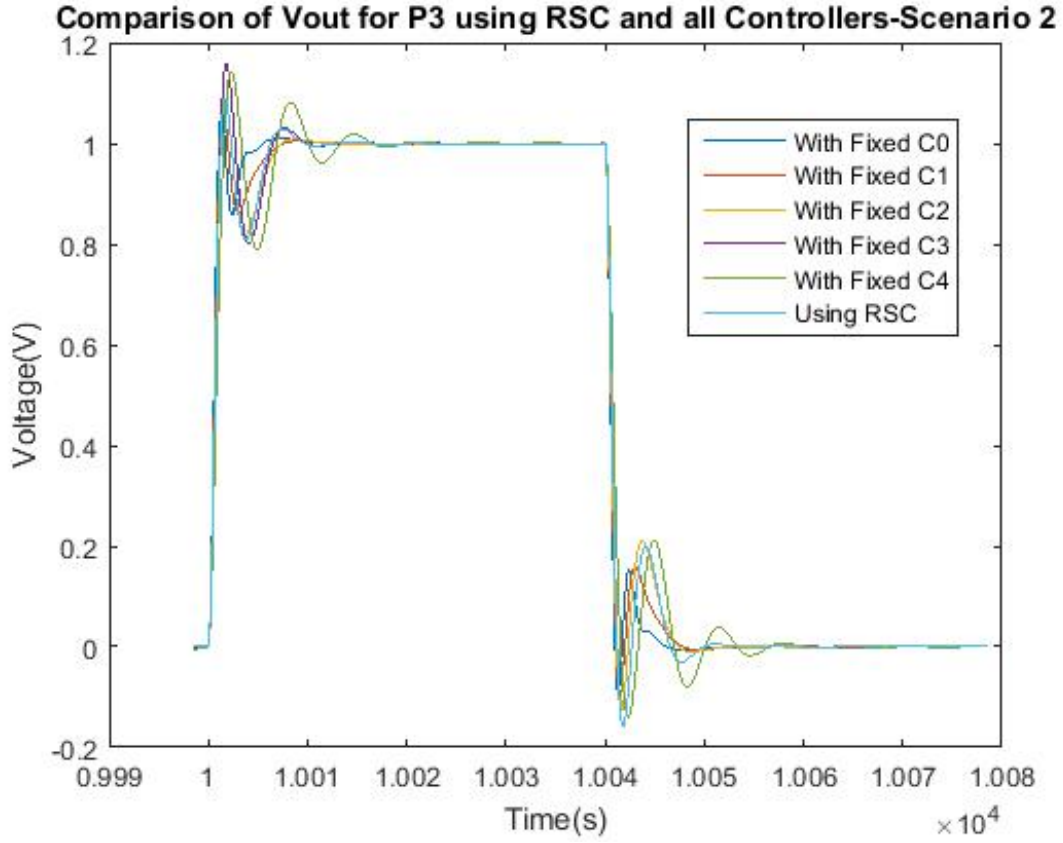| Controller	Phase Margin (deg)	Cutoff Frequency (rad/sec)
C0	74.8	3.08
C1	75.7	2.45
C2	75.7	2.00
C3	73.1	1.79
C4	69.6	1.41
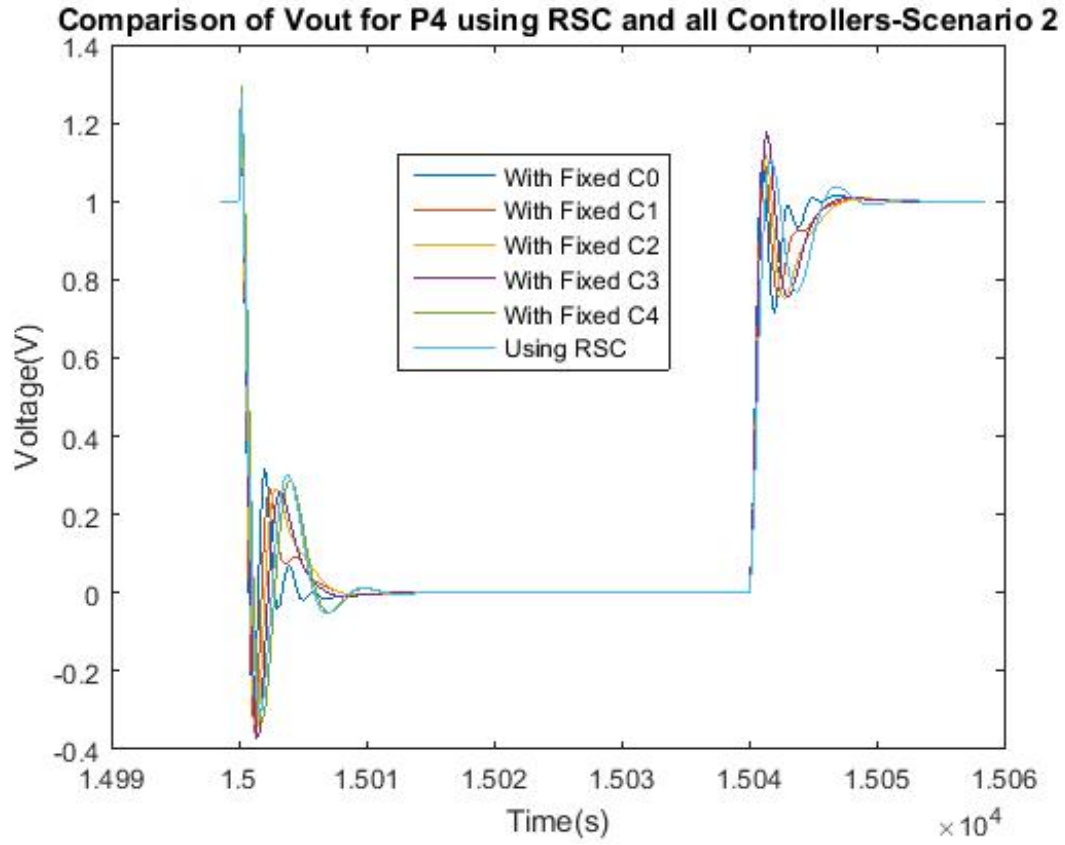
Figure 39. Comparison of the Voltage at the Output of Plant P4 for Scenario 2 Using all the Fixed Controllers versus RSC

6.4 Effects of Disturbances at the Plant Input

The effect of disturbances at the plant input is also considered in this study. The purpose of this analysis is to observe how the system chooses the controller for each plant transition in scenario 1 and scenario 2. Two type of disturbances were considered for the simulation results: the uniform distributed random signal and the sinusoidal signal.
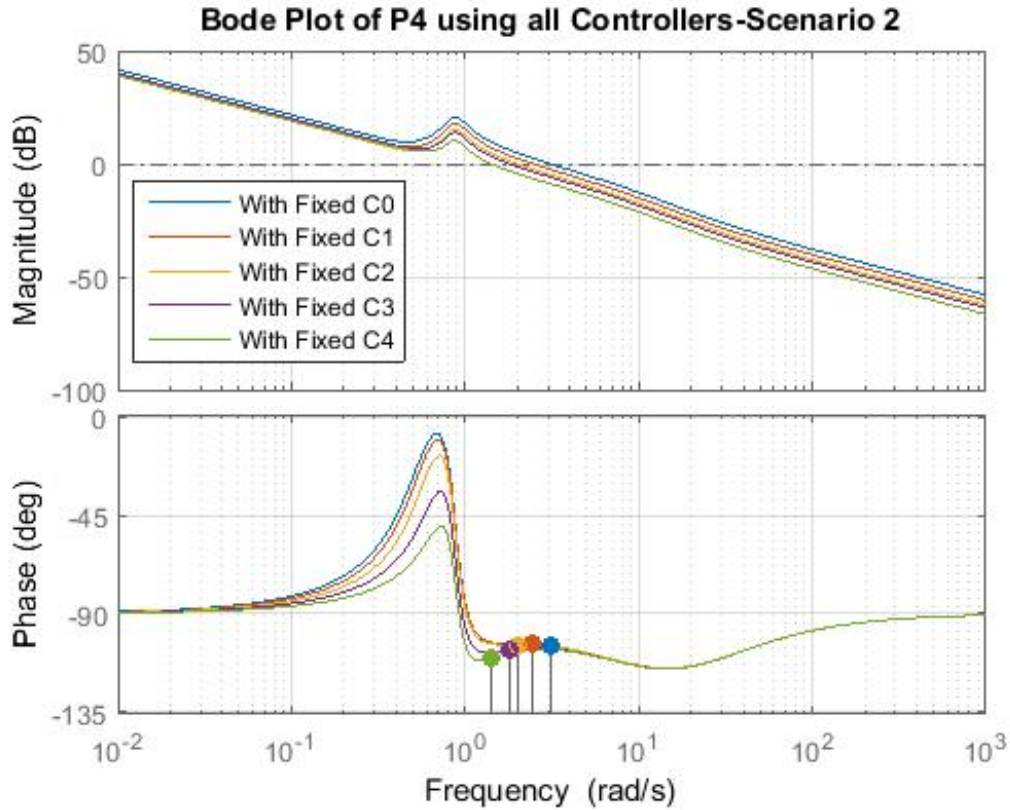
Figure 40. Comparison of the Frequency Response of Plant P4 for Scenario 2 Using all the Fixed Controllers

6.4.1   Uniform Distributed Random Signal

We studied the effects of the disturbances by applying a uniform distributed random signal at the plant input. For values between $\pm 1 \times 10^{-6}$ to $\pm 1 \times 10^{-1}$, we could not observe any change in the selection of optimal controllers using the robust stability condition. However, when we apply a value of ± 1, almost all the optimal controllers are selected except after 1.14×10^4 seconds as shown in Fig. 41. A similar behavior happens when a bigger disturbance is applied. Nevertheless, it is important to mention that to be able to observe a change in the system, a tremendous amount
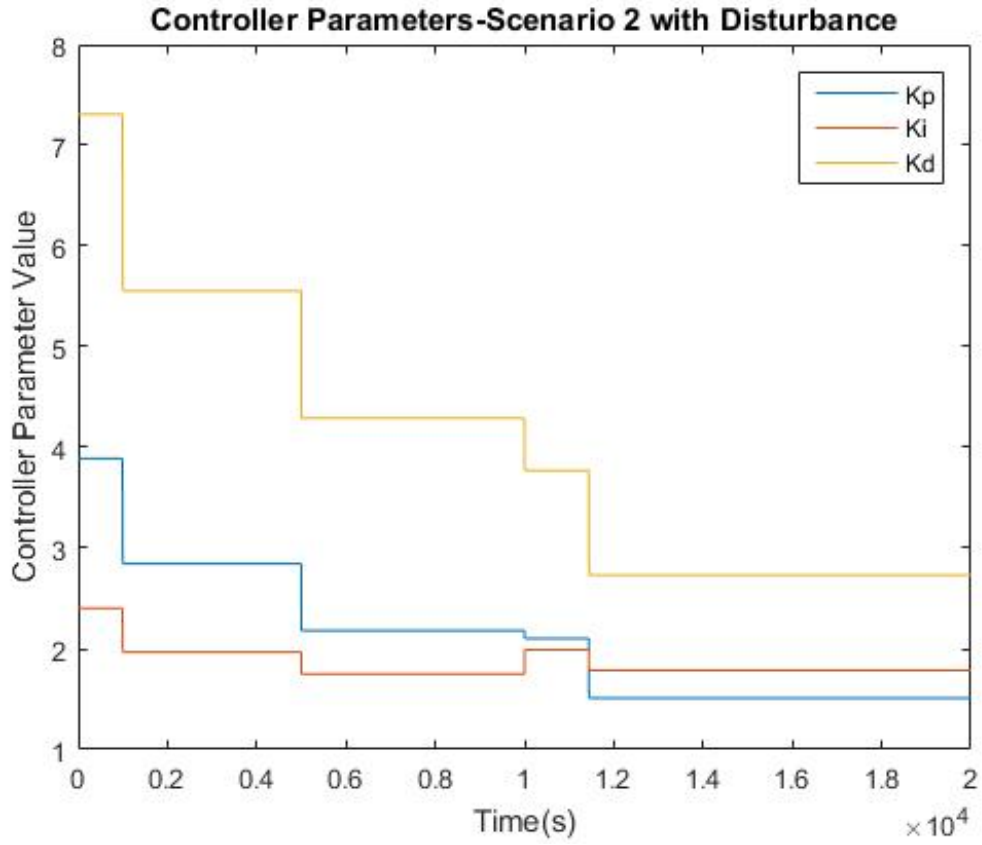
Figure 41. Controller Parameters in Scenario 2 with Disturbances

of disturbance would need to be applied which makes the system unstable as shown in Fig. 42.

Fig. 42 displays the voltage at the output when the system transitions to plant $P3$ and it has a disturbance of ±1 within the uniformly distributed random signal at the plant input. This huge disturbance was needed in order to observe a change in the selection of the optimal controller using robust stability condition that was not the correct one. For comparison purposes, we plotted the response with the controller chosen using RSC versus the response of the controller that should have been selected. With the correct controller, the response of the system has a slightly higher peak than
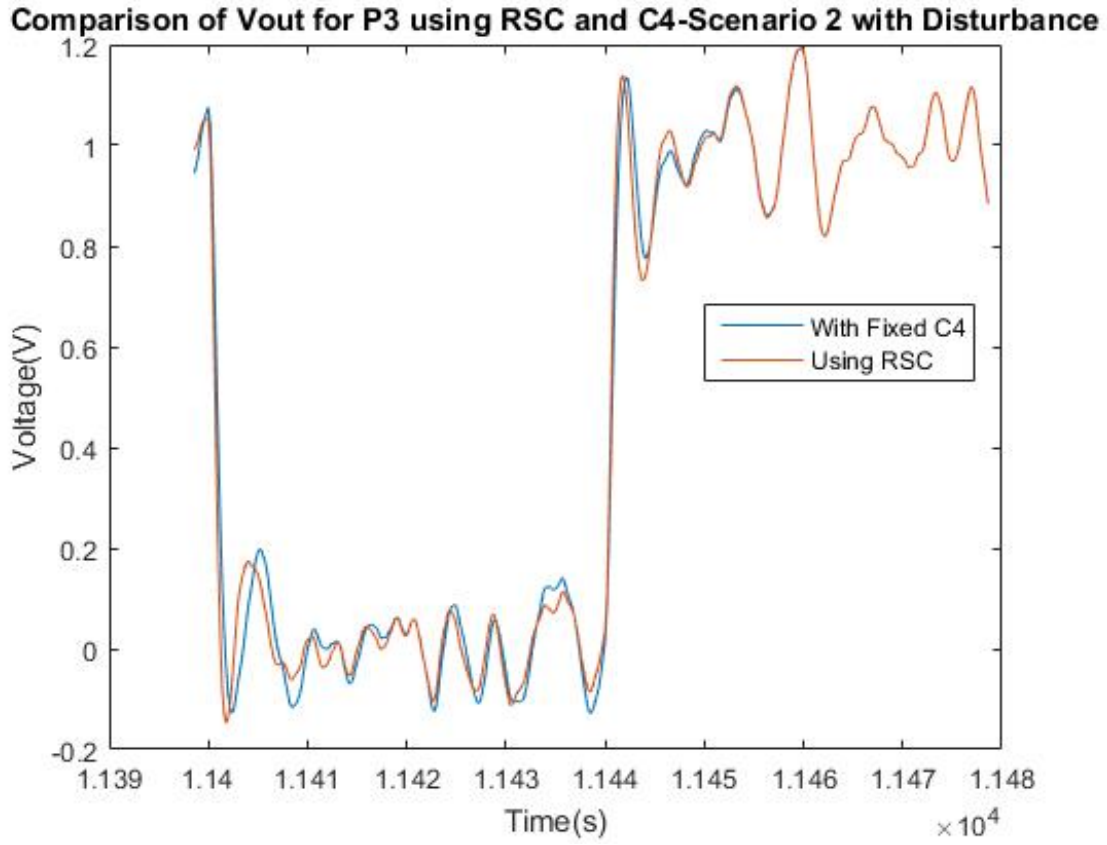
Figure 42. Voltage at the Output Using RSC vs C4 in Scenario 2 with Disturbances

with the controller chosen by RSC. However, the difference is not so significant and more important, the system is completely unstable due to the amount of disturbance which makes the study of this amount of disturbance probably meaningless.

6.4.2 Sinusoidal Signal

We also studied the effect of disturbances under a sinusoidal signal. In scenario 1, the frequency chosen was nearby the cutoff frequency of the system which was kept to $1.19rad/sec$ while the amplitude was increased gradually from -1×10^{-6} to 1. When the amplitude of the sinusoidal noise was between -1×10^{-6} and -1×10^{-1}
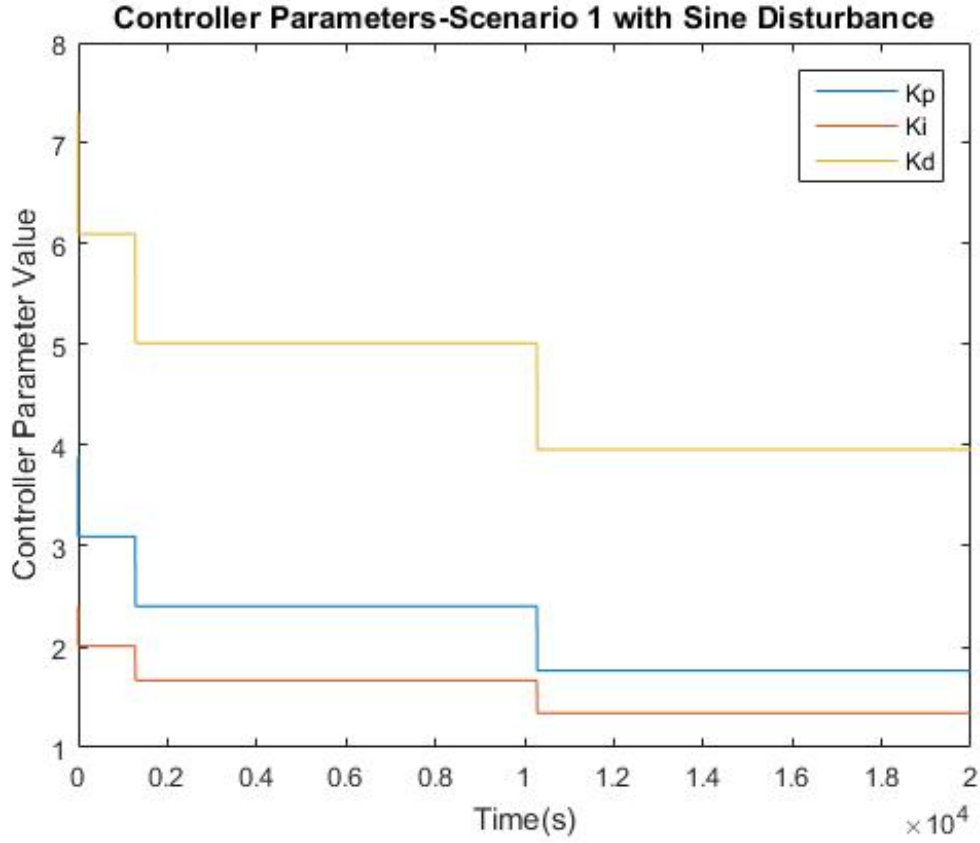
Figure 43. Controller Parameters in Scenario 1 with Sinusoidal Disturbances

no change was observed in the proper selection of the optimal controller using robust stability condition. For an amplitude of -1×10^{-1} there is no change in the controller selection; however, the controlled output presented visible oscillations. Only when the amplitude increased to 1 there is a change in the proper selection of controllers as shown in Fig. 43. The controller selected at around 1250 seconds was controller C3; however, the controller selected should have been controller C1 or C2 from time $t = 1000sec$ to $t = 5000sec$. Also, at around 1.0285×10^4 seconds the controller selected should have been C3; however, controller C4 was chosen instead.

For comparison purposes, we have plotted the controlled output when the system
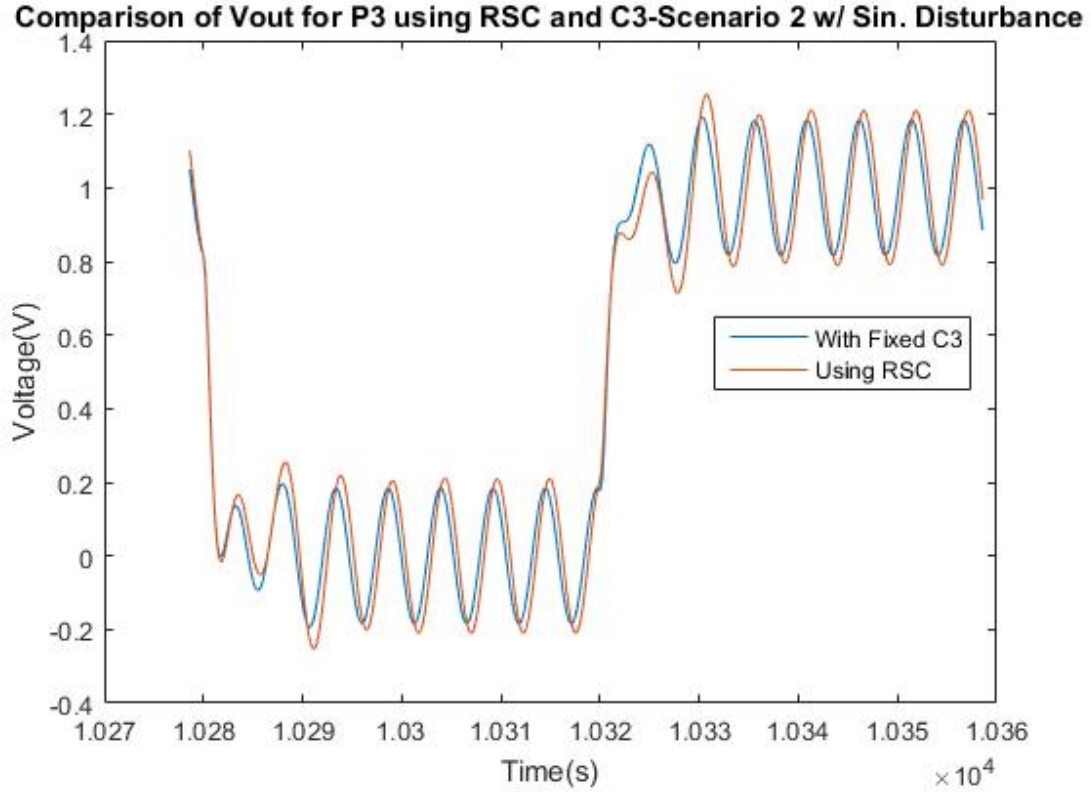
Figure 44. Controller Parameters in Scenario 1 with Sinusoidal Disturbances

selected controller C4 using robust stability condition versus controller C3 in Fig. 44. When controller C4 is selected, a higher overshoot is depicted in the controlled output than using the fixed controller C3. However, the difference is not so significant. Additionally, this analysis may not me considerably meaningful since we had to increase the amplitude of the noise signal high enough to be able to see a change in the proper selection of controllers which unavoidable makes the system unstable.

A sinusoidal disturbance was also introduced at the plant input in scenario 2. The frequency of the sinusoidal signal was kept at $1 rad/sec$ while the amplitude of the signal was gradually increased. For amplitudes from 1×10^{-6} to 1×10^{-3} there was no change in the proper selection of controllers. When the amplitude was increased to

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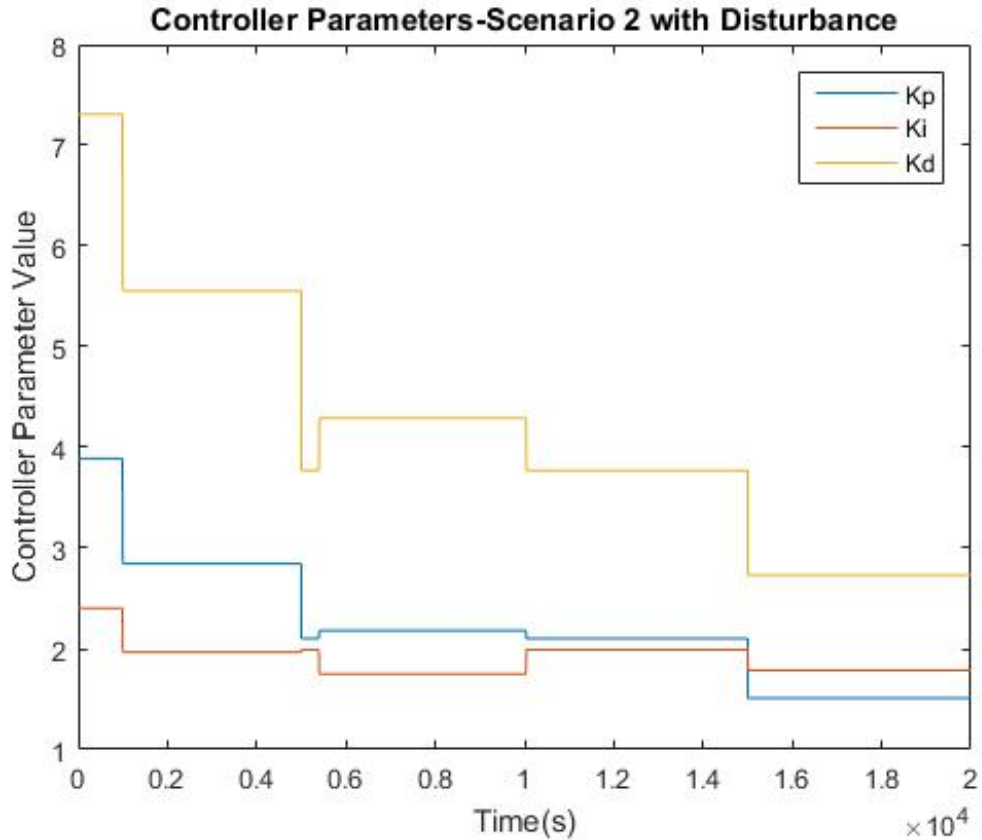
Figure 45. Controller Parameters in Scenario 2 with Sinusoidal Disturbances

1×10^{-2} still no change took effect, but little oscillations were visible at the controlled output. Only when the amplitude was increased to 1×10^{-2} a change was observed in the controller parameters using the robust stability condition. The change is observed at time $t = 5000$ seconds as shown in Fig. 45. The controller chosen was C3 at the beginning of the transition, but after than 400 seconds the corresponding controller (C2) for that plant is selected.

Fig. 46 shows the voltage at the output during the transition time where the optimal controller is not selected (at around 5000 seconds). The response makes a comparison between the output if we kept controller C3 fixed versus the controller

Comparison of Vout for P2 using RSC and C3-Scenario 2 w/ Sin. Disturbance
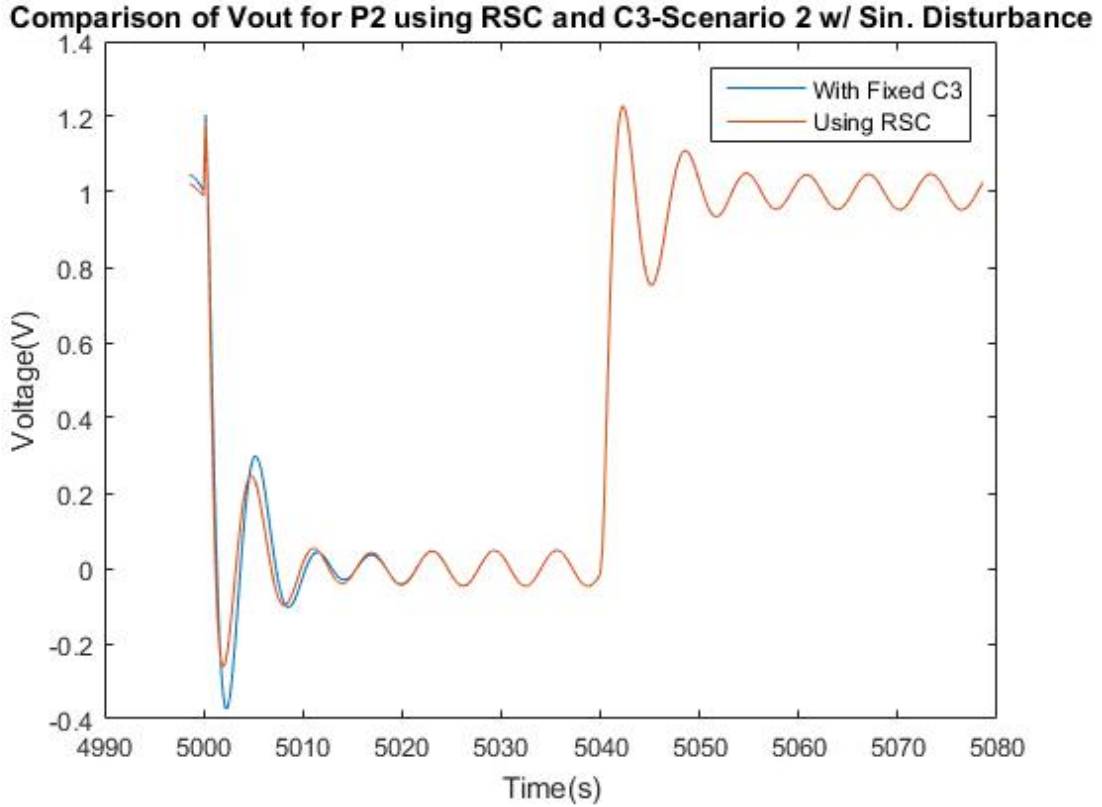
Figure 46. Voltage at the Output Using RSC vs C3 in Scenario 2 with Sinusoidal Disturbances

selected using robust stability condition. Although the fixed controller reaches a higher overshoot, the difference is not too remarkable. Additionally, since the required amplitude to be able to observe a change in the proper selection of controllers is peculiarly high, this analysis might not be so meaningful because the system would be unavoidably unstable.

Chapter 7

SWITCHING CONTROLLER

The new approach given to the adaptation of the buck converter is by using the robust stability condition to switch the controller. The PID controller has been designed using the frequency loop shaping technique together with a low-pass filter. The controller was discretized using "Tustin" and a sampling time of 0.2 seconds.

7.1   Switching Logic

The switching logic of the system is a follows:

- A function determines the controller parameters ($params$), the current robust stability condition ($CurrentRSC$) and an index associated to the controller parameters (Ind). This calculation is based on the previous calculated robust stability condition (RSC), the five different controllers ($C1$, $C2$, $C3$, $C4$ and $C5$), a hysteresis value (h) and the current index ($currentInd$).
- The function determines the current temporary robust stability condition ($CurrentRSCTemp$) which will be the robust stability condition of the current index ($RSC(currentInd)$).
- Then, it calculates the minimum robust stability condition ($minRSC$) and minimum index ($minInd$) by evaluating the minimum of the previous robust stability condition ($min(RSC)$).
- It evaluates if the current temporary robust stability condition ($CurrentRSCTemp$) is greater than the minimum robust stability condi-

tion ($minRSC$) multiplied by the hysteresis value plus one ($h + 1$). This is executed so that the switching does not occur unless the $CurrentRSCTemp$ surpasses a threshold value. That way we minimize the number of switching, especially at the transient response.

- If the previous value is satisfied, then the selected index (Ind) will correspond to the minimum index ($minInd$). Additionally, the current robust stability condition ($CurrentRSC$) will correspond to the minimum robust stability condition ($minRSC$).

- If the previous condition is not satisfied, then the selected index (Ind) will be the current index ($currentInd$). Also, the current robust stability condition ($CurrentRSC$) will be the current temporary robust stability condition ($CurrentRSCTemp$).

- The switching will take place based on the index value (Ind). Thus, if the index (Ind) equals to 1, then the parameters ($params$) selected will correspond to controller 1 ($C1$). If the index (Ind) equals to 2, then the parameters ($params$) selected will correspond to controller 2 ($C2$). Similarly, the same logic will be applied for the rest of the controllers.

Fig. 47 shows the result of the adaptation for the robust stability condition when the plant changes its dynamics at times 1000, 5000, 10000 and 15000 seconds for scenario 1.

Since these plants are not so different from each other, it is difficult to adapt the system properly. We can observe the following performance:

- For times from $t = 0$ to $t \leq 1000$ seconds, the minimum robust stability condition corresponds to controller 0 as it was expected.

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Figure 47. Robust Stability Condition for all the Controllers in Scenario 1

- For times from $t > 1000$ and $t \le 5000$ seconds, the minimum robust stability condition corresponds to controller 2; however, it should have been the RSC for controller 1.

- For times from $t > 5000$ and $t \le 10000$ seconds, the minimum robust stability condition corresponds to controller 2 as it was expected.

- For times from $t > 10000$ and $t \le 15000$ seconds, the minimum robust stability condition calculated corresponds to controller 2; however, it should have been the RSC of controller 3.

- For times from $t > 15000$ seconds, the minimum robust stability condition

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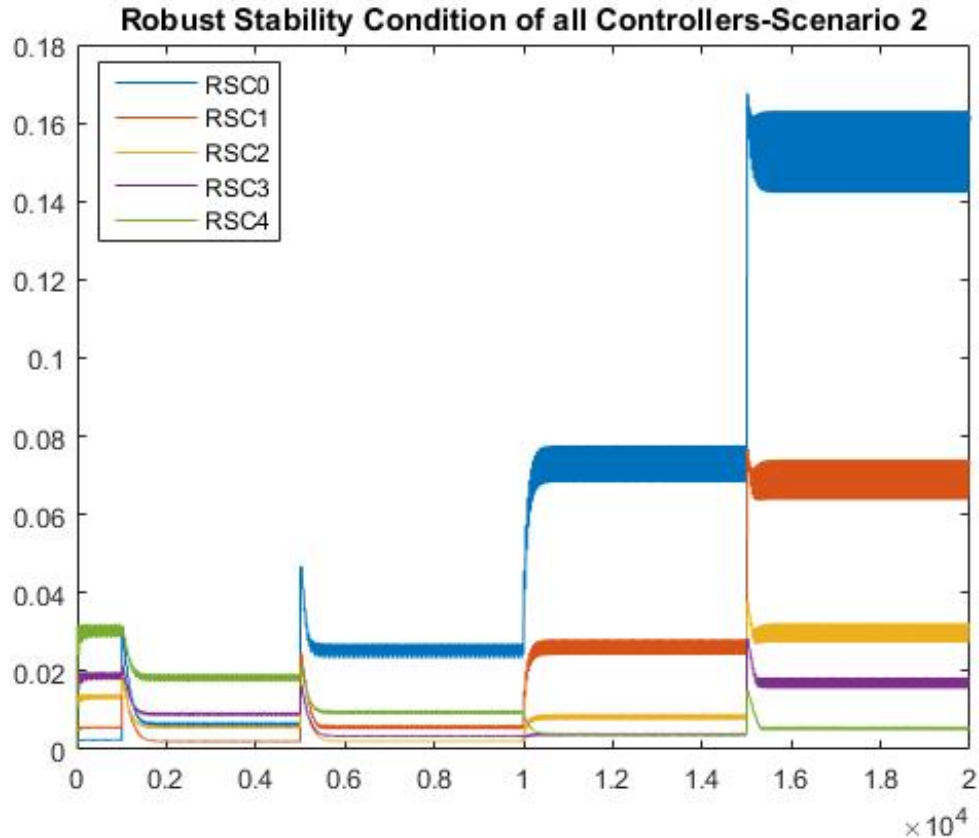
Figure 48. Robust Stability Condition for all the Controllers in Scenario 2

calculated corresponds to controller 3; however, it should have been the RSC of controller 4.

Fig. 48 shows the result of the robust stability condition for scenario 2. Similar to scenario 1, the plant changes its parameters at times 1000, 5000, 1000 and 15000 seconds.

We can highlight the following results from the robust stability condition calculation:

- For times from $t = 0$ to $t \leq 1000$ seconds, the minimum robust stability condition calculated corresponds to controller 0 as it was expected.
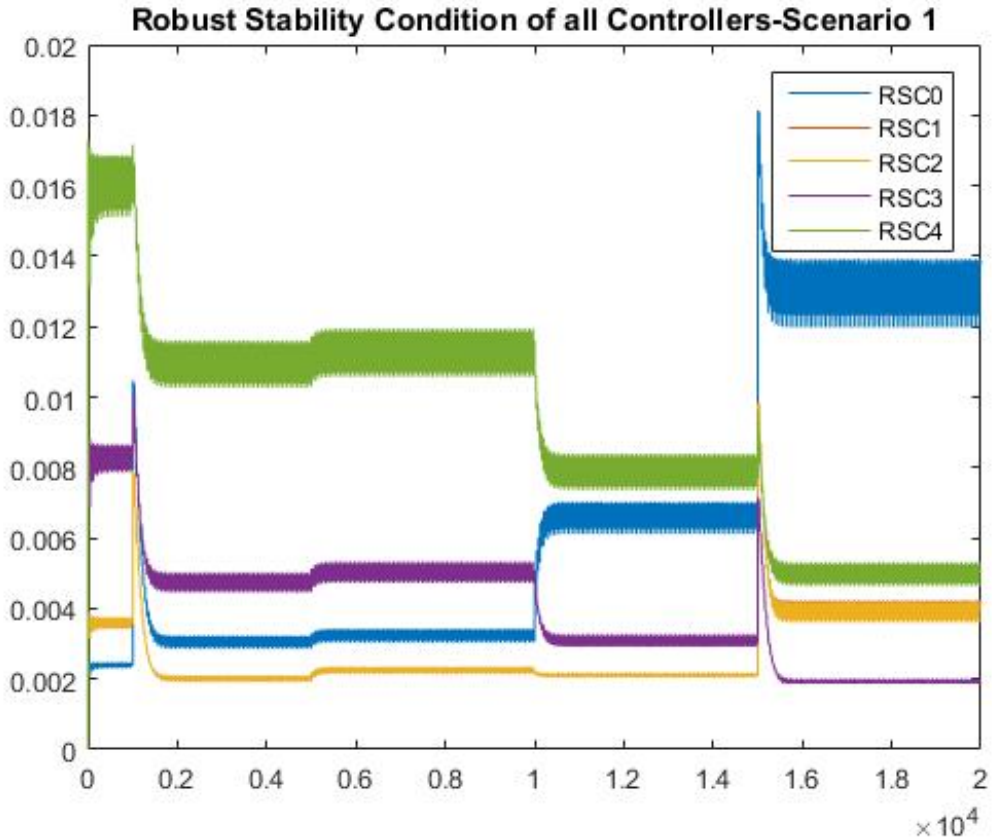
- For times from $t > 1000$ and $t \le 5000$ seconds, although the minimum robust stability condition for controllers 1 and 2 are very close, the lowest value is obtained for controller 1. This is consistent to the results that we were expecting.

- For times from $t > 5000$ and $t \le 10000$ seconds, the minimum value for the robust stability condition is obtained for controller 2 as expected.

- For times from $t > 10000$ and $t \le 15000$ seconds, the minimum robust stability condition are between controllers 2 and 3, but the lowest value corresponds to controller 3 as it was expected.

- For times from $t > 15000$ seconds, we can clearly observe that the minimum robust stability condition corresponds to controller 4 as we were expecting.

For scenario 2, the correct controllers were selected for each of the plants that took place at different times. This differs from scenario 1 where random controllers were chosen for specific plants. One of the main reasons why this is happening is due to the fact that the frequency response in scenario 1 are not very significant different as in scenario 2.

Chapter 8

CONCLUSION

We have shown a simulation of the on-line system identification process for the buck converter. We began our analysis by obtaining the nominal plant transfer function of the buck converter. This allowed us to determine the PRBS signal required to properly identify the system.

The system identification process was performed using a recursive least squares algorithm. The plant was scaled down by a factor of 10^6 to simplify computations in the Simulink model. The estimation error and parameter error were generated to demonstrate that the system was converging to its true parameters. The estimation error shows an absolute value of approximately 1×10^{-5} in less that 10ms. The parameter error was initialized to have different values which were off from the true parameters. This allowed us to observe when the regressor was operating on the system and to determine if the plant was converging. All the parameters were finally converging at a value which is less that $100\mu s$.

After performing the on-line system identification for the buck converter, three different techniques were used to design a PID controller: PID+filter using gain and phase margin specifications, pole-zero cancellation, and a PID+filter using the Frequency Loop Shaping technique. Pole-zero cancellation and the design using gain and phase margin specifications are relatively easy to compute. After a quick manipulation of the system parameters, we could obtain the gains for the proportional, integral and derivative actions. Frequency loop shaping, however, requires the solution

of an optimization problem in which we try to minimize the frequency response against a target loop in an $L\infty$ sense.

All the controllers met the parameter specifications required by the system. However, the frequency loop shaping controller provides a better frequency response compared to the other controllers. When the compensated loop was analyzed, we observed that the response given by all controllers is very similar at the cutoff frequency. However, the FLS controller provides a higher gain at lower frequencies. Additionally, the step response and disturbance rejection are also better when a FLS controller was implemented. The step response shows that the system stabilizes faster compared to the other controllers. We could also observe a little overshoot when the FLS controller was implemented; however; this feature can be improved by the introduction of a pre-filter in the controlled loop.

Additionally, the disturbance rejection shows that the system rejects disturbances at the plant input when a FLS was implemented compared to the other two controllers. This is a desired characteristic since we would like our system to act fast in the presence of any disturbance at the plant input.

Moreover, since we showed that the FLS controller provides better responses, we should point out that we could not obtain feasible values for resistors and capacitors consistent with the type 3 controller. Therefore, using that structure would require an optimization problem to be solved so that practical values could be found for theses elements.

Another alternative would be to implement a direct estimation of the controller parameters along the lines of [35], as it has been shown in this study. We performed first a full adaptation by identifying the parameters of the system and design the controller after the about 2000 seconds. However, by using the robust stability

condition, the optimal controller is selected after about 500 seconds which makes it more appropriate compared to the performance of full adaptation.

Two different scenarios were evaluated that corresponded to plants that were degrading over time. The first scenario considered: 1) The original plant, 2) A plant that deteriorated by 10% in the inductor while the capacitor remained the same, 3) A plant that deteriorated by 10% in the capacitor while the inductor remained the same, 4) A plant where both the capacitor and the inductor deteriorated by 10% and 5) A plant where both the capacitor and the inductor deteriorated by 15%. However, their frequency response looks very similar to each other. Therefore, even when robust stability condition was evaluated, the optimal controller was not selected at each transition time. This does not necessarily mean that the system did not work properly because more than one controller could be satisfying the design requirements. To observe a significance difference in the performance of the adaptation using the robust stability condition, we evaluated a second scenario.

Scenario two consisted of the following plants: 1) The original plant, 2) A plant that degraded equally in both the capacitor and inductor by 10%, 3) A plant that deteriorated equally in both the capacitor and inductor by 20%, 4) A plant that deteriorated in the capacitor and inductor by 30% and 5) A plant that deteriorated equally in the capacitor and inductor values by 40%. The frequency response of the above plants was more noticeable which allowed a proper adaptation of the system by using the robust stability condition (RSC). Once the RSC was calculated, the optimal controller was selected at each plant transition.

Finally, the effects of disturbances were studied in both scenarios. We introduced a uniformly distributed random signal at the plant input. For significant low disturbance values ($\pm 1 \times 10^{-6}$ to $\pm 1 \times 10^{-1}$) no changes are produced in the controller selection based

on the robust stability condition in both scenarios. However, when the disturbance is increased to ±1 or higher, the optimal controller was not always selected for all the plant transition. However, the system will be completely unstable which will probably make the use of the robust stability condition meaningless for the selection of controllers. A similar result was also obtained when we introduced a sinusoidal signal as disturbance at the plant input.

Chapter 9

FUTURE WORK

A new set of experiments is required with the evaluation board to better identify the system. The result of this experiment should be consistent with the nominal plant. Therefore, we should ensure that the system is not hitting saturation levels for a long period of time since this makes the system highly non-linear. Identifying non-linear systems becomes a more complex calculation.

Additionally, after reviewing the results obtained from the controller design step, we may suggest different solutions for the implementation of the Frequency Loop Shaping controller. First, if we want to implement a type 3 controller, an optimization problem is required to obtain a feasible values for the resistors and capacitors.

Another alternative would be to implement a digital controller for the buck converter. This may allow us to obtain feasible controllers for the physical system. However, this will also require a study of the quantization levels. The effects of quantization levels on buck converters have been studied from in a simulation point of view [32]. In this study, the authors presented the advantages and disadvantages of using a digital controller on a buck converter. The simulation model analyses the effect of quantization levels in the whole system which involves the compensation network, the error voltage and the pulse width modulator. A type 2 compensator was used for this study and the quantization blocks were limited to four, eight, twelve, sixteen and thirty two-bit representation. As expected, when the number of bits increased, the desired response was achieved. It was also shown that when the number of bits equals 12, the model almost approximated the unquantized system.

Additionally, either if we decide to implement an analog or digital controller, a deeper study of switching controller is necessary. In this scenario, we would have a limited number of controllers. Therefore, we would need to determine which controller is more appropriate to be implemented in the buck converter at a specific time. The proper selection of a specific controller will be assessed by evaluating a metric. If the new identified plant satisfies the metric, then the loop will select a new controller. In the same vein, recent studies show that adaptive switching controller has been proposed as an alternative to control plants instead of the conventional adaptive scenario [5]. The idea is to have a supervisor controller that evaluates the finite candidate controllers by using recorded data of the plant. The advantage of this study is that the performance of each independent controller can be predicted; therefore, it allows to determine the best controller at each specific time. Additionally, the algorithm selects the waiting time between switches. However, we would need to verify if this study will have practical implementation on the buck converter.

For the adaptation, we would also like to study one more variability. The capacitors have a voltage dependence which is nonlinear. They are usually specified in the data-sheets in terms linear and quadratic voltage coefficients. Therefore, as a future work, we would like to analyze these cases, especially because they become particularly important during transient load times.

Additionally, we would like to test the results of our simulation on a physical system either using low cost equipment such as the Arduino boards that has been used in a myriad of applications [31] or by implementing more sophisticated electronic boards such as National Instruments (NI) Data Acquisition Boards together with the Labview software. This will allow us to demonstrate the proper operation of

the system in closed loop. These experiments should produce similar results to the simulations presented in this study.

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