Development of Silver-Free Silicon Photovoltaic Solar Cells

with All-Aluminum Electrodes

by

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ABSTRACT

To date, the most popular and dominant material for commercial solar cells is crystalline silicon (or wafer-Si). It has the highest cell efficiency and cell lifetime out of all commercial solar cells. Although the potential of crystalline-Si solar cells in supplying energy demands is enormous, their future growth will likely be constrained by two major bottlenecks. The first is the high electricity input to produce crystalline-Si solar cells and modules, and the second is the limited supply of silver (Ag) reserves. These bottlenecks prevent crystalline-Si solar cells from reaching terawatt-scale deployment, which means the electricity produced by crystalline-Si solar cells would never fulfill a noticeable portion of our energy demands in the future. In order to solve the issue of Ag limitation for the front metal grid, aluminum (Al) electroplating has been developed as an alternative metallization technique in the fabrication of crystalline-Si solar cells. The plating is carried out in a near-room-temperature ionic liquid by means of galvanostatic electrolysis. It has been found that dense, adherent Al deposits with resistivity in the high 10^{-6} Ω-cm range can be reproducibly obtained directly on Si substrates and nickel seed layers. An all-Al Si solar cell, with an electroplated Al front electrode and a screen-printed Al back electrode, has been successfully demonstrated based on commercial p-type monocrystalline-Si solar cells, and its efficiency is approaching 15%. Further optimization of the cell fabrication process, in particular a suitable patterning technique for the front silicon nitride layer, is expected to increase the efficiency of the cell to ~18%. This shows the potential of Al electroplating in cell metallization is promising and replacing Ag with Al as the front finger electrode is feasible.

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CHAPTER 1 INTRODUCTION

1.1 Motivation

Over the past few decades, the fossil fuels, coming from coal, natural gas and oil, have been the dominant resource for world energy supply. In the statistical review published by British Petroleum, the consumption of the fossil fuels in 2014 continued to increase despite the slow growth in energy demand [1]. Global oil consumption grew 0.8 percent in 2014, while natural gas and coal consumption each increased by 0.4 percent. However, this situation could change in the coming decades because fossil fuels not only are limited in supply but also cause detrimental impact on the environment like climate change through the emission of global warming gases. Therefore, the world has been searching for alternative energy resources, which can substitute the fossil fuels in the near future. Nuclear energy, using nuclear fission to release energy, has been considered as a promising substitute for the fossil fuels due to its lower cost and clean production of electricity. However, nuclear energy raises concerns about safety and radioactive waste disposal. In addition, it takes a long time to build a nuclear plant, making it less feasible for it to fulfill the rising demand for energy. A more sustainable and cleaner energy source needs to be developed to reduce the global usage of fossil and nuclear energy.

With significant cost reductions in both wind and solar energy, renewable energy is growing rapidly, and record numbers of new wind and solar installations have been coming online in the United States over the past few years [2]. Among all the renewable sources, solar energy is the fastest-growing renewable generation source. Photovoltaics (PV), a form of solar energy where light is directly converted to electricity typically using a semiconductor material, is one of the most promising candidates for sustainable energy source because sunlight is free, essentially unlimited,

and available almost in any part of the world. The impressive growth of global PV market can be clearly seen by tracking the evolution of the global cumulative installed PV capacity, as shown in Figure 1.1 [3]. At the end of 2014, the capacity almost reached 180 GW_p, and it was anticipated that solar PV would continue growing and hit the target of 200 GW_p installations over the next three years.

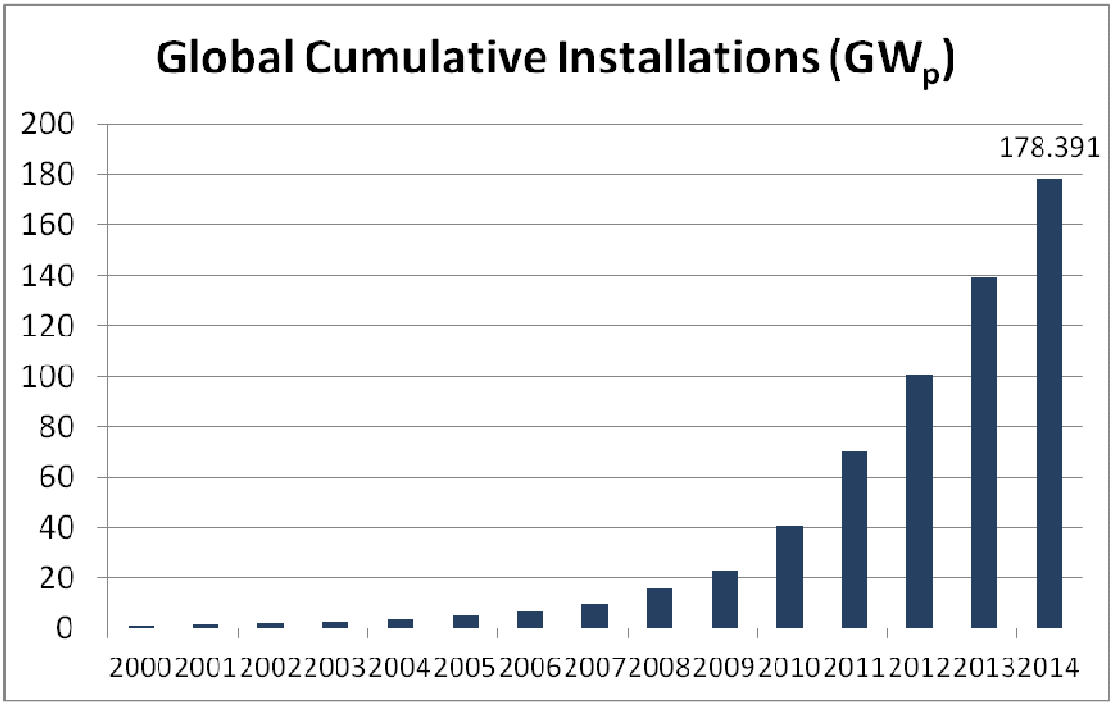

Figure 1.1 Global cumulative installed PV capacity from 2000 to 2014.

PV provides a number of advantages over fossil energy, nuclear energy, and even other renewable energy sources:

1) PV systems do not require fuel, which eliminates the risk associated with fluctuating fuel costs, and this advantage is shared by some other renewable energy sources. There is also no requirement for the disposal of fuel. The economic and safety risks associated with nuclear fuel disposal are still under dispute.

2) The energy produced by PV systems is free of pollutants and greenhouse gas

emissions. Besides environmental issues, it should be noted that recent reports indicate hidden health care costs associated with populations living near coal fired power plants [4]. These hidden costs are not typically included in cost comparison between PV and coal.

3) PV systems are not localized in the world and can be installed and operated with a relative ease on a rooftop, so transmission and distribution costs can be significantly reduced. It is worth mentioning the electricity generated at the point of use is of more value than that generated at a remote place from which it is supplied.

4) PV systems are comprised of highly reliable, solid-state devices with low operation and maintenance (O&M) requirements. The current O&M costs for PV are a much lower percentage of the total levelized cost of energy (LCOE) when compared to other power generation technologies [5], with potential to be reduced even further with advances in module level electronics.

5) Due to improvements in fast switching power devices and inverter technology [6], integration of PV into the utility grid can now be realized in a way that significantly enhances the stability of the grid and provides added value, like power factor control and dispatchable reactive power (referred to as "ancillary services" in the utility sector) [7].

Although the costs related to PV modules and systems have dropped drastically over the last few decades, the LCOE of PV is still higher than that of fossil fuels in many places [5]. In the United States, solar PV only accounts for ~0.4% of the total energy consumed in 2014, as shown in Figure 1.2, due to a higher LCOE (~$0.125/kWh) compared to fossil fuels (≤$0.1/kWh) [2]. To make PV a truly competitive energy source to the conventional fossil fuels, it is necessary to further

reduce the costs at all levels, including material, cell, module, and system.

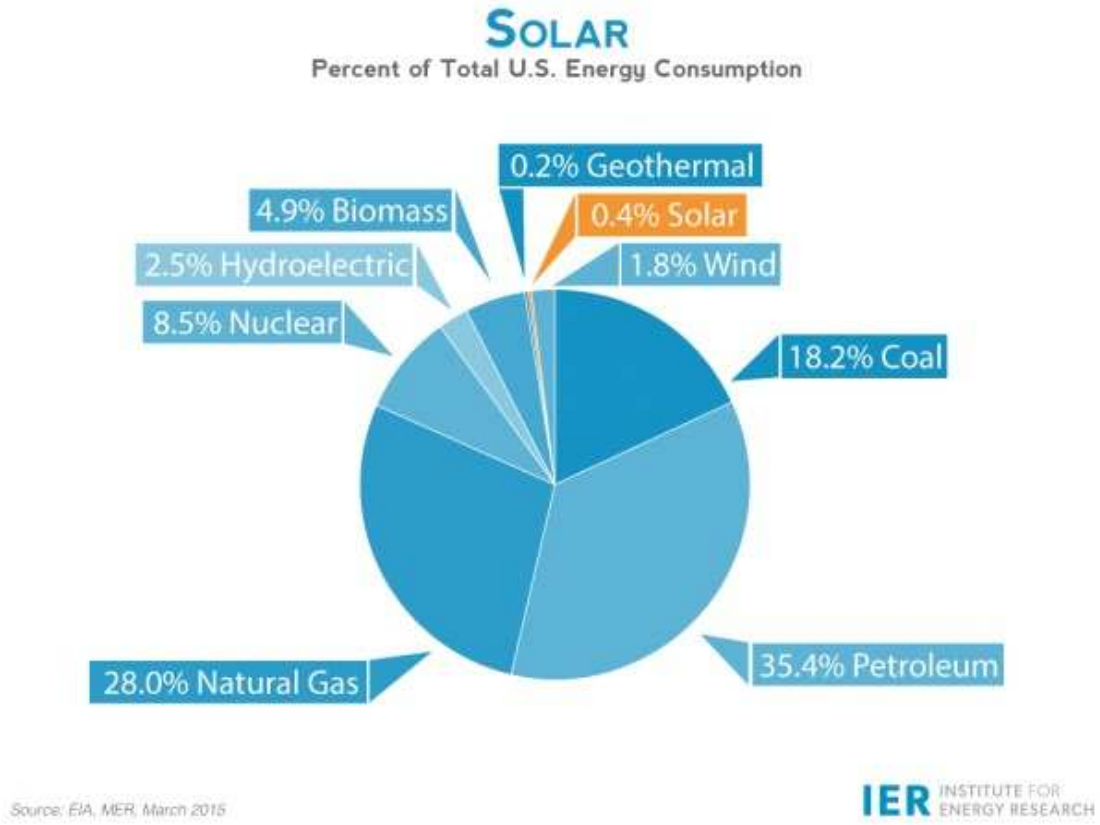

Figure 1.2 Percent of total U.S. energy consumption in 2014.

There are two obvious ways to bring down the PV module price: increase the conversion efficiency and reduce the material, cell processing and manufacturing cost. This criterion forms the overall scope and objective of my PhD research, which is using cheaper contact material and simplifying the whole process flow to fabricate solar cells with efficiency close to what commercial solar cells have achieved. The research would particularly focus on substituting the front silver (Ag) electrodes of crystalline silicon (Si) solar cells with a cheaper and Earth-abundant material such as aluminum (Al).

1.2 Overview of the Photovoltaic Technology

PV is a simple method of utilizing the energy of sun. PV energy conversion is a one-step process which converts light energy directly into electricity using PV devices (solar cells). The explanation relies on quantum theory, in which light is made up of packets of energy, called photons. Their energy depends solely on the frequency of the light, and the energy of visible photons is sufficient to excite electrons up to higher energy levels, where they are free to move. In a solar cell, there is a built-in potential which separates the excited charge carriers before they can relax, and further drives the electrical current through an external load. The effectiveness of a solar cell depends on the different selections of light absorbing materials and the connection between materials and external circuit. Solar cells are commonly connected together electrically, in series or in a series-parallel configuration, to increase the voltage and current of the interconnected ensemble. The final component is called a PV module in which these cells are encapsulated by a front glass cover and a rear cover to protect themselves from the environmental hazards.

The photovoltaic effect was first discovered by Edmund Bequerel in 1839 [8]. His experimental setup was composed of a silver chloride (AgCl) electrode and a platinum (Pt) electrode in an acidic solution. When light was shone on the AgCl electrode, he observed a voltage drop across the two electrodes. In 1883, Charles Fritts demonstrated the large area and all solid-state solar cell by depositing an extremely thin layer of gold (Au) on semiconductor selenium (Se) [9]. This early solar cell was based on Schottky barrier between semiconductor-metal interfaces, where a semitransparent layer of metal deposited on top of the semiconductor. This provided both the asymmetric electrical junction, which is necessary for photovoltaic effect, and the access of incident light to junction. In the 1950s, with the development of

good quality Si wafers, researchers begun looking into the potential application of crystalline Si in solar cells. Meanwhile, discovery of a way to fabricate p-n junction in Si was followed the development of Si electronics. The p-n junction structures showed much better rectifying and photovoltaic behavior than Schottky barrier. The first Si solar cell with a p-n junction was demonstrated by D. Chapin et al. of Bell Laboratories in 1954 [10], and the conversion efficiency was about 6%. Since then, Si, either monocrystalline or multicrystalline, has remained the foremost PV material and dominated the solar cell market, gaining from the advances of Si-based microelectronics industry.

To compete with wafer-Si technologies, thin film PV technologies were developed to lower the cost of module manufacturing by reducing the processing steps and amount of active material required to create a module, at the expense of lower efficiencies. In general, this is accomplished by depositing a thin inorganic semiconductor film, called the absorber layer, onto a substrate. The absorber normally features a direct bandgap in the range of 1–1.75 eV, allowing for strong optical absorption of the visible and near-infrared wavelengths available from the solar spectrum. Various thin film material systems have been utilized by the industry, and the most successful absorber materials have been hydrogenated amorphous silicon (a-Si:H), cadmium telluride (CdTe), and copper indium gallium diselenide (CIGS). However, for the CdTe and CIGS systems, limited availability and increasing prices of Te and In may be the obstacles to their future development according to experts working in the PV industry [11].

While thin films were developed to provide an alternative with cheaper cost but lower efficiency to wafer-Si, multijunction III-V solar cells, also known as tandem cells, were developed to push the boundary of solar cell efficiencies. Efficiencies as

high as 46% have been achieved under concentrated light and 38.8% under one sun [12] with an incredibly high cost. This higher cost is due to both the materials requirements (e.g., substrates) and the expensive, low throughput epitaxial crystal growth methods (e.g., metal-organic chemical vapor deposition, molecular beam epitaxy) required to create these devices, which is why concentration of light is normally used to reduce the amount of material needed [13]. The efficiency boost primarily comes from the use of multiple p-n junctions stacked on top of each other, each with a bandgap engineered to absorb light with a certain range of wavelengths.

In addition to wafer-Si, thin film and multijunction III-V technologies, other materials and device concepts have been developed at the laboratory scale with little to no commercial impact. Perhaps the most notable technology in this category would be organic PV, which is based on the use of organic semiconductor materials. Dye-sensitized solar cells are another technology of interest to the PV community. More recently, perovskite materials have emerged as a potentially attractive technology due to the demonstration of a non-stabilized cell efficiency of 21% by EPFL [14]. Concerns over both the short-term and long-term stability of organic PV, dye-sensitized solar cells, and perovskite cells are current market barriers for these technologies.

Other emerging PV technologies aim to break the well-known Shockley-Queisser limit by exploiting quantum confinement or by using some other novel energy conversion process (e.g., hot carrier solar cells, multiple exciton generation, intermediate band solar cells). Despite the advanced and innovative concepts, the majority of these technologies are still at the very early stages of the R&D cycle.

Figure 1.3 shows the progression of record laboratory efficiencies for current

solar cell technologies between 1976 and 2015 [14], which is maintained and updated by NREL. It can be seen that current commercially available solar cell technologies include 1) wafer-Si solar cells, either monocrystalline or multicrystalline, 2) CdTe cells, 3) thin-film Si cells, either amorphous or microcrystalline, 4) CIGS cells, and 5) III-V compound semiconductor multijunction tandem cells. On the other hand, currently developing solar cell technologies include 1) dye-sensitized solar cells, 2) perovskite cells, 3) organic solar cells, 4) quantum dot cells, and 5) thin film copper zinc tin selenide sulfide (CZTSS) cells. In general, there are two major directions for the development of current solar cell technologies. The first one is using more cost-effective ways to produce PV devices and materials, which includes photoelectrochemical junctions and alternative materials such as polycrystalline Si, amorphous Si, and other thin film and organic materials. The second one is improving device efficiency with tandem and other multiple bandgaps structures.

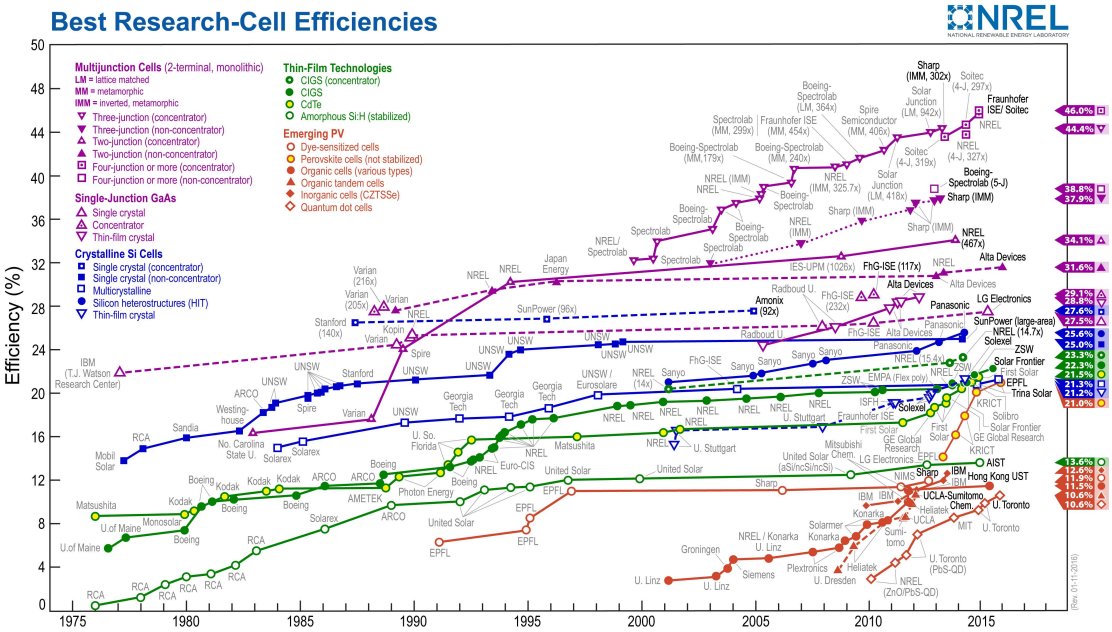

Figure 1.3 Progression of record laboratory efficiencies for current solar cell technologies between 1976 and 2015.

1.3 Chapter Organization

This chapter provides an introduction to the current PV technology, from why people need to develop renewable energy sources, what advantages the PV technology has compared to the conventional fossil energy to what issues the current PV technology has to prevent it from becoming the mainstream energy source. Developing an approach to solve the cost issue is the main focus and objective of my thesis work. Moreover, a brief overview of the current PV technology is introduced, in which the unique features of different material systems are discussed.

In Chapter 2, the basic operation and fundamental physics of solar cells are provided, including the typical structure of a solar cell, characteristics of a solar cell, and loss mechanisms in a solar cell. Since the wafer-Si solar cell is the most common solar cell commercially available today, it is used as an example to show the cell structure, in which the functions of different layers are discussed. Several important parameters which are used to characterize solar cells are defined and discussed. Various loss mechanisms in solar cells, including optical losses, resistive losses, and recombination losses, are discussed to explain why there is a discrepancy between the theoretical and the actual efficiency.

Chapter 3 provides a brief overview of crystalline-Si solar cells, which dominate the global solar cell market with ~90% of market share. Although the potential of crystalline-Si solar cells in supplying energy demands is enormous, their future growth will likely be constrained by two fundamental roadblocks. The first one is high energy input for the production of crystalline-Si modules. A much more energy-efficient process flow needs to be developed in order to solve this bottleneck. The second one is the scarcity of Ag reserve for the front metal grid. An alternative metallization technique with a low-cost and Earth-abundant metal to substitute for

screen-printed Ag has to be investigated to address this issue, which is the motivaion behind the development of room-temperature Al electroplating on Si substrates in this work.

In Chapter 4, we report the development of Al electroplating on Si substrates in a near-room-temperature ionic liquid for the metallization of crystalline-Si solar cells. The electrolyte is prepared by mixing anhydrous aluminum chloride and 1-ethyl-3-methylimidazolium tetrachloroaluminate. The plating is carried out by means of galvanostatic electrolysis. The structural and compositional properties of the Al deposits are characterized, and the sheet resistance of the deposits is investigated to reveal the effects of pre-bake conditions, deposition temperature, and post-deposition annealing conditions. It has been found that dense, adherent Al deposits with resistivity in the high 10^{-6} Ω-cm range can be reproducibly obtained directly on Si substrates.

In Chapter 5, the integration of Al electroplating in the metallization process of commercial p-type monocrystalline-Si solar cells is reported. The design of the front grid pattern for our all-Al solar cells is first introduced, in which the design rules and pattern optimization are elucidated. The process flow, cell performance, and issues caused by the fabrication method are discussed. An all-Al Si solar cell, with an electroplated Al front electrode and a screen-printed Al back electrode, has been successfully demonstrated and its performance has been characterized. The effect of annealing for the front Al/Ni electrode in air at different temperatures on cell performance has been investigated.

Chapter 6 provides a conclusion of this work and future outlook on the possible development of cell structures and Al plating technique.

CHAPTER 2 BASIC OPERATION OF SOLAR CELLS

2.1 Solar Cell Structure

A photovoltaic solar cell is an optoelectronic device which directly converts solar energy into electrical energy. Generally speaking, there are two requirements need to be presented simultaneously in any photovoltaic solar cells to realize this process:

1) A material in which the absorption of light generates charge carriers, which are excited electrons and the vacant states left by those electrons.

2) The separation of charge carriers by a built-in potential difference, or electromotive force, which drives electrons with higher energy from the solar cell into an external circuit or load.

There are a variety of materials and techniques of charge separation in different cell technologies, but their operations are all based on the two vital processes mentioned above. Typically, the materials for light absorption can be categorized into inorganic semiconductors and organic semiconductors. Solar cells including wafer-Si, thin-film CdTe, thin-film Si, thin-film CIGS, III-V compound semiconductor multi-junction tandem cells, and those developing cells such as gallium arsenide (GaAs) single-junction, CZTSS, and perovskite cells all employ inorganic absorber. On the other hand, the absorber for solar cells like dye-sensitized cells and various types of organic cells is an organic material. In terms of charge separation, there are many different approaches to build up a potential difference, which varies from a p-n junction to a Schottky junction to a heterojunction between two dissimilar semiconductors. In practice, all the commercial solar cells today, wafer-Si, CdTe, thin-film Si, and CIGS, use a p-n junction for charge separation due to its superior performance and reliability to all other approaches.

Figure 2.1 shows the basic schematic of a wafer-Si solar cell [15], which is the

most common solar cell commercially available today. For Si solar cells, the basic design focuses on the optimization of surface reflection, carrier separation, recombination and parasitic resistances to reach about 25% theoretical efficiency. The Si substrate (base), either monocrystalline or multicrystalline Si, is p-type with a resistivity of about 1 Ω-cm. Although silicon's bandgap is slightly low for an optimum solar cell and it is an indirect material with a low absorption coefficient, its abundance and dominance of the integrated circuit industry have made it difficult for other materials to compete in current PV market. The cell thickness can be as thin as about 100 μm with great light trapping and surface passivation. However, thickness between 200 and 400 μm are generally used, partly for practical issues such as making and handling with thin wafers. The front surface is textured with random pyramids to reduce reflection by increasing the chances of reflected light bouncing back onto the surface. A phosphorus diffusion is performed at the front side to form n^+ emitter with thickness of about 0.5 μm. The front emitter is doped to a level sufficient to conduct away the generated charge carriers with very little resistive losses. The front emitter cannot be too thick; otherwise, a great amount of carrier recombination would take place within this region. On the contrary, by making the front emitter thin, a large fraction of the carriers generated by the incident light are created within a diffusion length of the p-n junction. The front metal grid is placed on the surface to conduct away all the current generated, which is made of Ag. There is a trade-off between the shading losses and resistive losses of front metal grid. This makes the design of front metal grid an important topic, and engineers usually follow some basic rules when designing grid pattern [16]. The back electrode is Al, and the Al is also diffused into Si to form a heavily doped p^+ region, which is called the back surface field (BSF). The interface between the high and low doped p-type regions behaves like an

electrical junction and a built-in electric field at the interface creates a barrier to minority carrier flow to the rear surface. Thus, the minority carrier concentration is maintained at higher levels in the bulk of the device, which minimize the impact of rear surface recombination. Both the front Ag grid and the back Al contact are formed by screen-printing technology because of its simplicity, high throughput, and low manufacturing cost. The material for anti-reflection coating (ARC) is silicon nitride (SiN_x if nonstoichiometric) deposited by plasma-enhanced chemical vapor deposition (PECVD), and the thickness is around 75 nm. Moreover, the SiN_x layer is often used for n-type Si surface passivation, which lowers surface recombination by reducing the number of dangling bonds at the Si surface and by providing field induced passivation via its built-in positive charge.

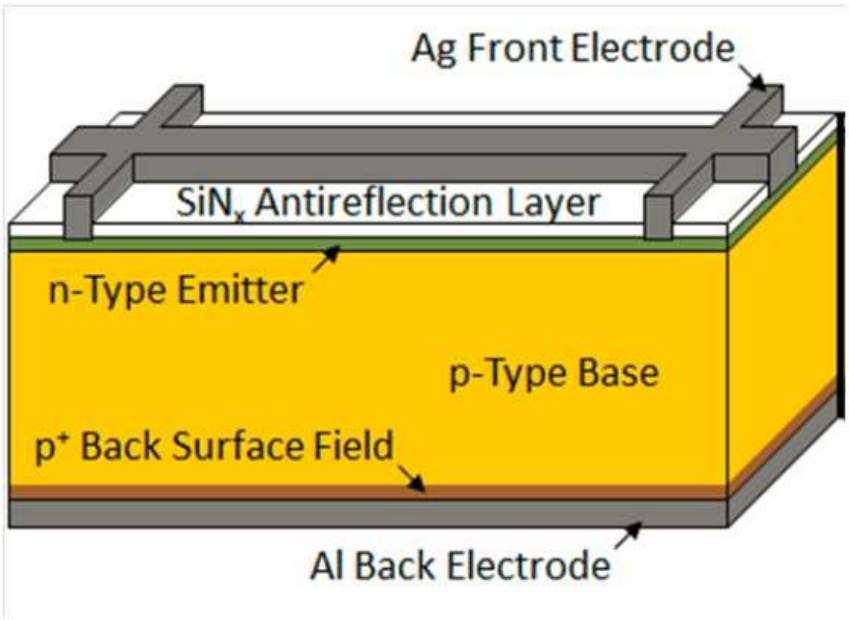

Figure 2.1 Schematic of a wafer-Si solar cell. Surface texturing is not shown, and the figure is not drawn to scale.

2.2 Characteristics of Solar Cell

Several important parameters which are used to characterize solar cells are defined and discussed in this section. Most of the parameters such as short-circuit

current, open-circuit voltage, fill factor, and cell efficiency are determined from the current-voltage characteristic (I-V curve) of the cell under illumination.

2.2.1 Short-circuit Current and Open-circuit Voltage

A solar cell can simply replace a battery in an electric circuit, and the cell would not do anything in the dark. When a light shines on the cell to switch it on, it develops a voltage. The voltage developed when two terminals are isolated (infinite load resistance) is called the open-circuit voltage (V_{oc}), which is the maximum voltage available from a solar cell at zero current. The current through the solar cell when two terminals are connected together is the short-circuit current (I_{sc}). The short-circuit current results from the generation and collection of light-generated carriers. For a solar cell with moderate resistive losses, the short-circuit current and the light-generated current are identical. Therefore, the short-circuit current is the largest current which can be drawn from the solar cell. Since the current is roughly proportional to the illuminated area, the short-circuit current density (J_{sc}) is also a useful factor for comparison of cell's performance.

2.2.2 Photocurrent and Quantum Efficiency

The current generated by a solar cell under illumination at short circuit is called light-generated current or photocurrent, which is dependent on the incident light. To relate the photocurrent density (J_{sc}) to the solar spectrum, the cell's quantum efficiency (*QE*) is needed [17]. The *QE(E)* is the ratio of the number of carriers collected by the solar cell to the number of photons with a given energy incident on the solar cell. It may be given as a function of either photon wavelength or energy. Energy is a more convenient parameter for the physics of solar cells. Thus,

$$J_{sc} = q \int \varphi(E) \times QE(E) d(E) \tag{2.1}$$

where $\varphi(E)$ is the incident photon flux density, which is defined as the number of photons with energy in the range E to $E+dE$ incident on unit area in unit time and q is the electric charge. QE depends on the absorption coefficient of the material, the effectiveness of charge separation and the probability of charge collection in the device. It is a key factor in describing the performance of solar cells under various conditions.

2.2.3 Dark Current and Open-circuit Voltage

When a voltage or bias is applied across the solar cell, a current which flows in the opposite direction to the photocurrent is generated, resulting in the reduction of net current from its short-circuit value. This reverse current is usually called the dark current in analogy to the current $I_{dark}(V)$ which flows across the device in the dark. Most solar cells behave like a diode in the dark, which means its I-V curve would have a much larger current under forward bias than under reverse bias. This rectifying behavior is a feature of photovoltaic devices. For an ideal diode, the dark current density $J_{dark}(V)$ can be expressed as

$$J_{dark}(V) = J_0[exp(\frac{qV}{kT}) - 1] \tag{2.2}$$

where J_0 is the reverse saturation current density, k is the Boltzmann constant and T is the temperature in degrees Kelvin.

The current-voltage characteristic of the solar cell can be approximated as the superposition of the I-V curve in the dark with the light-generated current (or short-circuit current). Although the reverse current which flows through the cell under illumination is not exactly equal to the current flowing in the dark, the approximation

is quite reasonable for many photovoltaic materials and devices. Also, the sign expression for current and voltage in solar cells is that the photocurrent is positive, which is the opposite to the common convention people use in electronic devices. The relation of voltage-current density is then given by

$$J(V) = J_{sc} - J_{dark}(V). \tag{2.3}$$

For an ideal diode, it becomes

$$J(V) = J_{sc} - J_0[exp(\frac{qV}{kT})-1]. \tag{2.4}$$

An equation for V_{oc} is found when the dark current and short-circuit current cancel each other out from the above equation. For an ideal diode,

$$V_{oc} = \frac{kT}{q} ln(\frac{J_{sc}}{J_0} + 1) \tag{2.5}$$

The above equation shows that V_{oc} depends on the saturation current and the short-circuit current of the solar cell. While the value of J_{sc} typically does not change too much, the key effect is the saturation current, since this value may vary by orders of magnitude. The saturation current density, J_0, is related to the recombination in solar cell [18]. Based on the open-circuit voltage, one can approximately know the amount of recombination in the device.

2.2.4 Fill Factor and Efficiency

The short-circuit current and open-circuit voltage are the maximum current and voltage from a solar cell, respectively. The operating regime of the cell is within the range of V_{oc} and J_{sc}. The cell's power density reaches its maximum at maximum power point, which occurs at voltage (V_m) with a corresponding current density (J_m), as shown in Figure 2.2 [17].The fill factor (often abbreviated as *FF*) is defined as the

ratio of the maximum power from the solar cell to the product of V_{oc} and J_{sc}:

$$FF = \frac{J_m \cdot V_m}{J_{sc} \cdot V_{oc}}. \tag{2.6}$$

The fill factor measures the "squareness" of the J-V curve and is also the area of largest rectangle which can fit in the J-V curve.

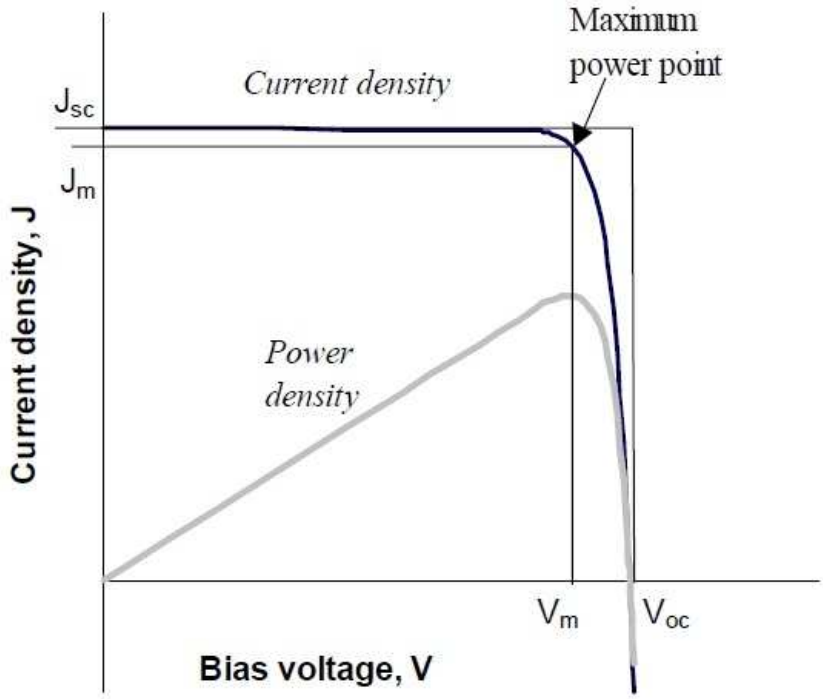

Figure 2.2 The current-voltage and power-voltage characteristics of an ideal cell. The maximum power density $J_m \times V_m$ is given by the area of inner rectangle, while the area of outer rectangle is $V_{oc} \times J_{sc}$.

The efficiency is the most commonly used parameter to compare the performance of different solar cells. The efficiency (η) is defined as the ratio of energy output from the solar cell to the input power density from the sun (P_{in}),

$$\eta = \frac{J_m \cdot V_m}{P_{in}}, \tag{2.7}$$

which is related to V_{oc} and J_{sc} using FF,

$$\eta = \frac{V_{oc} \cdot J_{sc} \cdot FF}{P_{in}}. \tag{2.8}$$

These four quantities J_{sc}, V_{oc}, FF, and η are key characteristics in determining one solar cell's performance. The efficiency depends on the spectrum, intensity of the incident sunlight, and the temperature of the solar cell. Hence, the illumination condition under which the efficiency is measured should be carefully controlled to compare the performance of one cell to another. The Standard Test Condition (STC) for solar cells is the Air Mass 1.5 (AM 1.5) spectrum with an input power density of 1000 W/m^2 and a temperature of 25°C.

2.2.5 Parasitic Resistances

For an ideal solar cell, it is electrically equivalent to a current generator in parallel with a non-linear resistive element such as a diode. When illuminated, the solar cell generates the photocurrent which is divided between the diode and external load. However, in real cells, the power is actually dissipated through the resistance of the contacts and through leakage currents around the sides of the device. These are resistive effects in solar cells, which are electrically equivalent to two parasitic resistances: 1) series resistance (R_s) and 2) shunt resistance (R_{sh}), as shown in Figure 2.3.

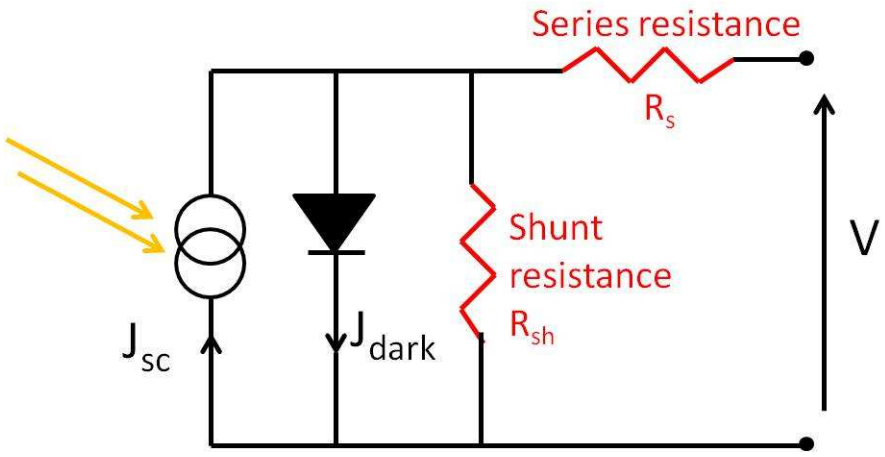

Figure 2.3 Equivalent circuit of a solar cell including series and shunt resistance.

The series resistance is caused by 1) the current flow through the emitter and base of the solar cell, 2) the contact resistance between cell material and metal contacts, and 3) the current flow through the front metal contacts including busbar and fingers. Series resistance is a particular problem at high current densities, for instance under concentrated light. The parallel or shunt resistance results from leakage of current through the manufacturing defects in cell and around the edges of the device. The shunt resistance is a problem in poorly rectifying devices and is particularly severe under low illumination. The effect of these two parasitic resistances is to reduce the fill factor, so typically we want R_s to be as small and R_{sh} to be as large as possible for an efficient solar cell. When both series and shunt resistances are present, the diode equation becomes

$$J = J_{sc} - J_0[exp(\frac{q(V + JAR_s)}{kT}) - 1] - \frac{V + JAR_s}{R_{sh}}, \qquad (2.9)$$

where A is the area of cell.

2.3 Loss Mechanisms in Solar Cells

The theoretical efficiency of crystalline Si solar cells under one sun illumination

is about 29.4% [19]. However, Si solar cells with record efficiencies, which were fabricated by SunPower, Panasonic, and UNSW are currently 25.0~25.5% [20-22]. The discrepancy between the theoretical and the actual efficiency is caused by various loss mechanisms in solar cells, which include optical losses, resistive losses, and recombination losses. The optical losses are due to the fact that not every photon from the solar spectrum enters the absorber of a solar cell, and not every photon which enters a solar cell is absorbed and converted to electron-hole pairs. Figure 2.4 illustrates three main optical loss mechanisms, which are 1) reflection loss, 2) shading loss, and 3) incomplete absorption. The resistive losses are due to the consumption of the potential by various resistances in the cell, which reduces the power delivered to the external load. The recombination losses are caused by several recombination processes in which photo-generated charge carriers recombine with each other before they reach the external load. Minimizing these loss mechanisms in a cost-effective way to achieve higher cell efficiency records has been the major focus of solar cell research over the past few decades.

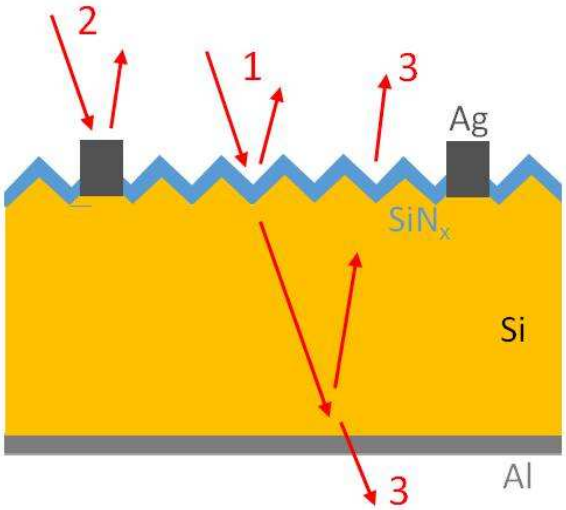

Figure 2.4 Three optical losses in the wafer-Si solar cell. “1” is reflection at front surface and Si/SiN_x interface, “2” is shadowing by front metal electrode, and “3” is incomplete absorption.

2.3.1 Reflection Loss

When photons reach an interface between two materials of different refractive indices, part or all of it is reflected back at the interface and does not enter the second material. In the case of a Si solar cell, the reflectance at the interface of air and Si is over 35% under normal incidence. The reflection can be minimized by two techniques: anti-reflection coating and surface texturing.

1) Anti-reflection coating (ARC): ARC is formed by sandwiching a thin dielectric film between the Si and air to reduce the reflection of incident light via destructive interference of the waves reflected from the top and bottom surfaces of the dielectric (Figure 2.5). Proper selection of thickness (d_{AR}) and refractive index (n_{AR}) of the ARC layer can reduce reflection significantly.

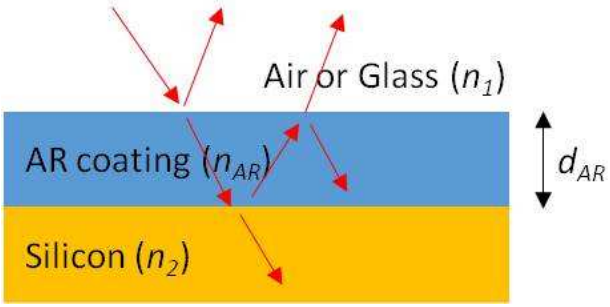

Figure 2.5 Schematic of a single anti-reflection coating layer for Si solar cells.

For a single ARC layer, the reflectance (R) can be expressed by the Fresnel equations [23]:

$$R = \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos\theta}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos\theta}, \quad \theta = \frac{2\pi \cdot n_{AR} d_{AR}}{\lambda}, \tag{2.10}$$

$$r_1 = \frac{n_1 - n_{AR}}{n_1 + n_{AR}}, \quad r_2 = \frac{n_{AR} - n_2}{n_{AR} + n_2} \tag{2.10}$$

where n is the refractive index of each layer. The reflectance has minimum R_{min} when

$n_{AR} \cdot d_{AR} = \frac{\lambda}{4}$ (quarter-wavelength destructive interference) and is obtained by:

$$R_{min} = \frac{(n_1 n_2 - n_{AR}^2)^2}{(n_1 n_2 + n_{AR}^2)^2}. \quad (2.11)$$

For the broad solar spectrum, the wavelength (λ) at maximum intensity, about 630 nm, is often used to determine the thickness of the ARC layer. There is also an optimum value for the refractive index of the ARC layer, which makes R_{min} become zero at the desired wavelength:

$$n_{AR} = \sqrt{n_1 n_2}. \quad (2.12)$$

As solar cells are typically packaged into modules, the material on top of the cells is glass with a refractive index of about 1.5. Therefore, the optimum index of the ARC layer on wafer-Si solar cells is around 2.4 at 630 nm.

2) Surface texturing: surface texturing is another effective and common technique for minimizing the reflection. Texturing of Si surface can be done by immersing a Si (100) wafer into an alkaline solution, which contains sodium hydroxide (NaOH) or potassium hydroxide (KOH). The etch rate on the (111) planes is much smaller than on the (100) planes. This exposes the (111) planes in the Si crystal, resulting in pyramids of random sizes on the wafer. These random pyramids reduces the reflection by increasing the number of bounces of incident light, as illustrated in Figure 2.6. For a Si wafer in air, the reflectance of Si surface can be reduced from 35% to about 12% after surface texturing. In today's wafer-Si solar cells, a SiN_x ARC layer is often deposited on textured Si wafers, and the combination of these two techniques can further reduce the surface reflectance to almost zero at a particular wavelength and incident angle.

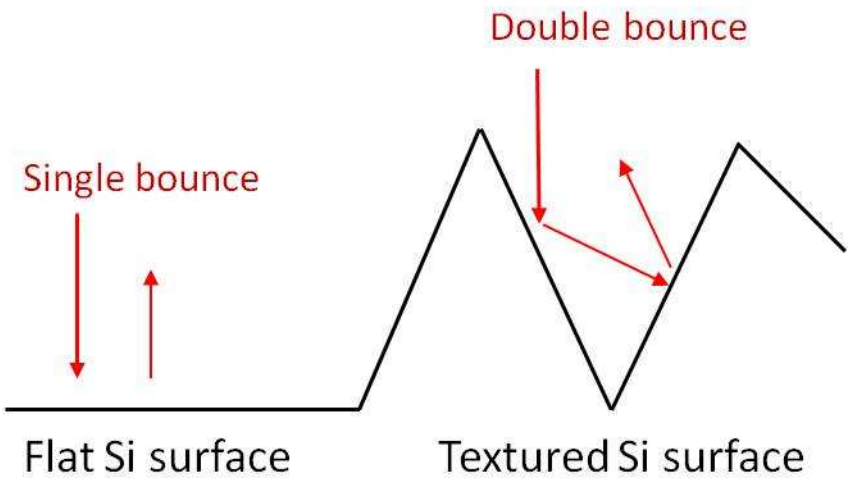

Figure 2.6 Comparison of bounces of incident light on flat Si surface and textured Si surface.

2.3.2 Shading Loss

A finished solar cell needs to be contacted at the front and back side in order to extract power from the cell. However, the front metal contact prevents the light to enter into the cell, resulting in a reduced light-generated current. The front metal contact has to be in a grid shape (busbars and fingers) to allow sunlight to pass through. Typically, the front metal contact covers 5-10% of the cell surface area. Reducing the width of the metal busbars or fingers can simply reduce the shading loss, but this would increase the resistive losses as the cross section of the metal grid gets smaller and the distance which charge carriers need to travel before being collected becomes longer. Thus, the design of front metal grid has to be optimized to balance the shading and resistive losses. It is also possible to place both contacts on the rear side of the cell to avoid the shadowing loss, and this structure is called the interdigitated back contact (IBC) solar cell. The best efficiency of the IBC cell (large-area) is 25%, fabricated by SunPower on a commercial cell [22].

2.3.3 Incomplete Absorption

The loss of incomplete absorption refers to the loss of photons with energy $E>E_g$, which escape the cell from either the front or back surfaces due to thin cell thickness or insufficient optical path length through the cell. Incomplete absorption is also called optical leak, which can be minimized by appropriate light trapping that enhances the absorption of photons with long wavelength by reflecting them back into the cell from the surfaces. Light trapping is realized by changing the angle of incident light such that the light can travel at certain angle, rather than perpendicular to the surface, leading to an increased optical path length. Thus, the front surface is textured in order for the light to meet the surface at certain angles. When light gets reflected from the back surface and travels from back to front in a cell, it goes from the high-index semiconductor to the low-index ARC layer. Because of this reverse index profile, total internal reflection can occur at the front surface at the critical angle (θ_c), which is given by:

$$\theta_c = arcsin\frac{n_{AR}}{n_2}. \tag{2.13}$$

At this angle, the refracted light travels along the interface, and no light enters the ARC layer. When the incident angle is larger than θ_c, all the light is specularly reflected back into the semiconductor. For the rear surface of most wafer-Si solar cells, the metal electrode, typically Al, can serve as a reflector. If the rear surface is textured, the surface recombination would also increase due to an increased interface trap density. Therefore, the rear surface often remains planar in the structure design of wafer-Si solar cells with higher efficiency.

2.3.4 Resistive Losses

The resistive losses are caused by the series resistance (R_s) and shunt resistance (R_{sh}) of a solar cell. The R_{sh} generally results from process-induced defects, resulting in partial shunting of the p-n junction. Shunting lowers the R_{sh} and reduces the amount of photocurrent flowing through the p-n junction, which decreases the voltage of the solar cell. It is worth noting that R_{sh} is not a design parameter, but the R_s is a design parameter which can be controlled.

Figure 2.7 illustrates the path of current flow in a wafer-Si solar cell [15]. The current flows vertically in the base but horizontally in the emitter. The fingers collect currents from different regions of the cell and the busbars collect currents from all the fingers. The R_s of a solar cell consists of several components, which are resistances in the current path, including:

1) The back Al/Si contact resistance R_1;

2) The base resistance R_2;

3) The emitter resistance R_3;

4) The front Ag/Si contact resistance R_4;

5) The finger resistance R_5; and

6) The busbar resistance R_6.

Resistance is proportional to the length and inversely proportional to the cross section of a given material. The direction of the current in Figure 2.7 indicates that the back contact resistance R_1 and base resistance R_2 are small compared to other resistances since the cross section of R_1 and R_2 is large. The resistive losses in Si solar cells are often determined by the remaining four resistances, emitter resistance R_3, front contact resistance R_4, finger resistance R_5, and busbar resistance R_6. Emitter resistance R_3, finger resistance R_5, and busbar resistance R_6, are design parameters in

a solar cell. It is very important to have the proper emitter and grid design for lowering the R_s and increasing the cell efficiency.

For the emitter design, there is a tradeoff between resistive losses and recombination losses in the emitter. The high doping level in the emitter significantly reduces the lifetime and diffusion length of photo-generated charge carriers, resulting in high recombination losses in the emitter. While a thinner emitter with a lower doping level can be used to minimize the recombination losses, this reduces the cross section for the current flowing horizontally along the emitter and increases the emitter resistance. The design of the fingers and busbars is a compromise between shadowing losses and resistive losses. Wider fingers and busbars reduce the resistances but block more incident sunlight, while narrower fingers and busbars reduce shadowing losses but increase resistive losses. The design of the front grid pattern for our all-Al solar cells will be discussed in more detail in Chapter 5, in which the design rules and pattern optimization will be elucidated.

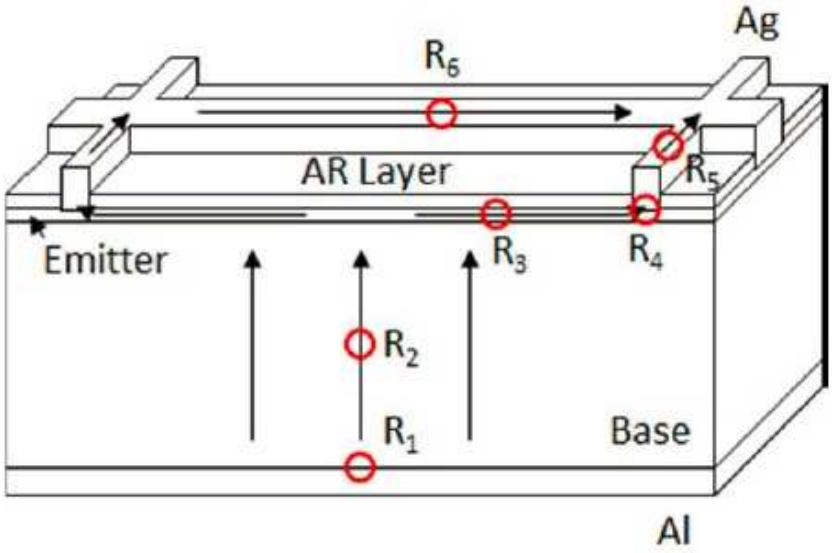

Figure 2.7 Path and direction of the electron flow in wafer-Si solar cells. Various resistances are labeled with red circles. Dominant resistances include emitter resistance R_3, front contact resistance R_4, finger resistance R_5, and busbar resistance R_6.

2.3.5 Recombination Losses

When a solar cell is illuminated, the absorption of each photon creates an excited electron and a vacant state (hole) in the absorber. They need to be separated and extracted by the electrodes to generate an electric power output. Recombination losses refer to losses in which an excited electron falls back into a vacant state before they reach the electrodes. There are four types of recombination processes in solar cells based on inorganic semiconductor: 1) Radiative recombination; 2) Auger recombination; 3) Shockley-Read-Hall (SRH) recombination; and 4) Surface recombination.

1) Radiative (Band-to-Band) recombination: An excited electron in the conduction band directly recombines with a hole in the valence band, which releases a photon with energy equal to the bandgap of the semiconductor (Figure 2.8). The rate of radiative recombination is proportional to the number of carriers in the conduction band and the number of empty states in the valence band. This recombination is dominant in direct bandgap semiconductors such as CdTe, but it is not that important in indirect bandgap materials like Si.

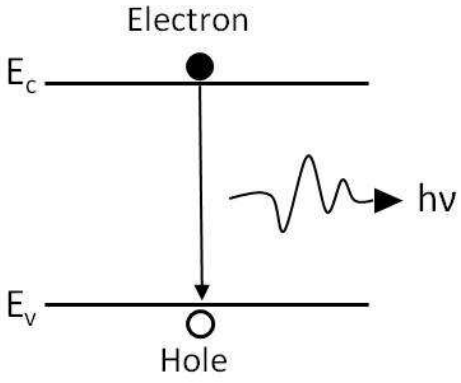

Figure 2.8 Radiative recombination in inorganic semiconductors.

2) Auger recombination: An electron in the conduction band recombines with a hole in the valence band, and the energy associated with the recombination excites

another electron in the conduction band to a higher-energy state (Figure 2.9). The excited electron will quickly lose its excess energy through multiple steps of relaxation (scattering) and come down to the minimum of the conduction band. This can also happen to a hole: the energy released through recombination can excite a hole into a higher-energy state, which will eventually relax to the maximum of the valence band. Auger recombination occurs at a very high carrier concentration in the semiconductor.

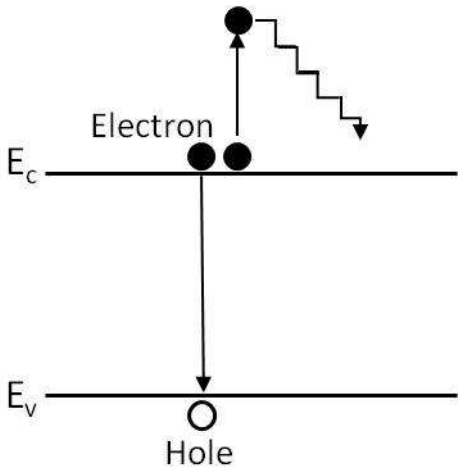

Figure 2.9 Auger recombination in inorganic semiconductors.

3) Shockley-Read-Hall (SRH) recombination: Various structural defects, including impurities, dislocations, and grain boundaries in the crystal lattice, often introduce electronic states near the middle of the bandgap in the semiconductor. These defect states, or trap states, can act as recombination centers for charge carriers. The SRH recombination involves two step processes, as illustrated in Figure 2.10. First, an electron (or hole) is trapped by an energy state in the energy level introduced by the defects. If a hole moves up to the same energy state before the electron is re-emitted into the conduction band, they then recombine with each other. While recombination through defects is present in direct bandgap semiconductors, it is particularly important in indirect bandgap semiconductors such as Si. Minimizing defect densities

in Si is critical to increase the lifetime and diffusion length of charge carriers, thus improving the cell efficiency.

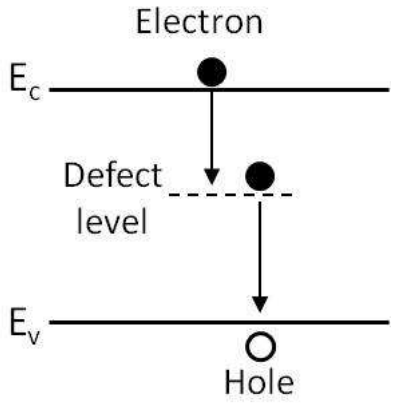

Figure 2.10 Shockley-Read-Hall (SRH) recombination in inorganic semiconductors.

4) Surface recombination: Si surface has a large number of unsaturated dangling bonds, which introduce surface defect states within the forbidden gap (Figure 2.11) [24]. These states act as recombination centers, resulting in surface recombination. Surface passivation is a technique used for reducing the surface recombination, which involves two approaches: chemical passivation and field-effect passivation.

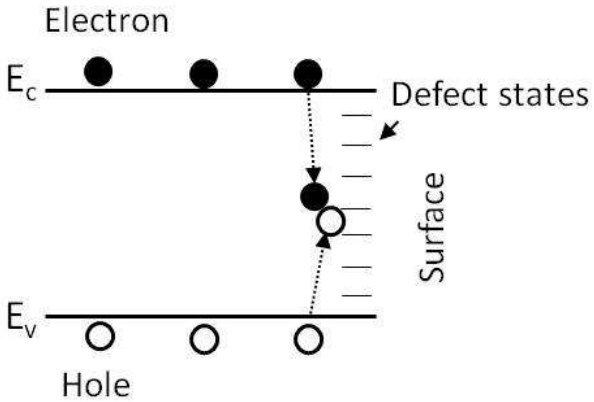

Figure 2.11 Surface recombination at Si surface.

The chemical passivation terminates the dangling bonds on the Si surfaces and reduces the density of surface states (D_{it}) with a thin dielectric film. Thermally-grown

silicon dioxide (SiO_2), PECVD-grown SiN_x, and aluminum oxide (Al_2O_3) can be used for this purpose. Right selection of these dielectric thin films can provide excellent surface passivation for high cell efficiency. The field-effect passivation is based on the reduction of either electron or hole concentration at the Si surface with a built-in electric field. The electric field can induce an accumulation layer by repelling minority carriers from the Si surface. This charge accumulation at the surface lowers the recombination because recombination rate is the maximum when the electron and hole concentrations at the Si surface are equal. A good example is the negatively-charged Al_2O_3 dielectric layer for field-effect passivation on p-type Si surface.

CHAPTER 3 BOTTLENECKS FOR CRYSTALLINE-SI SOLAR CELLS

3.1 Brief Overview of Crystalline-Si Solar Cells

Out of all the solar cell technologies available commercially in the market, crystalline-Si solar cells, including multicrystalline and monocrystalline dominate the solar cell market with about 89% of market share in 2015, according to NPD Solarbuzz (now IHS technology) PV Technology Roadmap report (Figure 3.1) [25]. Suppliers of high efficiency solar panels based on premium crystalline-Si, such as SunPower and Panasonic, comprise 3% market share and are expected to increase their capacity over the next few years. Thin-film cell technologies, led by First Solar and Solar Frontier only account for nearly 8% of the market share. Among them, CdTe panels manufactured by First Solar is the leader with roughly 5% of the market.

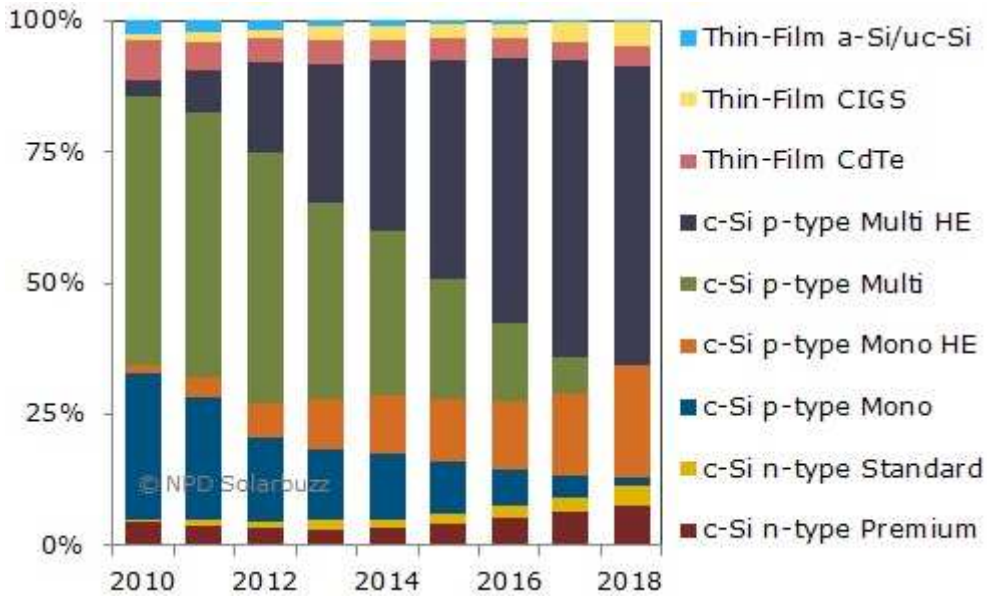

Figure 3.1 Accelerated Technology Roadmap Scenario Forecast by PV Technology Type.

There are several technical factors leading to the dominance of Si in the solar cell industry. Among them, technologies developed by the Si-based microelectronics industry by the 1970s, when the solar industry was born, undoubtedly contributed to its dominance since fabrication techniques, device physics, and materials science had

all been well established for Si in those years. Although it can be foreseen that crystalline-Si solar cells will still be the workhorse of PV industry for years to come, they have some major limitations, which hinder them to reach terawatt-scale deployment. The production of crystalline-Si solar cells consists of fabrication processes with intensive energy input and high cost, but their efficiency and cell lifetime are the highest. They are made on silicon wafers, which is among the most abundant elements on earth. Monocrystalline-Si solar cells use mono-Si wafers grown by Czochralski process as substrates. The efficiency of monocrystalline-Si solar cells has reached 25%, while that of multicrystalline-Si solar cells, which are manufactured through directional solidification, is around 20%. Despite the fact that the potential of crystalline-Si solar cells in supplying energy demands is enormous, their future growth will likely be constrained by the fundamental roadblocks. In Chapter 3.2 and 3.3, we will discuss two major bottlenecks now faced by PV industry: 1) high energy input and 2) limited silver reserve. We will explain our approach to solve them, especially in Chapter 3.3 regarding the bottleneck of silver reserve.

3.2 Energy Input

The fabrication of crystalline-Si solar cells is energy intensive, costly, and polluting. Figure 3.2 shows the process flow for the fabrication of monocrystalline-Si solar cells [26]. It can be seen that there are major steps included in the fabrication, which are quartz reduction to metallurgical-grade (MG) Si, distillation of trichlorosilane ($SiHCl_3$), Siemens process to produce polycrystalline-Si (poly-Si), Czochralski growth of monocrystalline-Si ingot, wafering, and cell fabrication. The electricity input for each step is also labeled. Quartz is first reduced to MG Si in an electric-arc furnace with charcoal at ~1900°C, which releases several million tons of

carbon dioxide (CO_2) into the atmosphere. MG-Si is reacted with hydrochloric acid (HCl) to form $SiHCl_3$, which is purified by multiple distillation. The corrosive $SiHCl_3$ often results in frequent replacement of the stainless steel equipment. The purified $SiHCl_3$ is then reduced by hydrogen (H_2) to produce high-purity poly-Si in the Siemens process, which takes place on a high-purity Si rod at ~1150°C with an electrical current passing through it. The Siemens process is a very energy-intensive process. Subsequently, monocrystalline-Si ingot is obtained by the crystallization of high-purity poly-Si at extremely high temperature in Czochralski process, which is again an energy-intensive step.

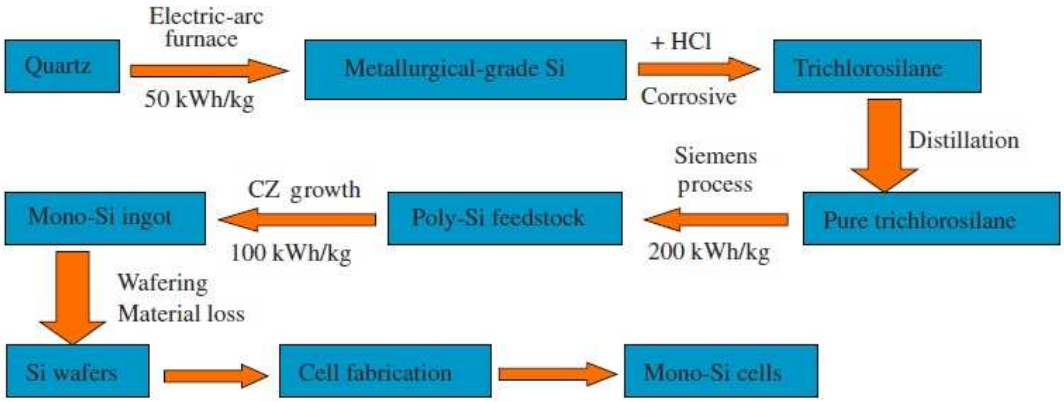

Figure 3.2 Fabrication process flow for monocrystalline-Si solar cells.

If we assume 20% material loss for each step except the wafering step, which has about 65% material loss, the total electricity needed to produce 1 kg of monocrystalline-Si wafers is about 1000 kilowatt hour (kWh). Moreover, it takes a huge amount of extra electricity to turn Si wafers into cells and modules, in which the sealing of a cell module with an Al frame is a very energy-intensive process. It was estimated that the electricity consumption for the production of monocrystalline-Si wafers a year was 2.5 times as many as the electricity produced from monocrystalline-Si solar cells under the best scenario. To our earth, it would be really

difficult to squeeze out 10% of its electricity consumption just for solar cells. Therefore, in order to reach terawatt-scale deployment of monocrystalline-Si solar cells, new process flow need to be developed to significantly reduce the energy input for the production of mono-Si cells and modules. Due to this purpose, the PV industry has been looking into the potential of the fluidized-bed reactor (FBR) process. Several companies, including REC Silicon and SunEdison, are exploring the application of the FBR technology and establishing poly-Si production lines based on this process. Compared to the Siemens process, the FBR process uses much lower electricity for producing high-purity poly-Si, meaning the manufacturing cost can be reduced. According to the most recent International Technology Roadmap for Photovoltaic (ITRPV), it is expected that the FBR technology will increase its share substantially in poly-Si production over the next decade, as shown in Figure 3.3 [27].

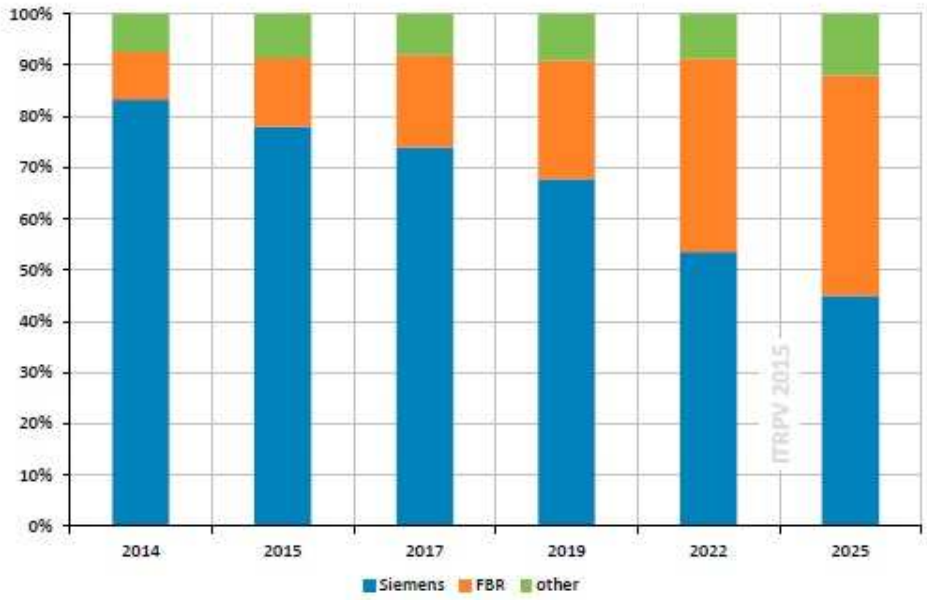

Figure 3.3 Expected change in the distribution of poly-Si production technologies.

3.3 Silver Reserve

In most commercial crystalline-Si solar cells today, Ag is used as the front finger

electrode on the n-type emitter, while Al is used as the back electrode on the p-type base, as shown in Figure 2.1. In addition to the bottleneck of high energy input, crystalline-Si solar cells suffer from the scarcity of Ag for terawatt-scale deployment. Ag provides some advantages over other metals as front metallization, such as low resistivity and resistance to oxidation. The known reserve of Ag is 530000 metric tons according to the mineral commodity summaries published by U.S. Geological Survey in 2015 [28]. The density of Ag is 10.5 g/cm^3. If we assume the Ag contacts are 12 μm thick and the fraction of front metallization is 7%, the peak output of crystalline-Si solar cells with an efficiency of 17% would be around 10.1 TW_p. This value equals an averaged output of 1.5 TW or only 3% of the projected energy demand in 2100 (46 TW) [29]. This estimation is done under the best scenario, in which all the silver reserve are used for the production of crystalline-Si solar cells. If we take into consideration other commercial usages such as batteries, mirrors, photography, and jewelry, which also consume Ag, the total energy these cells can provide may be much less than 3% of the energy demand in 2100. The cost associated with Ag material and processing has become a significant portion of the cell fabrication cost as the module price continues its decline [30]. Due to the limited supply of Ag, a rise in silver price is guaranteed, which makes cost control difficult for cell manufacturers. These factors have motivated industry-wide efforts to develop an alternative metallization technique with a lower-cost and Earth-abundant metal for the front finger electrode.

Among all capable metallization techniques, finger contacts composed of nickel/copper (Ni/Cu) metal stacks has been investigated extensively in recent years [31-36], and cells with efficiencies above 20% have been successfully demonstrated with an electroplated Cu/Ni front electrode. The most important feature of

electroplated Ni/Cu stacks is that this metallization technique can be realized with lower materials cost. The formation of Ni/Cu contact stacks involves three major steps: 1) Patterning of SiN_x ARC layer; 2) Deposition of a Ni seed and barrier layer, followed by 3) deposition of a Cu electrode. The conventional Ag contact is usually formed by screen-printing and firing the Ag paste through SiN_x ARC layer. However, Ni/Cu-based metallization requires an additional step to open the SiN_x ARC layer in order to form the contact grid. For patterning the front dielectric layer, various approaches have been investigated, including: 1) Photolithography and wet etching [37]; 2) Laser chemical processing [38]; 3) Laser ablation [39]; and 4) Mechanical scribing [40]. After the opening of front dielectric layer, the Ni seed and barrier layer is formed by either electroless plating or light-induced plating. The Cu electrode, which is the main conducting layer, is deposited by light-induced plating developed at the Fraunhofer Institute for Solar Energy [41]. After the deposition of Ni/Cu stacks, a thin capping layer of Ag or tin (Sn) is usually electroplated on top of the Cu electrode. The purpose of this capping layer is to prevent the Cu metal lines from being oxidized and help to solder the interconnecting tabs. Figure 3.4 shows a schematic of Ni/Cu/Ag or Sn-based metallization schemes.

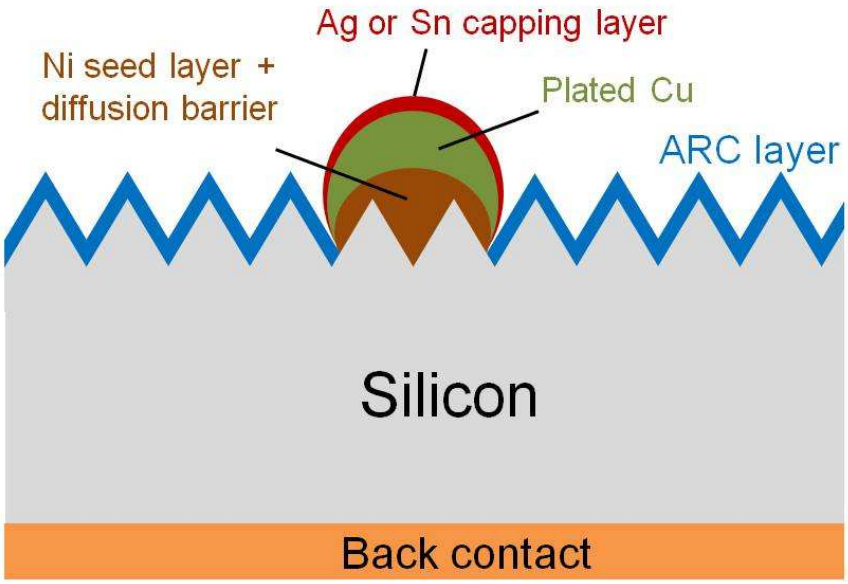

Figure3.4 Schematic of Ni/Cu/Ag or Sn-based metallization schemes.

In terms of electrical resistivity and material abundance, Al is another promising candidate to substitute for Ag as the front electrode in crystalline-Si solar cells [42]. Little has been done to investigate the possibility. The biggest advantage of Cu is its low resistivity. Electroplated Cu has its resistivity close to its bulk value, far lower than that of screen-printed Ag. From our experience, the resistivity of electroplated Al is 2–3 times larger than electroplated Cu and similar to screen-printed Ag. However, Cu has several intrinsic issues as an electrode in Si solar cells. Cu introduces deep states in Si, degrading the efficiency of the cell, so the Ni barrier layer is required to prevent Cu from contacting and diffusing into Si. Oxidation of Cu is another concern for module reliability. In comparison, Al is a proven electrode material in crystalline-Si solar cells. It can be in direct contact with Si without introducing deep states. It has excellent reliability as it is protected from oxidation by a dense Al_2O_3 film which naturally forms on it.

There are several possible processes for Al metallization on crystalline-Si solar

cells. Kessler et al. [43] reported vacuum-based in-line evaporation for the Al front electrode on back-junction cells with efficiencies approaching 20%. In principle, sputter deposition can also be used for Al metallization, but both evaporation and sputtering are vacuum-based processes which would result in high processing costs for Al electrodes. Hanwha Solar America proposed a design concept of IBC cells with screen-printed Al as the electrodes for both contact polarities [44] although it has yet to be demonstrated. Screen-printed Al would be compatible with current industrial process for Al metallization. However, it is unclear how screen-printed Al works on n-type Si since the cell performance would be degraded if Al diffuses into n-type Si. This goes back to the firing temperature for the Al electrode on n-type Si. It has to be low enough, which excludes Al pastes with >700˚C firing temperature. Low-temperature fired Al paste with a low resistivity is still not commercially available yet. Therefore, a solution-based metallization process with a low processing temperature for Al electrodes is desirable, and is the motivation behind the development of room-temperature Al electroplating on Si substrates in our lab. This metallization process will be discussed in more detail in Chapter 4.

3.4 Summary

The deployment of solar cells have to be expand to tens of peak terawatts in order to make a noticeable impact on future energy demands. Out of all the solar cell technologies commercially available today, crystalline-Si solar cells dominate the cell industry with nearly 90% of the market share. Although the potential of crystalline-Si solar cells in supplying energy demands is enormous, their future growth will likely be constrained by the two major bottlenecks. The first one is high energy input for the production of crystalline-Si modules. With current technology, we would have to save

a lot of electricity to fabricate those modules. A much more energy-efficient process flow needs to be developed in order to solve this bottleneck. The second one is the scarcity of Ag reserve for the front metal grid. An alternative metallization technique with a low-cost and Earth-abundant metal has to be investigated and developed to substitute for conventional screen-printing of Ag.

CHAPTER 4 ELECTROPLATING OF ALUMINUM ON SILICON IN AN IONIC LIQUID

4.1 Introduction

Room-temperature or near-room-temperature electroplating of Al requires a non-aqueous solvent for an Al precursor because of the larger negative standard potential of Al/Al(III) couple (-1.67 V vs. NHE). Many solvents have been reported for this purpose [45]. including organic solvents and ionic liquids. Three types of organic solvents have been used to dissolve Al halides for Al electroplating: aromatic hydrocarbons [46], dimethylsulfone [47], and ethers [48]. Although high quality Al deposits can be obtained with these solvents, the relatively narrow electrochemical window, low electrical conductivity, low solubility of Al halides, high volatility and flammability make industrial applications of these organic solvents limited. Ionic liquids are a relatively new class of solvents for Al electroplating. They are characterized by high electrical conductivity, low viscosity, low toxicity, non-flammability, high thermal and chemical stability, and wide electrochemical window, making them ideal solvents for Al electroplating. Various ionic liquids for Al electroplating have been reported [49-59], which are typically mixtures of aluminum chloride ($AlCl_3$) and an organic halide (RX), such as 1-ethyl-3-methylimidazolium chloride (EMIC) and 1-butyl-3-methylimidazolium chloride (BMIC). These ionic liquids show adjustable Lewis acid-base properties, which are acidic when the molar ratio of $AlCl_3$: RX is >1. Al electroplating can be performed only under acidic conditions.

Electroplating of Al in an ionic liquid has been carried out on metallic substrates such as stainless steel [56], platinum [50, 54], tungsten [50, 51, 55], gold [53], copper [52], iron [54], and glassy carbon [50]. The deposited Al often serves as an

anticorrosion coating. Although Al electroplating on Si has been reported [59], report of electroplated Al on Si substrates as a low-cost metallization method in Si photovoltaics and microelectronics has yet to appear in the literature. A major difference between electroplating on Si substrate vs. on metallic substrate is the high resistivity of Si, which is typically in 10^{-2}–10 Ω-cm. For most metals, the resistivity is in 10^{-5}–10^{-6} Ω-cm. Another problem is the native oxide on Si, which is electrically insulating and hinders electroplating.

In this Chapter, we report the results on electroplating of Al on Si substrates in an above-room-temperature ionic liquid. Dense and adherent Al deposits have been reproducibly obtained directly on Si substrates from a 3:2 molar ratio $AlCl_3$: EMIC solution at temperatures slightly above 100˚C. In addition to structural and compositional characterization of the Al deposits, it is of great interest to examine their electrical properties for applications in metallization. The effects of deposition parameters such as pre-bake conditions, deposition temperature, and post-deposition annealing on the sheet resistance of the deposits were investigated. The resistivity of the Al deposits after annealing was in the high 10^{-6} Ω-cm range, similar to that of screen-printed Ag from an Ag paste. This electroplating process has been integrated in the fabrication of a p-type monocrystalline-Si solar cell for n-side metallization, which will be discussed in Chapter 5.

4.2 Experimental

We prepared the electroplating solution and conducted Al electroplating in a dry nitrogen box with a continuous nitrogen flow, which prevents the ionic liquid from absorbing moisture. All the chemicals, 1-ethyl-3-methylimidazolium tetrachloroaluminate ((EMIM)$AlCl_4$) (≥95%, Aldrich) and anhydrous $AlCl_3$ powder

(99%, Aldrich), were used as received. The electroplating solution was prepared by mixing 3:2 molar ratio of $AlCl_3$ and (EMIM)$AlCl_4$ in a dry beaker with continuous magnetic bar stirring at ambient temperature, ensuring Lewis acidic property. On completion of the room temperature mixing, a pre-bake was performed in which the obtained electrolyte was heated to different temperatures for different times in order to drive out the residual moisture in the electrolyte. Then, the temperature of the electrolyte was changed to a predetermined temperature for Al deposition. The effect of pre-bake conditions and deposition temperature was investigated through the sheet resistance of the resultant Al deposits.

A three-electrode electrochemical cell was employed for all the experiments, as shown in Figure 4.1. Textured Si wafers, either n-type or p-type with resistivity between 0.3–1 Ω-cm, were used as the substrates. A thin SiN_x layer was deposited on the backside of the Si wafer to ensure one-side Al deposition. Prior to electroplating, the Si wafer was cleaned in diluted hydrofluoric acid (HF) to remove native oxide on Si surface. Al wires of 99.99% purity were used as the sacrificial counter and reference electrodes. This makes the electroplating solution reusable for many deposition runs, as the Al anode supplies Al to the solution and keeps the Al concentration in the solution constant. The Al wires were cleaned with a short dip in 37% hydrochloric acid (HCl), followed by a deionized (DI) water rinse. After cleaning, the Al wires and the Si wafer (as the cathode/working electrode) were immediately assembled and then transferred to the dry nitrogen box. The deposition of Al was performed at a temperature near the boiling point of water, and the electrolyte was magnetically stirred. The electroplating process was carried out galvanostatically, i.e. under a constant current of ~15 mA/cm^2 for half an hour. After deposition, excess ionic liquid was removed from the sample by dipping it in absolute

alcohol. The sample was then rinsed with DI water and dried with nitrogen. Post-deposition annealing under vacuum was also conducted to further reduce the sheet resistance of the Al deposits.

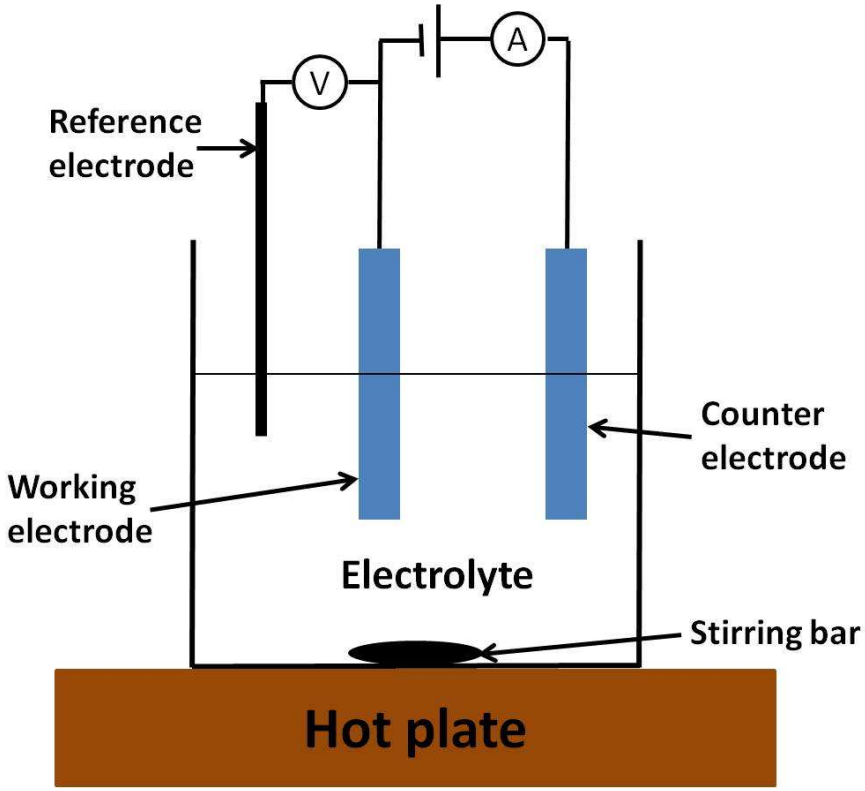

Figure 4.1 Schematic of electrochemical cell setup for Al electroplating.

A scanning electron microscope (SEM) equipped with energy dispersive X-ray analysis (EDX) was utilized to examine the surface morphology and composition of the Al deposits. The crystal structure was studied with an X-ray diffractometer (XRD) with Cu K_α radiation. The sheet resistance of the Al deposits was measured with a four-point probe. The nominal thickness of the Al deposits was calculated by the following equation:

$$\text{Nominal thickness } (\mu\text{m}) = \frac{J(\text{A/cm}^2) \times t \times 27(\text{amu})}{96485 \times 3 \times 2.7(\text{g/cm}^3)} \times 10^4 . \qquad (4.1)$$

4.3 Results and Discussion

Surface cleaning of the substrate prior to deposition is critical for Al electroplating. We used diluted HF to clean the Si substrate, which is effective enough to remove native oxide and leaves a clean Si surface for electroplating. It was found that whitish, dense, and adherent Al can be plated directly on Si if the resistivity of the Si substrate is below ~1 Ω-cm. For Si substrates with >1 Ω-cm resistivity, the Al deposits were greyish and poorly adherent to the Si substrate. A seed layer of metal, such as Ni or Ni silicide (NiSi), was required in this case.

Figure 4.2 shows top-view SEM images of Al deposits on a Si substrate and a NiSi-coated Si substrate at 70˚C and 15 mA/cm^2 for 30 min without pre-bake of the electroplating solution. As shown in Fig. 4.2(a), the as-deposited Al film directly on the Si substrate is dense and reasonably homogeneous with large Al crystallites on the order of 10–20 μm. For the NiSi-coated Si substrate which is used specifically for Si with >1 Ω-cm resistivity, the as-deposited Al film is dense with smaller crystallites on the order of 2–4 μm but more homogeneous than that obtained directly on Si, evidenced in Fig. 4.2(b). The increased homogeneity of Al on NiSi can be attributed to the fact that NiSi has a lower resistivity than Si, resulting in a more even current distribution in the substrate during electroplating. However, the adherence between NiSi and Al was so poor that the Al film could be easily peeled off regardless of surface preparation. Considering this material issue, the following results were obtained from Al deposits directly on textured n-type Si substrates with resistivity between 0.3–1 Ω-cm.

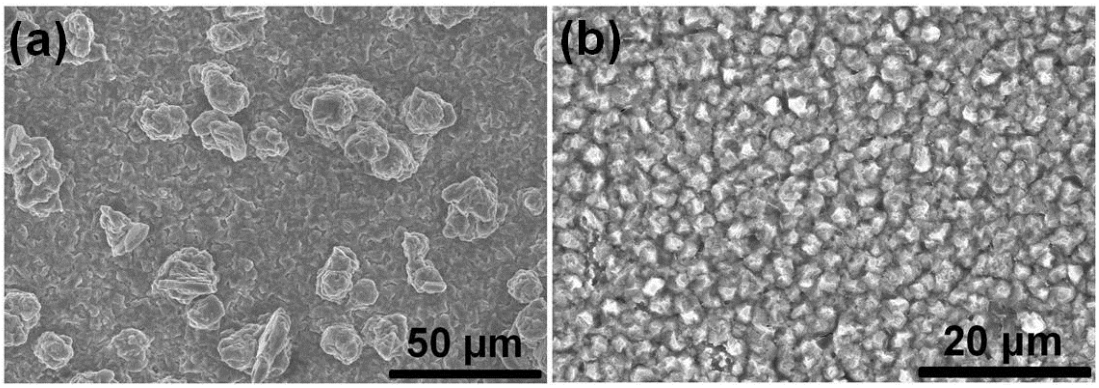

Figure 4.2 Top-view SEM images of Al deposits on (a) a Si substrate with resistivity below 1 Ω-cm and (b) a NiSi-coated Si substrate at 70˚C and 15 mA/cm^2 for 30 min without pre-bake of the electroplating solution.

Figure 4.3 shows the corresponding EDX analysis and XRD pattern of the Al deposit in Fig. 4.2(a). In Fig. 4.3(a), the deposit displays only one strong peak of Al around 1.5 keV without any other peaks of different materials, suggesting a pure Al deposit under the conditions described. As shown in Fig. 4.3(b), all the four peaks of the deposit are related to Al and identified as Al(111), (200), (220), and (311), further confirming that the composition of the deposit is pure metallic Al.

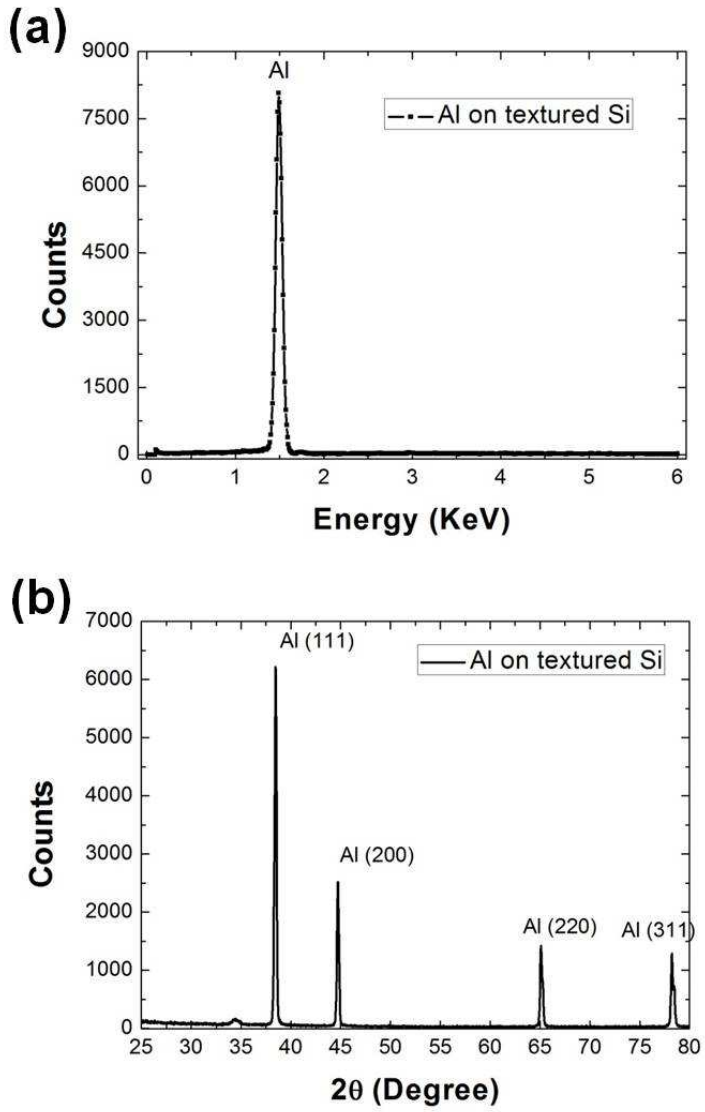

Figure 4.3 (a) EDX spectrum and (b) XRD pattern of an Al deposit obtained on Si substrate with resistivity below 1 Ω-cm at 70˚C and 15 mA/cm^2 for 30 min without pre-bake of the electroplating solution.

The sheet resistance of electroplated Al was investigated. The effects of pre-bake conditions, deposition temperature, and post-deposition annealing conditions were examined. Three different temperatures (100, 120, and 140˚C) and two different pre-bake times (30 and 60 min) were chosen as the conditions for moisture removal in the electroplating solution. After pre-bake, the solution temperature was changed to 70˚C for a 30-min deposition at 15 mA/cm^2. Figure 4.4 shows the sheet resistances of Al deposits as a function of pre-bake temperature and time. The Al deposits show

significant reduction in sheet resistance when the pre-bake temperature exceeds 100˚C, which is the boiling point of water at one atmosphere. It was also noticed that the humidity level in the dry nitrogen box dropped from 19% to 16% after the electroplating solution was baked at 120˚C for 60 min. This supports the assumption that the pre-bake drives out moisture from the solution. Moisture in the solution increases the possibility of Al_2O_3 formation in the Al deposit, which is an insulator and increases the resistivity of the Al deposit. It can be seen in Fig. 4.4 that the lowest sheet resistance is obtained at 120˚C for 60 min, which is then used as the pre-bake conditions for all the subsequent experiments.

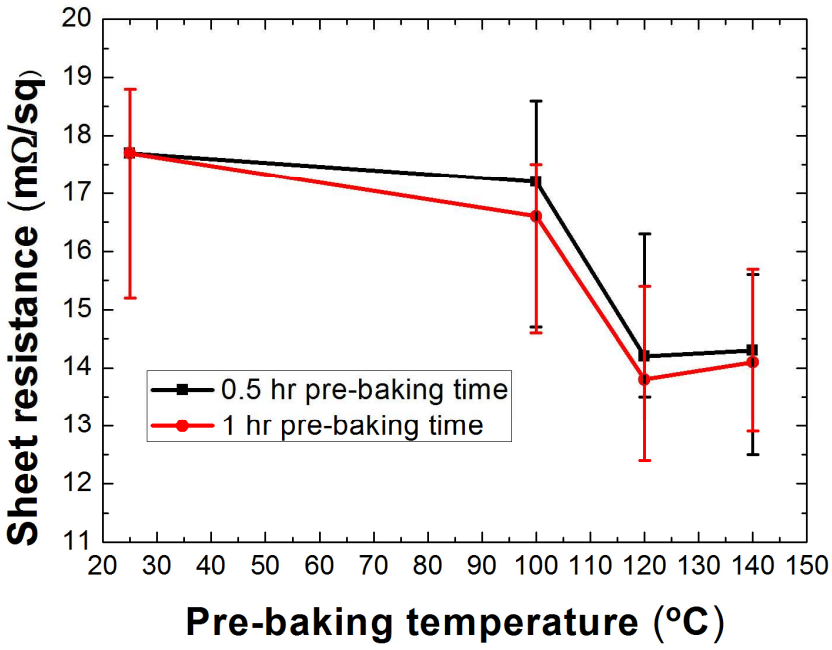

Figure 4.4 Sheet resistance of Al deposits as a function of pre-bake temperature after 30- and 60-min pre-bake.

Figure 4.5 shows the sheet resistance of Al deposits as a function of deposition temperature before and after vacuum annealing at 350˚C for 20 min. All the Al deposits were obtained on Si substrates at 15 mA/cm^2 for 30 min, and their nominal thickness is ~9 μm based on the total charge accumulated during electroplating. It is

clear that the sheet resistance decreases as the deposition temperature increases. The exact reason is still under investigation. One possibility is that higher temperatures keep moisture out of the electroplating solution, reducing the amount of Al_2O_3 in the deposits. Another possibility is that higher temperatures increase the density of the Al deposits, making the resistivity closer to the bulk value.

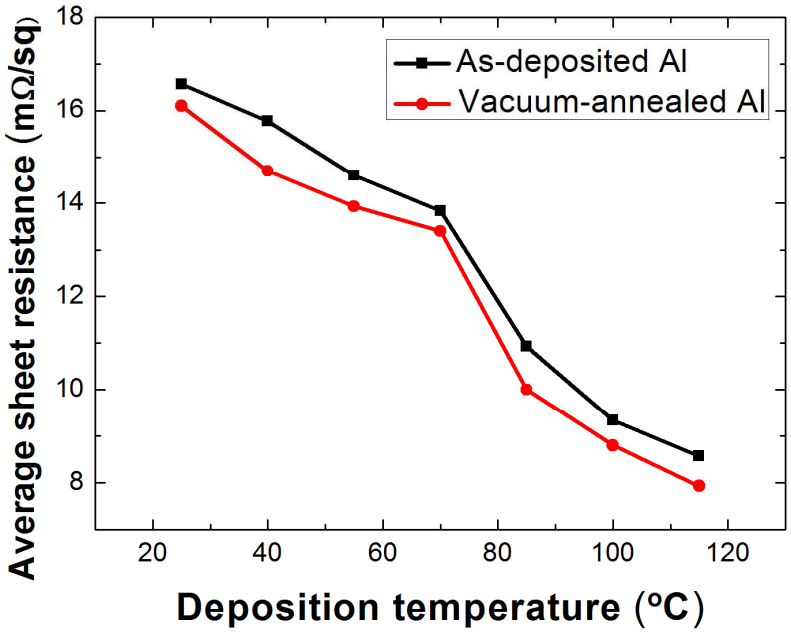

Figure 4.5 Sheet resistance of Al deposits as a function of deposition temperature before and after vacuum annealing at 350˚C for 20 min.

As shown in Fig. 4.5, the sheet resistance of the Al deposits was slightly reduced by post-deposition annealing. This may have resulted from the fact that annealing at higher temperatures than the electroplating temperature further increased the density of the Al film. The minimum sheet resistance obtained is ~8 mΩ/sq for 9-μm Al, corresponding to a resistivity of ~7×10^{-6} Ω-cm. It should be noted that the nominal thickness of the Al deposits was calculated under the assumption of 100% current efficiency. In actuality, the current efficiency should be around 80–90%, meaning that the real thickness of the deposits should be lower than the calculated thickness.

Therefore, the actual resistivity of the Al films could be lower than ~7×10^{-6} Ω-cm.

4.4 Summary

It has been shown that dense and adherent Al deposits with low electrical resistivity can be obtained directly on Si substrates by electroplating over a wide range of temperatures using galvanostatic deposition. Electroplating conditions such as pre-bake conditions, deposition temperature, and post-deposition annealing affect the electrical resistivity of the Al deposits. For reliable and low-resistivity Al deposits, the pre-bake and deposition temperatures should be above 100˚C. The resistivity of electroplated Al is in the high 10^{-6} Ω-cm range, similar to that of screen-printed Ag. The maximum process temperature for electroplated Al is well below 400˚C. This makes Al electroplating a promising metallization method for crystalline-Si solar cells.

CHAPTER 5 ELECTROPLATED ALUMINUM AS THE FRONT ELECTRODE IN CRYSTALLINE-SI SOLAR CELLS

5.1 Introduction

In Chapter 4, we showed that dense and adherent Al films could be reproducibly obtained directly on Si substrates by electroplating and the maximum process temperature could be around 400˚C, well below the typical firing temperatures for Al pastes. In this Chapter, the integration of Al electroplating as the metallization technique for front finger electrode on n-type Si in commercial p-type monocrystalline-Si solar cells from Hareon Solar is reported. In the first section, the design of the front grid pattern for our all-Al solar cells will be introduced, in which the design rules and pattern optimization are investigated. In the subsequent sections, the process flow, cell performance, and issues caused by the fabrication method will be discussed. An all-Al Si solar cell, with an electroplated Al front electrode and a screen-printed Al back electrode, has been successfully demonstrated and its performance has been characterized. To overcome the issue of poorly-adherent Al deposits on Si substrate with >1 Ω-cm resistivity, the electroplated Al front electrode has a Ni seed layer to serve as the adhesion layer. The effect of annealing for the front Al/Ni electrode in air at different temperatures on cell performance has been investigated.

5.2 Design of Front Contact Pattern

In crystalline-Si solar cells, the front contact is usually implemented using a grid of screen-printed metallic paste. The grids typically have two kinds of gridlines: busbars and fingers. Busbars are larger and connected directly to the external leads, while fingers are smaller areas of metallization which collect current for delivery to

the busbars. The key trade-off in top contact design is the balance between the increased resistive losses associated with a widely-spaced grid and the increased shading losses caused by a high fraction of metallization on the top surface.

5.2.1 Parameters

The physical parameters used for the grid design were provided based on industrial datasheets and semi-empirical experience. Let us assume the efficiency of the solar cell is 20% under standard testing conditions (100 mW/cm^2), which corresponds to a power output of 20 mW/cm^2. If the assumed fill-factor (FF) is 80% then the actual power output is 25 mW/cm2. To select the typical values of short-circuit current density (J_{sc}) and open-circuit voltage (V_{oc}), assuming there are no optical or resistive losses, the following equation is used:

$$P_{max} = J_{sc} \times V_{oc}. \quad (5.1)$$

The values used in the calculation are typical of what researchers have obtained on crystalline-Si solar cells: a J_{sc} of 38 mA/cm^2 and a V_{oc} of 0.66 V.

The grid resistance is determined by the resistivity of the metal used to make the metal contact and the aspect ratio of the metallization pattern. A low resistivity and a high metal height-to-width aspect ratio are desirable in solar cells. In practice these parameters are limited by the fabrication technology used to make the solar cell. Here, the resistivity of the Al front finger electrode is assumed to be 9×10^{-6} Ω-cm, and its thickness is 5 μm, which results in a sheet resistance of 0.018 Ω/sq. The sheet resistance of the front n^+ emitter (R_{sheet}) fabricated by phosphorus diffusion is assumed to be 90 Ω/sq. Table 5.1 below summarizes the parameters of the cell used in the pattern design.

Table 5.1 Physical parameters used in the design of front pattern.

Parameter	**Value**	**Description**
FF	80%	Fill-factor
J_{sc}	38 mA/cm^2	Short-circuit current density
V_{oc}	0.66 V	Open-circuit voltage
ρ	9×10^{-6} Ω-cm	Resistivity of Al electrode
T	5×10^{-4} cm	Thickness of Al electrode
R_{sheet}	90 Ω/sq	Sheet resistance of n^+ emitter
A	1 inch^2	Area of the cell

5.2.2 Assumption

In the design of the front contact pattern, the current density is assumed to be generated uniformly across the entire surface of the solar cell. The most accurate method for quantifying resistive losses is based on the fact that current generated in the cell would travel the shortest distance to a finger or busbar, as shown on the left in Figure 5.1. However, to simplify the analysis, it is assumed that current would not travel directly to a busbar and instead only to the nearest finger, as shown by the right image in Figure 5.1. This assumption seems justifiable because it would make the calculated resistive losses larger than what experimental evidence has shown.

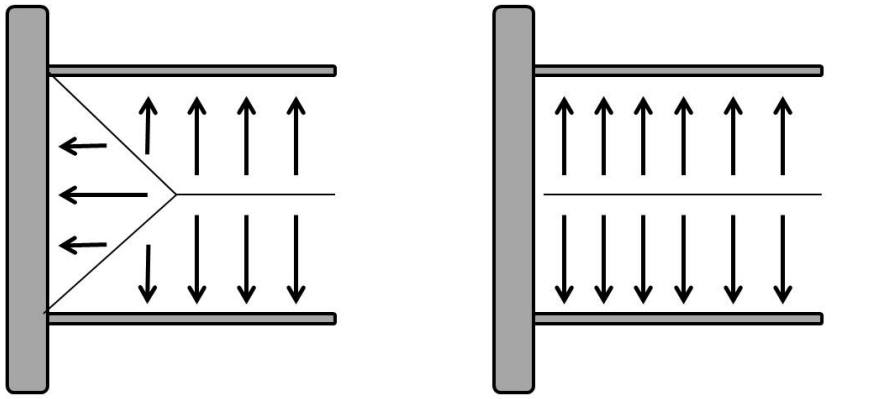

Figure 5.1 Actual vs. assumed behavior of current flow.

5.2.3 Grid Design

For the solar cell fabricated in our lab, the actual area (1 inch by 1 inch) was relatively small, so only one busbar was used in the design. The distance from the tips of each finger and busbar to the edge of cell is set to be 0.1 cm to minimize the effects of shading loss. The quantitative aspects of the design process did not require any complicated numerical calculations. The only design rule followed was to calculate the power loss (P_{loss}) and then express it as a fraction of the maximum cell power (P_{max}). The power loss is a combination of resistive losses in the n^+ emitter layer, resistive losses along the fingers, and resistive losses along the busbar. By scaling the fractional power loss ($P_{\%loss} = P_{loss}/P_{max}$) so that it is level across the entire cell, we were able to optimize the dimensions of the contact pattern.

1) Resistive Losses in Busbar:

Since the probe would be placed in contact with the middle of the busbar during the I-V measurement, only half of the busbar was considered in the calculation of power loss. To get the optimal dimension of busbar width (W_b), we need to find the fraction between the power loss along the busbar and maximum power, which are

both a function of busbar width. Figure 5.2 shows a schematic of the busbar used for the calculation of resistive losses. The length of half busbar is 1.17 cm. The incremental power loss in the section *dL* is given by:

$$dP_{loss} = I^2 dR. \tag{5.2}$$

The lateral current flow (I_1), which includes the shading loss, depends on the distance (L). It is zero at the edge of the cell and increases linearly to its maximum at the middle of the busbar. The equation for the current is:

$$I_1 = J\times(L+0.1)\times 2.54 - J\times L\times W_b, \tag{5.3}$$

where J is the current density (J_{sc} is used in the calculation).

The differential resistance (dR_1) is given by:

$$dR_1 = \rho\times\frac{dL}{W_b\times T}, \tag{5.4}$$

where ρ and T are the resistivity and thickness of the Al electrode, respectively. The equation for the calculation of W_b is:

$$\int_0^{1.17} I_1^2 dR_1 = P_{\%loss}\times 0.038\times 0.66\times(1.27\times 2.54 - W_b\times 1.17). \tag{5.5}$$

If the range of $P_{\%loss}$ is from 2% to 3%, W_b ranging from 0.07 cm to 0.046 cm can be obtained. We chose 0.06 cm as the value of W_b. It should be noted that J_{sc} and V_{oc} are used as the current density and voltage in the calculation. Ideally, the current density and voltage at the maximum power point should be used instead. This means the actual resistive losses along the busbar would be smaller than the one calculated here, which is acceptable for the design.

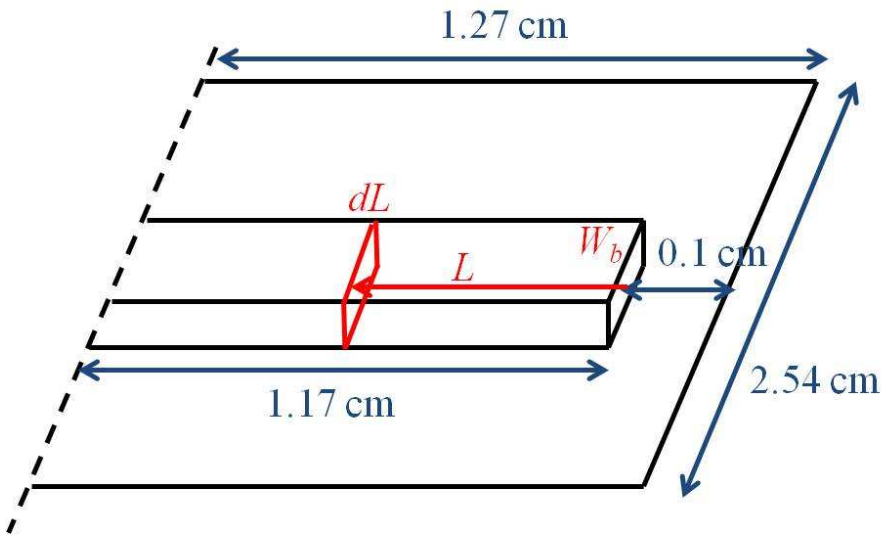

Figure 5.2 Schematic of a busbar used for the calculation of resistive losses. The figure is not drawn to scale.

2) Resistive Losses in n^+ Emitter

Based on the sheet resistance of the front emitter, the power loss due to the emitter resistance can be calculated as a function of finger spacing (S) in the top contact. It should be mentioned that the distance through which current flows in the emitter is not constant. On the one hand, current can be collected from the base close to the finger and therefore has only a short distance to flow to the finger. On the other hand, the length of the resistive path seen by the current is half the finger spacing if the current enters the emitter between the fingers. Figure 5.3 shows a schematic of current flow in the front emitter. The finger length (L_f) is $(2.54-0.06)/2-0.1 = 1.14$cm. The incremental power loss in the section dy has the same form as Equation 5.2. The lateral current flow (I_2), which is zero at the midpoint between grating lines and increases linearly to its maximum at the grating line, is given by:

$$I_2 = J \times 1.14 \times y. \tag{5.6}$$

The differential resistance (dR_2) is given by:

$$dR_2 = R_{sheet} \times \frac{dy}{1.14}. \tag{5.7}$$

The equation for the calculation of S is:

$$\int_0^{S/2} I_2^2 dR_2 = P_{\%loss} \times 0.038 \times 0.66 \times 1.14 \times (S/2). \tag{5.8}$$

By following the same design rule, S ranging from 0.215 cm to 0.264 cm can be obtained if the $P_{\%loss}$ is from 2% to 3%. These values will be included in the calculation of finger width.

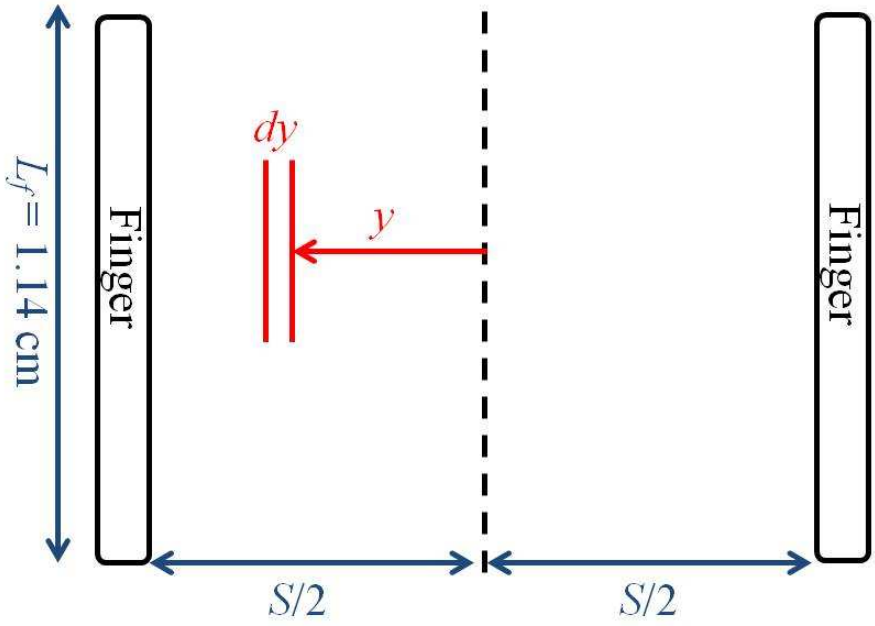

Figure 5.3 Schematic of the current flow in the front emitter.

3) Resistive Losses in Fingers

The power loss along a finger is calculated with the incorporation of finger spacing from the corresponding $P_{\%loss}$ to get the optimal value of finger width (W_f). Figure 5.4 shows a schematic of a finger for the calculation of resistive losses. For the current behavior, it is assumed that the current is uniformly generated and flows perpendicularly into the finger. Consider an element dx at a distance x from the end of the finger. The lateral current flow, including the shading loss, is:

$$I_3 = J\times(x+0.1)\times S + J\times 0.1\times W_f. \tag{5.9}$$

The differential resistance (dR_3) is given by:

$$dR_3 = \rho\times\frac{dx}{W_f\times T}. \tag{5.10}$$

The equation for the calculation of W_f is:

$$\int_0^{1.14} I_3^2 dR_3 = P_{\%loss}\times 0.038\times 0.66\times(1.24\times S + W_f\times 0.1). \tag{5.11}$$

Again, W_f ranging from 57 μm to 47 μm can be obtained if the $P_{\%loss}$ is from 2% to 3%. It should be noted that each $P_{\%loss}$ has a corresponding value of S, which was calculated previously.

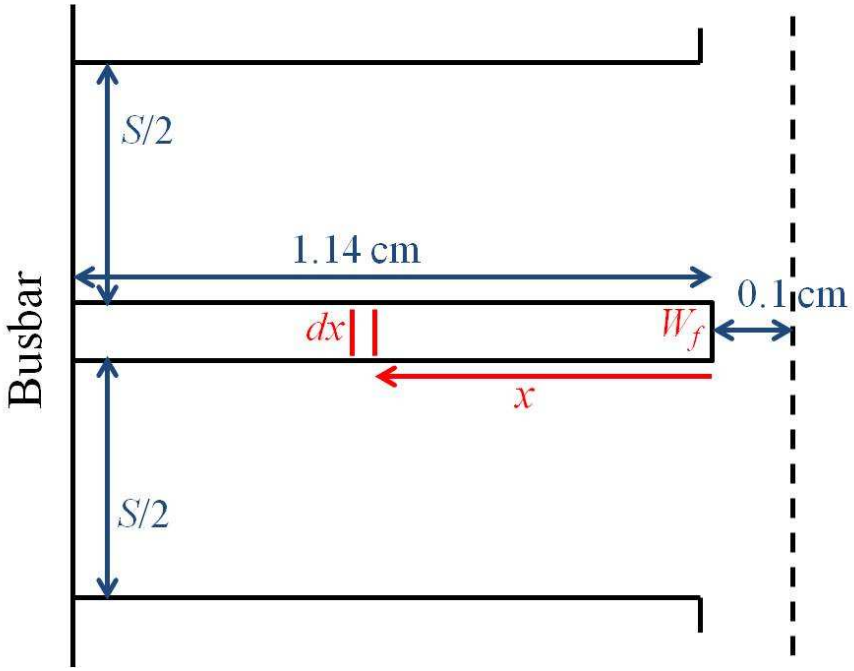

Figure 5.4 Schematic of a finger used for the calculation of resistive losses.

By limiting the $P_{\%loss}$ in the busbar, the emitter, and the finger to the same range and setting the number of fingers on each side of the busbar to be 11, the dimensions of the contact pattern can be obtained. The busbar width is 0.06 cm, the finger spacing is 0.226 cm, and the finger width is 50 μm. For the fractional power loss in each part,

$P_{\%loss}$ in the busbar is 2.31%, $P_{\%loss}$ in the emitter is 2.2%, and $P_{\%loss}$ in the finger is 2.4%.

5.2.4 Optimization

The fractional power loss in the busbar mentioned above is calculated without considering the shading loss caused by the fingers. To include the shading from the rectangular fingers, the area of the busbar was divided into 12 segments, for each either factoring in fingers on each side or a lack of fingers. The power loss of each segment was calculated and then added up. The $P_{\%loss}$ in the busbar decreases to 2.27% after the shading of fingers is included.

It was reported that a tapered finger has lower resistive loss than a finger of constant width [16]. To further optimize the pattern design, we changed the rectangle fingers to tapered fingers while keeping the area fixed. This is because the fractional power loss is proportional to the current flow and inversely proportional to the finger width. Thus, by increasing the width near the base of the finger (where current is higher) and tapering down to the tip of the finger (where current is lower) the fractional power loss can be made uniform across the entire area of the finger. Figure 5.5 shows a schematic of a tapered finger and its width at the base and tip. The base and tip width of the finger can be calculated by setting the ratio ($W_{f,tip}/W_{f,base}$) equal the current ratio (I_{tip}/I_{base}):

$$\begin{cases} W_{f,tip} + W_{f,base} = 2 \times 0.005 \\ \dfrac{W_{f,tip}}{W_{f,base}} = \dfrac{I_{tip}}{I_{base}} = \dfrac{0.038 \times 0.1 \times (0.226 + 0.005)}{0.038 \times 1.24 \times (0.226 + 0.005) - 0.038 \times 1.14 \times 0.005} \end{cases}. \quad (5.12)$$

From the above simultaneous equations, the tip width is 8 μm, and the base width is 92 μm.

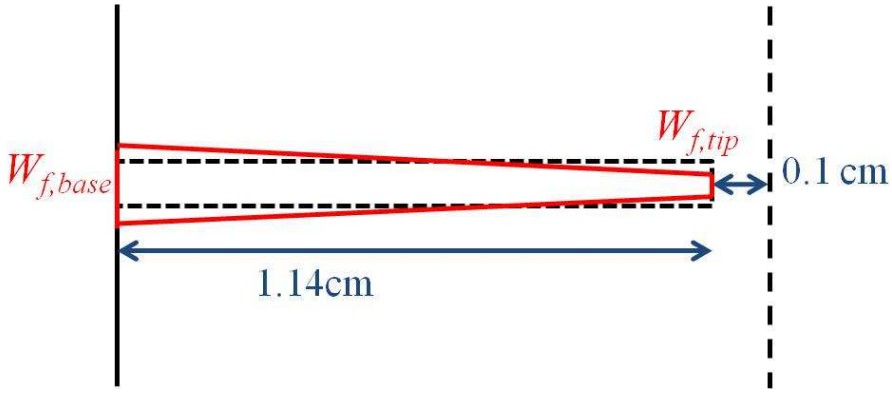

Figure 5.5 Schematic of a tapered finger for the calculation of its width.

After the rectangular fingers are changed to tapered fingers, the $P_{\%loss}$ in the finger drops to 2.12%. The tip and base width would still be different from the optimal values as a result of metallization techniques. The minimum line-width of the metal contact is limited by which technique researchers use. An 8μm-wide finger cannot be achieved by screen printing through the mask, but it is possible to achieve that by electroplating on the opening of dielectric layer. The metallization fraction of the final contact pattern is ~4.5%, and the sketch of final design is shown in Figure 5.6.

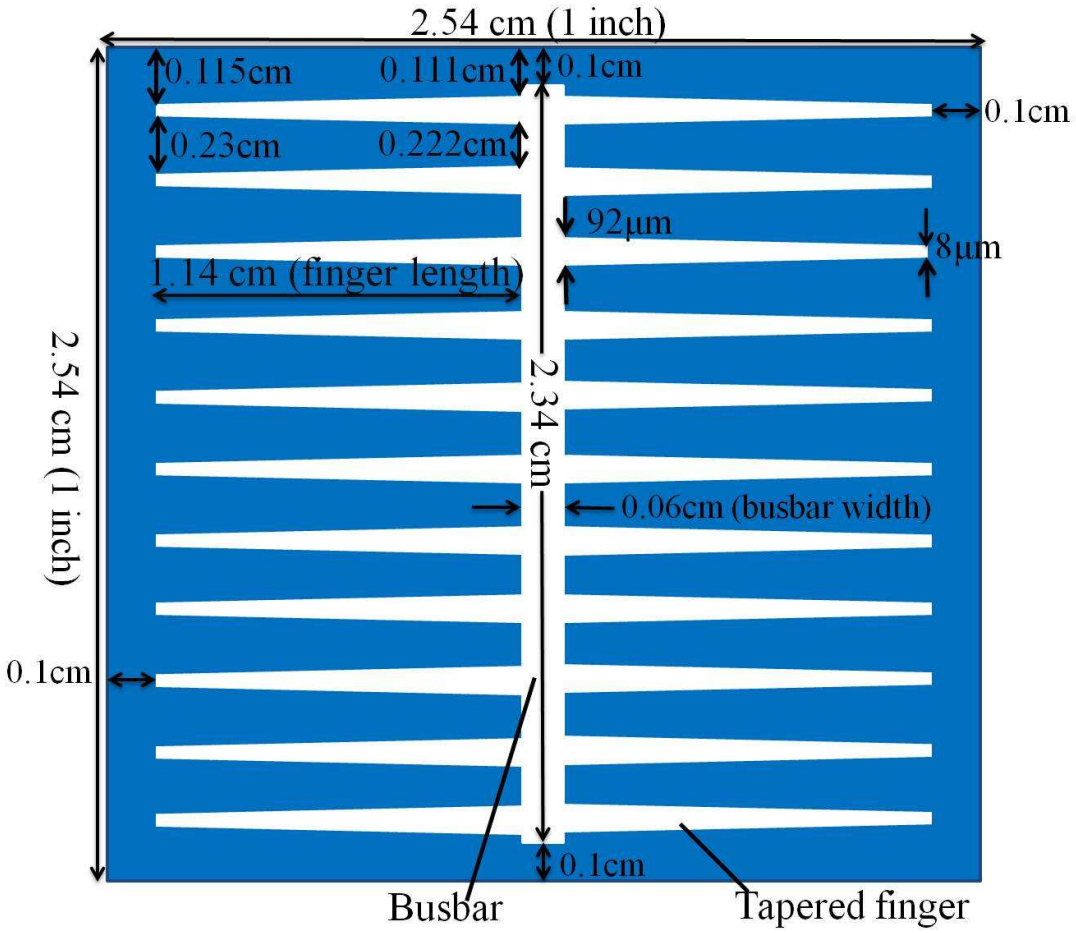

Figure 5.6 A sketch of the final grid design for the front Al electrode.

5.3 Experimental

Partially-processed commercial p-type monocrystalline-Si solar cells with a front SiN_x coating, an n^+ front emitter, a p^+ back-surface field and a screen-printed Al back electrode were obtained from Hareon Solar. All the subsequent processes for patterning and metallization were performed at ASU. The process flow for this all-Al p-type Si solar cell is shown in Figure 5.7. The cell fabrication starts with a 12.5×12.5 cm^2, p-type, CZ Si(100) wafer. After random pyramid texturing, the thickness of the wafer is ~170 μm. Phosphorus diffusion is performed on the front side using phosphoryl chloride ($POCl_3$) to form the n^+ emitter with a sheet resistance of 90±5 Ω/sq. A layer of SiN_x (~75 nm) is deposited on the n^+ emitter by PECVD after

removal of the phosphosilicate glass. Subsequently, the backside Al electrode is screen printed and then the wafer goes through a firing step at ~750˚C, which forms the p^+ back-surface field.

When the partially-processed monocrystalline-Si cells were received, they were cut into small cells of 3.75×5 cm^2 for front-side patterning and metallization. The size of the cells is limited by our electroplating tool. The front SiN_x layer was patterned by photolithography, followed by sputter deposition of Ni (~200 nm) over the patterned photoresist. It should be noted that laser ablation is likely more cost-effective for patterning the SiN_x layer. For the deposition of the Ni seed layer, electroless plating or light-induced electroplating are actually production-ready. Unfortunately we have no such capabilities. The Ni seed layer is required to facilitate Al electroplating since electroplated Al on Si substrates with over 1 Ω-cm resistivity shows poor adhesion. Our choice of Ni as the seed layer is compatible with the Cu electroplating process being developed for crystalline-Si solar cells. It was found that dense and adherent Al finger electrodes can be electroplated onto a Ni seed layer.

The lift-off step was performed by dipping the cells into acetone in an ultrasonic bath, which removed Ni over photoresist and left Ni only in the openings of the SiN_x layer. Electroplating of Al on Ni was carried out in an ionic liquid, consisting of a mixture of $AlCl_3$ and (EMIM)$AlCl_4$, prepared in a dry nitrogen box. Prior to electroplating, the ionic liquid was baked to drive out any moisture in it. The Ni surface was cleaned by a short dip in diluted hydrochloric acid, followed by a deionized water rinse. During electroplating, the backside of the Si cell was covered with a Teflon sheet to limit Al deposition to only the front Ni seed layer. Al electroplating was self-aligned and conducted under a constant current density of ~15 mA/cm^2 at a temperature of ~80˚C. The thickness of the resultant Al layer is ~25 μm.

A final annealing was performed in a rapid-thermal processing furnace in air at temperatures ranging from 150˚C to 400˚C for 1 min to improve the front Al/Ni contact.

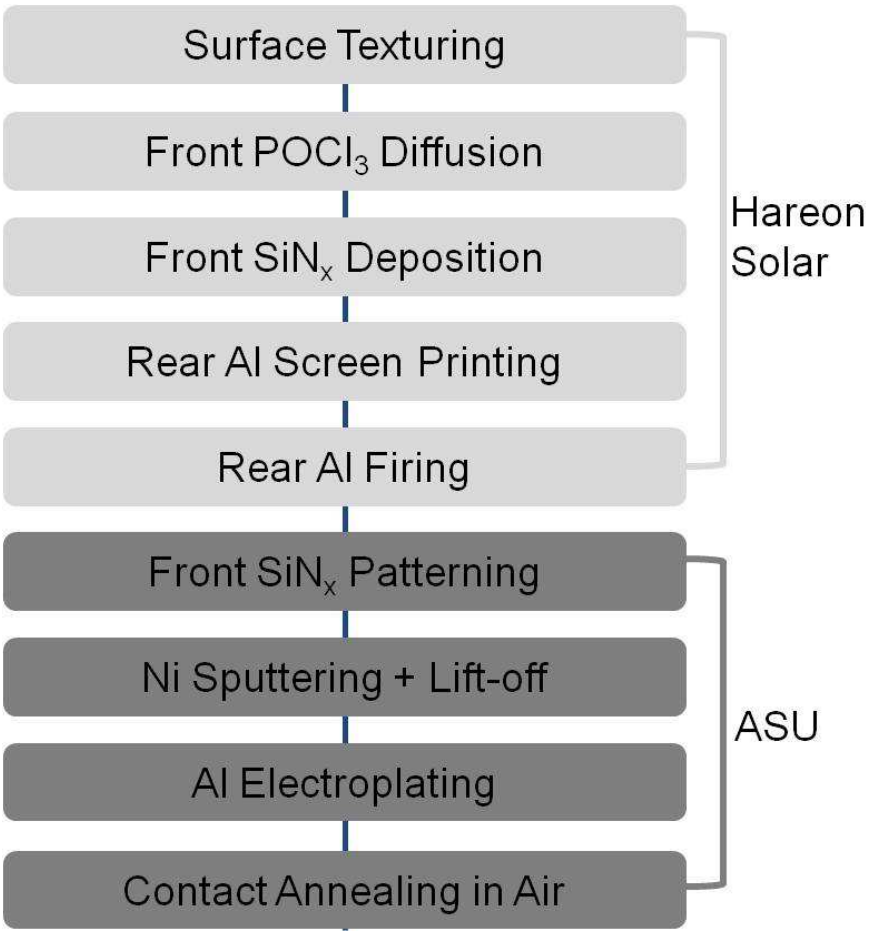

Figure 5.7 Fabrication process flow for an all-Al p-type crystalline-Si solar cell.

Figure 5.8 shows a schematic cross-section of the all-Al p-type Si solar cell obtained. Figure 5.9 is a photograph of a finished all-Al cell, with a size of 2.54×2.54 cm^2. The two rectangular pads next to the cell are the contact points for electroplating of Al. The electroplated Al on the Ni seed layer is dense and continuous along the finger openings, as shown in Figure 5.9. To characterize the Al deposit on the Ni seed layer, the composition and crystal structure were examined by EDX and XRD. The performance of the cell with different annealing temperatures was characterized by a solar simulator. Electroluminescence (EL) was conducted to reveal process

imperfections and surface defects of the cell.

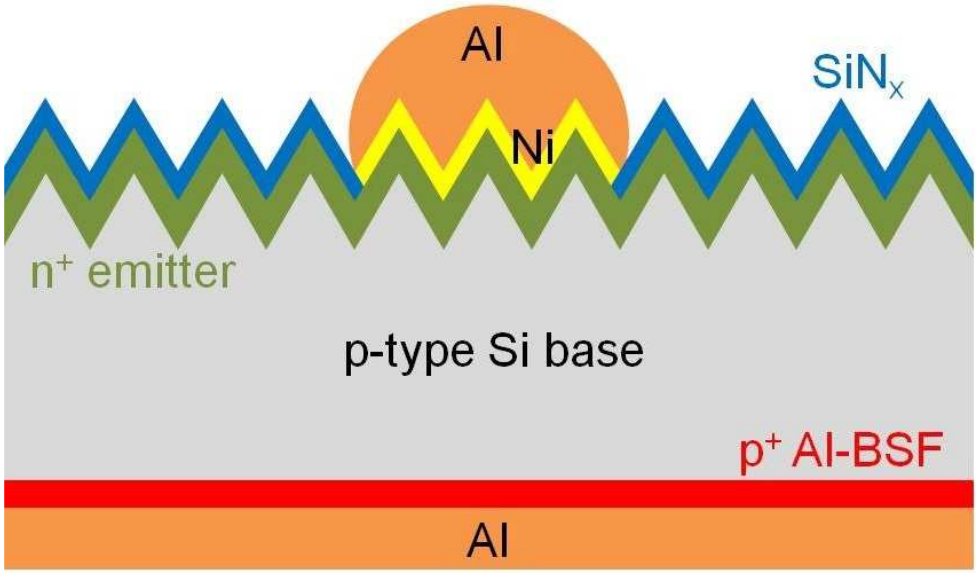

Figure 5.8 Schematic cross-section of an all-Al p-type crystalline Si solar cell.

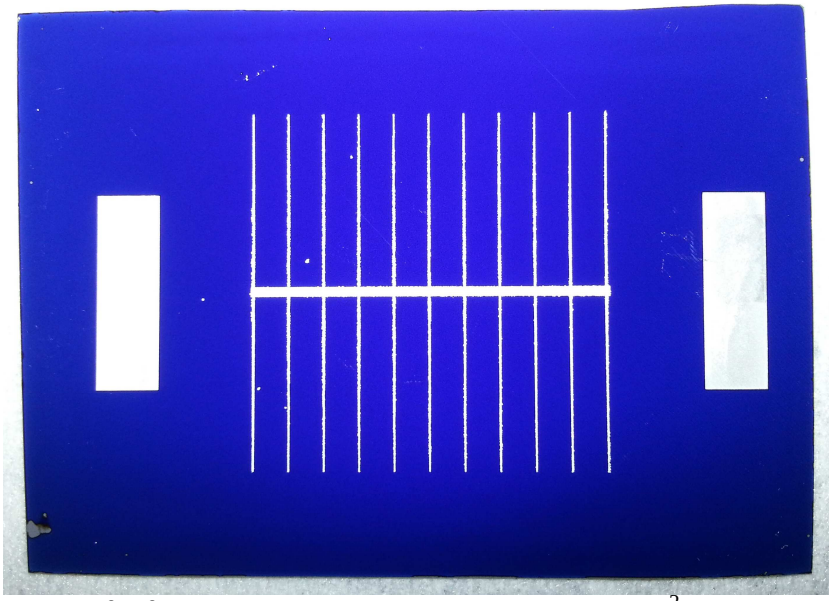

Figure 5.9 Photo of a finished all-Al p-type cell (2.54×2.54 cm^2) with electroplated Al front and screen-printed Al back electrodes.

5.4 Results and Discussion

Figure 5.10 shows the EDX analysis and XRD pattern of electroplated Al on a Ni seed layer. In Fig. 5.10(a), the deposit displays only one strong peak of Al around 1.5 keV without any other peaks of different materials, suggesting a pure Al deposit. As

shown in Fig. 5.10(b), all four peaks of the deposit are related to Al and identified as Al(111), (200), (220), and (311), respectively, further confirming that the composition of the deposit is pure metallic Al.

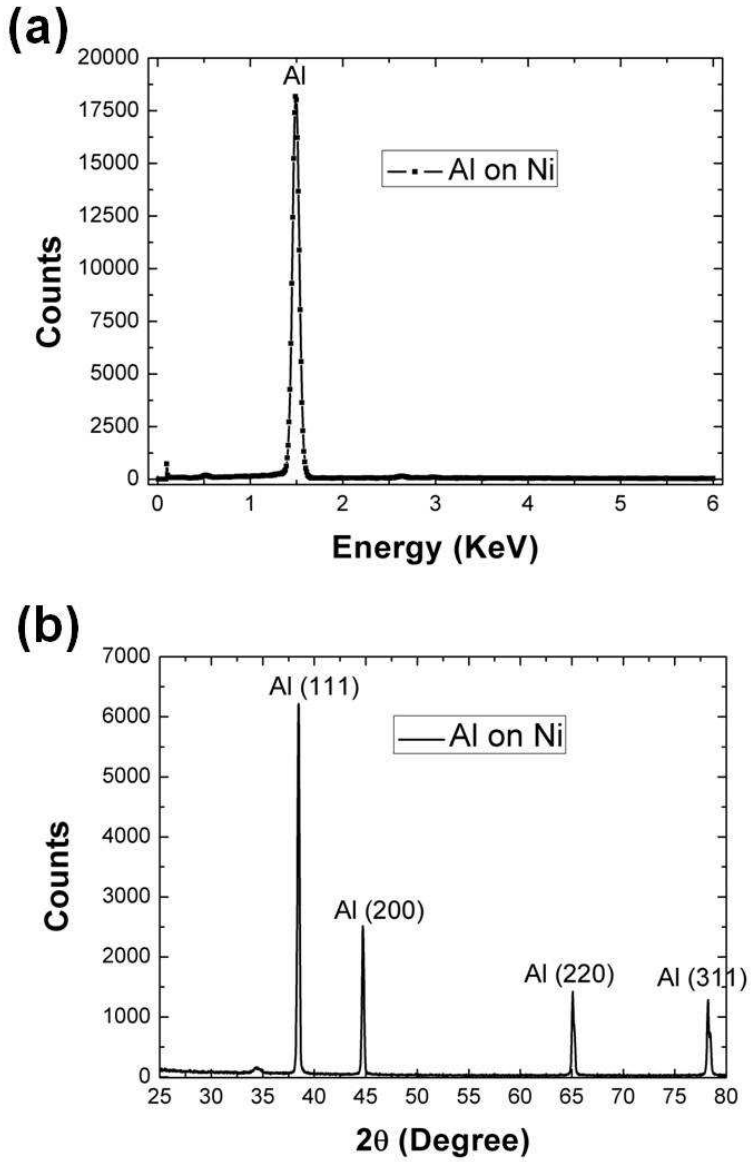

Figure 5.10 (a) EDX spectrum and (b) XRD pattern of electroplated Al on a Ni seed layer.

The effect of final annealing in air at temperatures from 150˚C to 400˚C on cell performance has been examined. The cell was characterized under standard conditions: AM 1.5G, 100 mW/cm^2, 25˚C. The area of the cell is 2.54×2.54 cm^2, and the front finger electrode accounts for ~4.5% of the cell area. Table 5.2 summarizes the one-sun

parameters of the all-Al p-type Si cell at three different annealing temperatures. Figure 5.11 shows the normalized efficiency of the cell as a function of contact annealing temperature. The normalized efficiency is defined as the ratio of η/η_o, where η is the measured efficiency and η_o is the efficiency of the cell before annealing.

Table 5.2 One-sun parameters of an all-Al Si solar cell with three different annealing temperatures.

	V_{oc} (mV)	**J_{sc} (mA/cm^2)**	**FF (%)**	**η (%)**	**R_{sh} (Ωcm^2)**	**R_s (Ωcm^2)**
No annealing	617	35.84	64.3	14.2	181	0.75
Annealed at 200˚C (best)	626	35.98	64.6	14.6	212	0.79
Annealed at 400˚C	601	35.56	50.9	10.7	23	1.65

In Table 5.2, it can be seen that the cell before annealing already shows a low shunt resistance (R_{sh}) of 181 Ω-cm^2, which we believe is the reason for the low fill-factor of 64.3%. A possible reason for the low shunt resistance is the possible damage to the shallow emitter junction during front SiN_x patterning by photolithography. Multiple rounds of cell fabrication have been carried out to optimize the shunt resistance, as shown in Figure 5.12. In each fabrication round, we modified only the photolithography step to minimize damage to the emitter junction. It is noted that the cell efficiency improves with an increasing shunt resistance. Further optimization of the front patterning process is needed. Alternatively, laser ablation should be employed here due to its less damage to the emitter junction, and it is faster and cleaner than photolithography. On the other hand, the cell without annealing shows good performance in short-circuit current density (J_{sc}) and series

resistance (R_s), suggesting that the electroplated Al is continuous without voids and thus low resistivity.

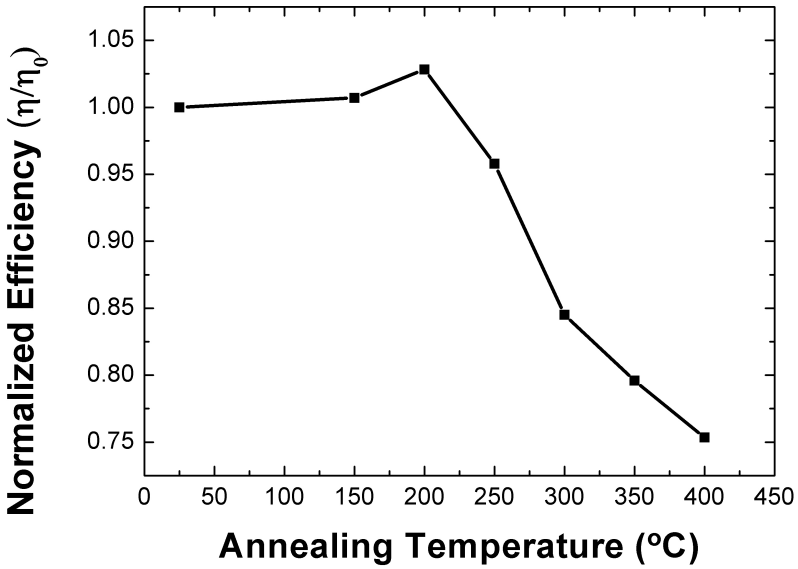

Figure 5.11 Normalized efficiency of an all-Al p-type cell as a function of contact annealing temperature.

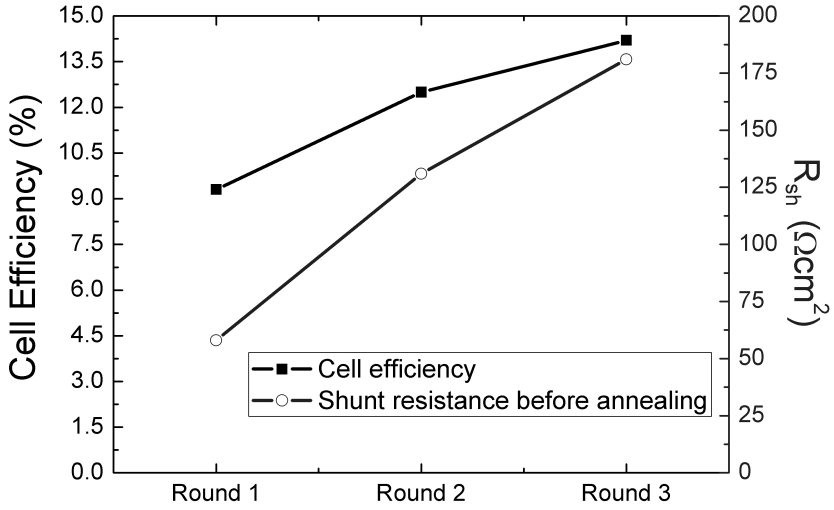

Figure 5.12 Comparison of cell efficiency and shunt resistance between fabrication rounds.

As shown in Figure 5.11 and Table 5.2, annealing at 200˚C results in a slightly-increased open-circuit voltage (V_{oc}) and fill factor (FF). However, the efficiency drops drastically when the annealing temperature exceeds 200˚C. This is different from the Cu/Ni electrode which is annealed between 250˚C and 400˚C in an inert gas [31]. As the annealing temperature goes above 250˚C, the shunt resistance starts to decrease and eventually reaches 23 Ω-cm^2 and the series resistance starts to increase all the way to 1.65 Ω-cm^2 at 400˚C. At the same time, the open-circuit voltage is reduced by 25 mV between 200˚C and 400˚C.

There are multiple reasons for the effect of annealing temperature on cell performance. Our annealing furnace is not a dedicated, clean Si furnace, so there can be metallic contaminations into the cell during annealing for the lower open-circuit voltage. The formation temperature of Ni silicide starts at 250˚C. Its formation at the Ni/Si interface increases the series resistance while thinning the emitter junction. The later reduces the shunt resistance of the cell. Another possibility for the increased series resistance is the increased Al_2O_3 thickness in the Al electrode when the annealing temperature exceeds 200˚C. Further investigation into different annealing environments for electroplated Al is needed.

Figure 5.13 is an EL image of an all-Al p-type cell. The light intensity of the image is inversely proportional to the local resistance, so poorly contacted and resistive regions show up as dim and dark areas. It can be seen that the areas between finger electrodes are dim, suggesting that the emitter junction may be too shallow and has a relatively high sheet resistance. This supports our hypothesis that the emitter junction is shallow and can be easily damaged during patterning. Dark straight marks in the image are likely caused by scratching during shipping, which are another possible reason for the low shunt resistance of the cell.

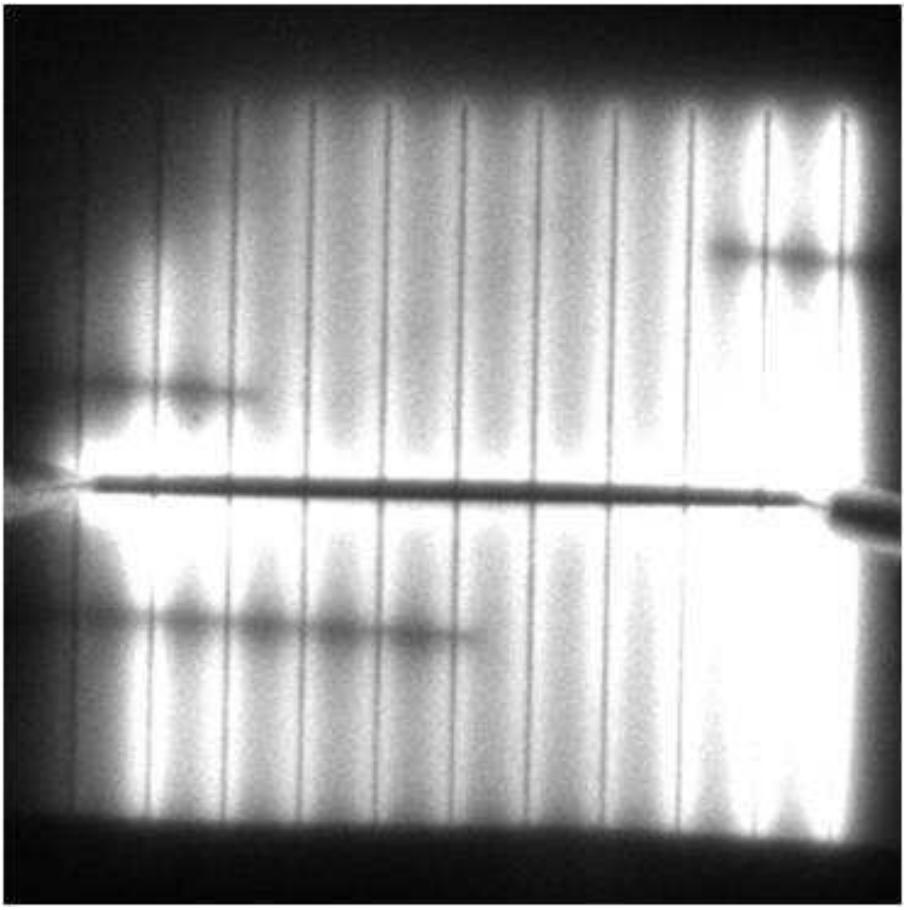

Figure 5.13 EL image of an all-Al p-type mono-Si solar cell.

Figure 5.14 is the I-V curve under one-sun illumination for the all-Al p-type cell after annealing at 200˚C, which is one of the best-efficiency cells so far. The efficiency is 14.6% with an open-circuit voltage of 626 mV, a short-circuit current of ~36 mA/cm^2, and a fill factor of 64.6%. The fill factor still has room for improvement, which may be limited by the patterning process for the SiN_x layer. If a higher fill factor of 80% can be achieved, the efficiency of this all-Al cell will reach 18%. This shows both the potential of Al electroplating as the metallization process for the front finger electrode on n-type Si and the importance of an appropriate patterning process for the front SiN_x layer.

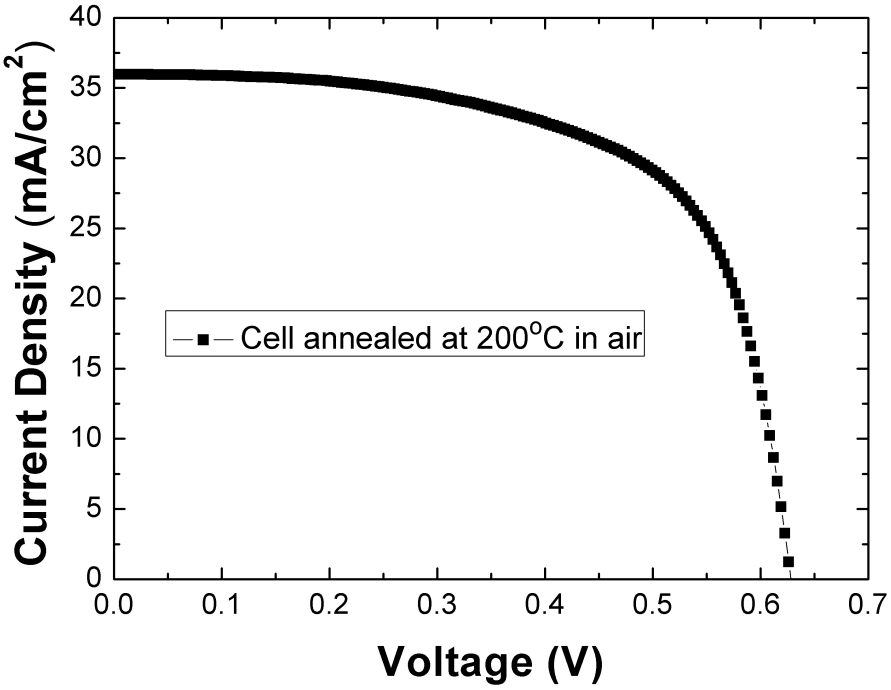

Figure 5.14 I-V curve under one-sun illumination for an all-Al p-type Si solar cell annealed at 200˚C.

5.5 Summary

An all-Al p-type mono-Si solar cell, with an electroplated Al front electrode and a screen-printed Al back electrode, has been demonstrated. The cell is fabricated on partially-processed commercial p-type mono-Si cells obtained from a production line. It is shown that dense, continuous and pure metallic Al fingers can be electroplated onto a Ni seed layer. The effect of annealing for the Al/Ni electrode in air at different temperatures on the performance of the cell has been investigated. Annealing at 200˚C results in the best-performance cell with an efficiency of 14.6%. Further optimization of the cell fabrication process, in particular a suitable patterning technique for the front SiN_x layer, is expected to increase the efficiency of the cell to ~18%.

CHAPTER 6 CONCLUSION AND FUTURE OUTLOOK

6.1 Conclusion

Crystalline-Si solar cells dominate the PV industry with ~90% of commercial market share today thanks to the well-developed technology established by the Si-based microelectronics industry. Despite the rapid growth in global installed capacity and significant drop in module price, the relatively high manufacturing cost associated with crystalline-Si solar cells is one of the main roadblocks to widespread utilization of solar electricity. In order to reach grid parity, the reduction of manufacturing costs by using low-cost processing techniques and materials has been a key focus of Si-PV research. This work proposed an alternative metallization technique to address the cost issue associated with front Ag electrodes of crystalline-Si solar cells, which is room-temperature Al electroplaing. It has been found that dense and adherent Al deposits with low electrical resistivity can be obtained directly on Si substrates by electroplating over a wide range of temperatures. For reliable and low-resistivity Al deposits, the pre-bake and deposition temperatures should be slightly above 100˚C. The resistivity of electroplated Al is in the high 10^{-6} Ω-cm range, similar to that of screen-printed Ag. Compared to screen-printed Al with >700˚C firing temperature, the maximum process temperature for electroplated Al is well below 400˚C, which is beneficial for the n-side metallization of Si solar cells.

With the advantages of being a non-vacuumed and low-temperature metallization technique, Al electroplating has been integrated into the fabrication of commercial p-type monocrystalline-Si solar cells. Photolithography is employed to pattern the front SiN_x dielectric layer, but laser ablation is a better choice due to the fact that it is faster and cleaner. To overcome the issue of poorly-adherent Al deposits on Si substrates with >1 Ω-cm resistivity, the electroplated Al front electrode has a Ni seed

layer to facilitate the current distribution during plating. It has been found that dense, continuous and pure metallic Al fingers can be electroplated onto a Ni seed layer. An all-Al p-type mono-Si solar cell, with an electroplated Al front electrode and a screen-printed Al back electrode, has been successfully demonstrated. Annealing at 200˚C results in the best-performing cell with an efficiency of 14.6%. This shows that Al electroplating is a promising candidate of metallization techniques to substitute for conventional screen-printing of Ag electrodes. Further optimization of the cell fabrication process, in particular a suitable patterning technique for the front SiN_x layer, is expected to increase the efficiency of the cell to ~18%.

6.2 Future Outlook

The cell structure with electroplated Al front electrode discussed in Chapter 5 is based on p-type Si wafers. Currently, about 93% of crystalline-Si module production is based on p-type Si wafers while the n-type Si wafers only have a market share of 7%, as shown in Figure 6.1 [27]. This is due to two main reasons:

1) Until 1980s, PV was mostly used for space applications where p-type Si is more durable since it is more tolerant to high energy particle radiation in space.

2) The processing sequence, particularly the phosphorus diffusion for the n^+ emitter formation, is well established in industrial solar cell production for many years.

However, many researchers have studied phosphorus-doped n-type Si for PV since then and confirmed its superior electrical properties compared to the p-type Si. First, n-type Si is less sensitive to the harmful metallic impurities, such as interstitial Fe (Fe_i), which are usually present in the feedstock Si or introduced during cell manufacturing. These impurities can degrade bulk lifetime and cell performance by

introducing SRH recombination centers. Therefore, n-type Si has higher minority carrier lifetime and longer diffusion length compared to p-type Si with a similar impurity concentration, which provides n-type Si solar cells opportunity to achieve higher cell efficiency than p-type Si solar cells [60]. Second, due to the absence of boron, n-type Si does not suffer from light-induced degradation (LID) which can cause reduction in 0.5~1% absolute cell efficiency [61]. The LID is cause by boron-oxygen (B-O) complexes which are formed by prolonged light exposure of boron-doped p-type Si.

As a consequence, cell structures based on n-type Si wafers have attracted considerable attention in the research and development of Si solar cells in recent years, including the development of industrial tools and technologies for commercializing n-type Si cells. SunPower and Panasonic are two of the companies which use n-type Si wafers for high efficiency solar modules today. According to the ITRPV, it was predicted that the market share of n-type monocrystalline Si may reach ~30% by 2022. This underlines the potential of this material in industrial manufacturing.

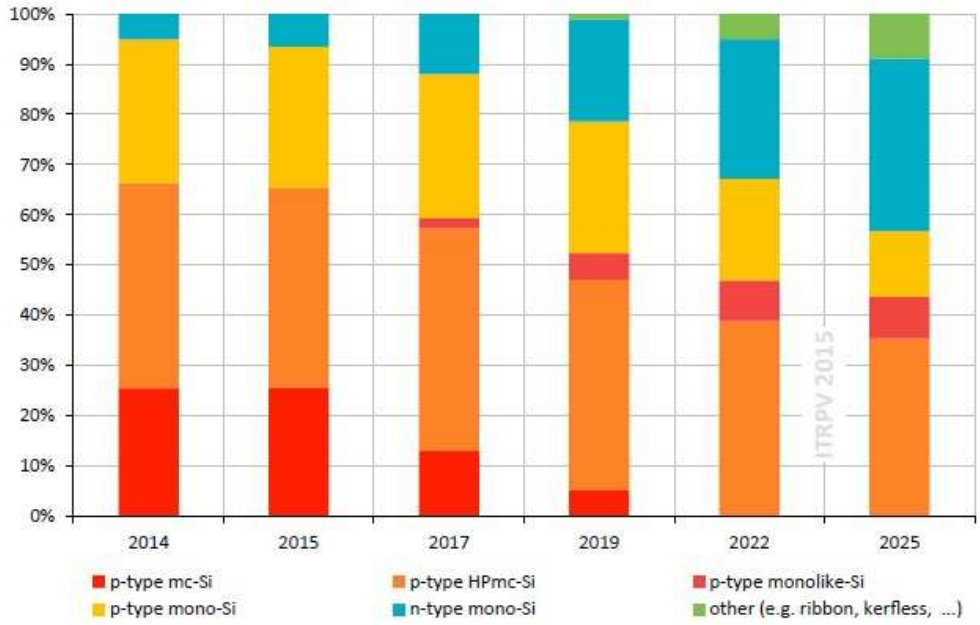

Figure 6.1 World market shares for different types of Si wafers.

In our future plan, crystalline-Si solar cells based on n-type Si wafers with all-Al electrodes will be fabricated. The cell structure will feature an Al-alloyed p^+ rear emitter and an n^+ front surface field (FSF). The advantage of placing n^+ surface field on the front side is that the damage to the shallow emitter junction can be avoided when photolithography is used for patterning the front dielectric layer. For solar cells with a rear emitter or back junction, the quality of Si wafers has to be high, i.e. this type of solar cells is mainly restricted to monocrystalline Si. Figure 6.2 schematically illustrates the cell structure.

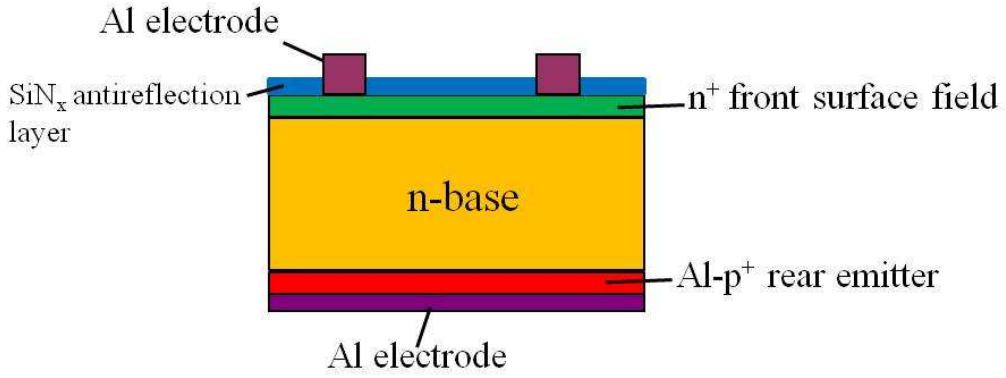

Figure 6.2 Schematic of solar cell structure with an Al-p+ rear emitter. Surface texturing is not shown.

The proposed fabrication process flow for an n-type Si solar cell featuring a rear emitter and all-Al electrodes is shown in Figure 6.3. The processing starts with a (100)-oriented phosphorus-doped n-type CZ Si wafer with a resistivity of ~5 Ω-cm and thickness of 200 μm. The Si wafer is first textured with random pyramids in a NaOH/isopropanol solution at 70°C. Then, phosphorus diffusion is performed on the front side using $POCl_3$ source in a tube furnace around 850°C to form an n^+ FSF. After the removal of phosphorus silicate glass, a 75 nm thick SiNx antireflection coating is deposited by PECVD on the n^+ FSF. Subsequently, the backside Al electrode is screen printed and then the wafer goes through a firing step at ~750˚C, which forms the

Al-alloyed p^+ rear emitter. The firing time and temperature should be carefully controlled to optimize the depth of p^+ layer and to prevent voids from forming at the interface of Al and Al-Si alloys during the firing process. The front SiN_x layer is patterned by photolithography, and the rest of the metallization process will be exactly the same as the steps discussed in Chapter 5. Since the damage to the emitter junction can be avoided, the shunting issue caused by Ni spiking during the contact annealing can be minimized, suggesting the contact annealing may be conducted at a higher temperature.

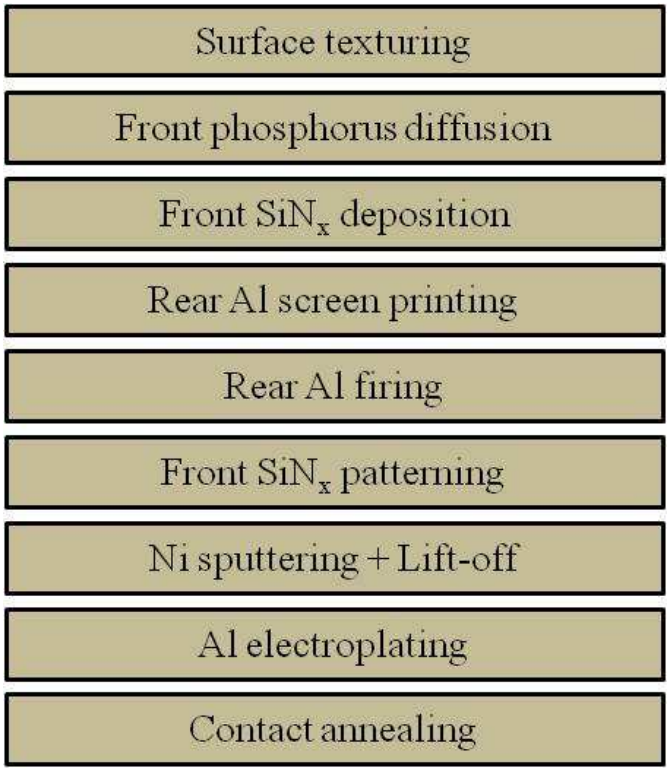

Figure 6.3 Fabrication process flow of an n-type Si solar cell featuring a rear emitter and all-Al electrodes.

Based on the current electroplating setup in our lab, we can only do Al plating on Si solar cells with relatively small areas. The reason why we cannot do plating on large-area cells (156 mm by 156 mm) is due to the fact that the sheet resistance across the entire wafer will be very large even with a metal seed layer. This will lead to the

nonuniformity in thickness of the electroplated Al, which becomes thin on the region far away from the electrical contact. To make Al electroplating a more industry-compatible metallization technique, we need to improve the uniformity of electroplated Al across the whole wafer, which is why the development of light-induced Al plating is desired. As mentioned in Chapter 3, light-induced Cu plating has been investigated extensively by the PV industry and research centers in recent years, and several light-induced plating toolsets for metallization of Si solar cells are either commercially available today or under development. Figure 6.4 shows a schematic of electrochemical cell setup for light-induced Cu plating [63]. The light-induced plating process works on the same principle as the conventional electroplating process. However, the photo-generated carriers from a light source can facilitate the uniform distribution of current density across the grid pattern during plating. The process includes the immersion of a patterned cell into the electrolyte bath with an appropriate light source. A Cu electrode is connected to the anode of a dc voltage source. A protective potential is applied at the back of the solar cell in order to make the rear-side of the cell more cathodic, which helps to reduce the corrosion of the Al back electrode. The photo-generated electrons get swept to the n-side of solar cell by the built-in potential and recombine with the Cu ions, resulting in the deposition of Cu on the metal seed layer. Compared to electroless plating and electroplating, light-induced plating can be done more uniformly across the entire cell as the applied potential can bias the cell such that it operates closer to its short-circuit conditions [64]. Due to this important advantage, development of light-induced Al plating in our lab is included in the future plan.

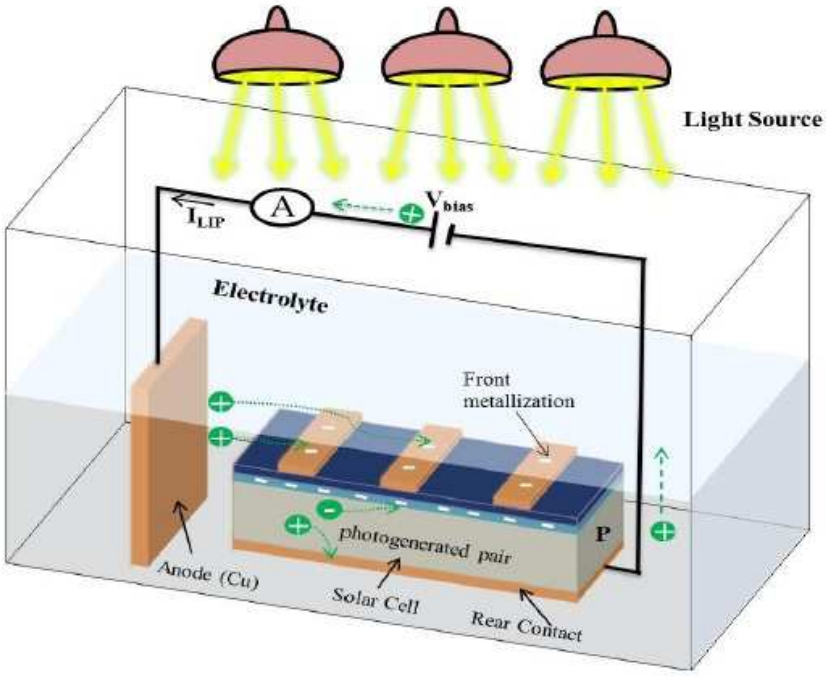

Figure 6.4 Schematic of the electrochemical cell setup for light-induced Cu plating.

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