A Novel Boost Converter Based LED Driver Chip

Targeting Mobile Applications

by

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of the Requirements for the Degree
Doctor of Philosophy

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ABSTRACT

A novel integrated constant current LED driver design on a single chip is developed in this dissertation. The entire design consists of two sections. The first section is a DC-DC switching regulator (boost regulator) as the frontend power supply; the second section is the constant current LED driver system.

In the first section, a pulse width modulated (PWM) peak current mode boost regulator is utilized. The overall boost regulator system and its related sub-cells are explained. Among them, an original error amplifier design, a current sensing circuit and slope compensation circuit are presented.

In the second section – the focus of this dissertation – a highly accurate constant current LED driver system design is unveiled. The detailed description of this highly accurate LED driver system and its related sub-cells are presented. A hybrid PWM and linear current modulation scheme to adjust the LED driver output currents is explained. The novel design ideas to improve the LED current accuracy and channel-to-channel output current mismatch are also explained in detail. These ideas include a novel LED driver system architecture utilizing 1) a dynamic current mirror structure and 2) a closed loop structure to keep the feedback loop of the LED driver active all the time during both PWM on-duty and PWM off-duty periods. Inside the LED driver structure, the driving amplifier with a novel slew rate enhancement circuit to dramatically accelerate its response time is also presented. These novel design ideas have been successfully approved by the technical committee of a large semiconductor company and submitted to US Patent and Trademark Office within three patent applications.

DEDICATION

This PhD work is dedicated to my family.

ACKNOWLEDGMENTS

I highly appreciate Dr. Holbert's extremely patient guidance and work to help my PhD study and Dr. Holbert's critical advices during my difficult times of my PhD progress.

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1 INTRODUCTION

1.1 Lighting Device History

It is believed that humans very possibly began to use lamps in 70,000 BC [1-1]. Particularly, a hollow rock, shell or other naturally found object was used with soaked animal fat for lighting. Since around the 7th century BC, terra cotta lamps were made for lighting purposes instead of using handheld torches.

Modern lighting devices were invented in Europe in the 18th century. During this period, coal and natural gas lamp use became widespread. Around 1784, coal gas was first utilized as a lighting source [1-2].

Early in the 19th century, gaslight became a major street lighting source for most cities in the United States and Europe. Low-pressure sodium and high-pressure mercury lamps were invented and became popular in the 1930s to replace gas lighting for city streets. Then electric lights at the turn of the 19th century were deployed and they replaced gas lighting in homes [1-2].

Sir Joseph Swann in England and Thomas Edison in the USA both invented the first electric incandescent bulbs/lamps in the 1870s. Thomas Edison received U.S. Patent 223,898 [1-3] for his incandescent lamp in 1880.

Friedrich Meyer, Hans Spanner and Edmund Germer in the USA patented a fluorescent lamp in 1927 [1-4]. Elmer Fridrich and Emmett Wiley were approved and granted U.S. Patent 2,883,571 [1-5] for a tungsten halogen lamp — an improved type of incandescent lamp — in 1959.

In the 1960s, the light emitting diode (LED) was invented. In 1962, Nick Holonyack Jr. [1-6] invented the red LED, the first LED of visible light. He used GaAsP (gallium arsenide phosphide) on a GaAs substrate. In 1972, M. George Craford [1-7] [1-8] created the first yellow LED at Monsanto using GaAsP. He also developed a brighter red LED. In 1992, Shuji Nakamura [1-9]

led the development of the world's first bright blue LED using GaN (gallium nitride). This blue LED can be in commercial production. It helped Shuji Nakamura to win the 2014 Nobel Prize in Physics. He was cited "for the invention of efficient blue light-emitting diodes which has enabled bright and energy-saving white light sources" [1-10].

Today, LED lighting use is wide-spread due to its excellent efficiency, its light spectrum modulation and its brightness, which can be easily changed by frequency modulation. A dedicated control circuit driver usually accompanies each LED application.

1.2 LED Industry Trend and Market Capacity

IHS Inc. is a leading global marketing research company for information and analytics. According to its report LED IC DRIVER 2013 [1-11], LED brightness has been steadily improved and the use of new materials allows them to move into new applications. In the 1970s and 1980s, the available LEDs were mostly used in status lights. In the 1990s, higher brightness nitride LEDs were created, permitting such LEDs to be used for backlighting in consumer devices and other applications. It also allowed white LEDs to be developed using phosphors. Strong application and market growth occurred up to 2005, but the growth slowed down for several years due to the mobile handset market saturation. Figure 1 shows the LED driver IC worldwide market trend based on IHS data.

The situation changed in 2010 due primarily to economic recovery and the growth of LED-backlit televisions. Strong growth continued after 2010, primarily driven by the use of LED backlighting in consumer applications such as TVs, general-purpose lighting and notebook backlighting.

Based on IHS's report, the LED driver integrated chips (IC) market reached about $1 billion in 2012. These ICs are important supporting and controlling electronic components for LED lighting applications.

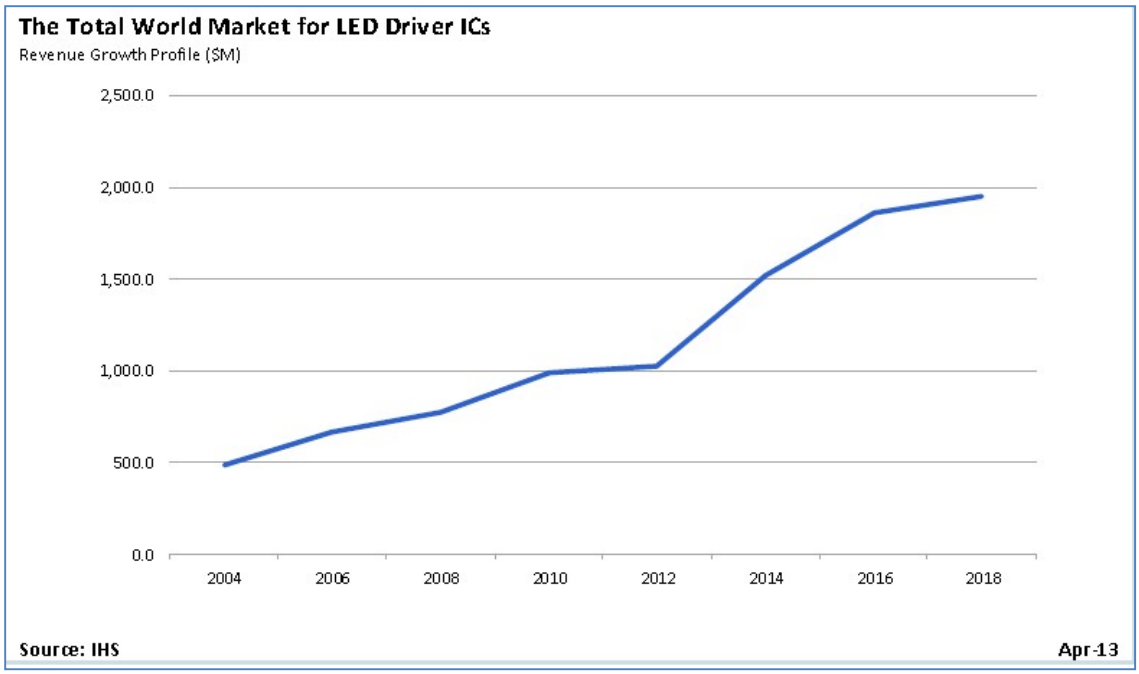


Figure 1. Worldwide LED Driver IC Market Projection [1-11].

1.3 LED Performance Requirement and Application Areas

LEDs are devices that generate light with a low DC voltage supply source. Their brightness increases with the current through them. LED lighting can be controlled better if their DC current can be well regulated. In addition, the LED must be protected from over current and/or over voltage conditions, and voltage fluctuations. Otherwise, LEDs may perform poorly and show unwanted light flickers, or they can even be damaged permanently.

Additionally, the light spectrum of any LED device is dependent on the current through it. It is usually a common practice to use the LED driver IC to control and maintain a targeted constant LED current among all LEDs over operation. Therefore, a PWM (pulse width modulation) signal is

used to turn on and turn off a LED to adjust the overall brightness. LEDs are most likely arranged into multiple channels with multiple LEDs within each channel.

The LED driver IC application market can usually be divided into the following major types [1-11]:

- Backlighting – such as backlighting for LED displays;
- Camera flash – illumination for photographs;
- Integrated IC – multiple functions on one IC;
- Illumination – used to drive LEDs to light up a physical space or area, including all automatic exterior lighting lamps;
- High resolution displays where LEDs are the display components other than backlighting;
- Low resolution displays such as channel letters, traffic lights and signs; and
- Seven segment/dot matrix displays.

1.4 The Basic LED Driver Structure

The common structure of a LED driver system is shown in Figure 2. The system is usually configured as a frontend power supply regulator connected to backend linear current driver(s) to drive single/multiple LED strings.

The backend current driver controls the specified constant current through LEDs. The backend current drivers can be replaced by precision resistors. This is popular in some less integrated applications where the resistors are not integrated on chip and current does not need to be adjusted over a wide range. For a backlighting application in which the LED currents need to be adjusted over a wide range, such as a 1:4000 ratio, well designed backend current drivers are necessary.

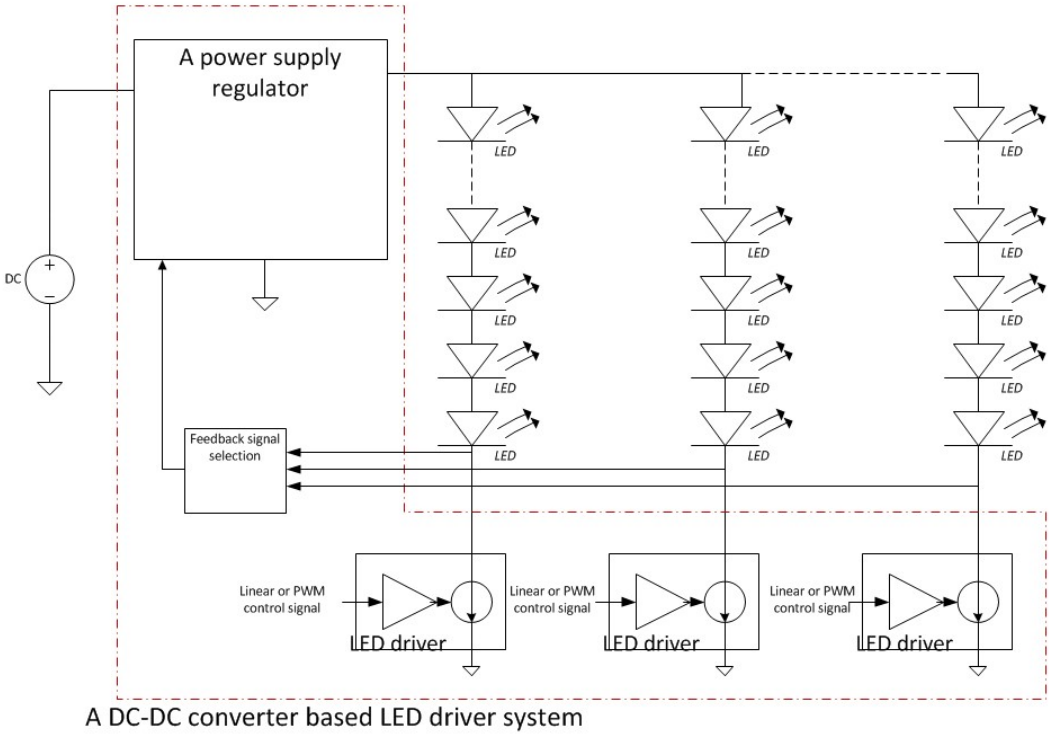


Figure 2. A DC-DC Converter Based LED Driver System

The power supply regulator can be a linear regulator (i.e. low drop out regulator or LDO), a switching mode regulator (such as a buck, boost or a buck-boost, etc.), or simply some resistors which are used to limit current.

Based on the market data [1-11], the power supply regulator in today's designs is a switching mode regulator which can reach up to typically 90%-95% efficiency in today's mobile applications of smart phones and tablets, computer applications such as laptops, and general applications such as high definition TV screens, etc.

In most recent mobile applications, a boost regulator is usually used as the power supply regulator because the lithium-ion battery supply voltage is generally in the range of 2.7 V to 4.2 V, while a string of LEDs needs voltage from around 15 V to 40 V. This is a suitable condition for a boost regulator as the front-end power supply regulator.

1.5 The Proposed Design Target and Its Application Area

In this dissertation, a boost regulator based LED driver targeting mobile applications (e.g., tablets and smart phones) is developed. Since mobile applications use batteries as their power supply, the major requirements for this design are as follows:

1. Very high LED current accuracy with very low channel-to-channel mismatch among the currents from different LED current drivers on the same chip.
2. The LED current extraction ratio needs to be in the range of 1:4000.
3. Hybrid LED current control (PWM dimming at <25% current level and linear dimming at >25% current level). It helps to improve accuracy at low current level and save power at high current level.
4. High efficiency, which requires 1) low quiescent and 2) efficient design for the boost regulator, to help to extend battery life.
5. Small die area to save cost. These mobile applications belong to consumer electronics. The total price of a device is a relatively sensitive issue for the end users – i.e. consumers. Therefore, a low cost design is preferred.

The function diagram of the developed design in this dissertation is in Figure 3. In the system, one boost regulator, which integrates all the control circuit and power NMOS switches on chip, supplies the current to the 6 parallel LED drivers. The reason for 6 parallel LED drivers is because an electronic device such as a tablet computer needs typically 6 LED strings for backlighting. In comparison, a smart phone typically only needs 3 LED strings. The design in this dissertation primarily targets tablet applications.

The boost regulator utilizes a PWM peak current mode structure. Its inductor and synchronizing diode are off-chip. Its associated supporting circuits such as bandgap reference, clock generator and spectrum spreading circuits are all on chip.

The currents from the 6 parallel constant current LED drivers are controlled by linear dimming and/or PWM dimming digital logic signals, which are sent to chip via a digital interface. The minimum voltage of the bottom voltages of the 6 LED strings is selected via a minimum voltage selection circuit, then it is sent to the boost regulator to form its feedback control loop.

The primary focus of this dissertation is to achieve a high performance design for those constant current LED drivers. A boost regulator is also added into the design since it is needed to supply the power and form the feedback control loop.

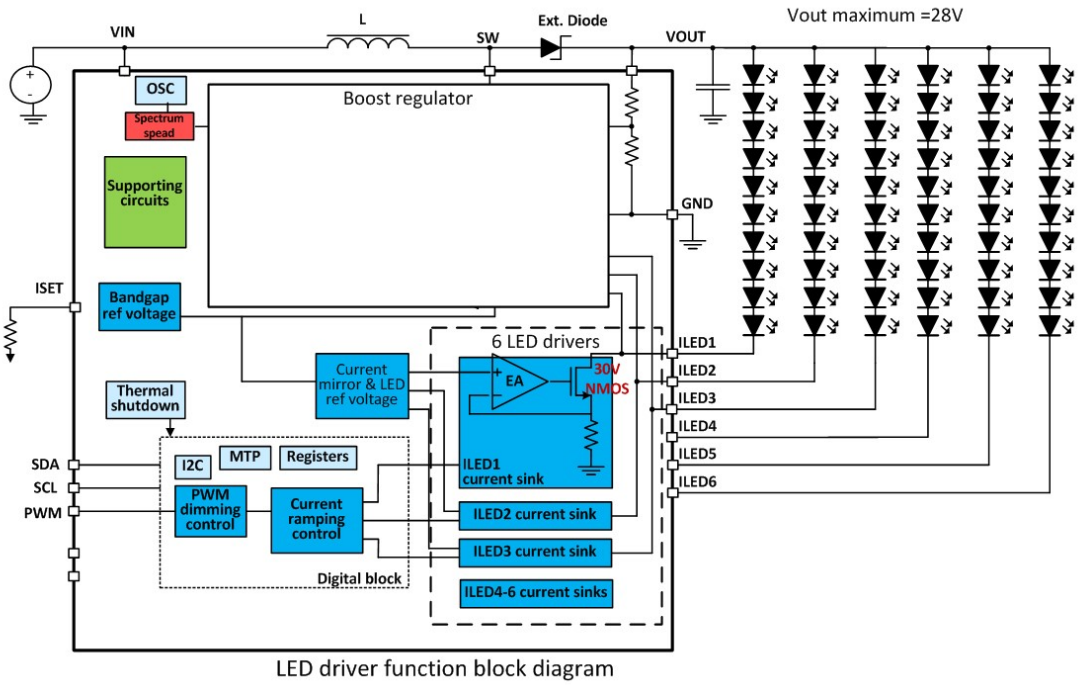


Figure 3. LED Driver Function Block Diagram.

While striving to achieve the high efficiency and reduce die area, the following innovation areas were targeted and addressed.

1) Achievement of high LED current accuracy and highly reduced channel-to-channel mismatch. A novel overall LED driver architecture (including its reference generator and

LED drivers) is invented to improve LED current accuracy and reduce its channel-to-channel mismatch.

2) A novel driving amplifier in each LED driver is developed to improve the driver speed by using a creative slew rate enhancement technique at a low quiescent current level.
3) Hybrid LED brightness dimming (linear dimming plus PWM dimming) is developed to drive the LED drivers.
4) A novel spectrum spreading design for the boost regulator switching clock is developed to reduce the switching noise at a fixed frequency.
5) A novel error amplifier design for boost regulator is developed to speed up the transient response of the boost regulator.

The goal of this design is to achieve a fully functional system with these novel circuit designs.

2 INVESTIGATION OF PRIOR ARTS

In recent years, multiple papers on LED driver designs have been published. Meanwhile, multiple LED driver ICs have also been introduced by companies such as Texas Instruments (TI), Maxim Integrated Products, and Linear Technology.

Some major publications will be examined and reviewed below.

2.1 Published Scientific Literature

In recent years, many papers have been published on LED drivers. These papers include designs such as AC-DC power supplied LED drivers, and DC-DC power supplied LED drivers. The applications of these designs are in the range of general lighting, flash lighting, screen backlighting, and dashboard backlighting. From all of them, the following papers have been selected for review here as their application environment is very similar to that of this dissertation. Along with providing a summary of the work in the papers, a critical analysis is also undertaken by the author of this dissertation.

In reference [2-1], an 8-channel LED driver design is presented. Hsieh et al. focus on the design of the linear LED driver to improve the LED channel-to-channel matching by using a calibration process, as shown in Figure 4.

A channel-to-channel mismatch analysis is shown in Figure 5. It can be seen that a differential current ΔI goes through each of the two R_F resistors. This will cause some additional LED current mismatch.

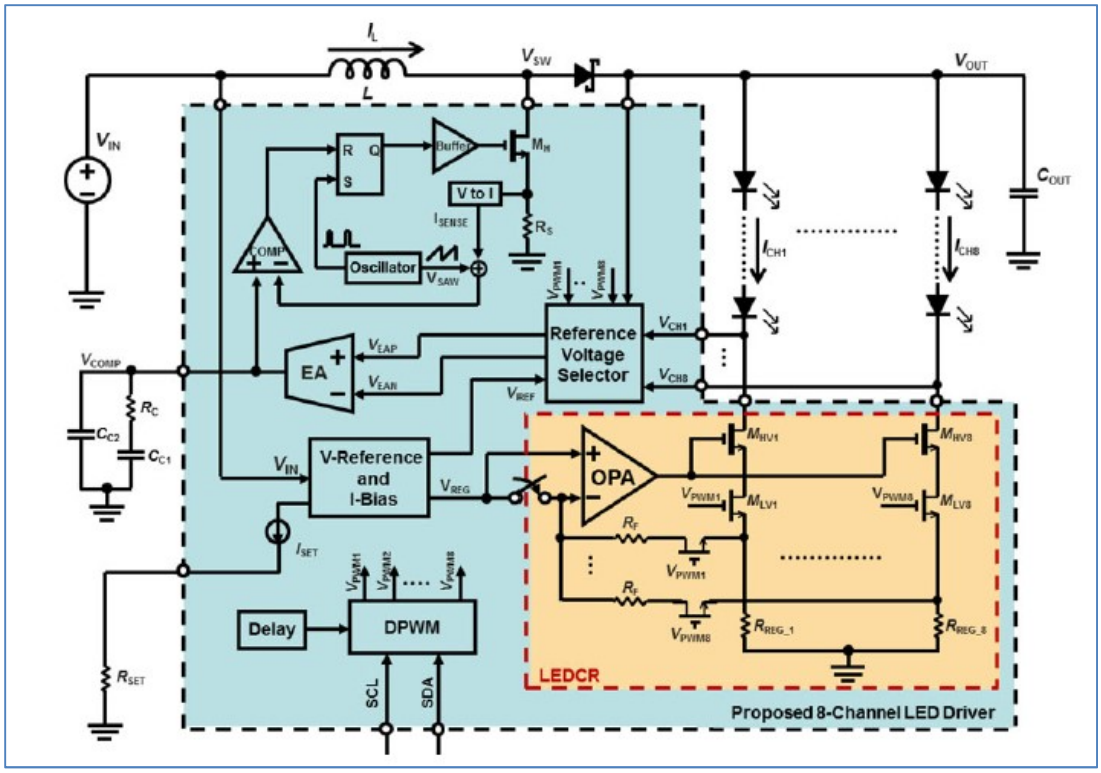


Figure 4. Circuit Diagram of Reference [2-1].

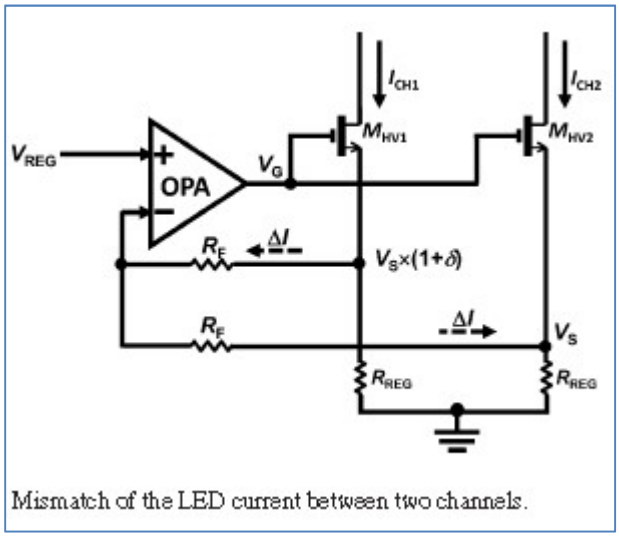


Figure 5. Circuit Diagram for LED Mismatch Analysis in Reference [2-1].

Although the paper claimed the channel-to-channel mismatch is very low, it does not quantify the value. Based on typical process variation data, the M_{HV1} and M_{HV2} in Figure 5 are usually high voltage devices that will have higher gate-to-source voltage Vgs mismatch, which is generally

higher than the input offset of the op-amp using low voltage MOSFETs in the figure. As a result, such an approach will bring more variation than a regular multi op-amp driver approach.

In references [2-2] and [2-3], a similar switching mode multi-channel-LED-driver design is implemented. Figure 6 shows the circuit to detect minimum bottom voltage of the multiple LED strings via using multiple parallel diodes.

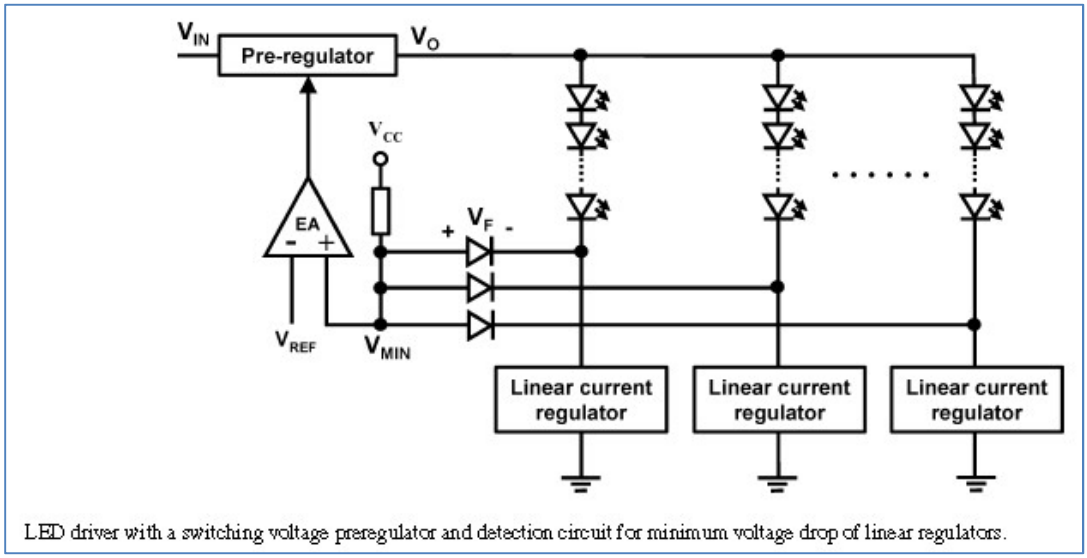


Figure 6. LED Driver Circuit in References [2-2] and [2-3].

That novel circuit utilizes an analog OR function. There is a diode for each LED string, with the anode of each diode connected together. Normally, only the diode which is connected to the minimum LED string voltage will conduct current from V_{MIN}. As a result, V_{MIN} is the minimum LED string bottom voltage plus the diode voltage drop. This structure is recognized and called an analog OR function. This minimum voltage detection technique is a great idea to help to guarantee that the desired LED currents and brightness can be always achieved. Such a configuration is a popular approach in today's designs since it gives a minimized channel-to-channel mismatch if properly designed.

However, these parallel diodes used in an analog OR function have floating cathodes which allow connections to the respective LED string bottom nodes. This type of diode is not commonly

available in today's low-cost CMOS silicon processes. Some other ways to achieve the same analog OR function needs to be found. One alternative approach is to use diode-connected MOSFETs to replicate those real diodes, but these MOSFETs will have much higher voltage mismatches than those original diodes, which will cause more offset in the overall system.

Additionally, there is no description in their design to show how to improve the LED current accuracy and its channel-to-channel mismatch.

In reference [2-4], another novel approach utilizing the analog OR function to detect the maximum LED string bottom voltage to improve efficiency is proposed. The circuit diagram is shown in Figure 7. There is one diode for each LED string (D_1, D_2, and D_n). The cathodes of the diodes are all connected together to the voltage V_E. Therefore, only the diode connecting the maximum voltage will conduct the given current or most of it.

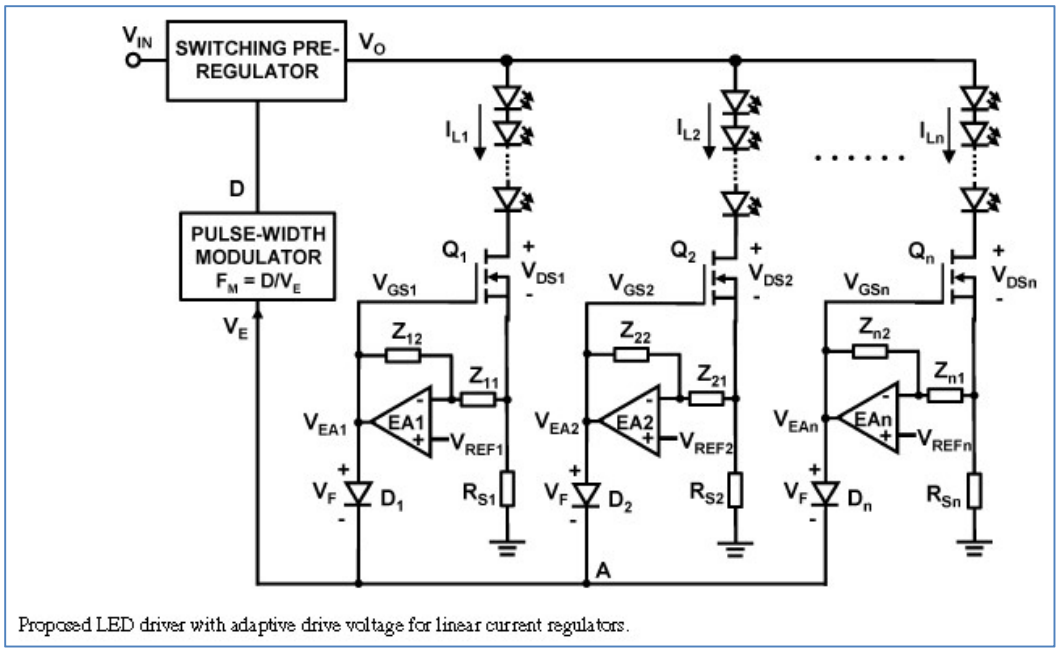


Figure 7. LED Driver Structure in Reference [2-4].

Hu and Jovanovic utilize a linear-regulator-type LED driver to control each gate voltage (V_{GS1}, V_{GS2} and V_{GSn}) of each respective power NMOS (Q_1, Q_2, and Q_n) in parallel. Such a structure could possibly provide the maximum efficiency for the overall LED driver system.

However, there are two concerns in this design. At first, the input offset voltage of each amplifier (EA1, EA2, or EAn) introduces a major error to the channel-to-channel LED current mismatches and absolute accuracy. Secondly, for example, in the configuration of the EA1 feedback loop, the amplification effect between Z_{12} and Z_{11} due to the feedback loop will also amplify the amplifier's input offset at the same ratio. It will make the input offset introduced error much worse. The other channels have the same effect. As a result, the channel-to-channel mismatch becomes even worse.

Reference [2-5] proposes a single-inductor multiple-output (SIMO) boost LED driver that balances multiple channel currents using a novel time-division multiplexing conduction scheme. The circuit diagram is shown in Figure 8. By turning on the inductor for an equal amount of time for each LED string, the average current of each channel is potentially made equal in an open-loop fashion. The design also has a function of changing the sequence of connection within each discharging period. Kim et al. claim that the experimental results with a prototype LED driver demonstrate a power efficiency of 93.0% excluding the controller field-programmable gate array (FPGA) power and a maximum current balance error of 2.04% while delivering 12.4 W to three channels of high-brightness white LEDs.

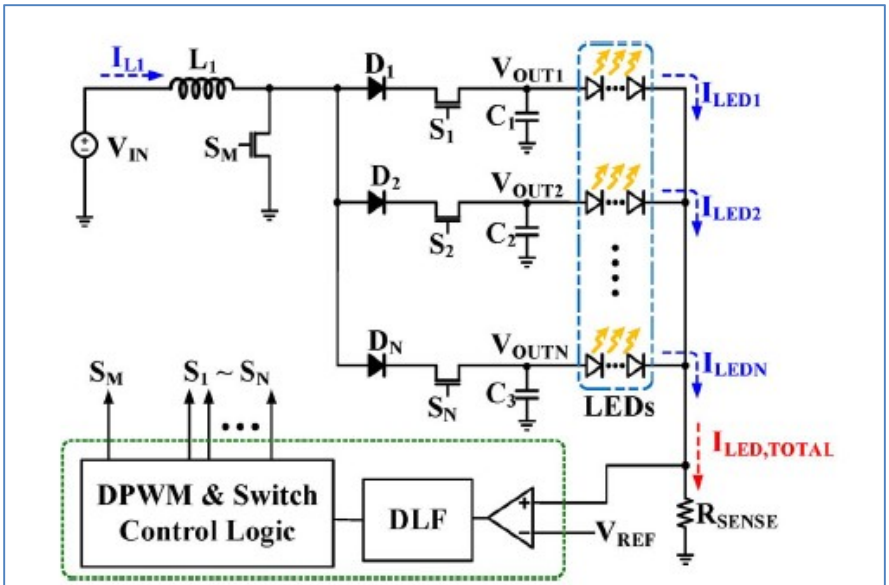


Fig. 2. SIMO boost converter topology of the proposed multichannel current-balancing LED backlight driver.

Figure 8. Circuit Diagram in Reference [2-5].

However, such a configuration will require one high voltage diode (D_1, D_2, or D_N) and one high voltage switch (S_1, S_2, or S_N) for each LED string. The switches S_1 to S_N are usually PMOS type instead of NMOS because they are operated at the high voltage end. Since voltages at V_{OUT1}, V_{OUT2} and V_{OUTN} can generally be in the range of 30 V to 40 V for typical applications, 30 V - 40 V diodes and switches are needed for the application. Such high voltage diodes and high voltage PMOS switches are generally expensive and they are also mostly not on chip since low-cost modern CMOS processes do not have them. An alternative low cost approach is to connect the anodes of all the LED strings together while using high voltage NMOS switches to regulate the LED strings bottom voltages since the high voltage NMOS is usually included in a low-cost analog CMOS process in today's semiconductor industry.

Since the mobility of a p-type carrier in a doped silicon crystal is about 2-3 times slower than that of a n-type carrier in a doped silicon crystal, the high voltage PMOS size is usually 2-3 times larger than a same voltage NMOS for a given turn-on conduction resistance value. Therefore, it is

usually more economical to use NMOS than PMOS. That is also one of the main reasons that high voltage NMOS is more welcome for being integrated on a silicon process.

In addition, this design of [2-5] needs multiple output capacitors for each channel (C_1, C_2, C_3), rather than a single output capacitor. These capacitors are generally off chip due to their sizes, it could dramatically increase the total system cost and board area. In comparison, the above-mentioned high voltage NMOS based approach will only need one such capacitor.

In reference [2-6], another SIMO architecture is proposed. Comparing to [2-5], the front-end high voltage diodes are removed and the current of each LED channel is regulated individually.

The drawbacks of such a configuration are: 1) the use of high voltage (HV) PMOS instead of high voltage NMOS; and 2) each LED channel has one output capacitor (Ca, Cb, Cn) which is generally off chip due to their big sizes. Like the previous SIMO design, their total cost and occupied board area are generally higher than a single output capacitor for a SISO (single input single output) LED driver system.

Meanwhile, Yu et al. do not explicitly explain whether there is any measure to take care of the input offset voltage of each feedback amplifier (CAa, CAb, CAn). These input offset voltages could dramatically degrade the channel-to-channel matching between the LED strings. These offset voltages have to be treated in order to achieve a matching result.

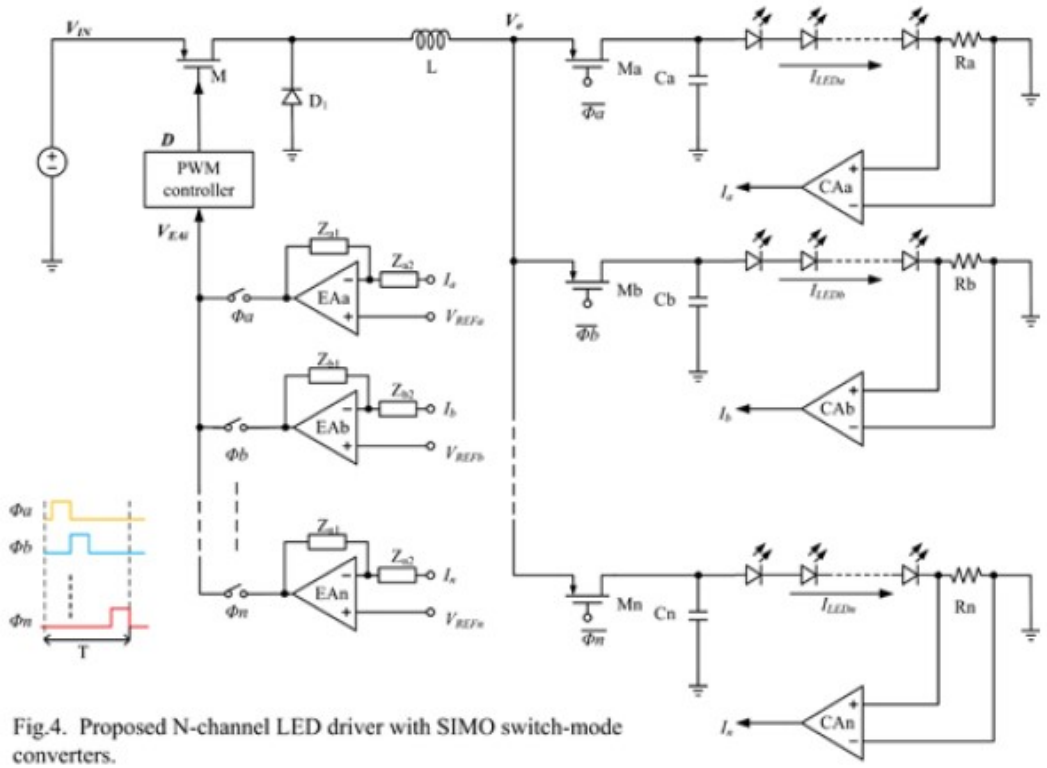


Fig.4. Proposed N-channel LED driver with SIMO switch-mode converters.

Figure 9. Circuit Diagram in Reference [2-6].

In reference [2-7], a 3-channel LED driver chip design, which tries to use precise current balance, is proposed. In the paper, device layout matching topologies are used and analyzed for trying to achieve accurate current balance among LED channels with excellent insensitivity to process, voltage and temperature (PVT) variations, and for trying to achieve small variation of the trimming-free bandgap reference voltage. The circuit diagram is shown in Figure 10.

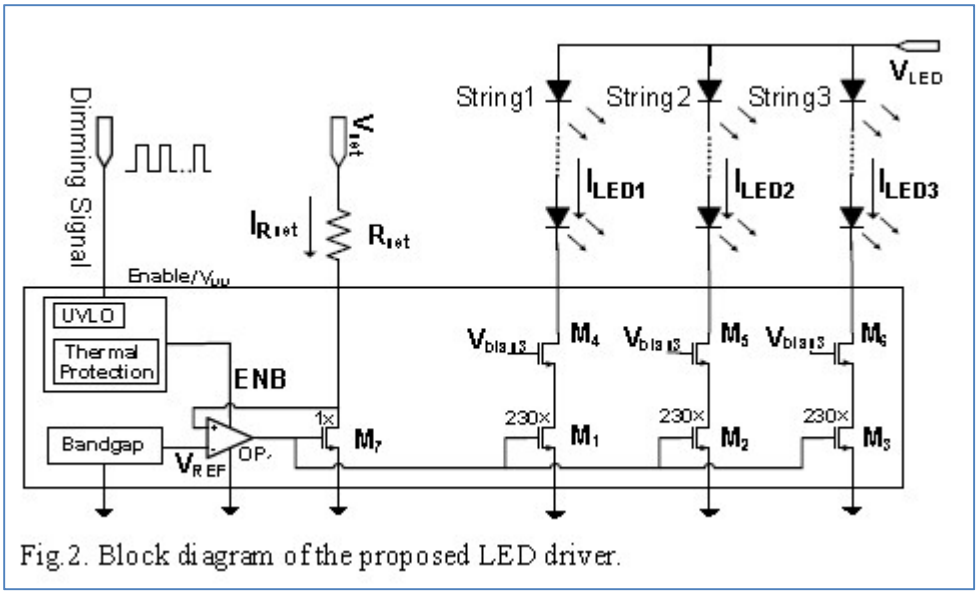


Fig.2. Block diagram of the proposed LED driver.

Figure 10. LED Driver Circuit Diagram in Reference [2-7].

However, this layout matching technique has its own limits. Due to the mismatch of M_1, M_2, and M_3 over process variation, temperature variation, aging and mechanical stress, the matching of LED channels could be dramatically degraded. In the paper [2-7], the authors claim a 0.2% matching measured over 100 test chips. This result is only tested at room temperature and without mechanical stress (i.e., package stress and electronic board stress). In addition, the number of tested chips is probably not adequate to claim a channel-to-channel mismatch maximum specification over all PVT conditions. From the analysis of the threshold voltage V_T of MOSFETs, which has a bigger variation over temperature and stress, the actual deployed result over all different conditions will probably have a bigger variation than claimed in the paper.

In reference [2-8], a PFM (pulse frequency modulation) type approach to adjust the average LED current is presented. The technique is called ‘Pulse Current Modulation’ in the paper. In the approach, the average LED current is adjusted not by linear current amplitude control or PWM (pulse width modulation) control, but by the number of narrow current pulses within a given period. A LED current only conducts when there is a narrow pulse. For a given long time period, if the

number of the pulses is high, the average LED current is high, and the corresponding LED brightness is high. The circuit diagram and its signal diagram are shown in Figure 11. The proposed LED driver system diagram is shown in Figure 12.

Each pulse is designed to last roughly several microseconds, which is quite long for some applications. In fact, the turn-on/off speed of a LED current in any typical regular design is in the range of several hundred nanoseconds if low quiescent is required and there is no special treatment. It is almost impossible to design a much narrower pulse width without sacrificing the LED current accuracy.

This design can be applicable for certain applications that can tolerate a slow PWM dimming frequency for the LEDs, such as a 400 Hz PWM dimming frequency. As a result, this design has two practical limitations. The first is that it needs a relatively very long period in order to achieve a high LED brightness contrast ratio (such as 1:4000) since each narrow pulse is as long as several microseconds. It will produce a slow PWM dimming frequency which might not be tolerable in many mobile applications. The reason is that the lowest allowable clock frequency for LEDs is 20 kHz, which is the upper end frequency of audible voice. It is not desired to allow the PWM dimming frequency to LEDs to encroach into the audible voice frequency range. Otherwise, it could be perceived as audible noise. The second limitation is that it will probably be less efficient since this scheme will require more switching actions to generate large numbers of current pulses for a given period than conventional PWM dimming and/or linear dimming approaches. Each switching action consumes power to charge and discharge the gate capacitance of a power MOSFET handling LED current.

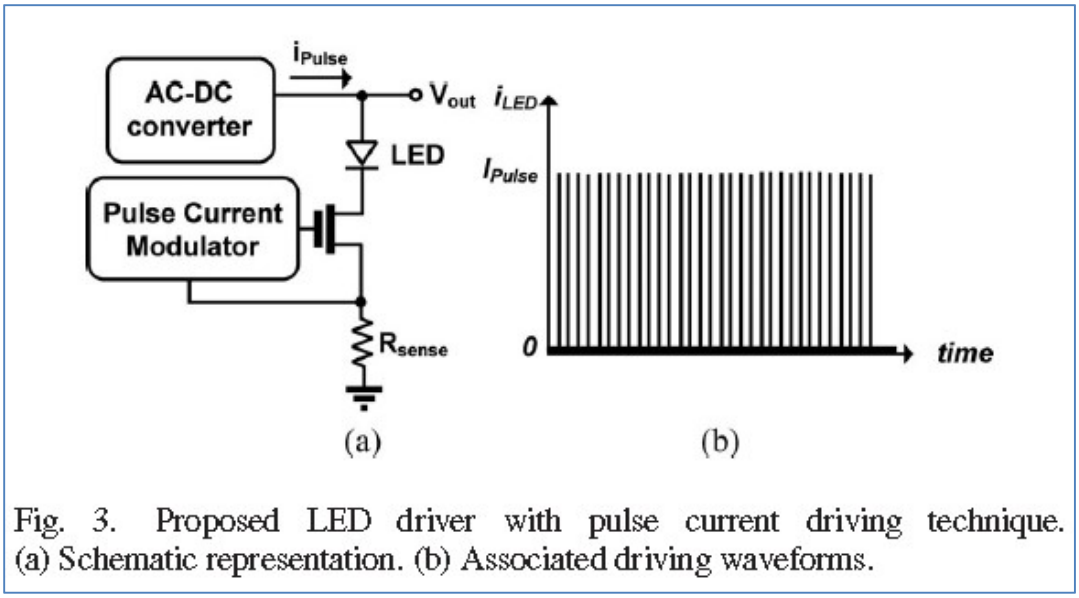


Fig. 3. Proposed LED driver with pulse current driving technique. (a) Schematic representation. (b) Associated driving waveforms.

Figure 11. LED Driver Circuit Architecture of Reference [2-8].

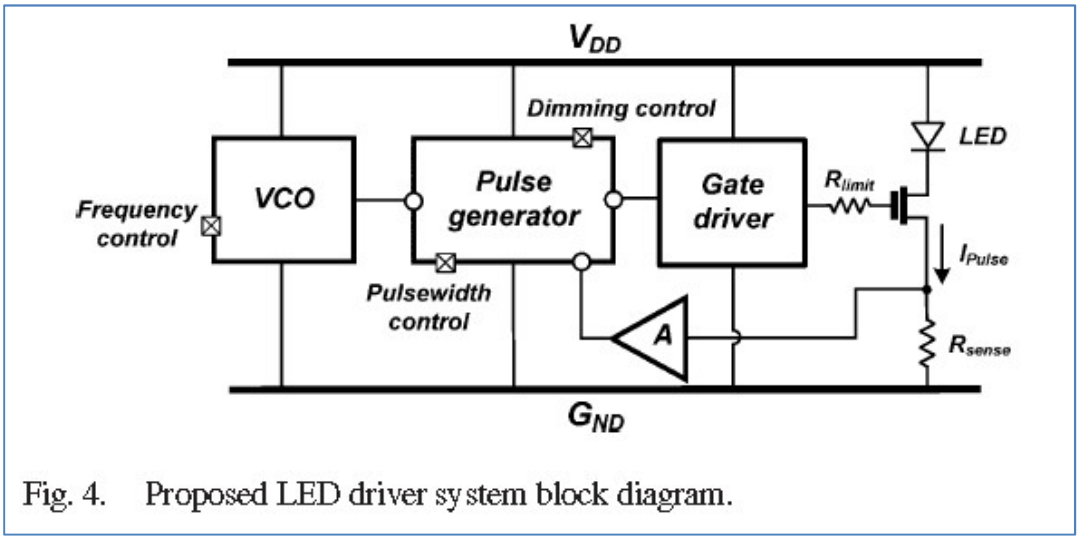


Fig. 4. Proposed LED driver system block diagram.

Figure 12. LED Driver Block Diagram of Reference [2-8].

In reference [2-9], a synchronous boost based LED driver design is presented. Its design target is only for an application at low power supply voltage such as 5 V. The proposed LED driver system architecture is shown in Figure 13. It only drives 2 LEDs in series. As a result, the whole system efficiency is not as high as the designs with large numbers of LEDs in series.

Meanwhile, this design is only for one single string of LEDs, it does not need to specify channel-to-channel mismatch design requirement. Therefore, it is relatively easier to design and its design is much less challenging than the proposed design in this dissertation.

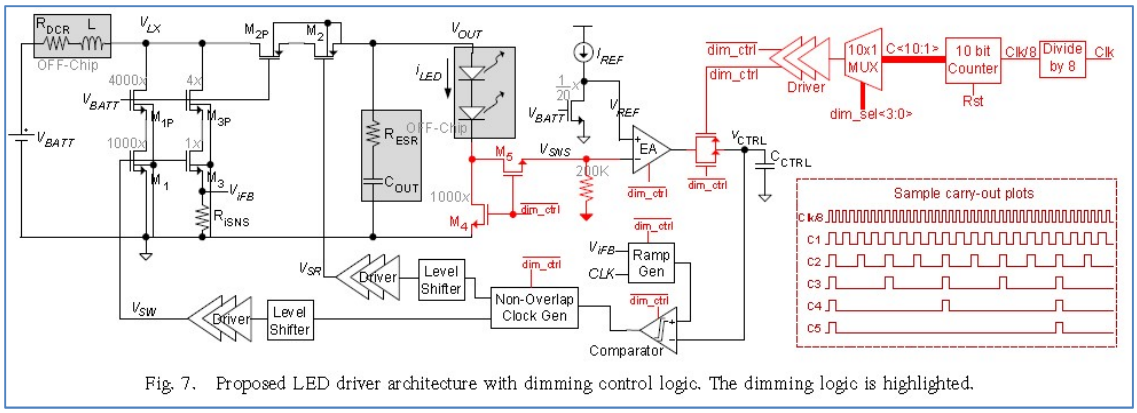


Fig. 7. Proposed LED driver architecture with dimming control logic. The dimming logic is highlighted.

Figure 13. Circuit Block Diagram of Reference [2-9].

In reference [2-10], another buck-boost based LED driver is presented. This design is a fully integrated on-chip system. It shows a high efficiency up to 91% as shown in Table 1. The functional diagram and circuit diagram of [2-10] are shown in Figure 14 and Figure 15, respectively.

Table 1. Excerpted Performance Table of Reference [2-10]

Parameter	*Value*
Technology	0.18μm CMOS with 5V option
Chip area	1.65×2.5mm^2
Input voltage (V_{in})	2.7V-5.5V
Output voltage (V_{out})	0V-5V
Output current (I_{out})	0.1A-2A
Switching frequency	2.5MHz
Output voltage ripple	<10mV
Line regulation	<0.2%/V
Efficiency	Max: 91% Min: 80%
Output current settling time	<20μs
Output voltage settling time	<20μs

However, such a high efficiency is probably achieved with a sacrifice of the die size which is 1.65 mm x 2.5 mm, which is a relatively big die size compared to other common designs. In addition, the output voltage of the switching regulator is only 5 V, which is also a low power voltage application. Since the design only has one LED string as its output load, it does not need to have a LED current channel-to-channel mismatch design requirement.

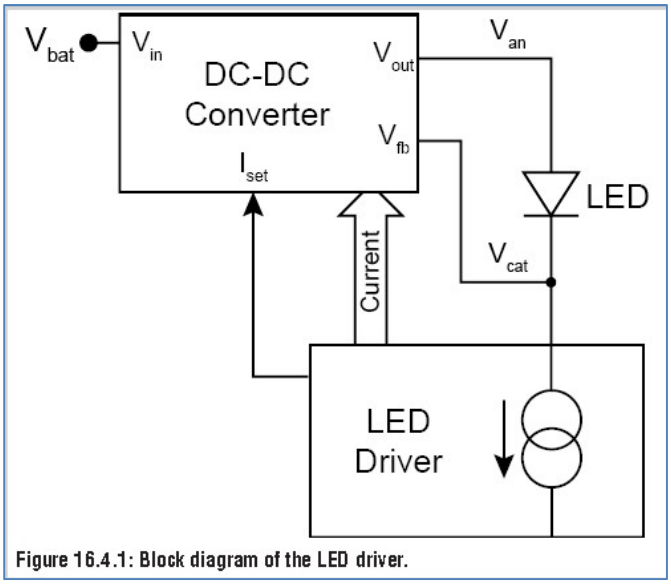


Figure 14. Function Diagram of Reference [2-10].

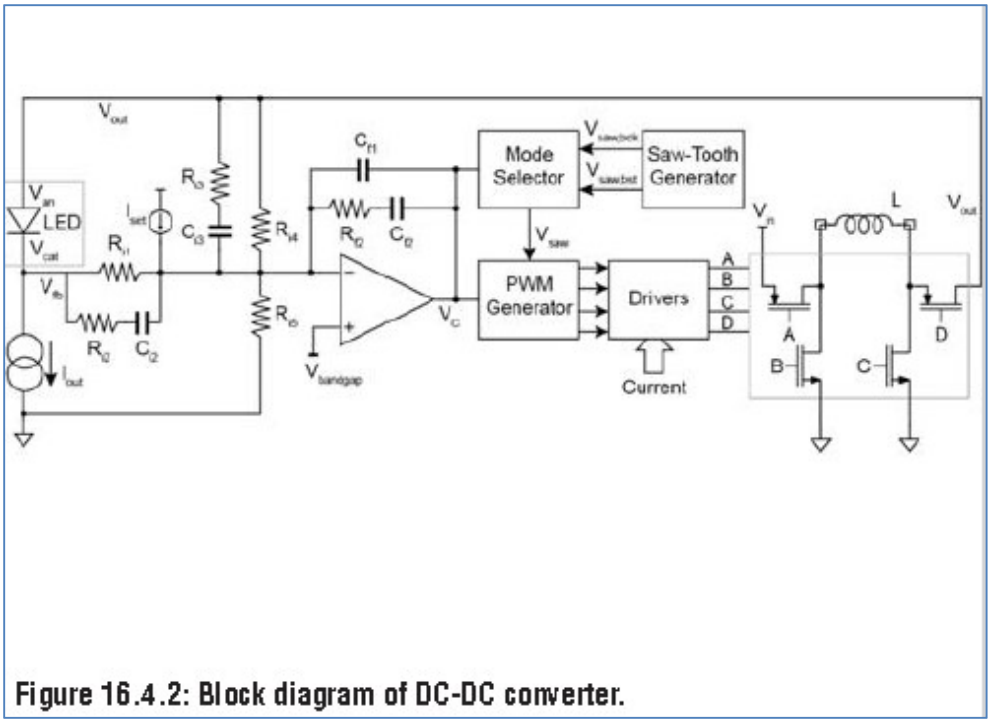


Figure 16.4.2: Block diagram of DC-DC converter.

Figure 15. DC-DC Converter Circuit Block Diagram of Reference [2-10].

In reference [2-11], a boost converter based LED driver system to drive red/green/blue (RGB) LEDs for LCD backlighting is presented. Hsieh and Chen design the boost regulator by completing the internal compensation control in current mode. The proposed circuit is shown in Figure 16.

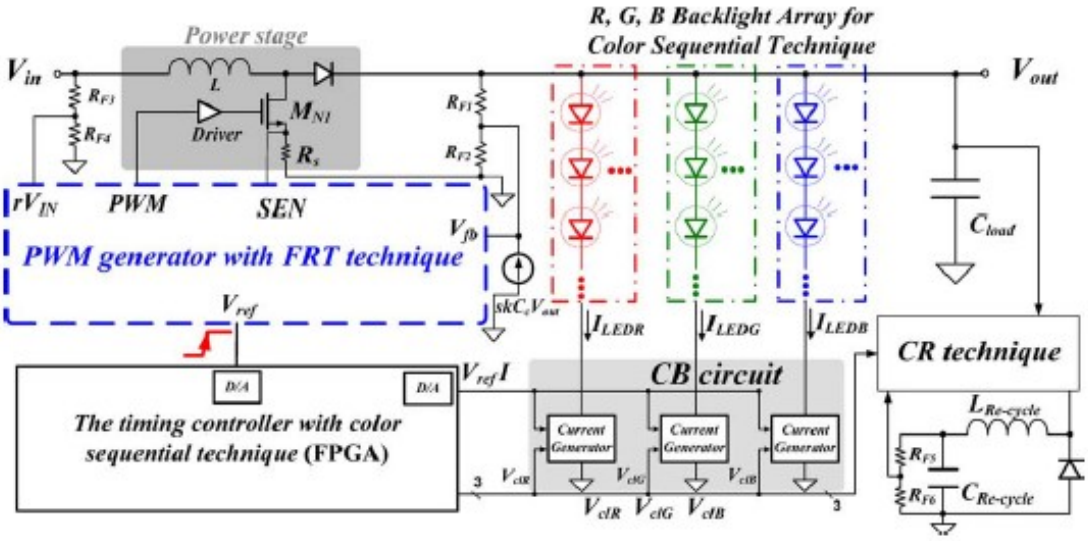


Fig. 6. The proposed LED driver contains the FRT, CR techniques, and the current balance (CB) circuit.

Figure 16. Proposed LED Driver System in Reference [2-11].

However, the authors probably failed to consider the variation of the right-half-plane (RHP) zero over all the load changes. The paper does not show and analyze the impact of the RHP zero's variation in the Bode plot in Figure 17. For PWM continuous current mode boost regulators, it is well known that a RHP zero can increase the gain by 20 dB per decade while the phase can shift down 90 degrees in the open loop analysis of a closed loop [2-11]. Therefore, it can potentially reduce the system stability. There is no easy way to compensate for this RHP zero in the feedback loop system stability design. To make the system stable, the practical approach is to make the system unity gain bandwidth to be less than the location of the RHP zero so that the acceptable phase margin can be guaranteed.

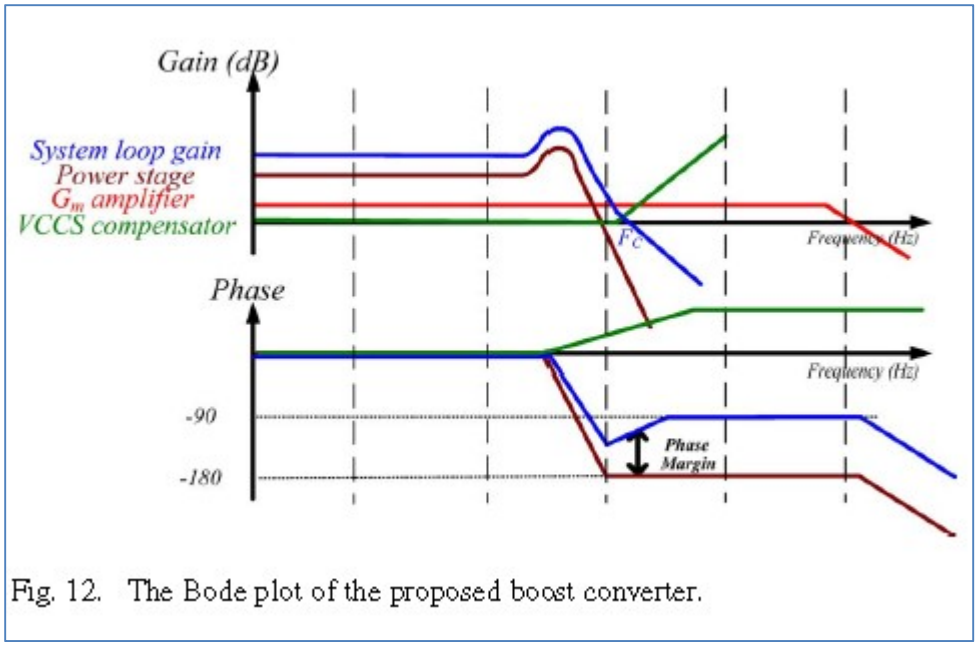


Fig. 12. The Bode plot of the proposed boost converter.

Figure 17. Boost Converter Open-loop Bode Plot of Reference [2-11].

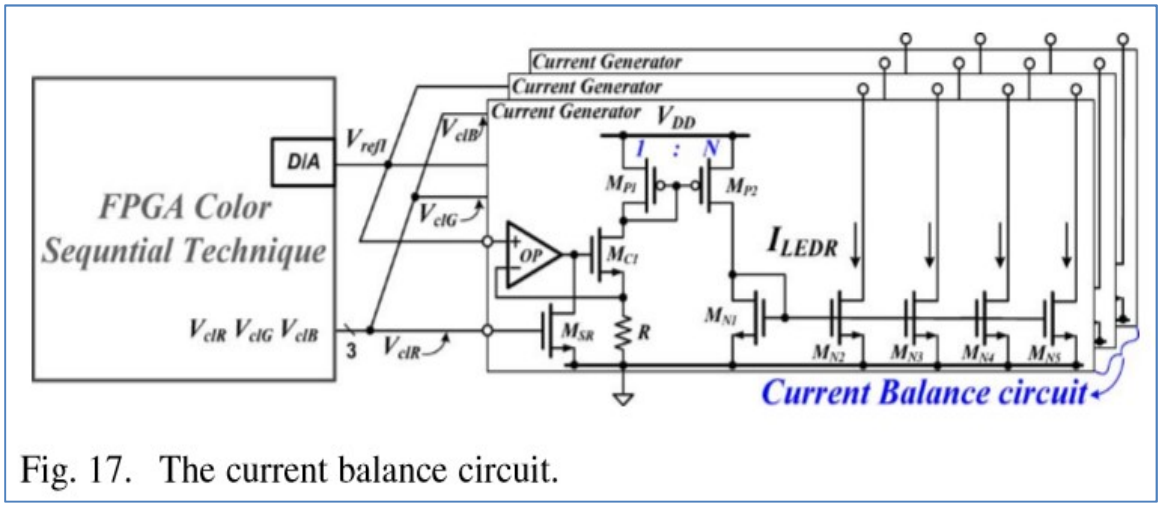


Fig. 17. The current balance circuit.

Figure 18. LED Driver Design of Reference [2-11].

Meanwhile, as shown in Figure 18, its LED driver design shows that the channel-to-channel mismatch and LED current value accuracy do not have high precision and accuracy. The reason is the multiple LED drivers are based on a simple NMOS current mirror structure of M_{N1} and $M_{N2}/M_{N3}/M_{N4}/M_{N5}$. Matching of these single device current mirrors will more likely suffer from

device process mismatch, channel length modulation effect, temperature variation and mechanical stress, and layout parasitics.

The LED current accuracy is based on the simple current mirror matching between M_{N1} and $M_{N2}/M_{N3}/M_{N4}/M_{N5,}$ which can usually give an accuracy of 5% to 10% over all the PVT conditions. The LED current channel-to-channel mismatch is based on the matching between any two of the NMOS devices M_{N2}, M_{N3}, M_{N4}, and M_{N5}, which will also give a mismatch value of 5% to 10% over all the PVT conditions. Therefore, it can be concluded that this design does not put forth a careful consideration on how to improve the LED driver current accuracy and channel-to-channel mismatch.

In reference [2-12], a boost-regulator-based multi-channel LED driver is presented. The overall system structure is as good as in other published papers. It is shown in Figure 19.

However, the LED driver control design cannot reach high LED current accuracy and high channel-to-channel matching. As shown in Figure 20, we can observe that the un-cascoded bottom MOSFET (M1 and M2) matching suffers from device mismatch, temperature variation, mechanical stress and layout parasitics. This drawback can cause up to several percent variation (probably 5%-10% over PVT) in its accuracy and channel-to-channel mismatch over process variation, temperature, voltage and mechanical stress. It is probably impossible to directly use this approach to achieve a low channel-to-channel mismatch specification such as 2%.

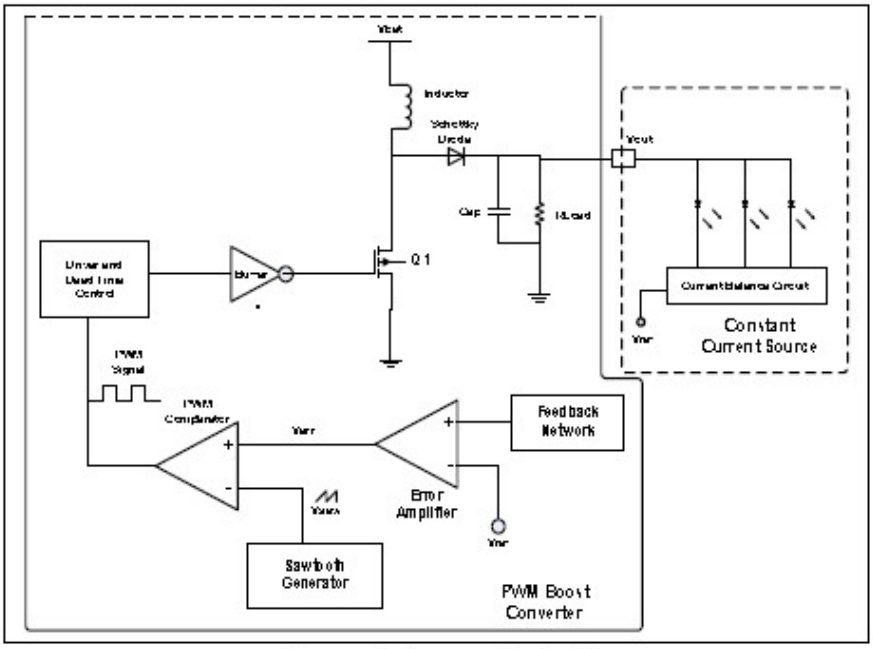


Figure 1. System Block Diagram

Figure 19. System Block Diagram of Reference [2-12].

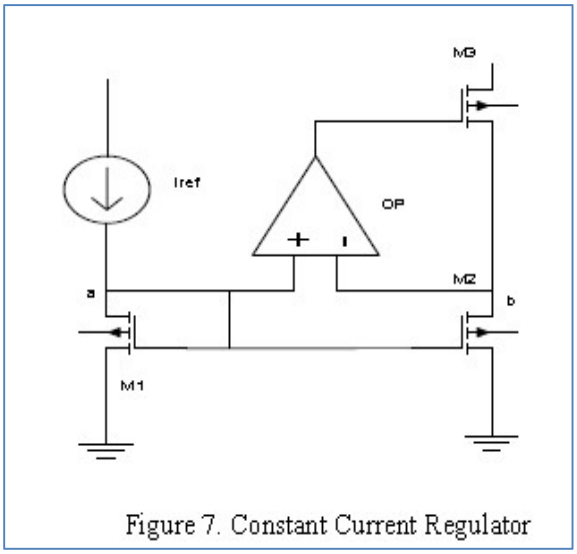


Figure 7. Constant Current Regulator

Figure 20. LED Driver Control Circuit Diagram of Reference [2-12].

In fact, to reduce this variation, it is probably better to use resistors to replace those MOSFETS for better accuracy and lower mismatch since resistor matching is generally better. For example, typical polysilicon resistor matching can easily reach 1% over PVT.

In reference [2-13], a boost converter based multi-channel LED driver is presented. The LED driver control design is shown in Figure 21. Like other designs, the LED driver design suffers in terms of LED current accuracy and channel-to-channel mismatch errors. The main reason is that there are larger mismatch on the NMOS at the bottom NMOS mirror (mn2 and mn3), mismatch of the PMOS current mirror (mp1/mp3 versus mp2/mp4) and that of the rest of the circuit over PVT and any mechanical stresses.

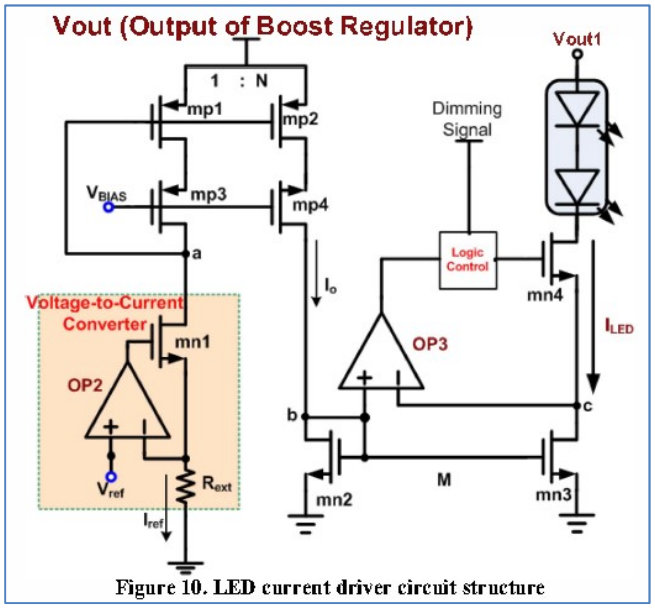


Figure 10. LED current driver circuit structure

Figure 21. LED Driver Control Circuit Diagram [2-13].

Reference [2-14] is not a publication of LED driver design. Rather, the authors provide some basic LED electronic properties that are very useful for LED driver designs. This paper provides information regarding the influence of the LED current waveform, which depends on the driver topology and control, on the luminous flux. The luminous efficiency is also investigated experimentally for different LEDs, i.e., a red, a green and a blue 1 watt LED.

In reference [2-15], a buck-boost based switching regulator with LED drivers is proposed. One main contribution of the paper is that, based on the Taylor series to describe the LED exponential function, the dc and small-signal transfer functions of LED arrays are derived for the system analysis of the employed single-loop CCM (continuous current mode) buck–boost LED driver. In addition, this design employs an array of 6 x 20 =120 LEDs as load. That means it has 6 LED driver channels with 20 LEDs on each channel. The measurement loop circuit diagram is shown in Figure 22.

However, the design is mainly focused on a theoretical analysis and approval of the system. The design is done by discrete components, not on an integrated circuit chip. Therefore, it is hard to evaluate its potential integrated LED driver performance with respect to accuracy and channel-to-channel mismatch.

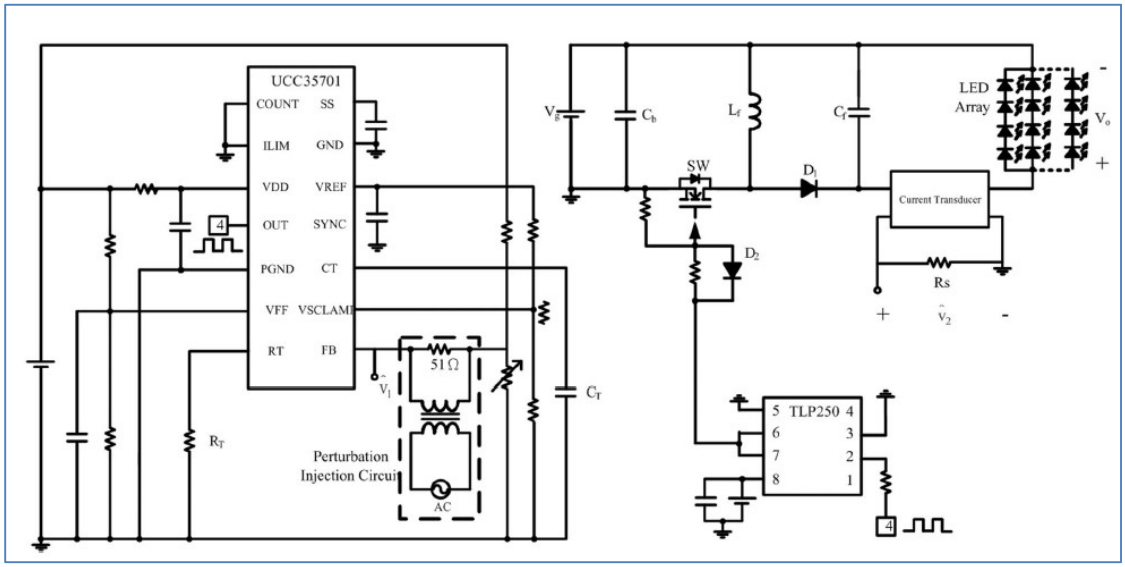


Figure 22. Measurement Loop Circuit Diagram of Reference [2-15].

In conjunction with reference [2-15], reference [2-16] presents a Taylor series expression for a LED model that can be used for the analysis of the LED driver system. The Taylor series is utilized to express the Shockley equation of LEDs in the derivations of the dc and small-signal

equivalent models. Based on the proposed LED models, Lin et al. provide a model for the LED array with *M* parallel strings of *N* LEDs in series. They also provide the equivalent resistances of the *N*×*M* LED array. The results could probably be used for detailed analysis and simulation purposes for any future LED array designs.

Many other published LED driver designs, such as [2-20], [2-21], [2-22], and [2-23], are in the AC-DC application environment. Because their LED driver sections are similar to the aforementioned references, and because these applications are in the AC-DC area which is not the design environment for this dissertation, they are not described and analyzed here in detail.

2.2 Some Commercial Products

The products that are mainly examined are the Texas Instruments LP8555/LP8556/LP8557 series [2-17] [2-18] [2-19]. These three products possess the same basic design architectures of a boost regulator with multiple LED drivers and similar performances. The LP8555 and LP8556 are mainly used for automotive and industrial applications. The LP8557 is mainly targeted to mobile applications such as tablet computers. Therefore, the LP8557 is primarily examined in relation to the design in this dissertation. Based on its datasheet, the LP8557 has the following features:

1) PWM peak-current mode boost regulator. Its output voltage is up to 30 V;
2) Hybrid LED current control combining linear and PWM controls together. When the LED current is between 25% and 100%, it is in linear control. When the LED current is less than 25%, it is in PWM control
3) The LED current accuracy is ±4%;
4) The LED channel-to-channel mismatch maximum and minimum limits are not given. Only a typical 0.5% value is listed.

In comparison, our design is to result in a LED driver chip with a target of ±2% channel-to-channel mismatch accuracy and ±4% or better LED current accuracy in addition to the major features that are already shown for the LP8557.

3 BASIC THEORY OF THE LED DRIVER SYSTEM FUNCTIONS

The basic LED driver system has been described in Section 1.4. In this chapter, the detailed LED driver system and basic theory of the DC-DC switching regulator are introduced.

3.1 System Diagram

There are multiple LED driver system structures [3-1]. For a LED driver system for mobile applications such as smart phones and tablets, the functional diagram for a fundamental backlighting LED driver is shown in Figure 23.

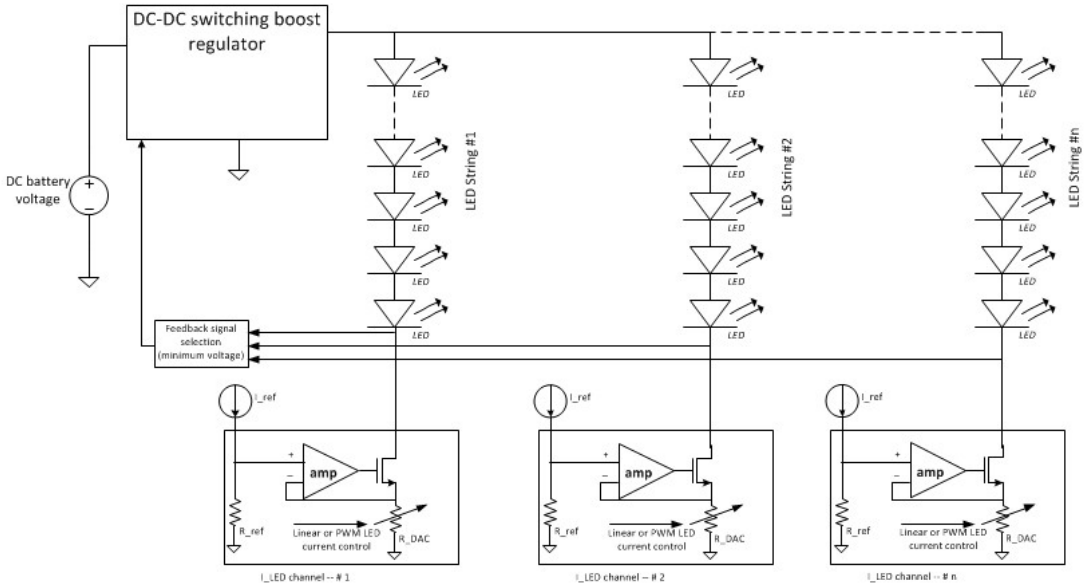


Figure 23. Functional Diagram of the Backlighting LED Driver for Mobile Applications.

In the diagram, there is a front-end DC-DC switching mode boost regulator. The boost regulator is needed because the power supply for the whole LED system is a battery, usually a lithium-ion battery in today's applications. Therefore, a boost regulator is needed to raise the supply voltage. Its basic structure is explained in the switching power supply theory within Section 3.2.

As shown in Figure 23, there is a multi-channel linear LED driver system to control the current through each LED channel. Although there are some other slightly different structures from this diagram such as using a single op-amp driver to control multiple LED channels, as listed in the previous chapter, the LED driver design shown in Figure 23 is still the fundamental approach of the backlighting LED current controls in high-end mobile applications that require highly accurate LED currents.

Therefore, the structure in Figure 23 is used in the design of this dissertation. It also turns out that this structure can provide the benefit of the improvement of both high LED current accuracy and very low channel-to-channel current mismatch.

3.2 Buck, Boost and Buck-Boost Operation Theory

Inductor-based switching regulators are widely used in today's mobile applications due to their high energy efficiency and capability to handle high currents. Most integrated DC-DC switching regulators (or converters) are buck, boost and buck-boost types due to their relatively easy implementation and control. Their operation is described here in the following sub-sections based on reference [3-2]. The basic structures and steady-state relationship equations for each type are briefly introduced.

3.2.1 The Buck Regulator

The inductor-based buck regulator provides an output voltage that is always lower than its input voltage. The basic structure of a buck regulator is shown as in Figure 24.

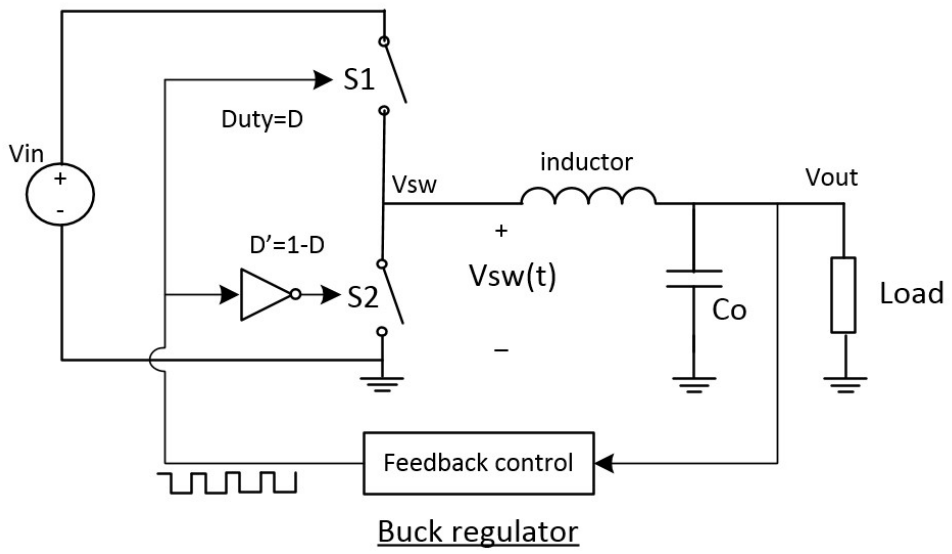


Figure 24. Basic Buck Regulator Structure.

The basic operation of the buck regulator is described as follows. A feedback control circuit receives the feedback signal from the output Vout, and it then generates a control signal to turn-on/off the switches S1 and S2. S1 and S2 are turned on and off alternately at a high switching frequency. By conventional definition, the duty cycle of S1 is usually defined as the converter's duty cycle 'D'. When switch S1 is closed, input current from Vin runs through the inductor and into the load, charging the inductor and increasing Vout. At steady state, when Vout reaches its regulated value, S1 is opened and S2 is closed. Then current will continue to flow through the inductor and begin to flow through S2, as the inductor magnetic field does not change immediately. The inductor energy discharges. Then the next cycle starts at time T as shown in Figure 25. S2 is opened and S1 is closed before the inductor completely discharges in continuous current operation mode. The previous cycle repeats.

The ratio of Vout to Vin can be adjusted by varying the duty cycle of S1. The longer S1 is turned on, the higher the Vout that can be achieved. Ideally with lossless switches and inductor, the overall system efficiency will be at 100%. In reality, because the switches, the inductor and other components in the control loop have some associated power loss during operation, the total efficiency cannot be 100%, but can be close to it. The transient waveform is shown in Figure 25.

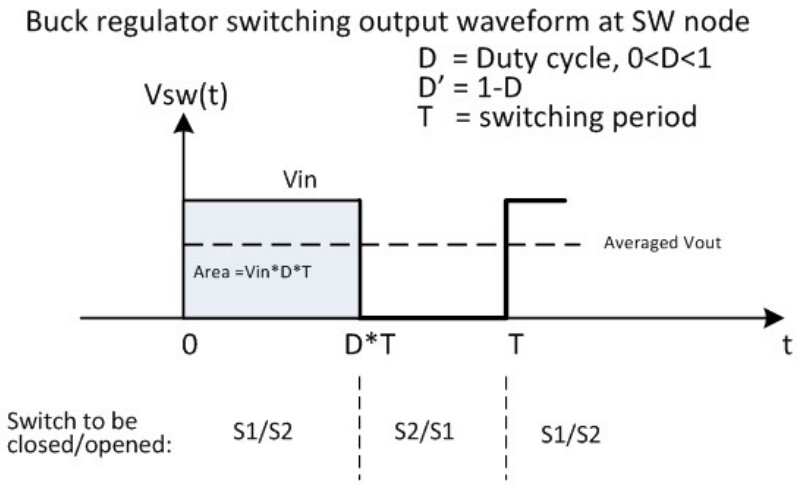


Figure 25. An Ideal Buck Regulator Transient Switching Output Waveform.

The relationship between the average output voltage and the input voltage can be found by using the time-voltage balance relationship over one full switching cycle. The average voltage <Vsw> at the switching node 'Vsw' in Figure 24 is the DC output voltage Vout. Then,

$$< \mathrm{Vsw} >= \mathrm{Vout} = \frac{1}{\mathrm{T}} * \int_0^{\mathrm{T}} [\mathrm{Vsw(t)\,dt}] \qquad (1)$$

$$\Rightarrow \quad \mathrm{Vout} = \frac{1}{\mathrm{T}} \cdot \mathrm{D} \cdot \mathrm{T} \cdot \mathrm{Vin} = \mathrm{D} \cdot \mathrm{Vin} \qquad (2)$$

Where, <Vsw> is the average voltage at 'Vsw' node; Vout is the DC output voltage at steady state; *D* is the duty cycle, 0<*D*<1; and Vin is the DC input voltage.

3.2.2 The Boost Regulator

The inductor-based boost regulator provides an output voltage that is always higher than its input voltage. An output capacitor is normally added to the output of the converter to filter and reduce output voltage ripple. The boost regulator circuit diagram is shown in Figure 26**Error! Reference source not found.**.

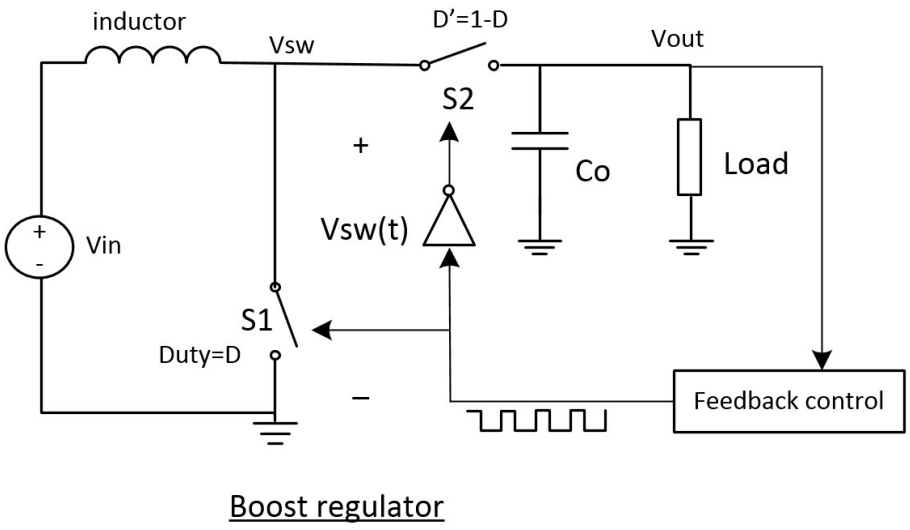


Figure 26. Basic Boost Regulator Structure.

The boost regulator operation is similar to the buck regulator operation described in the previous subsection. By conventional definition, the duty cycle of S1 is defined as the converter's duty cycle, called 'D' in this analysis. When switch S1 is closed, input current from Vin runs through the inductor and toward the ground, charging the inductor by increasing its magnetic field. When the duty cycle D reaches its desired value, S1 is opened and S2 is closed. Then current begins to flow through S2 and through the inductor because inductor magnetic field does not change immediately. The output node is charged and Vout is increased. In continuous current mode operation, the inductor energy discharges, but before the inductor completely discharges S2 is opened and S1 is closed. The previous cycle repeats.

The ratio of Vout to Vin can be adjusted by varying the duty cycle of S1. The longer S1 is turned on, the more energy that can be stored into the inductor at each duty cycle. Thus, a higher Vout is achieved. Ideally with lossless switches and inductor, the overall system efficiency will be at 100%. In reality, due to the operating loss of the switches, the inductor and other control circuits, the total efficiency cannot reach 100%, but can be close to it.

The relationship between average output voltage and the input voltage can be found by using the time-voltage balance relationship over one full switching cycle, similar to the derivation process

as in the buck regulator. The average voltage <Vsw> at the switching node 'Vsw' in Figure 26 is the DC input voltage Vin. Then,

$$< \mathrm{Vsw} >= \mathrm{Vin} = \frac{1}{\mathrm{T}} * \int_0^{\mathrm{T}} [\mathrm{Vsw(t)\ dt}] = \frac{1}{\mathrm{T}} \cdot (1 - \mathrm{D}) \cdot \mathrm{T} \cdot \mathrm{Vout} \qquad (3)$$

$$\Rightarrow \quad \mathrm{Vout} = \frac{\mathrm{Vin}}{1-\mathrm{D}}. \qquad (4)$$

Where, <Vsw> is the average voltage at 'Vsw' node; Vout is the DC output voltage at steady state; D is the duty cycle, 0<D<1; and Vin is the DC input voltage.

3.2.3 The Buck-Boost Regulator

The inductor-based buck-boost regulator provides an output voltage that can be higher or lower than its input voltage. The buck-boost regulator's circuit diagram appears in Figure 27.

Its normal operation is similar to the buck regulator or the boost regulator. The duty cycle of S1 is usually defined as the converter's duty cycle 'D'. When switch S1 is closed, input current from Vin runs through the inductor and toward the ground, charging the inductor by increasing its magnetic field. When the desired duty cycle D is reached, S1 is opened and S2 is closed. Then the current flows through S2 and the inductor because the inductor magnetic field does not change immediately. The output node is charged and Vout is increased while the inductor energy discharges. Then this cycle repeats, as S2 is opened and S1 is closed before the inductor completely discharges (in continuous current mode operation).

The ratio of Vout to Vin can be adjusted by varying the duty cycle of S1. The longer S1 is turned on, the more energy that is stored into the inductor at each duty cycle, and the higher Vout that can be achieved.

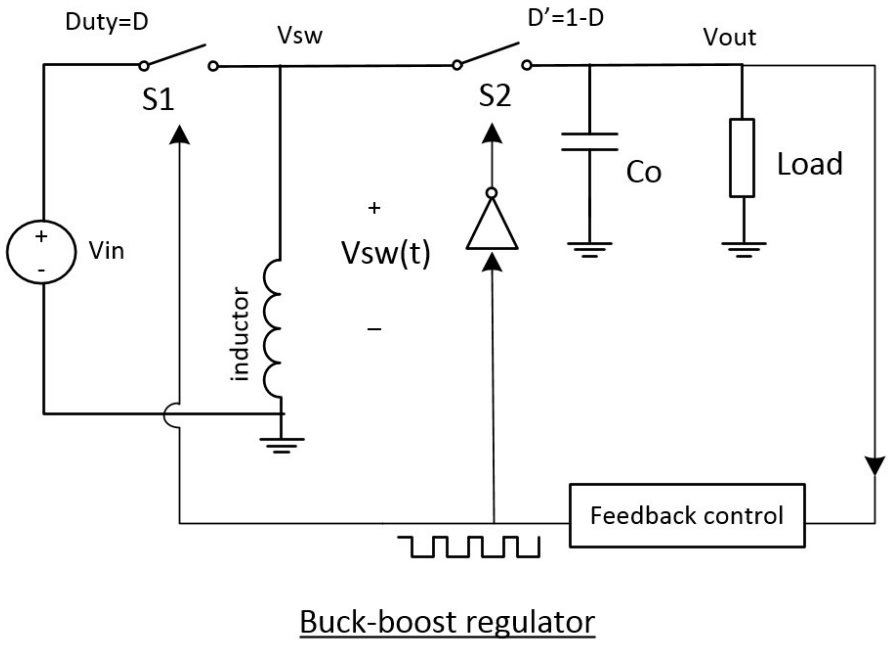


Figure 27. Basic Buck-Boost Regulator Structure.

The input voltage and output voltage relationship of a buck-boost converter is a bit more complex. The relationship between average output voltage and its input voltage can be found by using the time-voltage balance relationship over one full switching cycle, as shown in buck regulator section. The average voltage <Vsw> at the switching node 'Vsw' in Figure 27 is the ground voltage 0 V. Then,

$$< \mathrm{Vsw} >= 0 = \frac{1}{\mathrm{T}} * \int_0^{\mathrm{T}} [\mathrm{Vsw(t)\,dt}] = \frac{1}{\mathrm{T}} \cdot [\mathrm{D \cdot Vin} + (1 - \mathrm{D}) \cdot \mathrm{T} \cdot \mathrm{Vout}\,] \qquad (5)$$

$$\Rightarrow \quad \mathrm{Vout} = \frac{-\mathrm{D}}{1-\mathrm{D}} * \mathrm{Vin} \qquad (6)$$

Where, <Vsw> is the average voltage at 'Vsw' node; Vout is the DC output voltage at steady state; D is the duty cycle, 0<D<1; and Vin is the DC input voltage.

3.2.4 System Control Approach of The Switching Regulators

There are multiple control approaches for a switching regulator.

First, based on whether its switching frequency is fixed or un-fixed, there are two control categories: one is called PWM (Pulse Width Modulation) mode; the other is PFM (Pulse Frequency Modulation) mode. PWM mode control utilizes a fixed frequency while PFM mode has a varying switching frequency. For most of the mobile applications, PWM mode is preferred because mobile devices do not want a large noise to contaminate its communication signal frequency bandwidth. Since the PFM mode will generate noise over a wide frequency range, it is very hard to filter the noise out. PWM mode generates switching noise at a fixed frequency, it is much easier to contain the noise and filter it out. Therefore, PWM mode is selected for our design.

In PWM mode control, based on the feedback loop topology, we can also have two categories: voltage mode or current mode. The basic control approach is called voltage mode control, which means that the feedback signal is purely from its output voltage. Such a control approach is simple and easy to understand. However, due to the inductor and output capacitor forming a pair of complex double poles, it needs a lot of effort to make the system stable. To stabilize the system, a very narrow loop bandwidth is usually implemented. Consequently, the narrow bandwidth makes the system response undesirably slow for many applications. Alternatively, the current mode approach is often used since it will make the loop stability design easier and potentially also could make loop bandwidth wider.

In current mode, there are generally two categories: one category includes peak current mode, valley current mode and emulated current mode. The peak current mode is mostly useful for applications running at high PWM duty cycle since it has a minimum duty cycle requirement. The valley current mode is for applications running mostly at low PWM duty cycle. The emulated current mode uses a sample-and-hold approach to utilize the previously sampled current value for the control at the next duty cycle. The emulated current mode is a more complicated design

approach, but it can be tailored and designed for applications running at either low PWM duty cycle or high PWM duty cycle. The other category is called average current mode, which uses an average current signal for current loop control.

In our design, the peak current mode is chosen due to its simple implementation. It is selected also because the boost regulator in our LED driver application always operates at high PWM duty cycles; therefore, we do not have a strict minimum duty cycle requirement, which is usually the design limitation for a peak current mode control.

3.2.5 The Boost Regulator System Structure and Stability

Since the system is to be used for high-end mobile applications, the DC-DC switching mode boost regulator will be operated in a PWM fixed-frequency peak-current mode to quarantine the switching noise in a limited bandwidth. The basic structure is given in Figure 28. The detailed design architecture and final implementations are described in Chapter 4 and Chapter 5.

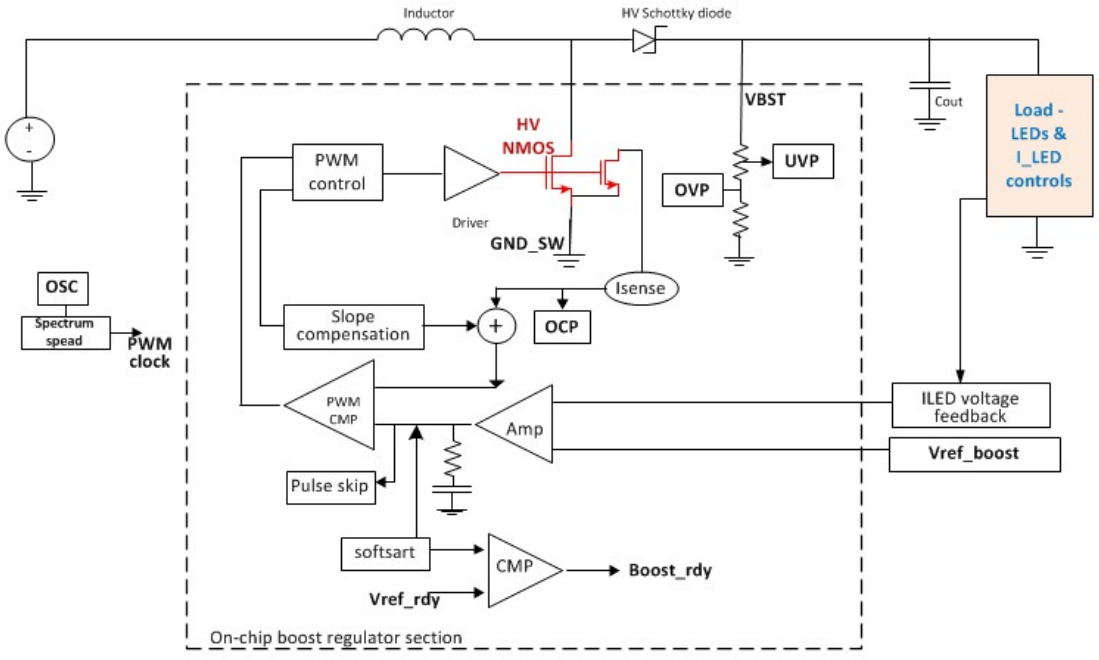


Figure 28. A Boost Regulator Function Block Diagram Used for LED Driver System.

(In Figure 28: Amp: Amplifier; CMP: Comparator; OVP: Over Voltage Protection; UVP: Under Voltage Protection; OCP: Over Current Protection; HV: high voltage; OSC: oscillator; Freq: frequency; Isense: Current sensing circuit; Softstart: soft start control.)

The system stability theory for a PWM fixed-frequency peak-current-mode boost converter has been well analyzed in Ridley's IEEE paper [3-3] and his PhD dissertation [3-4]. Although some other modeling references [3-6], [3-7] have also shown some merits of unification of all switching regulator topologies, Ridley's approach is chosen for its simplicity and completeness. Reference [3-3] provides the complete system analysis of a PWM peak-current-mode switching regulator. The major contribution of the paper is that for the first time, it correctly shows the impact of the sampling effect of the inner inductor current sensing control loop on the outer voltage feedback loop. The theory is also applicable to the peak-current-mode boost regulator in this design. Note that, in Ridley's work, Vorperian's transformer model [3-5] is utilized as the basis. Vorperian's idea of this transformer model is that the switching structure formed by the switches can be modeled as a transformer, which converts the input DC voltage to an output DC voltage. Please refer to the papers for details.

Although the basic architecture of a boost regulator has not changed over many applications, the circuit structure implementation of a boost regulator can still be different and innovative to properly fit a special application situation. This is the case for our design. The design details will be shown in Chapters 4 and 5.

For a boost regulator, one major factor that limits the closed loop bandwidth is the RHP (right half plane) zero shown in the pole-zero S-plane plot. Usually the RHP zero is at low frequency when the duty cycle is high [3-2].

$$Z_{RHP} = \frac{Rout*(1-D)^2}{L} \qquad (7)$$

Where, Z_{RHP} is the RHP (right half plane) zero; Rout is the equivalent output impedance; D is the duty cycle; L is the inductor value.

From the above equation, the RHP zero increases when the duty cycle D decreases. The RHP zero also increases as the Rout becomes larger.

Practically speaking for a conventional continuous current mode PWM boost regulator, the loop bandwidth is typically designed to stay at roughly one-third of the minimum RHP zero location to guarantee stability over all the process and parameter variations.

For our LED backlighting design, the situation is a little special. The effective Rout in the RHP zero equation is relatively large because the constant current LED driver, as the load of the regulator, is equivalent to a current source which offers high impedance. As a result, the effective Rout is mainly dominated by the boost regulator system output impedance itself. The RHP zero location is probably at lower frequency than a boost regulator which drives a regular load. Its location is identified by using system simulations rather than using manual calculations in this design.

There are practical design references [3-8], [3-9], and [3-10] showing some detailed boost regulator system stability design techniques. In these references, not only the detailed boost regulator modeling and stability analysis are provided, but the compensation approach to make the system stable is also given.

3.3 The Linear LED Driver Control Loop Design and Operation

The major portion of this PhD study focuses on the design of highly accurate and fast LED drivers. Feedback control loops are used for the overall accurate control. For detailed feedback control theory, refer to [3-11]. Some LED driver design considerations [3-12] are also evaluated.

For the multiple-channel LED driver accuracy control in this design, there are essentially two important parameters.

The first parameter is the absolute accuracy of LED current (I_LED) for each LED channel over any chips. It is called ‘LED current accuracy’ or ‘I_LED accuracy’ in this dissertation. The lighting

nature of LEDs requires a constant DC current that corresponds to a constant light brightness. This goal requires that the DC current through a LED channel be accurate enough at any given control condition. If the current is not accurate, the LED brightness among LED strings could vary too much, which leads to observable brightness variations among different devices such as cellphones or tablets.

The second parameter is the LED channel-to-channel current mismatch among all LED channels on a single chip. It is called ‘I_LED mismatch’ or simply ‘mismatch’ in this dissertation. To maintain a uniform brightness within a single screen supported by LED backlighting, it is necessary to keep the LED current for each channel as uniform as possible. In other words, the I_LED mismatch between all the channels needs to be as small as possible.

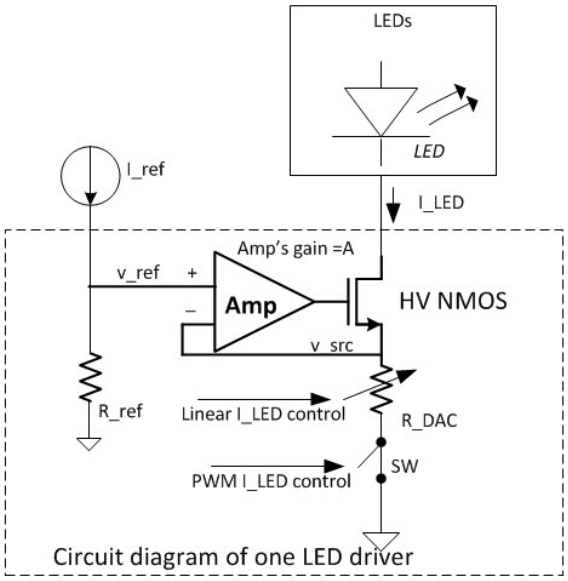


Figure 29. Circuit Diagram of The Proposed Constant Current LED Driver.

Our design diagram of a basic LED driver circuit for one LED channel is shown in Figure 29. As seen in Figure 29, in order to keep a tightly controlled LED current (I_LED), a feedback loop is used for accuracy control. For a given input reference current (I_ref), the feedback loop will force v_ref and v_src to be within a tolerable small feedback loop error. The loop error is determined by the open loop gain. The feedback loop is formed by the amplifier (Amp), the high voltage NMOS

device (HV NMOS) and the resistor R_DAC, which is a resistor array forming a DAC (Digital-to-Analog Conversion) function. R_DAC can be considered as a pure resistor during this loop analysis.

In normal operation, the switch (SW) is always closed. It can be considered negligible for this analysis.

If the amplifier's gain is A and the gain from the HV NMOS with R_DAC is 'f', then the feedback loop error will be

$$\text{Error} = \frac{1}{1+\text{f}*\text{A}} \qquad (8)$$

With a design ensuring that '$\text{f} * \text{A}$' is large enough, the '*Error*' can be small and negligible. In real practice, the $f * A$ can be reasonably designed to be 1000. Then the '*Error*' is only a negligible 0.1% for 4% LED current accuracy and 2% channel-to-channel mismatch requirements.

The designed LED current will be

$$\text{I\_LED} = \frac{\text{I\_ref}*\text{R\_ref}}{\text{R\_DAC}} \qquad (9)$$

Based on this equation, with an accurate I_ref, we can obtain an accurate I_LED, assuming R_ref and R_DAC match well to each other. Actually, R_ref and R_DAC match very well when they are designed using the same type of resistors with a careful design and layout on chip. However, there is 1% matching at 6 sigma between R_ref and R_DAC due to process variations. Since additional switches are used in R_DAC for the DAC (digital to analog conversion) function, the resistance of the switches will have some additional contribution to the total mismatch value. In our design, the switch resistance is kept at about 10% of total resistance of R_DAC to limit its impact. The same switch resistance on R_DAC will also be proportionally added to R_ref for matching purposes. As a result, the total R_ref and R_DAC matching will be roughly 1.6%. This total 1.6% resistor mismatch will be considered in the final I_LED accuracy calculation and design.

3.4 The LED Driver System Operation

3.4.1 Linear LED Current Control

In the above LED driver design, I_LED can be proportionally controlled and adjusted by controlling the 1/R_DAC value. This approach is called linear LED current control. The LED brightness is proportional to I_LED. Such a linear I_LED control approach is shown in Figure 30.

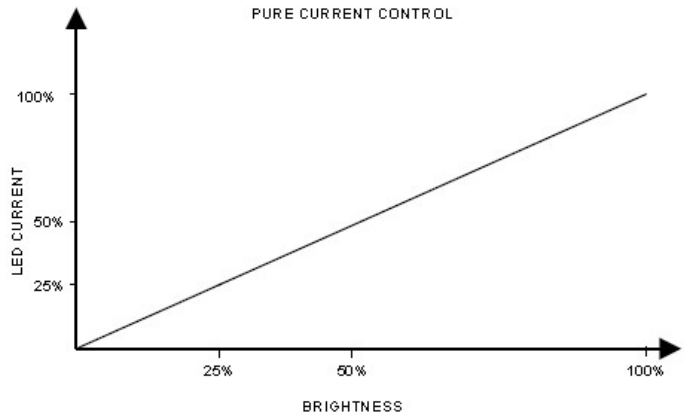


Figure 30. Brightness to LED Current Relationship in Linear LED Current Control Mode.

3.4.2 PWM LED Current Control

It is well known that the light color shade (or light frequency spectrum) of a LED is dependent on the current level through the LED. At different current levels, the light color shade is different. This phenomenon invites a PWM control topology for LED drivers, in addition to the regular linear current control approach. The idea is to use a PWM clock signal to quickly turn the LEDs on during the PWM duty on cycle at a given constant current, and to turn them off during PWM duty off time. The constant current level is set by R_DAC. As a result, the effective averaged LED current will be based on the duty cycle of the PWM clock multiplied by the constant current. Since the PWM frequency is much faster than the human eye's recognition response time of ~150 ms [3-13], people can only recognize the average lighting effect of the LEDs. This PWM control mode generally will consume more power and is less efficient than the linear control mode due to the continuous PWM switching transitions.

The PWM control mode is shown in Figure 31. As seen from the diagram, the higher the LED brightness, which is proportional to the average LED current, the wider the PWM duty cycle pulses. When the LED brightness is zero, the PWM duty cycle is zero; when the brightness is 50%, the PWM duty cycle is 50%; when the brightness is 100%, the PWM duty cycle is 100%.

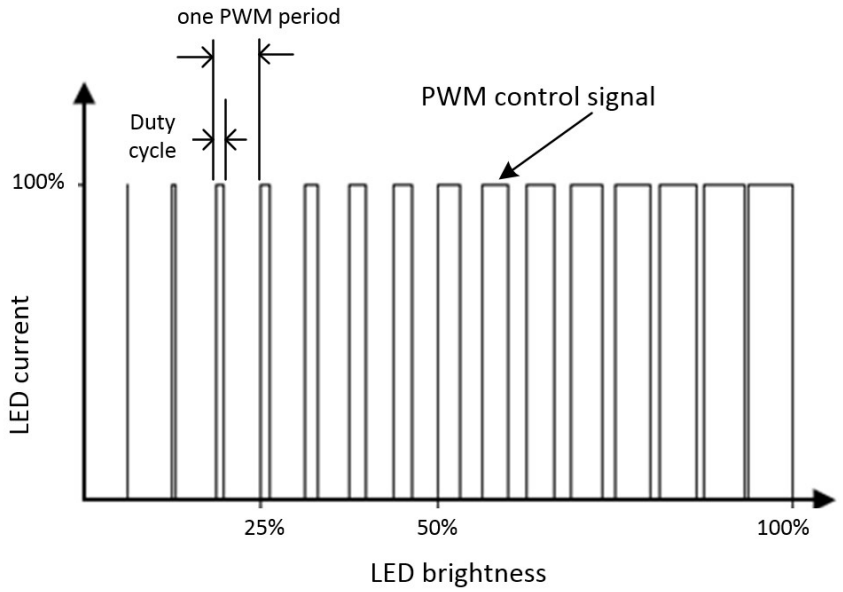


Figure 31. Brightness to LED Current Relationship in PWM Current Control Mode.

3.4.3 Hybrid PWM LED Current Control

The hybrid PWM LED current control mode uses the linear control mode when I_LED is at a high current level, and switches to the PWM control mode when I_LED is at a low level. This control mode is adopted in our design. In our design, when I_LED is more than 25% of its full value, linear control mode is used. When I_LED is less than 25% of its full value, PWM control mode is used. The benefit of doing so is to save power compared to a fully PWM control mode being used over the entire current range from 0% to 100%. The hybrid control mode diagram is shown in Figure 32.

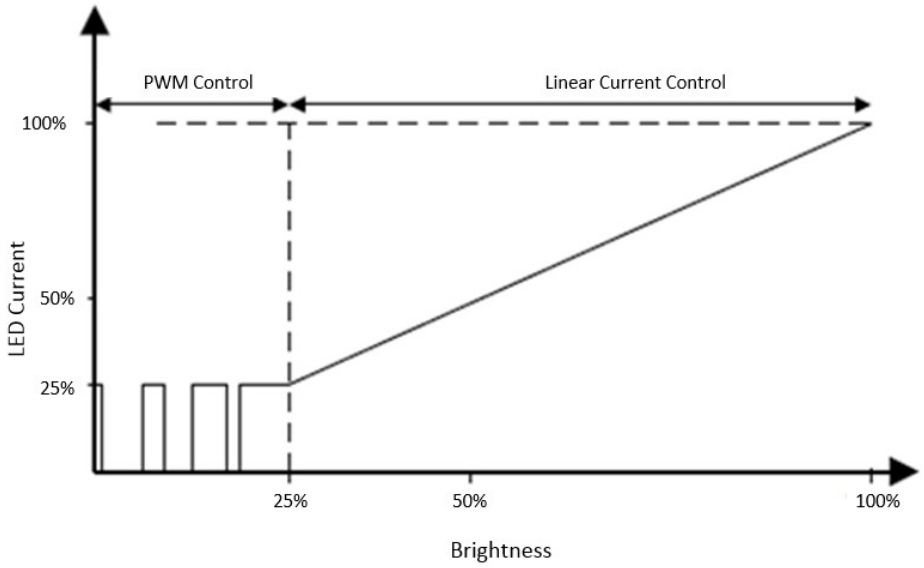


Figure 32. Brightness to LED Current Relationship in Hybrid PWM and Linear Current Control Mode.

The hybrid PWM LED current control mode has been used in several commercial products recently. One example is the LED driver product LP8557 from Texas Instruments [2-17].

4 DESIGN STRUCTURE OF THE ENTIRE LED DRIVER SYSTEM

This chapter describes the basic design specifications and basic building structures of the design cells.

4.1 System Design Considerations

Based on the system application requirements and the purpose of a competitive design, some electrical characteristics and specifications are created as guidance and targets for the design. They are summarized in the following subsections.

4.1.1 Boost Regulator Electrical Characteristics

Table 2 gives the basic design specifications and guidelines for the boost regulator based on the planned targets of the innovative design in this dissertation.

Table 2. Boost Regulator Electrical Design Specifications

Specifications						
Symbol	**Parameter name**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
R_{DS}_ON	Power NMOS switch ON	I_{SW} = 0.5 A		0.2		Ω
V_{BOOST}_MIN	Minimum output voltage	Typical condition		7		V
V_{BOOST}_MAX	Maximum output voltage	Typical condition		28		
I_{SW_CL}	Switching node pin current	Typical condition		2.4		A
I_{LOAD_MAX}	Maximum continuous load current	I_{SW}_LIM = 2.4 A VIN = 3 V, VOUT = 24 V		160		mA
f_{SW}	Switching frequency	Typical condition		1000		kHz
t_{PULSE} _MIN	Switch pulse minimum width	No load		60		ns

Typical conditions are defined at T_A = 25°C, V_{DD} = 3.6 V.

4.1.2 LED Driver System Electrical Characteristics

Table 3 gives the basic design specification and guidelines for the LED driver system based on the planned targets of the innovative design in this dissertation.

Table 3. LED Driver System Electrical Specifications

Specifications						
Symbol	**Parameter name**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
$I_{LEAKAGE}$	Leakage current	Outputs LED1...LED6, V_{OUT} = 28 V		1		µA
I_{LED}_MAX	Maximum sink current LED1...6	Typical condition, -40C to 85C		25		mA
I_{LED}_ACC	LED current accuracy	Output current set to 20 mA	–4		4	%
I_{MATCH}	Channel to Channel current	Output current set to 20 mA	-2	0.5	2	
V_{SAT}	Saturation voltage	Output current set to 20 mA		200		mV
n/a	LED current driver PWM Turn on /off	Output current set to 20 mA		100		ns
n/a	LED pin typical feedback regulation voltage	Output current set to 20 mA		0.4		V

Typical conditions are defined at T_A = 25°C, V_{DD} = 3.6 V.

4.2 LED Driver System Architecture and Its Cell Designs

As mentioned before, the design goals for the LED driver system are to make it an accurate and fast system. In addition to the previously listed references, additional analog integrated circuit design books such as [4-1], [4-2], [4-3] and [4-4] are also consulted during the detailed analog circuit design process.

4.2.1 Architecture Selection

There are multiple ways to design the LED driver system. The objective of this design is to achieve a very high-accuracy constant current LED driver system. Therefore, closed feedback loops are employed in the system. The overall system design is shown in Figure 33.

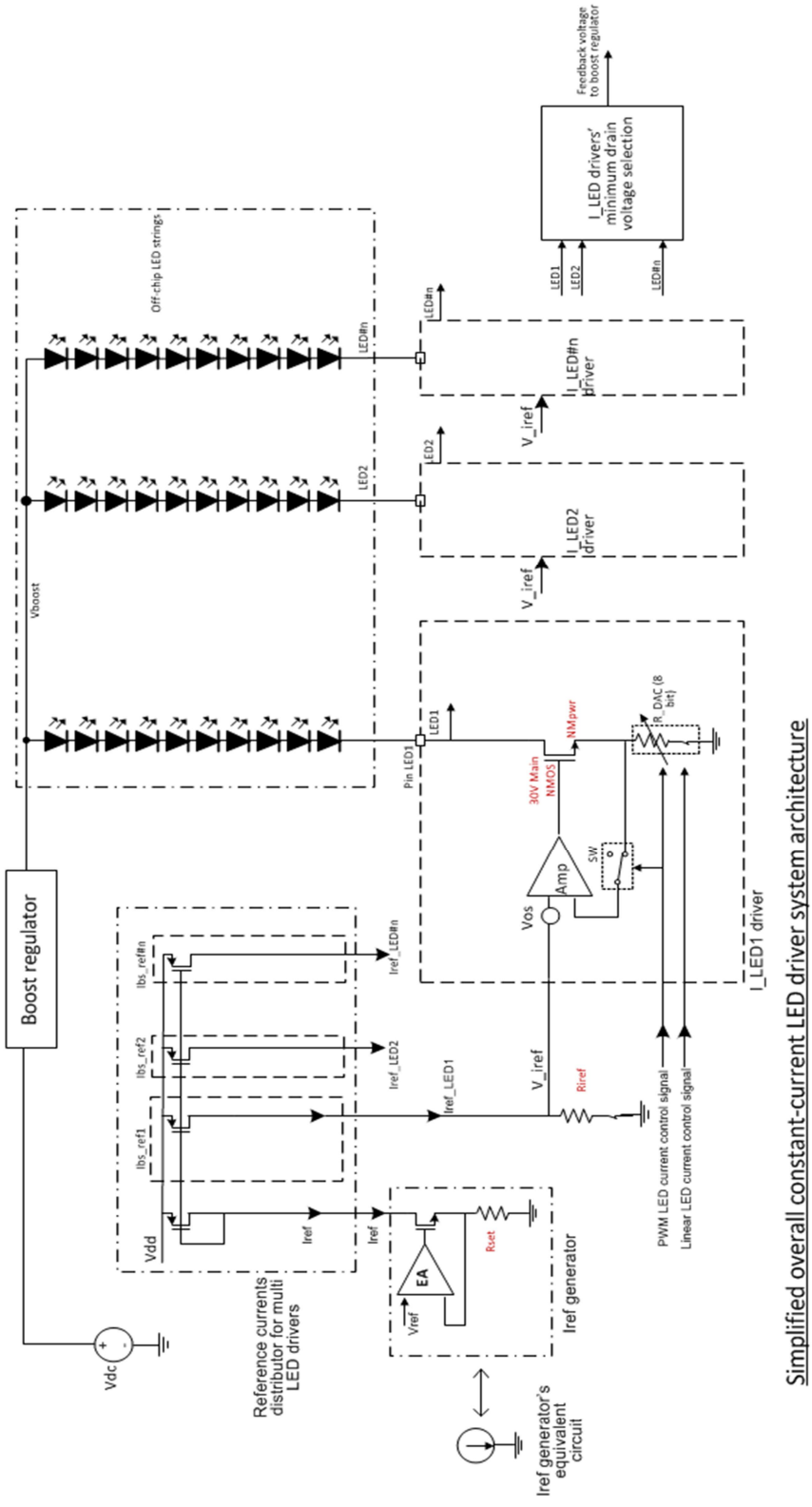


Figure 33. Simplified Overall LED Driver System Architecture with One Reference Resistor $R_{iref.}$

The system has three major sections.

The first section is called ‘Iref generator’. It uses a closed feedback loop to generate an accurate reference current ‘Iref’ based on a given resistor ‘Rset’ and a given accurate bandgap reference voltage ‘Vref’. This section is functionally equivalent to a current source.

The second section is termed ‘Reference currents distributor for multi LED drivers’. This section converts the reference current ‘Iref’ into multiple reference currents ‘Iref_LED1’, ‘Iref_LED2’, etc. based on the system design requirement. This section performs as a current mirror circuit with multiple current outputs.

The third section is a group of identical constant-current drivers for the LED strings. They are called ‘I_LED1 driver’, I_LED2 driver’, I_LED#n driver’ for LED1 string, LED2 string and LED#n string, respectively. Each driver uses the given reference input voltage ‘V_iref’ to accurately generate a constant DC current.

This architecture is the foundation of the proposed LED driver system. For accurate system performance, suitable design techniques must be applied to remove all the mismatches and offset voltages existing in the system. Otherwise, the designed result will not meet the proposed accuracy specifications.

4.2.2 The Overall LED Driver System Architecture

The LED driver system is shown as part of the circuit diagram in Figure 33. The overall LED driver system includes a reference current generator ‘I_ref generator’, six LED current drivers ‘I_LED# driver’, where ‘#’ represents 1 to 6, and a minimum voltage selection circuit ‘I_LED minimum drain voltage selection’.

4.2.3 Circuit Structures to Overcome Error Sources in The LED Driver System

Each of the three major sections can introduce errors into the system. The first step to improve system accuracy is to identify all the major error sources in the system.

4.2.3.1 Reference Current 'Iref' Generator and Its Introduced Error Treatment

The 'Iref generator' circuit diagram is shown in Figure 34. 'Iref' is the referenced current which will be used to generate all six LED reference currents.

In the 'Iref generator', the major error contribution is from the Rset variation. Therefore in our design, Rset will be an accurate external resistor. An off-chip resistor can have 1% accuracy or even better, whereas the accuracy of an on-chip resistor can only be as good as 15% to 20%. The input offset of the error amplifier 'EA', which is designed to be 2 mV/sigma, will contribute a negligible error if we set the 'Vref' voltage to be as large as the bandgap voltage 1.25 V.

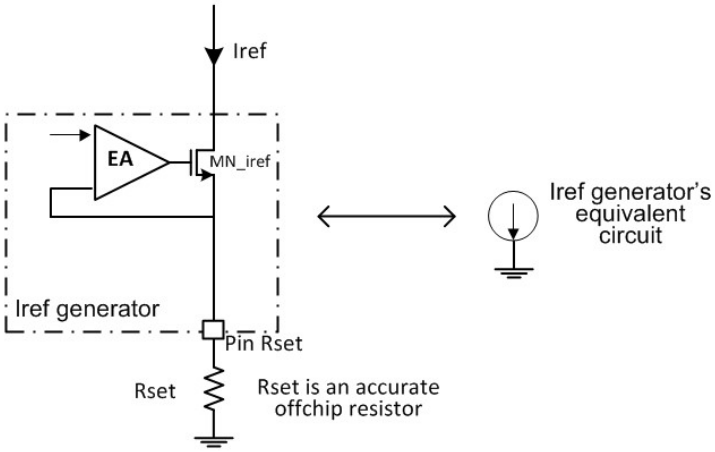


Figure 34. Circuit Architecture of The Iref Generator.

The error amplifier 'EA' is a PMOS input stage folded cascode amplifier structure. Its simplified diagram is shown in Figure 35. The reason to use PMOS input stage is to accommodate any reference voltage from 0 V to 1.25 V.

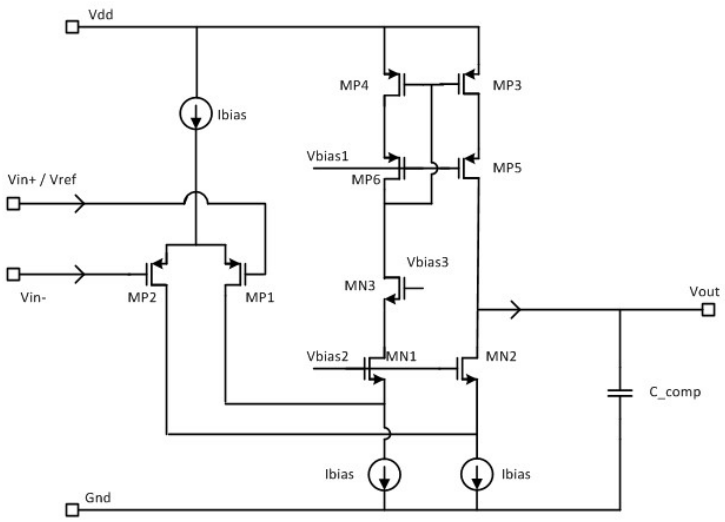


Figure 35. Simplified Folded Cascode Amplifier 'EA' Structure.

4.2.3.2 Reference Currents Distributor for LED Drivers and Its Introduced Error Treatment

The circuit 'Reference currents distributor for multi LED drivers' is a current mirror based circuit. Its main circuit error contribution to the whole LED driver system is the current mirror's mismatch among its current outputs. For a typically designed current mirror with regular cascode, the maximum mismatch error could still be up to a typical 3% to 5% over PVT (Process variation, Voltage range and Temperature range) at 6 sigma, based on our simulation results. Therefore, an actively regulated cascode is used to reduce the variation. Such an approach can reduce the current mirror mismatch down to 1.5% error at 6 sigma with reasonably large current mirror sizes, based on our simulation results. However, this 1.5% error is still a big contributor, which will cause our overall design to miss the overall 2%-3% channel-to-channel mismatch design target. To further improve the circuit, a creative dynamic current mirror design approach is taken to dramatically reduce this mismatch error to roughly 0.4% from 1.5% over PVT. The basic design architecture of such a dynamic current mirror is shown in Figure 36.

This circuit is part of the patent application in process now [5-2].

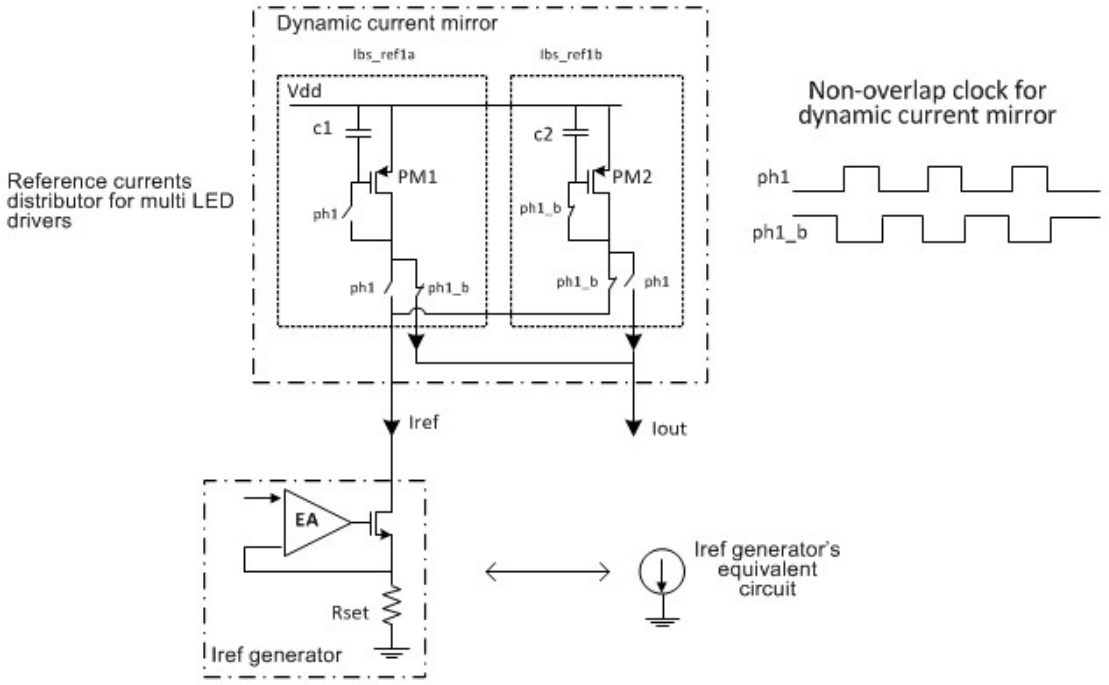


Figure 36. Simplified Dynamic Current Mirror Circuit Architecture.

As shown in Figure 36, a non-overlap clock is used in the system. During phase ‘ph1’, the ‘ph1’ controlled switches are closed while the ‘ph1_b’ controlled switches are opened. As a result, the PMOS PM1 is formed as a diode-connected PMOS and is charged by the reference current ‘Iref’. The gate voltage of PM2 is held by the holding capacitor C2 and its output current is constant; hence, PM2 acts as a current source. During phase ‘ph1_b’, the ‘ph1’ controlled switches are opened while ‘ph1_b’ controlled switches are closed. PM1 acts like a current source while PM2 is charged by the reference current ‘Iref’. PM1’s output current is equal to ‘Iref’ since it was set by the ‘Iref’ during ‘ph1’ cycle. The above two states occur alternately following the non-overlap clock.

This dynamic current mirror approach has much better accuracy over any conventional current mirrors. Unlike conventional current mirror approaches, the current outputs of the dynamic current mirror remain constant over PVT due to the nature of the frequent update of the ‘Iref’ on PMOS devices PM1 and PM2, following the non-overlapping clocks. The major error source in this

design is the charge injection of those switches during their turn-on and turn-off times. With properly large sizes of holding capacitors C1 and C2, this charge injection error can be minimized to be negligible.

4.2.3.3 Constant Current LED Driver and Its Introduced Error Treatment

The constant current LED driver circuit diagram is shown in Figure 37. 'I_LED driver' represents one of the constant current LED drivers in the system. The constant current LED drivers are the final output stage of the overall LED driver system, which directly supply constant current for their respective LED strings. In each LED driver design, the first major error contribution is the input offset 'Vos' of the error amplifier 'Amp'. The second major error is the mismatch error between the reference setting resistor Riref and the LED current output setting resistor R_DAC.

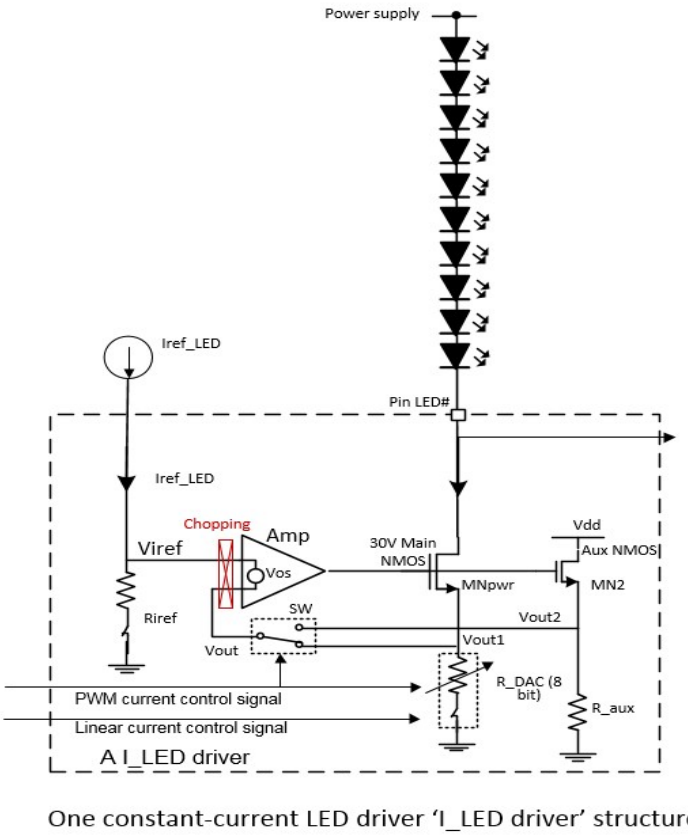


Figure 37. Constant Current LED Driver with a Distributed Reference Current Iref_LED.

To overcome the first error, a chopping scheme is employed for the error amplifier in this design. The chopping amplifier uses a high-speed switching chopping clock and structure to move the DC input offset voltage from DC voltage (zero frequency) to the chopping frequency where the noise is not a concern. For LED lighting in this application, the forbidden frequency spectrum is the audio frequency range from 10 Hz to 20 kHz. Therefore, a chopping frequency above 20 kHz is generally applied. For the best optimized effort, the 1 MHz clock frequency of the boost regulator in the LED driver system is selected so that this chopping noise is overlapped with the boost regulator switching frequency noise at the same frequency (1 MHz). As a result, these two noises can be filtered out together.

For the second error, if we use one single resistor Riref for multiple I_LED drivers as shown in Figure 33, we will suffer from an additional inaccuracy caused by the voltage differences among all the I_LED driver grounds due to different LED current values and different parasitic resistances on the metal traces. This error can lead to an additional 1%-2% inaccuracy in the overall system based on the system simulation and calculation. Therefore, it is better to assign one reference resistor Riref for each LED driver so that each Riref and its respective I_LED driver can be grounded together easily, as shown in Figure 37. As a result, each I_LED driver and its reference resistor Riref will have a common ground. The second error is completely removed.

4.2.3.4 Improvement of the 'I_LED Driver' Driving Speed During PWM Transitions

As shown in Figure 37, the output LED current is also subject to a PWM mode control, in which the I_LED (LED output current) will turn fully on during the PWM's on duty and will turn fully off during PWM's off duty. The PWM logic input signal is called 'PWM current control signal' in the diagram and it is from the chip's central digital logic block. The PWM logic duty cycle range is from 0% to 100%. For high output accuracy, it is required that the I_LED driver must respond fast enough to this input PWM logic signal. Otherwise, if the I_LED driver has a slow response, then its output current will not satisfy the accuracy requirement defined by the PWM duty. Such a case is especially true at a low PWM duty cycle (such as from 1% to 10%).

To achieve this PWM duty based accuracy, a special design idea has been successfully implemented on the ‘Amp’ design and the entire feedback loop design of the ‘I_LED driver’ to accelerate their turn-on/off speed without dramatically increasing the quiescent current. This improvement technique is to increase the driving slew rate of the ‘Amp’ during the PWM on/off transition times. Another improvement technique is to keep the whole feedback loop always active by alternating the feedback voltage by controlling the switch ‘SW’ in the diagram. During the PWM on duty (on time), the feedback voltage of the control loop is taken from the main output branch formed by ‘MNpwr’ and ‘R_dac’, as shown in the circuit diagram. During the PWM off duty (off time), the feedback voltage is taken from an alternative output branch formed by ‘MN2 and ‘R_aux’, as shown in the diagram. Therefore, the feedback loop of the ‘I_LED Driver’ is kept always active. As a result, the gate of the high voltage NMOS device ‘MNpwr’ is always kept close to its normal operating voltage. During the PWM on duty, the overall feedback control loop can quickly recover the ‘MNpwr’ device into its normal operating condition.

A patent application for this circuit architecture has been filed with the US Patent and Trademark Office and it is in the process now [5-3].

4.2.4 LED Minimum Voltage Selection for Boost Regulator Feedback Voltage

As shown in Figure 33, there is a ‘‘I_LED drivers’ minimum drain voltage selection circuit’, which selects the minimum LED voltage and then sends it as feedback to the boost regulator. This circuit can be implemented using an analog ‘OR’ function. The circuit diagram is shown in Figure 38.

‘LED1’ to ‘LED6’ are the six input pins which are the nodes of the bottom voltages of the six LED strings, respectively. NMOS devices MN1 to MN6 are the six 30 V devices used to protect the internal devices MP1 to MP6, respectively. MP1 to MP6 are the six PMOS devices performing the analog ‘OR’ function. Their output voltage node ‘ Vled_min_feedback’ is sent to one input of the error amplifier of the boost regulator control loop. To accommendate voltage levelshifting due to the analog ‘OR’ function, the reference voltage ‘vref’ in the circuit digram is also level shifted up

via the PMOS device MP7 and then is sent to the other input of the error amplifier.

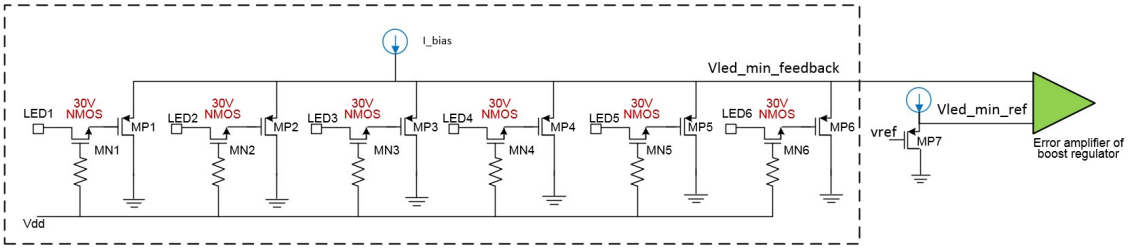


Figure 38. A Minimum LED Voltage Selection and Feedback Circuit.

4.3 Boost Regulator Architecture and Its Cell Designs

4.3.1 Architecture Selection

4.3.1.1 The Type of Boost Regulator Control Architecture to Use

This is a mobile application requiring less noise; therefore, PWM peak current mode is chosen. The PWM mode will help to confine all switching noise at the switching frequency. Some EMI (electro-magnetic interference) reduction can be achieved by adjusting the PWM switching speed. The peak current mode has advantages of easier loop stability design and faster transient responses than the regular voltage mode.

4.3.1.2 Digital Control versus Analog Control for Boost Regulator

The core control approach of the boost regulator is chosen as analog. A digital control core has a major advantage – it is programmable and it can be easily scaled and reused for any future designs. However, in terms of die area, transient response speed and operating quiescent current Idd, digital control is not always advantageous because a digital control loop for the PWM peak current mode needs several ADCs (analog to digital converters) and analog current sensing. ADCs will consume additional current that is not otherwise needed in an analog core even though the digital logic consumes very low current.

The overall transient response speed of a digital control is limited by 1) the clock frequency for the digital control logic; and 2) the intrinsic speeds of the ADCs. On the other hand, analog control core does not have such a limitation.

4.3.1.3 Continuous Current Mode versus Discontinuous Current Mode

A continuous current mode switching boost regulator will have less ringing noise and EMI due to the smaller peak current compared to a discontinuous current mode unit. It will also help to reduce the cost of the inductors and capacitors since the smaller spike currents in the continuous current mode regulators mean lower prices for any inductors and capacitors. The higher the spike currents, the more expensive are the inductors and capacitors. The continuous current mode is therefore a preferable solution for mobile applications, which usually require a less noisy environment.

4.3.2 Final Boost Regulator Architecture

Based on all the above considerations, the boost regulator is chosen as a PWM fixed frequency peak current mode regulator. Its functional diagram is shown in Figure 39.

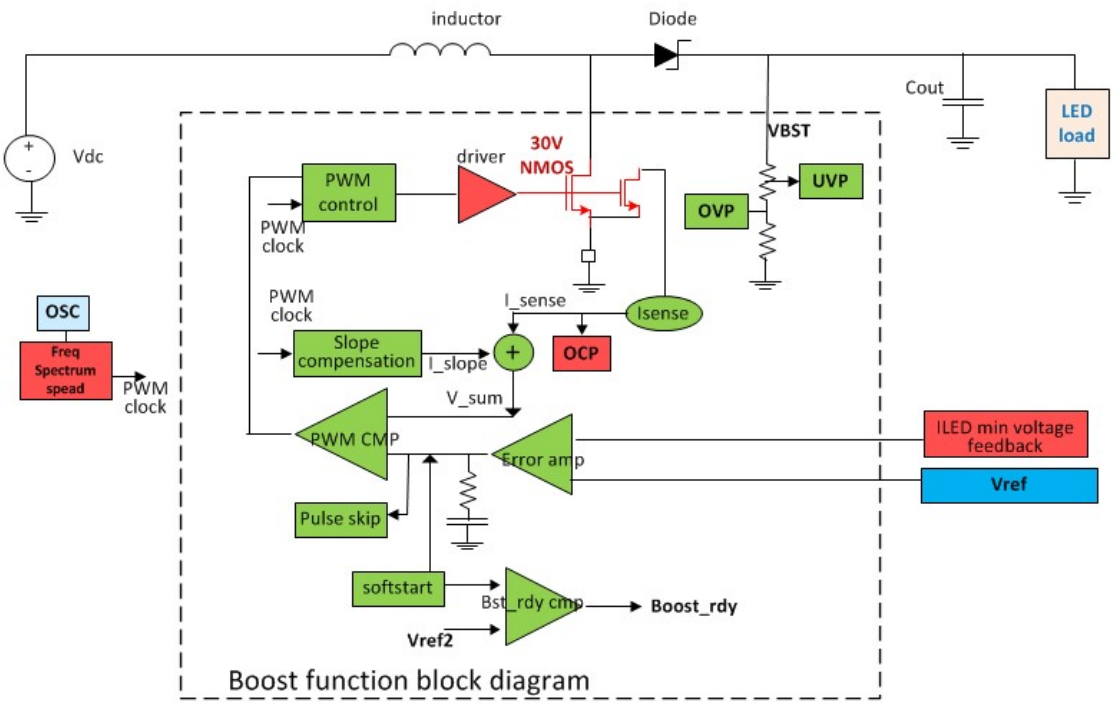


Figure 39. Proposed Boost Regulator Architecture Diagram.

The following performance attributes are the major design considerations.

1) Loop stability,
2) Peak current limit function,
3) Line regulation,
4) Load regulation, and
5) Output voltage accuracy.

4.3.3 The Major Cell Designs and Their Architectures

The following subsections describe the structures and considerations of all the individual major design blocks/cells.

4.3.3.1 30 V NMOS Power Switch

This is just a single 30 V NMOS as shown in the proposed boost regulator architecture diagram of Figure 39. It is the major power switch which has to sustain 30 V. It is designed to be a typical 0.2 Ω power switch.

4.3.3.2 The Driver for The Power Switch

The 'driver' in Figure 39 is designed to have two separate, but identical, drivers in parallel. Normally both drivers are used. A logic control signal is employed to turn off one driver in order to set a slower driving speed. The purpose is to control the turn on/off slew rate and time in order to reduce switching noise, which is directly related to EMI noise.

An anti-shoot-through logic is also added for the last stage of the drivers.

4.3.3.3 Peak Current Sensing Circuit – 'Isense'

'Isense' in the boost regulator architecture is the current sensing circuit. The circuit diagram is shown in Figure 40. This current sensing circuit provides two functions for the boost regulator: 1) create a ramp signal for the PWM comparator; and 2) provide a signal for peak current limit detection. The peak current limit is used to limit the maximum peak current in the inductor for device protection purpose.

This design uses a common-gate input amplifier to sense Vds of the power NMOS and generate an output current based on the sensed Vds. The output current passes through a poly resistor to provide a sensed voltage. This current sensing approach has an output voltage variation due to the matching of the Rdson of the power NMOS and that of the sense NMOS, input offset of the amplifier, and the current mirror output variation. The total variation is more or less around 50% over PVT based on the simulation data. Therefore, a trim circuit is usually added in the design to adjust the 'Isense' output to a pre-defined target value during production test time. The trim process will reduce the entire error to a pre-defined and acceptable low level.

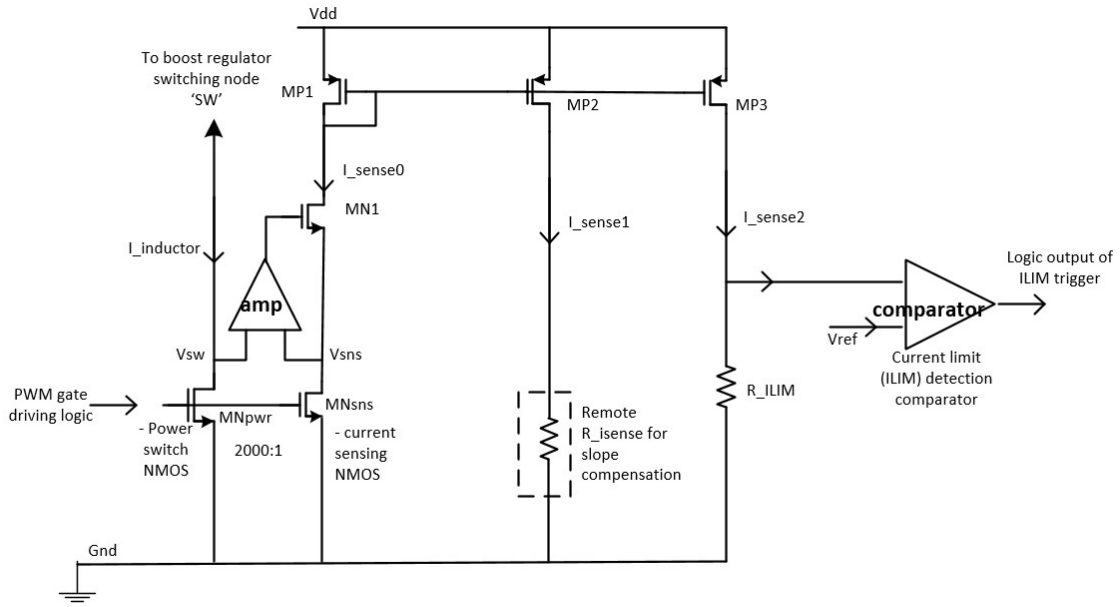


Figure 40. Current Sense and Peak Current Limit Circuit Architecture.

Figure 40 shows the circuit diagram during its operating state when the power switch 'MNpwr' is turned on. In Figure 40, the device 'MNpwr' is the power switch of the boost regulator. 'MNsns' is the current sense device. These two devices have a device width ratio of 2000:1, as an example in the circuit diagram, while their device lengths are the same. The amplifier 'amp' and the NMOS device 'MN1' form a feedback loop which forces node 'Vsns' to be equal to node 'Vsw'. As a result, in this case, the output current 'I_sense0' is 1/2000 of the sensed current 'I_inductor'.

'MP1', 'MP2' and 'MP3' form a current mirror. As a result, I_sense1' = 'I_sense2' = 'I_sense0'. 'Isense1' is sent to a remote resistor for slope compensation usage. 'I_sense2' is used for current limit detection design.

4.3.3.4 Current Limit 'ILIM' with Trim

'ILIM' represents the peak current limit in this dissertation. The current limit design is shown as part of the design in Figure 40. The ILIM logic output is triggered when the sensing output current 'I_sense2' reaches a pre-defined threshold. The cell design is in combination with 'Isense' circuit due to their closely correlated nature.

4.3.3.5 Error Amplifier with Compensation

The circuit diagram is shown in Figure 41. This is the main error amplifier with its associated compensation network for the boost regulator feedback loop. The error amplifier employs a gm-C (transconductance-capacitor) type of amplifier. It is a folded cascode error amplifier structure. The associated feedback loop compensation network, formed by resistor R_comp and capacitor C_comp for system stability design, are also shown in the circuit diagram.

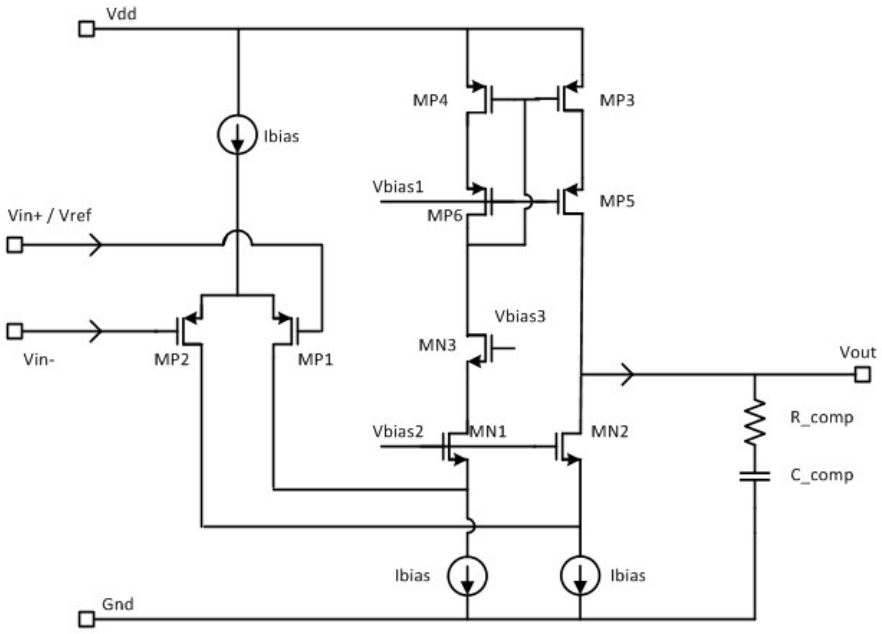


Figure 41. Simplified Boost Regulator Gm Amplifier with Compensation Network.

4.3.3.6 Slope Compensation Cell and The Summation Cell

Slope compensation is a specialized compensation circuit for peak current mode based switching regulators to eliminate their potential sub-harmonic oscillation. The theory of slope compensation has been explained in many design books and papers. Reference [3-1] has a good explanation.

The simplified ‘slope compensation’ and ‘summation’ circuit architecture diagrams are shown in Figure 42. The slope compensation current generation circuit is shown in Figure 42 (a).

The summation circuit is used to add the slope compensation signal to the sensed peak current signal, which is from the current sensing cell ‘Isense’. To reduce operating current consumption, a resistor-based analog adder is used for the summation cell, refer to Figure 42 (b).

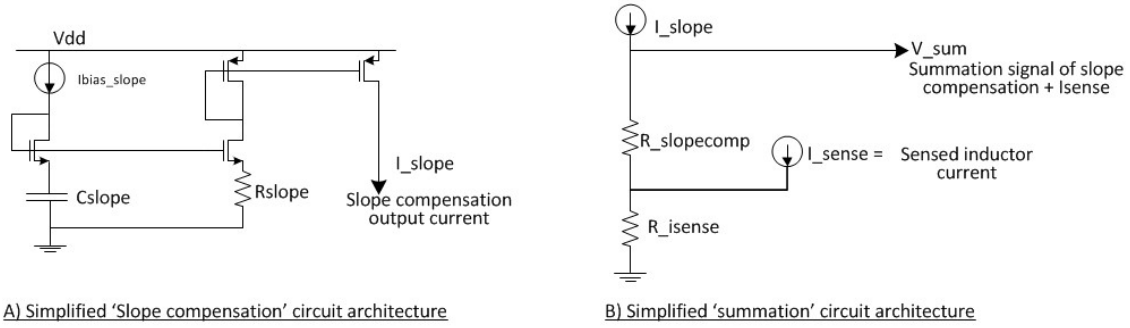


Figure 42. Slope Compensation Circuit Architecture and Summation Circuit Architecture.

Note that the resistor values for ‘Isense’ and ‘slope compensation’ are calculated based on the sub-harmonic stability criterion for all resistor and current mirror process variations. An additional fixed bias current via ‘R_slopecomp’ and ‘R_isense’ is also needed in the real design to keep a minimum common mode voltage on the slope compensation input.

4.3.3.7 The Soft-Start Circuit

This softstart circuit ‘softstart’ is used to slowly and softly start the boost regulator. It uses a fixed biasing current to slowly charge up a capacitor connected to the reference voltage. As a result, the reference voltage is slowly raised up and the soft-start function is achieved. This circuit is not incorporated in this dissertation since it is not essential.

4.3.3.8 PWM Comparator

The PWM comparator circuit ‘PWM CMP’, as shown in Figure 39, is used to generate PWM clock signals by comparing the two inputs: 1) the output of the error amplifier, and 2) the generated ramp signal (Iramp + slope comp).

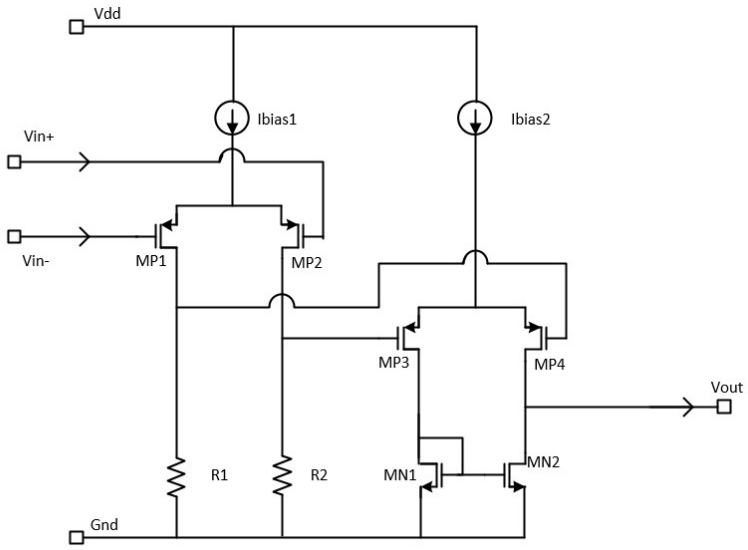


Figure 43. PWM Comparator Architecture.

This comparator circuit is a PMOS differential pair input based comparator as shown in Figure 43. It utilizes a two-stage cascade structure. The first stage comparator is formed by Ibias1, MP1, MP2, R1 and R2. The main purpose is to allow it to adapt the low-side input common mode range of roughly 0 V. The use of resistors R1 and R2 as the output stage of the first comparator achieves a faster circuit compared to a conventional NMOS-current-mirror based output stage. The second stage comparator is formed by Ibias2, MP3, MP4, MN2 and MN2. It is a regular comparator using a current-mirrored-output stage to allow a large output voltage swing. The overall comparator design is a fast circuit.

4.3.3.9 PWM Control

The boost regulator's PWM logic control cell 'PWM control' incorporates all the given logic inputs via logic circuits to a decision on when and how to turn on/off the power switch. This is a pure logic cell with latches.

The following functions are implemented in this logic cell.

1. Normal PWM operation logic which is latch-based. The reason to use latches is to remove the ringing on the signals due to the noisy environment.
2. Peak current limit function.
3. Boost regulator turn on/off logic.
4. Output-voltage-too-low protection logic.
5. Pulse skip logic.
6. Shutdown logic. The boost regulator cannot be immediately shut down when IL (inductor current) is still high. The LED drivers need to be shut down first. Logic is implemented to first reduce the duty cycle to its low end, and then shut the boost regulator down.

4.3.3.10 Pulse-Skipping Mode Detection Circuit

The pulse-skipping mode detection design uses an internal burst-mode control scheme. The idea is to monitor the error amplifier output voltage ‘eampout’ as the gross inductor peak current information. Then use a sample-and-hold circuit to remove the slope compensation information embedded in the ‘eampout’. Thereafter, compare this processed signal with a fixed preset voltage signal that represents the desired pulse skip peak current level. When ‘eampout’ is less than the preset voltage, then skip pulse.

5 FINAL DESIGN IMPLEMENTATIONS AND SIMULATIONS

In this chapter, the proposed system modeling is first simulated. Based on the successful model, detailed circuits are implemented. At the end, the overall system is integrated together and simulated. The simulation verifies that the results are successful.

All the circuit schematics and simulations in this dissertation are designed in the Cadence design environment [5-1].

5.1 Modeling Simulation of the Proposed System

The overall system includes both the boost regulator and the LED drivers. Based on the proposed system, a system model is established as the first step to verify the system function.

The entire system model is set up based on Figure 33. Additional voltage sources and enabling signals to control the system are used to perform different operation modes.

The simulation results are given in Figure 44, Figure 45 and Figure 46.

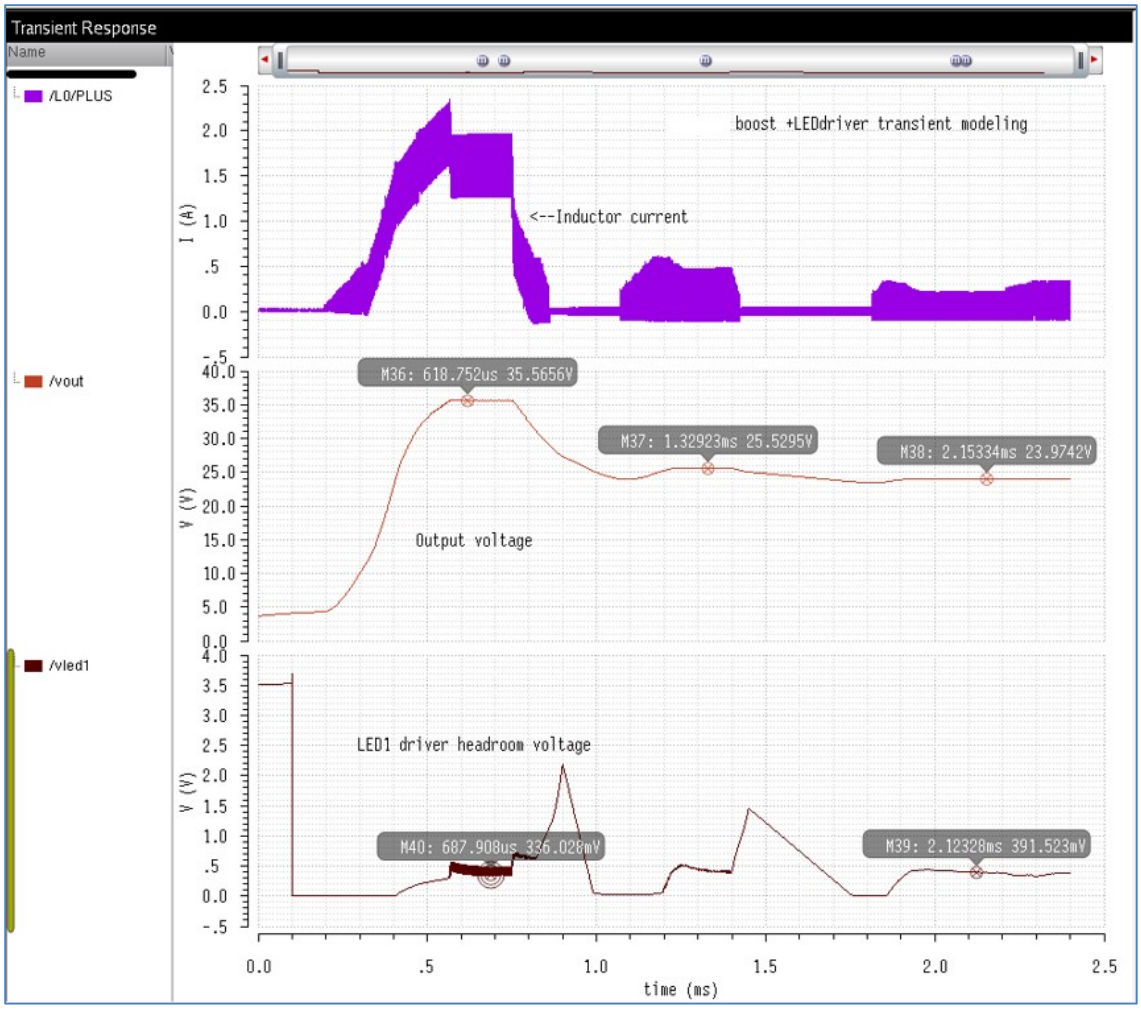


Figure 44. Overall Simulation Result 1 of the ‘Boost + LED Driver’ Model.

Figure 44 shows an overall system startup transition and normal operation modes at different LED current levels. The top signal ‘/L0/plus’ is the inductor current of the boost regulator, which is at switching mode. The signal responds adaptively to the output current load changes during the whole simulation period.

The second signal ‘/vout’ is the boost regulator output voltage. It runs up to 35 V at the initial startup time and then stabilizes. The ‘/vout’ is then reduced and remains at 25 V at roughly 1.2 ms following a load current reduction. Then it declines to 23.972 V at roughly 1.9 ms at a further load current reduction.

The third signal ‘/vled1’is the LED1 pin voltage. It always returns back and stays around 0.4 V at its own steady state after some overshoot and/or undershoot. The reference voltage for all voltage regulations at the LED1-LED6 pins is 0.4 V. It can be noticed that there is considerable switching noise on the signal ‘/vled1’ during the time from roughly 0.55 ms to 0.75 ms. One can conclude from the simulation plots in Figure 44 that the overall system design is stable over the simulation time.

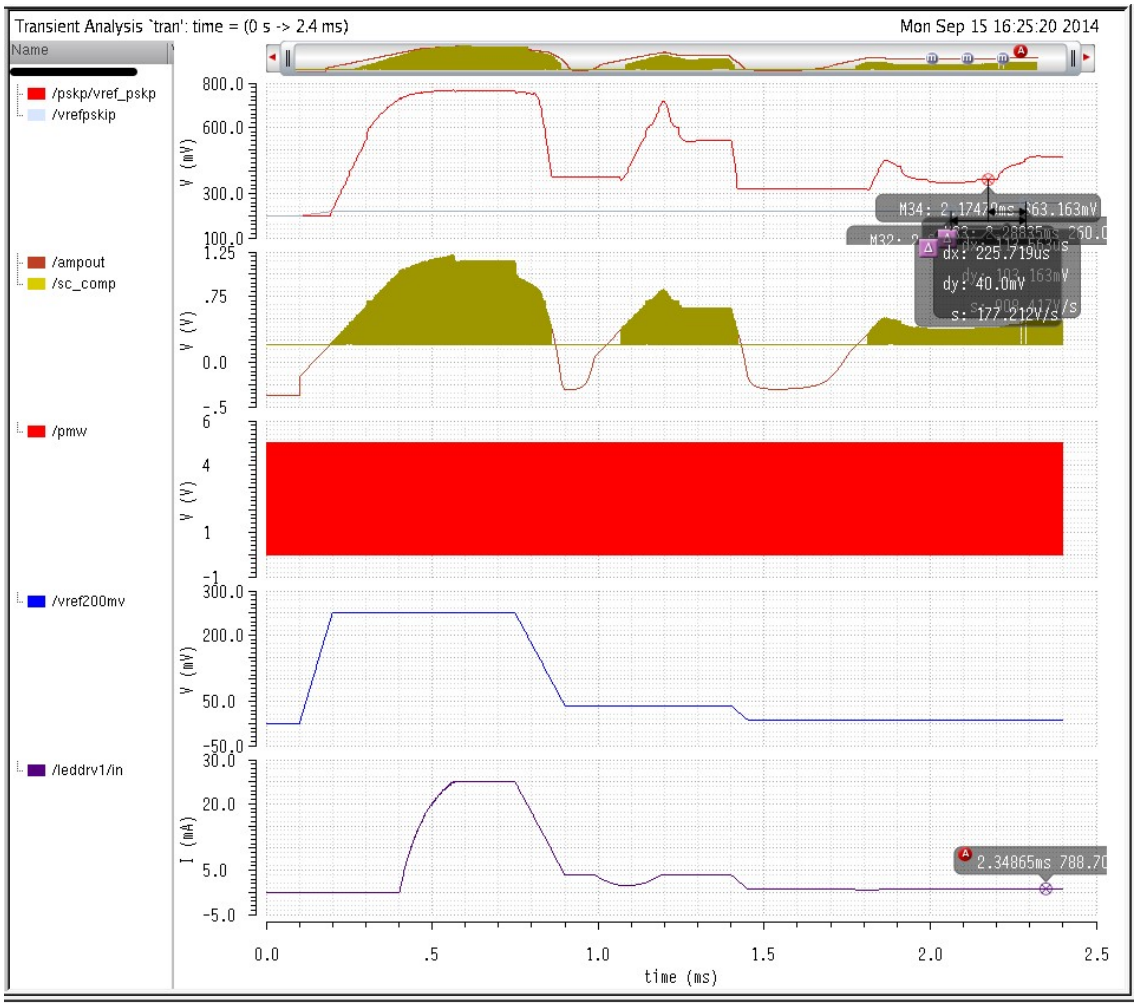


Figure 45. Overall Simulation Result 2 of the ‘boost + LED Driver’ Model.

Figure 45 shows some additional signals from the same simulation result. The graph mainly shows 1) the error amplifier output signal ‘/ampout’ of the boost regulator, 2) the internal PWM output signal ‘/pmw’ to the boost regulator power switch, 3) the LED1 current ‘/leddrv1/in’, 4) the

current control signal ‘/vref200mv’ which directly represents the boost regulator’s load current changes, and 5) the pulse skip mode signal ‘/pskip/vrefpskip’.

It can be seen from Figure 45 that, 1) ‘/ampout’ responds to the output load condition changes accordingly; 2) the internal PWM output signal ‘/pmw’ keeps its proper operation over the whole simulation time; 3) the LED1 current ‘/leddrv1/in’ adjusts itself accordingly to follow the signal ‘/vref200mv’ changes over the entire simulation time; 4) at roughly 2.0 ms, the signal ‘/pskip/vrefpskip’ becomes fluctuated because the boost regulator enters the pulse skip mode since the output load current becomes so small.

Figure 46 is a zoom-in plot of Figure 45 at the time of roughly 2.2 ms. It provides a close look at the detailed pulse skip mode operation.

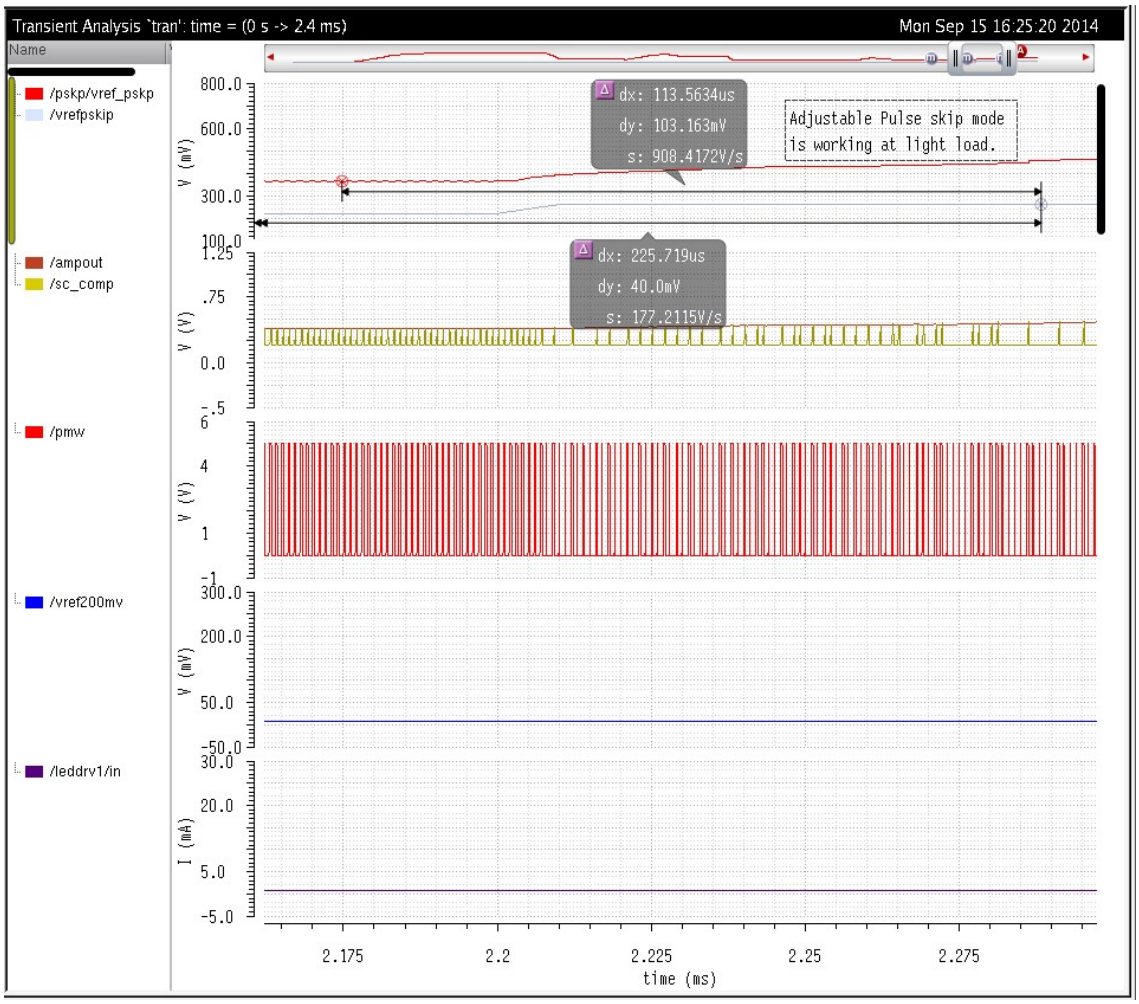


Figure 46. Zoom-in Plot of the Model Simulation Showing the Adjustable Pulse Skip Mode.

All of the above simulation results show that the entire system, comprised of both the boost regulator and the LED driver system, operates steadily and performs as required. In the simulation, the LED drivers are 6 identical closed-loop-regulated constant current LED drivers.

5.2 Design of the Proposed LED Driver System and Circuits

The final overall system design is shown in Figure 47. As shown in the diagram, there are total of six LED driver channels. So, six reference currents are needed. A reference current (Iref_LED1 to

Iref_LED6) is sent to each LED driver, respectively. Overall, the six constant current LED drivers, the reference current generation circuit and the minimum voltage selector circuit are all included in the system.

This novel system architecture has been filed as a U.S. patent application [5-2]. In the following subsections, all the major design blocks are described.

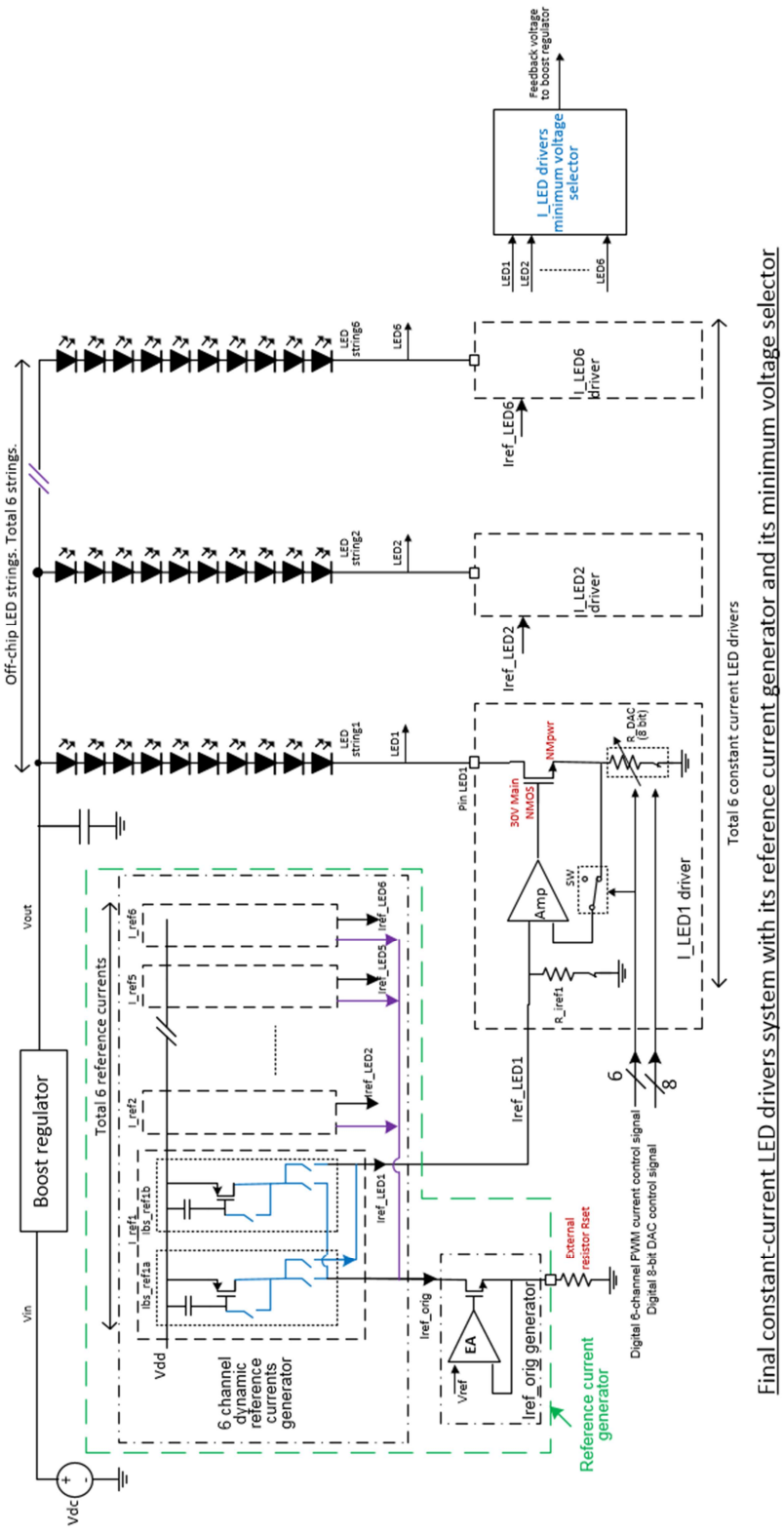


Figure 47. Final Designed Constant Current LED Driver System.

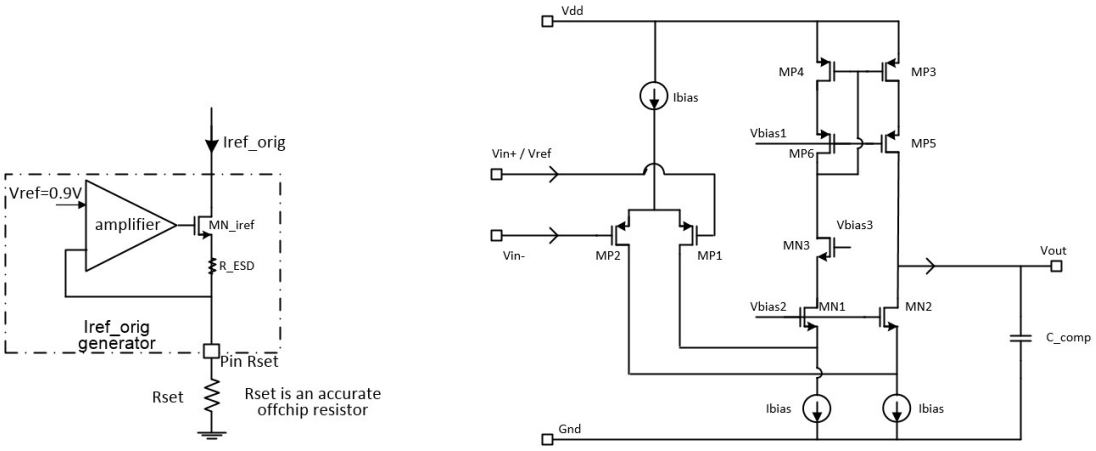
5.2.1 The Reference Current Generator

5.2.1.1 Initial Base Reference Current Generator 'Iref_orig generator'

The initial base reference current 'Iref_orig' is generated by a closed feedback loop shown in Figure 48 (A). A given reference voltage 'Vref' is applied to the top of the external resistor 'Rset' via the closed loop. As a result, it can be seen that the relationship is:

$$\text{Iref\_orig} = \frac{\text{Vref}}{\text{Rset}} \qquad (10)$$

The structure of the amplifier is shown in Figure 48 (B). It is a regular differential input folded cascoded amplifier.



(A) Iref_orig generator (B) Internal structure of the amplifier

Figure 48. Original Reference Current Control Loop for Dynamic Reference Current Generator.

5.2.1.2 The Dynamic Reference Currents Generator and Its Digital Logic

As shown in Figure 47, the dynamic reference currents generator is to produce highly accurate biasing currents for the six LED current drivers in terms of total accuracy and channel-to-channel mismatch. The final designed circuit diagram is in Figure 49.

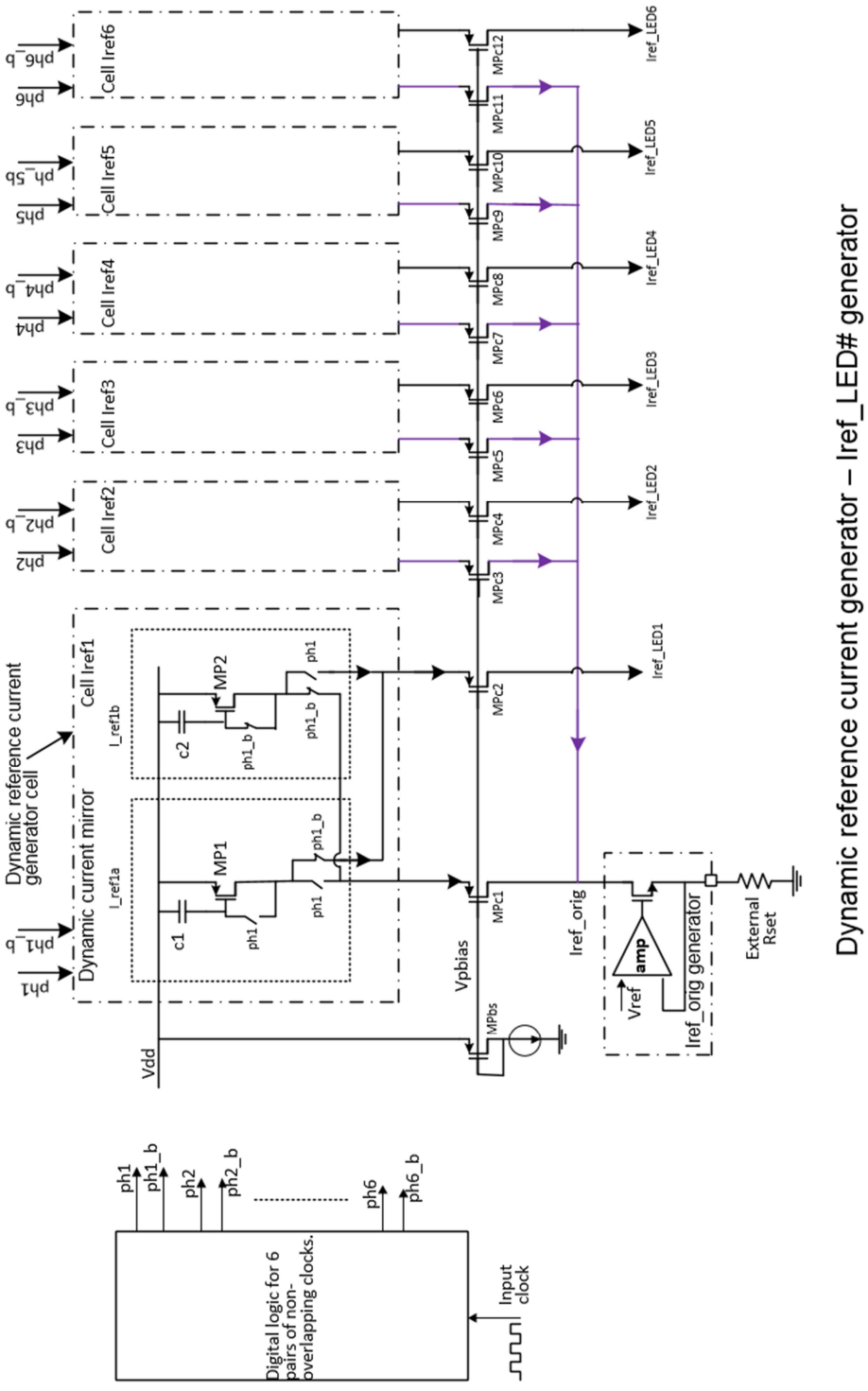


Figure 49. Dynamic Reference Current Generator Circuit of LED Driver System.

In Figure 49, the PMOS device ‘MPbs’ is used to generate a biasing voltage for all the twelve cascoding PMOS devices MPc1 - MPc12. They are newly added in the final design. These devices are used to cascode the dynamic current mirror outputs in order to reduce the channel length modulation effect of the current mirrors. The channel length modulation effect can deteriorate the current mirror output current accuracy.

Also in Figure 49, there is a six-phase non-overlap clock generated by the digital logic cell ‘Digital logic for 6 pairs of non-overlapping clocks’ on the basis of a given input clock signal. The input clock signal is actually chosen to be the same boost regulator clock signal because it makes synchronization easy. The digital logic circuit design is shown in Figure 50. The synchronized output clock waveforms are shown in Figure 51.

All the output clock signals are non-overlapping to prevent current leaking between any two different phases. Any current leakage causing a voltage change on the holding capacitors such as C1 and C2 will lead to an error in the accuracy of the overall dynamic current mirror performance. Proper design of the non-overlapping clocks can completely remove this error.

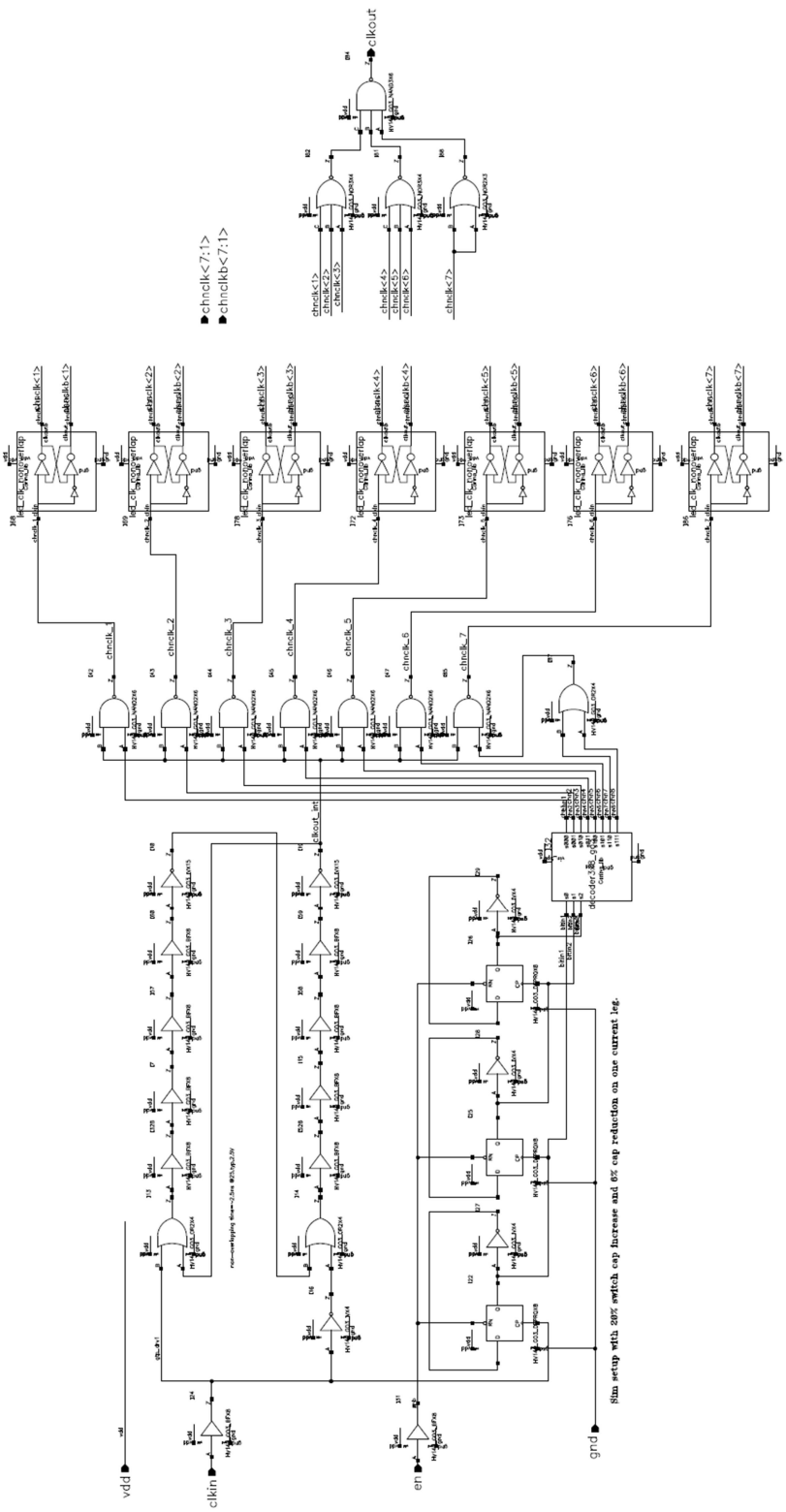


Figure 50. Digital Logic for the Six Channel Dynamic Reference Currents Generator.

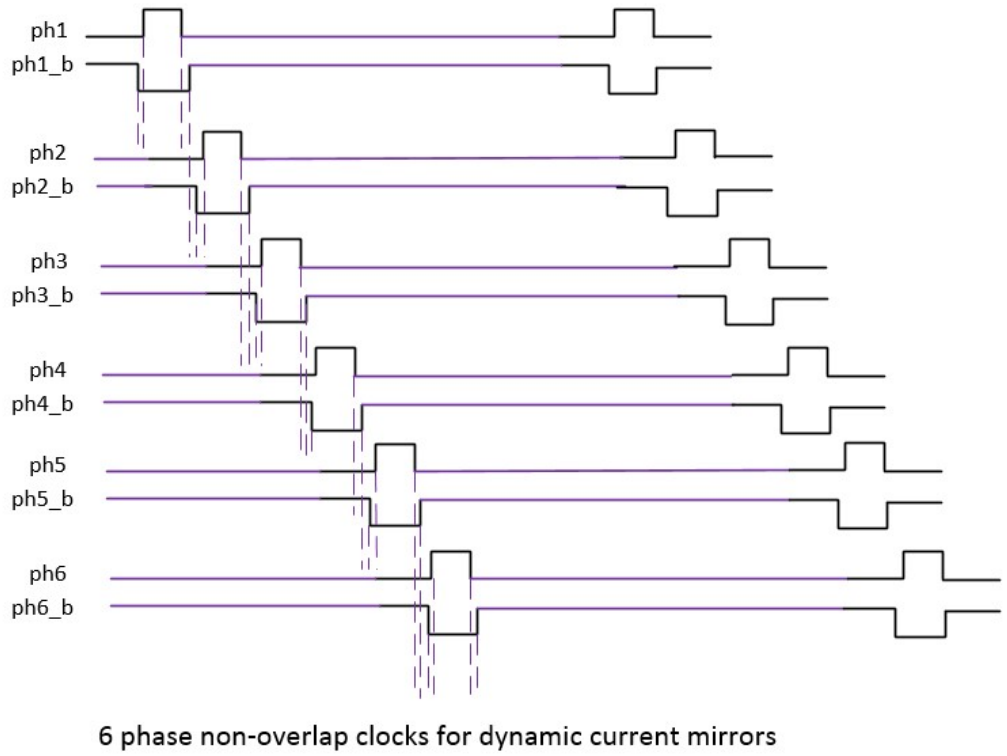


Figure 51. Six Phase Non-Overlap Clocks for Dynamic Current Mirror.

Since this dynamic current mirror is similar to a switching capacitor circuit, the well-known electronic charge injection problem during a switch turning on/off for any switch capacitor circuit is also a potential concern for this dynamic current mirror design. The injected electronic charges stored on holding capacitors due to any switch turning off causes an error in the current mirror accuracy. This error cannot be completely removed due to the operation of those switches. It can only be minimized by 1) reducing the sizes of the switches, and/or 2) increasing the sizes of those holding capacitors. Fortunately, the above two techniques can be implemented together, and they are enough to keep the absolute value accuracy and matching accuracy of the current mirrors to be less than 0.5% over all the process corners, which is accurate enough for this design.

5.2.2 The Constant Current LED Driver Design

There are six LED drivers in the LED driver system. Each driver utilizes the same set of circuits as shown in Figure 52.

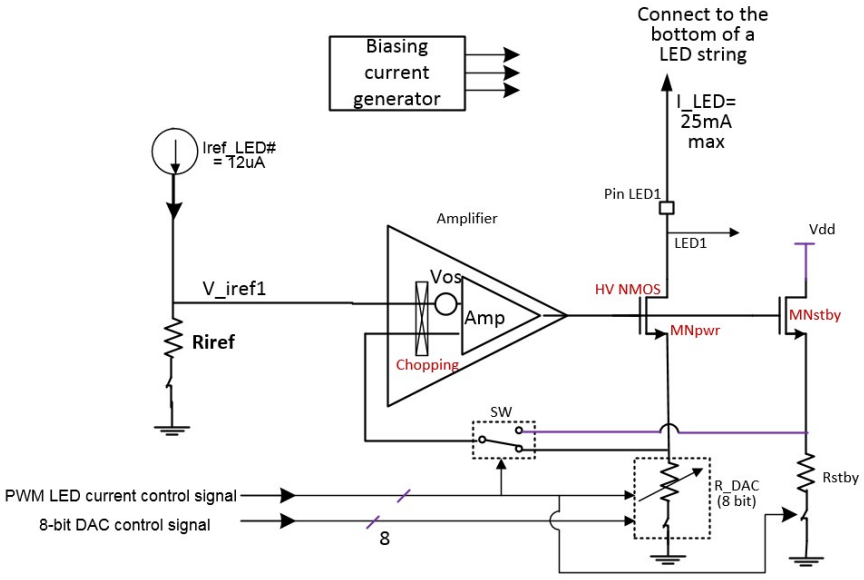


Figure 52. Top Level Schematic of One LED Output Driver.

The advantages of this LED driver design over the previous designs implemented by other engineers are:

1) Higher accuracy,
2) Fast PWM input signal response, and
3) Lower quiescent current.

Comparing to the previous designs, the disadvantage of this new design is that the die area has a minor increase since each LED driver needs an individual reference resistor ‘Riref’, as shown in Figure 52.

In the following subsections, detailed explanations for the design cells in Figure 52 are presented.

5.2.2.1 Biasing Current Generator

As shown in Figure 52, the ‘biasing current generator’ is used to supply quiescent biasing currents to all the analog circuits which need them. The detailed design is shown in Figure 53. A cascoded biasing current mirror technique is used in the design. This technique is a very popular and well-known approach to improve the current mirror accuracy.

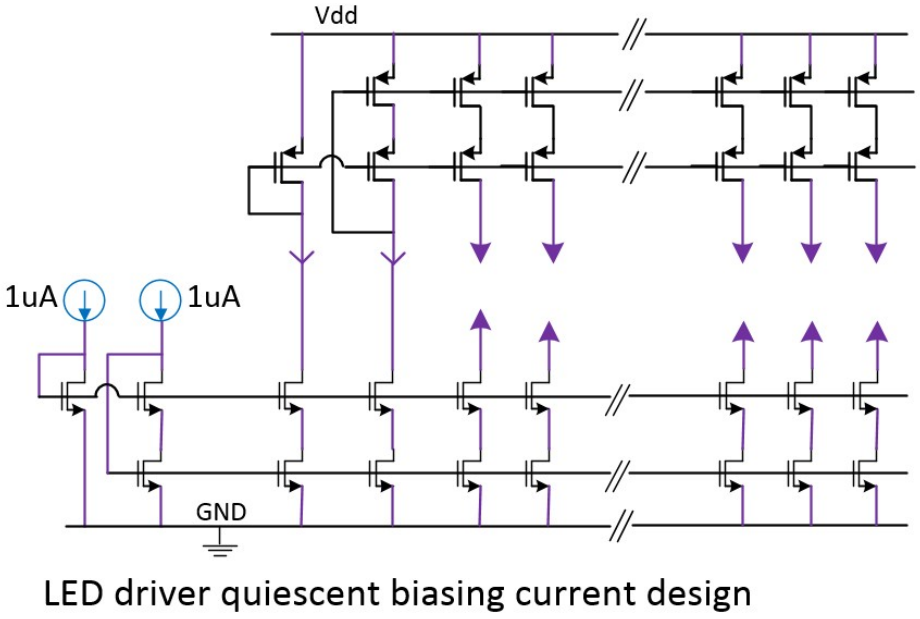


Figure 53. LED Driver Quiescent Biasing Current Design Schematic.

5.2.2.2 Driving Amplifier of the Constant Current LED Driver

The circuit ‘Amp’ shown in Figure 52 is the driving amplifier of the constant current LED driver. It is a novel design which has been filed as a patent application to US patent office [5-3]. The entire circuit is shown in Figure 54.

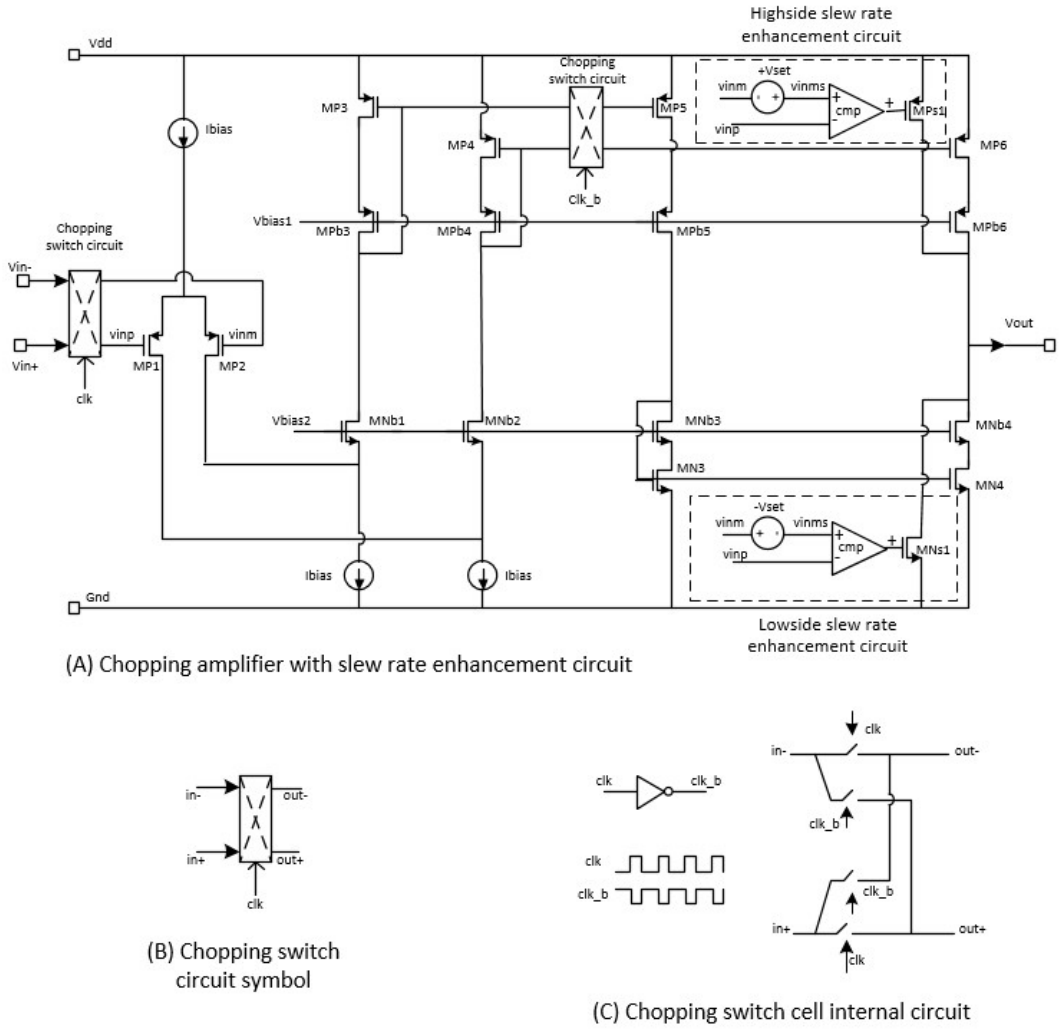


Figure 54. Chopping Amplifier with Slew-Rate Enhancement Design.

The major innovations of this design are

1) Its basic structure is a folded cascade input stage with a current string rail-to-rail output stage.
2) Novel slew rate enhancement circuits are added for both the high side and the low side of the output stage. It greatly increases the circuit speed without impairing the system stability. The detailed slew rate enhancement circuits are be implemented by either 1) detecting the input currents on the two input MOSFETs, or 2) directly detecting the

differential input voltage using an additional differential pair. In this design, the first detection approach is employed due to its circuit simplicity.

3) In addition, a chopping technique is used to reduce the input offset of the whole closed loop system.

Figure 55 shows the simulations of two typical responses of two different LED drivers to a PWM signal. The first response is the new LED driver using the proposed slew rate enhanced driving amplifier. The second is the same LED driver design without activating the slew rate enhancement circuit. Figure 55 clearly shows that the slew rate enhancement circuit dramatically increases the response speed while keeping the quiescent current at a low level. In the simulation result, the rising propagation delay is about 108 ns for the slew rate enhanced design, while it is 856 ns for the design without the slew rate enhancement. It is also worthy to notice that both designs consume roughly the same amount of quiescent current. In summary, the slew rate enhanced design can greatly increase the driving speed with negligible increase of quiescent current consumption.

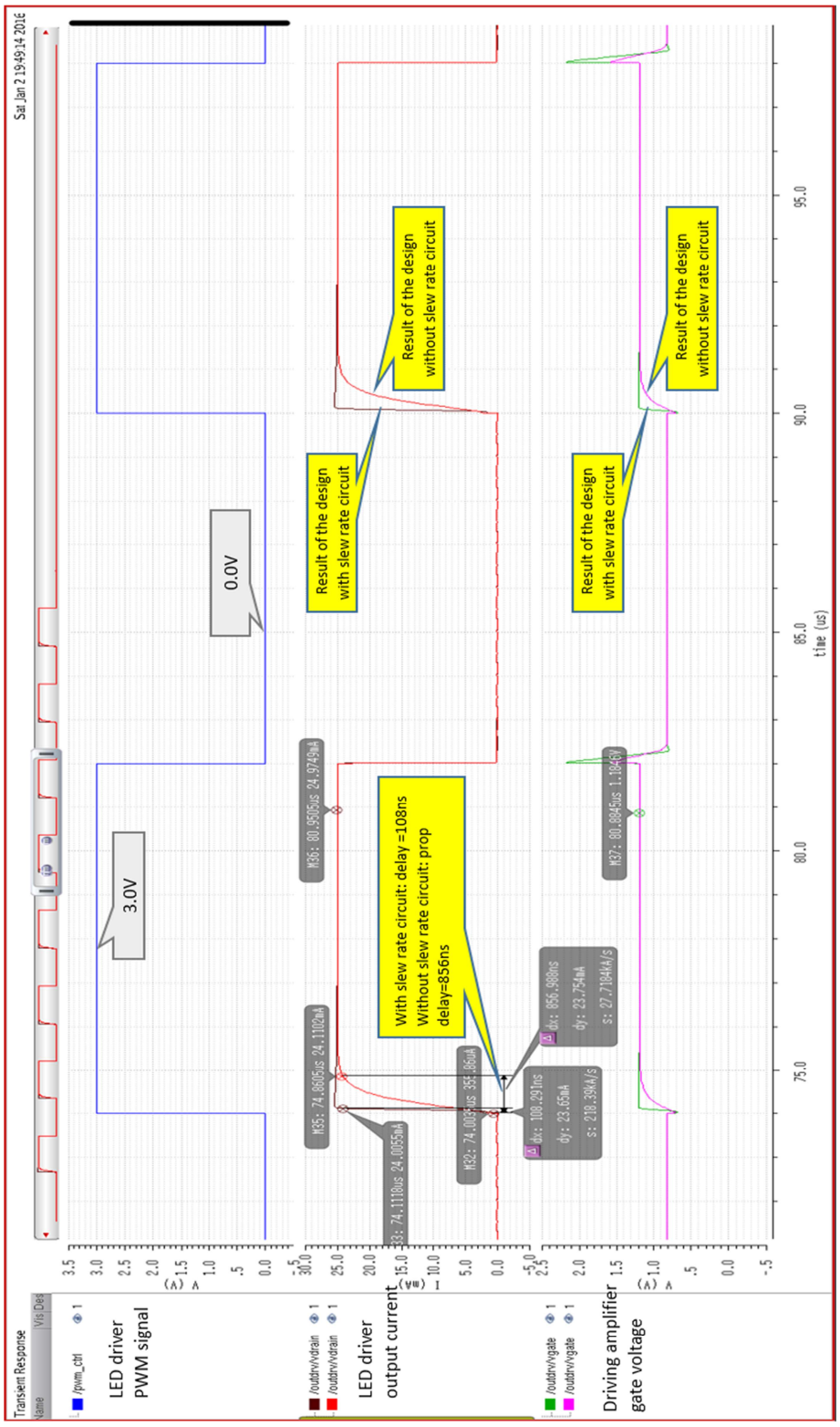


Figure 55. Transient Responses of the LED Driver with The Slew Rate Enhancement Circuit Versus without It.

5.2.2.3 Resistor DAC

This is a resistor-based digital to analog converter (DAC) to adjust the LED driver output current. It is shown as ‘R_DAC’ in Figure 52. This resistor DAC is used to change the LED output current by either DAC logic input signals or by PWM duty logic input signals. The detailed design circuit is shown in Figure 56.

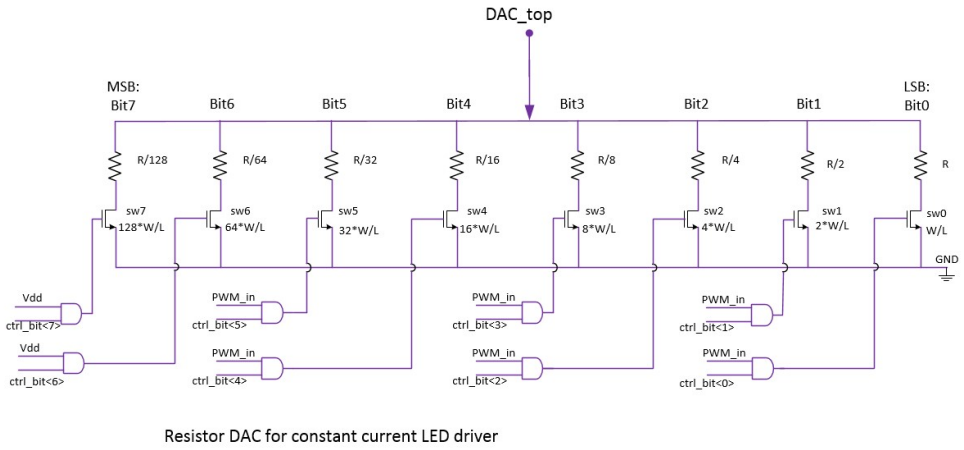


Figure 56. Schematic of Resistor DAC for The Constant Current LED Driver.

5.2.2.4 Feedback Loop Multiplex Switch

The feedback loop 2-1 multiplex switch circuit is shown as ‘SW’ in Figure 52. In the feedback loop of the LED driver, the cell ‘SW’ is used to switch the feedback input signal from either the main current leg or the auxiliary current leg. ‘SW’ is implemented as a simple NMOS based analog 2-to-1 multiplex. The circuit diagram is shown in Figure 57.

When the PWM signal is ‘on’, ‘SW’ connects the main LED current leg to the feedback input node of the amplifier ‘Amp’. When the PWM signal is ‘off’, ‘SW’ connects the auxiliary current leg to the feedback input of ‘Amp’.

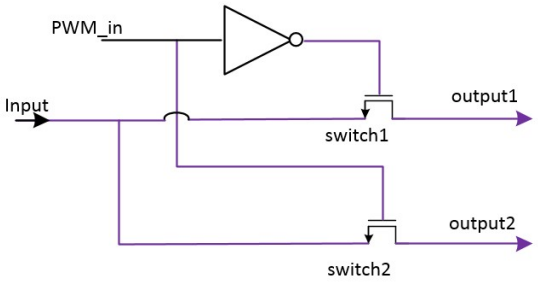


Figure 57. 2-to-1 Multiplex Switch for Feedback Signal Selection.

5.2.3 Top Level of The Six Constant Current LED Driver in Parallel

The top level schematic of the six LED drivers is shown in Figure 58. This is the real top level schematic in the design, which is used for all the top level simulations. Each driver has all the associated signals connected.

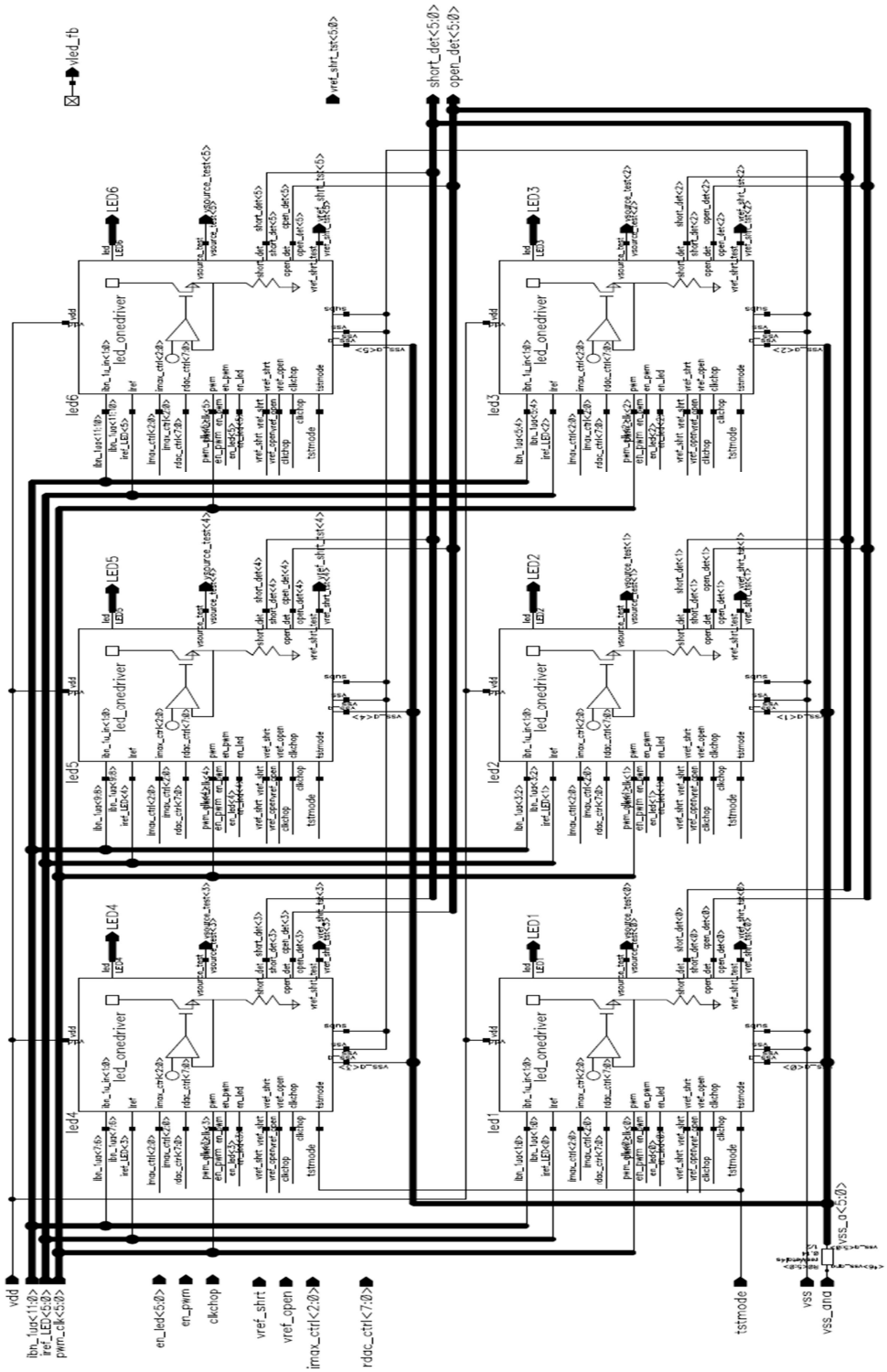


Figure 58. Top Level Schematic of The Total 6 Constant Current LED Drivers.

Figure 59 shows the transient simulation result of one of the LED drivers. It is a simulation result over process corners, temperature and voltage range of 2.5-5.5 V. The graph shows at the disable signal ‘pd_led’ = ‘low’, the LED driver responds the PWM input signal by toggling its output currents. Over all the corners, it can be noticed that the turn-on and turn-off transitions are still kept as fast as expected.

Notice that there is a little overshoot when the LED output current is immediately turned on. It is intentionally designed to keep the turn-on transition fast (at roughly 100 ns) by increasing the maximum output current of the slew rate enhancement circuit. In fact, this adjustment capability to change the transition speed is also an additional advantage of utilizing the slew rate circuit.

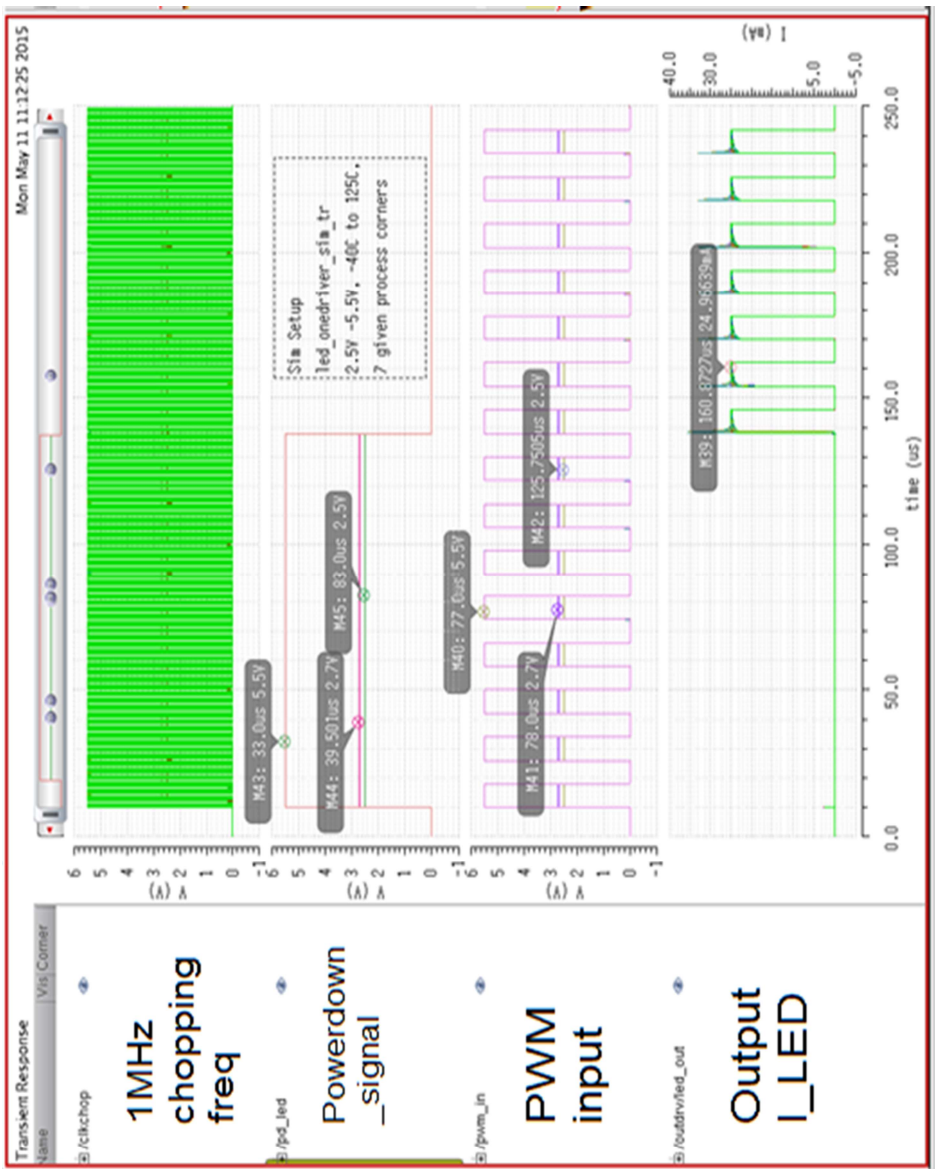


Figure 59. One Complete LED Driver's Transient Simulation Result Over PVT Corners.

5.2.4 The Minimum Voltage Selection Design

The 'I_LED drivers minimum voltage selector' shown in Figure 47 is a feedback voltage selection cell which chooses the minimum of the 6 LED strings cathode voltages and then sends it to the feedback input of the boost regulator's gm amplifier. The final circuit design is shown in Figure 60. In the final design, the major changes are: 1) the circuit enable signal 'EN' and its enable logic are

added; and 2) the diodes D1, D2, … and D6 are added to clamp the gate voltages of MP1, MP2, … and MP6, respectively.

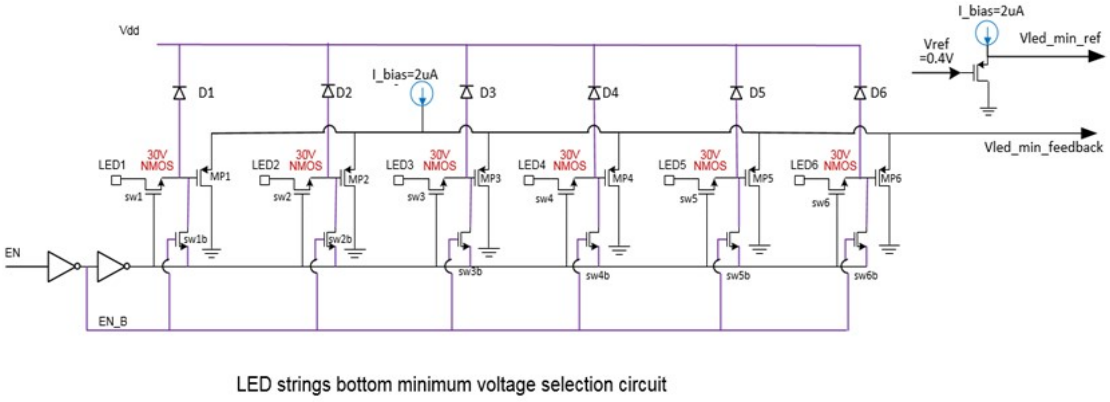


Figure 60. LED Strings Bottom Minimum Voltage Selection Circuit.

5.3 Design of The Proposed Boost Regulator System And Circuit

5.3.1 The Boost Regulator Structure

The final designed boost regulator control system architecture is shown in the shaded area of Figure 61. In this architecture, all the basic blocks of a peak-current PWM mode boost regulator are shown. In the following subsection, all these major blocks will be described.

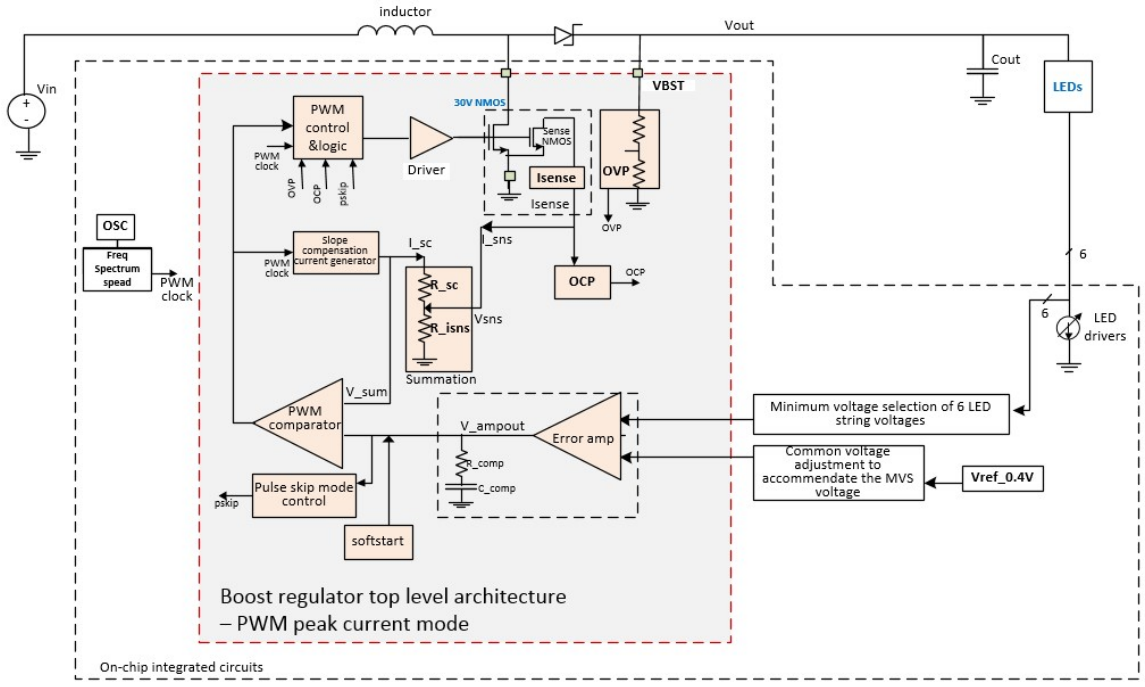


Figure 61. Boost Regulator Top Level System Architecture.

5.3.2 Error Amplifier 'Error amp'

Figure 62 shows the error amplifier 'Error amp' structure with its compensation network (consisting of R_comp, C_comp and C_highfreq). The compensation network is for the system stability of the boost regulator feedback loop. The amplifier is based on the folded cascode structure. A 'slew rate enhancement control' circuit is added to both the high output side and the low output side of the amplifier output stage. These slew rate enhancement circuits help to speed up the boost regulator transient response speed. Overall, the structure of this slew rate enhanced amplifier is a novel and original design for a boost regulator design by the dissertation author.

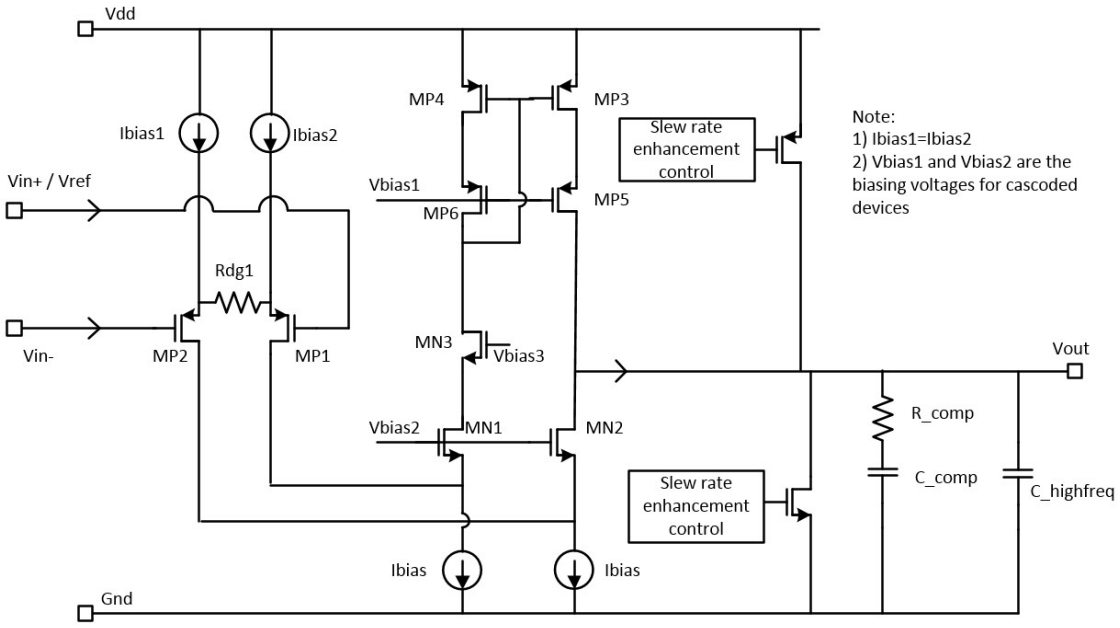


Figure 62. Boost Regulator Error Amplifier with Its Overall System Compensation Network.

5.3.3 Current Sensing Circuit 'Isense'

The basic structure and operational principle have been explained in Section 4.3.3.3. The new additions are those cascoded PMOS devices (MP2c, MP3c) and their associated circuits (Ib1, Ib2, MNb1, and MPb1) to keep the output current accurate and well matched. The final design is shown in Figure 63.

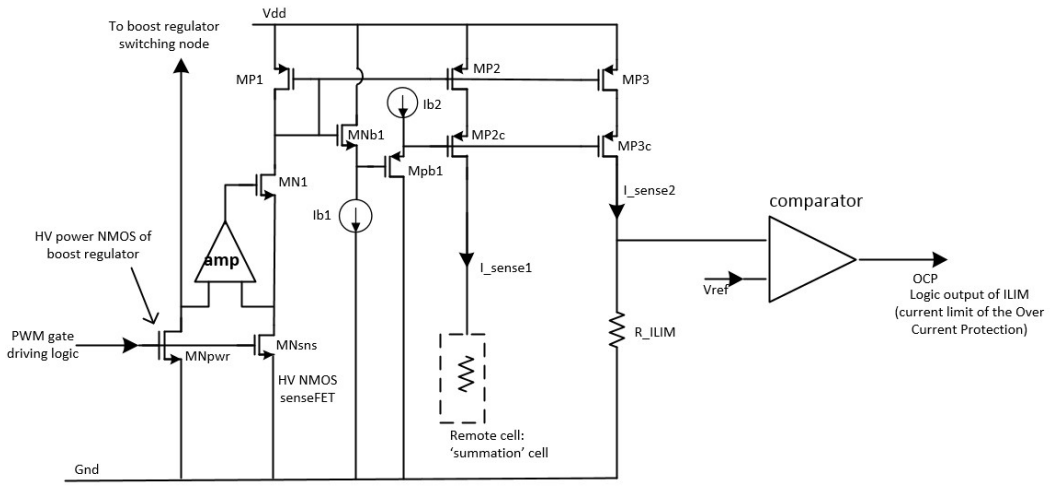


Figure 63. Current Sense Circuit Design.

5.3.4 Over Voltage Protection Cell 'OVP'

The over voltage protection design 'OVP', shown in Figure 64, uses a resistor divider (R1+Rhys, R2) to detect the boost regulator output voltage. The detected voltage is then compared with a fixed reference voltage. When the detected voltage is higher, then an over-voltage logic output signal is sent to the regulator control logic to stop boost regulator switching. Hysteresis is added in the design to prevent any ringing during the detection process. The idea is to use the logic output signal to turn on/off SW1 to generate an input voltage difference as a hysteresis voltage.

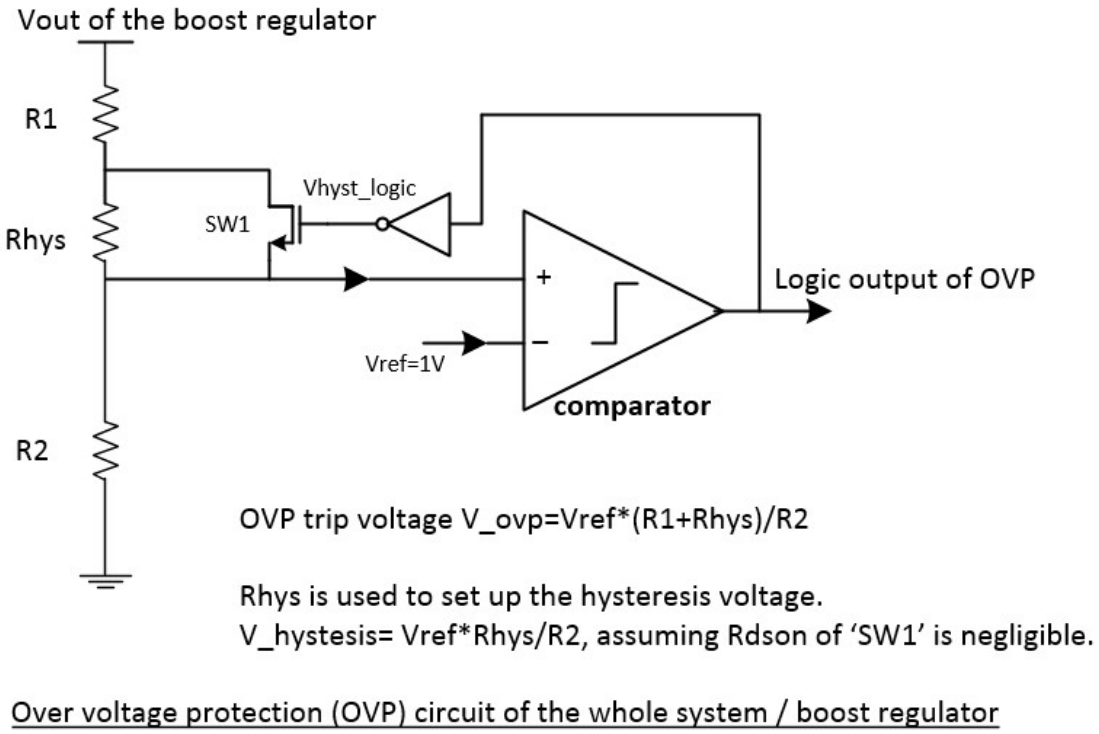


Figure 64. Over Voltage Protection Circuit Design Structure.

5.3.5 Over Current Protection Cell 'OCP'

The circuit design is shown in the dashed line square in Figure 65. This over current protection cell 'OCP' is closely connected to the current sense circuit 'Isense' since 'OCP' uses the sensed output current 'I_sense2' from the 'Isense' cell. In the OCP cell, the sensed output current, which actually represents the inductor current, runs through the resistor 'R_ILIM' to set up a sensed voltage. The sensed voltage is compared with a fixed reference voltage 'Vref' which represents a targeted current limit. When the sensed voltage is higher than the reference voltage 'Vref', which means the inductor current is over the preset current limit, an over-current logic output signal is sent to the boost regulator control system to force the power NMOS 'MNpwr' to turn off if 'MNpwr' is still on.

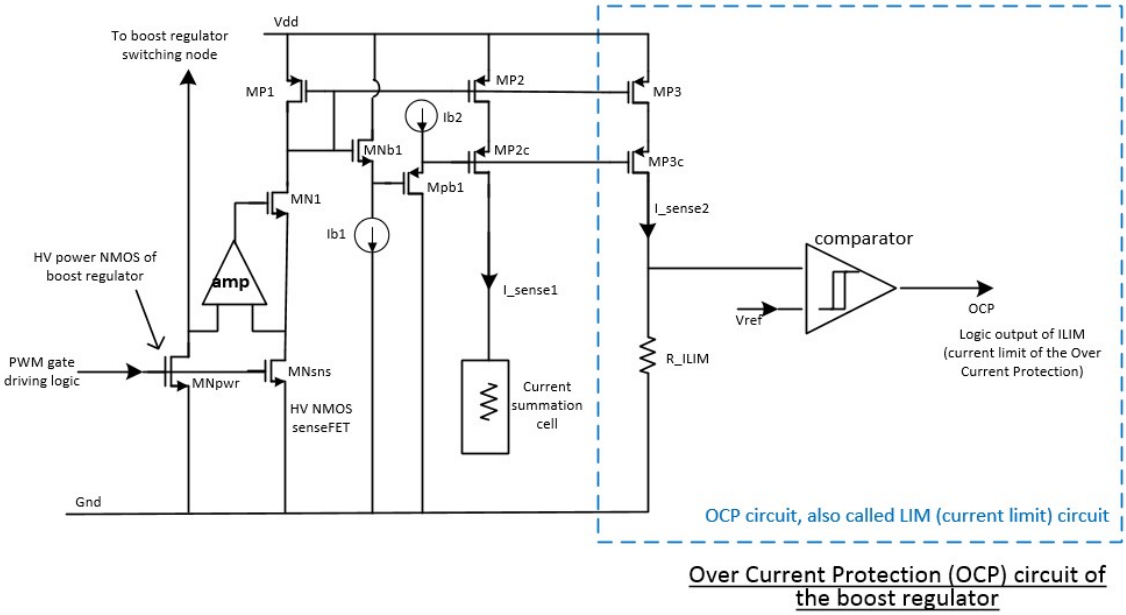


Figure 65. Over Current Protection Circuit Design Structure.

5.3.6 PWM Comparator

The final design of the ‘PWM comparator’ is the same as shown in Section 4.3.3.8. This is a two-stage differential amplifier-structure-based comparator as shown in Figure 66. The first stage is used to accommodate input common mode voltage range.

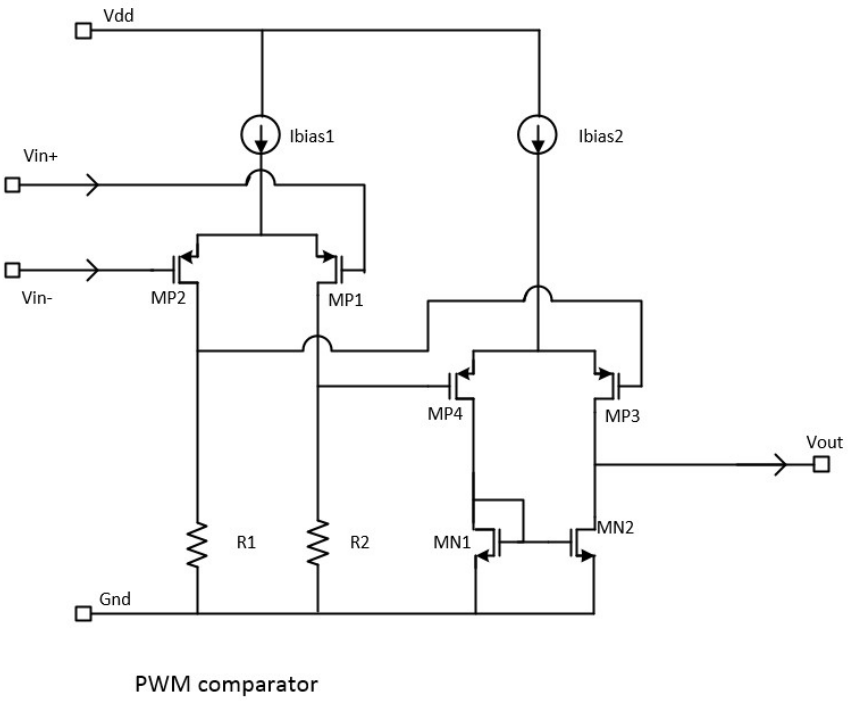


Figure 66. PWM Comparator Circuit Design.

5.3.7 Slope Compensation Circuit

The basic circuit is explained in Section 4.3.3.6. The detailed design circuit is shown in Figure 67. This circuit includes the 'slope compensation current generator' cell and the 'summation' cell. The 'slope compensation current generator' is used to produce a current 'I_slope' that is proportional to time.

$$\mathrm{I\_slope} = \frac{\mathrm{Ibias \cdot Cslope}}{\mathrm{Rslope}} \cdot \mathrm{t} \qquad (11)$$

Where, 'Ibias' is a constant DC biasing current for 'I_slope' generation; 'Cslope' is the capacitor; and 'Rslope' is the resistor, as shown in Figure 67. 't' in the equation is the time duration for 'Ibias' to charge the capacitor 'Cslope'.

The 'summation' cell performs a current summation functions as follows.

$$\mathrm{V\_sum} = \mathrm{R\_isns} \cdot \mathrm{I\_sense} + (\mathrm{R_{sc}} + \mathrm{Risns}) \cdot \mathrm{I\_slope} \qquad (12)$$

Where, ‘V_sum’ is the summation voltage; ‘R_isns’ is a resistor for ‘I_sense’; and ‘R_sc’ is a resistor for slope compensation current ‘I_slope’, as shown in Figure 67.

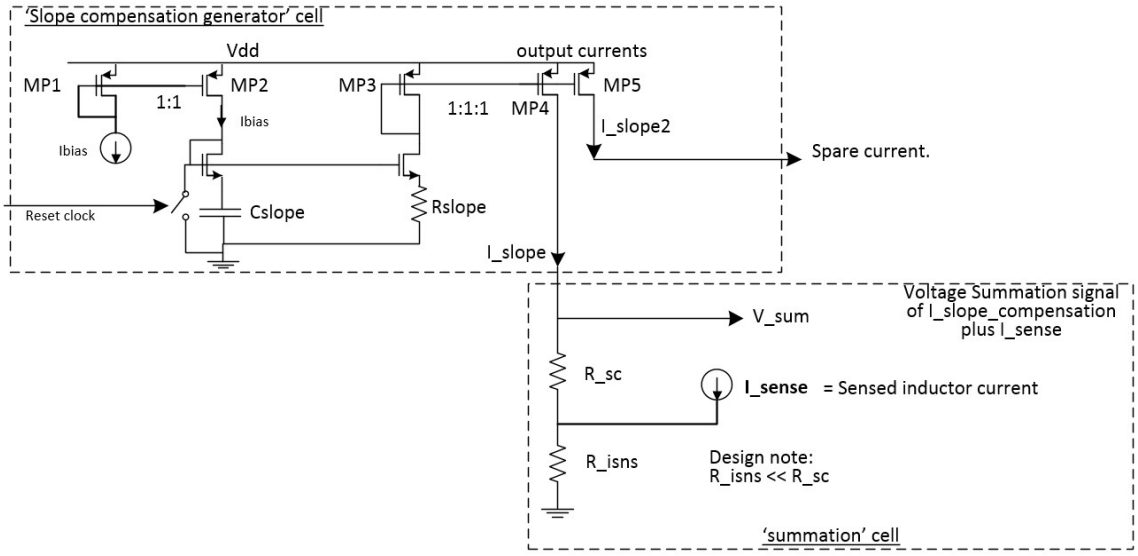


Figure 67. Slope Compensation and Summation Circuit Design Structure.

5.3.8 Pulse Skip Mode Control

The ‘pulse skip mode control’ design, shown in Figure 68, utilizes the idea that the boost regulator error amplifier’s output voltage represents the actual peak inductor current plus the slope compensation signal in our designed PWM peak current mode switching regulator structure. Therefore, the error amplifier output voltage ‘V_ampout’ is measured against a fixed reference voltage ‘Vref_pskip’ via a comparator. During normal boost regulator operation, at low switching duty cycle, the voltage percentage from the slope compensation in ‘V_ampout’ is relatively small and can be roughly neglected. Therefore, ‘V_ampout’ grossly represents the peak current value of the inductor current at this condition.

The fixed reference voltage ‘Vref_pskip’ sets up the triggering value of the inductor current to enter the pulse skip mode. When ‘V_ampout’ is below ‘Vref_pskip’ voltage, the comparator output

is triggered and this signal goes to the control logic to force the boost regulator to skip a whole clock cycle (it is called a pulse skip). When the 'V_ampout' is above 'Vref_pskip', the comparator is not triggered, and the boost regulator runs in its normal operation.

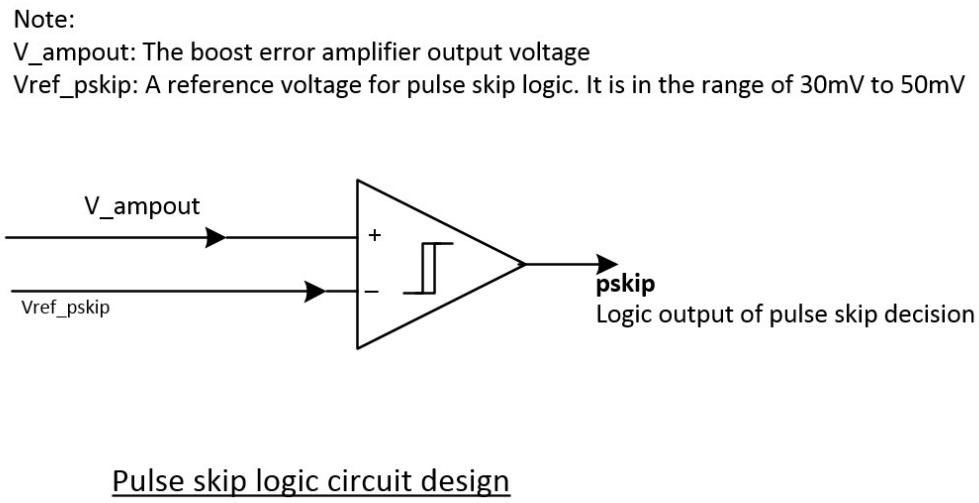


Figure 68. Pulse Skip Mode Circuit Design Structure.

5.3.9 Soft-Start

This specific cell is not fully implemented in this design since the boost regulator normal startup time is slow enough and can meet our system startup design testing purpose. So, no design description is shown here. In real industrial and commercial applications, this feature is generally required.

5.4 Top Level Simulations of The Overall System

All the designs are finally integrated together into an overall system consisting of both the LED driver system and the boost regulator. The following top level simulations are performed to verify its performance.

5.4.1 Normal LED Current Step Up/Down Simulation without PWM Function

This simulation is an overall system sim without enabling the LED current PWM toggling function. In this simulation, the PWM logic is set to not toggle the LED driver output currents; only the DAC digital logic input signals are allowed to activate and change the LED output currents. The purpose of this simulation is to examine the normal DAC function and its output values.

The simulation result is shown in Figure 69. It can be observed that, when the DAC logic input signals toggle, the LED current magnitudes double their values at each step. The steps are shown to be correctly defined by the DAC logic input signals. Then the LED currents reduce their values by half at each step, as defined in the DAC logic input signals. It also importantly shows that the LED output currents can stay at one-fourth (a quarter) of their full scale during the PWM input logic toggling period as expected.

Note that there is some small accuracy variation at the quarter of the full LED current level in the simulation result. The full scale current value shown in the simulation plot is 24.6 mA, which gives a calculated quarter scale value of 6.15 mA. However, the quarter scale value shown in the simulation is only 6.001 mA. This is a 2.5% error. It is probably due mainly to the mismatch of some resistors and MOSFETs between the reference resistor leg and the DAC resistor leg. It can be improved by future careful design and matching improvement layout techniques. On the other hand, the accuracy requirement at lower LED currents can be loose and it is not even specified in most of the industrial and commercial applications, mainly due to the difficult matching accuracy at lower currents.

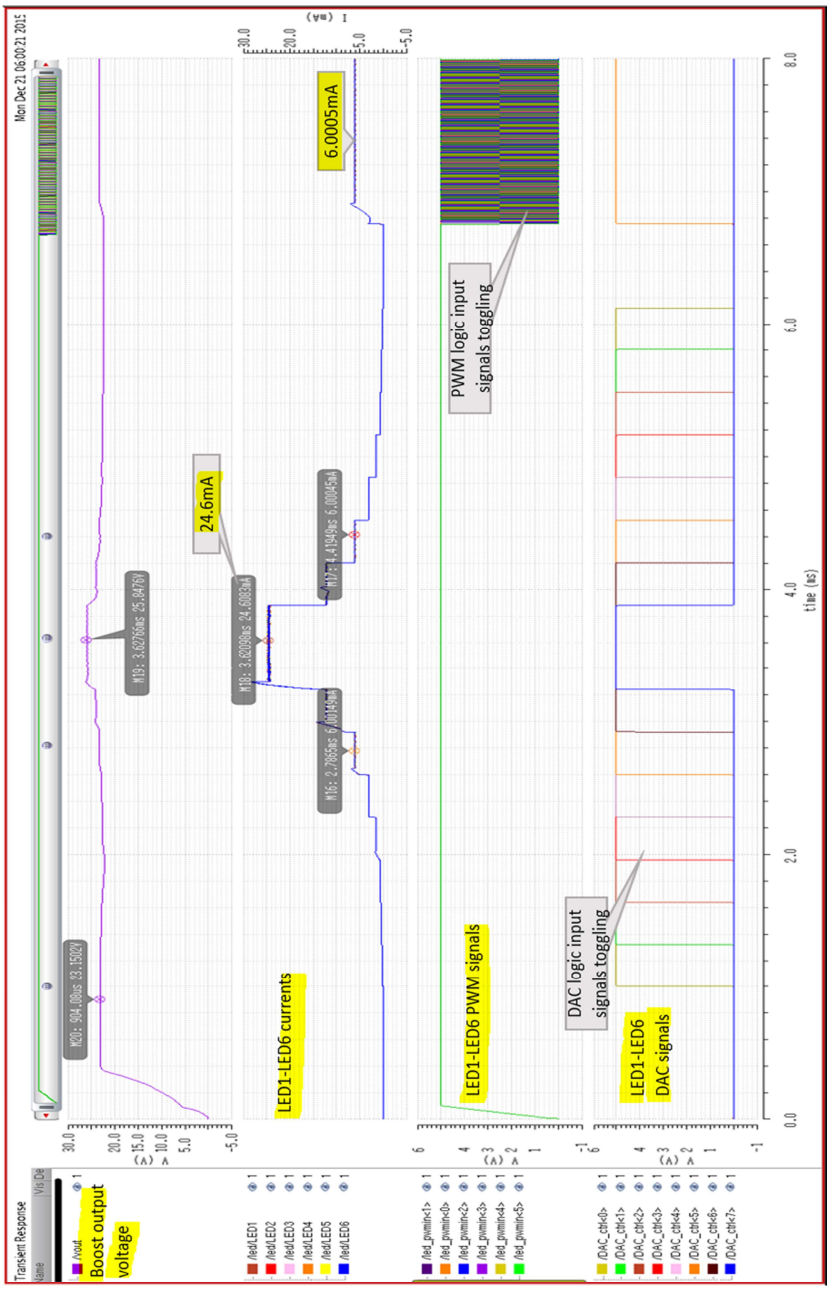


Figure 69. Top Level Simulation Result without Enabling LED Current PWM Toggling.

5.4.2 Normal LED Current Step Up/Down Simulation with LED Current PWM Toggling

In contrast to the previous simulation, the simulation shown in Figure 70 uses all the same LED output current steps, and in addition, the LED output currents are toggled by following the LED PWM logic input signals.

It can be observed that, when the DAC logic input signals toggle, the LED currents step up by doubling themselves; then the LED currents step down by cutting their values by half. This is the same result as in the previous simulation in Figure 69.

Additionally, it can also be observed that the LED output currents toggle between 0 mA and one-fourth of the full scale during the toggling period of the PWM logic input signals.

The above results confirm the originally-proposed hybrid LED current control scheme is achieved. The hybrid LED current adjustment scheme is: when a LED current is above its quarter scale, the LED current is adjusted linearly by using the DAC logic input signals to control it. When it is below its quarter scale, the LED output current is adjusted by toggling the PWM logic input signal, where the average LED output current is controlled by the duty cycle of the PWM signal.

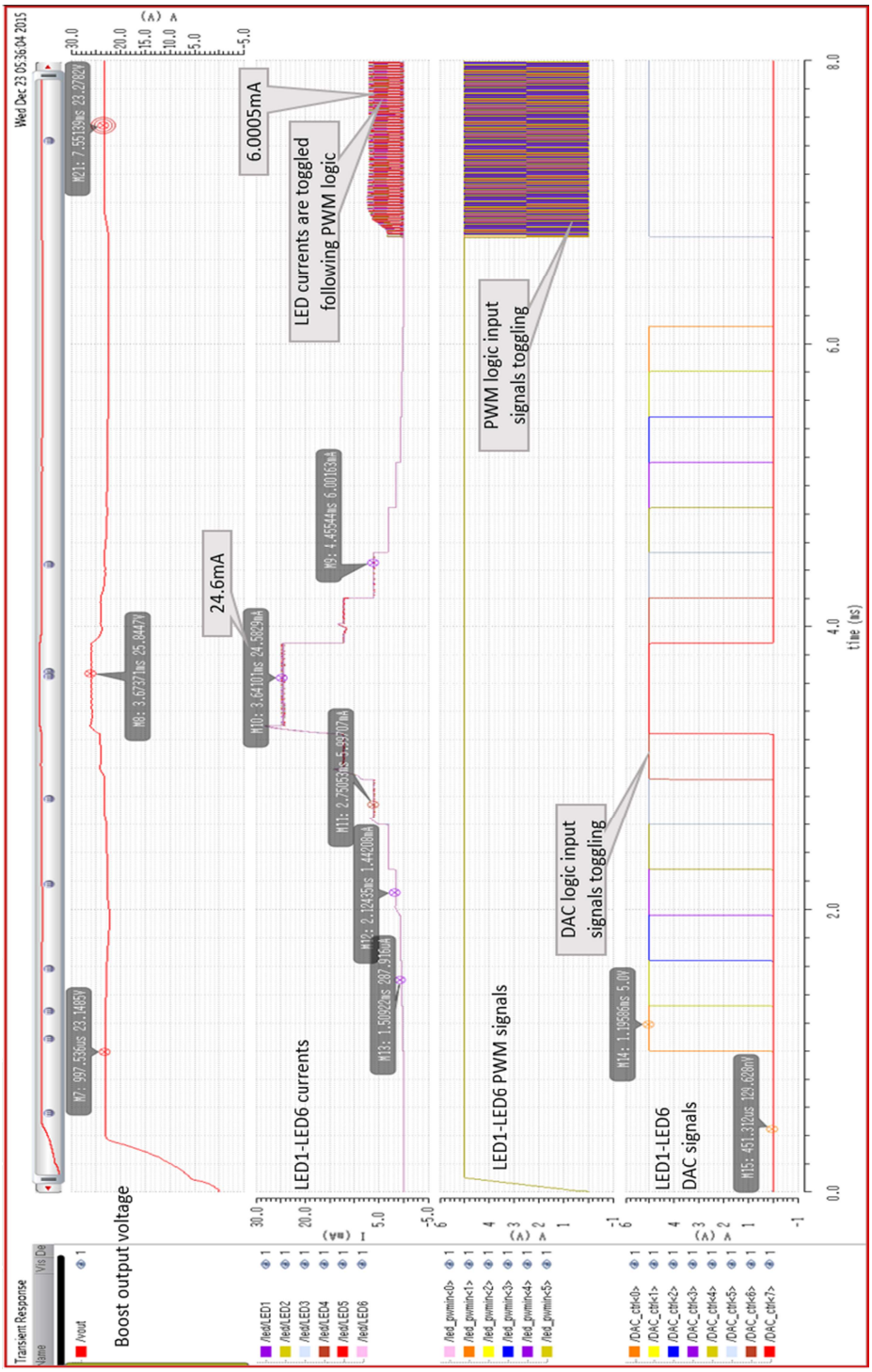


Figure 70. Top Level Simulation Result with LED Current PWM Toggling.

Figure 71 and Figure 72 are the zoom-in plots of Figure 70. Figure 71 shows the detailed LED PWM input signals toggling. Figure 72 shows that the corresponding LED currents are toggled following the LED PWM input signals.

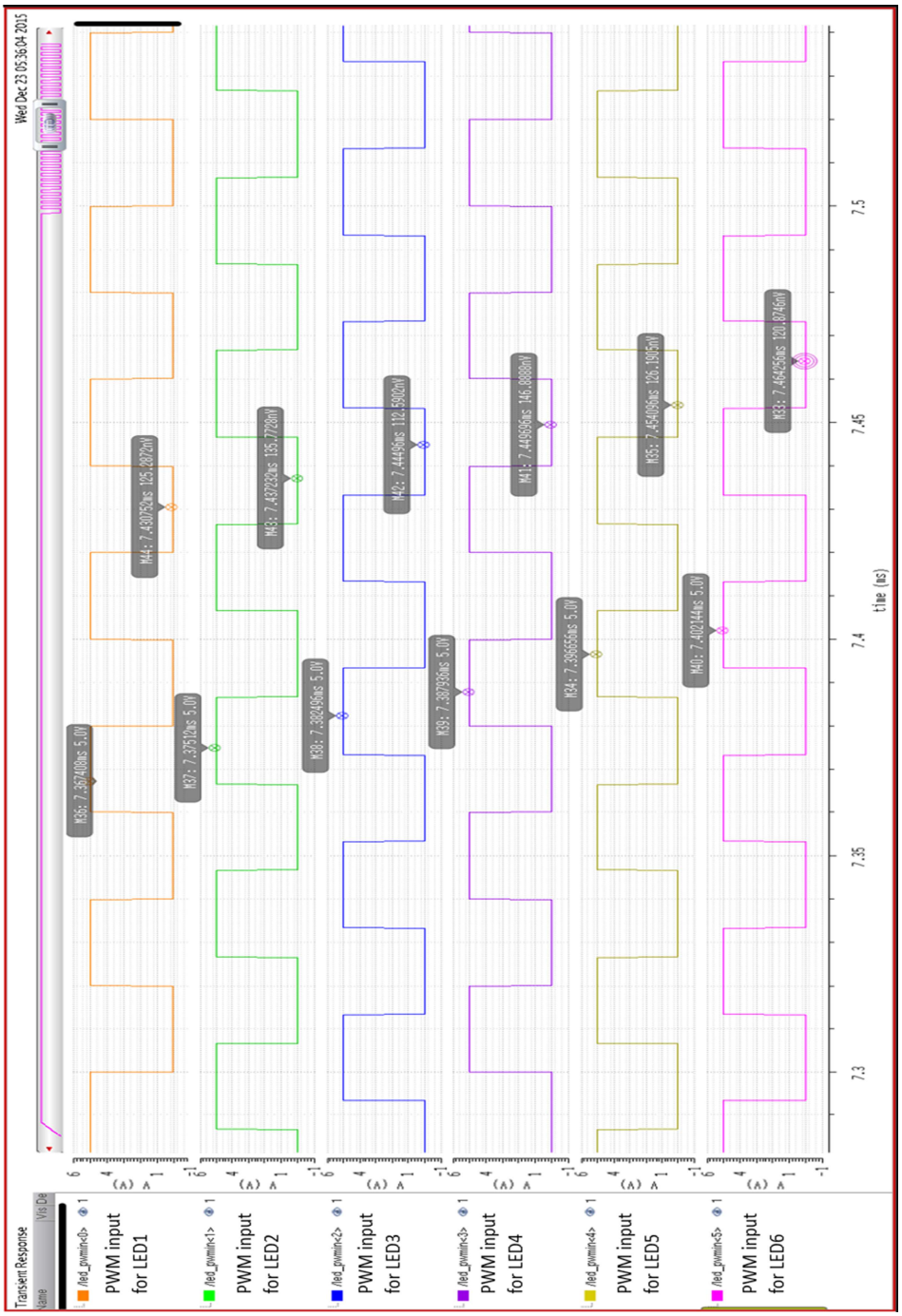


Figure 71. PWM Input Signals Zoom-In Plot of The Top Level Simulation Result.

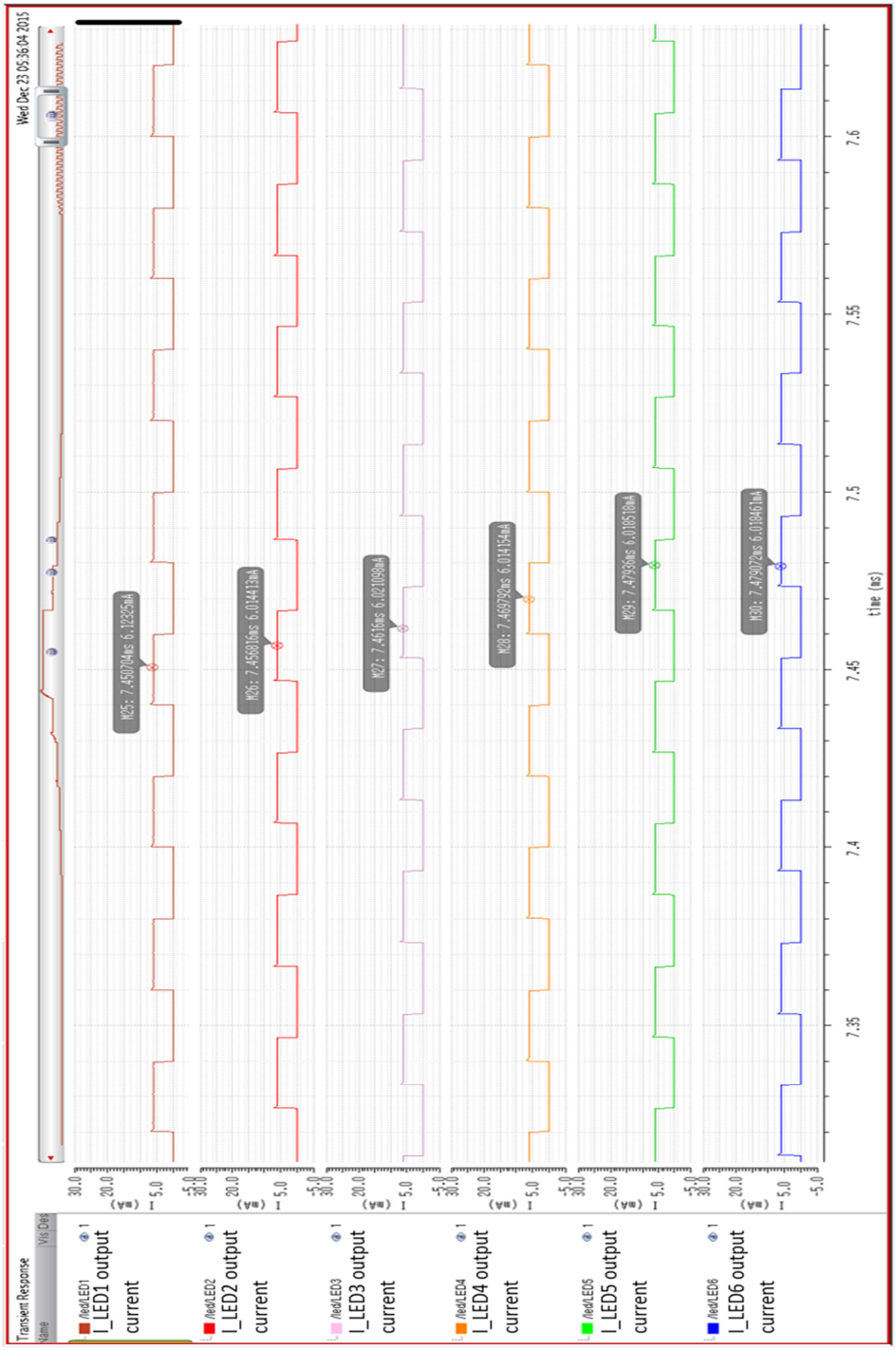


Figure 72. LED Currents Toggling Zoom-In Plot of The Top Level Simulation Result.

5.4.3 Top Level Over Voltage Protection and Over Current Protection Simulation

The OCP (over current protection) and OVP (over voltage protection) top level simulations are shown in Figure 73. As shown in the simulation result, the OCP is triggered during the periods of both roughly 3.5 ms – 3.7 ms and roughly 4.5 ms – 4.7 ms. OVP is triggered at the time period roughly from 4.4 ms to 4.7 ms. It can be concluded that 1) OCP output logic is successfully triggered when the output loading current is intentionally increased to cause the inductor current reach the OCP trigger level; and 2) OVP is successfully triggered when the number of LEDs in one LED string is increased intentionally to cause the increase of the boost regulator output voltage which eventually goes above the OVP trigger voltage.

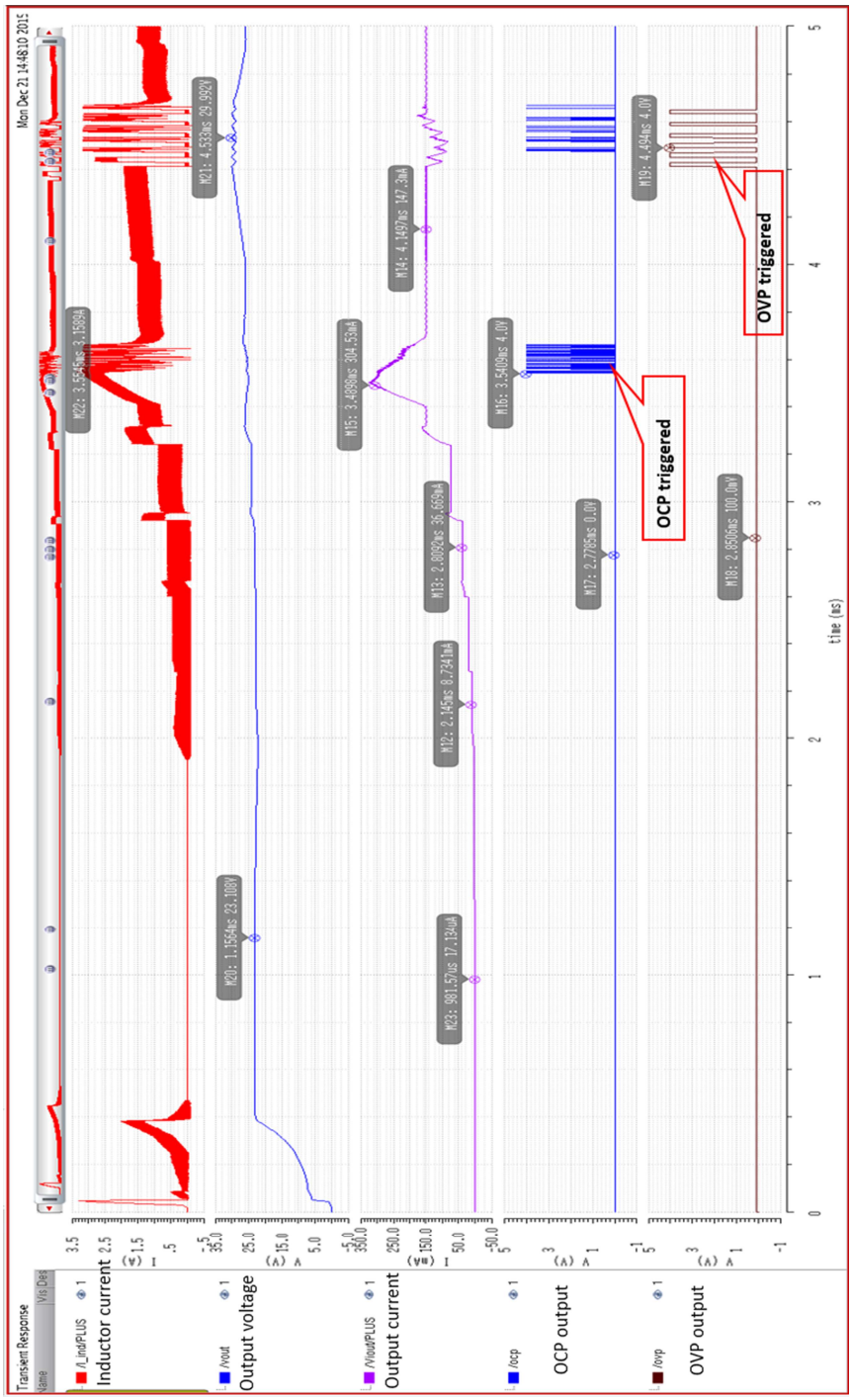


Figure 73. Top Level Simulations at OCP and OVP Conditions.

5.5 Performance Comparison of This LED Driver System Design versus A Previous Design

5.5.1 Brief Introduction of a Previous LED Driver System Design and Performance

There is a previous design of an LED driver chip, which is a pure 16 channel constant current LED driver chip without the boost regulator integrated on chip. The design was done by different designers and it was the predecessor of the design in this dissertation. The function diagram is shown in Figure 74.

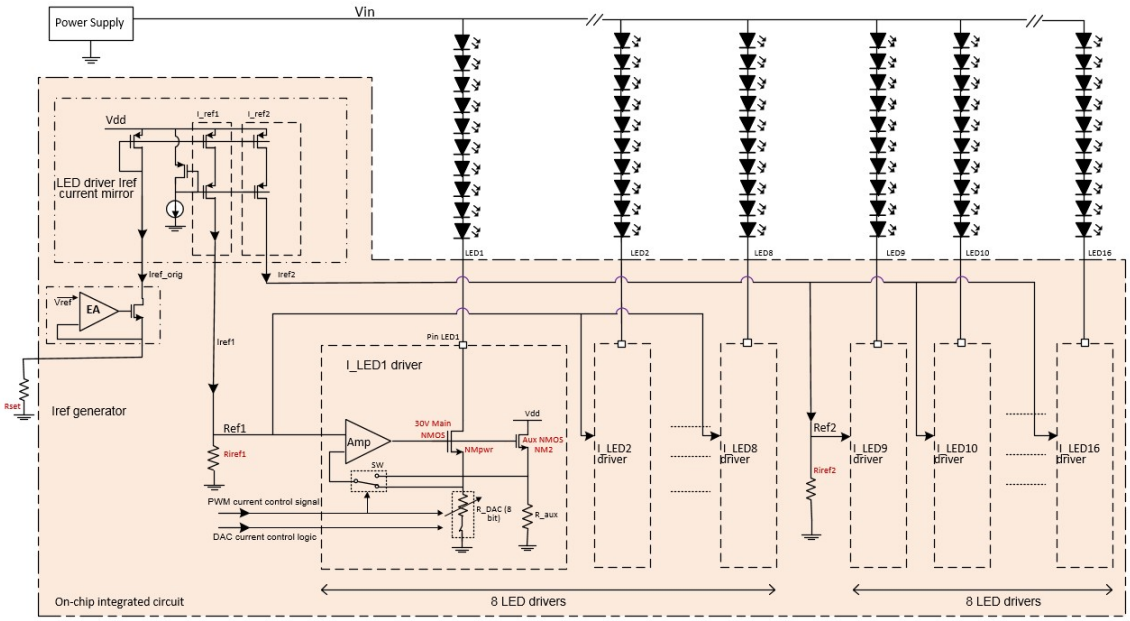


Figure 74. A Previous Design – A 16 Channel Constant Current LED Driver System Architecture.

Each LED driver's maximum current is 57 mA. The chip power supply is Vdd =3 V to 5.5 V. The voltage on its LED current output pin is a maximum of 20 V, while the new design in this dissertation can sustain 28 V. As shown, the predecessor design uses the conventional cascoded current mirror structure to generate only two reference currents -- Iref1 and Iref2. Each reference current is used to support eight constant current LED drivers.

The driving amplifier 'Amp' in the predecessor design is a conventional operational amplifier without any slew rate enhancement circuit. It utilizes a conventional operational amplifier design

structure – a differential input stage followed with current mirrors which drive a rail-to-rail output stage. The quiescent current of each amplifier is designed to consume 270 uA in order to turn on/off a LED output current fast in response to a PWM logic input signal. In comparison, the new design consumes only 56 uA in its amplifier while achieving roughly 30% faster turn-on/off speed. In addition, since there is no chopping technique used in the predecessor design, the input offset of the amplifier directly translates itself into roughly 3%~4% mismatch errors of the LED output currents, which are considered big and undesired errors.

The layout of this predecessor design is shown in Figure 75. It is implemented on a 0.14 um HV 5 V CMOS process. The die size is 1.56 mm x 2.12 mm = 3.3 mm^2.

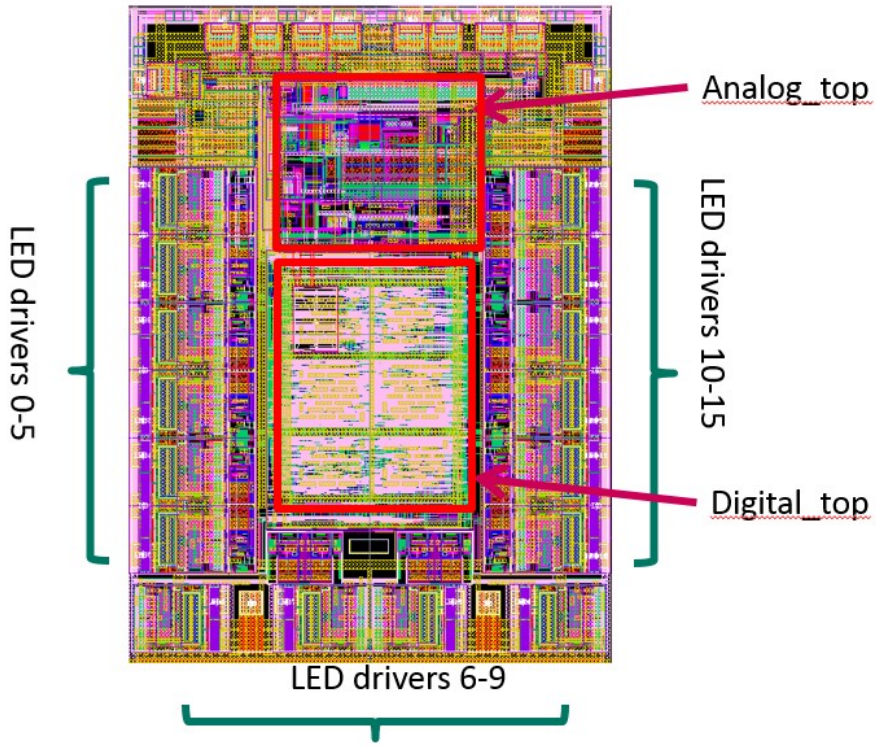


Figure 75. Layout of The Predecessor Design.

5.5.2 Simulation Result of The Current Accuracy and The Channel-To-Channel Mismatch of The Proposed Design

Each circuit segment of the overall LED driver system has been simulated individually using the Monte Carlo statistical simulation tool in Cadence simulation environment [5-4]. The results are then summarized to determine the final LED current absolute value accuracy and channel-to-channel mismatch based on the Gaussian probability distribution calculation (root-mean-square approach). The result is shown in Table 4. This result is intentionally over-calculated by adding some design margin to cover those potentially unexpected variations and errors which do not readily show up in the simulations. The detailed calculation procedure is not shown here due to some proprietary data related to the company's process.

Table 4. Simulation Result of The LED Driver Current Accuracy And Channel-to-Channel Mismatch

Items	Result before mechanical stress	Result after given mechanical stress	Notes
LED output current accuracy	**2.95% (Note 1)**	**3.88% (Note 2)**	Note 1: Value at 6 sigma, which is the RMS of all the individual variations at 6 sigma. Note 2: Value at 6 sigma plus the given mechanical stress.
LED output current channel-to-channel Mismatch	**1.46% (Note 1)**	**2.02% (Note 2)**	

Note that the mechanical stress mentioned in Table 4 mainly refers to the stress on a die introduced by the chip packaging process. This mechanical stress is also called packaging stress. This stress is considered as a major impact on electronic performance of the integrated circuits on a die. Another mechanical stress introduced by soldering a chip package on an electronic board is not considered in this dissertation because it has much less impact than the packaging stress.

5.5.3 Summary of the Performance Comparison

The LED driver performance between the predecessor design and the proposed design is summarized here.

Table 5. Summary of The Performance Comparison

Items	Predecessor Design		This Design
	Simulation Result	Silicon Result	Simulation Result
Quiescent power consumption per one LED driver at Vdd=5V	1500 uW	~1500 uW	300 uW
Quiescent current of each LED driver	**300** uA	~300 uA	**60** uA
Maximum current of one LED driver	57 mA	57 mA	25 mA
LED driver output current absolute value accuracy over process, voltage and temperature at 6 sigma	6.44% (with 6% bandgap trim) – extrapolated result	6.7% (with 6% bandgap trim) – extrapolated result	3.88% (with reference voltage trim)
LED driver current matching accuracy over process, voltage and temperature at 6 sigma	5.1%	6%	2.03%
LED current PWM response time – rising time	133 ns rising typical	130 ns rising typical	109 ns rising typical
LED current PWM response time – falling time	78 ns falling typical	70 ns falling typical	9 ns falling typical
Operating Vdd voltage	3 V to 5.5 V	3 V to 5.5 V	2.7 V to 5.5 V

From the summary in Table 5, the following conclusions can be obtained:

1) The predecessor design draws 4 times more quiescent current than the proposed design of this dissertation, while the rising time to PWM logic in the predecessor design has is 130 ns versus 109 ns in the proposed design. It indicates that the proposed design has a roughly 30% speed improvement while only having one-fifth the quiescent power consumption.
2) The LED output current accuracy has improved from 6.7% to 3.88% at 6 sigma range.

3) The LED output current channel-to-channel mismatching accuracy has improved from 6% to 2.03% at 6 sigma range. This specification is the key item for any backlighting LED driver design.

6 SUMMARY AND FUTURE WORK

6.1 Performance Summary

A constant-current-LED-drivers system with high LED current accuracy and with very low channel-to-channel mismatch is designed. Few LED driver designs have achieved such a high accuracy (around 4% target) and low mismatch (around 2% target) so far in today's academic and commercial research area [2-17], [5-5]. One example is the product ISL97692 [5-5], which claims to achieve maximum 3% LED output current accuracy and maximum 2.5% channel-to-channel current mismatch accuracy. This PhD dissertation design achieves this target with some novel design ideas. The new ideas include 1) a novel LED driver system structure including dynamic current mirror, 2) fast and accurate LED current driver circuit; and 3) distributed reference current for each LED driver.

In addition, a peak current mode PWM boost regulator is added to the system as the front-end power supply portion of the whole LED driver system. It is designed with some original ideas also, including 1) a novel gm error amplifier for the boost regulator; and 2) a novel clock spectrum spreading circuit design which has been filed in a patent application by the author and his colleague.

The final simulation results and performance comparison with an old design are presented in regards to the LED driver system. The LED output current accuracy shows a 72% improvement from a maximum of 6.7% in the predecessor design to a maximum of 3.88% in this new design. The LED output current channel-to-channel current mismatch shows a 200% improvement from a maximum of 6% in the predecessor design to a maximum of 2.03% in this new design.

6.2 Patent Applications

The following related design structures have been filed with US Patent and Trademark Office (USPTO) as patent applications after review and approval by the high level technical committee of a very large semiconductor company. The patent applications are:

1. The entire LED driver system architecture [5-2], filed in September 2015. The invention is solely under the author's name.
2. The driving amplifier of the constant-current-output LED driver structure which has a fast and accurate performance [5-3], filed in December 2015. The invention is also solely under the author's name.
3. A clock spectrum spreading circuit [5-4]. It is filed by the author and a coworker in 2015. Since the circuit design is indirectly related to the essential LED driver and its front-end boost regulator design. It is not detailed in this dissertation.

6.3 Future Work

Future work of this research is to implement the whole design in silicon to further verify the conclusions in this dissertation. Other future efforts include:

1) More patent applications potentially can be filed. They include, but are not limited to, the novel design of the boost regulator error amplifier described in Section 5.3.2, and an updated version of the pulse skip mode control described in Section 5.3.8.
2) A silicon result is needed for further design result verification. Due to a product decision change of the company where author works, this design is not presently slated for tape-out in silicon. Therefore, a silicon result cannot be shown here.
3) Some more simulations can be performed to further verify the system in addition to the simulation results in Section 5.4.

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