Novel Rail Clamp Architectures and Their Systematic Design

by

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ABSTRACT

Rail clamp circuits are widely used for electrostatic discharge (ESD) protection in semiconductor products today. A step-by-step design procedure for the traditional RC and single-inverter-based rail clamp circuit and the design, simulation, implementation, and operation of two novel rail clamp circuits are described for use in the ESD protection of complementary metal-oxide-semiconductor (CMOS) circuits. The step-by-step design procedure for the traditional circuit is technology-node independent, can be fully automated, and aims to achieve a minimal area design that meets specified leakage and ESD specifications under all valid process, voltage, and temperature (PVT) conditions. The first novel rail clamp circuit presented employs a comparator inside the traditional circuit to reduce the value of the time constant needed. The second circuit uses a dynamic time constant approach in which the value of the time constant is dynamically adjusted after the clamp is triggered. Important metrics for the two new circuits such as ESD performance, latch-on immunity, clamp recovery time, supply noise immunity, fastest power-on time supported, and area are evaluated over an industry-standard PVT space using SPICE simulations and measurements on a fabricated 40 nm test chip.

DEDICATION

To my teachers

ACKNOWLEDGMENTS

As the PhD journey draws to a close, it is hard for me to believe that I am indeed seeing the proverbial light at the end of the tunnel. As with every other accomplishment, there are so many people behind-the-scenes who have played key roles knowingly or unknowingly in the completion of this thesis. Certainly, reflecting on the contributions of these fine individuals makes me realize that I am merely another instrument that has helped complete this work and I am far from the real 'doer'.

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CHAPTER 1

INTRODUCTION

Electrostatic discharge (ESD) refers to the phenomenon when there is sudden transfer of charge between two bodies. Almost all of us have experienced some flavor of electrostatic discharge in our daily lives. A ‘shock’ when touching a metal doorknob after walking across the carpet, or when touching a metal cart in a grocery store, seeing sparks flying out of clothes taken from a dryer etc. are all common experiences of electrostatic discharge. These electrostatic discharges occur over small distances. Another more intense form of electrostatic discharge that can occur over large distances is lightning. Most people often view electrostatic discharge as an annoyance and probably think they could do without electrostatic discharge! But like everything in nature there are several benefits to ESD as well. For example, it has been reported that the atmosphere is electrostatically cleaned of exhaust gases. Historically too, lightning played an important role in the discovery of electricity that has radically improved the quality of human life.

Objects can get charged due to either triboelectric charging or induction. Triboelectric charging results when two objects of opposite affinity rub against each other. Such a motion can result in both objects acquiring opposite charges that can discharge suddenly later when they come in contact with a good conductor with a discharge path to ground. In the case of semiconductor die, such an electrostatic discharge which results in transient current flowing through the die can damage the circuits in the die. The damage is usually seen as oxide or junction damage or metal melting. Clearly, damage of circuits is undesirable as this translates to low yield and low

profit for the business. To predict the effect of ESD on semiconductor circuits, various models have been proposed to model the ESD event.

ESD Models

There are three models for the ESD event used in the semiconductor industry today. They are the Human Body Model (HBM), Machine Model (MM), and the Charged Device Model (CDM).

Human Body Model (HBM)

The HBM models the charged human being discharging into the semiconductor die. The human is modelled as a 100 pF capacitor with 1500 Ω series resistance. The initial capacitor voltage models the charge on the human before discharge. A schematic of the model is shown in Figure 1. The standardized spec by the ESD Association is available in [1].

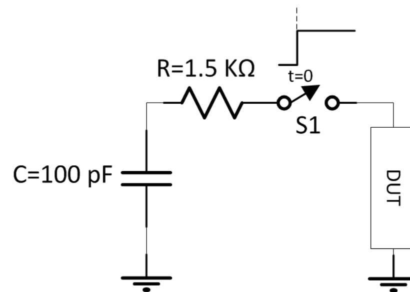

Figure 1 Human Body Model for the ESD Event

Machine Model (MM)

The MM models the discharge event that may occur during machine handling of the semiconductor die. For example, during automated handling, the semiconductor die can build up charge while sliding along a metal line and can later discharge when it comes in contact with a conducting path to ground. The MM is shown in Figure 2 and the standardized spec is available in [2]. The MM finds its primary use in the automotive

industry but has recently fallen out of favor to the HBM since there is good correlation between the two models.

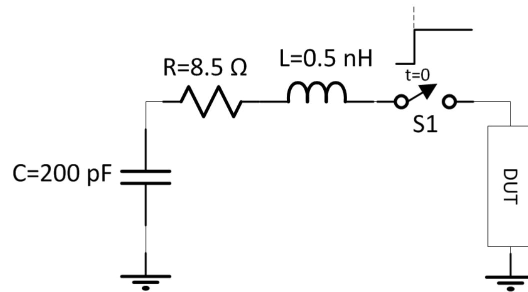

Figure 2 Machine Model for the ESD Event

Charged Device Model (CDM)

The CDM is the most recent among the three models and models the event of the die self-charging and discharging. The event has the fastest rise times and is therefore very sensitive to package parasitics and other stray elements in the testing circuits. Therefore, an accurate model is often difficult to build but efforts have been made in [3].

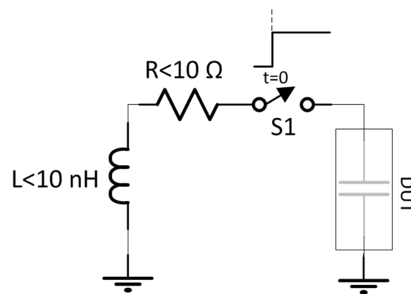

Figure 3 Charged Device Model for the ESD Event

Motivation to Study ESD

Apart from the obvious reasons of protecting circuits from damage, increasing yield and the resulting profitability, several trends in the semiconductor industry today indicate that ESD will be an increasingly important issue in the future. These trends are shrinking process dimensions and increasing sensitivity to damage, increasing count of IO pins on

products, and the need to support new IO requirements like power sequence independence, fast power-up applications, ability to tolerate signal on IO pins when chip is unpowered etc.

Process trends

Since the process technology nodes in the semiconductor industry scale every 1½ to 2 years, the process inherently becomes more susceptible to damage from high voltages due to shrinking oxide, junction, and metal thicknesses. Since thinner oxides and junctions breakdown at lower voltages, ESD design becomes increasingly important as technologies scale. Thinner metals are doubly detrimental to ESD protection because their safe current limits decrease, and they are more resistive which allows more voltage build up on the die.

Apart from the processes becoming inherently weaker from an ESD perspective, the number of active processes every generation is also increasing. Older processes continue to live even with newer processes becoming available. Moreover, processes are being continuously optimized for best performance. These optimizations often can have unexpected impacts on ESD impact. These optimizations and increase in the number of supported processes strain available resources to support and develop ESD designs. Such strain can be considerably alleviated by developing and employing a generic protection strategy.

IO Pin count trends

With the increasing amount of logic gates in the chip every technology, the number of IO pins to support the increased functions also increases. The number of IO pins can be empirically estimated using Rent's equation

$$N_p = kN_{gates}^{\beta}$$

where N_p is the number or IO pins, k is a constant determined by the circuit type (microprocessor, memory, gate array, etc), N_{gates} is the number of gates, and β is a factor of the particular circuit. The increasing trend of IO pins emphasizes the need for a methodical ESD strategy to protect circuits since the product is only as good as its weakest ESD path.

Special-purpose IO requirements

As technologies have increased in complexity, new IO requirements are now required to enable circuit operation. It is critical that the ESD protection scheme adopted does not interfere with the circuit's ability to support these new requirements. Some examples of special circuits include

- Applications requiring IO pins to be tolerant to voltages higher than supply voltages. In such a case, using an up-diode from the IO to the power rail does not work because this diode would be forward-biased during the tolerant condition and result in a large input current.
- Applications requiring IO pins to tolerate voltages even when the IO power supply is down.
- Hot-plug applications require that devices be able to handle fast power-on conditions.
- Circuitry operating with power supply voltages much higher than a single device rated voltage.

ESD Protection Strategies

Although it is possible to get products to pass ESD design specifications using an iterative methodology of testing and fixing, this is rarely practical. Such a random methodology can be very time consuming and invariably causes delays in getting the product to market. Such a methodology may only be feasible for isolated pins on a product and even in those cases, for reasons mentioned above, very risky.

The more practical protection strategy is to use a protection scheme that offers a low impedance path for the ESD current between any two pins on the die during the ESD event. Such a path is active only during the ESD event and remains inactive during normal powered-on operation of the die. Since the path is high impedance during normal powered-on operation of the die, the protection circuits don't interfere with regular circuit operation. Such a protection strategy is shown in Figure 4. The arrows indicate the direction of current possible through the device during the ESD event.

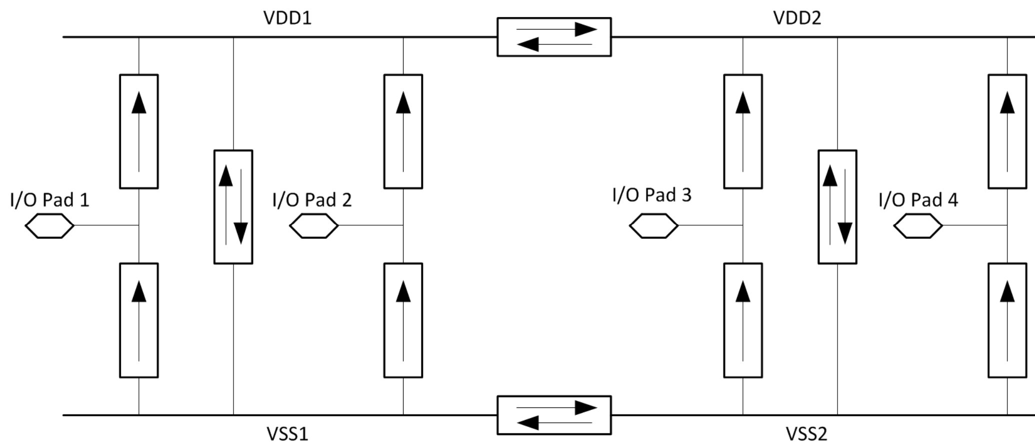

Figure 4 A Generic Methodical ESD Protection Strategy

The ESD path can be constructed using devices that operate close to or in their regular operating modes (linear or saturation) or in a breakdown mode. A wide variety of breakdown-type devices have been used for ESD protection in CMOS circuits. These

include thick field oxide devices, grounded gate NMOS (GGNMOS) devices, silicon controlled recitifiers (SCRs) and spark gaps. For an overview of these devices, please see [4]. Non-breakdown approaches used diodes, MOSFETs, and BJTs operating close to their regular operating regimes to protect circuitry. Operating devices in the breakdown mode makes the scheme dependent on layout and susceptible to process variation. So, ESD designers tend to prefer the non-breakdown approach. The non-breakdown approach also enables ESD simulations to predict and verify ESD performance. For these reasons, the non-breakdown method is also the approach taken for work in this thesis.

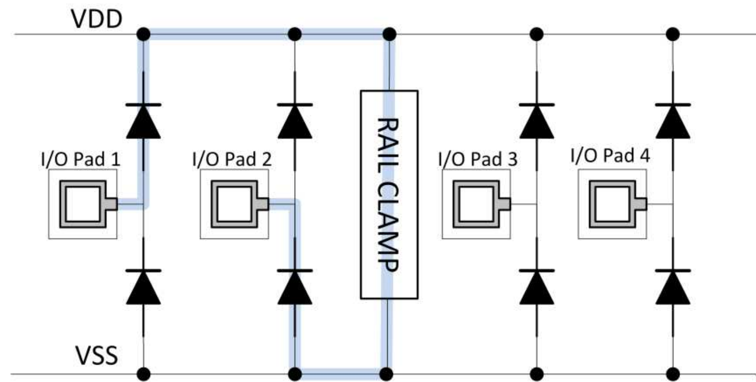

Figure 5 ESD Protection Strategy Used in Many Semiconductor Chips Today

One of the popular ESD strategies used in chips today is shown in Figure 5. The strategy is a more specific implementation of the generic strategy shown in Figure 4. The protection scheme uses diodes from every signal I/O to the power or ESD rail, and to a ground rail. In addition to these diodes, rail clamps are distributed on the die to complete the ESD current path. The strategy ensures that a low impedance path is available for the ESD event between any two pins on the die. For example, during a positive ESD event on pad1 with respect to pad3, the ESD current flows through the up-diode DU1 from pad1 to the VDD rail, then through the rail clamp from the VDD to the VSS rail, and finally

though the down-diode DDN3 from VSS to pad3. The rail clamp is an important element in this scheme and is designed to short-circuit the VDD and VSS rails only during the ESD event. When powered-on during normal operation, the rail clamp is designed to be inactive and have minimum impact on regular circuit operation.

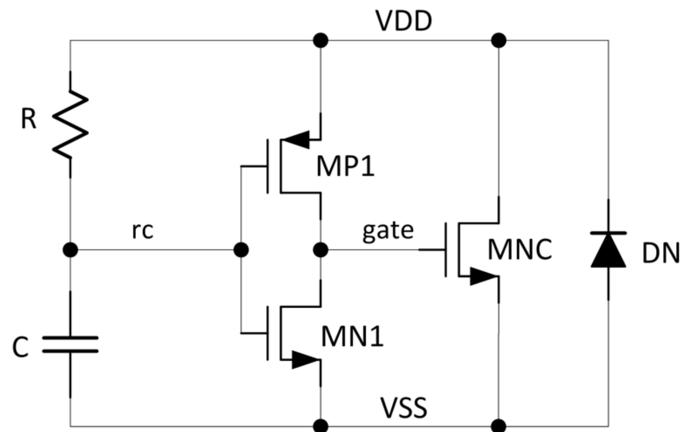

Figure 6 The Non-snapback RC and Single-inverter-based Rail Clamp

The single RC time-constant-based non-snapback rail clamp [5] shown in Figure 6 has been the de facto standard in the industry ever since its introduction over two decades ago. The large RC time constant in this circuit ensures that the rc node stays low initially during the ESD event. Due to this low voltage input, the inverter drives the gate node high during the ESD event to turn-on the clamping transistor MNC. As the ESD energy is dissipated, and the rc node charges up, the clamp turns-off after a certain time when the rc node reaches the trip-point of the inverter. During normal powered-on operation, the rc node is charged to VDD and the gate node is driven low, keeping the clamp in the off state.

CHAPTER 2

PRIOR WORK AND LIMITATIONS

Since the work in this thesis has primarily focused on the two aspects of design automation for rail clamps, and new rail clamp circuits, the prior literature is presented under these two section headings.

Rail Clamp Design Automation

Design automation work on ESD protection have primarily focused on catching chip level concerns such as high metal line resistance along the ESD current path, missing ESD protection elements etc. Some such works include [6-8]. Literature on design methodology for ESD protection has focused on either optimizing either chip level strategy or individual ESD devices. [9] illustrates a chip level ESD design methodology that is technology independent. The work focusses on the top level strategy and only design constraints for the rail clamps are mentioned. More recently, [10] presents a method to size elements like transistors, and gated diodes in a FINFET process for ESD-leakage tradeoffs. This work relies on experimental data from TLP machine and seeks to take advantage of layout effects such as fin width to fine tune the ESD element. The work does not aim to optimize the full rail clamp circuit. [11] also presented a TLP experiment-based optimization technique for high voltage DMOS applications. Other works like [12] and [13] present TCAD simulation-based approaches to find the best ESD protection device. Often early in the process, the designer does not have access to experimental ESD data. Also as technologies advance, foundries are more reluctant than ever before to share process information to enable TCAD flows. Thus, experiment and TCAD-based design methods for ESD protection are not always feasible when designers begin designing in a

process node. Also from our experience, once a circuit has been designed, there is much reluctance in the industry to revisit the circuit only for optimizing it. Designs tend to be revisited only if there is a problem. In this work, our goal is to do the best optimization for the traditional rail clamp (shown in Figure 6) with the standard foundry provided SPICE models. Since the active rail clamp only operates in the well-known operating regimes, we are able to rely on standard foundry provided models to optimize the rail clamp circuit.

Authors have reported using a wide range of values for the circuit elements in this circuit in the literature. For instance, a large number of time constant values ranging from 100 ns [14] to 2 μs [15] have been quoted in the literature for these rail clamp circuits. Other values quoted include greater than 1000 ns [16, 17], 866 ns [18] and 1.5 μs-2 μs [19]. Further, from discussions with designers, we have learned that some designers are only comfortable with higher value time constants, up to 5 μs. It is not always clear what assumptions were made in these cases or what corner cases were considered. In the proposed design methodology, we present for the first time, a method to size the time constant based on the residual voltage left behind on the rail after the ESD event has been dissipated. Clamping devices used in literature are mostly NMOS transistors usually with a few thousand microns of width. Some works like [19, 20] use a PMOS clamping device citing better ESD performance or leakage characteristics for these devices in the considered process. With the proposed design methodology, the designer is able to select the best clamping device type and size in any given process to meet the required design specifications.

Rail Clamp Architectures

ESD protection circuits can be designed choosing to operate the clamping transistor in either snapback mode or the regular linear or saturation modes. Snapback is used to refer to the region of MOSFET operation when the FET operates like a bipolar device when the drain junction avalanches due to high electric field. Under this condition, the n-MOSFET operates like a BJT with the drain as the collector, substrate as the base, and the source as the emitter [21]. The snapback region is not modeled in foundry provided SPICE models. Also, the snapback behavior of the MOSFET is not consistent across foundries. These reasons have led designers to prefer circuit solutions that operate the devices in the linear or saturation mode. Since SPICE models are very accurate in these regimes, designers are able to simulate the ESD event and predict ESD performance readily using this method. The current work also uses this approach.

Rail clamps that have used the non-breakdown approach can further be classified into single time-constant-based [5, 17, 22-25], dual time-constant-based [18, 26] and latch or feedback-based rail clamps [15, 27-31]. Merrill & Issaq [5] presented the first transient RC time-constant-based rail clamp showing that circuits in regular operating regimes can be used for ESD protection. Ker [14] used the transient rail clamp to improve the ESD performance of a 0.8 μm technology die from 0.5 kV to above 3 kV. Chen and Ker [32] showed that using a three inverter string in the transient clamp offered no advantage over using a single-inverter-based design. The authors in [17] presented a rail clamp architecture that used a reduced time constant and separate paths for turning-on and turning-off the rail clamp. The large turn-off delay was implemented by using weak MOSFETs as resistors to charge capacitors in the turn-off path. Other architectures

implemented the time constants in different ways such as a diode connected transistor and the parasitic well capacitance of the clamping transistor [22] and a capacitor in series with stack of diode connected transistors [23]. Thijs et al.'s design [24] eliminated the need for a diode between the rails to protect during the negative ESD event by making the clamping device bi-directional. More recently, a comparator was employed in the single time constant rail clamp to save area and reduce the time constant value [25].

The first dual time constant rail clamp [26] can support faster power ramps and is immune to lock-on due to absence of feedback but doesn't offer any area savings over the RC and single-inverter-based circuit. It has been shown [18] that the fastest power supply ramp that can be supported by this architecture can be limited because of the wide transition regime between the ESD regime and the power-up regime. The rail clamp presented in [18] solved both the area and wide transition regime limitations but the design was not immune to lock-on, particularly if the power rail routing to the rail clamp was resistive [33].

Feedback was employed in [15] to alleviate the effect of gate leakage in MOSFET capacitors in ESD clamps. The technique was applied to a high voltage clamp targeted for high performance processes but the design dissipates static power. Cascaded p-FET feedback was employed in [27] to prolong the on-time of the rail clamp. The circuit relies on leakage current of a MOSFET for circuit operation. Other works that employ feedback include [28] which presented a latch-based clamp and [29] that used a thyristor in the rail clamp. Sarbishaei et al. [30] added the ability to deactivate the latch for the latch-based clamp. Yeh and Ker [31] employed a stack of diodes to mitigate the risk of lock-on inside a latch-like trigger circuit.

All these circuits present new ideas and focus on achieving area-efficient realizations of the rail clamp. Most works however do not discuss the operation of the presented circuit in a given PVT space. From our design experience, it can be challenging to design these circuits to maintain functionality inside an industry-standard PVT space. The large variation in these circuits primarily arises from the use of active elements to replace the time constant elements. The resistance and capacitance of these active elements vary significantly from their nominal values as process, temperature and voltage vary.

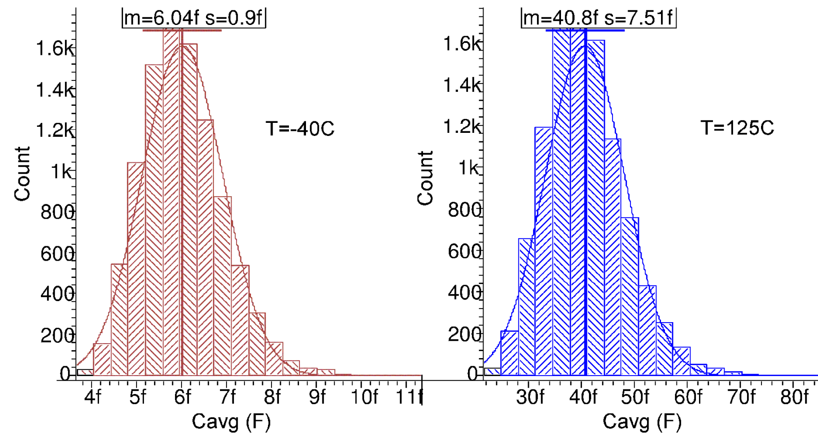

Figure 7 Distribution of Average DC Capacitance of a NMOS 1μm/0.1μm Transistor at Temperature Extremes as the Gate Transitions from 0V to VDD (Using 10,000 Points)

For example, Figure 7 shows the variation in the average gate capacitance of a 1μm/0.1μm NMOS device when the gate terminal is varied from 0 V to the supply voltage. The capacitance value can vary between 3.3 fF to 63.3 fF. Also, the resistance of the same device measured with gate-to-source and drain-to-source voltages at VDD/2 can vary from 17.5 kΩ to 310 kΩ over the given PVT space. This resistance variation is shown in Figure 8.

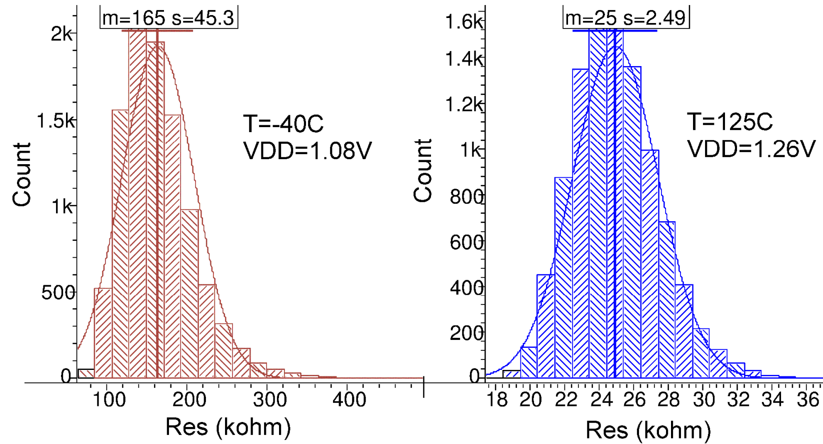

Figure 8 Distribution of Large Signal Resistance Values of a NMOS 1μm/0.1μm Transistor at Voltage and Temperature Extremes with VGS=VDS=VDD/2 (Using 10,000 Points)

The leakage current of the same device can vary by several orders of magnitude as shown in Figure 9. The drain-to-source leakage current of the NMOS device is seen to vary from a few fA to 4.4 nA.

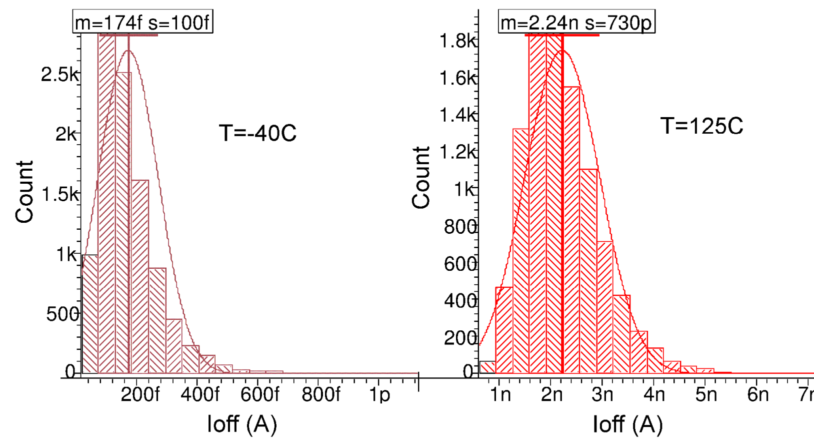

Figure 9 Distribution of Drain Leakage Current of a NMOS 1μm/0.1μm Transistor at Temperature Extremes with VGS=0, VDS=VDD (Using 10,000 Points)

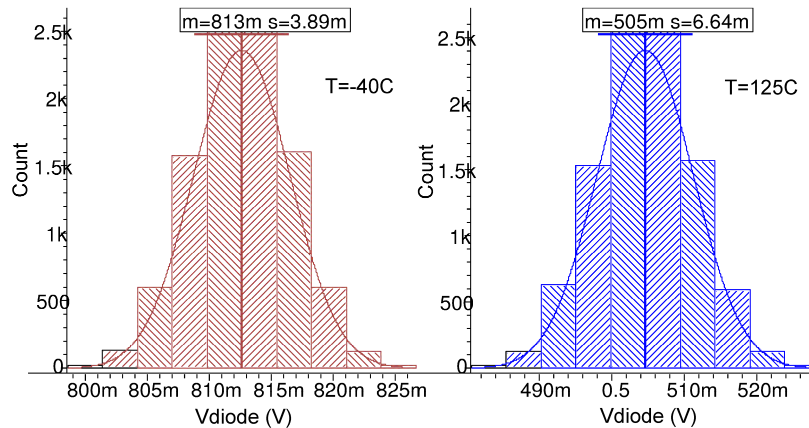

Figure 10 Distribution of Forward Diode Voltage for a 2μm x 2μm Diode at Temperature Extremes with Constant Bias Current of 1 μA (Using 10,000 Points)

Figure 10 shows the distribution of the forward-diode voltage for a 4 μm^2 area diode when biased with constant current of 1 μA. The diode voltage can vary from 480 mV to 824 mV. These large variations in the parameters of active devices support our experience that many rail clamp architectures that use such circuit structures are unable to maintain functionality over the standard PVT design space. For some other circuits, because of the large variation, the circuit elements have to be sized up considerably from their nominal values to meet specifications at all corners making their area savings much less attractive. Another consequence of this large variation is that several specifications like the fastest power ramp supported by the circuit are significantly worse from their nominal values. This specification degradation limits the usefulness of the design in a real-world environment. Clearly, applications could benefit from rail clamp architectures that are area efficient but don't suffer from such large variations in performance over PVT conditions. Two such architectures are presented later.

CHAPTER 3

SYSTEMATIC DESIGN OF THE TRADITIONAL RC AND SINGLE-INVERTER-BASED RAIL CLAMP

The non-snapback active rail clamp circuit shown in Figure 6 was introduced in [5] and uses a single RC time constant along with an inverter and a clamping MOSFET device. Another flavor of this rail clamp uses a string of three inverters, instead of one, but this circuit has been shown to have no advantage over the single-inverter-based design [32]. Since [5], there have been several new rail clamp topologies discussed in the literature. For a list of such architectures, see [33]. These circuits offer significant area savings, due to the reduced time constants employed. However, many of these clamps include some sort of feedback and need detailed analyses to ensure the prevention of a latched-on state. The latched-on state is used to refer to a condition in which the rail clamp if turned on during normal powered-on mode, stays in that mode indefinitely. Such a latched-on state can be catastrophic since the power and ground rails remain shorted till the power is reset. Moreover, many of these circuits are difficult to design into products because of the large process variation in today's processes [25]. Because of these difficulties with other rail clamp circuits, the RC and single-inverter-based circuit continues to be widely used in the industry today.

In spite of its popularity, there is no literature on the circuit's design tradeoffs or automation. The goal of this work is to propose, illustrate, and validate a design methodology for this rail clamp that can be employed for design in a real-world scenario. The methodology can also be used to automate the full design. The methodology uses well known parameters like transistor saturation currents, I_{DS}, and leakage currents, I_{OFF},

and parasitic capacitances on nodes to design a robust circuit. Using such an approach makes the design methodology universal and applicable to all process nodes. The method aims to achieve the minimum area design that can meet a particular ESD performance and leakage target. This goal is a frequent requirement in the industry. Designers in the industry are required to ensure that their designs work in the process, voltage, and temperature design space of the product and therefore this methodology takes into account these factors and ensures that the resulting design meets ESD and leakage targets at all valid corner conditions. The industry-standard approach of simulating the design over corners that model the extremes in variation is used. The design method is explained and validated using a 40 nm low power process. For the spice simulations, the process corners considered are slow, fast, slown-fastp, fastn-slowp, and typical. The temperature corners considered are 25 C, 125 C, and −40 C, and the voltage corners considered are 1.08 V, 1.20 V, and 1.26 V. These corner conditions are the industry-standard supported by the foundry for the considered process. Finally, the design yielded by the proposed methodology is compared with viable designs obtained by randomly and aggressively sampling the design space 250,000 times.

Rail Clamp Operation

During normal powered-on operation, the 'rc' node in Figure 6 is charged to VDD. The inverter drives the 'gate' node low and ensures that the clamping transistor, MNC, is switched off. Thus the rail clamp is inactive during normal powered-on operation of the die.

In the case of a positive ESD strike on the VDD rail with respect to VSS, the 'rc' node stays low initially due to the RC time constant. Because the input to the inverter is

low, the inverter drives the 'gate' node to VDD. When the gate of the MNC transistor is driven high, MNC turns on, and offers a path for the ESD current to flow from VDD to VSS. As the ESD energy is dissipated, the voltage on the VDD node falls. At the same time the voltage on the 'rc' node charges up towards VDD. When the 'rc' node crosses the trip-point of the inverter, the 'gate' node is driven low and the clamp is shut off. This ESD response is shown Figure . As soon as the clamp turns on, the voltage on the VDD rail is clamped to a safe value called the clamped voltage, Vclmp. The clamp turns off after a certain time, toff. When this happens, the residual energy in the ESD event causes the voltage on the VDD rail to climb back up to a certain value, Vres.

During a negative ESD strike on VDD with respect to VSS, the diode DN is forward-biased and conducts the ESD current. This diode is not part of the original circuit in [5] but is widely used in the industry for robust ESD performance during the negative ESD event.

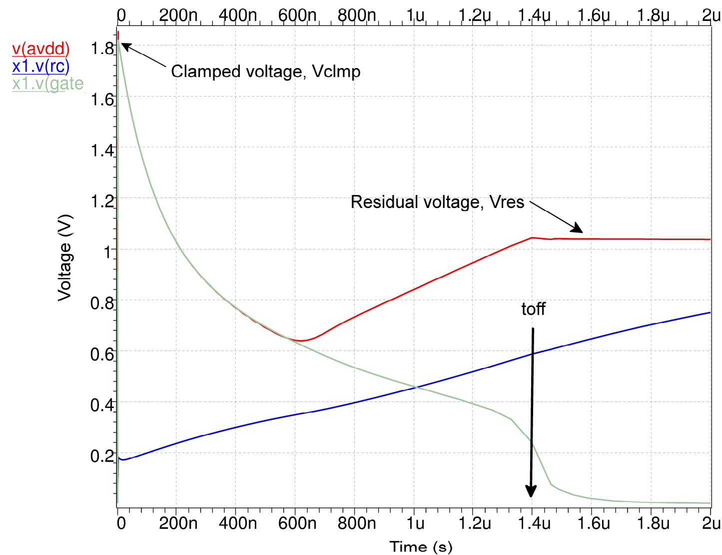

Figure 11 Typical VDD Waveform during the ESD Event

Rail Clamp Characteristics

The important specifications for the rail clamp are ESD performance, leakage during normal powered-on operation, and silicon area.

ESD Performance

All products today require compliance to the Human Body Model (HBM) ESD specification [1], usually to 2000 V.

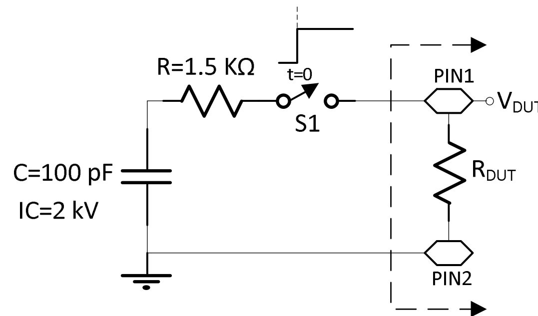

Figure 12 Human Body Model for the ESD Event (2000 V)

The HBM shown in Figure 12 models the human as 100 pF capacitor in series with 1500 Ω resistance. The individual charged to the specification limit (e.g. 2000 V) discharges between any two pins on the die. For a 2000V HBM event, the peak current can be computed to be approximately 2000V / 1500Ω = 1.3 A ($R_{DUT} << 1500$ Ω).

For the specific case when PIN1=VDD, PIN2=VSS, R_{DUT} is the clamp resistance, R_{CLMP}. The initial peak voltage on the VDD rail in this case, V_{clmp}, results from voltage division between the 1.5 kΩ resistor and the clamp resistance (neglecting bus and package parasitic impedances). Making a simplifying assumption that the clamp resistance is constant during the time of ESD discharge, the time constant for the discharge event can be calculated to be approximately 150 ns (R_{CLMP} is negligible

compared to 1.5 kΩ). The voltage on the VDD rail as a function of time during the ESD event can be mathematically be calculated to be

$$V_{DUT} = V_{clmp} e^{-\frac{t}{150n}}$$

At a later instant in time, the clamp turns off, and the residual charge on the capacitor causes the voltage on the VDD rail to rise. This residual voltage on the rail after the clamp turns off can be calculated as

$$V_{res} = \frac{\text{Residual charge}}{\text{capacitance}} = \frac{200\text{nC}\ e^{-t_{off}/150n}}{100\text{pF}}$$

Here, t_{off} is the time duration for which the clamp is actively conducting. 200 nC is the initial charge on the human during the 2 kV HBM event, calculated using the familiar Q=CV relation with V=2000 V and C=100 pF (see Figure 12), In most practical cases, the residual voltage is lower than that predicted by the above equation because of the additional on die parasitic capacitance between the rails. However, in isolated smaller power segments, there may be little additional capacitance. So, we assume the worst case of no additional capacitance here. The residual voltage left behind on the rail after the ESD event is an important reliability consideration, especially for low power processes [34]. In our design, we design to keep the clamp conducting long enough to limit this residual voltage below the rated voltage of the devices for reliable ESD protection.

To be compliant to the 2 kV ESD performance specification, the protection scheme on the die should ensure that the voltage on the tested pin with respect to the power and ground rails on the die is clamped below a certain maximum voltage limit during the ESD event. This voltage limit should be lower than both the gate breakdown and the drain snapback voltage of transistors to safely dissipate the ESD energy. With

this constraint in mind, the ESD designer budgets a voltage drop across every element in the ESD path. For example, in this 40 nm process, the voltage drop across the clamping diode (V_{diode}) and the rail clamp (V_{clmp}) in Figure 5 may be budgeted 1.3 V and 1.8 V, respectively, during the ESD event. The resistance of the metal connections in the ESD path may be limited to 0.7 Ω which limits the voltage drop in the metal (V_{metal}) to 0.91 V for a 2 kV HBM event. The maximum voltage on the pin, V_{pin}, with respect to the ground on the chip can be calculated as

$$V_{pin} = V_{diode} + V_{clmp} + V_{metal}$$

Summing the voltages across the different elements, we see that the pin could see up to 4.01 V during the ESD event. In this process, the snapback voltage of the device is 4.1 V and the gate breakdown voltage of the device for a 100 ns pulse is 5 V.

Leakage

The leakage of the rail clamp is dominated by the large clamping MOSFET, MNC. The leakage in the inverter is negligible and can be reduced even further, if needed, by using long gate lengths for the inverter devices. Some realizations may use a MOS capacitor to realize the time constant. In this case, it may be argued that the gate leakage of the MOS capacitor may contribute some leakage current. But such active capacitor realizations can only be used if the gate leakage of the device is very small since any current through the large resistor used to realize the time constant can cause the rc node to be lower than the VDD rail leading to shoot-through current in the inverter. For a design that ensures that the rc node charges all the way to VDD during normal powered operation, an accurate first-order estimate of the circuit leakage is possible by analyzing only the clamping device, MNC.

Area

The dominant contributors to the area of the rail clamp are the clamping transistor and the time constant circuit. Therefore, it is necessary to optimize these elements from an area perspective also. The clamping transistor will have to burn the area needed to meet the leakage target but no more. It is also important to use as small a time constant as possible to minimize its area. The best clamp design would be one that meets the required ESD and leakage targets and uses the least silicon real estate. This is the goal of our presented design methodology as well.

Design Methodology

In this section, we detail the sizing of the different circuit elements in the rail clamp.

Clamp Transistor

The clamping transistor determines the initial clamped voltage and dominates the leakage performance of the rail clamp. The length of the device used for this transistor is critical for area, and leakage tradeoffs. A smaller length results in reduced area but can result in unacceptable leakage. Using a larger length usually yields a lower leakage design, but increases area. To determine the best possible device, the I_{DSAT} and I_{DOFF} (both per µm width) of the device for different gate lengths are simulated. For best accuracy, the I_{DSAT} is measured at the target clamped voltage whereas the I_{DOFF} is measured at the regular operating voltage. These simulations are run over all process, voltage, and temperature (PVT) corners. As a figure of merit (FOM), $I_{DSAT,min}/I_{DOFF,max}$ can be plotted for different gate lengths. Here, $I_{DSAT,min}$ is the minimum I_{DSAT} over all process corners. Similarly, $I_{DOFF,max}$ is the maximum leakage number achieved over all

PVT conditions. A peak in the FOM vs. gate length indicates the length that yields the maximum saturation current with minimum leakage.

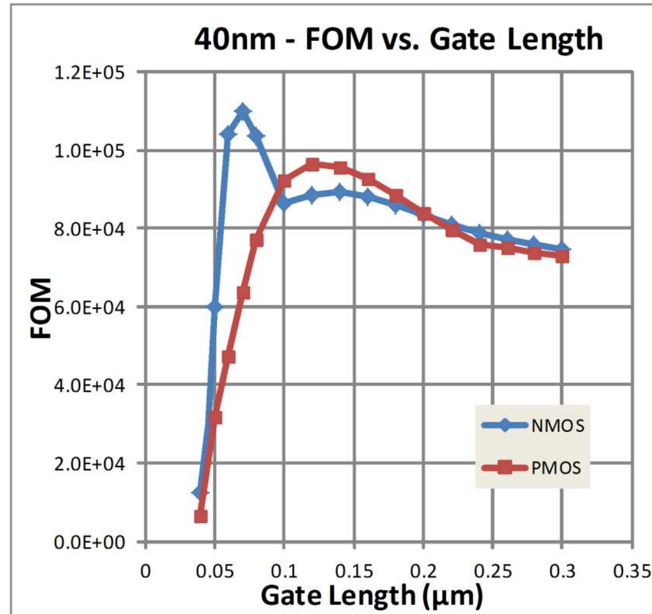

Figure 13 Idsat/Ioff Vs. Gate Length for the Core Device

Figure 13 shows the FOM trend for the 40 nm process. For many modern processes, this peaking behavior is seen in the MOSFET used in core circuitry. This trend is in contrast to the expected increasing trend for older technology nodes. Using a length greater than this optimal value does not provide any leakage improvement but increases area. The width of the MNC device can be sized to provide a minimum I_{DSAT} of 1.3 A at the targeted clamp voltage, i.e. $W_{MNC}=1.3/I_{DSAT,min}$. A very good worst case leakage estimate for the selected device and the full rail clamp over all corners can be arrived at by using $W_{MNC}*I_{DOFF,max}$ or W_{MNC}/FOM. Based on data in Figure 13, a gate length of 70 nm was chosen for the MNC device in our design. The total width of the MNC device was calculated to be 1380 µm which is realized with 138 fingers and a unit finger width of 10 µm. The individual finger width is flexible but a larger finger width is chosen

because it helps save overall area. For most modern technologies, this width can be set to the maximum finger width that is allowed by the process design rule. With a transistor of this size, the maximum leakage over PVT corners of the clamp is expected to be 4.6 μA. To select the most appropriate device, the FOM simulations should be run on all flavors of the device (low and high threshold voltage versions) and the PMOS device as well. For a PMOS clamping transistor based design, the circuit connections of the time constant elements R, and C are swapped with respect to the traditional circuit to retain the same function.

Often, the designer may not have a specific leakage target to shoot for. In these cases, choosing the gate length where the FOM peaks gives the best tradeoff between leakage and area. If there is no specific leakage target and no FOM peak, the designer can choose the minimum gate length to get the least area design. Designing the rail clamp using this method also lets the designer explore the absolute minimum leakage design possible using this traditional architecture. The design procedure for determining the best clamping transistor type and its dimensions is summarized in the flowchart in Figure 14.

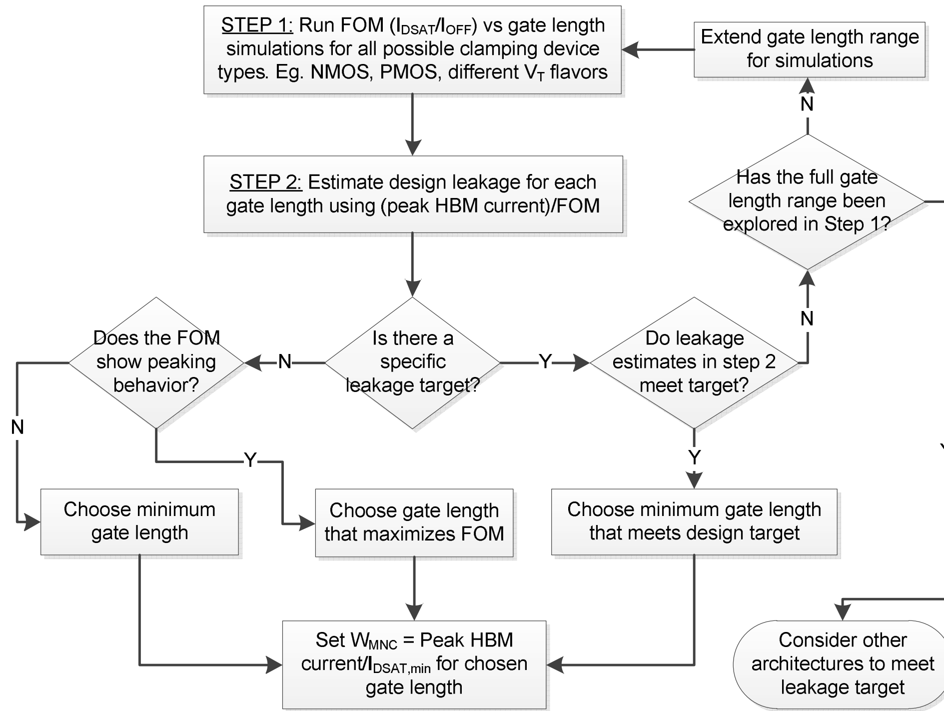

Figure 14 Method to Determine the Best Clamping Device and its Dimensions

Time constant

The on time of the rail clamp is determined by the RC time constant, and the inverter trip-point. To demonstrate the effect of the inverter trip-point on the clamp's on time and the residual voltage, we use the setup shown in Figure 15.

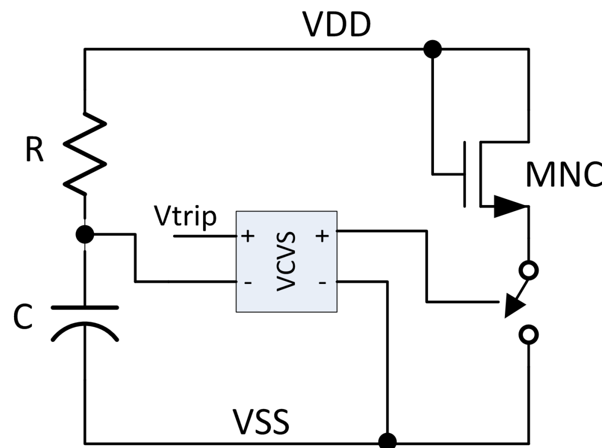

Figure 15 Setup to Determine the Time Constant

In this setup, the inverter is modeled as a voltage controlled voltage source. The trip-point of the inverter can be set to any required ratio of VDD using a large resistive divider (not shown) from VDD to VSS. This enables us to quickly set the inverter trip-point without going through the more involved process of sizing the inverter transistors. To see the effect the inverter trip-point can have on the on-time of the clamp, we can choose an arbitrary time constant value and view the clamp performance for different inverter trip-points.

Figure 16 shows the ESD performance of the setup using an RC time constant of 0.9 μs, for inverter trip-points from 40% VDD to 90% VDD. The time constant value chosen for this experiment is arbitrary, only serving to illustrate the effect of the inverter trip-point. MNC transistor size determined earlier is used for this analysis. From the results, clearly, the inverter trip-point can have a considerable impact on the time the clamp stays conducting during the ESD event. A higher trip-point inverter ensures that the clamp stays on for longer before disengaging. That is, a higher trip-point inverter enables the designer to use a smaller time constant which translates into area savings. The trip-point of the inverter varies considerably over process corners and if this variation is not accounted for during design, the clamp can suffer from early time-out at many corners. Also, due to process variation in technology nodes, a design that achieves a very high trip-point for all process corner conditions is difficult to achieve.

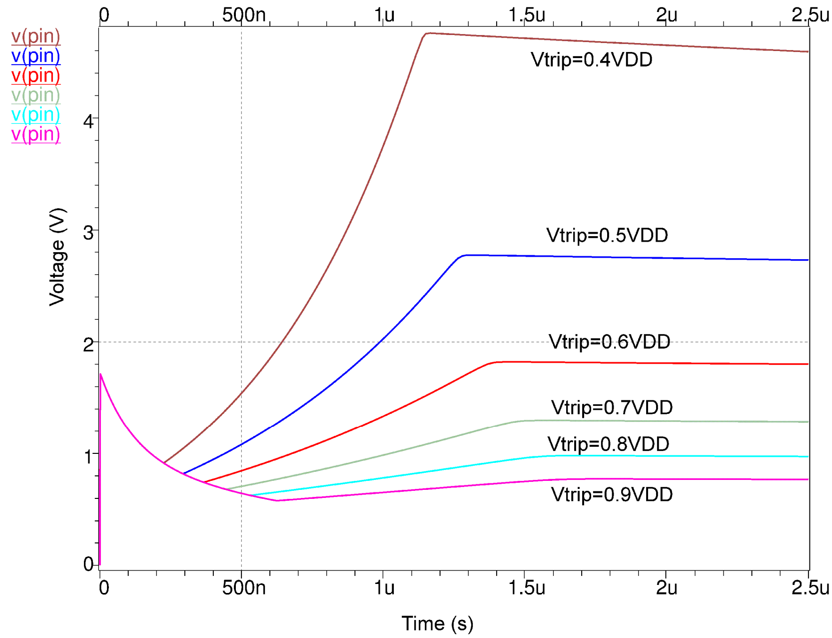

Figure 16 Effect of Inverter Trip-point on the Residual Voltage

From design experience, we propose that a reasonably high trip-point for the inverter that can be achieved over all corners is 0.6VDD. We will later prove that this is a good thumb rule value to use. To size the time constant, we can set Vtrip in Figure 15 to 0.6VDD and step through the time constant values in simulations till the residual ESD voltage, Vres, is below the rated device voltage at all corners. This procedure is shown next in Figure 17.

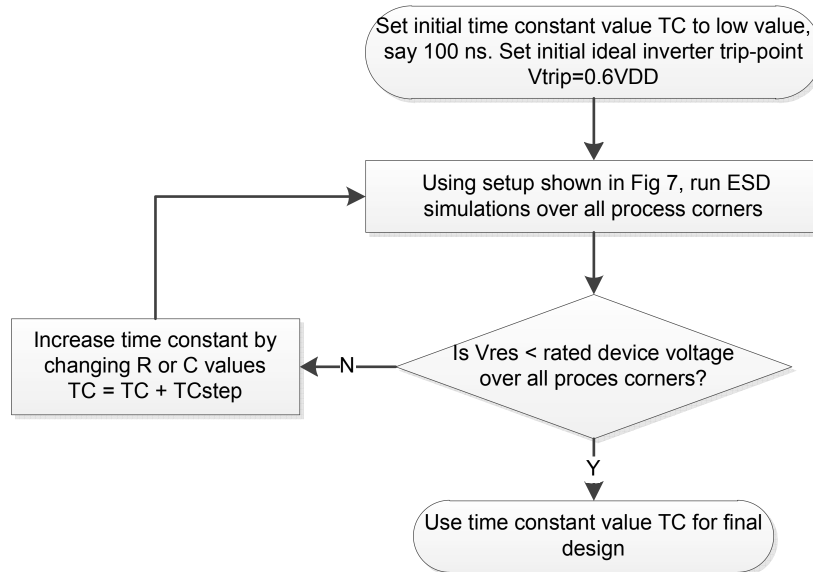

Figure 17 Determining the Time Constant for the Rail Clamp Circuit

One advantage of sizing the time constant this way is that the variation in the R, and C elements are automatically taken into account when the simulation in Figure is run over corners and there is no need to account for the variation in these elements separately. This method also works well irrespective of how the elements are realized. The capacitor can be realized as a metal capacitor or MOSFET capacitor. The resistor is usually realized using a high sheet resistance resistor available in all CMOS technologies. A MOSFET resistor is not preferred for the rail clamp [27]. In our design, an RC time constant of 1.23 μs assuming a minimum inverter trip-point of 0.6VDD ensures that the residual voltage is less than 1.26 V over all corners. The determined time constant value can be realized using a combination of R, and C values that yields a minimum silicon area design. For example, in the considered process, there are six layers of metal and the metal capacitor can include metal layers from M1 to M6. Since the layout of both the resistor and M1-M6 metal capacitor renders the area unavailable for transistors, the most area efficient implementation of the time constant results when the metal capacitor is

placed over the resistor. The area of the resistor and capacitor structures can be estimated using process specific information and the simple equations in Table 1. Equations to estimate the area of transistors (required later for estimating full design area) are also included in the same table for completeness.

Table 1 Equations to Estimate Silicon Area

Equations to estimate Si area	Term Definitions
Resistor $A_{res} = L_{res}W_{res} + (n_{stripes} - 1)L_{max}W_{rspacing}$ $L_{res} = \frac{R.W_{res}}{\rho_{sh}}$ $n_{stripes} = roundup\left(\frac{L_{res}}{L_{max}}\right)$	A_{res} = estimated area of the resistor with resistance, R L_{res} = total length of the resistor W_{res} = width of the resistor stripe $n_{stripes}$ = no of stripes to realize full resistor L_{max} = DRC rule for maximum length of single resistor stripe $W_{rspacing}$ = DRC rule for spacing between resistor stripes ρ_{sh} = sheet resistance of resistor in ohms/sq
Capacitor $A_{cap} = \frac{C}{C_{density}}$	A_{cap} = estimated area of capacitor with capacitance C $C_{density}$ = capacitance density per μm^2 of area

Transistor $$A_{mos} = (mL_{mos} + (m+1)L_{drain})W_{mos}$$	A_{mos} = estimated area of p/n MOSFET m = number of fingers of MOSFET L_{drain} = length of drain of MOSFET W_{mos} = width of single finger of MOSFET

After an initial arbitrary assignment of resistance and capacitance values to realize the determined time constant, these values can be tweaked maintaining the targeted time constant value till roughly equal layout area of R and C components is achieved. This optimization procedure is shown in Figure 18.

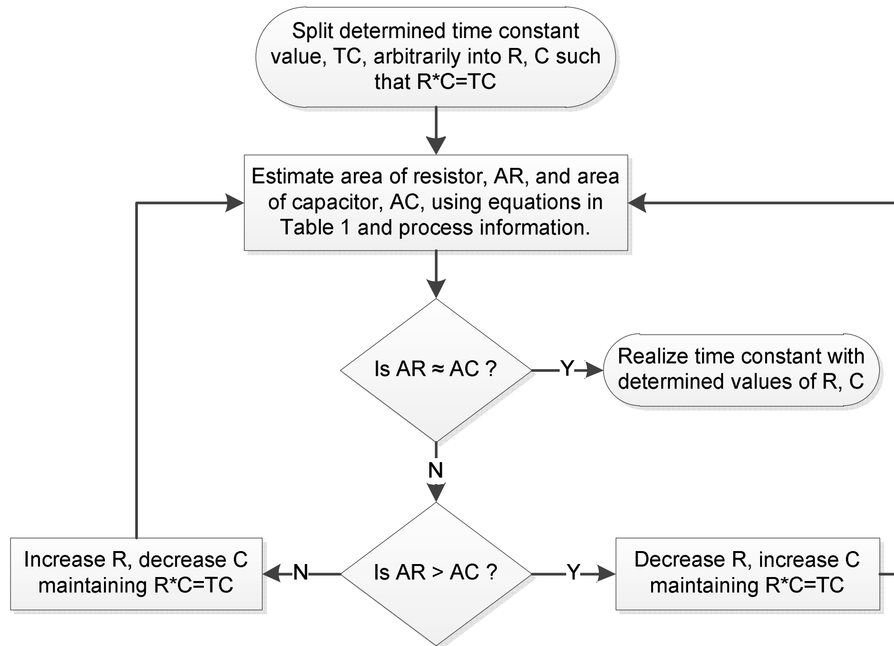

Figure 18 Optimizing the Resistor and Metal Capacitor for Silicon Area

Inverter

One role of the inverter mentioned earlier is to determine the clamp's on time during the ESD event. Besides this function, the PMOS in the inverter must drive the gate node strongly during the ESD event to quickly turn on the clamping transistor. The NMOS in the inverter must drive the gate node low during and after power up to keep the clamp switched off.

To size the inverter transistors, first, we need to gauge the capacitive load on the 'gate' net. A good approximation of this capacitance is the gate capacitance of the MNC transistor. This capacitance value is easily obtained from SPICE for the clamping device size determined earlier. Once this capacitance is available (1.5 pF in our design), the PMOS can be sized to supply a minimum I_{DSAT} over all process corners that will charge the gate cap in less than 1 ns. We aim for a response time of 1 ns for the rail clamp since the HBM standard specifies the ESD event with rise times from 2 ns to 10 ns. We can use the familiar relation $I = C\,dV/dt$ to find the required minimum I_{DSAT} value. In our example design, the PMOS is sized to have minimum I_{DSAT} of 2.7 mA so that it is able to charge the gate capacitance of 1.5 pF in less than 1 ns. The gate length for the PMOS device can be chosen from the FOM simulation results. If a peak FOM exists, the designer can choose the gate length where the peak exists. In the absence of a peak, the designer can choose twice the minimum gate length.

The size (W/L) of the NMOS transistor, MN, should be large enough to keep the "gate" node low during power ramp-up. Power-on times for the vast majority of applications are usually in the hundreds of microseconds. The inverter NMOS sized to discharge the gate cap faster than 100 ns is amply sufficient to hold the gate node low for

such ramp-up times. In our design, the NMOS is sized to have I_{DSAT} greater than 19 μA to discharge the gate cap in less than 100 ns. The gate length of the NMOS can be much larger than the minimum. The area penalty in using larger than minimum gate length is negligible as the I_{DSAT} required from the NMOS is small. From the discussion in section 0, the inverter trip-point should be higher than 0.6VDD. After sizing the inverter transistors as described, we can increase the size of the PMOS transistor if required to meet this constraint. The trip-point requirement only needs to be met at room temperature since the ESD tests are only run at room temperature. It is not necessary to meet the trip-point constraint over extreme temperature corners. A summary of the described design procedure for the inverter devices is given in the flowchart below.

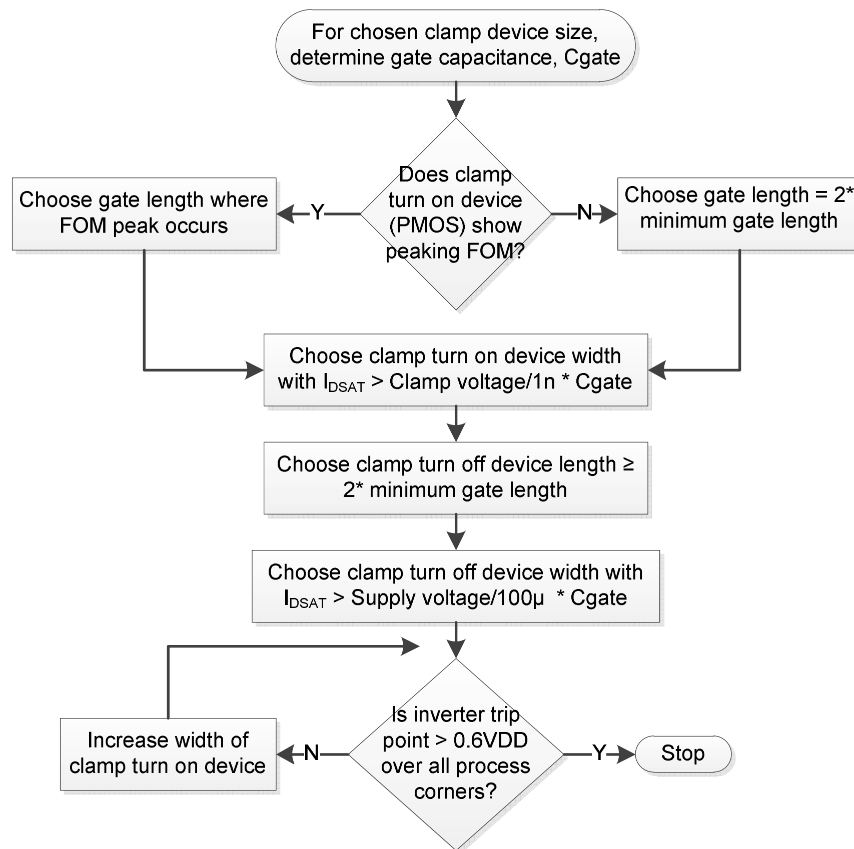

Figure 19 Designing the Inverter Devices

Achieved Design and Performance Results

Table 2 summarizes the design obtained by following the proposed design methodology. The widths and lengths of the MOSFET devices are denoted by W and L, respectively, subscripted by the name of the device.

Table 2 Design Obtained by Using the Proposed Methodology

Design Parameter	Value
R	1080 kΩ
C	1.14 pF
W_{MP}	57 μm
L_{MP}	0.12 μm
W_{MN}	20 μm
L_{MN}	0.12 μm
W_{MNC}	1380 μm
L_{MNC}	0.07 μm

Simulations to predict the 2kV HBM response of the designed clamp show that the initial peak voltage is less than 1.75V and the residual voltage after clamp turn off is less than 1.26 V over all process corners. These results over process corners are shown next in Figure 20Figure . The process corners for the ESD test include the following – typical, slowlow, slowhigh, fastlow, fasthigh, snfplow, snfphigh, fnsplow, and fnsphigh. Since the ESD tests are run at nominal temperature on an un-powered die, voltage and temperature corners for this test are not necessary.

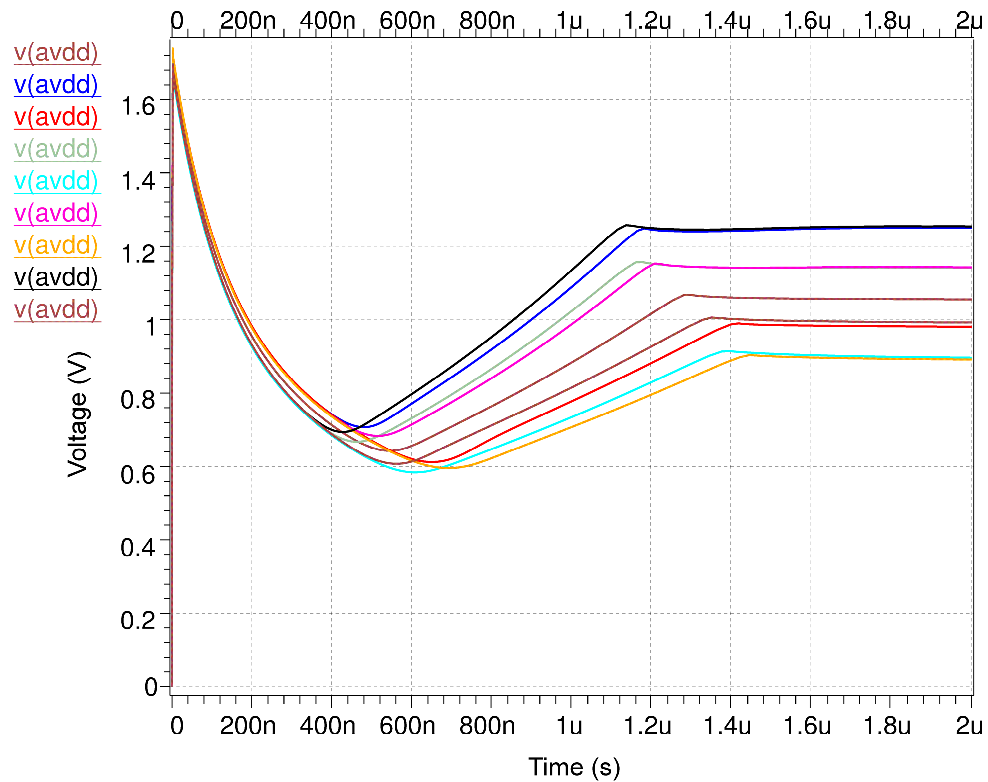

Figure 20 Simulated 2 kV HBM Response of the Obtained Design over All Process Corners

The maximum leakage current in the rail clamp over PVT conditions is 4.7 µA and is only 100 nA different from our estimate earlier. Power-on simulations with a power ramp-up time of 10 µs show that the gate node is held low reliably during and after power-on with a peak power-supply current of less than 0.21mA over all PVT conditions. These power-on results are shown in Figure 21. Both the leakage and power-on tests are simulated using all nine process corners, three voltage corners (1.08 V, 1.20 V, and 1.26 V) and three temperature corners (-40 C, 25 C, and 125 C).

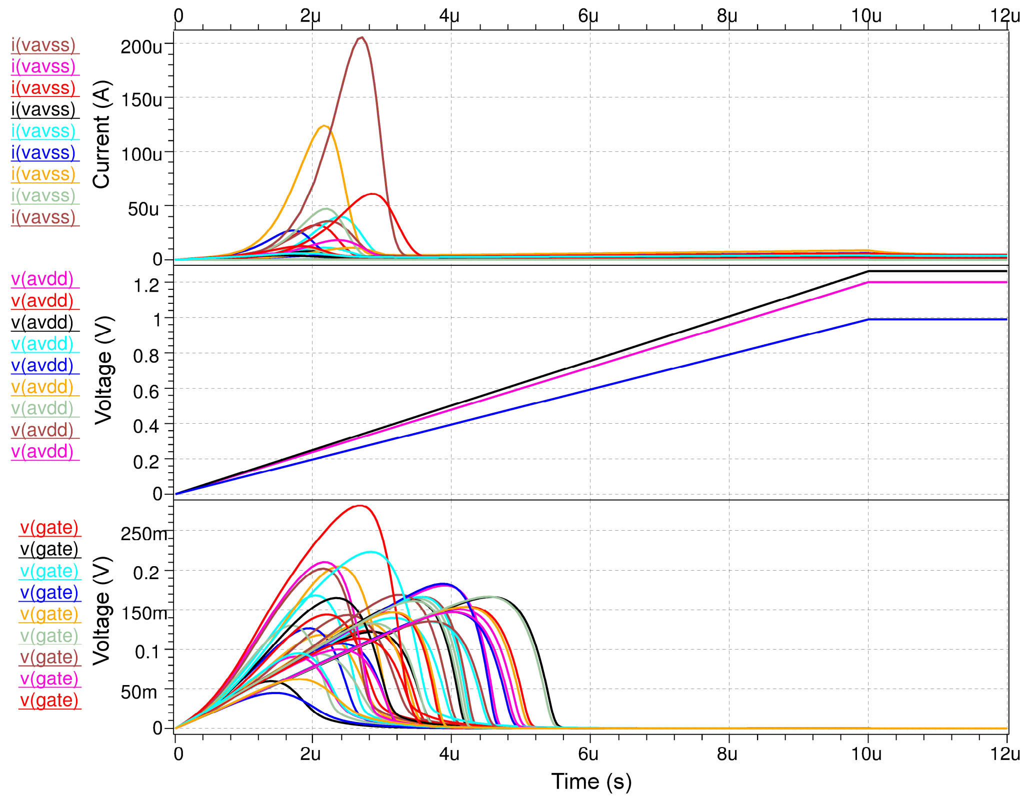

Figure 21 Simulated Power-on Performance of the Obtained Design over All PVT Corners

Methodology Validation

To validate the proposed methodology and determine if the resulting design is close to the optimal solution, another parallel design method to locate the best solution using simulations and randomly sampling the design space was employed. For this experiment, the input parameters are the widths and lengths of the MOSFET devices, MP, MN, and MNC, and the values of the time constant elements, resistor R, and capacitor C. These eight input parameters are uniformly sampled from the design space shown in Table 3. A total of 250,000 points are run to gain good coverage of the input space. The output parameters measured are the maximum leakage, peak clamped voltage, residual voltage after clamp turn off, and area. The simulations are run at the worst case

condition for the specific output parameter. For example, simulations to determine the maximum leakage are run at fast process corner, maximum voltage, and high temperature. Similarly, the simulation to determine the peak ESD clamp voltage and residual voltages are run at their respective worst case corners. The area is estimated using parametric equations shown earlier in Table 1 and the sampled input parameter values. Process specific information such as capacitor density, resistor sheet resistance, maximum length of resistor, length of drain and source regions etc. are used to calculate the estimated area. Output specification limits of 1.8V for the peak clamp voltage during the ESD event, 1.3V for the residual voltage, and 5μA for the leakage current are used to identify robust designs. These limits are close to the specifications of the obtained design shown in Table 2.

From the 250,000 designs that were sampled, 42,031 designs met the leakage specification, and 38,467 designs met the ESD performance specifications. Eight designs met both the leakage and ESD performance specifications. The parameters of these eight designs that met all the specifications are shown in Table 4. The maximum leakage, ESD performance parameters and area estimates for these designs are also given. Among the eight designs, design #6 yielded the lowest area design with an estimated area of 1281 μm^2. In contrast, the area estimate for the design in Table 2 is only 942 μm^2. Even though the generated designs meet all the specifications, the generated designs are at least 36% bigger. From these results, we infer that the presented design methodology is very effective at obtaining an optimum design.

Table 3 Design Space for Uniform Sampling

Input Parameters	Minimum	Maximum

R	300 kΩ	1300 kΩ
C	0.1 pF	2.9 pF
W_{MP}	1.5 µm	88 µm
L_{MP}	0.04 µm	1 µm
W_{MN}	10 µm	590 µm
L_{MN}	0.04 µm	4 µm
W_{MNC}	1000 µm	3000 µm
L_{MNC}	0.04 µm	0.5 µm

Table 4 Viable Designs Obtained by Uniformly Sampling the Design Space

#	R (MΩ)	C (pF)	W_{MP} (µm)	L_{MP} (µm)	W_{MN} (µm)	L_{MN} (µm)	W_{MNC} (µm)	L_{MNC} (µm)	V_{clmp} (V)	V_{res} (V)	$I_{leakage}$ (µA)	Area (µm^2)
1	0.829	1.672	31.06	0.326	474.65	0.069	1318	0.062	1.79	1.3	4.924	1287
2	0.887	2.406	46.77	0.142	199.74	0.312	1357	0.071	1.77	0.894	4.995	1538
3	0.476	2.849	52.92	0.26	74.47	1.215	1315	0.068	1.79	1.085	4.848	1685
4	1.116	1.956	56.95	0.501	54.93	0.226	1424	0.072	1.77	0.721	4.821	1346
5	0.801	2.831	58.61	0.596	127.02	0.246	1346	0.064	1.78	0.916	4.852	1695
6	0.628	1.856	37.44	0.509	12.32	3.829	1361	0.065	1.8	1.192	4.896	1281
7	1.098	1.836	40.26	0.375	140.38	0.198	1361	0.068	1.79	0.923	4.767	1298
8	0.834	2.616	47.20	0.519	11.76	3.63	1360	0.066	1.79	0.195	4.876	1587

The proposed design methodology and verification strategy was also employed for core clamps in 65 nm and 28 nm technologies. The results corresponding to these technology nodes are summarized in Table 5 and Table 6. In these technologies also, the design resulting from following the proposed methodology was the most optimum compared to an exhaustive blind search in the design space. In 28 nm, the design used a PMOS clamping device since the PMOS offered a better FOM than the NMOS device. In the PMOS clamping device based design, the R and C element positions are reversed

from the NMOS clamping based design to maintain similar functionality and the inverter is designed for trip-point ≤ 0.4VDD.

Table 5 Summary of Results from Clamp Design in 65 nm Technology

<table>
<tr><td>Technology</td><td>65 nm (low power)</td></tr>
<tr><td>Target clamp voltage</td><td>≤ 2.0 V</td></tr>
<tr><td>Target residual voltage</td><td>≤ 1.29 V</td></tr>
<tr><td>Target leakage</td><td>≤ 5 μA</td></tr>
<tr><td>PVT corners for analysis</td><td>Process (MOS): typical, slow, fast, snfp, fnsp
Process (Resistor): low, mid, high
Supply voltage: 1.08 V to 1.29 V, 1.2 V nominal
Temperature: -40 C to 125 C, 25 C nominal</td></tr>
<tr><td>Design obtained from proposed methodology</td><td><table>
<tr><td>Design Parameter</td><td>Value</td></tr>
<tr><td>R</td><td>1280 kΩ</td></tr>
<tr><td>C</td><td>1.18 pF</td></tr>
<tr><td>W_{MP}</td><td>30 μm</td></tr>
<tr><td>L_{MP}</td><td>0.12 μm</td></tr>
<tr><td>W_{MN}</td><td>3 μm</td></tr>
<tr><td>L_{MN}</td><td>0.12 μm</td></tr>
<tr><td>W_{MNC}</td><td>1720 μm</td></tr>
<tr><td>L_{MNC}</td><td>0.15 μm</td></tr>
</table></td></tr>
<tr><td>Estimated area of design</td><td>1572 μm^2</td></tr>
<tr><td>Sampling design space for verification</td><td><table>
<tr><td>Input Parameters</td><td>Minimum</td><td>Maximum</td></tr>
<tr><td>R</td><td>300 kΩ</td><td>1300 kΩ</td></tr>
<tr><td>C</td><td>0.1 pF</td><td>3.0 pF</td></tr>
<tr><td>W_{MP}</td><td>3 μm</td><td>180 μm</td></tr>
<tr><td>L_{MP}</td><td>0.06 μm</td><td>1 μm</td></tr>
<tr><td>W_{MN}</td><td>3 μm</td><td>180 μm</td></tr>
<tr><td>L_{MN}</td><td>0.06 μm</td><td>4 μm</td></tr>
</table></td></tr>
</table>

W_{MNC}	1000 µm	3000 µm
L_{MNC}	0.06 µm	0.5 µm

No. of sample points	250,000
No. of designs that met ESD specifications	43,547
No. of designs that met leakage specifications	155,560
No. of designs that met all specifications	4934

Top three designs obtained from sampling design space

#	R (MΩ)	C (pF)	W_{MP} (µm)	L_{MP} (µm)	W_{MN} (µm)	L_{MN} (µm)	W_{MNC} (µm)	L_{MNC} (µm)	V_{clmp} (V)	V_{res} (V)	$I_{leakage}$ (µA)	Area (µm^2)
1	1.05	1.31	108.2	0.2	5.2	3.9	1749.3	0.16	1.95	0.00	4.70	1729.41
2	0.88	0.64	61.0	0.4	7.9	3.4	2258.5	0.18	1.89	0.00	4.50	1770.85
3	0.72	1.29	122.5	0.2	3.3	0.9	1918.8	0.16	1.84	0.00	4.86	1778.02

Area savings from using proposed methodology	10%

Table 6 Summary of Results from Clamp Design in 28 nm Technology

Technology	28 nm
Target clamp voltage	≤ 1.5 V
Target residual voltage	≤ 1.05 V
Target leakage	≤ 5 µA
PVT corners for analysis	Process (MOS): typical, slow, fast, snfp, fnsp Process (Resistor): low, mid, high Supply voltage: 0.81 V to 1.05 V, 0.9 V nominal Temperature: -40 C to 125 C, 25 C nominal
Design obtained from proposed methodology	

Design Parameter	Value
R	765 kΩ
C	1.41 pF
W_{MP}	3 µm

L_{MP}	0.12 µm
W_{MN}	21 µm
L_{MN}	0.08 µm
W_{MC}	1488 µm
L_{MC}	0.09 µm

Estimated area of design 941 μm^2

Sampling design space for verification

Input Parameters	Minimum	Maximum
R	300 kΩ	1300 kΩ
C	0.1 pF	3.0 pF
W_{MP}	3 µm	180 µm
L_{MP}	0.03 µm	1 µm
W_{MN}	3 µm	180 µm
L_{MN}	0.03 µm	4 µm
W_{MC}	1000 µm	3000 µm
L_{MC}	0.03 µm	0.5 µm

No. of sample points	250,000
No. of designs that met ESD specifications	28,902
No. of designs that met leakage specifications	154,681
No. of designs that met all specifications	3185

Top three designs obtained from sampling design space

#	R (MΩ)	C (pF)	W_{MP} (µm)	L_{MP} (µm)	W_{MN} (µm)	L_{MN} (µm)	W_{MNC} (µm)	L_{MNC} (µm)	V_{clmp} (V)	V_{res} (V)	$I_{leakage}$ (µA)	Area (μm^2)
1	0.46	0.76	4.3	0.7	46.9	0.5	2087.1	0.48	1.40	0.00	4.60	1003.14
2	0.73	0.93	33.0	0.4	21.0	0.5	1783.2	0.50	1.49	0.00	4.98	1022.96
3	0.84	0.92	16.1	0.4	14.5	0.2	1674.9	0.19	1.49	0.00	4.64	1026.25

Area savings from using proposed methodology 7%

Chapter Summary

In this chapter, a design method for the RC and single-inverter-based circuit that yields robust rail clamp circuits was detailed. The presented method only requires the designer to specify the target clamp and residual voltages. After these are specified, the design process does not require any more designer effort or intuition. The various simulations like determining the I_{DSAT} and I_{DOFF} data for different gate lengths at operating voltage and targeted clamp voltage conditions, determining the gate capacitance, and simulations for time constant sizing can be automated using simple scripts. The simulation results can be read using parsing utilities available in all popular programming languages. Sizing the different elements after the simulations are run and the results are parsed is straightforward and only involves writing some 'if-then' type statements. A robust rail clamp circuit can be generated with no designer intervention and less than 50 short simulations (including the corner cases) in a few minutes. The effectiveness of the design methodology was shown in three different technology nodes – 65 nm, 40 nm and 28 nm. The methodology can also be readily applied to the more recent FINFET based technologies.

CHAPTER 4

COMPARATOR-BASED RAIL CLAMP

The traditional RC and inverter-based rail clamp shown in Figure 6 is realized in the described 40 nm process and will be treated as the baseline design for comparison when the comparator-based clamp is introduced later. Several factors necessitate a large time constant circuit in the traditional architecture. One reason is the need to keep the clamp conducting for long enough to dissipate the energy in the ESD event to safe levels. Also, process variations cause deviations in the values of R, C, and the trip point of the inverter from their nominal values. To account for changes caused by process variation, the nominal values of R and C components must be sized up to keep the clamp on long enough at all process corners. In our baseline realization, the nominal values for R and C are 900 kΩ, and 1.4 pF, respectively. These components are realized as poly resistors and metal-oxide-metal capacitor in layout. The clamping transistor MNC has a total width of 1600 μm, and 0.1 μm length. A device of this size enables the voltage between the rails to be clamped at roughly 1.8 V for a 2 kV Human Body Model (HBM) ESD event. The clamp stays conducting for anywhere between 1.2 μs and 1.6 μs before deactivating. It is important to keep the clamp on long enough to limit the residual voltage on the rail to less than the maximum rated device voltage, especially for low-power processes [34].

The on-time of the traditional rail clamp, t_{on}, can be estimated by using the first order charging characteristics of the rc node as

$$t_{on} = -RC \ln\left(1 - \frac{V_{trip}}{V_{DD}}\right) \qquad (1)$$

where R, C are the values of resistor and capacitor used to realize the time constant, V_{trip} is the trip point of the inverter and V_{DD} is the supply voltage.

Using the exponential discharge characteristics of the HBM event [1], it can be shown that the clamp needs to stay conducting for at least 1.1 μs during the ESD event to limit the residual voltage on the rail to below 1.26 V. Using equation (1) and assuming a minimum trip point of $0.65V_{DD}$ for the inverter, we can compute the time constant value to be 1.05 μs. To account for process variations in the values of *R*, *C*, the time constant for the baseline circuit is increased roughly 20% from this value to 1.26 μs. Simulations are then used to confirm and fine tune the baseline design.

Concept

If we are able set the trip-point or threshold of the inverter to a very accurate value over all PVT conditions, we can save in time constant area from not having to oversize the R and C elements to account for process variation. Moreover, if this trip point was fixed at a high value like 80% V_{DD} over all corners, we would be able to extract a constant large delay value before deactivating the clamp. From equation (1), we see that if the trip point is increased from 65% V_{DD} to 80% V_{DD}, the on-time increases from 1.05*RC* to 1.6*RC*. A higher trip point enables us to retain the same on-time with a smaller time constant. With this higher trip point, the time constant can be reduced almost 35% of the baseline value. Also, during ESD event dissipation, the voltage on the rail is dissipated quickly in the first 300 ns to 400 ns following the event, but the clamp needs to remain on for much longer to limit the residual voltage when the clamp deactivates. Thus, if we were to use a circuit block to turn off the clamp so that it would require a minimum voltage for operation, we would only need to size the time constant long enough for the voltage on the rail to dissipate below this minimum operating voltage. This would enable the time constant value to be in the 300 ns to 400 ns range. After V_{DD} falls below this

minimum voltage, the clamp pre-charged to the active state would stay on and dissipate the entire event.

In this work, the circuit block used to achieve the above functions is a simple differential amplifier used as a comparator. This idea is shown as a simplified block diagram in Figure 22.

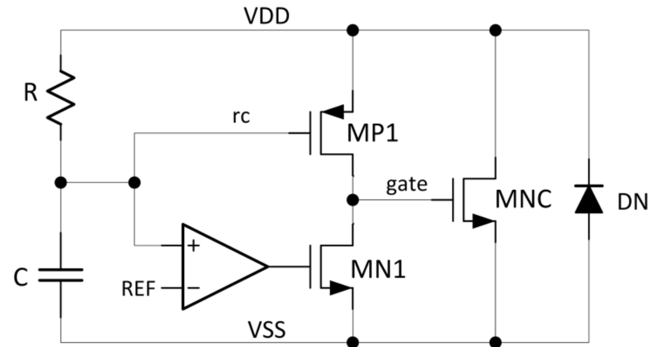

Figure 22 Block Diagram of the Comparator-based Rail Clamp

The static power dissipation resulting from an always-on comparator and reference generator can be solved by selectively switching on the comparator only after the clamp has been activated during the ESD event. During normal powered-up operation when the clamp is dormant, the reference-voltage generator and comparator are switched off to save power.

Circuit Schematic and Design

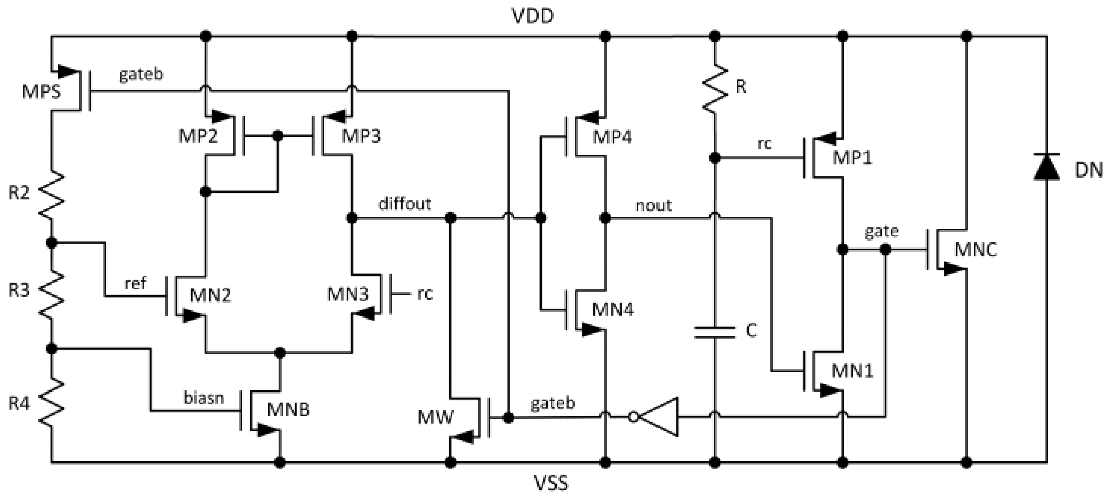

Figure 23 Full Schematic of the Comparator-based Rail Clamp

The full circuit schematic with the comparator is shown in Figure 23. MNC is sized such that the clamped voltage on the VDD rail is less than 1.8V during the ESD event. HBM specifications model the ESD event with rise times from 2-10 ns. Therefore, MP1 is sized to turn on MNC within 1 ns. Transistors MP1 and MNC in the new clamp are the same size as in the baseline design. The clamp on-time is no longer sensitive to the ratio of MP1 and MN1 sizes, as the clamp's on-time is now set by the comparator. This change allows transistor MN1 to be sized up from the baseline design, to reliably hold the gate node low during normal powered-up operation. In this design, MN1 was sized such that its saturation current, I_{DSAT}, was half that of MP1. Diode DN which turns on during a negative ESD transient on the VDD rail with respect to VSS is retained with the same size as the baseline design and is sized to yield a diode resistance less than 1.5 Ω. The R and C component values in this circuit are 600 kΩ and 600 fF, respectively. The resistor and capacitor are realized using poly resistors and metal-oxide-metal capacitor in layout, respectively. Based on discussion in section "Concept", we started

with a time constant value of 400 ns and used simulations to fine tune this value. Since predicting the bandwidth of the comparator as a function of supply voltage is difficult to do with hand calculations, we have relied on simulations to take advantage of this effect.

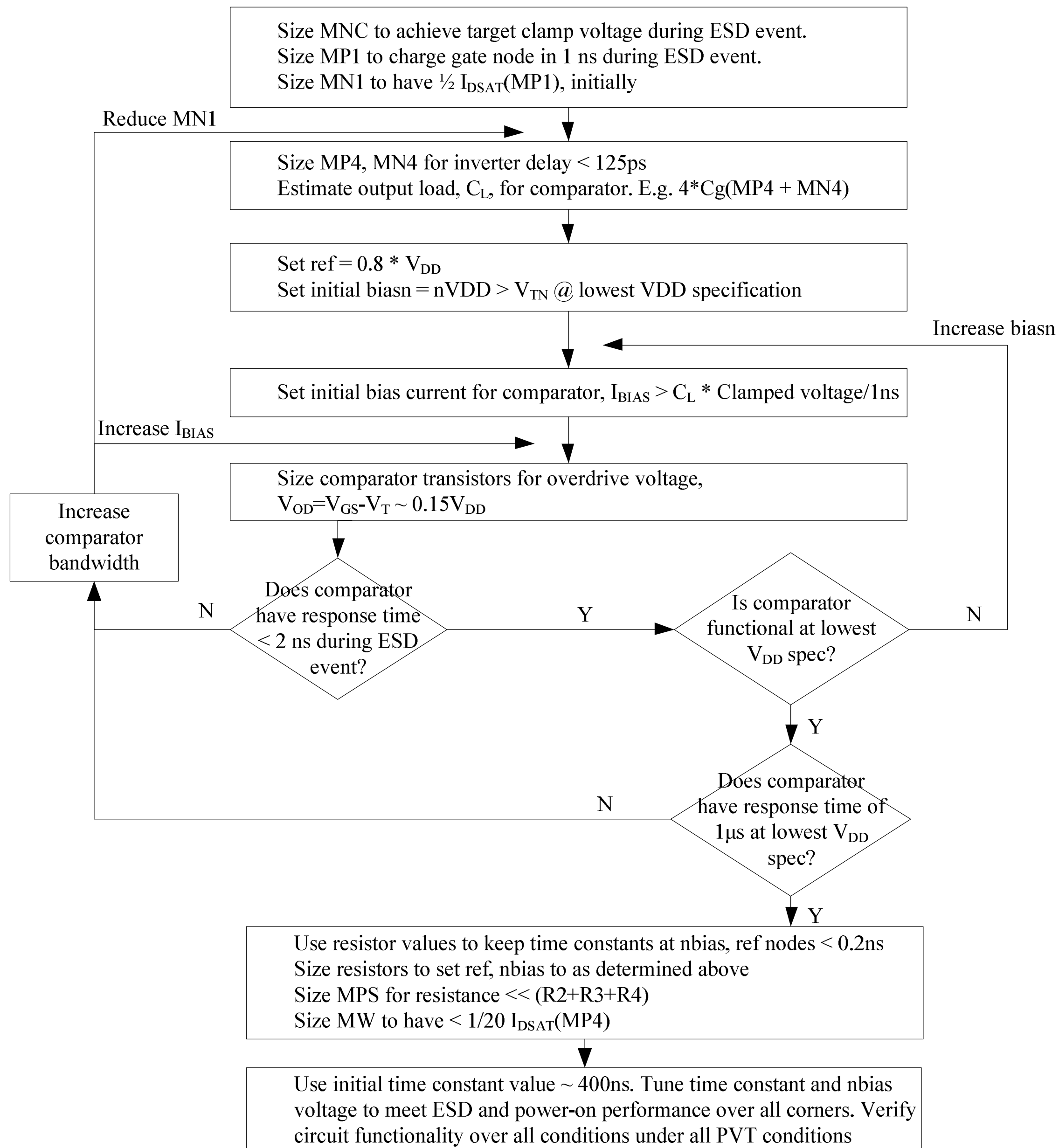

Figure 24 Procedure Followed to Design the Comparator-based Rail Clamp

The comparator circuit is built by cascading a differential amplifier and an inverter. Since the reference voltage is close to the power rail, NMOS input transistors

are preferred to ensure enough headroom for all the transistors. Input transistors MN2 and MN3, and load transistors MP2 and MP3 are matched using interdigitated layout. The reference voltage is generated using a simple resistor divider. In our design, R2, R3, and R4 are realized using poly resistors and their values are in the ratio 2:4:4 to generate a reference voltage, *ref*, equal to 80% VDD, and a bias voltage, biasn, equal to 40% VDD. Using a switch, MPS, the resistor divider is activated only when the clamp is conducting. The comparator is activated by tapping off the resistor string and using transistor MNB as the tail current sink. MW is a very weak transistor that can be easily overdriven by the differential stage preceding it, and is used to ensure that *nout* stays high during normal chip operation, when the comparator is shut off.

To arrive at the specifications for the comparator, we note that its requirements are to drive nout low during the ESD event, and drive nout high if mis-triggered during or after power-up. Power-up times are usually much slower than ESD events. Therefore, for design, the more constraining case is usually designing the comparator to be responsive during the ESD event. To be sufficiently fast, we aim for a comparator response time of 1 ns. This design is not difficult since the load that the comparator drives is only from associated line metal and parasitic capacitances of the transistors. For instance, in our design, the capacitance at nout is only 125 fF, approximately. Moreover, ESD tests are run only at room temperature and the rail voltage is elevated above normal operating voltage during the ESD event. These factors also help simplify design effort. The inverter devices MP4, and MN4 are sized for I_{DSAT} to achieve a delay of approximately 125 ps. Since the comparator operates in the large signal regime, its speed is limited by the slew rate of the diff-amp which can be approximated by I_{SS}/C_L, where I_{SS} is the bias current set

in transistor MNB, and C_L is the capacitance at the diffout node. For design, we estimated the input cap at the input of the inverter (MP4, MN4) and used four times this value as an initial estimate. The final design has ~150 fF capacitance on the diffout node. The comparator is then designed to have a bias current to meet the slew rate requirement at all corners (I_{BIAS} > 150 fF*(1.8V/1 ns) = 250 μA in our design). The resistor chain is sized to yield ref=0.8VDD and biasn=0.4VDD. The bias voltage, biasn, is chosen to sufficiently over-drive the MNB transistor at the lowest operating supply voltage. The nominal threshold voltage values for the core PMOS and NMOS transistors in this process are 0.38V and 0.35V, respectively. The biasn voltage also determines to first order what the lowest operating voltage for the comparator will be. A higher VDD ratio chosen for this net will allow the comparator to operate at lower supply voltages. The net capacitance on the ref and biasn nodes is only due to metal and transistors and approximately 20 fF in our design. The absolute value of resistors used in the resistor chain can be in the order of a few kΩ to ensure that these nodes respond quickly to changes in VDD. The procedure followed to design the rail clamp circuit is shown in Figure 24.

ESD Operation

The clamp activation behavior is similar to that of the traditional circuit. Immediately after the ESD event, the *rc* node stays low, turning on the PMOS transistor, MP1, and activating the clamping transistor MNC. By keeping the turn-on action similar to the traditional single-inverter-based rail clamp, we are able to retain its quick turn-on characteristics. After the *gate* node has been driven high, and the clamp switched on, the resistor-string reference-generator and comparator are activated, and the comparator drives *nout* low.

One noteworthy advantage of this clamp architecture is that with proper design the ESD event can be dissipated completely. This is unlike the traditional circuit, which leaves a residual voltage on the rail after the clamp deactivates. This behavior is achieved because the comparator circuit needs a certain minimum VDD voltage to function. After the clamp turns on during the ESD event, the time constant only needs to ensure the clamp stays on long enough to bring the VDD voltage below this minimum voltage. As the VDD voltage falls, the comparator bandwidth decreases, and it is not able to respond quickly to input changes. Eventually, as VDD voltage falls further, the comparator circuit runs out of headroom, and is unable to drive high even if voltage at the *rc* node is higher than the reference voltage and sufficient time is given to resolve the inputs. This results in the clamp staying on for an extended period, fully discharging the ESD event.

Normal Powered-up Operation

As the power supply ramps up, for ramp times much slower than the RC time constant, the *rc* node closely follows VDD and keeps MP1 off. The *gate* node starts low and as VDD ramps up, *gateb* is driven high which pulls *diffout* low and *nout* high, so that MN1 drives the *gate* node low, to keep MNC in the off state. We show later that even if the clamp were triggered during power-up, it would recover within one microsecond.

Area Savings

The RC time constant in the new circuit is only 360 ns whereas a time constant of 1.26 μs was required for the traditional design. There is some additional area overhead in the new design for the comparator and reference generator. In this process technology, using poly resistors and metal-oxide-metal capacitors, the 1.26 μs time constant with the single-stage inverter was realized in 890 μm^2. The trigger circuit for the new circuit along

with the additional comparator logic can be realized in 720 μm^2 area. Even with the additional overhead of the comparator and logic circuit, an area saving of approximately 20% in the trigger circuit is possible with the new design. The layout of the proposed clamp identifying the important circuit components is shown in Figure 25.

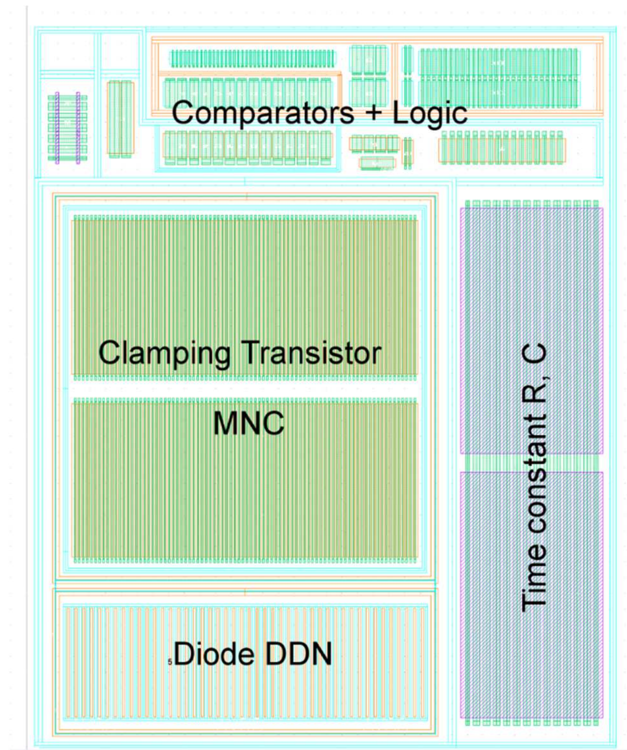

Figure 25 Layout of the Comparator-based Rail Clamp

The clamping transistor MNC is operated in the linear mode during ESD events and so the drain regions of this device do not have to be silicide-blocked for current ballasting.

Performance Comparison – Simulation Results

We compare the performance of the new design with the popular prior-art circuit. The factors considered are ESD performance, fastest power supply ramp rate that can be supported, power supply noise immunity, and immunity to mis-trigger. We show that the new design outperforms or matches the traditional topology in all these cases. All the

results presented in this section are based on layout-extracted simulations and have been simulated over all process corners and, if applicable, voltage and temperature corners as well.

ESD Performance

The HBM model simulates the ESD event by allowing a 100 pF capacitor with an initial voltage equal to the specification limit to discharge between two pins on the die in series with a 1500 Ω resistor. This setup was shown earlier in Figure 12.

The response to a 2 kV HBM event for the comparator-based and baseline clamps over all process corners is shown in Figure 26.

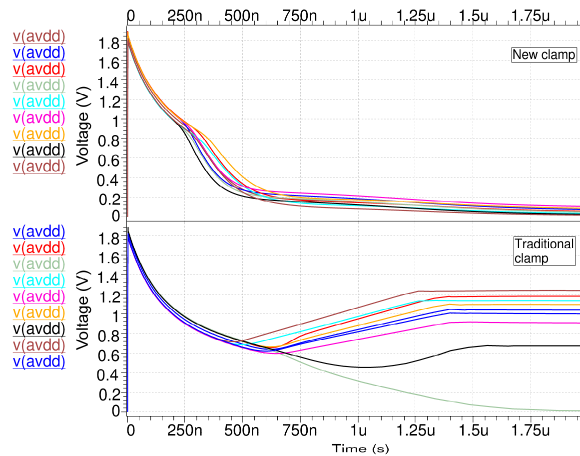

Figure 26 2 kV HBM ESD Response for the Comparator-based Clamp and Traditional Clamp over All Process Corners. The peak clamped voltages are similar but the comparator-based design enables more complete event discharge.

Since ESD tests are run at room temperature, these simulations were run only at 25 C. We see that the clamp peak performance is similar for the two cases but the new clamp architecture leads to more complete ESD event discharge, as explained earlier.

Supply Ramp Rate

Fast-ramping power supplies can trigger the rail clamp because the circuit is unable to distinguish between fast power-on events and ESD events. To find the fastest ramp time that can be supported by the clamps, we ramp up the supply at different ramp times and measure the current drawn from the power supply. Figure 27 shows the power supply current drawn for the worst case corner (maximum current draw) for different supply ramp times for the new and traditional clamps.

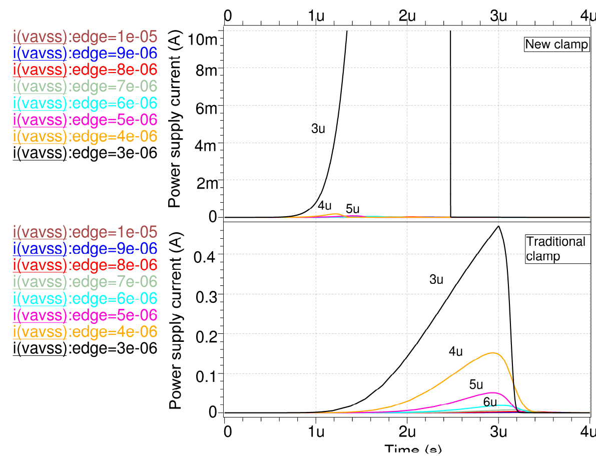

Figure 27 Power Supply Current as a Function of Power Ramp Time for the Comparator-Based Clamp (Worst Case Corner).

For fast power-on ramp times, the clamps turn on, indicated by the increased power supply current. For slower power-on times, the clamps remain switched off and consume little current. If the peak current draw is below 2 mA, we conclude that the ramp rate is safe to apply. From Figure 27, we conclude that a ramp time of 4 μs for the new clamp, and 7 μs for the baseline clamp are acceptable limits. The new clamp supports faster ramp time applications and this is attributed to the reduced time constant in the new clamp. We also see that transition window going from the ESD regime to the power-up

regime [18] is much smaller for the new clamp. The transition window is less than one microsecond for the new clamp, but around 4 μs wide for the traditional clamp.

Supply Noise Immunity

Supply noise immunity of the clamps was investigated by superimposing a pseudo random bit stream (PRBS) on the VDD and VSS rails. This method has been suggested in [28]. The characteristics of the PRBS used were an amplitude of 15% VDD, 200 ps edge, and 500 MHz frequency. From Figure 28, we see that the peak currents are approximately 6.5 mA for the typical corner. Over all corners, the peak currents can be as high as 7.3 mA. These currents are much smaller than the peak switching currents that would be required to cause such large voltage overshoots on the rails [28]. The magnitude of these currents in the baseline clamp was also very similar.

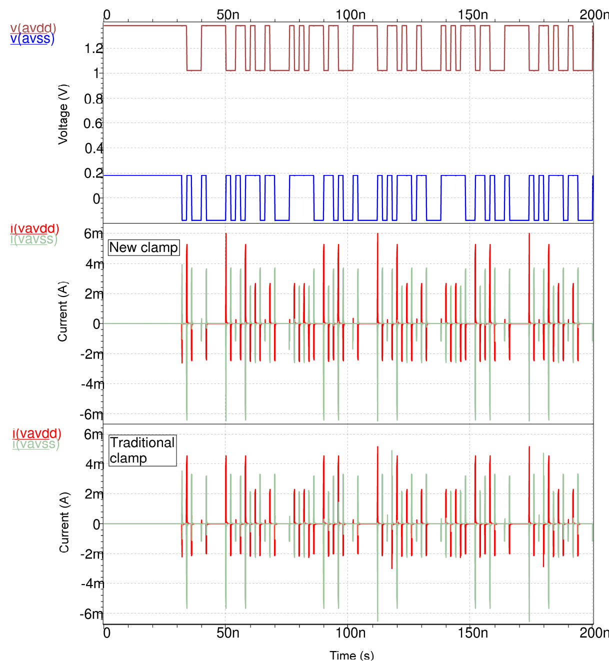

Figure 28 Supply Noise Immunity of the Comparator-based Clamp at Nominal Conditions.

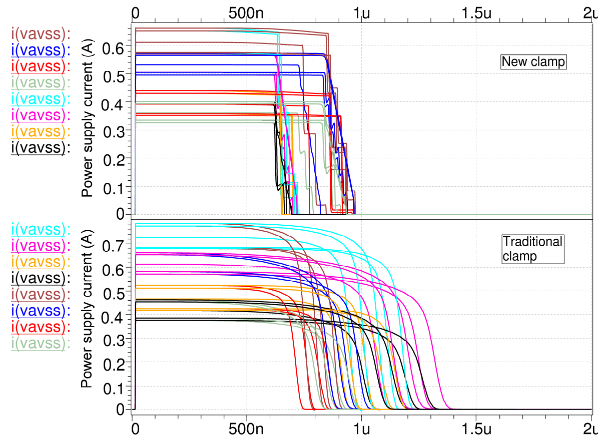

Figure 29 Recovery Times for the Comparator-based Clamp and the Baseline Clamp over All PVT Corners.

Mis-trigger Immunity and Clamp Recovery Time

To study the risk of the clamp staying in a locked-on position, we can artificially trigger the circuit with very fast power-up (5 ns). When the current drawn from the supply dies down, we infer that the clamp has corrected and shut itself off. Figure 29 shows the current draw for this scenario over all corners. We see that the new clamp shuts itself off between 650 ns and 970 ns if mis-triggered. The baseline clamp takes up to 1.4 µs to recover. The quick power-up scenario was simulated with up to 10 Ω series impedance to account for on-die voltage drop which has been shown to increase the risk of latch-on [33]. This increased the maximum shut-off for the new clamp to 1.14 µs but no locked-on risk was found.

Performance Comparison - Experimental Results

A test chip with the proposed clamp circuit was taped-out in 40 nm process. The test-chip also included the traditional RC and single-inverter-based baseline rail clamp.

Both these circuits used identically sized clamping devices (MNC) to clamp between the rails.

Transmission Line Pulse Test Results

Transmission line pulse (TLP) testing using 100 ns wide pulses was performed on both the new and baseline rail clamps. The new clamp showed robust ESD performance and failed only at very high ESD stress levels that correspond to 4.5 kV HBM. The baseline clamp with identically sized clamping device also showed similar ESD performance. These TLP results are shown in Figure 30 and Figure 31. Our design target of 2 kV HBM was met with considerable margin.

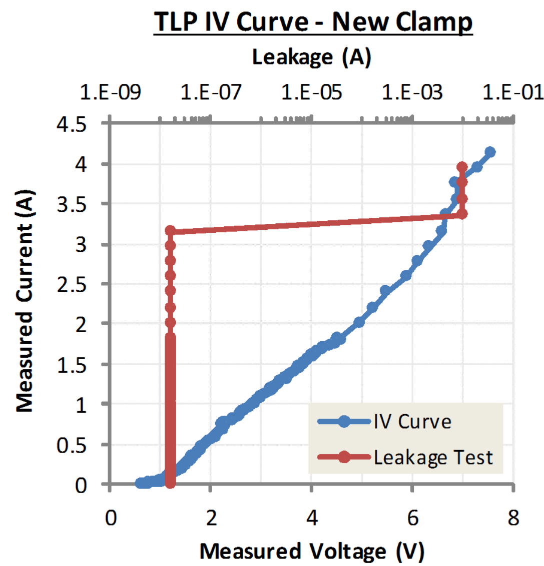

Figure 30 TLP Test Results for the Comparator-based Clamp. The clamp exhibits robust ESD performance.

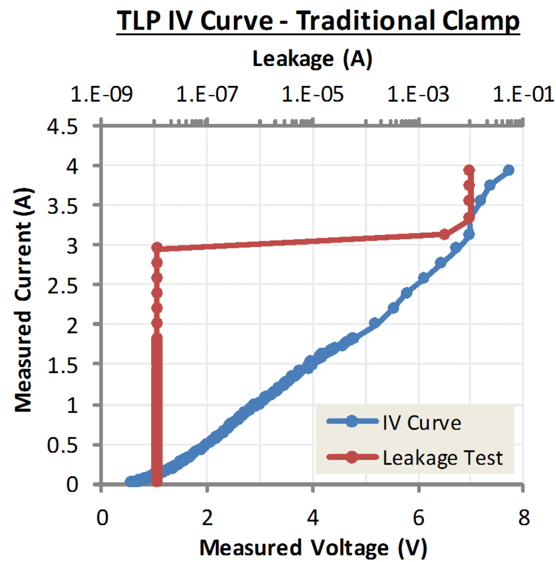

Figure 31 TLP Test Results for the Baseline Clamp. Results are very similar and show good ESD performance.

Leakage Measurements

Measurement results summarized in Table 7 showed marginal leakage difference between the new clamp and the baseline clamp. The average leakage for ten parts measured at 25 C and 1.20 V was 35.5 nA for the new clamp and 26 nA for the baseline design. At 125 C and power supply at 1.26 V (worst case for leakage), the average leakage was 519 nA for the new clamp and 479 nA for the baseline clamp. As expected, the leakage in the new architecture is slightly higher due to the presence of additional circuitry for the comparator and reference generator. The leakage for the new clamp is still low and will be acceptable for most low-power applications. For most product applications, the power supply leakage will be dominated by the digital gates in the core of the chip.

Table 7 Leakage Characteristics of the Comparator-based and Baseline Rail Clamps

Leakage condition	Baseline clamp	New clamp
1.20V, 25C	26.0 nA	35.5 nA
1.26V, 125C	479 nA	519 nA

Mistrigger Immunity, Clamp Recovery Time and Fastest Supply Ramp Rate Supported

To determine the clamp's mistrigger immunity, recovery time in the case of a false trigger, and the fastest power supply ramp that can be supported, we used the test setup shown in Figure 32 [33]. The input signal is applied on the rail through a small series resistance, R1. By probing the voltage waveform at V2 and comparing it with the applied signal (V1), we are able to determine if the clamp is conducting. When the clamp is conducting, the current through the resistor causes a voltage drop across the series resistor, R1, causing V2 to be lower than V1.

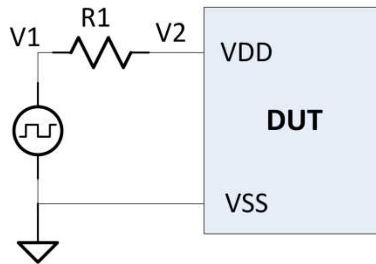

Figure 32 Test Bench Setup to Determine Clamp Recovery Time, Latch-on Immunity, and Fastest Power Ramp that can be Supported.

To gauge the clamp's recovery time and mistrigger immunity, the input signal applied is a power ramp with a sharp 5 ns edge. Figure 33 shows the nominal waveforms measured at node V2 when such an input signal is applied for the new and traditional clamps.

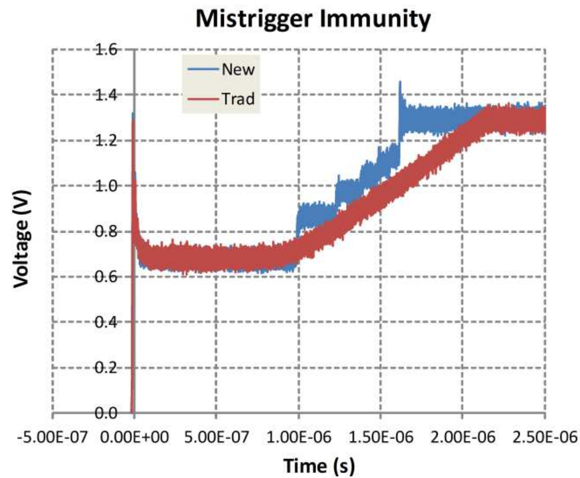

Figure 33 Clamp Recovery Test for the Comparator-based and Baseline Clamps. The comparator-based clamp recovers faster from a mis-trigger event than the traditional clamp.

We see that the new clamp takes about 1.6 μs to recover while the baseline clamp takes 2.2 μs to recover. These values are larger than what was seen in simulation and this was traced to be due to the series resistance in the package and board. Nevertheless, the trend showing quicker mis-trigger recovery for the new clamp is evident.

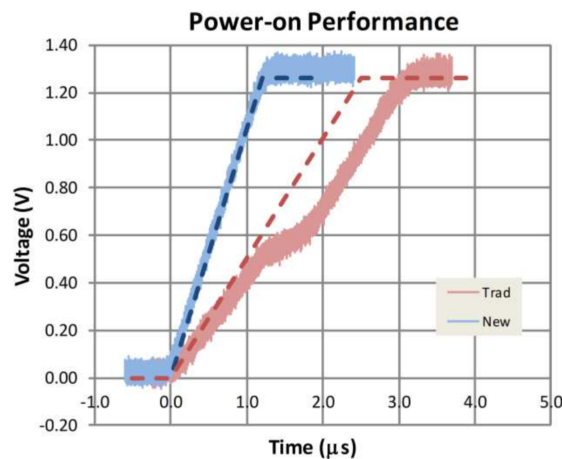

Figure 34 Power-on Behavior of the Comparator-based and Traditional Clamps at Nominal conditions. The new clamp does not turn on for a 1.2 μs power ramp whereas the traditional clamp turns on for a 2.5 μs power ramp.

Figure 34 shows the nominal waveforms during power-up at 25 C for the new and traditional clamps. Both the applied voltage waveforms (dotted lines) and the waveforms probed at node V2 (in Figure 32) are shown. The baseline clamp is seen to turn on for a 2.5 μs power ramp while the new clamp does not turn on for a 1.2 μs power ramp, proving that the new clamp is able to support considerably faster power ramps than the traditional circuit.

A comparison between the baseline clamp and the new clamp is summarized in Table 8. The new clamp matches or outperforms the baseline clamp with only a small leakage penalty.

Table 8 Comparison of the Comparator-based and Baseline Rail Clamps

Parameter	Baseline clamp	New clamp
Trigger circuit area	890 μm^2	720 μm^2
Fastest power-on time supported	7 μs	4 μs
HBM performance	4.5 kV	4.5 kV
Maximum clamp recovery time	1600 ns	970 ns
Worst case leakage	2.209 μA	2.345 μA

Table 9 Comparison of the Comparator-based Rail clamp with Prior Works

	[27]	[17]	[31]	This work
Technology	90 nm	90 nm	65 nm	40 nm
Trigger circuit area	NR	>70% area savings over baseline	> 50% area savings over baseline	720 μm^2 >20% area savings over baseline
Power-on Rep.	1 μs	1 μs (nom)	25 ns (nom)	1 μs (nom)

time	Sim.	400 ns (nom) 1 µs (PVT)	1.5 µs (nom) <u>175 µs (PVT)</u>	25 ns (nom) 50 ns (PVT)	4 µs (PVT)
Recovery time	Rep.	1 µs (nom)	300-500 ns	NR	820 ns (nom) 970 ns (PVT)
	Sim.	1 µs (nom) <u>141 µs (PVT)</u>	500 ns (nom) 702 ns (PVT)	<u>Locked-on</u>	
Leakage	Rep.	NR	NR	NR	71.74 nA (nom) 2.345 µA (PVT)
	Sim.	77.27 nA (nom) 2.455 µA (PVT)	70.75 nA (nom) 2.47 µA (PVT)	65.39 nA (nom) 2.195 µA (PVT)	

NR-not reported, Rep-reported value, Sim-simulation of equivalent design

Table 9 compares the new clamp with some prior works. As pointed out in section “Rail Clamp Architectures” page 11, most prior studies focus on area reduction and publish only nominal values. These numbers have been noted as “nom” in the table. To make a fair comparison, we need to evaluate the architectures within a PVT space. For this purpose, we have implemented the prior work architectures in the said 40 nm process. During design we matched the implemented design’s nominal performance with the reported nominal values. We then simulated these designs over the PVT space to ascertain their worst-case performance. All architectures have the same clamping transistor width and have similar ESD performance. Leakage performance is also similar since the leakage is dominated by the clamping transistor.

Prior architectures are unable to maintain good performance in the entire PVT window. For instance, design [27] suffers from a large recovery time because it relies on leakage through a PMOS device to correct after a mis-trigger event. Design [17] uses weak transistors in the clamp switch-off path. These transistors become very slow across corners as power supplies are ramping up and the gate node of the clamp can couple high

turning-on the clamp at some corners. This limits the fastest power-on ramp that is this architecture is able to support. Design [31] relies on a string of diodes to keep the holding voltage above the power supply. The forward voltage across the diode can vary from 0.3V to 0.7V over the PVT window and this large variation makes the architecture prone to latch-on. In fact our implementation used a diode string of up to four diodes to help alleviate this issue, but the design still was not immune to latch-on.

When the comparison is done over a full PVT window, the presented clamp offers a very competitive circuit and is the only robust design over varying PVT conditions. Evaluating these architectures over industry-standard PVT conditions is necessary since a real-world design is only as good at its performance in the worst case corner.

Chapter Summary

The comparator-based rail clamp offers several advantages compared to the traditional prior art such as 20% area savings in the trigger circuit area, supporting power supply ramp rates that are almost twice as fast, dissipating the ESD energy more cleanly with little residual charge, recovering faster from false triggers and offering comparable supply noise immunity. These claims have been proved using both simulations covering process, voltage, and temperature corners, and through experimental results.

CHAPTER 5

RAIL CLAMP WITH DYNAMIC TIME CONSTANT ADJUSTMENT (DTCA)

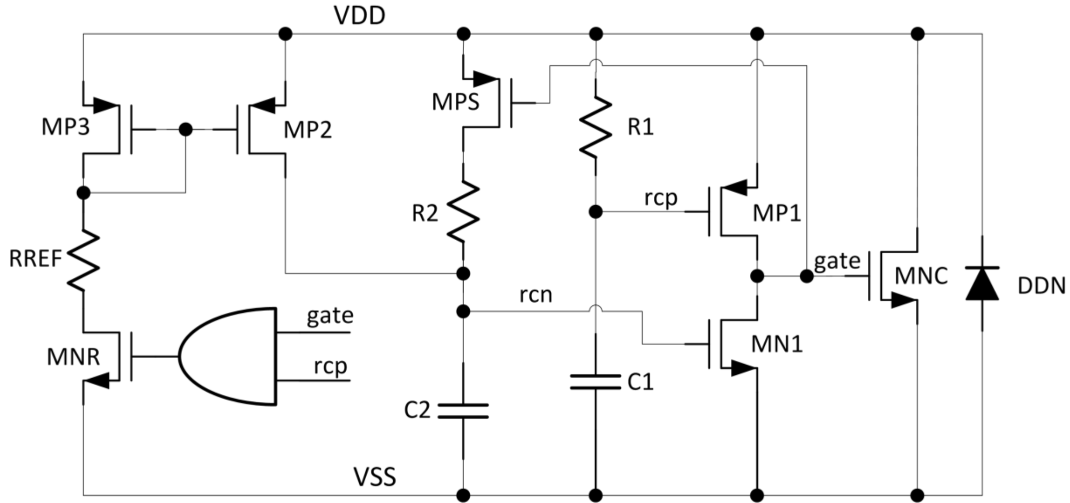

Figure 35 Schematic of the Rail Clamp with Dynamic Time Constant Adjustment (DTCA)

The schematic of the new clamp circuit is shown in Figure 35. The clamping transistor MNC is sized to clamp the voltage between the rails to a target value during the ESD event. In our design, Width/Length (W/L) of MNC is 1600 µm/0.1 µm. The resistor R1, and capacitor C1 comprise the trigger time constant and drive the PMOS transistor MP1 that activates the clamp during the ESD event. In this design, R1 = 100 kΩ and C1 = 320 fF. Note that there is only one transistor, MP1, from the *rcp* node to the gate of MNC, just like the traditional RC and single inverter based clamp. This helps increase the response time of the clamp. The resistor R2 and capacitor C2 comprise another time constant and drive the transistor MN1. In our design, R2 is 50 kΩ and C2 is 640 fF to keep R2C2≈R1C1. Transistors MP2, MP3. and reference resistor (RREF) comprise a current sourcing mirror that connects to the rcn node. Resistors R1, R2, and RREF are realized as poly resistors, and capacitors C1 and C2 are metal-on-metal capacitors. This

implementation is done to limit process variation in these elements. Typical process variation numbers are ±20% for poly resistors and ±10% for metal capacitors. As discussed earlier in prior work (page 11), using MOSFETs as resistors or capacitors can yield variation much higher than these values. Also, an elaborate analysis in [27] has shown that clamp designs with poly resistors are more robust than designs using MOSFETs as resistors. Using MOS resistors has been shown to cause lock-on behavior, and cause large current draw during power-up [27]. Moreover, excessive sensitivity in a slew rate detection circuit built with only MOS devices has been shown to be one of the reasons for the clamp in [18] to lock into an on-position during normal power-up operation [33]. Note that the transistors MP1 and MN1 are driven separately in this design. This is one of the major differences compared to the circuit in [18] where these transistor gates are driven together. As will be explained later, driving the two transistor gates separately allows a much quicker voltage discharge, closer to the ideal exponential voltage behavior. Further, by driving the gates of these transistors independently, we avoid the high-gain region of the inverter which can cause oscillations in some clamp designs [30]. DDN is realized as n-diode (n-diffusion in a p-well) to protect circuitry in the event of a negative ESD strike on VDD with respect to VSS.

ESD Operation

The HBM model simulates the ESD event by allowing a 100 pF capacitor with an initial voltage equal to the specification limit to discharge between two pins on the die in series with a 1500 Ω resistor. This setup was already shown in Figure 12. In the event of a positive ESD strike on the VDD rail, the *rcp* node initially stays low and MP1 switches ON to drive the *gate* node high. The *rcn* node is also low initially and ensures MN1 is

off. When the *gate* node is driven high, the clamping transistor MNC switches ON, dissipating the ESD event. Also, when the *gate* node is driven high, transistor MPS is switched off, effectively increasing the second time constant to a very large value. Switching MPS off disables the current path from VDD to *rcn* through R2. When this happens, *rcn* becomes a high impedance node that is precharged low. Since R1C1≈30 ns, *rcp* quickly catches up to VDD (in tens of ns) after the ESD strike, and deactivates MP1. The *gate* node, now precharged high, is also in a high impedance state, with neither MP1 nor MN1 driving the *gate* node. This keeps the clamping transistor MNC ON, allowing it to actively dissipate the ESD energy. Figure 36 shows the voltages at the various nodes of interest in the rail clamp during a 2 kV Human Body Model (HBM) event. Only the first 300 ns are shown for better clarity.

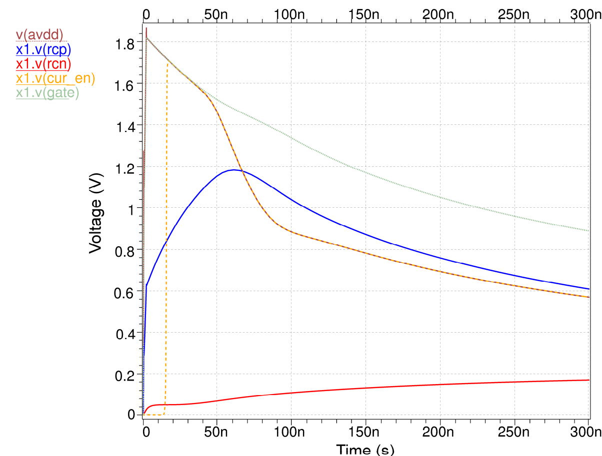

Figure 36 Voltage Waveforms at Various Nodes of Interest in the Rail Clamp with DTCA during the Initial Phase of the 2 kV HBM ESD Event.

To deactivate the clamp, node *rcn* has to charge high; this is done by charging the *rcn* node using the current mirror. The current mirror is activated using an AND gate with inputs *rcp* and *gate*. This ensures that the current mirror is engaged only after *rcp* has

caught up to VDD, and the clamp is engaged. This gate is also used to extract some delay from the trigger time constant, rather than relying on only the current mirror to introduce the required delay before disengaging the clamp. The current mirror is designed to source a nominal current of 500 nA when VDD = 1.2V. The current mirror is operated in the saturation region, and we do not rely on leakage current to charge *rcn*. This is done to get more predictable behavior, since leakage current varies by orders of magnitude over PVT (see Figure 9). To ensure operation in the saturation region while sourcing small currents, transistors MP3 and MP2 have long lengths (8 μm in this design). We can estimate the delay introduced by the 0.5 μA current charging C2, to a threshold voltage (≈0.35V) to be ≈420 ns. This is a rough estimate since the VDD, at the time of the ESD event, is varying and could be below or above 1.2V at the time the mirror is engaged. Also, we get an additional few tens of nanoseconds delay using the AND gate, since the current mirror is not engaged until *rcp* catches up to VDD. Because the *gate* node is precharged high and no longer driven actively to VDD after the initial engagement, the *gate* node continues to stay high, even though the VDD is being discharged. In fact, the gate of MNC stays higher than VDD as the ESD event is discharged. This maintains low clamp resistance as the event progresses. If the gate of MNC is actively driven, the *gate* node tracks VDD, and VDS = VGS for the MNC transistor. Now, since VGS > VDS, the transistor operation is in the linear mode and the clamp voltage falls at a faster rate than with the traditional clamps that drive the gate actively throughout the duration of the ESD event. This advantage with a high impedance gate is also mentioned in [17]. Figure 37 shows the nominal ESD response of the proposed clamp, alongside the ESD response of a traditional clamp that drives the gate node actively throughout the ESD event.

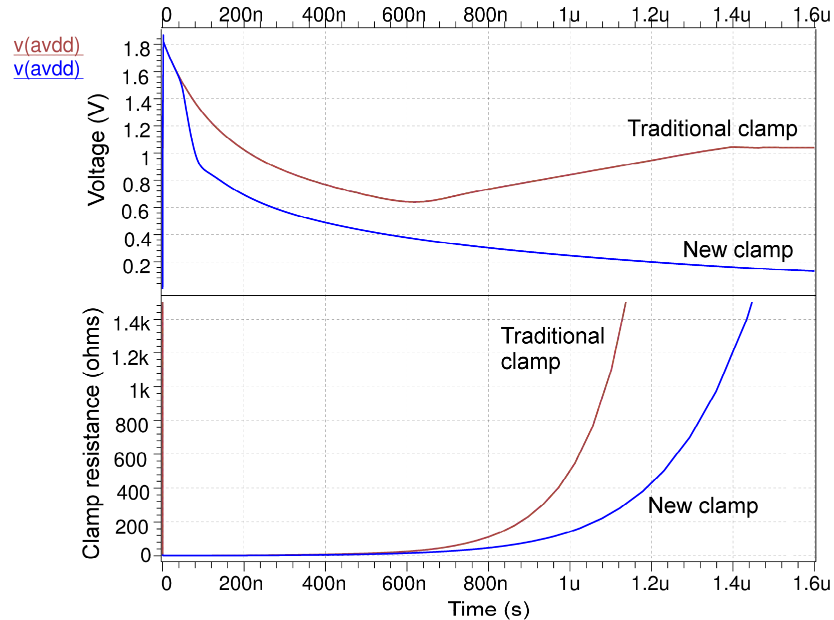

Figure 37 Nominal Response and Large Signal Clamp Resistance during the 2 kV HBM ESD Event for the Rail Clamp with DTCA and the Traditional Clamps.

In this case, the traditional RC and inverter based baseline clamp is used, but the arguments made here will hold for all rail clamp architectures that drive the gates of transistors MP1 and MN1 together throughout the ESD event. We can see that the with the proposed rail clamp the voltage on the VDD rail falls quicker and there is little to no residual voltage on the rail.

Also shown is the clamp resistance in both these architectures as the event progresses. Even though the clamp resistance starts off at the same low value in both these clamps, the clamp resistance increases more rapidly as the event progresses using architectures that drive the gate of the clamping MOSFET throughout the event. As a result of this, the voltage discharge on the VDD rail is not exponential. The voltage on the VDD rail more closely resembles the ideal exponential waveform with the proposed

rail clamp. Also, as VDD decreases, the current, sourced by the current mirror, decreases and prolongs the clamp ON time until the full event is discharged.

Normal Powered-up Operation

During normal power-on (for ramp rates >> R1C1 time constant), *rcp* tracks VDD and ensures that MP1 is not conducting. When VDD voltage goes above the *gate* node by a threshold voltage, MPS conducts and pulls *rcn* to VDD. This turns on MN1 and pulls the *gate* node low, disengaging the clamping transistor MNC fully. Nominal waveforms for a 500 ns power-up case are shown in Figure 38.

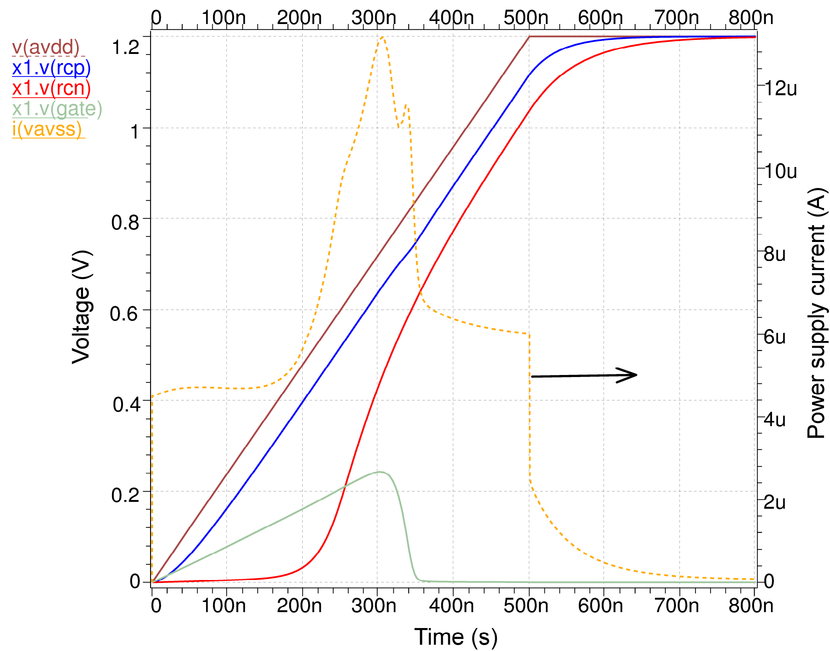

Figure 38 Supply Current and Voltages at Nodes of Interest in the Rail Clamp with DTCA during a 500 ns Power-on Event.

We see that the peak current draw, in this case, is only 14 µA showing that the clamp is not activated, even for such fast ramp time. We will show later that even if the clamp is activated for some reason, the circuit recovers very quickly and turns off the clamp.

Area Savings

Figure 39 shows the layout for the new clamp in the 40 nm CMOS process. The trigger circuit, comprising the resistors, capacitors, current reference, and logic circuitry, occupies roughly 723 μm^2. The baseline single time constant RC (1.2 μs) and inverted-based trigger circuit, using poly resistors and metal capacitors, was realized in 894 μm^2 in this process. From this, we estimate that a trigger circuit area reduction of at least 20% should be possible using the new circuit, compared to the traditional RC and inverter based approach. There is also potential for further area reduction, estimated to be another 20% if the metal caps are placed on higher metal layers and over the MOSFETs. This has not been done in this work since our primary aim in this work was proof-of-concept and robust operation over industry-standard operating conditions rather than area savings.

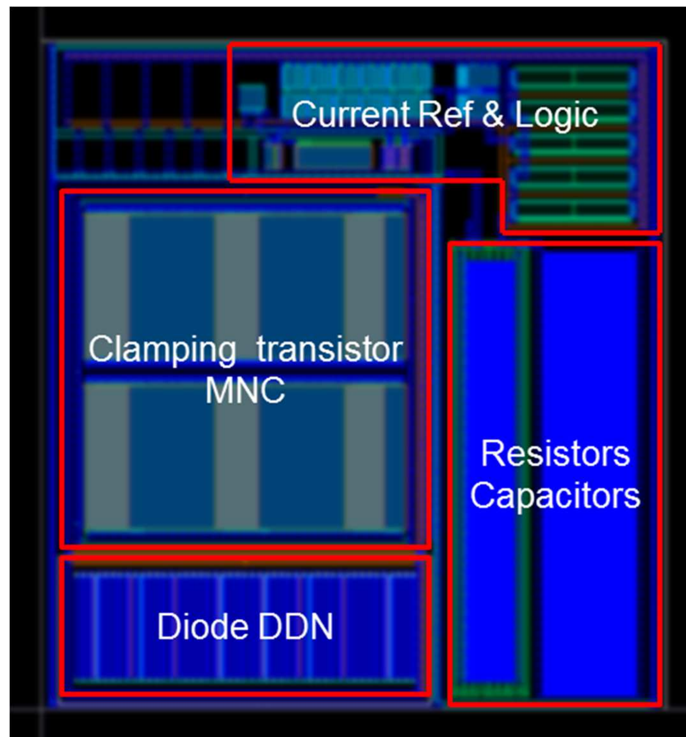

Figure 39 Layout of the Rail Clamp with DTCA

Many prior art rail clamp circuits have used MOSFETs as capacitors and resistors to realize area competitive implementations. But these studies have not elaborated on the process variation or yield concerns that come with such an implementation. In this work, the passive elements are not realized using MOSFETs to keep process variation to a minimum. The fastest power supply ramp that can be supported is limited by the maximum time constant value that may result over process corners. By limiting the process variation, the clamp topology is able to support a faster power supply ramp over all corners. In this study, there is also some area penalty resulting from designing the current mirror circuitry to work in the saturation region. If leakage characteristics of devices are used, these circuits can be realized using less silicon area. From our experience, leakage models between foundries may not be very accurate and so we decided to minimize our risk. These design trade-offs can be made depending on the specific designer use model.

Simulation Results Over PVT Conditions

We compare the performance of the new design with the popular prior-art circuit. The factors considered are ESD performance, fastest power supply ramp rate that can be supported, and clamp recovery time after a false trigger event. We show that the new design outperforms or matches the traditional topology in all these cases. All the results presented in this section are based on layout-extracted simulations and have been simulated over all process corners and, if applicable, voltage and temperature corners as well.

ESD Performance

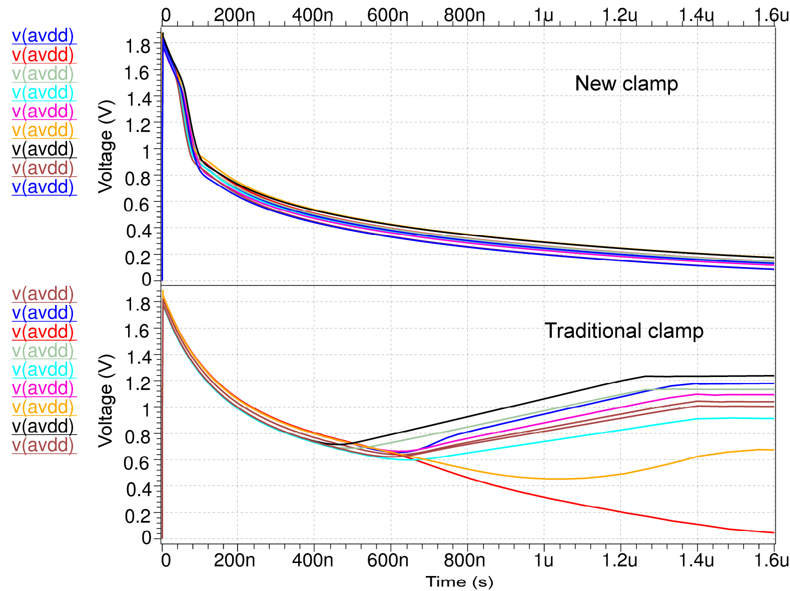

Figure 40 2 kV HBM ESD Response for the Clamp with DTCA and the Traditional Clamp over All Process Corners. The peak clamped voltages are similar but the new design enables more complete event discharge.

The response to a 2 kV HBM event for the new and baseline clamps over all process corners is shown in Figure 40. Since ESD tests are run at room temperature, these simulations were run only at 25 C. We see that the clamp peak performance is similar for the two cases but the new clamp architecture leads to quicker and more complete ESD event discharge, as explained earlier, over all corner cases.

Supply Ramp Rate

Fast-ramping power supplies can trigger the rail clamp because the circuit is unable to distinguish between fast power-on events and ESD events. To find the fastest ramp time that can be supported by the clamp, we ramp up the supply at different ramp times and measure the current drawn from the power supply. Figure 41 shows the power

supply current drawn for the worst case corner (maximum current draw) for different supply ramp times for the new and traditional clamps.

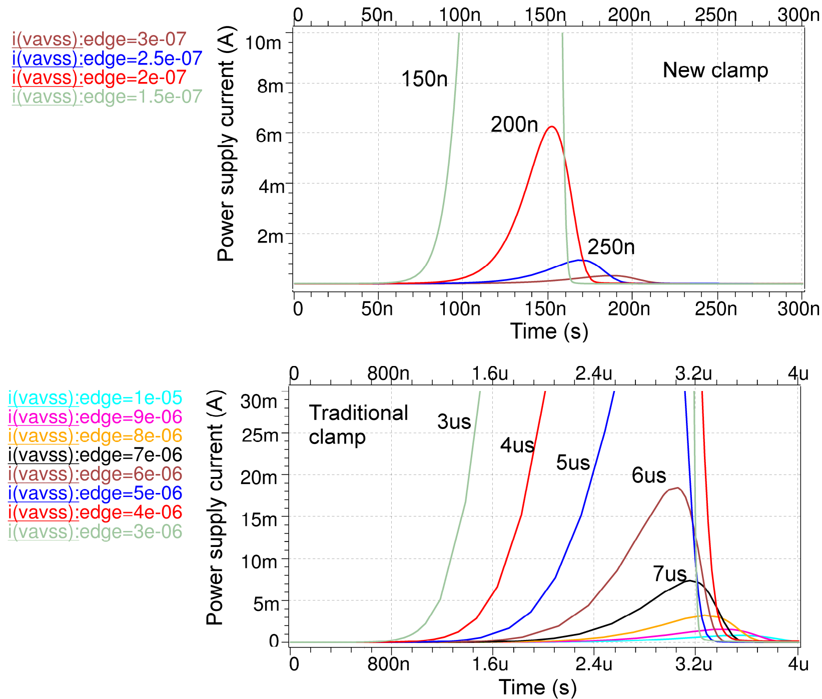

Figure 41 Power Supply Current as a Function of Power-up Time for the Rail Clamp with DTCA and the Baseline Rail Clamp at the Worst Case Corner.

The maximum current draw occurs at the slowN-fastP corner at 125°C. Note that the time scales used are different for the two plots for increased clarity. For fast power-on ramp times, the clamps turn on, indicated by the increased power supply current. For slower power-on times, the clamps remain switched off and consume little current. If the peak current draw is below 10 mA, we conclude that the ramp rate is safe to apply. From Figure 27, we conclude that a ramp time of 200 ns for the new clamp, and 7 µs for the baseline clamp are acceptable limits. The new clamp supports much faster ramp time applications because it uses a small trigger time constant. We also see that transition window going from the ESD regime to the power-up regime [18] is much smaller for the

new clamp. The transition window is less than 50 ns for the new clamp, but around 4 μs wide for the traditional clamp.

Mis-trigger Immunity and Clamp Recovery Time

To study the risk of the clamp staying in a locked-on position, we can artificially trigger the circuit with very fast power-up (5 ns). When the current drawn from the supply dies down, we infer that the clamp has corrected and shut itself off. Figure 42 shows the current draw for this scenario over all corners.

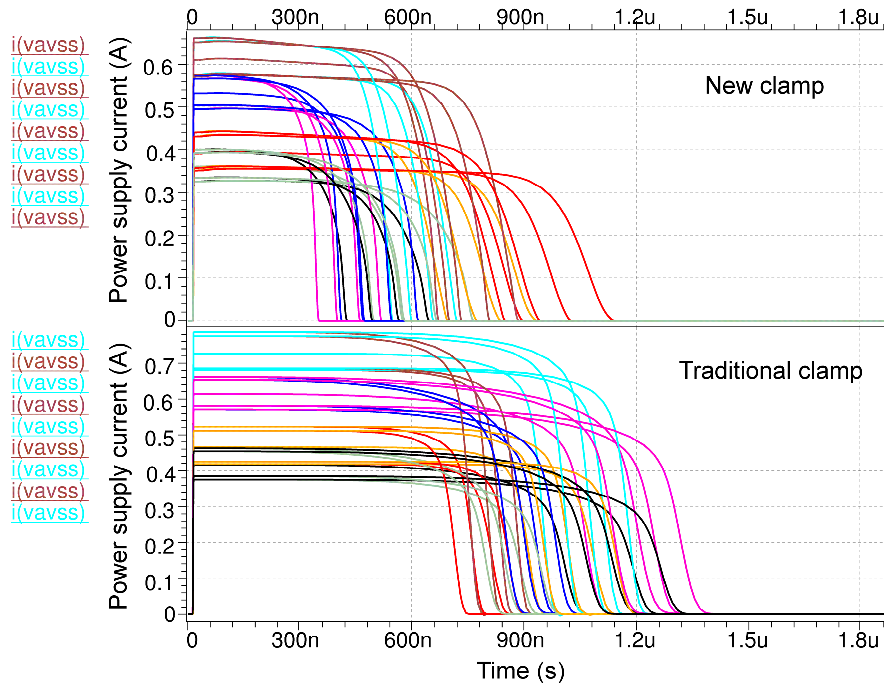

Figure 42 Clamp Recovery Times for the Clamp with DTCA and the Baseline Clamp over All PVT Corners.

We see that the new clamp shuts itself off between 350 ns and 1140 ns when falsely triggered. The baseline clamp takes up to 1.4 μs to recover. The quick power-up scenario was simulated with up to 10 Ω series impedance to account for on-die voltage drop which has been shown to increase the risk of latch-on [33]. Even with a very

conservative 10 Ω series resistance, the voltage drop did not prevent the clamp from recovering. With 10 Ω series resistance, the recovery time ranged from 740 ns to 2.5 µs.

Performance Comparison - Experimental Results

A test chip with the proposed clamp circuit was taped-out in 40 nm process. The test-chip also included the traditional RC and single-inverter-based baseline rail clamp. Both these circuits used identically sized clamping devices (MNC) to clamp between the rails.

Transmission Line Pulse Test Results

Transmission line pulse (TLP) testing using 100 ns wide pulses was performed on both the new and baseline rail clamps. The new clamp showed robust ESD performance and failed only at very high ESD stress levels that correspond to 4.5 kV HBM. The baseline clamp with identically sized clamping device also showed similar ESD performance. These TLP results are shown in Figure 43 and Figure 44. Our design target of 2 kV HBM was met with considerable margin. All the three parts tested for this study yielded the same performance.

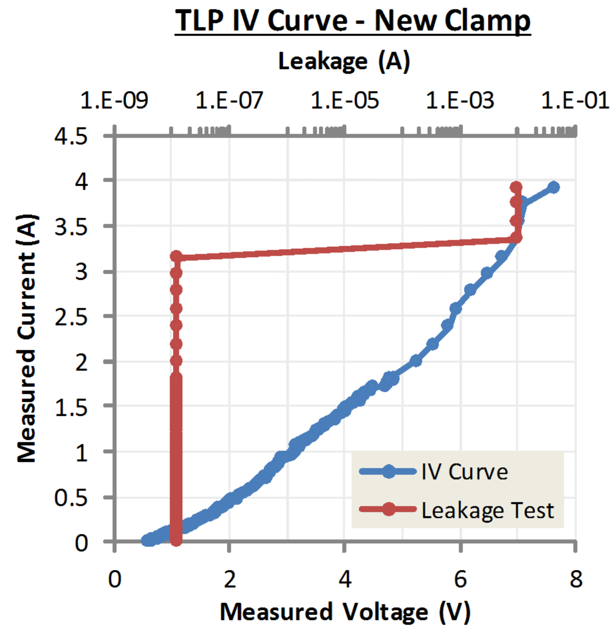

Figure 43 TLP Test Results for the Clamp with DTCA Showing Robust ESD Performance.

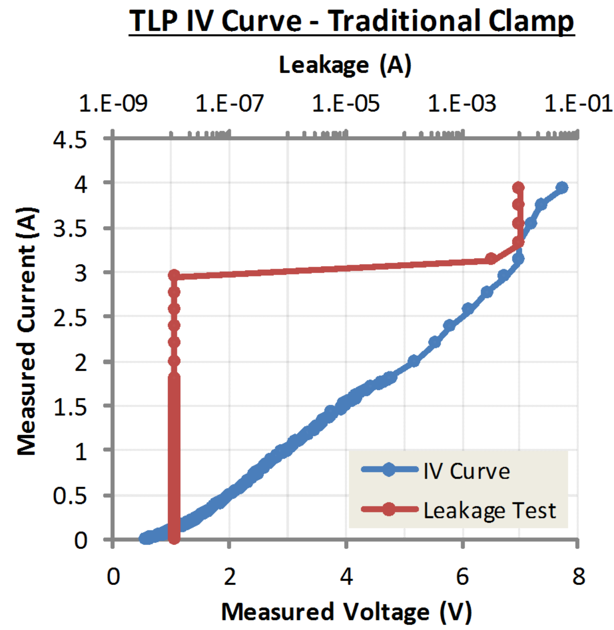

Figure 44 TLP Test Results for the Baseline Clamp

Leakage Measurements

Measurement results summarized in Table 10 showed marginal leakage difference between the new clamp and the baseline clamp.

Table 10 Leakage Characteristics of the Clamp with Dynamic Time Constant Adjustment (DTCA) and the Baseline Clamp

Leakage condition	Baseline clamp	New clamp
1.20V, 25C	26.0 nA	28.7 nA
1.26V, 125C	479 nA	524 nA

The average leakage for ten parts measured at 25 C and 1.20 V was 28.7 nA for the new clamp and 26 nA for the baseline design. At 125 C and power supply at 1.26 V (worst case for leakage), the average leakage was 524 nA for the new clamp and 479 nA for the baseline clamp. As expected, the leakage in the new architecture is slightly higher due to the presence of additional circuitry like the current mirror. The leakage for the new clamp is still low and will be acceptable for most low-power applications. For most product applications, the power supply leakage will be dominated by the digital gates in the core of the chip.

Mistrigger Immunity, Clamp Recovery Time and Fastest Supply Ramp Rate Supported

To determine the clamp's mistrigger immunity, recovery time in the case of a false trigger, and the fastest power supply ramp that can be supported, we used the test setup shown in Figure 32 [33]. The input signal is applied on the rail through a small series resistance, R1. By probing the voltage waveform at V2 and comparing it with the applied signal (V1), we are able to determine if the clamp is conducting. When the clamp

is conducting, the current through the resistor causes a voltage drop across the series resistor, R1, causing V2 to be lower than V1.

To gauge the clamp's recovery time and mistrigger immunity, the input signal applied is a power ramp with a sharp 5 ns edge. Figure 45 shows the nominal waveforms measured at node V2 when such an input signal is applied for the new and traditional clamps.

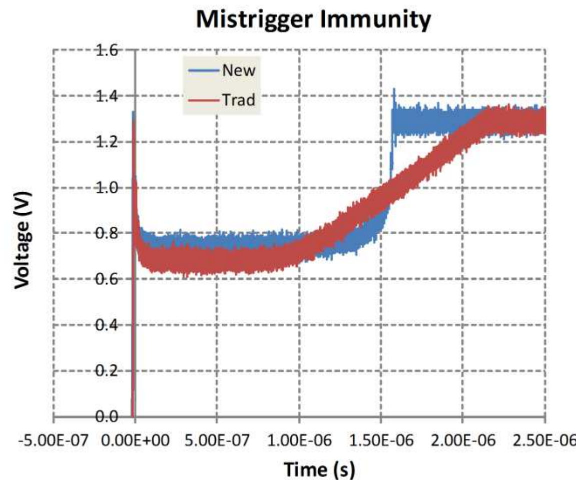

Figure 45 Clamp Recovery Test (node V2) for the Rail Clamp with DTCA and the Baseline Clamp. The new clamp recovers faster from a mis-trigger event than the traditional clamp.

We see that the new clamp takes about 1.6 µs to recover while the baseline clamp takes 2.2 µs to recover. These values are larger than what was seen in simulation for both rail clamps and this was traced to be due to the series resistance in the package and board. Nevertheless, the trend showing quicker false-trigger recovery for the new clamp is evident.

Figure 46 shows the nominal waveforms during power-up at 25 C for the new and traditional clamps. Both the applied voltage waveforms (dotted lines) and the waveforms

probed at node V2 (in Figure 32) are shown. The baseline clamp is seen to turn on for a 2.5 µs power ramp while the new clamp does not turn on even for a 250 ns power ramp, proving that the new clamp is able to support power ramps that are much faster than ramps that can be supported with the traditional circuit.

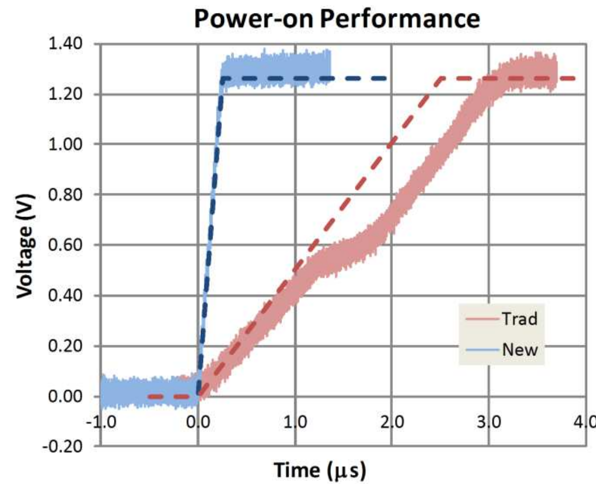

Figure 46 Power-on Behavior (node V2) of the Rail Clamp with DTCA and the Traditional Clamp at Nominal Conditions. The new clamp does not turn on for a 250 ns power ramp whereas the traditional clamp turns on for a 2.5 µs power ramp.

A comparison between the baseline clamp and the new clamp is summarized in Table 11.

Table 11 Comparison of the Rail Clamp with DTCA and the Baseline Clamp

Parameter	Baseline clamp	New clamp
Trigger circuit area	890 μm^2	723 μm^2
Fastest power-on time supported	7 µs	200 ns
HBM performance	4.5 kV	4.5 kV
Maximum clamp recovery time	1600 ns	1140 ns
Worst case leakage	2.21 µA	2.54 µA

The new clamp matches or outperforms the baseline clamp with only a small leakage penalty. Table 12 compares the new clamp with some prior works.

Table 12 Comparison of the Rail Clamp with DTCA with Prior Works

		[27]	[17]	[31]	[25]	This work
Technology		90 nm	90 nm	65 nm	40 nm	40 nm
Trigger circuit area		NR	>70% area savings over baseline	> 50% area savings over baseline	720 μm^2 >20% area savings over baseline	723 μm^2 >20% area savings over baseline
Power-on time	Rep.	1 µs	1 µs (nom)	25 ns (nom)	1 µs (nom) 4 µs (PVT)	50 ns (nom) 200 ns (PVT)
	Sim.	400 ns (nom) 1 µs (PVT)	1.5 µs (nom) 175 µs (PVT)	25 ns (nom) 50 ns (PVT)		
Recovery time	Rep.	1 µs (nom)	300-500 ns	NR	820 ns (nom) 970 ns (PVT)	885 ns (nom) 1140 ns (PVT)
	Sim.	1 µs (nom) 141 µs (PVT)	500 ns (nom) 702 ns (PVT)	Locked-on		
Leakage	Rep.	NR	NR	NR	71.74 nA (nom) 2.345 µA (PVT)	67.77 nA (nom) 2.537 µA (PVT)
	Sim.	77.27 nA (nom) 2.455 µA (PVT)	70.75 nA (nom) 2.47 µA (PVT)	65.39 nA (nom) 2.195 µA (PVT)		

NR-not reported, Rep-reported value, Sim-simulation of equivalent design

As pointed out earlier, most prior studies focus on area reduction and publish only nominal values. These numbers have been noted as “nom” in the table. To make a fair comparison, we need to evaluate the architectures within a PVT space. For this purpose, we have implemented the prior work architectures in the said 40 nm process. During design we matched the implemented design’s nominal performance with the reported nominal values. We then simulated these designs over the PVT space to ascertain their worst-case performance. All architectures have the same clamping transistor width and

have similar ESD performance. Leakage performance is also similar since the leakage is dominated by the clamping transistor.

Prior architectures are unable to maintain good performance in the entire PVT window. For instance, design [27] suffers from a large recovery time because it relies on leakage through a PMOS device to correct after a mis-trigger event. Design [17] uses weak transistors in the clamp switch-off path. These transistors become very slow across corners as power supplies are ramping up and the gate node of the clamp can couple high turning-on the clamp at some corners. This limits the fastest power-on ramp that is this architecture is able to support. Design [31] relies on a string of diodes to keep the holding voltage above the power supply. The forward voltage across this diode can vary from 0.3V to 0.7V over the PVT window and this large variation makes the architecture prone to latch-on. In fact our implementation used a diode string of up to four diodes to help alleviate this issue, but the design still was not immune to latch-on.

When the comparison is done over a full PVT window, the presented clamp offers a very competitive circuit and is a robust design over varying PVT conditions. Evaluating these architectures over industry-standard PVT conditions is necessary since a real-world design is only as good at its performance in the worst case corner.

Chapter Summary

The rail clamp presented in this chapter offers several advantages compared to the traditional prior art such as at least 20% area savings in the trigger circuit area, supporting power supply ramp rates that are as fast as 200 ns, dissipating the ESD energy more cleanly with little residual charge, recovering faster from false triggers and robust performance in an industry-standard PVT space. These results were proved using both

simulations covering process, voltage, and temperature corners, and through experimental results.

CHAPTER 6

FUTURE WORK AND CONCLUSIONS

The following are some ideas for related future work

1. Optimization and CAD automation for the presented comparator-based and dynamic time-constant-based rail clamps, similar to the traditional RC and single-inverter-based-rail clamp.
2. Robust and full proof method to study and prove latch-on immunity of rail clamps that employ any type of feedback, enabling designers to ensure that designs can never lock-on over the operating PVT space.
3. ESD protection for RF pins that have stringent parasitic capacitance requirements.
4. New rail clamp architectures that can support faster power-on applications while maintaining robust performance over PVT conditions.
5. On die protection strategies to help increase robustness to system level ESD tests like IEC 61000.

A method to automate and optimize the widely used RC and single-inverter-based rail clamp was presented. The methodology aims to obtain the most area efficient design that meets the given ESD and leakage targets over all process, voltage and temperature corners. Because the methodology takes PVT conditions into consideration, the methodology can be adopted readily by designers in the industry to obtain very close to optimum designs. The effectiveness of the methodology was proven by comparing it to designs obtained by randomly and exhaustively sampling the design space. The technology independence of the methodology was proven by evaluating the method in three different technologies.

In addition to the above, two new novel rail clamp circuits were also thoroughly studied. The first rail clamp modifies the traditional rail clamp and employs a comparator to reduce the size and area of the time constant circuit. The second rail clamp uses a dual time constant architecture. Both these circuits were shown to have significant advantages over the traditional design and their operation was evaluated inside an industry-standard process, voltage, and temperature space.

REFERENCES

[1] *For Electrostatic Discharge Sensitivity Testing-Human Body Model(HBM)-Component Level*, ESD Association Standard ESDA/JEDEC JS-001-2014, Sep. 2014.

[2] *For Electrostatic Discharge Sensitivity Testing-Machine Model(MM)*, ESD Association Standard ANSI/ESDA/JEDEC JESD22-A115C, Nov. 2010.

[3] *For Electrostatic Discharge Sensitivity Testing-Charged Device Model(CDM)-Device Level*, ESD Association Standard ESDA/JEDEC JS002-2014, Apr. 2015.

[4] S. Dabral and T.J. Maloney, in *Basic ESD and I/O Design*, Wiley-Interscience, 1998.

[5] R. Merrill and E. Issaq, "ESD design methodology," in *Proc. Elect. Overstress/Electrostat. Discharge Symp.*, 1993, pp. 233–237.

[6] L. Lin, X. Wang, H. Tang, Q. Fang, H. Zhao, A. Wang, R. Zhan, H. Xie, C. Gill, B. Zhao, Y. Zhou, G. Zhang and X. Wang, "Whole-chip ESD protection design verification by CAD," in *Proc. Elect. Overstress/Electrostat. Discharge Symp. (EOS/ESD'09)*, 2009, pp. 1-10.

[7] K.K. Hsueh, Sin-Hao Ke, J. Lee and E. Rosenbaum, "UVeriESD: An ESD verification tool for SoC design," in *Proc. Asia Pacific Conf. on Circuits and Systems (APCCAS '08)*, 2008, pp. 53-56.

[8] R. Zhan, H. Feng, Q. Wu, H. Xie, X. Guan, G. Chen and A.Z.H. Wang, "ESDExtractor: A new technology-independent CAD tool for arbitrary ESD protection device extraction," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 10, pp. 1362-1370, Sep. 2003.

[9] J.C. Bernier, G.D. Croft and W.R. Young, "A process independent ESD design methodology," in *Proc. IEEE International Symp. on Circuits and Systems (ISCAS '99)*, 1999, pp. 218-221.

[10] S. Thijs, C. Russ, D. Tremouilles, A. Griffoni, D. Linten, M. Scholz, N. Collaert, R. Rooyackers, M. Jurczak, M. Sawada, T. Nakaei, T. Hasebe, C. Duvvury, H. Gossner and G. Groeseneken, "Design methodology of FinFET devices that meet IC-Level HBM ESD targets," in *Proc. Elect. Overstress/Electrostat. Discharge Symp. (EOS/ESD'08)*, 2008, pp. 294-302.

[11] S. Malobabic, J.A. Salcedo, A.W. Righter, J.J. Hajjar and J.J. Liou, "A new ESD design methodology for high voltage DMOS applications," in *Proc. Elect. Overstress/Electrostat. Discharge Symp. (EOS/ESD'10)*, 2010, pp. 1-10.

[12] R. Zhu, F. Yao, S. Wang, A. Wang, L. Wu, X. Zhang and B. Chi, "A study of process/device/layout co-design for full-chip ESD protection in BCD technology," *Solid-State and Integrated Circuit Technology (ICSICT), 2012 IEEE 11th International Conference on*, 2012, pp. 1-3.

[13] J.A. Salcedo, J.J. Liou, Z. Liu and J.E. Vinson, "TCAD Methodology for Design of SCR Devices for Electrostatic Discharge (ESD) Applications," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 822-832, Apr. 2007.

[14] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.

[15] S. S. Poon and T. J. Maloney, "New considerations for MOSFET power clamps," *Microelectron. Reliab.*, vol. 43, pp. 987–991, Jul. 2003.

[16] C.A. Torres, J.W. Miller, M. Stockinger, M.D. Akers, M.G. Khazhinsky and J.C. Weldon, "Modular, portable, and easily simulated ESD protection networks for advanced CMOS technologies," in *Proc. Elect. Overstress/Electrostat. Discharge Symposium (EOS/ESD '01)*, 2001, pp. 81-94.

[17] J. Li et al., "Design and characterization of a multi-RC-triggered MOSFET-based power clamp for on-chip ESD protection," in *Proc. Elect. Overstress/Electrostat. Discharge Symp. (EOS/ESD'06)*, 2006, pp. 179–185.

[18] M. Stockinger et al., "Boosted and distributed rail clamp networks for ESD protection in advanced CMOS technologies," in *Proc. Elect. Overstress/Electrostat. Discharge Symp. (EOS/ESD'03)*, 2003, pp. 1–10.

[19] T.J. Maloney and W. Kan, "Stacked PMOS clamps for high voltage power supply protection," in *Proc. Elect. Overstress/Electrostat. Discharge Symposium*, 1999, pp. 70-77.

[20] C.-T. Yeh, Y.-C. Liang and M.-D. Ker, "PMOS-based power-rail ESD clamp circuit with adjustable holding voltage controlled by ESD detection circuit," in *Proc. Elect. Overstress/Electrostat. Discharge Symposium (EOS/ESD '11)*, 2011, pp. 1-6.

[21] C. Duvvury, "ESD protection device issues for IC designs," in *Proc. IEEE Conf. Custom Integr. Circuits*, 2001, pp. 41–48.

[22] C.-T. Yeh and M.-D. Ker, "High area-efficient ESD clamp circuit with equivalent RC-based detection mechanism in a 65-nm CMOS process," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1011–1018, Mar. 2013.

[23] S.-H. Chen and M.-D. Ker, “Area-efficient ESD-transient detection circuit with smaller capacitance for on-chip power-rail ESD protection in CMOS ICs,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 5, pp. 359–363, May 2009.

[24] S. Thijs, D. Trémouilles, D. Linten, N. M. Iyer, A. Griffoni, and G. Groeseneken, “Advanced ESD power clamp design for SOI FinFET CMOS technology,” in *Proc. IEEE Int. Conf. IC Des. Technol. (ICICDT)*, 2010, pp. 43–46.

[25] R. Venkatasubramanian, K. Oertle, and S. Ozev, “A comparator-based rail clamp,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 4, pp. 1493-1502, April 2016.

[26] J. W. Miller, C. A. Torres, and T. L. Cooper, “Circuit for electrostatic discharge protection,” U.S. Patent 5,946,177, Aug. 31, 1999.

[27] J. Li, R. Gauthier, and E. Rosenbaum, “A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection,” in *Proc. Elect. Overstress/Electrostat. Discharge Symp. (EOS/ESD’04)*, 2004, pp. 1–7.

[28] J. C. Smith and G. Boselli, “A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies,” *Microelectron. Reliab.*, vol. 45, pp. 201–210, Feb. 2005.

[29] H. Sarbishaei, O. Semenov, and M. Sachdev, “A transient power supply ESD clamp with CMOS thyristor delay element,” in *Proc. 29th Elect. Overstress/Electrost. Discharge Symp. (EOS/ESD’07)*, 2007, pp. 7A.3-1–7A.3-8.

[30] H. Sarbishaei, O. Semenov, and M. Sachdev, “A new flip-flop-based transient power supply clamp for ESD protection,” *IEEE Trans. Device Mater. Reliab.*, vol. 8, no. 2, pp. 358–367, Jun. 2008.

[31] C.-T. Yeh and M.-D. Ker, “Capacitor-less design of power-rail ESD clamp circuit with adjustable holding voltage for on-chip ESD protection,” *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2476–2486, Nov. 2010.

[32] S.-H. Chen and M.-D. Ker, “Optimization on NMOS-based power-rail ESD clamp circuits with gate-driven mechanism in a 0.13-µm CMOS technology,” in *Proc. 15th IEEE Int. Conf. Electron. Circuits Syst. (ICECS’08)*, 2008, pp. 666–669.

[33] A. Gerdemann, J. W. Miller, M. Stockinger, N. Herr, A. Dobbin, and R. Ricklefs, “When good trigger circuits go bad: A case history,” in *Proc. 33rd Elect. Overstress/Electrost. Discharge Symp. (EOS/ESD’11)*, 2011, pp. 1–6.

[34] R. A. Ashton, B. E. Weir, G. Weiss, and T. Meuse, "Voltages before and after HBM stress and their effect on dynamically triggered power supply clamps," in *Proc. Elect. Overstress/Electrost. Discharge Symp. (EOS/ESD'04)*, 2004, pp. 1–7.