

Flexible Electronics Powered by Mixed Metal Oxide Thin Film Transistors

by

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ABSTRACT

A low temperature amorphous oxide thin film transistor (TFT) and amorphous silicon PIN diode backplane technology for large area flexible digital x-ray detectors has been developed to create 7.9-in. diagonal backplanes. The critical steps in the evolution of the backplane process include the qualification and optimization of the low temperature (200 °C) metal oxide TFT and a-Si PIN photodiode process, the stability of the devices under forward and reverse bias stress, the transfer of the process to flexible plastic substrates, and the fabrication and assembly of the flexible detectors.

Mixed oxide semiconductor TFTs on flexible plastic substrates suffer from performance and stability issues related to the maximum processing temperature limitation of the polymer. A novel device architecture based upon a dual active layer improves both the performance and stability. Devices are directly fabricated below 200 °C on a polyethylene naphthalate (PEN) substrate using mixed metal oxides of either zinc indium oxide (ZIO) or indium gallium zinc oxide (IGZO) as the active semiconductor. The dual active layer architecture allows for adjustment to the saturation mobility and threshold voltage stability without the requirement of high temperature annealing, which is not compatible with flexible plastic substrates like PEN. The device performance and stability is strongly dependent upon the composition of the mixed metal oxide; this dependency provides a simple route to improving the threshold voltage stability and drive performance. By switching from a single to a dual active layer, the saturation mobility increases from 1.2 cm²/V-s to 18.0 cm²/V-s, while the rate of the threshold voltage shift decreases by an order of magnitude. This approach could assist in enabling the production of devices on flexible substrates using amorphous oxide semiconductors.

Low temperature (200°C) processed amorphous silicon photodiodes were developed successfully by balancing the tradeoffs between low temperature and low stress (less than -70 MPa compressive) and device performance. Devices with a dark current of less than 1.0 pA/mm² and a quantum efficiency of 68% have been demonstrated. Alternative processing techniques, such as pixelating the PIN diode and using organic photodiodes have also been explored for applications where extreme flexibility is desired.

DEDICATION

I dedicate this work to my newest son, Noah, whose fun-filled personality kept me relaxed and always ready to laugh.

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CHAPTER 1

INTRODUCTION

Overview

Flexible electronics have attracted much interest in the electronics research community recently due to their significantly improved ruggedness and potential to reduce the cost over the current, rigid industry standard. This dissertation investigates fabrication techniques for a specific flexible electronic device, the digital x-ray detector, and the challenges that must be overcome to bring a flexible digital x-ray detector to market.

This dissertation is organized as follows. The motivation behind the push towards amorphous oxide semiconductors and some of the new technology used to enable flexible electronics, like flexible x-ray detectors, is described in this introductory chapter. The implementation and optimization of an amorphous oxide semiconductor process on flexible substrates is described in Chapter 2, and Chapter 3 focuses specifically on the optimization of the active layer deposition process to enhance device performance. The incorporation of a photodiode into the flexible thin film transistor (TFT) technology developed in Chapters 2 and 3 is described in Chapter 4, while Chapter 5 discusses some of the key improvements made to the photodiode process. Finally, Chapter 6 provides summary conclusions and suggestions for further studies.

Brief Background on Thin Film Transistors

The typical thin film transistor (TFT) components are the gate, gate dielectric, active layer, source, and drain as illustrated in Figure 1.1. The following paragraph will briefly describe the function for each layer in the device.

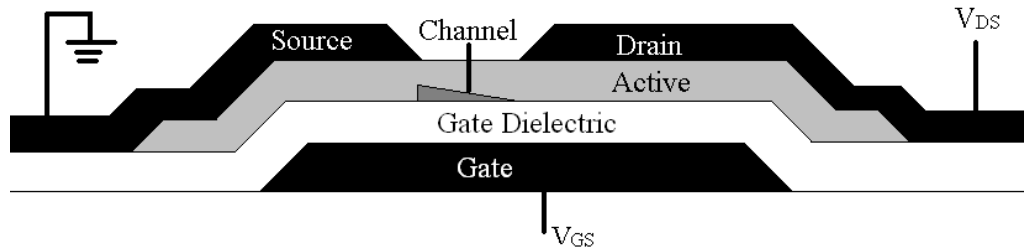


Figure 1.1: Basic Thin Film Transistor (TFT) Components and Structure

The function of the gate is to induce the formation of a conductive channel in the active layer when a positive voltage is applied to the gate relative to the source. The active layer then conducts carriers, either electrons for n-channel devices or holes for p-channel devices. This dissertation will focus on n-channel devices and all subsequent descriptions will be for n-channel devices unless otherwise noted. When the gate potential is negative, an electric field is induced in the channel that repels delocalized electrons away from the active layer/gate dielectric interface, which prevents conduction of carriers through the semiconductor. Conversely when the gate potential is positive, the electrons begin to accumulate within 5 nm of the gate dielectric (Tickle 1969).

Application of a potential (voltage) across the channel can induce current in the device. In this case, electrons pass from the grounded source to the biased drain through the conductive channel in the semiconductor when a voltage greater than the threshold voltage (approximately minimum potential required to turn the device on) is applied.

The gate voltage (V_{GS}) and drain voltage (V_{DS}) can be controlled independently, and transistors are usually characterized by holding one of the terminals at a constant voltage and sweeping the other voltage over a specific range. Once the sweep is complete, the terminal that was held constant is stepped to a new value and the sweep is

completed again. A family of curves is generated after the sweeps are completed. Sweeps of the drain voltage with the gate voltage held constant are known as output curves. For output curves, it is typical to step through 4-5 gate voltage in the range of 0-20 V. The sweep occurs from 0 to 20 V. The output curves should intersect at the origin. If the x-intercept is significantly greater than 0, then current crowding is occurring at the drain, which could indicate the presence of a barrier. The output curves are also used to extract the drain conductance, which is simply the slope in the linear region, and to determine if there are any short channel effects.

For transfer curves, it is typical to step through 2-5 drain voltages in the range of -20 to 20 V. Sweeps generally start at -20V (forward sweeps), but can also start at +20V (reverse sweeps). An observed behavior difference between the forward and reverse sweeps, commonly referred to as hysteresis, can indicate the presence of defects in the active layer or gate dielectric. The ratio of the maximum drain current I_{DS} (sometimes referred to as the on current I_{on}) divided by the minimum I_{DS} (leakage current or I_{off}) is commonly referred to as the On/Off ratio. In display applications, the On/Off ratio is usually related to the display contrast ratio. Other key parameters that can be extracted are described in the following sections.

There are typically three identifiable operating regimes for a transistor as illustrated in the example transfer and output curves shown in Figure 1.2. An exponential increase in current with increasing gate voltage is observed at low potentials in the subthreshold regime. The slope of the current increase is an important device metric known as the subthreshold slope. Subthreshold slope is defined as the gate voltage required to induce a decade increase in the drain current at a constant drain voltage.

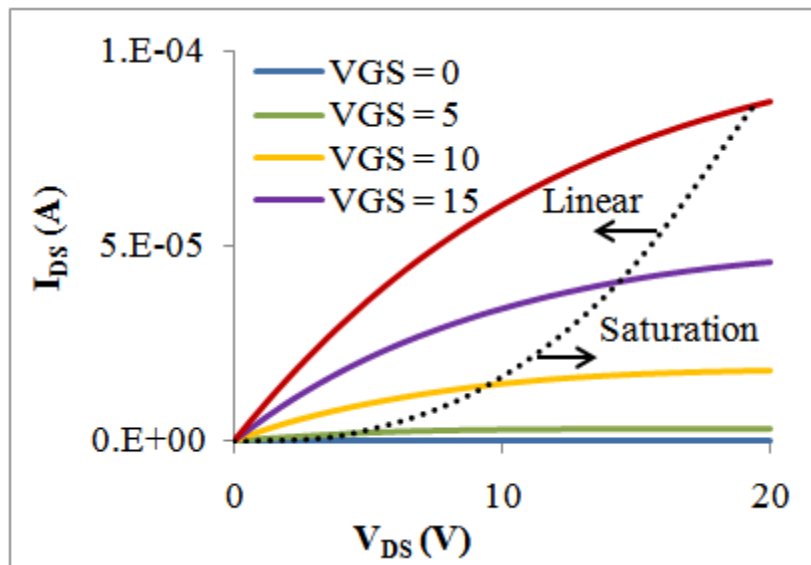
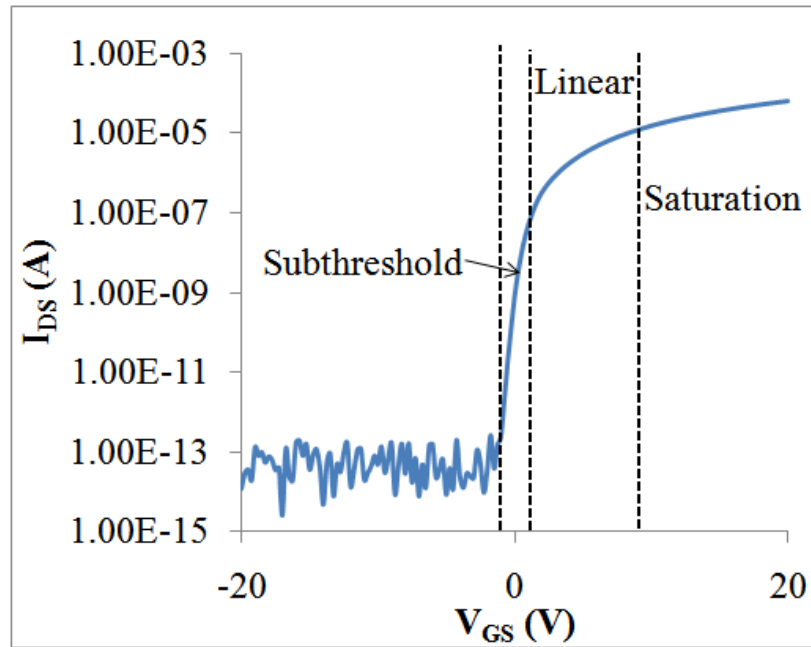


Figure 1.2: Transfer Curve and Output Curves Demonstrating Subthreshold, Linear, and Saturation Regimes.

Further increasing the potential results in the linear regime, which can be described by the square-law model:

$$I_{D_{lin}} = \mu_{sat} C_{ox} \left(\frac{W}{2L} \right) \left[(V_G - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad 1.1$$

where μ_{sat} is the saturation mobility; C_{ox} is the gate dielectric capacitance; (W/L) is the aspect ratio of the device; V_T is the threshold voltage; V_G is the gate voltage; and V_{DS} is the drain to source voltage.

At low V_{DS} , the squared term at the end of Equation 1.1 is insignificant and the device behaves like a variable resistor with the drain current proportional to the drain voltage. As V_{DS} increases, electrons in the region surrounding the drain are depleted, creating a pinch off point and the device is considered saturated. The drain current reaches a plateau when V_D is equal to $V_G - V_T$. This value is referred to as the saturation voltage (V_{DSAT}).

The value for V_{DSAT} can be inserted into Equation 1.1 to solve for the saturation current:

$$I_{D_{sat}} = \mu_{sat} C_{ox} \frac{W}{2L} (V_G - V_T)^2 \quad 1.2$$

In saturation mode, the device functions as a constant current source where the drive current is dependent on the gate voltage. The shape of the channel in Figure 1.1 is representative of a device that is at the onset of saturation. When the device is in saturation, the saturation mobility can be extracted using Equation 1.2 by plotting $\sqrt{I_{D_{sat}}}$ vs. V_G and calculating the slope:

$$\mu_{\text{sat}} = \frac{2L}{WC_{\text{ox}}} \left(\frac{\partial \sqrt{I_{\text{D}}}}{\partial V_{\text{G}}} \right)^2 \quad 1.3$$

The saturation mobility is a useful metric for quantifying the quality of the transistor as it characterizes how quickly an electron can move through the active layer. As Equation 1.2 shows, a higher mobility leads to a higher current. In emissive display applications, current is usually related to brightness.

The threshold voltage (V_{T}) can also be determined from the same $\sqrt{I_{\text{Dsat}}}$ vs. V_{G} curve by extracting the x-intercept as demonstrated in Figure 1.3. The V_{T} of the device in Figure 1.3 is approximately 0.7 V. The V_{T} is the voltage at which the onset of an inversion layer is formed in the active layer and can be thought of as the “on” voltage of the transistor. A value between 0 and 2 V is usually preferred.

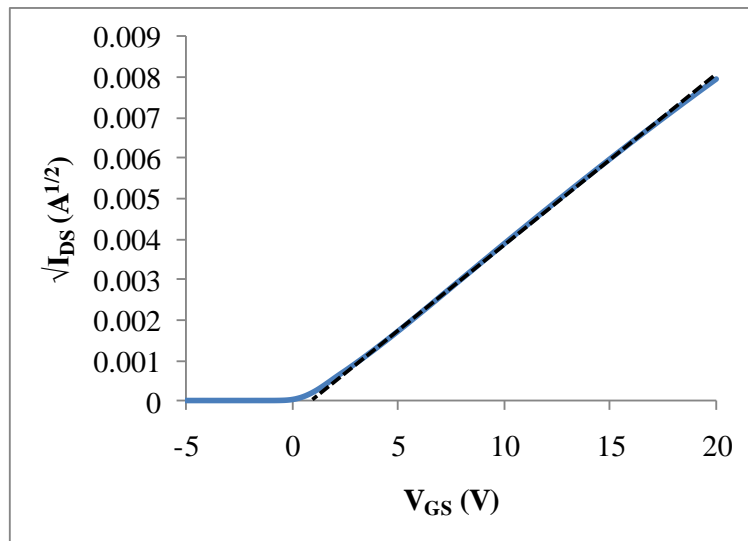


Figure 1.3: Extraction of V_{T} from the $\sqrt{I_{\text{D}}}$ vs. V_{G} Curve

Brief Background on Diodes

A diode is a semiconductor device that severely limits the current flow in one direction. A diode usually consists of a single semiconductor with a distinct junction where the doping changes from p-doping (hole rich) to n-doping (electron rich). At the ends of the diode are metal contacts which can, but do not have to, form an ohmic contact with the semiconductor to help transport current towards and away from the diode. The differing carrier concentration at the ends of the diode gives rise to a small diffusion current. As electrons diffuse towards the electron deficient p-doped side of the diode a built in potential is generated by the leftover ionized acceptor and donor atoms on the opposite side of the diode. This built in potential is one key component of a diode that enables solar cells and photodetectors.

When a forward bias is applied to a diode, the positive terminal is connected to the p-doped side of the diode and the negative terminal is connected to the n-doped side. In this state, electrons are encouraged to flow from the n-doped side to the p-doped side and out the positive terminal. The current in this state is dominated by the injection current.

If a reverse bias is applied to a diode, the positive terminal is connected to the n-doped side and the negative terminal is connected to the p-doped side. In this state, electrons are not encouraged to flow through the diode, but instead are routed directly from n-doped side to the positive terminal. Only a small diffusion current, which is typically 4-5 orders of magnitude less than the forward bias injection current and does not

greatly vary with the applied voltage, is present when the diode is operated under reverse bias.

Semiconductors are sensitive to light energy that exceeds the energy bandgap of the semiconductor. If an incident photon with energy exceeding the bandgap energy of the semiconductor is absorbed, an electron/hole pair can be generated. Even if there is no outside applied bias, the internal built in voltage is significant enough to separate the electron/hole pair generating a current flow opposing the injection current. If the diode is operated under reverse bias, the photogenerated current will generally dominate the diffusion current allowing for the calculation of incident irradiance.

In addition to acting as an electrical check valve, a diode has its own capacitance, which varies depending on the applied bias. Applying a strong reverse bias (-5 V) can fully deplete most semiconductor diodes. The depleted semiconductor helps store charge in the diode when the voltage is cut off. Digital x-ray detectors exploit this capacitance to enable active matrix digital x-ray detectors.

The I-V characteristics of a one-dimensional ideal diode are governed by the ideal diode equation (Equation 1.4), which describes the drift and diffusion current through the diode and is derived from the continuity equation. The ideal diode equation is given by:

$$I_D = I_S \left(e^{\frac{qV_D}{nkT}} - 1 \right) \quad 1.4$$

where I_D is the diode current, I_S is the reverse saturation current, q is the charge of an electron, V_D is the voltage applied across the diode, n is the diode ideality factor, k is Boltzmann's constant, and T is the absolute temperature.

Amorphous Silicon PIN Photodiodes

An amorphous silicon PIN photodiode is a special type of diode that is designed to detect light. The typical PIN diode components are a p-doped semiconductor, a lightly doped, nearly intrinsic semiconductor layer, an n-doped semiconductor, and the metal contacts on both ends of the diode connected to the rest of the circuitry. In the case of a photodiode, usually one of the doped layers and its corresponding contact metal are adequately translucent to allow for the capture of light in the intrinsic layer. A typical diode structure, shown below in Figure 1.4, is connected in series to a thin film transistor. The major diode components are surrounded by the red box.

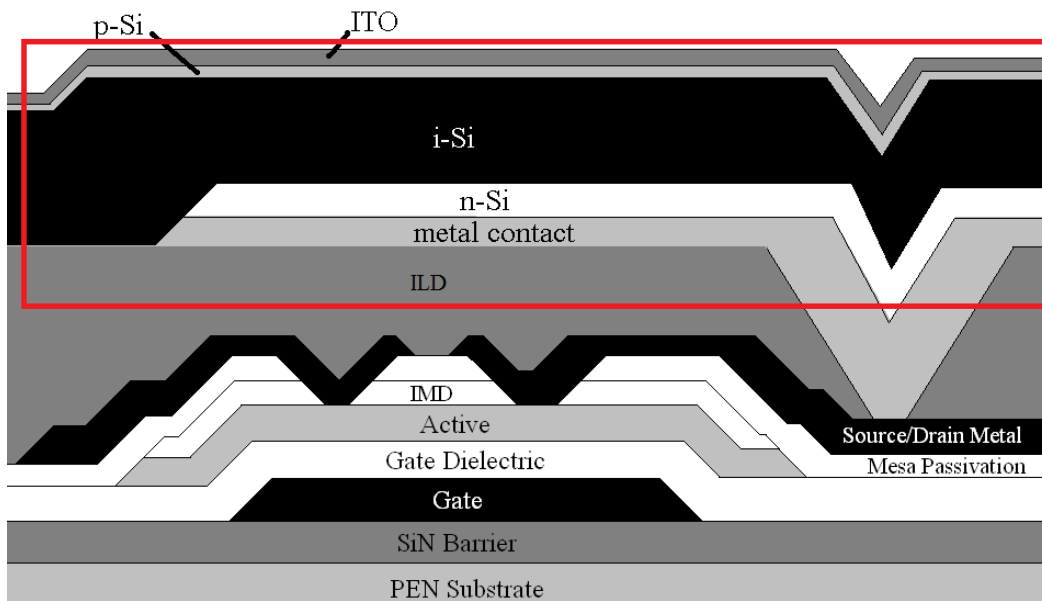


Figure 1.4: PIN Diode Connected in Series to a Thin Film Transistor

In the example provided in Figure 1.4, the light enters from the top through the indium tin oxide (ITO) layer and p-doped silicon (p-Si) and is absorbed in the comparatively thicker undoped or “intrinsic” amorphous silicon layer (i-Si). The absorbed photon is converted to an exciton, which separates into a mobile electron and

hole. The diode is reverse biased with the negative terminal connected to the ITO/p-Si side of diode, which draws holes toward the p-Si and electrons to the n-Si. The electrons are allowed to pass from the source to the drain through the TFT when the gate is sufficiently on and are read out at the edge of the detector by a charge sense amplifier.

As described in the previous section, the diode I-V characteristics can be compared to the ideal diode equation (Equation. 1.4) when the diode is in the dark. The reverse saturation current and diode ideality factor can be extracted from plotting the I-V characteristics of the diode in the dark on a semilog plot. The saturation current and ideality factor are related to the carrier lifetime with lower values for both parameters indicating longer carrier lifetime and a higher quality diode. In addition to fitting the ideal diode equation, the minimum dark current and the dark current at -5 V are extracted. The applied voltage across the diode (V_{bias}) in the sensor array is usually -4V.

When operated in the presence of light, the ideal diode equation is modified to include a new term, I_L , which is the current generated by light absorbed by the diode, as shown in Equation 1.5.

$$I_D = I_S \left(e^{\frac{qV_D}{nkT}} - 1 \right) - I_L \quad 1.5$$

The light current is a negative number, as it flows in the opposite direction of injection current generated when operating under forward bias. The light current generally dominates the total current output of a reverse-biased diode, making them ideal as a photo detector. This light current depends on the number of photons incident to the diode and the quantum efficiency (i.e., number of electrons generated per incident

photons). The short circuit current (I_{SC}) of the diode, which is the current when the voltage is zero, can be used to calculate the quantum efficiency if the irradiance is known. Determining the irradiance can be accomplished by providing a narrow emission spectra light source, like a light emitting diode (LED), and measuring the irradiance with a calibrated photodiode. Maximizing the quantum efficiency is another way to improve the signal to noise ratio of an x-ray detector and lower the noise floor. A good quality commercial photodiode will have 80-90% conversion efficiency over the visible spectrum. Quantum efficiency can be affected by the absorbance and reflectance of thin film layers between the diode and the light source and by the optical properties, film thickness, and quality of the diode layers.

Real diodes can deviate significantly from the ideal model due to series resistance and shunt resistance. A series resistance is a parasitic resistance placed in the path of the photogenerated electron or hole, and can be a result of high sheet resistance of the metal contact layer, high contact resistance, presence of significant electrically active defects in the semiconductor layers, and poor mobility of the carriers through the diode layers. Series resistance can be extracted by comparing the forward bias characteristics of the diode dark operation to the ideal diode equation fit. The deviation of the real diode from the ideal diode can be used to determine the series resistance as a real diode will start to follow Ohm's law when the applied bias is sufficiently large. The voltage difference between the ideal diode and the real diode (as demonstrated by the yellow line in Figure 1.5) divided by the current is the series resistance. For the yellow line drawn in Figure 1.5, the series resistance is approximately 50 k Ω .

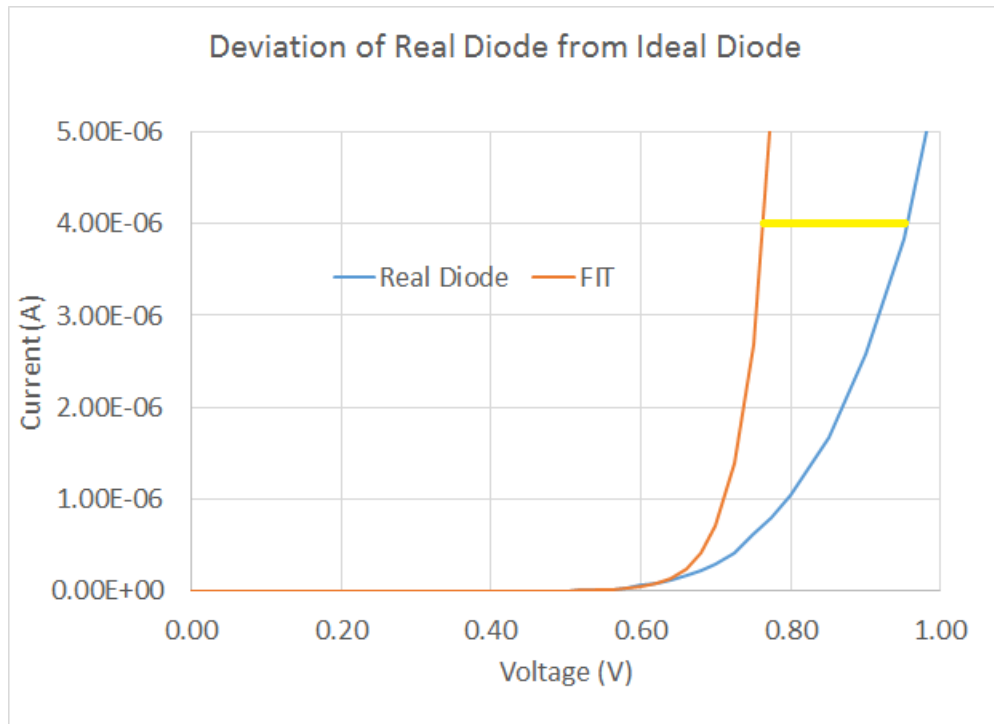


Figure 1.5: Comparison of a Real Diode and the Ideal Diode Equation Showing Series Resistance

Diodes can also suffer from shunts, which act as alternate resistive paths through the diode and are usually attributed to defects or impurities in the diode material. Shunt resistance is most noticeable as a deviation in the slope of the I-V sweep from the horizontal near the origin. Excessive shunt conductance can be an indication of a poor quality diode film. The shunt resistance can also be modulated by the diode film thickness with a thicker film increasing the overall resistance of the diode as well as decreasing the electric field across the diode.

Organic Photodiodes

Considerable research on organic photodiodes for solar cells has provided a significant head start towards the application of the technology to an x-ray detector

(Aernouts, et al. 2008). As opposed to an inorganic photodiode, organic photodiodes are usually constructed as a bulk heterojunction diode with phase-separated electron acceptor and donor materials. Light is typically absorbed in the donor material, which produces an exciton (an excited state) that does not immediately separate into an electron/hole pair since the energy of the photon alone is not enough to liberate the electron. Instead, the exciton must diffuse to the donor/acceptor boundary where the electron is captured by the acceptor material. The liberated hole can now freely move towards the negative electrode through the donor material (Aernouts, et al. 2008).

Organic photodiodes have some distinct processing advantages over PECVD grown a-Si, including the potential for additive processing through certain techniques such as screen printing or inkjet printing. These additive processing techniques are generally lower cost and lower temperature compared to vacuum-deposited, subtractive processing since they replace deposition, photolithography, and etching into a single processing step. However, the organic photodiodes are usually less efficient, possess a larger dark current, are more sensitive to moisture and oxygen, and are less stable under operation. In addition, the radiation hardness of the organic materials has not been studied in depth. Most of the efficiency issues are related to the conversion of an exciton into an electron-hole pair and the lifetime of the exciton and charge carriers. For this reason, a bulk heterojunction structure is employed where the donor and acceptor material are mixed, forming a dendritic network with a large interfacial area where an exciton can be converted into an electron and a hole.

The electrons and holes move from the bulk heterojunction into electron and hole transport layers via hopping. The function of the transport layers is to prevent the passage

of the opposing charge carrier. An ideal electron transport layer has a disproportionately high electron mobility compared to its hole mobility. After passing through the transport layer, the charges are transferred to the metal electrodes where the current can be measured. The basic “standard” organic bulk heterojunction diode structure is shown in Figure 1.6.

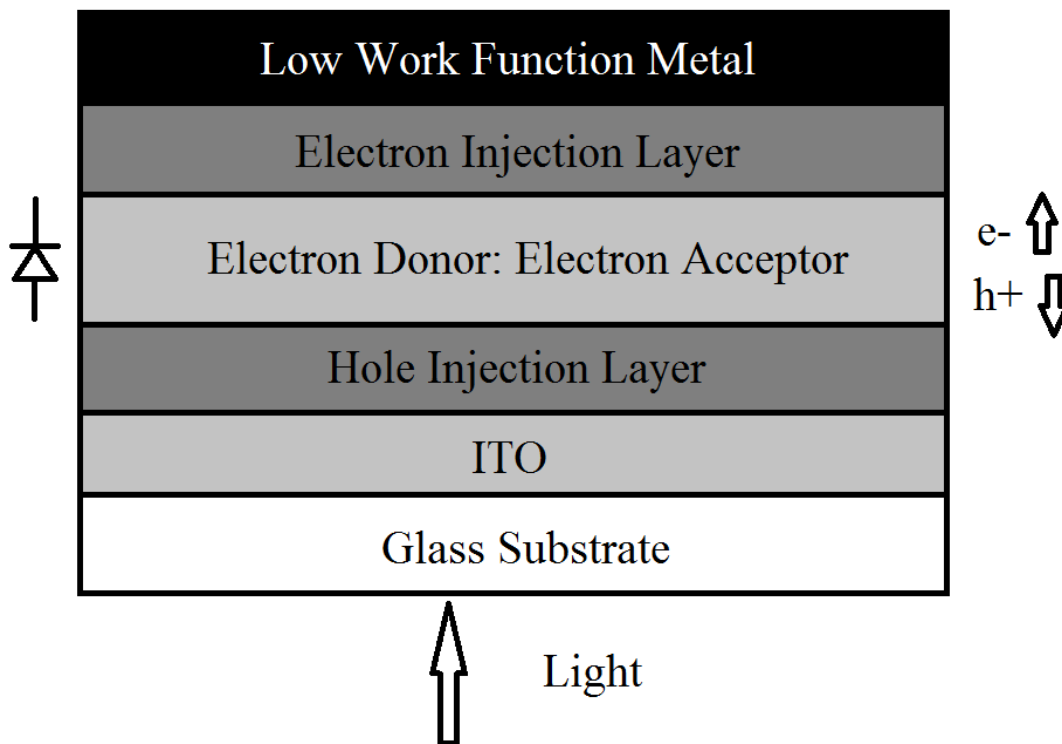


Figure 1.6: Standard Organic Photodiode Structure

One potential disadvantage to the “standard” organic bulk heterojunction photodiode is that the low work function cathode metal is on the top of the structure. When an NMOS transistor is placed in series with the standard organic photodiode structure, the gate voltage must be overdriven to exceed the positive bias (relative to the source) applied to the low work function metal cathode, placing extra stress on the gate

dielectric and active layer. In theory, the structure could be flipped, but this would expose the organic layers to the ITO sputter process, which contains oxygen and will damage the exposed organic films.

Instead the diode polarity could be flipped by using a high work function metal such as gold or silver as the cathode. In this case, the ITO would act as the low work function electrode and would donate electrons. An example of an inverted organic photodiode is shown in Figure 1.7.

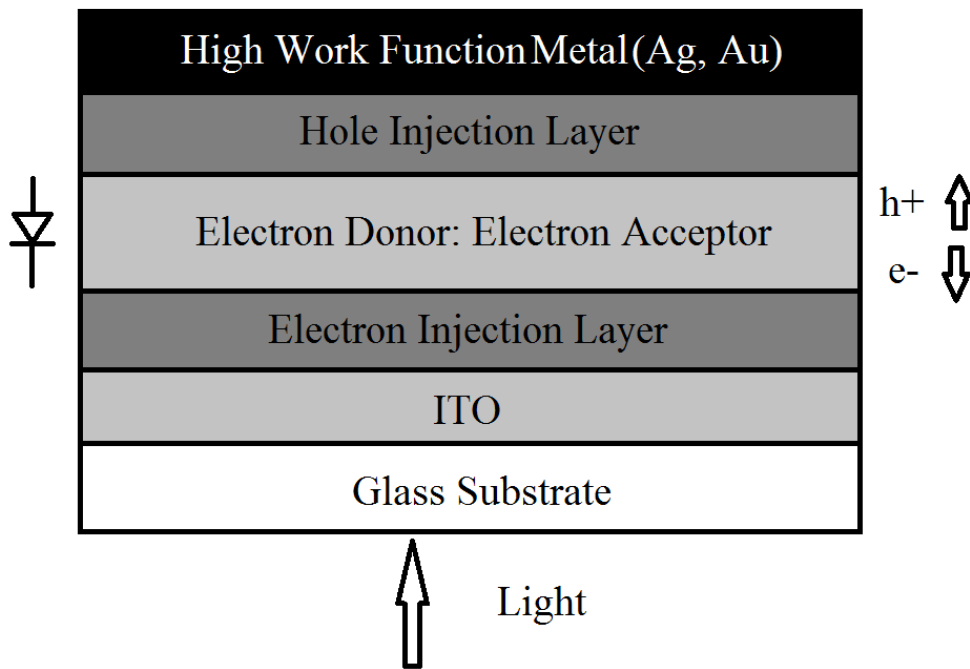


Figure 1.7: Inverted Organic Photodiode Structure

Examining a band diagram of the inverted structures reveals a significant difference between the lowest unoccupied molecular orbit (LUMO) of the PCBM electron acceptor (-3.9 eV) and the ITO electrode work function (-4.8 eV). Nanoparticles of titania have been proposed as an electron injection layer in solution processed organic solar cells because the LUMO of titania is -4.2 eV (Lim, et al. 2012), which is between

the LUMO of PCBM and the work function of ITO. However, titania nanoparticles are considered an IARC Group 2B carcinogen. Research into an appropriate electron injection layer for low temperature solution processing will be required. Nanoparticle dispersions of metal oxides, like zinc oxide, which have exceptional electron mobility and virtually no hole mobility will be explored. In addition, surface treatments for the ITO electrode that could lower the work function of the surface, such as a hydrogen or nitrogen plasma treatment, will also be explored.

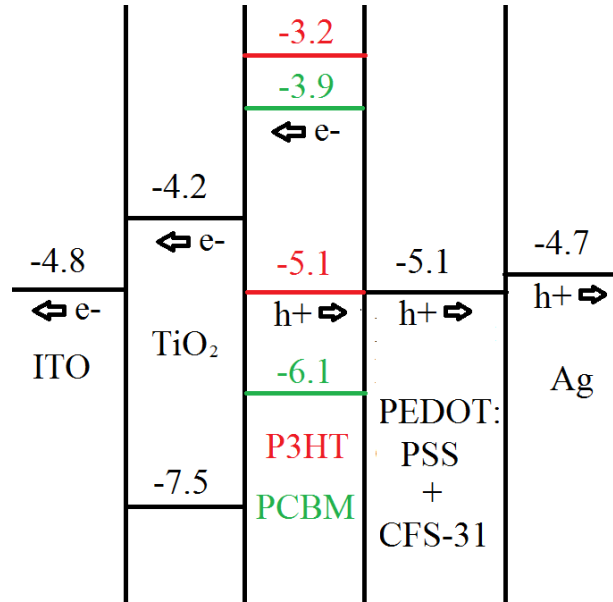


Figure 1.8: Electronic Band Structure of an Inverted Organic Photodiode. HOMO and LUMO Values are Provided by Lim, et al, (Lim, et al. 2012).

Another issue is related to the hole transport layer. The most common solution processed hole transport layer is Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS), which is hydrophilic and whose highest occupied molecular orbital (HOMO) energy level matches the HOMO level of P3HT and the work function of the silver electrode, allowing the holes to hop from the P3HT through the

PEDOT:PSS to the silver without allowing electrons through. However, the bulk heterojunction material is hydrophobic, creating wetting issues. There are numerous fluorosurfactants available on the market that can help an aqueous solution wet to a hydrophobic surface. In the example presented in Figure 1.8, the surfactant is Dow Corning CFS-31. In most cases, the fluorosurfactant is spin coated and baked. Spin coating is inefficient and wasteful (less green) over large area substrates, so the capability of these fluorosurfactants to be inkjet coated will be investigated.

Also note as shown in Figure 1.8, that the HOMO and LUMO of the PCBM are lower than the HOMO and LUMO of the P3HT, creating an overlap that makes the charge separation possible. If the LUMO of the P3HT were significantly higher than the PCBM, then excitons formed in the P3HT would simply revert back to ground state since it would take more energy to transfer the electron to the PCBM acceptor. Potential bulk heterojunction material candidates will need to have a similar HOMO/LUMO overlap like P3HT/PCBM to be successful.

Introduction to Semiconductor Processing Techniques

Semiconductor device fabrication consists of a sequence of thin film processing steps comprising multiple additive and subtractive techniques including photolithographic patterning in order to achieve the three-dimensional transistor structure presented in Figure 1.1. At its most basic level, these processes add (additive process) or remove (subtractive process) material in order to form a device structure. Thin film processes explored in this dissertation include sputter deposition, plasma enhanced chemical vapor deposition, photolithography, wet etching, and dry etching. A brief description of each process is described below.

Sputter Deposition

Sputtering is a process where atoms or clusters of atoms are ejected from a surface after an incident ion created in a plasma impinges on the surface with sufficient energy. The energy from the incident ion is imparted to target species, which can travel up to the surface and may ultimately aid in the ejection of one or more atoms from the surface, in the same manner as a cue ball in billiards (Chapman 1980). The threshold energy for sputtering is around 20-30 V, but sputter yields increase until several hundred volts of ion energy, where implantation becomes significant (Lieberman and Lichtenberg 1994).

Sputter deposition in semiconductor processing usually takes place in a vacuum at a pressure between 5 and 10 mTorr. The low pressure allows for the formation of a plasma, which can be thought of as a weakly ionized gas, when a direct current (DC) or radio frequency (RF) field is applied to the chamber. The low pressure also increases the mean free path, which is the average distance between collisions, allowing for ballistic transport of atoms and molecules.

For sputter deposition, a target is used as the actively driven electrode, where positive ions impinge and vaporize the target surface, creating a plume of effluents that are intentionally deposited onto a substrate. Sputtered films maintain excellent stoichiometric control, especially in comparison to an electron beam or thermally evaporated material (Lieberman and Lichtenberg 1994).

Plasma Enhanced Chemical Vapor Deposition

Low temperature, high quality films can be grown through plasma-enhanced chemical vapor deposition (PECVD) at much lower temperatures than conventional CVD. A glow discharge is used instead of purely thermal energy to generate the reactive species that deposit onto the surface. For example, the activation energy of silane (SiH_4) is 1.5 eV for high-temperature CVD and 0.025- 0.1 eV for PECVD (Lieberman and Lichtenberg 1994). Additional substrate heating is used to improve reaction speed, film density, local crystalline order, and conformality.

Photolithography

Photolithography starts with the casting of a UV sensitive organic film, known as photoresist, on to the substrate. The organic material can be spin cast (dispensed while the wafer is spinning at a speed between 500 and 5000 RPM), sprayed in a process similar to an industrial paint spray, or forced through a slotted opening as in extrusion or slot dye coating. The coat process is usually followed by a bake at a temperature between 95 and 120 °C to drive off the majority of the volatile solvents in which the UV sensitive organic material was dissolved. A pattern is transferred into the organic film by exposing the organic film to UV light through a patterned mask. The opaque portion of the mask protects the underlying portions of the organic film from the UV radiation while the transparent portion allows UV light to expose the surface. In the case of positive photoresist (negative photoresist demonstrates the opposite behavior), the solubility of the photoresist in a basic solution is increased. The weakened photoresist is susceptible to dissolution in a developer. Following the develop process, the wafers are rinsed and baked on a hot plate to remove any residual water. This final bake can occur between 105

and 150 °C, depending upon the photoresist. At higher temperatures, the organic photoresist begins to soften, allowing the patterned features to reflow and form into structures with tapered sidewalls.

Etching

Following the photolithography process is an etch process that is designed to transfer the pattern from the photoresist into the underlying layer by removing the material that is not protected by the photoresist mask. There are two principal techniques used to etch semiconductor materials. The first is wet etching, which simply uses a controlled mixture of acids, oxidizers, and/or bases to chemically remove the layer. Wet etching is generally isotropic (non-directional) and can be very selective for the underlying layer over the photoresist if the correct chemical mix is chosen.

An alternative method is dry etching, which uses a reactive plasma to etch materials. Relatively inert gases can be introduced into a vacuum chamber where an electric field is applied to generate a plasma. Reactions in a plasma can result in the formation of highly reactive ions and free radicals. Anisotropic (directional) etching is possible due to the presence of a negative charge at the anode of the chamber and etching by charged species in the plasma. If a wafer is placed on the anode, positive ions can be directed to the wafer. This form of dry etching is known as reactive ion etching (RIE).

Flat Panel Display Processing

Before discussing flexible display technology, it is important to understand the basics behind conventional flat panel display processing that yields rigid planar displays. Processing begins with a substrate, typically borosilicate glass. Glass is chosen because the substrate material must be transparent to visible light in order for the backlight of the

flat panel to shine through to the viewer (in the case of conventional liquid crystal displays). The glass substrate is generally free from mobile contaminants such as sodium that can degrade amorphous silicon thin film transistors (TFTs) (Kuo, Okajima and Takeichi, Plasma Processing in the Fabrication of Amorphous Silicon Thin-Film-Transistor arrays 1999). A schematic of a typical liquid crystal display (LCD) is illustrated in Figure 1.9.

The display fabrication begins with the back plane, which contains thin film transistor (TFT) elements as well as the anode for the liquid crystals (in the case of LCDs). Controlling each pixel with a TFT (commonly referred to as active matrix displays) results in a wider viewing angle, reduced “ghosting” of images, and lower power consumption than passive matrix displays (Kuo, Okajima and Takeichi, Plasma Processing in the Fabrication of Amorphous Silicon Thin-Film-Transistor arrays 1999). The individual TFT layers are generally between 50 and 400 nm thick. Most of the dielectric and semiconductor layers are silicon based, which is convenient with respect to thermal expansion because the substrate is also silicon-based and has a similar thermal expansion coefficient (Kuo, Okajima and Takeichi, Plasma Processing in the Fabrication of Amorphous Silicon Thin-Film-Transistor arrays 1999).

There are four common layouts for the TFT layers as shown in Figure 1.10. These are inverted staggered trilayer, inverted staggered bilayer, staggered, and coplanar TFT architectures.

The inverted staggered trilayer structure is most commonly applied to amorphous silicon based TFTs due to its superior performance over the other structures (Hiranaka, Yoshimura and Yamaguchi 1989) and its ability to be fabricated with a large margin for

error (Kuo, Okajima and Takeichi, Plasma Processing in the Fabrication of Amorphous Silicon Thin-Film-Transistor arrays 1999). Amorphous silicon (a-Si:H) is preferred because the source material for the amorphous silicon (SiH_4 gas) is readily available and the PECVD deposition process for amorphous silicon can be tightly controlled (Kuo, Okajima and Takeichi, Plasma Processing in the Fabrication of Amorphous Silicon Thin-Film-Transistor arrays 1999).

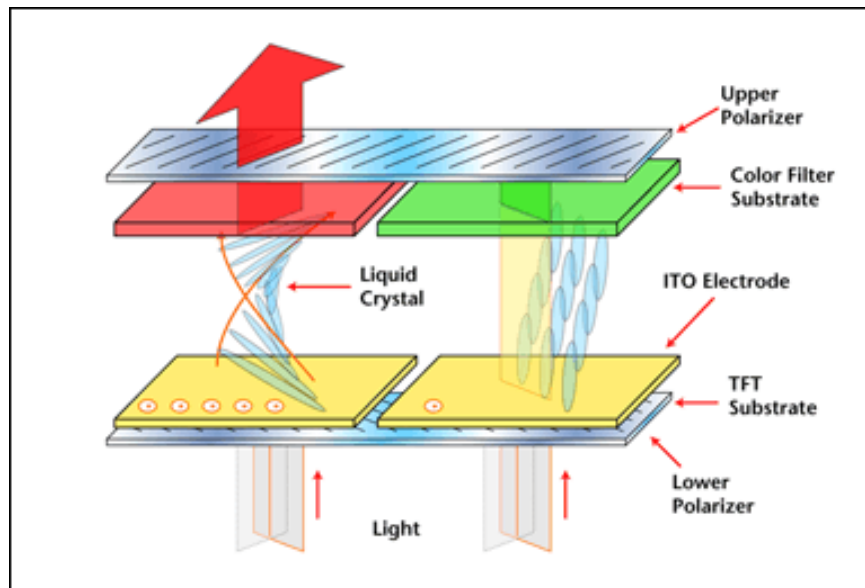


Figure 1.9: LCD Schematic. The TFT Substrate and Lower Polarizer Comprise the Back Plane, while the ITO Electrode, Liquid Crystals, Color Filter, and Upper Polarizer Comprise the Front Plane (Stone 2006).

In the inverted staggered trilayer architecture, the gate layer is deposited first. Metals are typically preferred; although doped polysilicon has been used in Complementary Metal Oxide Semiconductor (CMOS) technology. The gate metal impacts the threshold voltage (as described in section 1.2) of the transistor through the work function difference between the gate metal and the semiconductor. Common gate metals include aluminum, molybdenum, chromium, and tungsten, and alloys of those

metals (Kuo, Okajima and Takeichi, Plasma Processing in the Fabrication of Amorphous Silicon Thin-Film-Transistor arrays 1999). The deposition of the gate is usually performed by sputtering.

The deposition of the gate dielectric, the semiconductor active layer, and the active layer passivation follow the patterning of the gate. These layers can be grown sequentially in the same PECVD chamber or in separate chambers. Sequential deposition in the same chamber can improve the semiconductor / dielectric interface by lowering the interface density of states. The deposition conditions can dramatically impact device performance. For example, the SiH_2/SiH ratio has been shown to increase with increasing power (Miki, et al. 1987) due to the increase in free hydrogen in the plasma. This increase in the SiH_2 concentration in the film leads to increased threshold voltage and decreased on current. Higher power can also lead to the roughening of the underlying gate dielectric, which can reduce the mobility of carriers in the channel by providing scattering sites. The temperature of the deposition process can also greatly affect the TFT performance. At higher temperatures, diffusion of hydrogen is encouraged, which facilitates the passivation of dangling silicon bonds. The reduction in dangling bonds improves device performance and stability (Y. Kuo, Plasma Etching and Deposition for a-Si:H Thin Film Transistors 1995). However, increasing the temperature also decreases the amount of hydrogen in the plasma. For a-Si:H deposition, the optimal process temperature usually falls between 200 and 280 °C.

The choice of the gate dielectric and channel passivation material can also significantly affect the device performance. Hydrogenated silicon nitride is the preferred choice because the hydrogen in the film can passivate dangling bonds in the a-Si:H better

than silicon dioxide (Kuo, Okajima and Takeichi, Plasma Processing in the Fabrication of Amorphous Silicon Thin-Film-Transistor arrays 1999).

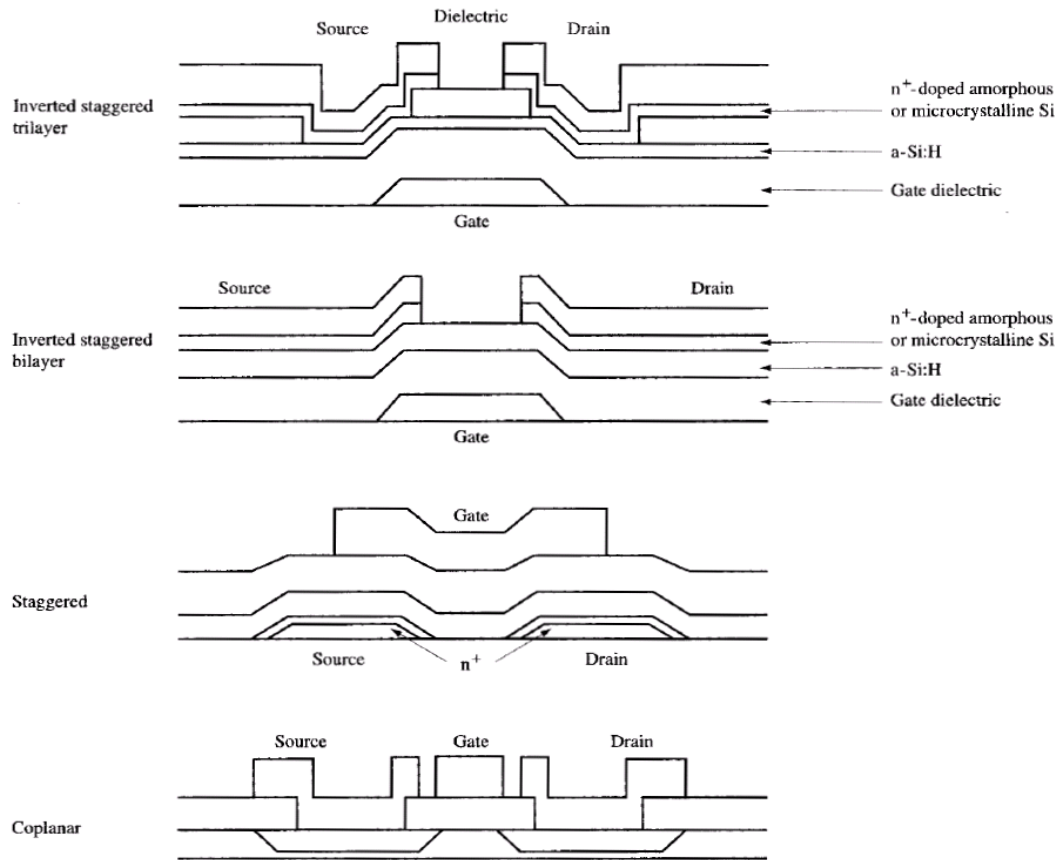


Figure 1.10: Cross-Sectional View of Inverted Staggered Trilayer, Inverted Staggered Bilayer, Staggered, and Coplanar TFT Architectures (Kuo, Okajima and Takeichi, Plasma Processing in the Fabrication of Amorphous Silicon Thin-Film-Transistor arrays 1999).

The active and passivation layers are etched to create islands of the active material. The isolation of the active material allows for individual control of each pixel. The gate dielectric is not etched to provide isolation to the gate metal from subsequent metal depositions. The etch process can be followed by the deposition of an additional passivation layer to protect the exposed sidewall of the active layer or can proceed

directly to another photolithography/etch cycle to open contacts to the gate and active layer.

Once contacts are opened, a heavily doped silicon layer is deposited. The purpose of this heavily doped layer (termed “n+” in NMOS devices where electrons are the carriers) is to bridge the work function difference between the a-Si:H active layer and the source/ drain metal, which creates an ohmic (linear current/voltage characteristics) contact. The resistivity of this n+ layer should be minimized as the contact resistance accounts for approximately 10% of the total on resistance of the TFT⁴. The deposition of the source/drain metal follows the deposition of the n+ layer. The choice of metal can affect the performance of the devices. Metals with low resistivity such as aluminum or copper are typically selected to reduce losses over long metal runs.

The pixel anode is then defined with the following processing steps. An additional dielectric layer is deposited on the source/drain metal to reduce parasitic capacitance effects from the source/drain metal and is usually greater than 1 μm thick. The pixel anode is formed in a transparent conducting oxide such as indium tin oxide (ITO). Transparency is required because light from the LCD backlight must pass through the anode. The anode is usually passivated with another dielectric to complete the back plane process.

The display front plane comprises the remaining processes required to complete the display. The front plane in an LCD consists of the liquid crystals, polarizers, color filter, and the cathode. The liquid crystal realign when an electric field is generated between the anode and the cathode allowing polarized light to pass. When there is no field present, the light is reflected. The intensity of the field determines the amount of

light allowed to pass. Red, green and blue color filters (and more recently yellow filters as well) can be added to generate a wide gamut of colors. Once the front plane is complete, device drivers and packaging are incorporated to complete the display. This work focuses on the backplane technologies.

Introduction to Flexible Displays

Flexible displays have captured manufacturing interests over conventional flat panel displays due their thinner profile, conformability, robustness with respect to breakage and lighter weight. These advantages could lead to a new generation of flexible displays that could be shaped to fit most any conceivable application including wearable displays integrated into clothing, foldable or rollable displays that could be stored while not in use, and conforming and unique-shaped displays for equipment consoles. Robust and lightweight flexible displays could conceivably replace glass-based displays in cell phones and televisions. An example of an electrophoretic flexible display is shown in Figure 1.11.



Figure 1.11: Flexible Display Produced on 125 μm Thick Stainless Steel Foil

Flexible Substrate Materials

The fabrication of the flexible display starts with the choice of the substrate material. There are three main classes of flexible substrates: flexible glass (Crawford 2005), metal foil (Wu, et al. 1997) (Chuang, et al. 2007) (Jeong, Jin, et al. 2007) and polymeric (J. S. Park, T. W. Kim, et al. 2009) (Song, et al. 2010) (Sugimoto, et al. 2004) films. The ideal substrate would be colorless and transparent (for bottom emitting organic light emitting diode, or OLED, emissive displays), flexible and rollable, low-cost, resistant to chemical attack, dimensionally stable under thermal cycling and would have low permeability to water and oxygen and thus able to act as an intrinsic barrier layer. If this barrier layer were inherent in the substrate, simply laminating two film sheets together would be sufficient to package the device at low cost. No material has emerged that fills all of these needs simultaneously (see Table 1.1).

Table 1.1: Comparison of Substrate Properties of Interest for Stainless Steel, Plastics such as Polyethylene Naphthalate (PEN) and Polyimide (PI), and Glass

Property	Stainless Steel	Plastics (PEN, PI)	Glass
Weight (g/m^2)	800	120	220
Safe bending radius (cm)	4	4	40
Visually transparent?	No	Some	Yes
Max process temp ($^{\circ}\text{C}$)	1000	180, 300	600
CTE ($\text{ppm}/^{\circ}\text{C}$)	10	16	5
Elastic Modulus (GPa)	200	5	70
Permeable O_2 , H_2O	No	Yes	No
Planarization necessary?	Yes	Yes	No
Electrical conductivity	High	Low	Low

Flexible Glass

Thin sheets of glass can be made flexible with very small thicknesses (less than 100 μm). Glass at a thickness between 400 and 700 μm is the current standard substrate material for flat panel display fabrication, acting as perfect impermeable barrier layers and offering superior optical properties, ultra-smooth surfaces, and low thermal expansion coefficients. However, glass sheets that are sufficiently thin to also be flexible are highly susceptible to breaking and cracking along the edges if even slightly mishandled. Coating the glass sheets with a thin polymer layer around the edges and surface makes the substrates less prone to breaking during minor handling mistakes in

production and also reduces the influence of existing defects. Even with this hybrid approach, flexible glass substrates cannot currently be used in large scale manufacturing due to low yield related to glass breakage (Crawford 2005).

Stainless Steel

Stainless steel (SS) is a strong candidate for applications where transparency is not required. SS foils, produced with thicknesses of 125 μm , provide durable, flexible substrates that tolerate high temperature processes with much better dimensional stability than plastic. The foils provide a perfect diffusion barrier to oxygen and water vapor and have proved to be successful substrates for both amorphous and crystalline silicon-based TFTs used to make top-emitting active matrix OLED devices (Wu, et al. 1997). Finally, at 10 ppm/ $^{\circ}\text{C}$, SS films also have a lower CTE than polymer films. The steel foils, however, have a rough surface due to rolling mill marks and are highly conductive, so an insulating spin-on-glass (SOG) planarization layer must be coated on top of the stainless steel. The planarization layer ensures flat, non-conductive surfaces that will translate into accurate device registration on subsequent layers.

Plastic Films

Plastic engineered films are very appealing substrate materials for flexible electronics due to their low cost and toughness. Dupont's Teonex brand of polyethylene naphthalate (PEN), has emerged as a leading candidate. As seen in Figure 1.12, PEN shows a remarkably smooth, defect-free surface quality after pretreatment with an adhesion layer. PEN has a Young's modulus three times greater than typical amorphous plastic films due to its semicrystalline, biaxially oriented nature.

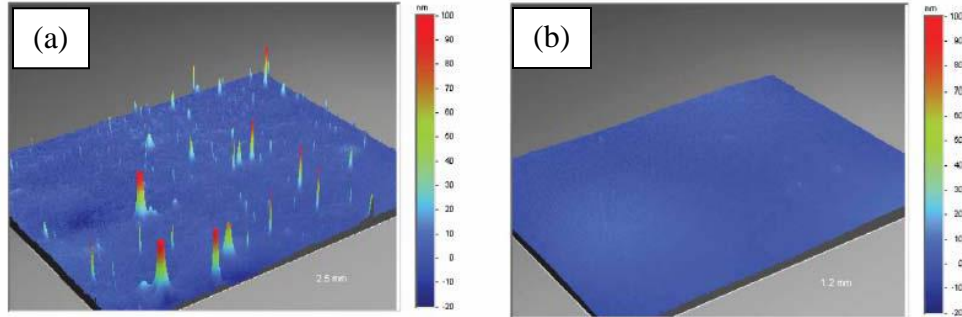


Figure 1.12: Atomic Force Microscope Height Images Showing the Surface Smoothness of (a) Industrial Grade Polyethylene Naphthalate (PEN) and (b) DuPont's Surface Tailored Teonex[®] Q65 Film (MacDonald 2004)

Natural thermal expansion also needs to be taken into account when dealing with thin film stacks on polymers. Thermal expansion is quantified by the coefficient of thermal expansion (CTE) of the material. Relative to other polymers, PEN has a relatively low CTE of about 13 ppm/ °C, but what is important is that the substrate is coupled with a layer that has a similar CTE. Any mismatch in thermal expansion coefficients during thermal cycling could cause high levels of residual stress and film cracking.

Manufacturing Challenges for Flexible Displays

Currently, there are five primary approaches toward fabricating flexible displays: roll-to-roll processing, transfer processing, substrate laser release processing, substrate mechanical release processing, and bond/debond processing.

Roll-to-Roll

The roll-to-roll approach involves processing directly on a roll of flexible material. The roll is loaded at one of the equipment and fed through the equipment for processing to a reel on the output side. An example demonstrating the transfer of a

photoresist pattern into a layer of indium tin oxide (ITO) by wet etching (Krebs, Gevorgyan and Alstrup 2009) is shown in Figure 1.13. The material is first fed into the CuCl_2 ITO Etch bath using a series of rollers. The material proceeds directly to the resist strip bath containing NaOH, which is followed by rinsing in DI water and drying with heated nitrogen. The feed rate is constant through all of the baths so each individual bath must be designed to allow adequate residence time of the material for each process to complete. All processing takes place on the freestanding flexible material.

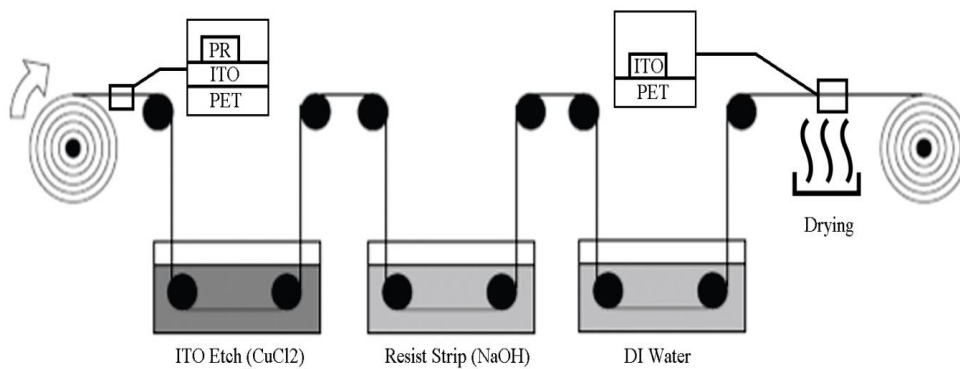


Figure 1.13: Schematic of Roll to Roll ITO Etch and Resist Strip Process (Krebs, Gevorgyan and Alstrup 2009).

However, current semiconductor processing technologies are geared toward the handling of rigid substrates. Examples of semiconductor processing equipment are demonstrated in Figure 1.14. Figure 1.14(a) shows a wet bench that processes batches of 25 wafers at a time. This wet bench would be the plate to plate processing analog of the roll to roll ITO etch demonstrated in Figure 1.13. The 25 wafers are first placed in the bath in the far left by the robot to etch the ITO, then the wafers are pulled from the ITO etch placed and placed in the NaOH resist strip bath. Once the resist is stripped, the wafers are placed into the quick dump rinse tank at the front of the bench (the water spray nozzles for this tank are visible in Figure 1.14(a)). Once the wafers have been rinsed, the

wafers are placed into the spin rinse dryer (SRD) which is partially visible at the right edge of Figure 1.14(a).

The equipment in Figure 1.14(b) is a Rite Track 8800 photoresist coater and developer. Wafers are placed into a boat that holds 25 wafers at left end of the track at the bottom of Figure 1.14(b) for adhesion layer coating (usually hexamethyldisilazane), followed by resist dispense, solvent bake out on a hot plate, and cooling on a water-chilled plate. The wafers are pulled from the right end of the track and sent to the next processing step. As opposed to the roll to roll process presented in Figure 1.13, the wafers in these batch operations are always handled from the back (non-processing) side of the wafer.



Figure 1.14: Images of (a) Automated Batch Processing Wet Etch Hood and (b) Photoresist Coater and Developer Track

Since most semiconductor processing equipment is geared towards plate to plate processing, significant investment in equipment and processing is required for the integration of roll-to-roll technology. As shown in Figure 1.13, the process side of the substrate comes into contact with rollers multiple times, which could lead to defects and device failure. Effective in-line metrology is also problematic.

SUFTLA

An alternative methodology that utilizes the more traditional plate-to-plate processing is a pattern transfer process such as Surface-Free Technology by Laser Annealing (SUFTLA) (Inoue, et al. 2002). The SUFTLA process involves fabricating TFTs on to a glass substrate as described in Section 1.4 with one major difference. An amorphous silicon exfoliation layer is deposited on to the glass substrate prior to the deposition of any of the device layers. Once the device fabrication is complete, another substrate (the first transfer substrate) is glued to the process side of the glass wafer using a UV-curable, water-soluble adhesive. Once this adhesive is cured, a XeCl excimer laser ($\lambda = 307 \text{ nm}$) is used to melt the a-Si exfoliation layer, which releases hydrogen to force the substrate apart. The rest of the device layers are protected because the a-Si absorbs most of the radiation.

The now liberated backside of the device is glued to a flexible plastic substrate using a permanent, non-water soluble adhesive. The first transfer substrate is cut up and the entire assembly is soaked in water to dissolve the water soluble, temporary adhesive (Inoue, et al. 2002). The equipment for the SUFTLA transfer process is expensive relative to other semiconductor processing equipment and is not considered feasible for

production. In addition, the processing time increases as the substrate area increases and is only appropriate for wafer-scale processing (Hatano, et al. n.d.).

EPLAR

A third option, known as Electronics on Plastic by Laser Release (EPLaR) (The Society for Information Display 2011), involves spin casting a thick polyimide layer (50-100 μm) to a glass substrate as shown in Figure 1.15. Once the polyimide is cast, the process flow follows the basic display manufacture process presented in Section 1.4. Once the TFT fabrication is complete, the polyimide is released from the glass substrate via excimer laser similar to the SUFTLA process. The basic process flow is illustrated in Figure 1.15.

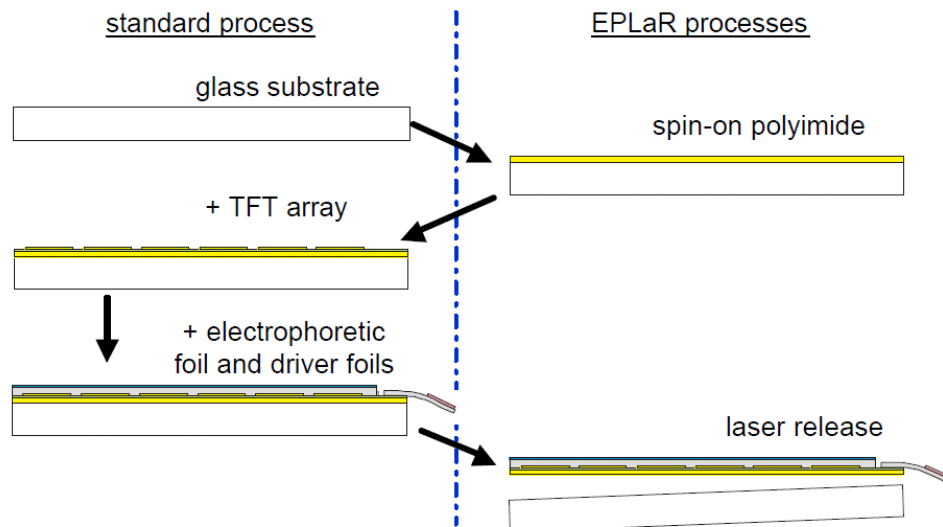


Figure 1.15: Basic Process Flow of the EPLaR Process (The Society for Information Display 2011)

Like the SUFTLA process, the EPLaR process main disadvantages are the cost and processing time of the laser release process as substrate size increases. The maximum

process temperature is set by the glass transition temperature of the polyimide. In addition, the polyimide may not be desirable for applications where visible light must shine through the substrate as polyimide films tend to have an orange tint.

FLEX UP

FLEX Universal Plane Substrate (UP) process was developed by ITRI out of Taiwan. Similar to the EPLAR process, the FLEX UP process uses slot die coating to cast polyimide as the base substrate. The adhesion strength of the polyimide to traditional borosilicate display glass is quite high and precludes an easy successful mechanical debond. However, one benefit of the high adhesion strength is that the substrate is less likely to debond from the carrier during processing.

In order to enable a satisfactory debond, an organic release layer (typically PMMA based) is applied to substrate prior to the polyimide coat. However, the release layer is not applied to the whole substrate as a small picture frame is left around the edge of the glass substrate carrier to encourage the edges to remain bonded to the substrate throughout the process.

After the device layers are fabricated, the backplane is cut inside the release layer picture frame and is removed via suction cups. The release layer remains bonded to the glass carrier substrate, which can now be reclaimed if desired.

Bond/Debond

The fourth option, known as the bond/debond or temporary binding process, involves processing a flexible substrate bonded temporarily to a rigid carrier. The basic process flow for the bond process is shown in Figure 1.16 (Raupp, et al. 2007). A temporary adhesive is spin-coated on to a rigid carrier. If the adhesive is thermally cured,

a bake usually follows the spin process. The flexible substrate is then mounted to the adhesive-coated carrier through a toll laminator. The adhesive is cured either by UV exposure or by baking or a combination of both. The processing of the TFTs proceeds as described in Section 1.4. The maximum processing temperature depends on the glass transition temperature of the substrate.

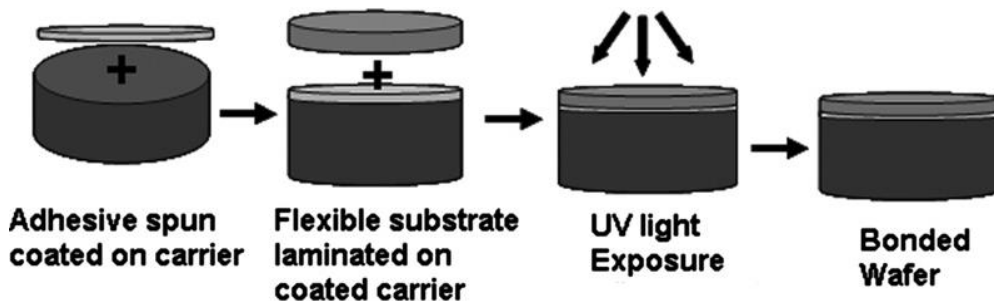


Figure 1.16: Bond Process Flow

The rigid carrier suppresses the bowing of the flexible substrate during processing to provide the requisite dimensional stability during device fabrication. Following device fabrication, the flexible substrate can be debonded from the rigid carrier to yield a flexible display.

The main advantage of the bond/debond process is that the process requires little additional investment to an already existing display fab. Unlike the SUFTLA and EPLaR processes, the bond/debond process is scalable to larger area substrates without significant alterations to the process. The main disadvantage of the bond/debond process is related to controlling the substrate deformation (i.e., warp and bow), which can cause wafer handling and pattern alignment issues, substrate distortion, and in extreme cases delamination of the flexible substrate during processing. However, Haq, et al., has

demonstrated a suitable bond/debond process that is capable of effective processing up to 200°C (Haq, et al. 2010). The present work utilizes the bond/debond process for the fabrication of flexible back planes.

There are many additional issues related to processing of flexible substrates irrespective of the technique used for handling the flexible substrates, including substrate defectivity, low melting temperature of the substrate, and substrate deformation during processing. These issues can severely limit the performance of electrical devices fabricated on flexible substrates. For example, the current technology of choice for active matrix LCD displays is hydrogenated amorphous silicon (a-Si:H). In commercial flat panel display TFT array fabrication, the amorphous silicon active layer as well as most of the dielectric layers is deposited at temperatures in excess of 300 °C on rigid glass substrates. This relatively high processing temperature allows for the optimal drive performance and device longevity as discussed in Section 1.4. The low melting temperature of plastic substrates generally prohibits processing above 200 °C; resulting in a lower performance, less stable a-Si film. Therefore, it would be desirable to explore a TFT technology that could be deposited at a lower temperature compatible with transparent colorless plastic substrates, but still demonstrate high performance and stability and be deposited over a large area in a production environment. One potential replacement for a-Si:H is transparent oxide semiconductors, which is the focus of this dissertation.

Mixed Metal Oxides

Transparent oxide semiconductors have drawn considerable attention due to their electrical (high mobility in the amorphous phase) and optical (> 90% visible light

transmission) properties (Hosono, Yasukawa and Kawazoe, Novel Oxide Amorphous Semiconductors: Transparent Conducting Amorphous Oxides 1996) (Itagaki, et al. 2008) (Chiang, et al. 2005). The term “transparent oxide semiconductors” covers a wide range of metal oxides including those of gallium, indium, zinc, aluminum, zirconium, hafnium, and tin that exploit their spherically symmetric s orbital conduction bands to produce their attractive properties. The spatial spread of the vacant s orbital allows direct overlap between neighboring metal atoms resulting in higher mobility than the sterically hindered hybrid sp^3 orbitals of amorphous silicon. Soon after their discovery, tremendous interest was generated in examining oxide semiconductors as a replacement for a-Si:H in the fabrication of thin film transistors (TFTs) for active matrix flat panel displays (Y. Kuo, Thin Film Transistors Materials and Processes, Volume 1: Amorphous Silicon Thin Film Transistors 2004) due to their improved saturation mobility (H. Hosono, Ionic Amorphous Oxide Semiconductors: Material Design, Carrier Transport, and Device Application 2006) (Nishii, et al. 2003) and threshold voltage stability (Jeong, Yang, et al. 2008) (Chong, Jo and Lee 2010) in comparison to a-Si:H. This increased mobility allows for the shrinking of the TFTs that control the individual pixels of the display and subsequently allows for the creation of higher resolution displays with improved yield.

Gate Dielectric

The gate dielectric is a key component of the TFT as its thickness and dielectric constant determine the electric field strength, which influences the source to drain current with thinner material and higher dielectric constant being desired. However, the gate dielectric material at the mixed metal oxide interface also is critical to the threshold voltage stability, especially under illumination.

Kwon, et al. (Kwon, Jung, et al. 2010) explored the negative gate bias illuminated temperature threshold voltage stability of HIZO (10:56:34 Hf:In:Zn atomic ratio) when using a bilayer gate dielectric. The gate dielectric thickness of 40 nm total thickness was maintained. In all cases, the first 35 nm of gate dielectric was PECVD SiN grown at 350°C. The interfacial layer, which is in direct contact with the active layer, was varied between 5 nm depositions of PECVD SiN (also grown at 350 °C), PECVD SiO₂ (grown at 350 °C), ALD grown AlO, and ALD grown HfO. The results demonstrated that the devices with interfacial SiO₂ (-0.97 V shift after 3 hours, VGS = -20, VDS = 10, T = 60 °C, P = 1 atm, 100% N₂ atmosphere) and AlO (-1.9 V shift) were more stable than SiN (-11 V shift) and HfO (-15 V shift). The results suggest that the mechanism for the threshold voltage instability is tied to photogenerated hole trapping at the gate dielectric interface. The photogenerated electrons are pulled out the drain by the applied positive voltage at the drain combined with the negative gate voltage forcing the electrons toward the back channel. The resultant hole becomes trapped at the interface or is injected into the gate dielectric, enhancing the applied field and thus lowering the threshold voltage.

The injection of photogenerated holes is enhanced in SiN due to its smaller band gap and smaller valence band offset resulting in a smaller barrier to hole injection. The valence band offset for HfO is higher than SiN (1.3 eV vs. 0.15 eV), yet the stability was worse. Kwon hypothesized that the hole injection mechanism was enhanced by Poole–Frenkel trapping (attributed to poor dielectric quality), which accelerates the injection of holes through the barrier. The high quality and large band gap of the ALD AlO and PECVD SiO₂ minimized hole injection into the gate dielectric, enabling an improvement in the illuminated bias stress behavior.

Another issue with high-k gate dielectric is Coulomb scattering in the channel due to defects in the high-k gate dielectric. Park, et al (Park, et al. 2009) demonstrated that a dual gate dielectric layer (PECVD SiN capped with ALD TiO) resulted in a lower mobility than the single layer PECVD SiN devices. Park demonstrated that as the TiO layer thickness increased, the mobility decreased. The mobility was enhanced by increasing the temperature, leading Park to conclude that the mobility degradation in the TiO capped devices resulted from Coulomb scattering. The SiN devices demonstrated the opposite behavior, suggesting that phonon scattering was the primary mobility degradation mechanism at elevated temperatures. A plot of $d(\mu_{FE})/dT$ vs. TiO thickness suggested that there was an optimal thickness of TiO that would counteract the phonon degradation mechanism of the SiN resulting in a device whose mobility was stable with temperature.

One might wonder why the gate dielectric should not simply be composed of SiO₂ only. Since the dielectric constant is low (3.9), the gate dielectric film must be thinner than a SiN film (dielectric constant = 6.0) to achieve the same capacitance and thus the same drive current. However, the thinner gate dielectric has a higher vertical electrical field. Ji, et al. (K. H. Ji, et al. 2011) showed that a SiN/SiO₂ (120 nm/80 nm, SiO₂ in contact with the IGZO) gate dielectric was more stable than a 120nm SiO₂ gate dielectric with a similar capacitance. Ji hypothesized that the higher electric field of the thinner SiO₂ only gate dielectric structure allowed for the injection of more photogenerated holes into the gate dielectric, resulting in a more negative threshold shift under illumination. Ji also compared a SiN only gate dielectric layer, which had the lowest electric field but demonstrated the largest threshold voltage shift. Ji hypothesized that the SiN valence

band offset with respect to IGZO was smaller (0.15 eV vs. 2.8 eV for SiO₂), allowing photogenerated holes to be more easily injected into the gate dielectric.

Active Layer Thickness

As mixed metal oxides are a defect semiconductor, the active layer thickness is an important parameter in determining device performance. Increasing the thickness of the active layer results in a slight increase in the mobility, but significantly decreases the threshold voltage, flattens the subthreshold slope, and increases the off current (Nakata, et al. 2012) as shown in Figure 1.17 due to the increase in the electron donor (oxygen vacancy) density. Additional negative gate voltage is required to fully deplete the thicker IGZO and adequately turn off the device.

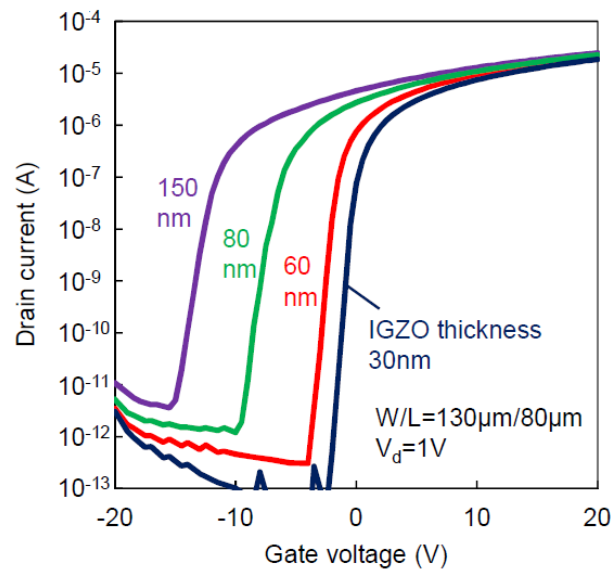


Figure 1.17: IDS-VGS Curve of TFT with various IGZO Active Layer Thicknesses (Nakata, et al. 2012).

The increased thickness does not result in an increase in the on current because only delocalized electrons near the channel participate. Therefore, the IGZO thickness should be as thin as possible to maintain adequate thickness control. However, as

described later, making the active layer too thin may allow anneal and plasma treatment processes to deleteriously affect the drive performance of the TFT by filling oxygen vacancies near the gate dielectric interface. Most research and technology development groups have used an active layer thickness between 30 nm and 60 nm.

Composition of the Mixed Metal Oxide

The choice of the active layer composition has a significant effect on the device characteristics. Probably the most common mixed metal oxide semiconductor reported in the literature is indium gallium zinc oxide (IGZO). Each of the metal oxide components of IGZO has a specific function. Indium oxide (In_2O_3) is a transparent conducting oxide. It is the overlapping spherical s-orbitals of the indium oxide that contribute the most to the high electron mobility of mixed metal oxide semiconductors. In comparison, carriers in amorphous silicon are transported through covalently bonded overlapping sp^3 or p orbitals. In the amorphous phase, the covalent bonds can be strained and impede transport. The s orbitals of the amorphous mixed metal oxide are insensitive to local strained bonds and thus, electron transport is not affected significantly (Kamiya, Nomura and Hosono 2009).

The zinc oxide introduces crystalline disorder into the mixture due to its hexagonal wurtzite structure. Indium oxides typically exist in bixbyite-type cubic crystals. When sufficient concentrations (~1:1 atomic ratio is common) of both oxides are present, no single structure can dominate, which results in the formation of an amorphous film. Amorphous films are desirable because they can be atomically smooth and do not have grain boundaries that can impede device performance (J. S. Park, K. S. Kim, et al.

2009). The role of the zinc oxide is not purely structural, as zinc oxide also contributes to the high mobility of electrons in IGZO.

The gallium oxide introduces stability with respect to oxygen vacancies. Gallium-oxygen bonds are stronger than zinc-oxygen or indium-oxygen bonds. The gallium suppresses the formation of oxygen vacancies, which acts to decrease the electron mobility, but improves the long-term stability of the device (Nomura, Takagi, et al. 2006). In spite of the vacancy suppression, it is still possible to fabricate a device with a field effect mobility of $10 \text{ cm}^2/\text{V}\cdot\text{s}$ with a V_T less than 1 V after 10 000 h of gate bias stress (Jeong, Yang, et al. 2008). Much research is being focused on the choice of the vacancy suppressor. Aluminum (Nomura, Takagi, et al. 2006), zirconium (J. S. Park, K. S. Kim, et al. 2009), and hafnium (C. J. Kim, et al. 2009) have all shown significant decreases in mobility with a significant improvement in the long-term stability of the device.

Some of the key device parametric results along with the maximum process temperature are shown in Table 1.2. Included in the table are the current results for the a-Si TFT process at the Flexible Electronics and Display Center (FEDC) for comparison and recent “state of the art” results that have been published.

Due to concerns of the large range availability of gallium and indium, some groups, such as John Wager’s group at Oregon State University, have chosen to focus on zinc tin oxide (ZTO) (Chiang, et al. 2005). The performance of ZTO is comparable to IGZO, but requires a high temperature anneal (between 300°C and 600°C) in order to achieve the same performance.

Table 1.2: Comparison of Mixed Metal Oxide TFT Performance for Various Materials

	μ_{sat} ($\text{cm}^2/\text{V-S}$)	V_T shift	V_T stress (s)	Max Process T ($^{\circ}\text{C}$)
a-Si:H (Kim, et al. 2010)	0.77	0.6	30000	350
FEDC a-Si:H (Kaftanoglu, et al. 2011)	0.7	10.4	10000	200
IGZO (Sato, et al. 2009)	11	0.47	10000	250
ZrInZnO (J. S. Park, K. S. Kim, et al. 2009)	3.9	1	216000	350
HIZO (C. J. Kim, et al. 2009)	9.3	0.43	57600	250
ZTO (Triska, et al. 2010)	13.3	8	100000	400

Etch Stop Layer

Passivation of the mixed metal oxide backchannel is crucial to the device stability of the TFT. In some reports, a passivation layer, defined as an “etch stop” layer, has been

deposited before the source/drain metal is deposited to protect the exposed back channel surface of the $\text{In}_2\text{Ga}_2\text{ZnO}_7$ from damage during the patterning of the source/drain metal. Jeong, et al. (Jeong, Yang, et al. 2008) studied passivated (i.e., with etch stop) and unpassivated (see Figure 1.18) bottom gate structures and found that the threshold voltage of the unpassivated structures would shift 8 V after 10 hours under positive gate bias stress ($V_{DS} = 0 \text{ V}$ and $V_{GS} = 15 \text{ V}$). Jeong's group found that the threshold voltage shift was related to the absorption of O_2 during forward bias operation, which was confirmed by adjusting the O_2 partial pressure during the test. The electronegative oxygen atoms then bonded to a depleted metal cation by stealing an electron and thus increasing the threshold voltage. The oxygen atom would desorb when the device was shut off, leading to a threshold voltage recovery.

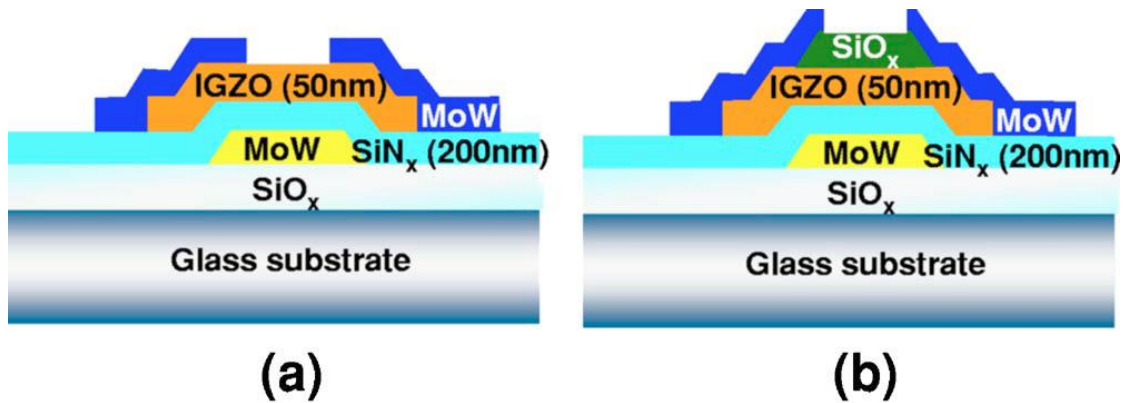


Figure 1.18: Passivation Study Structures Used by Jeong: (a) Nonpassivated Bottom Gate and (b) "Etch Stop" Bottom Gate (Jeong, Yang, et al. 2008)

Jeong investigated three potential etch stop layers including an unspecified photoacryl material, PECVD SiO_2 , and a "dense" PECVD SiO_2 film, which were deposited after the active layer was patterned, but before the molybdenum source/drain metal was sputter deposited. The photoacryl layer etch stop was shown to be no better

than no etch stop. It was surmised that photoacryl layer was too permeable to water ($1 \text{ g/m}^2 \text{ WVTR}$) and oxygen ($3 \text{ mL/m}^2 \text{ O}_2$ transmission rate) to be an adequate passivation layer.

The standard 100 nm thick PECVD SiO_2 film demonstrated only a 2V threshold voltage shift under the same stressing conditions as the unpassivated device. The threshold voltage shift was reduced to 0.01 V by implementing a “denser” 100 nm PECVD SiO_2 film. Jeong attributes the improved stability to the water and oxygen barrier properties of the SiO_2 and suggests that water vapor transmission rate (WVTR) and oxygen transmission rate are important metrics of a good passivation layer with respect to positive gate bias stress.

Source Drain Metallurgy

A wide range of materials have been selected for the source drain metallurgy including: molybdenum, aluminum, tantalum, titanium, gold, indium zinc oxide, indium gallium zinc oxide, and indium tin oxide. Molybdenum and titanium are the most common metals employed because of their low contact resistance ($\sim 100 \Omega$ at $V_{GS} = 20$ and $L = 15 \mu\text{m}$), although aluminum and copper have also been presented as potentially worthy options (Kima, et al. 2010). However, MoO_3 , which can form at the IGZO/SD interface, can contribute to negative threshold voltage shifting due to oxygen vacancies generated in the creation of MoO_3 (J.-Y. Kwon, K. Son, et al. 2010). One additional advantage of titanium is that it can be annealed to form a TiO contact layer that suppresses carrier generation (i.e., the formation of oxygen vacancies via reaction with the source drain metal).

Shimura from Hideo Hosono's group demonstrated that the contact resistance between the source/drain metal and the oxide semiconductor increased with increasing work function of the source/drain metal (Shimura, et al. 2008). Shimura compared PLD-deposited IZO and ITO and evaporated silver, indium, titanium, gold, and platinum by patterning the various metals to form pads of variable spacing on blanket-coated IGZO glass substrates. Gold and platinum were shown to have non-linear I-V characteristics demonstrating Schottky like contacts. ITO and IZO contacts were shown to be ohmic.

Barquinha, et al. (Barquinha, et al. 2008) demonstrated that the contact resistance between the source/drain metal and the oxide active material could be decreased by annealing in a Barnstead Thermolyne F21130 tubular furnace, with a constant flow of nitrogen, at 250 °C for one hour after the device fabrication was completed. The timing of the anneal was important as annealing before the source/drain deposition did not have as much of an effect on the drive characteristics. The improvement in the drive characteristics were attributed to a decrease in the contact resistance between the active material and the source/drain material by interdiffusion of the two layers. TOF-SIMS plots demonstrate a significantly broader intersection between the source/drain material (titanium, in this case) and the IGZO active layer. Other source/drain materials such as IZO, molybdenum, and a titanium/gold bilayer (with Ti in contact with the IGZO) using unpassivated top gate TFTs. In the case of molybdenum, no change was noted in the TOF-SIMS plot indicating that no interdiffusion was taking place between the molybdenum and the IGZO layer. The contact resistance was a factor of two (10 k Ω vs. 20 k Ω) lower for titanium when compared to molybdenum.

Passivation with Etch Stop Layer

Although the etch stop layer and the source/drain metal are the only layers in direct contact with the active material, some publications have demonstrated that the source/drain metal passivation can affect the device performance. Park, et al. (J. Park, et al. 2010) reported the influence of SiO₂ and SiN passivation (100 nm thick in both cases) on the negative bias stability of HIZO TFTs under illumination. The SiN passivated devices exhibited higher mobility (14.9 cm²/V-s vs. 6.6 cm²/V-s), but a more severe negative threshold voltage shift (-4.5 V vs. -2.0 V) under negative gate bias illuminated stress conditions (LCD light source at 200 Lux, 5000s, VGS = -20, VDS = 10). Hydrogen from the NH₃ and SiH₄ source gases was incorporated into the SiN PECVD passivation layer and diffused into and through the SiO₂ etch stop layer, through the HIZO active layer to the gate dielectric interface. The hydrogen atoms in HIZO act as an electron donor, thus reducing the threshold voltage, while the atoms at the gate dielectric interface (PECVD SiO₂) act as hole traps thus further shifting the threshold voltage in the negative direction when the device is under illumination.

Passivation without Etch Stop Layer

Some groups have demonstrated results without using an etch stop layer by employing a post source/drain metal etch treatment that oxidizes the exposed active material back channel surface prior to passivation deposition. For example, Jae Chul Park, et al. (J. Park, S. Kim, et al. 2008) demonstrated that reliable device performance was still possible without an etch stop layer if the exposed backchannel surface is treated with an N₂O plasma prior to the deposition of the SiO₂. The 60 s overetch of a SF₆/O₂ dry etch utilized to etch the Mo source/drain layer was responsible for creating a 3 nm thick

In-rich layer on the back channel surface by scavenging oxygen. The dry etch was used because the Mo wet etch would chemically attack the IGZO layer. The N₂O plasma was carried out at 150°C for 5 minutes and then followed in situ by the SiO₂ final passivation deposition.

The gas flow rates during the SiO₂ PECVD passivation deposition can have a significant effect on the threshold voltage of the completed devices. Kwon, et al. (J. Y. Kwon, et al. 2009) demonstrated that a N₂O:SiH₄ flow ratio of 10 during the deposition of a 500 nm thick passivation layer resulted in a TFT with a threshold voltage of -20 V after a 200°C, 1 hour anneal in air. Increasing the ratio to 55 increased the threshold voltage to -11 V. The threshold voltage did not become positive until the flow ratio was increased to 100 (2500 sccm N₂O: 25 sccm SiH₄).

Mixed Metal Oxide on Flexible Substrates

Although the performance of mixed metal oxides is superior to a-Si:H, the maximum process temperature typically exceeds 250°C. It is important to note that the temperatures listed in Table 1.2 are only the maximum reported temperature. In most cases, the temperature of the active layer post deposition anneal is quoted, but the temperature of the PECVD steps is not listed. Thus, it is not surprising that reported performance on flexible substrates has lagged behind the results presented in Table 1.2. In addition, most reported results have used lift off processes or materials that would be incompatible with commercial display manufacturing.

IGZO TFTs have been fabricated on polyethylene terephthalate (PET) substrates (Lim, et al. 2008) using the basic device structure shown in Figure 1.19. The maximum process temperature for the process was listed as 90 °C for the PECVD of the gate

dielectric. Most of the layers were patterned using lift off. In, addition, the source/drain metal is IZO, which is too resistive ($60 \Omega/\square$), for use in large area displays.

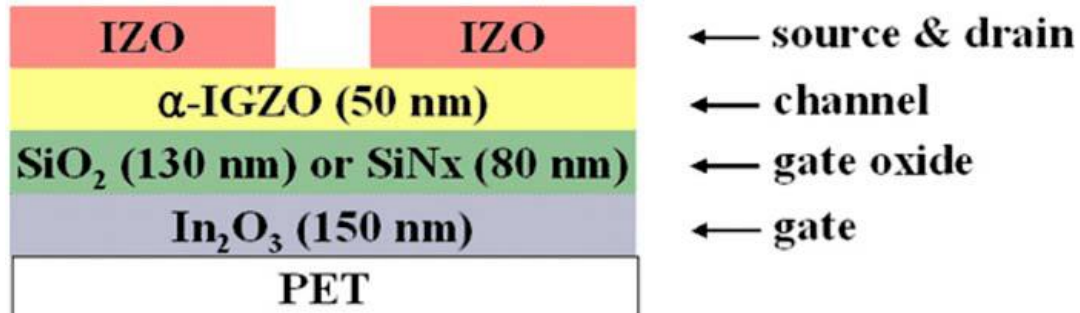


Figure 1.19: Basic Device Structure Presented by Lim, et al. (Lim, et al. 2008)

The device performance was comparable to the results presented in Table 1.2, with μ_{sat} of $12.1 \text{ cm}^2/\text{V}\cdot\text{s}$ and a V_T of 1.25 V. However, the leakage for these devices was on the order of 5 nA, which is approximately a factor of 1000 greater than desirable. In addition, device stability was presented in terms of shelf life, which means that the devices were not stressed for many minutes or even hours as they would during the regular operation of an electronic device. Instead, the devices were placed on a shelf and left to age and tested over a 6 month interval. The device performance did not significantly shift, which is desirable, but unremarkable.

Jackson, et al. (Jackson, Hoffman and Herman 2005) demonstrated ZTO TFTs fabricated on stainless steel flexible substrate with a saturation mobility of $14 \text{ cm}^2/\text{V}\cdot\text{s}$. The maximum processing temperature was $300 \text{ }^\circ\text{C}$ for the SiON gate dielectric. In addition, a $250 \text{ }^\circ\text{C}$ anneal was performed after the deposition of the ZTO active layer. The more difficult patterning steps, specifically the ZTO patterning and the ITO source/drain contact, were performed by shadow masking during the deposition cycle. Although the saturation mobility is comparable to other groups processing on rigid substrates, the

threshold voltage is -16V and the leakage current is 0.1 nA. The extreme negative value for the threshold voltage is undesirable because of the large negative voltage that would be required to turn off the device. With a sufficiently negative gate voltage, any display fabricated with this technology would have low contrast.

Nomura, et al. (Nomura, Ohta, et al. 2004) demonstrated IGZO TFTs with the structure shown in Figure 1.20 on polyethylene terephthalate (PET) sheets. Like Jackson, Nomura's group patterned most of the layers via shadow masking. The gate and source drain in this case are both ITO, which could not be used in a large area display.

The saturation mobility reported by Nomura ranged from 6 to 9 cm²/V-s on PET substrates. The leakage current for the devices was approximately 100 nA, which is far too high for use in a practical electronic device. The threshold voltage stability was not reported.

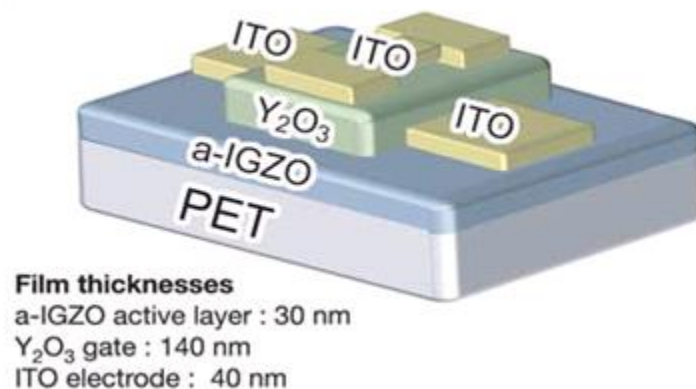


Figure 1.20: Flexible IGZO TFT Structure Presented by Nomura (Nomura, Ohta, et al. 2004)

Conclusions

Although there have been many reports on mixed metal oxide device and their incorporation on flexible substrates, most of the work was conducted using processes and/or materials that would not be suitable for large scale production on large area displays. There appear to be many challenges in incorporating mixed metal oxides into a manufacturable process that have not been solved. While the drive performance, specifically the saturation mobility, of device fabricated on flexible substrates is comparable to the performance of the same devices on rigid substrates, most of the work presented has demonstrated poor off characteristics and limited or no long term V_T stability data. Chapters 2 and 3 will address some of these manufacturing issues and will present manufacturable solutions to the problem illustrated in Chapter 1. The work presented makes use of the bond/debond technique for processing on flexible substrates, since the bond/debond process would require little additional capital equipment to be incorporated into an already existing display manufacturing facility.

CHAPTER 2 HIGH PERFORMANCE MIXED OXIDE SEMICONDUCTOR TRANSISTORS ON FLEXIBLE POLYETHYLENE NAPHTHALATE SUBSTRATES

Introduction

The integration of high performance mixed metal oxide TFTs on flexible substrates requires the optimization of many individual semiconductor processes. The optimization process focused on the following processes: gate, gate dielectric, active layer deposition, active layer etching, source/drain metallurgy, and interlayer dielectric (ILD). These processes were optimized systematically through Design of Experiments (DOE) by fabricating transistors and evaluating the electrical performance.

An inverted staggered trilayer design similar to that previously described by Kaftanoglu et al. (Kaftanoglu, et al. 2011) was selected for the TFT as shown in Figure 2.1. All processing conditions were selected to be compatible with fabrication of devices on flexible poly (ethylene naphthalate) (PEN) substrates. Devices were initially fabricated on silicon substrates capped with 300 nm of thermal SiO₂ to allow for cross-sections of the etch processes to be examined more easily.

The initial deposition baseline process conditions and the composition of the ZIO target were chosen based on previous results published by Itagaki (Itagaki, et al. 2008). The device parameters of transistors fabricated with this process were used as a baseline to compare future experimental results. In total, 60 wafers were processed under this baseline condition with 600 TFTs characterized. Once the baseline was established, process improvements were sought through Design of Experiments.

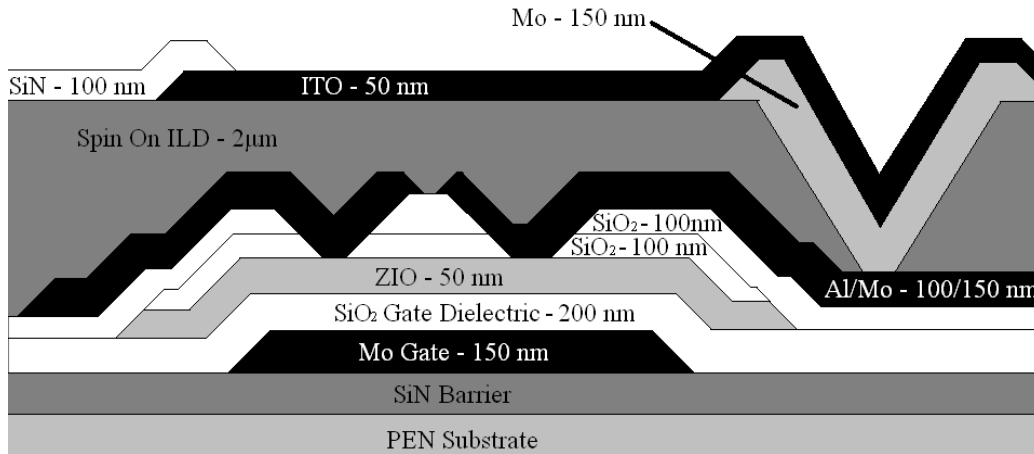


Figure 2.1: Inverted Staggered Trilayer TFT Structure with Active Mesa Sidewall Passivation

Transistor performance data are measured for 20 individual test transistors with a 96- μm channel width W and 9- μm channel length L ($W/L = 10.67$) distributed at different locations on each wafer; every wafer in every lot is tested. We focused on the following seven key TFT performance parameters: drive current, effective saturation mobility, threshold voltage, subthreshold slope, hysteresis, and drain-source leakage current (off current), which served as responses in the DOE analysis. In addition, the performance of these parameters was also monitored with respect to electrical stress. The completed backplanes could be fabricated into bottom emitting OLED displays to visibly and tangibly demonstrate the results of the process development in an integrated functioning array device..

Substrate

Most of the initial development was completed on thermally oxidized 150 mm silicon wafers. The substrates were nominally 675 μm thick with a crystal orientation of $\langle 100 \rangle$ and a bulk resistivity between 5-30 $\Omega\text{-cm}$. The oxide layer was 300 nm thick. The

function of the oxide layer was to insulate the gate metal from any potential parasitic effects of the silicon substrate.

Experiments were also conducted on flexible polyethylene naphthalate (PEN) substrates. The PEN substrate (125 μm thick) was obtained from DuPont Teijin Films (trade name Teonex Q65A) and was temporarily bonded to a 640 μm thick alumina carrier (CoorsTek) for processing (Haq, et al. 2010).

A UV curable adhesive (Product no WFP20141- 94B) was obtained from Henkel Corporation and spin-coated on to the alumina carrier. A protective film (SEC Blue Low Tack Squares P/N 18133-7.50) was applied to the PEN prior to lamination to protect the processing side of the PEN from particles from the process. The PEN was cut approximately to a diameter of 144 mm to prevent the PEN from overlapping the edge of the alumina carrier and interfering with automatic flat finding modules in some of the process equipment.

The flexible PEN substrate was laminated to the adhesive-coated alumina carrier using a Western Magnum hot roll laminator. The adhesive was cured by exposing the adhesive to UV light (315-400 nm wavelength) through the transparent PEN substrate for 20 s in a Dymax curing unit. The bonded substrate was baked under vacuum for one hour at 180 $^{\circ}\text{C}$ to test the viability of the bond to withstand the TFT fabrication processes.

The undersized PEN substrate results in a small amount of residual adhesive left at the edge of the alumina carrier. The adhesive is sensitive to many of the standard TFT processes and must be removed or else the material will embrittle and break off, forming particulates. The protective low tack tape is used as a mask to protect the PEN while the exposed adhesive is removed via oxygen plasma. The blue tape is then removed from the

PEN substrate. The wafer is then cleaned in soapy solution consisting of 80 mL of Detergent 8 and 4L of DI water to facilitate desorption of contaminants followed by a rinse in a quick dump rinser (QDR) and spin dry in a spin rinse dryer (SRD). Following the rinse, a 300 nm thick layer of SiN is deposited on the surface to protect the PEN from future processing steps. The substrate is now ready for thin film processing.

The PEN/adhesive/alumina substrate system is designed to enable processing in typical semiconductor FAB equipment without handling issues associated with substrate deformation or photolithography alignment registration issues as described previously by Haq, et al. (Haq, et al. 2010). Device performance on PEN was generally equivalent to the device performance on silicon. As the process improved, small differences between devices fabricated on PEN and devices fabricated on silicon began to emerge due to significant reductions in the process variability. Therefore, 2-4 silicon wafers were always included in any PEN experiment to serve as a baseline.

Gate

The TFTs were fabricated with an inverted staggered design, meaning that the gate metal is deposited first. At the Flexible Electronics and Display Center, there are several choices for the gate metal including: molybdenum, aluminum doped with 1% silicon by mass, “pure” aluminum, tantalum, ZIO, IGZO, and ITO. The mixed oxides ZIO, IGZO, and ITO were all eliminated because of their high sheet resistance ($> 80 \Omega/\text{square}$). The gate itself does not need to carry current; however there are other locations with a contact down to gate that do carry significant current.

Molybdenum was chosen because of the ease of sloping the sidewall during etch and the smoothness of the surface compared to aluminum and tantalum. A smooth

sidewall is important to ensure good step coverage of the subsequent thin film deposition. Inadequate step coverage can lead to drain to gate shorts, which can adversely affect the performance of a display TFT array.

A rough gate metal surface followed by conformal deposition by the gate dielectric and active layer could result in the artificial lengthening of the channel by scattering. If non-conformal deposition occurs, the gate could make contact with the active layer resulting in a short.

The molybdenum gate metal was deposited to a thickness of 150 nm. At this thickness, the sheet resistance is 1.0 Ω /square, which is more than adequate to handle the current flowing through the molybdenum at the locations where power lines must drop down to the gate level to pass under other power lines.

Following the deposition step, the wafers were cleaned with a soapy mixture of Detergent 8 (5% by vol.) and DI water in an ultrasonic tank. The wafers were then rinsed in a quick dump rinser (QDR) with DI water and dried in a spin rinse dryer (SRD).

After cleaning, the wafers were patterned with a photoresist (AZ Materials 5214E) layer. The wafers first pass through a vacuum oven to provide a thin coat of hexamethyldisilazane (HMDS) on the surface. The photoresist was spun to a thickness of 1.5 μm . Following the spin, the wafers were baked on a hot plate at 105 $^{\circ}\text{C}$ for 60 s. The spin and bake were performed on a Rite Track 8800 automated cassette to cassette track coater. The wafers were given a unique serial number near the wafer flat at this step using an SSI-1000 exposure tool that exposes small circular dots. The wafer is translated through the field of view to produce characters. The main gate pattern is defined by UV light exposure in a Canon MPA 600-MF projection aligner. The stepper magnification

ratio is 1:1 meaning the exposed pattern is the same dimension as the pattern on the mask. The exposure energy density was 140 mJ/cm^2 . The wafers were then puddle developed for 60 seconds using AZ MIF 300 developer followed by a final hard bake at $140 \text{ }^\circ\text{C}$ for 60 s. This final reflow bake partially melts the resist resulting in the formation of rounded features due to surface tension on the melted resist.

The rounded features have sloped edges that can be easily transferred to the underlying material through a non-selective etch process. In this case, the selected etch process is dry etching. A dry etch allows for greater control of the sidewall profile and critical dimension (CD) than wet etching. The dry etch was conducted in an Applied Materials 8330 (AMAT 8330) batch etch system. The AMAT 8330 can etch 18×150 mm wafers at a time.

Gate Dielectric and Passivation

There were three candidate materials (SiO_2 , SiN , and Al_2O_3) for thin film dielectric layers. These three materials were evaluated by fabricating metal-insulator-metal (MIM) capacitors and testing the breakdown characteristics of the insulator. The materials were then inserted into the TFT process where the output and transfer characteristics were compared.

To dry etch the dielectric layers, a reactive ion etch (RIE) (Tegal 901) was utilized operating at 200 Watts, 400 mTorr, nominal substrate temperature of $40 \text{ }^\circ\text{C}$, and a gas feed consisting of 10 sccm of CHF_3 and 20 sccm of O_2 .

Active Layer Deposition

A ceramic target with a composition of 60% zinc oxide and 40% indium oxide by mass, similar to the composition reported by Itagaki (Itagaki, et al. 2008), was utilized for

deposition of the active layer in the initial development work. The ZIO was deposited using DC reactive sputtering (MRC 603 sputtering system) operating at 200 W (0.439 W/cm^2) at a pressure of 6 mTorr and a nominal substrate temperature of $40 \text{ }^\circ\text{C}$. A mixture of argon and oxygen (2% O_2) was used as the deposition feed gas.

The initial deposition baseline process conditions and the composition of the ZIO target were chosen based on previous results published by Itagaki. The process conditions for this baseline condition were 6 mTorr operating pressure, 200 W operating power, 4 sccm of O_2 and 200 sccm Ar. In total, 60 wafers were processed under this baseline condition with 600 TFTs characterized.

Active Layer Etching

Photolithographic patterning of the layers was performed using a Canon MPA-605 aligner with AZ Materials 5214 photoresist. After etching, the photoresist was stripped in a Gasonics L3510 downstream microwave plasma asher.

To dry etch the ZIO active layers, the AMAT 8330 was operated at 1000 W (0.314 W/cm^2), 10 mTorr, a nominal substrate temperature of $95 \text{ }^\circ\text{C}$, and a feed gas consisting of 100 sccm of HCl, 20 sccm of O_2 , and 10 sccm of CH_4 . A similar dry etch process was reported by Saia, et al. (Saia, Kwanswick and Wei 1991) for indium tin oxide (ITO).

Two wet etch processes were explored for the patterning of the ZIO active layer. The first consisted of a commercial buffered HF (10% by volume) and deionized water mixture (Ultra Etch NP 10:1 manufactured by KMG Electronic Chemicals). The buffered hydrofluoric acid mixture was also used to etch silicon dioxide dielectric layers. Diluted

HF is commonly used to etch zinc oxide based materials during TFT fabrication (Cheong, et al. 2008, Jeon 2008, S. K. Park, et al. 2009, K. H. Kim, et al. 2011).

The second wet etch consisted of a mixture of 37% HCl (45% by volume), 69.5% HNO₃ (5% by volume), and deionized water (50% by volume). This mixture is common in LCD manufacturing for the patterning of indium tin oxide (ITO) (Bahadur 1990) as it does not attack glass, which is a common substrate for display applications.

To characterize the structure of the devices, a field emission scanning electron microscope (FESEM, JEOL 6300) was employed. Samples on silicon wafers were cleaved to fit into the FESEM and gold coated in a Hummer 6.2 sputter system for 120 s to a thickness of approximately 15 nm. Cross-section samples were mounted in a sample holder with the cleaved side of interest facing the gold target while top-down samples were mounted with the processed side of the wafer of the wafer facing the target.

Contact Etching

A Mesa Passivation deposition follows the active layer etching. The mesa passivation is 100 nm thick and protects the exposed sidewall of the metal oxide active layer from future processing. The layer is composed of PECVD SiO₂ and uses the same process conditions described in the gate dielectric section.

In the inverted staggered trilayer device setup, contacts must be opened to the gate and the metal oxide active layer. These two layers are at different levels meaning that the respective contacts' vias will be at different depths. In the a-Si process, separate masks were fabricated for the two contacts as the a-Si contact was the shallower via. Etching SiN or SiO₂ selectively with respect to a-Si is very difficult without using hydrofluoric acid (HF). Buffered HF does not etch a-Si, but the critical dimension (CD) of the contacts

can be blown out during the requisite overetch to open the deeper gate contacts. In order to preserve the CD of the active contacts, separate masks were used to open the active contact and gate contact.

This design feature was incorporated into the mixed oxide TFT process because the a-Si TFT mask sets were used to initially characterize the mixed oxide TFT performance. As stated in Section 2.1.4, the mixed oxide materials are vulnerable to buffered HF. Since buffered HF is not an option, dry etching must be used (Williams, Gupta and Wasilik 2003).

A controllable slope was obtained using the Tegal 901 RIE system. The pressure was set to 400 mTorr, the power to 150 W, the O₂ gas flow was set to 10 sccm and the CHF₃ was set to 20 sccm. The process was originally designed for a contact etch that opened on to ITO. It was determined that OLED diodes that were fabricated on ITO that had been etched by CHF₃ outperformed OLED diodes fabricated on ITO that had been etched by SF₆. It was reasoned that the carbon from the CHF₃ was scavenging oxygen from the surface of the ITO creating an oxygen deficient surface that reduced the contact resistance. Both the gate and active contacts are opened with the same process for the same duration in anticipation of combining the etch steps in a future design.

Source Drain Metallurgy

As with the gate metal, there is a large selection of materials available to choose from including: molybdenum, aluminum doped with 1% silicon by mass, “pure” aluminum, tantalum, ZIO, IGZO, and ITO. Initial experiments focused on molybdenum as the source/drain metal due to its usage by many groups pursuing metal oxide TFTs (Jeon 2008, J. Park, C. Kim, et al. 2008, Barquinha, et al. 2008). However, the sheet

resistance for molybdenum is $1.0 \Omega/\square$ which was determined to be too high for display applications based on simulations, especially as the display resolution increased beyond QVGA. In addition, these initial experiments only focused on fabricating TFTs without subsequent display builds, and therefore only required processing through source/drain metal. Additional layers are needed to fabricate the pixel anode. These additional layers require etching processes that are not highly selective to Mo.

Ideally, the source/drain layer should be resistant to fluorine plasmas as the next layer deposited (ILD) is $2 \mu\text{m}$ and is etched in an SF_6/O_2 plasma. Mo etches rapidly in this plasma process and would be easily removed during the overetch of the ILD. Therefore, it was decided to explore materials that are impervious to fluorine plasma. Two materials, ITO and Al with 1% silicon, were considered viable candidates because they were already qualified for use in the a-Si TFT process. However, a literature search indicated that Al/ITO contacts were undesirable due to the formation of insulating aluminum oxide at the interface (Lee, et al. 2002). In addition, Bahadur, et al. (Bahadur 1990) had noticed severe current crowding in the output characteristics at low drain voltage in devices fabricated with Al S/D contacts indicating the creation of a large barrier between the aluminum and the metal oxide active layer. Instead, it was decided to use Al in combination with an interfacial layer. In this experiment, Ta and Mo were chosen as the contact layers. An additional cell featuring ITO was also included.

The source/drain metal is deposited in a KDF 744 or an MRC 603 sputtering system. The initial development was performed using 150 nm of molybdenum sputtered at 1000 W at 6 mTorr with 100 sccm of Ar. TFTs using the standard molybdenum source/drain metal were compared with devices featuring ITO, a bilayer featuring 200 nm

of Al doped with 1% by wt. Si with a 50 nm Ta contact layer, and a bilayer featuring 200 nm of Al with a 150 nm Mo contact layer.

Interlayer Dielectric (ILD)

The PTS-R ILD process begins with the coating of a 100 nm thick SiO₂ wetting layer. A wetting layer is necessary because the solvents used to dissolve PTS-R are corrosive to aluminum. SiO₂ was chosen over SiN because the relative etch rate of SiO₂ is slower than both SiN and PTS-R. The SiO₂ is at the bottom of the via. During the etch, the PTS-R will be etched faster than the SiO₂ resulting in a shallow slope at the bottom of the via.

The PTS-R is syringe dispensed on to the SiO₂ using a manual syringe on a Rite Track 8800 coater track. The wafers are soft baked at 200 °C for 1 min to drive off most of the solvents and then cured in a Despatch Oven at 200 °C for 1 h. The PTS-R is then capped with a 100 nm SiO₂ layer to protect the PTS-R from the harsh etch chemistries of the later processes. AZ 9260 resist is spun to a thickness of 3.3 μm with a reflow bake at 140 °C to slope the sidewalls.

Pixel Anode

The pixel anode consists of a 150 nm molybdenum plug, 50 nm ITO layer, and 100 nm SiN Overglass passivation layer. The Mo plug serves as an interfacial layer between the aluminum source/drain metal and the ITO anode (Lee, et al. 2002) and a contact for the Mg/Ag OLED cathode metal. For top emitting OLED designs, the anode also serves as a reflector that blocks light from passing through the TFT and the substrate. The Mo deposition process was identical to the deposition of the gate metal. The metal is sputter deposited in a KDF 744 or MRC 603 sputter tool to a thickness of 150 nm. The

sheet resistance at 150 nm is $1 \Omega/\square$. The Mo plug was photo patterned and etched in the same manner as described in Section 2.2.2.

The ITO layer was reactively sputtered in a KDF 744 using 5000 W of RF power at a frequency of 13.56 MHz. The target is a ceramic target that is 90% indium oxide by mass and 10% tin oxide. The pressure was set to 3.5 mTorr by flowing 5 sccm of O_2 and 100 sccm of Ar. The ITO was etched using the same dry etch that was described in Section 2.4 for the active layer.

The ITO was capped with a 100 nm SiN passivation layer (Overglass) to define the active pixel area and to prevent dirt from bridging neighboring ITO anodes. The layer was etched using the same process described in Section 2.7 for the contact etch. Once the resist was stripped using the Gasonics L3510 ash process described previously, the samples were rinsed in the QDR and dried in the SRD. This final step completed the back plane fabrication process.

OLED Display Build

OLED backplanes feature two transistors and one capacitor in each pixel. The electrical schematic for an OLED pixel is shown in Figure 2.2

The display operates by “scanning” the gate voltage along one of the axes of the display. Voltage is applied to only one gate line at a time. The amount of time it takes for all of the gate lines to be activated determines the refresh rate. For example, a 60 Hz display will cycle through every gate line 60 times in 1 s. The gate voltage is set significantly above the source voltage (usually 12-15 V) to put the row select TFT (T1 in Figure 2.2) in the linear region. In this mode, T1 behaves like a variable resistor where the drive current is proportional to the source voltage. The source line voltage is adjusted

for each line during the gate scan and determines the amount of charge that will be stored to the capacitor. Since T1 is off during most of the cycle, a capacitor is needed to make sure that the OLED is lit for the entire cycle. The voltage applied to the gate of the drive TFT (T2 in Figure 2.2) is set by the voltage applied by V source during the gate scan. V drive is constant and is set to a value that places T2 in saturation (usually 12-15 V). In saturation, T2 behaves like a constant current source that is controlled by the gate voltage which is set by the source voltage applied to T1. OLEDs are current controlled diodes. As the current increases, the luminance of the OLED emitting materials increases. In a color display, blue, green, and red emitting materials can be deposited in adjacent pixels. By adjusting the current (and thus the luminance) of the adjacent pixels, one can create a wide gamut of colors. In this work a monochromatic flexible OLED was fabricated.

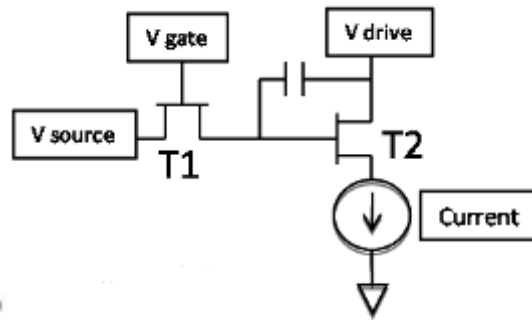


Figure 2.2: OLED Pixel Circuit Diagram

Gate Developments

The original etch process was developed for the FEDC's a-Si TFT process as described by Raupp, et al. (Raupp, et al. 2007) where adequate results were achieved when the thickness of the SiN gate dielectric was increased from 200 nm to 300 nm.

Initial experiments with the original gate etch combined with the 200 nm thick silicon dioxide gate dielectric demonstrated limited gate to source shorting at crossovers. The shorting was hypothesized to have originated from either pinholes in the silicon dioxide or inadequate step coverage of the silicon dioxide over the gate metal sidewall. Data presented in the gate dielectric section indicated that pinholes in the dielectric were unlikely so the gate metal etch profile was studied.

The step coverage of the SiO₂ gate dielectric and passivation layers was investigated by fabricating wafers through all processing steps until the contacts had been opened. At this point, the ZIO active layer is protected by the Mesa Passivation and the IMD and is only exposed where the source/drain contacts were opened. Six wafers processed with the standard gate metal etch were dipped in a mixture of 37% HCl (45% by volume), 69.5% HNO₃ (5% by volume), and deionized water (50% by volume). This mixture is common in LCD manufacturing for the patterning of indium tin oxide (ITO) and also etches ZIO. The HCl/HNO₃ mixture was selected because the etch rate of SiO₂ in the mixture is negligible. The contacts were opened to allow the mixture to attack the exposed ZIO to provide a visual reference. The wafers were submerged in the bath for 8 minutes and examined under a microscope. Figure 2.3 shows a microscope image after the dip.

The image shows that significant IGZO etching took place at the contact openings (expected) and at locations where the IGZO crossed over the gate metal. The IGZO was not etched along boundaries where there was no gate metal crossover, further supporting the hypothesis of inadequate step coverage over the gate metal. Additional wafers were processed through the full process and were examined in a JEOL 6100 field emission

scanning electron microscope (FESEM). Figure 2.4 demonstrates a typical gate metal crossover.

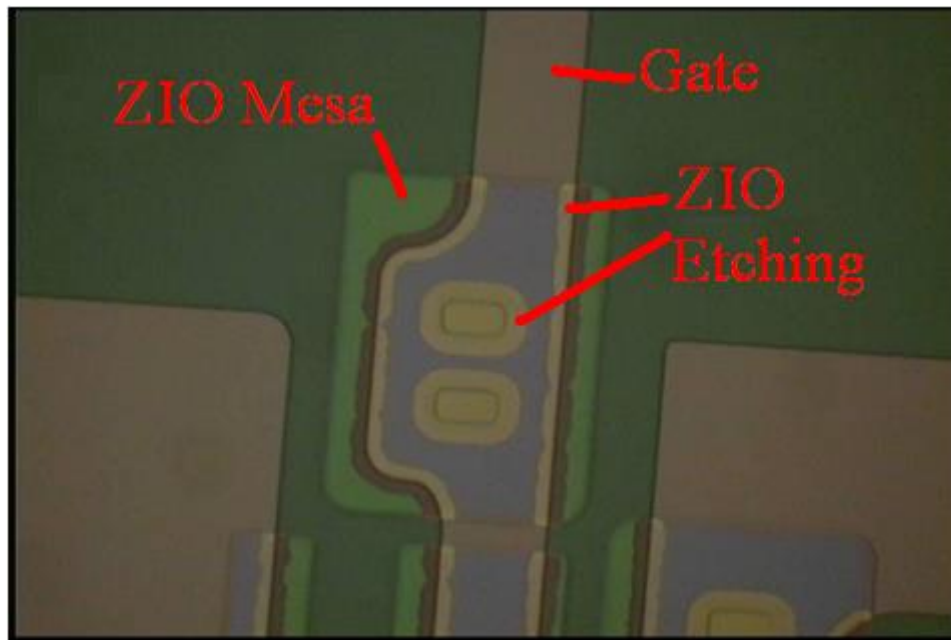


Figure 2.3: The ZIO Active Layer Has Been Attacked by the HCl/HNO₃ Mixture Where the Active Layer Crosses over the Gate.

The micrograph shows that there are voids present in the IGZO active and SiO₂ passivation layers. Although the voids in this micrograph do not extend completely to the gate in this particular micrograph, there is sufficient evidence to suggest that the coverage is inadequate.

It was decided to adjust the slope of the gate etch instead of altering the SiO₂ deposition process to improve the conformality of the deposition process. Changing the gate dielectric characteristics to improve step coverage could have unintended deleterious effects on the device performance. Changes to the gate metal etch sidewall profile would allow for improved step coverage without risking undesirable changes to the device performance.

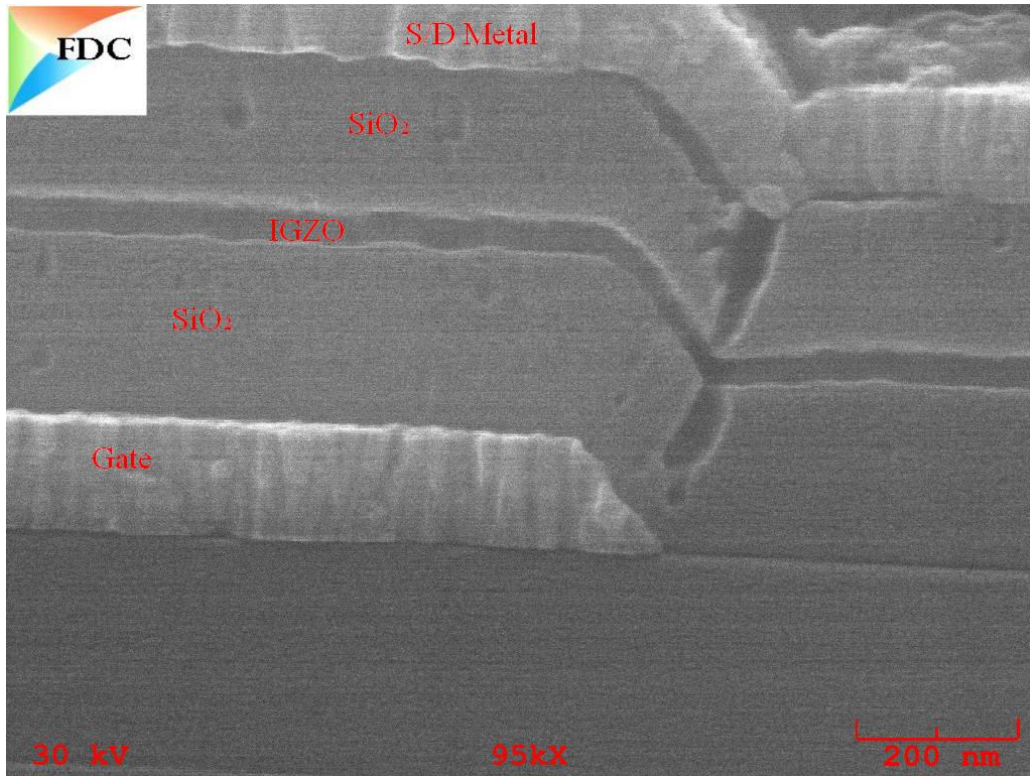


Figure 2.4: FESEM Micrograph Demonstrating Voids in the Gate Dielectric, IGZO Active, and Passivation Layers

The etched sidewall angle was decreased by simply increasing the oxygen to chlorine ratio from 1:1 (80 sccm: 80 sccm) to 6:1(90 sccm: 15sccm) while maintaining the pressure at 15 mTorr and power at 600 W. The increase in the oxygen concentration increased the photoresist erosion rate, resulting in a flatter sidewall profile as shown in Figure 2.5.

Devices fabricated with the new etch process did not show a statistically significant performance difference when compared to devices fabricated with the original etch process. However, the functional TFT yield increased significantly from 50% to 83%, as the number of source to drain shorts in the array decreased.

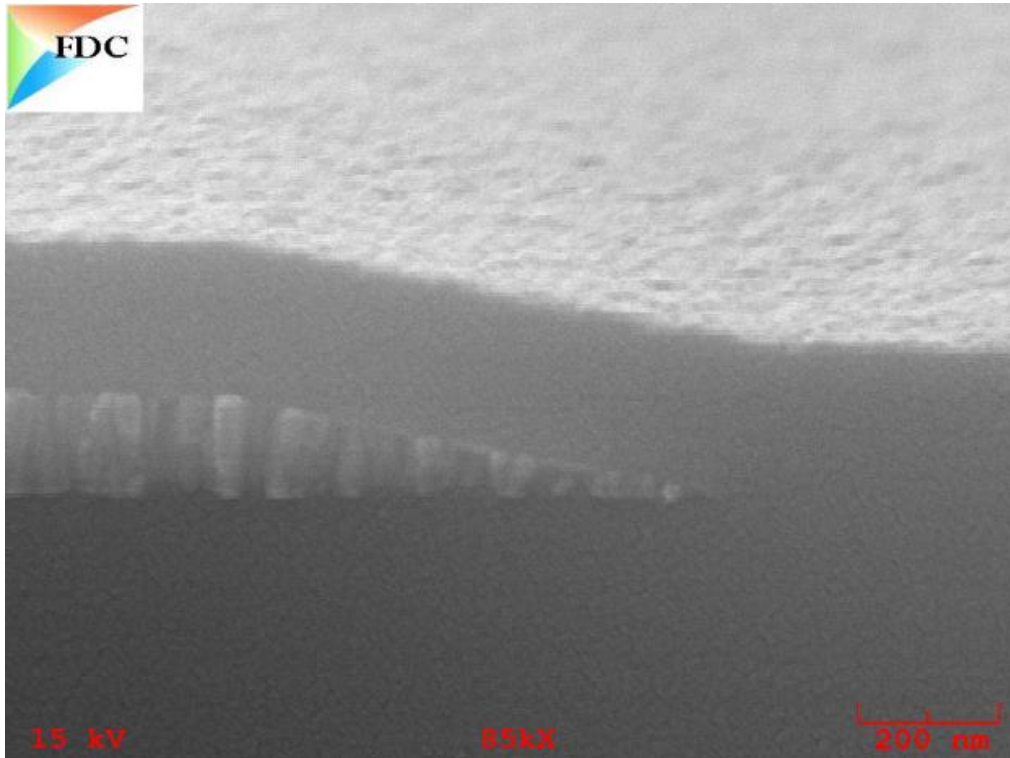


Figure 2.5: FESEM Micrograph Showing Improved Step Coverage with Reduced Sidewall Profile Angle

Gate Dielectric and Passivation Developments

Aluminum oxide was eliminated because the breakdown voltage was less than 20 V for more than half of the capacitors fabricated. This breakdown level is woefully inadequate for TFTs where the gate to source voltage reaches a maximum of 20 V during test. Breakdown tests on capacitor structures featuring 300 nm of silicon nitride indicated that the breakdown voltage is 230 ± 31 V, and a 3-sigma lower limit (137 V) that is significantly larger than the maximum expected operating voltage. Breakdown tests on capacitor structures featuring 100 nm of silicon oxide indicated that the breakdown voltage is 313 ± 32 V, with a 3σ lower limit (217 V) that is significantly larger than the maximum expected operating voltage.

The SiN deposition process was designed for use with a-Si TFTs. With respect to a-Si:H, the known critical materials properties that correlate with film quality and resulting TFT performance include N:Si atomic ratio, hydrogen concentration, and SiH₂/SiH ratio (Saia, Kwanswick and Wei 1991). Film stress is important for process integration issues including film adhesion, whereas index of refraction has been shown to be a good indicator of film quality (Y. Kuo, PECVD Silicon Nitride as a Gate Dielectric for Amorphous Silicon Thin Film Transistor-Process and Device Performance 1995) with indices in the 1.85–1.90 range, exhibiting the best performance and specifically the lowest V_t. Using the available literature as a guide, a baseline 180 °C PECVD process was developed using conditions that produced a nitrogen-rich film (N:Si atomic ratio >1.6) with an average index of refraction of 1.85. The SiH₂/SiH ratio was minimized by employing a low applied power density and high hydrogen dilution factor of more than 50:1 (silane to molecular hydrogen flow rate), which resulted in a slow deposition rate process (~1 nm/s).

Fourier Transform Infrared Spectroscopy (FTIR) demonstrates the presence of a significant amount of hydrogen as indicated by the presence of a peak at 2200 cm⁻¹ in Figure 2.6 (Doughty, et al. 1999). The other peaks correlate to SiN symmetric stretching mode at 500 cm⁻¹ (Tsu, Lucovsky and Mantini 1986) and stretching mode at 845 cm⁻¹, Si–NH–Si bending mode at 1100 cm⁻¹, and NH stretching mode at 3320 cm⁻¹ (Doughty, et al. 1999).

SiN is a more desirable choice as a gate dielectric than SiO₂ because of its higher dielectric constant (7.0) in comparison to SiO₂ (3.9). The dielectric constant and the

dielectric thickness determine the capacitance per unit area as defined by the following equation:

$$C_{\text{gate}} = \epsilon_0 \epsilon / t_{\text{gate}} \quad 2.1$$

where C_{gate} is the gate dielectric capacitance per unit area, ϵ_0 is the permittivity of a vacuum (8.854×10^{-12} F/m), ϵ is the dielectric constant of the gate dielectric, and t_{gate} is the thickness of the gate. A larger C_{gate} is desirable as transistors are dependent on the electric field applied in the active region. In addition, a higher dielectric constant allows for smaller capacitors to be fabricated, which can free up space to improve yield or allow for higher density arrays

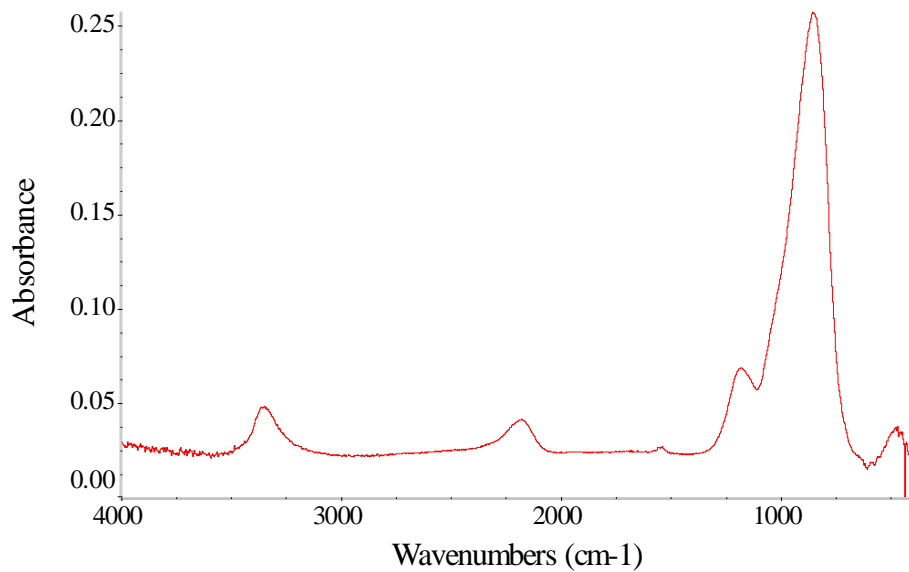


Figure 2.6: FTIR Spectra of Typical SiN Gate Dielectric Layer

However, SiN depositions usually incorporate a significant amount of hydrogen. Hydrogen is a known donor in oxide transistors (Kim, et al. 2007), so minimizing the hydrogen content was believed to be an important factor in the device lifetime. The silicon oxide deposition process therefore avoided the use of hydrogen as a process gas. It was expected that some hydrogen would remain in the film because of the presence of

silane, so an attempt was made to minimize any peaks in the FTIR related to hydrogen. The etch rate of the SiO₂ film was tested in a 1:10 mixture of Buffered Oxide Etch (BOE) and water. The FTIR spectra and BOE etch rate were compared to the spectra and BOE etch rate of thermal oxide films grown by Rogue Valley.

Figure 2.7 shows the absorbance spectra in the 4000–500 cm⁻¹ range for three films deposited at SiH₄ to N₂O flow ratios of 5:2000, 35:2000, and 65:2000. These values constitute two of the axial runs as well as the center point for the central composite design used to screen and optimize the SiO₂ film. A spectra from a 300 nm thick thermal oxide film from Rogue Valley is also included.

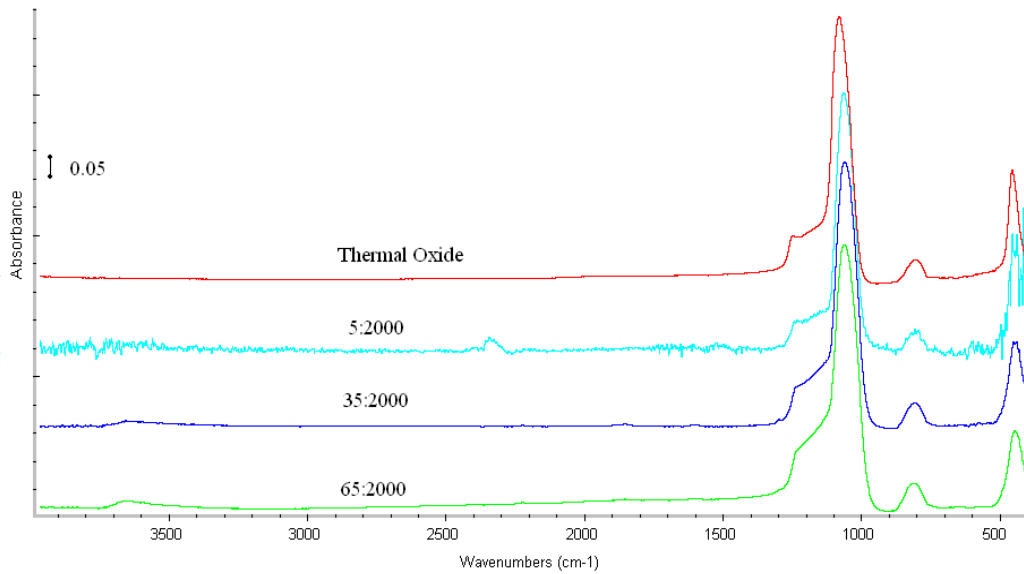


Figure 2.7: Transmission Infrared Spectra for As-Deposited SiO₂ films at Fixed Applied Plasma Power, Total Pressure, and Nitrous Oxide Flow Rates for Three Different SiH₄:N₂O Flow Ratios.

All of the spectra show the expected absorption bands at 450 cm⁻¹, 800 cm⁻¹, and 1040 cm⁻¹. These peaks are attributed to the rocking, bending, and stretching of the Si–O bond (Pai, et al. 1986, Innocenzi and Falcaro 2003). The large peak at 1040 cm⁻¹ has a

shoulder that seems to peak at 1250 cm^{-1} . The ratio of the peak height to the shoulder should give a relative comparison for the density of the film (Bensch 1990). A lower peak height at 1250 cm^{-1} relative to the peak height at 1040 cm^{-1} indicates a more dense film. The film density appears to increase with lower silane flow.

With the exception of the thermal oxide film, all of the spectra show evidence of the presence of hydrogen due to the broad and shallow peak near 3650 cm^{-1} that is typically attributed to silanol (Si–OH) stretching vibrations (Pai, et al. 1986). Eliminating the presence of hydrogen in PECVD grown SiO_2 is usually accomplished with a high temperature anneal post process. The required anneal temperature to effectively eliminate the appearance of silanol in the FTIR spectra can be as low as $350\text{ }^\circ\text{C}$, which is far above the glass transition temperature for most plastics. Since the ultimate goal is process on PEN, which has a glass transition temperature is approximately $240\text{ }^\circ\text{C}$; it was decided to simply minimize the ratio of Si–OH to Si–O.

The process featuring a feed gas flow ratio of 35:2000 (SiH_4 : N_2O) was eventually selected for the baselining experiments because the deposition rates of the lower silane concentration films were below 0.25 \AA/s . The deposition rate for the selected process is 2.8 \AA/s . Breakdown tests on capacitor structures featuring 1000 \AA of silicon oxide indicate that the breakdown voltage is $313\text{ +/- }32\text{ V}$, while the BOE etch rate is $34.3\text{ +/- }0.5\text{ \AA/s}$.

TFTs were grown with the same basic structure but with different gate dielectrics to compare the effect of the gate dielectric composition. Devices with 300 nm of SiN as a gate dielectric were considered shorted between the source and drain as there was limited control of the drain current by the gate voltage. Devices with 200 nm of SiO_2 as a gate

dielectric demonstrated expected transistor behavior with adequate off current as shown in Figure 2.8.

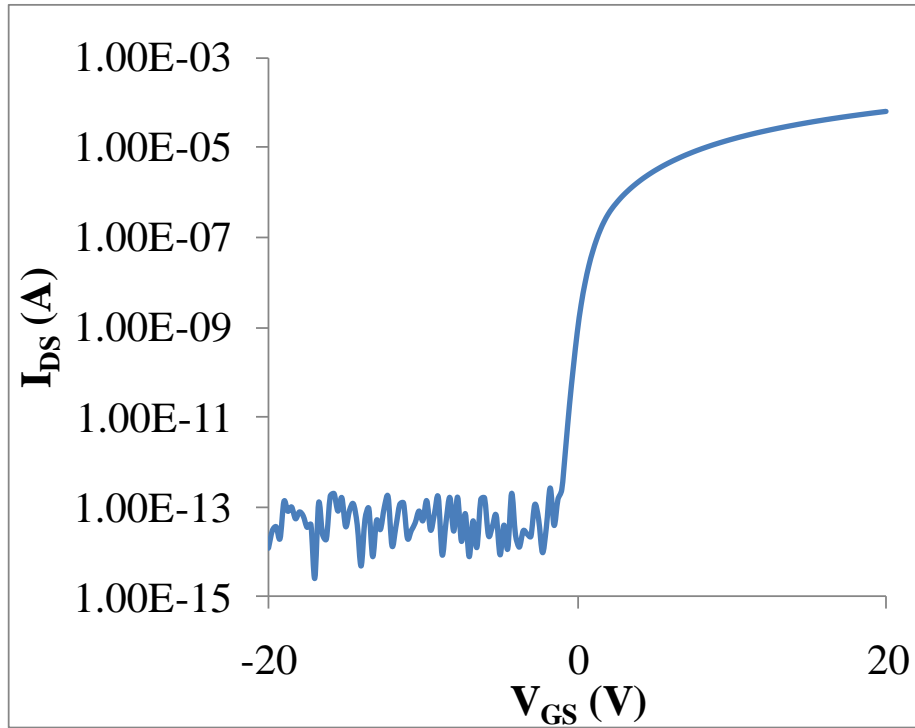


Figure 2.8: I_{DS} - V_{GS} Curve of TFT with 200 nm SiO_2 Gate Dielectric

It was hypothesized that the hydrogen from the SiN migrated into the active layer and reacted with the metal oxide to create oxygen vacancies thus swelling the carrier concentration. In an attempt to prevent the hydrogen from reacting with the metal oxide active layer, another experiment was completed with a two layer gate dielectric consisting of 200 nm of SiN in contact with the gate metal and 50 nm of SiO_2 . The capacitance of the SiN and SiO_2 can be added together and expressed as an effective SiO_2 thickness of 161 nm. Devices fabricated with this two layer stack should demonstrate a higher current than devices with 200 nm of SiO_2 as the gate dielectric.

Devices fabricated with the SiN/ SiO_2 demonstrated a higher drive current (56.2 μA) in devices with a $9 \times 9 \mu\text{m}$ IGZO active area than devices fabricated with a single

layer of SiO₂ (22.1 μA). However, there were still a significant number of failures with high source to drain leakage. Of the 168 devices tested, 125 (74.4%) demonstrated leakage greater than 1 μA. None of the 168 devices with the single layer of SiO₂ demonstrated a leakage higher than 0.4 pA. The results suggest that increasing the thickness of the SiO₂ would help reduce the leakage even further. However, additional increases in the SiO₂ thickness would decrease the capacitance. Since the devices with the single layer of SiO₂ demonstrate consistently low leakage, it was concluded that the single layer of SiO₂ was the most appropriate gate dielectric given the selection.

Active Layer Deposition Developments

The mixed oxide material to be tested was zinc indium oxide (ZIO). The ZIO layer was deposited by reactive DC sputtering using a ceramic target with a composition of 60% zinc oxide and 40% indium oxide to allow for direct comparison to results reported by Itagaki (Itagaki, et al. 2008).

The median performance of the baseline, as well as the median performance after active layer deposition optimization, is summarized in Table 2.1. The saturation mobility of the baseline is much lower than reported by other groups, while the subthreshold slope is much higher (Itagaki, et al. 2008) (H. Hosono, *Ionic Amorphous Oxide Semiconductors: Material Design, Carrier Transport, and Device Application* 2006) (Chiang, et al. 2008).

Screening experiments indicated a strong dependence on the oxygen content in the feed gas. If the oxygen gas flow was shut off, the film sheet resistance dropped to 300 Ω/square on a 50 nm thick film. Devices fabricated at conditions with no oxygen added would fail to turn off. The optimal setpoint was therefore the minimum possible setpoint

of the oxygen mass flow controller. This minimum setpoint resulted in a feed gas mixture that was 2% oxygen.

Table 2.1: TFT Performance Parameter Summary for the ZIO Process (Initial Baseline through Active Layer Deposition Optimization)

Parameter	Initial	Post ZIO
	Baseline	Optimization
Drive Current (μA)	23.8	49.6
Sat. Mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	1.36	2.29
Subthreshold Slope (V/dec)	1.31	0.51
Threshold Voltage (V)	3.3	1.6
Log (S-D Leakage (A))	-12	-13.1
Hysteresis (V)	0.25	0.25

Once the oxygen concentration was set, further optimization of the process pressure and power revealed that the threshold voltage could be reduced with no deleterious effects by increasing the sputter power. The drive performance improvement was statistically significant, but still paled in comparison to results from other groups with similar material sets (Itagaki, et al. 2008, H. Hosono, Ionic Amorphous Oxide Semiconductors: Material Design, Carrier Transport, and Device Application 2006, Chiang, et al. 2008). Details of the actions necessary to improve the device performance are covered in detail in Chapter 3.

Wet ZIO Etch

To provide calibration for the etch rates, blanket-coated ZIO wafers were examined as a function of the etch composition. A standard buffered HF (10 vol-%) etch can fully remove a 50 nm thick ZIO film within 5 s. By switching to a 5 vol-%HCl/45 vol-%HNO₃ mixture in water, the ZIO etch rate is reduced to 6.1 nm/min. The slower etch rate of the HCl/HNO₃ is desirable for process control; the typical duration of an etch process is on the order of 5-10 min. The extremely fast etch rate of the buffered HF makes precise CD control difficult as the total etch time required is only several seconds.

With the relative etch rate understood for the two wet chemistries, lithographic patterning of the ZIO provides a route to understand how the etch chemistry impacts the sidewall morphology of the wet etch. Figure 2.9 illustrates the sidewall profile obtained using the buffered HF etch. This sidewall has a dimpled appearance, which can lead to difficulties in conformal coverage in comparison to a smooth surface. For traditional rigid substrates such as silicon or glass, this morphology generally does not significantly adversely impact yield, but deposition conformality requires higher temperatures that can pose serious problems for flexible plastic substrates. Additionally, the uneven sidewalls could lead to local thickness variations in the subsequent film depositions. The variation would, at a minimum, require additional overetching during subsequent etching steps to prevent shorting. In a worst case scenario, thin films may have difficulty covering the topology to yield voids in the structure that could be detrimental to performance.

To explain the origins of the dimpled morphology, the relative selectivity of the wet etch for zinc oxide and indium oxide can be significantly different, which will leave pockets of one oxide. This selectivity difference creates rougher surfaces at the line edge

than a more non-selective etch would generate. In addition to the rough sidewall, the ZIO is still not fully cleared from the line using the fast HF wet etch. Two potential causes for the particles in the field are again the relative etch selectivity that might not fully clear the area or formation of particles at the sidewall by selective dissolution of one component of the metal oxide. If loose particles are formed, this could significantly impact device yield in a manufacturing environment. The particles can be eliminated by increasing the etch time. However, there is a tradeoff because a patterned film will continue to be etched laterally during this overetch. Despite the significant difference in etch rate between the buffered HF and HCl/HNO₃ solution, a similar sidewall profile is also obtained when using HCl/HNO₃ for the wet etch. Figure 2.9 shows that there are still pieces of the etched film in the field.

In addition to the concerns regarding sidewall uniformity present in the wet etch of ZIO, there are additional potential complications in the selected device architecture (Figure 2.1); due to the overlay, the same mask is used in the etch of both ZIO and the SiO₂ channel passivation layer. In this case, the relative etch rates for the ZIO and SiO₂ are important to controlling the final lithographically defined features. For both wet etch chemistries, the ZIO etches significantly faster than the SiO₂ layer (138 nm/min for HF and <0.2 nm/min for HCl/HNO₃). This difference in etch rate could lead to a substantial undercut of the SiO₂ passivation, which is unfavorable for step coverage of the source/drain metal. Figure 2.10 illustrates a representative cross-section micrograph of the features formed using the buffered HF wet etch when the SiO₂ passivation layer and subsequent deposition/patterning are included to create an operating TFT. The ZIO layer in this case is etched laterally, which creates a 1 μm overhang in the SiO₂ passivation

layer. The HCl/HNO₃ etch also yields a significant overhang that is similar to that obtained from buffered HF.

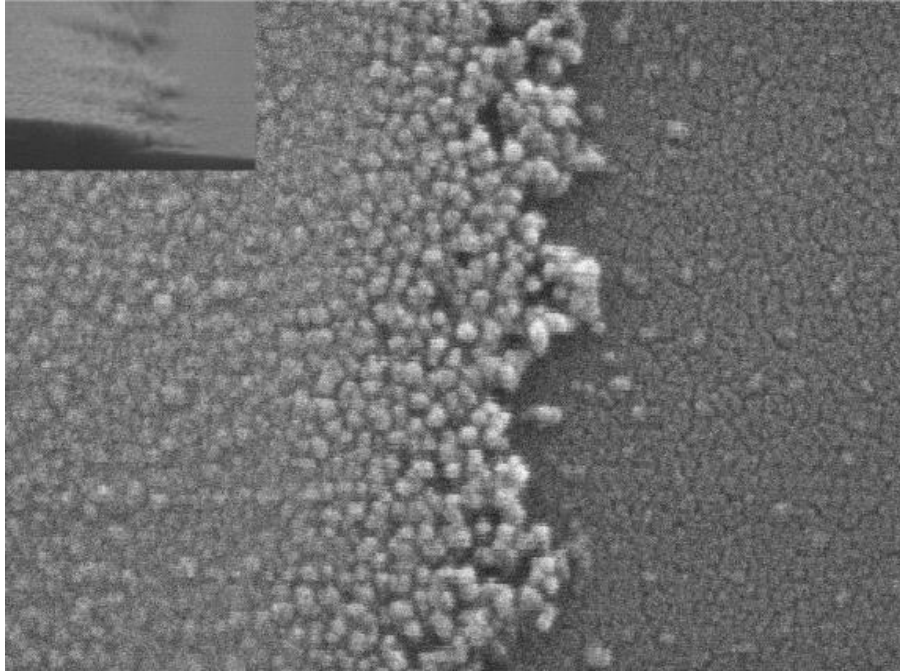


Figure 2.9: Micrographs of Lithographically Patterned Line Edge Using a Buffered HF etch of ZIO. Inset Illustrates a Cross-Section of the Patterned Feature. The Sample Was Gold Flashed Prior to Imaging.

The subsequent deposited layer for mesa sidewall passivation is able to cover the sidewall, but the mesa sidewall passivation appears to be forming a crack. A top down schematic of the device structure is presented in Figure 2.11. The overhang shown in Figure 2.10 is represented by the solid (green online) line surrounding the rectangular ZIO active area. Conductive Mo or Al could be deposited into the area underneath the overhang during the subsequent source/drain metal sputter deposition. Metal deposited under the overhang would be shielded from the directional RIE etch of the source drain etch. Ultimately this mechanism would yield a continuous thread of metal capable of

shorting the source to the drain as illustrated in Figure 2.11, which would degrade device yield.

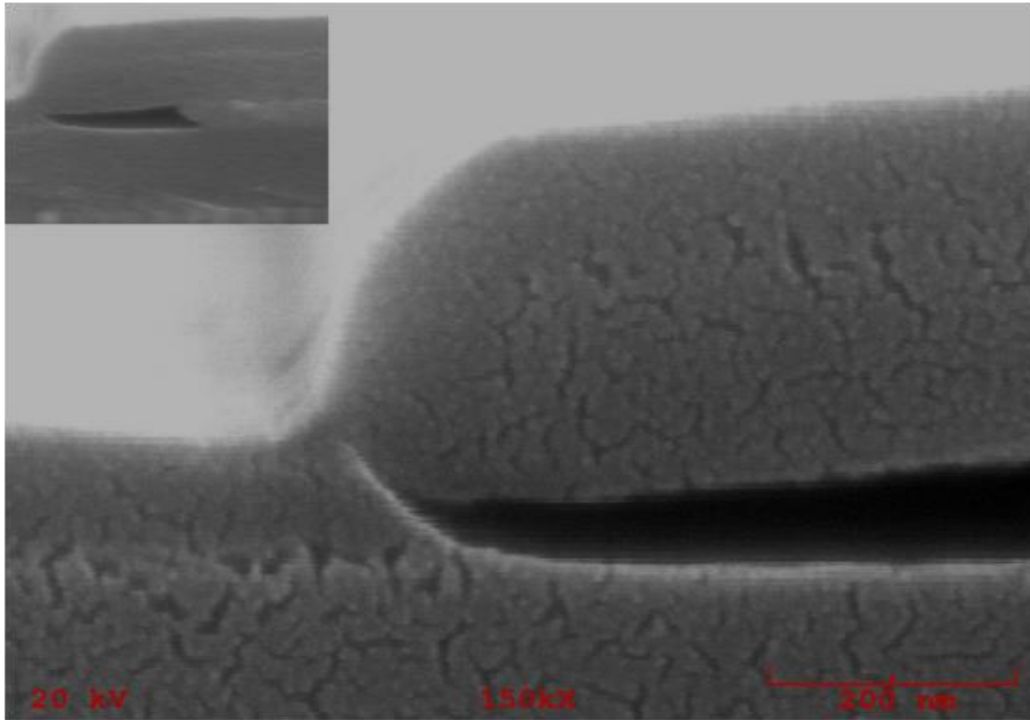


Figure 2.10: Cross Section Micrograph of Wet Etch for ZIO When Passivation Layer and Subsequent Deposition/Patterning are Included. The ZIO is Undercut, but There is Still Adequate Step Coverage for an Operational TFT

To further investigate the impact of the wet etch undercut, the transistor performance for a total of 60 TFTs is tested for each of the two wet etch processes with no statistical difference in performance between buffered HF and HCl/HNO₃ etch. In both cases, the device yield was less than 50% with a significant number of these failed devices exhibiting shorting of the source and drain; this finding is consistent with the proposed shorting from undercutting of the ZIO (Figure 2.10). To further illustrate these issues with these devices, I_{off} is $<1 \mu A$ for only 34 of the 120 devices tested. The results show intrawafer variation; a single wafer typically has some devices with reasonable

transistor characteristics randomly mixed with transistors that exhibit significant shorting between the source and the drain. The mean TFT performance using the wet etch (among the 49 devices that exhibit transistor characteristics) is a V_T of -3.42 ± 1.47 V, μ_{sat} of 6.57 ± 0.73 $\text{cm}^2/\text{V}\cdot\text{s}$, a SS of 2.41 ± 1.01 V/decade, an on current (I_{on}) of 35.3 ± 3.3 $\mu\text{A}/(\text{W}/\text{L})$, and a median I_{off} of 61.2 $\text{nA}/(\text{W}/\text{L})$.

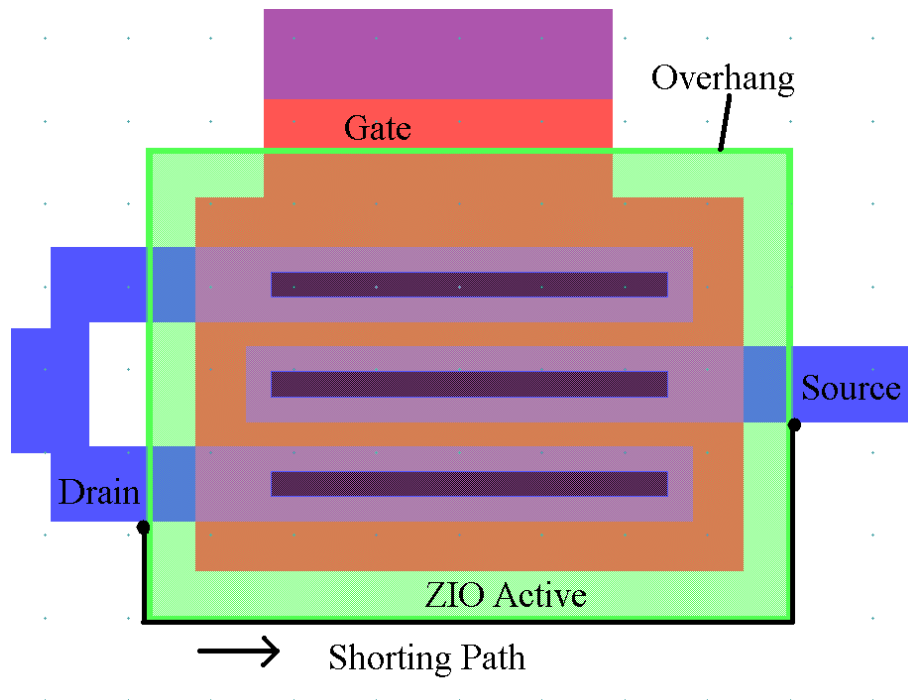


Figure 2.11: Schematic of Potential Short Path that can Develop from the Undercutting Wet Etch Chemistry

Wet ZIO Etch with Etch Stopper Structure

In order to avoid the undercut problem, separate etch of the ZIO layer and the passivation layer could be performed with an additional passivation layer deposited after patterning the source/drain material to cover the exposed portions of the ZIO active layer. This additional passivation layer protects the ZIO from adsorbed oxygen or water from

the environment, which can result in a decrease in TFT performance (S. K. Park, et al. 2009). The architecture of the etch stopper is shown in Figure 2.12.

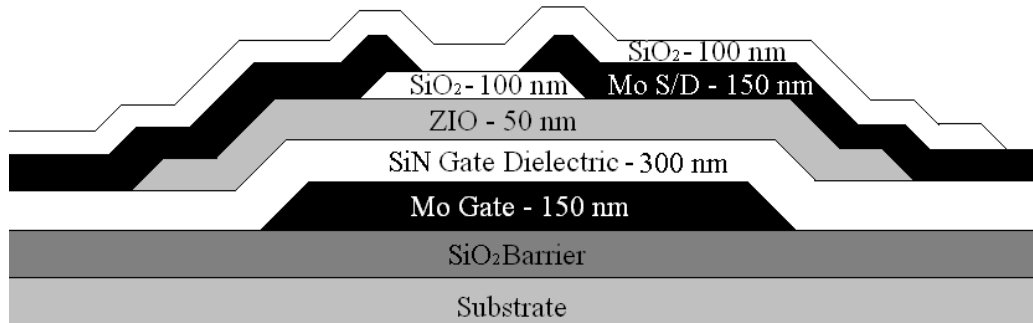


Figure 2.12: Schematic of the Device Architecture Including an Etch Stopper Structure

In this process flow, the gate dielectric, the ZIO active layer and the channel passivation layer or “etch stopper” layer are deposited sequentially as described in the prior section. However, the etch stopper layer is patterned first using the SiO₂ dry etch process. A separate photolithographic mask is subsequently used to pattern the ZIO active layer, which is etched with the buffered HF solution. This patterning scheme eliminates the undercut issue as evidenced by improvement in the device yield to nearly 80%. Additionally, the median I_{off} for the devices is reduced to 0.59 pA/(W/L). However, the drive performance decays with this structure with the median V_T increasing to 3.66 V, the median μ_{sat} decreasing to 1.09 cm²/V-s, while the subthreshold is 2.09 V/decade, and the I_{on} is 3.1 μA/(W/L). The decreased drive performance can be attributed to exposure of the ZIO active layer during the etch stopper etch and the oxygen plasma ash processes. In particular, the oxygen plasma ash can inject oxygen into the ZIO, which fills oxygen vacancies to decrease the carrier concentration.

ZIO Dry Etch

The previous results demonstrate the sensitivity of the ZIO active layer to processing. Therefore, protection of the active layer with adequate passivation prior to further processing is desired, but this approach requires concurrent patterning of the channel passivation and the ZIO active layer. However, this scheme yields unfavorable results when using the standard wet etches.

Greater control over the etch selectivity and sidewall morphology can be achieved using a dry etch. For an etch at 10 mTorr with the RF power set to 1000 W (0.314 W/cm², 414 V DC self-bias) and a gas feed consisting of 10 sccm of O₂, 100 sccm of HCl, and 20 sccm of CH₄, an etch rate of 4.8 ± 0.7 nm/min for the ZIO is achieved with a selectivity to SiO₂ of 1.49, a selectivity to SiN of 1.67, and a selectivity to photoresist of 0.1. The low selectivity to SiO₂ should act to prevent the etch process from undercutting the SiO₂ passivation layer as observed previously for both wet etch chemistries.

Lithographic patterning of the blanket-coated ZIO wafers was performed to understand how the dry etch process impacts the sidewall morphology. Figure 2.13 illustrates a top view of the sidewall. The sidewall edge is more uniform than for the wet etch process shown in Figure 2.9. The total thickness of the active layer is approximately 50 nm, but the length of the sidewall is approximately 150 nm indicative of a sidewall slope of $\sim 20^\circ$. Moreover, the sidewall is smoother than the choppy sidewall obtained from the wet etch (Figure 2.9); this morphology should enable improved step coverage of subsequent depositions. Additionally, no residual material can be observed in the field (right side of Figure 2.13), which indicates a complete etch of the ZIO.

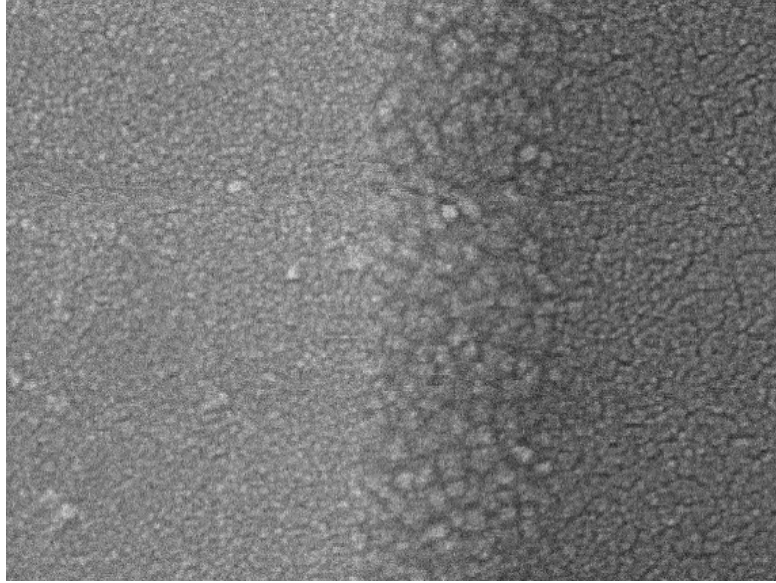


Figure 2.13: Micrograph of the Dry Etched ZIO Sidewall. The Sample was Gold Flashed Prior to Viewing in the FESEM.

To further evaluate the dry etch process, devices are fabricated using the structure presented in Figure 2.1. Figure 2.14 illustrates a typical etch profile of device using the ZIO dry etch and the step coverage of the subsequent depositions. The sidewall angle is approximately 24° from the horizontal and can easily be covered by the subsequent line of sight thin film depositions. There is no indication of a step coverage issue that was present with the wet etch.

As the structure appears to be improved relative to the wet etch, the TFT device performance was also investigated to confirm the improvement. Devices fabricated with the dry etch process exhibit a median source to drain leakage of 0.56 pA ($52 \text{ fA}/(\text{W}/\text{L})$), which is approximately 3 orders of magnitude lower than the original wet etch. Of the 80 devices tested, I_{off} is not larger than 4.2 pA ($0.4 \text{ pA}/(\text{W}/\text{L})$) for any single device.

Moreover, the drive performance is comparable to the wet etch structure as I_{on} was $8.2 \pm 2.0 \text{ }\mu\text{A}/(\text{W}/\text{L})$, the mean μ_{sat} was $6.42 \pm 1.12 \text{ cm}^2/\text{V}\cdot\text{s}$, the V_{T} was $4.85 \pm 0.65 \text{ V}$, and the

SS was 1.04 ± 0.08 V/dec. Table 2.2 summarizes the differences in performance obtained from the wet and dry etch when using the inverted staggered device structure.

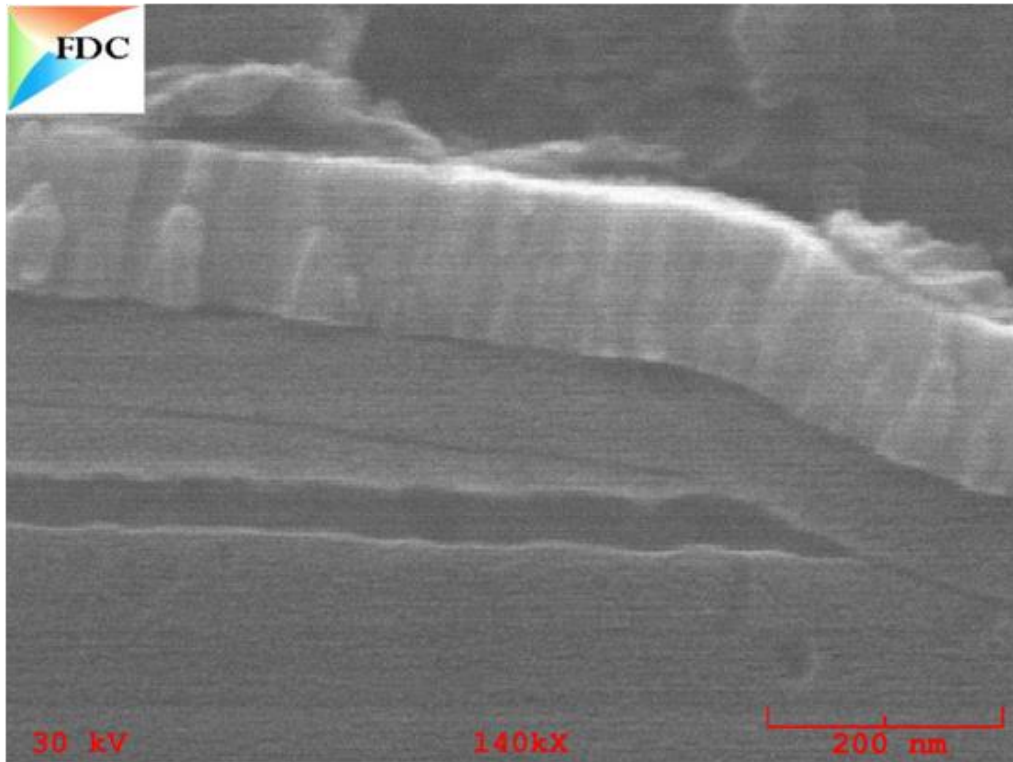


Figure 2.14: Typical ZIO Dry Etch Profile with Subsequent Layer Deposition.

Table 2.2: Comparison of Wet and Dry Etch TFT Mean Parametric Performance with the Inverted Staggered Structure

	Wet (HF and HCl/HNO ₃)	Dry
V _T (V)	-3.42 (1.47)	4.85 (0.65)
μ _{sat} (cm ² /V-s)	6.57 (0.73)	6.42 (1.12)
SS (V/decade)	2.41 (1.01)	1.04 (0.08)
I _{on} (μA/(W/L))	35.3 (3.2)	8.2 (2.0)
Median I _{off} (pA/(W/L))	61.2	0.052

The results indicate a significant decrease in the I_{off} and SS with limited degradation in the drive performance when using a dry etch. The significant improvement in the yield is predominately attributed to the improved sidewall profile of the dry etch, which prevents high I_{off} (shorting). However, the dry etch process increases the V_T , which could however be corrected by tuning of the active layer deposition processes. Nonetheless, a positive V_T is typically more desirable than a negative V_T as the device needs to be “off” when the voltage is zero.

A dry etch of ZIO leads to better performance than a wet etch due to improvements in etch selectivity and full passivation of the active layer during processing. The wet etch processes exhibits a large selectivity to ZIO over SiO_2 and SiN dielectric layers. To overcome this selectivity issue, separate patterning of the passivation and the active layer can be utilized in an etch stopper type device layout, but then the ZIO is exposed to other processes without passivation. A dry etch minimizes the etch selectivity between ZIO and the dielectric and provides improved sidewall profile control and accordingly step coverage of the subsequent depositions. The SS and V_T are higher than desirable for the dry etch, but the etch is consistently reproducible with high device yield. The yield improved from 28% to 100% by using the dry etch in place of the wet etch. Future work will focus on improving the V_T and SS by optimizing the gate dielectric and active layer deposition processes. The dry etch provides a route to a consistent etch process for the active layer and enables future process optimization for ZIO-based devices.

Source/Drain Metallurgy Developments

The $96 \times 9 \mu\text{m}$ TFTs were characterized and analyzed for this experiment. The control cell featured 150 nm of molybdenum as the source/drain metal. The cell featuring the ITO source/drain metal demonstrated the statistically lowest mobility ($7.82 \text{ cm}^2/\text{V}\cdot\text{s}$) and lowest drive current ($405 \mu\text{A}$). The decreased drive current is attributed to the line resistance of the ITO. The sheet resistance of ITO at 50 nm thick is $80 \Omega/\square$ and there are roughly 40 squares between the TFT and the prober pads resulting in a significant voltage drop. Therefore, the actual applied drain voltage was likely much lower than the output drain voltage.

The cell featuring tantalum was not expected to perform well because tantalum forms an insulating oxide much like aluminum. However, the mean drive current ($417 \mu\text{A}$) and saturation mobility ($10.3 \text{ cm}^2/\text{V}\cdot\text{s}$) were comparable, but statistically poorer than the control cell ($546 \mu\text{A}$ and $12.6 \text{ cm}^2/\text{V}\cdot\text{s}$). The median saturation mobility was much closer to the control cell ($12.4 \text{ cm}^2/\text{V}\cdot\text{s}$ versus $12.5 \text{ cm}^2/\text{V}\cdot\text{s}$ for the control cell) indicating that there may have been a few devices skewing the mean performance.

Approximately 12 out of the 60 devices tested from the Ta/Al cell feature a drive current that is less than $10 \mu\text{A}$. These poor performing devices typically demonstrate a non-zero intercept in the output characteristics as shown in Figure 2.15 which is an indication of current crowding and the presence of a significant barrier between the source and drain. The barrier is likely tantalum oxide, which is a dielectric.

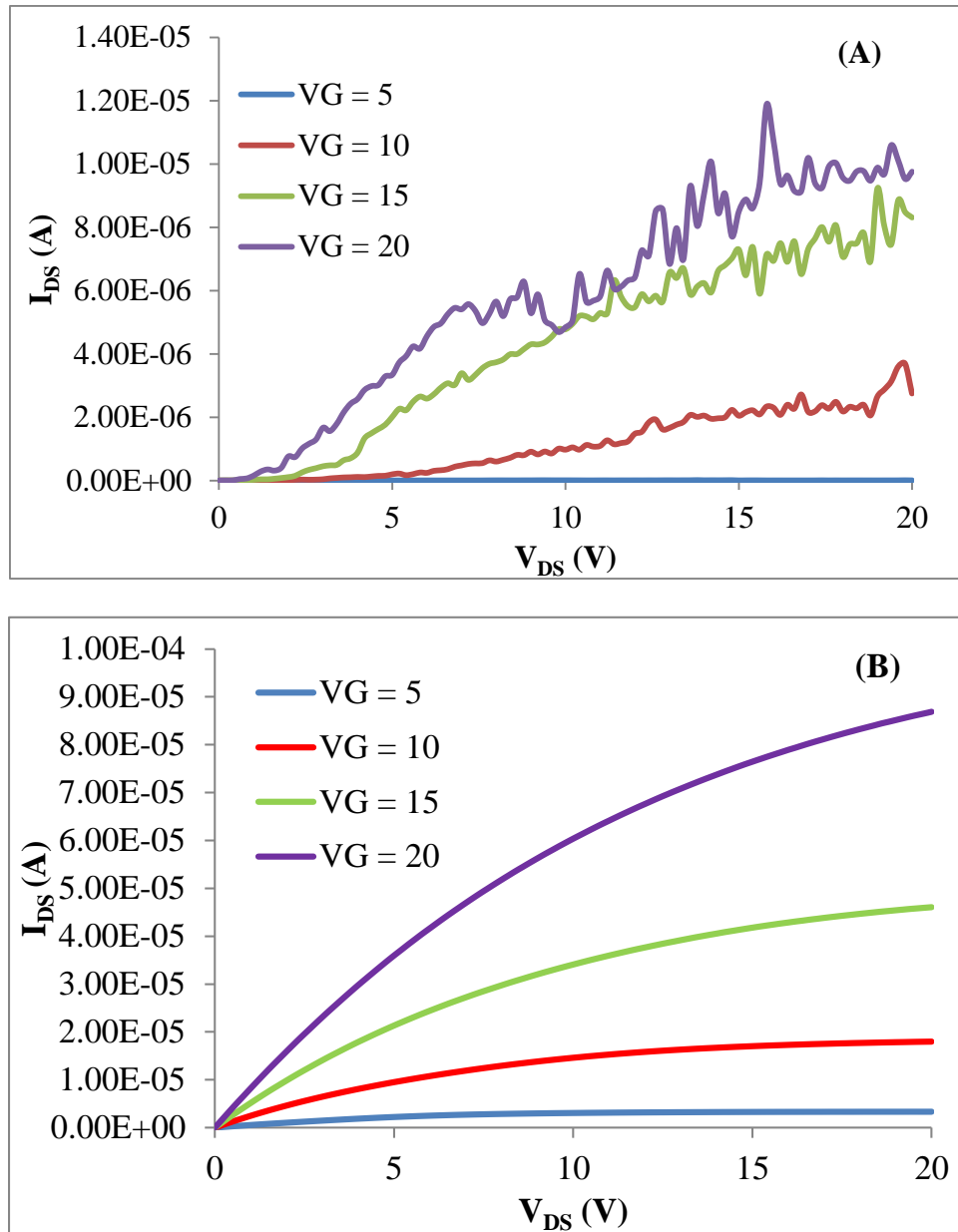


Figure 2.15: (A) Output Characteristics of a Device with Ta/Al Source/Drain Metal Demonstrating Current Crowding at Low V_{DS} and (B) Output Characteristics of a Device with Mo/Al Source/Drain Metal Demonstrating Normal Behavior.

The cell featuring the Al/Mo bilayer demonstrated statistically improved drive current ($598 \mu\text{A}$) and saturation mobility ($14.3 \text{ cm}^2/\text{V}\cdot\text{s}$) over the control cell. In addition, the median source to drain leakage was two orders of magnitude (1.6 fA versus 269 fA)

for the control cell) lower. The reduction in leakage is attributed to the oxidation of the aluminum source/drain layer. The source/drain layer in this experiment is exposed to the atmosphere because processing was stopped immediately after source/drain etching. The control cell features molybdenum, which forms a weakly conducting oxide. The test setup is outside of the cleanroom so contamination may have been attracted to the exposed conductive molybdenum oxide during test operations. The Al/Mo bilayer devices may have been protected by the formation of an insulating native oxide on the aluminum. The results indicate that the Al/Mo bilayer is adequate for the source/drain material.

Interlayer Dielectric (ILD) Developments

Initially, 500 nm SiN was used as the ILD layer. However, the PECVD grown SiN is conformal and does not planarize topology. In addition, electrophoretic displays fabricated with 500 nm of SiN demonstrated evidence of cross talk (Figure 2.16a).

Thicker depositions of SiN were not considered reliable because of the stress of the film. In addition, the SiN does not address the need for planarity as OLED displays fabricated on topology demonstrate luminance variations (Figure 2.16b)

The poor visual appearance of displays fabricated with SiN ILD resulted in a search for a new material to serve as the ILD. Spin on glass (SOG) materials are attractive alternatives because of their low dielectric constant (3.0) and planarizing ability (Doux, et al. 2006). Most SOG's are applied in liquid form and are cured by applying thermal energy. In most cases, the temperature of the cure is in excess of 400 °C, which far exceeds the melting temperature of most polymer substrates. However, a spin on glass material from Honeywell (trade name PTS-R) was found to have a cure temperature of

200 °C at a thickness of 2 μm. The material was ordered and incorporated into the TFT process flow. The low dielectric constant of the PTS-R significantly reduced the crosstalk in electrophoretic displays (Figure 2.16c) and its ability to planarize improved intrapixel luminance uniformity (Figure 2.16d).

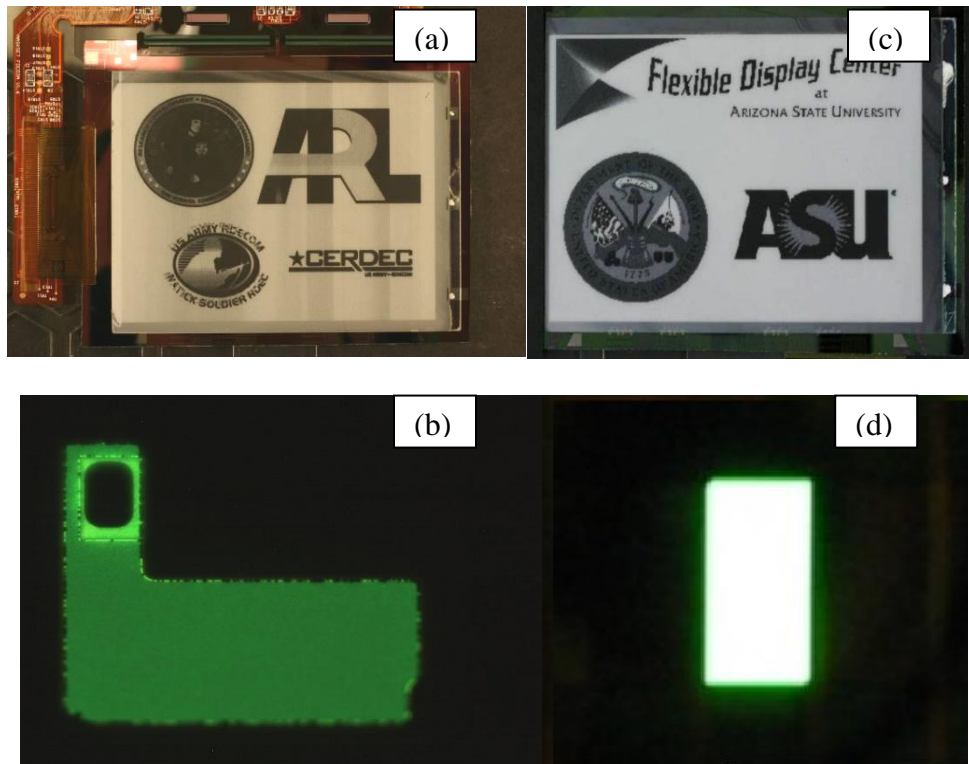


Figure 2.16: Electrophoretic Display with SiN Non Planarizing ILD (a) and with PTS-R (b) and OLED Pixel Fabricated with SiN ILD (c) and with PTS-R (d)

The ILD was etched in a Tegal 901 reactive ion etcher (RIE) with the process pressure set to 400 mTorr, the power set to 200 W, the SF₆ flow set to 10 sccm and the O₂ flow set to 20 sccm. The O₂/SF₆ ratio is a main factor in determining the etch rate of the PTS-R and the photoresist. The flow ratio was adjusted to achieve a 1:1 selectivity between the PTS-R and the photoresist yielding a sidewall slope of approximately 35° from the horizontal. The shallow slope allows for adequate step coverage of the relatively

thin anode layers (Figure 2.17). The resist was stripped by oxygen plasma etching in the Tegal 901 at a substrate temperature of 45 °C or by wet stripping in a bath of Baker's PRS 3000 solvent strip at 60 °C, followed by an intermediate rinse in room temperature 100% isopropanol, QDR, and SRD. The performance of the respective processes is considered statistically equivalent. The low temperature Tegal 901 was chosen over the more conventional Gasonics L3510 microwave downstream asher and Tegal 965 barrel asher due to issues with cracking in the PTS-R under the higher temperature conditions of the Tegal 965 and Gasonics L3510. It was determined that the substrate temperature had to remain below 120 °C to prevent the PTS-R from cracking.

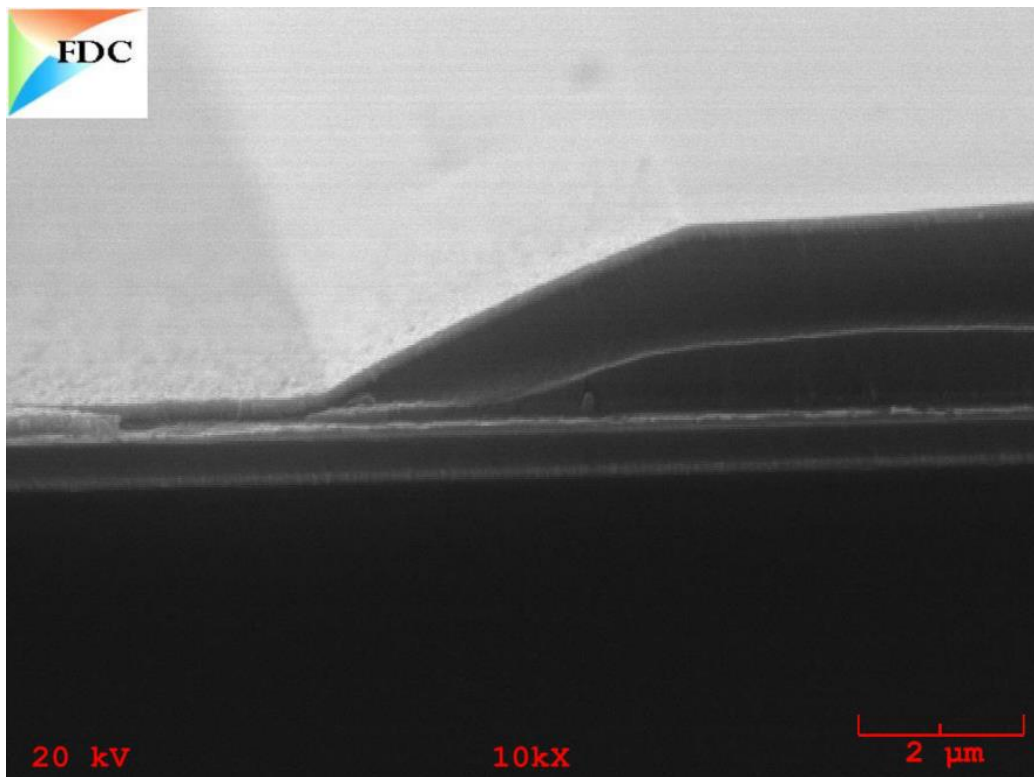


Figure 2.17: SEM Micrograph Demonstrating Sloped ILD etch

It is difficult to verify the via integrity through inspections in the FESEM. Therefore, an electrical test was developed for testing individual pixels in completed

backplanes. The test relies on the continuity of the anode materials from the probe contact to the contact with the source of the pixel TFT. A schematic of the test setup for an OLED array is shown in Figure 2.18.

A grounded probe needle contacts every pixel at the source of the drive TFT while power is applied to the VDD, gate (G), and source (S) terminals. A “low” current value indicates that there is either an issue with one of the TFTs or a discontinuity in the via. A QVGA array has 76800 pixels, so a lot of data can be collected quickly and a visual map of the array can be generated. In these visual maps, a white pixel indicates a short in a severe case or a “hot” pixel (high current) in a less-severe case, and a black pixel represents an open circuit in a severe case or a “cold” pixel in a less-severe case. A high-yield high quality array would show a map of a nearly even “deep blue sea.” A typical, high-yield array map is shown in Figure 2.19.

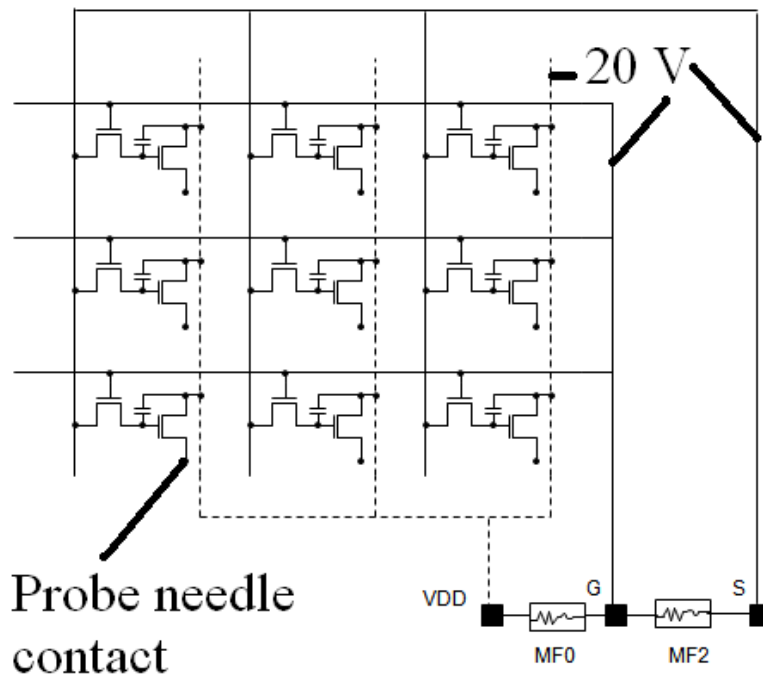


Figure 2.18: Array Test Circuit

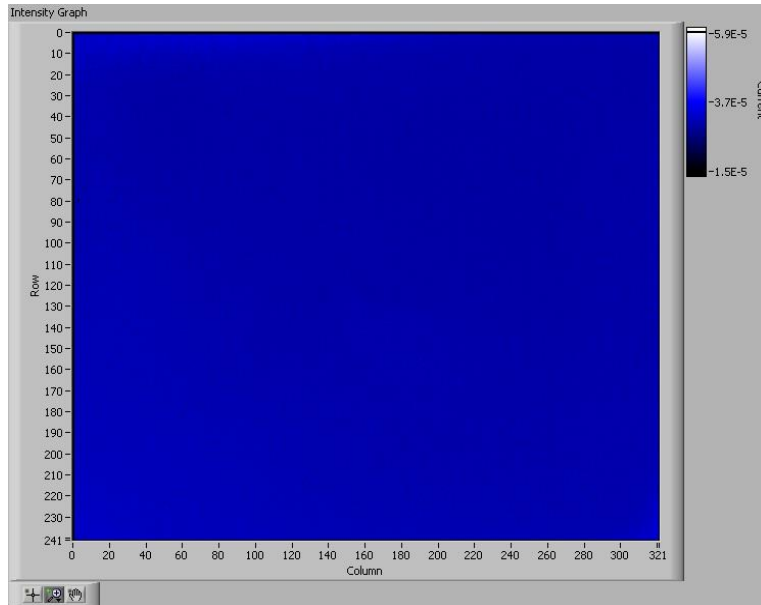


Figure 2.19: Array Current Map Demonstrating Good Yield

Poor yield was initially observed when SiN was used as the ILD wetting and capping layer. Occasionally, arrays would demonstrate large “dark” spots in the array map that were indicative of either an issue with the TFT or a discontinuity in the via. An example of a defective array map with “dark” spots is shown in Figure 2.20.

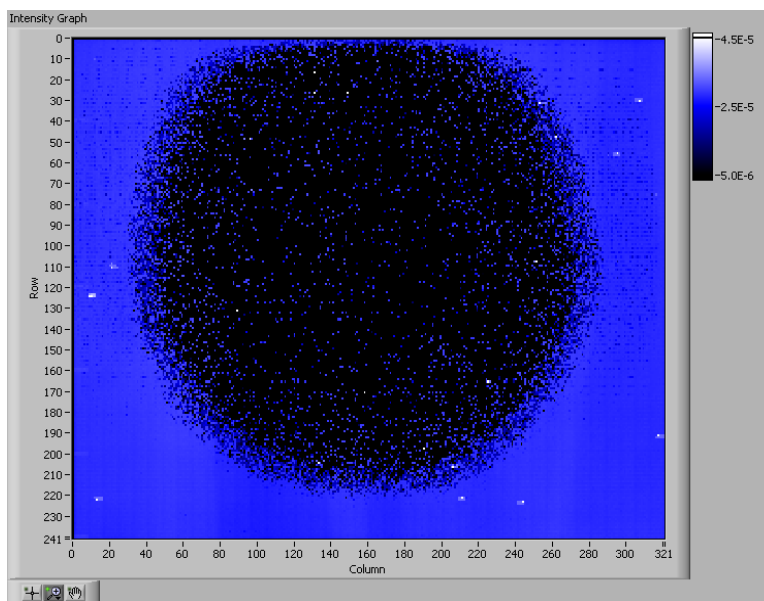


Figure 2.20: Array Map Demonstrating Poor Yield

A FESEM analysis of the defective area indicated poor step coverage by the subsequent metal deposition due to a reentrant profile of the SiN wetting and capping layers. The SiN was etching laterally faster than the photoresist or the PTS-R yielding an undercut profile at the top and bottom of the via. An example demonstrating an undercut with poor step coverage is shown in Figure 2.21.

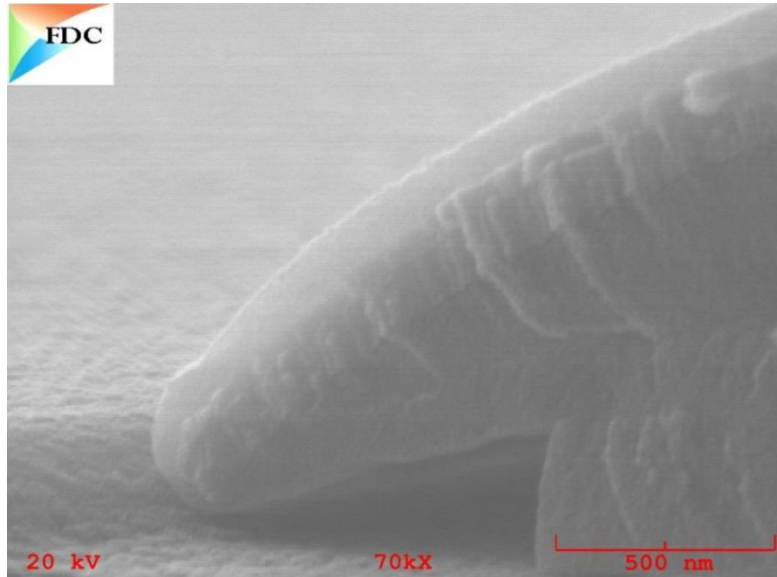


Figure 2.21: Undercutting of the SiN Wetting Layer and Demonstration of Step Coverage Issues for Subsequent Depositions.

The issue was resolved by switching to SiO₂, which etches at approximately one-half the etch rate of the PTS-R and the photoresist. The lateral etch rate of the SiO₂ is low enough that a reasonable etch profile is obtained.

Stress Testing Results

The threshold voltage shift at various DC bias conditions was compared with amorphous silicon. As seen in Figure 2.22, the change in threshold voltage is comparable to amorphous silicon for the negative DC bias stress conditions, with the threshold voltage changing by as much as -2.2 V. However, for positive DC bias stress, the

threshold voltage shifts between 0.2 – 1.3 V after 10 000 s of stress, which is significantly less than the shift observed in amorphous silicon TFTs. The standard deviation for the voltage shift at 10 000 s is typically between 0.3-1.0 V depending on the bias condition.

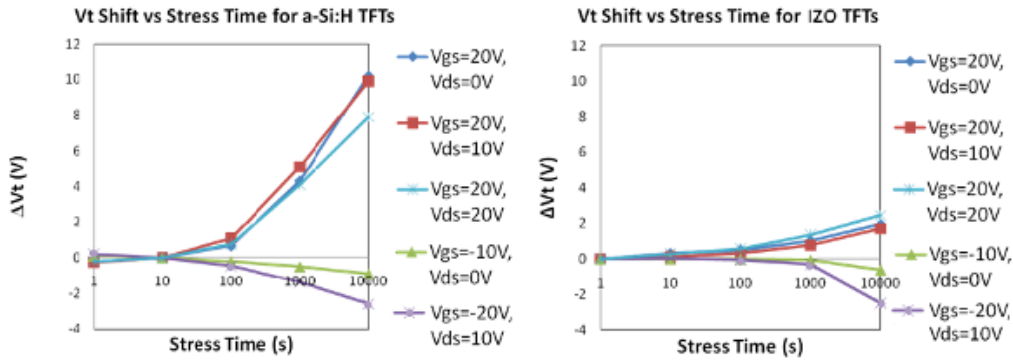


Figure 2.22: Comparison of Threshold Voltage Degradation of a-Si:H and ZIO TFTs

The improved DC stress stability of ZIO in comparison to amorphous silicon is readily observable when examining the change in the output current of the drive transistor (T2) of the OLED pixel circuit as shown in Figure 2.23. As the current degrades, the luminance of the OLED will also degrade. One can see that the a-Si pixel current drops approximately 2.5 μA (37%) after two hours of operation, while the drop in the ZIO pixel current is only 0.3 μA (3%).

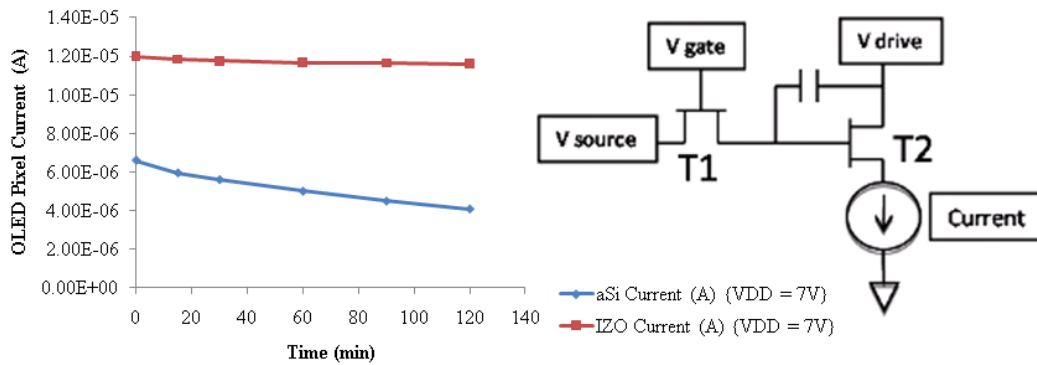


Figure 2.23: Test Setup and Results of Constant Voltage Test

OLED Display Build

The OLED device structure has a median efficiency of 5.8 cd/A, and was developed by Xiaohui Yang at the FEDC. The details of the OLED process are discussed elsewhere (Yang, et al. 2008). A fully built QVGA white OLED display is shown in Figure 2.24.

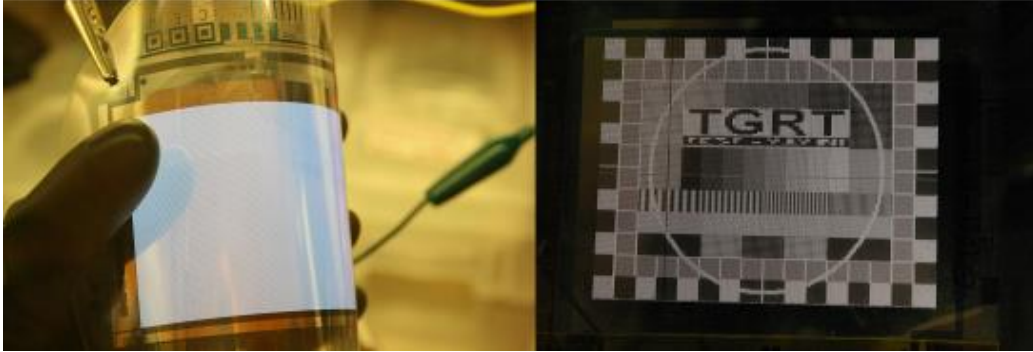


Figure 2.24: FEDC's Completed White Active Matrix OLED Display with ZIO TFTs

The display resolution is a QVGA, which contains 320 columns of pixels and 240 rows of pixels, and is nominally 4.1" along its diagonal with an aperture ratio of 34.4%, and a pixel density of 98.7 ppi. Each individual pixel consumes an area that is $67600 \mu\text{m}^2$, and contains two transistors and one capacitor. The select transistor dimensions are $75 \mu\text{m}$ by $11 \mu\text{m}$, while the drive transistors dimensions are $240 \mu\text{m}$ by $11 \mu\text{m}$. The capacitor has a capacitance of 1.12 pF.

The maximum luminance is 600 cd/m^2 .

Conclusions

We have embarked on a critical path in flexible zinc indium oxide active-matrix backplane technology development that includes the following foundational elements described in this chapter:

- Baseline low-temperature ZIO process development and improvement on a 6-inch pilot line to produce quality transistor arrays with reasonable yields
- Optimization and statistically-based improvement of ZIO drive performance
- Threshold voltage stability improvements over amorphous silicon
- Transition to processing on flexible plastic with current bond-debond process tools and materials
- Successful fabrication of white OLED displays with ZIO backplane technology

CHAPTER 3 NEW ACTIVE LAYER DEPOSITION PROCESS BASED UPON DUAL-LAYER CONCEPT

Introduction

Critical thin film transistor (TFT) properties in pixel circuit design include the threshold voltage and its shift due to voltage stress. The shift in threshold voltage will eventually result in incomplete turn-off or incomplete turn-on of the affected pixels depending on the direction of the shift. Stabilization of the threshold voltage for mixed metal oxide semiconductors can be achieved through one or more high temperature (>300 °C) post processing steps (Chiang, et al. 2005). Unfortunately, these high temperature steps are incompatible with processing on flexible plastic substrates, such as polyethylene naphthalate (PEN). There is a substantial development effort in the display community to shift from glass to flexible plastic substrates that would provide a more rugged, thinner, and lightweight display backplane. PEN is compatible with much of the same cleaning chemistries as glass (Wong and Salleo 2009). Moreover, PEN is an insulator like glass and thus avoids parasitic coupling capacitance that can affect devices fabricated on metal foils that could withstand the higher temperature post-processing. The colorless and highly transparent PEN material could provide an ideal substrate for low power, bottom emission, organic light emitting diode (OLED) displays.

The initial deposition conditions, specifically the composition of the feed gas during the reactive sputtering of the mixed metal oxide semiconductor, have a significant effect on the transistor performance of the finished TFTs. Typically, argon and oxygen are introduced to the chamber during the semiconductor deposition and the flow rates are held constant during the deposition process. Decreasing the concentration of oxygen in

the feed gas increases the saturation mobility and decreases the threshold voltage of the finished TFT (Chiang, et al. 2008). Oxygen concentration in the feed gas reported in literature ranges from 2% (Sato, et al. 2009) to 10% (Chiang, et al. 2008) with the saturation mobility increasing with decreasing oxygen concentration. Films that are deposited without oxygen in the feed gas during the deposition process are too conductive for TFTs (Chiang, et al. 2008).

Achieving repeatable and reliable constant oxygen feed gas concentration between 0% and 2% poses a difficult process control problem. For a typical commercial standard sputter deposition system, pumping conductance is such that a flow rate of less than 1 sccm of oxygen is required to achieve the concentration and chamber deposition pressure. In situations where it is not practical to use such a small oxygen flow rate, an intriguing option is to perform a staged deposition process where the oxygen concentration starts at 0% and is changed to 2% during the deposition, thereby creating a dual layer semiconductor.

In this chapter, the influences of composition and thickness of dual layer transparent oxide semiconductors on the performance of TFTs are systematically examined. The use of a dual layer architecture allows the independent control of mobility and threshold voltage through compositional variations in the dual active layer. With proper tuning of the active layer compositions, the required device properties can be achieved without the use of a high temperature anneal, which is critical for the use of mixed metal oxides for flexible electronics and display applications.

TFT Fabrication

To deposit the metal oxide layer, two different targets were utilized: 60% zinc oxide and 40% indium oxide (ZIO) by mass and 33.3% indium oxide, 33.3% gallium oxide, and 33.3% zinc oxide (IGZO) by mass. So that we could directly compare our dual layer devices with previously-reported single layer devices, these sputter target compositions match the target compositions used by Itagaki (Itagaki, et al. 2008) for ZIO and Lim (Lim, et al. 2008) and Kwon (J. Y. Kwon, et al. 2009) among others for IGZO.

The TFTs were fabricated with a bottom gate, inverted, staggered design. The transistors function as n-type devices in enhancement mode. The backplane TFT structure was similar to that previously described by Kaftanoglu et al. (Kaftanoglu, et al. 2011), except here the two active layers were IGZO/ZIO. This device architecture is illustrated in Figure 3.1.

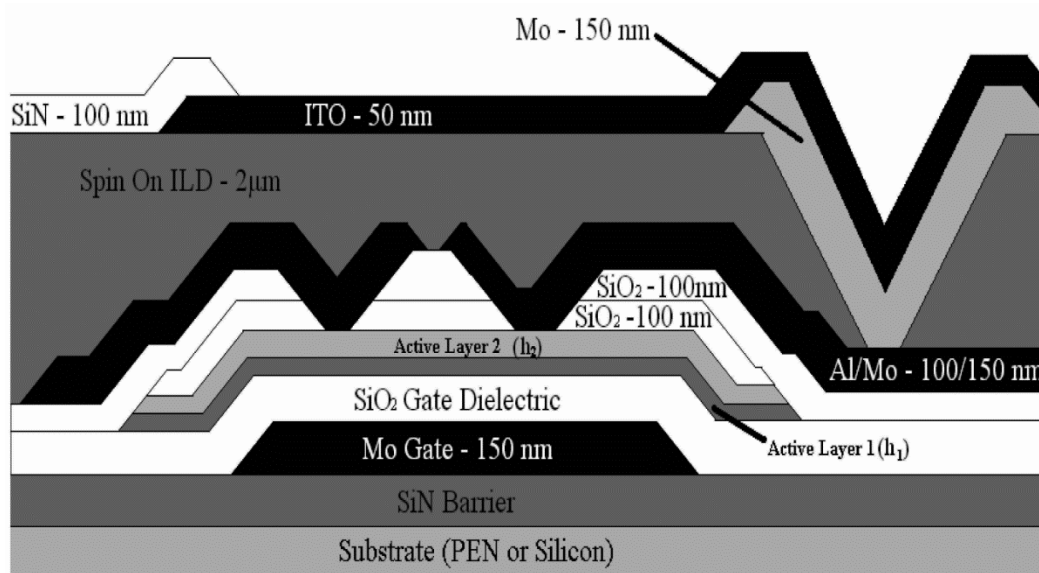


Figure 3.1: Schematic of the Backplane Pixel Structure

The PEN substrate (125 μm thick) was obtained from DuPont Teijin Films (trade name Teonex Q65A) and was temporarily bonded to an alumina carrier (150 mm

diameter, CoorsTek) for processing as described previously (Haq, et al. 2010). To rule out any potential substrate effects, TFTs were also fabricated on silicon substrates (150 mm) under identical process conditions and protocols as those used for PEN substrates; there were no statistical differences in the device performance between those fabricated on silicon or PEN. Devices were fabricated using the process steps described as follows. The substrates were cleaned in a PCT megasonic tank with a mixture of Alconox Detergent 8 (5% by volume) and deionized water. A silicon nitride substrate barrier film was deposited by PECVD (AMAT P5000) followed by deposition of the molybdenum gate metal by DC sputtering (MRC 603). The gate dielectric (SiO_2 , 20 nm thick) and passivation layers were all deposited by PECVD (AKT 1600 deposition system) at a process temperature of 180 °C. The dual active layer was deposited using DC reactive sputtering (MRC 603 sputtering system) operating at 300 W at a pressure of 16 mTorr and a nominal substrate temperature of 40 °C. Active Layer 1, with thickness h_1 , was the layer in contact with the gate dielectric and Active Layer 2, with thickness h_2 , was the layer in contact with the source and drain. The cumulative thickness of active layers ($h_1 + h_2$) was maintained at 50 nm. The deposition of both active layers was always completed in situ without breaking vacuum to prevent atmospheric oxygen from altering the composition of the active layers in the interfacial region. A mixture of argon and oxygen (varied from 0 to 10% oxygen) was used as the deposition feed gas. The molybdenum/aluminum source and drain were deposited by DC sputtering (MRC 603). The thick spin-on interlayer dielectric from Honeywell (trade name PTS-R) that encapsulates the TFT was cured at 200 °C for 1 h in a N_2 environment; this is the maximum temperature for the entire process. The pixel anode consisted of sputter

deposited (KDF 744) molybdenum and indium tin oxide (10% tin oxide by weight) layers. Each pixel was passivated by silicon nitride. Etching of the individual layers was completed using an AMAT 8330 dry etcher for the metal and active layer etching and a Tegal 901 parallel plate reactive ion etcher for all dielectric etching. AZ Materials 5214 photoresist was patterned using a Canon MPA-605 aligner for each photolithography step. The photoresist was stripped in a Gasonics L3510 downstream microwave plasma asher. All TFTs were fabricated with $W/L = 10.5$ and $L = 9 \mu\text{m}$.

For comparison purposes, single layer IGZO and ZIO TFTs were first separately fabricated to establish the baseline electrical characteristics of each film as well as the dependence of the electrical performance on the active layer deposition process conditions. Dual active layers were then deposited with the same target material (either the IGZO or ZIO target) with process conditions altered after the completion of the first layer to generate a more resistive second layer (Active Layer 2) to prevent source to drain shorting. The thicknesses of the individual layers were varied, but the cumulative thickness was maintained at 50 nm. Dual active layers were also deposited with varying layer composition through sequential deposition using one sputter target and then the other. This experimental design enabled systematic investigation of the role of the dual active layer on the performance of metal oxide-based TFTs.

Test Setup

The TFT electrical performance was quantified using a probe station with a Keithley 4200 Semiconductor Characterization System (SCS). Transistor performance was measured for 10 individual test transistors distributed across the wafer. For each deposition condition, 12 wafers were processed and examined for a total of 120 devices

tested per processing condition; this testing scheme provided a route to quantify intrawafer and wafer-to-wafer variations in device performance. For each TFT, the saturation mobility and the threshold voltage were extracted from the drain current (I_D) as a function of the gate voltage (V_G) transfer characteristics of the test transistors. This parameter extraction assumed that the device was in saturation and that the saturation drain current can be expressed as

$$I_{D_{\text{sat}}} = \mu_{\text{sat}} C_{\text{ox}} (W/(2L)) (V_G - V_T)^2 \quad \text{when } V_G > V_T \quad (3.1)$$

where μ_{sat} is the saturation mobility; C_{ox} is the gate dielectric capacitance; (W/L) is the aspect ratio of the device; and V_T is the threshold voltage. Both the threshold voltage and saturation mobility were extracted graphically from the $\sqrt{I_D}$ versus V_G curve using the intercept and maximum slope, respectively. The performance of these parameters was also monitored with respect to electrical stress, where devices were stressed at either $V_G = +20$ V or $V_G = -20$ V with the drain voltage set to 0 V. The shift in the threshold voltage was determined after stressing for 10 min.

Single Active Layer Device Results

To provide a baseline comparison for the dual layer devices, electrical properties of analogous single component active layer devices are examined first. Figure 3.2 illustrates a representative transfer curve for a single layer transparent oxide-based transistor. Typically, both the saturation mobility and threshold voltage can readily be extracted from the transfer curve by a linear fit of the square root of the drain current as a function of the gate voltage. However in this case, there is non-ideal behavior in V_{GS} near the threshold voltage; a gradual rise in I_{DS} with increasing V_{GS} occurs instead of the textbook “hockey stick” curve. This aberrant behavior in Figure 3.2 is likely related to the

parasitic access resistance to the channel, which can be modeled as a barrier device in the source circuit. Nonetheless, it is possible to extract an “effective” saturation mobility and threshold voltage from this transfer curve to assess the performance of the device as a function of processing conditions. Statistically identical performance is obtained for devices fabricated on either PEN or silicon wafers.

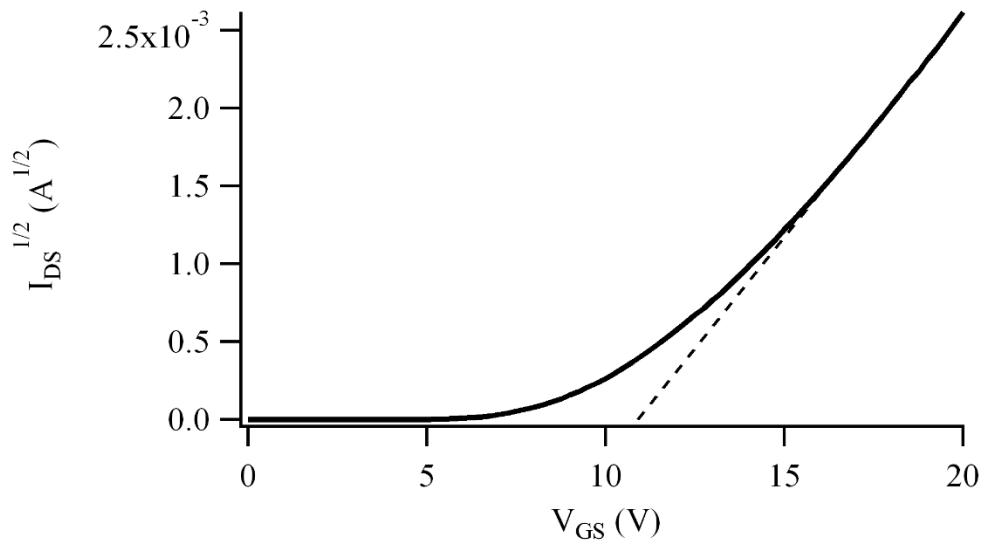


Figure 3.2: Representative Transfer Curve for a ZIO Based Transistor Using a Single Layer Channel. The Dashed Line is the Best Fit Used to Extract Threshold Voltage (11 V) and Saturation Mobility ($2.1 \text{ cm}^2/\text{V}\cdot\text{s}$).

Figure 3.3 shows how the oxygen concentration in the feed gas impacts the saturation mobility and threshold voltage for ZIO based transistors. For the range of conditions studied, a lower oxygen concentration in the feed gas leads to a desirable increase in the mobility and a decrease in threshold voltage. As the oxygen concentration in the feed gas is decreased it is likely that oxygen vacancy concentration in the deposited active layer increases. With 0% O_2 in the feed gas, the transfer curve for all devices has an appearance similar to the example shown in Figure 3.4, in which the devices exhibit a

lack of appreciable modulation of the drain current by the gate voltage. Thus oxygen cannot be completely eliminated in the feed gas since the resultant devices will be constantly ‘on’ due to the low resistivity of the film. These results are consistent with previously reported oxygen feed gas dependencies reported by Wager and coworkers (Chiang, et al. 2008).

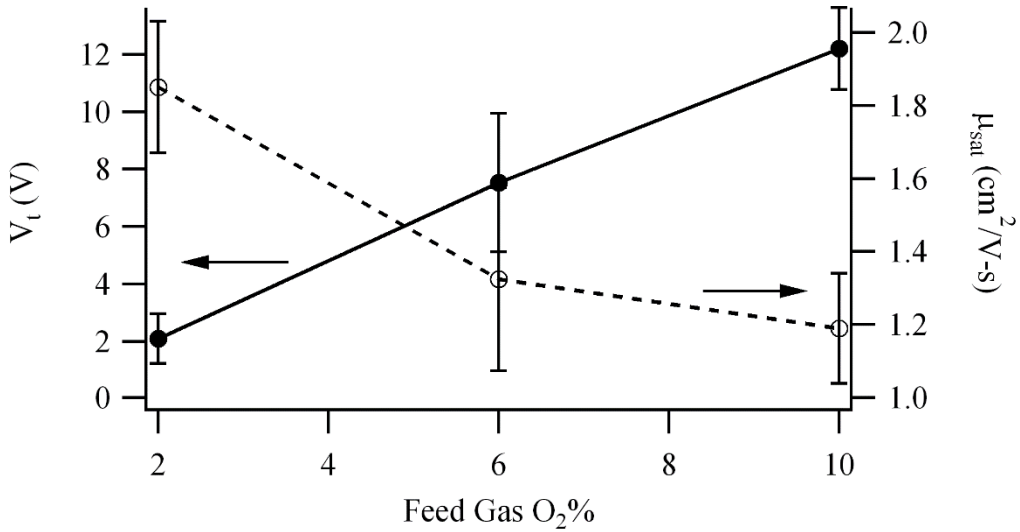


Figure 3.3: Impact of Oxygen Concentration in the Feed Gas During Deposition of the Active Layer on Threshold Voltage (●) and Saturation Mobility (■) (W/L = 10.5)

Dual Active Layer Device Results

Device performance can be improved by simply combining films with desirable features. For example, a film deposited with no oxygen in the feed gas with a resistivity of approximately 0.003 Ω-cm is too conductive for use as a single active layer and results in a short of the source to the drain (Figure 3.4). However, this increased conductivity is desirable in the first layer of a dual layer stack. Such a structure allows for a higher density of carriers near the gate dielectric interface without shorting the device. For the second layer, a ZIO film deposited with 2% oxygen concentration in the deposition feed

gas would be resistive enough at 10 Ω -cm to reduce the source to drain leakage current to 10^{-13} A when the device is in the off state. All dual layer devices described in this article utilize 2% oxygen concentration in the feed gas for the second layer.

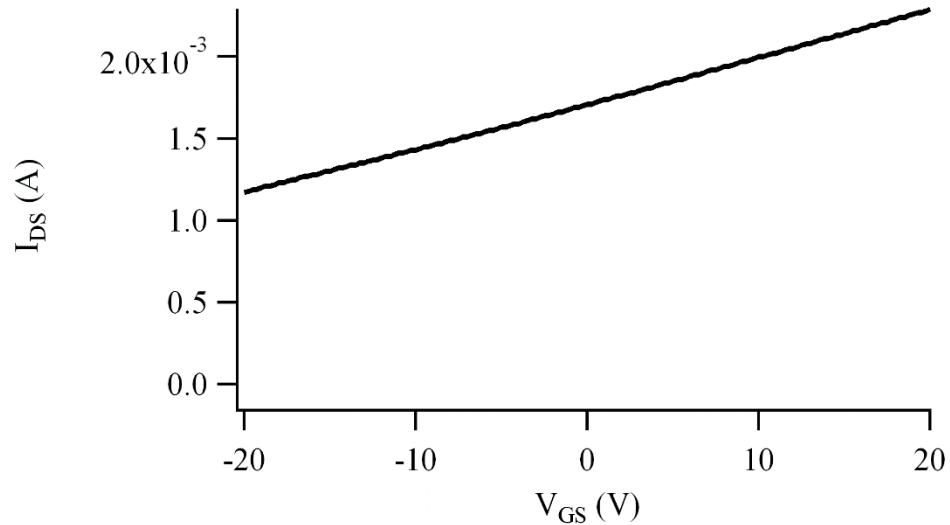


Figure 3.4: Transfer Curve of Device Fabricated without O_2 in the Feed Gas. This Device Lacks the Ability to Significantly Modulate the Drain Current with Applied Potential and is Considered as a Failed Device.

This strategy was used to fabricate a series of dual layer devices; Figure 3.5 shows the threshold voltage (a), saturation mobility and on-off ratio (b) of the resultant dual layer stacks versus first active layer thickness h_1 with total thickness held constant at 50 nm. Note that the data points at $h_1 = 0$ represent the values for the respective single layer ZIO or IGZO devices. The dual layer devices exhibit substantially higher saturation mobility and substantially reduced threshold voltage than the corresponding single layer devices. Greater performance improvements are observed for ZIO than for IGZO.

At $h_1 = 10$ nm for ZIO and $h_1 = 20$ nm for IGZO, the device yield is greater than 95%. The typical failed devices do not turn off as demonstrated by the lack of adequate

modulation of the drain current by the gate voltage (low on-off ratio) as shown in the example in Figure 3.4. As h_1 increases further beyond thicknesses reported in Figure 3.5, the fraction of devices that fail to turn off increases sharply and thus we have not reported their performance as the yield is unacceptable.

The improvement in the performance based on modulation in h_1 can be attributed to a decrease in the access resistance to the channel. The conductive channel, where the electrons flow from the source to the drain, is generally only a few nm thick (Tickle 1969). In a top contact/bottom gate device, the current must transit an unmodulated region of the semiconductor between the contact and the induced channel. The resistivity of the first layer, at approximately 0.003 Ω -cm, decreases the overall resistivity of the semiconductor and thus reduces the access resistance for the device.

In addition to the static performance difference, there is a change in the behavior of the devices under DC gate bias stress depending on h_1 . The change in the threshold voltage after 10 min of operation is compared in Figure 3.6 for various h_1 .

The composition of the active layer and h_1 have little effect on the threshold voltage shift during positive gate bias stress as the shift is approximately 1 V in most cases. However, the threshold voltage shift due to negative bias stress is strongly dependent upon the composition of the active layer. ZIO based devices exhibit a negative shift in the threshold voltage, while devices fabricated with IGZO TFTs show a positive shift. In addition the threshold voltage shift for ZIO devices is strongly dependent on active layer 1 film thickness, whereas the shift for IGZO is less sensitive to layer 1 thickness.

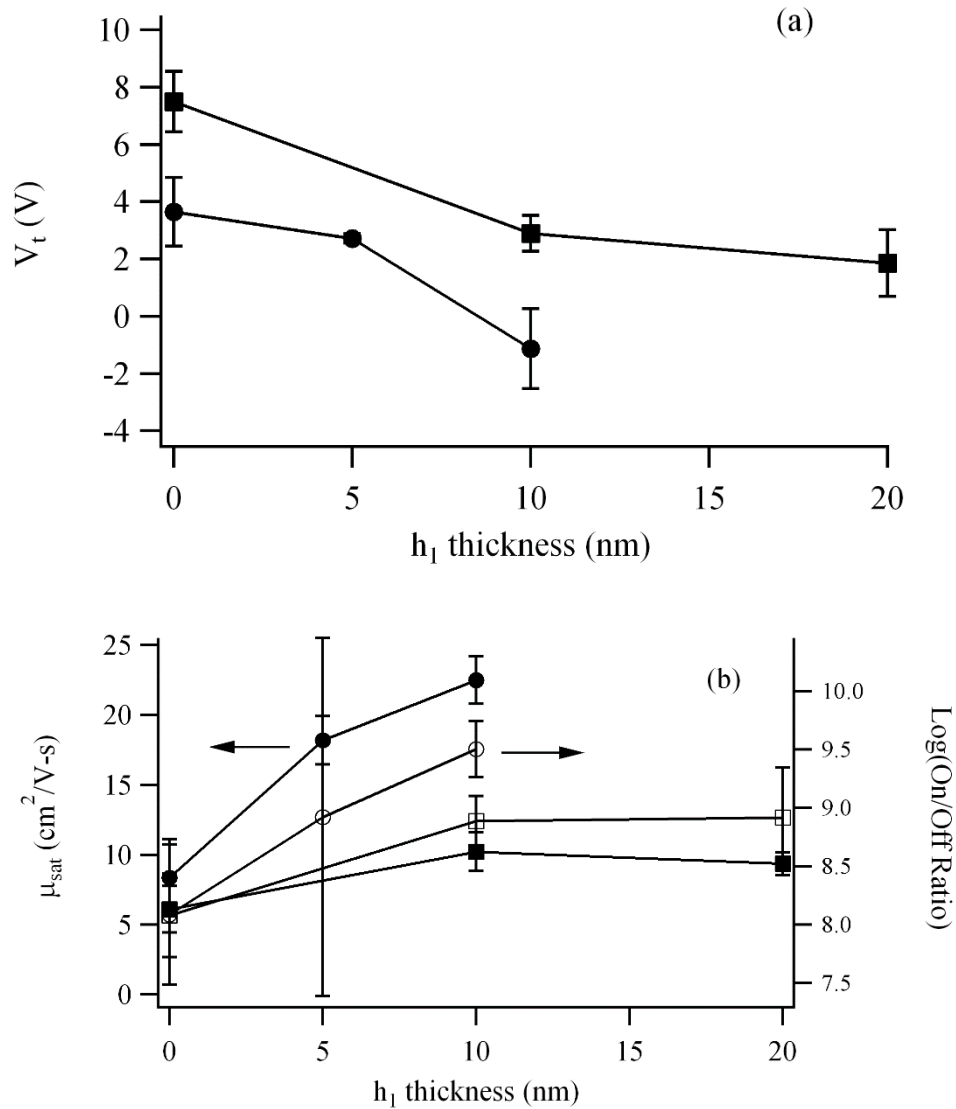


Figure 3.5: Impact of the Thickness of the First Active Layer on (a) Threshold Voltage, (b) Saturation Mobility (Closed Symbols), and On/Off Ratio (Open Symbols) for (●) ZIO and (■) IGZO Devices. The Cumulative Thickness of the First and Second Layers is Maintained at 50 nm in All Cases.

A large negative shift in the threshold voltage can lead to the TFT failing to turn off unless held at a negative potential, which is not practical for TFTs in operation. Conversely, the devices exhibiting a positive threshold voltage shift will require an

increasing amount of voltage to turn on until the threshold voltage drifts beyond the capability of the electronics controlling the TFTs or exceeds the breakdown voltage of the gate dielectric.

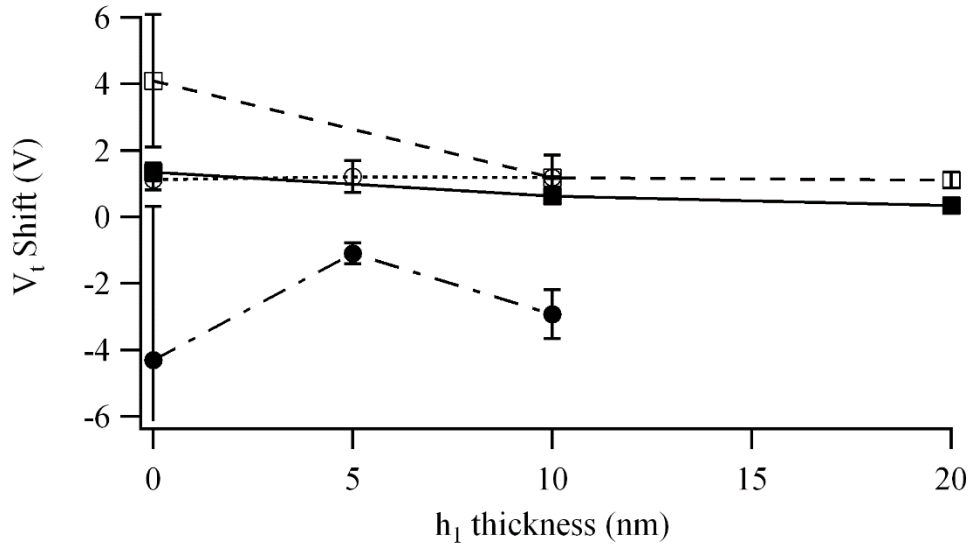


Figure 3.6: Impact of h_1 on the Threshold Voltage Shift Induced by Stress Condition for (\bullet , \circ) ZIO and (\blacksquare , \square) IGZO with $V_{GS} = -20$ V for 10 min (Closed Symbols) and $+20$ V for 10 min (Open Symbols).

Moreover for OLED applications, the variation in threshold voltage will lead to instabilities in the brightness and difficulties in color control. Thus, minimization of the threshold voltage shift is desired. This shift in the threshold voltage is typically related to mobile ions (for example, hydrogen from the PECVD silicon nitride or silicon oxide dielectrics), trapping of carriers due to oxygen vacancies, the creation of the defect states near the gate dielectric interface or in the active layer bulk, or any combination thereof. With this background, it is possible to understand the mechanisms by which the threshold voltage shift is dependent upon the composition and h_1 .

To understand the compositional impact of the difference in performance between ZIO and IGZO, the nature of the cation interaction with oxygen must be considered. Gallium bonds with oxygen are much tighter than analogous bonds between oxygen and indium or zinc; this difference will result in fewer generated oxygen vacancies for materials containing gallium. During reverse gate bias of the device, these vacancies can ionize and diffuse toward the gate. The net result is a negative shift in the threshold voltage over time when a negative gate bias is applied. As a result, the threshold voltage shift for IGZO under negative gate bias is less than that for ZIO (Figure 3.6). It is presently unclear why the threshold shift depends on h_1 . As h_1 decreases, it appears that the parasitic access resistance increases as evidenced by a transfer curve that is comparable to the extraction demonstrated in Figure 3.2. As the device is stressed, the access resistance drops due to the creation of oxygen vacancies and the threshold voltage extraction actually improves. The improving fit may exaggerate the perceived shift in the threshold voltage since the basis for parameter extraction is in effect different.

Mixed Active Layer Device Results

To further explore the performance of dual layer devices, a series of TFTs were fabricated through sequential deposition of ZIO and IGZO with varying composition of the active layers. Device architectures were systematically fabricated in which h_1 consisted of an oxygen deficient layer from one target while h_2 consisted of a more resistive layer deposited using the other target. As for all devices previously examined, the sum of h_1 and h_2 was set to 50 nm. Four device architectures with such “mixed” active layers were tested as described in Table 3.1.

Table 3.1: Active Layer Thickness and Composition of Devices Fabricated using Both IGZO and ZIO.

Device	d ₁	d ₂	d ₃	d ₄
h ₁ target	IGZO	IGZO	ZIO	ZIO
h ₁ feed gas O ₂ %	0%	0%	0%	0%
h ₁ thickness	10 nm	20 nm	5 nm	10 nm
h ₂ target	ZIO	ZIO	IGZO	IGZO
h ₂ feed gas O ₂ %	2%	2%	2%	2%
h ₂ thickness	40 nm	30 nm	45 nm	40 nm

Figure 3.7 shows the dependence of threshold voltage, on/off ratio and saturation mobility on the device structure as listed in Table 3.1. The mean saturation mobility ($9 \text{ cm}^2/\text{V}\cdot\text{s}$) and on/off ratio (6×10^8) of devices d₁ and d₂, which were fabricated by first depositing IGZO (h₁) and subsequently ZIO (h₂) without breaking vacuum, are not statistically different from the saturation mobility and on/off ratio of devices that were fabricated with a dual layer of IGZO that were presented in Figure 3.5. The same is true of devices d₃ and d₄, which were fabricated with ZIO as h₁ and IGZO as h₂ and feature a saturation mobility of $18 \text{ cm}^2/\text{V}\cdot\text{s}$ and on-off ratio of 2×10^9 . This mobility and on/off current ratio are not statistically different from the dual layer ZIO-only devices presented in Figure 3.5. The results again show that the initial device performance is strongly dependent on the h₁ thickness and composition.

The increased conductivity of h₁ also results in a much cleaner extraction of the threshold voltage as shown by a representative TFT in Figure 3.8a. The transfer

characteristics of the same device are also included (Figure 3.8b). The improved fit of the transfer curve is likely attributable to the lower resistivity of the active layer and thus the lower access resistance to the channel.

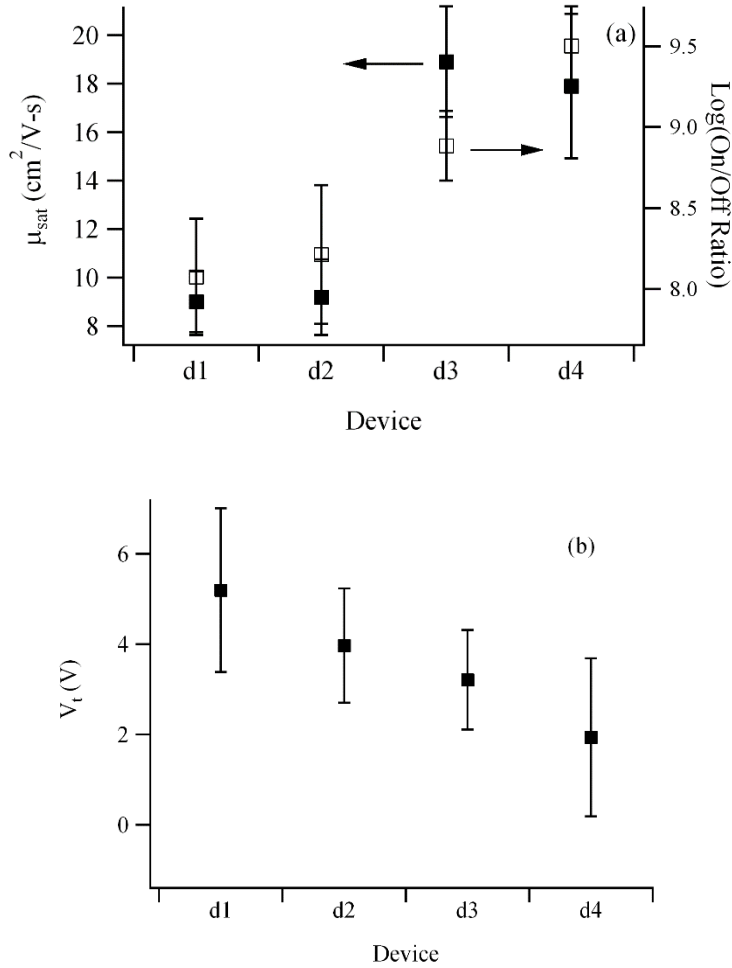


Figure 3.7: Initial Saturation Mobility, On/Off Current, (a) and Threshold Voltage (b) of Devices Described in Table 3.1.

The average threshold voltage shift based on the device structures described in Table 3.1 is shown in Figure 3.9. Devices d₁ and d₂, which feature IGZO as h₁, show a small, but statistically significant negative shift in the threshold voltage. This behavior is in contrast to the behavior observed for the dual IGZO active layer device shown in

Figure 3.6. The same behavior is observed for devices d_3 and d_4 which feature ZIO as h_1 . In both cases, it would appear that the threshold voltage shift due to negative gate bias stress is dependent on the composition of h_2 .

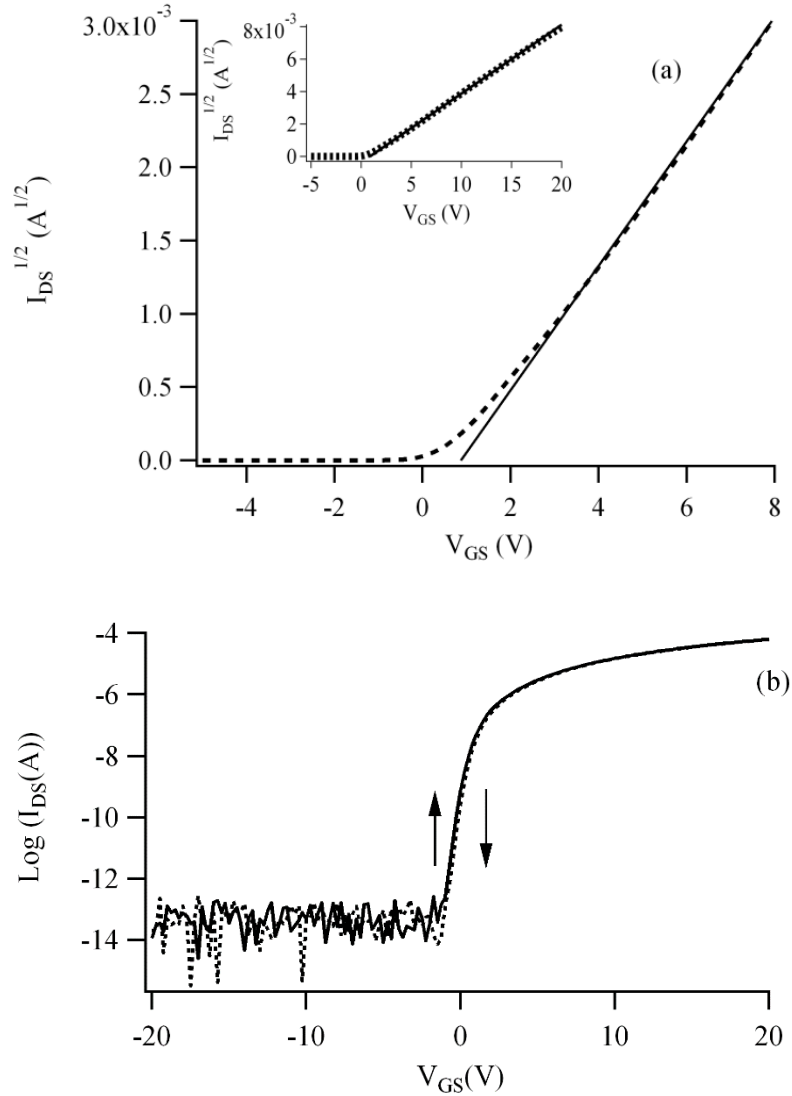


Figure 3.8: Threshold Voltage Extraction (a) and Transfer Characteristics (b) Showing Forward Sweep (Solid Line) and Reverse Sweep (Dashed Line) of Selected d_2 Dual Active Layer TFT.

As the threshold voltage shift is predominantly dependent upon the composition

of the second layer in the active stack, the source for oxygen vacancies (and ultimately the device instability) appears to be within or transported through this layer. If the vacancies are initially present when deposited, then it would be expected that turning off the transistors during the initial characterization of the device would be difficult. Thus, the vacancies are likely generated during operation. One potential source for such vacancies is through reaction of the molybdenum source-drain metal with the oxide semiconductor to generate oxygen vacancies at the contact with the second layer h_2 . Gallium bonds to oxygen are stronger than the analogous indium or zinc bonds to oxygen, therefore ZIO should be more susceptible to forming vacancies than IGZO.

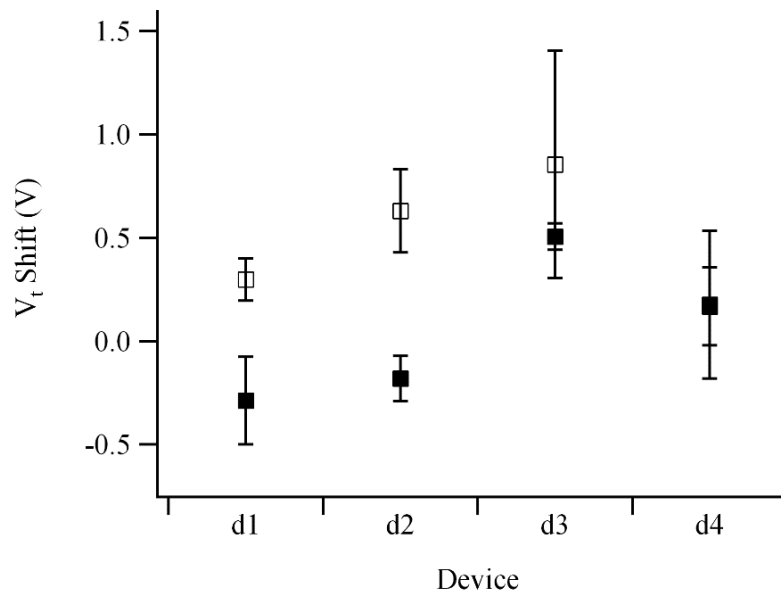


Figure 3.9: Threshold Voltage Shift Versus Device Structure and Stress Condition with $V_{GS} = -20$ V for 20 Minutes (Closed Symbols) and $+20$ V for 20 Minutes (Open Symbols).

As Figure 3.9 demonstrates, devices fabricated with ZIO as the second layer h_2 exhibit a negative shift in the threshold voltage under negative gate bias stress as one

would expect if oxygen vacancies were being generated. Devices with IGZO as h_2 actually demonstrate a positive threshold voltage shift under negative gate bias stress, which suggests that oxygen vacancy generation is not the dominant defect generation process.

Conclusions

A novel device structure for high performance and improved stability TFTs has been developed that is based upon a dual active layer architecture. Devices with this dual active layer exhibit improved performance and stability under gate bias stress when compared to their single layer counterparts. The film properties of the first layer in contact with the gate dielectric are critical in determining the initial saturation mobility and threshold voltage, while the properties of the second layer in the active stack appear to control the threshold voltage stability. By judiciously selecting the components of the two active layers, it is possible to achieve both high performance and good stability that cannot be easily obtained with a single layer device without high temperature annealing. The procedures used in the fabrication of these devices are extendable to a production process, in particular for manufacturing on flexible substrates where high temperature anneals are not possible.

CHAPTER 4 FLEXIBLE AMORPHOUS SILICON PIN DIODES FOR INDIRECT X-RAY DETECTORS WITH AMORPHOUS SILICON AND INDIUM GALLIUM ZINC OXIDE TRANSISTORS

Introduction

Radiography is currently the most common medical imaging procedure performed (Moy 1999). As the average age of the world's population increases, the demand for radiography is expected to increase dramatically especially in less developed countries where the market may skip conventional x-ray film technology and move straight to digital radiography (World Health Organization 2011). Remote locations in less developed countries may impose challenging equipment durability requirements, which may limit the use of existing fragile glass substrate based flat-panel digital x-ray detectors for digital radiography and create demand for a much more ruggedized version.

In addition to the growing demand from the medical diagnostic field, radiography has seen expansive growth into non-medical markets, such as security imaging and non-destructive testing for integrity analysis (i.e., looking for micro-cracks and crack initiation in pipelines or inspection of aircraft structures). There is an increasing demand for more portable, flexible, rugged, and lightweight radiation detectors for medical first responders, military, and security applications where digitizing the x-ray image can allow it to be electronically transmitted to remote experts for immediate analysis. Some possible applications for ruggedized, flexible radiation detectors include the remote analysis of radiographs taken on the battlefield or in limited-infrastructure locales, non-

destructive testing of curved objects such as oil pipelines and airplane wings, and identification of suspicious objects where a fixed detector is impractical.

Though some portable x-ray panels do exist, they are comprised of glass TFT panels, and are rather bulky due to the ruggedization (extensive reinforcement) required to protect the costly panel from breakage. Ruggedization is already employed in tablets in liquid crystal displays (LCD) in order to meet United States military specifications (mil spec). As the basic components of a radiation detector are similar to an LCD display, one can compare the weight of a consumer tablet with that of a tablet that meets mil spec. For example, the Apple iPad 2 uses a 9.7” LCD display and weighs approximately 0.6 kg (Apple Inc. n.d.), while a ruggedized Guardian Model 310 tablet with a 10.4” diagonal display weighs 2.8 kg (Industrial Computing n.d.), over 4 times more than the iPad2. Given the cost of these panels, it would be advantageous to have a more rugged system that would be less prone to breakage and be much lighter for mobile users to carry.

Along with being both portable and lightweight, a digital x-ray panel with some degree of flexibility or bendability is also an appealing medical diagnostic or industrial imaging tool, especially if the overall digital x-ray detector thickness can be also minimized. A paramedic would be able to easily slide a thin and slightly flexible digital x-ray detector panel directly underneath the victim of a car accident at the scene or an inspector could wrap the x-ray detector around an oil pipeline for non-destructive structural health monitoring. Ruggedization of conventional glass TFT panels can increase their thickness up to approximately 2 inches, which clearly makes them more difficult to slide underneath an injured patient who likely needs to be disturbed as little as possible.

The a-Si PIN diode-based detectors are not limited to x-ray detectors; they can be readily adapted to detect neutrons, alpha particles, or other forms of radiation with the appropriate conversion layer. In this paper, we report on the challenges of implementing a PIN diode fabrication process on a flexible substrate and the results of the successful fabrication of a 200 mm diagonal x-ray detector fabricated on flexible Gen II (370 mm x 470 mm) polyethylene naphthalate (PEN) substrate.

Digital X-Ray Detector Operation

The basic components of an indirect digital x-ray detector include a conversion film that converts the incident x-rays into visible photons, a photodiode that detects the light emitted from the x-ray phosphor conversion film, and a thin film transistor (TFT) that acts as a switch for the readout of the charge collected. The fabrication of an x-ray detector is similar to a flat panel LCD, while the operation of the panel can be compared to a large digital camera. The x-ray source typically consists of a vacuum tube in which high voltage (30-150 kV is typical) electrons are accelerated into a metallic anode. The accelerated electrons pass close to the nuclei of the target material, or strike an inner shell electron in some cases, and produce an x-ray as the electron is slowed considerably by the opposing charge of the nucleus (Zink 1997). In the event of an inner electron shell collision, an electron from the outer shell moves into the vacancy in the inner shell and give off an x-ray with energy that is characteristic of the anode material.

X-rays from the source pass through the patient or device under examination with some of the x-rays attenuated by the nuclei of the intervening material. At the kilovolt energies typically employed by medical x-ray detectors, attenuation is usually the result of photoelectric absorption or Compton scattering. Photoelectric absorption produces

meaningful data because an x-ray photon is absorbed and releases an electron from the absorbing atom. The x-ray absorption is proportional to the atomic number, the density, and the thickness of the absorbing media (Carlton and Adler 2012). As an example, bone, which has a higher effective atomic number and is relatively dense, will absorb more x-rays than soft tissue, which results in a contrast difference in the completed radiograph.

X-rays that do pass through the patient are absorbed by the detector. A flat panel digital x-ray detector is usually classified as direct conversion or indirect conversion depending on the process for converting the incident x-rays into charge. Direct conversion detectors utilize a photoconductive layer of amorphous selenium, which absorb the x-ray and produce an electron/hole pair. When a bias is applied across the selenium, the generated charge carriers are pulled towards the electrodes. When an x-ray is absorbed and generates an electron/hole pair, the charge carrier is drawn to the opposing electrode with limited scattering in comparison to indirect detection techniques (Schaefer-Prokop, et al. 2008). However, the amorphous selenium has a smaller capture cross-section in comparison to the cesium iodide (CsI) screens used in indirect conversion thus requiring the patient to be exposed to a higher dosage of x-rays to achieve the same resolution. In addition, the selenium film is usually 0.25-1.0 mm thick requiring a large voltage on the order of 10kV across the selenium to provide a sufficient electric field to extract the incident x-ray generated charge carriers (Schaefer-Prokop, et al. 2008). The main advantage of amorphous selenium is the spatial resolution of the detector.

Indirect sensor arrays usually fall into one of two device structures: passive pixel sensors and active pixel sensors. In an indirect passive pixel sensor array, the TFTs are

laid out in a grid and are connected to a gate line and a source line. There is one TFT per cell (pixel), which performs the function of a switch. The gate lines bias the TFTs “on” to enable the source lines to carry charge that was stored in the PIN diode to charge sense electronics at the edge of the panel. The gate lines are scanned sequentially so that only one gate line is on at any given time; the remaining gate lines and TFTs are off and the associated PIN diodes accumulate charge depending on the number of scintillator photons incident to the diode. The scan rate depends on the application, but can vary between 10 Hz and full video (60 Hz). The charge is drained from the diode through the TFT within 10-100 μ s where it is analyzed by circuitry in the periphery and transmitted to a computer to produce a digital image.

Active pixel sensor arrays differ from passive pixel sensor arrays due to the presence of additional circuitry that provides in-cell amplification. In a typical passive pixel, one incident photon produces no more than one electron. Active pixel sensors produce more than one electron either by introducing additional layers in the PIN diode structure to induce carrier avalanche, or by adding transistors, such as a common source amplifier, to multiply the charge stored in the diode. Amorphous silicon TFTs have very low mobility and are ill-suited for amplifiers. IGZO devices are more suited as the higher mobility of IGZO allows for smaller transistors to be used for the amplification circuitry.

The PIN diode is operated under a negative bias on the order of -5 to -10 V, which leads to the creation of a large depletion region in the PIN diode. When the TFT is off, photons are absorbed which generate electron-hole pairs causing the depletion region to diminish. During readout, the diode ideally returns to its pre-irradiated state with all of

the photo-generated electrons passing through the TFT. Any leftover carriers can create a ghost image known as image lag.

a-Si TFT Process

The TFT process is loosely based on the process first described by Raupp, et al. in 2007 (Raupp, et al. 2007), and utilizes amorphous silicon (a-Si) as the active material. Amorphous silicon was chosen initially because they are the most common TFT technology found in digital x-ray detectors. The difficulty in focusing x-rays creates a need for a large area detector. Historically, this requirement made the a-Si TFT technology that had already been heavily researched and employed to fabricate LCDs of a similar sizing scale a logical choice as the TFT technology for digital radiography.

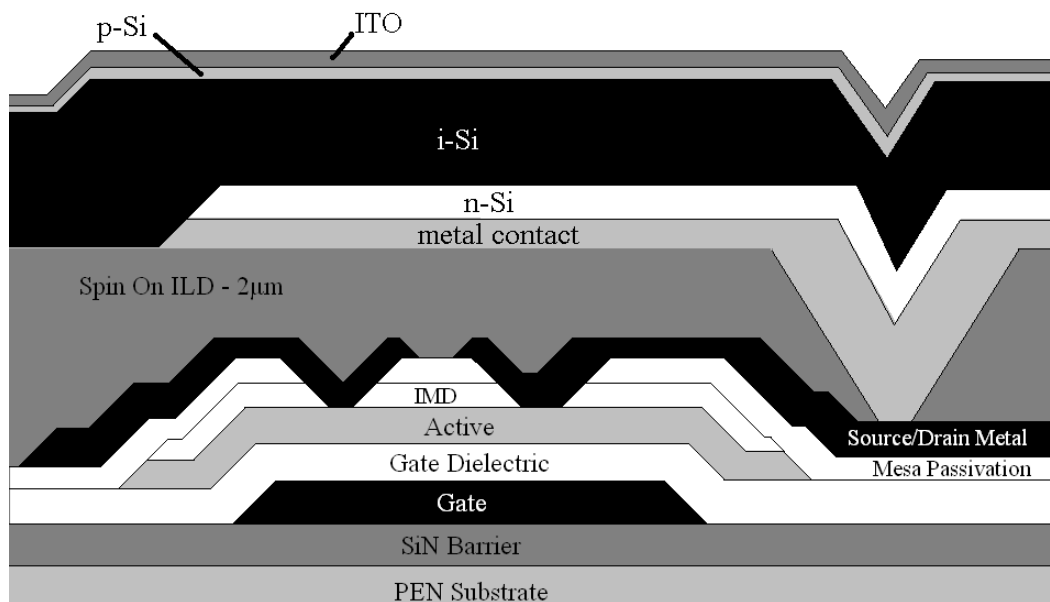


Figure 4.1. Backplane Pixel Structure

Fabrication begins with lamination of a polyethylene naphthalate (PEN) substrate to a rigid carrier via a temporary adhesive (Haq, et al. 2010). The PEN substrate is capped with a SiN barrier that acts as an etch stop to protect the PEN substrate from

damage and as a barrier against moisture and oxygen transmission through the PEN. The TFTs for the sensor array were fabricated with a bottom gate, inverted-staggered design and feature one transistor (passive pixel device) and one PIN diode for each pixel as shown in Figure 4.1.

The TFT fabrication process is completed in 4 masks (Gate, Active Island, Contact, and Source/Drain) with an additional 3 masks for the interlayer dielectric (ILD) and PIN diode layer patterning. In this work the active layer consists of plasma enhanced chemical vapor deposition (PECVD) a-Si; the gate dielectric, intermetal dielectric (IMD), and Mesa Passivation layers are all PECVD silicon nitride (SiN). The deposition temperature of the PECVD steps is maintained at 185°C (significantly below the melting point of the PEN substrate), while the maximum process temperature is 200°C, required for the one hour cure of the organic fluoropolymer-based ILD.

Figure 4.2 shows typical performance of the a-Si TFTs. The TFT array process was originally designed to produce backplanes for flexible electrophoretic and organic light emitting diode (OLED) displays on 150 mm substrates and was eventually scaled up to Gen II (370 x 470 mm) rectangular substrates. This work leverages the prior extensive development by integrating a PIN diode with each pixel TFT instead of the display imaging layer. The operation of the detector is analogous to the operation of a display whereby the gate lines are scanned multiple times per second. As opposed to displays, where drivers supply a specific voltage along the data line to set the condition of the individual pixel, a charge sense amplifier reads the charge that had been stored in the PIN diode. As with displays, it is important that the pixel TFTs have low leakage (on the order of 10 fA) in the off state and acceptable mobility (greater than 0.1 cm²/V-s for the lowest

frame rate applications) that does not vary significantly with irradiation and applied gate and drain bias stress.

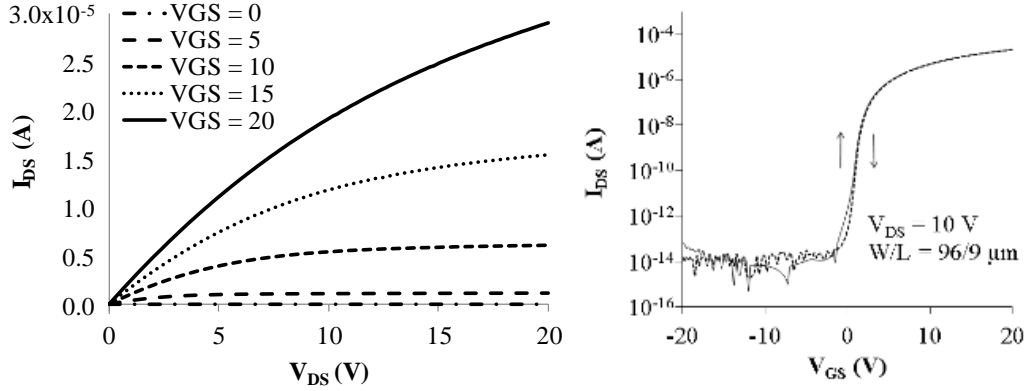


Figure 4.2. Typical Output (Left) and Transfer (Right) Characteristics of a-Si TFT on Flexible Gen II PEN Substrate after PIN Diode Processing. The Extracted Saturation Mobility is $0.7 \text{ cm}^2/\text{V}\cdot\text{s}$.

Oxide TFT Process

Although a-Si is the most common TFT technology, there are other materials that could be used as the TFT active material. LCD and organic light emitting diode (OLED) display have also been successfully fabricated in production with polysilicon and mixed metal oxide semiconductors such as indium gallium zinc oxide (IGZO). Polysilicon is generally not favored for radiation detectors because its grain boundaries are more susceptible than a-Si to radiation damage by incident x-ray photons that are not captured and converted by the scintillator layer (Zentai 2011).

Oxide semiconductors have drawn considerable attention due to their unique electrical and optical properties (Hosono, Yasukawa and Kawazoe, Novel Oxide Amorphous Semiconductors: Transparent Conducting Amorphous Oxides 1996). Thin

film transistors fabricated with an oxide channel have shown higher saturation mobility, lower off current, and improved threshold voltage stability in comparison to amorphous silicon (a-Si:H) (Marrs, Moyer, et al. 2011), thus enabling higher resolution detectors with higher refresh speed for applications such as digital fluoroscopy. Additionally, these mixed metal oxides can be deposited using conventional RF or DC sputtering techniques near room temperature and can be incorporated into an existing a-Si production facility with minimal capital investment (Wager 2014).

Oxide TFT-based x-ray detectors were fabricated as a comparison to the a-Si TFTs using the same inverted-staggered trilayer structure presented in Figure 4.1. The IGZO layer was deposited by reactive DC sputtering using a ceramic target with an atomic formula of $\text{In}_2\text{Ga}_2\text{ZnO}_7$. The fabrication process features PECVD silicon oxide for the IMD and gate dielectric in place of silicon nitride. The gate dielectric, active layer, and IMD are deposited in sequence with minimal delay to protect the IGZO active layer from atmospheric contamination. The temperature of all PECVD steps does not exceed 185 °C.

The deposition conditions of the gate dielectric and IMD layers can have a profound effect on the device output performance especially in the case of plasma enhanced chemical vapor deposition (PECVD). Hydrogen in the plasma can react with the exposed IGZO to produce additional oxygen vacancies resulting in higher source to drain leakage. If the damage from the hydrogen is too severe, the backchannel surface will become sufficiently conductive to the degree that transistor characteristics are not realized.

PECVD silicon nitride (SiN) films generally have an atomic concentration between 20% and 30% hydrogen when the deposition temperature is set to 185°C or less. We found that TFTs fabricated with SiN as the gate dielectric or IMD failed to exhibit transistor transfer characteristics. PECVD SiO₂ films have a lower concentration of hydrogen (< 5% is typical), and IGZO TFT's fabricated with SiO₂ exhibit good transfer characteristics representing a significant improvement over previously reported a-Si TFTs [1] as demonstrated in Figure 4.3.

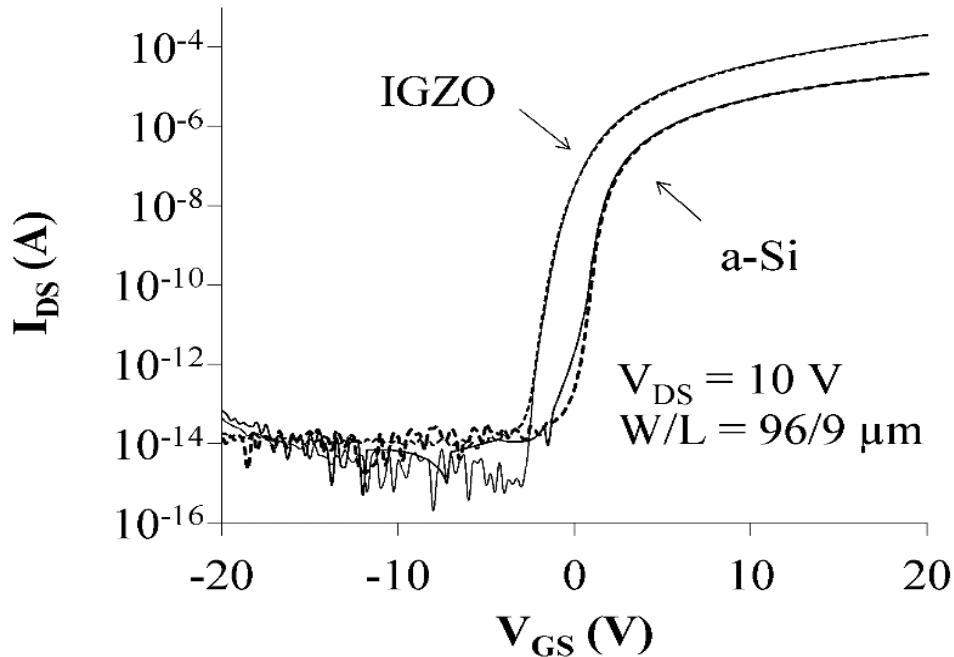


Figure 4.3. Transfer Characteristics Showing Forward Sweep (Solid Line) and Reverse Sweep (Dashed Line) of Selected IGZO and a-Si TFT (96x9 μm Device Geometry with IGZO $\mu_{\text{sat}} = 13 \text{ cm}^2/\text{V}\cdot\text{s}$ and a-Si $\mu_{\text{sat}} = 0.7 \text{ cm}^2/\text{V}\cdot\text{s}$)

The SiO₂ gate dielectric and IMD experiments demonstrate that the hydrogen composition of layers in direct contact with the active layer significantly affects device performance. However, there are other dielectric layers in the device structure shown in

Figure 4.1 that do not contact the IGZO. An example is the SiN barrier layer. The barrier layer acts as an etch stop for the gate metal etch, protecting the PEN substrate from etch damage. In addition, the barrier layer is a moisture barrier that protects the TFT and diode from atmospheric contamination that can adversely affect IGZO TFT performance (Jeong, Yang, et al. 2008). Water vapor transmission rates through SiN are typically lower than SiO₂, so SiN is preferred for barrier applications. However, the gate dielectric and IMD study show that hydrogen inclusion in the film can lead to persistent conductivity in the IGZO.

In order to test the effect of hydrogen concentration of the barrier layer on IGZO TFT performance, three barrier layers with differing hydrogen concentrations were grown on silicon substrates to eliminate the effect of moisture transmission through the substrate. The hydrogen concentration in the barrier layer was estimated using Fourier transform infrared spectroscopy and the methods described by Lanford and Rand (Lanford and Rand 1978). The first barrier (Barrier 1) layer was 300 nm of thermal silicon dioxide, which had no detectable concentration of hydrogen as determined by FTIR. The second barrier layer (Barrier 2) was a PECVD grown 300 nm SiN layer with a hydrogen concentration of 8×10^{21} atoms/cm³. The third barrier layer (Barrier 3) was a PECVD grown 300 nm SiN layer with a hydrogen concentration of 4×10^{22} atoms/cm³. A total of 80 devices were fabricated with each barrier layer. The other device layers were processed the same.

The results in Figure 4.4A show that the threshold voltage shifts in the negative direction with increasing hydrogen concentration and suggest that hydrogen is diffusing into the gate dielectric and possibly all the way to the active layer. The mechanism

appears diffusion related as the magnitude of the threshold voltage change depends on the hydrogen concentration.

The results show that hydrogen incorporation can affect the performance of IGZO even when the hydrogenated layer is not in direct contact with the active layer. Amorphous silicon (a-Si) based PIN diode processing involves multiple PECVD steps with a significant concentration of hydrogen in the plasma and deposited films. Therefore, it is important to account for changes in the threshold voltage of the IGZO as a result of the hydrogen necessarily incorporated into the diode films. A comparison of the transfer characteristics before and after the PIN diode process is shown Figure 4.4B. The threshold voltage shifts in the negative direction (~ 5 V) after PIN diode deposition. The off current is an important metric for the readout TFT since a significant off current will increase the noise in the detector output. Therefore, it is necessary to adjust the IGZO deposition process to obtain a significantly positive threshold voltage to offset the negative threshold voltage shift caused by the PIN diode process. The threshold voltage can easily be adjusted by increasing the oxygen content of the feed gas during the IGZO sputter deposition (Chiang, et al. 2008). Another option for mitigating the threshold voltage shift is to change the PIN diode process. However, the PIN i-Si deposition is quite sensitive to changes in the hydrogen flow. Moreover, for fabrication of flexible detectors the constraint of low stress processing of the various thin films presents additional complications. For these reasons we prefer to focus on process modifications to “pre-compensate” the TFT rather than PIN diode process changes.

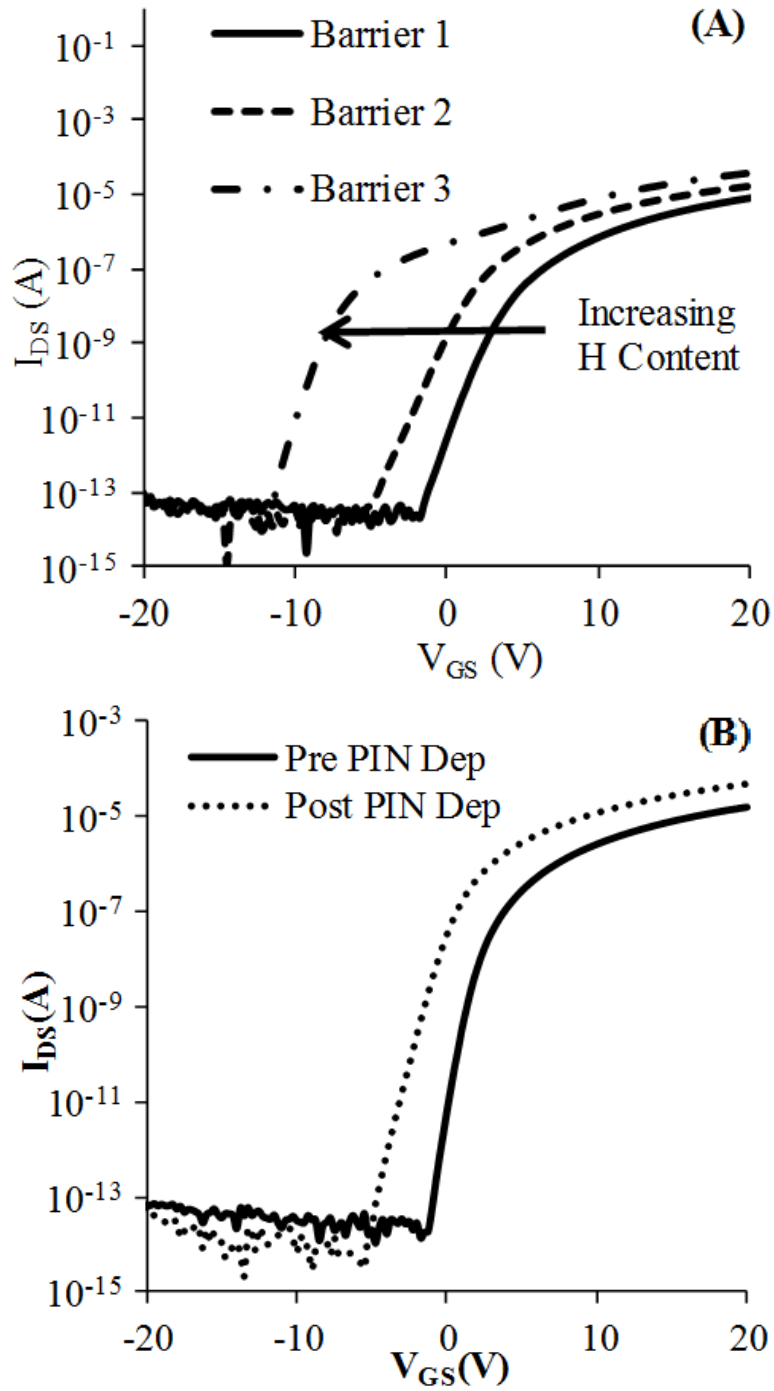


Figure 4.4. I_{DS} - V_{GS} Curve of Selected $9 \times 9 \mu\text{m}$ TFT Devices with Barrier 1, Barrier 2, and Barrier 3 Deposition Process (A) and of IGZO TFT Before and After PIN Diode Deposition (B)

Another potential issue with using IGZO in an x-ray detector is the stability of the threshold voltage under ionizing radiation. This so-called radiation hardness and has not been studied extensively for IGZO. The scintillator material does not convert all of the incident x-ray photons into light and some x-rays will be absorbed by the TFT. The radiation hardness of IGZO was tested by exposing IGZO TFTs to a known dosage of gamma radiation from a cobalt 60 source. The device transfer characteristics were measured and then the device was placed in the radiation chamber for additional exposure. Unfortunately, the TFTs could not be tested under reverse bias, which would mimic the actual operation of an x-ray detector. The transfer characteristics were plotted for dosages of 0, 15, and 122 krad in Figure 4.5. The selected TFT demonstrates approximately a total net -2 V shift to the threshold voltage.

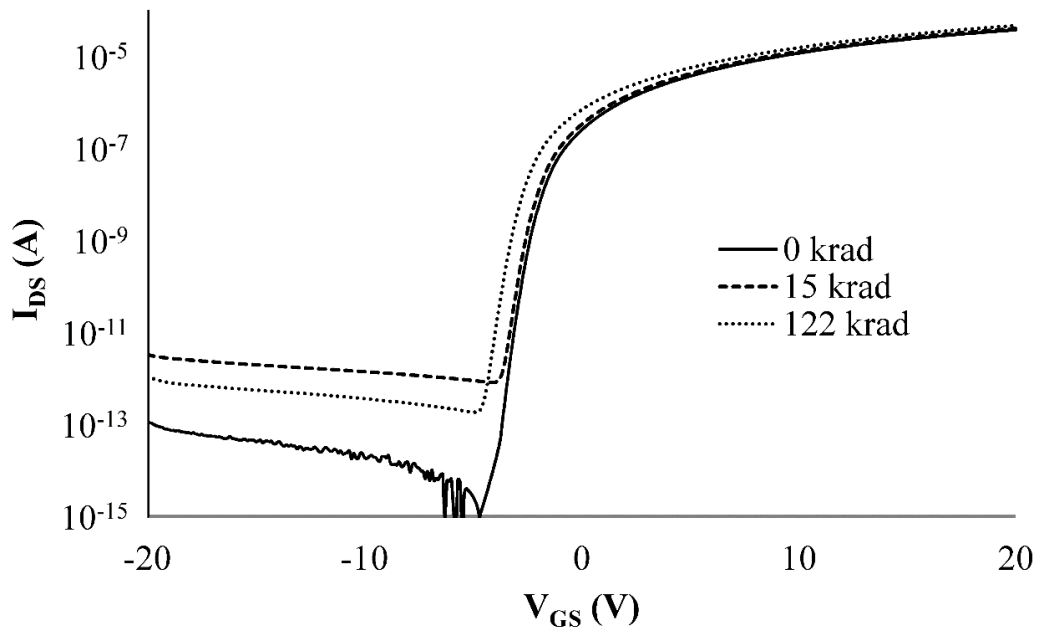


Figure 4.5. IDS-VGS of Selected 9x9 μm TFT Device after Exposure to Doses of 0, 15, and 122 krad of Gamma Radiation from a Cobalt-60 Source

Although the shift is relatively small given the dosage, the shift occurs in the negative direction and exhibits an increase in the dark current. The increase in dark current will reduce the sensitivity of the detector by increasing the noise floor, meaning that a higher x-ray dosage will be required for a given signal to noise ratio as the detector ages. The mechanism of the degradation is not fully understood at this time. However, other groups have shown similar results for IGZO TFTs when exposing the devices to irradiation from sources with a higher energy than the band gap of IGZO (~3.1 eV). In all cases, the effect of the radiation was to shift the threshold voltage in the negative direction due to the ionization of oxygen vacancy sites throughout the IGZO which can lead to trapping of photo-generated holes either at the IGZO/gate dielectric interface or the injection of photo-generated holes into the gate dielectric (Ghaffarzadeh, et al. 2010) (K. H. Ji, J. I. Kim, et al. 2010).

PIN Diode Fabrication

Once the TFT fabrication is complete, a planarizing fluoropolymer ILD layer is spray coated on the surface to a thickness of 2 μm in the field using an EVG 150 spray coater, followed by a 200°C bake with a 1 hour soak time in a Despatch LCD2 Oven. The planarization of the device layers allows for almost full fill factor fabrication. In addition, the ILD material provides a significant diffusion barrier for hydrogen or other contaminants. The ILD contacts are opened using dry etching. The sidewalls are sloped to allow for adequate step coverage of the subsequent thin film deposition steps. The n-Si contact metal and the n-Si layer are deposited after the ILD is patterned. The n-Si contact metal consists of a trilayer stack of tantalum, aluminum, and tantalum each grown to 50 nm thick. The n-Si and n contact metal are exposed beyond the edge of the array and

must be intact after the subsequent processing steps to enable electrical contact to the drivers. The Ta/Al/Ta layer is designed to be compatible with the indium tin oxide (ITO)/p-Si/i-Si etch process. The n-Si is patterned at each pixel via dry etching with a minimum spacing between each pixel of 56 μm . The entire pixel is a 207 μm square.

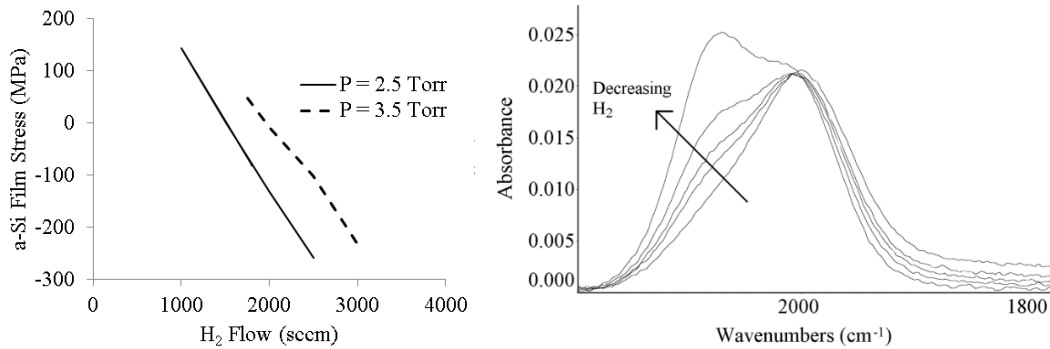


Figure 4.6. Effect of H₂ Gas Flow Rate During a-Si Deposition on Film Stress (Left) and FTIR Spectra (Right). The FTIR Spectra are Focused on the Si-H Stretching Peak at 2000 cm^{-1} and the Si-H₂ Stretching Peak at 2090 cm^{-1} . All Spectra are Plotted on a Common Scale with Baseline Correction.

The i-Si, p-Si, and ITO (10% tin doping) are deposited following the n-Si etch. The i-Si layer is grown to a thickness of 1.2 μm in an AKT 1600 PECVD system compatible with Gen II substrates to enable the capture of photons emitted in the visible wavelengths and to maximize the shunt resistance (leakage path between the p-Si and n-Si layers) of the PIN diode. Amorphous silicon PIN diodes generally demonstrate peak quantum efficiency in the green wavelengths; therefore, MCI DRZ-Plus Tb doped Gd₂O₂S scintillators, which convert x-rays to visible light with peak emission near 545 nm, are laminated on top of the PIN diode structure. The ITO layer is deposited 50 nm thick to allow adequate transmission of light from the scintillating layer to the photodiode

while minimizing the reflection of light at the p-Si/ITO interface and serving as the V_{bias} connection to the diodes.

The most challenging aspect of the deposition process is the control of the i-Si film stress while maintaining adequate device performance. Initial fabrication runs used the TFT active layer a-Si deposition process for the i-Si deposition. The film stress for the TFT a-Si deposition process is -701 ± 39 MPa on average. Unfortunately, the relatively high stress of the a-Si film resulted in excessive curl after the array was debonded from the rigid carrier, which precluded the drivers from being attached to the array. Such excessive curl is not observed in the standard display process because the area of the high stress a-Si active layer constitutes only 0.87% of the pixel cell area, whereas the i-Si PIN layer covers 100% of the pixel cell. In addition, the i-Si film is 24 times thicker than the 50 nm thick TFT active layer.

A number of process parameters could be adjusted to produce a lower (i.e., less negative) stress a-Si deposition. However, many simple single parameter adjustments achieve lower thin film stress at a cost of the quality of the i-Si film and associated device performance. For example, film stress can be decreased by lowering the H_2 concentration in the SiH_4/H_2 mixture fed into the PECVD chamber as shown in Figure 4.6. In this process, hydrogen acts as an etchant and participates in the breakdown of the SiH_4 . Reducing the H_2 flow results in an increase in the concentration of silicon polyhydrides and a systematic decrease in the index of refraction indicative of an increase in the porosity. The collapse of hydrogenated voids in the film is responsible for an increase in the tensile stress (i.e. more positive intrinsic film stress) (Johlin, et al. 2012).

The silicon/hydrogen bonding structure of the a-Si film was investigated via transmission infrared spectroscopy using a Thermolectron ECO/RS Fourier Transform Infrared Spectrometer (FTIR). Figure 4.6 shows the dependence of the IR absorbance spectra on the H₂ gas flow. The increased concentration of silicon polyhydride bonding is evidenced by the presence of a shoulder in the FTIR spectra of the a-Si thin film in the Si-H stretching peak centered at 2000 cm⁻¹. The shoulder is actually a separate peak at 2090 cm⁻¹ that depends on the concentration of Si-H₂ and Si-H₃ bonds present in the film. The area of the shoulder increases with decreasing H₂ gas flow.

Silicon polyhydrides are undesirable because they are electrically active defects that provide a leakage path through the diode under dark conditions and inhibit the transit of photogenerated electrons via recombination (Lucovsky, et al. 1989). Simply decreasing the hydrogen gas flow alone is therefore not an acceptable solution. A suitable balance between film stress and film quality can be achieved by finding the optimal balance between adjustments of the other process parameters of the AKT 1600 PECVD system (process pressure, susceptor spacing, and deposition power). Our final process recipe provides an adequate quality i-Si film with a film stress of -80 MPa at a deposition rate of 20 nm/min.

Another method for reducing the overall stress on the flexible substrate involves adjusting the film thickness of the i-Si. Naturally, there is a tradeoff between the percentage of incident light that is absorbed and the film thickness, so it is important to consider the application when deciding on the i-Si thickness. This is one area where indirect detectors have a significant advantage over direct detectors. In a direct detector, the detector material must be grown to thickness adequate to absorb most of the x-rays. In

the case of amorphous selenium, which is the most common direct detector, the selenium must be on the order of 20 μm thick. However, with indirect detectors, one can laminate, or simply place on top of the detector depending on the application, the scintillator after processing. Therefore, the scintillator does not go through the aggressive temperature cycling of the deposition processes imparting stress due to coefficient of thermal expansion differences. The scintillator material could be tailored to emit visible light (peak wavelength is 545 nm in this paper) in a region where the absorption depth is much shallower and the efficiency is much higher for the semiconductor diode allowing for a thinner i-Si film.

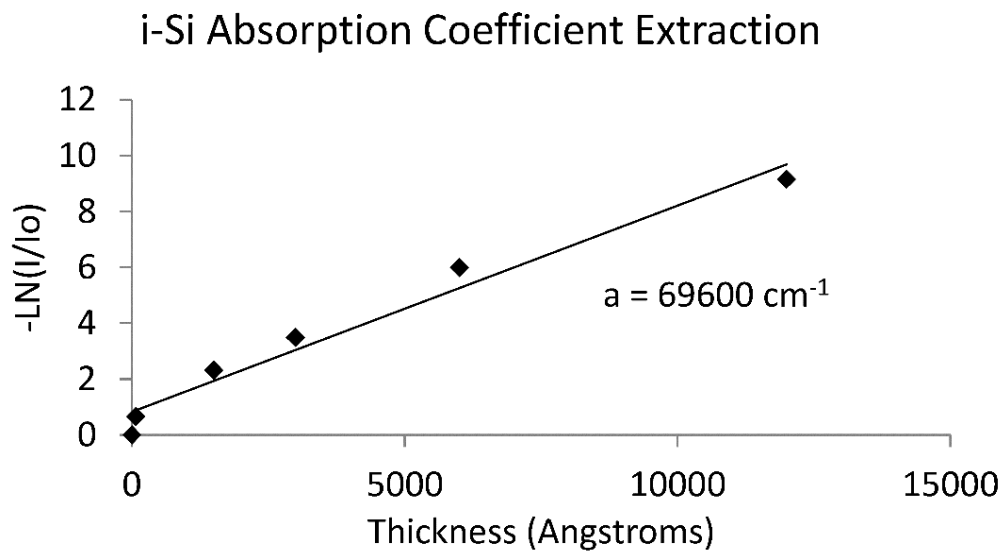


Figure 4.7. Semilog Plot of the Ratio of the Light Transmitted to the Light Incident Versus the Thickness of the i-Si Layer

The absorption coefficient for the low stress i-Si film was determined using UV-Vis spectroscopy by measuring the transmittance of various thicknesses of the i-Si film. The transmission of 545 nm light, which is the peak emission wavelength of the

scintillator material, was plotted versus the i-Si thickness in Figure 4.7 to determine that the absorption coefficient at 545 nm is 69600 cm^{-1} . At a film thickness of 6000 \AA , 99.25% of the 545 nm light is absorbed which should be adequate enough to avoid any meaningful reduction in the quantum efficiency.

PIN Diode Results

PIN diode test structures with an active area of 1 mm^2 were fabricated to test the performance of the lower stress i-Si deposition process. A probe station fitted with a Keithley 4200 Semiconductor Characterization System was used to characterize the diode performance. The probe card on the probe station is fitted with a green diffuse LED illuminator, which imparts an irradiance of 132 W/m^2 at a peak wavelength of 520 nm. The diode is swept from -5V to +1V in the dark and again with the illuminator set to maximum. The fill factor, open circuit voltage (V_{OC}), and short circuit current (I_{SC}) are extracted from the illuminated curve. The dark characteristics are fitted to the ideal diode equation (Equation 4.1)

$$I_D = I_S \left(e^{\frac{qV_D}{nkT}} - 1 \right) \quad 4.1$$

where I_D is the diode current, I_S is the reverse saturation current, q is the charge of an electron, V_D is the voltage applied across the diode, n is the diode ideality factor, k is Boltzmann's constant, and T is the temperature. The reverse saturation current and diode ideality factor can be extracted from plotting the I-V characteristics of the diode in the dark on a semilog plot. The saturation current and ideality factor are related to the carrier lifetime with lower values for both parameters indicating longer carrier lifetime

indicating a higher quality diode. In addition to fitting the ideal diode equation, the minimum dark current and the dark current at -5 V are extracted. The applied voltage across the diode (V_{bias}) in the sensor array is usually -4V.

The extracted diode ideality factor is 1.48 +/- 0.08 for the low stress flex Gen II process at an i-Si thickness of 1.2 μm while the dark current median is 2.4 pA/mm^2 at V_{bias} of -5V while the median minimum dark current is 0.1 pA/mm^2 . The quantum efficiency of the diode at 520 nm can be extracted using the short circuit current and incident light power to be 0.85. Typical a-Si diode curves are presented in Figure 4.8.

Figure 4.8A compares the illuminated and dark performance on the same linear scale. The dark current is shown on a log scale in Figure 4.8B. The dark sweep is separated into a forward sweep and a reverse sweep to enable plotting of a log scale. The reverse sweep current is actually the absolute value of the dark current.

After the diode and TFT structures have been tested, the array is debonded. Due to the compressive stress of the i-Si there is still measurable curl as the array tries to roll up with the thin films facing outward as shown in Figure 4.9. When the i-Si film stress is -400 MPa or worse, the curl was significant enough to break the Tape Automated Bonding (TAB) seal between the back plane and the packaged driver assembly. Once the driver assembly was successfully connected, the MCI DRZ-Plus Tb doped $\text{Gd}_2\text{O}_2\text{S}$ scintillator was laminated to the top of the backplane, which was followed by final packaging (provided by PARC, Palo Alto Research Corp) to protect the board electronics from incident x-rays.

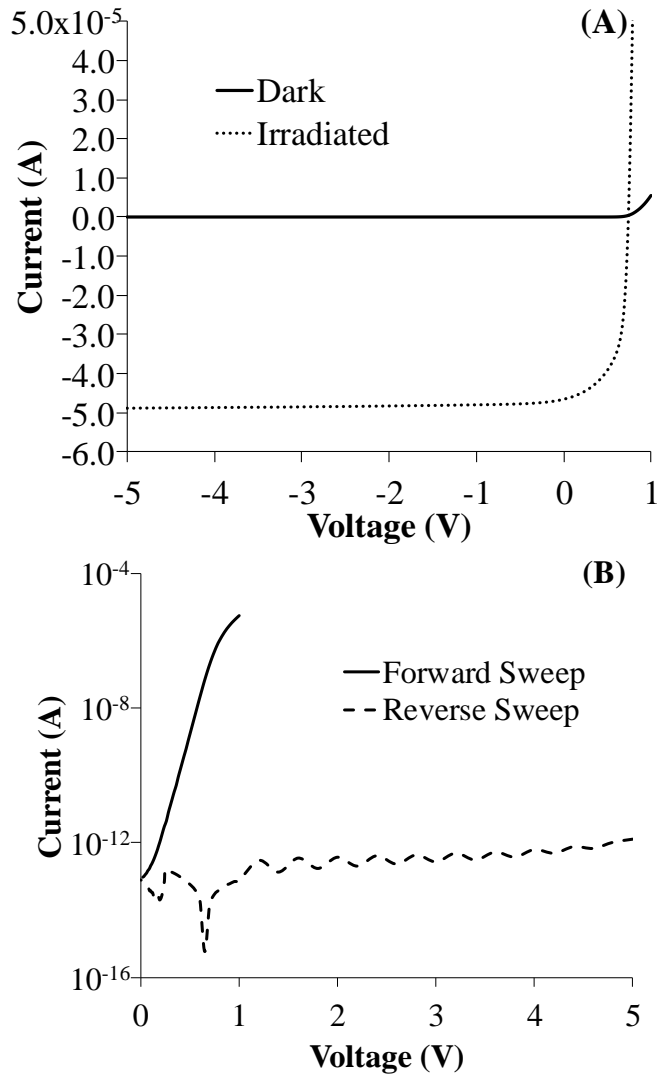


Figure 4.8. Typical a-Si PIN Diode Performance with Illuminated and Dark Performance Shown on the Same Linear Scale (A) and the Dark I-V Characteristics Shown on a Log Scale (B). The Forward and Reverse Sweep Are Separated Due to the Difficulties of Plotting Negative Numbers on a Log Scale.

Imaging examples for the 200 mm diagonal x-ray detectors are provided in Figure 4.10. Post image processing was used to optimize the contrast and despeckle. In addition, defective gate and scan lines were electronically interpolated; these are noticeable as dark

grey vertical lines that appear in both images in Figure 4.10. The lineouts and small speckling of open pixels are attributed to particulate defects and incomplete patterning of vias, respectively. The successful fabrication of the 200 mm diagonal array represents what we believe to be the world's largest flexible x-ray detector.

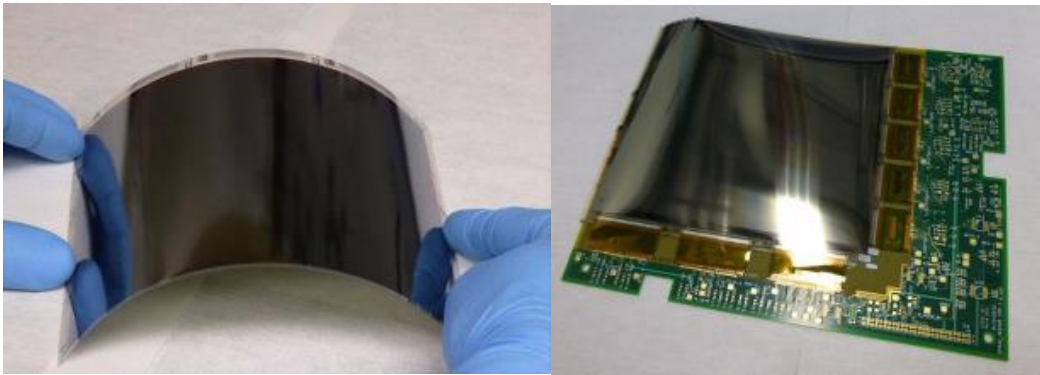


Figure 4.9. Debonded 200 mm Diagonal Flexible PIN Diode Array Prior to Assembly (Left) and after Driver Attach (Right).

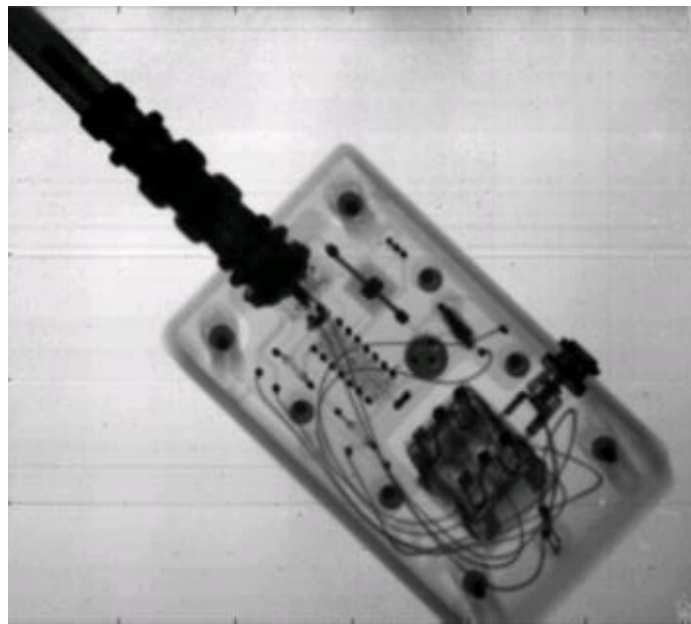


Figure 4.10. Imaging Example from a 7.9" 720x640 Array Fabricated on the Gen II Pilot Line at the Flexible Electronics and Display Center.

Conclusions

The results show that careful tuning of the a-Si stress combined with a flexible substrate technology compatible with thin film processing can enable the production of high quality a-Si PIN diode sensor arrays with manageable curl. The a-Si PIN diode sensors are not limited to x-ray detectors and can be outfitted to detect other radiation with an appropriate conversion layer, opening up a variety of security and diagnostic markets to flexible electronic technology.

CHAPTER 5 IMPROVEMENTS AND ALTERNATE PROCESSING TECHNIQUES FOR REDUCING THE INTRINSIC FILM STRESS OF FLEXIBLE AMORPHOUS SILICON PIN DIODE BASED X-RAY DETECTORS

Introduction and Current Approach

Flexible electronics are becoming more prevalent as previously developed flexible display technology is being implemented to produce a wide variety of devices (Smith, et al. 2014) including flexible x-ray detectors. Although the concept of a fully flexible x-ray detector can be appealing and may open digital radiography to new uses, the primary benefit of switching from conventional display glass to flexible substrates is the cost savings associated with the elimination of the significant ruggedization that must be incorporated to limit detector breakage (Marrs, et al. 2013).

With this goal in mind, active matrix TFT flexible display technology can be easily ported to digital x-ray detectors, which have a similar structure to LCD displays. However, one major difference is the presence of a photodiode connected in series with a thin film transistor at each pixel. The simplest approach is to pattern the n-Si layer of the photodiode at each pixel while leaving the i-Si, p-Si, and transparent conductor top metal contact continuous over the entire array.

One huge advantage of this full fill factor approach is that the entire pixel is covered by the i-Si absorption layer, thus eliminating any “dead” spots in the pixel where photon strikes will not be detected. This full fill factor approach also produces the smallest pixel size for a given set of design rules.

There are some significant drawbacks to the full fill factor design that are exacerbated by the use of PEN as a substrate. Since there is a large coefficient of thermal

expansion (CTE) mismatch between PEN and amorphous silicon (13 ppm/°C versus 3 ppm/°C), detectors fabricated with the full fill factor approach have a tendency to curl significantly after debonding the flexible substrate. In addition, the deposition process for the amorphous silicon diode layers takes place at 200°C, which is near the melting temperature of the PEN (240°C) and can take upwards of one hour to deposit the requisite 1.2 μm thick film. The extended exposure at the elevated temperature of the PECVD deposition risks embrittling the PEN and ruining the detector. In spite of these drawbacks, full fill factor x-ray detectors on PEN substrates have been successfully demonstrated by multiple groups. Previous results from the Flexible Electronics and Display Center are shared below in Figure 5.1a. However, the process is not without drawbacks as the i-Si deposition process must be tightly controlled as the risk of stress related failures is high if the intrinsic film stress of the i-Si layer decreases below approximately -100 MPa (compressive). An example of a stress related failure is shown in Figure 5.1b

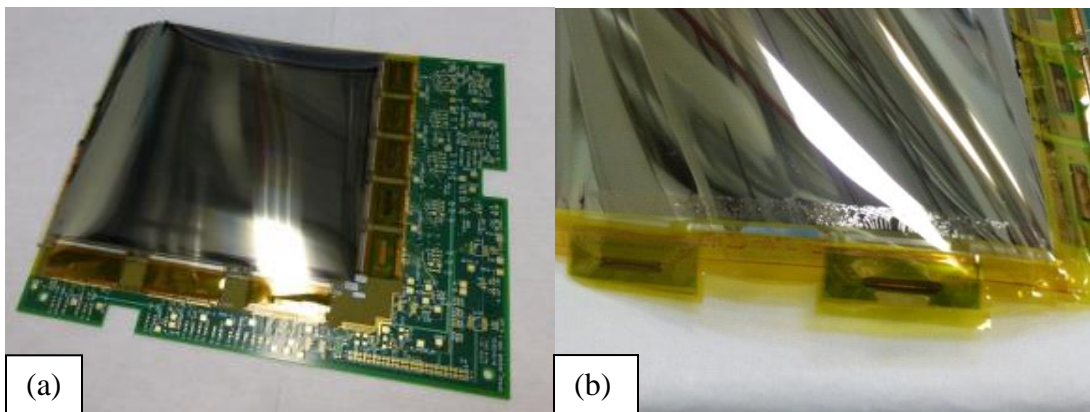


Figure 5.1: Full Fill Factor Digital X-Ray Detector Fabricated and Assembled at the Flexible Electronics and Display Center (a) and X-Ray Detector Backplane Showing Stress Related Failure Due to High Intrinsic Film Stress in the i-Si Layer (b).

Alternative Substrate Approach: Polyimide

One method for alleviating stress in the entire film stack is to use a flexible substrate whose thermal expansion coefficient is a closer match to thermal expansion coefficient of the deposited thin films. A class of flexible substrate materials that is receiving considerable attention because of their compatible thermal properties are polyimides. Polyimides are currently used in the EPLAR, SUFTLA, and FLEX UP processes briefly introduced in Chapter 1. The main advantages of polyimides over PEN as a substrate are that the coefficient of thermal expansion for polyimide is roughly 4 times smaller than PEN, while the safer operating temperature is roughly 200°C higher. A comparison of the thermal properties of HD Microsystems PI 2611 (HD Microsystems 2009), a polyimide, DuPont Teonex Q51 (Synflex 2013), and silicon (Petersen 1982, Virginia Semiconductor 2002) are shown below in Table 5.1.

Table 5.1: Comparison of Structural, Thermal, and Electrical Properties of Polyimide, PEN, and Silicon

	HD Microsystems PI 2611	DuPont Teonex Q51 PEN	Silicon	Units
Tensile Strength	350	274.6	7000	MPa
Glass Transition Temperature	360	121	-	°C
Continuous Operation Temperature	-	180	-	°C
Melting Temperature	620 (decomposes)	269	1415	°C
Coefficient of Thermal Expansion	3	13	2.6	ppm/°C
Dielectric Constant	2.9	3	11.9	

The increased operating temperature of the polyimide would allow for safe processing of a-Si at temperatures above 275°C, which is a typical deposition temperature for high quality TFT and PIN diode a-Si films, without risk of significant

thermal damage to the substrate. In addition, the coefficient of thermal expansion of the PI 2611 is within 0.4 ppm/°C of silicon, meaning that it is less likely that debonded polyimide substrates with a-Si depositions will curl on their own if the substrate is not significantly stretched during debond.

The curl of the polyimide substrate after debond depends on the formulation of the polyimide spin/spray casting solution and adhesion layer. Significant stress can be imparted on the polyimide if the peel strength is significantly above 80 g/inch, resulting in the elongation or stretching of the polyimide. The polyimide monomer formulation is a factor in the coefficient of thermal expansion for the final film. If the peel strength is too high or the coefficient of thermal expansion is significantly different from the thin films deposited, significant curl will be present in the debonded polyimide, rendering the flexible x-ray detector unusable. However, using HD microsystems 2600 series polyimide with an appropriate adhesion promoter at the edge of the rigid carrier substrate can yield a flexible substrate that is easily debonded post process and does not exhibit significant curl. The curl of the 2600 series polyimide is lower than PEN. A comparison of a debonded PEN x-ray detector, a debonded polyimide x-ray detector with large peel strength and debonded polyimide x-ray detector with appropriate peel strength and minimal thermal expansion coefficient mismatch is shown below in Figure 5.2.

Once the polyimide substrate is debonded, the user can be quite rough with the substrate and not be concerned with film cracking or peeling. One must be very cautious and slow while debonding the PEN as perturbations during the debond process can cause the inorganic PIN diode layers to buckle (Figure 5.3) under the sudden in change in applied peeling force as residual stress in the PEN is released.

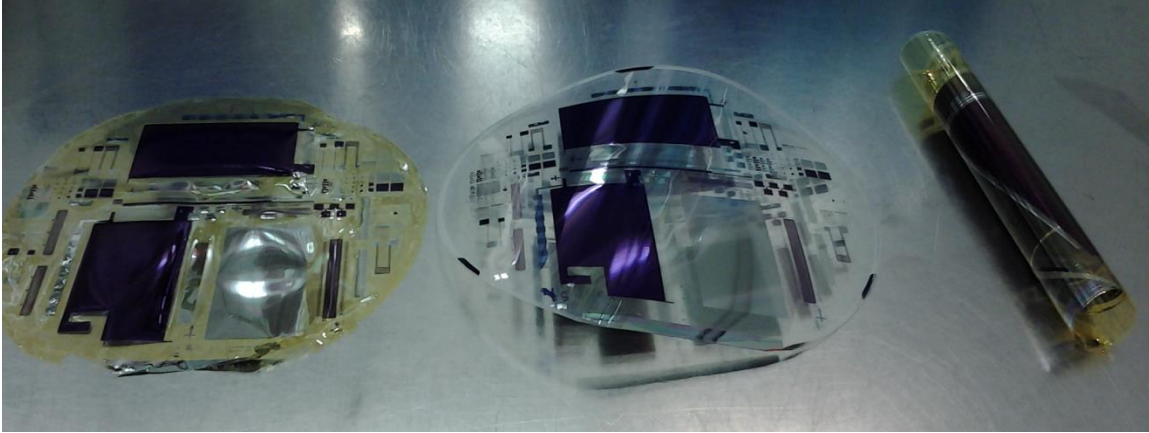


Figure 5.2: Curl Comparison of Low CTE Polyimide, PEN, and High CTE Polyimide Debonded

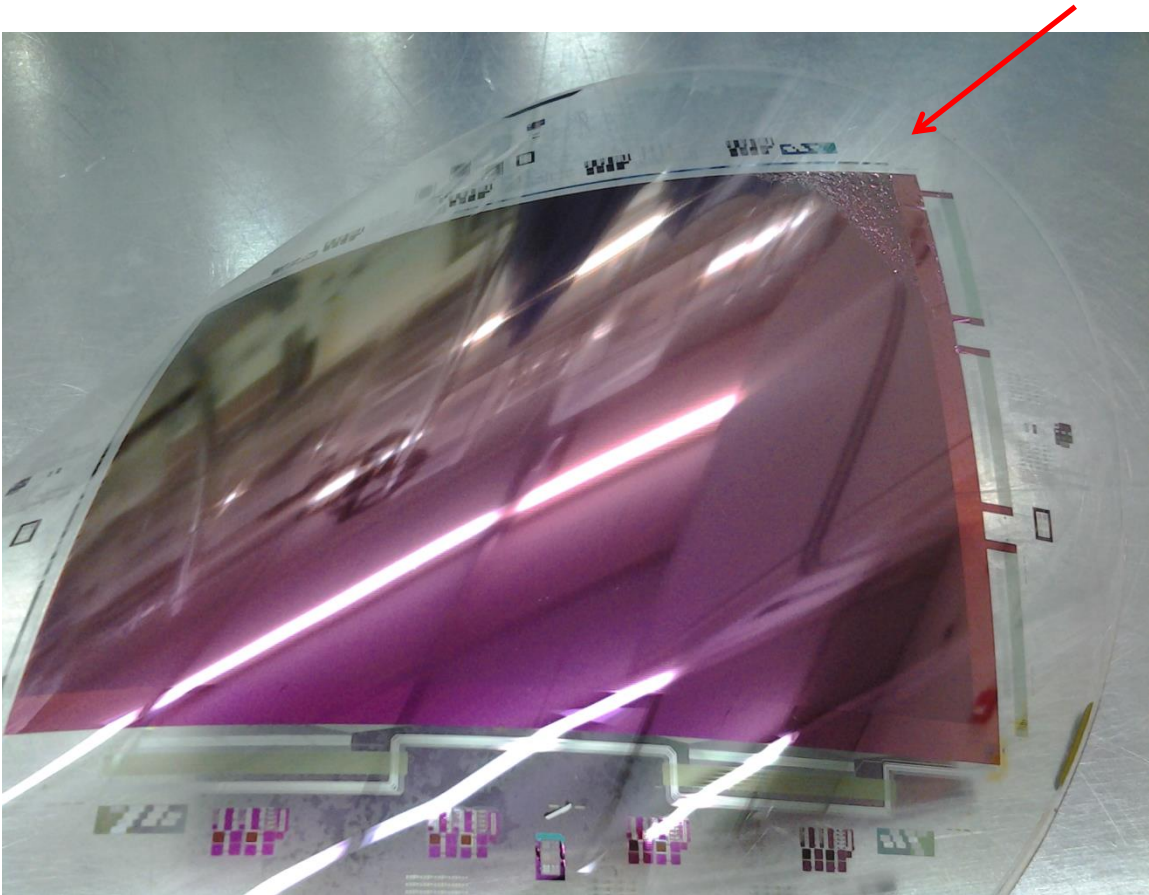


Figure 5.3: PIN Diode Layer Film Buckling Induced by Uneven Release of Stress in the Flexible PEN Substrate as a Result of Perturbations in the Debond Process

The maximum processing temperature of the TFT and PIN diode processing is 200°C, which is 20°C above the recommended continuous operation temperature but still 69°C below the melting temperature listed in Table 5.1. However, at 210°C and above, the PEN crystallizes, leading to significant shrinkage, and is prone to fracture during the debond process (Cygan, et al. 1993). Minor perturbations in the temperature of the TFT and PIN diode thin film deposition processes could significantly affect the structure of the PEN while it is still bonded potentially leading to film buckling during the debond process.

In addition to the reduced curl and the improved film adhesion post debond, another advantage of using polyimide over PEN is the significantly higher glass transition temperature of the polyimide (360°C vs 121°C, respectively). The higher glass transition temperature allows for a higher deposition temperature during the PECVD steps. The added degree of freedom allows for a higher quality finished as the higher deposition temperature can lead to a lower dark current, higher quantum efficiency, and higher fill factor for the PIN diode films.

Simply increasing the deposition temperature of the PIN diode films from 200°C to 250°C without making any other changes to the other deposition parameters results in a significant increase in the quantum efficiency at 520 nm of the photodiodes from 57.8% to 61.8% when using a green LED light source with measured irradiance of 100 W/m². The increased deposition temperature of the PIN diode layers results in a denser, higher quality film that has fewer trap sites available to grab photogenerated electrons and holes before leaving the diode.

Alternative PIN Diode Structure Approach: Pixelated Diode

The current full fill factor design places the PIN diode over top of the TFT and also uses an ITO common electrode for the V_{bias} connection on the p-doped side of the PIN diode. The i-Si, p-Si, and ITO blanket the entire x-ray detector array and are etched outside the array in the field and over the driver connections. A cross-sectional schematic illustrates the basic pixel design for this approach in Figure 5.4. The red box highlights the PIN diode layers.

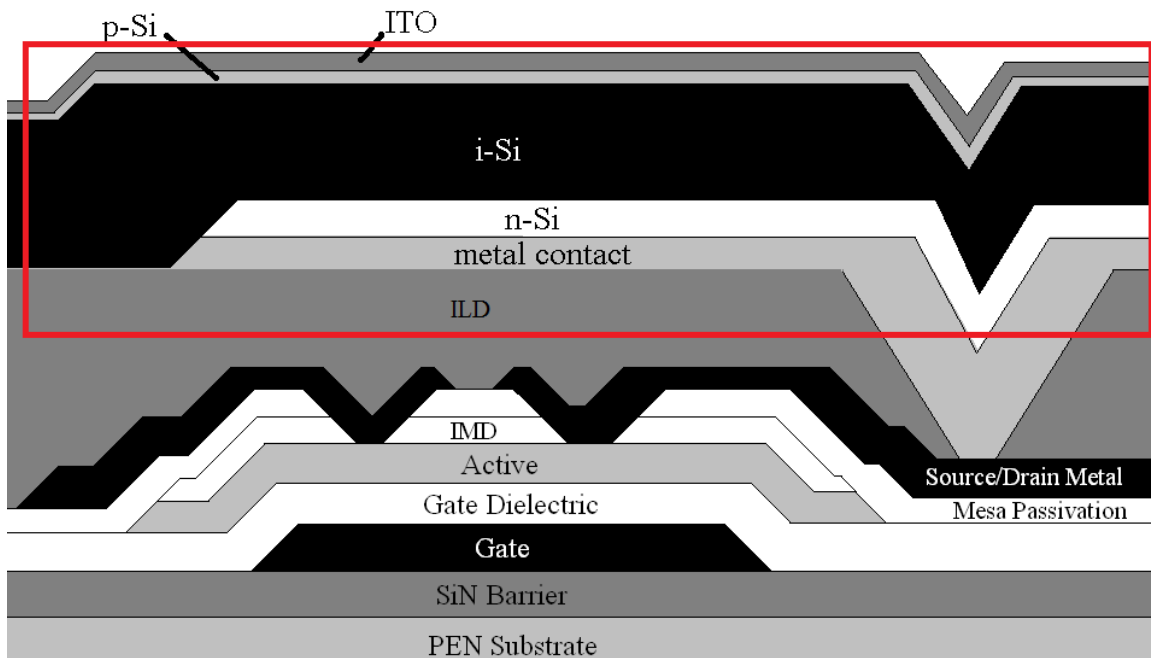


Figure 5.4: Full Fill Factor PIN Photodiode Connected in Series to a TFT

Although the full fill factor design does produce a smaller area, higher resolution pixel when subjected to the same design rules as alternative structures (Theil, et al. 2002), there are some potential disadvantages as well. For example, since the i-Si is blanket deposited across the array, it imparts more stress on the substrate system than if the i-Si layer were patterned. In addition, there is also potential the potential for crosstalk between the arrays as photons absorbed over a certain pixel could instead be read out by a

neighboring pixel because the i-Si film is continuous over the entire array. Pixelating the photodiode requires the V_{bias} connection to the p-doped side of the diode to be made using a subsequent metal deposition step. The readout lines can also be moved to this subsequent deposition step and then brought down to the TFT through a via at each pixel. This modification enables the maximum separation between the gate lines and the readout lines, which reduces the parasitic capacitance (noise) between the two. A cross-sectional schematic illustrates the basic pixel design for this approach in Figure 5.5. The red box highlights the PIN diode layers.

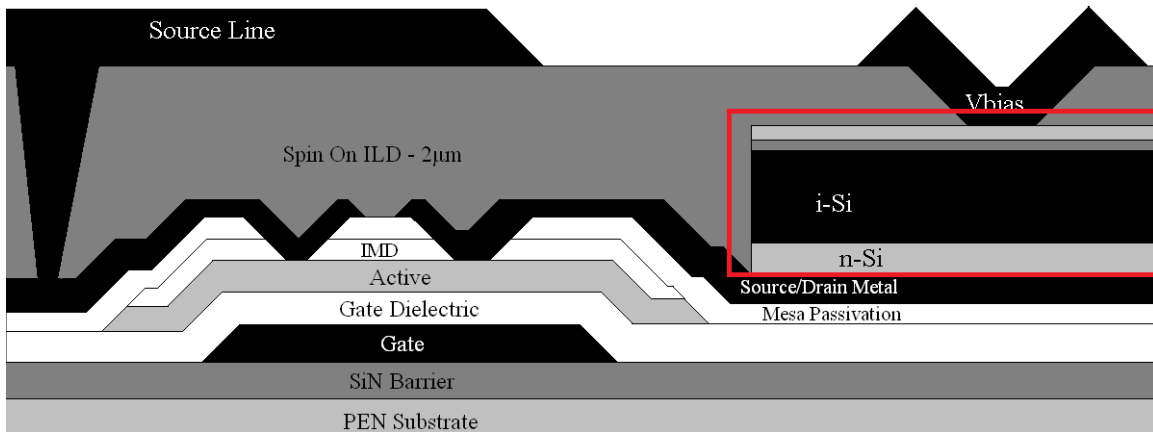


Figure 5.5: Patterned PIN Photodiode Connected in Series to a TFT

The patterned PIN diode structure replaces the ITO V_{bias} connection with any opaque metal of choice. If aluminum is used, the resistivity difference between aluminum and ITO is over a factor of 100 ($4.1 \mu\Omega\text{-cm}$ vs $528 \mu\Omega\text{-cm}$), which should provide an immediate benefit by reducing the series resistance in the device. The ITO thickness and thus the sheet resistance is governed by optical constraints as well as electrical constraints as the ITO layer needs to be an anti-reflection coating at the target wavelength for detection of incident light. In the case of a digital x-ray detector using a CsI scintillator, the target light wavelength for detection is the peak emission wavelength of the

scintillator (roughly 525 nm). The ideal ITO thickness to produce minimum reflection at this wavelength is approximately 65 nm thick as calculated from Snell's Law. However, the V_{bias} connection in the pixelated PIN diode structure depicted in Figure 5.5 does not have such optical constraints because the layer is so thick that it is sufficiently opaque to most visible light and only covers a small portion of the photodiode. This feature allows the separate control of the electrical and optical properties of the V_{bias} connection.

By using aluminum as the V_{bias} connection over ITO, the series resistance can be significantly reduced while still maintaining the optical properties necessary to maximize photon absorption in the photodiode. Series resistance is a parasitic, power consuming parameter whose effect on the diode performance is illustrated by Equation 5.1, which is a modification to the ideal diode equation (Equation 4.1):

$$I_D = I_S \left(e^{\frac{q(V_D - I_D R_s)}{nkT}} - 1 \right) \quad 5.1$$

where I_D is the diode current, I_S is the reverse saturation current, q is the charge of an electron, V_D is the voltage applied across the diode, R_s is the series resistance, n is the diode ideality factor, k is Boltzmann's constant, and T is the temperature. The main contribution to series resistance comes from the diode contact resistance, bulk resistance of the diode layers, and the sheet resistance of the top metal layer (Dadu, Kapoor and Tripathi 2002). The deleterious effects of series resistance are most noticeable at voltages near the near the open circuit voltage of the photodiode (Honsberg and Bowden 2015) as a deviation in the slope of the I-V curve from the vertical affecting the fill factor, the

short circuit current, and quantum efficiency in extreme cases (Dadu, Kapoor and Tripathi 2002).

Comparing 1 mm² diodes fabricated with a blanket PIN diode structure with ITO top contact and no passivation (as shown in Figure 5.4) with diodes that are passivated and utilizing a metal strap as the top V_{bias} contact (as shown in Figure 5.5) shows that dark characteristics generally favor the pixelated PIN diode both under forward bias and reverse bias (Figure 5.6A). The improvement under forward bias is likely attributable to the reduced series resistance, which begins to dominate the I-V characteristic as the voltage increases above 0.5 V. The primary advantage to decreasing the series resistance is to reduce the image lag. A lower resistance allows charge to be drained faster enabling faster refresh rates.

Under reverse bias operation, under which a photodiode will spend most of its operating lifetime, the leakage current for the pixelated diode is lower than the blanket coated diode and stays relatively flat with increasingly negative applied voltage (Figure 5.6B).

The passivation may be responsible for the lower dark current as changing the passivation seems to affect the final dark current characteristics. For example, when no passivation is used, the diodes are so leaky that it is difficult to consider them “diodes”. In the example present above, the passivation layer is actually a two layer stack featuring 2.0 μm of spin on SU-8 polymer and 300 nm of PECVD grown SiN. If only the SU-8 polymer is applied as the passivation layer, the initial dark current is greatly improved. However, the dark current begins to degrade during continuous operation under reverse bias as shown in Figure 5.7.

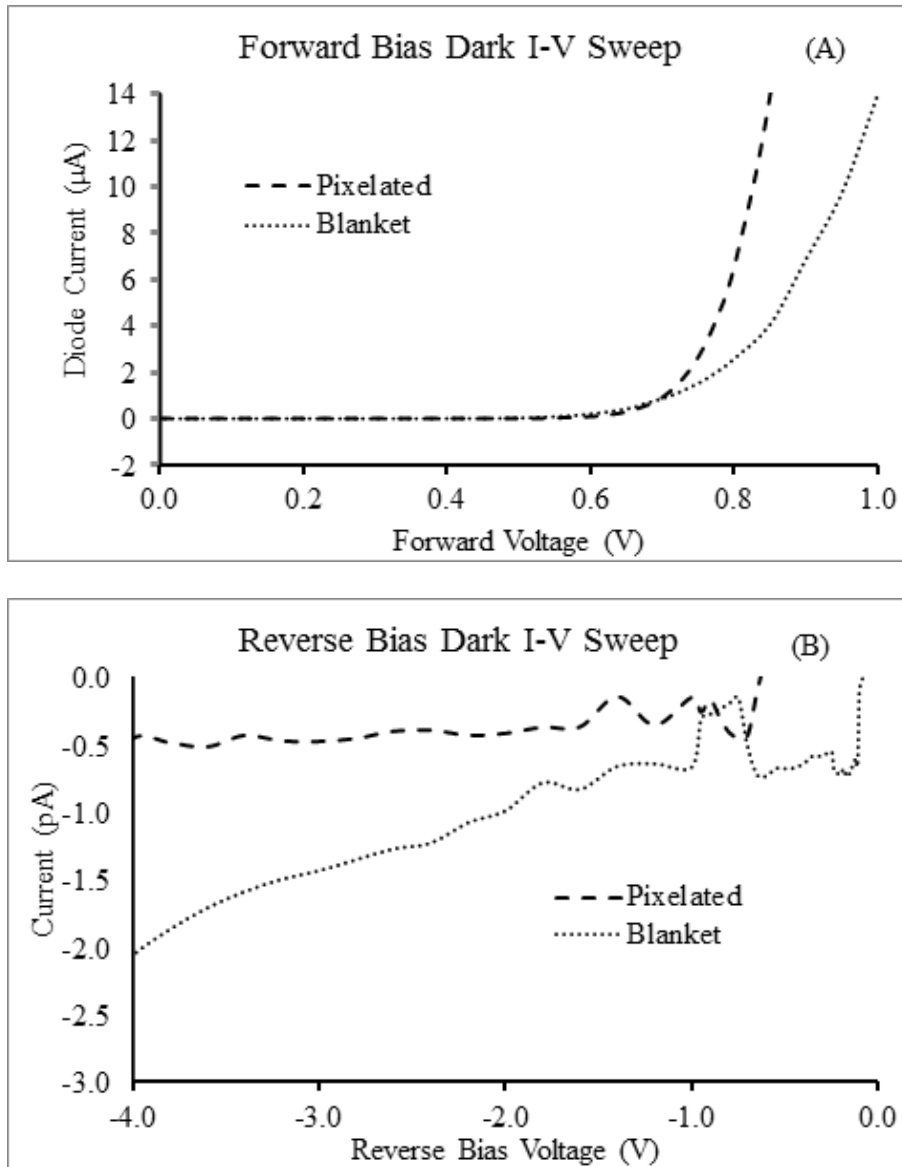


Figure 5.6: Forward (A) and Reverse (B) Dark I-V Sweep Comparison between Blanket and Pixelated PIN Diodes

If only SiN is used as the passivation material, the initial dark current is larger than the initial dark current for SU-8 coated diodes. However, the dark current is relatively stable versus time as shown in Figure 5.7. The degradation patterns suggest that the PECVD SiN film deposition process may be damaging the exposed PIN diode layers potentially increasing surface recombination/generation while the SU-8 by itself may be

an inadequate atmospheric contaminant barrier. The best results are observed when the SU-8 is coated first and is followed by a SiN deposition.

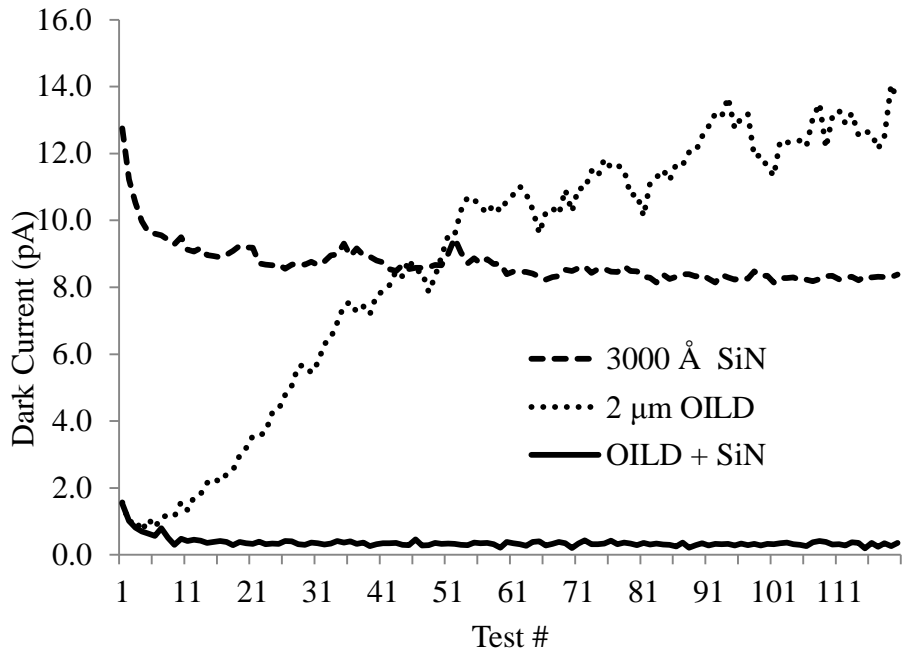


Figure 5.7: Change in Dark Current vs. Time for Three Different Photodiode Passivation Schemes

The effect of surface generation/recombination can be verified by looking at the performance of photodiodes with the same detection area (i.e., the surface area of the side of the diode facing the incident light) but with a different perimeter. Square diodes have the minimum perimeter possible for a given area and thus have the smallest surface area of i-Si sidewalls exposed. Diodes with a rectangular shape have a larger area for potential surface recombination and generation to occur and thus should have a higher dark current than a square diode. To illustrate this point, two different diode geometries were investigated. Diode A has a 1 mm x 1 mm square cross-section exposed to the incident

light while Diode B has a 2 mm x 0.5 mm rectangular cross-section exposed to the incident light. Both diodes have the same capture area (1 mm²).

A T-Test reveals a small, but statistically significant difference in the logarithm of the dark current with the rectangular diodes having greater than 2 times the dark current of the square diodes.

The effect of the diode edge can also be illustrated by testing a structure where there is a diode completely surrounded by another diode as a protective backside guard ring as shown in Figure 5.8. The backside guard ring reduces the electric field at the edge of the device and prevents the depletion region from reaching the edge of the diode thus mitigating surface leakages and enabling the capture of carriers generated outside of the active area (Nam, et al. 2006). The beneficial effects of the guard ring can be enhanced by grounding the n side of the diode as opposed to leaving it float.

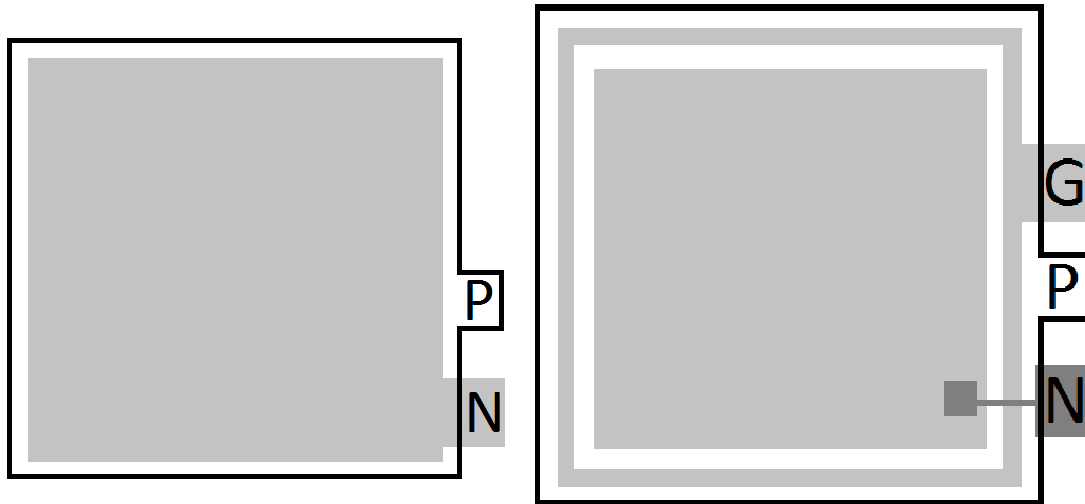


Figure 5.8: Top Down Drawing Comparing an Unguarded PIN Diode with Only N and P Terminals (Left) and Guarded PIN Diode Structure with Added Guard Ring (G) in Addition to the N and P Terminals (Right).

Comparing dark sweeps from diodes with and without guard rings shows that the devices with the guard ring demonstrate a substantial reduction in the dark current (Figure 5.9). In addition, devices with the guard ring are less sensitive to environmental conditions, specifically air temperature and humidity.

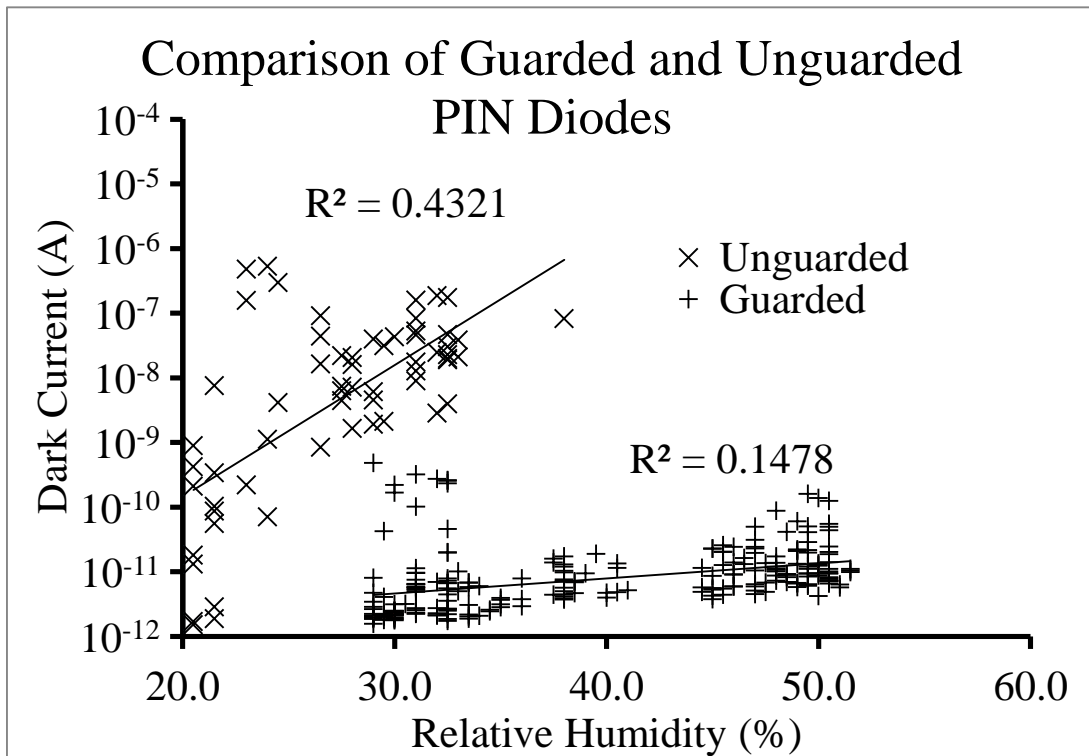


Figure 5.9: Comparison of the Dark Current vs. Relative Humidity for Guarded and Unguarded PIN Diodes.

Another advantage of the pixelated PIN diode is that the i-Si absorbing layer is no longer continuous over the entire array, making it extremely difficult for photons absorbed over one pixel to be read out by a neighboring pixel. This reduction in cross-talk between neighboring pixels results in increased contrast and improved resolution. Figure 5.10 shows a comparison between an array with a blanket i-Si layer and a pixel patterned i-Si when exposed to the same irradiance with the same gate on time for the

TFT array. The pixel patterned sample demonstrates a higher contrast indicating a lower detection threshold.

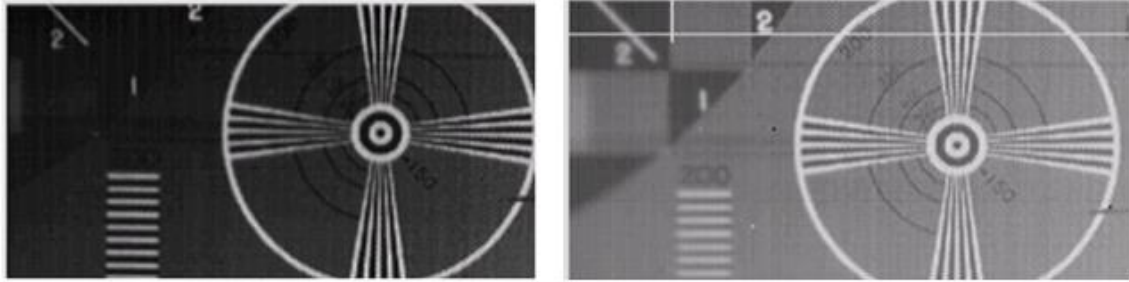


Figure 5.10: Full Fill Factor Blanket i-Si Photodiode Array (Left) Compared to Pixel Pattern Photodiode Array (Right)

Alternative Diode Approach: Organic Photodiodes

An alternate approach to reducing the stress of the intrinsic silicon is to remove the high stress a-Si layers from the film stack and replace it with a more flexible photodiode option. Digital x-ray detectors usually come in one of two flavors: indirect conversion, where an x-ray phosphor scintillator film captures the x-rays and converts them to visible light that is captured by an a-Si photodiode, and direct conversion, where the x-ray is absorbed and converted into an electrical signal in a photoconductor such as amorphous selenium (Kuo, et al. 2014). Amorphous selenium must be 100-200 μm thick in order to obtain a reasonably high quantum efficiency (98%) to be effective as a detector and to adequately protect the underlying thin film transistor layers from the deleterious effects of ionizing radiation. If flexible plastic substrates are to be used, then the selenium must be evaporated, as any known CVD techniques would take place well above the melting temperature of any plastic flexible substrate.

Evaporating on large area substrates typical of x-ray detectors is not ideal due to line of sight issues, but it is not impossible either. However, the selenium film is usually deposited as a blanket film, and the film thickness can be equal to or several times greater than the substrate thickness when a flexible substrate is employed. Given that selenium is very brittle, extreme care must be taken to avoid flexing the detector once the selenium has been deposited (Kuo, et al. 2014).

Although selenium can be deposited on a flexible substrate, it is not a major upgrade with respect to breakage over glass substrates since the selenium can be cracked and shattered on a flexible substrate just like the glass substrates in a digital x-ray detector. An intriguing alternative flexible solution lies in organic photodiodes. Organic photodiodes constitute a class of materials where the photodetector is produced from organic compounds.

Organic photodiodes are usually fabricated using either small molecule evaporation or polymer solution processing to form the photodetector layer. Carrier blocking and/or transport layers can be deposited between the photodetector material and one or both of the metal electrodes, which are constructed out of conductive materials with dissimilar work functions. Both techniques have their drawbacks as solution processing techniques can attack previously deposited organic layers if the solvents are not chosen carefully, while vapor deposition relies on line of sight between source and substrate, which can cause thickness and/or doping variation challenges across a deposited film. Vapor deposition equipment is also significantly more expensive in most cases due to the need for high vacuum. This work focuses on solution processing.

Solution processing of photodiodes usually involves the dissolution of an electron donor and electron acceptor in a solvent in which both the acceptor and donor have reasonably high solubility (Gelinck, et al. 2015). The acceptor and donor material also have limited, but greater than zero, solubility in each other, allowing for the creation of a bulk heterojunction diode where the donor and acceptor are intermixed with each other, greatly increasing the surface area of donor/acceptor boundary relative to a planar structure. The intermixing of the donor and acceptor are crucial to the operation of an organic photodiode as the diffusion length of an exciton, the product of the absorption of a photon in an organic photodiode, is on the order of 10 nm. With respect to the current state of the art organic photodiodes, most visible light is absorbed by the electron donor, usually a polymer (polythiophenes are common) with pi conjugation such as Poly(3-hexylthiophene-2,5-diyl) (P3HT), where delocalized pi electrons can hop along the polymer chains until it reaches an interface where an acceptor, such as a fullerene derivative like (6,6)-phenyl C61 butyric acid methyl ester (PCBM) steals the electron. The exciton has enough energy from the photon absorption to help it break free from the donor material and be swept up by the acceptor material, allowing the electron to complete its journey to the positively biased higher work function electrode. The newly created hole in the donor material is filled by an electron from the negatively biased lower work function electrode.

The main advantages for organic photodiodes over other competing detector technologies with respect to flexible electronics is the low stress, low temperature deposition process, the resultant inherent flexibility of the material once it is deposited in comparison to inorganic detector alternatives, and the low cost associated with solution

processing. Additional cost savings are realized when solution processing by eliminating at least two deposition/photolithography/etch processing cycles. Further cost reductions could be realized by purchasing low cost TFT LCD display panels from Asia and solution processing organic photodiodes on top of the TFT arrays, thus eliminating the need to purchase expensive vacuum or photolithography equipment.

The potential advantages for organic photodiodes are currently offset by some critical issues specifically related to the long term stability of the detectors and the significantly lower quantum efficiency of the current state of the art in comparison to inorganic photodiode based detectors.

To better illustrate the issues and benefits of organic photodiodes over their inorganic brethren, photodiode test structures were fabricated to compare the performance of P3HT/PCBM based organic photodiodes and the current state of the art flexible amorphous silicon photodiodes. The basic structure of the organic photodiode detector is very similar to the structure of the amorphous silicon photodiode based detectors presented in Figure 4.1 with the PIN layers replaced by a bulk heterojunction photodiode and the two electrode metals changed as shown in Figure 5.11.

The organic photodiodes were inkjet printed from a 1:0.75:66.8:31.45 weight ratio mixture of P3HT:PCBM:o-dichlorobenzene:mesitylene first used by Liliu (Lilliu, et al. 2011). The dichlorobenzene/mesitylene based solvent can be tailored to minimize the surface roughness. Diode performance was characterized utilizing a Micro Manipulator Model 4060 probe station fitted with Keithley 4200 Semiconductor Characterization System. The diodes were swept from -1 V to +1 V. The absolute value of the current was taken to enable semilog plotting of the data. The reverse sweep data shows that the

organic photodiodes demonstrate a significantly larger dark leakage current than the amorphous silicon based photodiodes. In addition, the dark current continues to increase with repeated testing as shown in Figure 5.12, while the amorphous silicon photodiode is generally stable with repeated tests.

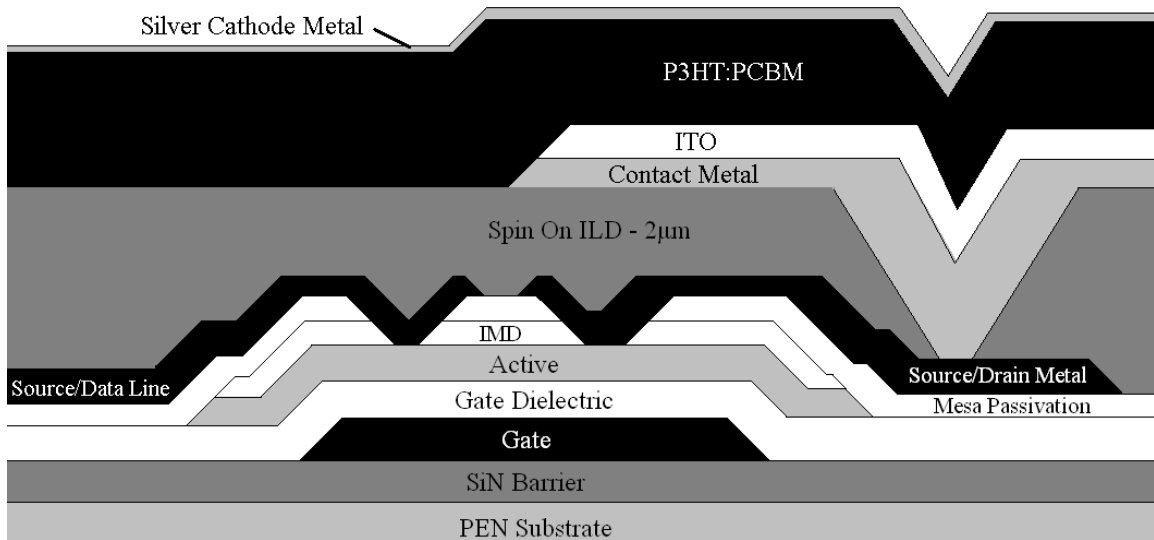


Figure 5.11: Organic Photodiode Pixel Structure

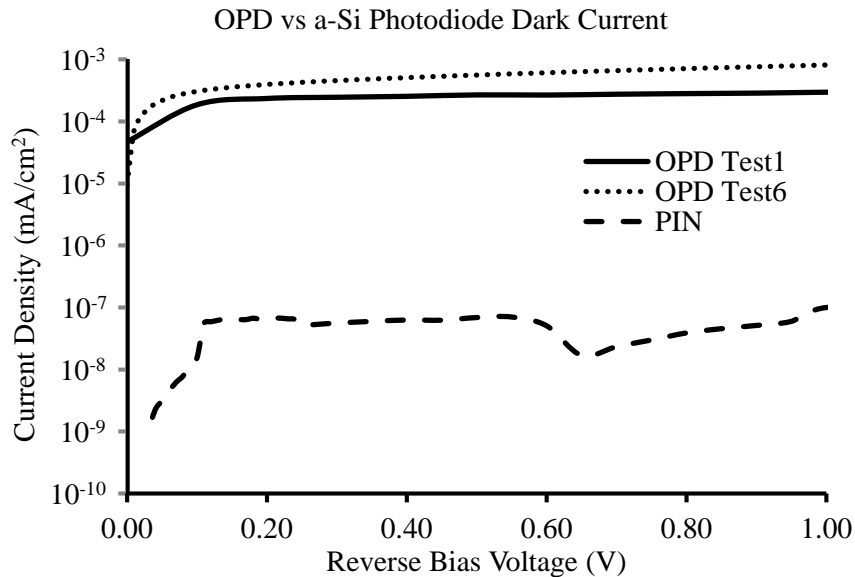


Figure 5.12: Comparison of Dark Performance of Organic Photodiodes and a-Si PIN Photodiodes. The First and Sixth Curve Trace for the Organic Photodiode are Shown.

Tests under 1 sol of irradiation reveal that the organic photodiodes are significantly less efficient (less than 1% efficient) than inorganic diodes and also appear to have issues with series resistance and shunts as shown in Figure 5.13 based on the slope of the I-V curve at the x and y intercept respectively (Zhou, et al. 2012). Although better Organic photodiode performance is demonstrated in the literature (Eoma, et al. 2010), even those “hero” results still fall short of the performance and efficiency of a-Si PIN photodiodes.

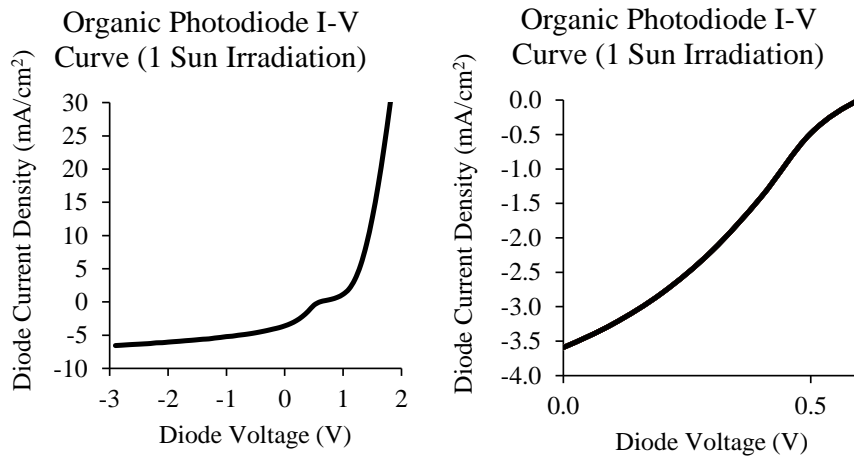


Figure 5.13: Organic Photodiode I-V Curve when Exposed to 1 Sun Irradiance.

In spite of the relatively high dark current and low efficiency, x-ray detectors with organic photodiodes were fabricated and tested. Unfortunately, the diode leakage was too significant for the tester and no satisfactory imaging was possible. In order to achieve adequate signal to noise, the leakage must decrease by a factor of 10-50 times lower than the current leakage level based on experience with a-Si PIN photodiodes.

Lowering the dark current was possible using slot die coating in place of inkjet coating of the same P3HT:PCBM donor: acceptor combination. The quantum efficiency of the OPD was greatly improved over the FEDC diodes, but still 20-25% less than the

base a-Si photodiodes. The dark current was sufficiently low to allow for successful imaging.

Although initial imaging proved successful, the detectors appear to have a shelf life issue as significant dead spots begin to appear in the array after it had been left in a cleanroom environment for seven months (Figure 5.14). The degradation pattern is reminiscent of the degradation observed in OLEDs, where the primary issue is the oxidation of the cathode metal placing a large series resistance in the path of the diode current that usually has a bias toward the edge of the array. The degradation under atmospheric conditions means that a moisture barrier encapsulant must be used to preserve the integrity of the diode. Unfortunately, this requirement puts another layer in the path of the light on its way to the diode.

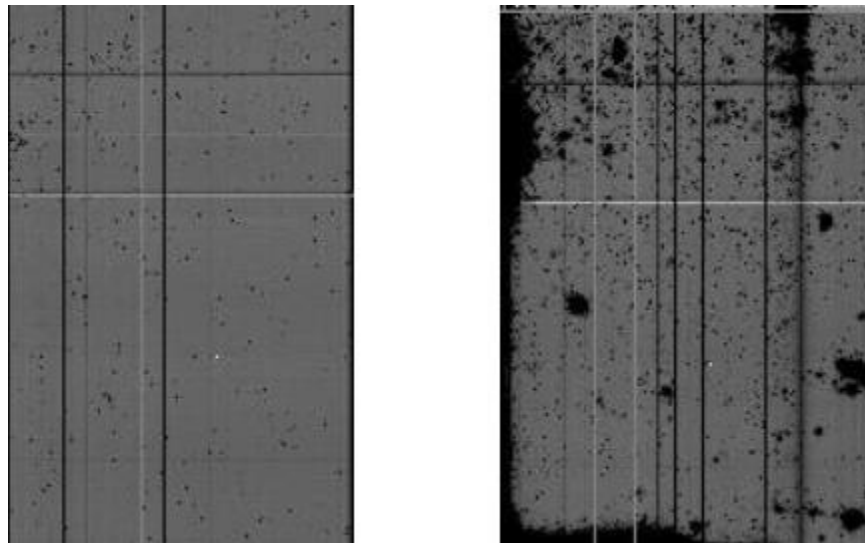


Figure 5.14: Initial Detector Background Image (Left) and After 7 Months of Storage in Cleanroom (Right). Dark Spots are considered to be Failed Pixels.

Performance of the organic photodiodes continues to improve, but may never equal the performance of a-Si because of the added issue of exciton lifetime, the

degradation under atmospheric conditions of the diode (specifically the cathode), and the extra layers (encapsulation, metallic cathode) placed in the path of the light source.

Conclusions

Three different approaches were evaluated to replace the current full fill factor a-Si photodiode approach with a process that is more robust with respect to flexing and bending of the substrate. All three approaches showed no instances of cracking and delaminating of the diode material under the normal flexure that occurs during the debond process and during the driver attach process. In addition, the polyimide substrate and pixelated diode processes also provide additional value add to the detector performance by allowing for increased processing temperature and reduced pixel to pixel leakage. The organic photodiode process does not offer any significant electrical improvements and in most cases, when compared to a-Si PIN diodes, demonstrates significant deleterious side effects including reduced quantum efficiency and poorer shelf life. The cost benefit of using solution processing may allow detector manufacturers to overlook, but not necessarily overcome, some of the deleterious performance issues.

CHAPTER 6 CONCLUSIONS AND FUTURE WORK

Conclusions

Flexible OLED displays based on mixed oxide TFTs have been successfully fabricated on PEN substrates. These TFTs were processed at a maximum temperature of 200 °C and have a saturation mobility of up to 18 cm²/V-s.

The second chapter established key processing breakthroughs in establishing a reasonable process baseline. Some of these notable process breakthroughs include the reduction of the gate etch sidewall angle, the establishment of SiO₂ gate dielectric of choice, the optimization of the active layer deposition by adjusting the process parameters, the selection of a dry etch process over a wet etch for improved step coverage of the active layer, exploration and selection of various source/drain metallurgy, establishment of a planarizing ILD process to enable high density top emission OLED displays, and migration of the process to flexible substrates.

The third chapter established a novel structure for high performance and improved stability TFTs based upon a dual active layer architecture. Devices with this dual active layer exhibit improved performance and stability under gate bias stress when compared to their single layer counterparts. The film properties of the first layer in contact with the gate dielectric are critical in determining the initial saturation mobility and threshold voltage, while the properties of the second layer in the active stack appear to control the threshold voltage stability. By judiciously selecting the components of the two active layers, it is possible to achieve both high performance and good stability that cannot be easily obtained with a single layer device without high temperature annealing. The procedures used in the fabrication of these devices are extendable to a production

process, in particular for manufacturing on flexible substrates where high temperature anneals are not possible.

The fourth chapter expanded the scope of flexible displays into flexible electronic devices, specifically digital x-ray detectors. The process challenges of incorporating the high stress a-Si PIN diode as well as the viability, stability, and radiation hardness of IGZO TFT based x-ray detector were explored. Flexible, passive pixel IGZO backed x-ray detectors appear to be a viable alternative to conventional glass based digital x-ray detectors.

The fifth chapter demonstrated process and structural improvements to the x-ray detector process introduced in Chapter 4 to improve the robustness of the detector with respect to flexure. Using a higher melting temperature substrate such as polyimide over PEN allows for high processing temperatures during some of the crucial TFT and diode processing steps provide an extra degree of freedom to improve the performance of the a-Si based photodiodes while virtually eliminating any issues with flexure during normal debond and driver attach operations. Choosing to pixelate the photodiode does significantly reduce the aperture ratio but does greatly reduce the diode leakage by reducing edge initiated leakage paths and crosstalk between pixels by placing breaks in the i-Si capture layer. Organic photodiodes are desirable to manufacturers as a low cost replacement to a-Si photodiodes. However, the performance of the photodiodes still significantly trails the performance of a-Si photodiodes with respect to leakage, quantum efficiency, and shelf life.

Future Work

There is still much to research with respect to mixed oxide TFTs. Mixed oxide devices have shown instability with respect to irradiation in the visible green and lower wavelengths. The instability has been attributed to oxygen vacancy formation and has been suppressed but not completely eliminated in literature.

The mixed oxide deposition process is crucial to the performance of the TFT. Other techniques for depositing the mixed oxide could be explored including solution processing and RF sputtering. Processing on flexible substrates continues to be a challenge due to the temperature constraints of the substrate limiting the maximum IGZO anneal temperature.

Although curved television displays have been fabricated up to 55" on the diagonal, truly flexible large area displays have not made it to the marketplace yet. At the FEDC, we have demonstrated the largest flexible OLED display in the world at 14.7" along the diagonal. However, the defectivity evident in these prototype display show that there is still much work to be done before large area flexible OLED displays hit the market.

A quicker path to bringing flexible, robust, low cost electronic devices to the market might be to pursue other electronic device technologies that are more forgiving to defects. One example demonstrated by the FEDC are flexible x-ray detectors. Defective lines can be interpolated out of industrial x-ray detectors and have fewer electronic components (transistors, capacitors, diodes) per pixel than an OLED display.

Organic photodiodes are a potential cost effective and more flexible option as the detector layer in digital x-ray detectors. However, electrical test results for organic are

poor in comparison to a-Si PIN diodes and need to be improved significantly before being incorporated in digital x-ray detectors.

Irradiation Bias Stability

One fundamental issue with mixed oxide semiconductors that has recently been discussed in the literature is the light stability of mixed oxide TFTs during operation (Ghaffarzadeh, et al. 2010, Fung, et al. 2008, Yao, et al. 2011). The optical band gap of mixed oxide semiconductors typically falls between 3.0 and 3.3 eV, but can demonstrate absorption of light down to 2.6 eV (yellow) depending on the quality of the oxide film. When exposed to light, mixed oxide TFTs demonstrate a sizable negative shift in the threshold voltage that depends on the intensity and wavelength of the radiation. As the intensity increases and the wavelength decreases, the threshold voltage shift becomes increasingly negative. The decrease in the threshold voltage is attributed to the formation of oxygen vacancies in the active layer. An example for IGZO could be expressed by the following chemical reaction (Yao, et al. 2011):



This light instability is a major issue for displays that generate their own light (OLED) or allow light to pass through the display (LCD). Sensitivity to green and blue light would not be acceptable as the display would quickly fail.

A total of 28 IGZO devices fabricated using the dual layer process presented in Chapter 3 were subject to UV irradiation in a Dymax flood exposure unit with lamp intensity of 75 mW/cm² at primary lamp wavelength of 365 nm. Each group of 28 devices was subject to varying intervals (10s, 100s, 1000s, and 10000s) of irradiation

under the UV lamp. The wafers were then tested using the probe setup described in Chapters 2 and 3 with approximately 10 minutes of delay in between the irradiation and the TFT characterization. The results were tabulated and compared with the initial TFT measurements prior to any exposure. Figure 6.1 shows that saturation mobility increases and negative threshold voltage shifts increase with increasing UV exposure; these results are consistent with the literature.

The results presented by Yao (Yao, et al. 2011), indicate that the original oxygen content in the film is a strong factor in determining the magnitude of the V_T shift. The reaction mechanism presented suggests that it may be possible to stress mixed oxide devices in process to improve the device performance as well as the UV light stress stability.

The effect of in process irradiation could be explored by exposing wafers to a specific dosage based on the results from Figure 6.1 at various steps in the process. For example, if oxygen vacancy generation is occurring as a result of UV irradiation, then it may be possible to boost the performance by exposing the wafers to UV irradiation after the deposition of the active layer but prior to the passivation deposition.

UV irradiation after the active layer deposition may generate too many vacancies, so the UV treatment should be applied between different steps after the active layer passivation has been deposited. The UV irradiation could be conveniently applied by a Dymax flood exposure unit.

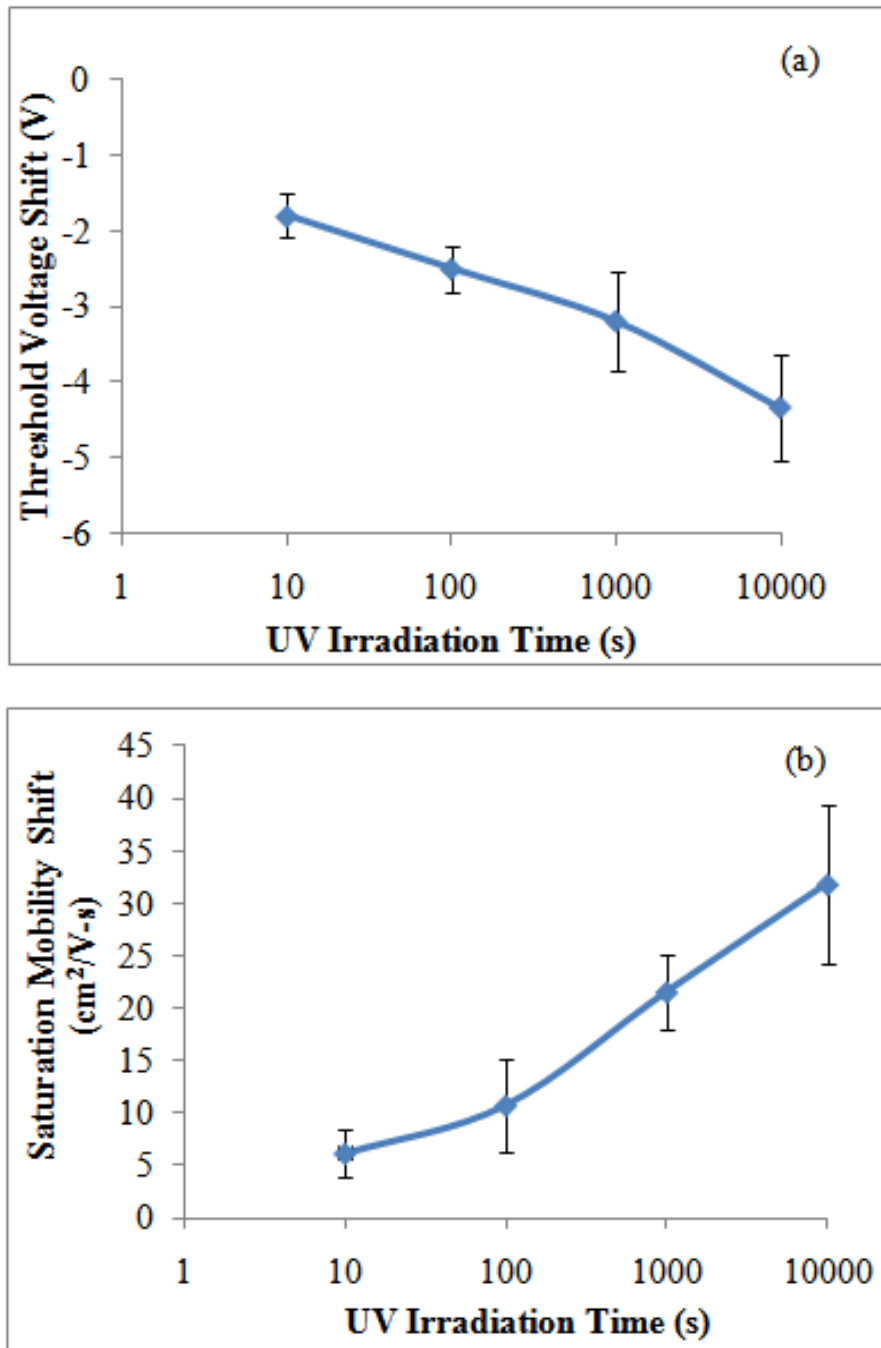


Figure 6.1: Threshold Voltage Shift (a) and Saturation Mobility Shift (b) as a Function of UV Irradiation Time.

It is also important to understand any potential recovery mechanisms if they exist. It would be an unfair comparison if only initial performance of the UV treated TFTs was compared with untreated TFTs. The potential gains of the UV treatment are not useful unless the gains are relatively permanent. Therefore the recovery time of the devices should be determined by storing UV treated wafers in the dark and recharacterizing the TFT performance at regular intervals. If the recovery process is slow (i.e. longer than 2-3 weeks), then it may be possible to accelerate the recovery by heating the devices. Since the primary defects created during UV exposure of mixed oxide semiconductors are oxygen vacancies, studying the recovery characteristics at different temperatures could allow for the extraction of the activation energy required to eliminate oxygen vacancies.

Organic Photodiodes

While digital x-ray detectors are easier to yield than OLED displays, they present their own unique challenges with respect to incorporating a diode into the process. The current best practices flexible x-ray detectors use a-Si PIN photodiodes. Unfortunately, the thickness of the intrinsic a-Si layer is on the order of 1.2 to 1.5 μm to insure the complete absorption of the incident light transmitted from the back of the scintillator and to lower the electric field which helps reduce the dark current.

Although several techniques were presented that mitigate issues with respect to the intrinsic film stress of the a-Si, the most cost effective path may be to completely replace the a-Si photodiode with an organic photodiode. Solution processing of organic photodiodes is significantly cheaper than conventional subtractive processing. However, simply converting the diode portion of the detector fabrication process to solution processing does not eliminate the need for vacuum deposition and subtractive processing,

as the TFTs still need to be fabricated. X-ray detector manufacturing can still cut their costs even more by forgoing the TFT array fabrication on site and instead buy completed TFT arrays from display manufacturers. Then the x-ray detector manufacturer can simply print the photodiode layers on the completed display panel.

However, the quality of organic photodiodes still greatly trails the quality of a-Si PIN diode photodetectors in terms of most detector performance metrics. Organic photodiode performance must therefore improve to be seriously considered for the more stringent x-ray detector technologies such as fluoroscopy. In addition, organic photodiodes are not stable under atmospheric conditions and must be protected by a moisture barrier. X-ray detectors are supposed to last longer than cell phones, so the moisture barrier technology needs to be even better than the current state of the art for OLED displays in cell phones.

Solution Processed Mixed Oxides

Advances continue to be made in solution processing of mixed metal oxides. Solution processing has some advantages over traditional vacuum sputtering including process uniformity, control of the film composition, and lower cost of equipment, while disadvantages include generally high curing temperature, poorer device performance, and lower throughput (Song, et al. 2010, S. K. Park, et al. 2009, K. H. Kim, et al. 2011, Hardy and Bael 2011, Kim, et al. 2010).

Recent breakthroughs in solution processing have brought maximum processing temperatures down to 200 °C (K. H. Kim, et al. 2011, Hardy and Bael 2011) for the active layer, but the TFT performance continues to lag behind conventionally sputtered mixed oxides. In addition, some groups claim low temperature processing for the active

layer, but use a high temperature (350 °C) PECVD SiO₂ gate dielectric. As the temperature of the cure increase over 450°C, a saturation mobility of 2.5 cm²/V-s is possible (Kim, et al. 2010). Solution processing may be a viable avenue for fabricating flexible displays and should be explored.

Precursor formulations are well defined, so it would be easy to reproduce results first on silicon substrates due to the high curing temperature reported by most groups. Once a baseline has been established, incremental changes to the process could be made with the intent to reduce or eliminate the high temperature cure. For example, both spin and spray coating are available to coat the precursors. The different coating techniques may affect the final density of the film. Instead of using thermal annealing, it may be possible to cure the material using a plasma or UV light (Walther, et al. 2011). Doping the precursor material may also have an effect on the required cure temperature as well as the device performance. For example, Ahn, et al. (Ahn, et al. 2010) demonstrated a factor of 5 improvement in the saturation mobility of spin cast tin doped zinc oxide quantum dot TFTs by adding SnCl₂ to the zinc oxide quantum dot suspension prior to spinning. The optical properties of these films could be compared to sputtered deposited mixed oxide films during the initial characterization of the process. For process temperatures that are compatible with PEN substrates, TFTs can be fabricated on flexible substrates and compared with TFTs of conventionally deposited materials.

RF Sputtering

The work in Chapters 2 and 3 focused on DC sputtering in an MRC 603. RF sputtering is the more common approach with ceramic targets (Triska, et al. 2010, J. Y. Kwon, et al. 2009, Hayashi, et al. 2007). However, no systematic study has demonstrated

which deposition process is preferred. There are concerns that DC reactive sputtering can result in the poisoning of the target if the reaction rate is faster than the sputtering rate (Depla and De Gryse 2003, Waite and Shah 2007), which has been demonstrated for silicon oxide and silicon nitride films. Target poisoning could cause a gradual shift in the deposition of the mixed oxide material leading to gradual shift in performance.

The process presented in Chapter 3 utilizes a two-step deposition process where the first step does not use oxygen. The target is lit before the wafers are in front of the target so it is possible that the poisoned portion of the target is removed before the wafers are exposed to the process. In addition, the process has been in place for less than 6 months and the current IGZO target has been lit for approximately 10 hours. The expected end of life for this target is approximately 100 hours. Long term tracking of the TFT results will be necessary to determine if target poisoning is occurring.

A comparison between RF and DC sputtering can be achieved in Sunic SUNICEL Plus 400 vacuum deposition system available at the FEDC. The sputter chambers in the system are set up to allow for DC or RF sputtering of the same target. An experiment could be set up where the gas flow, pressure, active layer thickness and target composition are the same. The deposition rate at same numerical power setting is expected to be different for DC versus RF applied power. Therefore, it will either be necessary to adjust the deposition time to match the thickness or the deposition power setting to adjust the rate. Both methods should be explored independently.

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