GaN-on-Si RF Switched Mode Power Amplifiers

for Non-Constant Envelope Signals

by

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ABSTRACT

This work implements three switched mode power amplifier topologies namely inverse class-D (CMCD), push-pull class-E and inverse push-pull class-E, in a GaN-on-Si process for medium power level (5-10W) femto/pico-cells base-station applications. The presented power amplifiers address practical implementation design constraints and explore the fundamental performance limitations of switched-mode power amplifiers for cellular band. The designs are analyzed and compared with respect to non-idealities like finite on-resistance, finite-Q of inductors, bond-wire effects, input signal duty cycle, and supply and component variations. These architectures are designed for non-constant envelope inputs in the form of digitally modulated signals such as RFPWM, which undergo duty cycle variation. After comparing the three topologies, this work concludes that the inverse push-pull class-E power amplifier shows lower efficiency degradation at reduced duty cycles. For GaN based discrete power amplifiers which have less drain capacitance compared to GaAs or CMOS and where the switch loss is dominated by wire-bonds, an inverse push-pull class-E gives highest output power at highest efficiency. Push-pull class-E can give efficiencies comparable to inverse push-pull class-E in presence of bondwires on tuning the Zero-Voltage Switching (ZVS) network components but at a lower output power. Current-Mode Class-D (CMCD) is affected most by the presence of bondwires and gives least output power and efficiency compared to other two topologies. For systems dominated by drain capacitance loss or which has no bondwires, the CMCD and push-pull class-E gives better output power than inverse push-pull class-E. However, CMCD is more suitable for high breakdown voltage process.

ACKNOWLEDGMENTS

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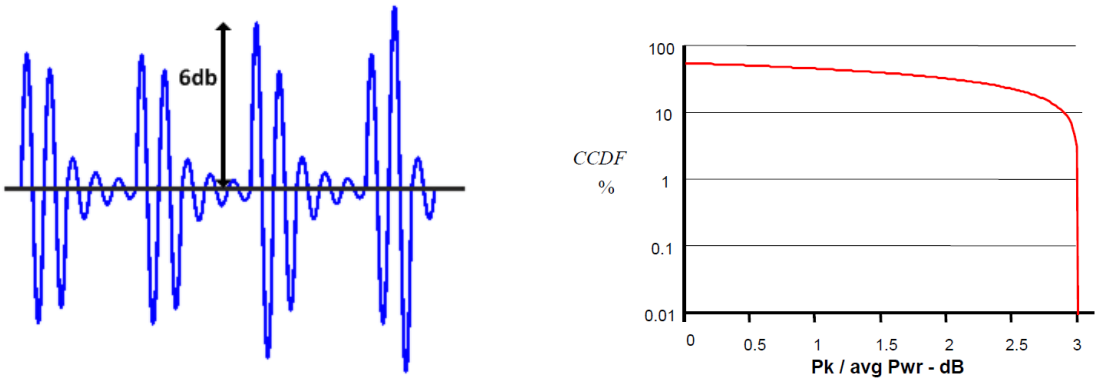
INTRODUCTION

1.1 Motivation

In the modern world of wireless communications with Internet of Things (IoT) on the rise, data traffic almost doubles every year [1]. The main cause of this is the rapid customer adoption of smart phones having mobile internet in addition to usual audio signals. To cope up with the demands for higher data rates, smaller cellular networks have been installed in densely populated areas known as femto/pico cells. Complex multi-carrier modulation schemes like OFDM have been adopted in 4G LTE standards. In this emerging LTE-centric era for base-stations, micro/pico/femto cells, and handsets, it is necessary to have signals with large bandwidth and high Peak-to-Average Power Ratio (PAPR) in order to supply the necessary data rates for 4G and beyond [2]. Figure 1(a) shows a signal with high PAPR, where the average power level is 6dB lower than the peak power. The complimentary cumulative density function (CCDF) of such a high PAPR signal is shown in Figure 1(b), and illustrates that the probability of peak occurrence is low. Since the wireless transmitters' power amplifiers (PAs) are designed to give best efficiencies at peak power, the PA operates at reduced efficiencies for most of the time. Therefore, the price paid for these increased demands on power amplification is reduced power amplifier efficiency.



(a) (b)

Figure 1: (a) Signal with high PAPR (b) CCDF of high PAPR signal

Handsets demand high efficiency power amplifiers to boost the battery life, while base stations require high efficiency to increase reliability and lower the cost of heat-sinks. Doherty power amplifiers are the most common and widely used power amplifier architecture in modern base-station transmitters, as it enables high backed-off efficiency while maintaining PA linearity. Doherty PAs work on the principle of load modulation [3]. For handsets, envelope tracking, which uses supply modulation, is the most widely used form of efficiency enhancement for backed-off power levels [4].

With rapid progress in compound semiconductor structures like GaN/GaAs/InP, as well as the rapid evolution of digital processing technologies, the digital transmitter architecture employing a Switched-Mode Power Amplifier (SMPA) is becoming an increasingly more viable solution to meet the demands for RF transceiver programmability and efficiency. The SMPA is the main challenge for realizing a digital transmitter. A switched-mode power amplifier is theoretically 100% efficient because the transistors operate as switches unlike linear amplifiers which employ the devices as current sources. However, device parasitics limit this theoretical 100% value, and this

research explores these fundamental power, efficiency and speed limitations. The transmitter unit, which is responsible for generation of high power RF signal information, is the most power hungry unit of a Base Transceiver Station (BTS). Furthermore, heat sinks for these transmitters add cost, space, and maintenance. If this energy consumption can be reduced through efficient utilization of the DC power, the station's operating and installation costs (OPEX and CAPEX) will be significantly reduced. Therefore, energy efficiency is the most important parameter for a base-station transmitter. On other hand, component and size is most important for handsets. There has been a significant amount of research on transmitter efficiency enhancement techniques using a linear amplifier building block. Less work has been done to explore the efficiency, linearity, and practical realization of digital transmitter architectures. Apart from high efficiency, wide RF operating bandwidth is desirable in modern day transmitters. For example, the LTE standard uses 44 frequency bands spread across 700MHz – 3.5GHz range. Implementation of future infrastructure that supports dynamic spectrum allocation will not be possible without broadBand RF bandwidth transmitters. This work focuses on a digital transmitter architecture in an effort eliminate the need for multiple PAs in a single transmitter.

1.2 Digital Transmitter Architecture

A block diagram of a conventional transmitter is shown in Figure 2. The baseband signal processing is usually done in the digital domain using DSP integrated on a CMOS process. Up-conversion and modulation are done in analog domain using DACs and Local Oscillators (LO). A linear power amplifier (class A/AB, class F) is employed for

each band in a conventional transmitter, and this amplifier suffers from low efficiency, thus limiting the overall transmitter efficiency.

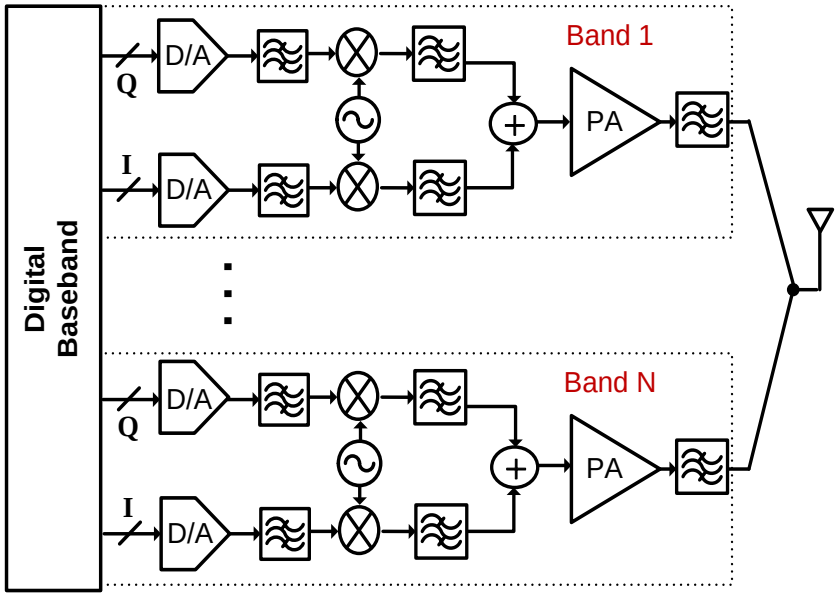


Figure 2: Block diagram of a conventional up-conversion Transmitter, where each band is supported by a different up conversion chain.

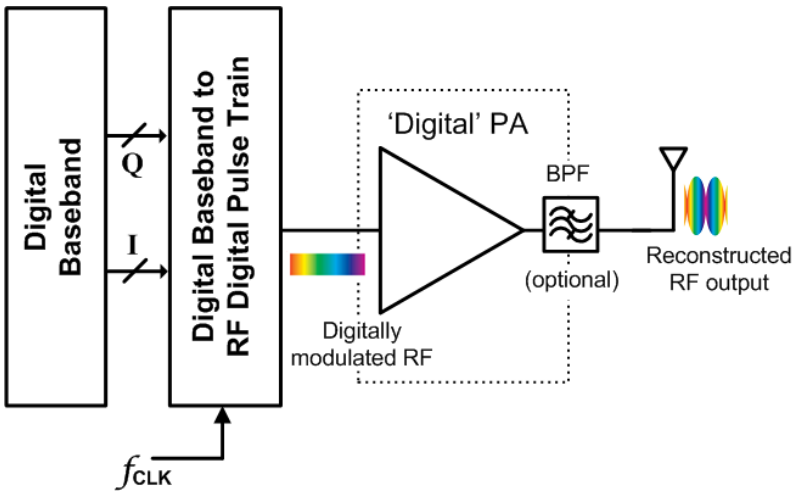


Figure 3: Block diagram of a Digital Transmitter

In contrast, a digital transmitter (Figure 3) uses an efficient switched-mode power amplifier (SMPA) in addition to a digital modulator. The baseband signal is digitized and processed in DSP. The amplitude information is then encoded into pulses using techniques such as RFPWM, Bandpass Delta-Sigma modulation (BPDSM), or Bandpass Pulse-Width and-Position Modulation (PWPM) [2]-[4]. Digital transmitters can be easily reconfigured and reprogrammed at the base-band using high-speed DSPs. Amplitude information in an RFPWM-based digital transmitter is manifested as change in duty cycle of the digital input signal that is driving the SMPA, whereas phase information is manifested as the timing of switching [4]. Power Back-Off (PBO) corresponds to reduced duty cycles, and in order to maintain high efficiency at PBO, the SMPA must be able to efficiently amplify the reduced duty cycles.

Modern wireless communications systems are now being fully integrated into RF systems-on-chip (SOC) with the exception of the power amplifier. CMOS PAs scaled in size and supply voltage has potential for integration but is limited due to following 2 major reasons:

1. Low supply voltage and device breakdown limits the maximum achievable PA output power [7], [8].
2. On-chip passive components (i.e. inductors) have loss, due to the CMOS substrate and thin metal layers [9].

With the rapid advancement in III-V compound semiconductors; medium-power (5-10W) SMPA implementation has become feasible. The design of efficient SMPAs using Gallium Nitride-no-Silicon (GaN-on-Si) is the focus of this thesis.

1.3 Digital Transmitter Challenges

Though a digital transmitter shows promise for achieving high efficiency, the following investigations must be performed before these transmitters can be adopted by industry:

- Process technology (GaN vs GaAs vs LDMOS)
- SMPA topology (class D/E/F)
- Encoding scheme
- Driver Design

The major challenge is to achieve a combination of the best process technology, most efficient SMPA topology and coding scheme, and implement suitable drivers. This work is an effort to investigate the best process technology with most efficient SMPA topology. The overall efficiency of the digital transmitter is not only limited by the SMPA efficiency, but also by the coding efficiency. Overall transmitter efficiency is given as:

$$\eta_{transmitter} = \eta_{coding} \times \eta_{SMPA} \tag{1.1}$$

RFPWM has a better coding efficiency than DSM; hence RFPWM is more suitable for SMPAs, though DSM provides noise shaping capability [11]. At times it may be advantageous to use multilevel RZ signal for switching the PAs. Figures 4 summarizes the major the challenges in a digital transmitter design.

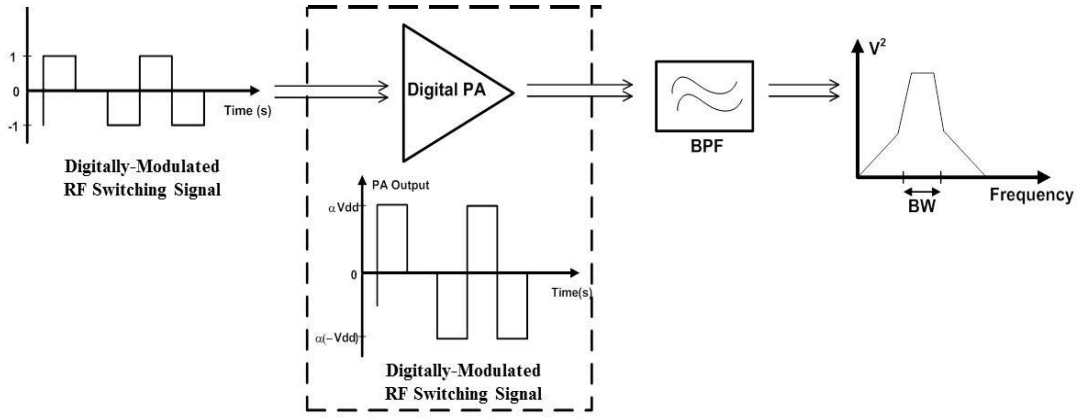


Figure 4: Digital Transmitter Challenges

1.4 Thesis Contributions

This thesis focuses on theory, design and practical realization of SMPAs that are compatible with digital transmitter architectures. The practical issues with existing SMPA architectures have been discussed and three SMPA topologies have been implemented in a GaN-on-Si process. These architectures have been investigated for medium power (5-10W) femto cell applications at 900MHz. This work targets LTE bands 5(UL- 824-849MHz, DL-869-894MHz), 6(UL- 824-849MHz, DL-869-894MHz) and 8(UL- 824-849MHz, DL-869-894MHz).

Though GaN PAs have been demonstrated to give good performance at high power levels, they have not been demonstrated for low and medium power levels amplifying non-constant envelope signals modulated in the form of RFPWM. SMPAs are known for efficient amplification of constant-envelope signals like GSM, GMSK. However, with non-constant envelope (reduced duty-cycles) the output power of the SMPA goes down. They have switching loss that dominates and doesn't go down, whereas output power goes down reducing the overall efficiency. In the case of RPWM, pulses may become so

narrow that the input signal information is lost and the output does not reflect the input signal. Thus, we need to employ SMPAs that can efficiently amplify reduced duty cycles with minimal efficiency degradation at power back-off. Various SMPA topologies are investigated for the above mentioned application, and three SMPA topologies are implemented: Current-Mode Class-D (CMCD), Push-pull class-E, and Inverse push-pull class-E. These amplifier architectures have been compared with respect to theoretical analysis, simulation, and measured results. It has been concluded that the inverse push-pull class-E gives higher output power as compared to others in the presence of bondwire inductances. Table 1 shows the target switched-mode PA to be designed in this work.

Parameter	**Target**
Application	Pico/femto cells
Frequency Range	800-1000 MHz
Process Technology	GaN-on-Si
Power Range	5-7W
Efficiency	75-80%
Modulation scheme	LTE

Table 1: PA Design Target

CHAPTER 2

SWITCHED MODE POWER AMPLIFIERS

2.1 Introduction

In switched-mode power amplifiers, the transistor operates in triode and cut-off regions, as shown in Figure 5. As a result, there is very low current-voltage overlap. Theoretically, SMPAs are 100% efficient, assuming an ideal transistor with zero knee voltage and zero on-resistance.

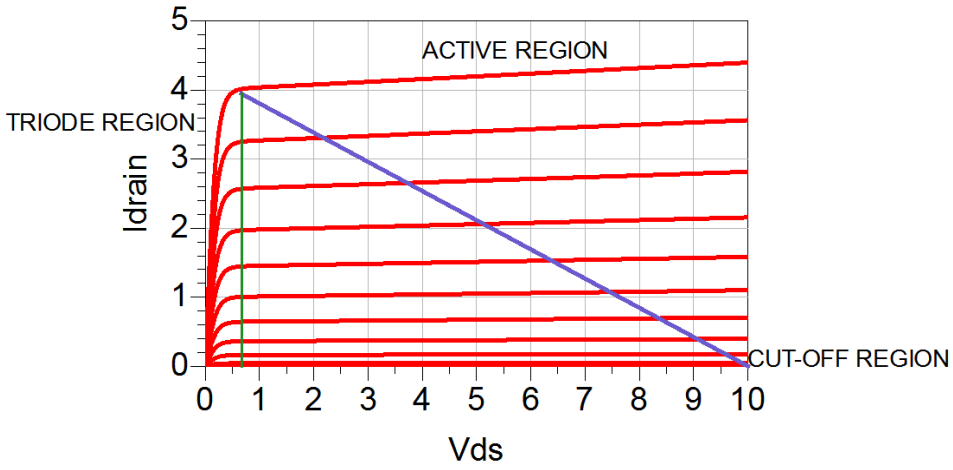


Figure 5: Transistor I-V Characteristics showing Region of Operation

However, any transistor operating as a switch is non-ideal and has parasitic elements, which lead to losses and non-100% efficiency. Section 2.2 describes the device loss when operating as a switch. Section 2.3 highlights the advantages of GaN, and Sections 2.4 through 2.9 describe various switched-mode PA architectures that address the device switching loss and have been implemented in GaN-on-Si.

2.2 Switch losses

A transistor operating as a switch can be modelled as shown in Figure 6(b). The switch model includes parasitic losses associated with a device. When the switch is ON, finite switch on-resistance R_{ON} causes loss. When the switch makes an ON-to-OFF transition, parasitic series inductance L_s causes loss (Figure 6(c)) given as:

$$\left.\begin{aligned} P_{L_S} &= \frac{L_S \times {I_{OFF}}^2 \times f}{2} \\ P_{R_{ON}} &= R_{ON} \times {I_{DC}}^2 \end{aligned}\right\} \tag{2.1}$$

Where P_{L_S} is the power loss due to parasitic series inductor, $P_{R_{ON}}$ is the power loss due switch on-resistance, I_{OFF} is the current through the just before turning ON.

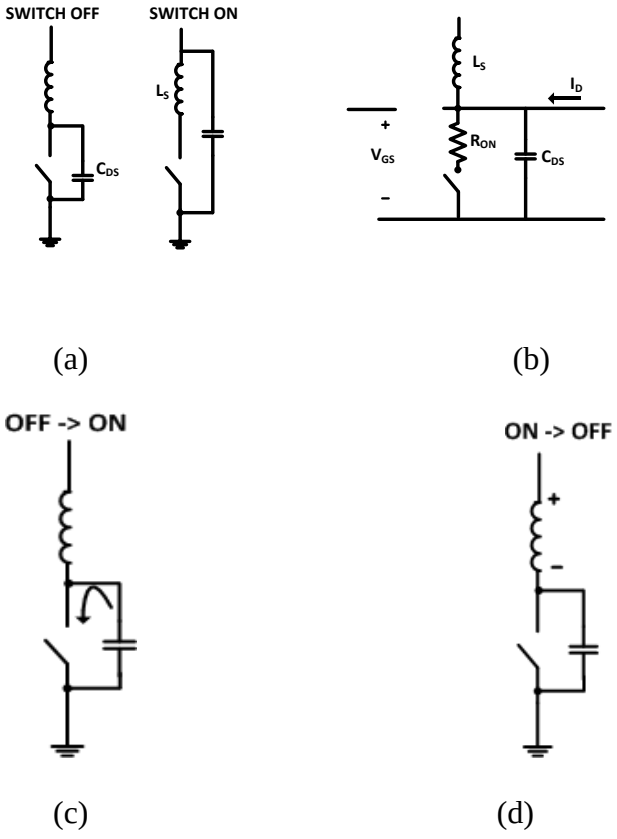


Figure 6 : Switch (a) symbol (b) model (c) turn-on loss (d) turn-off loss

When the switch is making ON-to-OFF transition, there is also loss associated with the charging and discharging of parasitic drain capacitance C_{DS} (Figure 6(d)) given as:

$$P_{C_{DS}} = \frac{C_{DS} \times V_{ON}^{\ 2} \times f}{2} \tag{2.2}$$

Where $P_{C_{DS}}$ is the power loss due to parasitic drain capacitance, V_{DS} is the voltage across the switch just before turning off, and f is the switching frequency.

2.3 Why GaN based Switch Mode Power Amplifier?

GaN is a compound semiconductor of group III-V and exhibits useful properties for microwave/RF power amplifiers as summarized in Table 2. These traits include high power density, high breakdown voltage, high current density, high electron mobility, and low R_{on} & C_{ds}.

DEVICE	***Eg(eV)***	***$\mathcal{E}_r$(F/m)***	***E_c(V/m)***	***K(W/°K.cm)***
Si	1.12	11.9	$3X10^5$	1.5
GaAs	1.43	12.5	$4X10^5$	0.54
GaN	**3.4**	**9**	**$2X10^6$**	**1.3**
SiC	3.2	10	$7X10^5$	4.5

GaN-on-Si used due to lower cost

Table 2: Material Properties of Si, GaAs, GaN and SiC

These advantages can be explained with respect to Table 2 shown above, which compares GaN, GaAs and Silicon. GaN has wide bandgap (*Eg)*, which leads to high

breakdown voltage and high power density. GaN has a high critical Electric field ($\mathcal{E}_r$) causing high current density and high electron mobility. GaN has low relative permittivity ($\mathcal{E}_r$), which means the device size can be increased with small increase in device parasitic capacitance C_{DS}. This would also lead to low R_{ON}. However, GaN has low thermal conductivity as compared to GaAs or SiC. SiC has excellent thermal conductivity, and certain GaN-based transistors are grown on SiC substrate. But, GaN-on-SiC is expensive. Being a lower cost alternative, GaN-on-Si is used in this work.

2.4 Class-E Power Amplifiers

Class-E is the most common type of switched mode power amplifier, working on the principle of minimizing switching power consumption during the current-voltage overlap by applying two boundary conditions of zero voltage switching (ZVS) and zero derivative switching (ZVDS). This switching criterion is also known as soft switching. The optimum class-E imposes the following three conditions at the drain waveforms:

1. The rise of the voltage waveform is delayed until after the transistor has turned off,
2. The collector voltage is zero at the time the transistor turns on and
3. The slope of the collector voltage is zero at the time the transistor turn on

This is accomplished using a passive RLC load network. The conventional single ended class-E power amplifier is shown in Figure 8. The drain parasitic capacitance C_{DS} has an external parallel capacitor C_{ext} along with a series inductor. This network ensures that the drain voltage is zero when the switch turns ON. The values are chosen such that the voltage waveform's derivative is also at zero (ZVDS). Figure 9 shows ideal drain voltage and drain current waveform in a class-E power amplifier. Theses waveforms are

shaped such that the current and voltage transitions are displaced from each other in time and result in zero product.

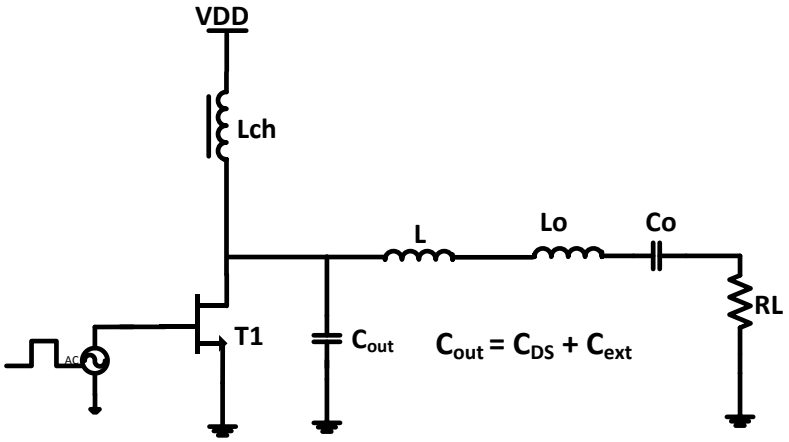


Figure 7: Single Ended Class-E Power Amplifier

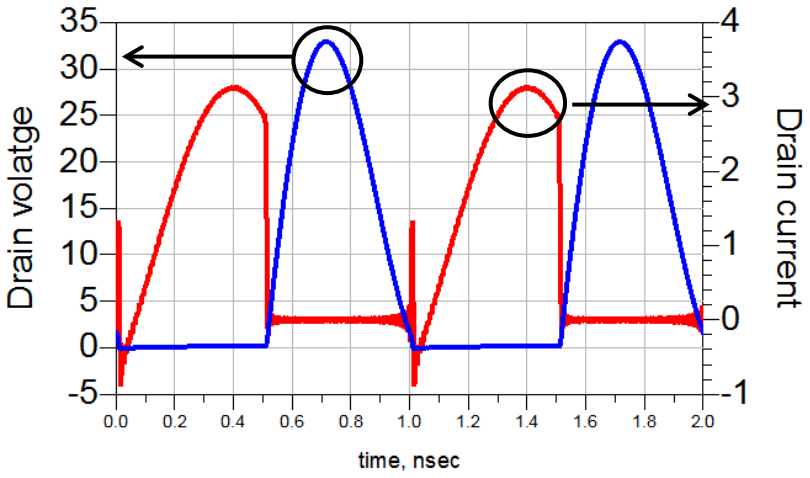


Figure 8: Ideal Class-E waveforms

Conceptually, the class-E PA works by storing energy in an inductor L_{ch} when the switch is closed and then releasing that energy into a passive resonant network consisting of C_{OUT}, L, L_o and C_o when the switch is opened. Therefore, if the duration of switch closure is reduced or increased, the amount of energy stored per cycle is

reduced or increased proportionately. A change in duty cycle therefore corresponds to a change in output power. The class-E concept was introduced by Sokal in 1975 [19] and was extensively analyzed by Raab and Kazimierzcuk [20], [24]-[28]. These works provide class-E Design equations and component values to achieve 100% theoretical efficiency but, impose a condition of 50% duty cycle to obtain maximum output power.

However, it has since been proven that soft switching is not necessary to obtain 100% efficiency, though it de-sensitizes the effect of minor mistuning on efficiency [28]. Soft switching actually places additional constraint on power and frequency. Relaxing this soft switching condition (ZVDS ≠0) gives additional design flexibility in terms of operating frequency, output power, and load resistance matching [32], [33]. This is referred to as sub-optimum class-E. However, this design flexibility comes at the cost of lower output power as compared to an optimum class-E design. Class-E amplifiers have been extensively analyzed for both optimal and sub-optimal design with respect to circuit losses, component variations, duty cycle, and frequency variations [27]-[31]. The variation in input power (P_i), output power (P_o), and drain efficiency (η) of a class-E PA with respect to duty cycle (D) is as follows [20]:

$$\left.\begin{aligned} P_O &= \frac{{V_{DD}}^2 g^2 R_L}{2R_{DC}} \\ \eta &= \frac{P_o}{P_i} = \frac{g^2}{2} \times \frac{R_L}{R_{dc}} \end{aligned}\right\} \tag{2.3}$$

$$g(\psi,\phi,y) = \frac{\left[2y\sin\phi_1.\sin y - 2y.\cos\phi.\cos y + 2\cos\phi_1.\sin y\right]}{\left[-2\sin(\phi - y).\sin y.\sin\phi_1 - 0.5\sin 2y.\cos(2\phi+\psi) + y\cos\psi\right]}$$

$$R_{dc} = \frac{1}{2\pi B}\left\{\left[2y^2 + 2yg.\sin(\phi - y)\right] - 2g.\sin\phi, \sin y\right\}$$

$$\phi_1 = \phi + \psi\,; \quad y = (1-D)\times\pi$$

Where g is the dc-to-ac voltage transfer function, ϕ is the output phase angle

ψ is the load phase angle, R_{dc} is the dc input resistance seen by the power supply,

R is the load resistance, D is the duty cycle

Component values of class-E are given as [20]:

$$\left.\begin{aligned} C_{OUT} &= \frac{P_O}{\pi\omega.V_{DD}{}^2} \\ R_L &= 0.577\times\frac{V_{DD}{}^2}{P_O} \\ L &= 0.665\times\frac{V_{DD}{}^2}{\omega.P_O} \end{aligned}\right\} \qquad (2.4)$$

Class-E limitations:

Class-E PAs exhibit a few fundamental performance limitations as detailed in this section:

1. Class-E PAs have a frequency limitation due to the drain parasitic capacitance, given as [31]:

$$f_{\max} = \frac{1}{2}\times\left|\frac{y\times\cos y - \sin y}{\frac{y}{\sin y}}\right|\times\frac{1}{\pi^2\times R\times C_{OUT}} \qquad (2.5)$$

$$y = (1-D)\times\pi \;\;\&\;\; C_{OUT} = C + C_{DS}$$

Where, D is the duty cycle, C is the external shunt capacitor for ZVS, C_{DS} is the device parasitic capacitance and R is the optimum load resistance.

At higher frequencies, the C_{OUT} required for ZVS may be smaller than C_{DS}, which limits the frequency of operation. GaN devices have a lower C_{DS} and hence can potentially operate at higher frequencies. Equation 2.7 also shows that f_{max} is the function of duty cycle.

2. The peak drain voltage and currents in an optimum class-E is given as:

$$\left.\begin{aligned} Vsw_{\max} &= 3.56V_{DD} \\ Isw_{\max} &= 2.84I_{DC} \end{aligned}\right\} \tag{2.6}$$

It was however shown that through sub-optimal design, peak voltage and current at the drain can be set as a design parameter by varying phase angle of the output voltage [36]. Nonetheless, the peak drain voltage will be at least three times the supply voltage, which is not possible to implement using devices with low breakdown voltage, unless cascoding is employed [50].

Furthermore, if the class-E is driven by RFPWM with variable duty cycle, the peak voltages increase at non-50% duty ratios. The following equations relate peak voltage and current at the drain as a function of duty cycle [34]:

$$\left.\begin{aligned} Vsw_{\max}(D) &= \frac{V_{DD}\tan(\pi D+\phi).\sin(\pi D)}{(1-D)\left[\pi(1-D)\cos(\pi D)+\sin(\pi D)\right]} \\ Isw_{\max} &= I_{DC}\left[1-\frac{2\pi(1-D)\sin(\omega t+\phi)}{\cos(2\pi D+\phi)-\cos(\phi)}\right] \end{aligned}\right\} \tag{2.7}$$

Where ϕ is the output voltage phase, D is the duty cycle

The above equations imply that peak current increases for D<0.5, whereas peak voltage increases for D>0.5. GaN devices typically have breakdown voltage in excess of 50V and class-E power amplifiers can therefore be easily implemented using GaN.

3. Because of high peak voltage and currents the power utilization factor (PUF), or the maximum power output capability, of class-E power amplifiers is low [28].

$$P_{\max} = \frac{P_{out}}{Vsw_{\max} \times Isw_{\max}} \tag{2.8}$$

As a result, class-E power amplifiers do not utilize the transistors to their fullest power handling capability.

Sub-optimal class-E designed for non-50% duty cycle and a finite choke inductance gives the advantages of higher efficiency and design flexibility at the cost of low output power [37]. The single ended class-E has low output power, so using a class-E in push-pull configuration gives advantages of sub-optimal design as well as high output power. For the target application of medium power femto cells at 900 MHz, a push-pull class-E configuration gives higher power than a single ended class-E (analyzed in Chapter 3). Choosing a 2:1 turn's ratio for the output balun avoids the use of a 50-ohm impedance transformation network at the output. Several papers [42] have done an explicit 2nd harmonic termination on single ended class-E for better efficiency, which requires additional components.

2.5 Inverse Class-E Power Amplifiers

Unlike class-E, inverse class-E accomplishes zero-current switching (ZCS) and zero-current derivative switching (ZCDS) (Figures 10 and 11). Inverse class-E power amplifiers mitigate power losses due to parasitic series drain inductance L_S. However, they do not account for parasitic drain capacitance C_{DS}, since ZVS and ZVDS is not employed. Inverse class-E power amplifiers are suitable for discrete PA realizations, where the effect of bond-wire inductance can exacerbate the effect of parasitic series drain inductance, causing ZCS to become more important than ZVS. Moreover, for III-V based PAs like GaN, the drain capacitance is lower as compared to other processes. Inverse class-E power amplifiers have an advantage over class-E for both integrated as well as discrete high power amplifier realization [40].

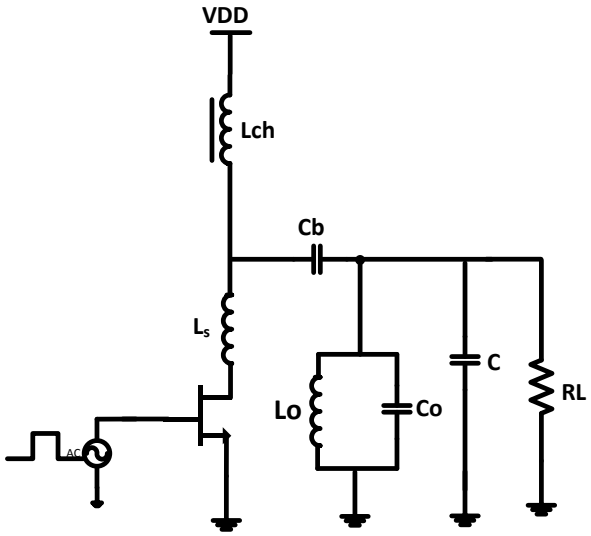


Figure 9 : Single Ended Inverse Class-E Power Amplifier

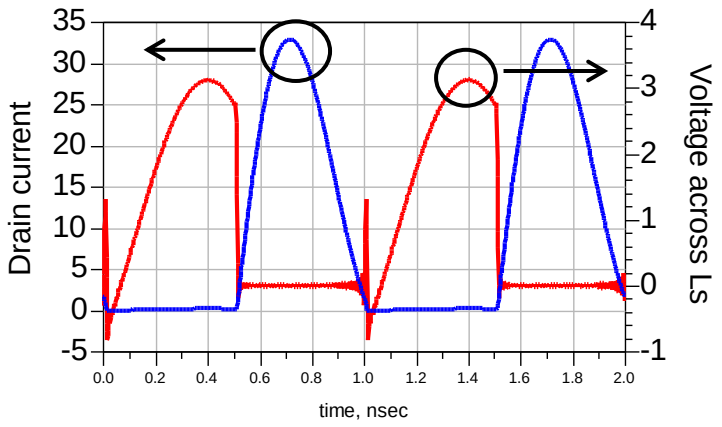


Figure 10: Inverse Class-E waveforms

The general design equations for inverse class-E design and components values are as follows [40]-[41]:

$$\left.\begin{aligned}\eta &= \frac{P_o}{P_i} = \frac{\alpha^2}{2}\times\frac{G}{G_{dc}}\\ P_O &= \frac{{V_{DD}}^2\times\alpha^2\times G}{2}\end{aligned}\right\} \tag{2.9}$$

$$G_{dc} = \frac{1}{2\pi X}\left\{\left[2y^2 + 2y\alpha.\sin(\phi - y)\right] - 2\alpha.\sin\phi, \sin y\right\}$$

$$\alpha(\psi,\phi,y) = \frac{\left[2y\sin\phi_1.\sin y - 2y.\cos\phi.\cos y + 2\cos\phi_1.\sin y\right]}{\left[-2\sin(\phi - y).\sin y.\sin\phi_1 - 0.5\sin 2y.\cos(2\phi + \psi) + y\cos\psi\right]}$$

$$\phi_1 = \phi + \psi\,;\ \ y = (1 - D)\times\pi$$

Where α is dc-to-ac voltage transfer function, ϕ is the output phase angle, ψ is the load phase angle, G_{dc} = dc input conductance seen by the power supply and G = load conductance. Component values of the inverse class-E are given as [32]:

$$\left.\begin{aligned} C &= 0.665 \times \frac{P_O}{\omega . {V_{DD}}^2} \\ R_L &= 1.73 \times \frac{{V_{DD}}^2}{P_O} \\ L_S &= \frac{{V_{DD}}^2}{\pi \omega . P_O} \\ C_O &= \frac{Q_{LC}}{\omega . R} \\ L_O &= \frac{1}{\omega^2 . C_O} \end{aligned}\right\} \tag{2.10}$$

The maximum drain voltage and current for an inverse class-E is given as [44]:

$$\left.\begin{aligned} Vsw_{\max} &= 2.8 V_{DD} \\ Isw_{\max} &= 3.58 I_{DC} \end{aligned}\right\} \tag{2.11}$$

Thus, the peak drain voltage is lower as compared to class-E. This implies that inverse class-E can be used for low breakdown voltage with more ease as compared to a class-E. Further inverse class-E requires lower inductor values for ZCS operation. Lower inductor values imply higher self-resonating frequency and higher frequency of operation. Moreover, this series inductor can incorporate the parasitic series drain inductance. Therefore, inverse class-E is also suited for integrated circuit realization.

Like class-E, inverse class-E power amplifiers can also be designed under sub-optimal conditions (i.e. with zero current switching, but non-zero current slope) [46]. The suboptimal design has the same advantages of having more design flexibility like class-E at the sacrifice of output power. However, the inverse class-E can operate at higher output power compared to a class-E at the same efficiency [41]. The advantage of using

a push-pull structure is the same as in the class-E power amplifier and hence an inverse push-pull class-E power amplifier was implemented in this work.

GaN based inverse class-E power amplifiers have advantages in terms of parasitic losses in terms of R_{ON} and C_{DS}. Power dissipation in an inverse class-E from the switch on-resistance is given as [40]:

$$\left.\begin{aligned} P_D &= 4.7583 \times P_O \times r \times G \\ \eta &= \frac{1}{1 + 4.7583.r.G} \end{aligned}\right\} \tag{2.12}$$

Where r = on resistance of the device, G = load conductance, and η = drain efficiency

When plotting η vs r, it was shown that as r increases above 4 ohm, η degradation is more than in a class-E. Therefore, above a certain on-resistance, the inverse class-E is more sensitive to Ron of the transistor. However, GaN has a low Ron, and the efficiency degradation due R_{ON} is less. It has also been proven that drain efficiency of an inverse class-E power amplifier does not go down monotonically with the parasitic drain capacitance as one may expect [48]. Hence, efficiency degradation due to C_{DS} is less, though ZVS is not satisfied.

Frequency limitation:

The maximum frequency of operation in an inverse class-E is determined by the parasitic drain inductance and maximum device breakdown voltage. At a certain RF frequency the series inductor requirement to accomplish ZCS will be lower than the parasitic series drain inductance. This will limit the inverse class-E's frequency of operation. Assuming the minimum value of L required in series with the drain comes

completely from the parasitic inductance, from inverse class-E design equations we have [48]:

$$\left.\begin{aligned} L_S &= \frac{{V_{DD}}^2}{\pi.\omega.P_O} \\ V_{D\max} &= 2.86V_{DD} \\ f_{\max} &= 0.0062\times\frac{{V_{D\max}}^2}{L_s.P_O} \end{aligned}\right\} \tag{2.13}$$

Where L_s is the parasitic drain inductance, V_{Dmax} is the peak drain voltage, and P_o is the output power.

The above equations show that an inverse class-E power amplifier with high breakdown voltages will have high operating frequency. Hence, GaN devices are suited for inverse class-E power amplifiers. Unlike class-E power amplifier, f_{max} does not depend on duty-cycle.

Furthermore, using Equation 2.9, when output power and drain efficiency is plotted as a function of input duty cycle, it is observed that the inverse class-E power amplifier undergoes less efficiency degradation under variable duty cycle and delivers higher peak powers at higher efficiency compared to a standard class-E [41]. It is also shown that inverse class-E PAs are more tolerant to circuit parameter variations.

Though mathematically proven in [41], it was not implemented or experimentally verified. Low power MESFET based inverse class-E has been implemented in [42], but with constant envelope inputs. As a result, a medium power (5-7W) GaN-based inverse class-E power amplifier for non-constant envelope input signal was implemented in this work.

2.6 Class-F Power Amplifiers

Not a switched mode amplifier in the real sense, single ended class-F PAs (Figure 11) work on the principle of waveform engineering, wherein drain voltage/current waveforms are shaped such that efficiency approaches an ideal value of 100% by presenting appropriate harmonic terminations. Figure 13 shows ideal drain voltage and current waveforms in a class-F power amplifier. An ideal class-F sees a short and open at even and odd harmonics, respectively. Infinite harmonic terminations are required to obtain high efficiency making implementation difficult and lossy. However, in practice, presenting the correct impedance through third harmonic gives adequate efficiency. These PAs are not suitable for variable duty cycle/ RFPWM type signals, as they work on overdriven sine waves (50% duty cycle).

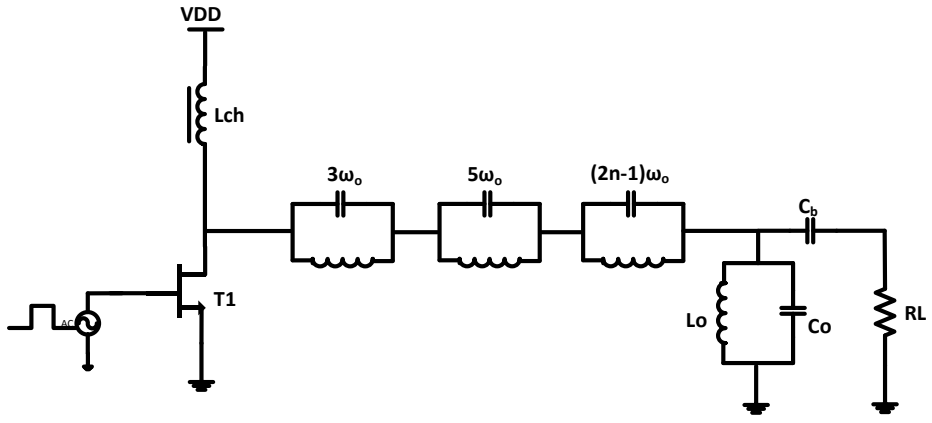


Figure 11 : Class-F Power Amplifier

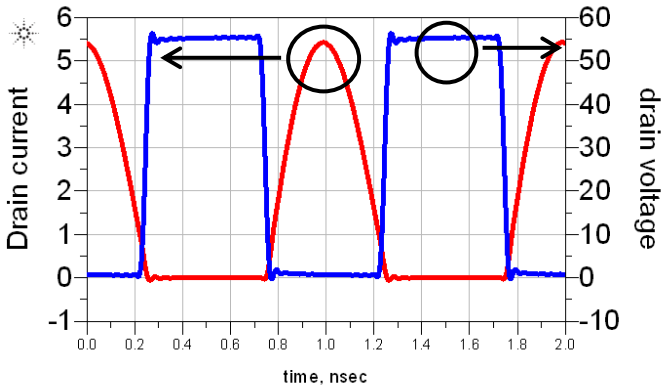


Figure 12 : Ideal Class-F waveforms

Class-F amplifiers require either a transmission element or a lumped-element equivalent to achieve proper operation, which results in large area. These are used to create large impedances at odd harmonic frequencies in order to create a square wave drain voltage. Due to parasitic drain capacitance, it is difficult to achieve large impedance at high frequency without additional tuning. Thus class-F PAs are also frequency limited because of device parasitic elements.

2.7 Inverse Class-F Power Amplifiers

Inverse class-F (Figure 14) is the dual of class-F, wherein the drain sees an open at even harmonic and short at odd harmonics. Drain current and voltage waveforms are interchanged as compared to class-F. For microwave frequencies, presenting an open at the second harmonic is easier than presenting it at the third harmonic. Hence inverse class-F is preferred. As compared to class-E, class-F waveforms exhibit higher P_{max} and better power utilization factor (PUF). The odd harmonic tuning in class-F/F^{-1} is affected by the even harmonic and vice-versa. A way to remove this dependency is the combined

use of a push-pull architecture with class-E tuning. Various harmonic control techniques in [17]-[18] show efficiency improvement.

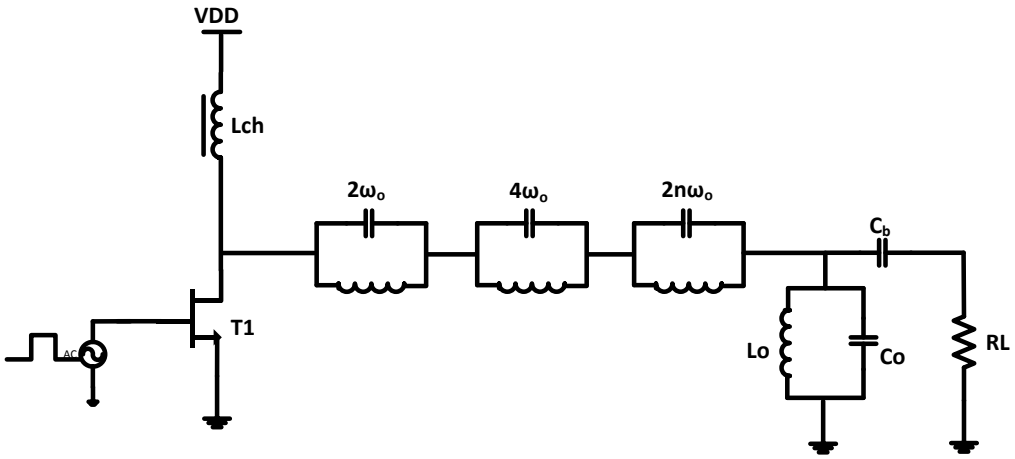


Figure 13: Inverse Class-F Power Amplifier

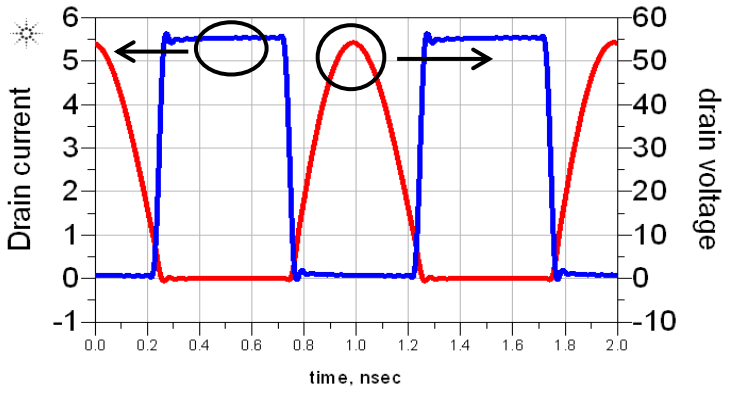


Figure 14: Inverse Class-F waveforms

There is a clever way to short-circuit an odd harmonic without adversely affecting the impedances of the adjacent even harmonics by utilizing a push-pull circuit of two identically tuned switching amplifiers. This architecture is referred to as the class EF_{odd} family of switching amplifiers, as shown in Figure 16 [17]. However, there is an easier way to accomplish this using a current-mode class-D (CMCD), as discussed in the next section.

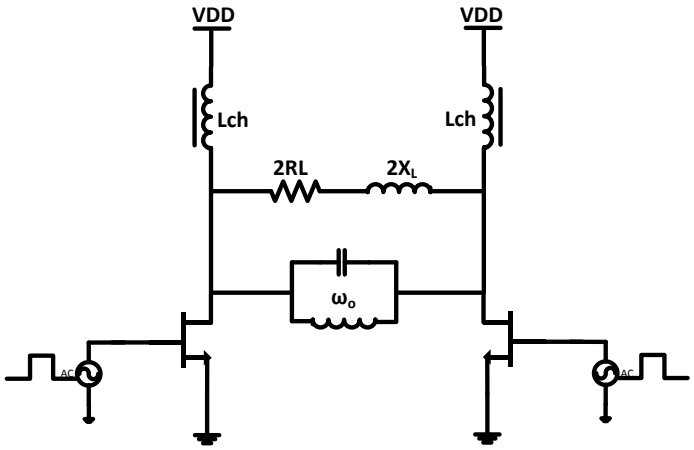


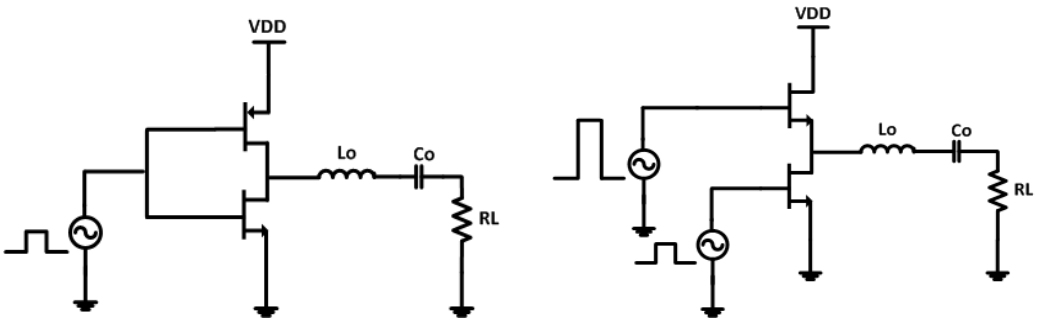
Figure 15: Class-EFodd Power Amplifier

2.8 Class- D Power Amplifiers

Though class-D amplifiers have conventionally been known to give high efficiency at audio frequencies, the first high efficiency RF PA was proposed with analytical design equations in [9]. Because of the switching nature of these amplifiers, they theoretically attain efficiency of 100%. However, as frequency goes up, the switching losses given by (2) and (3) cause tremendous efficiency degradation. There is no mechanism to counter these switching losses in a Voltage Mode Class D (VMCD) PA; therefore, efficiency and frequency of operation are limited. However, single ended VMCD (Figure 16) PAs are suitable for non-constant envelope signals applied in the form of Bandpass Delta-Sigma Modulation (BDSM) or RFPWM [13]-[15], since the duty cycle variation or aperiodic BDSM pulses does not affect the efficiency. It is also suited for H-bridge structures [16] and CMOS-based, low power digital polar modulated systems [17]. But, being single-ended, the VMCD gives low output powers. Although techniques like duty cycle reduction can be employed [13] to avoid overlap, single ended

VMCD PAs are not efficient at RF frequencies. Although single VMCD PAs can be implemented with relative ease in processes which have complimentary devices like CMOS, driving the high-side device is challenging and lossy in processes that have only n-channel devices (e.g. GaN). Techniques like bootstrap have been demonstrated for high-side drive [11], but have added complexity and frequency limitations.

Output power can be increased by using a push-pull configuration, but VMCD needs a center tapped transformer, which is lossy at RF frequencies (Figure 17). Furthermore, switching losses due to device parasitics is not mitigated on this architecture. Equation 2.14 shows design equations for a push-pull VMCD PA. Several transformer-coupled VMCD PAs have been demonstrated with constant-envelope input for frequencies below 500MHz [9], [12]. A transformer-coupled VMCD with limited efficiency using a 337MHz WCDMA input was demonstrated in [18].



(a) (b)

Figure 16: Single-ended Class-D power amplifier (a) in CMOS (b) in GaN

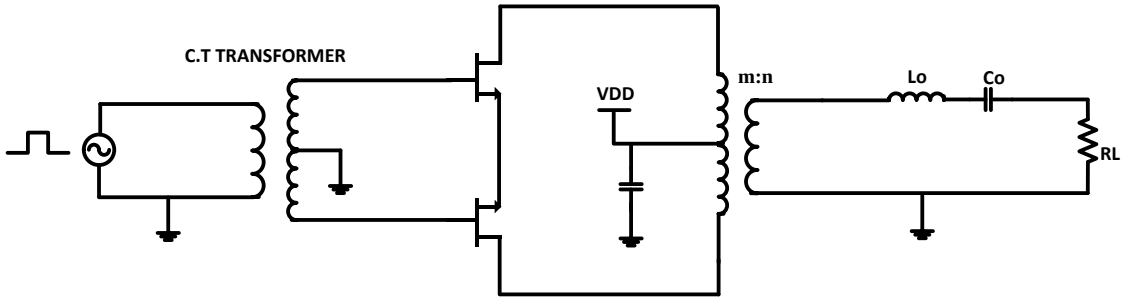


Figure 17: Voltage-Mode Class-D Power Amplifier

Design equations for VMCD [2]:

$$\left.\begin{aligned} V_{D\max} &= 2V_{DD} \\ I_{L\max} &= I_{D\max} = \frac{4V_{DD}}{\pi R} \\ I_{DC} &= \frac{8V_{DD}}{\pi^2 R} \\ P_{om} &= P_{DC} = \frac{8{V_{DD}}^2}{\pi^2 R} \\ V_{L\max} &= \frac{4}{\pi}.\left(\frac{n}{m}\right).V_{DD} \\ R &= \left(\frac{m}{n}\right)^2.R_L \end{aligned}\right\} \qquad (2.14)$$

Where, I_{Lmax} and V_{Lmax} is peak load current and load voltage, I_{Dmax} and V_{Dmax} is the maximum drain current and drain voltage, I_{DC} is average drain current, P_{om} is the maximum output power, R is the resistance looking into the primary of the transformer and n:m is the transformer turns ratio.

From Equation 2.14, it is evident that output power and efficiency is directly proportional to supply voltage (V_{DD}) and independent of input signal. Furthermore, VMCD has better power utilization factor (PUF), since drain voltage is flatter compared with class-E power amplifiers.

VMCD PAs have lower efficiency as compared to class-E or CMCD due to device parasitic losses. These losses as functions of input duty cycles and frequency are expressed as [10], [20] - [21]:

$$\left.\begin{aligned}
P_{overlap} &= \frac{\tau}{3}\times\cot(\alpha)\times P_L \\
P_{R_{ON}} &= \frac{{V_{DD}}^2\times R_{ON}}{\left[R_{ON}+\frac{2\times R_L}{\pi^2}\times\sin^2\left(\frac{\alpha}{2}\right)\right]^2} \\
P_{L_S} &= \frac{2\times f\times L_S\times {V_{DD}}^2}{\left[\frac{2}{\pi^2}\times R_L\times\sin^2\left(\frac{\alpha}{2}\right)+2\times f\times L_S\right]^2} \\
P_{C_{DS}} &= \frac{2\pi^2\times {V_{DD}}^2\times {R_L}^2\times f\times C_{DS}\times\cos^2\left(\frac{\alpha}{2}\right)}{\sin^2\left(\frac{\alpha}{2}\right)\times\left[4{R_L}^2\times f\times C_{DS}\times\cos^2\left(\frac{\alpha}{2}\right)+R_L\right]^2} \\
P_{\tau} &= (I_{DC1}+I_{DC2})^2\times R_{ON}\times\sin^2\left(\frac{\tau}{2}\right) \\
\eta_{k,loss} &= 1-\frac{2I_{DD}.V_K+4{I_{DD}}^2.R_{ON}+(C_{DS}.\omega\pi.V_{DD})^2.R_{ON}}{2I_{DD}.V_{DD}}
\end{aligned}\right\} \quad (2.15)$$

Where, $P_{C_{DS}}$ = power loss due to drain to source parasitic capacitance,

P_{L_S} = power loss due to series parasitic inductance,

$P_{R_{ON}}$ = power loss due to switch on-resistance,

$P_{overlap}$ = power loss due drain current-voltage overlap,

P_{τ} = power loss due finite switching time of the input pulse

$\eta_{k,loss}$ = efficiency degradation due to knee voltage

α = 2π.D; D = duty cycle.

In VMCD (single-ended or Transformer coupled), there is no mechanism to overcome the losses, hence VMCDs are not suited for high frequencies.

2.9 Inverse Class-D Power Amplifiers

An inverse class-D amplifier, also known as a Current-Mode Class-D (CMCD) power amplifier (Figure 18) is a good alternative for high frequencies due to its architecture. CMCD can achieve high efficiency by incorporating the parasitic device capacitance in the tank circuit such that when the device switches ON, there is no voltage across it. Thus, CMCD PAs achieve ZVS during the switch turn-on [22]-[26]. Compared to a VMCD, CMCD power amplifiers can operate at higher frequencies due the fact that C_{DS} loss is accounted at the frequency of operation. CMCDs are easier to realize because they do not require a complimentary device like single ended class-D, or a center tapped transformer as in transformer coupled VMCD. CMCD is a push-pull amplifier, but can be implemented with a balun, which has lower insertion loss compared to a center tapped transformer. The drain voltage in CMCD swings as high as $\pi*V_{DD}$. Therefore, low breakdown voltage devices such as CMOS cannot implement a CMCD with ease. GaN devices are well suited for CMCD PAs due to low device parasitics.

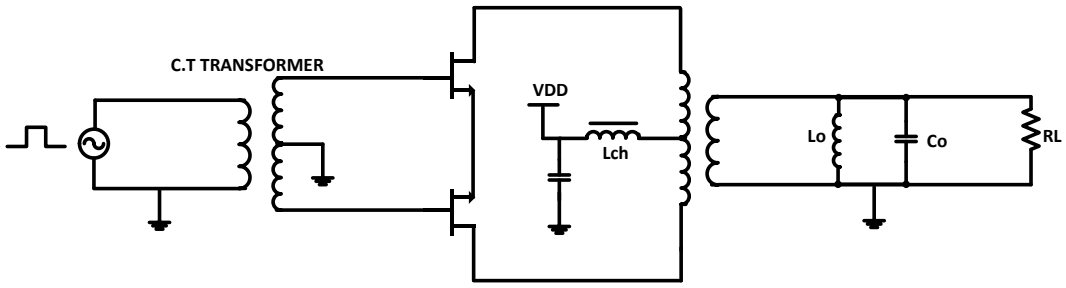


Figure 18: Current-Mode Class-D Power Amplifier

Design equations for CMCD [2]:

$$\left.\begin{aligned} V_{D\max} &= \pi V_{DD} \\ I_{DC} = I_{D\max} &= \frac{\pi^2 V_{DD}}{8R} \\ P_{om} = P_{DC} &= \frac{\pi^2 V_{DD}{}^2}{8R} \\ I_{L\max} &= \frac{\pi}{2}.\left(\frac{n}{m}\right).V_{DD} \\ V_{L\max} &= \frac{\pi}{2}.\left(\frac{n}{m}\right).\left(\frac{V_{DD}}{R_L}\right) \\ R &= \left(\frac{m}{n}\right)^2.R_L \end{aligned}\right\} \quad (2.16)$$

Where, I_{Lmax} and V_{Lmax} is peak load current and load voltage, I_{Dmax} and V_{Dmax} is the maximum drain current and drain voltage, I_{DC} is average drain current, P_{om} is the maximum output power, R is the resistance looking into the primary of the transformer and n:m is the transformer turns ratio. An equation 2.16 show that output power and drain efficiency is directly proportional to supply voltage and does not depend upon input signal power.

Push-pull/ Balanced Circuit topology advantages:

CMCD PAs present ideal class-F^{-1} type waveforms at the drain (square wave current and half sinusoidal voltage), which give high drain efficiency. The drain in CMCD sees a class-F^{-1} loading (2^{nd} harmonic open and 3^{rd} harmonic short) at the drain due to the balun and tank circuit. Balanced circuits are intrinsically open at even harmonics, and the tank circuit presents a short at odd harmonics. CMCDs are inherently class EF_{odd}. However, at higher RF frequencies, the CMCD performance is limited by the output balun. Also, driving a CMCD with square pulses needs a wideband balun at its

input. This also adds loss. Using an “n: 1” balun, the 50 ohm impedance transformation can be relaxed at the PA output, thus reducing the matching network’s loss.

CHAPTER 3

PA DESIGN AND IMPLEMENTATION

3.1. Circuit Design

Based on the description of the switched-mode power amplifiers in Chapter 2, the following three SMPA topologies (Figure 19-21) have been implemented for medium power, non-constant envelope input signals at 900MHz:

1. Current Mode class-D
2. Push-pull class-E
3. Inverse push-pull class-E

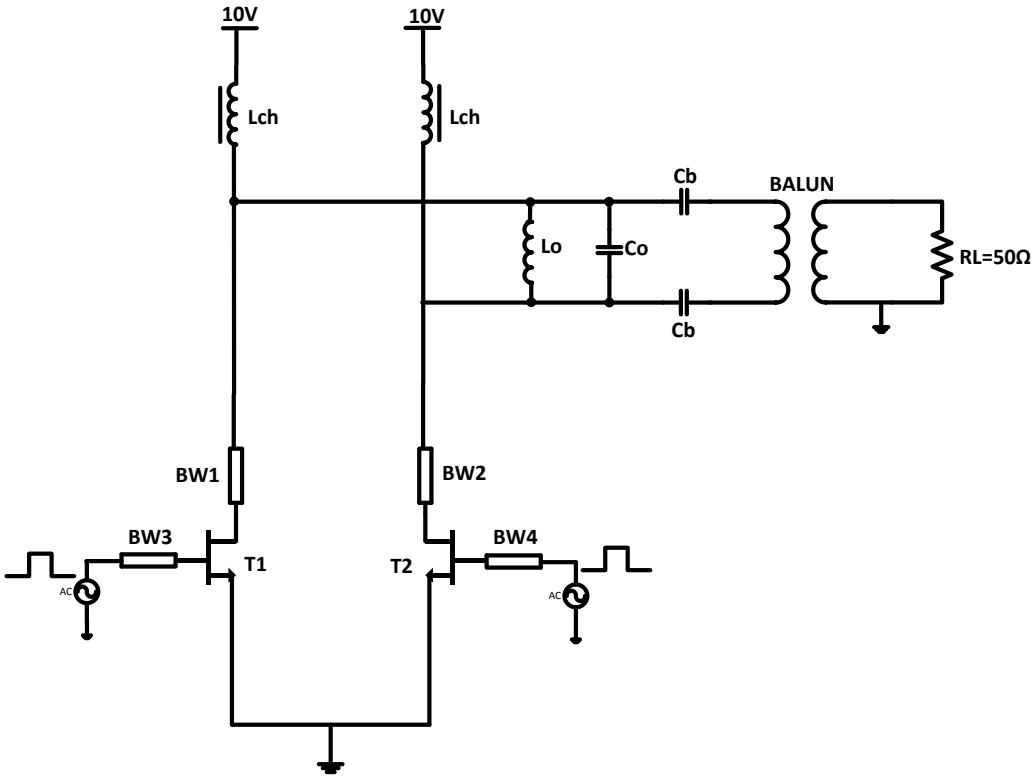


Figure 19 : Implemented Current-Mode Class-D Power Amplifier

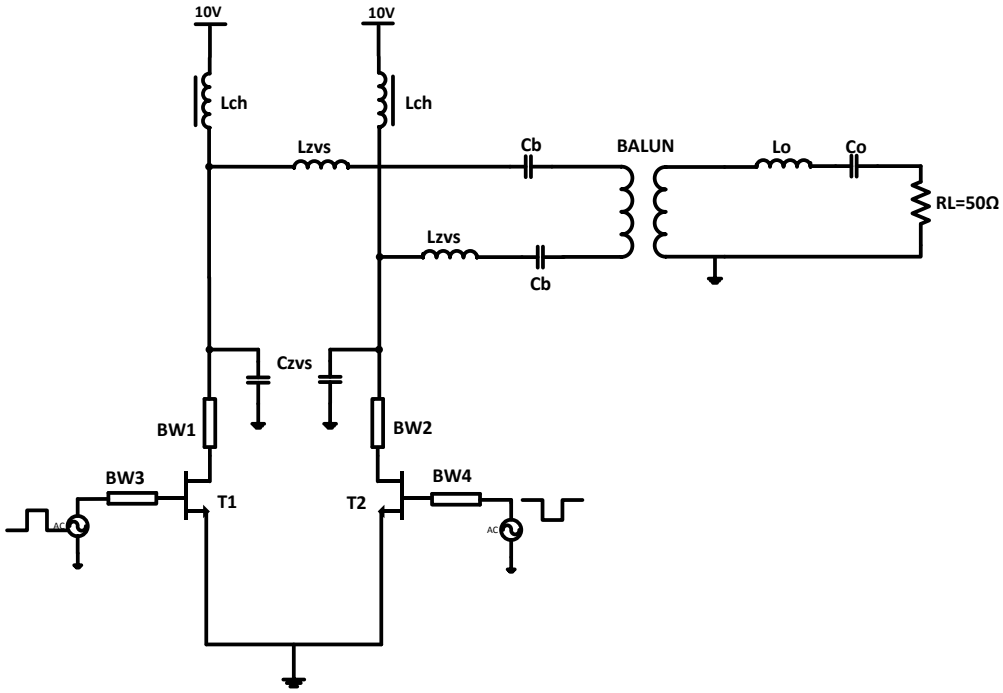


Figure 20 : Implemented Push-pull Class-E Power Amplifier

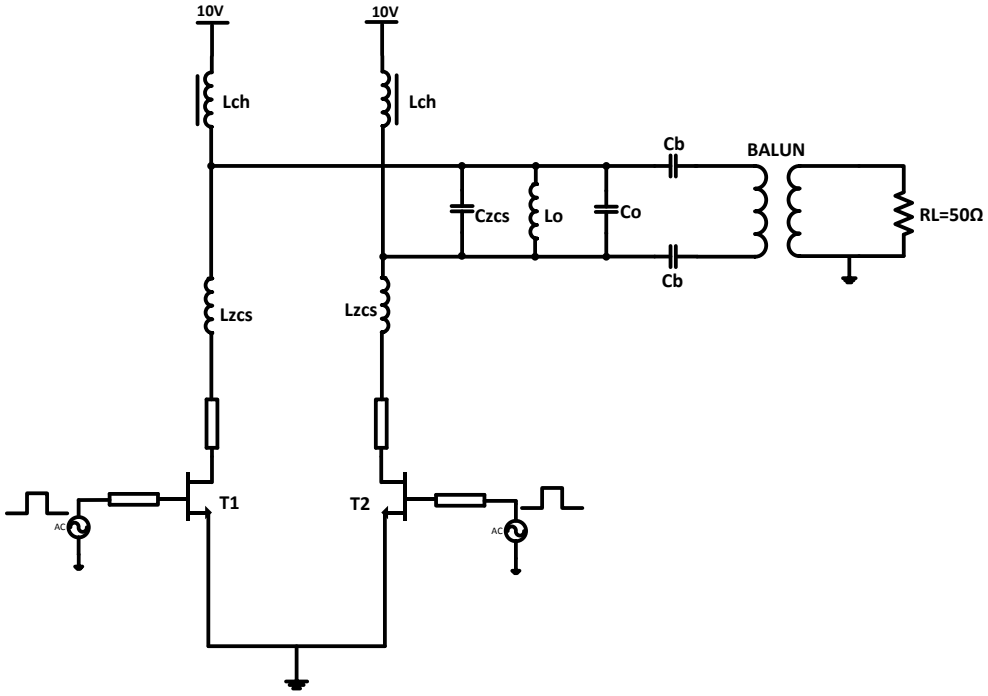
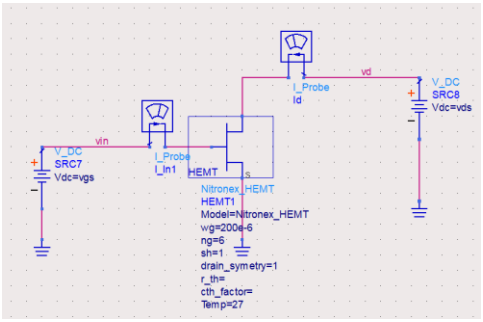
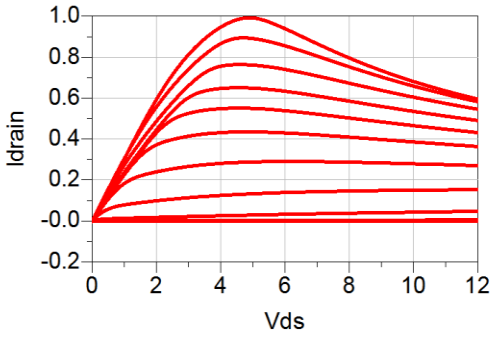


Figure 21: Implemented Inverse Push-pull Class-E Power Amplifier

In addition to the three implemented architectures, a VMCD PA was also simulated for comparison. These PAs have been implemented using GaN-on-Silicon (GaN-on-Si) discrete devices within an RF PCB design. The PAs employ 4mm GaN-on-Si devices from Nitronex. These devices were custom modelled to include self-heating effects and enable transient simulations. Since the design was targeted for medium power (5-7W) femto cell applications, a 10V supply was chosen, which forms the I-V characteristics as in Figure 22. The Id versus Vgs characteristics was used to determine the amplitude of the input switching pulse.



(a)



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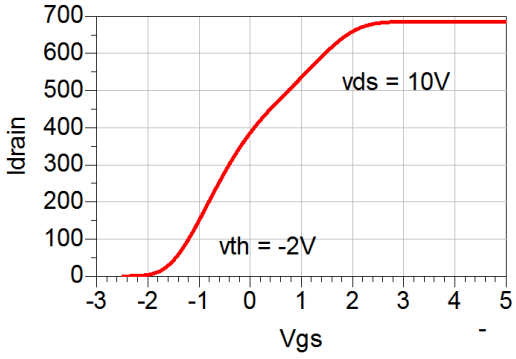
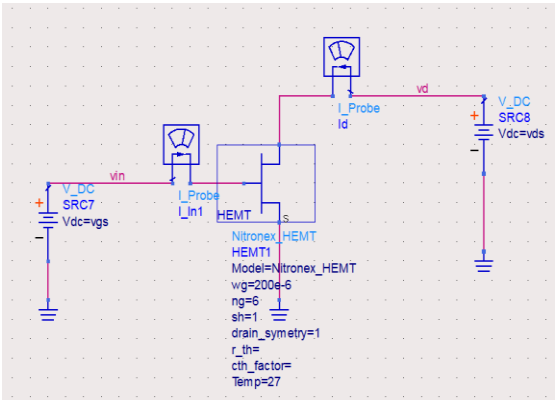


(c)



(d)

Figure 22: I-V Charactrisitcs of 4mm GaN device. (a) RF simulator schematic (b) Id vs Vds for different Vgs (c) Id vs Vgs at Vds=10V (d) Id vs Vds at Vgs=2V

From the I-V charactrisitcs, a threshold voltage, Vth= -1.9V, and an input pulse of -2.5V to +2V is required to completely switch the device.

The design eqauations for class-E, inverse class-E, VMCD, and CMCD summarized in Chapter 2 were used as a starting point the design with ideal passive components at 50% duty cycle square wave. In simulation , the load resistance was then swept to obtain the best performance (best output power and drain efficiecny). Sub-optimal class-E/inverse class-E was designed due to their design flexibilty. ZVS was achieved at the drain node in simulation by minimizing the current-voltage overlap. Furthermore, duty cycle was varied and plotted against output power and drain efficiency. The circuits were also simulated for overdriven sine wave by biasing in class-B with input matching and a stability network. Large signal input matching was provided at the gate. Figure 22 shows the inverse push-pull class-E with input matching and stabilization.

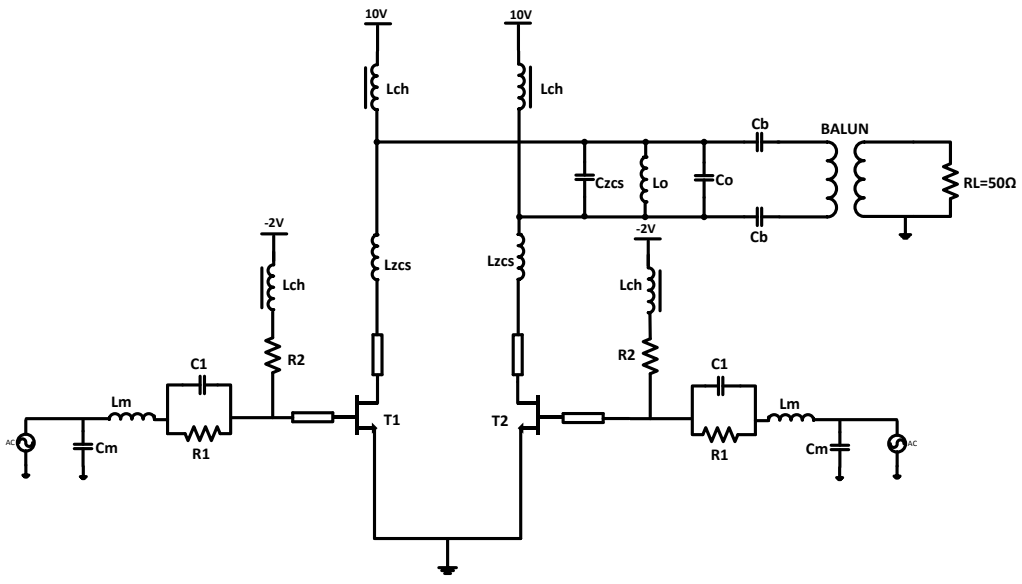


Figure 23: Inverse Push-pull Class-E amplifier with Input Matching and Stability Network for Overdriven Sinusoidal Input

3.2. Simulation Results

Table 1 and 2 shows simulation results for 50% duty cycle at 10V V_{DD} and 900MHz switching frequency. The GaN devices have parasitic elements C_{DS} and L_s. However, ideal passive components (R, L and C) were used in simulation. To reveal the superiority of the inverse class-E power amplifier, the same simulation is performed with bond wires at the device gate and drain. After including the bondwire inductances, the circuits were re-tuned to get the best drain efficiency.

PA Topology	Drain Efficiency (%)	DC Power(W)	RF Output Power(W)
VMCD	49.22	14.4	7.36
CMCD	78.45	10.22	8.021
Push-pull Class-E	75.1	11.38	8.54
Inverse Push-pull Class-E	76.9	9.73	7.48

Table 3: Simulation Results at 50% Duty Cycle without Bondwires

PA Topology	Drain Efficiency (%)	DC Power(W)	RF Output Power(W)
VMCD	48.36	8.63	4.46
CMCD	78.02	6.98	5.442
Push-pull Class-E	73	8.26	6.03
Inverse Push-pull Class-E	75.2	10.05	7.56

Table 4: Simulation Results at 50% Duty Cycle with Bondwires

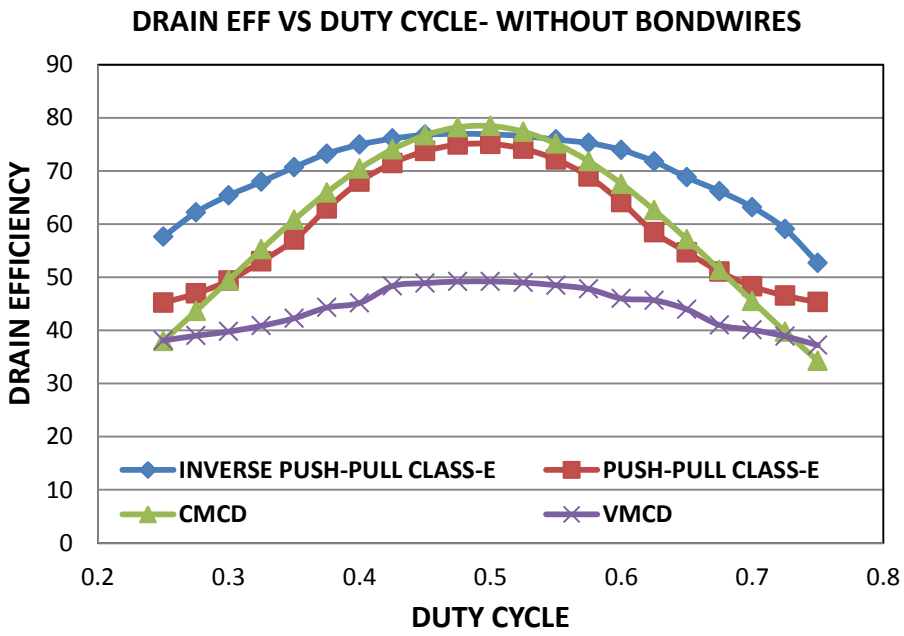


Figure 24 : Drain Efficiency vs Duty-Cycle- without Bondwires

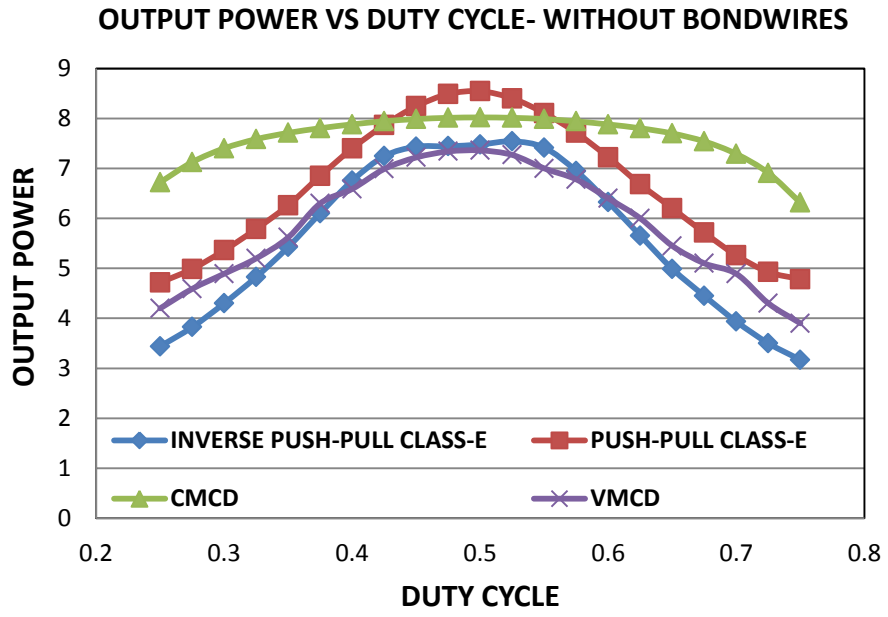


Figure 25: Output Power vs Duty-Cycle- without Bondwires

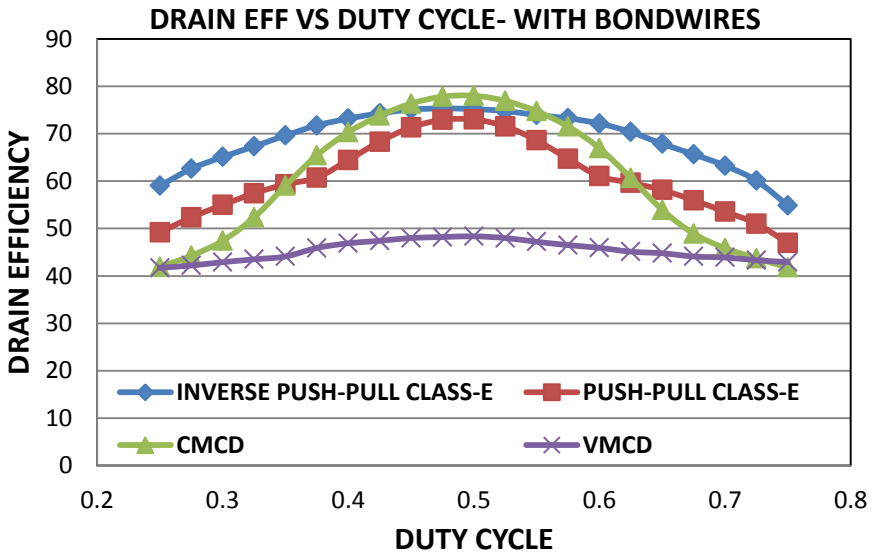


Figure 26: Drain Efficiency vs Duty-Cycle- with Bondwires

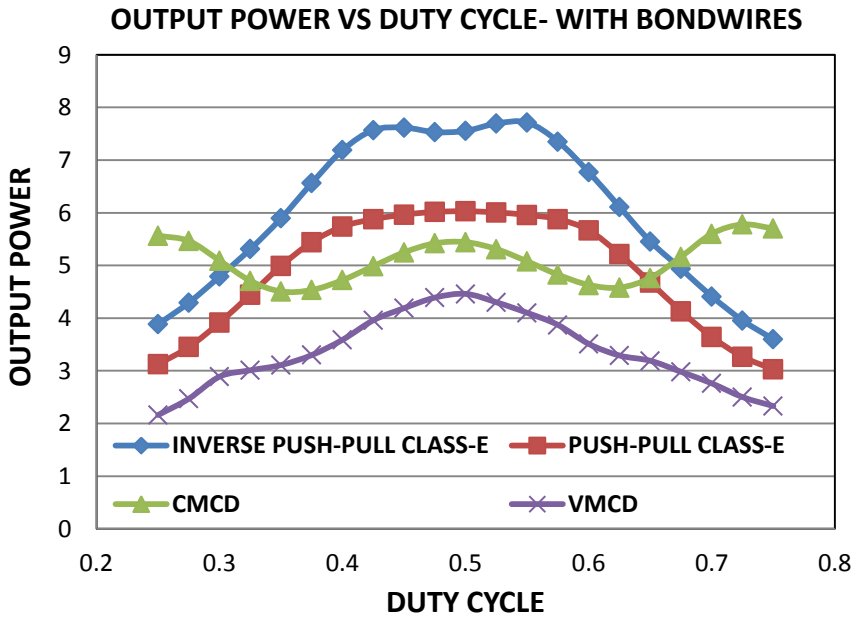


Figure 27: Output Power vs Duty-Cycle- with Bondwires

Without bond-wire inductances, C_{DS} is the only loss mechanism that must be mitigated, so class-E and CMCD with ZVS have higher output power compared to

inverse class-E as illustrated in Figure 25. However, efficiency degradation with duty cycle variation (power back-off) is less in inverse class-E as compared to class-E and CMCD, as shown in Figure 24. The efficiency of the inverse class-E power amplifier is always more constant duty cycle than class-E and CMCD, with or without bondwires (Figures 24 and 26). With bond-wire inductances, the PA must mitigate losses due to both L_s and C_{DS}. Also, losses due to bondwires dominate over C_{DS} losses (C_{DS} being lower in GaN); hence, inverse class-E can obtain higher output power at higher efficiency compared to class-E and CMCD (Figure 27).

Even though VMCD does not undergo much efficiency degradation under reduced duty cycle conditions, its efficiency is quite low as compared to other topologies implemented in this research. Even though the three implemented topologies undergo efficiency degradation, their backed-off efficiency is still comparable to the maximum VMCD efficiency. Hence, the presented architectures have a good potential for amplifying non-constant envelope signals, like RFPWM, in a digital transmitter.

Table 4 shows simulation results with all non-ideal components, using s-parameter files for passives and modelling the 50 ohm traces as coplanar waveguides in an RF simulator. The PAs are driven with a 50% duty cycle square wave.

PA topology	Output Power (W)	DC Power (W)	Drain Efficiency
Inverse push-pull class-E	7.34	9.88	74.29
Push-pull class-E	4.95	6.66	74.28
CMCD	4.83	6.87	70.3

Table 5: Simulation results with non-ideal components at 50% duty square wave

CHAPTER 4

BOARD DESIGN AND SIMULATION RESULTS

4.1. Board Design

The three SMPA topologies mentioned in Chapter were implemented by wire bonding two 4mm Nitronex GaN-on-Si die (Figure 30) in the form of a differential pair on a two layer board of FR4 material. The die pad is coated with gold, and high thermal conductivity epoxy by Epotech is used to attach the die on the board. The following components were used: high Q inductors and capacitors from Coilcraft and Murata, respectively and a 2:1 low insertion loss discrete balun by Anaren Microwave. The 2:1 balun helped to achieve the impedance transformation of the optimum load resistance to a 50 ohm antenna load, thus avoiding an output L-match. The s-parameters of these files were used in simulation before the board layout. To replicate the 50-ohm trace width, the traces on the layout were done using coplanar waveguide approximation. Figure 28 shows the board layout in National Instrument's Ultiboard tool. Figure 29 shows the top-view of the implemented SMPA board. The board is mounted on a brass-block for heat dissipation. As seen in Figure 29, the balun occupies most of the board space. This board has a provision to implement all the three power amplifiers by placing appropriate components for the respective power amplifiers.

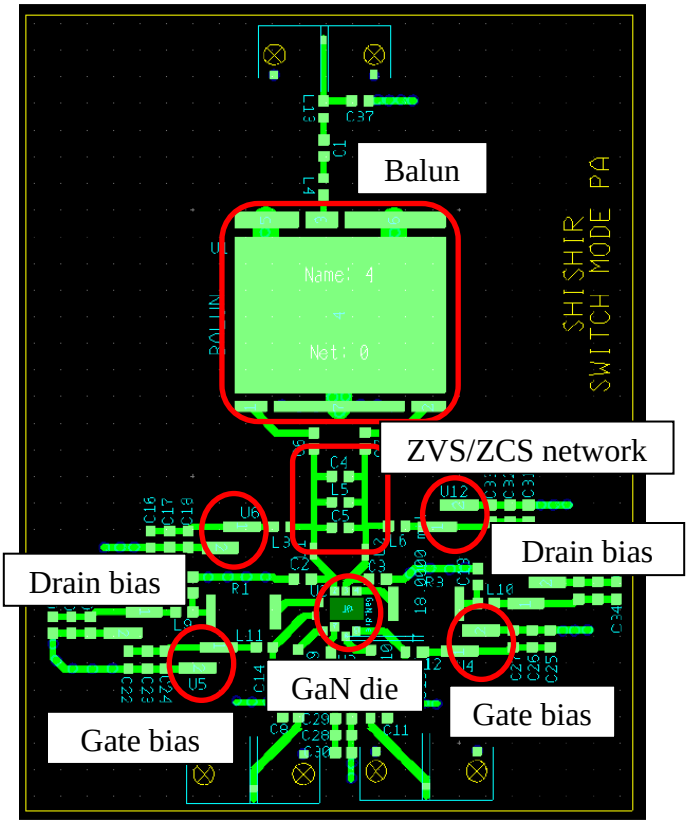


Figure 28: Board Layout

4.2. Measurement Set-up

Figure 31 shows the block diagram of lab measurement set-up and Figure 32 shows the photo of lab set-up. The SMPA board was measured with 50% square wave inputs. Overdriven sine wave was used to replicate 50% duty cycle square wave input. 5W linear amplifier by mini-circuits ZHL-%W-422+ was used to overdrive the input sine wave from signal generator. The output form the mini-circuits amplifier is converted into differential inputs using a broadBand balun from Hyperlabs (HL-9402). From ADS simulations, it was determined that the 4mm GaN devices need 26-28dBm input power tone to completely overdrive them and give similar performance, as if driven by a 50% duty cycle square wave.

However, the broadBand balun has an input power limit of 30dBm in addition to having insertion loss of 6.5dB. As a result, the maximum input power that goes at the power amplifiers is around 23dBm. This power does not completely mimic a 50% duty cycle square wave and there is some power loss due to finite rise time of the sine waves.

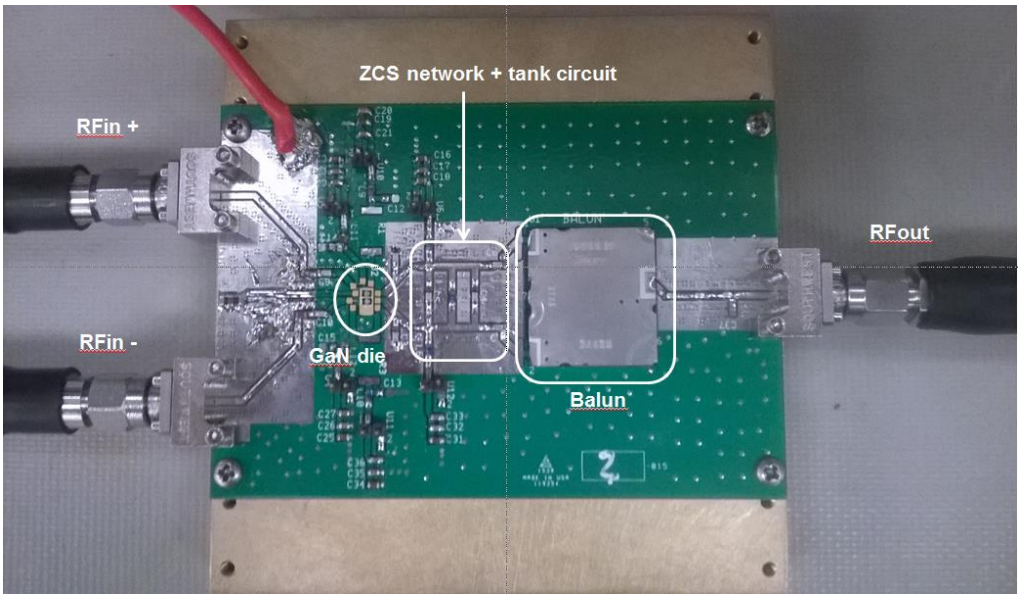


Figure 29: Inverse Push-pull Class-E amplifier Board on Brass Block (Heat Sink)

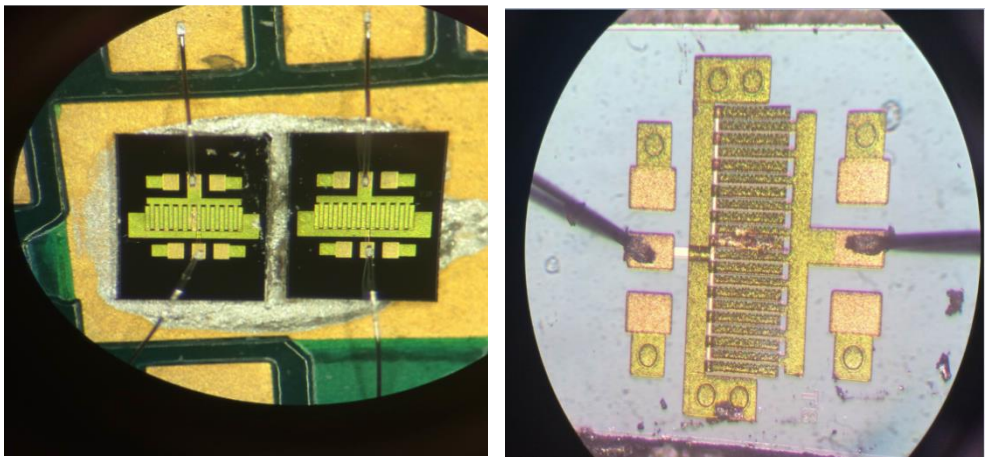


Figure 30: Die Photograph

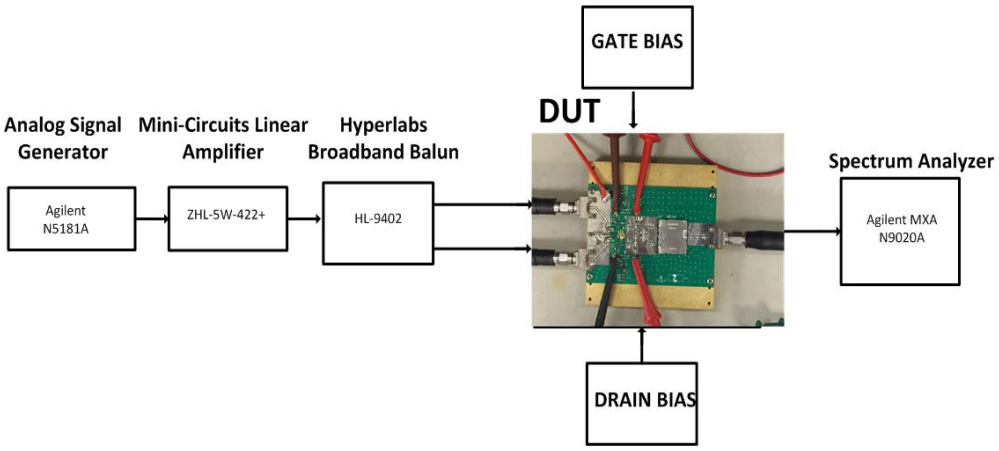


Figure 31: Block Diagram of Measurement Set-up

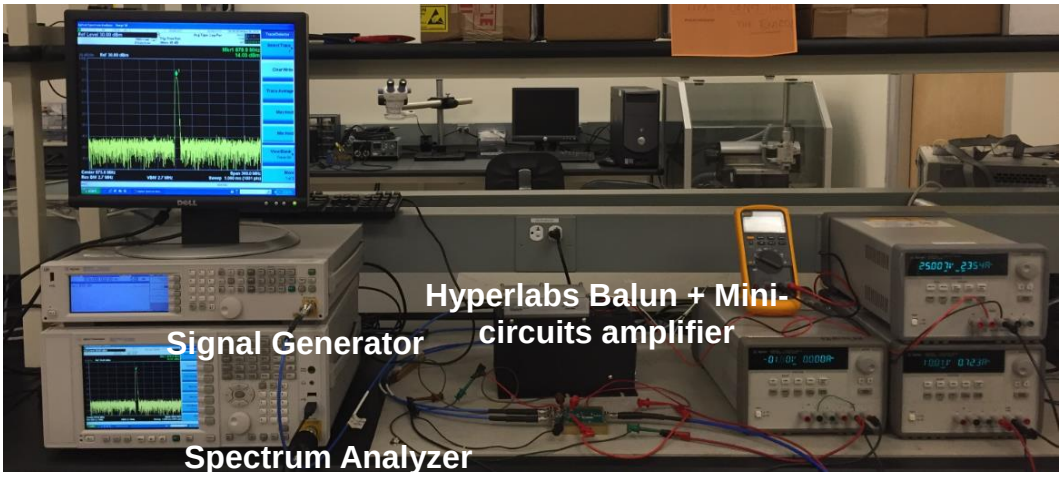
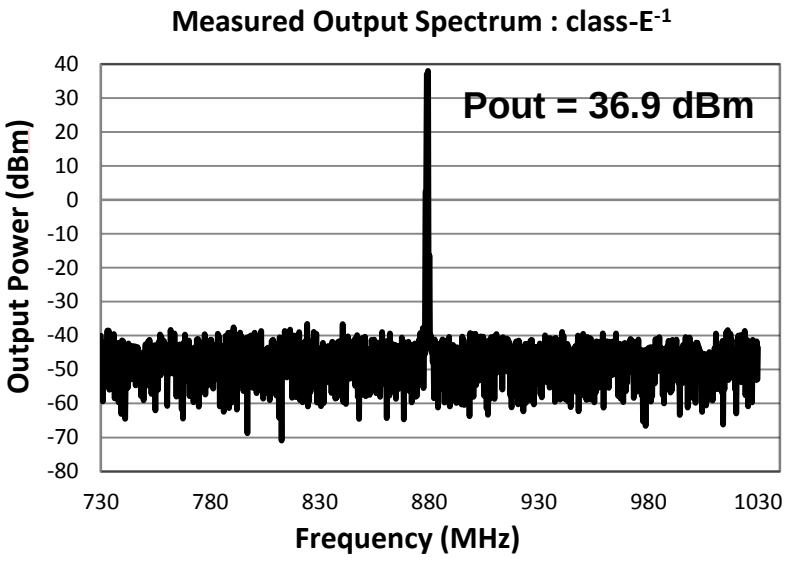


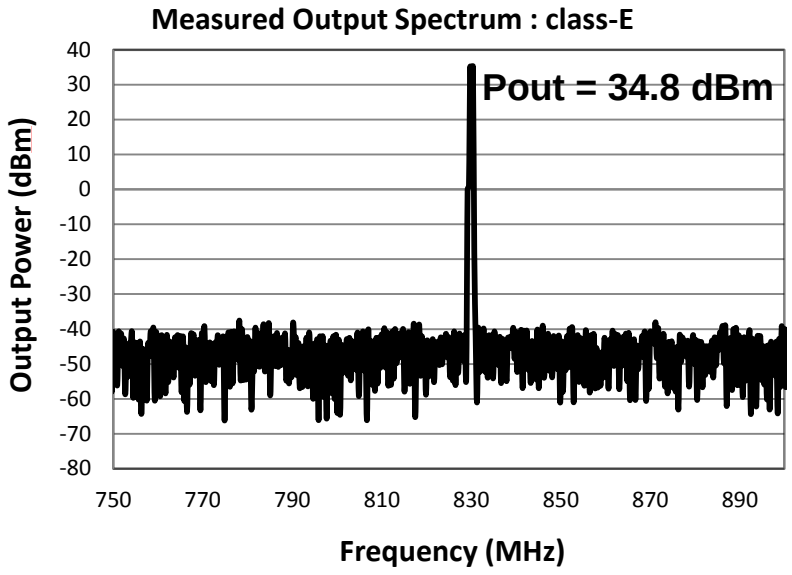
Figure 32: Lab Set-up Photo

4.3. Measurement Results

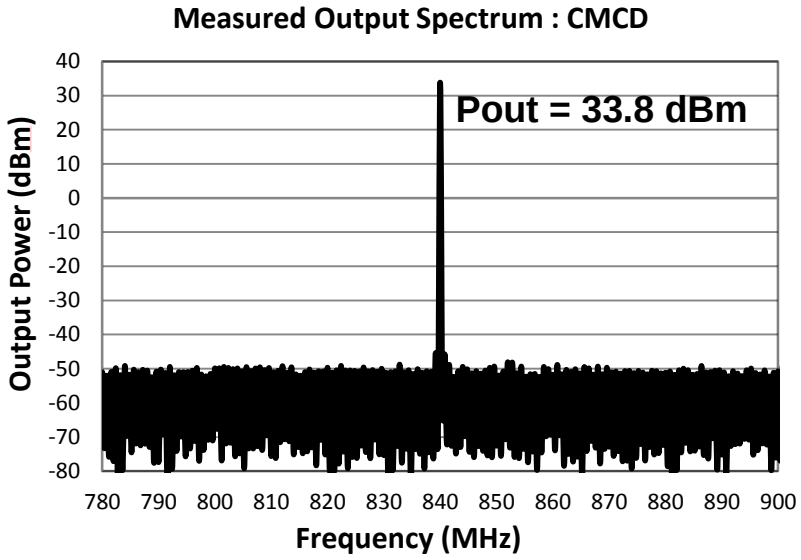
Figure 33 shows the measured output spectrum of the three power amplifiers. Output power vs frequency and drain efficiency vs frequency of the three PA topologies are shown in Figure 34. Section 4.4 analyzes the measurement results and compares it with simulation.


Measured Output Spectrum : class-E-1
Pout = 36.9 dBm
Output Power (dBm)
40
30
20
10
0
-10
-20
-30
-40
-50
-60
-70
-80
730
780
830
880
930
980
1030
Frequency (MHz)

(a)

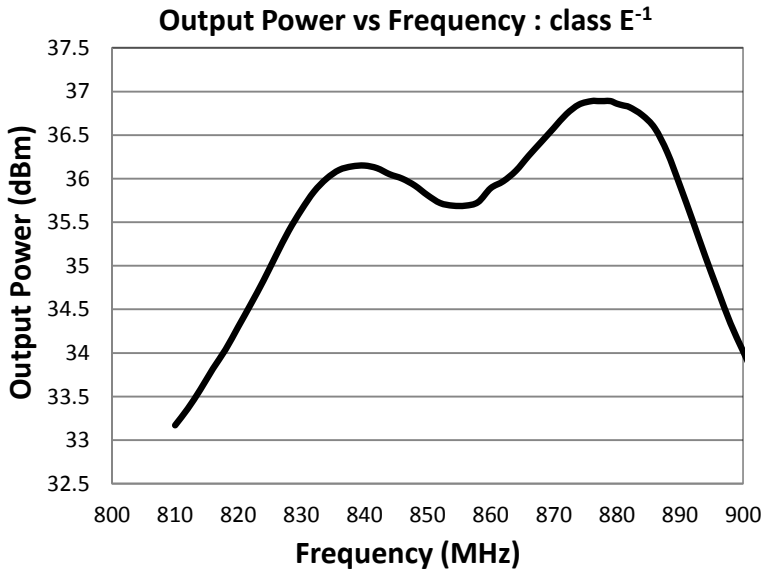

Measured Output Spectrum : class-E
Pout = 34.8 dBm
Output Power (dBm)
40
30
20
10
0
-10
-20
-30
-40
-50
-60
-70
-80
750
770
790
810
830
850
870
890
Frequency (MHz)

(b)

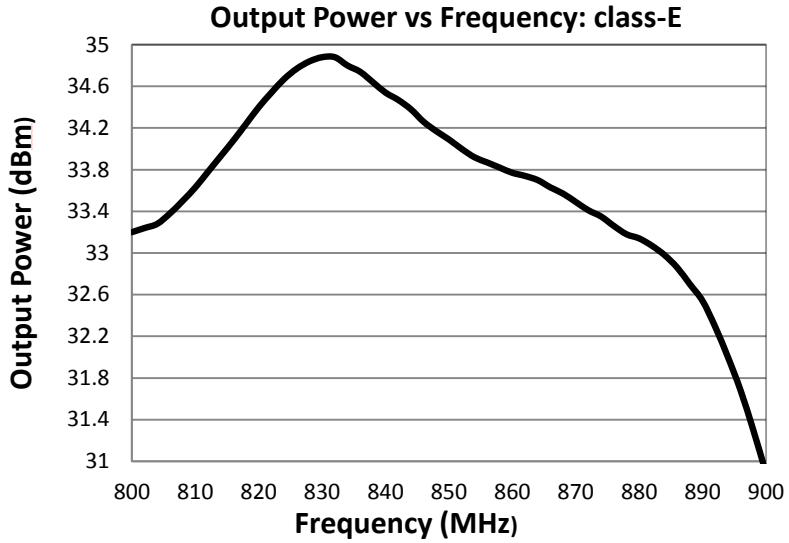


(c)

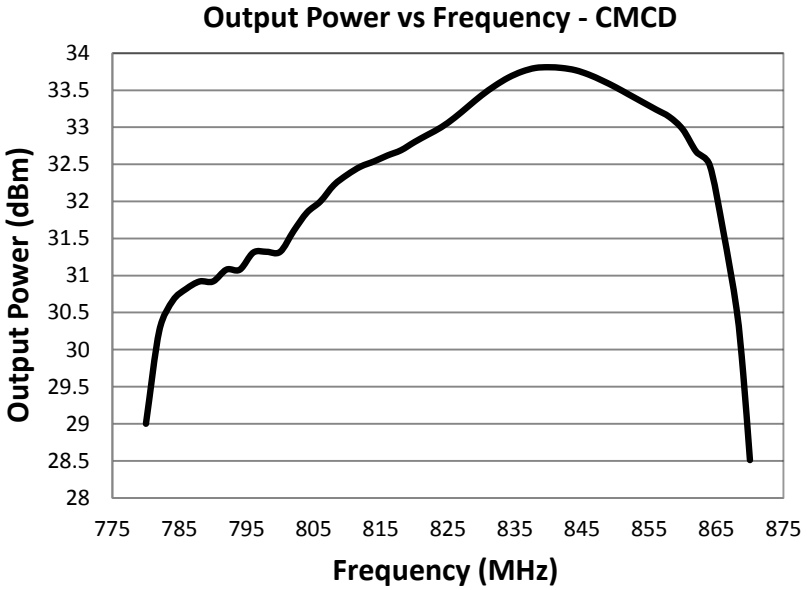
Figure 33: Measured Output Spectrum (a) Inverse push-pull Class-E (b) Push-pull Class-E (c) Current-Mode Class-D



(a)

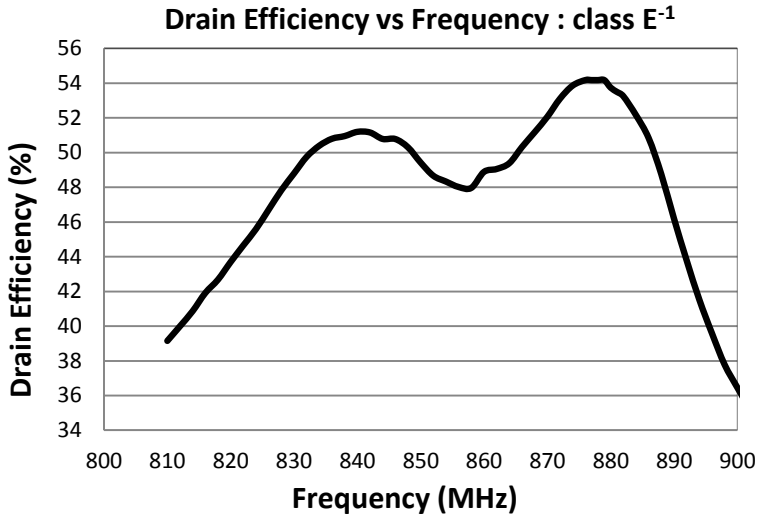


(b)

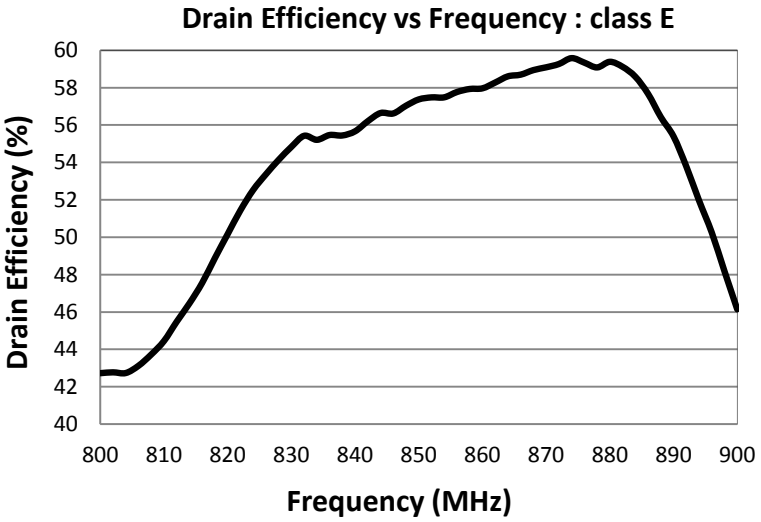


(c)

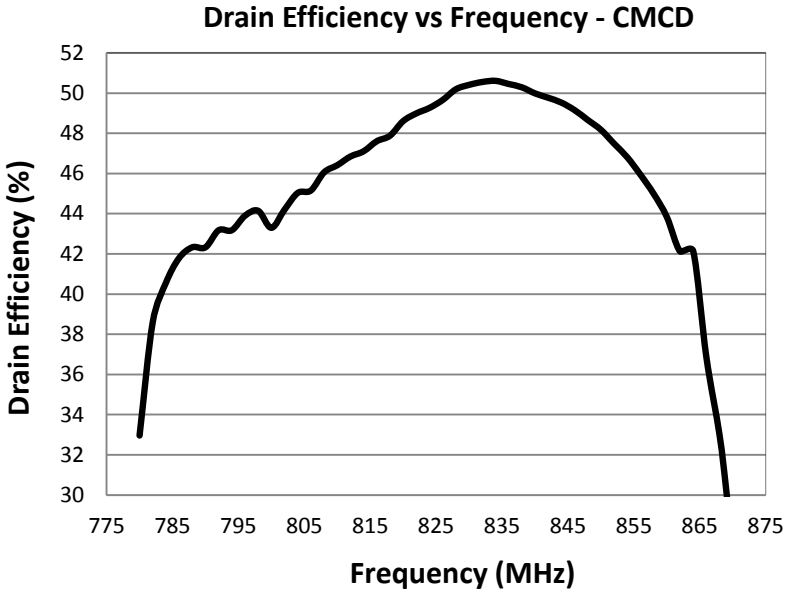
Figure 34: Measured Output Power vs Frequency (a) Inverse push-pull Class-E (b) Push-pull Class-E (c) Current-Mode Class-D


Drain Efficiency vs Frequency : class E-1
Drain Efficiency (%)
56
54
52
50
48
46
44
42
40
38
36
34
800 810 820 830 840 850 860 870 880 890 900
Frequency (MHz)

(a)


Drain Efficiency vs Frequency : class E
Drain Efficiency (%)
60
58
56
54
52
50
48
46
44
42
40
800 810 820 830 840 850 860 870 880 890 900
Frequency (MHz)

(b)



(c)

Figure 35: Measured Drain Efficiency vs Frequency (a) Inverse push-pull Class-E (b) Push-pull Class-E (c) Current-Mode Class-D

4.4. Measurement vs Simulation

Figures 34 and 35 shows that the power amplifiers drift form the designed 900MHz and gives better performance close to 880MHz for inverse push-pull class-E and push-pull class-E while at 840MHz for CMCD. The power amplifiers are fairly broadBand over 80-100 MHz range.

Table 6 shows a comparison of the measurement versus simulation results. In order to have fair comparison, the power amplifiers were driven with overdriven sine-wave by using power tone of 23dBm in simulation. 23dBm input power does not overdrive the GaN devices completely, which is shown in terms of reduced output power and efficiency as compared to Table 5 in Chapter 3. The measured output power and drain efficiencies are close to simulation results. With the provision of a high power

balun, the power amplifiers can be driven harder, close to a 50% duty cycle square wave (with 27dBm power at PA inputs). The results then are expected close to the values shown in Table 5.

PA topology	Measurement Results			Simulation Results		
	Output Power (dBm)	Output Power (W)	Drain Efficiency (%)	Output Power (dBm)	Output Power (W)	Drain Efficiency (%)
Inverse push-pull class-E	36.9	4.9	54.42	37.47	5.58	64.77
Push-pull class-E	34.8	3.02	58.1	36.19	4.16	63.08
CMCD	33.8	2.4	50.41	35.87	3.86	61.4

Table 6: Measurement vs Simulation results for overdriven sinewave input

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusions

Designing medium power SMPA systems for non-constant envelope signals is a challenging task. This work focuses on the design of the switched-mode power stage. However, for a digital transmitter, the design of the modulator and pre-driver for the main stage is equally important to achieve high overall efficiency. With the evolution of high performance GaN devices exhibiting important features like high breakdown, low parasitic, high power density, SMPAs show promise for implementation in future digital transmitter architectures. Some conclusions that can be drawn from this work are:

1. In-depth analysis of Inverse push-pull class-E, Push-pull class-E and Current-mode Class-D have been performed, and highest performance switched-mode power amplifiers have been implemented and compared with respect to duty-cycle variation in simulation.

2. The implemented SMPA topologies undergo efficiency degradation at power back-off (reduced duty cycle variation) due to violation of the ZVS or ZCS conditions in the class-E architectures. However, efficiency of these SMPAs is quite high as compared to a conventional class-D power amplifier. Even under backed-off conditions, the reduced efficiency is comparable with the maximum efficiency of single ended or VMCD PAs.

3. The inverse push-pull class-E power amplifier is a good option for GaN based discrete power amplifiers due its capability of incorporating the bondwire inductance and

its resilience to duty-cycle and component variations. This architecture is able to deliver high power at high efficiencies.

4. For systems with low parasitic series inductance, where low drain parasitic capacitance is the dominant cause of switching loss, Push-pull class-E and CMCD are good options for medium power femto cell applications.

5. For low voltage processes like CMOS, CMCD is a better candidate due to its better PUF. However, design of low loss on-chip balun is a challenge.

6. The three SMPA topologies have been implemented in GaN-on-Si and their performance match with simulation results with 50% duty-cycle input.

5.2 Future Work

1. Driving 4mm GaN devices with a square wave is a challenging task. An efficient GaN driver on a CMOS or SiGe process can help to improve the overall system efficiency.

2. Though the implemented topologies provide an alternative for non-constant envelope signals, if the ZVS condition is maintained at reduced duty cycles, then the efficiency degradation can be mitigated. This can be accomplished by varying the imaginary impedance of the ZVS/ZCS tuning network [52]. The proposed passive for this reactance modulation is a varactor [53]. Design of large dynamic range, inexpensive and small varactor can be very useful. Other techniques of modulating the drain impedance with the pulse width of input can be investigated.

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