Power Management IC for Single Solar Cell

by

# Shrikant Singh

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Approved November 2015 by the Graduate Supervisory Committee:

Sayfe Kiaei, Chair Bertan Bakkaloglu Jennifer Kitchen

ARIZONA STATE UNIVERSITY

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#### ABSTRACT

A single solar cell provides close to 0.5 V output at its maximum power point, which is very low for any electronic circuit to operate. To get rid of this problem, traditionally multiple solar cells are connected in series to get higher voltage. The disadvantage of this approach is the efficiency loss for partial shading or mismatch. Even as low as 6-7% of shading can result in more than 90% power loss. Therefore, Maximum Power Point Tracking (MPPT) at single solar cell level is the most efficient way to extract power from solar cell.

Power Management IC (MPIC) used to extract power from single solar cell, needs to start at 0.3 V input. MPPT circuitry should be implemented with minimal power and area overhead. To start the PMIC at 0.3 V, a switch capacitor charge pump is utilized as an auxiliary start up circuit for generating a regulated 1.8 V auxiliary supply from 0.3 V input. The auxiliary supply powers up a MPPT converter followed by a regulated converter. At the start up both the converters operate at 100 kHz clock with 80% duty cycle and system output voltage starts rising. When the system output crosses 2.7 V, the auxiliary start up circuit is turned off and the supply voltage for both the converters is derived from the system output itself. In steady-state condition the system output is regulated to 3.0 V.

A fully integrated analog MPPT technique is proposed to extract maximum power from the solar cell. This technique does not require Analog to Digital Converter (ADC) and Digital Signal Processor (DSP), thus reduces area and power overhead. The proposed MPPT techniques includes a switch capacitor based power sensor which senses current of boost converter without using any sense resistor. A complete system is designed which starts from 0.3 V solar cell voltage and provides regulated 3.0 V system output. To my spiritual guru H.H Sant Shri Asharam Ji Bapu for his teachings of Sanatan Dharm, which made me a better human being & to my parents

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## Chapter 1

# INTRODUCTION

# 1.1 Motivation

Solar energy is the need for future energy demand. Emerging markets for wearable medical electronics, wireless sensor node, Internet of Things (IoT) require power harnessed from the environment to eliminate the need of battery. For medium power range from few mW to few Watts photovoltaic (PV) power supply systems are frequently used. Conventional PV module consists of small solar cell connected in series due to which they suffer from inefficient power generation. In the worst case, partial shading of even around 6-7% of total surface can result in no power generation [9, 21]. Partial shading is very common in urban areas due to un-uniformed irradiation of sunlight and obstacles which can lead to a serious drawback for PV module based applications. To alleviate the problem of efficiency loss, due to partial shading series connection of single solar cells should be avoided. This implies that power should be directly processed from a single solar cell or parallel connection of such cells.

# 1.2 Challenges

Challenges involved in the design of these systems are

- Start up from an extremely low input voltage around 0.3V.
- Extract maximum power available from the solar cell.

The presented system solution is implemented to circumvent the above challenges. A switched capacitor charge pump is used as an auxiliary start up circuit; it is used only during the start up and turned off later to save power. An Inductor based Boost Switching



Figure 1.1: Use of Solar Power Management Unit.

regulator is used as a Maximum Power Point Tracking (MPPT) circuit. Since the MPPT output is unregulated voltage and most of the application needs a regulated voltage, another switching regulator is employed after MPPT to regulate the final output voltage.

# 1.3 Prior Work Limitation/Proposed MPPT

Implementation of MPPT requires to sense current and voltage to estimate the power level. Several existing solution for power management of single solar cell utilizes either lossy current sensing technique and/or high power and area consuming Analog to Digital Converter (ADC) and Digital Signal Processor (DSP) or external off-chip micro controller [5, 13]. For small sensor nodes and wearable medical electronics the area and power consumption of this implemented MPPT solution can be large. A MPPT circuit implementation utilizing a novel resistor less isolated current/power sensing is proposed in this work.

# 1.4 Thesis Organization

Keeping in mind the above constraints and challenges involved, a power management system is realized both using off the shelf component and custom designed Integrated circuit which is described in this thesis. Thesis is organized in 5 chapters. Chapter 1 gives a brief introduction of this work, emphasizes the motivation and talk about the prior work in this area. Chapter 2 covers the system overview of Power Management IC (PMIC) for single solar cell. Chapter 3 presents the novel Analog MPPT architecture. Simulation and Measurement results will be discussed in Chapter 4. Finally conclusion and possible future work is presented in Chapter 5.

## Chapter 2

# SYSTEM OVERVIEW OF PMIC FOR SINGLE SOLAR CELL

A complete system including start up, MPPT, Voltage Regulation Module (VRM), biasing, references etc. are designed in a single integrated circuit chip. The system is shown in figure 2.1



Figure 2.1: Top Level Implementation for Power Management IC for Single Solar Cell

An auxiliary switched capacitor charge pump circuit is employed to supply the system power during start-up. A Maximum Power Point Tracking (MPPT) boost converter is connected to solar cell to keep its operating voltage and current such that it is delivering maximum power. Output voltage of MPPT boost is not regulated. Since electronic circuit requires a regulated voltage, a regulation boost is employed after MPPT boost to keep final output voltage *VOUT\_REG* to a regulated predefined value. Once *VOUT\_REG* is stable, the charge pump is turned off automatically and supply for MPPT and regulation boost is provided by the voltage *VOUT\_REG*. These blocks are described in more detail in later sections and chapters.

### 2.1 Photovoltaic Cell

To design an electrical power management system for PV, it is better to understand its electrical property and electrical model. Photovoltaic cell is an electronic device which converts light into an electric energy [7]. Sun light falls on one side of PV cell and a voltage is developed across its terminal and if load is connected a current will start flowing in the load. Its simple electrical model can be represented as in figure 2.2.



Figure 2.2: Electrical Model for Photovoltaic Cell.

where

 $I_{SC}$  = Short circuit current  $V_{OC}$  = PV output current at MPPT  $I_{MPPT}$  = PV output current at MPPT  $V_{MPPT}$  = PV output voltage at MPPT  $P_{MPPT}$  = PV output voltage at MPPT

From P-V curve we can see that power attains maximum value only at one point (MPPT point) and in either direction of voltage, power start decreasing. So, it signifies that to extract maximum power from this cell, operating point must be maintained as close as possible to MPPT point.

We can see from the I-V plot that PV cell behave as constant current in one region and constant voltage in another region, these two regions intersect at point  $(V_{MPPT}, I_{MPPT})$  which is nothing but maximum power point. And the electrical characteristic equation of solar cell is as in equation (2.1)

$$\mathbf{I} = \mathbf{I}_{L} - I_{O} e^{\left[\frac{q(V+IR_{S})}{nkT}\right]} - \frac{V+IR_{S}}{R_{SH}}$$
(2.1)

Where

 $I_L$  = light generated current

 $I_0$  = dark saturation current, the diode leakage current density in the absence of light

q = absolute value of electron charge  $(1.602 \times 10^{-19} C)$ 

k= Boltzmanns Constant (1.38064852  $\times$   $10^{-23}m^2kgs^{-2}K^{-1})$ 

T = absolute temperature (K)

 $R_S$  = Series Resistance

 $R_{SH}$  = Shunt Resistance

Characteristic resistance of a solar cell is the output resistance of the solar cell at its maximum power point. Characteristic resistance of PV cell is defined as

$$R_{CH} = \frac{V_{MPPT}}{I_{MPPT}} = \frac{V_{OC}}{I_{SC}}$$

For maximum power transfer from PV cell, the load should be equal to the characteristic resistance of PV cell.



Figure 2.3: For Maximum Power Transfer Load Resistance Should be Equal to Characteristic Resistance  $(R_{CH})$ 

Since, only one load resistance value  $R_{LOAD}$  can be connected to PV cell with characteristic impedance of  $R_{CH}$  to extract maximum power, its not practical to connect any load directly with PV cell. We require some electrical interface between a load and PV output to match the load resistance with characteristic resistance. In other words, interface circuitry is needed to maintain operating condition of PV cell near to MPPT.

Interface circuit can be implemented by a switching regulator which can transform the load resistance to characteristic resistance by modulating duty cycle. This concept is represented in figure 2.4



Figure 2.4: Switching regulator as a maximum power point tracking (MPPT) block is connected between PV cell and load resistance. Duty cycle is modulated to transform the resistance

### 2.2 Auxiliary Startup Charge Pump

Single solar cell can provide less than 0.5V, which is not sufficient to operate the CMOS circuitry. A higher voltage is needed to operate the CMOS circuit. Switched capacitor charge pump are widely used in power management for boosting low input voltages to high voltage. Switched capacitor charge pump can be fully integrated inside IC due to their small form factor. For low power level switch capacitors charge pump are best choice. In literature there are many implementation of charge pumps and start up [1, 2, 4, 8, 10, 14, 17–20, 25].

A Nakagome voltage doubler charge pump topology [3, 17] is used in this research. A voltage of 0.3 V is being boosted to regulated 1.8 V. This auxiliary supply voltage is used to power auxiliary clock source, which generate clock of 100 kHz at 80% duty cycle with 1.8 V drive. This clock source will drive the power mos of the main inductor based switching

regulator. Output of switching regulator will continue to rise and being constantly monitored, once this output crosses 2.7 V, charge pump will be turned off and power for drivers and other circuitry is extracted from this same output. A Nakagome charge pump based voltage doubler is shown in figure 2.5



Figure 2.5: Nakagome Charge Pump Based Voltage Doubler

To generate 1.8V from voltage as close to 250mV at least 8 stage of voltage doubler is needed. The complete charge pump is shown in figure 2.6. A ring oscillator is used as a clock source. Charge pump output voltage regulation is achieved by gating this ring oscillator clock.



Figure 2.6: Auxiliary Switch Capacitor Charge Pump

To make this charge pump self-starting, proper sequence should be followed, as internal reference is also working on  $AUX_VOUT$ , without proper care charge pump will not start. Figure 2.7 shows the complete charge pump with internal band-gap voltage reference & power on reset (POR).

 $AUX\_VOUT$  is used to generate clock with voltage levels of 1.8V, also the frequency of this clock is roughly 100 KHz at duty cycle of around 80%.

Calculating Frequency of Auxiliary Clock

 $F_{CLK-AUX} = \frac{1}{6(T_{INV}+T_{RC})}$  Calculating Duty Cycle of Auxiliary Clock  $D_{CLK-AUX} = \frac{T_{INV}}{6(T_{INV}+T_{RC})}$ 

At typical corner  $T_{INV}$  and  $T_{RC}$  are chosen such that  $F_{CLK-AUX}$  is close to 100 KHz and  $D_{CLK-AUX} = 0.8$ . High duty cycle will ensure that two boost connected in series will



Figure 2.7: Auxiliary Switch Capacitor Charge Pump with Bandgap & Startup



Figure 2.8: Clock Generator Running Off Auxiliary Supply of 1.8V, Driving Both the Boost Converter with 100 KHz Clock With 80% Duty Cycle

boost voltage as low as 0.3V to 3V. On resistance of power NMOS is,  $Ron_NMOS = 718\Omega$  for  $W/L = 1000\mu/180n$ 

### 2.3 Boost Converter

Switching Regulator is inevitably used in power management circuit due to their superior efficiency performance compared to linear regulator [6]. In principle, switching regulator dissipate less power as compared to linear regulator, where as major power is dissipated across the pass device. More over as against linear converters switching regulators can even boost, invert or isolate the input voltage. In this research Boost switching regulator is used for boosting low input voltage of PV cell. Two boost converters are employed, one is for implementing MPPT and the other one is for providing the regulated output voltage. In this section we will describe the boost converter operating principle. Figure 2.9 shows the basic boost Converter with ideal switches



Figure 2.9: Ideal Boost Converter

 $V_g$  is a DC voltage source connected to the network of switches, capacitor and inductor. As no lossy component is present in power path, like in a linear regulator. Ideally, this ideal boost converter can process power with 100% efficiency. Duty Cycle D is defined as ,  $D=\frac{T_{ON}}{T_{SW}}$  &  $0\leq D\leq 1$ 

Complement D' = 1 - D

# **Boost Analysis**

# Sub-interval 1:

The equivalent circuit when switch S1 is close is shown in figure 2.10



Figure 2.10: Boost Configuration when Switch S1 is Closed

Inductor Voltage  $V_L(t) = V_g$ 

Once the inductor voltage is known, Inductor current can be found using

 $V_{L}(t) = L \frac{di_L(t)}{dt}$ 

The inductor charges with a constant slope of  $V_g/L$ 

# Sub interval 2:

The equivalent circuit when switch S2 is close is shown in figure 2.11



Figure 2.11: Boost Configuration when Switch S2 is Closed

Inductor voltage  $V_L = V_g - v(t)$ 

Applying small ripple approximation  $V_L(t) = V_g - V$ 

Once the inductor voltage is known, Inductor current can again be found

Using  $V_L(t) = L \frac{di_L(t)}{dt}$ Solve for the slope:  $\frac{di_L(t)}{dt} = \frac{V_L(t)}{L} = \frac{V_g - V}{L}$ 

The inductor current charges with a constant slope Inductor voltage & current waveform are shown in figure 2.12



Figure 2.12: Boost Inductor Voltage & Current Waveform

Change in IL = slope × length of sub – interval  $2\Delta I_L = \frac{V_g}{L}DT_s$  $\Delta I_L = \frac{V_g}{2L}DT_s$ 

$$\Delta L = \frac{V_g}{2\Delta I_L} DT_s$$

Voltage Conversion Ratio

Applying volt-sec balance to inductor over one period

$$\int_0^{T_s} V_L(t)dt = V_g DT_s + (Vg - V)D'T_s$$
$$V_g(D + D') - V.D' = 0$$

Solving for V, we will get

$$V = \frac{V_g}{D'}$$

Voltage Conversion Ratio is therefore



Figure 2.13: Voltage Conversion Ratio as a Function of Duty Cycle D for an Ideal Boost Converter

Applying capacitor charge balance

$$\begin{split} \int_{0}^{T_{s}} I_{c}(t) dt &= (-\frac{V}{R}) DT_{s} + (1 - \frac{V}{R}) D'T_{s} \\ -\frac{V}{R} (D + D') + ID' &= 0 \ I = \frac{V}{D'R} \ I = \frac{V_{g}}{D'^{2}R} \end{split}$$

Capacitor voltage ripple



Figure 2.14: Output Voltage Ripple

Capacitor voltage slope during interval 1:

$$\frac{dV_c}{dt} = \frac{I_c(t))}{C} = -\frac{V}{RC}$$

Capacitor voltage slope during subinterval 2:

$$\frac{dV_c}{dt} = \frac{I_c(t))}{C} = \frac{I}{C} - \frac{V}{RC}$$
$$-2\Delta V = -\frac{V}{RC}DT_s$$

Solving for for peak ripple, we get

$$\Delta V = -\frac{V}{2RC}DT_s$$

# 2.4 Synchronous Switch Drivers

Top switch in boost type switching regulator is normally implemented by diode. If diode is employed it will reduce the efficiency and insert a forward biased diode drop. if mos-switch is used instead of diode, it can alleviate the above mentioned problems. But mos-switch needs a drive signal between its gate and source. For grounded mos switch, at bottom it is straight forward to apply a driving signal as source is connected to ground. But in top switch as source is floating, a floating drive signal is to be generated. This kind of driving topology is called Synchronous drivers. Synchronous drivers improve the efficiency and decrease the forward voltage drop, which would have been present if passive switch diode is used. Synchronous driver involve more complexity in circuit design. A traditional synchronous driver is shown in figure 2.15



Figure 2.15: Synchronous Drivers for Boost Converter

Level shifter is required to shift the ground referred drive signal to a floating drive signal. Level shifter used in this design is taken from figure 5 in [16] which is shown in figure 2.16 here. Other drivers technique which can be used is presented in [26]

If top & bottom switches are closed together, a substantial energy will be lost. Therefore normally they are operated from non-overlapping clock generator to get rid of any loss. The non-overlapping clock generator is shown in figure. The dead time between these clock phases is adjusted to have minimum switching loss, in this research this dead time is kept fixed and can be trimmed through trim bits. More advance driver utilizing adaptive or predictive delay control can be used /citejing2010soft,musunuri2005improvement.

A significant power is also wasted in shoot through current of the drivers, to alleviate this problem even final buffer nmos & pmos are operated from non-overlapped signals. Figure shows the final buffer stage for driving power mos 2.18



Figure 2.16: Level Shifter Used in Synchronous Driver to Generate Floating Clock Driver



Figure 2.17: Non Overlapping Clock Generator for Driving Top & Bottom Switch

# 2.5 Voltage Regulation Boost

Almost all of the electronic circuit requires regulated supply. There exist several ways to achieve voltage regulation. In this section we will discuss the control method for switching regulator. There can be voltage mode, current mode or hysteric regulator each one of them has advantages and disadvantages over the other [11, 12]. These methods are briefly explained here.



Figure 2.18: Last Stage of The Driver

### 2.5.1 Voltage Mode Control

Output voltage is feedback to an error amplifier which generates error voltage to generate proper control signal for boost converter.

$$\begin{split} \frac{\hat{v_o}}{\hat{d}} &= \frac{V_g}{(1-D)^2} \frac{(1+sCR_c)(1-\frac{sL_e}{R_LOAD})}{1+\frac{s}{\omega_0Q}+\frac{s^2}{\omega_0^2}}\\ \omega_0 &= \frac{1}{\sqrt{(L_eC)}}\\ L_e &= \frac{L}{D'^2}\\ \omega_0 Q &= \frac{R_{LOAD}}{L_e} \end{split}$$

Boost converter adds a new complexity to the stability problem, it has an RHP zero. A type III compensator is needed to design the loop for voltage-mode boost converter operating in CCM. The phase boost of this type of compensator is very helpful to offset the sharp phase drop that occurs after the resonant frequency of the power stage of boost converter. RHP zero has additional constraints on the design of the loop compensation & crossover frequency, but they can be managed well as long as the RHP zero frequency is understood and placed properly by appropriate power stage component selection. The



Figure 2.19: Typical Voltage Mode Controlled Boost Converter

usual way to deal with RHP zero is to pushing it out to higher frequency. A typical voltage mode controlled boost converter is shown in figure 2.20



Figure 2.20: Typical Voltage Mode Controlled Boost Converter With Compensator

#### 2.5.2 Current Mode Control

In this technique, the peak current in the power switch or inductor is sensed, and switch is turned off at a programmed level of current. There is in effect a fast acting inner current loop along with the outer (slower) voltage loop which carries out the output regulation.



Figure 2.21: Current Mode Control

#### 2.5.3 Hysteric Control

A PWM comparator works is by creating ON-OFF pulses from the intersection of two voltage profiles at its input terminals: one steady voltage level (the control voltage), and the another sawtooth voltage profile. If we directly apply the reference voltage as a smooth voltage level instead of the error voltage on the other terminal, and use a sawtooth based on inductor current (as in Current Mode), it will become a Hysteric control. Its transient response is excellent. Drawback of this approach is that frequency of operation is not constant, for EMI sensitive application it is desirable to have minimal frequency variation.



Figure 2.22: Hysteric Mode Control

### 2.6 Quasi Fixed Frequency Constant on Time (COT) Control

For CCM boost converter, RHP zero complicates the compensator design. Hysteric control can be used as it is simpler and fastest, but its implementation generally increases system cost and decrease efficiency. Also, in traditional hysteric control switching frequency is not constant. To overcome the above limitation a Quasi Fixed Frequency Constant on Time (COT) Control is used from [23, 24], which is very simple and effective. The on time of the boost switch is pre-determined by an on-time generator corresponding to the requirement of fixed frequency operation, and the boost switch off time is modulated in the traditional hysteric way. Also pulse frequency modulation (PFM) comes free at light load, which improves the light load efficiency compared with traditional PWM control.

The block diagram of the COT boost converter is shown in figure 2.23. The control scheme is based on a comparator and two single-shot timers.

The key system waveforms are shown in the figure 2.24, it shows that how off time is determined by the voltage regulation requirement and ON time is fixed.

If on time  $T_{ON}$  is fixed constant value, frequency will change, to keep frequency constant either a Phase Locked Loop (PLL) can be used, which compare the system frequency with a reference frequency and correct the system frequency if it deviates from its specified



Figure 2.23: Operating Principal of The Quasi Fixed Frequency Constant On Time Controlled Boost converter



Figure 2.24: Quasi Fixed Frequency Constant on Time Controlled Boost Converter Waveform in CCM Operation

value. However, the additional PLL makes the controller structure complex and increase the chip area. Furthermore, once there is a voltage step at the input, a loop response time is needed to adjust the on-timer to generate the new value. Another way to make frequency constant is to sense the input & output voltage and then to calculate the corresponding Ton directly, this circuit is shown in figure 2.25

$$\frac{V_o}{V_g} = \frac{1}{1-D} = \frac{1}{1-\frac{T_{ON}}{T_S}}$$
$$T_{ON} = T_S \frac{V_o - V_g}{V_o}$$



Figure 2.25: Quasi Fixed Frequency Constant on Time Controller Logic Implementation

Analyzing the circuit we get

$$\frac{VoREF}{R} * \frac{T_{ON}}{C} = \frac{VoREF - VIN}{K}$$
$$T_{ON} = \frac{RC}{K} * \frac{VoREF - VIN}{VoREF}$$

Which implies that calculated  $T_S = \frac{RC}{K}$ 

In voltage mode and current mode controlled power converter, the accuracy of the output voltage is always improved by introducing a low frequency pole in the control loop. Thus the DC error will be integrated to produce a large control signal for close loop correction. In hysteric control, there is no integrator in the feedback loop. A outer voltage loop is added, a low frequency pole introduce by gm amplifier and the compensation capacitor Cc can be at low frequency. This outer loop will improve the steady state accuracy. The complete control scheme is shown in figure 2.26



Figure 2.26: Complete COT System with Improved DC Accuracy

# 2.7 Reference Bias & Control Blocks

Voltage and current reference circuit are essential in almost all the analog and mixed signal ICs. Desired bias current/voltage should be constant across process, supply & temperature (PVT) variations. Required accuracy of these reference depends on the application at hand like in high precision data converter reference should also be very accurate. In this section bandgap voltage reference, Current bias generator, Power-On-Reset (POR) circuits will be discussed.

# 2.7.1 Bandgap Voltage Reference

Bandgap reference generates a constant voltage across PVT. It basic principle is based on adding two source having opposite polarity temperature coefficient in proportion to get a voltage with zero temperature coefficient.

$$VBE_1 = V_T ln(\frac{I_1}{I_S}) VBE_1 = V_T ln(\frac{I_2}{I_S})$$

 $V_{BE}$  is Negative to Absolute Temperature (NTAT)

$$\Delta VBE = VBE_1 - VBE_2 = V_T ln(\frac{I_1}{I_S})$$

As there are N diodes

$$I_2 = I_1/N$$

$$\Delta VBE = VBE_1 - VBE_2 = V_T ln(\frac{I_1}{I_S})$$

# $\Delta V_{BE}$ is Proportional to Absolute Temperature (PTAT)

$$VBG = VBE_3 + \frac{R_2}{R_1} \Delta VBE$$
$$\frac{\partial VBG}{\partial T} = 0$$
$$\frac{\partial VBG}{\partial T} = \frac{\partial VBE_3}{\partial T} + \frac{R_2}{R_1} * \frac{\partial \Delta VBE}{\partial T} = 0$$
$$\frac{R_2}{R_1} = -\frac{T_{CO} \cdot VB3}{T_{CO} \cdot \Delta VBE}$$



Figure 2.27: Bandgap Voltage Reference Circuit



Figure 2.28: Power on Reset Timings

2.7.2 Power on Reset (POR)

Power-on-reset (POR) circuit is required by all the system which have memory element like flip flop which needs to be initialized to a known value. POR signal ensure a proper initialization of system after supply is up. Figure 2.28 shows the POR signal as a result of supply.

# 2.7.3 Current Bias Circuit

Voltage to current (V2I) circuit is used to generate reference current needed in the IC. The following figure 2.29 shows the V2I architecture.



[!htb]

Figure 2.29: Voltage to Current Converter Used to Generate Current Biasing

# 2.7.4 Low Dropout Regulator (LDO)

For sensitive analog circuit clean supply is desirable. Switching regulator supply has voltage ripple which can cause performance degradation of sensitive analog circuitry. Power Sensor in MPPT circuit and other control circuit require stable and clean supply, for this purpose an on chip low dropout regulator (LDO) is used. A traditional PMOS type LDO is designed which is shown in the figure. In normal condition this LDO will have input of 3.0V and its output will be regulated to 1.8V.



Figure 2.30: Low Dropout Regulator (LDO)

# Chapter 3

# MAXIMUM POWER POINT TRACKING

Maximum power point tracking as explained in earlier chapter is required to harness maximum power from the PV cell. In this section detailed design and analysis of the proposed MPPT block will be covered.



Figure 3.1: MPPT Implementation by Boost Type Switching Regulator

MPPT is achieved by boost type switching regulator. To calculate power output voltage and output current needs to be sensed and multiplied together. Perturb & Observe algorithm is used for MPPT [21].

Figure 3.2 shows that power as a function of boost control duty cycle. We can see that maximum power occurs only at one particular duty cycle. The flow chart for P&O algorithm is shown in figure 3.3. Output of Boost converter is sensed and based on the increment & decrement of power values, duty cycle D is modulated to reach the maximum power point.



Figure 3.2: Power-Duty Characteristic of Boost Output Connected to PV Cell



Figure 3.3: Perturb & Observe (P&O) Algorithm for Maximum Power Point Tracking

## Chapter 4

### SIMULATION AND MEASUREMENT RESULTS

A test IC is designed in 180nm technology node with 6 metal layers. This PDK has 1.8V, 5.5V, 20V transistors required for the system design. Low threshold transistors (LVT/N-VT/ZVT) were not present in this PDK, which would have been ideal for start-up design from 0.3V.

# 4.1 IC Layout

Complete system layout is present in figure 4.1. Dimension of IC is 2.450mmX2.700mmi.e total area is  $(6.615mm^2)$ .

### 4.2 Test Board Design

A PCB is designed to test the IC is shown in figure 4.3. PCB is a 2 layer board having a dimension of  $8inches \times 6inches$  & uses FR-4 material. Necessary test modes and probing points were added on PCB for ease in debugging. Provision for external Reference voltage, external supply, and external clock is also included in the PCB.

#### 4.3 Measurement Setup

Measurement setup is shown in figure 4.4 with all the major instruments shown. Test DC voltage is provided by Agilent E3631A DC power supplies. External Clock to IC for debugging process, is provided by HP 33120A Function Generator. Mixed Signal Oscilloscope MSO-X 2024A is used for monitoring waveform. A solar cell is soldered on PCB, for providing irradiation to this cell; a light source with intensity control is utilized. Keithely 2100  $6\frac{1}{2}$ digit multimeter is used for DC voltage measurement. Tekpower 3710A DC



Figure 4.1: IC Layout of the System

electronic load is used for load characteristic.

# 4.3.1 Auxiliary Start-up Charge Pump Measurement Results

Measurement shows the self-start-up functionality of designed auxiliary charge pump. Charge pump is functional with 0.45V and will continue to function till 0.33V. As a debugging step, charge pump is operated by external clock of 10 KHz and it has been observed that charge pump is functional from as low as 0.3V.

Boost output node voltage = 1.4 V. Internally generated 1.8 V drive, 100 KHz 83.33% Duty Cycle is operating this boost.



Figure 4.2: Die Micrograph

# 4.3.2 Measurement of Internal LDO, Bias Voltage and Current Generation

# 4.3.3 MPPT Result

Voltage to Time Converter (VTC) serves as important block for power sensor. It is providing clock to switch converter power sensor. Figure shows the measured result for VTC. In figure characteristic of VTC is shown, with gain error of 11.14% it follows the ideal characteristics.

Finally in figure simulated result of MPPT functionality is shown, MPPT loop is locked to require to duty cycle to operate connected solar cell.



Figure 4.3: Designed Printed Circuit Board (PCB) for Testing the IC



Figure 4.4: Setup for Test & Measurement



Figure 4.5: Startup Charge Pump is Starting up from 0.45V



Figure 4.6: Startup Charge Pump Starting up from 0.3V with External Clock

# 4.3.4 Voltage Regulation Module

Simulation result for Voltage Regulation Module is shown in figure. Input voltage is varied from 0.5V to 2.5V, it can be seen that output is regulated to 3.0V.



Figure 4.7: First Boost (MPPT) is Generating 1.4 V from 0.3 V when Driven from Startup Circuitry. Drive Signal has 1.8 V Drive @100 KHz with 83.33% Duty Cycle



Figure 4.8: Switching Node & Bootstrapped Level Shifted Node Switching Node Profile



Figure 4.9: Top Level Supply Monitoring Plot Shows that Startup is Activated whenever Output Voltage Falls Below 2.7V



Figure 4.10: Zoomed in Version of Above Plot



Figure 4.11: Internal LDO, Bandgap Reference and Voltage to Current (V2I) Outputs



Figure 4.12: Switch Capacitor Differentiators is Used Only Once in One MPPT Cycle. It is Kept Turned Off to Save Power

S.No	Voltage (mV)	Measured Time (ns)	Ideal Time (ns)
1	50	37.4	50
2	100	90.4	100
3	150	132	150
4	200	172	200
5	250	221	250
6	300	265	300
7	350	306	350
8	400	353	400
9	450	395	450
10	500	444	500
11	550	488	550
12	600	534	600
13	650	582	650
14	700	622	700

Table 4.1: Voltage to Time Converter Measurement Results



Figure 4.13: Voltage to Time Converter (VTC) Output for Input Control Voltage of 400mV, Output Clock of Time Period T=358 ns



Figure 4.14: Voltage to Time Converter Transfer Characteristic



Figure 4.15: Simulation of MPPT Control Showing Duty Cycle is Locked to Required Value to Maintain MPPT



Figure 4.16: Simulation of the Voltage Regulation Module (VRM). Output is Regulated to 3V, with Input Variations from 0.5 to 2.5V

### Chapter 5

### CONCLUSION AND FUTURE WORK

This thesis has demonstrated the design of a power management IC for extracting maximum power from a single solar cell. Main challenges are start up of PMIC at 0.3 V and efficiently extract power. The PMIC works in two phases. At start up phase, a switch capacitor charge pump based auxiliary power source generates a regulated 1.8 V to power up MPPT and regulation converters. In steady state the auxiliary power source is turned off and converters generates regulated 3.0 V system output voltage. In start up phase, both MPPT and regulation boost converters works at 100 kHz with fixed duty cycle of 80% which eventually generate 3V at the final output of the system, once this output crosses 2.7V, auxiliary start up circuit is turned off to save power and the control circuitry for converters is deriving its power from the system output.

Measurement results show that this PMIC starts from 0.3 V input with external clock. With internal clock, minimum start up voltage is observed to be 0.45 V and is functional till 0.33V. Measured results shows that if system output falls below 2.7 V, auxiliary start up circuit will turn on again. Simulation result of MPPT circuit shows that converter is locked to the desired duty cycle. Voltage regulation module simulation result shows functionality for input voltage variation from 0.5 V to 2.5 V.

Future work can be done to make start up circuit more compact using either resonant based start up circuit or other advance charge pump technique to boost 0.3 V to higher voltage using considerably less silicon area. MPPT implementation can be done with adaptive duty cycle so that initially MPPT can work with larger duty cycle steps and once it reaches MPPT, step size can be reduced. This will minimize limit cycle oscillation at maximum power point, which is inherent in perturb and observe algorithm. A better algorithm instead of P&O algorithm can be used for MPPT. Voltage regulation module can be eliminated, if regulation functionality can be integrated in this MPPT boost converter. This will improve the overall system efficiency.

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