Solar Micro Inverter Modeling and Reliability

by

Arkanatha Sastry Manchanahalli Ranganatha

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science

Approved October 2015 by the
Graduate Supervisory Committee:

Raja Ayyanar, Chair
George Karady
Jiangchao Qin

ARIZONA STATE UNIVERSITY

December 2015

ABSTRACT

The demand for cleaner energy technology is increasing very rapidly. Hence it is important to increase the efficiency and reliability of this emerging clean energy technologies. This thesis focuses on modeling and reliability of solar micro inverters. In order to make photovoltaics (PV) cost competitive with traditional energy sources, the economies of scale have been guiding inverter design in two directions: large, centralized, utility-scale (∼500 kW) inverters vs. small, modular, module level (∼300 W) power electronics (MLPE). MLPE, such as microinverters and DC power optimizers, offer advantages in safety, system operations and maintenance, energy yield, and component lifetime due to their smaller size, lower power handling requirements, and module-level power point tracking and monitoring capability [1]. However, they suffer from two main disadvantages: first, depending on array topology (especially the proximity to the PV module), they can be subjected to more extreme environments (i.e. temperature cycling) during the day, resulting in a negative impact to reliability; second, since solar installations can have tens of thousands to millions of modules (and as many MLPE units), it may be difficult or impossible to track and repair units as they go out of service. Therefore identifying the weak links in this system is of critical importance to develop more reliable micro inverters.

While an overwhelming majority of time and research has focused on PV module efficiency and reliability, these issues have been largely ignored for the balance of system components. As a relatively nascent industry, the PV power electronics industry does not have the extensive, standardized reliability design and testing procedures that exist in the module industry or other more mature power electronics industries (e.g. automotive). To do so, the critical components which are at risk and their impact on the system performance has to be studied. This thesis identifies and addresses some of the issues related to reliability of solar micro inverters.

This thesis presents detailed discussions on various components of solar micro inverter and their design. A micro inverter with very similar electrical specifications in comparison with commercial micro inverter is modeled in detail and verified. Components in various stages of micro inverter are listed and their typical failure mechanisms are reviewed. A detailed FMEA is conducted for a typical micro inverter to identify the weak links of the system. Based on the S, O and D metrics, risk priority number (RPN) is calculated to list the critical at-risk components. Degradation of DC bus capacitor is identified as one the failure mechanism and the degradation model is built to study its effect on the system performance. The system is tested for surge immunity using standard ring and combinational surge waveforms as per IEEE 62.41 and IEC 61000-4-5 standards. All the simulation presented in this thesis is performed using PLECS simulation software.

DEDICATION

Dedicated to my beloved grandparents, my uncle Satyanarayana M V, aunt Nagaratna and my parents Geetha and Ranganatha M V for all their sacrifices and efforts towards the welfare of our family and making me what I am today. They are great source of inspiration to me.

ACKNOWLEDGMENTS

Firstly I thank almighty for showering her blessings on me, without which I could not have accomplished this.

I owe a great debt of gratitude to my advisor, Prof. Raja Ayyanar for giving me a chance to work in his lab under his guidance. My deepest regards to him for introducing me to advanced power electronics and renewable energy systems. I wholeheartedly thank him for his constant support throughout.

I would like to thank Prof. George Karady and Prof. Jiangchao Qin for being members of my thesis committee.

My sincere thanks to all other professors at Arizona State University whose courses gave me good technical foundation to carry out this research work. I would also thank Nina Millmyn, and my graduate advisor, Toni Mengert for their support.

I thank Jack Flicker of Sandia National Laboratory and Prof. Govindsamy Tamizhmani of TUV PTL, for sharing their knowledge and providing valuable suggestions throughout the project.

I thank my lab colleagues Siddharth Kulasekaran, Jinia Roy, Tong Yao, Chenhao Nan, Ziwei Yu, Yinglai Xia, VSS Pavan Kumar Hari, Robert Mongrain (Scott) for your immense support and help. I have thoroughly enjoyed your company for all these days. I specially thank Siddharth, Jinia and Tong for their invaluable support during coursework and research.

My special thanks to Gurudatta Belavadi, Mr. & Mrs. Balakrishna, Manjusha Hari, Suhas Kashyap, Nikhil Pai, Adarsh and Sandeep for their priceless support especially whenever it was needed. I am deeply indebted to you all.

Finally, I thank my parents Mr. Ranganatha and Mrs. Geetha, my lovely sister Akhila, brother-in-law Dr. Chandrashekar for their unconditional love, support and constant encouragement. I also thank Supreetha, Achyutha, Anantha and my entire family for their support. I badly miss my grandparents and my well wishers Lt. Kalyani Nagaraj and Lt. Kamala Krishnachar. Nonetheless, their blessings are with me. I am really grateful to you all.

TABLE OF CONTENTS

CHAPTER Page

CHAPTER Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

Chapter 1

INTRODUCTION

There has been tremendous improvements to efficiency and affordability of renewable technologies in the recent years. This in conjunction with rapidly rising awareness of the ill effects of carbon emissions and green houses gases has resulted in creation of government policies and incentives for power generation using renewable resources. It also helps in achieving renewable portfolio requirements for each states. They range from financing, rebates and tax incentives to consumers. These measures have helped implement and improve sustainable energy.

1.1 Past, present and future of energy

In this technology driven era of the world, the need for reliable, affordable, continuous and high quality energy is ever increasing. The global energy consumption is projected to increase by 37% between 2013 and 2035, with average growth of 1.4% p.a. and some of the main factors being increasing population and rapid growth of countries such as India and China [2]. The forecasts of energy production of different regions of the world is depicted in Figure 1.1. Energy plays a major role in the economic growth of any country. At present, the largest contributors of energy generation are fossil fuel sources. However, coal and crude oil are limited resources and are rapidly depleting and hence the reliance on them has to be reduced.

This has led to placing huge emphasis on the development and implementation of renewable energy sources in the electricity generation mix. The graph in Figure 1.2 shows the global trends in renewable energy installed capacity. The utilization of solar energy has rapidly increased over the recent years. A great number of policies and initiatives are being enacted by governments to implement renewable and sustainable

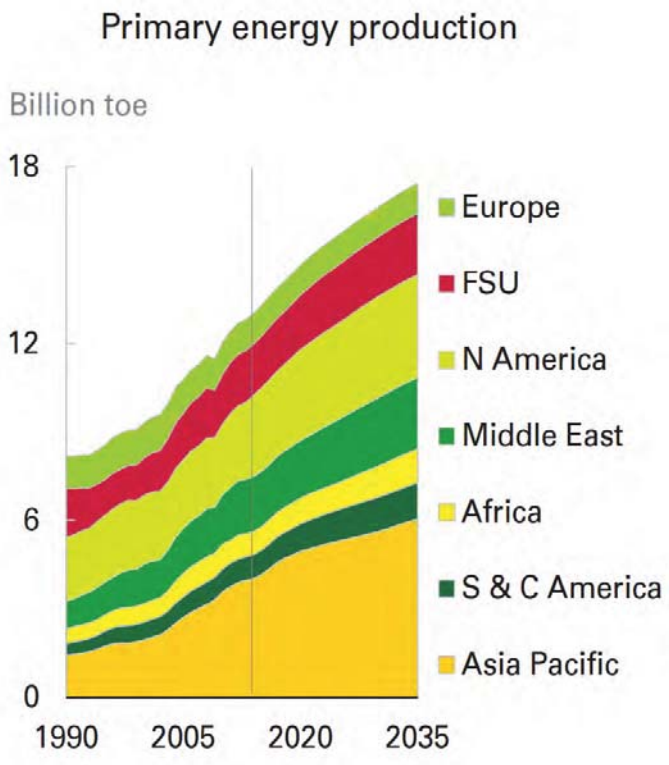


Figure 1.1 – Forecast of energy production of different region [2]

energy production. One such instance is the renewable production portfolios, which is a regulatory mandate to increase renewable energy production and have it account for a larger part of the energy production mix [3]. Solar energy is the cleanest, most abundant renewable energy source and has tremendous potential to supply all global energy demand. This is illustrated in the following example - if just 0.16% of the land on Earth is covered with 10% efficient solar conversion systems, it would provide 20 TW of power, nearly twice the worlds consumption rate of fossil energy and while producing no carbon emissions [4]. Some popular solar energy technologies are solar thermal and photovoltaic systems.

Photovoltaic (PV) is the most widely used technology to harvest solar energy. PV systems make use of solar panels to capture the energy and power electronic systems to perform the required power level conversions. Historically, the biggest disadvantage against PV systems are its low efficiency and high cost. Though operating and fuel

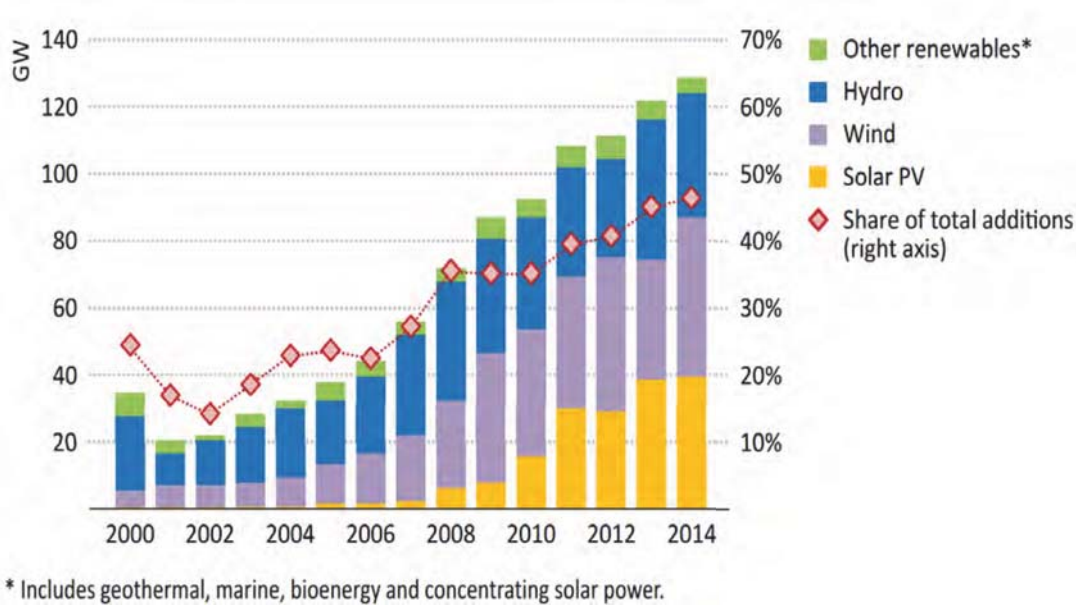


Figure 1.2 – Global renewable based power capacity addition by type [3]

costs for PV is less, capital cost is very high which raises the overall price of electricity. This has been one of the deterrents for investing in PV for a long time. But this trend is changing, and it has actually been observed that the overall cost, i.e the levelized cost of energy (LCOE) works out cheaper than conventional electricity pricing, as depicted in Figure 1.3 [4]. This reduction in LCOE can be attributed to the great leaps in PV technology in the recent years, like increased efficiency and reduced manufacturing costs of solar cells and associated power electronics.

PV systems are being implemented extensively around the world, from large grid connected solar farms to smaller household rooftop installations. This is forecasted to increase much further, and photovoltaic solar energy generation is expected to account for 16% of the total generation as illustrated in Figure 1.4 [5].

1.2 Introduction to PV systems

The PV cell produces DC power which by itself cannot be used or fed to the grid. The cells are connected in series like a string so as to obtain larger output voltage and in larger systems, such strings are further connected in parallel. There are complex power electronics systems connected to the PV cells for the required power and voltage

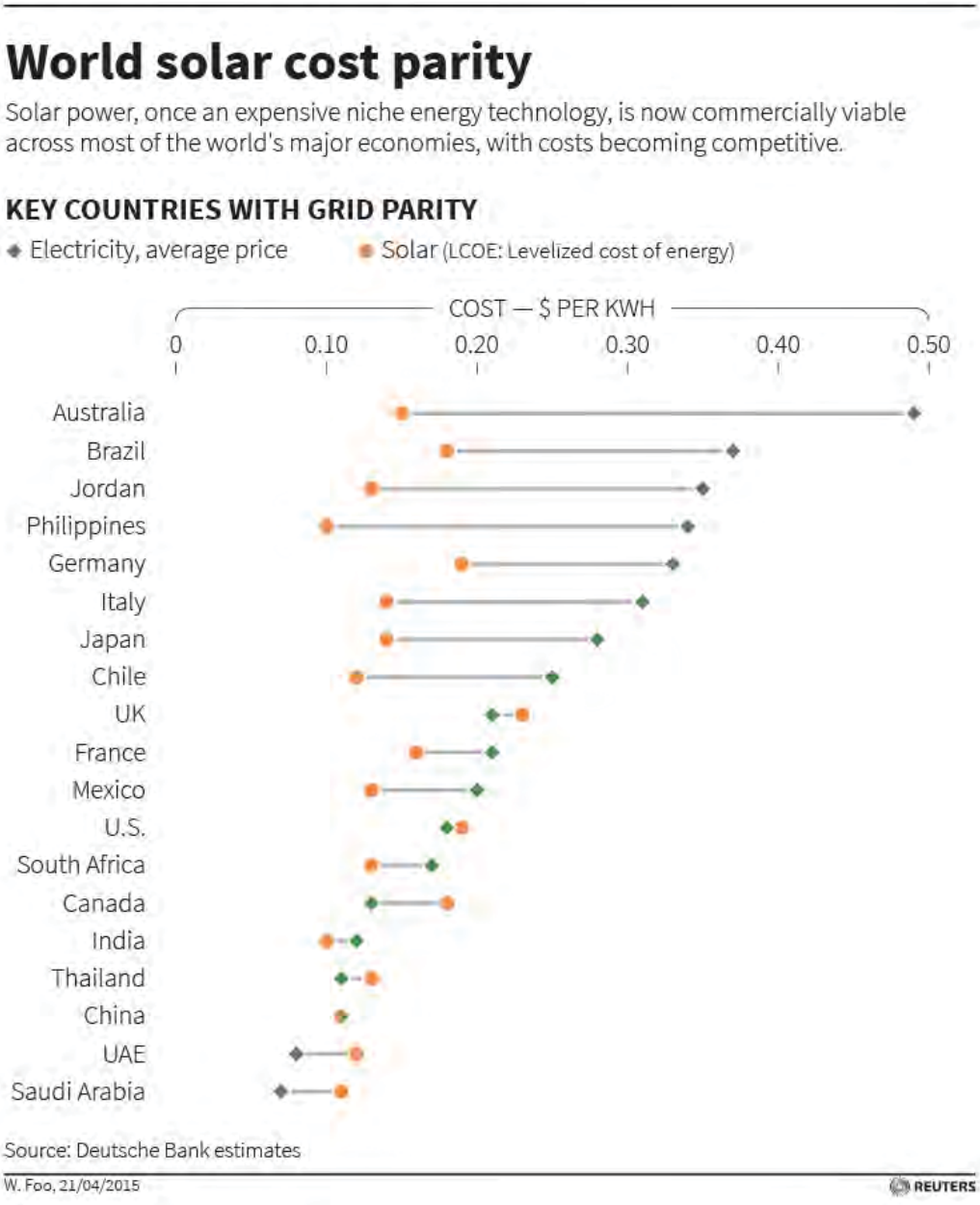


Figure 1.3 – Grid parity of key countries [4]

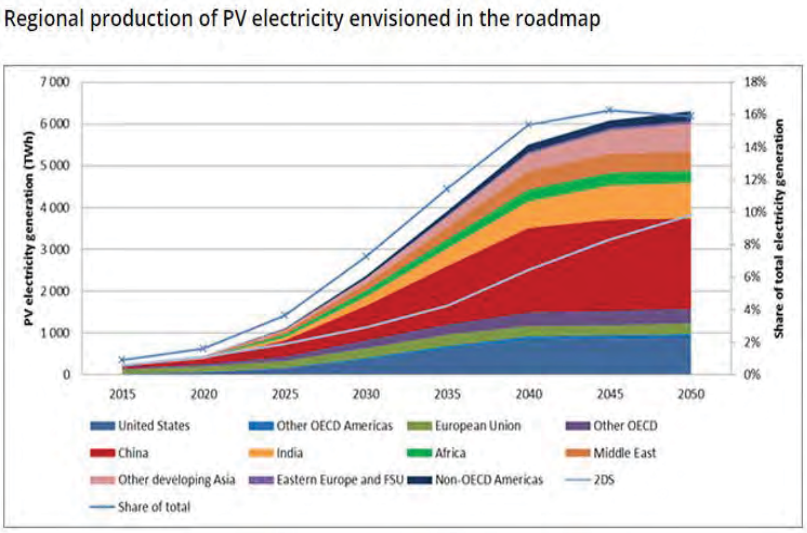


Figure 1.4 – Forecast of PV electricity production [5]

level conversion and control. The inverter is fundamental component of a functioning PV system, whose main functions include the conversion of DC to AC power and Maximum power point tracking. Inverters can be designed suitably to work in off-grid or grid-connected PV systems. Modern day inverters are highly efficient, and operate with a high power factor and low harmonic distortion.

One basis of classification of inverters is on their size and scale of application, in which they can be classified as micro, string and central inverters. Micro inverters are usually for individual panels with an output power level of less than 500 W. The output is commonly single phase AC, which can be connected to the grid. Since a micro inverter control the output of a single panel, the MPPT tracking is more efficient resulting in greater energy production. These are developed as modular units with the panel and the inverter and are ideal for residential and off grid applications.

In larger systems, it is more practical to have an inverter connected to many PV panels. These include string and central inverters. String inverters are used in a system with a single string of PV panels. The power output is usually in the range of 2 to 5 MW and is ideal for residential rooftop solar installations. The maximum

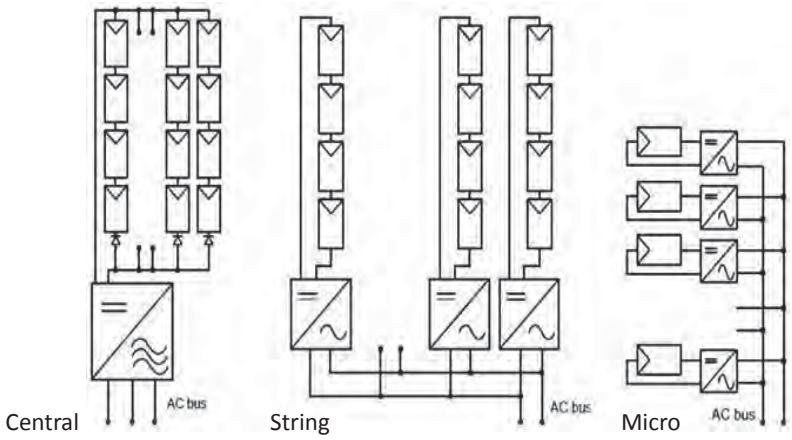


Figure 1.5 – PV system classification

power tracking is not as optimal as the micro inverter, but better than in a central inverter system. In larger utility scale application, many such strings are connected to a single inverter. Such a system is called the central inverter. They operate in the scale of several MWs and have 3 phase output. The MPPT is less optimal than in string and micro inverters. Since these inverters are going to be grid connected, they incorporate several complex and advance grid support features such as active and reactive power support, fault recovery support and so on.

Figure 1.5 shows the arrangement of PV panels and inverters in central, string and micro inverter based PV system.

1.3 Module Level Power Electronics

Module level power electronics (MLPE) is a term used to describe a completely independent electronic system present in each photovoltaic panel. They include both DC optimizer and solar micro inverter. Figure 1.6 shows major players in module level power electronics industry [6].

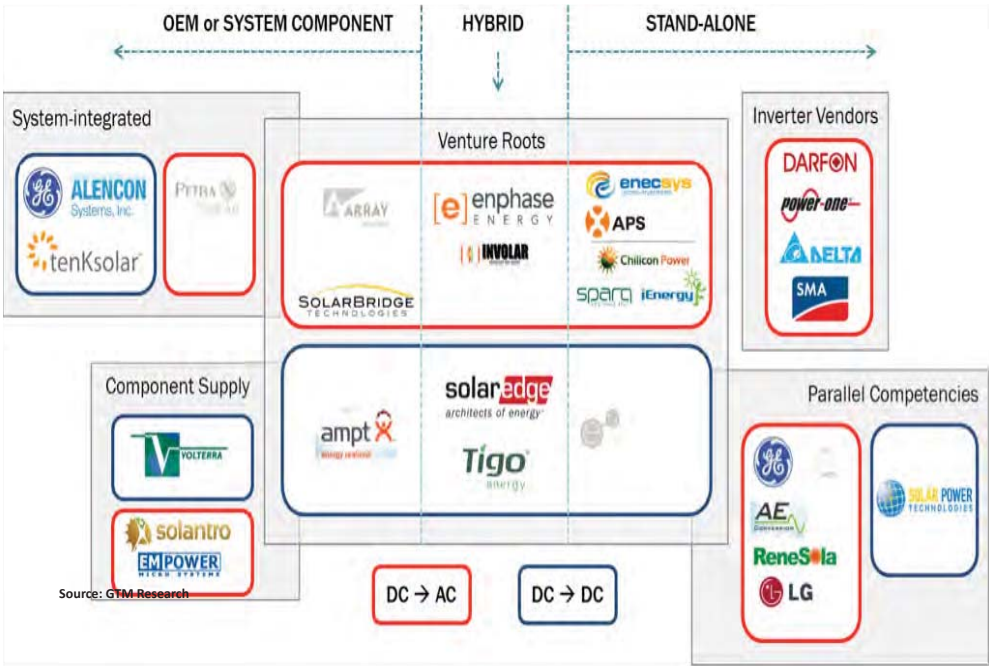


Figure 1.6 – Major players in MLPE industry [6]

1.3.1 DC optimizers

DC optimizers are DC-DC converters that sets the operating point of a photovoltaic panel so as to extract the maximum power available at that instant. Unlike the traditional DC-DC converters, DC optimizer does not perform buck or boost operation, rather they control the input to optimize the power that is being extracted. Thus, these devices increase the energy harnessed from solar photovoltaic systems by continuously tracking the maximum power available at each module at a given instance. They perform maximum power point tracking operation (MPPT) for each module with low components count. They are either embedded on to the module by manufacturers or could be individually purchased and installed.

1.3.2 Solar micro inverters

Solar micro inverter is a power electronic system that converts PV panel output (DC) to grid connectable AC power. These devices incorporates MPPT algorithm.

Typically they are single phase inverters and their ratings are comparable to the ratings of PV panel since they are connected to each module. Perhaps, off late there are commercial three phase micro inverters that is connected to two or three panels. The concept of solar micro inverter is extensively discussed in chapter 2 and 3.

1.4 Organization of thesis

The organization of the report is as follows. In Chapter 2 the general components of a solar micro inverter is introduced in great detail.

Chapter 3 discusses the modeling of a solar micro inverter with electrical specifications similar to those of commercial micro inverters. The simulation results along with the performance of controllers with a step change in insolation are presented. In Chapter 4, the failure mode effect and analysis of micro inverters are discussed. The top at-risk components are identified. Chapter 5 provides the reliability analysis of micro inverters and also provides the result of degradation modeling of DC bus capacitor. Impact of high intensity surge on the micro inverter performance is also presented. In Chapter 6, the work carried out in this thesis are summarized and scope of future work is mentioned.

Chapter 2

COMPONENTS OF SOLAR MICRO INVERTERS

The module integrated converters (MIC) technology has gained universal popularity in grid connected photovoltaic systems and they could be beneficial in lowering the balance of system cost and achieve better total system cost [7]. Solar micro inverters offers greater energy harvest compared to string inverters. They exist in the range of few hundred watts, and the biggest commercially available single phase micro inverter is rated at 300 W. Since these devices are connected to each photovoltaic module, their power ratings are very similar to those of commercially available photovoltaic modules.

Solar micro inverters can be broadly classified based on their topology (type of isolation). Each of these categories could either be single phase or three phase. Three phase micro inverter topologies can be extensively found in literature but are seldom used in practice. In addition, each of these topologies can be of grid tied or off grid type. But in reality, almost all the commercially available solar micro inverters in the market are grid tied inverters. The three types of isolation based on which the solar micro inverters are categorized are:

- Low frequency transformer
- High frequency transformer
- Transformerless

Using low frequency transformer isolation is perhaps a very old trend. Figure 2.1 shows the block diagram of micro inverter employing low frequency transformer. This topology was used in the first few generations of solar micro inverters. It makes the

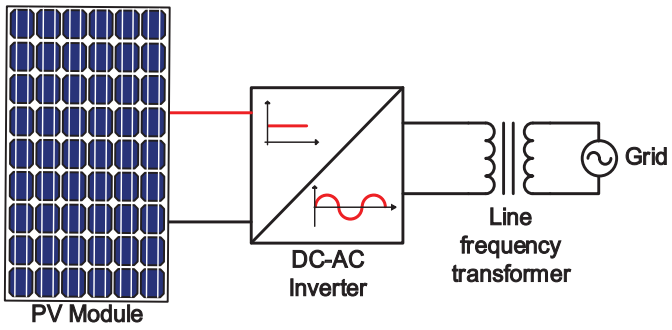


Figure 2.1 – Solar micro inverter with low frequency transformer

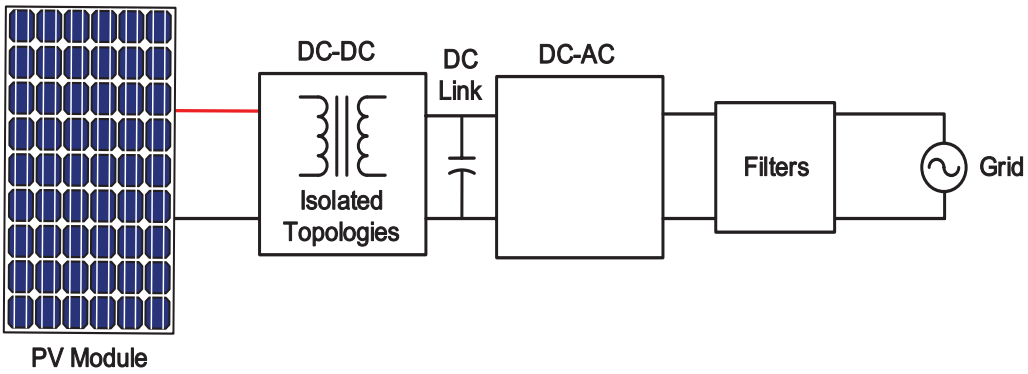


Figure 2.2 – Solar micro inverter with high frequency transformer

micro inverter bulky and lossy. With the advancements in power electronics technologies, high frequency transformer based topologies are very popular. In fact, all the commercially available solar micro inverters have high frequency transformer based isolation. Investigation of this family of solar micro inverters is extensively presented in this report. Almost all the commercial grid connected PV inverter have galvanic isolation. However, there are discussions among experts on considering transformerless topologies for grid connected inverters. Isolation is mainly to achieve the voltage gain. Figure 2.2 shows the block diagram of micro inverter based on high frequency transformers.

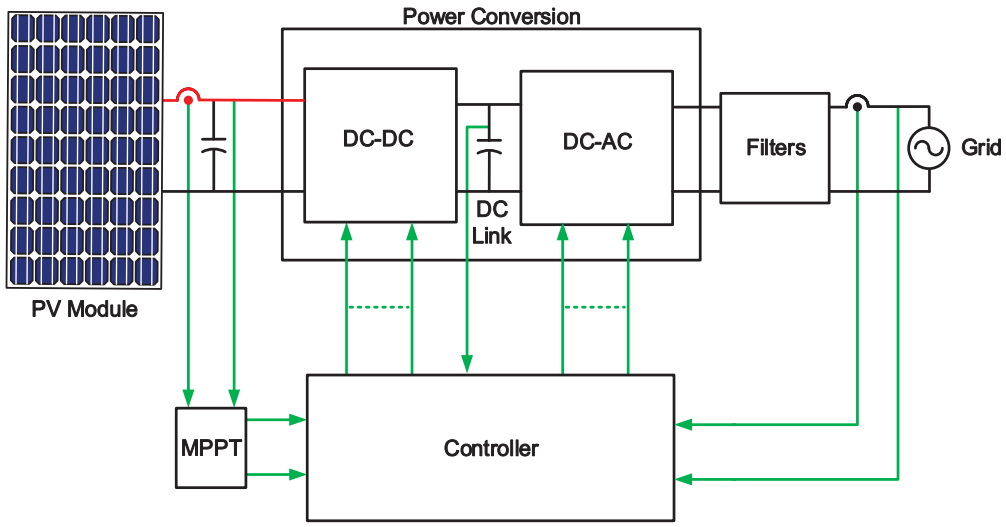


Figure 2.3 – Block diagram of a solar micro inverter with two stage conversion

Power density, efficiency, reliability and balance of system (BOS) costs are the important factors that drive the design of solar micro inverters. Apart from power conversion, solar micro inverter has many additional functions to perform in order to successfully feed the power extracted from photovoltaic panel to the grid. Figure 2.3 shows the block diagram of a typical solar micro inverter representing various blocks. In general, such inverters are comprised of the following subsystems, namely:

- DC and AC interconnects
- Maximum power point tracking (MPPT) controller
- Power conversion
- Filters
- Controller
- Communication

2.1 DC and AC interconnects

This includes the AC and DC cabling as well as AC and DC connectors. Most commonly found AC and DC connectors are MC4 and amphenol connectors. The DC input is connected through a disconnect switch. Input and output stages have DC and AC fuses respectively, for over current protection.

2.2 Maximum power point tracking (MPPT)

Essentially, power generation using solar photovoltaic panel is less efficient even on this day in comparison with conventional resources like coal. Solar cells have a theoretical limit on their efficiency. Currently, the conversion efficiency of commercial PV panels in the field are around 20% to 25%. Figure 2.4 shows the maximum conversion efficiency achieved by any solar cell till present day [8]. With such low efficiency, it is important that all the power generated by the PV module is extracted. Figure 2.5 shows the typical P-V and I-V characteristics for a PV module. The shaded area is the maximum available power. P_{MPP} is the optimum operating point where the PV generates its maximum power and is called maximum power point. This point keeps shifting depending on the insolation and other physical conditions. In order to increase the energy yield, the maximum power point has to be tracked continuously and operate the PV module at this point. An algorithm that automatically and continuously tracks P_{MPP} point is called maximum power point tracking (MPPT) algorithm and the electronics system that does this function is called maximum power point tracker. There are many algorithms that are prevalent. Some of the simplest, yet effective algorithms that are widely used are hill climbing method, also known as perturb and observe (P&O) and the incremental conductance method. The flowcharts of perturb and observe algorithm and incremental conductance algorithm is as shown in figure 2.6 and figure 2.7 respectively.

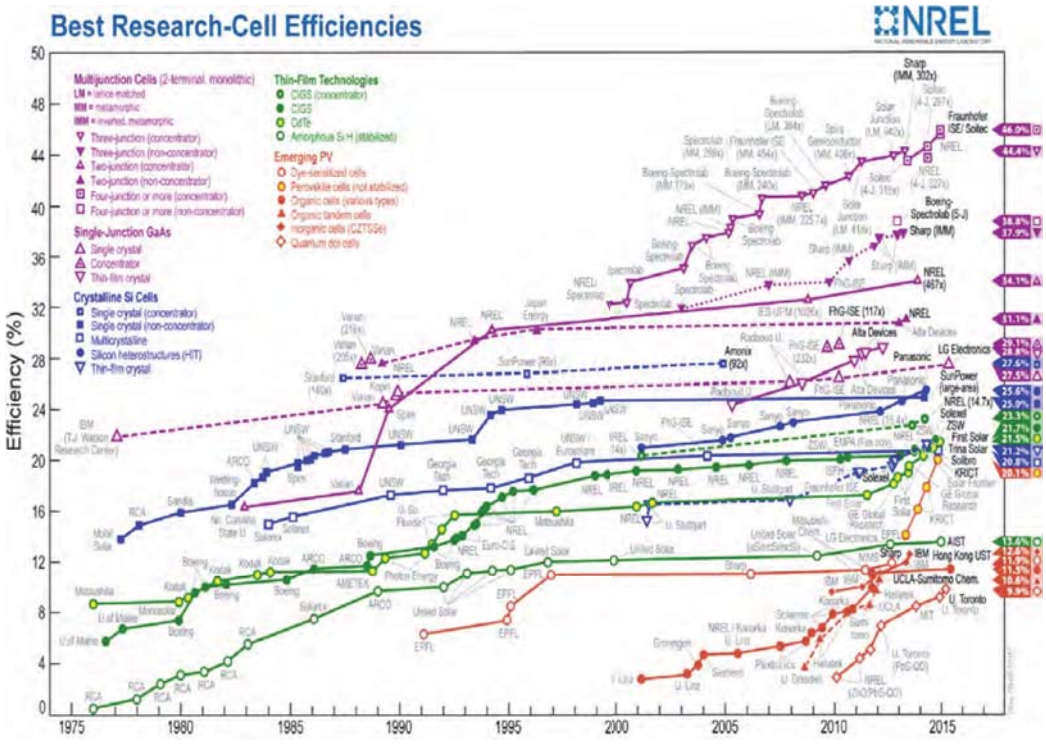


Figure 2.4 – Conversion efficiency of solar cell [8]

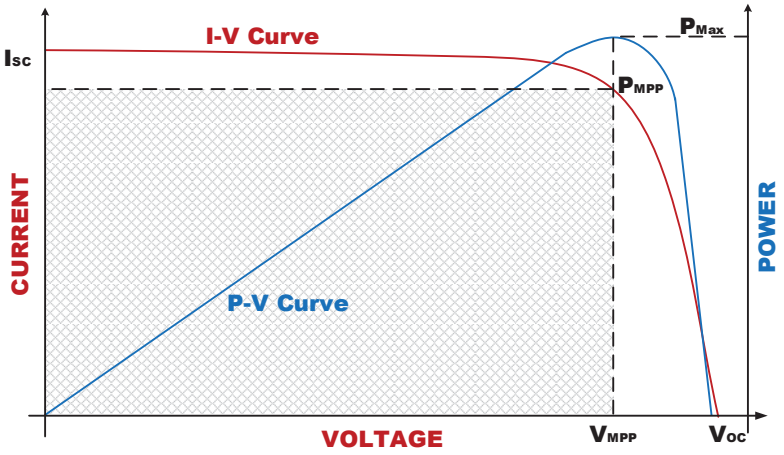


Figure 2.5 – Typical I-V and P-V curve for a PV module

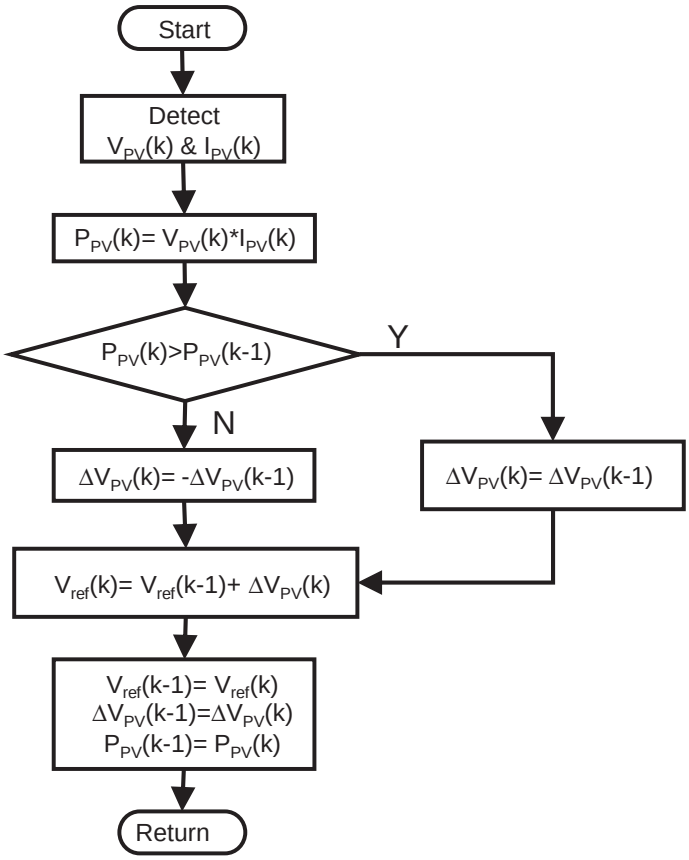


Figure 2.6 – Flow chart of Hill climbing or perturb and observe algorithm

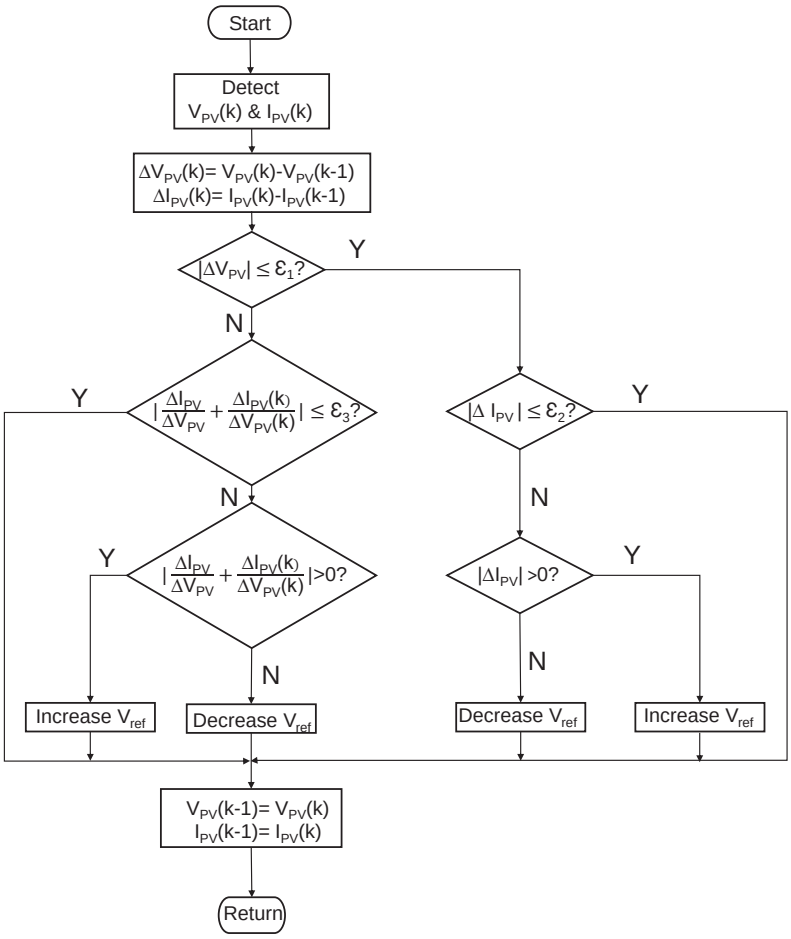


Figure 2.7 – Flow chart of incremental conductance algorithm

2.3 Power Conversion

The power conversion is generally a two stage conversion process, the front end being the DC-DC stage followed by DC-AC stage on the grid side. In order to achieve high voltage gain (30 V to around 350 V or 400 V), almost all the commercially available micro inverters make use of isolated topologies like flyback, forward or full bridge derived topologies for the front end DC-DC stage. In case of low frequency transformer based micro inverter, the front end converter is non-isolated like a buck, boost or buck-boost derived topology.

The PV panel voltage is in the range of 25 V to 45 V. This voltage is processed differently in different categories of micro inverters mentioned early in this chapter. In the case of low frequency based micro inverters, the panel voltage is converted to rectified sine wave of power frequency by the front end converter. Then this rectified wave is unfolded by the inverter stage switched at power frequency. Since the power is processed at power frequency, the filtering requirements are absolutely minimal or some times none. This type of power conversion has very low power density and is also less efficient. On the other hand, the latter two categories, i.e., high frequency transformer based topology and transformerless topology converts the low voltage DC from the panel to high voltage DC. DC link capacitors are used for power decoupling. There are other means of power decoupling as well but in terms of commercially available micro inverters, DC link is prevalent for power decoupling. The inverter stage is switched at higher frequency in the order of few kHz range. Advanced pulse width modulation (PWM) techniques are used improve the power quality. As a result of higher switching frequency, sophisticated filtering is required to achieve the total harmonic distortion (THD) specification dictated by the grid interconnections standards.

2.4 Filters

Filters are connected between power poles of inverter stage and the grid. Filters perform two important tasks, namely, filtering high switching frequency components present in grid current and also protecting the switches in inverter stage from transients. There are many types of filter structures. The most widely used filter structures are as shown in Figure 2.8 where v_{AB} is the line to line PWM voltage represented as a pulse source and v_g is the grid voltage. Out of these three types, L filter is the most basic filter and termed as first order filter and LCL is the advanced filter termed as third order filter.In order to meet the stringent current THD, most of the micro inverters use third order filters.

The L filter has poor performance in terms of damping the high frequency noise. In the case of LC filter,the output capacitor always sees the harmonics in the line voltage (if any) since it is directly connected across the grid and it may result in high currents through them.

The LCL filter encompasses the good properties associated with the L and the LC filters. In addition, LCL filter offers faster roll off due to the addition of a pole due to the presence of the second inductor. As a result, the filtering is even better compared to the other two filters. It also protects the capacitor from being directly exposed to line voltage harmonics. The bode magnitude plot for the all the three types of filters represented in the Figure 2.8 is shown in Figure 2.9.

The capacitor voltage is same as the grid voltage in LC filter since it is directly connected across the grid terminals. Even though it seems like there are two energy storage element, the capacitor voltage is not considered as a state while deriving the transfer function for this filter since grid voltage is assumed to be constant. Hence the response of L and LC filter are overlapped in the Figure 2.9. The transfer function from inverter PWM voltage v_{AB} to grid current i_g of both L and LC is as shown in

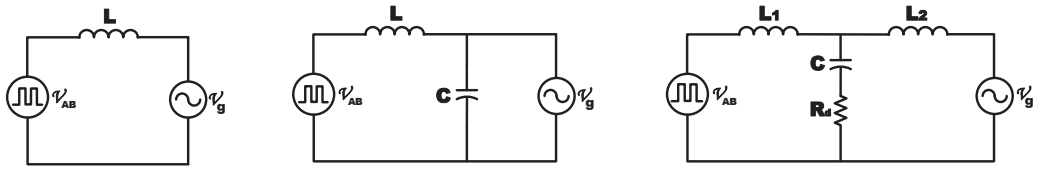


Figure 2.8 – Basic types of line filters: L, LC, and LCL.

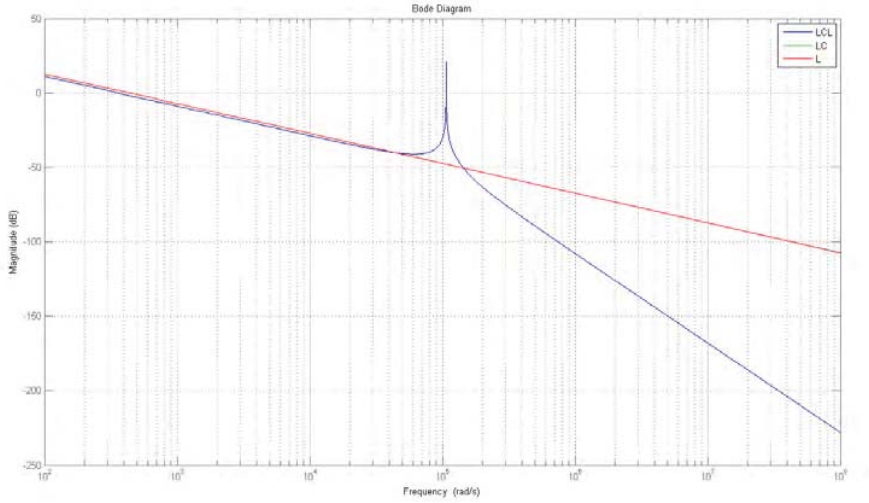


Figure 2.9 – Bode magnitude responses of all three types of filters (L, LC and LCL)

equation 2.1 and the transfer function of LCL filter is as shown by the equation 2.2. As the order of the filter is increased, the quality of filtering is better but at the cost of increase in the number of inductors and capacitors used. Hence it is not a practical solution for micro inverters.

$$\frac{\tilde{i_g}(s)}{\tilde{v_{AB}}(s)} = \frac{1}{sL + r_L} \tag{2.1}$$

$$\frac{\tilde{i_g}(s)}{\tilde{v_{AB}}(s)} = \frac{1}{L_1 L_2 C\ s^3 + (L_1 C\ r_{L_2} + L_2 C\ r_{L_1})s^2 + (C\ r_{L_1}\ r_{L_2} + L_1 + L_2)s + (r_{L_1} + r_{L_2})} \tag{2.2}$$

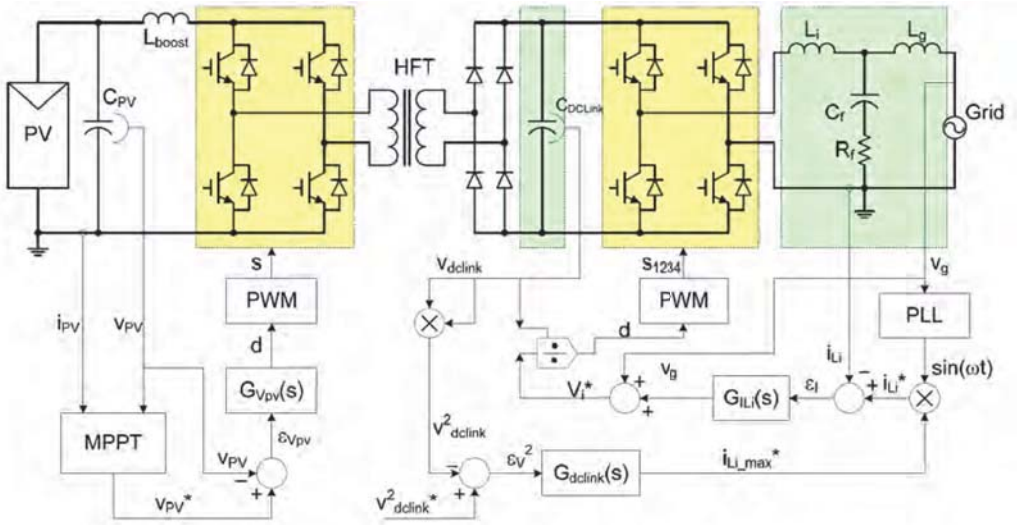


Figure 2.10 – Control structure of a typical solar micro inverter [37]

2.5 Controller

There are various types of controllers in a grid interactive PV system. Figure 2.10 shows the various controllers in a micro inverter. Apart from the above list of controllers, there could be controllers for communication, servicing interrupts and so on. But those are not discussed in this thesis. The most important controllers found in any solar micro inverters are:

- MPPT controller
- Grid current controller
- DC link voltage controller
- Phase locked loop (PLL) controller

2.5.1 MPPT controller

Maximum power point tracking has been discussed in section 2.2. This controller is used in implementing MPPT algorithm. It is achieved by front end DC-DC converter,

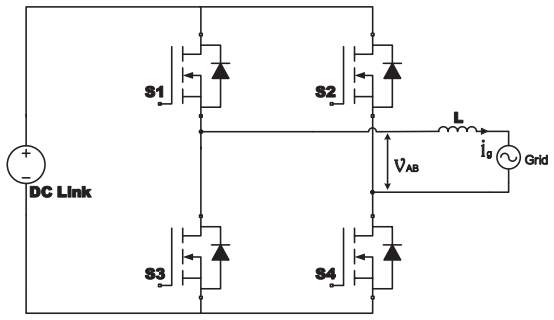


Figure 2.11 – Simple H-bridge inverter with L filter

which regulates its input to MPP voltage referenced by the MPPT algorithm.

2.5.2 Grid current controller

Grid current controller processes the current to be fed to the grid. The magnitude of the current that is to be fed at any instance is given by the preceding DC link controller. The phase and frequency reference is provided by the PLL controller. These two quantities are multiplied to get the reference current. Considering a simple H-bridge inverter with a DC link denoted by a constant DC source as shown in Figure 2.11, the transfer function from PWM voltage to grid current is expressed by equation 2.1. This is considered to be the plant and the grid current controller section is pictorially represented in Figure 2.12. As a rule of thumb, the bandwidth of this controller is chosen to be $1/10^{th}$ of the inverter switching frequency. The grid voltage is used as a feed forward input in order to reject the disturbance at the input (if any). However, the draw back of this controller is that there is a small steady state error in magnitude and phase. This can be overcome by implementing more advanced grid current controller like proportional resonant (PR) controller.

2.5.3 DC link controller

DC-AC stage regulates the DC link voltage. Control of this voltage is through changing the amplitude reference of sinusoidal AC line current. The bandwidth of this

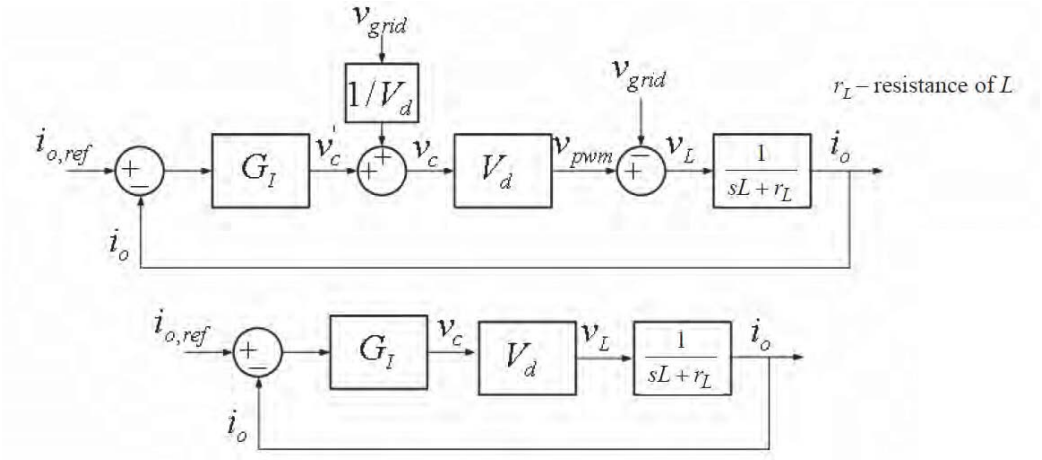


Figure 2.12 – Stucture of a grid current controller [37]

controller is chosen to be very small of the order of 5 Hz to 10 Hz so that the reference wave shape of line current is not distorted. The structure of DC link controller is as shown in Figure 2.13. This controller is based on the concept of energy balancing. Assuming an ideal loss less system, the power at the input is same as the sum of power stored at DC link and power available at the output. Referring to Figure 2.11,

$$\frac{1}{2}\frac{d}{dt}(C_{dc\ link}V_{dc\ link}^2) = P_{in} - i_g v_g \tag{2.3}$$

$$\frac{C_{dc\ link}}{2}\frac{d}{dt}(V_{dc\ link}^2) = P_{in} - \frac{\hat{I}_g\hat{V}_g}{2}\left(\frac{1-\cos(2\omega_o t)}{2}\right) \tag{2.4}$$

Since the bandwidth of the controller is so small, the controller does not respond to 120 Hz ripple. Hence the equation 2.4 can be reduced to,

$$\frac{C_{dc\ link}}{2}\frac{d}{dt}(V_{dc\ link}^2) = P_{in} - \frac{\hat{I}_g\hat{V}_g}{2} \tag{2.5}$$

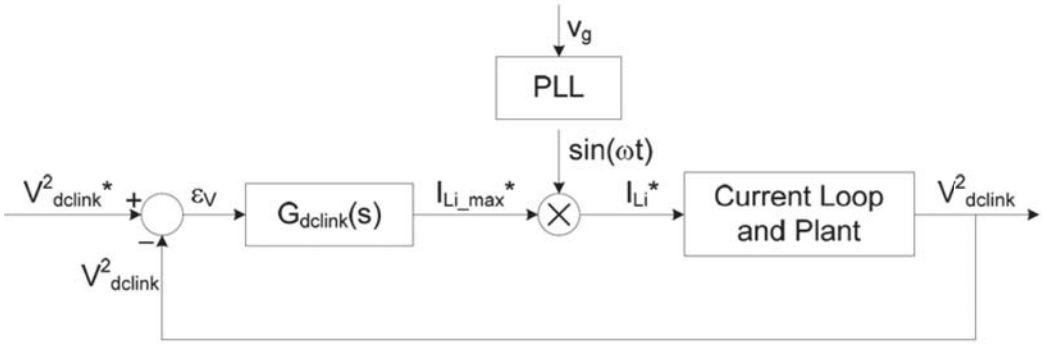


Figure 2.13 – Stucture of a DC link voltage controller [37]

Assuming constant input power and constant grid voltage, the transfer function for DC link controller can be expressed as,

$$\frac{C_{dc\ link}}{2}\ s\ V^2_{dc\ link}(s) = -\frac{\hat{V}_g}{2}\ \hat{I}_g(s) \tag{2.6}$$

$$\frac{V^2_{dc\ link}(s)}{\hat{I}_g(s)} = -\frac{\hat{V}_g}{s\ C_{dc\ link}} \tag{2.7}$$

Equation 2.7 shows that it is easy to have an expression in terms of $V^2_{dc\ link}$ rather than just $V_{dc\ link}$. In addition, the negative sign in equation 2.7 denotes the inverse relationship between grid current and DC link voltage, i.e., as the grid current increases, the DC link voltage decreases and vice versa.

2.5.4 Phase locked loop (PLL) controller

It is required to operate PV inverter system in synchronism with the grid, as per IEEE 1547 standards. Hence, it is required to control the internal reference signal of the inverter in phase with the grid voltage. This is known as grid synchronization. Of the methods available to achieve this, phase locked loop (PLL) is the main technique used. The PLL system generates an output signal in closed loop whose phase is related to the phase of the internal reference signal. The output signal is proportional to the

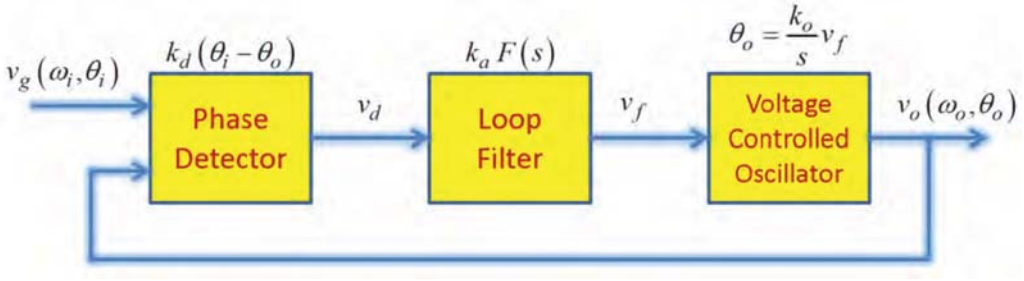


Figure 2.14 – Simple structure of a phase locked loop [37]

phase difference between the input and output waveforms. Figure 2.14 shows a simple block diagram to implement PLL. PLL is designed as a simple PI controller.

2.6 Communication

The main drawback of using micro inverters in a fairly bigger PV system is monitoring their status. It is not easy to identify a faulty micro inverter amidst huge pool of such micro inverters in case of a PV plant. To get rid of this drawback, almost all commercial micro inverters communicate with server to let the user know about the status of the micro inverter. Essentially, the user can know the status of the plant in addition to data such as plant location co-ordinates, fault monitoring, energy yield and so forth. SMA multigate, ABB CDD units are some of the examples for communication devices. Most of the commercial inverters are based on RF communication, power-line communication and other wireless (internet based) communication protocols. Nonetheless, this section is not of primary interest from power electronics point of view and hence not much emphasis is given on this section.

Chapter 3

MODELING AND DESIGN OF SOLAR MICRO INVERTER

There are many commercial micro inverter available in the market today. Figure 3.1 shows the market share of residential inverters in the US [9]. Almost all these manufacturers have micro inverters in their product segments. Enphase and SMA have bulk of the market share followed by other manufacturers like ABB, SolarBridge and so forth.

Table 3.1 shows the comparison of important electrical specifications of various manufacturers within similar power range. Based on this comparison, a generic specification is generated for modeling a micro inverter as listed in Table 3.2.

3.1 Power conversion stage

The two power conversion stages, DC-DC and DC-AC, are to be designed. In order to achieve MPPT operation, the DC-DC stage regulates the input to the reference voltage set by the MPPT stage. The DC-AC converter regulates the DC link voltage which happens to be the input for that stage.

Table 3.1 – Comparison of electrical specifications of various commercial $\simeq$ 250 W micro inverters

Micro inverter	Power	MPPT	Efficiency	PF	Ambient Max
Enecsys 250 NL	250 W	24 V - 35 V	95.5% CEC	-	$-40^oc - +85^oc$
Enphase M250	250 W	27 V - 39 V	96.5% CEC	>0.95	$-40^oc - +65^oc$
SolarBridge Pantheon II P250LV	250 W	18 V - 37 V	95% CEC	>0.99	$-40^oc - +65^oc$
SMA Sunnyboy 240-US	240 W	23 V - 39 V	95.9% CEC	-	$-40^oc - +65^oc$
ABB MICRO-0.25-I-OUTD	250 W	25 V - 60 V	96% CEC	>0.95	$-40^oc - +75^oc$

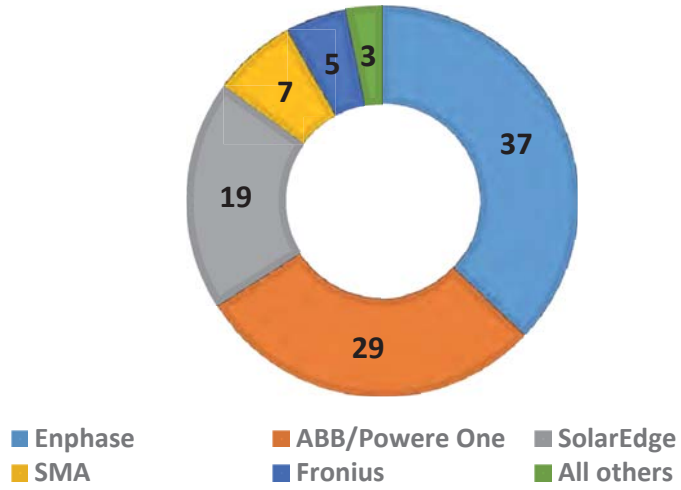


Figure 3.1 – Leading US residential inverter supplier 1H 2014 [9]

Table 3.2 – Electrical specifications of the micro inverter to be modeled

Parameter	**Value**
AC Power	250 W
Output voltage	208 V
MPPT Range	20 V - 45 V
PF	UPF
THD	< 5 %
Isolation	HF transformer

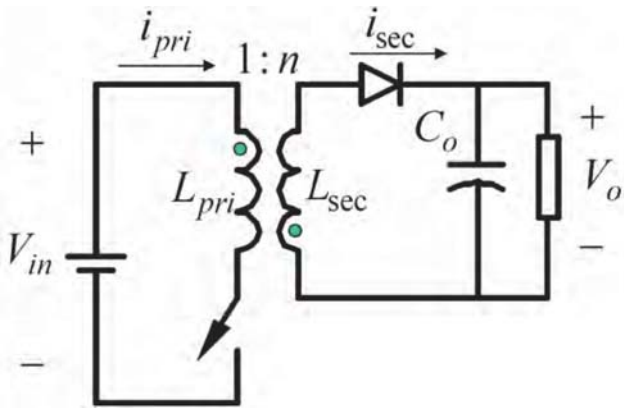


Figure 3.2 – Flyback converter topology

3.1.1 DC-DC stage

In line with the specifications of commercial micro inverters, high frequency isolation based topology with a DC link is preferred. Hence flyback topology is chosen to be the front end converter. Flyback converter has the least part count compared to other isolated converter topologies with just a coupled inductor, capacitor, diode and a switch. The operating principle is based on buck-boost topology. Figure 3.2 shows the circuit diagram of flyback converter.

The input-output relationship for a flyback converter is expressed as

$$\frac{V_o}{V_i} = n \cdot \frac{D}{(1-D)} \tag{3.1}$$

where V_o is the output voltage, which in this case happens to be DC link voltage, V_i is the input voltage, n is the transformer turns ratio and D is the duty ratio.

To generate an AC voltage of 208 V_{rms}, the minimum DC link voltage has to be around 300 V. Considering some margin, DC link voltage is selected to be around 350 V. There are two variables in equation 3.1, i.e., n and D. Lower value of n leads to higher voltage stress across switch and higher D leads to higher current through the switch. One needs to optimize these values. In this case, limiting the maximum

duty ratio (D_{max}) to 0.8, the value of n is found to be 7.142. With the magnetizing inductance referred to the primary of the transformer, the equation to find its value is expressed in equation 3.2.

$$L_m = \frac{V_o \cdot (1 - D_{min}) \cdot T_s}{n \cdot \Delta I_{in}} \tag{3.2}$$

where L_m is the magnetizing inductance, D_{min} is the minimum duty ratio, T_s is the switching time period and ΔI_{in} is the maximum allowable ripple current at the input. The switching frequency is chosen to be 150 kHz and maximum allowable ripple is 10% of the input current. The magnetizing inductance is found to be 10.51 μH.

3.1.2 DC-AC stage

H-bridge inverter is the most widely used inverter topology for micro inverters and even string inverters. It is also very common to see H-bridge inverter driven by unipolar PWM.

Decoupling network

The size of the DC link capacitor that decouples the DC and AC stage is designed based on the 120 Hz ripple. As mentioned earlier, 300 V is required to generate 208 V_{rms}. If DC link goes below 300 V, the output power quality takes a toll. Hence safety margin is considered and 350 V is selected as DC bus voltage.

$$P_o = \hat{V_g} \sin(\omega t) \cdot \hat{I_g} \sin(\omega t) \tag{3.3}$$

where $\hat{V_g}$ and $\hat{I_g}$ are peak grid voltage and grid current respectively and ω is the angular frequency.

$$\implies P_o = \frac{\hat{V_g} \cdot \hat{I_g}}{2} (1 - \cos(2\omega t)) \tag{3.4}$$

It can be observed that the output power has two quantities. The first term $\frac{\hat{V_g} \cdot \hat{I_g}}{2}$ is the constant power and the second term $-\frac{\hat{V_g} \cdot \hat{I_g}}{2}\ \cos(2\omega t)$ is the pulsating power. The current due to the second component flows through the DC link capacitor and its instantaneous value can be expressed as,

$$\bar{i}_{c_{dc\ link}}(t) \ = \ -\frac{\hat{V_g} \cdot \hat{I_g}}{2 \cdot V_{dc\ link}}\ \cos(2\omega t)) \tag{3.5}$$

Thus, the expression for instantaneous value of voltage ripple across DC link capacitor is obtained by integrating the expression 3.5,

$$\bar{v}_{c_{dc\ link\ ripple}}(t) \ = \ \int \bar{i}_{c_{dc\ link}}(t) \cdot dt \ = \ -\frac{\hat{V_g} \cdot \hat{I_g}}{4 \cdot \omega \cdot V_{dc\ link} \cdot C_{dc\ link}}\ \sin(2\omega t) \tag{3.6}$$

Equation 3.6 is rewritten to find the value of DC link capacitor as shown in equation 3.7.

$$C_{dc\ link} \ = \ \frac{P_o}{2 \cdot \omega \cdot V_{dc\ link} \cdot \Delta V_{c_{dc\ link\ ripple}}} \tag{3.7}$$

The negative sign in 3.5 denotes that the current is flowing into the capacitor. In this modeling, the capacitor values calculated comes to 54.13 μF. The next higher standard capacitor value is considered which is 66 μF.

Inverter

Some modifications has been done to the typical H-bridge inverter by adding an inductor between the two switches of each power pole and it is as shown in the Figure 3.3. In this arrangement, the current through the device can be limited in case of a shoot through fault. Thus, in the case of a shoot through fault, the rise in inductor current (i_{L_1}) can be sensed and the gate pulses can be blocked thereby preventing the failure. This arrangement makes the inverter and in turn the PV system more reliable. On the other hand, the disadvantage is that it calls for an additional inductor

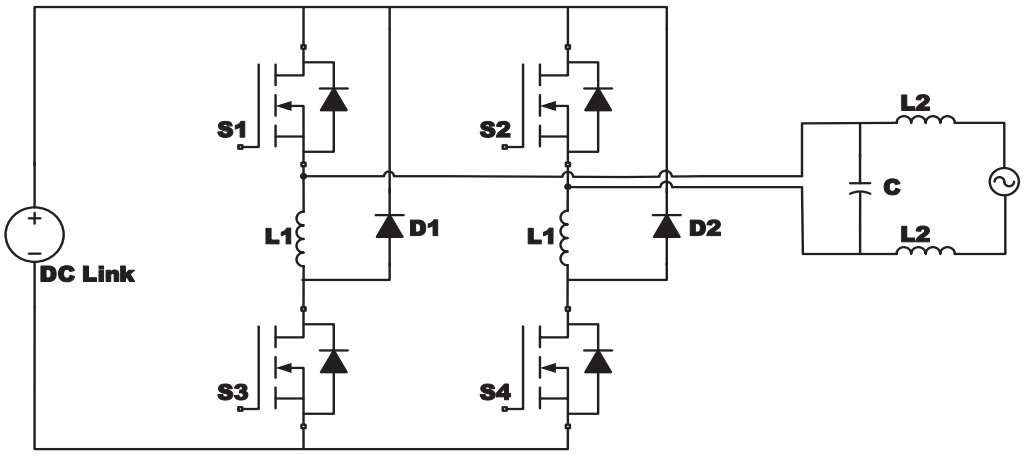


Figure 3.3 – A new variant of H-bridge inverter

which increases overall volume of the micro inverter in addition to adding extra cost.

Referring to Figure 3.3, inductors L_1 on each power pole forms LCL filter together with C and L_2 during operation of each power pole. It can be noted that L_1 cannot be split in to half and used on each leg where as L_2 can be split into two halves. This can also be considered an other disadvantage. A better understanding can be reached by referring Figure 3.4.

This variant of H-bridge inverter cannot be driven by the conventional unipolar PWM. Switch pairs S_1 - S_4 and S_2 - S_3 should work together for successful operation with suitable dead time between transition of operation from one leg to another in order to discharge the inductor L_1. Hence, a new pulse width modulation (PWM) technique has been used. It is called hybrid PWM. In this case, switch pairs S_1 and S_2 are switched at low frequency and switches S_3 and $S4$ are switched at high frequency. In this design, S_1 and S_2 are switched at 60 Hz (line frequency) and switches S_2 and S_3 are switched at 50 kHz. The switching pattern of this hybrid PWM is as shown in Figure 3.5 and Figure 3.6. The realization of this PWM is depicted in the Figure

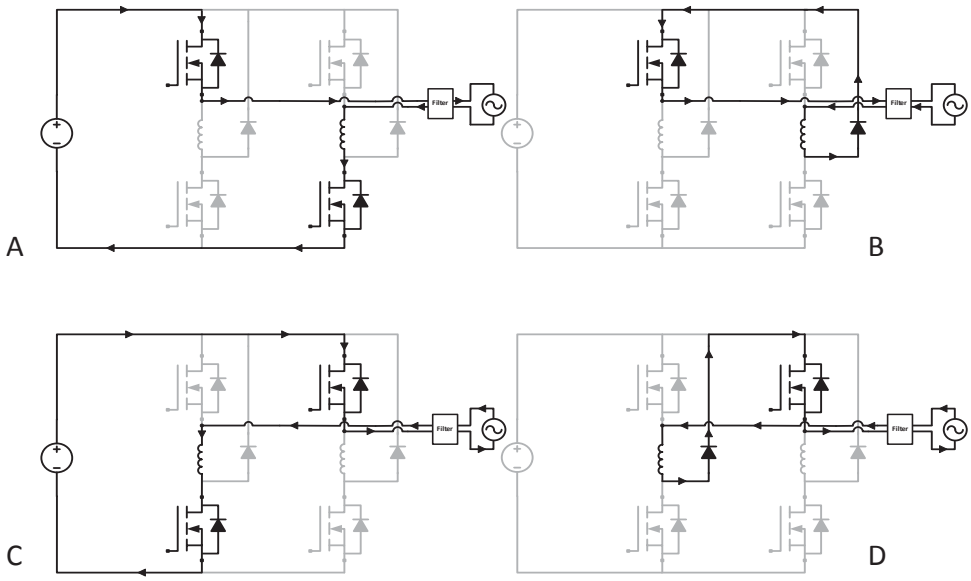


Figure 3.4 – Modes of operation of the new variant of H-bridge inverter

3.7.

3.2 Controller design

3.2.1 MPPT controller

In order to design the MPPT controller, the small signal model of the plant is required to generate the plant transfer function. In this modeling, the plant is the front end flyback converter and its transfer function from duty ratio $\tilde{d}$ to output $\tilde{v}_{PV}$ (since the parameter to be controlled is the input voltage of flyback converter). Figure 3.8 shows the small signal model of flyback converter [10]. In this controller design, the output voltage of flyback converter is assumed to be constant.

The transfer function from duty ratio $\tilde{d}$ to output $\tilde{v}_{PV}$ is found to be as shown in the equation 3.8.

$$\frac{\tilde{v}_{PV}}{\tilde{d}} = \frac{-(I_{CP}R_{PV}L_M s + R_{PV}V_{PV}D)}{s^2 C_{PV}L_M R_{PV} + sL_M - R_{PV}D^2} \tag{3.8}$$

K-factor type of controller design is employed due to its simplicity in design. It

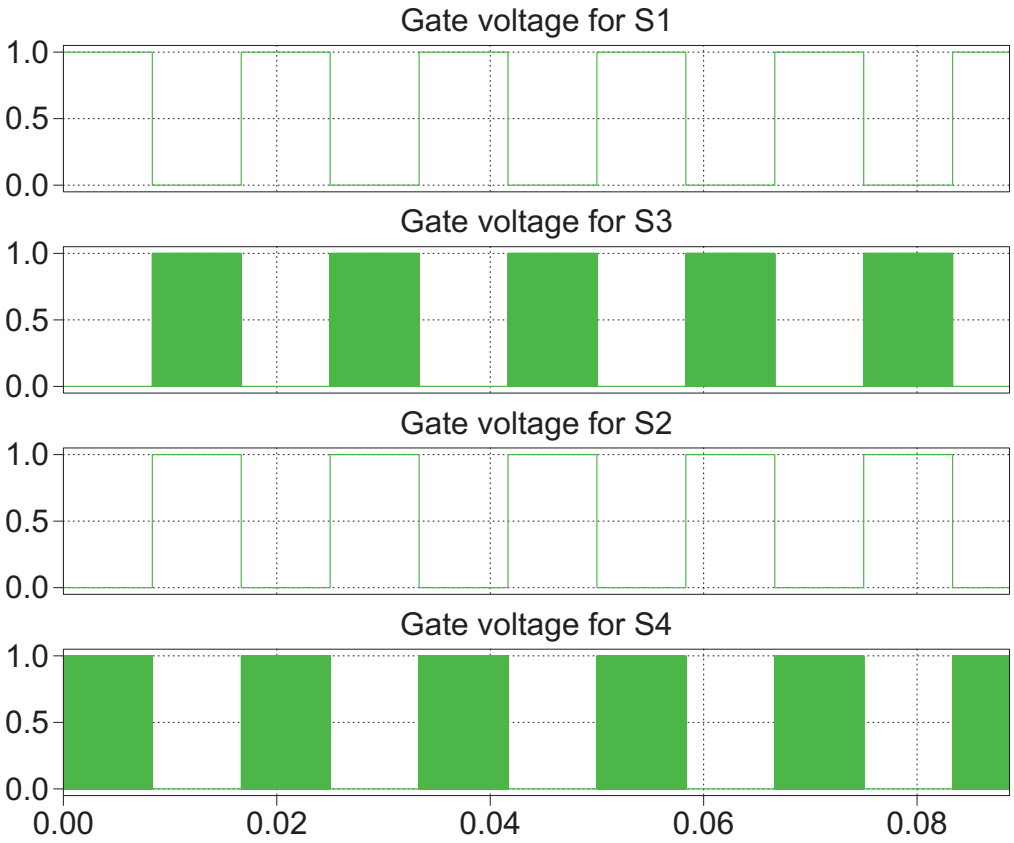


Figure 3.5 – Hybrid PWM switching waveforms

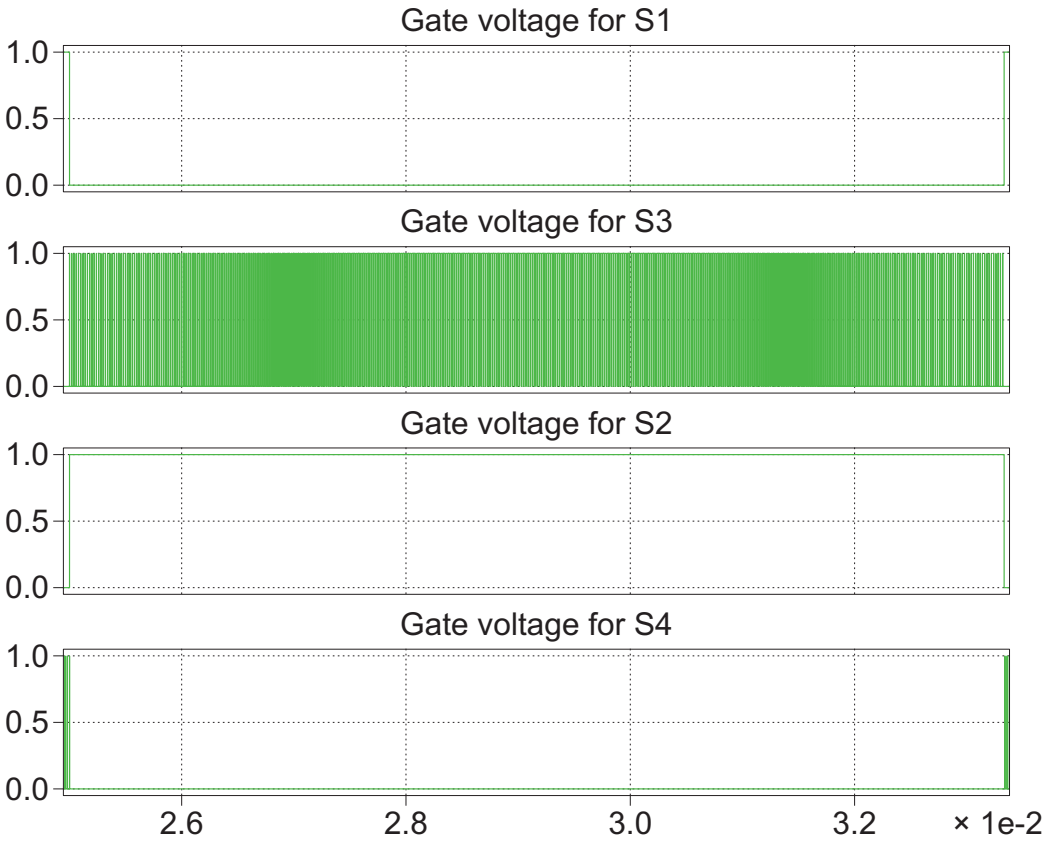


Figure 3.6 – Zoomed waveform of 3.5 to show switching

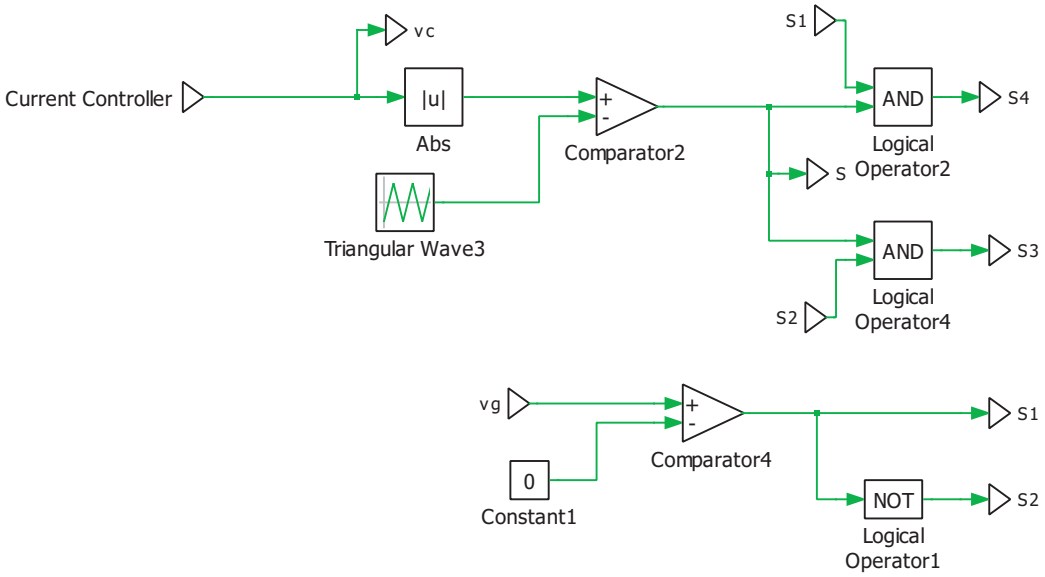


Figure 3.7 – Realization of logic for generating hybrid PWM shown in Figure 3.5

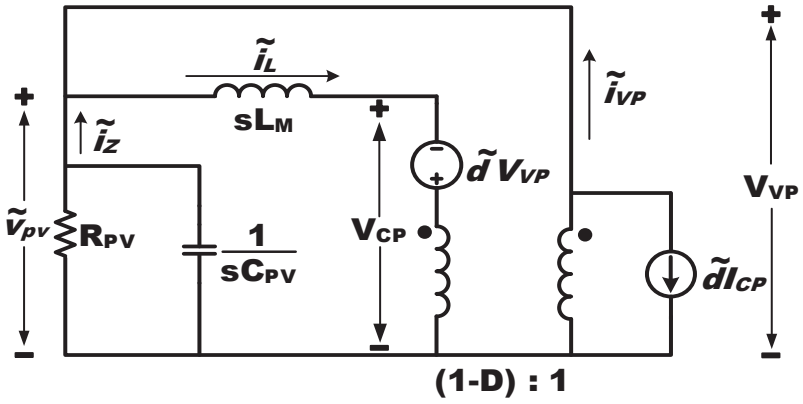


Figure 3.8 – Small signal model of flyback converter

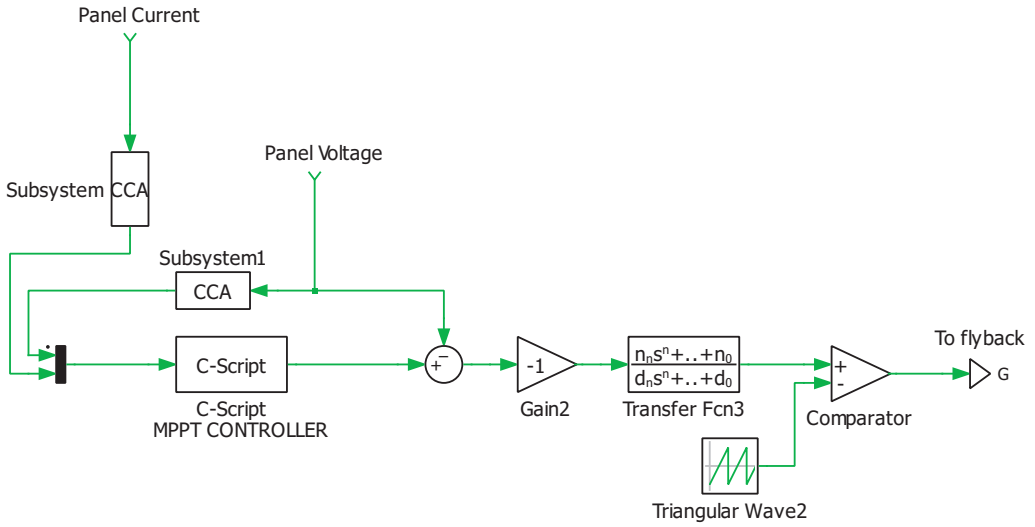


Figure 3.9 – Implementation of MPPT in simulation

turned out that type-2 controller along with an integrator is sufficient to stabilize the loop. The cross over frequency (f_c) of 2 kHz and phase margin (PM) of 60 deg was considered for the controller design. The structure of the designed controller is given by the equation 3.9. The MPPT algorithm is implemented using the c-script block in PLECS simulation tool (v3.7.2) as shown in the Figure 3.9.

$$G_{MPPT}(s) = \frac{-(0.1056 \cdot s \ + \ 173.8)}{1.042 \cdot 10^{-5} \cdot s^2 + s} \tag{3.9}$$

3.2.2 Grid current controller

The plant for which this controller designed is the inverter as shown in Figure 3.10 which connected to grid through a LCL filter. The plant transfer function from i_g to v_c is to be known in order to design the controller. From small signal analysis of the the system shown in the Figure 3.10, the transfer function is found to be as shown in equation 3.10. Grid voltage feed-forward based current controller is chosen due to

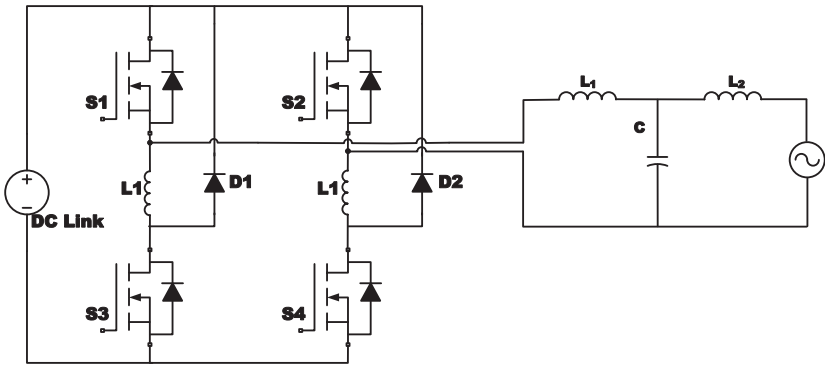


Figure 3.10 – Inverter connected to the grid through a LCL filter

simplicity. The controller block diagram is as shown in the Figure 2.12.

$$\frac{\tilde{i_g}(s)}{\tilde{v_c}(s)} = \frac{V_{dc\ link}}{L_1L_2C\ s^3 + (L_1C\ r_{L_2} + L_2C\ r_{L_1})s^2 + (C\ r_{L_1}\ r_{L_2} + L_1 + L_2)s + (r_{L_1} + r_{L_2})} \tag{3.10}$$

The input to this controller, the reference current is obtained from PLL and DC link voltage controller. The controller output is the reference controller voltage v_c The magnitude reference for the current to be controlled is obtained from from DC link controller stage. It can be seen that the grid voltage is fed forward to reject any disturbance in the grid voltage and it is later on subtracted by the actual voltage.

For this controller design, K-factor type-2 controller is used. Phase margin (PM) of 60 deg and cross over frequency (f_c) of $1/10th$ the switching frequency is used. The designed grid current controller is expressed by the equation 3.11.

$$G_{cc}(s) \ = \ \frac{465.722}{s} \cdot \frac{\frac{1}{4209.4868} \cdot s + 1}{\frac{1}{58618.0331} \cdot s + 1} \tag{3.11}$$

The implementation of grid current controller in PLECS is depicted in the Figure 3.11.

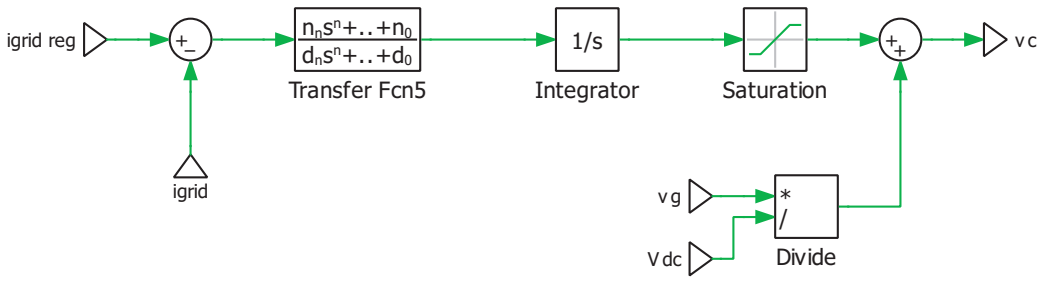


Figure 3.11 – PLECS implementation of grid current controller

3.2.3 DC link controller

The DC link voltage is assumed to be constant in MPPT controller design though the flyback converter does not control it. The inverter controls the DC link voltage by regulating the current fed to the grid. Equation 2.7 describes this action. This controller is based on the energy balance technique described in section 3.1.2. The structure of the DC link controller used in this model is as shown in the Figure 2.13. The output of this controller is the magnitude of the current to be fed to the grid.

K-factor type-2 controller is used in this design. It turned out that the response of this controller was sluggish and poor. To improve to performance, PI controller is used. With PI controller, the performance of the controller is improved in terms of settling time and overshoot. Tuning of PI controller is done using the MATLAB control system toolbox. The PLECS implementation of this controller is as shown in the Figure 3.12. The plant for the design of this controller is given by equation 2.7. The controller transfer function is given by 3.12. The closed loop frequency response for the DC link controller is shown in the Figure 3.13.

$$G_{DC}(s) \;=\; -1.996 \cdot 10^{-6} + \frac{-1.026 \cdot 10^{-5}}{s} \tag{3.12}$$

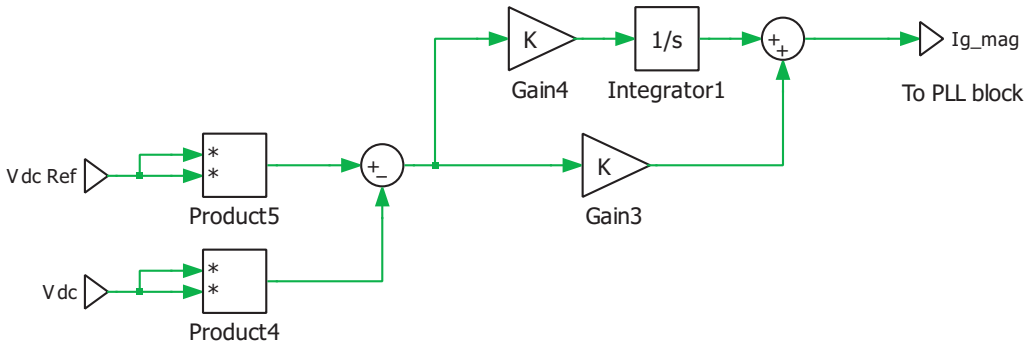


Figure 3.12 – PLECS implementation of DC link voltage controller

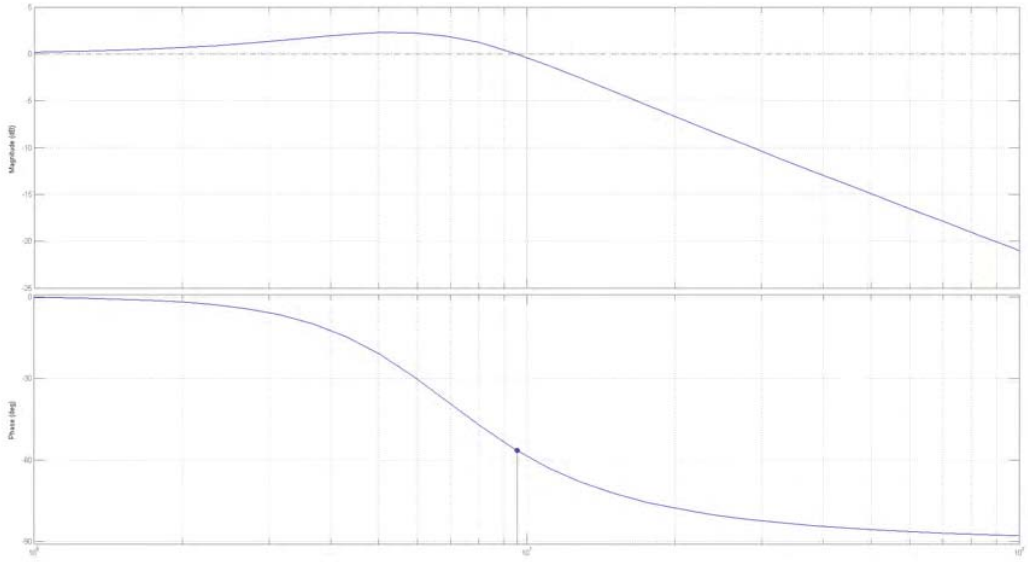


Figure 3.13 – Closed loop frequency response of DC link controller

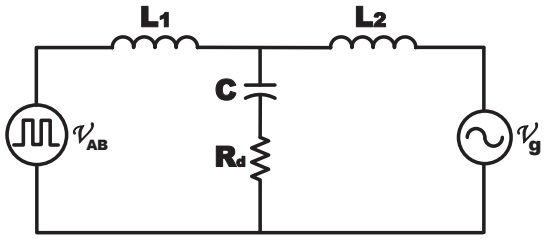


Figure 3.14 – LCL filter with passive damping

3.3 Filter design

In order to meet the THD requirement, good filtering is of primary importance. More often, a low pass passive power filter is connected between the inverter and the grid. It is used to limit the the harmonic currents generated by sine wave PWM injected into the grid at point of common coupling (PCC) [11]. In grid connected power electronic systems, attenuation of harmonics around switching frequency is of prime importance to meet the IEEE 1547.2-2008 [12] and 519-1992 [13]. The currents due to high frequency components leads to high frequency conducted emission, which has to be limited [11].

In section 2.4, the comparison of different filters are shown. After reviewing their pros and cons, LCL filter is chosen to be the structure for line filter. Referring to Figure 3.14, L_1, C and L_2 together forms the LCL line filter. Considering maximum allowable ripple current (Δi_{max}) to be 10% of the rated current, L_1 is calculated using the equation 3.13 [14] where f_s is the switching frequency.

$$L_1 = \frac{V_{dc\ link}}{6 f_s \Delta i_{max}} \tag{3.13}$$

Assuming around 1.5% of reactive power to be absorbed by the capacitor, the equation to find C is given in equation 3.14 [15], where ω_g is the angular power frequency and

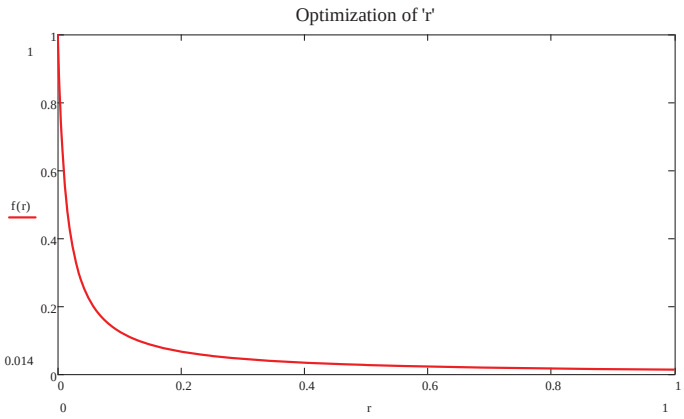


Figure 3.15 – Plot of harmonic attenuation at the switching frequency against r

P is the rated power.

$$C = \frac{0.015 \cdot P}{\omega_g v_g^2} \tag{3.14}$$

The ripple attenuation that passes from the inverter to the grid can be calculated and is extensively discussed in [15]. Design of grid side inductor L_2 is based on optimization of ripple reduction factor r and is given by equation 3.16. Neglecting the losses, the ripple attenuation factor is calculated based on the equation 3.15 [15] where i is the current through inner inductor and i_g is the current through the grid side inductor. The plot of $f(r) = \frac{i_g(h_{sw})}{i(h_{sw})}$ against r is as shown in the Figure 3.15.

$$\frac{i_g(h_{sw})}{i(h_{sw})} = \frac{1}{1 + r \cdot |1 - a \cdot x|} \tag{3.15}$$

where, $a = L_1 C \omega_s^2$ and x is the percentage of the reactive power absorbed at rated condition. Value of r selected for calculating L_2 is 0.16.

$$L_2 = r \cdot L_1 \tag{3.16}$$

The resonant frequency for an LCL filter [15] is given by ,

Table 3.3 – LCL filter component parameter values

Component	Value
L_1	2.4 mH
L_2	480 μH
C	220 nF
R_d	20 Ω

$$\omega_r = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{3.17}$$

At ω_r, the filter offers zero impedance. Thus necessary damping should be provided at this condition to avoid any oscillations. Hence, the damping value is set to a similar order of magnitude as impedance of series capacitor at resonant frequency. The damping value is selected is selected as $1/3rd$ of the impedance at resonant frequency [15].

$$R_d = \frac{\omega_r \cdot C}{3} \tag{3.18}$$

By using equations 3.13, 3.14, 3.15, 3.16, 3.17 and 3.18, LCL filter component values can be calculated. The parameter values of LCL filter components used in this design are given in Table 3.3.

3.4 Simulation results

PLECS standalone (v.3.7.2) software is used to build the simulation model. MPPT algorithm has been implemented using c-script block. Grid is assumed to be a simple ac 208 V_{rms} voltage source at 60 Hz. PV panel has been model by referring to Trina solar TSM-245 PA05 datasheet. The design of each component has already been discussed in previous sections of this chapter. The I-V and P-V curves of the PV panel modeled is represented in Figure 3.16. Figure 3.17 shows the 350 V DC link voltage along with the panel V_{MPP} voltage and I_{MPP} current. Blue waveform corresponds to I_{MPP} and red corresponds to V_{MPP}.

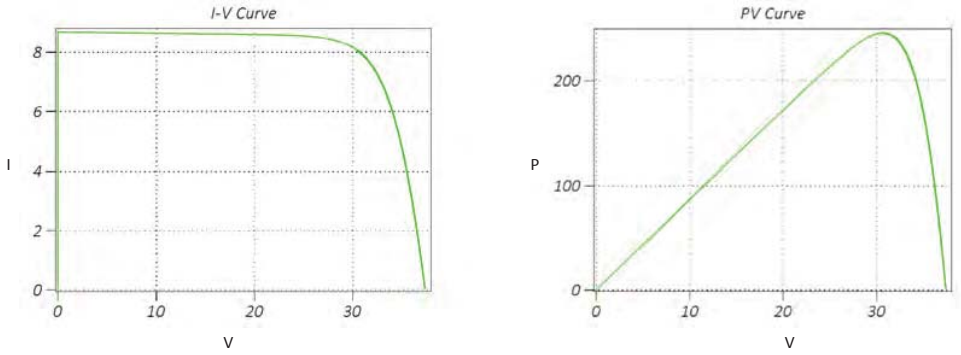


Figure 3.16 – Simulation of I-V and P-V characteristics of PV panel

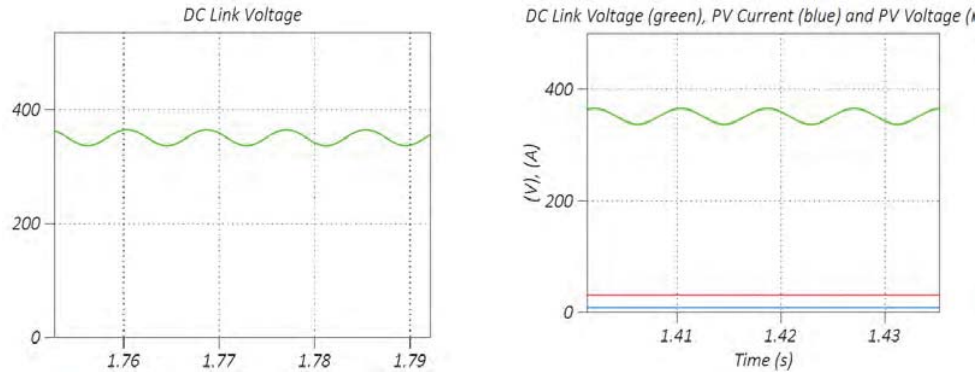


Figure 3.17 – Simulation of input voltage, input current and DC link voltage

Figure 3.18 shows the grid voltage, current and FFT of the grid current. The grid voltage is scaled down so that both voltage and current can be seen in the same window. The schematic of the 250 W micro inverter is as shown in the Figure 3.19.

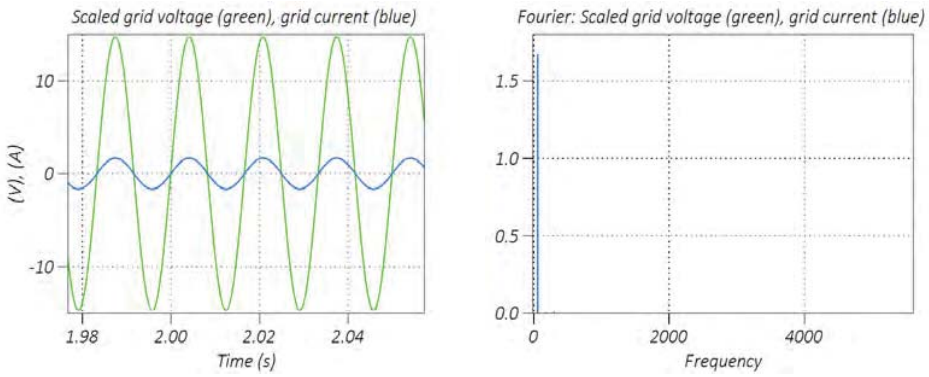


Figure 3.18 – Simulation of grid voltage, current and FFT

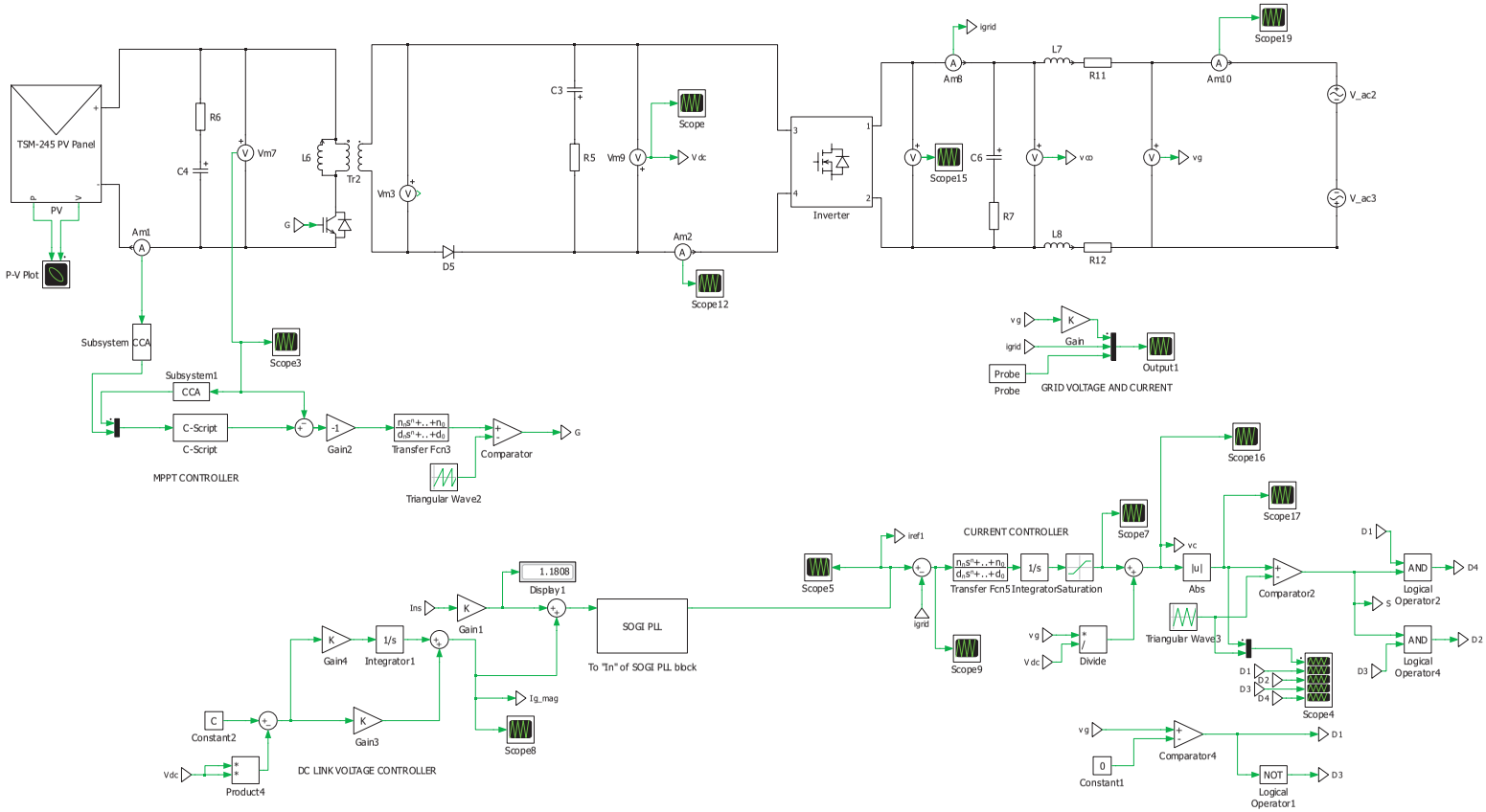


Figure 3.19 – Simulation model of complete solar micro inverter including PV panel

Chapter 4

FAILURE MODES AND EFFECT ANALYSIS OF SOLAR MICRO INVERTERS

4.1 Overview of inverter reliability and its importance

The average cost of PV systems in the US over time is shown in Figure 4.1 [16]. The trend of research in both past and present is more biased towards production costs of PV module technology than the cost of necessary grid connected power electronics. As the cost of PV modules drops, the focus could shift towards inverter cost. Inverters constitute 8-12% of the total lifetime PV cost [17]. The cost of PV system split into different components is shown in Figure 4.2 [16]. It can be observed that the cost is well above the DOE benchmark for 2020.

One of the important factor of the inverter component is inverter reliability. PV modules have long lifetimes with warranties offered up to 25 years. The mean time between failure (MTBF) of these systems in the field have been calculated to be 522 years for residential and 6,666 years for utility systems [18]. Ideally, the inverter has to operate with similar reliability metrics. But in reality, it is necessary to replace or repair an inverter multiple times over the lifetime of PV module. In the case of MLPEs, repairing is mostly impossible since the units are potted with epoxy to sustain extreme environmental conditions. Moreover, incidental costs like loss of power generation during downtime, labor charges will be incurred in addition to the cost of replacing the faulty unit.

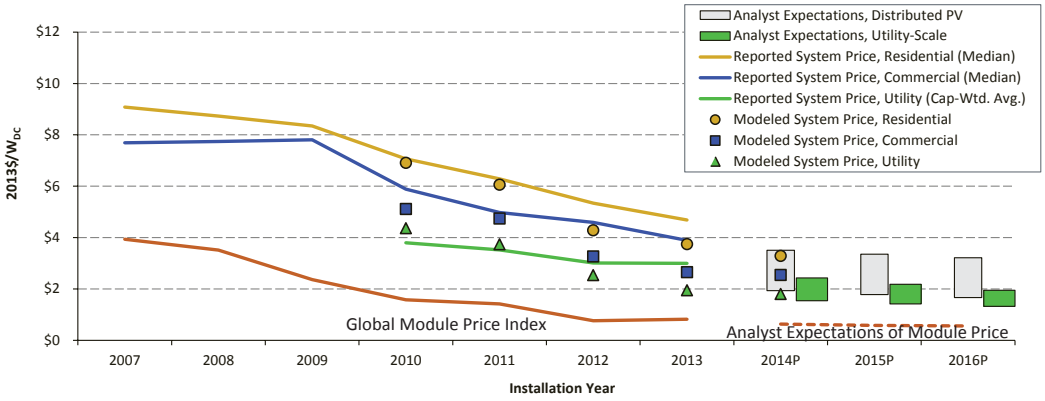


Figure 4.1 – Average PV system cost in the US over time [16]

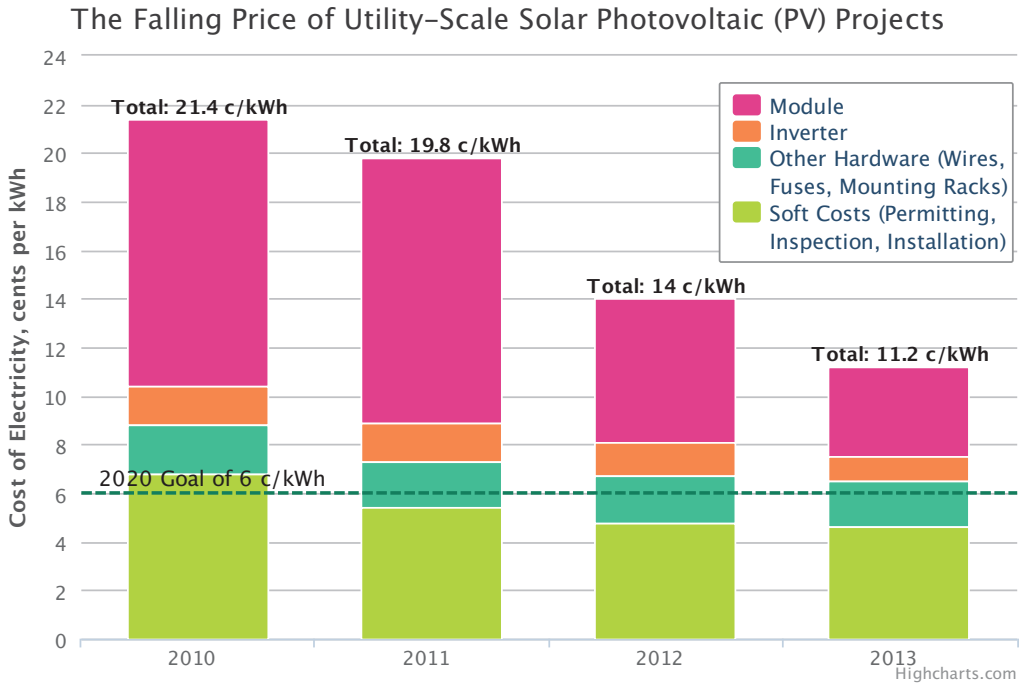


Figure 4.2 – Cost breakup of PV system over time [16]

4.2 Introduction to FMEA

The advantages of module level power electronic devices has been discussed in earlier chapters. As a result, popularity of MLPE devices is rapidly growing in PV industry. On the other hand, there is no established procedure or a tool to assess reliability of MLPE devices. A step towards building such reliability assessment tool has been initiated by PREDICTS (Physics of Reliability: Evaluating Design Insights for Component Technologies in Solar) team which includes micro inverters and micro converters [19]. Essentially, the first step in conducting reliability study is to perform failure mode and effect analysis (FMEA).

Due to the fact that PV power electronics or rather module level power electronics industry is relatively new, it lacks in statistical failure and test data and also the standardized reliability measuring accelerated tests unlike module industry or other more mature power electronics industries. By recommending standard accelerated tests that have been thoroughly correlated to fielded MLPE failure rates, modes and mechanisms, and environmental stressors, the confidence of system operators, integrators, manufacturers, and financiers is increased, decreasing the cost of financing and operating large solar installations. By performing FMEA analysis of the system, the weak links and thus the components that are at risk are exposed.

An FMEA is structured as a hierarchy with orders from largest category to the smallest as shown in Figure 4.3 [19]. From largest category to smallest, the FMEA consists of System $\mapsto$ Subsystem $\mapsto$ Component $\mapsto$ Function $\mapsto$ Failure Mode $\mapsto$ Effect on System $\mapsto$ Failure Mechanisms.

A generic MLPE unit hierarchy has been set up according to Figure 4.4. The MLPE unit is split into subsystems consisting of DC input, Power Conversion Stage, AC output, Control Circuitry, and Enclosure. Each of these subsystems is then broken down by components with functions, effects on the system, failure modes, and failure

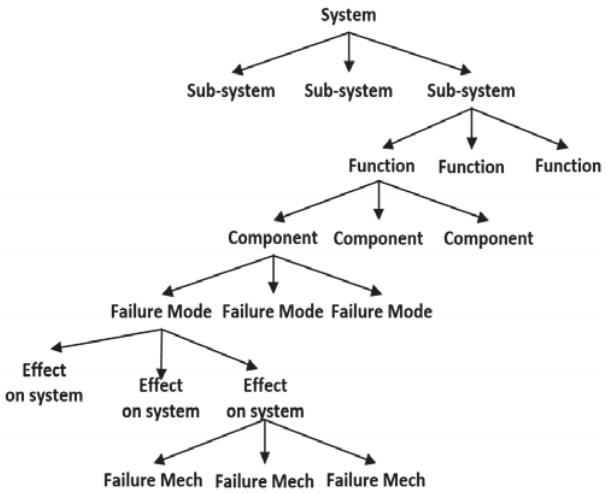


Figure 4.3 – Hierarchy of various stages for FMEA analysis

mechanisms.

The heart of any FMEA is a list of components and all possible failure mechanisms for those components in a device. These failure mechanisms can then be categorized and ranked based on three criteria: occurrence, severity, and detectability [20, 21]. This is done by making bulk list of failure modes and componentry in MLPE devices based on extensive literature and patent searches, details provided by the manufacturers. This type of list is necessary to identify all component level failure modes and mechanisms in an MLPE device. Once the typical components are identified, a list of failure mechanisms and the critical stressors corresponding to these mechanisms is investigated for each of the main components of a micro inverter detailed in Figure 4.4.

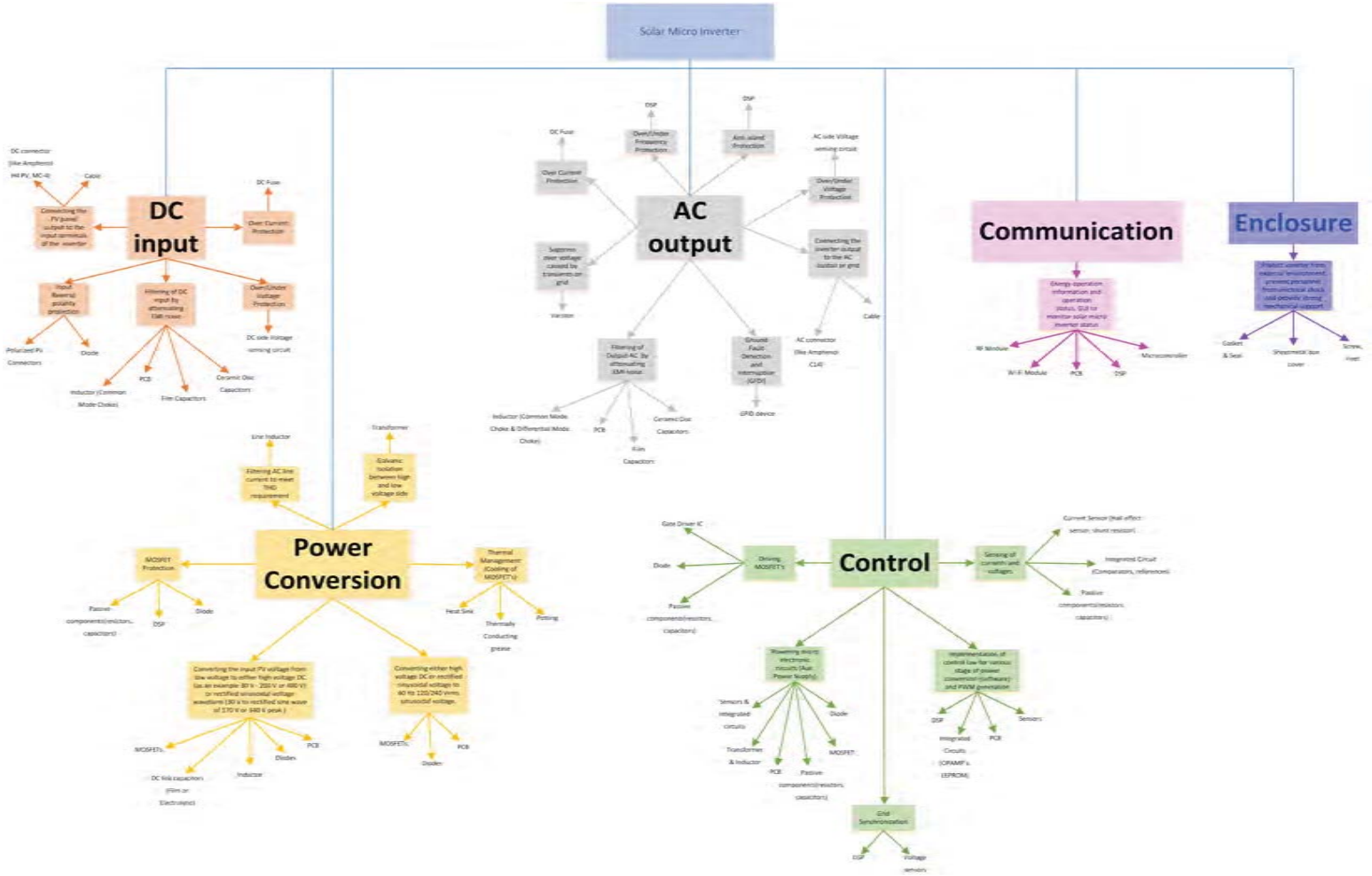


Figure 4.4 – Diagram of FMEA of generic MLPE unit showing subsystems and components

Component	Failure modes	Critical failure mechanisms	Critical stressors
MOSFET	Secondary breakdown	Over voltage/current stress	V_{DS}, I_D
	Gate shorting	Partial puncture of gate oxide by ESD followed by excessive gate voltage	V_{GS}
	Latch-up and triggering of parasitic	Large $\frac{dv}{dt}$ during turn-off triggers the parasitic BJT in power MOSFETs	$\frac{dv}{dt}$
	Shift in device performance characteristics (e.g. threshold voltage, leakage current, transconductance) which eventually leads to device degradation	Electric field distortion by the contaminants in the passivation of the high-field region	Charge effects-Ionic contamination
		Growth of defects in the gate oxide	Hot carrier injection
	Device degradation	Development of slow trapping levels, micro-cracking of aluminium metallization, and electro-migration of metallization	High current densities

Figure 4.5 – Failure modes for MOSFET exclusively

The failures modes of some of the critical components in a solar micro inverter found from extensive literature search are tabulated. The lists corresponding to the power semiconductor devices, capacitors and other passive components are presented in figures 4.5, 4.6, 4.7, and 4.8 respectively. It shows the failure mechanism, failure modes and the critical stressors for the corresponding failure mode found in literature [22–25] for MOSFET, MOSFET and/or diode, different types of capacitors, and other components like inductors, PCB, integrated circuits and so forth, respectively. In figures 4.5, 4.6, 4.7, and 4.8, V_{DS}, is drain to source voltage, I_D, is the drain current, V_{GS}, is the gate to source voltage, V_C is the capacitor voltage, i_c, is the capacitor current, and T_a is the ambient temperature.

This bulk list of components and possible failure modes was used to develop a survey for the industry. The survey was sent to a number of member of the MLPE community to determine which of the possible failure modes were the most important for reliability in a field use environment.

Component	Failure modes	Critical failure mechanisms	Critical stressors
MOSFET and/or Diode	Single event induced burnout	Heavy ions also called cosmic rays when strike the device	External radiation
	Bond wire lift off	Bond failures are caused by crack growth at the bond wire/chip interface. The resulting crack initiation and propagation is driven by stress−strain hysteresis energy loss as the temperature, and hence stress cycles during operation	Temperature swings and different CTEs between Si and Al
	Solder fatigue and cracking between the module substrate and the base plate and/or the device chip and substrate	It arises as the silicon die and copper substrate have different CTE, resulting in a shear stress in the solder layer and eventually cracks (voids). These voids reduce the effective area for heat to escape by conduction from the die; therefore, the die becomes hotter on average, and the process accelerates as the voids grow. The severe localized heating due to increased thermal resistance of the die damages the chip	Initial solder micro structure, substrate metallization, and inter-metallic compounds
	Packaging degradation	Thermo mechanical fatigue stress	Mismatch in the CTE of the different materials in the chip and package, and the local temperature swings. In addition,Humidity, thermal cycling, environmental factors
Schottky Diode	Atomic migration, contact migration	Metallization of the semiconductor	Electromotive force, inter- diffusion, and the mechanical stress during the manufacturing process

Figure 4.6 – Failure modes common for both diode and MOSFET

Component	Failure modes	Critical failure mechanisms	Critical stressors
Al capacitor	Open circuit	Self-heating dielectric breakdown	V_c, T_a, i_c
		Disconnection of terminals	Vibration
	Short circuit	Dielectric breakdown of oxide layer	V_c, T_a, i_c
	Wear out - electrical parameter drift $(C, ESR, \tan\delta, I_{LC}, R_p)$	Electrolyte vaporization	T_a, i_c
		Electrochemical reaction (e.g., degradation of oxide layer, anode foil capacitance drop)	V_c
MPPF capacitor	Open circuit	Self-heating dielectric breakdown	$V_c, T_a, \frac{dV_c}{dt}$
		Connection instability by heat contraction of a dielectric film	T_a, i_c
		Reduction in electrode area caused by oxidation of evaporated metal due to moisture absorption	Humidity
	Short circuit	Dielectric film breakdown	$V_c, \frac{dV_c}{dt}$
		Self-heating due to over current	T_a, i_c
		Moisture absorption by film	Humidity
	Wear out - electrical parameter drift $(C, ESR, \tan\delta, I_{LC}, R_p)$	Dielectric loss	V_c, T_a, i_c, humidity
MLC capacitor	Short circuit	Dielectric breakdown	V_c, T_a, i_c
		Cracking	Vibration
	Wear out - electrical parameter drift $(C, ESR, \tan\delta, I_{LC}, R_p)$	Oxide vacancy migration; dielectric puncture, insulation degradation; micro crack with ceramic	V_c, T_a, i_c,vibration

Figure 4.7 – Failure modes for capacitors [28]

Component	Failure modes	Critical failure mechanisms	Critical stressors
Inductor	Short circuit	Destruction of wire insulation	Local overheating
	Change in inductance value	Cracks in brittle ferrite core	Mechanical stress
PCB	Open circuit	Corner cracking, inner layer cracks	Difference in thermal expansion between copper and epoxy
		Solder joint fatigue	Temperature cycling
	Intermittent shorts, current leakage, dielectric breakdown	Conductive Anodic Filament (metallic electo-migration), Electrochemical migration	Electric field
		CTE mismatch	Temperature cycling
Thick/thin film resistor	Increase in resistance		Transient electrical conditions like burnouts/ power-on
	Open circuit	Cracking/separation of coating	Manufacturing defect, thermal shock
Integrated circuits	Electromigration failure	Mismatch between the incoming and the outgoing ion flux creating a void, which causes an open or short in the metal line	Temperature, current density
	Dielectric breakdown affecting the early life of dynamic memory devices	It is triggered when the electric field reaches the critical value required to cause carrier multiplication	Voltage, temperature, uneven oxide growth
	Degradation of the performance characteristics	Hot carrier generated by the electric field gets trapped either in the bulk of the gate dielectric, or in the interface region between the dielectric and the semiconductor. The trapped carriers perturb the normal distribution of the electric fields leading to the degradation of the device characteristics	Electric field

Figure 4.8 – Failure modes for other components

4.3 Risk priority number (RPN)

In order to identify the most critical components and failure mechanisms, risk priority number (RPN) for each of the identified failure modes are developed. This RPN calculation follows the IEC 60812 2006-01 standard and is an effective approach for quantification of the criticality of the failure mode [20]. The RPN value is calculated by equation 4.1 according to the standard.

$$RPN \;=\; S \cdot O \cdot D \tag{4.1}$$

where 'S' is the severity, which is an estimate of how strongly the effects of the failure will affect the system or the user. This is the measure of severity or criticality of the failure mode and is a non-dimensional number.

'O' is the occurrence, which denotes the probability of occurrence of a failure mode for a predetermined or stated time period. It may be defined as a ranking number rather than the actual probability of occurrence.

'D' is the detectability, which is an approximation of the chance to identify and eliminate the failure before the system or user is affected. This number is usually ranked in reverse order from the severity or occurrence numbers: the higher the detection number, the less probable the detection is. This means that the low probability of detection will yield to higher RPN.

For ranking of failure modes for MLPE products the severity and occurrence are more relevant and hence the detectability factor is omitted. The approach to determine RPN is to obtain the occurrence factor through a survey of major MLPE manufacturers and obtain the severity factor both through a thorough analysis on the various subsystems, their functions, the components involved in each subsystem/function, the failure modes and mechanisms of each component and the effect of

each failure mode on reliability as well as a survey by MLPE manufacturers.

The top at-risk components as identified by the survey are (as per S · O metric):

1. DC and AC Interconnects-Intermittent contact as a result of improper tightening/loose connection
2. Electrolytic capacitors-Open/Short circuit failure of DC link capacitors as a result of wear out
3. Solder joint fatigue as a result of temperature cycling
4. Enclosure-Moisture ingress as a result of corrosion
5. MOSFET/diode-open/short circuit failure as a result of degradation
6. Surge supression devices - as a result of surge

4.4 Survey results

Figure 4.9 shows the pie chart of average ppm for electrolytic capacitor failure and Figure 4.10 shows average failure occurrence (ppm) of various components. Based on these criticalities, the accelerated tests has to be designed. Since the trend of using metallized thin film capacitors (MTFC) in DC link has started, the failure mechanism associated with metallized thin film capacitors are also investigated.

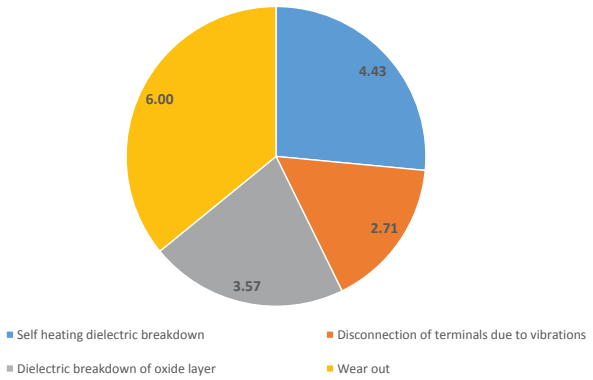


Figure 4.9 – Pie chart representing averaged number(ppm) for various electrolytic capacitor failure mechanism [19]

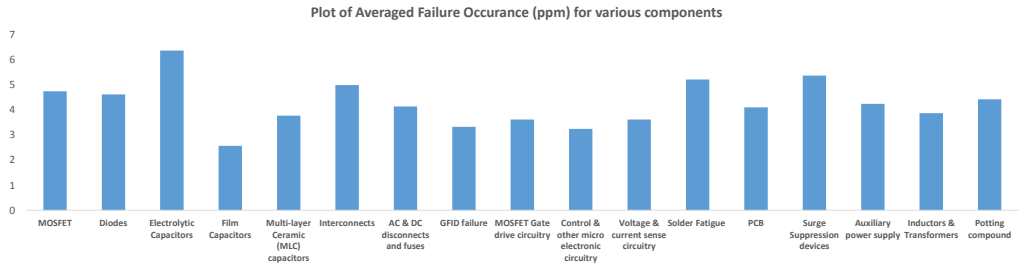


Figure 4.10 – Plot of average failure occurrence (ppm) of various components [19]

Chapter 5

RELIABILITY OF SOLAR MICRO INVERTERS

Analysis of PV systems operated by SunEdison between January 2010 and March 2012 (27 months) shows that 43% of over 3500 tickets were raised for service of inverters because of which 36 kWh of energy was lost. 7% of total energy lost was due to capacitor related issues [26]. In fact, there are debates in the industry regarding reliability of electrolytic capacitors vs. thin film capacitors in inverters. Bus capacitors are considered to be the weakest link of an inverter in terms of reliability, decreasing the inverter lifetime as much as 50% as a result of thermal cycling which increases internal temperatures [27]. Hence it is very relevant to study the performance of solar micro inverters with different capacitors used at DC bus.

5.1 Review of DC bus capacitors

DC bus capacitors are important component in any power electronic circuit. As mentioned earlier, the failure of DC bus capacitor is one of the main concern of power electronic circuit designers. The root cause for this failure can be attributed to various reasons and few important reasons are as follows [28]:

- Considering minimum design margin to gain cost competitiveness for the product without considering the due risk.
- Power converters are exposed to extreme environment and continuous operation in emerging applications like PV and wind inverter.
- Lack of heat dissipation area due to the pressure of increasing the power density.

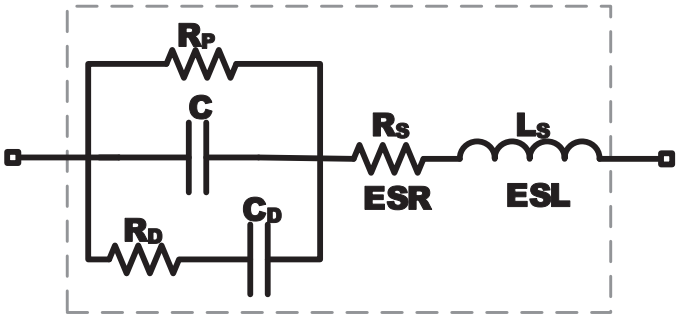


Figure 5.1 – Detailed lumped model of a capacitor

DC bus capacitors could fail due to internal and external factors, such as manufacturing defect, wear-out, factors like operating temperature, current, voltage, humidity, mechanical stress and so forth. Essentially, the failure can be either catastrophic due to over stress or slow failure due to degradation [28]. The degradation or wear out is due to thermal stress and electrical stress.

Mainly aluminum electrolytic capacitors and metallized film capacitors are used extensively as DC bus capacitors. Modern day applications even use ceramic capacitors for DC link, but these are not very popular and hence not considered in this investigation. Most of the commercial solar micro inverter manufacturers disclose that their product is free of electrolytic capacitors. Very few micro inverters use electrolytic capacitor and Enphase is one among them.

The detailed model of DC bus capacitor is as shown in Figure 5.1 where C is the actual capacitance, R_S is equivalent series resistance, R_L is the equivalent series inductance, R_D is the insulation resistance, C_D is the dielectric loss due to dielectric absorption and R_P is the insulation resistance [28]. The value of R_D, R_P and C_D is very small comparatively and hence can be neglected. The simplified model is shown in Figure 5.2 and this model will be considered for simulation. The model shown in Figure 5.2 remains same for both electrolytic and film capacitors.

Figure 5.2 – Simplified lumped model of a capacitor

5.1.1 Electrolytic capacitors

Electrolytic capacitors gets its name from the way it is manufactured. The oxide layer is deposited on the surface of electrode by an electrochemical process, which acts as dieletric. The most commonly used oxide are formed using aluminum and tantalum. Zirconium, niobium, hafnium, titanium and few other metals also exhibit excellent dielectric properties but these are not commercialized in large scale. The electrode on which oxide is deposited is made to act as anode. Thus the electrodes are polarized in this capacitor.

Failure modes

Electrolytic capacitors have two primary modes of failure, physical and chemical. The primary physical failure mechanism for electrolytic capacitor is vaporization of the electrolyte through polymer seals. A decrease in the volume of the electrolyte leads to an increase in the capacitor ESR [29]. Vaporization of the electrolyte may be driven by increased internal temperatures due to ripple current or simple evaporation through poor quality sealing. Many researchers cite electrolyte vaporization as the primary wear out mechanism for electrolytic capacitor [29, 67].

The failure of electrolytic capacitors can broadly be classified as physical and chemical failures [29]. The physics is related to vaporization of electrolyte. There is not much space for the vapor to escape. The possible path is through the polymer seal which has tiny pores in them. The cross sectional view of electrolytic capacitor is depicted in the Figure 5.3 [30]. The major chunk of series resistance in an electrolytic

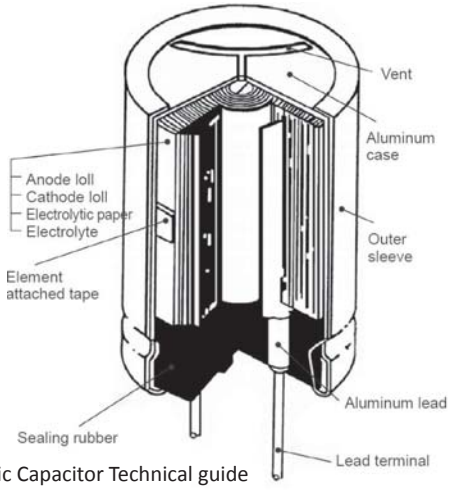


Figure 5.3 – Cross-sectional view of electrolytic capacitor [30]

capacitor is contributed by electrolyte. In order to reduce this, capacitor manufacturers have come up with electrolytes with large percentages of H_2O (∼75-85%). This H_2O content helps in oxide reformation. Under ideal case, the leakage current in the electrolytic capacitor drives a H_2O/Al reaction which reforms any compromised Al_2O_3 [29].

$$Al(OH)_3 \longrightarrow 2AlO(OH) + 2H_2O \longrightarrow Al_2O_3 + 3H_2O$$

$$2Al + 6H_2O \longrightarrow 2Al(OH)_3 + 3H_2$$

$$2Al + 3H_2O \longrightarrow Al_2O_3 + 3H_2 \uparrow$$

From the chemical reaction, it is evident that the H_2O content helps in reforming the oxide. On the other hand, this is done at the expense of consuming H_2O which further increases the equivalent series resistance (ESR). In addition, the liberation of H_2 gas increases the internal pressure of the capacitor. The bulging of electrolytic ca-

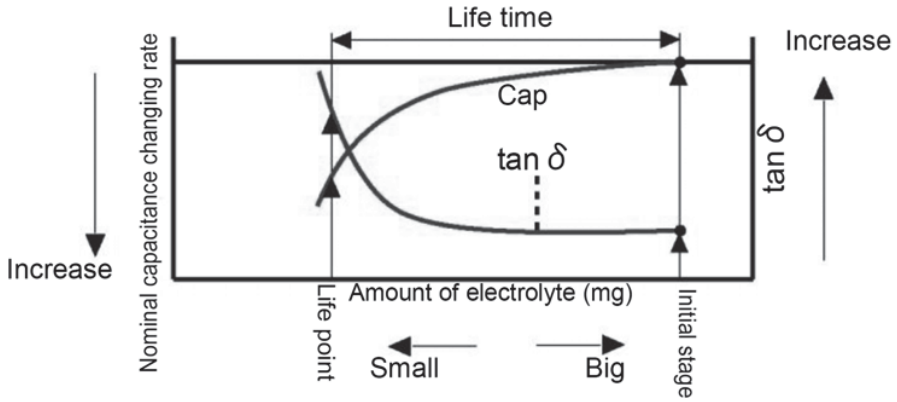


Figure 5.4 – Characteristics of degradation of electrolytic capacitor [30]

pacitor is due to this reaction. Once the interior pressure reaches ∼7 atm, the pressure relief valves release, bursting the capacitor can thereby destroying the capacitor [29].

The degradation of electrolytic capacitor is better explained in Figure 5.4 [30]. The degradation precursor for an electrolytic capacitor is therefore its capacitance C, ESR or combination of both. The end of life criteria for an electrolytic capacitor from an industry stand point is considered to be 20% reduction in its capacitance from initial value and/or increase in ESR ∼ 2-3 times from its initial value [28].

5.1.2 Metallized film capacitors

These capacitors are existing from many years. The advancement in this capacitor technology has brought the price down by significant margin. They are being extensively used. Film capacitors are considered to be more reliable compared to electrolytic capacitors. They make use of a plastic film as dielectric. Plastic film coated with extremely thin layers of alloys like zinc or aluminum through vacuum deposition to form the electrodes. These two films are tightly held together and wound. This ends are sprayed with metal to form the external electrical connection terminal [31]. The biggest advantage of film capacitors is its self healing property

of dielectric. Materials like polypropylene, polyester, teflon, mylar and so forth are mostly used as the dielectric in these capacitors.

Failure modes of metallized film capacitor

The most commonly found failures in metallized film capacitors are breakdown of self healing dielectric material, failure due to moisture ingress and detachment of terminals. All film capacitors have one or the other defects. They can range from air pockets to foreign particles to inconsistencies in dielectric film. In these regions, the breakdown voltage is much lower than rated voltage. Manufacturing defects or inherent impurity in dielectrics forms the weak links. When the electrical stress increases, these points breakdown and the dielectric recovers itself. At each localized breakdown instance, there is a small loss in capacitance. Due to many such events, the dielectric looses its strength. When the energy released during breakdown in beyond the energy required for self healing, the capacitor breaks down [32]. Certain gasses are discharged during each breakdown instance. These are trapped inside due to lack of exit paths. These gases breakdown at certain temperature and pressure under application of voltage and starts conducting thereby failing the capacitor. In case of PV inverters, moisture ingress is a serious concern since micro inverters operate in outdoor environment. In the case of moisture ingress, the terminals experience oxidation and leads to loss of contact. The terminal contacts are lost even when capacitors are subjected to vibrations.

5.1.3 Degradation modeling

Since most of the commercial micro inverters use metallized film capacitors in the DC link, it is very important to study the effect of degradation on the performance of the system. Figure 5.5 shows the degradation profile of metallized film capacitors over time in general [29]. The accelerated test performed on actual film capacitors

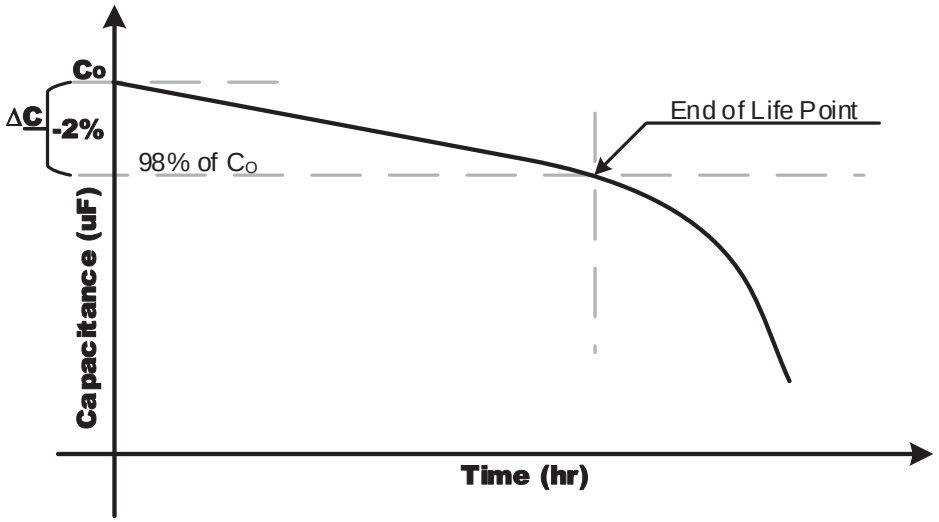


Figure 5.5 – Characteristics of degradation of electrolytic capacitor

proves that the degradation profile is correct and it is as shown in [31, 33, 34]. The degradation precursors for film capacitor is its capacitance and dissipation factor. Dissipation factor is related to ESR of the capacitor. According to industry standards, the end of life criteria for film capacitor is 2% to 5% reduction in capacitance from initial value and/or increase in dissipation factor by two times.

From the Figure 5.5, it is evident that the degradation is linear till the point of end of life. From there on, the curve becomes non-linear and leads to faster degradation. Hence, film capacitors must not be operated beyond the end of life point. If there is a failure, it is soft failure or fails safe till this end of life point. After this point, the failure is catastrophic. The physics behind this that till end of life point, the phenomenon of self healing breakdown takes place. At the end of life point, the capacitance has become weak but still operational. On further usage, the vapor trapped inside can be ionized start to conduct. This results in short circuit and leads to failure of components and equipments down the lane. On the other hand, the findings from simulation is that till the end of life point, the change in performance and its impact on the system is negligible. Hence in complex and expensive power

converters, health monitoring of these capacitors are employed [35].

In chapter 3, the micro inverter which is modeled uses $66\mu F$ film capacitor. A commercial film capacitor of $66\mu F$, 450 V with an ESR of $5m\Omega$ is found from component database [36]. The expression for degradation of this capacitor with respect to time is obtained by performing polynomial fitting and is given by equation 5.1.

$$C(t) = -3 \cdot 10^{-7} \cdot t^4 + 1 \cdot 10^{-6} \cdot t^3 - 2 \cdot 10^{-6} \cdot t^2 + 8 \cdot 10^{-7} \cdot t + 7 \cdot 10^{-5} \quad (5.1)$$

Since the simulation cannot be run for the entire time of actual degradation, mathematical manipulations are performed to simulate 1600 h data in 3 s. Similarly, the ESR variations are also incorporated and is given by equation 5.2.

$$R(t) = 0.003 \cdot t^6 - 0.0194 \cdot t^5 + 0.0456 \cdot t^4 - 0.0472 \cdot t^3 + 0.0218 \cdot t^2 - 0.0036 \cdot t + 0.005 \quad (5.2)$$

The variable capacitance and variable resistance components in PLECS component toolbox are used. The implementation of degradation in PLECS is as shown in Figure 5.6. The degradation profile from PLECS simulation is shown in Figure 5.7 for C and ESR.

The micro inverter was simulated with these degradation profiles. The waveforms across various points of interest is captured. Figure 5.8 shows the variation of DC link voltage over time. Time $t = 3s$ corresponds to end of life point. It can be observed that as the capacitor degrades, the ripple voltage increases. After 3 s, the ripple increases abruptly which denotes catastrophic failure. It is also important to note that till 3 s, the change in ripple is not significant. Figure 5.9 shows the zoomed waveforms of ripple at initial and end of life conditions. Figure 5.10 shows the grid current distortion due to increase in ripple voltage across DC bus.

The 66 μF film capacitor is simulated at two specific conditions - pristine and end

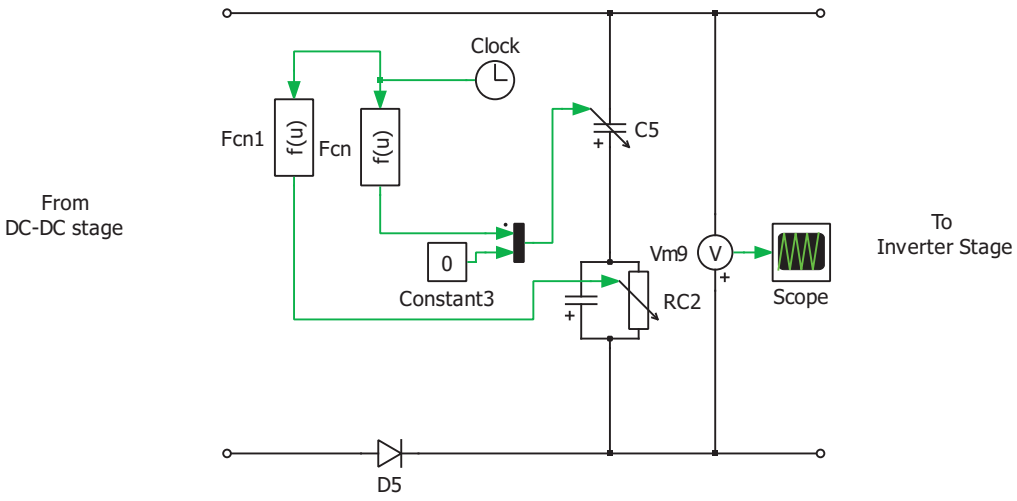


Figure 5.6 – Implementation of degradation in PLECS

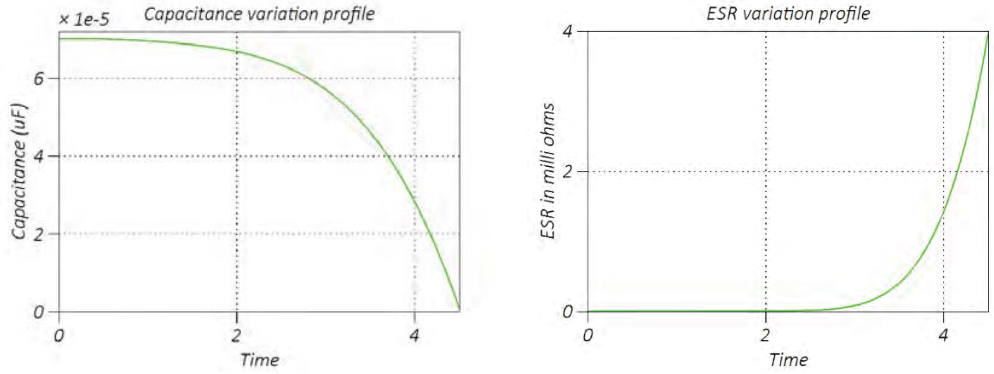


Figure 5.7 – Simulation of degradation of C and ESR over time

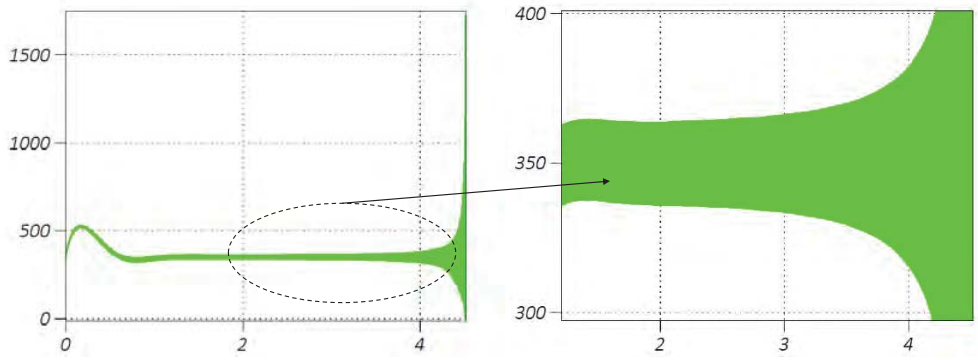


Figure 5.8 – Simulated DC link voltage variation with degradation of C and ESR modeled

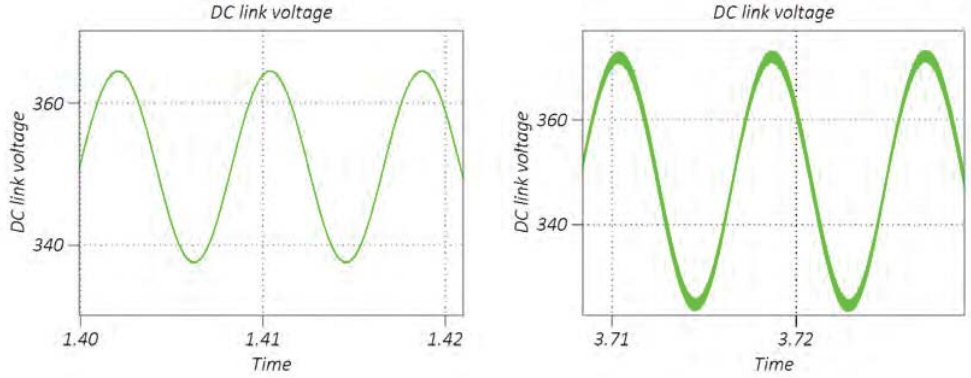


Figure 5.9 – Comparison of the DC link ripple waveforms (zoomed waveforms of Figure 5.8) (a) Capacitor in pristine condition (b) Capacitor in end of life condition

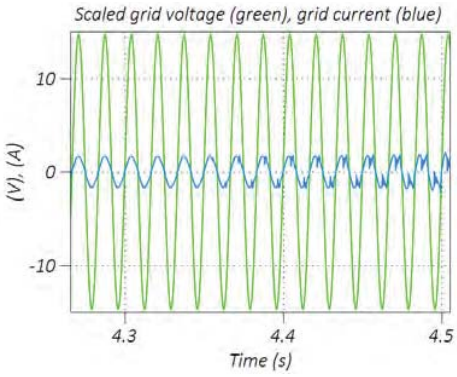


Figure 5.10 – Impact of capacitor degradation on grid voltage and current

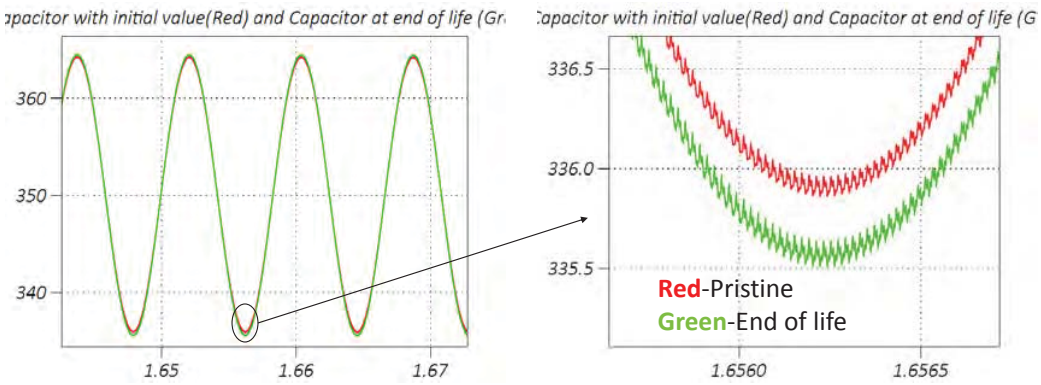


Figure 5.11 – DC link voltage with film capacitor in DC link

of life. The ripple in DC link voltage is analyzed. Figure 5.11 shows the waveforms of DC link voltage at these two conditions. The red waveform corresponds to capacitor in pristine condition and the green waveform corresponds to capacitor in end of life condition of film capacitor. This proves that till the end of life condition, the performance change is not very significant. On the other hand, it can be said that it could go unnoticed. But as seen in previous waveforms, the capacitor may fail short and bring down the inverter if they are not replaced.

In order to compare the ripple in DC link voltage with electrolytic capacitor, electrolytic capacitor is considered for DC link design. Unlike film capacitor, electrolytic capacitor is selected based on ESR requirements [37]. As a rule of thumb, the capacitance is around ten times that of film capacitors. Hence the commercially available electrolytic capacitor of 680 μF 450 V and ESR of 362.5$m\Omega$ used in PV applications is selected [38]. The model is simulated for two conditions - capacitor in pristine and end of life condition. Figure 5.12 shows the ripple voltage in DC link. The red waveform corresponds to capacitor in pristine condition and the green waveform corresponds to capacitor in end of life condition of electrolytic capacitor i.e., reduction in capacitance by 20% and increase in ESR by 200%. It is evident that there is considerable increase in ripple voltage as the capacitor is degraded.

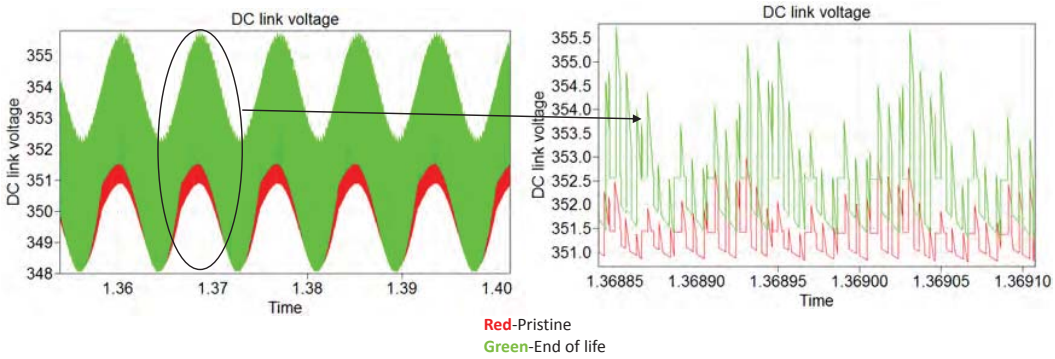


Figure 5.12 – DC link voltage with electrolytic capacitor in DC link

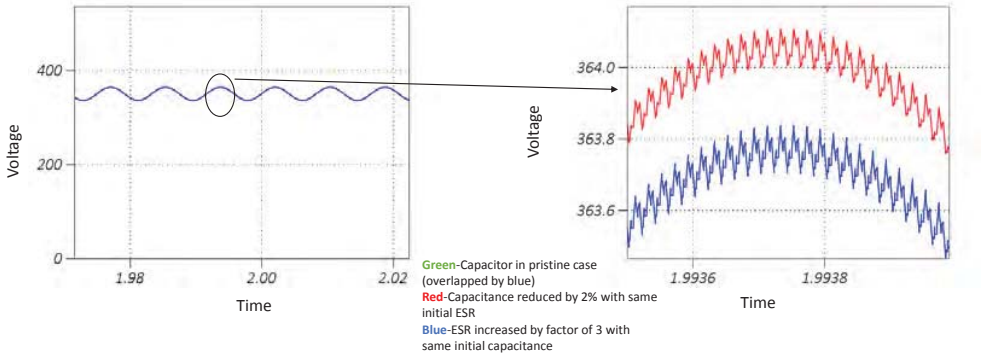


Figure 5.13 – DC link voltage with film capacitor operated with different degradation profiles

Figure 5.13 corresponds to a case where in only capacitance or only ESR or both are varied over time for a film capacitor. The green waveform (overlapped by blue waveform) corresponds to capacitor in pristine condition. The red waveform corresponds to a condition where only the capacitance is reduced to 98% of its initial value but ESR is retained to initial value. The blue waveform corresponds to the condition where capacitance is retained in its initial value but ESR is increased by a factor of three. Though the change in ripple is not very significant, the results gives the direction that impact of decrease in capacitance is more.

5.2 Grid transients test

A dedicated design qualification standard is unavailable for PV inverters. By doing so, the reliability and quality of PV inverters can be improved. Electric stress has been identified as one of the missing link in testing PV inverters [39]. IEEE has proposed surge testing for low voltage connected equipments through recommended practices document like IEEE 62.45 [40]. IEC also has a standard on surge testing and surge measurement techniques [41, 42]. The parent document for all the surge testing, measurement standards and recommended practices are IEC 61000-4-4 and IEC 61000-4-5 standards [41, 42].

According to [43], Surge is a word used to describe a sudden rise in voltage, beyond the normal system voltage, that lasts less than one cycle. IEEE 62.41.1 discusses about the relevance of conducting this test. It says that "These problems have received increased attention in recent years because of the widespread application of complex semiconductor devices that are more sensitive to voltage surges than vacuum tubes, relays and earlier generations of semiconductor devices" [44].

The reason behind surge testing is to determine the immunity level of the equipment under test for withstanding surge. This is done at different levels for different equipments. Types of surge tests are design test, qualification test, production test and diagnostics test. The consequence of these tests could either upset the operation of EUT, damage the EUT permanently, or there could be no change to the operation of EUT. Surge test can also be either powered or unpowered. The powered tests are basically carried on electronic units and unpowered tests are usually done to qualify non electronic components like connectors, mechanical parts and so forth.

The standards define two basic surge waveforms namely ring wave surge and combination wave surge. Figure 5.14 shows the normalized waveform of standard 100 kHz ring wave surge. No short circuit current wave is specified for ring wave

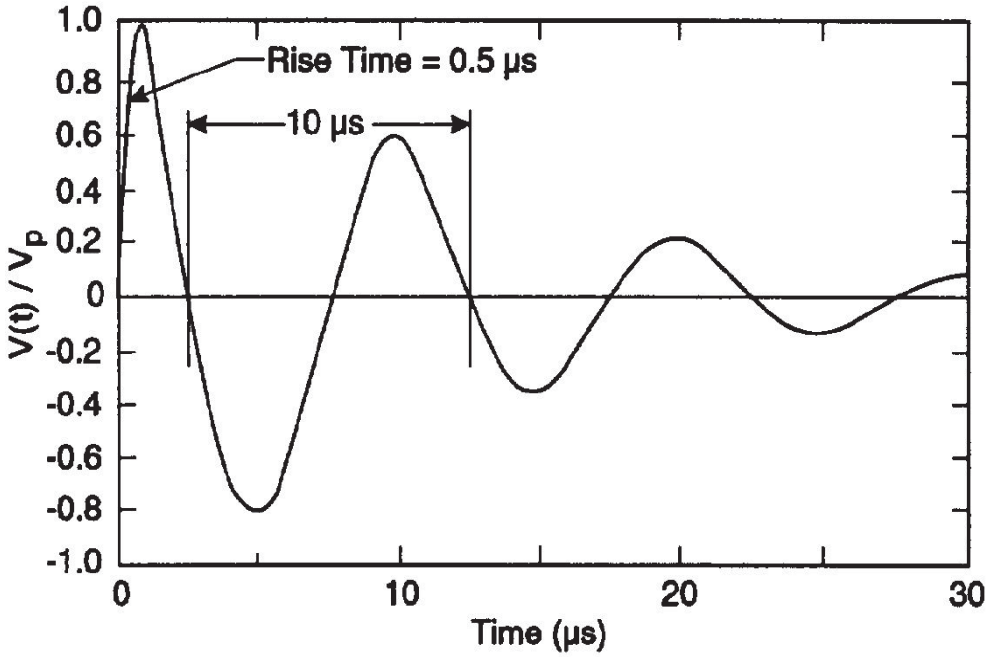


Figure 5.14 – 100 kHz Ring wave surge according to IEC and IEEE standards [44]

surge. Combination surge has two waveforms namely open circuit voltage and short circuit current. Figure 5.15 shows the normalized voltage waveform of combination wave surge and Figure 5.16 shows the normalized shot circuit current waveform of the combination wave surge. The typical rise time and the duration of each of these waveform are also depicted in their respective figures. The intensity of surge to be applied has also been mentioned in the standards which corresponds to different environmental exposure levels [40, 42]. Historically, the open circuit waveform was applied to test the BIL of insulators and the short circuit waveform was used to test the surge protection devices. Both these waveforms are the after effects of surge and hence they are applied together [45].

IEEE 62.41 proposes different surge waveforms for the test based on the location and exposure level of the equipment under test. Figure 5.17 shows the picture representing the locations categorized by IEEE 62.41 as locations- A,B and C. Location C corresponds to equipment being placed just at the service entrance or slightly out-

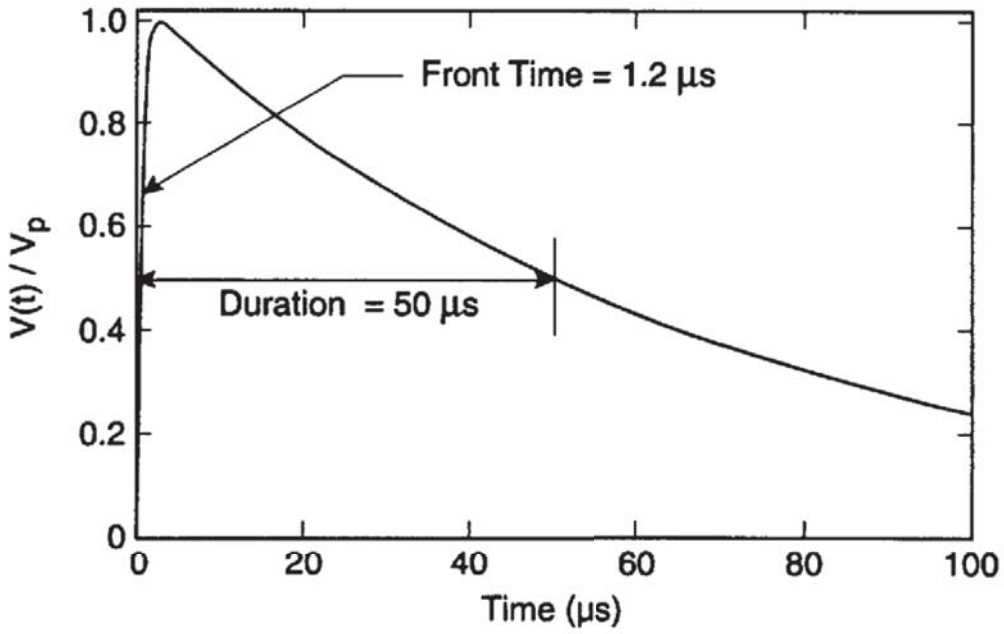


Figure 5.15 – Open circuit voltage waveform of combination surge according to IEC and IEEE standards [44]

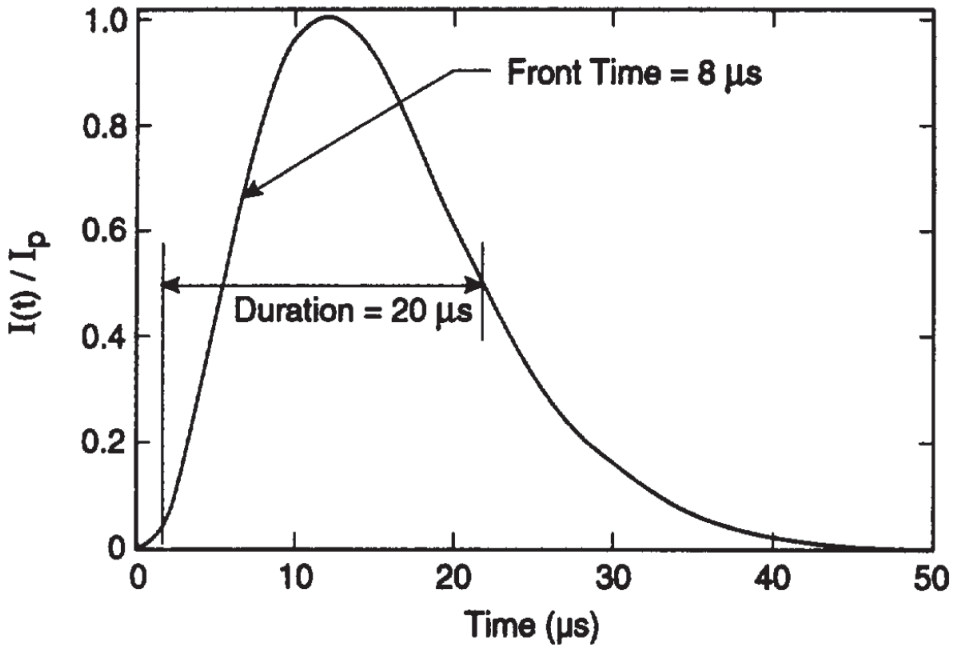


Figure 5.16 – Short circuit current waveform of combination surge according to IEC and IEEE standards [44]

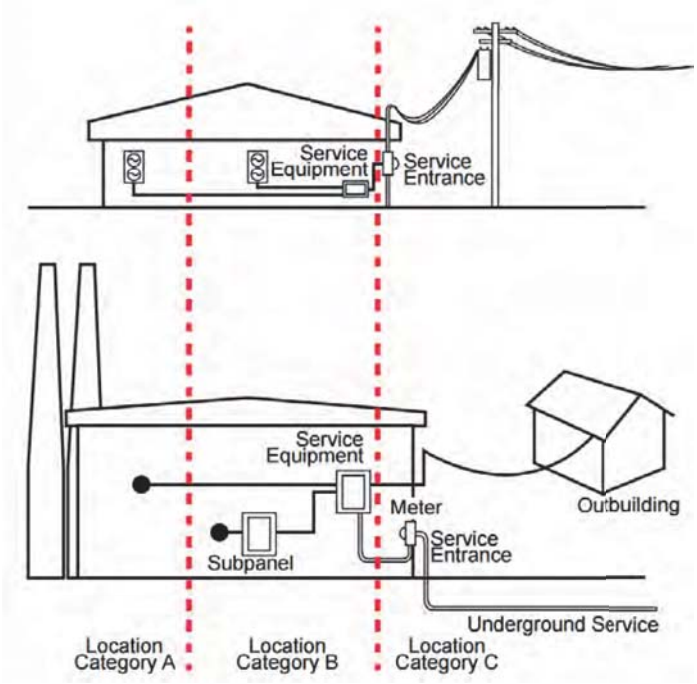


Figure 5.17 – Location category according to IEEE 62.41 [44]

side. Location A corresponds to equipment being placed at a certain distance from the service entrance and location B is in between the two.

Exposure levels are categorized as low medium and high in IEEE 62.41. Surges can also be generated due to switching transients. Low exposure corresponds to low lightning areas and less switching activity. Correspondingly, medium and high exposure areas have high lightning and switching activity. It is always better to have the information of lightning density of a particular location of interest rather than just knowing just the number of strikes. Figure 5.18 shows one such map for the United States of America in 2014 [46].

Considering solar micro inverter to be the equipment under test whose usage will be in the US, it is best to select location B or location C for the location category and medium exposure level [43].

With the idea of location and exposure level, Table-1 in IEEE 62.45-2002 suggests

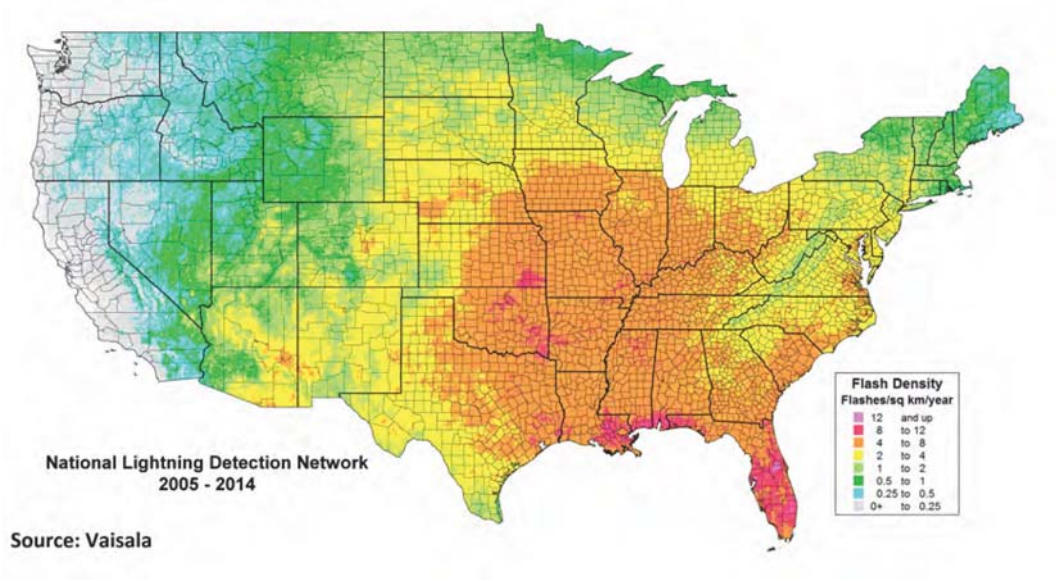


Figure 5.18 – Flash density maps for the US in 2014 [46]

the test waveforms to be both standard ring wave and standard combination wave [40]. The open circuit voltage suggested is 6 kV. The short circuit current is indirectly suggested via source impedance i.e., the source impedance of the surge generator is dictated by the standard. For a combination wave generator, the source impedance suggested is 2 Ω. Hence short circuit current is given by equation 5.3 and it comes to 3 kA.

$$I_{SC} = \frac{V_{OC}}{Z_S} \tag{5.3}$$

5.2.1 Implementation of surge waveform

The surge waveforms shown in figures 5.14, 5.15 and 5.16 can be implemented by designing electronic surge generators with complex wave shaping circuitry. It is not a easy task to generate surge wave form with precise timings and wave shape. In practice, electronic surge simulators are available in the market. Since this thesis deals with simulation study, mathematical modeling approach is chosen. The equation to generate these surge waveform has been mentioned in IEEE 62.45 and IEC 61000-4-5.

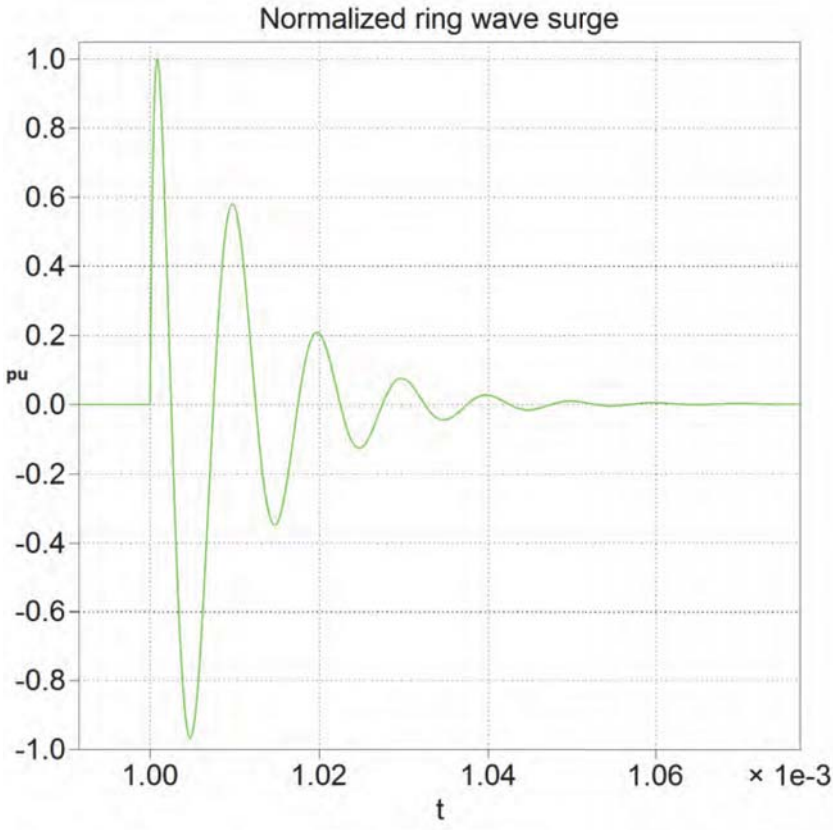


Figure 5.19 – PLECS implementation of 100 kHz ring wave surge

100 kHz ring wave open circuit voltage waveform is given by the equation 5.4 where, τ_1 is 0.533 μs, τ_2 is 9.788 μs, ω is $2.25 \cdot 10^5$ rad/s, and A is 1.590. V_p is the magnitude of the surge to be generated. Figure 5.19 shows the PLECS implementation of ring wave surge.

$$V(t) \;=\; AV_p\big(1 - e^{\frac{-t}{\tau_1}}\big)e^{\frac{-t}{\tau_2}}\cos(\omega t) \tag{5.4}$$

The expression for combination wave surge is expressed in equation 5.5 and 5.6. In equation 5.5, V_p is the magnitude of open circuit voltage, τ_1 is 0.4074 μs and τ_2 is 68.22 μs and A is 1.037 and in equation 5.6, I_p is the magnitude of the short circuit current, τ is 3.911 μs and A is 0.01243 $(\mu s)^{-3}$. PLECS implementation of

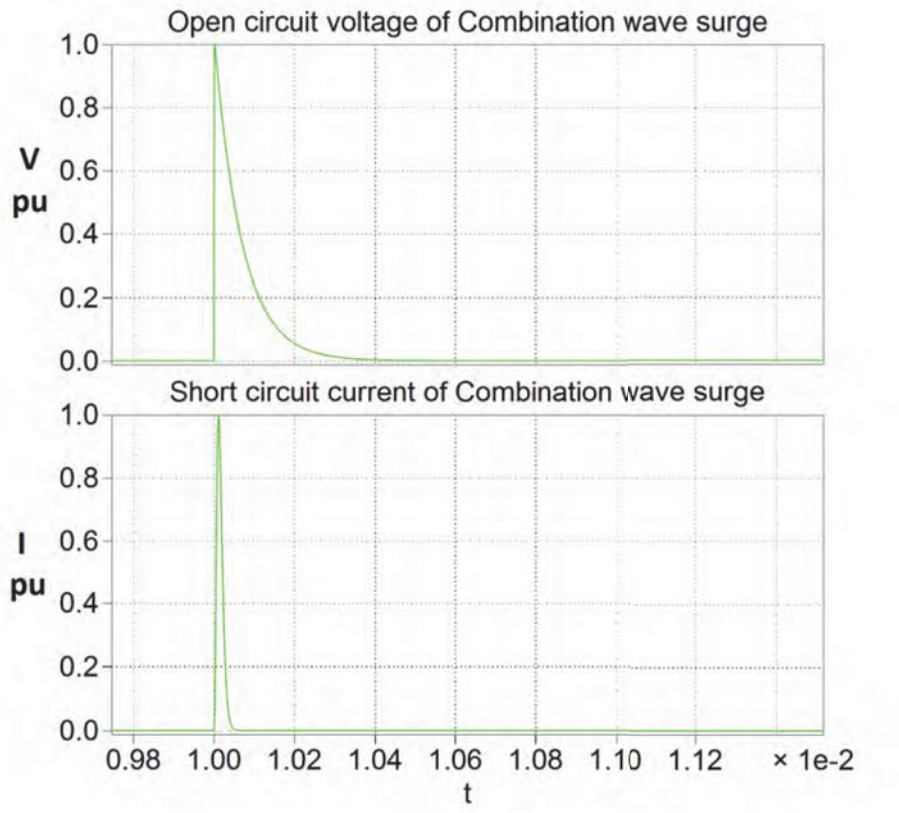


Figure 5.20 – PLECS implementation of combination wave surge

combination wave surge is shown in Figure 5.20.

$$V(t) \;=\; AV_p\big(1 - e^{\frac{-t}{\tau_1}}\big)e^{\frac{-t}{\tau_2}} \tag{5.5}$$

$$I_p(t) \;=\; AI_p t^3 e^{\frac{-t}{\tau}} \tag{5.6}$$

5.2.2 Back filter

IEEE and IEC standard recommend the use of decoupling network to be connected in between grid and EUT. It is known as back filter. This ensures that the surge

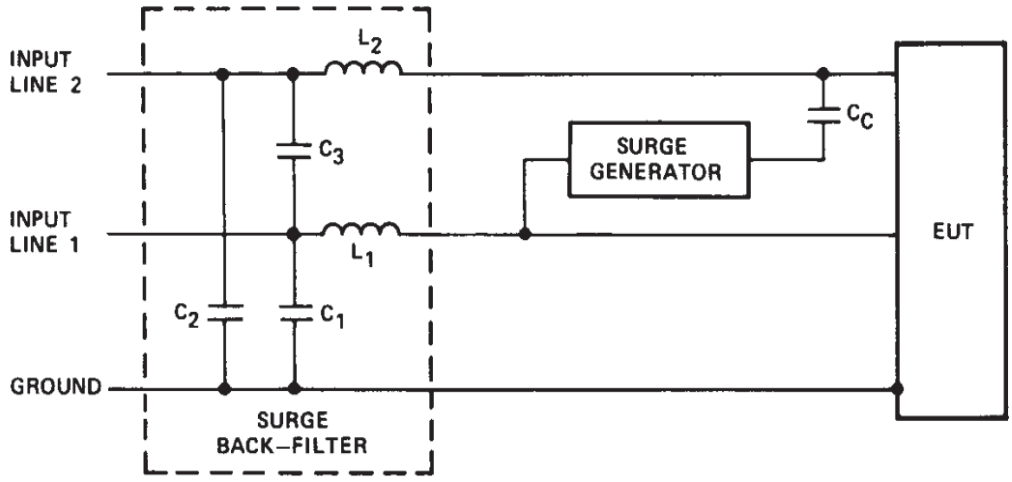


Figure 5.21 – CDN configuration with shunt coupled surge generator to EUT [45]

waveform does not flow through the grid but only through EUT. Similarly, in order to avoid load of the generator, the standard recommends a coupling capacitor. The structure of coupling and decoupling network (CDN) depends on the configuration of EUT, i.e., single phase or three phase, and if the surge is to be applied between line to line or line to neutral. The detailed explanation is given in [40]. Since the system being modeled is single phase, the surge is applied between line and return path. The configuration of the coupling decoupling network for single phase EUT is as shown in Figure 5.21 [45]. In this figure, the shunt coupling of surge generator is seen.

For this kind of coupling, the standard suggest coupling capacitor C_C to be 18 μF. If the current through the EUT is less that 16 A at rated conditions, then as per IEC 61000-4-5, inductors L_1 and L_2 in Figure 5.21 can be any value less than 1.5 mH. It is important to note that the voltage drop across this inductor should not exceed 10% of the grid voltage. This filter should offer low impedance to line frequency current and high impedance to high frequency. Essentially it is a low pass filter. Usually the rule of thumb is to use the inductance of 1.5 mH if the current through the EUT is less [42]. Figure 5.22 shows the implementation of surge generator and back filter. The value of inductor chosen is 1.5 mH and the capacitance is 500 μH so that cut-off

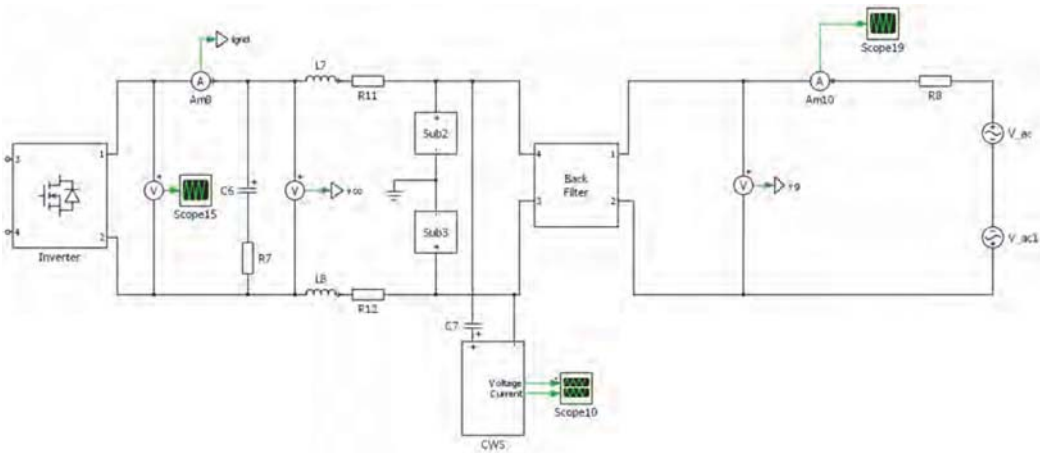


Figure 5.22 – PLECS implementation of surge generator and back filter

frequency is 180 Hz.

5.2.3 Simulation of application of surge waveform

Figure 5.23 shows the 6 kV combinational wave surge applied on the micro inverter. The impact of this surge on the system is analyzed. Figure 5.24 shows the DC link voltage waveform. It can be observed that due to application of surge, DC link voltage shoots up by 75 V. Figure 5.25 shows the waveform across upper and lower switch of the inverter. It can be observed that there is a short duration spike of about 19 A through the upper switch and voltage variation is not significant. On the other hand, from the lower switch waveform, it is evident that the current spike causes the voltage across the inductor to rise and hence there is voltage spike across the lower switch. There is no current spike in the lower switch.

Varistor model

Figure 5.26 depicts the model of varistor. Varistor has been modeled as current dependent voltage source according to [47]. Figure 5.27 shows the current through the varistor. The V-I characteristics of varistor is as shown in Figure 5.28. The VI

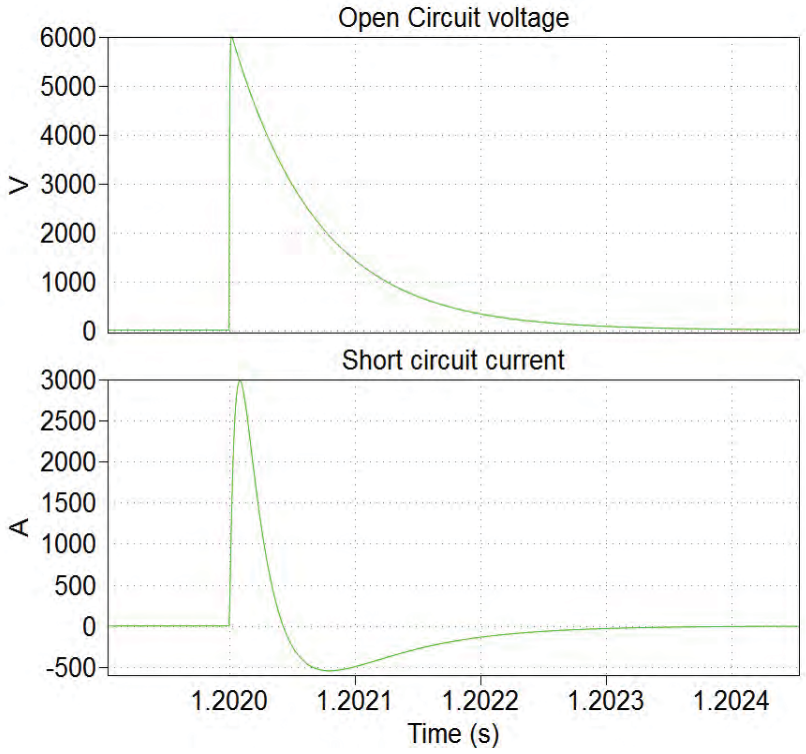


Figure 5.23 – PLECS implementation of 6 kV combinational wave surge

characteristics is plotted on linear scale in PLECS since it cannot plot on log scale. EPCOS S20K275 varistor is considered for the model and its VI characteristics is as shown in Figure 5.29 [47]. The data is exported on MATLAB and plotted on log scale. It is very difficult to mathematically model a varistor due to its extreme non linearity and hence a very basic approximate model has been used. Figure 5.30 shows the grid waveforms due to surge. The disturbance in the grid current is due to effect of the surge. The grid current shoots up by almost 16 A in both the direction mainly because of the discrepancy in the varistor model. The grid current controller and PLL controller is robust enough to control the grid current within limits and bring it back in shape.

6 kV ring wave surge is also applied on the system to study its impact. The standard does not recommend any short circuit current waveform for ring wave surge. The impact of ring wave surge on system is not significant compared to combinational

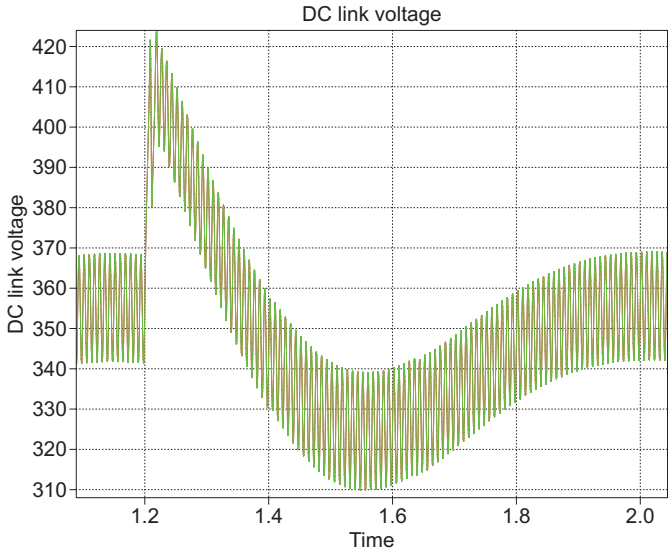
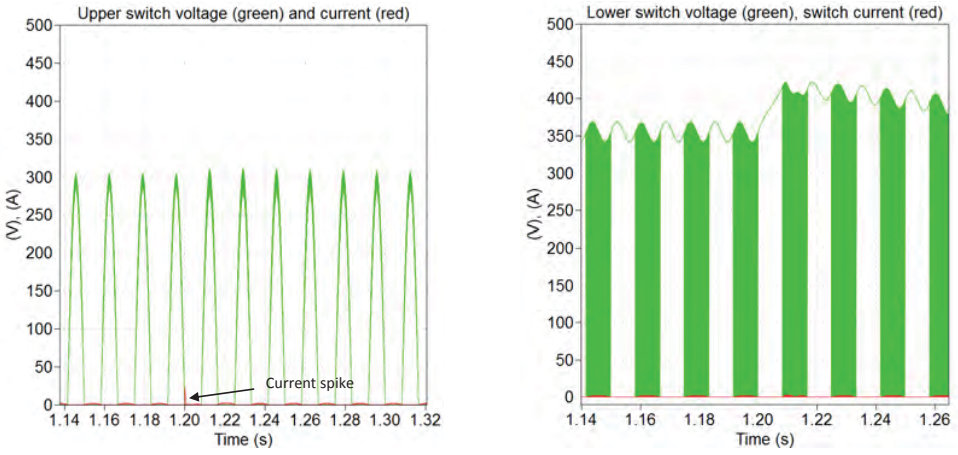


Figure 5.24 – Impact of 6 kV combinational wave surge on DC link voltage



Upper switch Lower switch

Figure 5.25 – Voltage across low side and high side switches of inverter

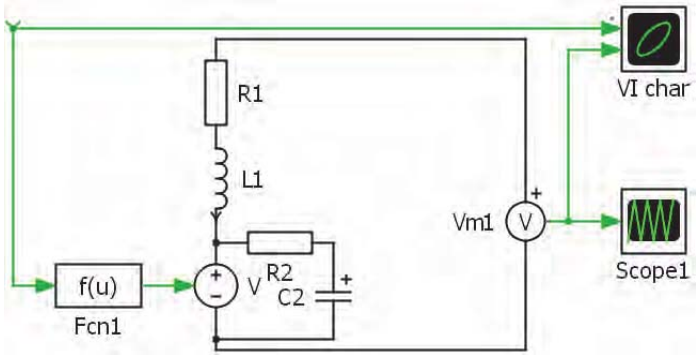


Figure 5.26 – PLECS implementation metal oxide varistor

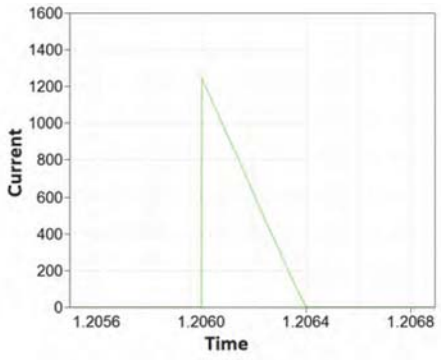


Figure 5.27 – Current through varistor during surge

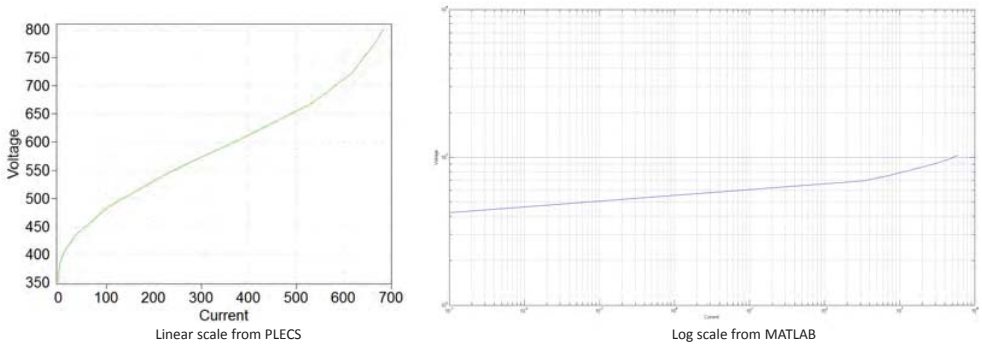


Figure 5.28 – VI characteristics of the modeled varistor

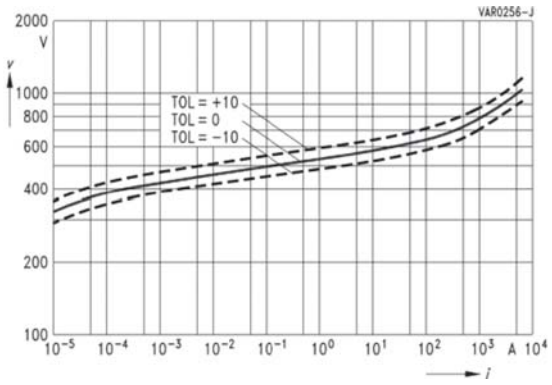


Figure 5.29 – VI characteristics of EPCOS S20K275 [47]

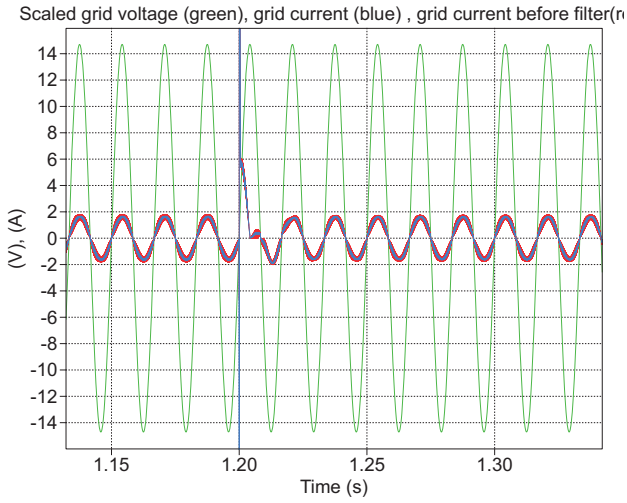


Figure 5.30 – Grid voltage and grid current distortion due to combination wave surge

wave surge [48]. Figure 5.31 and 5.32 shows the impact of ring wave surge on DC link voltage and the grid voltage and current. The DC link voltage sees a rise in voltage of almost 40 V. In fact, if the system has immunity to combinational wave surge, then it is mostly guaranteed that the system can sustain the impact of ring wave surge, which infers that combinational wave surge is critical [48]. Ring wave surge test is essential and becomes critical if the equipment will be operated in location-A where the length of cables are significant and offers higher inductance.

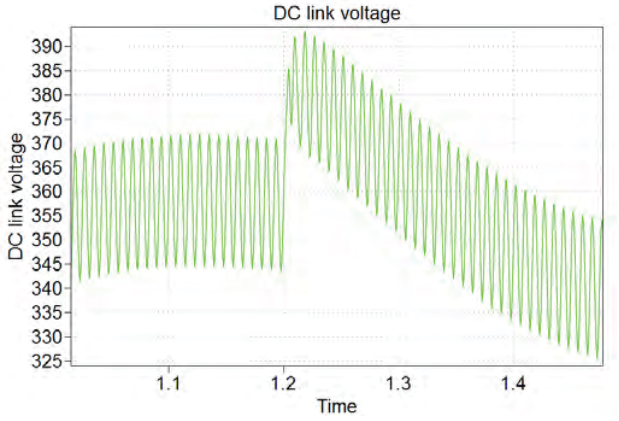


Figure 5.31 – DC link voltage distortion due to 6 kV ring wave surge

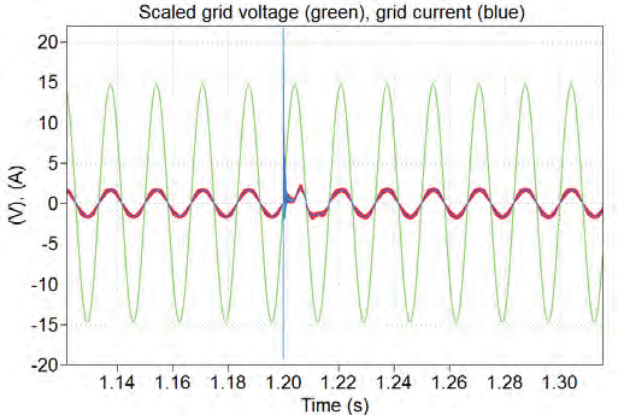


Figure 5.32 – Grid voltage and grid current distortion due to 6 kV ring wave surge

Chapter 6

CONCLUSIONS

The present energy scenario and the prominence of solar energy especially solar photovoltaics were reviewed. The motivating factor for this thesis is to identify and analyze the weak links in existing solar micro inverters. With this knowledge, a more reliable design procedure can be derived and also a testing protocol can be developed. As a result,the life of PV inverters can be increased to match the lifetime of photovoltaic modules.

Different generations of micro inverters employing different power conversion architectures were discussed. The advantages and disadvantages of low frequency and high frequency based micro inverters were reviewed. Basic components of a typical grid connected inverter were discussed in detail starting from connectors to MPPT to power conversion to controllers and filters. Upon carefully analyzing the electrical specifications of the $\sim$250 W commercial micro inverters available in North America, similar electrical specifications were derived. Based on these specifications, a grid connected single phase micro inverter was designed with all the stages mentioned earlier. A different variation of H-bridge inverter was used.

A detailed list of components and their failure modes were identified and FMEA was performed on micro inverters to identify the weak links in the system. A list of five at-risk components was identified by concept of RPN. One of the failure modes was the DC bus capacitor, which is a very important and serious problem. Physics of failures of DC bus capacitor was researched and a degradation model was developed to study the effect of capacitor degradation on the performance of the system. Finally, the grid transient test required for PV micro inverters was researched. The type of surge

waveform based on location and exposure levels was identified. Mathematical models were developed and surge was applied on the system to study its impact. Simulation shows that the micro inverters are capable of operating under these stresses.

REFERENCES

[1] T. Heinrichs. (2013) Sandia R&D Funded under New DOE SunShot Program. [Online]. Available: http://energy.sandia.gov/sandia-rd-funded-under-new-doe-sunshot-program/

[2] Anonymous, "BP energy outlook 2035," [Online; accessed 1-Oct-2015]. [Online]. Available: http://www.bp.com/content/dam/bp/pdf/Energy-economics/energy-outlook-2015/Energy_Outlook_2035_booklet.pdf

[3] International Energy Agency, "World energy outlook special report 2015," [Online; accessed 8-Sep-2015]. [Online]. Available: https://www.iea.org/publications/freepublications/publication/WEO2015SpecialReportonEnergyandClimateChange.pdf

[4] M. Corones, "Solar energy enjoys a glowing outlook," [Online; accessed 10-Sep-2015]. [Online]. Available: http://blogs.reuters.com/data-dive/2015/05/04/solar-energy-enjoys-a-growing-tailwind/

[5] International Energy Agency, "Technology roadmap," [Online; accessed 3-Sep-2015]. [Online]. Available: https://www.iea.org/publications/freepublications/publication/TechnologyRoadmapSolarPhotovoltaicEnergy_2014edition.pdf

[6] P. Grana and M. Shiao, "The microinverter and DC optimizer landscape 2014: The evolution from market niche to market success," *PR Newswire Europe Including UK Disclose*, 2014. [Online]. Available: http://www.greentechmedia.com/research/report/the-microinverter-and-dc-optimizer-landscape-2014

[7] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different dc link configurations," *Power Electronics, IEEE Transactions on*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[8] NREL, "Research cell efficiency records." [Online]. Available: http://www.nrel.gov/ncpv/

[9] M. Munsell. (2014) Who leads the us residential inverter market? [Online]. Available: https://www.greentechmedia.com/articles/read/who-is-leading-the-u.s.-residential-inverter-market

[10] T. Yao, "Maximum-voltage-unit-guided maximum power point tracking for rooftop pv system," Phoenix, AZ, USA, Aug. 2013.

[11] W. Wu, Y. He, T. Tang, and F. Blaabjerg, "A new design method for the passive damped LCL and LLCL filter-based single-phase grid-tied inverter," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 10, pp. 4339–4350, Oct 2013.

[12] "IEEE application guide for IEEE std 1547(tm), IEEE standard for interconnecting distributed resources with electric power systems," *IEEE Std 1547.2-2008*, pp. 1–217, April 2009.

[13] "IEEE recommended practice and requirements for harmonic control in electric power systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, June 2014.

[14] A. Reznik, M. Simoes, A. Al-Durra, and S. Muyeen, "LCL filter design and performance analysis for small wind turbine systems," in *Power Electronics and Machines in Wind Applications (PEMWA), 2012 IEEE*, July 2012, pp. 1–7.

[15] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *Industry Applications, IEEE Transactions on*, vol. 41, no. 5, pp. 1281–1291, Sept 2005.

[16] Anonymous, "Office of energy efficiency and renewable energy." [Online]. Available: http://energy.gov/eere/sunshot/photovoltaics

[17] Y. Xue, K. Divya, G. Griepentrog, M. Liviu, S. Suresh, and M. Manjrekar, "Towards next generation photovoltaic inverters," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, Sept 2011, pp. 2467–2474.

[18] A. Maish, "Defining requirements for improved photovoltaic system reliability," *Progress in Photovoltaics: Research and Applications*, vol. 7, no. 3, pp. 165–173, 1999. [Online]. Available: http://dx.doi.org/10.1002/(SICI)1099-159X(199905/06)7:3⟨165::AID-PIP270⟩3.0.CO;2-S

[19] A. Sastry, S. Kulasekaran, J. Flicker, R. Ayyanar, G. TamizhMani, J. Roy, D. Srinivasan, and I. Tilford, "Failure modes and effect analysis of module level power electronics," in *Photovoltaic Specialists Conference (PVSC),in print, 2015 IEEE 42nd*, June 2015, pp. 1–3.

[20] "IEC Std 60812:2006, Analysis techniques for system reliability - Procedure for failure mode and effects analysis (FMEA)," *IEC Std 60812:2006*, pp. 1–93, 2006.

[21] S. Shrestha, J. Mallineni, K. Yedidi, B. Knisely, S. Tatapudi, J. Kuitche, and G. Tamizhmani, "Determination of dominant failure modes using fmeca on the field deployed c-si modules under hot-dry desert climate," *Photovoltaics, IEEE Journal of*, vol. 5, no. 1, pp. 174–182, Jan 2015.

[22] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *Power Electronics, IEEE Transactions on*, vol. 25, no. 11, pp. 2734–2752, Nov 2010.

[23] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability

driver in power electronics," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, no. 1, pp. 97–114, March 2014.

[24] H. Post, P. Letullier, T. Briolat, R. Humke, R. Schuhmann, K. Saarinen, W. Werner, Y. Ousten, G. Lekens, A. Dehbi, and W. Wondrak, "Failure mechanisms and qualification testing of passive components," *Microelectronics Reliability*, vol. 45, no. 911, pp. 1626 – 1632, 2005, proceedings of the 16th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271405002386

[25] L. Xiaoyu, S. Jiang, W. Yun, and Z. Chenhui, "Research on failure modes and mechanisms of integrated circuits," in *Prognostics and System Health Management Conference (PHM-Shenzhen), 2011*, May 2011, pp. 1–3.

[26] A. Golnas, "PV system reliability: An operator perspective," *IEEE Journal of Photovoltaics*, vol. 3, no. 1, pp. 416–421, Jan 2013.

[27] J. Flicker, R. Kaplar, M. Marinella, and J. Granata, "Pv inverter performance and reliability: What is the role of the bus capacitor?" in *Photovoltaic Specialists Conference (PVSC), Volume 2, 2012 IEEE 38th*, June 2012, pp. 1–3.

[28] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters-an overview," *Industry Applications, IEEE Transactions on*, vol. 50, no. 5, pp. 3569–3578, Sept 2014.

[29] J. Flicker, "Capacitor reliability in photovoltaic inverters," Aug 2013.

[30] Anonymous, "Technical guide of aluminium electrolytic capacitors," Panasonic, Tech. Rep., April 2013. [Online]. Available: http://industrial.panasonic.com/lecs/jp/i/29880/TAL_E/TAL_E.pdf

[31] M. Makdessi, A. Sari, and P. Venet, "Metallized polymer film capacitors ageing law based on capacitance degradation," *Microelectronics Reliability*, vol. 54, no. 910, pp. 1823 – 1827, 2014, sI: {ESREF} 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271414002996

[32] L. Fuchang, D. Xin, L. Jin, Y. Zonggan, and W. Nanyan, "On the failure mechanism of metallized polypropylene pulse capacitors," in *Electrical Insulation and Dielectric Phenomena, 2000 Annual Report Conference on*, vol. 2, 2000, pp. 592–595 vol.2.

[33] J. Flicker, R. Kaplar, M. Marinella, and J. Granata, "Lifetime testing of metallized thin film capacitors for inverter applications," in *Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th*, June 2013, pp. 3340–3342.

[34] Z. Li, H. Li, F. Lin, Y. Chen, D. Liu, B. Wang, H. Li, and Q. Zhang, "Lifetime investigation and prediction of metallized polypropylene film capacitors," *Microelectronics Reliability*, vol. 53, no. 12, pp. 1962 – 1967, 2013. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271413001571

[35] D. Astigarraga, F. Arizti, F. Martin Ibanez, and A. Galarza, "Online indirect measurement of esr and capacity for phm of capacitors," in *Control and Modeling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on*, June 2014, pp. 1–6.

[36] Panasonic, "Metallized polypropylene film capacitors/ezpe datasheet," [Online; accessed 31-July-2015]. [Online]. Available: http://industrial.panasonic.com/lecs/www-data/pdf/ABD0000/ABD0000CE64.pdf

[37] R. Ayyanar, "Course notes for renewable electric energy system spring 2014," Arizona State University, Tempe.

[38] United Chemi-Con Inc, "U36D Series Engineering bulletin," [Online; accessed 27-Sep-2015]. [Online]. Available: http://media.digikey.com/pdf/Data%20Sheets/United%20Chemi-Con%20PDFs/U36D%20Series.pdf

[39] S. Venkataramanan, R. Ayyanar, G. Maracas, G. TamizhMani, M. Marinella, and J. Granata, "Gap analysis towards a design qualification standard development for grid-connected photovoltaic inverters," in *Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE*, June 2011, pp. 003 744–003 749.

[40] "IEEE Recommended Practice on Surge Testing for Equipment Connected to Low-Voltage (1000 V and Less) AC Power Circuits," *IEEE Std C62.45-2002 (Revision of IEEE Std C62.45-1992)*, pp. 1–85, 2003.

[41] "Electromagnetic compatibility (EMC) Part 4-4: Testing and measurement techniques Electrical fast transient/burst immunity test," *IEC Std 61000-4-4*, pp. 1–92, 2012.

[42] "Electromagnetic compatibility (EMC) Part 4-5: Testing and measurement techniques Surge immunity test," *IEC Std 61000-4-5*, pp. 1–160, 2014.

[43] A. Boyd, B. Chancy, D. Phillips, J. Powell, and D. Uselton, "Application of surge and ring test in qualifying solar pv inverters," Lennox Industries Inc, Tech. Rep., 2014. [Online]. Available: http://www.nrel.gov/pv/pdfs/2014_pvmrw_36_uselton.pdf

[44] "IEEE Guide on the Surge Environment in Low-Voltage (1000 V and less) AC Power Circuits," *IEEE Std C62.41.1-2002*, pp. 1–162, 2003.

[45] P. Richman, "Criteria and designs for surge couplers and back-filters," in *Electromagnetic Compatibility, 1989., IEEE 1989 National Symposium on*, May 1989, pp. 202–207.

[46] Vaisala, "National lightning detection network." [Online]. Available: http://www.vaisala.com/en/energy/Weather-Measurement/Lightning-Networks-and-Data/Pages/NLDN.aspx

[47] EPCOS, "SIOV metal oxide varistors application notes." [Online]. Available: http://de.tdk.eu/blob/185762/download/3/siov-applications.pdf

[48] S. B. Alampoondi Venkataramanan, "Gap analysis towards a design qualification standard development for grid-connected photovoltaic inverters," 2011, MS dissertation, Arizona State University.